



INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI
SHORT ABSTRACT OF THESIS

Name of the Student : Mriganka Biswas
Roll Number : 146102032
Programme of Study : Ph.D.
Thesis Title : DC-DC Converters with High Step-up/Step-down Conversion Ratio and Reduced Voltage Stress
Name of Thesis Supervisor(s) : Prof Somanath Majhi and Prof Harshal B. Nemade
Thesis Submitted to the Department/ Center : Electronics and Electrical Engineering
Date of completion of Thesis Viva-Voce Exam : 14/07/2021
Key words for description of Thesis Work : DC-DC Converter, Step-up Converter, Step-down Converter, Coupled Inductor, Current Ripple, Voltage Ripple, Voltage Stress, Efficiency

SHORT ABSTRACT

The thesis presents the design and implementation of DC-DC converters with improved step-up/step-down conversion ratio and reduced voltage stress. Firstly, a high step-down buck converter (HSDBuC) is proposed to produce a lower output voltage at a sufficiently higher duty ratio compared to the conventional buck converter (CBuC). The step-down voltage conversion ratio is modified by a series-parallel transition of two identical capacitors of a switch-capacitor cell. The cell consists of two parallel switches and two cross-connected identical capacitors. These identical capacitors are charged in series and discharged in parallel by producing a lower output voltage compared to CBuC at the same duty ratio. The modified voltage conversion ratio reduces the ripples in inductor currents and output voltage. The proposed HSDBuC utilizes a dual winding coupled inductor to further reduce the ripples in inductor currents and output voltage. The voltage and current stresses of the semiconductor devices employed in HSDBuC are less.

The switch-capacitor cell utilized to modify the voltage conversion ratio of HSDBuC is also used to improve the step-down conversion ratio of the conventional interleaved buck converter (CIBuC). The modified voltage conversion ratio helps to reduce the voltage and current stresses of the semiconductor devices of the proposed high step-down interleaved buck converter (HSDIBuC). The two single inductors at the output end of the HSDIBuC are replaced by a dual-winding coupled inductor (DWCI) to further improve the ripples in inductor currents and achieve a lower value of the output filter capacitor. A systematic step-by-step analysis is performed for different cases of operations to investigate the effect of the coupling factor of DWCI in the reduction of

ripple and the size of the output filter capacitor of the high step-down interleaved buck converter with a dual-winding coupled inductor (HSDIBuC-DWCI).

Subsequently, the voltage conversion ratio of the conventional boost converter (CBoC) as well as conventional interleaved boost converter (CIBoC) is enhanced using a diode-capacitor cell. The proposed high step-up boost converter (HSUBoC) reduces the ripples in input current, inductor current and output voltage with the help of DWCI. Thereafter, the diode-capacitor cell is used to modify the voltage conversion ratio of CIBoC. The voltage stresses of the proposed high step-up interleaved boost converter (HSUIBoC) are less than the output voltage.

All the analyses and the subsequent design procedures of the proposed HSDBuC, HSDIBuC, HSDIBuC-DWCI, HSUBoC and HSUIBoC are accomplished in continuous conduction mode (CCM). In the voltage-mode control (VMC) framework, suitable controllers for each of these converters are designed to investigate the sensitivity to the load parameter variation and the performance under varying reference output voltage. Finally, the proposed converters are implemented in hardware and their performances are verified experimentally.

