



**INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI
SHORT ABSTRACT OF THESIS**

Name of the Student : PIYOOSH P
Roll Number : 146101001
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Name of Thesis Supervisor(s) : Dr. Arnab Sarkar, Dr. Santosh Biswas
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SHORT ABSTRACT

Nowadays, safety-critical embedded systems are increasingly being implemented on computing platforms which involve complex microarchitectural designs with multi-million gates per chip and small feature sizes, to meet the computation and performance demands of the applications. Although, such intricate sophistication is inevitable, they come with associated side-effects such as, high energy dissipation and increase in the probability of faults. In addition, a significant class of contemporary embedded systems are driven by limited energy sources like batteries. On the other hand, there is an increasing trend in many futuristic safety-critical systems to be shipped with quantifiable measures of system reliability. Increased reliability/tolerance against faults are typically achieved through additional hardware resources and/or by utilizing residual system capacity. Similarly, execution slowdown and switching parts of the system into inactive low-power states, are two commonly used system level strategies towards enhancing energy efficiency. Therefore, energy-awareness and fault tolerance have emerged as critically important design constraints in the development of modern safety-critical systems. In this dissertation, we present a few novel scheduling and modeling strategies for safety-critical systems which aim to achieve one of the following objectives: 1) energy minimization, 2) fault tolerance, 3) fault tolerance with energy-awareness, and 4) low-overhead fault detection. All the presented works have been validated through extensive simulation based experiments using synthetically generated workloads as well as real world benchmarks. The obtained results have demonstrated the versatility and efficacy of the proposed approaches.