Fabrication of CoPc and PTCDI-Ph based low-operating voltage organic field-effect transistors

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By

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Dedicated to

..... My Beloved Parents

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Statement

I hereby declare that this thesis entitled "***Fabrication of CoPc and PTCDI-Ph based low-operating voltage organic field-effect transistors***" is the outcome of research work carried out by me under the supervision of Dr. Dipak Kumar Goswami, Associate Professor, at the Department of Physics, Indian Institute of Technology Guwahati, India.

In keeping with the general practice of reporting scientific observations, due acknowledgement has been made whenever work described here has been based on the findings of other investigators.

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CERTIFICATE

This is to certify that the thesis entitled "Fabrication of CoPc and PTCDI-Ph based low operating voltage organic field-effect transistors" which is being submitted by Murali Gedda in partial fulfillment of the degree of Doctor of Philosophy in Science (Physics) of Indian Institute of Technology Guwahati, Guwahati is a record of his own research work carried out by him. He has carried out his investigations for the last four years on the subject matter of the thesis under my guidance at Indian Institute of Technology Guwahati, Guwahati. The matter embodied in the thesis has not been submitted for the award of any other degree by him or by anybody else.

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TH-1322_10612101

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TH-1322_10612101

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TH-1322_10612101

Table of Contents

Synopsis i

Chapter I: Introduction 1

1.1 Organic Semiconductors 1
1.2 Organic Semiconducting Molecule 3
1.2.1 Metal Phthalocyanines (MPcs) 3
1.2.2 Perylene Derivatives 4
1.3 Growth of Organic Thin-Film 5
1.3.1 Study of Rough Surface 6
1.4 Organic Field-Effect Transistors 8
1.5 Basic Design and Operation of OFETs 8
1.6 Hysteresis Effect in OFETs 13
1.7 Gate Dielectric Layer 16
1.8 References 17

Chapter II: Experimental Techniques 23

2.1 Film Deposition Techniques 24
2.1.1 Developed Deposition Systems 24
2.1.2 Standard Techniques 26
2.2 Microscopic Characterization Techniques 27
2.2.1 Atomic Force Microscopy 27
2.2.2 Electron Microscopy 32
2.3 Spectroscopic Characterization Techniques 37
2.3.1 Ultra-Violet Visible Spectroscopy 37
2.3.2 Fourier Transform Infra-Red Spectroscopy 38
2.3.3 X-Ray Diffraction Technique 39
2.4 Electrical Characterization Techniques 41

TH-1322_10612101

2.4.1 Probe Station 41
2.4.2 Semiconductor Characterization System 41
2.5 References 42

Chapter III: Kinetic Roughening in CoPc Thin Film Growth 45

3.1 Introduction 45
3.2 Experimental Details 47
3.3 Results and Discussions 47
3.3.1 Coverage Dependent Growth of CoPc Thin Films 47
3.3.2 Temperature Dependent Growth of CoPc Thin Films 52
3.3.3 Growth of CoPc on Mica (001) Substrate 56
3.4 Conclusions 59
3.5 References 59

Chapter IV: CoPc microstructures based OFETs with higher carrier mobility 63

4.1 Introduction 63
4.2 Experimental Details 65
4.2.1 Growth of CoPc Microstructures 65
4.2.2 Fabrication Process of CoPc Wires Based OFETs 66
4.3 Results and Discussions 67
4.3.1 CoPc Microstructure Growth on Various Substrates 67
4.3.2 CoPc Micro-Wires Based OFET Fabrication 75
4.4 Summary & Conclusions 79
4.5 References 79

Chapter V: Effect of growth temperature on the Performance of PTCDI-Ph OFETs 85

5.1 Introduction 85
5.2 Experimental Details 87

TH-1322_10612101

5.2.1 PTCDI-Ph Based OFET Fabrication on SiO_2 Substrate..... 87
5.2.2 OFET Fabrication on Organic Inorganic Dielectric Surface..... 88
5.3 Results and Discussions..... 90
5.3.1 Evolution of Surface Morphology..... 90
5.3.2 Electrical Characterizations..... 93
5.3.3 Film Morphology and Device Properties..... 97
5.4 Summary & Conclusions..... 102
5.5 References..... 102

Chapter VI: PTCDI-Ph Based Low–Operating Voltage OFETs with Metal – Oxide Gate Dielectrics 109

6.1 Introduction..... 109
6.2 Experimental Details..... 111
6.2.1 Synthesis of Metal-Oxide Precursor Sols..... 111
6.2.2 OFET Fabrication 112
6.3 Results and Discussions..... 114
6.3.1 Fabrication of OFETs using TiO_x /Al_2O_3 as bilayer gate dielectric.....114
6.3.2 OFETs based on $BaTiO_x$/ Al_2O_3 as dielectric layer..... 117
6.3.3 OFETs based on $SrTiO_x$/ Al_2O_3 as dielectric layer..... 118
6.3.4 OFETs based on $BaSrTiO_x$ / Al_2O_3 as dielectric layer..... 121
6.4 Summary & Conclusions..... 123
6.5 References..... 124

Chapter VII: Stability of Low-Operating Voltage OFETs based on PTCDI-Ph.....131

7.1 Introduction.....131
7.2 Experimental Details.....132
7.3 Results and Discussions.....132
7.3.1 Hysteresis in Transistor Output & Transfer Currents.....134
7.3.2 Reliability of Organic Field Effect Transistors.....136

TH-1322_10612101

7.3.3 Bias – Stress Effect on Transistors.....137
7.3.4 Stability after periodic application of bias-stress.....139
7.4 Summary and Conclusions.....140
7.5 References.....141

Chapter VIII: Summary and Conclusions.....143

List of Publications.....149

Conference Presentations.....151

Work Shops Attended.....152

TH-1322_10612101

Synopsis

Organic field-effect transistors (OFETs) based on organic semiconductors have attracted much interest as possible inexpensive and flexible alternatives to inorganic devices [1-3]. Despite considerable improvement in device properties, a better understanding of the growth of the active channel and the control over the growth can significantly enhance the charge transport through the device and reduce the operating voltage. This is crucial to further development of these organic devices [4-6]. In general, an accumulation layer is formed at the interface of organic active channel and dielectric layer due to applied gate voltage. As a result, charge carriers are accumulated within the few monolayers in the region very close to the interface [7, 8]. However, the trap states present in this region capture a portion of the induced carriers. Therefore, only the mobile carriers in the accumulation layer take part to turn on the device [9]. The trap states are usually imperfections associated with the chemical impurities and structural defects, which can be reduced significantly by the controlled growth of channel and the proper selection of the dielectric layer [10-12]. It has been demonstrated that the carrier mobility depends crucially on the morphology of the organic semiconductor channel as well as on the device engineering [13-15]. In this thesis, we outline our findings during the optimization of the growth of organic thin films and wires on different substrates by varying growth parameters and the fabrication of low operating voltage OFETs with enhanced carrier mobility. We have used Cobalt (II) Phthalocyanine (CoPc) and N,N′-diphenyl-3,4,9,10-perylenedicarboximide (PTCDI-Ph) as active channel materials of OFETs. Hybrid gate dielectric materials combining organic-inorganic or inorganic-inorganic materials have been used to improve capacitive coupling between gate and active channel, which also reduce the threshold voltage of the OFETs. We have studied the growth of active channel on top of the dielectric surfaces and optimized the growth for the fabrication of OFETs with better properties. The thesis has been organized in eight chapters: the first two contain the basic aspects concerning materials, different experimental techniques used and the working principles OFETs, while the other six chapters describe the experimental work as elaborated below.

TH-1322_10612101

Chapter I describes the overview of different growth processes and the kinetics of organic thin films and microstructures growth for the fabrication of efficient devices. The basic principles of OFET operation and properties related to charge transport in organic semiconductor are discussed. The roles of the morphology of the active channel and interfaces properties on the device parameters are elaborated. Brief description of the statistical characterization method of rough surfaces is discussed. This method has been extensively used to understand the growth mechanism.

Chapter II reviews the basic working principles and operations of some of the experimental techniques extensively used in this thesis. The development of experimental facilities to grow dielectric layer using anodization technique has also been reported. A custom designed thermal evaporation chamber that works with the principle of molecular beam epitaxy (MBE) for growing organic thin films was setup. Details of the growth chamber have been reported.

Chapter III includes the study of growth of CoPc thin films on SiO_2 and mica (001) ($KAl_2(AlSi_3)O_{10}(OH)_2$,$^2M_1$-muscovite**)** surfaces using thermal evaporation technique and their characterization. CoPc molecule is a p-type semiconductor and it is an interesting representative of metallophthalocyanines (MPc). This material has been emerging as an important class of advanced functional materials in molecular electronics and OFETs fabrication because of its high thermal and chemical stability. This molecule is also used as a material for the fabrication of OFETs based gas sensors [16]. In order to study the effect of surface structures on the growth, we have selected SiO_2 surfaces, which are amorphous in nature, and cleaved mica as a surface with atomically flat reconstructed surfaces. Mica can be cleaved very easily to form an atomically clean mica (001) surfaces in ambient condition. Both the surfaces were used to grow CoPc thin films. In order to study the dynamics of the thin film growth, we have analyzed the evolution of surface fluctuation by calculating height-height correlation function as the films grow with coverage and determined different scaling exponents such as roughness exponents, α, growth exponent, W and dynamic exponent, 1/z. We have observed the power law behavior of the interface width, $W(t)$ as $W(t) \sim t^{\beta}$ with α =0.38 ± 0.05 and in-plane correlation length $\xi(t)$ as $\xi(t) \sim t^{1/z}$, with 1/z = 0.23±0.06. The observed roughness exponent is α = 0.81 ± 0.05. No theoretical models reported so far

TH-1322_10612101

supporting the observed exponents in the growth of CoPc film on SiO_2 substrates. Therefore, the growth mechanism appears to belong to a different universality class. To study the kinetics of the growth, we have varied the substrate temperature from 25 to 220 °C during growth and monitor how diffusion of the molecules on the substrates affects the morphology. With the increased temperature, both interface width, W and in-plane correlation length, ξ. increases closely following an Arrhenius behavior as $W, \xi \sim \exp(-E_a / k_B T)$ with an activation energy E_a= 0.35±0.02 eV which represents the molecular translational and rotational barrier on the surfaces [17, 18]. In order to study the effect of substrate surface on the diffusion, we have grown the same molecule on mica (001) surfaces which is atomically clean. We have observed the growth of long strips as the temperature increases. The observed roughness exponent is α = 0.89 ± 0.07, which is very close to the value obtained in case of SiO_2 surfaces. However, observed activation energy along the length and width of the molecular strip are 0.07 eV and 0.17 eV, respectively. This explains the formation of long strips due to lower diffusion activation energy along the length of the strips.

Chapter IV presents the growth of CoPc wires on different substrates like SiO_2, mica, glass, metal coated glasses and nanoparticle templates at various substrate temperatures using physical vapor deposition technique. The electron transport through the active channel not only depends on the mobile carrier density at the accumulation region but also depends the crystalline quality of the channel such that electron transport through hopping improves. CoPc films grown on SiO_2 and mica surfaces showed the formation of mounds with lots of defects. As a result, these films were not suitable to fabricate high performance devices. Nevertheless, the reported carrier mobility of CoPc thin film based OFETs are very poor (~10^{-4} cm^2/Vs) [16]. In order to grow better crystalline CoPc channel, we have used physical vapor deposition technique to grow CoPc molecular wires. Glass, SiO_2 and mica surfaces were also used to grow CoPc wires. However, we have observed CoPc wires of about 50 μm long on SiO_2 surfaces for 20 min growth time. These wires are single crystal in nature as confirmed by x-ray diffraction (XRD) technique. We have fabricated CoPc molecular wires based OFETs exploiting the design of the devices using bi-layer dielectric materials. Though the crystallinity improves significantly in case of wires, however, at the same time, the use of organic-inorganic hybrid dielectric improved the capacitive coupling between gate and active

TH-1322_10612101

channel. As a result, carrier mobility improved in these devices. We have used poly(vinyl-alcohol) (PVP) /Al_2O_3 system as hybrid dielectric for the fabrication of CoPc wires based OFETs. Al_2O_3 layers were grown using anodization of Al films [19-21]. Better capacitive coupling is achieved with CoPc wires due to the lower surface free energy of PVA (~ 0.045 J/m^2) than Al_2O_3 (~ 1.7 J/m^2). Optimizations of individual layer thicknesses are carried out in order to obtain lower leakage current and higher capacitances. We have observed significant enhancement of carrier mobility to 1.11 ± 0.20 cm^2/Vs with threshold voltage − 7.8 V and on/off ratio ~10^4. The structural and morphological characterizations were carried out by means of FESEM, XRD and TEM. The fabrication of CoPc wires based OFETs using hybrid dielectric layer is reported. The carrier mobility obtained from these OFETs is 1.11 cm^2/Vs. The reported operating voltage for CoPc based transistors is about 100V. However, we have achieved the operating voltage to 20 V.

Chapter V describes the growth of PTCDI-Ph (*n*-type semiconductors) films on SiO_2 and polymer dielectric surfaces. Fabrication and characterization of OFETs based on PTCDI-Ph films on SiO_2 and hybrid dielectric layer are described. We have explored the effect of substrate temperature on the growth of active channel and the performance of the OFETs. In general, the organic dielectric materials make better capacitive coupling between the gate and the active channel [22-27]. Organic nature of interface between active channel and dielectric layer may provide a more efficient capacitive coupling with the channel, perhaps because of better matching in surface energy of these materials [19, 25]. Therefore, we have considered using hybrid dielectric in combination of organic and inorganic material as gate dielectric for the fabrication of OFETs. PTCDI-Ph films were used as channel materials for the fabrication of OFETs using various hybrid dielectric materials to optimize the device structures for low voltage operation with enhanced carrier mobility. PTCDI-Ph films were grown on a hybrid dielectric consisting layers of poly (methyl methacrylate) (PMMA) and Al_2O_3. Substrate temperature was varied between 30 and 120 °C during the growth of PTCDI-Ph film on top dielectric film of PMMA surfaces. The evolution of surface morphology with the substrate temperatures was studied from the height-height correlation function calculated from the atomic force microscopy (AFM) images of surface grown at different substrate temperature. We have observed the average roughness exponents (α) of 0.81 ± 0.06, which is close to the

TH-1322_10612101

value obtained for Al_2O_3 and PMMA surfaces and is independent of growth temperatures. The field-effect carrier mobility obtained from the device designed at 90 °C substrate temperature showed the highest value of 0.02 cm^2/Vs. This has been attributed to the formation of smooth and uniform films of PTCDI-Ph on PMMA surfaces and achieved a better capacitive coupling between the active channel and the gate. As a result, mobile carrier density at the accumulation region enhanced. Our results also demonstrate a process design to fabricate OFETs with enhanced carrier mobility.

Chapter VI provides the synthesis of high-*k* metal-oxide gate dielectric sols like TiO_2, $BaTiO_3$, $SrTiO_3$ and $BaSrTiO_3$ for the fabrication of low operating voltage OFETs using PTCDI-Ph films as active channel. Extracted OFETs parameters and their dependency on the dielectric materials are discussed. In order to enhance the performance of the devices further, we have fabricated OFETs using hybrid dielectric materials with higher dielectric constants. Using a novel solution process method, we have synthesized $SrTiO_3$ on anodized Al_2O_3 [28-30]. The thickness of individual layers is optimized to obtain minimum leakage current and higher capacitance. The leakage current density obtained from the $SrTiO_3/Al_2O_3$ was below 10^{-8} A/cm^2 whereas for single layer of $SrTiO_3$alone produces leakage current of 10^{-4} A/cm^2. The band gap of $SrTiO_3$ (E_g = 3.2eV) [31] is relatively low which causes the huge amount of leakage current through $SrTiO_3$ single layer and it is controlled due to the blocking of electron conduction path by the highly stable Al_2O_3 layer with large band gap (E_g= 6–9 eV) [32-34]. As a result, carrier field-effect mobility enhanced due to increased mobile carrier density at the accumulation region. At the same time, the operating voltage also decreases. Due to the high capacitance of $SrTiO_3$(30 nm)/Al_2O_3 (10 nm) system, we have achieved operating voltages of the OFETs as low as 4 V. The effective capacitance measured from this system is about 65.4 nF/cm^2 which is relatively higher than SiO_2 (300nm)/Si system (~11.5 nF/cm^2). The extracted carrier mobility is 0.04 cm^2/Vs, threshold voltage range is 0.3-0.5 V. In addition to this, we also fabricated low operating voltage OFETs based on hybrid dielectric combining TiO_2, $BaTiO_3$, $BaSrTiO_3$ with Al_2O_3 and fabricated OFETs with operating voltage within 1.5 V and with carrier mobility of 0.02 cm^2/Vs.

Chapter VII presents the stability study using bias stress measurement of the *n*-type (PTCDI-Ph) OFETs fabricated using hybrid dielectric materials reported in the last section.

TH-1322_10612101

Degradation of the devices by monitoring the variation of device parameters during a period five months has been reported. The reliability of the devices as a result of voltage bias stresses and exposed to air for extended time are also discussed. Threshold voltage shifts in organic field effect transistors (OFETs) have been reported frequently [35, 36]. Cyclic sweeps of the gate voltage in OFETs reveal a hysteresis in the transfer characteristics (drain-source current versus gate-source voltage) thereby unfolding an electrical instability of the transistor element. The hysteresis free transistors are desired in integrated organic circuits. All the OFETs fabricated with hybrid dielectric materials showed almost nil hysteresis, which is the signature of better dielectric with less trap states [37, 38]. In order to examine the stability, we have extensively studied the bias stress experiments on the OFETs fabricated with hybrid dielectric of $SrTiO_3/Al_2O_3$. In addition, we have observed reproducible output characteristics without any significant changes in threshold voltage over 150 days.

Chapter VIII presents the summary and important conclusions of the entire work. In addition, highlights of the new findings and results related to growth of organic thin films, the fabrication of efficient OFETs are reported. Open challenges and the different innovative directions for future study of efficient OFET fabrications are addressed.

References

[1] H. Klauk, Organic Electronics, Materials, Manufacturing and Applications, Wiley-VCH, Weinheim, Germany, 2006.

[2] Z. Bao, J. Locklin, Organic Field-Effect Transistors CRC Press, Boca Raton, USA, 2007.

[3] A. Hoppe, T. Balster, T. Muck, V. Wagner, Scaling limits and MHz operation in thiophene-based field-effect transistors, Phys Status Solidi A, 205 (2008) 612-625.

[4] X.G. Zhao, X.W. Zhan, Electron transporting semiconducting polymers in organic electronics, Chem. Soc. Rev., 40 (2011) 3728-3743.

[5] C.D. Dimitrakopoulos, D.J. Mascaro, Organic thin- film transistors: A review of recent advances, IBM J. RES. & DEV., 45 (2001) 11-27.

[6] H. Klauk, Organic thin-film transistors, Chem Soc Rev, 39 (2010) 2643-2666.

[7] V. Coropceanu, J. Cornil, D.A. da Silva, Y. Olivier, R. Silbey, J.L. Bredas, Charge transport in organic semiconductors, Chem. Rev., 107 (2007) 926-952.

TH-1322_10612101

[8] M.E. Gershenson, V. Podzorov, A.F. Morpurgo, Colloquium: Electronic transport in single-crystal organic transistors, Rev. Mod. Phys., 78 (2006) 973-989.

[9] Y.L. Don Park, Jung Ah Lee, Hwa Sung Cho, Kilwon, Interface engineering in organic transistors, Mater. Today, 10 (2007) 46-54.

[10] B. Lee, Y. Chen, D. Fu, H.T. Yi, K. Czelen, H. Najafov, V. Podzorov, Trap healing and ultralow-noise Hall effect at the surface of organic semiconductors, Nat. Mater., 12 (2013) 1125–1129.

[11] C. Risko, J.-L. Brédas, Organic semiconductors: Healing contact, Nat. Mater., 12 (2013) 1084-1085.

[12] M. Pope, C.E. Swenberg, Electronic Processes in Organic Crystals and Polymers Oxford University Press1999.

[13] Y.Y. Lin, D.J. Gundlach, S.F. Nelson, T.N. Jackson, Stacked pentacene layer organic thin-film transistors with improved characteristics, IEEE Electron Device Lett., 18 (1997) 606-608.

[14] D.J. Gundlach, Y.Y. Lin, T.N. Jackson, S.F. Nelson, D.G. Schlom, Pentacene organic thin-film transistors - Molecular ordering and mobility, IEEE Electron Device Lett., 18 (1997) 87-89.

[15] T.W. Kelley, C.D. Frisbie, Gate voltage dependent resistance of a single organic semiconductor grain boundary, J. Phys. Chem. B, 105 (2001) 4538-4540.

[16] R.D. Yang, T. Gredig, C.N. Colesniuc, J. Park, I.K. Schuller, W.C. Trogler, A.C. Kummel, Ultrathin organic transistors for chemical sensing, Appl. Phys. Lett., 90 (2007) 263506 -263503.

[17] F. Biscarini, P. Samori, O. Greco, R. Zamboni, Scaling behavior of anisotropic organic thin films grown in high vacuum, Phys Rev Lett, 78 (1997) 2389-2392.

[18] D. Tsamouras, G. Palasantzas, Temperature dependence of the growth front roughening of oligomer films, Appl. Phys. Lett., 80 (2002) 4528-4530.

[19] L.A. Majewski, R. Schroeder, M. Grell, Flexible high capacitance gate insulators for organic field effect transistors, J. Phys. D: Appl. Phys., 37 (2004) 21-24.

[20] T.W. Hickmott, Interface states at the anodized Al2O3-metal interface, J Appl Phys, 89 (2001) 5502-5508.

TH-1322_10612101

[21] A.F. Hebard, S.A. Ajuria, R.H. Eick, Interface Contribution to the Capacitance of Thin-Film Al-Al2o3-Al Trilayer Structures, Appl Phys Lett, 51 (1987) 1349-1351.

[22] M.J. Panzer, C.R. Newman, C.D. Frisbie, Low-voltage operation of a pentacene field-effect transistor with a polymer electrolyte gate dielectric, Appl. Phys. Lett., 86 (2005) 103503-3.

[23] L.A. Majewski, R. Schroeder, M. Voigt, M. Grell, High performance organic transistors on cheap, commercial substrates, J Phys D Appl Phys, 37 (2004) 3367-3372.

[24] L.A. Majewski, R. Schroeder, M. Grell, One volt organic transistor, Adv. Mater., 17 (2005) 192-196.

[25] S. Kobayashi, T. Nishikawa, T. Takenobu, S. Mori, T. Shimoda, T. Mitani, H. Shimotani, N. Yoshimoto, S. Ogawa, Y. Iwasa, Control of carrier density by self-assembled monolayers in organic field-effect transistors, Nat Mater, 3 (2004) 317-322.

[26] C. Kim, A. Facchetti, T.J. Marks, Polymer gate dielectric surface viscoelasticity modulates pentacene transistor performance, Science, 318 (2007) 76-80.

[27] J. Puigdollers, C. Voz, A. Orpella, R. Quidant, I. Martin, M. Vetter, R. Alcubilla, Pentacene thin-film transistors with polymeric gate dielectric, Org Electron, 5 (2004) 67-71.

[28] F.M. Pontes, E.J.H. Lee, E.R. Leite, E. Longo, J.A. Varela, High dielectric constant of SrTiO3 thin films prepared by chemical process, J Mater Sci, 35 (2000) 4783-4787.

[29] J.P. George, J. Beeckman, W. Woestenborghs, P.F. Smet, W. Bogaerts, K. Neyts, Preferentially oriented BaTiO3 thin films deposited on silicon with thin intermediate buffer layers, Nanoscale Res. Lett., 8 (2013) 1-7.

[30] J. Ihlefeld, B. Laughlin, A. Hunt-Lowery, W. Borland, A. Kingon, J.P. Maria, Copper compatible barium titanate thin films for embedded passives, J Electroceram, 14 (2005) 95-102.

[31] K. van Benthem, C. Elsasser, R.H. French, Bulk electronic structure of SrTiO3: Experiment and theory, J Appl Phys, 90 (2001) 6156-6164.

[32] S. Duenas, H. Castan, H. Garcia, A. de Castro, L. Bailon, K. Kukli, A. Aidla, J. Aarik, H. Mandar, T. Uustare, J. Lu, A. Harsta, Influence of single and double deposition temperatures on the interface quality of atomic layer deposited Al2O3 dielectric thin films on silicon, J. Appl. Phys., 99 (2006) 054902-8.

[33] J. Robertson, High dielectric constant oxides, Eur Phys J-Appl Phys, 28 (2004) 265-291.

TH-1322_10612101

[34] C.K. Lee, E. Cho, H.S. Lee, K.S. Seol, S. Han, Comparative study of electronic structures and dielectric properties of alumina polymorphs by first-principles methods, Phys. Rev. B., 76 (2007) 245110-7.

[35] S.J. Zilker, C. Detcheverry, E. Cantatore, D.M. de Leeuw, Bias stress in organic thin-film transistors and logic gates, Appl. Phys. Lett., 79 (2001) 1124-1126.

[36] H.E. Katz, X.M. Hong, A. Dodabalapur, R. Sarpeshkar, Organic field-effect transistors with polarizable gate insulators, J. Appl. Phys., 91 (2002) 1572-1576.

[37] A. Wang, I. Kymissis, V. Bulovic, A.I. Akinwande, Engineering density of semiconductor-dielectric interface states to modulate threshold voltage in OFETs, Ieee T Electron Dev, 53 (2006) 9-13.

[38] P. Balk, Dielectrics for Field-Effect Technology, Adv Mater, 7 (1995) 703-710.

TH-1322_10612101

Chapter I

Introduction

1.1 Organic Semiconductors

The term organic semiconductors can be defined as a large family of organic materials that exhibit semiconducting properties. We can distinguish two main classes of organic semiconductors: low molecular weight materials (oligomers) and polymers. The common characteristic of both classes is the arrangement of the carbon atoms in a series of alternating single and double bonds, also called conjugation. In a conjugated system, carbon atoms are sp^2-hybridized (the 2*s* orbital is mixed with only two of the three available 2*p* orbitals), this means that only three σ bonds can be formed, leaving the p_z orbital unaltered. The mutual overlap between unhybridized p_z orbitals of adjacent carbons leads to the formation of π bonds.

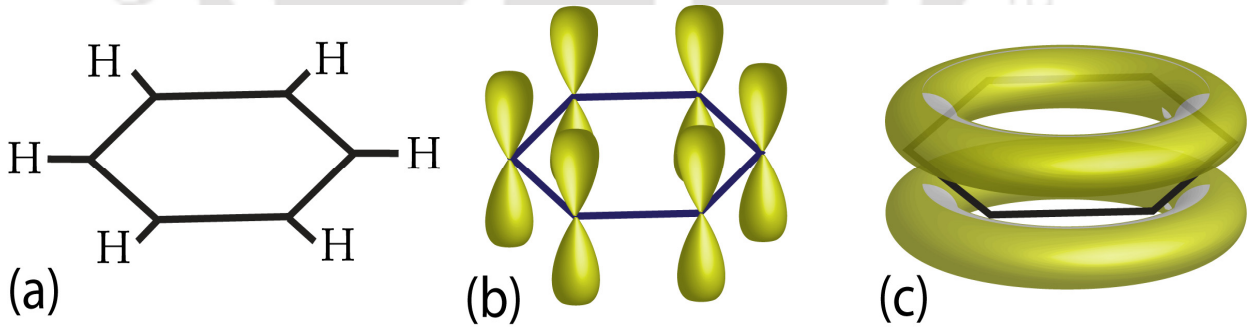

Figure 1.1: (a) σ – bonding framework, **(b)** arrangement of p_z – orbitals and **(c)** the "p_z" orbitals overlap to form the delocalized molecular "π" system of an aromatic molecule.

The electrons of overlapping p_z orbitals form a delocalized electronic orbital over the whole conjugation length (Figure 1.1). These delocalized π orbitals are the origin of the semiconducting properties of this class of materials. While both the σ and the π bonds have covalent nature, when organic molecules meet to form solids they are kept together by weak

TH-1322_10612101

van-der-Waals bonds due to π-π interaction. The consequences of this considerably weak intermolecular interaction between molecules in the organic solids are reflected not only in the mechanical and thermodynamic properties, but also in their electronic properties for charge transfer mechanism through the solid.

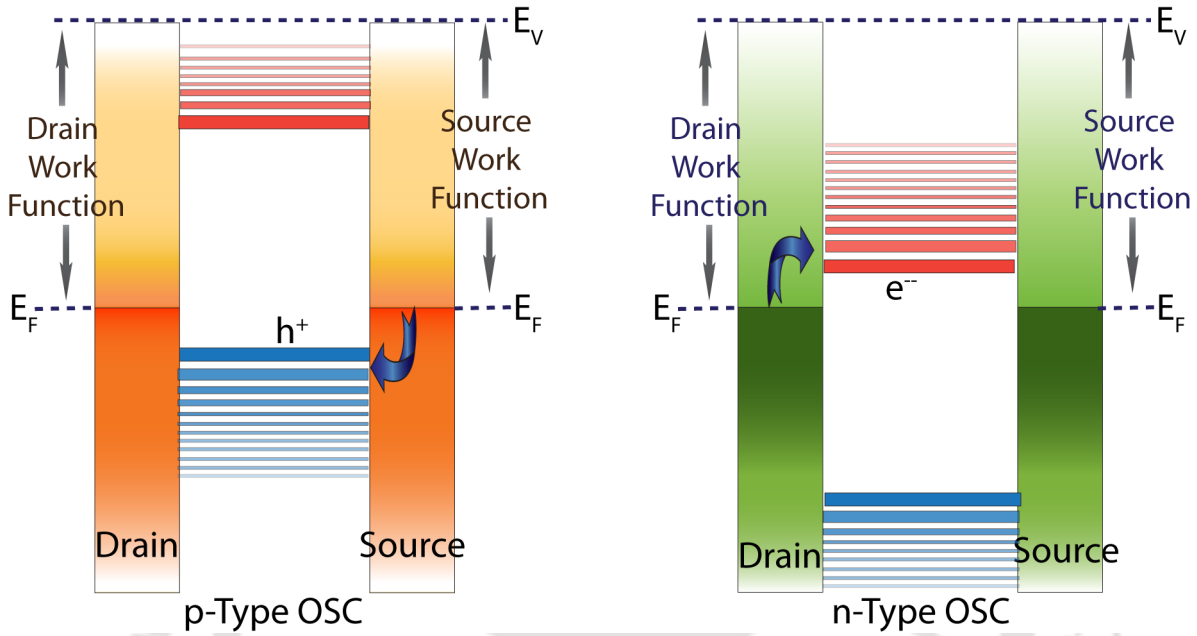

Figure 1.2: Representative energy diagrams to distinguish *p*- & *n*-type organic semiconductors through source – drain electrode band offsets with HOMO & LUMO levels.

The lowest electronic excitation of conjugated molecules is the π-π* transition. This transition leads to the formation of an electron-hole pair by Coulomb force. The energy difference between the π band, which is the highest occupied molecular orbital (HOMO), and the π* band, which is the lowest unoccupied molecular orbital (LUMO), is generally referred to as band gap, which is in the range of 1.5 – 3 eV [1]; thus the π-π* transition is possible, for example, upon light absorption. The unique properties of this class of materials make them attractive alternatives to epitaxially grown purely inorganic layers, especially for application in electronic devices, such as solar cells [2-4], light emitting diodes (LEDs) [5-8] and field-effect transistors (FETs) [9-13]. Depending on the nature of the semiconductors and electrodes used, the active channel formed can be *n*-type, where electrons are the charge carriers, or *p*-type where holes (electron deficient species) function as carriers. The

TH-1322_10612101

representative energy diagrams for both *p*-type and *n*-type organic semiconductors are shown in Figure 1.2.

1.2 Organic Semiconducting Molecules

In the following section, *n*- and *p*-type organic semiconducting molecules utilized in this thesis are presented. They belong to the group of aromatic molecules, a subclass of oligomers, which are characterized by a relatively simple shape consisting of several carbon rings to ensure the planarity of the molecular core. These molecules can be modified by functional end-groups. Their simple shape allows dense packing and facilitates crystallization of these molecules (see Figure 1.3). In addition, aromatic molecules have a high thermal stability making it possible to evaporate them under vacuum what, in turn, guarantees a good control over molecular packing within the films.

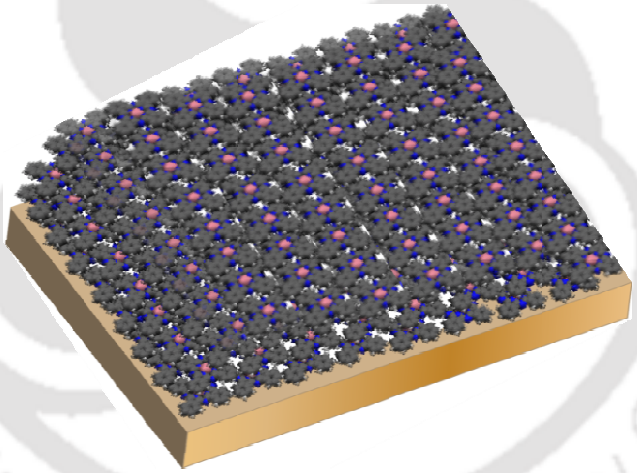

Figure 1.3: Dense molecular packing of organic small molecules on substrate.

1.2.1 MetalPhthalocyanine (MPc)

Cobalt Phthalocyanine

Phthalocyanines are porphyrin derivatives, which recently have attracted enormous interest due to their intense coloring properties associated with their use as blue and green pigments. Since the discovery of their semiconducting properties they are also employed as building blocks for the construction of new molecular materials for electronic and

TH-1322_10612101

optoelectronic applications. These phthalocyanines are planar molecules consisting of four iso–indole subunits linked together through nitrogen atoms. In the following subsections, we focus on one of representatives of the group of metal-phthalocyanines, which are characterized by the presence of a cobalt (Co) atom in the molecular center, (CoPc) ($C_{32}H_{16}N_8Co$). An important aspect of this molecule is that, besides its semiconducting behavior as a *p*-type material, it shows high thermal and chemical stability [14, 15]. From the crystallographic information reported for the bulk CoPc structures, it is known that several poly-morphs exist among α – and the β – configurations are best known [16-18]. Their structural properties are summarized in Table 1.1. α – CoPc is triclinic having one molecule within the unit cell whereas β – CoPc exhibits a monoclinic structure with $Z = 2$, where Z is the number of molecules per unit cell.

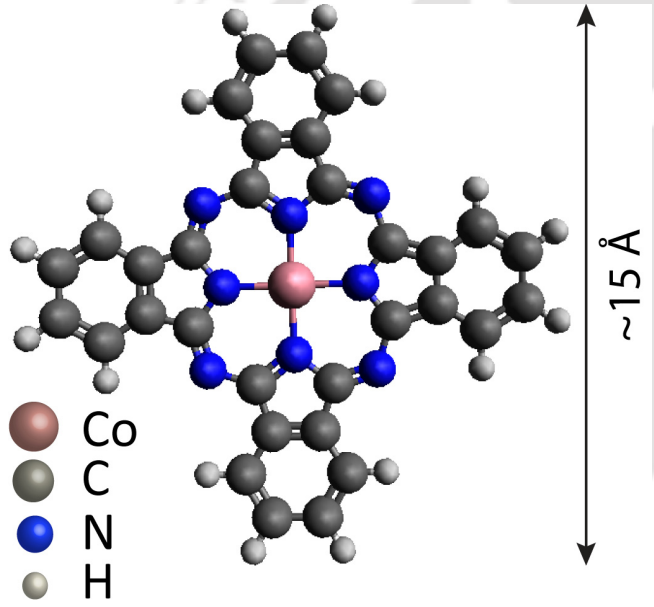

Figure 1.3: CoPc molecular Structure.

	α - CoPc	β - CoPc
a [Å]	12.090	14.5982
b [Å]	3.754	4.7937
c [Å]	12.800	19.4348
α	88.96º	90º
β	90.97º	120.782º
γ	95.09º	90º
Z	1	2

Table 1.1: Unit cell parameters reported for the structure of α-CoPc and β-CoPc [17].

1.2.2 Perylene derivative

N,N'-diphenyl-3,4,9,10-perylene tetra-carboxylic diimides

N,N'-diphenyl-3,4,9,10-perylene tetra-carboxylic diimide (PTCDI-Ph) belongs to the family of perylene bisimide, which were initially applied for industrial purposes as red vat

dyes. Later on, several perylene bisimide compounds were used in industrial applications as pigments due to weather and light-fastness, high thermal stability and insolubility. Recently, these molecules are being used for the fabrication of electronic devices and perylene bisimides are found to be one of the best *n*-type semiconductors available [19-22]. Recently, perylene bisimide derivatives were successfully synthesized showing reasonable charge carrier mobilities in ambient conditions [23, 24]. Among the different perylene bisimide compounds, we have chosen PTCDI-Ph as an *n*-type semiconductor. The molecule (PTCDI-Ph) consists of a planar core with two phenol groups on opposite sides as shown in Figure 1.4. As already mentioned in the motivation, there is a particular demand in *n*-type materials in order to enable the fabrication of organic field effect transistors, organic solar cells, ambipolar transistors and OLEDs in which both *p*- and *n*-type semiconductors are needed. Up to now, there are only few reports on the study of growth of thin films and fabrication of organic field-effect transistors where PTCDI-Ph as active materials. Most of the transistors characterized under vacuum conditions were reported. To ease of utility of such electronic devices under ambient conditions, more studies require to be done for using the molecules for the fabrication of OFETs with efficient performances.

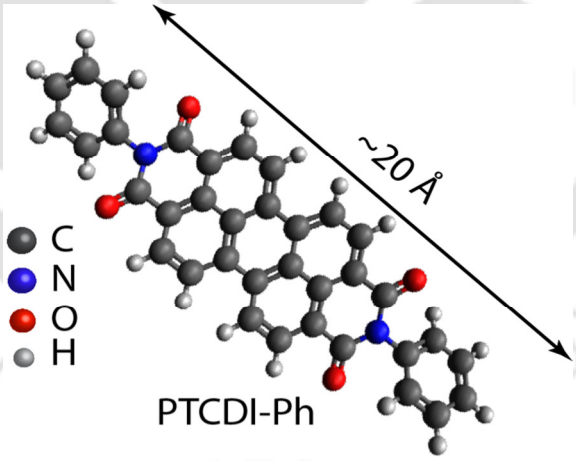

Figure 1.4: Molecular structure of PTCDI-Ph molecule.

1.3 Growth of Organic Thin-Films

The controlled growth of molecular thin films is of considerable importance because they form the basis of a wide range of electronic and optoelectronic devices [25]. The properties of these hetero structures depend strongly on the structural quality of the films and the nature

TH-1322_10612101

of the interface formed between layers of different materials. An atomically flat surface is an idealization rarely encountered in nature. Most surfaces are to some extent rough, making roughness a ubiquitous phenomenon. However, the rough surfaces or interfaces can significantly affect the performance of devices and therefore, it is important to study the evolution of rough surface as the film grows. In the next section, we discussed the methodology to analyze rough surfaces, which is followed in this thesis work.

1.3.1 Study of rough surface

A rough surface can be described by its height fluctuation above a well-defined reference plane, the height function $h(r, t)$, which is a function of substrate position coordinate, r and time, t. A typical height profile is shown in Figure 1.5. The time dependence is relevant only when a growing surface is considered. Only the height is not the most convenient way to describe the surface, usually the height does not follow any well-known function and thus an analytical expression is mostly excluded. For experimental and numerical investigations, however, the height function is often used directly. For most purposes, a more useful measure of the roughness is the root-mean-square (rms) value (often called the interface width (W) in the literature). In order to understand the correlation in height fluctuation, it is convenient to define height-height correlation function $G(r,t)$, which is defined as mean square of height difference between two surface positions separated by a distance r (Note: $G(r, t)$ has been calculated along the AFM scan direction, which is one dimensional. Therefore, in the definition of $G(r, t)$, r is distance between two points along the scan direction only) for the deposition time t as,

$$G(r,t) = \left\langle \left| h(r,t) - h(0,t) \right|^2 \right\rangle \qquad \text{---------- (1.3)}$$

Where $h(r,t)$ and $h(0,t)$ are the heights of the surfaces at the two different locations separated by a distance r. The rms value of the roughness also called the interface width gives the mean deviation from mean height, and is the most commonly used measure for the roughness. The interface width is defined as $W(t) \equiv \sqrt{\left\langle [h(r,t)]^2 \right\rangle}$. The detail description of analysis of rough surface using $G(r)$ is reported in the references [26-29]. The height-height correlation function can be written as;

TH-1322_10612101

$$G(r,t) \sim \begin{cases} 2W^2 & if \ \ r \gg \xi(t), \\ (m(t)r)^{2\alpha} & if \ \ r \ll \xi(t). \end{cases} \qquad \text{---------- (1.4)}$$

where, $\xi(t)$ the characteristic in-plane lateral length scale, α is the roughness scaling exponent and $m(t)$ is the local surface slope of the height profile for small length scale [28, 30].

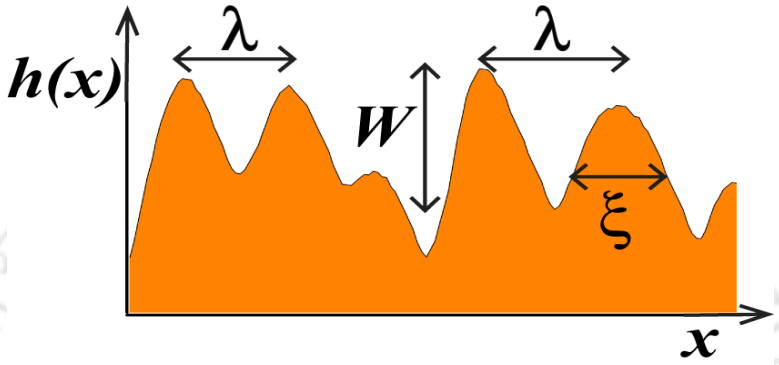

Figure 1.5: Schematic illustration of height profile showing different parameters to describe rough surface.

A typical plot of $G(r,t)$ vs r is shown in the Figure 1.6. $m(t)$ was calculated from the fitting of linear portion of log-log plot of $G(r,t)$ vs r as per the equation mentioned earlier. Lateral correlation length, $\xi(t)$ is the measure of the length beyond which surface heights are not significantly correlated. For the surfaces with island formation, this length essentially measures the size of the island [31]. Other parameter to characterize the surface, the wavelength (λ), on the other hand, signifies the average separation between islands. λ and ξ must satisfy the relation $\xi \leq \lambda$ as the islands are separated by at least their size. However, when the islands grow next to each other would imply that $\xi = \lambda$ [32]. The physical meanings of these parameters are described in Figure 1.5. W (shown by arrow marked in Figure 1.6) is the value of $G^{1/2}(r,\ t)$ at the first local maximum, as $W \sim G^{1/2}(\xi/2)$ where ξ, marked by an upward arrow, is the position of r at the first local minimum of $G^{1/2}(r)$ as shown in Figure 1.6 [33]. This definition of roughness amplitude is preferred over the large r limit of $G(r)$ because artifacts at large length scales can affect experimental data. In order to study the dynamics of the growth process, it is important to study the behavior of local slope $m(t)$. If $m(t)$ is independent of the growth time (i.e., $m(t)$ is independent of time t), then it is said to be

TH-1322_10612101

stationary growth. On the other hand, for non stationary growth *m(t)* increases with time and a up-shift in *G(r)* is observed.

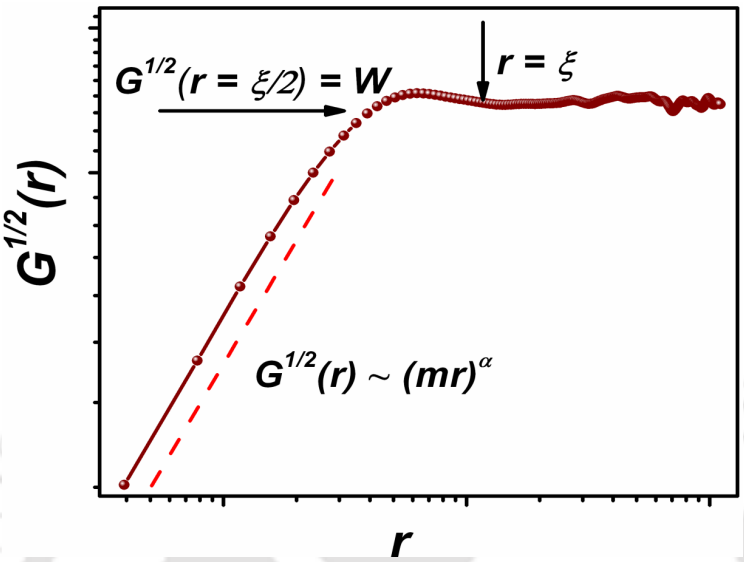

Figure 1.6: Representative height-height correlation function $G(r,t)$ vs r plot showing the different parameters describing rough surfaces.

1.4 Organic field-effect transistors

It was 1962, when the first thin-film transistor (TFT) was reported by *Paul K. Weimer* based on inorganic semiconductors [34]. Si, Ge etc. are undoubtedly the materials for modern microelectronic industry for TFT based electronics. However, during last few decades, organic semiconductors material based organic field-effect transistors (OFETs) have progressed significantly and showed promises to be competitive candidate for replacing some of the applications based on inorganic semiconductors [35, 36]. Though, enormous progresses have been made, there are several issues on the fabrication and operation of the devices are essential to study in order to achieve high performance of OFETs. In this section, we summarize the basic design of OFETs and general methodologies of the device characterization.

1.5 Basic design and operation of OFETs

An OFET is a three terminal device, where one electrode (the gate) is separated from the other two electrodes (the source and the drain) by an insulating layer (the dielectric). The

TH-1322_10612101

source and the drain electrodes are connected via an organic (*n*- or *p*-type) semiconductor with a defined geometry, the channel width *W* and the channel length *L*. The layers of the OFET are usually very thin to fabricate a stable freestanding device; therefore OFETs are built on a substrate (*e.g.* glass, Si wafer or plastic foil). Depending on the layer deposition sequence, four different types of OFET structures can be realized, as illustrated in Figure 1.7.

Current flows from the source electrode (*S*) to the drain electrode (*D*), upon applying a voltage between *S* and *D* (V_{DS}). This current flow is controlled by a voltage applied to a third electrode (gate). A small gate voltage (V_{GS}) induces charges at the interface between the dielectric and the semiconductor. The layer of accumulated charges at the semiconductor-dielectric interface is called channel. This channel enables current flow between source and drain (I_{DS}). The conductive channel is formed in the few nm thin layers at the semiconductor/dielectric interface [10, 37, 38].

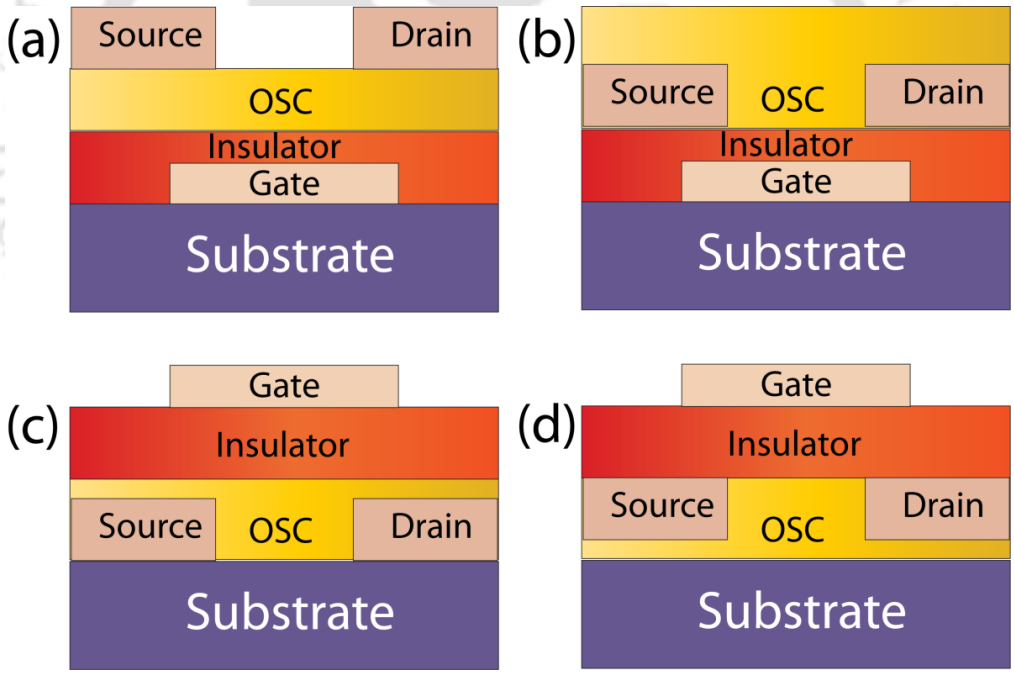

Figure 1.7: Schematic representation of different OFET configurations, **(a)** Top contact-bottom gate; **(b)** Bottom contact-bottom gate; **(c)** Bottom contact-top gate; **(d)** Top contact-top gate.

The transferred characteristics (I_{DS} versus V_{GS} at constant V_{DS}) and the output characteristics (I_{DS} versus V_{DS} at constant V_{GS}) of the devices are measured in order to

TH-1322_10612101

quantify the performance of the devices. The typical characteristics curves obtain from OFETs are shown in Figure 1.8. In output characteristics (see Figure 1.8a) V_{DS} is swept while a constant V_{GS} is applied. If a positive V_{GS} is applied to an *n*-type OFET, I_{DS} will increase linearly as V_{DS} increases from 0 V to a positive voltage. When V_{DS} is as large as V_{GS}, the field at the drain electrode is reduced to 0 and the channel is "pinches off". As a result, I_{DS} saturates. The maximum I_{DS} is therefore defined by V_{GS}.

To measure transfer characteristics V_{GS} is swept while a constant V_{DS} is applied (as shown in Figure 1.8(b)). The transfer characteristics can be measured in the linear region for lower V_{DS} and in the saturation regime for higher V_{DS}.

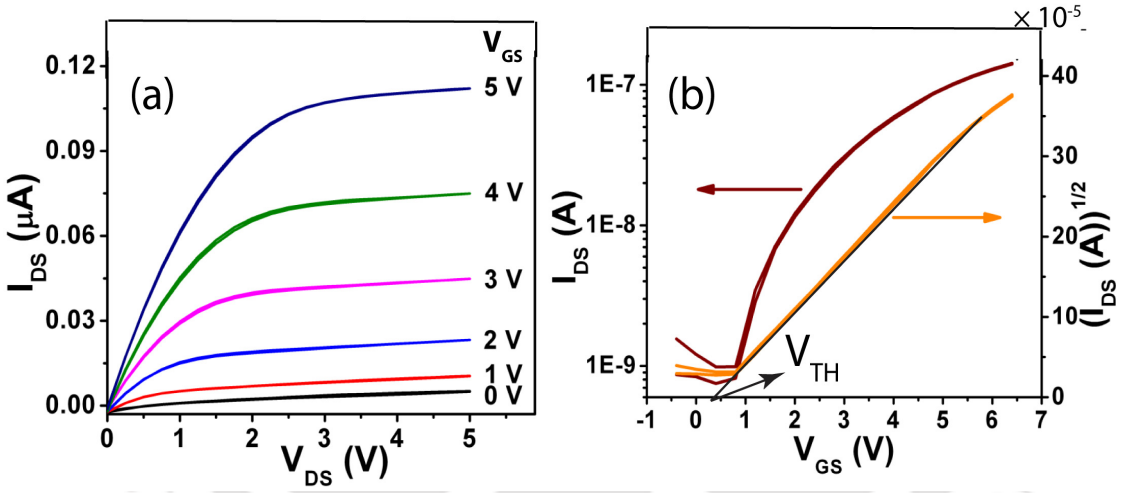

Figure 1.8: Typical **(a)** Output and **(b)** Transfer characteristics of *n*-type (PTCDI-Ph) based OFETs.

In order to quantify the performance of OFETs, a simple model of field-effect transistors describing I_{DS} in the linear regime can be used as follows [39]:

$$I_{DS,lin} = \frac{W}{L}\mu_{lin}C_i(V_{GS} - V_{th} - \frac{V_{DS}}{2})V_{DS} \qquad \text{---------- (1.5)}$$

And I_{DS} in the saturation regime as:

$$I_{DS,sat} = \frac{W}{2L}\mu_{sat}C_i(V_{GS} - V_{th})^2 \qquad \text{---------- (1.6)}$$

TH-1322_10612101

$$C_i = \frac{k\varepsilon_0 A}{d} \qquad \text{---------- (1.7)}$$

These two equations are valid under the assumptions, that *(i)* the field along the channel is much lower than across it (gradual channel approximation) and *(ii)* that the mobility is constant [38]. W and L are the channel width and length, respectively. Here, μ (i.e. μ_{lin} *and* μ_{sat}) is the field-effect mobility in two regions for the majority charge carriers, C_i is the geometric capacitance of the dielectric and V_{th} is the threshold voltage, which will be explained later. k is the dielectric constant of the insulator. The charge carrier mobility is calculated in either the saturation or in the linear regime from the above equations. The differential $\partial I_{DS}/\partial V_{GS}$ is called the transconductance. In an ideal device, the mobility calculated in the linear and saturation regime are the same and the mobility depends on the charge carrier density at the active channel, which is can be influenced by the applied V_{GS}. The above equations indicate that increasing either V_{GS} or V_{DS} can increase the current between the source and drain. Nonetheless, these two parameters can be increased to only a certain extent. As is also evident in eqs 1.5 and 1.6, another viable approach to minimize V_{GS} and/or increasing the electrical current is by adjusting the capacitance of the gate dielectric, C_i. As described in eq1.7, the capacitance depends linearly on dielectric constant, k and inversely on thickness of the layer, d. It is to be noted that typically in an efficient device, the ratio of d to channel lengths L, $d/L \leq 0.1$ is necessary to ensure that the field created by V_{GS}, and not the lateral field V_{DS}, determines the charge distribution within the channel [40]. Several groups have adopted the approach of reducing dielectric thickness to realize low-voltage operation in OFETs. For example, *Vuillaume et al.* employed an organic monolayer of carboxyl-terminated alkyl trichlorosilanes (thickness range 1.9-2.6 nm) with linear end groups for the gate dielectric to achieve working voltages below 2 V [41]. *Halik et. al.* demonstrated low-voltage organic transistors using self assembled mono-layers (SAMs) of (18-phenoxyoctadecyl)- trichlorosilane, thereby enhancing the mobility of pentacene devices to ~1 $cm^2 V^{-1} s^{-1}$ due to favorable interactions at the semiconductor-dielectric interface [42]. Finally, *Marks et al.* studied self-assembled multi-layers (SAMTs) grown from solution to achieve very low leakage currents and low operating voltages [43-45].

TH-1322_10612101

The contact resistance (R_C) can also influence the measured mobility [46]. The mobility in the saturation regime is less affected by V_{GS} and R_C, therefore eq.1.1 is used in this thesis work to calculate the mobility, as is normally done for MOSFETs. The threshold voltage V_{th} can be extracted by determining the x-axis intercept of $(I_{DS})^{1/2}$ versus V_{GS} in the saturation regime [47], as shown in Figure 1.8b [48]. V_{th} is the voltage, where the conducting channel is formed. In the accumulation region, V_{th} is given by [49]:

$$V_{th} = \pm \frac{qn_0 d}{C_i} + V_{fb} \qquad \text{---------- (1.8)}$$

where V_{fb} is the flat-band potential, which accounts for any work-function difference between the semiconductor and the gate metal. Here, q is the elementary charge, n_0 is the density of free carriers, and d is the thickness of the semiconductor. The sign of the right-hand side in the equation corresponds to the sign of the charge carriers [49]. From this equation a change in V_{th} between the forward and the reverse sweep of voltage, the response may not be reversible and thereby a hysteresis can be expected, if (i) n_0 changes (*e.g.* due to trapping of free charge carriers) (ii) C_i changes (*e.g.* charge injection from the gate into the dielectric or polarization of the dielectric) and (iii) V_{fb} changes (*e.g.* structural changes in the semiconductor). This defines the stability of the devices, which needs to be studied. For all digital applications, OFETs are typically used a switch by operating between on and off states. It is important to have higher on/off current ration in order to have better distinction between the states. This is also another parameter that defines the efficient performance of OFETs.

In general organic semiconductors are intrinsically non-doped and therefore non-conducting without an applied gate field ("normally off"). Field effect transistors using un-doped organic semiconductors work in the accumulation mode (the gate field accumulates charges at the semiconductor / dielectric interface that form the conducting channel). From the log-plot of transfer characteristics one can see that I_{DS} starts to increase before V_{th} is reached. This is the sub-threshold regime. In Si transistors the "kink" where I_{DS} starts to increase is called "turn on voltage" and describes the start of the inversion regime. As there is no inversion in organic semiconductors OFETs, the phrase "turn on voltage" can be misleading. Alternatively, "switch on voltage" can be used to describe the "kink" in the

TH-1322_10612101

logarithmic plot of the transfer characteristics where the current starts to increase [50]. The current increase in the sub-threshold regime is measured as the sub-threshold slope S (also called sub-threshold swing), which indicates the additional V_{GS} required to increase I_{DS} by a factor of ten (one decade). Values as low as about 100 mV/dec have been reported [42, 51], which is close to the theoretical limit of 60 mV/dec at RT [42, 52] and can be calculated using [39],

$$S = (\log 10)\frac{\partial V_{GS}}{\partial \ln(I_{DS})} = (\log 10)\frac{kT}{q}\left(\frac{C_i + C_D}{C_i}\right) \qquad \text{---------- (1.9)}$$

where C_D is the semiconductor depletion layer capacitance.

1.6 Hysteresis effect in OFETs

Hysteresis indicates the bistability in the OFET current. It is essentially the difference in the I_{DS} values observed during forward and backward sweeping of V_{GS}. It could be useful in non-volatile memory devices, but it has to be avoided in standard integrated circuits. Threshold voltage shifts due to bias stress have been reported more frequently, but detailed investigations of hysteresis effects are rare and a complete picture of the physical background that may cause hysteresis in OFETs is still unexplored. Some of the mechanisms causing hysteresis in OFETs are already quite well described in the literature on inorganic field-effect transistor devices.

a) *Interface trapped charges* (also called interface state or fast state) are defects or impurities at the interface that can be charged or discharged.
b) *Fixed charges in oxide* is a positive charge due to structural defects close to the channel (2 nm), which does not communicate with the under laying substrate.
c) *Trapped charges in dielectric* are electrons or holes trapped in the bulk of the dielectric layer. These traps can be introduced during device fabrication and the charges (electrons or holes) are injected during device operation.
d) *Mobile charges in dielectric* are mainly small alkali metal cations and H^+, but can also be larger cations or anions.

TH-1322_10612101

The occurrence of charges (a) to (d) in the Si-SiO_2 system is leading to hysteresis phenomena in inorganic transistor devices. Interestingly, the practical application of Si MOSFETs was delayed in the early 1960s because of severe gate bias instability problems caused by mobile ionic charges. Water is known to diffuse into not densely packed SiO_2. A small amount dissociates into H^+ and OH^-. These ions can drift in an electric field to the channel and cause threshold voltage shifts [53]. The hysteresis effects are very well observed in OFETs and causes instability in the device operation. Therefore, it is important to study the hysteresis effects in the OFETs. Cyclic transfer characteristics (I_{DS} vs V_{GS}), where I_{DS} depends on the sweep direction of V_{GS} show "hysteresis", which is schematically depicted in Figure 1.10. These reversible electrical bistabilities are frequently observed in organic field effect transistors. Depending on the microscopic effect the hysteresis can result in a back sweep current (the sweep from on to off) that is either higher or lower than the forward sweep current (the sweep from off to on state). This can be either "clockwise" or "anti-clockwise". However, these notations can be misleading, because the direction of the hysteresis also depends on the p- or n-type character of the OFETs of interests.

Figure 1.10 (a) and (b) show schematic transfer characteristics where the back sweep current is higher than the forward sweep current. For *p*-type OFETs the direction of this hysteresis is "clockwise" whereas for *n*-type OFETs the turning direction is "anti-clockwise".

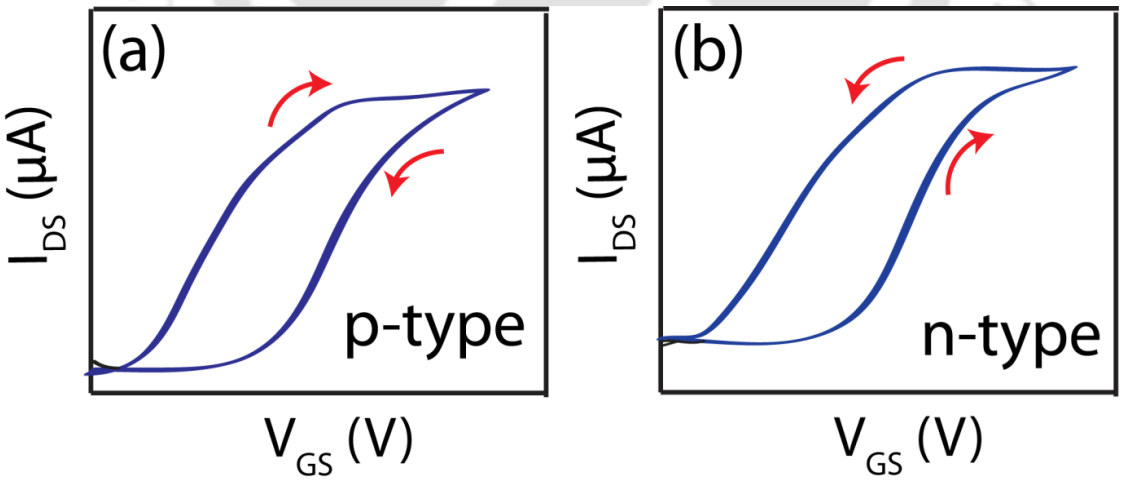

Figure 1.10: Schematic representation of hysteresis transfer curves of **(a)** *p*-type and **(b)** *n*-type OFETs.

TH-1322_10612101

Threshold voltage shifts are frequently observed due to bias stress effects on OFETs. Bias stress is the application of a (usually) constant V_{GS} for an extended time. Such bias stress causes instabilities, which may lead either to hysteresis, if the bias stress effect occurs to a large extent reversibly with V_{GS}, or to degradation, if the bias stresses effect is irreversible. Hysteresis and degradation might have the same physical origin [54-56]. The direction of the shift is such that a fully turned on OFET slowly turns itself off and vice versa [57]. Recovery is sometimes possible; it follows power law time dependence and may take a few days in the dark. Investigating the bias stress in an OFET can also cause a change in effective field effect mobility, which is attributed to an irreversible structural change in the semiconductor due to the electro-strictive effect [58].

Many physical effects causing hysteresis in OFETs are reported. Some of these effects are identical to those already mentioned for inorganic transistors and few more reasons are:

a) Effects of mobile charges close to or in the *semiconductor channel* (near the semiconductor / dielectric interface):
    1. Trapped majority or minority charges in the channel close to the semiconductor / dielectric interface.
    2. Charge injection from the semiconductor into the dielectric.
    3. Slow reactions (*e.g.* bipolaron formation) of mobile charge carriers in the polymeric semiconductor.
    4. Mobile ions in the semiconductor.

b) Effects resulting in a *bulk polarization of the gate dielectric*:
    1. Polarization of the dielectric (ferroelectrics as dielectric or meta-stable "quasi-ferroelectric" polarization in the dielectric).
    2. Mobile ions in the dielectric.

c) Charge *injection from the gate* electrode into the dielectric

Dielectric (gate insulator) with low k values ("low k dielectric") increases the mobility and reduces the hysteresis [59-61]. High-k dielectrics covered with a thin flat layer of a low-k dielectric result in OFETs with low voltage and high mobility [51, 62], whereas a rough interface causes additional traps, thus hysteresis increases [63, 64]. The optimized combinations of organic-inorganic (polymer-metal oxide) and inorganic-inorganic (metal

TH-1322_10612101

oxide-metal oxide) dielectrics are acquiring more importance to solve this hysteresis problem.

1.7 Gate dielectric layer

The main focus discussing the characteristics of OFETs is usually on the semiconductor and its properties. Ongoing research showed that the dielectric has major influences on the device properties. The necessary voltage to form the channel is determined by the capacitance of the dielectric layer. Traps, dipoles and the surface roughness of the dielectric have a strong influence on OFET performances. Furthermore, the dielectric can influence the morphology of the semiconductor.

The most common gate dielectrics used in both academia and industry are Si substrates having SiO_2 layers (typically 100-300 nm thick). The utilization of this dielectric is very convenient due to the ready availability of the thermally grown dioxide. In fact, silicon can be reacted with oxygen or nitrogen in a controlled manner to form superb insulating layers with excellent mechanical, electrical, and dielectric properties. Recently, it has been shown that the semiconductor-dielectric interface in these devices contains a large density of electron-trapping sites due the existence of surface hydroxyl groups, which are present in the form of silanols [65]. Neutralization of these sites has been partially solved using surface treatments in which a monolayer is self-assembled on the SiO_2 surface.

The interest in new dielectric materials has arisen primarily from the necessity for inexpensive device fabrication processes and the reduction of the operating voltages required for advanced flexible/printed electronics technologies. In fact, one of the major challenges in the development of OFETs has been the rather high voltages needed for their operation when using SiO_2 gate dielectrics ($k \approx 4$), making these devices impractical for low-priced applications. It is thus mandatory to search for thin, high-k gate dielectrics to achieve the requirements needed for new technologies. One of these requirements is reduction of the device size that can be also achieved using high-capacitance gate insulators. In this sense, SiO_2 has reached its scaling limit, directing the study of many groups in the search for

TH-1322_10612101

alternative metal oxides (HfO_2, Ta_2O_5, Al_2O_3, Y_2O_3, $BaTiO_3$, TiO_2, $SrTiO_3$ etc.) as alternative insulator layers.

The main advantage with the above mentioned metal-oxides are that they can be solution processable. It allows the fabrication of the devices at low temperatures, which leads to large area and flexible electronic applications, results low-cost device technology. In the following chapters, we have presented the details of synthesis and importance of different metal-oxides Al_2O_3, TiO_2, $BaTiO_3$, $SrTiO_3$, and $BaSrTiO_3$ via characterization of fabricated OFETs.

1.8 References

[1] W. Brutting, C. Adachi, Physics of Organic Semiconductors, 2nd ed., Wiley-Vch (2012).

[2] P. Peumans, S. Uchida, S.R. Forrest, Efficient bulk heterojunction photovoltaic cells using small-molecular-weight organic thin films, Nature, 425 (2003) 158-162.

[3] A. Hadipour, B. de Boer, P.W.M. Blom, Organic tandem and multi-junction solar cells, Adv. Funct. Mater., 18 (2008) 169-181.

[4] L.M. Chen, Z.R. Hong, G. Li, Y. Yang, Recent Progress in Polymer Solar Cells: Manipulation of Polymer: Fullerene Morphology and the Formation of Efficient Inverted Polymer Solar Cells, Adv. Mater., 21 (2009) 1434-1449.

[5] J.H. Burroughes, D.D.C. Bradley, A.R. Brown, R.N. Marks, K. Mackay, R.H. Friend, P.L. Burns, A.B. Holmes, Light-Emitting-Diodes Based on Conjugated Polymers, Nature, 347 (1990) 539-541.

[6] S. Reineke, F. Lindner, G. Schwartz, N. Seidler, K. Walzer, B. Lussem, K. Leo, White organic light-emitting diodes with fluorescent tube efficiency, Nature, 459 (2009) 234-238.

[7] G. Schwartz, S. Reineke, T.C. Rosenow, K. Walzer, K. Leo, Triplet Harvesting in Hybrid White Organic Light-Emitting Diodes, Adv. Funct. Mater., 19 (2009) 1319-1333.

[8] J.B. Wu, M. Agrawal, H.A. Becerril, Z.N. Bao, Z.F. Liu, Y.S. Chen, P. Peumans, Organic Light-Emitting Diodes on Solution-Processed Graphene Transparent Electrodes, ACS nano, 4 (2010) 43-48.

[9] F. Garnier, R. Hajlaoui, A. Yassar, P. Srivastava, All-Polymer Field-Effect Transistor Realized by Printing Techniques, Science, 265 (1994) 1684-1686.

TH-1322_10612101

[10] D. Braga, G. Horowitz, High-Performance Organic Field-Effect Transistors, Adv. Mater., 21 (2009) 1473-1486.

[11] Y.H. Kim, J.S. Heo, T.H. Kim, S. Park, M.H. Yoon, J. Kim, M.S. Oh, G.R. Yi, Y.Y. Noh, S.K. Park, Flexible metal-oxide devices made by room-temperature photochemical activation of sol-gel films, Nature, 489 (2012) 128-133.

[12] M.A. McCarthy, B. Liu, E.P. Donoghue, I. Kravchenko, D.Y. Kim, F. So, A.G. Rinzler, Low-Voltage, Low-Power, Organic Light-Emitting Transistors for Active Matrix Displays, Science, 332 (2011) 570-573.

[13] C.R. Kagan, D.B. Mitzi, C.D. Dimitrakopoulos, Organic-inorganic hybrid materials as semiconducting channels in thin-film field-effect transistors, Science, 286 (1999) 945-947.

[14] H.S. Soliman, A.M.A. El-Barry, N.M. Khosifan, M.M. El Nahass, Structural and electrical properties of thermally evaporated cobalt phthalocyanine (CoPc) thin films, European Physical Journal-Applied Physics, 37 (2007) 1-9.

[15] S.J. Qiu, H.L. Chu, J. Zhang, Y.N. Qi, L.X. Sun, F. Xu, Heat capacities and thermodynamic properties of CoPc and CoTMPP, J. Therm. Anal. Calorim., 91 (2008) 841-848.

[16] R.P. Linstead, J.M. Robertson, The stereochemistry of metallic phthalocyanines, J. Chem. Soc., (1936) 1736-1738.

[17] P. Ballirano, R. Caminiti, C. Ercolani, A. Maras, M.A. Orru, X-ray powder diffraction structure reinvestigation of the alpha and beta forms of cobalt phthalocyanine and kinetics of the alpha ->beta phase transition, J. Am. Chem. Soc., 120 (1998) 12798-12807.

[18] G.A. Williams, B.N. Figgis, R. Mason, S.A. Mason, P.E. Fielding, Structure of Phthalocyaninatocobalt(II) at 4.3 K - a Neutron Diffraction Study, J. Chem. Soc., (1980) 1688-1692.

[19] C.D. Dimitrakopoulos, P.R.L. Malenfant, Organic thin film transistors for large area electronics, Adv. Mater., 14 (2002) 99-117.

[20] R.J. Chesterfield, J.C. McKeen, C.R. Newman, C.D. Frisbie, P.C. Ewbank, K.R. Mann, L.L. Miller, Variable temperature film and contact resistance measurements on operating n-channel organic thin film transistors, J. Appl. Phys., 95 (2004) 6396-6405.

TH-1322_10612101

[21] S. Tatemichi, M. Ichikawa, T. Koyama, Y. Taniguchi, High mobility n-type thin-film transistors based on N,N '-ditridecyl perylene diimide with thermal treatments, Appl. Phys. Lett., 89 (2006) 112108-3.

[22] C. Rolin, K. Vasseur, S. Schols, M. Jouk, G. Duhoux, R. Muller, J. Genoe, P. Heremans, High mobility electron-conducting thin-film transistors by organic vapor phase deposition, Appl. Phys. Lett., 93 (2008) 033305-3.

[23] M.A. Koorie, Y. Khopkar, H.F. Ji, S.R. Zivanovic, Single Mesowire Transistor From Perylene Tetracarboxylic Diimide, IEEE Trans. Nanotechnol., 11 (2012) 448-450.

[24] P.R.L. Malenfant, C.D. Dimitrakopoulos, J.D. Gelorme, L.L. Kosbar, T.O. Graham, A. Curioni, W. Andreoni, N-type organic thin-film transistor with high field-effect mobility based on a N,N-'-dialkyl-3,4,9,10-perylene tetracarboxylic diimide derivative, Appl. Phys. Lett., 80 (2002) 2517-2519.

[25] S.R. Forrest, Ultrathin organic films grown by organic molecular beam deposition and related techniques, Chem. Rev., 97 (1997) 1793-1896.

[26] A.-L. Barabási, H.E. Stanley, Fractal Concepts in Surface Growth, Cambridge University Press, Cambridge, (1995).

[27] J. Lapujoulade, The roughening of metal surfaces, Surf. Sci. Reports . 20 (1994) 191-249.

[28] M. Pelliccione, T.-M. Lu, Evolution of thin film morphology: modeling and simulation, Springer-Verlag, New York, (2008).

[29] Y. Zhao, G.-C. Wang, T.-M. Lu, Characteriztion of Amorphus and Crystalline Rough Surface: Principles and Application, Academic Press, London, (2001).

[30] J.H. Jeffries, J. Zuo, M.M. Craig, Instability of Kinetic Roughening in Sputter-Deposition Growth of Pt on Glass, Phys. Rev. Lett., 76 (1996) 4931-4934.

[31] M. Pelliccione, T. Karabacak, C. Gaire, G.-C. Wang, T.-M. Lu, Mound formation in surface growth under shadowing, Phys. Rev. B., 74 (2006) 125420-125410.

[32] J.-K. Zuo, J.F. Wendelken, Evolution of Mound Morphology in Reversible Homoepitaxy on Cu(100), Phys. Rev. Lett., 78 (1997) 2791-2794.

[33] J. Kim, D.G. Cahill, R.S. Averback, Surface morphology of Ge(111) during etching by keV ions, Phys Rev B, 67 (2003) 045404-6.

[34] P.K. WEIMER, The TFT A New Thin-Film Transistor, Proc IRE, 50 (1962) 1462-1469.

TH-1322_10612101

[35] G.H. Gelinck, H.E.A. Huitema, E. Van Veenendaal, E. Cantatore, L. Schrijnemakers, J.B.P.H. Van der Putten, T.C.T. Geuns, M. Beenhakkers, J.B. Giesbers, B.H. Huisman, E.J. Meijer, E.M. Benito, F.J. Touwslager, A.W. Marsman, B.J.E. Van Rens, D.M. De Leeuw, Flexible active-matrix displays and shift registers based on solution-processed organic transistors, Nat. Mater., 3 (2004) 106-110.

[36] H. Klauk, Organic Electronics, Materials, Manufacturing and Applications, Wiley-VCH, Weinheim, Germany, 2006.

[37] G. Horowitz, R. Hajlaoui, R. Bourguiga, M. Hajlaoui, Theory of the organic field-effect transistor, Synth. Met., 101 (1999) 401-404.

[38] G. Horowitz, Organic Electronics: Materials, Manufacturing, and Applications, Wiley-VCH, Weinheim, Germany, 2006.

[39] S. SM., N. KK., Physics of Semiconductor Devices, Wiley, New Jersey, 2007.

[40] L.L. Chua, P.K.H. Ho, H. Sirringhaus, R.H. Friend, High-stability ultrathin spin-on benzocyclobutene gate dielectric for polymer field-effect transistors, Appl. Phys. Lett., 84 (2004) 3400-3402.

[41] J. Collet, O. Tharaud, A. Chapoton, D. Vuillaume, Low-voltage, 30 nm channel length, organic transistors with a self-assembled monolayer as gate insulating films, Appl. Phys. Lett., 76 (2000) 1941-1943.

[42] M. Halik, H. Klauk, U. Zschieschang, G. Schmid, C. Dehm, M. Schutz, S. Maisch, F. Effenberger, M. Brunnbauer, F. Stellacci, Low-voltage organic transistors with an amorphous molecular gate dielectric, Nature, 431 (2004) 963-966.

[43] M.H. Yoon, A. Facchetti, T.J. Marks, sigma-pi molecular dielectric multilayers for low-voltage organic thin-film transistors, PNAS, 102 (2005) 4678-4682.

[44] S.A. DiBenedetto, A. Facchetti, M.A. Ratner, T.J. Marks, Charge Conduction and Breakdown Mechanisms in Self-Assembled Nanodielectrics, J. Am. Chem. Soc., 131 (2009) 7158-7168.

[45] Y.G. Ha, A. Facchetti, T.J. Marks, Push-Pull pi-Electron Phosphonic-Acid-Based Self-Assembled Multilayer Nanodielectrics Fabricated in Ambient for Organic Transistors, Chem. Mater., 21 (2009) 1173-1175.

TH-1322_10612101

[46] G. Horowitz, M.E. Hajlaoui, R. Hajlaoui, Temperature and gate voltage dependence of hole mobility in polycrystalline oligothiophene thin film transistors, J. Appl. Phys., 87 (2000) 4456-4463.

[47] G. Horowitz, R. Hajlaoui, H. Bouchriha, R. Bourguiga, M. Hajlaoui, The concept of "threshold voltage" in organic field-effect transistors, Adv. Mater., 10 (1998) 923-927.

[48] M. Mottaghi, G. Horowitz, Field-induced mobility degradation in pentacene thin-film transistors, Org. Electron., 7 (2006) 528-536.

[49] G. Horowitz, Physics of Organic Field-Effect Transistors, Semiconducting Polymers, Wiley-VCH Verlag GmbH & Co. KGaA2005, pp. 463-514.

[50] K.P. Pernstich, S. Haas, D. Oberhoff, C. Goldmann, D.J. Gundlach, B. Batlogg, A.N. Rashid, G. Schitter, Threshold voltage shift in organic field effect transistors by dipole monolayers on the gate insulator, J. Appl. Phys., 96 (2004) 6431-6438.

[51] M. Zirkl, A. Haase, A. Fian, H. Schon, C. Sommer, G. Jakopic, G. Leising, B. Stadlober, I. Graz, N. Gaar, R. Schwodiauer, S. Bauer-Gogonea, S. Bauer, Low-voltage organic thin-film transistors with high-k nanocomposite gate dielectrics for flexible electronics and optothermal sensors, Adv. Mater., 19 (2007) 2241-2245.

[52] S. Scheinert, G. Paasch, Fabrication and analysis of polymer field-effect transistors, Phys Status Solidi A, 201 (2004) 1263-1301.

[53] A. Sharma, S.G.J. Mathijssen, E.C.P. Smits, M. Kemerink, D.M. de Leeuw, P.A. Bobbert, Proton migration mechanism for operational instabilities in organic field-effect transistors, Phys. Rev. B., 82 (2010) 075322-11.

[54] N. Padma, S.N. Sawant, V. Sudarsan, S. Sen, S.K. Gupta, Comparison of the role of holes and electrons in hysteresis and threshold voltage stability of organic field effect transistors, Phys Status Solidi A, 210 (2013) 2111-2120.

[55] R. Nouchi, Y. Kubozono, Anomalous hysteresis in organic field-effect transistors with SAM-modified electrodes: Structural switching of SAMs by electric field, Org. Electron., 11 (2010) 1025-1030.

[56] M. Egginger, M. Irimia-Vladu, R. Schwodiauer, A. Tanda, I. Frischauf, S. Bauer, N.S. Sariciftci, Mobile ionic impurities in poly(vinyl alcohol) gate dielectric: Possible source of the hysteresis in organic field-effect transistors, Adv. Mater., 20 (2008) 1018-1022.

TH-1322_10612101

[57] A. Salleo, R.A. Street, Light-induced bias stress reversal in polyfluorene thin-film transistors (vol 94, pg 471, 2003), J. Appl. Phys., 94 (2003) 4231-4231.

[58] R.A. Street, Bias-induced change in effective mobility observed in polymer transistors, Phys. Rev. B., 77 (2008) 165311-8.

[59] L.A. Majewski, M. Grell, S.D. Ogier, J. Veres, A novel gate insulator for flexible electronics, Org. Electron., 4 (2003) 27-32.

[60] J. Veres, S.D. Ogier, S.W. Leeming, D.C. Cupertino, S.M. Khaffaf, Low-k insulators as the choice of dielectrics in organic field-effect transistors, Adv. Funct. Mater., 13 (2003) 199-204.

[61] A.F. Stassen, R.W.I. de Boer, N.N. Iosad, A.F. Morpurgo, Influence of the gate dielectric on the mobility of rubrene single-crystal field-effect transistors, Appl. Phys. Lett., 85 (2004) 3899-3901.

[62] M. Gedda, N.V.V. Subbarao, S.M. Obaidulla, D.K. Goswami, High carrier mobility of CoPc wires based field-effect transistors using bi-layer gate dielectric, Aip. Adv., 3 (2013) 112123-7.

[63] U. Haas, H. Gold, A. Haase, G. Jakopic, B. Stadlober, Submicron pentacene-based organic thin film transistors on flexible substrates, Appl. Phys. Lett., 91 (2007) 043511-3.

[64] M. Irimia-Vladu, N. Marjanovic, A. Vlad, A.M. Ramil, G. Hernandez-Sosa, R. Schwodiauer, S. Bauer, N.S. Sariciftci, Vacuum-Processed Polyaniline-C-60 Organic Field Effect Transistors, Adv. Mater., 20 (2008) 3887-3892.

[65] V. Chandrasekhar, R. Boomishankar, S. Nagendran, Recent developments in the synthesis and structure of organosilanols, Chem. Rev., 104 (2004) 5847-5910.

TH-1322_10612101

Chapter - II

Experimental Techniques

This chapter presents an overview of different experimental techniques used in this thesis work. This includes the techniques for the growth of thin film and the techniques used for characterization of the films. The techniques related to the fabrication of organic field-effect transistors are also elaborated. Two major growth techniques, namely organic molecular beam deposition (OMBD) works under high vacuum condition and anodization techniques for thin film growth, were custom designed and fabricated for this thesis work. It is very crucial to attain a precise characterization of structural and morphological properties, which in general is only made possible by employing different complementary techniques. Several surface sensitive complementary techniques were used to study the growth or organic films and their structural information. Scanning electron microscope (SEM) and atomic force microscope (AFM) were exhaustively used to study the surface morphology. The dynamics of the film growth were studied by monitoring the evolution of surface morphology with time by AFM and SEM. The local structural formation at the molecular level was probed by transmission electron microscope (TEM) measurement on some of the systems.TEM and X-ray diffraction (XRD) are complementary as first one provides local real space information at a microscopic length scale whereas the latter probes in reciprocal space. XRD technique has also been used to study the overall structural information of few of the systems. The techniques related to electrical characterization of the OFETs are also elaborated. This includes semiconductor parameter characterization system and probe station, which is operated under vacuum. In this chapter, we have provided brief technical details together with their working principle of all the above techniques.

TH-1322_10612101

2.1 Film Deposition Techniques

In this thesis work, we have used several film deposition techniques for the growth of different parts of OFETs. Some of the techniques are developed and few are standard commercial systems.

2.1.1 Developed Deposition Systems

(a) Organic Molecular Beam Deposition System

Organic molecular beam deposition (OMBD) is a typical method of thin film preparation for small organic semiconductor molecules, which are mostly exhibits low solubility. OMBD system works under the principle of molecular beam epitaxy (MBE) that is used for evaporating inorganic materials under ultra high vacuum condition. However, as the organic molecules are less reactive to impurities, unlike inorganic materials, can be evaporated under high vacuum condition as well. We have designed OMBD system, which works under high vacuum (base pressure ~ 10^{-7} mbar). Though there are several standard designed OMBD chambers are available, it is needed to modify the design to expand the utility of the chamber.

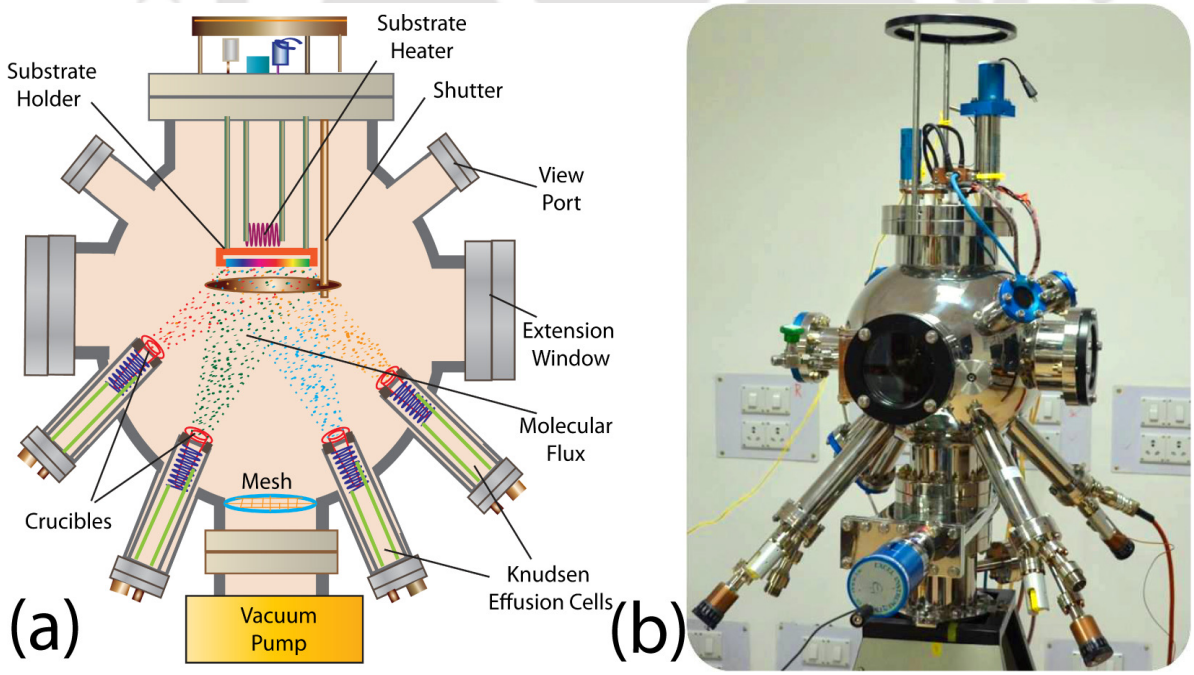

Figure 2.1 (a) Schematic representation of organic molecular beam deposition chamber and **(b)** Photograph of real chamber assembled in lab.

TH-1322_10612101

Figure 2.1(a) shows the typical chamber design and figure 2.1(b) shows the real photograph of designed chamber. This chamber has been designed such a way that one can do co-evaporation of four different compounds simultaneously with the help of four Knudsen-cells (brought from MBE-Komponenten GmbH) assembled at four different positions of chamber. Each Knudsen-cell contains one quartz crucible, which is used to load the organic compound and these crucibles are surrounded with heating coil.

(b) Anodization Technique

The high-quality Al_2O_3 gate insulators can be fabricated by electrochemical oxidation (anodization) of the gate metal [1]. Anodization is a solution based technique that can lead to very thin, pinhole-free, high capacitance OFET gate insulators on cheap substrates [2, 3]. In addition to that this process can yield a high-quality metal-oxide insulator at room temperature. Here, we have used glass slides (size: 15 mm × 25 mm) to serve as a device substrates. Every glass slide was initially cleaned with a 3:1 ratio mixture of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) followed by an ultrasonic bath at 80 ºC to remove the organic residues. A 300 nm thick aluminum strips with the dimensions of 1 mm × 20 mm were deposited on pre-cleaned substrate to serve as a define gate electrode. As a gate insulator, aluminum oxide (Al_2O_3) was electrochemically grown on the aluminum surface by galvanostatic anodization in 0.01 $molL^{-1}$ citric acid ($C_6H_8O_7$). The glass substrate with aluminum strip and a platinum electrode were immersed in to the electrolyte solution (shown in Figure 2.2).

Platinum serves as a counter electrode, and a thin layer of aluminum act as a working electrode. The electrolyte solution was placed on magnetic stirrer to have continuous stirring and degassed with argon gas during the whole anodization process with an applied constant current density of 0.3 $mAcm^{-2}$. By monitoring the anodization time of the galvanostatic process, the thickness of the oxide layer can be controlled. The reaction mechanism for this oxidation process follows as,

$$\text{Anode reaction: } 2Al + 3H_2O \rightarrow Al_2O_3 + 6e^- + 6H^+$$

$$\text{Cathode reaction: } \quad 6H^+ + 6e^- \rightarrow 3H_2$$

TH-1322_10612101

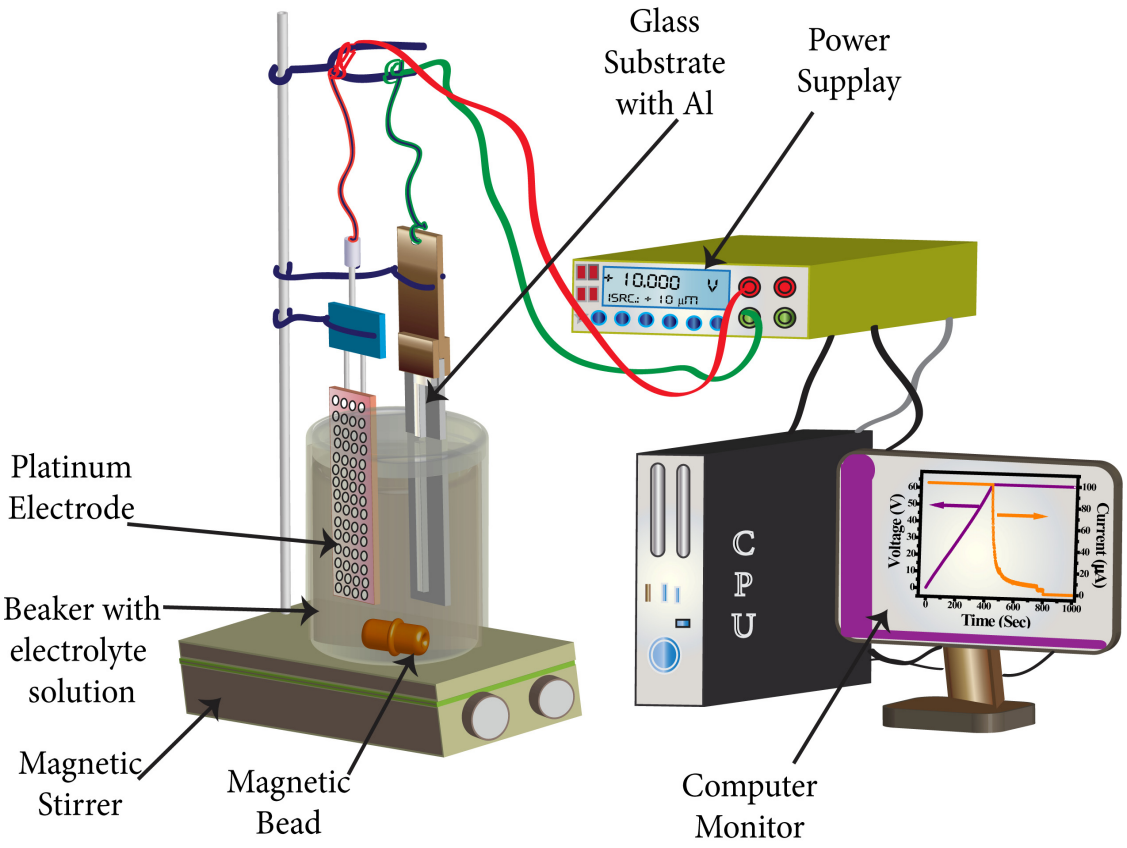

Figure 2.2: Schematic representation of typical anodization process in operating mode.

Further, the anodized sample will be transferred to an ultrasonic bath with de-ionized water at 80ºC for several minutes, results pinholes free alumina surface. To get rid of all water residues, heating of sample about 200ºC in an oven under reduced pressure for several hours is essential. In galvanostatic the anodization is performed by "ramping up the voltage up to a limiting anodization voltage V_A". The thickness d of the resulting films can be controlled very precisely via the anodisation voltage V_A, with $d = cV_A$. c is known as the "anodisation ratio" and is related to the electric breakdown field E_B via $E_B \approx c^{-1}$, for Al this value is 1.3nm/V.

2.1.2 Standard Techniques

(a) Organic Physical Vapor Deposition Technique

In organic vapor phase deposition (OVPD), an inert carrier gas is used to transport organic small molecules towards a cooled substrate. The main advantages of OVPD are

TH-1322_10612101

excellent morphology control [4] combined with high deposition throughputs [5]. Compared to vacuum and spin-coating techniques, OVPD gains an extra degree of freedom by using carrier gases. However, near the sublimation point, the vapor pressure of the organic material varies rapidly with temperature, making accurate control of transport rates by varying the source temperature difficult. Yet, if source temperatures are controlled to within a few degrees, the relative concentrations of organic constituents in the gas stream can be accurately varied by adjusting the carrier gas flow rates, thus making it suitable for the fabrication of organic nano/micro structures. The sizes of organic nano/micro structures can be controlled by varying deposition conditions such as substrate temperature, carrier gas flow rate, deposition time and deposition rate. The typical design of single zone furnace OVPD chamber is shown in Figure 2.3.

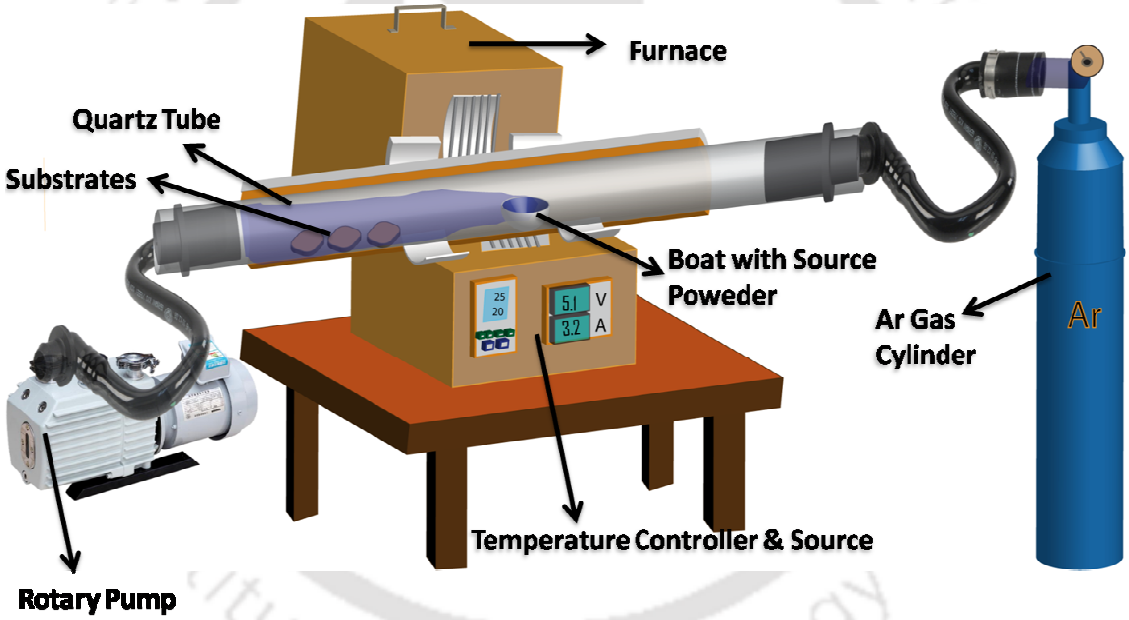

Figure 2.3: Schematic diagram of typical organic vapor phase deposition chamber in working mode.

2.2 Microscopic Characterization Techniques

2.2.1 Atomic Force Microscopy

In 1986 atomic force microscopy (AFM) was implemented allowing to image any arbitrary surface irrespective of material conductivity [6] and it is the one of most common

scanning probe microscopes (SPM). It works based on the simple principle that a sharp tip is brought in direct contact with a surface causing interactions between tip and surface. A certain physical variable such as force is probed while the tip is scanning a defined area on the sample. In general, a constant interaction between tip and sample surface is set thereby recording the reaction of the tip due to topographic changes.

The instrumental setup of AFM is rather simple consisting of a pyramidal shaped tip attached to a probe called cantilever with elastic constant K (see Figure 2.4) which scans the substrate surface at small distances [7]. A piezoelectric scanner is either moving the tip across the sample or the sample across a fixed tip. Deflections of the cantilever, arising from interaction forces between sample and tip, are usually measured by focusing a laser beam on the cantilever. The reflected beam from the top side of the cantilever is collected by a position-sensitive photodiode.

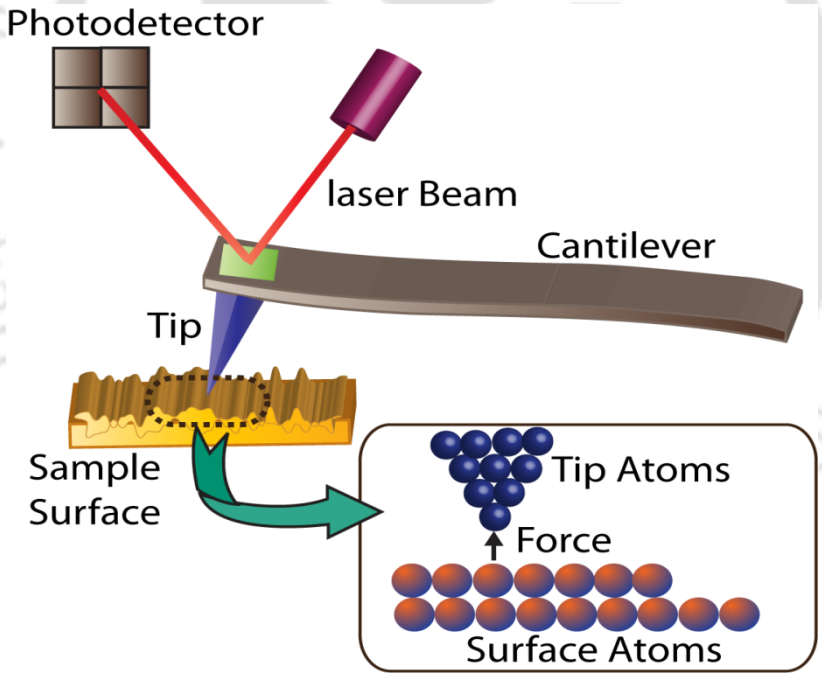

Figure 2.4: Schematic illustration of atomic force microscopy in operating mode.

In absence of interaction forces the reflection is centered in the photodiode. However, as soon as the tip "feels" a force there will be a deflection of the cantilever. As a result, the reflected laser beam is changing its position on the photodiode generating now a different photo current. If the photodiode contains four independent segments it is possible to

TH-1322_10612101

distinguish between deflection and torsion of the cantilever. In response to the normal force F_z the cantilever is bending down in z direction according to Hook's law $F_z = K\Delta z$ inducing a vertical displacement Δz. Torsions, however, lead to a lateral movement of the reflected laser beam on the photodiode. The tip-sample force as a function of distance does not follow a monotonic behavior which makes it difficult to operate the AFM with a stable feedback loop. Thus, different modes are present to overcome this difficulty which basically can be divided into the contact mode and dynamic modes.

Contact Mode: In the contact mode, the tip is brought in direct contact with the sample's surface. While the tip is scanning across the surface, it is deflected as the tip is moving over the surface corrugation. There is a whole zoo of forces contributing to the deflection: short-range repulsive forces arising from the overlap of the tip and sample orbitals, long range van-der Waals forces as a result of dipole-dipole interactions, electrostatic forces, friction forces and adhesion forces. The measurement of the topography can be either carried out in constant height mode or constant force mode, both illustrated in Figure 2.5.

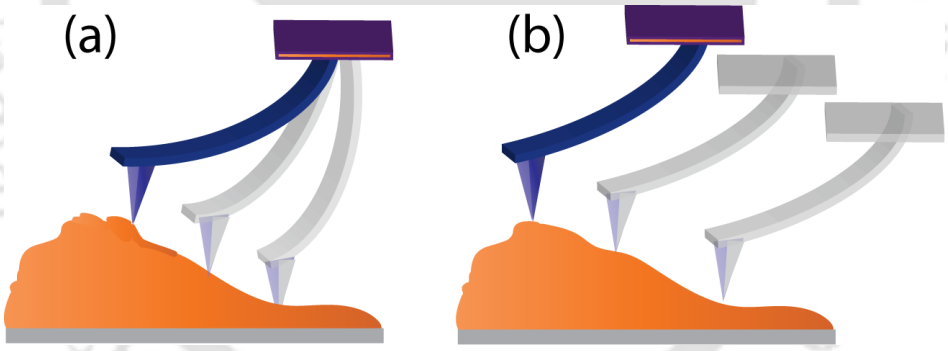

Figure 2.5: (a) Illustration of the constant height mode where the tip scans the surface at a constant height. **(b)** Constant force mode where the cantilever kept at a constant deflection.

The advantage of constant height mode is its simplicity since there is no demand on a feedback circuit. However, this mode is only applicable to very flat and smooth surface due to the tip's geometry. The constant force mode is more common. Here, the tip is kept at a constant cantilever deflection at each point by using a feedback circuit. If the cantilever deflection is changing, the feedback circuit immediately makes sure to get back to the initial cantilever position by moving the sample with the help of the piezoelectric scanner.

TH-1322_10612101

Therefore, the topography of the sample corresponds to the recorded changes in the cantilever-surface displacements. To display the force as a function of cantilever-surface distance is a general procedure to calibrate the cantilever sensitivity and to investigate the tip-sample interaction. Here, the cantilever deflection is measured while approaching and withdrawing the tip from the sample.

A special technique of contact mode is the jumping mode which is suitable to image softer samples and samples in liquids [8]. The working principle can be described as a cycle repeated at each image point with the following steps: first, the tip approaches into contact using a feedback which is in general performed on the cantilever deflection. Afterwards, it retracts out of contact and moves laterally one step. The relevant feature of jumping mode is that the lateral motion occurs when the tip is not in contact with the sample in order to avoid shear forces. However, the displacements in ambient conditions can be larger than 200 nm due to high adhesion forces. Therefore, the tip-sample separation and the approach step take a relatively long time which makes jumping mode a rather slow scanning mode. It should be kept in mind that images measured with an AFM are always a convolution of the probe geometry and the shape of the features being imaged. De-convolution of the tip should be taken into account for the analysis of samples with topographical characteristics in the nanometer scale.

Dynamic Mode (Non-Contact Mode): The idea of developing an AFM working in the so called dynamic mode or tapping mode or non-contact mode was to minimize the sample damage which is inherent in contact mode since it is operating in the repulsive regime. Figure 2.6 represents the schematic of tapping mode AFM. The dynamic mode, in contrast, is taking place in the attractive regime. Here, the cantilever is mounted on an actuator to allow a deliberate oscillation by external excitation amplitude 'A' and excitation frequency ω. It can be distinguished between two basic methods of dynamic operation: amplitude-modulation and frequency-modulation [9, 10]. Both modes have in common that the actuator is driven by fixed amplitude at a fixed frequency being close to the resonance frequency $\omega_0 = \sqrt{k/m}$ of the free cantilever. This can be simply described by a driven harmonic oscillator with damping via the differential equation:

TH-1322_10612101

$$m\ddot{z} + \frac{m\omega_0}{Q}\dot{z} + m\omega_0^2 z = m\omega_0^2 A\cos(\omega t) \qquad \text{---------- (2.1)}$$

here, Q is the quality factor related to the damping of the cantilever. The solution of this second order differential equation consists of the superposition of a transient term describing the adaption of the cantilever movement to the excitation frequency and a steady-state term with constant amplitude A_0, frequency ω and phase ϕ :

$$z(t) = A_t e^{-\omega_0 t/2Q}\, sin(\omega_0 t + \phi_t) + A_0\cos(\omega_0 t + \phi) \qquad \text{---------- (2.2)}$$

ϕ_t is the phase and A_t represents the amplitude of the transient term. The exponent $\omega_0 t/2Q$ determines the time τ after which the steady term dominates the motion.

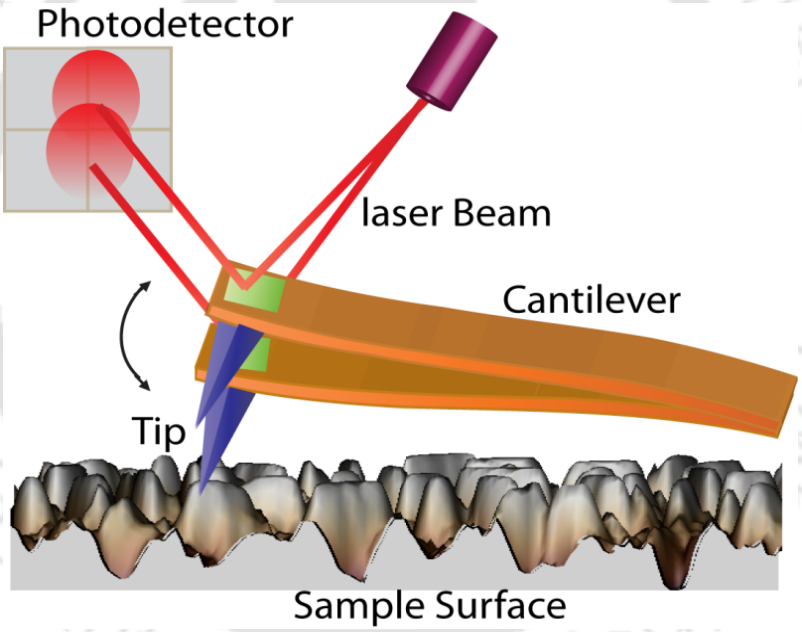

Figure 2.6: Schematic illustration of typical AFM operating in tapping mode.

When the tip approaches the sample, interaction forces change both the amplitude and the phase relative to the driving signal of the cantilever. The important difference between amplitude-modulation and frequency-modulation is the feedback signal. In amplitude-modulation the change in amplitude is used as feedback. This change, however, does not happen instantaneously with a change in the tip-sample interaction but on a time scale of $\tau_{AM} \approx 2Q/\omega_0$ which makes this mode very slow. The problem was solved by introducing the

TH-1322_10612101

frequency-modulation where the change in the resonance frequency occurs within a single oscillation on a time scale of $\tau_{FM} \approx 1/\omega_0$.

Initially, both modes were meant to be non-contact modes implying that the cantilever is far away from the surface and clearly in the attractive regime. But the amplitude-modulation mode was also later used at an intermediate regime involving repulsive tip-sample interactions which is nowadays usually called tapping mode [11-13].

2.2.2 Electron Microscopy

The aim of any microscopy is to resolve structures which are not able to be seen by the naked eye. In the previous section, it was shown that this is manageable by the manufacture of sharp tips brought in close contact to the sample surface thereby exploiting the presence of different interactions between the tip and the sample. Another approach was accomplished by the introduction of electron microscopy which uses the wave nature of electrons discovered by Louis de Broglie in 1924. The term of an electron microscope was first used by *Knoll* and *Ruska* in 1932 and they succeeded in recording electron images [14, 15]. For this achievement, Ruska received the Nobel Prize (somewhat late) in 1986.

It is known that the limit of the resolution is given by the wavelength of the light. Therefore, electron microscopes (whose electron beams possess a wavelength of about 105 times smaller than that of light waves) exhibit the essential advantage over light microscopes that they can resolve structures in the atomic regime down to one to two Angstroms. In the next section, two representatives of electron microscopes will be shortly introduced namely the transmission electron microscope (TEM) and the scanning electron micro- scope (SEM) which both works under vacuum. References [16, 17] are suggested for a more profound understanding of both techniques.

(a) Transmission Electron Microscopy

Transmission electron microscopy (TEM) can be divided into imaging and analytical TEM. Conventional TEM and high resolution TEM (HRTEM) allow an investigation of the micro- and nanostructure of the respective sample with a high spatial resolution down to the

TH-1322_10612101

atomic level. Analytical TEM, in addition, gives an insight into the chemical composition as well as the electronic structure of the illuminated specimen. One prerequisite for TEM-studies is the thickness of the sample which should not exceed 200 nm in order to assure that the high energy electrons pass through. Rotationally symmetric, inhomogeneous magnet fields guarantee a collimating and focusing of the electron beam. Figure 2.7 shows schematically the optical path in a conventional TEM. The beam is generated in the electron source (usually a heated tungsten filament, lanthanum hexa-boride (LaB_6) cathode or a field emission cathode) and accelerated by an electric potential in the range of typically several 100 kV. A Wehnelt-cylinder and a condenser lens system focus the electron beam on the specimen where the interaction processes take place.

The scattered electrons emerging from the thin sample are taken by the objective lens recombining them again to form an image in the image plane. In addition, a diffraction pattern is created in the back focal plane where an objective aperture can be inserted. Depending on the adjustment of the intermediate lens the viewing screen is showing either the diffraction pattern or the image. If the back focal plane of the objective lens acts as the object plane for the intermediate lens, the diffraction pattern can be observed on the screen. If, however, the image plane of the objective lens acts as the object plane, then the image is projected onto the viewing screen. The contrast differences in conventional TEMs are related to the specimen structure and occur in amorphous samples via scattering and in crystalline samples by diffraction.

One problem, which still has to be solved, is that the obtained diffraction pattern from the specimen contains electrons from its whole area. In this case, the viewing screen can be damaged due to the intense direct beam. Besides, the pattern is not very useful because the sample is very often buckled. The standard way to overcome this issue is to use a selecting aperture called selected-area electron diffraction (SAED) mode [18]. When using the diffraction pattern mode together with the SAED aperture two imaging operations can be performed by inserting the objective aperture: the bright-field (BF) image or the dark-field (DF) image. The BF image is characterized by selecting the direct beam with the objective aperture. In the DF image mode, the scattered electrons are chosen by adjusting the objective aperture.

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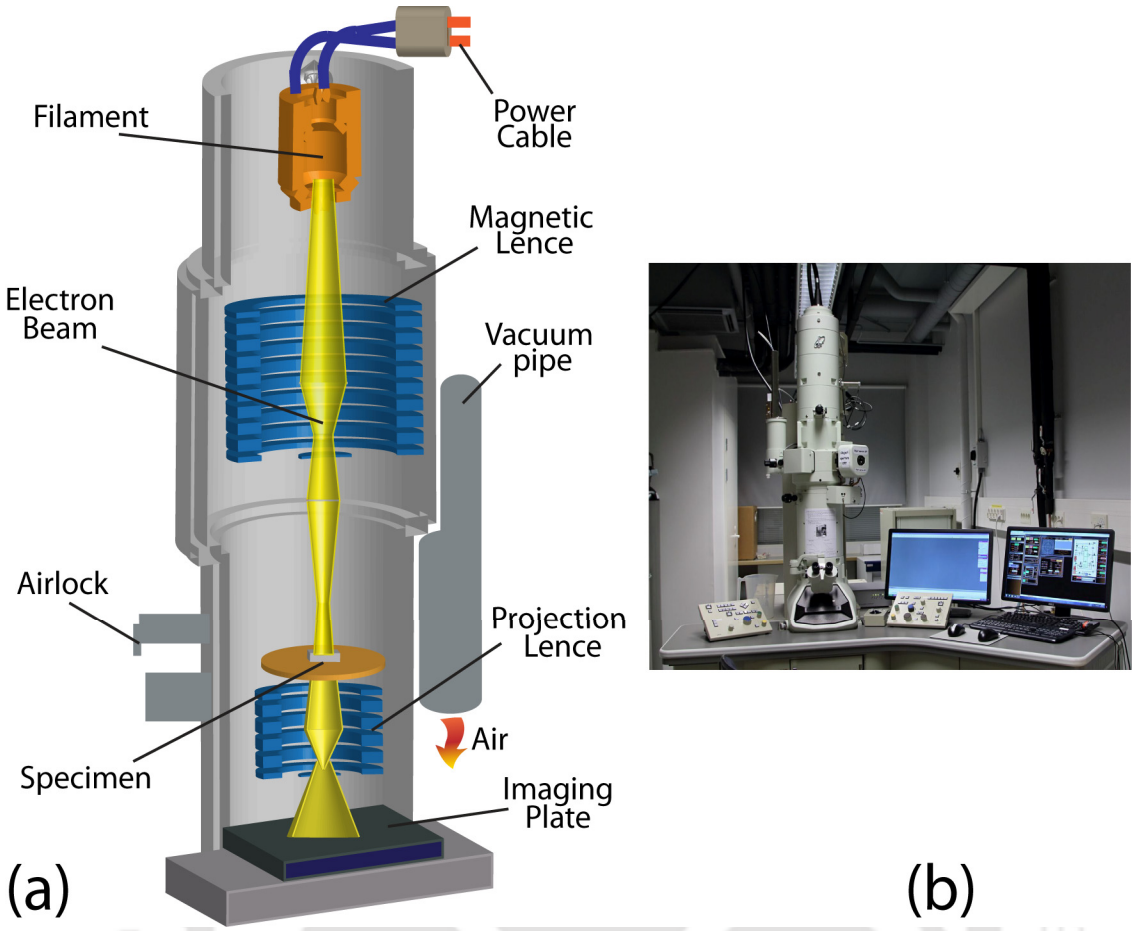

Figure 2.7: (a) Schematic representation of scheme of TEM and **(b)** Photograph of real equipment.

(b) Scanning Electron Microscopy

Scanning electron microscopy (SEM) has a lower resolution than TEM but allows to scan larger areas on the sample surface providing a representative overview of the respective specimen. In contrast to TEM where the electrons pass through the specimen and create "direct" images, is the image in SEM generated by backscattered electrons providing "indirect" images.

A bundled electron beam (the so called primary beam), which contains electrons accelerated by an electric potential in the range of only 1-40 keV, is scanning the sample surface. The electron beam impinges on the specimen surface and interaction processes take

TH-1322_10612101

place. These processes can be classified into elastic and inelastic scattering. Elastic scattering involves electrons which get deflected by the positively charged atomic nuclei thereby changing their trajectory without any loss in energy. The electrons which leave the sample again due to single or multiple scattering effects are called backscattered electrons. They possess energies in the same order of magnitude as the primary beam. Inelastic scattering occurs when primary electrons lose a part of their energy because of the interaction with the atomic shell or the atomic nuclei. They transfer a part of their energy to the electrons in the sample surface resulting in the emission of secondary electrons. These secondary electrons typically exhibit energies in the range of 10-50 eV and are rather "slow" with low kinetic energies. Therefore, the ones escaping from the specimen and collected by the detector are generated close to the surface (5 to 50 nm) thus leading to the possibility of probing the sample surface. The aforementioned backscattered electrons can also be used to image the sample surface providing a good material contrast. However, this mode is less surface sensitive since the penetration depth of the backscattered electrons is in the range of some 100 nm.

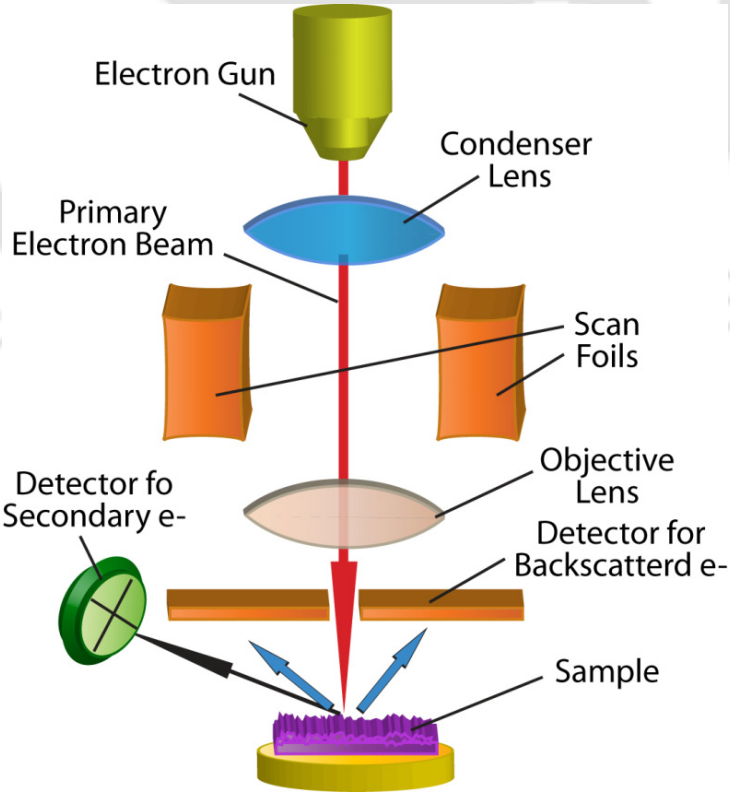

Figure 2.8: Schematic representation of working scheme of a typical SEM.

TH-1322_10612101

The setup of a typical SEM can be seen in Figure 2.8. It consists of an electron gun equipped with a filament cathode to create the electron beam. Similar to TEM, the electron source can either be a heated tungsten filament, a LaB_6 cathode or a field emission cathode. The beam is then focused by one or two condenser lenses. An objective lens projects the beam onto the sample surface and scan coils are used to deflect the beam making it possible to record the image of the specimen in a raster fashion.

(c) Field Emission Scanning Electron Microscopy

The field emission scanning electron microscopy (FESEM) is one of the most widely used imaging tools. It was one of the first surface analysis instruments that approached near-atomic resolution. A field-emission cathode in the electron gun of a scanning electron microscope provides narrower probing beams at low as well as high electron energy, resulting in both improved spatial resolution and minimized sample charging and damage.

Figure 2.9: Field emission scanning electron microscopy (FESEM) (Model: Sigma-Zeiss, Germany).

The field emitted electrons travel along the field lines and produce bright and dark patches on the fluorescent screen giving a one-to-one correspondence with the crystal planes of the hemispherical emitter. The emission current varies strongly with the local work

TH-1322_10612101

function in accordance with the Fowler-Nordheim equation [19]; hence, the FESEM image displays the projected work function map of the emitter surface. The closely packed faces have higher work functions than atomically rough regions and thus they show up in the image as dark spots on the brighter background. In short, the work function anisotropy of the crystal planes is mapped onto the screen as intensity variations. The magnification is given by the ratio $M=L/R$, where R is the tip apex radius and L is the tip-screen distance. Linear magnifications of about 10^5 to 10^6 are attained. The spatial resolution of this technique is of the order of 2 nm and is limited by the momentum of the emitted electrons parallel to the tip surface, which is of the order of the Fermi velocity of the electron in metal. A Sigma-Zeiss, Germany model equipment used in this thesis work and the photo graph of that one has shown in Figure 2.9.

2.3 Spectroscopic Characterization Techniques

2.3.1 Ultra Violet-Visible Spectroscopy

Ultra-Violet Visible spectroscopy (UV-Vis) is used to determine the absorption coefficients and optical band-gaps of materials at visible and ultra-violet wavelengths. This technique allows the quantification of the energy gap between the ground state of an electron and the next lowest state. This is identified as the wavelength at which absorption starts, known as absorption onset. The absorption coefficient, which is a measure of the amount of light that is absorbed by a material at a particular frequency, can also be quantified.

The energy required to promote an electron to the next available energy state depends on what type of bonding the electron is involved in inside the molecule. UV-Vis uses a light in the wavelength range of approximately 200 - 1000 nm, or 1.2-6.2 eV. This energy will excite electrons involved in π bonding into anti-bonding orbitals (π^*), and will also excite n-electrons, which are electrons in non-bonding molecular orbitals, into σ^* and π^* anti-bonding orbitals, but is not large enough to excite electrons from σ orbitals. The absorption spectra of a sample can unveil details of the material species that it contains the energy gap between the materials HOMO and LUMO, and the quantity of material species in the sample.

TH-1322_10612101

The equipment used in the experiments involved in this thesis was a Shimadzu UV-3101PC spectrophotometer, which is a typical example of a commercially available spectrometer shown in Figure 2.10.

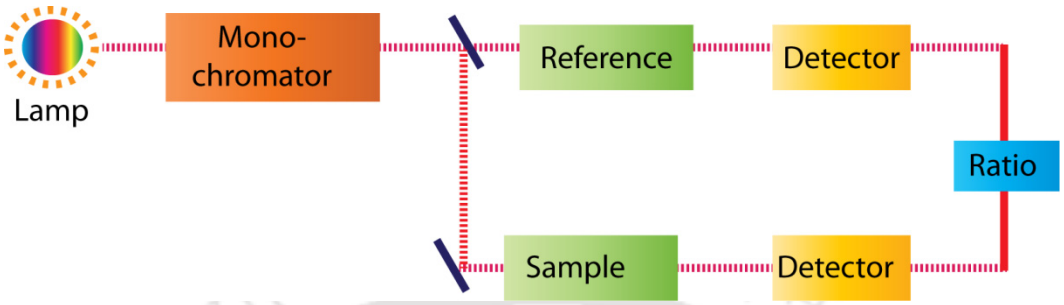

Figure 2.10: Working mechanism of UV-Vis. spectrophotometer.

2.3.2 Fourier transform infrared spectroscopy

Fourier Transform Infrared Spectroscopy (FTIR), the preferred method of infrared spectroscopy. In infrared spectroscopy, IR radiation is passed through a sample. Some of the infrared radiation is absorbed by the sample and some of it is passed through (transmitted). The resulting spectrum represents the molecular absorption and transmission, creating a molecular fingerprint of the sample with absorption/ transmission peaks which correspond to the frequencies of vibrations between the bonds of the atoms making up the material. Because each different material is a unique combination of atoms, no two compounds produce the exact same infrared spectrum. Therefore, infrared spectroscopy can result in a positive identification (qualitative analysis) of every different kind of material. In addition, the amplitude of the peak in the spectrum is a direct indication of the amount of material present. Generally, this spectroscopy is useful to identify the unknown materials in a composite, to determine the quality or consistency of a sample and to determine the amount of components in a mixture. The brief details of working mechanism and spectral analysis were documented in reference [20]. The photograph of FTIR taken from our lab is shown in Figure 2.11.

TH-1322_10612101

Figure 2.11: Photograph of FTIR spectroscopy used in this work.

2.3.3 X-ray diffraction Technique

The technique of X-ray diffraction is a very powerful technique that allows for the interpretation of the atomic structure of crystalline materials. A beam of electromagnetic radiation of wavelength 0.1-100 Å is directed at a sample, which diffracts the beam at an angle determined by the separation of the sample's atomic spacing and the wavelength of the incoming radiation. The angle and intensity of the diffracted beam can be detected using either a point or area detector and the structure of the sample can then be inferred from the recorded data.

The Bragg condition describes the criteria for a diffraction pattern that arises from the constructive interference caused by the scattering of x-rays from an ordered crystal. It is equivalent to the Laue condition and is characterized by the Bragg equation,

$$n\lambda = 2d\sin(\theta) \qquad \text{---------- (2.3)}$$

where d is the lattice spacing, θ is the angle of incidence of the radiation with respect to the crystal planes, of wavelength λ and n is the order of diffraction.

TH-1322_10612101

From the x-ray line profiles that are produced from the data it is possible to extract the 'particle' or 'domain' sizes of the materials under examination. Atypical crystal can be made up of many smaller grains, and particularly in the case of a nano-wire sample in which each wire is on the order of tens of nanometers in height and width and a few microns in length, some of these dimensions can be extracted from the data. For a nano-wire it might not be expected that the entire length forms one perfect crystal and rather that there are discontinuities along the long axis. For grain sizes from around 0.1 μm and below the diffraction patterns are very sensitive to the grain sizes and line broadening begins to occur, where the extent of the broadening is given by

$$B = \frac{K\lambda}{D\cos(\theta)} \qquad \text{---------- (2.4)}$$

Where B is the full width half maximum (FWHM) broadening of the diffraction line in radians, and D is the diameter of the crystal particle. K is the Scherrer's constant and is often cited in the literature to be 0.9, and was in fact derived in Scherrer's original paper to be $K = 2[2\ ln(2)/\pi]^{1/2} \approx 0.93$ [21]. Owing to the huge data bank available from JCPDS Powder Diffraction Files (PDF) covering practically every phase of every known material, crystal phase of the sample is identified from the peak positions of the diffractogram. Homogeneous or uniform elastic strain in the (*hkl*) direction can also be calculated from the shift in the diffraction peak positions, and the d_{hkl} spacing of the unstrained crystal. In this thesis, all the XRD data were taken from a commercially available model TTRAX-III, RIGAKU-2500 using a Cu $K_{\alpha 1}$ (λ=1.5406Å) radiation with nickel filter. Figure 2.12 represents the schematic illustration and photograph of commercial XRD unit.

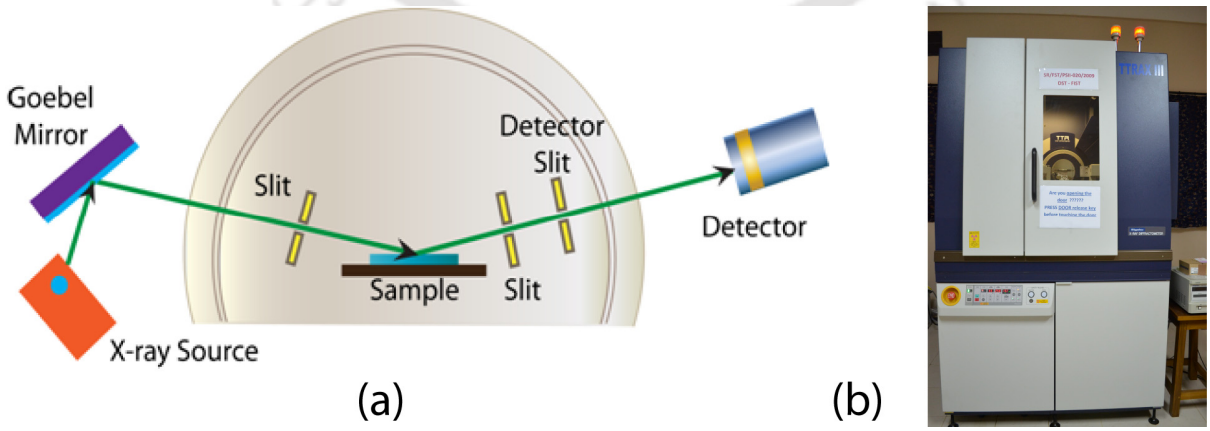

Figure 2.12: (**a**) Schematic representation of a typical XRD and (**b**) photograph of commercial XRD of model TTRAX-III, RIGAKU-2500.

TH-1322_10612101

2.4 Electrical Characterization Techniques

2.4.1 Probe Station

The model CRX-EM-HF Lake-Shore is a dynamic cryogen-free electromagnet-based micro manipulated probe station of four probes (see in figure), which finds application in nondestructive testing of devices on full and partial wafers up to 25 mm (~1 inch) in diameter has been used in this work. This platform is used to measure electro-optical, electrical, parametric, DC, high *Z*, RF and microwave properties of test devices and materials. A varied selection of cables, probes, sample holders and options help configure the CRX-EM-HF to satisfy specific measurement applications. However, out of all features, only electrical and parametric analyses have been used extensively in this work.

Figure 2.13: CRX-EM-HF-Lake Shore cryogen-free electromagnet-based probe station.

2.4.2 Semiconductor Characterization System

Keithley-4200 Semiconductor Characterization System (SCS) has been chosen for device parameter extraction. It is a parametric analyzer with a Windows-XP based software

TH-1322_10612101

environment which provides for measurement of DC *I-V*, *C-V*, and pulse characterization and stress-measurement/reliability testing of semiconductor devices and test structures. It performs lab grade DC and pulse device characterization, real-time plotting, and analysis with high precision and sub-femto amp resolution. It includes a complete embedded PC with windows operating system and mass storage. Doping profile extractions, high and low *k* dielectric characterization, flash memory testing, pulse testing of devices, high power MOSFET/BJT characterization, interface charge trap characterization and solar cell/photovoltaic device characterization can be performed using it.

Figure 2.14: Keithley-4200 Semiconductor Characterization System.

2.5 References

[1] L.A. Majewski, M. Grell, S.D. Ogier, J. Veres, A novel gate insulator for flexible electronics, Org. Electron., 4 (2003) 27-32.

[2] L.A. Majewski, R. Schroeder, M. Voigt, M. Grell, High performance organic transistors on cheap, commercial substrates, J. Phys. D. Appl. Phys., 37 (2004) 3367-3372.

TH-1322_10612101

[3] M. Gedda, N.V.V. Subbarao, S.M. Obaidulla, D.K. Goswami, High carrier mobility of CoPc wires based field-effect transistors using bi-layer gate dielectric, Aip Adv., 3 (2013) 112123-112127.

[4] F. Yang, M. Shtein, S.R. Forrest, Morphology control and material mixing by high-temperature organic vapor-phase deposition and its application to thin-film solar cells, J. Appl. Phys., 98 (2005) 014906-014910.

[5] C. Rolin, S. Steudel, K. Myny, D. Cheyns, S. Verlaak, J. Genoe, P. Heremans, Pentacene devices and logic gates fabricated by organic vapor phase deposition, Appl. Phys. Lett., 89 (2006) 203502-203503.

[6] G. Binnig, C.F. Quate, C. Gerber, Atomic Force Microscope, Phys. Rev. Lett., 56 (1986) 930-933.

[7] B. Bhushan, Handbook of Nanotechnology, Springer, Heidelberg, 2004.

[8] F. Moreno-Herrero, P.J. de Pablo, R. Fernandez-Sanchez, J. Colchero, J. Gomez-Herrero, A.M. Baro, Scanning force microscopy jumping and tapping modes in liquids, Appl. Phys. Lett., 81 (2002) 2620-2622.

[9] Y. Martin, C.C. Williams, H.K. Wickramasinghe, Atomic Force Microscope Force Mapping and Profiling on a Sub 100-a Scale, J. Appl. Phys., 61 (1987) 4723-4729.

[10] T.R. Albrecht, P. Grutter, D. Horne, D. Rugar, Frequency-Modulation Detection Using High-Q Cantilevers for Enhanced Force Microscope Sensitivity, J. Appl. Phys., 69 (1991) 668-673.

[11] Q. Zhong, D. Inniss, K. Kjoller, V.B. Elings, Fractured Polymer Silica Fiber Surface Studied by Tapping Mode Atomic-Force Microscopy, Surf. Sci., 290 (1993) L688-L692.

[12] P.K. Hansma, J.P. Cleveland, M. Radmacher, D.A. Walters, P.E. Hillner, M. Bezanilla, M. Fritz, D. Vie, H.G. Hansma, C.B. Prater, J. Massie, L. Fukunaga, J. Gurley, V. Elings, Tapping Mode Atomic-Force Microscopy in Liquids, Appl. Phys. Lett., 64 (1994) 1738-1740.

[13] C.A.J. Putman, K.O. Vanderwerf, B.G. Degrooth, N.F. Vanhulst, J. Greve, Tapping Mode Atomic-Force Microscopy in Liquid, Appl. Phys. Lett., 64 (1994) 2454-2456.

[14] M. Knoll, E. Ruska, Beitrag zur geometrischen Elektronenoptik. II, Ann. Phys., 404 (1932) 641-661.

TH-1322_10612101

[15] M. Knoll, E. Ruska, Beitrag zur geometrischen Elektronenoptik. I, Ann. Phys., 404 (1932) 607-640.

[16] D.B. Williams, C.B. Carter, Transmission Electron Microscopy, Plenum Press, New York, 1996.

[17] D. Brandon, W.D. Kaplan, Microstructural Characterization of Materials, Wiley, London, 2001.

[18] J.P. Le Poole, New electron microscope with continuously variable magnification, Philips techn, Rdsch, 1947.

[19] R.H. Fowler, L. Nordheim, Electron Emission in Intense Electric Fields, Proceedings of the Royal Society of London. Series A, 119 (1928) 173-181.

[20] P. Griffiths, J.A. de Hasseth, Fourier Transform Infrared Spectrometry, 2nd ed., Wiley-Blackwell2007.

[21] B.E. Warren, X-ray Diffraction, Addison-Wesley1969.

TH-1322_10612101

Chapter III

Kinetic Roughening in CoPc Thin Film Growth

3.1 Introduction

Organic thin films are used as active channels for the fabrication of thin film based organic field effect transistors. Therefore, the performances of the devices are found to crucially depend on the structure and morphologies of the films [1-3]. Detailed understanding of growth mechanisms in organic thin-film deposition is crucial for tailoring growth morphologies, which in turn determine the electrical properties of the resulting films. In past decades, several theoretical models were established to relate the thin film growth mechanism to a set of scaling exponents [4-6]. The exponents describe the variation of roughness and lateral correlation lengths as film grows with time. These models were tested for a large number of inorganic systems and few organic systems [7-9]. Growth of organic thin films is more complex than inorganic film growth due to anisotropy and very week intermolecular interaction (van der Waals type). Therefore, most of the organic film growth mechanisms showed anomalous scaling behavior supporting a different universality class, which needs further theoretical support. Therefore, knowledge on the growth of organic thin film is still far from complete.

In this chapter, we report the growth mechanism of cobalt (II) phthalocyanine (CoPc) thin films growth on SiO_2 surfaces (i.e. native SiO_2 on Si(100) substrate). CoPc has emerged as an important molecule because of its high thermal and chemical stability [10, 11]. However, CoPc was found to form islands at the early stage of the growth [10, 12]. As growth continues, the films become rough and no smooth film formation is observed. Therefore, the charge transport through the film is extremely poor to consider for fabrication of devices

TH-1322_10612101

based on CoPc thin-film active channel. However, the enhancement of carrier mobility is observed recently for the devices based on CoPc wires where better molecular alignment has been observed [13]. Due to poor film quality of CoPc, these molecules were attracted less attention for the fabrication of thin film based organic electronic devices and require detail understanding of the growth mechanism in order to have control over the growth at molecular level. In this work, we have studied the growth of CoPc films on SiO_2 surfaces and explored the possible reasons for such morphology formation. The scaling exponents were calculated to identify the roughening mechanism in the growth. The formation of rough films has been explained by the presence of an additional activation barrier for an adatom when crossing a step edge [14, 15], which is usually called Ehrlich-Schwöbelbarrier (ESB). The ESB found to vary as the film grows [16, 17]. In organic thin-film growth, a wide variety of growth morphologies are observed because of the complexity in their building blocks and inter-molecular interactions. Recently, the formation of mounds in organic thin-film growth [18-21], as well as theoretical efforts to understand the effect of ESB on the growth [21, 22], has been reported. In contrast to the epitaxial growth of inorganic materials, organic film growth is expected to be more complex because molecules are anisotropic and have internal degrees of freedom that open novel diffusion channels accompanied by changes in the molecular conformation. In those cases, ESB restrict the downward diffusion of the molecules and the deposited molecules on the steps piles up to form islands. As a result, the film becomes rough. Monomer bulk diffusion also was reported to be the origin of the kinetic roughening for the growth of polymer film by vapor deposition technique [7]. We have observed that the local diffusion of the CoPc molecules even at the elevated substrate temperature of 120°C plays crucial role for kinetic roughening of CoPc film on SiO_2 surfaces. In this case, the diffusion activation energies along the vertical and lateral growth direction were found to be similar. This indicates the favorable diffusion condition for CoPc molecules for upward and lateral diffusion.

In addition to SiO_2 substrates, to study the influence of the substrate surface on the growth of CoPc films, we have also used mica (001) ($KAl_2(AlSi_3O_{10})(OH)_2$–$^2{}_1$M muscovite) surfaces, which are atomically flat reconstructed surfaces. Freshly cleaved mica (001) surfaces form a pseudohexagonal structure. We have used these surfaces for the growth of

TH-1322_10612101

CoPc molecules. Due to three-fold symmetry in the mica surface lattice, it is expected to observe uniform diffusion of the CoPc molecule on these surfaces. We have studied the kinetics of the growth of CoPc microstructures on these surfaces.

3.2 Experimental Details

The powdered CoPc molecules were purchased from Alfa Aesar (USA) used as source material. Thin film growth was carried out in a custom designed organic molecular beam deposition apparatus with four Knudsen cells. The detailed design of this equipment can be found in section 2.1 of *chapter II*. We have used SiO_2 and freshly cleaved mica (001) as substrate surface for the growth of CoPc molecules. In order to clean SiO_2 substrates, initially the substrates were treated with piranha solution and then sonicated in several cycles with acetone, methanol, de-ionized water and finally purged with argon gas to remove residual contaminants. In the case of mica substrate, the cleaning of top surface has been carried out by cleaving of topmost few layers of mica with the help of scotch tape. The sublimation temperature of CoPc source powder was fixed at 350ºC. Series of CoPc films were grown with the function of coverage and substrate temperatures. To understand the growth mechanism as a function of film coverage, the deposition times were varied as 1 min, 2 min, 4 min, 6 min and 10 min. In order to study the diffusion of the molecules, we have grown CoPc films at various substrate temperatures, such as 25 ºC, 60 ºC, 120 ºC, 180 ºC and 220 ºC. Chamber pressure was maintained at approximately ~10^{-7} mbar during the growth with the fixed deposition rate ~0.2 Å/sec. The film surface morphology was monitored using an atomic force microscope (AFM) (Agilent 5500-SPM) in tapping mode to avoid any film damages due to tip surface interactions.

3.3 Results and Discussions

3.3.1 Coverage Dependent Growth of CoPc Thin Films

In this section, we describer the morphology evolution of the CoPc films on SiO_2 surfaces with the growth time. A typical atomic force micrograph (AFM) of clean SiO_2 surfaces is shown in Figure 3.1(a). The surface was found to be very smooth with rms

TH-1322_10612101

roughness is 0.3 nm. This is the roughness of native oxide layer formed on Si(100) surface and it is amorphous in nature. Figure 3.1(b–f) are showing the representative AFM images of CoPc films grown at 120°C substrate temperature with 1, 2, 4, 6 and 10 min deposition time, respectively. Formation of CoPc islands are clearly observed for the film with 1 & 2 min deposition time as shown in Figure 3.1(b-c). As the deposition time increases, these islands grow laterally as well as vertically forming percolated structures, which are shown in the subsequent AFM images in Figure 3.1(d–f). However, no uniform film formation is observed even after 10 min deposition of the molecules. Formation of large islands on top of the percolated structures is observed and marked using arrow as shown in Figure 3.1(f).

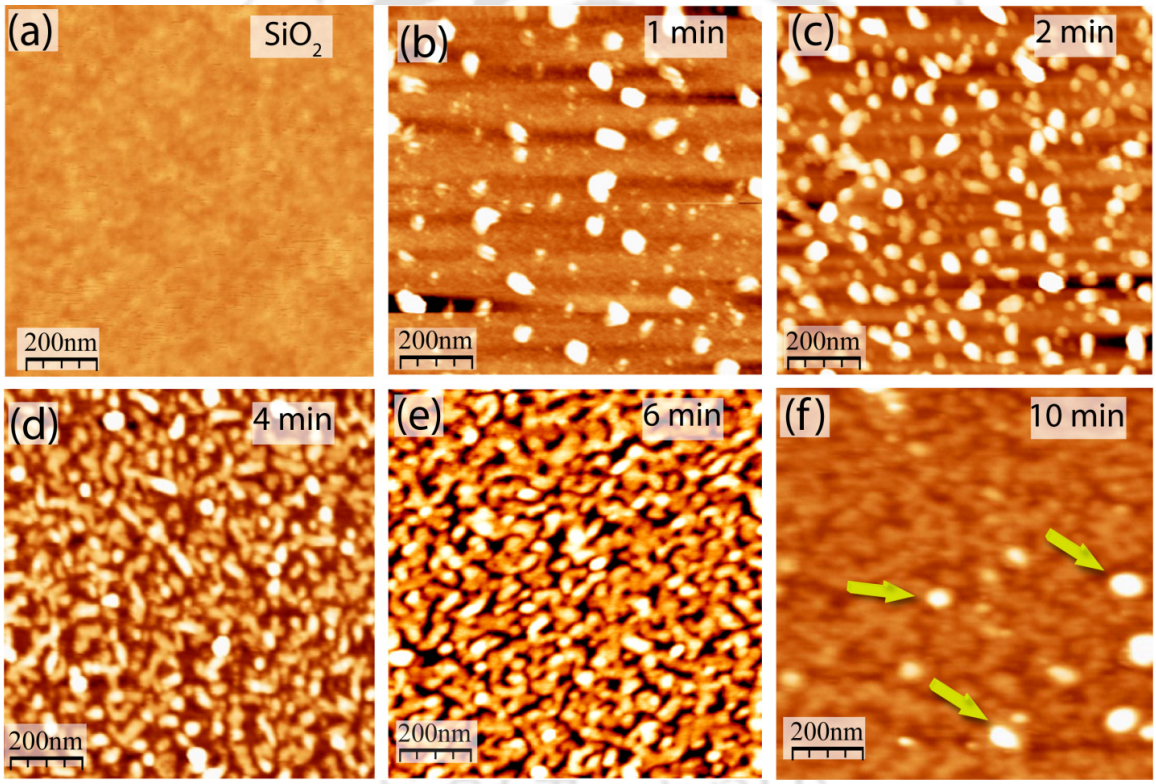

Figure 3.1: Representative AFM images of **(a)** SiO_2 surface and CoPc films grown on SiO_2 surfaces at 120 °C substrate temperature with various deposition times **(b)** 1 min, **(c)** 2 min, **(d)** 4 min, **(e)** 6 min and **(f)** 10 min.

In order to study the dynamic behavior of this growth process, we have calculated the different scaling exponents from the morphology evolution of the films. The variation of local surface slope of the islands during the growth is also studied. These quantities were determined from the height-height correlation function, *G(r,*t*),*which is defined as mean

TH-1322_10612101

square of height difference between two surface positions separated by a distance r for the deposition time t as, $G(r,t) = \left\langle \left[h(r,t) - h(0,t) \right]^2 \right\rangle$ where $h(r,t)$ and $h(0,t)$ are the heights of the surfaces at two different locations separated by a distance r. The bracket signifies an average over all available pairs of points obtained from the AFM images [23-26]. When r is small, the height-height correlation function varies as $G(r,t) = [m(t)r]^{2\alpha}$, with $r \ll \xi(t)$, where, $\xi(t)$ is the characteristic in-plane length scale, α is the roughness scaling exponent and $m(t)$ is the local surface slope of the height profile for small length scale [25, 27]. $m(t)$ was calculated from the fitting of linear portion of log-log plot of $G(r,t)$ vs r as per the equation mentioned earlier. The growth of the CoPc films can be studied by monitoring two parameters, which can describe the island growth. First parameter represents the average size of the island, whereas, the second one represents the average separation between islands. Lateral correlation length, $\xi(\theta)$, is the measure of the length beyond which surface heights are not significantly correlated. For the surfaces with island formation, this length essentially measures the size of the island [28]. Other parameter to characterize surface, the wavelength (λ), it signifies the average separation between islands. λ and ξ must satisfy the relation $\xi \leq \lambda$ as the islands are separated by at least their size. However, when the islands grow next to each other would imply that $\xi = \lambda$ [29]. In case of percolated structures, λ is not well defined. Therefore, we calculated ξ to characterize the CoPc film growth.

Figure 3.2 shows the log-log variation of $G^{1/2}(r,t)$ vs r. In order to determine ξ, we have calculated $G(r,t)$ from AFM images following the procedure described earlier. To avoid sampling induced effect in the $G(r,t)$ calculation from height fluctuations, care has been taken to include many AFM images in the averaging of $G(r,t)$ data. In our analysis we have checked that 6 to 10 AFM images taken from different parts of the sample were enough to give statistically reliable data to obtain $G(r,t)$ plot. An up shift of $G(r,t)$ data as deposition temperature increases, as shown in Figure 3.2, indicates a roughening in the growth process. To monitor the roughening process quantitatively, we measure the interface width $W(t)$ as function of t. Interface width $W(t)$ is essentially the rms roughness of the surface. $W(t)$ (shown by arrow mark in Figure 3.2) is the value of $G^{1/2}(r,t)$ at the first local maximum, as $W(t) = G^{1/2}(\xi/2)$ where ξ marked by an downward arrow, is the position of r at

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the first local minimum of $G^{1/2}(r,t)$ [30]. This definition of interface width is preferable over the large r limit of $G(r,t)$ as artifacts at large length scales can affect AFM data.

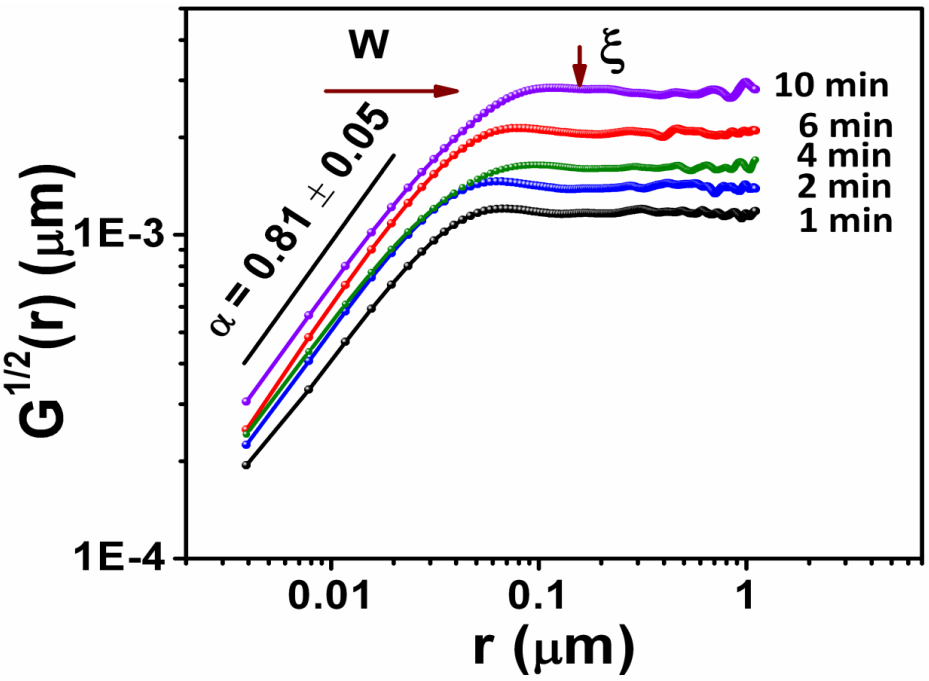

Figure 3.2: Height – height correlation plot with log-log variation of $G^{1/2}(r,t)$ vs r for the films grown at different deposition time intervals 1, 2, 4, 6 and 10 min.

The roughness exponent α was determined from a power fit to the linear part of the log-log plot of $G^{1/2}(r,t)$ vs r. α essentially represents the variation of height fluctuation as deposition time increases. It corresponds to the vertical growth of the film. The average α observed in the growth of CoPc film is 0.81± 0.05.Interface width, $W(t)$ increases following power law as, $W(t) \sim t^{\beta}$ with exponent β = 0.37±0.05. The exponent β characterizes the dynamics of the roughening process and is called growth exponent. The lateral correlation length, $\xi(t)$ increases following power law as, $\xi(t) \sim t^{1/z}$, with $1/z = 0.23 \pm 0.06$. The exponent 1/z is called dynamic exponent. Log-log variations of W and ξ versus t are shown above in Figure 3.3. Figure 3.3(a) shows the increasing nature of W as the film grows with t. This clearly indicates the roughening of the film growth. However, the increasing nature of $\xi$with t, as shown in Figure 3.3(b), indicates the lateral growth of the islands. This confirms that the

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islands grow vertically as well as laterally and the overall film becomes rough with an increased deposition time.

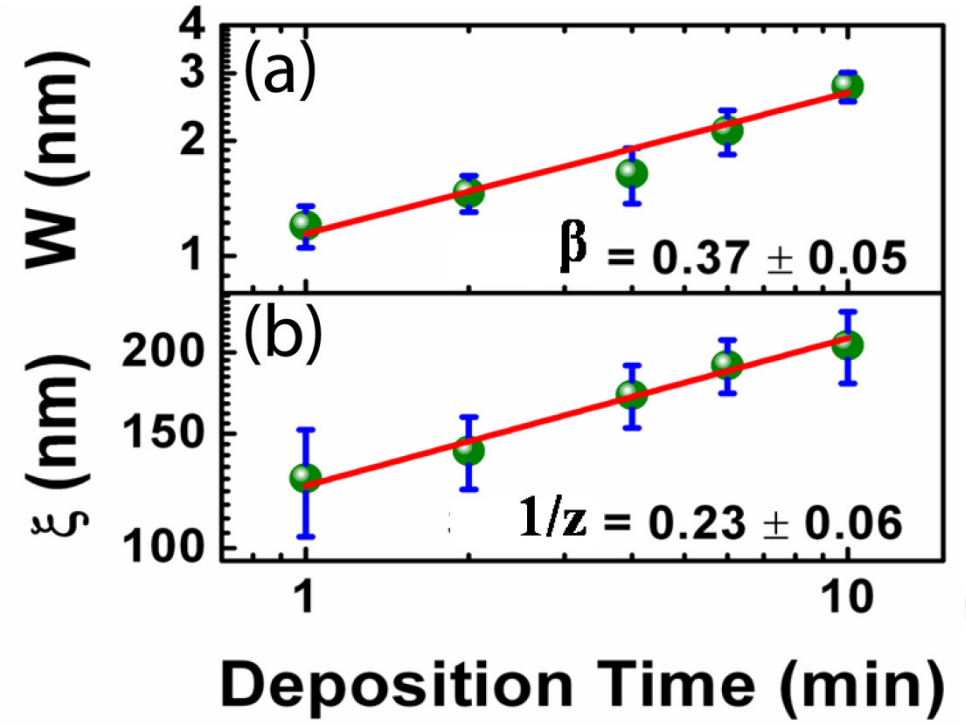

Figure 3.3: Log-log variation of **(a)** interface width (W) and **(b)** lateral correlation length (ξ) with respect to deposition time t. The estimated values of growth exponent, β, and dynamic exponent, $1/z$, also represented.

In order to quantify the dynamics of roughening, we have plotted ξ versus W for all the samples and it is shown in Figure 3.4. From the equations of W versus t and ξ versus t, as described earlier, one can easily derive that $W \sim \xi^{\gamma}$, with the exponent $\gamma = \beta/(1/z) = 1.67 \pm 0.23$, as measured from the linear fit. In this case, the ratio of $\beta = 0.37 \pm 0.05$ and $1/z = 0.23 \pm 0.06$, is 1.61 ± 0.13, which is comparable with the fitted value of γ within the measurement error. Therefore, the competition of lateral and vertical growth can be estimated by the value of $\gamma > 1$ and it is clearly indicating the faster vertical growth that corresponds to the roughening mechanism of the film growth.

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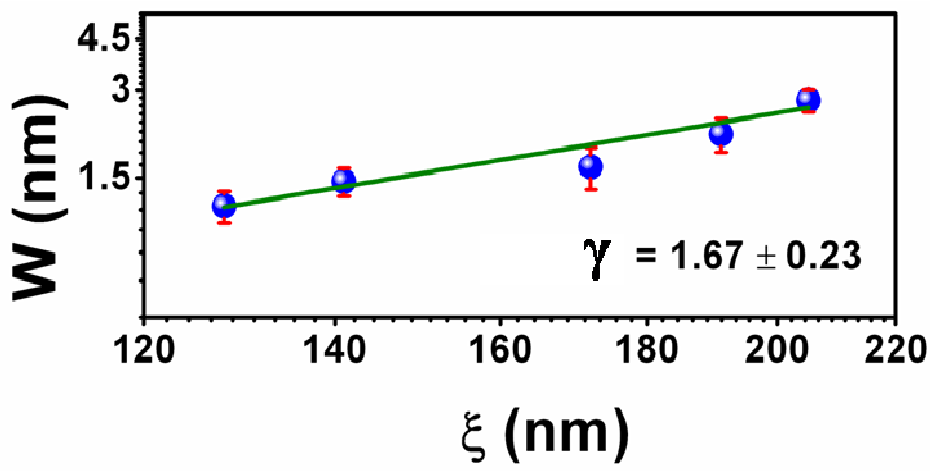

Figure 3.4: Log-log variation of interface width (W) versus lateral correlation length (ξ) calculated from the films grown at various time intervals to quantify the dynamics of the roughening.

The kinetic process that is responsible for different morphology formation is inter-layer mass transfer through diffusion of the molecules [31]. Inter-layer mass transport is decided by the diffusion activation energy along the local surface slope and the extra ESB at the step edge. The higher ESB inhibits step down diffusion process by forming 3D islands. However, 3D islands can also be formed in case of limited diffusion of the molecule by inhibiting growth kinetics. In order to gain knowledge about the diffusion of the molecules, we have varied the growth temperature, which essentially influence the diffusion of the molecules while growing.

3.3.2 Temperature Dependent Growth of CoPc Thin Films

To study the diffusion of CoPc molecules for identifying the origin of the roughening in CoPc films growth on SiO_2 surfaces, we have grown films at different substrate temperatures. Figure 3.5(a–e) show the representative AFM images of CoPc films grown at 25, 60, 120, 180 and 220°C substrate temperatures, respectively. As the substrate temperature increases, the diffusion of the molecules increase leading to the formation of smooth layer and possibly it improves crystalline quality of the films. As a result, the formation of flat

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underline layer together with larger islands on top can be seen at 220°C substrate temperature when diffusion of the molecules is supposed to be higher.

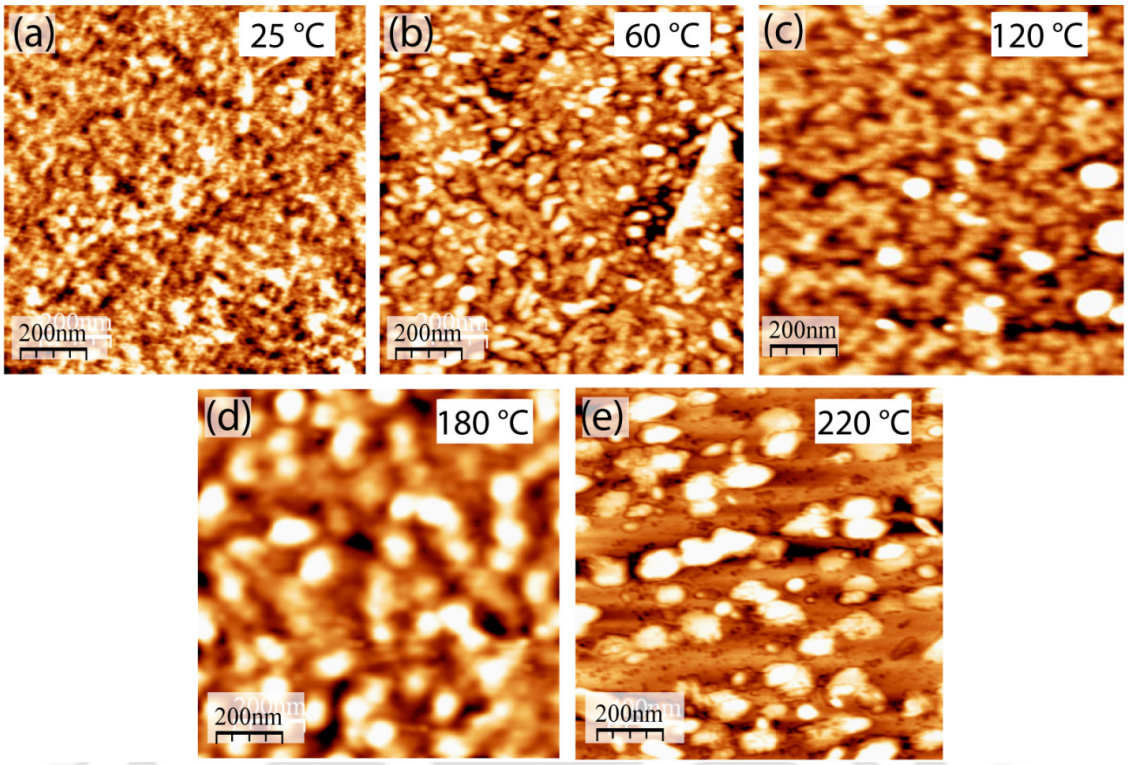

Figure 3.5: AFM topography images of CoPc films grown on SiO_2 surfaces at different substrate temperatures **(a)** 25 °C, **(b)** 60 °C, **(c)** 120 °C, **(d)** 180 °C and **(e)** 220 °C with 10 min deposition time.

To understand the evolution of the film morphology, we have calculated *G(r,t)*. Figure 3.6 shows the variation $G^{1/2}(r,t)$ versus r as before. The average α observed in this case is 0.78 ± 0.04. This is close to the value (0.81 ± 0.05) obtained while coverage of the CoPc were varied. The average value of α obtained from both the cases is 0.79 ± 0.06. With increase of substrate temperature, both interface width and lateral correlation lengths were closely following an Arrhenius behavior as $W, \xi \sim \exp(-E_a / k_B T)$, with surface diffusion activation energy E_a = 0.34 ± 0.03 eV, k_B is Boltzmann constant and T is the substrate temperature, as shown in Figure 3.7(a) and 3.7(b). This is interesting to observe similar activation barrier along vertical and horizontal growth. Activation barriers for W and ξ have been associated with rotational and translational barrier of the molecular diffusion [32]. In this case, they correspond to the diffusion of the molecule along the

TH-1322_10612101

local surface slope and in plane on the terraces, respectively. Therefore, lateral diffusion of the molecule is equally probable to the vertical diffusion of the molecule that contributes to up wards diffusion current of the molecules. However, the upward diffusion current can be purely controlled by ESB if one considers sufficient diffusion of the molecules at a given growth temperature.

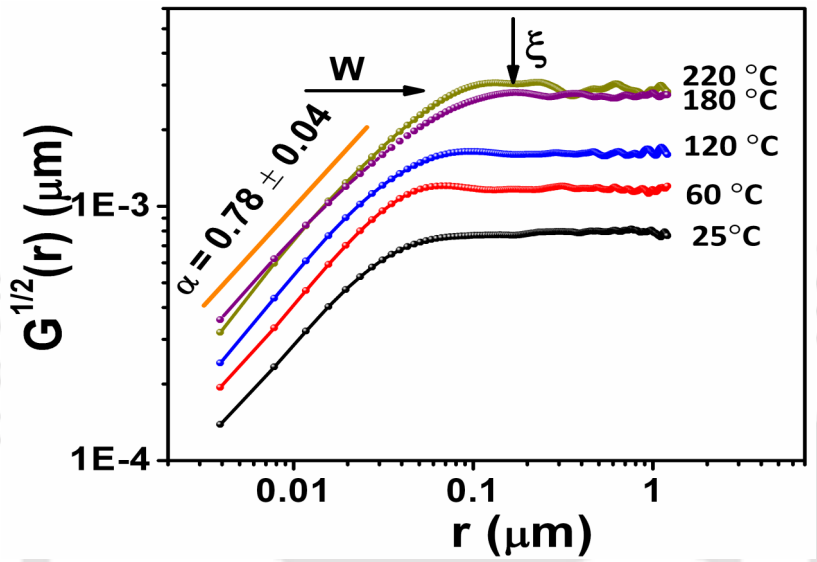

Figure 3.6: Hight-hight correlation plot with log-log variation of $G^{1/2}(r,t)$ vs r for the films with 10 min deposition timegrown at different substrate temperatures 25, 60, 120, 180 and 220 °C.

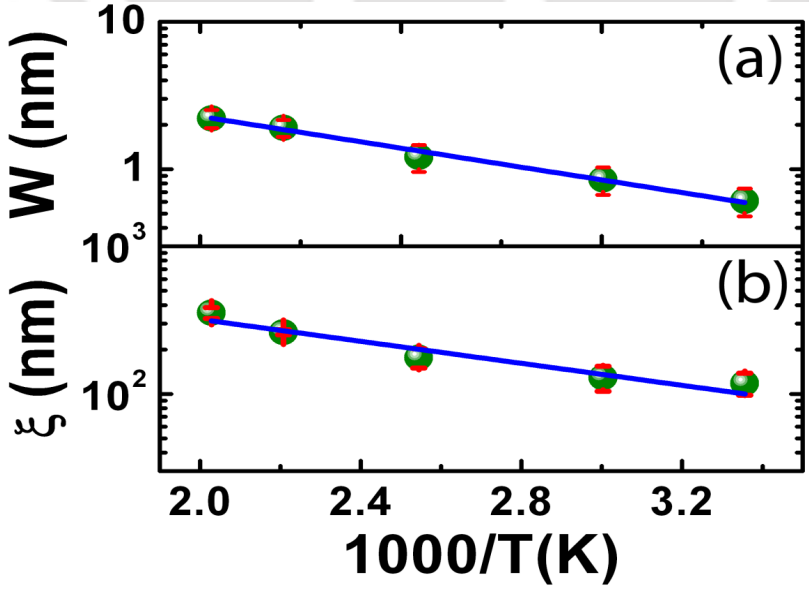

Figure 3.7: Arrhenius behavior of **(a)** interface width (W) and **(b)** lateral correlation length (ξ) with the function of substrate temperature T.

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To understand the detail diffusion process during the growth of CoPc film at 120 °C substrate temperature, we studied the variation of local surface slope, *m(t)*, as the deposition temperature increases. If *m(t)* is independent of the growth time, *t*, then it is said to be stationary growth. In such cases, height-height correlation function coincides for $r << \xi$. Whereas, for non-stationary growth due to limited diffusion of the molecules, the local slope *m(t)* increases with time and an up-shift of $G(r, t)$ can be observed as film thickness increases [27]. This represents island growth as we see for CoPc film. In order to study the growth, several theoretical models are proposed. In non-equilibrium film growth driven by surface diffusion, the growth equation is written as [9],

$$\frac{\partial h}{\partial t} = -\kappa\nabla^4 h + \lambda\nabla^2(\nabla h)^2 + F + \eta(r,t) \qquad \text{---------- (3.1)}$$

with, κ and λ are constants and η is a random fluctuation around the average flux *F* causing roughening. The linear and non-linear parts are decided by the constants and represent the detail growth processes. Linear equation corresponds to the local growth when atoms stick to the nearest kink sites irreversibly. When surface molecule is able to overcome the intermolecular interaction and hops to the next sites represents the intermediate diffusion of the molecules and the growth processes are described by the nonlinear equation [8]. In case of local diffusion, the local surface slope increases with time and can be described as $m(t) = \langle(\nabla h)\rangle^{1/2} = \sqrt{C \ln(t/t_c)}$, where *C* is constant and t_c is transition deposition time to the scaling regime [8, 33].

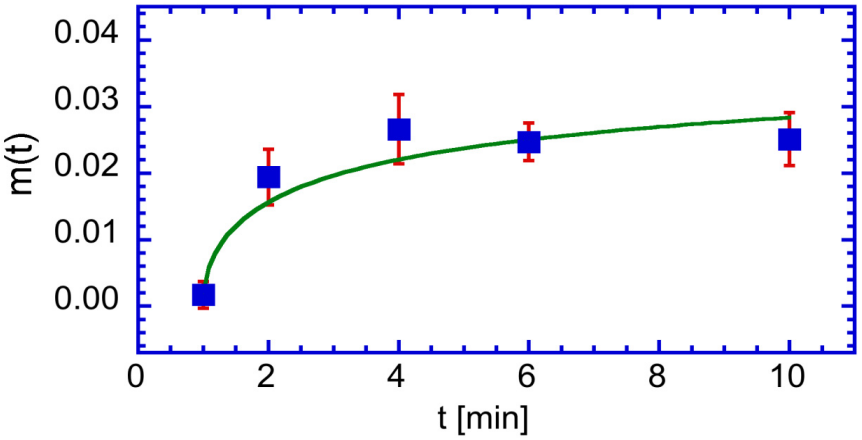

Figure 3.8: Variation of local slope (*m (t)*) with deposition time *t* for the films grown at different deposition time intervals.

TH-1322_10612101

Figure 3.8 shows the plot $m(t)$ versus t and the fit with the equation as described. The value of t_c obtained from the fit is 0.99 min. This indicates that our smallest coverage sample with 1min deposition time is already within the scaling regime. This dependency in local surface slope confirms the local surface diffusion of the molecules. Local surface diffusion apparently causes instability in the growth even at 120 °C substrate temperature. As a result, roughening in the CoPc growth at 120 °C substrate temperature is observed. It is to be noted that continuum growth equation involves only height profiles h and its derivatives, characteristic of the local nature of diffusion.

However, only diffusion model alone cannot explain the growth exponents, which we observed. From the theoretical treatments of non-equilibrium film growth, the predicted scaling exponents are α =2/3 and β =1/5 [34]. However, the linear growth equation predicts α = 1 and β = 1/4 [35]. On the other hand, due to step edge barrier (ESB), the diffusion can also be limited at the step edge and form uniformly sized pyramids with stationary slope. The predicted scaling exponents for ES barrier are α = 1 and β =1/4 [36]. None of these models support the exponents observed for CoPc growth. Actually, an understanding for the kinetic roughening in film growth is still far from complete [8]. Therefore, growth models considering the different issues related to organic film growth may be required to explain the exponents and may be belonging to a different universality class.

3.3.3 Growth of CoPc on mica (001) surfaces

From the last section, it was clear that the formation of islands significantly is influenced by the diffusion of the molecules. In order to study the influence of the substrate surfaces on the growth, we have studied growth of CoPc molecules on mica (001) surfaces as we increase the diffusion of the molecules by a systematic increase in the growth temperature. Freshly cleaved mica (001) surfaces were used for the growth. The bulk structures of mica is monoclinic with lattice constants of a = 5.20 Å, b = 9.03 Å, c = 20.11 Å and β = 95.78º; the easy accessible cleavage plane corresponds to (001) [37]. Figure 3.9 shows 1 µm × 1µm AFM images representing the surface morphology of CoPc films grown at different substrate temperatures, such as 25 °C; 60 °C; 120 °C; 180 °C ; 220 °C, respectively.

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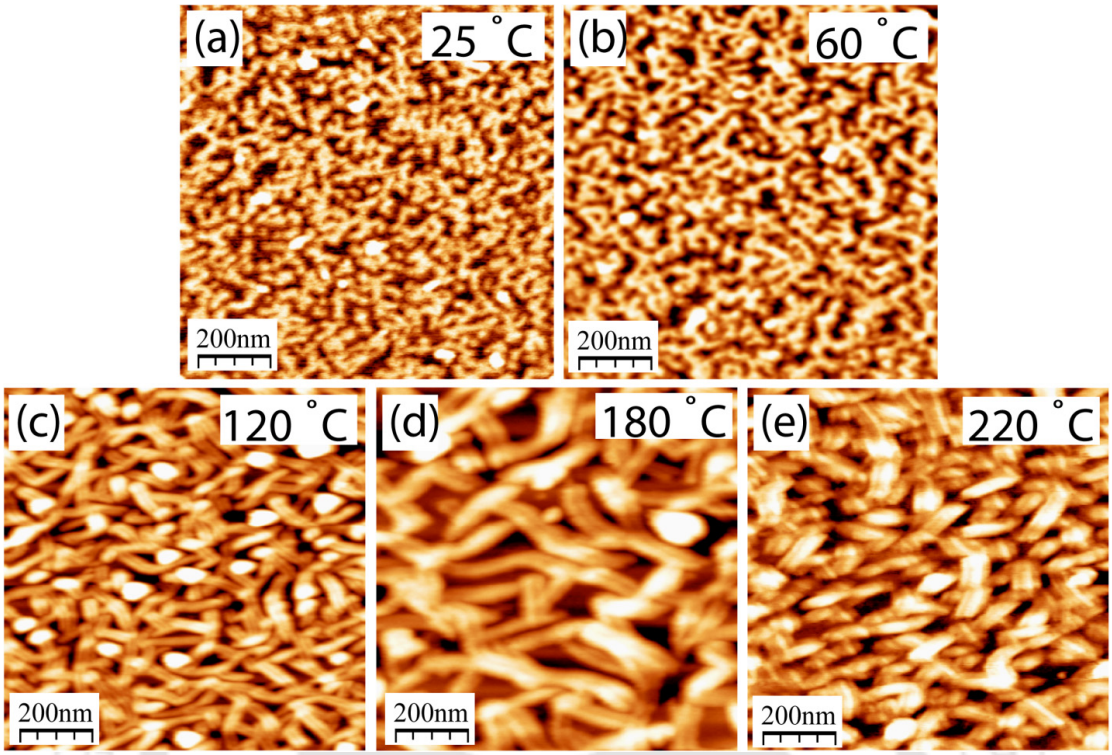

Figure 3.9: 1 μm × 1μm AFM images characterizing the surface morphology of CoPc films on mica at different substrate temperatures: **(a)** 25 °C; **(b)** 60 °C; **(c)** 120 °C; **(d)** 180 °C ; **(e)** 220 °C.

With the increased substrate temperature, the diffusion of the molecules increase leading to formation of long percolated micro structures with possible improvement in crystalline quality. The percolated structure formation starts from initial temperature 25°C onwards. The formation of elongated strips like structures going one over the other forming percolated type structure is observed at higher temperatures (120 °C and 180 °C, see Figure 3.9(c) and 3.9(d)). At very high temperature (220 °C), the distortion of these structures can be seen with reduced length as shown in Figure 3.9(e). This could be due to the instability the film growth arises because of high substrate temperatures. To study the effect of growth temperature on such formation of the films, we have calculated $G(r,t)$ for all the samples. Figure 3.10 shows the variation $G^{1/2}(r,t)$ versus r as earlier. The average α observed in this case is 0.89 ± 0.07. With increase of substrate temperature, both interface width and lateral correlation length are closely following an Arrhenius behavior as $W, \xi \sim \exp(-E_a / k_B T)$, with surface diffusion activation energies obtained as, $E_a(\xi) = 0.07 \pm 0.03$ eV and $E_a(W) = 0.17 \pm 0.04$ eV,

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which are shown in Figure 3.11(a) and 3.11(b). The observation of two different activation energies represents the dissimilar diffusion of the molecules along the lateral and the vertical growth.

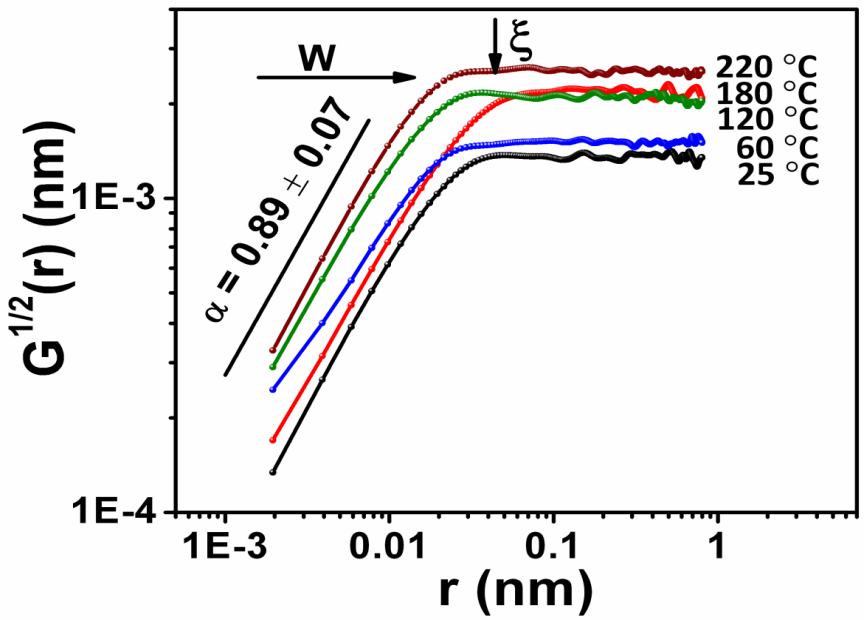

Figure 3.10: Height-height correlation plot with log-log variation of $G^{1/2}(r,t)$ vs r for the films grown at different substrate temperatures 25, 60, 120, 180 and 220 °C.

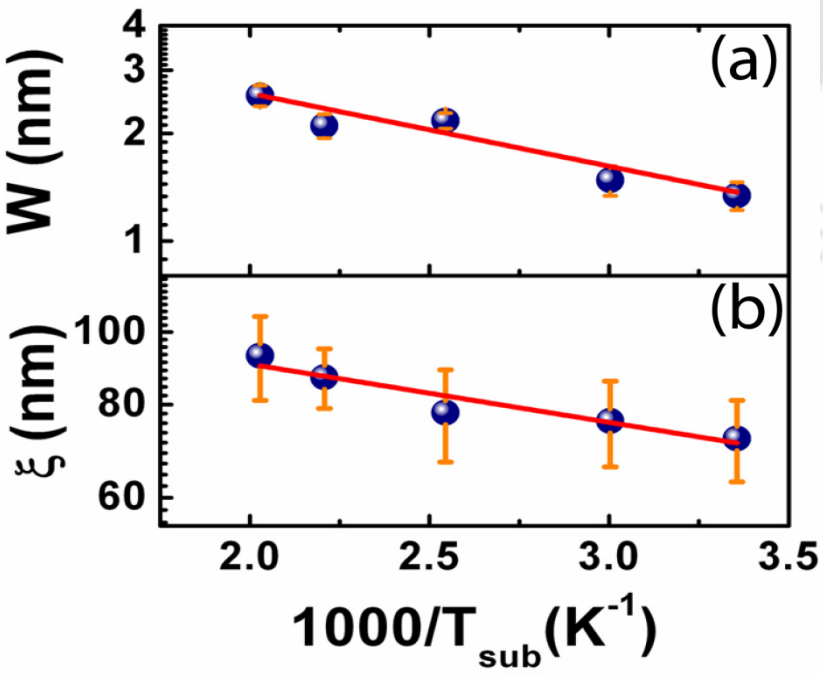

Figure 3.11: Arrhenius behavior of **(a)** interface width (W) and **(b)** lateral correlation length (ξ) with the function of deposition temperature T.

Lower surface diffusion activation energy for lateral growth possibly results percolated type structures. This clearly confirms that the diffusion of the molecules significantly influenced by the properties of substrate surfaces.

3.4 Conclusions

In conclusions, we report the origin of roughening in the growth of CoPc film on SiO_2 surfaces. We have observed equal diffusion activation energy for lateral and vertical diffusion of the molecules. However, it was found that local surface diffusion, which exists even at 120 °C growth temperatures, plays crucial role for roughening in CoPc film growth. In order to understand the effect of substrate temperature on the diffusion of CoPc molecules, we have studied the growth of CoPc molecules on the atomically cleaned mica (001) surfaces. The growth kinetics of CoPc molecule on mica has been discussed. The reported scaling exponents obtained from the growth of CoPc molecules on SiO_2 surfaces confirms that the growth belongs to a different universality class. Therefore, the understanding the growth of organic molecules is far from complete.

3.5 References

[1] M. Shtein, J. Mapel, J.B. Benziger, S.R. Forrest, Effects of film morphology and gate dielectric surface preparation on the electrical characteristics of organic-vapor-phase-deposited pentacene thin-film transistors, Appl. Phys. Lett., 81 (2002) 268-270.

[2] F. Liu, C. Wang, J.K. Baral, L. Zhang, J.J. Watkins, A.L. Briseno, T.P. Russell, Relating Chemical Structure to Device Performance via Morphology Control in Diketopyrrolopyrrole-Based Low Band Gap Polymers, J. Am. Chem. Soc., 135 (2013) 19248-19259.

[3] A.A. Virkar, S. Mannsfeld, Z. Bao, N. Stingelin, Organic semiconductor growth and morphology considerations for organic thin-film transistors, Adv. Mater., 22 (2010) 3857-3875.

[4] A.L.B.a.a.H.E. Stanley, Fractal Concepts in Surface Growth, Cambridge University Press, Cambridge, England 1995.

TH-1322_10612101

[5] P. Chatraphorn, Z. Toroczkai, S. Das Sarma, Epitaxial mounding in limited-mobility models of surface growth, Phys. Rev. B., 64 (2001) 205407-205423.

[6] G. Lengel, R.J. Phaneuf, E.D. Williams, S. Das Sarma, W. Beard, F.G. Johnson, Nonuniversality in mound formation during semiconductor growth, Phys. Rev. B., 60 (1999) 8469-8472.

[7] Y.P. Zhao, J.B. Fortin, G. Bonvallet, G.C. Wang, T.M. Lu, Kinetic roughening in polymer film growth by vapor deposition, Phys. Rev. Lett., 85 (2000) 3229-3232.

[8] J.H. Jeffries, J. Zuo, M.M. Craig, Instability of Kinetic Roughening in Sputter-Deposition Growth of Pt on Glass, Phys. Rev. Lett., 76 (1996) 4931-4934.

[9] Z. Lai, S. Das Sarma, Kinetic growth with surface relaxation: Continuum versus atomistic models, Phys. Rev. Lett., 66 (1991) 2348-2351.

[10] H.S. Soliman, A.M.A. El-Barry, N.M. Khosifan, M.M. El Nahass, Structural and electrical properties of thermally evaporated cobalt phthalocyanine (CoPc) thin films, Euro. Phys. J. Appl. Phys., 37 (2007) 1-9.

[11] S.J. Qiu, H.L. Chu, J. Zhang, Y.N. Qi, L.X. Sun, F. Xu, Heat capacities and thermodynamic properties of CoPc and CoTMPP, J. Therm. Anal. Calorim., 91 (2008) 841-848.

[12] B.E. Schuster, T.V. Basova, V.A. Plyashkevich, H. Peisert, T. Chasse, Effects of temperature on structural and morphological features of CoPc and CoPcF16 thin films, Thin Solid Films, 518 (2010) 7161-7166.

[13] M. Gedda, N.V.V. Subbarao, S.M. Obaidulla, D.K. Goswami, High carrier mobility of CoPc wires based field-effect transistors using bi-layer gate dielectric, Aip Adv., 3 (2013) 112123-7.

[14] G. Ehrlich, F.G. Hudda, Atomic View of Surface Self-Diffusion - Tungsten on Tungsten, J. Chem. Phys., 44 (1966) 1039-1049.

[15] Schwoebe.Rl, E.J. Shipsey, Step Motion on Crystal Surfaces, J. Appl. Phys., 37 (1966) 3682-3686.

[16] X.N. Zhang, E. Barrena, D. Goswami, D.G. de Oteyza, C. Weis, H. Dosch, Evidence for a Layer-Dependent Ehrlich-Schwobel Barrier in Organic Thin Film Growth, Phys. Rev. Lett., 103 (2009) 136101-4.

TH-1322_10612101

[17] E. Barrena, X.N. Zhang, D.G. de Oteyza, H. Dosch, Transition from layer-by-layer to rapid roughening in the growth of DIP on SiO2, Surf. Sci., 601 (2007) 2420-2425.

[18] F.J.M.Z. Heringdorf, M.C. Reuter, R.M. Tromp, Growth dynamics of pentacene thin films, Nature, 412 (2001) 517-520.

[19] L. Kilian, E. Umbach, M. Sokolowski, Molecular beam epitaxy of organic films investigated by high resolution low energy electron diffraction (SPA-LEED): 3,4,9,10-perylenetetracarboxylicacid-dianhydride (PTCDA) on Ag(111), Surf. Sci., 573 (2004) 359-378.

[20] S. Zorba, Y. Shapir, Y.L. Gao, Fractal-mound growth of pentacene thin films, Phys. Rev. B., 74 (2006) 245410-5.

[21] J.E. Goose, E.L. First, P. Clancy, Nature of step-edge barriers for small organic molecules, Phys. Rev. B., 81 (2010) 205310-20.

[22] M. Fendrich, J. Krug, Ehrlich-Schwoebel effect for organic molecules: Direct calculation of the step-edge barrier using empirical potentials, Phys. Rev. B., 76 (2007) 121302-3.

[23] A.-L. Barabási, H.E. Stanley, Fractal Concepts in Surface Growth, Cambridge University Press, Cambridge, 1995.

[24] J. Lapujoulade, The roughening of metal surfaces, Surf. Sci. Reports. 20 (1994) 191-249.

[25] M. Pelliccione, T.-M. Lu, Evolution of thin film morphology: modeling and simulation, Springer-Verlag, New York, 2008.

[26] Y. Zhao, G.-C. Wang, T.-M. Lu, Characteriztion of Amorphus and Crystalline Rough Surface: Principles and Application, Academic Press, London, 2001.

[27] J.H. Jeffries, J.-K. Zuo, M.M. Craig, Instability of Kinetic Roughening in Sputter-Deposition Growth of Pt on Glass, Phys. Rev. Lett., 76 (1996) 4931-4934.

[28] M. Pelliccione, T. Karabacak, C. Gaire, G.-C. Wang, T.-M. Lu, Mound formation in surface growth under shadowing, Phys. Rev. B., 74 (2006) 125420-125410.

[29] J.-K. Zuo, J.F. Wendelken, Evolution of Mound Morphology in Reversible Homoepitaxy on Cu(100), Phys. Rev. Lett., 78 (1997) 2791-2794.

[30] J. Kim, D.G. Cahill, R.S. Averback, Surface morphology of Ge(111) during etching by keV ions, Phys. Rev. B., 67 (2003) 045404-6.

TH-1322_10612101

[31] D. Zhong, M. Hirtz, W. Wang, R. Dou, L. Chi, H. Fuchs, Kinetics of island formation in organic film growth, Phys. Rev. B., 77 (2008) 113404-4.

[32] D. Tsamouras, G. Palasantzas, Temperature dependence of the growth front roughening of oligomer films, Appl. Phys. Lett., 80 (2002) 4528-4530.

[33] J.G. Amar, P.M. Lam, F. Family, Groove instabilities in surface growth with diffusion, Phys. Rev. E., 47 (1993) 3242-3245.

[34] Z. Lai, S. Das Sarma, Kinetic growth with surface relaxation: Continuum versus atomistic models, Phys. Rev. Lett., 66 (1991) 2348-2351.

[35] D.E. Wolf, J. Villain, Growth with Surface-Diffusion, Euro. phys. Lett., 13 (1990) 389-394.

[36] M. Siegert, M. Plischke, Slope Selection and Coarsening in Molecular-Beam Epitaxy, Phys. Rev. Lett., 73 (1994) 1517-1520.

[37] A. Lopezotero, Hot Wall Epitaxy, Thin Solid Films, 49 (1978) 3-57.

TH-1322_10612101

Chapter IV

CoPc microstructures based OFETs with higher carrier mobility

4.1 Introduction

Organic semiconductors are advantageous in general because of their facile and large-scale synthesis, solution processability, molecular and electronic tunability by fictionalization [1, 2]. One-dimensional (1D) organic nanostructures, such as nanowires, nanotubes, nanoribbons, and nanofibers prepared via self-assembly from conjugated small molecules or conjugated polymers constitute the next-generation materials for a vast array of electronic applications [3, 4]. They are promising materials for a multitude of applications including vapor sensors [5, 6], phototransistors [7, 8], solar cells [9], nanoscale lasers [10], memory elements [11], miniaturization of devices [12], and as the active semiconductor elements for organic field-effect transistors (OFETs) [13, 14]. The advances in molecular design and synthesis have made it possible to tune the molecular structures and properties of organic semiconductors to meet the technological requirements for fabricating practical devices. Especially, organic field-effect transistors (OFETs) have great potential in the wide range of applications such as flexible electronics [15], radio frequency identification (RFID) tags [16]. It is well known that the performance of the organic semiconductor is governed by how molecules or polymer chains assemble in the solid state [17, 18]. Because organic molecules in 1D nanowires self-assemble into highly organized single-crystalline 1D structures, they are ideal for fundamental studies. Moreover, these are model systems for elucidating transport mechanisms [4, 19], structure-property relationships [20], and for understanding intrinsic transport phenomena [21].

TH-1322_10612101

Studies on aromatic molecules have shown that self-assembly through strong π–π interactions can lead to the formation of one-dimensional nanostructures preferred for organic field-effect transistors (OFETs), since this packing theoretically results in high mobilities in devices [22]. This phenomenon is reported to be the result of increased overlap between the electronic wave functions of neighboring molecules in the stack [22]. Recent reports are demonstrating that the strong overlap in electronic wave functions leads to an increase in bandwidth and this directly correlates to electrical conductivity in the coherent transport regime [23-25]. OFETs with active channels of this kind of aromatic molecules are generally exploited to enhance carrier mobility.

The field-effect carrier mobility (μ_{FE}) of OFETs not only depends on the organic semiconductors and their molecular arrangement within the active channel of the device but also on the gate dielectric that controls the charge flow through the channel. Charge density in the active channel is largely confined to the first few monolayers at the dielectric-semiconductor interfaces [26-28]. Therefore, the mobility at this region is highest. As a result, a better capacitive coupling between active channel and the gate dielectric is expected to enhance charge carrier mobility of the devices. In order to achieve this, a proper selection of gate dielectric materials with specific device design is essential. Inorganic oxides such as SiO_2, Al_2O_3, TiO_2, Ta_2O_5 are frequently utilized high-*k* gate dielectric materials for OFETs fabrication. However, most of the high dielectric constant materials suffer from expensive deposition method and poor film quality requiring relatively thick films to reduce gate leakage current. As a result, the capacitance decreases and the operating voltage increase significantly.

Al_2O_3 is a promising material because of suitable low-cost deposition process through the conversion of Al by anodization [29-31]. Al_2O_3 also exhibits excellent insulating properties (dielectric constant ~ 8 – 10) with an electrical breakdown field of > 8 MV/cm [32]. However, anodized Al_2O_3 films are in general very rough to grow semiconductor channel on top of the film. Nevertheless, the leakage current is also very high. In such cases, multi-component dielectric system combining inorganic and organic dielectric films showed better performances of the devices [33, 34]. Organic nature of interface between active channel and dielectric layer may provide a more efficient capacitive coupling with the

TH-1322_10612101

channel, perhaps because of better matching in surface energy of these materials [29, 35]. Such high performance OFETs are demonstrated using polymer-treated inorganic dielectrics [33, 35]. Polyvinyl alcohol (PVA), poly (methyl methacrylate) (PMMA), poly(4-vinylphenol) (PVP) [36-38] are frequently utilized as organic component of dielectric polymer for OFETs fabrication.

In this chapter, we described the growth of CoPc microwires using organic vapor phase deposition (OVPD) method. Tested with several substrate surfaces to achieve long CoPc microwires, which can be used in wires based OFET fabrication as an active channel. CoPc microwires grown on different surfaces were characterized by means of FESEM, TEM, XRD, UV–Vis., Fourier transform infrared spectroscopy (FTIR). Fabrication processing steps and obtained device parameters were elucidated.

4.2 Experimental Details

4.2.1 Growth of CoPc Microstructures

Organic vapor phase deposition (OVPD) technique has been used for the growth of CoPc microstructures on different substrates. The details of this system are described in section 2.3 of *chapter II*, which is essentially a single zone furnace. The powdered *β*-cobalt phthalocyanine molecules were procured from Alfa Aesar (USA) and used as source material. Initially CoPc powder was loaded in a ceramic boat, which was placed into a quartz tube inside a horizontal tube furnace (as shown in Figure 2.3). The furnace temperature was kept at 400°C. To avoid the CoPc oxidation and to carry CoPc molecule, a flowing argon atmosphere was employed during the vapor deposition process. The argon gas flow rate was kept at 100 sccm (standard cubic centimeters per minute). Various substrates including glass, mica, silicon, and metal coated glasses were put along the downstream side of the flowing argon to collect the molecules. CoPc molecules form nano to micron size wire like structures. The microstructure synthesis have been done on different substrates at various substrate positions of 25 cm, 23 cm and 21 cm from the centre of furnace, which provides the substrate temperatures of 130 °C, 200 °C and 270 °C respectively.

TH-1322_10612101

4.2.2 Fabrication Process of CoPc wires based OFETs

For CoPc micro-wires based OFET fabrication, initially aluminum gate contact of thickness of 300 nm was deposited on pre-cleaned glass surfaces. A part of Al film was then anodized to form Al_2O_3 layer to be used as a gate dielectric layer. Anodized Al_2O_3 surfaces were found to be very rough with rms roughness is about 8.3 nm (concluded from AFM and profilometer data). In order to achieve a smooth interface between gate dielectric and organic channel, we have spin-coated the Al_2O_3 surfaces with 45 nm PVA (M_W~125,000) layer of 5wt%. In this process, the rms roughness of the dielectric surface reduced to 0.2 nm.

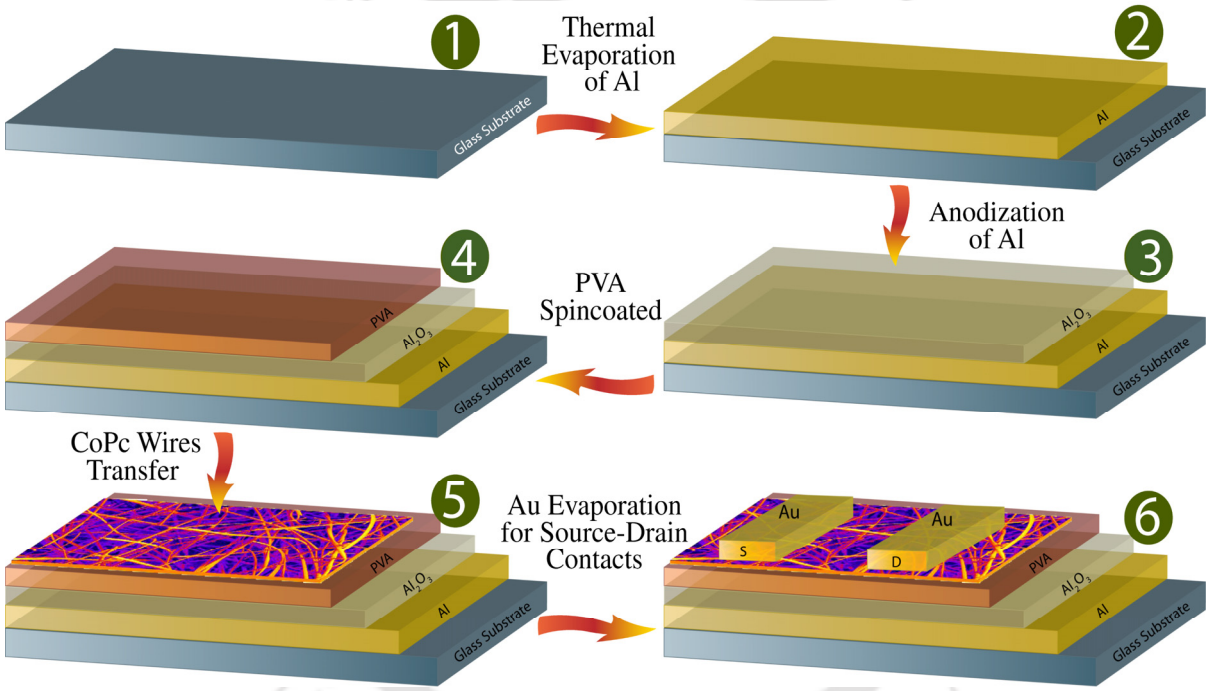

Figure 4.1: Illustration of different steps of the fabrication of CoPc microwires based OFET.

This is essentially due to lower surface free energy of PVA (~0.045 J/m^2) than Al_2O_3 (~1.7 J/m^2). The stack of Al_2O_3 and PVA layers were used as gate dielectric layer for the OFET fabrications. The relatively longer CoPc molecular wires obtained by tuning the growth process, were chosen for the fabrication and were separated from the substrates and dispersed in ethanol solvent. These micro-wires then transferred on to pre-prepared organic-inorganic hybrid dielectric surfaces. Gold (Au) electrodes were deposited by thermal evaporation with shadow-mask of 50 µm channel length and 1mm channel width. Figure 4.1 shows the

TH-1322_10612101

detailed fabrication steps of OFET. The output and transfer characteristics curves for the multi-wires OFETs were taken in air using Keithley-4200 SCS parameter analyzer and a probe station.

4.3 Results and Discussions

4.3.1 CoPc Microstructure Growth on Various Substrates

I. FESEM Results:

In this section, we summarize the FESEM results of CoPc wire like microstructures grown on different substrates. For the fabrication of OFETs based on the CoPc wires as active channel, we need to improve the length of the wires as long as possible such that a better connection between source and drain through the wires can be made. In order to achieve this, we have tested with several substrates and different growth temperatures to optimize the growth of CoPc 1D structure formation.

CoPc Growth on Glass Substrate: Figure 4.2 shows the FESEM images of thin strip like microstructures grown on ordinary glass substrates with different substrate temperatures, such as 130 °C, 200 °C and 270 °C respectively. In all the cases, growth time was fixed to 10 min with argon gas flow rate of 100 sccm. We have observed the formation of CoPc thin 1D strips with average size is about 1 μm at 130 °C growth temperature. As the growth temperature increases, strips grow to form CoPc 2D sheets together with long and thick strips as shown in Figure 4.2 (b &c). However, the maximum length of these sheet observed is about 3 μm at 270 °C growth temperature.

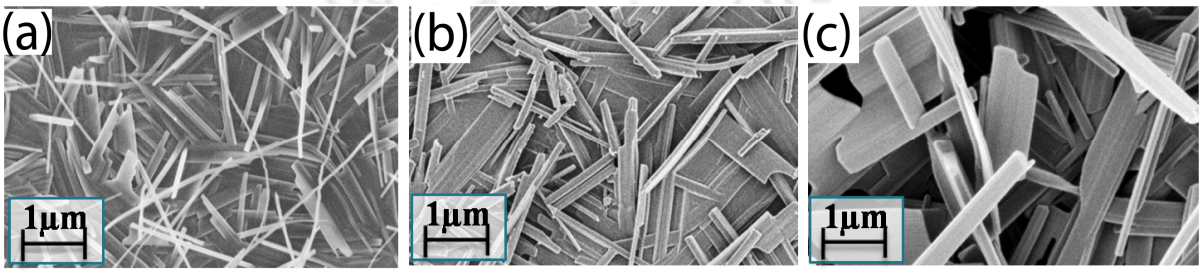

Figure 4.2: FESEM images of CoPc microstructures on glass substrates grown at substrate temperatures (**a**) 130 °C, (**b**) 200 °C and (**c**) 270 °C.

CoPc Growth on Mica Substrate: In the process of finding appropriate 1D structures of CoPc for OFETs fabrication, we have used muscovite mica ($KAl_2(AlSi_3)O_{10}(OH)_2$) as another substrate of choice, since the freshly cleaved mica form atomically cleaned mica (001) surfaces. In such case, the diffusion of the molecules will be influenced by the surface structures of the mica (001), which is essentially pseudo hexagonal 2D surface lattice [39]. Though, mica (001) surface has three fold symmetry, no structure formation is observed which follow the symmetry of the underlying mica surfaces. Moreover, we have observed the formation of unidirectional CoPc long strips, which are attached with the substrates as shown in Figure 4.3. As the growth temperature increases, the length of the strips are also increased unidirectional (Figure 4.3 (a-c)). This clearly confirms that the formation of these microstructures has less dependency on the surface structures. However, mica surfaces found to influence the growth of the CoPc to form very long strips. Since, the strips grow onto the surface and are attached with the substrates; it would be difficult to transfer the strips from mica substrates to the active channel of the devices.

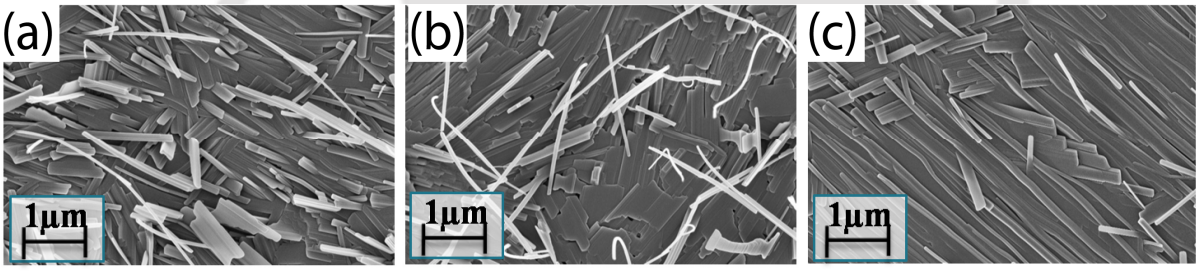

Figure 4.3: FESEM images of CoPc microstructures on mica substrate grown at various substrate temperatures (**a**) 130 °C, (**b**) 200 °C and (**c**) 270 °C.

CoPc Growth on Metallic Surfaces: In order to explore the effect of metal surface on the growth of CoPc microstructures, we have used metal films as the surface of interest. We have grown about 100 – 120 nm thick Ag, Al and Au films on glass substrates and were used for the growth of CoPc films. Representative FESEM images of the CoPc films grown at 130 °C, 200 °C and 270 °C substrate temperature are shown in Figure 4.4. The growth time for all the samples was kept 10 min. Figure 4.4 (a – c) show the morphology of CoPc films grown on Al/glass surfaces. Formation of micron size strips was observed. As the growth temperature increased, the size of the strips increase and are tending to form flat 2D CoPc strips as observed in case of glass substrates. However, the size of the strips is much smaller than the

TH-1322_10612101

2D strips observed in case of glass. In case of Ag/glass surfaces, we observed needle like structures formation. Sub-micron size crystal formation is observed as the growth temperature increased to 270 °C as shown in Figure 4.4 (d – f). In case of Au/glass surfaces, CoPc islands formation is observed on a wetting layer. As the growth temperature increases, the islands increase their sizes (see Figure 4.2(c)).

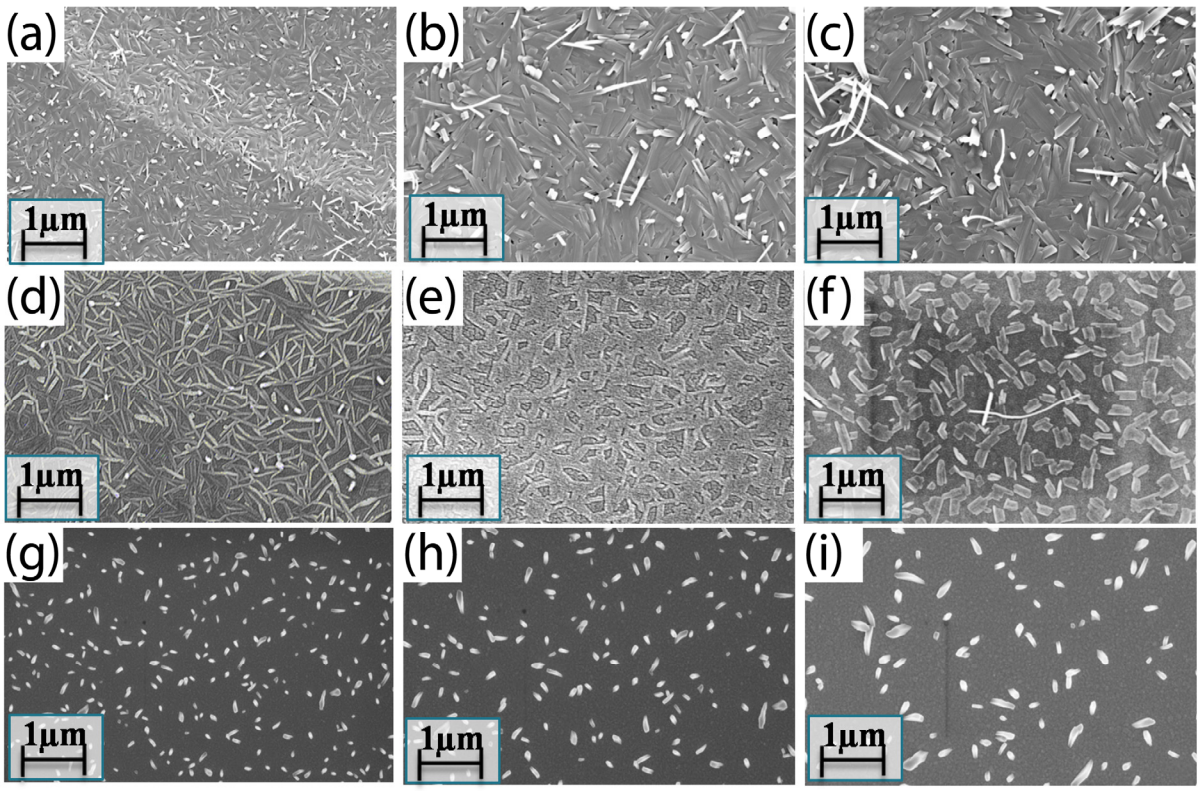

Figure 4.4: Representative FESEM images of CoPc microstructures on **(a-c)** Ag/Glass, **(d-f)** Al/Glass and **(g-i)** Au/Glass surfaces at different substrate temperatures 130 °C, 200 °C and 270 °C respectively.

Metal nanoparticles are reported to show highly catalytic properties and Au nanoparticles were exhaustively used to initiate organic wires growth [40-46]. We have also tested with Au nanoparticle to initiate CoPc wire formation. Au nanoparticles were grown in glass substrates using thermal evaporation followed by rapid thermal annealing. Typical FESEM image is shown in Figure 4.5(a). The formation of CoPc nanowires is observed as shown in Figure 4.6(b–c). However, the average size of the wires is about 300 nm. None of these microstructures grown on metal surfaces are suitable for the fabrication of CoPc wire based

TH-1322_10612101

OFETs. Since in our methodology, we require to transfer the wires to channel. These wires are relatively smaller in size.

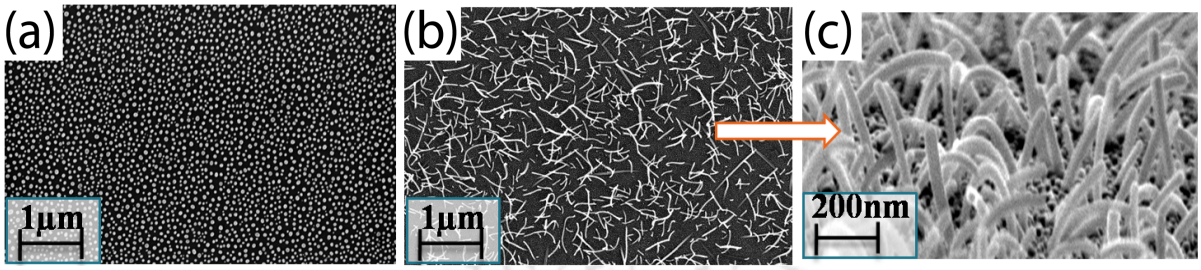

Figure 4.5: (a) FESEM image of Au nano-particle template, **(b)** Nanowires growth on template and its zoomed image **(c)**.

Micron wire Growth on SiO_2 Substrate:

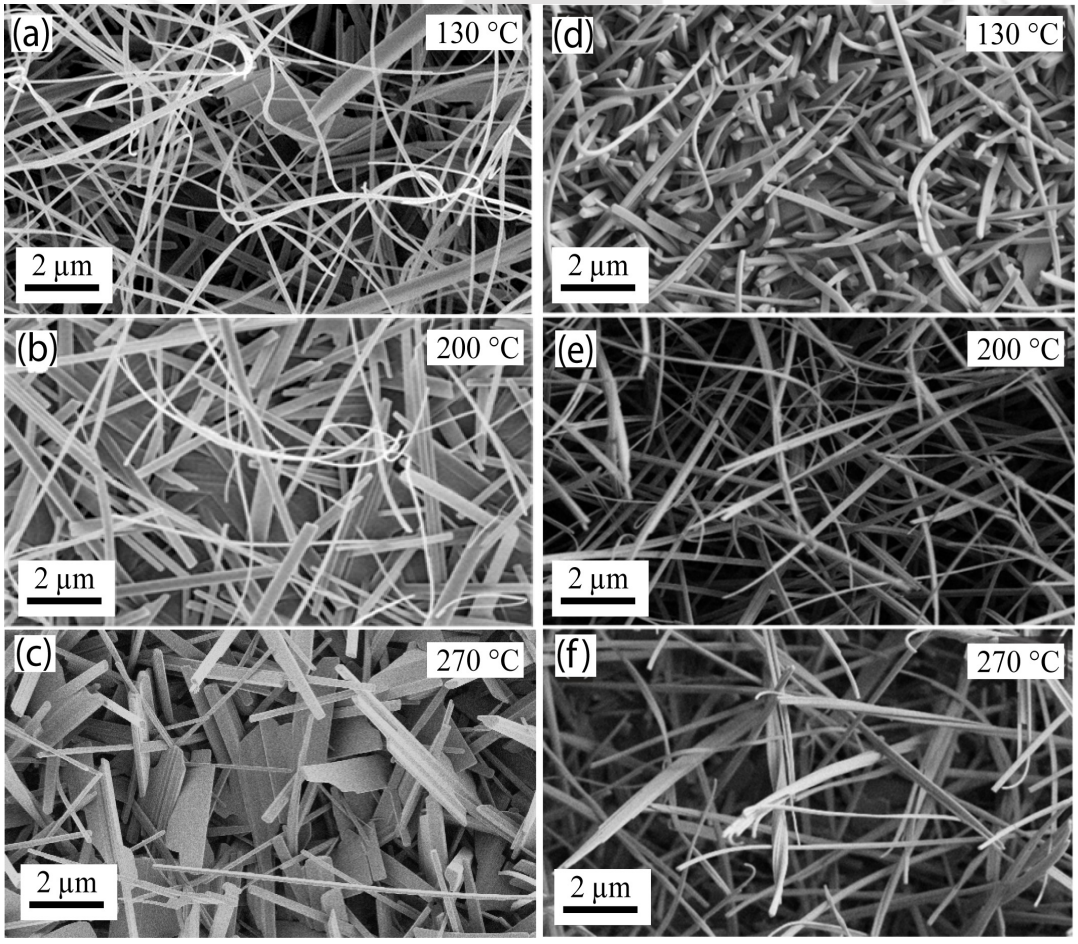

Figure 4.6: FESEM images of micron wires grown on SiO_2 substrate with different synthesis time 10 min (**a-c**) and 20 min (**d-f**) at various substrate temperatures 130 °C, 200 °C and 270°C.

In addition to glass and metal surfaces, we have used SiO_2 surfaces for the growth of CoPc microstructures. The substrate temperatures were varied to 130, 200 and 270 °C during the growth and CoPc molecules were grown for 10 min and 20 min. FESEM images of CoPc microstructures grown on SiO_2 surfaces are shown in Figure 4.6. We have observed the formation of nanostrips and nanowires at 130 °C substrate temperature for 10 min deposition time as shown in Figure 4.6(a). As the substrate temperature increases to 200 °C and 270 °C, we observed the formation of big crystals, microstripes and microwires, which are shown in the Figure 4.6(b) & (c). The typical length of the microstrips at 20 min growth time are about ~100 µm which are not clearly visible in the FESEM images shown in Figure 4.6(f) as only a section of the strips are exposed to the surface. These microstrips were removed from the substrates into ethanol solution and then transferred on the active channel of OFETs fabricated on glass substrates. Figure 4.7(a) shows the optical micrograph of the CoPc strips as active channel of the devices. The source and drain contacts are clearly visible. The dimension of active channel is about 50 µm. The average length of the micro strips is confirmed by optical micrograph as shown in Figure 4.7(b).

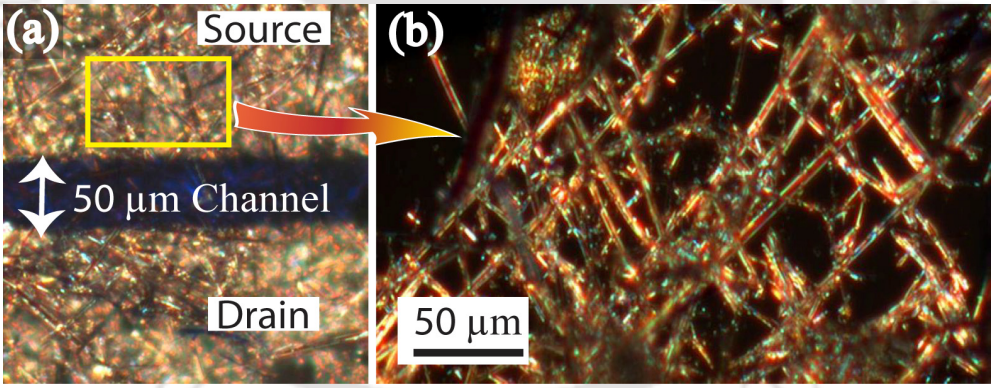

Figure 4.7: (a) Optical micrograph of CoPc wire based transistor with representation of source – drain electrodes and channel; **(b)** Magnified image CoPc wires in the channel.

II. FT-IR Results:

CoPc molecules were thermally evaporated in 400°C to grow the microstrips which were used for the fabrication of OFETs. In order to confirm that there was no decomposition of the molecules, we have analyzed the strips using FT-IR and compared the results with the source materials. Figure 4.8 shows the FT-IR results taken from the micro strips and the powder

TH-1322_10612101

CoPc molecules. The five characteristic IR bands observed in case of CoPc at 731, 782, 877, 915, and 1290 cm^{-1} are similar in both the cases, indicating that CoPc molecules do not undergo any decomposition or other chemical reactions during the growth process.

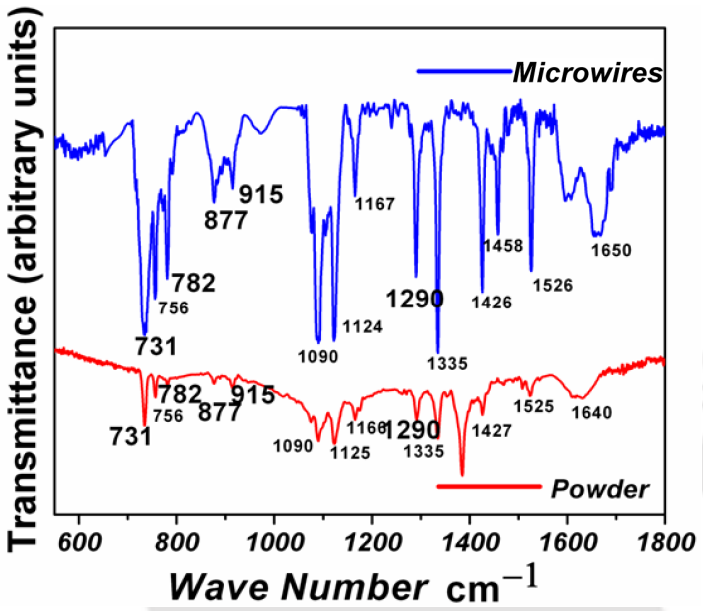

Figure 4.8: FTIR spectrogram of plain CoPc wires and its source powder with representing of significant peak positions.

III. UV-Vis. Results:

In order to study the optical response of the CoPc microstrips, we have performed UV-Vis. absorption study on the strips. The absorption spectra are given in the Figure 4.9. The tensile stress produced due to the constraint imposed by the substrate temperature, may affect the electronic structure and thereby result in new absorption spectra. The optical band gap for the as-deposited nanostrips with 20 min growth time was found to increase with substrate temperature. *Anderson et al.* have reported that the central metal atom of the phthalocyanines influences the optical absorption spectrum. *Yamashita et al.* [47] have observed that the *Q*-band absorption of CoPc shifts towards longer wavelengths when deposition temperatures are increased. It is the significance of α-phase and for CoPc nanowires, this phase shows two absorption maxima at the *Q*-band with wavelengths of 625 nm and 705 nm. The two maxima peaks are separated by 82 nm as shown in Figure 4.9. As the substrate temperature increased

to 270 ºC, the higher energy peak was shifted slightly. For the increase in substrate temperature from 130 ºC to 270 ºC, the observed peaks located at 705 nm remains there without any shift, but the peak at 625 nm has shifted. This result is due to phase change activity [48], and is in good agreement with the earlier observations of spectral change from α to β-phase by heat-treatment at a temperature of approximately about 300 °C [49]. With increasing substrate temperature, the *B*-band is slightly red-shifted. This is attributed to the formation of large-size microwires at higher growth temperature.

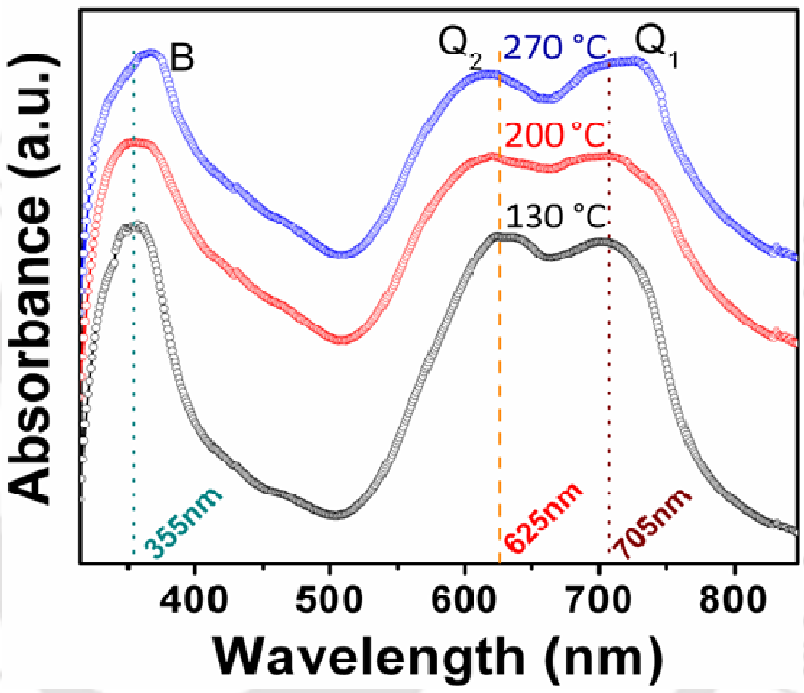

Figure 4.9: Absorption spectra for Cobalt phthalocyanine microwires at various substrate temperatures 130 °C, 200 °C and 270 °C with its band positions.

IV. XRD & TEM Results:

To reveal the crystal structure of CoPc microstructures, the XRD and TEM measurements were performed. Figure 4.10 shows the XRD pattern of powdered CoPc and its microwires deposited on SiO_2 substrate. All of the diffraction peaks can be indexed as tetragonal α-phase CoPc structure, which agree well with the literatures [50, 51]. By comparing both the XRD patterns, it is clear that existence of a single intense peak clearly

represents the highly order molecular arrangement within the wires. The diffraction peaks were indexed with tetragonal α-phase of CoPc structure. It is apparent from the analysis that out-of-plane orientation of the wires grown on the substrate is along [100] crystallographic direction. Our results agree well with the existing literatures describing preferential growth direction of these molecules in thin films [50, 52]. The first order peak corresponds to an inter planer spacing of 1.23 nm. Corresponding second and third order diffractions peaks are also observed as shown in the inset of Figure 4.10. This clearly revealed the single crystal nature of the wires.

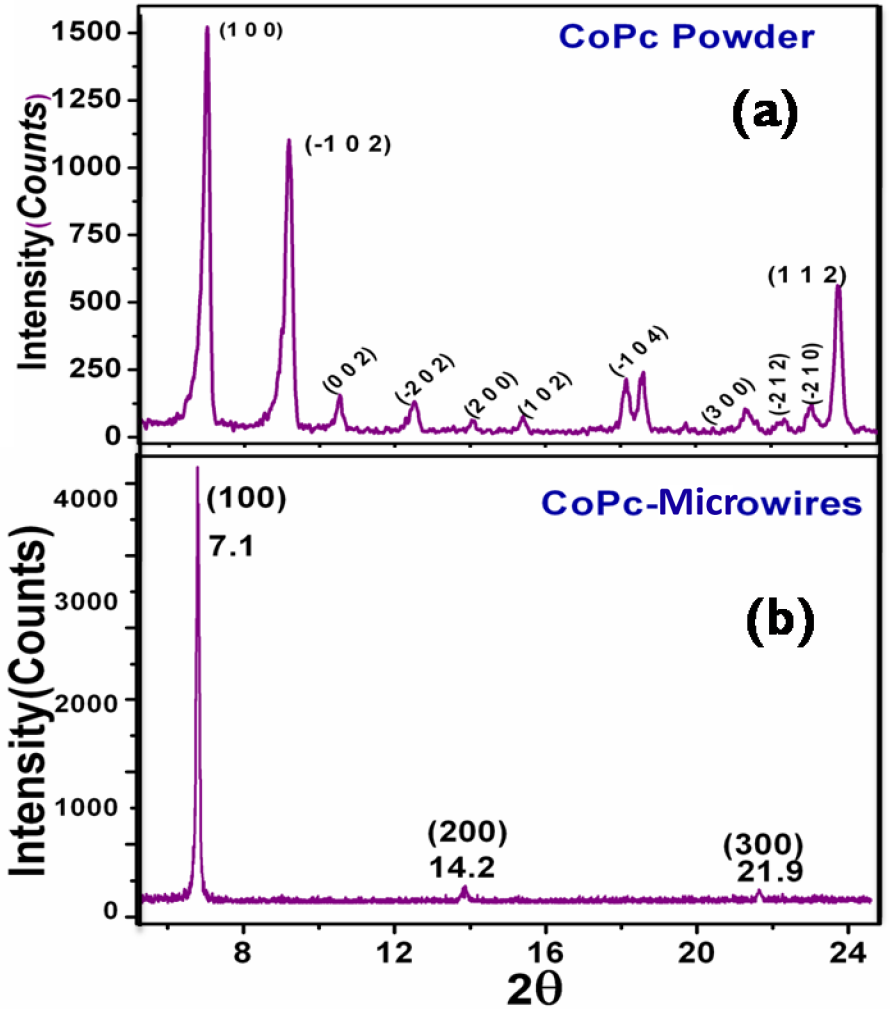

Figure 4.10: X-ray diffraction pattern of powdered CoPc and its microwires deposited on SiO_2 substrate.

TH-1322_10612101

It was shown also that the powder consists entirely of the polymorph, and with the appearance of additional peaks probably indicates the existence of a small proportion of different polymorph or impurities. The sharp diffraction peaks and the flat baseline of XRD curve indicate a perfect crystalline feature.

TEM planar view of a single wire is shown Figure 4.11(b). The crystalline nature of the wires was further confirmed by high-resolution transmission electron microscopy (HRTEM) as shown in Figure 4.11(c). The molecular planes within the wires are seen in HRTEM result. The inter-planer spacing measured form HRTEM images are about 1.22 nm, which confirm the spacing observed from XRD measurement.

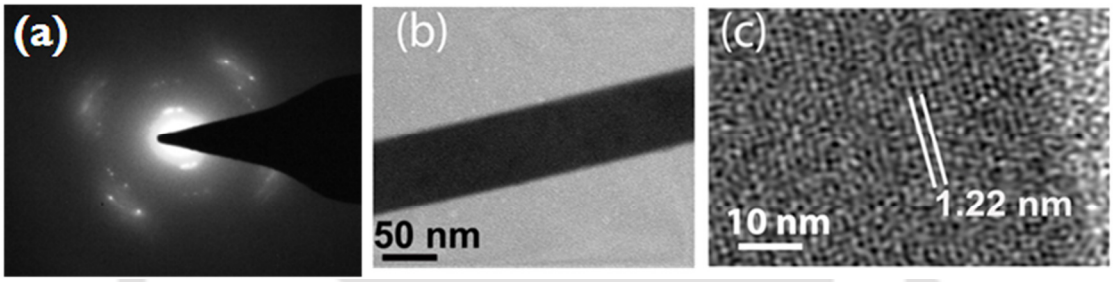

Figure 4.11: (a) SAED pattern of single CoPc wire, **(b)** TEM planar view of a single wire and **(c)** HRTEM image of single wire.

4.3.2 CoPc Micron-wires based OFET Fabrication

Efficient field-effect mechanism for OFETs can enhance the performance of the devices significantly by controlling the charge flow through the channel. We have optimized the device structure that ensures a better capacitive coupling between the gate and the channel through dielectric layer to enhance field-effect carrier mobility.

I. Optimization of Dielectric Layer Thickness

In our devices, we have used the dielectric layer as combination of Al_2O_3 and PVA. The total capacitance measured in Au/PVA-Al_2O_3/Al system largely depends on the capacitance arises from the geometric capacitance C_b due to dielectric layer in series with an effective interfacial capacitance C_i [30, 31]. The interfacial capacitance is associated with the interface states at the metal-insulator interfaces. The capacitance C_b can be written as $C_b = k\varepsilon_0 A / d$,

where k is dielectric constant and ε_0 is the permittivity of free space. A is the capacitive area and d is the effective thickness of the dielectric layer. Here C_b arises due to combined layer of Al_2O_3 and PVA. We have assumed a single capacitance due to their comparable dielectric constant. The measured capacitance (C_m) is considered as a series combination of C_b and C_i. As a result, one can write the measure capacitance with simple relation [30].

$$\frac{1}{C_m} = \frac{1}{C_b} + \frac{1}{C_i} = \frac{d}{k\varepsilon_0 A} + \frac{1}{C_i} \qquad \text{---------- (4.1)}$$

which can show a linear dependence of inverse capacitance with d with a non-zero intercept at $d = 0$. This dependency is verified and plotted in Figure 4.12(a). All the values of capacitance for different d were calculated for unit area. The value of k calculated from slope of linear fit, as shown in Figure 4.12(a), is 8.6 which is within the range of reported dielectric constant of Al_2O_3 and PVA materials. This value thus indicates good quality dielectric film obtained using organic-inorganic materials combination. From the zero thickness interception at inverse capacitance provides the value of C_i = 45 nF/cm^2. The cross over thickness at which $C_b = C_i$ occurs is d_l = 40 nm. This provides the lower limit of the thickness of the dielectric layer that can be used for the devices for better capacitive coupling with the channel. At any thickness smaller than d_l, the interface contribution dominates capacitive part of the dielectric materials. Therefore, thickness of the dielectric layer should be any thickness greater than d_l. However, the capacitance is inversely proportional to the thickness of the dielectric layer. As a result, any higher d also minimizes the capacitance. In order to find out the optimized thickness of the dielectric materials for our devices, we measured the leakage current through the capacitance. Figure 4.12(b) shows the plot for leakage current, J vs d, which clearly shows that the leakage current significantly decreases with the thickness of the dielectric film and reached to the value of about ~10^{-8} A/cm^2 at the thickness 75 nm. The leakage current is measured at the maximum gate operating voltage (-20 V) of the OFETs. Here, we have essentially varied the thickness of PVA layer on top of a 30 nm anodized Al_2O_3 film. We have selected final thickness of the dielectric layer as 75 nm for the fabrication of OFETs. This thickness includes 45 nm of PVA layer. 30 nm thickness of Al_2O_3 layer was chosen in order to keep the thickness of the PVA layer minimum. It is to be noted

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that without Al_2O_3 layer, the required thickness of PVA is about 1µm to achieve 10^{-8} A/cm^2 leakage current.

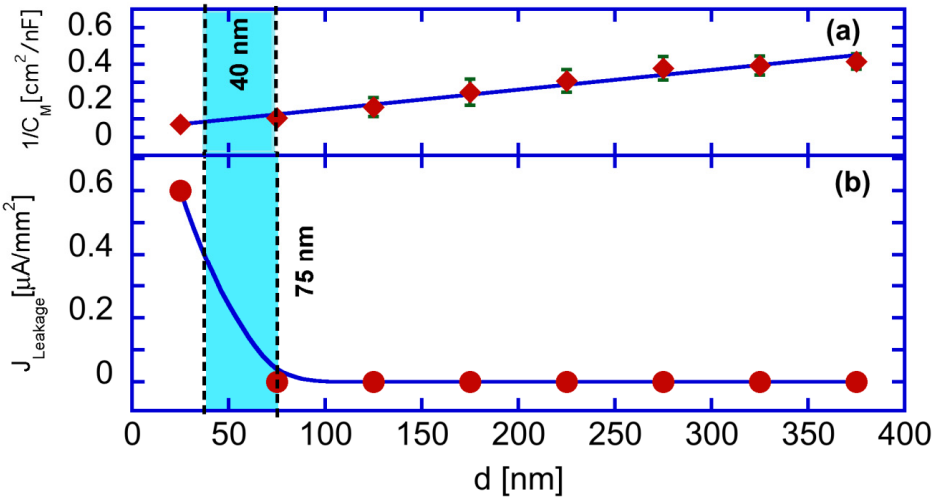

Figure 4.12: Representative plots of **(a)** Variation of capacitance with thickness and **(b)** Leakage current variation with thickness of hybrid dielectric.

II. Transistor Parameter Extraction

In order to fabricate OFETs, the CoPc wires grown on silicon substrates were transfer into ethanol solution in which the wires are not soluble. The CoPc wires suspended solution was then dropped onto the PVA dielectric surfaces. Once the ethanol was evaporated, the wires were deposited onto the dielectric surfaces. Gold (Au) electrodes were deposited by thermal evaporation with shadow–mask of 50 µm channel length and 1mm channel width. Figure 4.13(a) shows the typical design of OFET. Figure 4.13(b) shows an optical micrograph of the device top showing the source-drain contacts and the deposited CoPc wire mesh on the channel. The output and transfer characteristics curves for the multi-wires OFETs were collected in air using Keithley-4200 SCS parameter analyzer. The transfer characteristics in ambient exhibit a threshold voltage -7.8 V as shown in Figure 4.13(c-d). The on/off ratio obtained from the devices is ~10^4. The maximum obtained carrier mobility (μ_{FE}) is 1.65 cm^2/Vs and the average charge carrier mobility is 1.11 ± 0.20 cm^2/Vs based on more than 20 test devices. While calculating the mobility, we assumed that the channel width is completely covered by CoPc wires as shown in Figure 4.13(b). However, effective width

of the channel could be less than the actual channel width that we assumed in our calculations. Therefore, the actual mobility from these devices is expected to be more than the quoted value. It is to be noted that *Yang et al* observed the mobility 2.6×10^{-4} cm^2/Vs for 50 ML thick CoPc thin film based OFETs [53].

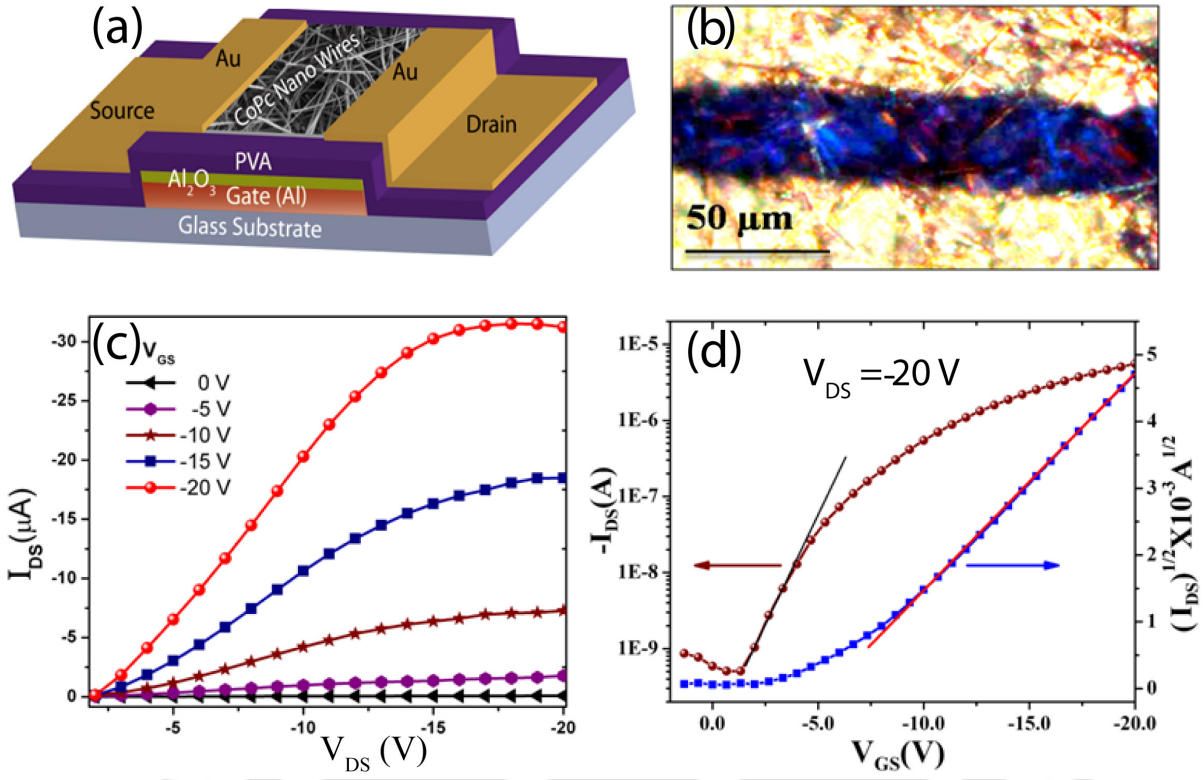

Figure 4.13: (a) Typical design of an OFET, **(b)** optical micrograph of showing the channel containing CoPc wires. Bright parts are source and drain connection, **(c)** output characteristics and **(d)** transfer curve and plots of $I_{DS}^{1/2}$ vs V_{GS} for CoPc wire based OFETs.

Zhang et al. demonstrated enhanced charge carrier mobility for thin film based transistors made of sandwiched CoPc and copper phthalocynine (CuPc) layers to 0.11 cm^2/Vs. In both the cases, the used dielectric materials were inorganic materials. The enhanced mobility observed in our OFETs is due to single crystal wires, which are essentially free form grain boundaries. However, we have used large number of interconnected CoPc wire-mesh within the channel. As a result, junctions between wires may be considered as defect boundaries, which may reduce the mobility. Single wire OFETs could eliminate this effect. The enhanced mobility observed is largely contributed by field-effect mobility in our case. This comes essentially from the major fraction of wires, which have better capacitive coupling with gate

TH-1322_10612101

and are directly in contact with the PVA surfaces. Highly smooth PVA surfaces results a better contact of the wires with the dielectric. Field-effect mobility was further improved by the appropriate selection of the dielectric materials and the thickness at which the leakage current is significantly low.

4.4 Summary & Conclusions

In this chapter we have investigated the 1D growth of CoPc microstructures. Studies on morphology of CoPc microstructures influenced by different surfaces like glass, mica, Ag/glass, Al/glass, Au/glass, Au nano-particle template and SiO_2 were done. With the optimized parameters like flow rate of carrier gas, substrate temperature, substrate type and deposition time, we were able to grow long 1D microwires. To ensure the crystalline quality and wires purity, the experiments were performed by means of XRD, TEM, FTIR and UV-Vis. Selective wires with high crystallinity were used in OFET fabrication. We have observed significant enhancement of field-effect carrier mobility of CoPc wire based OFETs. The enhanced mobility achieved by the combination of organic and inorganic materials as gate dielectric. At the same time, the proper selection of the thickness of the dielectric layers improves the capacitive coupling between channel and gate. In this case, the capacitance due to dielectric layer was dominated the contributions from interface capacitance. In order to identify the best process condition of OFET design, we varied the thickness of the dielectric layers combining with leakage current measurements and determined the thickness of the layer for better performance.

4.5 References

[1] M. Lloyd, Enhancing existing products with new technologies, Medical Dev. Tech., 18 (2007) 34-35.

[2] T.J. Shin, H. Yang, M.M. Ling, J. Locklin, L. Yang, B. Lee, M.E. Roberts, A.B. Mallik, Z. Bao, Tunable thin-film crystalline structures and field-effect mobility of oligofluorene-thiophene derivatives, Chem. Mater., 19 (2007) 5882-5889.

TH-1322_10612101

[3] E.W. Meijer, A.P.H.J. Schenning, Chemistry: Material marriage in electronics, Nature, 419 (2002) 353-354.

[4] A.N. Aleshin, Polymer nanofibers and nanotubes: Charge transport and device applications, Adv. Mater., 18 (2006) 17-27.

[5] J. Huang, S. Virji, B.H. Weiller, R.B. Kaner, Polyaniline nanofibers: Facile synthesis and chemical sensors, J. Am. Chem. Soc., 125 (2003) 314-315.

[6] S.C. Hernandez, D. Chaudhuri, W. Chen, N.V. Myung, A. Mulchandani, Single polypyrrole nanowire ammonia gas sensor, Electroanalysis, 19 (2007) 2125-2130.

[7] Q. Tang, L. Li, Y. Song, Y. Liu, H. Li, W. Xu, Y. Liu, W. Hu, D. Zhu, Photoswitches and phototransistors from organic single-crystalline sub-micro/nanometer ribbons, Adv. Mater., 19 (2007) 2624-2628.

[8] G.A. O'Brien, A.J. Quinn, D.A. Tanner, G. Redmond, A single polymer nanowire photodetector, Adv. Mater., 18 (2006) 2379-2383.

[9] S. Berson, R. De Bettignies, S. Bailly, S. Guillerez, Poly(3-hexylthiophene) fibers for photovoltaic applications, Adv. Funct. Mater., 17 (2007) 1377-1384.

[10] D. O'Carroll, I. Lieberwirth, G. Redmond, Microcavity effects and optically pumped lasing in single conjugated polymer nanowires, Nat. Nanotechnol., 2 (2007) 180-184.

[11] R.J. Tseng, J. Huang, J. Ouyang, R.B. Kaner, Y. Yang, Polyaniline nanofiber/gold nanoparticle nonvolatile memory, Nano Lett., 5 (2005) 1077-1080.

[12] T.Q. Nguyen, R. Martel, P. Avouris, M.L. Bushey, L. Brus, C. Nuckolls, Molecular Interactions in One-Dimensional Organic Nanostructures, J. Am. Chem. Soc., 126 (2004) 5234-5242.

[13] B.S. Ong, Y. Wu, P. Liu, S. Gardner, Structurally ordered polythiophene nanoparticles for high-performance organic thin-film transistors, Adv. Mater., 17 (2005) 1141-1144.

[14] A.K. Wanekaya, M.A. Bangar, M. Yun, W. Chen, N.V. Myung, A. Mulchandani, Field-effect transistors based on single nanowires of conducting polymers, J. Phys. Chem. C, 111 (2007) 5218-5221.

[15] T. Sekitani, U. Zschieschang, H. Klauk, T. Someya, Flexible organic transistors and circuits with extreme bending stability, Nat. Mater., 9 (2010) 1015-1022.

TH-1322_10612101

[16] K. Myny, S. Steudel, S. Smout, P. Vicca, F. Furthner, B. van der Putten, A.K. Tripathi, G.H. Gelinck, J. Genoe, W. Dehaene, P. Heremans, Organic RFID transponder chip with data rate compatible with electronic product coding, Org. Electron., 11 (2010) 1176-1179.

[17] D.M. DeLongchamp, S. Sambasivan, D.A. Fischer, E.K. Lin, P. Chang, A.R. Murphy, J.M.J. Fréchet, V. Subramanian, Direct correlation of organic semiconductor film structure to field-effect mobility, Adv. Mater., 17 (2005) 2340-2344.

[18] D.M. DeLongchamp, R.J. Kline, E.K. Lin, D.A. Fischer, L.J. Richter, L.A. Lucas, M. Heeney, I. McCulloch, J.E. Northrup, High carrier mobility polythiophene thin films: Structure determination by experiment and theory, Adv. Mater., 19 (2007) 833-837.

[19] J.A. Merlo, C.D. Frisbie, Field effect transport and trapping in regioregular polythiophene nanofibers, J. Phys. Chem. B, 108 (2004) 19169-19179.

[20] H. Yang, J.S. Tae, Z. Bao, C.Y. Ryu, Structural transitions of nanocrystalline domains in regioregular poly(3-hexyl thiophene) thin films, J. Poly. Sci., Part B: Polymer Physics, 45 (2007) 1303-1312.

[21] A.N. Aleshin, H.J. Lee, Y.W. Park, K. Akagi, One-Dimensional Transport in Polymer Nanofibers, Phys. Rev. Lett, 93 (2004) 196601-4.

[22] M.D. Curtis, J. Cao, J.W. Kampf, Solid-State Packing of Conjugated Oligomers: From π-Stacks to the Herringbone Structure, J. Am. Chem. Soc., 126 (2004) 4318-4328.

[23] J. Cornil, D. Beljonne, J.P. Calbert, J.L. Brédas, Interchain interactions in organic π-conjugated materials: Impact on electronic structure, optical response, and charge transport, Adv. Mater., 13 (2001) 1053-1067.

[24] F.J.M. Hoeben, P. Jonkheijm, E.W. Meijer, A.P.H.J. Schenning, About supramolecular assemblies of π-conjugated systems, Chem. Rev., 105 (2005) 1491-1546.

[25] A.P.H.J. Schenning, E.W. Meijer, Supramolecular electronics; nanowires from self-assembled π-conjugated systems, Chem. Commun., (2005) 3245-3258.

[26] C. Tanase, P.W.M. Blom, D.M. de Leeuw, E.J. Meijer, Charge carrier density dependence of the hole mobility in poly(p-phenylene vinylene), Phys. Status Solidi. A., 201 (2004) 1236-1245.

[27] G. Horowitz, Organic thin film transistors: From theory to real devices, J. Mater Res., 19 (2004) 1946-1962.

TH-1322_10612101

[28] M.A. Alam, A. Dodabalapur, M.R. Pinto, A two-dimensional simulation of organic transistors, IEEE Trans. Electron Devices, 44 (1997) 1332-1337.

[29] L.A. Majewski, R. Schroeder, M. Grell, Flexible high capacitance gate insulators for organic field effect transistors, J. Phys. D. Appl. Phys., 37 (2004) 21-24.

[30] T.W. Hickmott, Interface states at the anodized Al2O3-metal interface, J. Appl. Phys., 89 (2001) 5502-5508.

[31] A.F. Hebard, S.A. Ajuria, R.H. Eick, Interface Contribution to the Capacitance of Thin-Film Al-Al2o3-Al Trilayer Structures, Appl. Phys. Lett., 51 (1987) 1349-1351.

[32] H.C. Lin, P.D. Ye, G.D. Wilk, Leakage current and breakdown electric-field studies on ultrathin atomic-layer-deposited Al2O3 on GaAs, Appl. Phys. Lett., 87 (2005) 182904-3.

[33] L.A. Majewski, R. Schroeder, M. Grell, One volt organic transistor, Adv. Mater., 17 (2005) 192-196.

[34] J. Park, S.Y. Park, S.O. Shim, H. Kang, H.H. Lee, A polymer gate dielectric for high-mobility polymer thin-film transistors and solvent effects, Appl. Phys. Lett., 85 (2004) 3283-3285.

[35] S. Kobayashi, T. Nishikawa, T. Takenobu, S. Mori, T. Shimoda, T. Mitani, H. Shimotani, N. Yoshimoto, S. Ogawa, Y. Iwasa, Control of carrier density by self-assembled monolayers in organic field-effect transistors, Nat. Mater., 3 (2004) 317-322.

[36] C. Kim, A. Facchetti, T.J. Marks, Polymer gate dielectric surface viscoelasticity modulates pentacene transistor performance, Science, 318 (2007) 76-80.

[37] Y. Jang, D.H. Kim, Y.D. Park, J.H. Cho, M. Hwang, K.W. Cho, Low-voltage and high-field-effect mobility organic transistors with a polymer insulator, Appl. Phys. Lett., 88 (2006) 072101-3.

[38] J. Puigdollers, C. Voz, A. Orpella, R. Quidant, I. Martin, M. Vetter, R. Alcubilla, Pentacene thin-film transistors with polymeric gate dielectric, Org. Electron., 5 (2004) 67-71.

[39] X. Liu, Y. Zhang, D.K. Goswami, J.S. Okasinski, K. Salaita, P. Sun, M.J. Bedzyk, C.A. Mirkin, The controlled evolution of a polymer single crystal, Science, 307 (2005) 1763-1766.

[40] Y.M. Wu, X.J. Zhang, H.H. Pan, W. Deng, X.H. Zhang, X.W. Zhang, J.S. Jie, In-situ device integration of large-area patterned organic nanowire arrays for high-performance optical sensors, Sci Rep-Uk, 3 (2013) 1-8.

TH-1322_10612101

[41] K.J. Huang, Y.S. Hsiao, W.T. Whang, Selective growth and enhanced field emission properties of micropatterned iron phthalocyanine nanofiber arrays, Org. Electron., 12 (2011) 1826-1834.

[42] Y.S. Zhao, P. Zhan, J. Kim, C. Sun, J.X. Huang, Patterned Growth of Vertically Aligned Organic Nanowire Waveguide Arrays, ACS nano, 4 (2010) 1630-1636.

[43] M. Alcaire, J.R. Sanchez-Valencia, F.J. Aparicio, Z. Saghi, J.C. Gonzalez-Gonzalez, A. Barranco, Y.O. Zian, A.R. Gonzalez-Elipe, P. Midgley, J.P. Espinos, P. Groening, A. Borras, Soft plasma processing of organic nanowires: a route for the fabrication of 1D organic heterostructures and the template synthesis of inorganic 1D nanostructures, Nanoscale, 3 (2011) 4554-4559.

[44] N.Y. Jin-Phillipp, T.N. Krauss, P.A. van Aken, The Growth of One-Dimensional CuPcF16 Nanostructures on Gold Nanoparticles as Studied by Transmission Electron Microscopy Tomography, ACS nano, 6 (2012) 4039-4044.

[45] J. Oni, N. Sehlotho, Template-directed electrochemical synthesis of cobalt phthalocyanine nanowires, J. Porphyrins Phthalocyanines, 16 (2012) 935-938.

[46] B.N. Mbenkum, E. Barrena, X.N. Zhang, M. Kelsch, H. Dosch, Selective growth of organic 1-D structures on Au nanoparticle arrays, Nano Lett., 6 (2006) 2852-2855.

[47] A. Yamashita, T. Maruno, T. Hayashi, Absorption-Spectra of Organic-Molecular-Beam-Deposited Vanadylphthalocyanine and Titanylphthalocyanine, J. Phys. Chem., 97 (1993) 4567-4569.

[48] H.P. Xia, M. Nogami, Copper phthalocyanine bonding with gel and their optical properties, Opt. Mater., 15 (2000) 93-98.

[49] E.A. Lucia, F.D. Verderame, Spectra of polycrystalline phthalocyanines in the visible region, J. Chem. Phys., 48 (1968) 2674-2681.

[50] T. Enokida, R. Hirohashi, Cobalt Phthalocyanine Crystal Synthesized at Low-Temperature, Chem. Mater., 3 (1991) 918-921.

[51] S.I. Shihub, R.D. Gould, Structure and Phase-Change Phenomena in Evaporated Thin-Films of Cobalt Phthalocyanine, Phys. Status Solidi. A., 139 (1993) 129-138.

[52] B.E. Schuster, T.V. Basova, V.A. Plyashkevich, H. Peisert, T. Chasse, Effects of temperature on structural and morphological features of CoPc and CoPcF16 thin films, Thin Solid Films, 518 (2010) 7161-7166.

TH-1322_10612101

[53] R.D. Yang, T. Gredig, C.N. Colesniuc, J. Park, I.K. Schuller, W.C. Trogler, A.C. Kummel, Ultrathin organic transistors for chemical sensing, Appl. Phys. Lett., 90 (2007) 263506 -263503.

TH-1322_10612101

Chapter V

Effect of Growth Temperature on the Performance of PTCDI-Ph OFETs

5.1 Introduction

Generally, organic semiconducting active channels of the OFETs are grown on the gate dielectric surfaces. The gate field through the dielectric layer induces charge carriers in the active channel, which essentially creates conducting channel through the active layer. Therefore, it has been found that charge transport through the active channel depends closely on the morphology of the film in contact to the dielectric layers [1-3]. Thin films with high structural order are required to realize the novel electronic and optical applications that have been proposed for devices based on small conjugated molecules. Enormous progress have made in understanding how the performances of OFETs depends on the structural definition of the active channel grown on dielectric layers over last few decades [4-20]. It is also reported that the charge transport properties of conjugated molecules like perylene derivatives are intrinsically correlated with their crystalline structure, with the degree of orientation, and with grain size, although the exact form of these correlations is not yet well understood. Therefore, optimization of OFET performances requires the control and the understanding of the growth parameters of organic semiconductor channel on dielectric layers. In this chapter, we have studied the growth kinetics of the active organic channel grown on polymer dielectric layer. Thermodynamics and growth kinetics of the organic thin films on dielectric surfaces depends on different deposition parameters such as substrate temperature, coverage, deposition rate, chemical and structural nature of the substrate surfaces [21-25]. Substrate temperature influences on the diffusion of organic molecules on substrates and controls the film morphology. Since the charge transport through the organic channel is strongly correlated to the electronic structure and self-organization of the

TH-1322_10612101

molecules. The film morphology can be tuned by varying substrate temperature to optimize different OFET parameters such as carrier mobility, threshold voltage and on/off ratio [2]. Nevertheless, a dielectric layer used in the fabrication of OFETs also influences the above parameters [26]. Enormous research has been carrier out to understand the growth of organic film on dielectric surfaces like SiO_2 [2, 23]. Several other materials with higher dielectric constants are routinely being used for the fabrication of OFETs [27, 28]. Dielectric layer in OFETs has an important role to play in charge transport through the device. Charge density in the active channel of the device is largely confined to the first few monolayers at the dielectric-semiconductor interfaces [29-31]. Therefore, the mobility at this region is highest. As a result, a better capacitive coupling between active channel and the gate dielectric along with a better molecular assembly are expected to enhance field-effect carrier mobility of the device. This is due to the enhanced mobile carrier density at the accumulation layer. Therefore, the influence of dielectric layer on the growth of organic active channel has become important to study in order to fabricate efficient devices. To achieve this, a proper selection of gate dielectric materials with specific device design is essential along with the fabrication of active channel for better charge transport mechanism. In such cases, multi-component dielectric system combining inorganic and organic dielectric films showed better performances of the devices [32, 33]. Organic nature of the interface between the active channel and the dielectric layer may provide a more efficient capacitive coupling with the channel, perhaps because of better matching in surface energy of these materials [28, 34]. Such high performance OFETs are demonstrated using polymer-treated inorganic dielectrics [32, 34]. Polyvinyl alcohol (PVA), poly (methyl methacrylate) (PMMA) and poly(4-vinylphenol) (PVP) [35-37] are frequently utilized organic polymer dielectrics for OFETs fabrication. In this work, we have used the combination of PMMA and Al_2O_3 as the bi-layer dielectric for the fabrication of N,N′-diphenyl-3,4,9,10-perylenedicarboximide (PTCDI-Ph) as active channel of OFETs. We have explored the effect of substrate temperature on the growth of the active channel and showed how the carrier mobility can be enhanced by controlling the surface morphology of the organic channel grown on PMMA layer.

This chapter covers N,N′-diphenyl-3,4,9,10-perylenedicarboximide (PTCDI-Ph) thin film growth on SiO_2 and on a bilayer dielectric consisting layers of poly (methyl methacrylate) (PMMA) and Al_2O_3 for the fabrication of organic field-effect transistors (OFETs). Substrate

TH-1322_10612101

temperature was varied between 30 and 120 °C during the growth of PTCDI-Ph. The evolution of surface morphology with the substrate temperatures was studied. We have studied how the OFETs parameters, such as carrier mobility and threshold voltage, depend on the growth of the films. The characteristic parameters of rough surfaces were measured as the films grow. OFETs were fabricated with the same films and OFETs parameters were correlated with those parameters.

5.2 Experimental Details

PTCDI-Ph is one of the Perylene derivative synthesized, purified and used as an active material for the OFETs fabrication. Figure 5.1 shows the typical molecular structure of PTCDI-Ph molecule. Two sets of transistors were fabricated using two different dielectrics, such as SiO_2 and polymer surface. SiO_2 substrates are commonly considered as gate dielectric for the fabrication of microelectronic devices. However, in this study, SiO_2 substrates were used to compare the influence of substrates on the OFET parameters.

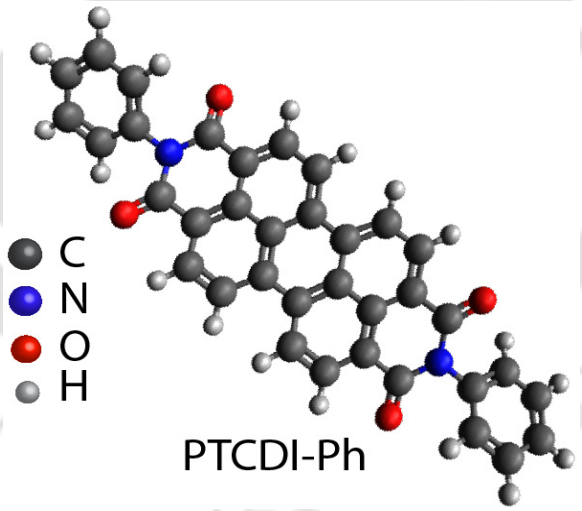

Figure 5.1: Molecular structure of PTCDI-Ph organic semiconductor.

5.2.1 PTCDI-Ph based OFET fabrication on SiO_2 substrate

Highly boron (B) doped silicon (Si) (Resistivity: 0.001-0.005 Ω-cm) with thermally grown oxide layer of 300 nm wafers were used to fabricate the devices. Initially, all the

TH-1322_10612101

substrates were treated with piranha solution followed by ultra-sonication by several cycles with acetone, methanol and de-ionized water. To eliminate residual contaminants and to make hydrophobic surface, substrates were then purged with argon (Ar) gas. All substrates were fixed to substrate holder of custom designed organic molecular beam deposition (OMBD) apparatus with four Knudsen cells. PTCDI-Ph thin films of ~85 nm thick were grown. The base pressure in the chamber was ~10^{-7} mbar and the deposition rate used is 1.2nm/min. The evaporation temperature of PTCDI-Ph was 390 ºC. Semiconducting active channels were deposited at different substrate temperatures on to the pre-cleaned SiO_2 substrates. We have deposited ~ 90 nm silver (Ag) as source and drain electrodes on to the active channel by using shadow mask. Figure 5.2 shows the typical illustration of the OFET devices fabricated in this work.

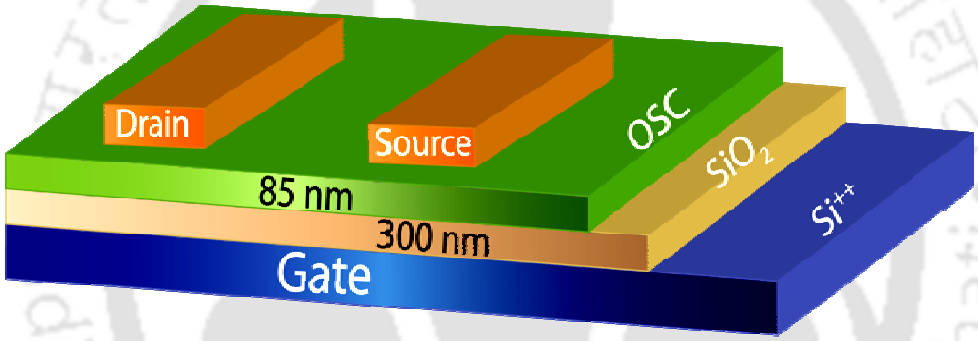

Figure 5.2: Schematic illustrations of organic field effect transistors.

The morphology of the thin-film was recorded using an atomic force microscope (AFM) in tapping mode. The images were then plane corrected to overcome pillow effects using software package WSxM5.0 Develop 6.5 [38]. OFET output and transfer characteristics were measured by means of Keithley-4200 semiconductor characterization system (SCS) connected with micro manipulated four probe station, which is described in the section 2.4.1 of *chapter II*.

5.2.2 OFET fabrication on Organic-Inorganic Dielectrics surface

PMMA-Al_2O_3 hybrid layers were used for the fabrication of another set of OFETs. Glass slides were chosen as the substrates to fabricate OFETs. The glass slides were cleaned using

TH-1322_10612101

piranha solution followed by several cycles of cleaning with DI-water, methanol and acetone in ultra-sonic bath. About 300 nm thick aluminum films were grown on the pre-cleaned glass surfaces using thermal evaporation techniques. A part of Al film was then anodized to form about ~10 nm thick Al_2O_3 layer to be used as one of the gate dielectric layers. Anodized Al_2O_3 surfaces were found to be rough with typical rms roughness of 23.9 nm. In order to achieve a smooth interface between gate dielectric and organic channel, we have spin-coated the Al_2O_3 surfaces with 45 nm PMMA (M_W ~ 2,50,000 g/mol) layer of 5 wt% of anisole solution. In this process, the rms roughness of the dielectric surface reduced to 1.42 nm. The smooth film formation is essentially due to lower surface free energy of PMMA (~0.037 J/m^2) than Al_2O_3 (~1.7 J/m^2).

The stack of Al_2O_3 and PMMA layers were used as gate dielectric layers for the OFETs fabrication. PTCDI-Ph films were deposited on the stack of Al_2O_3 and PMMA layers by thermal evaporation under high vacuum conditions with a base pressure of ~10^{-7} mbar at different substrate temperatures (30, 60, 90 and 120 °C). The deposition rate was around 0.5Å/s for the growth of an active layer of thickness of 85 ± 5 nm. Deposited films were further characterized by atomic force microscopy (AFM) to know the surface morphology of the films. The OFETs were fabricated using inverted-staggered (top contact) geometry as

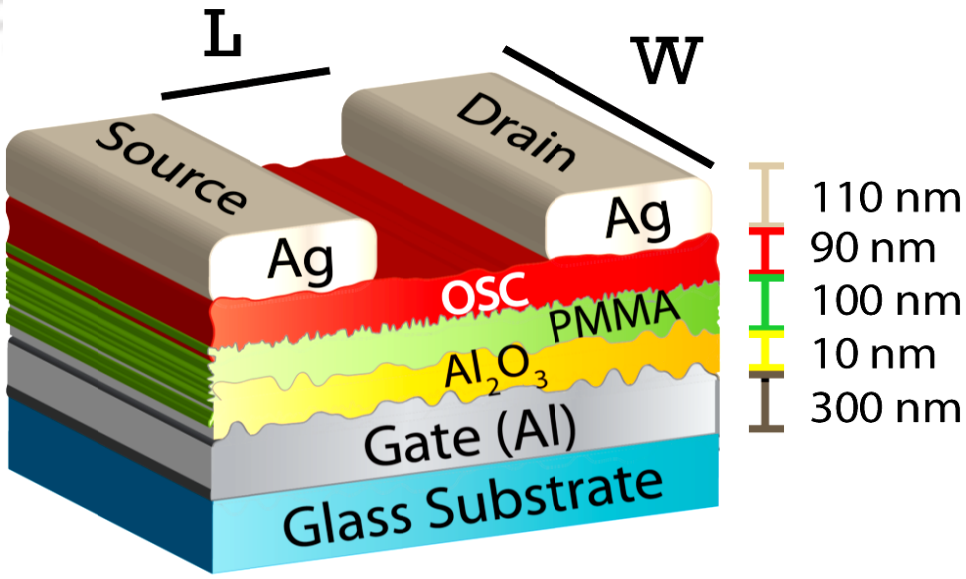

Figure 5.3: Typical design of OFET with organic-inorganic gate dielectric.

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shown in Figure 5.3. In order to grow source and drain contacts, silver (Ag) was deposited by thermal evaporation using shadow masks. The typical channel width (W) and length (L) of the designed OFETs are 1500 μm and 30 μm respectively. In general, gold, aluminum, silver and chromium metals are used as contact materials for OFETs to provide good electron injection into the active channel. The field-effect carrier mobility is also dependent on the work function of the metallic contacts [39, 40]. All the electrical measurements were performed under vacuum conditions (~10^{-2} mbar) by means of a Keithley-4200 SCS parameter analyzer. In ambient conditions, poor device performance has been observed. However, all the OFETs were recovered the performance immediately and shown better electrical characteristics under vacuum.

5.3 Results and Discussions

5.3.1 Evolution of surface morphology

(a) PTCDI-Ph/SiO_2 Film Morphology

Figure 5.4 shows the typical representative AFM images of PTCDI-Ph thin films on SiO_2 substrate grown at different substrate temperatures. Sample grown at 30ºC substrate temperature (see Figure 5.4(a)) is showing the formation of small random grains, which indicate a very poor molecular packing within the film with large numbers of grain boundaries. As the growth temperature increases, we have observed the formation of needle like long molecular terraces as shown in Figure 5.4(b-d). The formations of rectangular shaped terraces are clearly visible as shown in Figure 5.4(d). This indicates a better molecular arrangement in the film formation. However, at the same time, the films become rough as growth temperature increases and are not favorable for the fabrication of OFETs. Therefore, for better charge transport through the organic layer, one needs to have uniform molecular films in the active channel with enhanced crystalline quality [1, 41, 42]. Rougher surfaces make the films discontinuous and the charge hopping is restricted due to large grain boundaries. Therefore, optimized growth conditions are required to fabricate organic channel for better charge transport mechanism.

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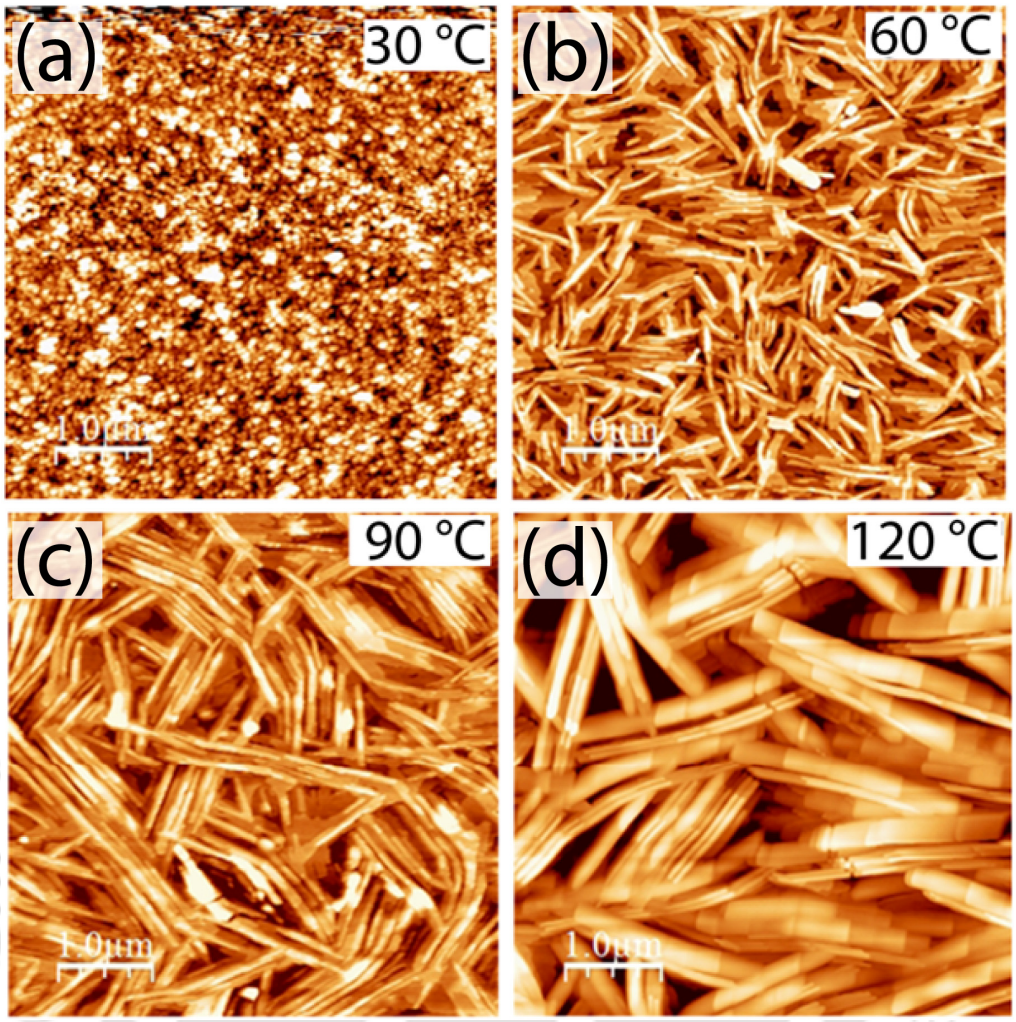

Figure 5.4: PTCDI-Ph/SiO_2 thin films topography obtained from AFM in tapping mode at various substrate temperatures 30, 60, 90 and 120 ºC.

(b) PTCDI-Ph/(PMMA/Al_2O_3) Film Morphology

Figure 5.5(a) shows representative AFM images of anodized Al_2O_3 surfaces. This clearly shows the formation of large grains, which essentially makes the surface very rough with typical rms roughness of 23.9 nm. As a result, high leakage current (~10^{-4} A/cm^2) was observed in this film. In order to minimize the leakage current, a PMMA layer was grown on Al_2O_3 surfaces. The typical AFM image of PMMA surfaces is shown in Figure 5.5(b). The roughness of the PMMA surfaces is reduced significantly and is typically about 1.42 nm. The thicknesses of both the layers have been optimized in order to achieve lower leakage current

TH-1322_10612101

with a minimum thickness and lower surface roughness. We observed the minimum leakage current of ~10^{-9} A/cm^2 at the thickness of 10 nm Al_2O_3 including 100 nm PMMA layer on top and also observed a reasonably higher capacitance(~14.3 nF/cm^2) from the combined layer dielectric system. It is to be noted that in order to achieve about ~10^{-9} A/cm^2 leakage current without Al_2O_3 layer, we need to use PMMA layer alone of about ~1 μm thick. By using bi-layer dielectric we were able to reduce the thickness of the dielectric layer significantly. PTCDI-Ph films were grown on the smooth PMMA surfaces at different substrate temperature.

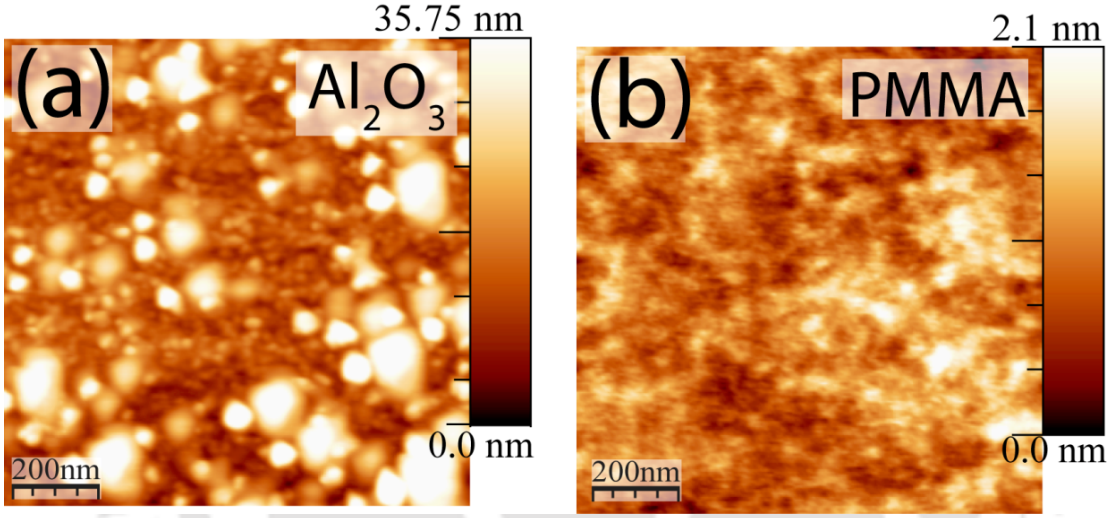

Figure 5.5: Tapping mode AFM images of **(a)** anodized Al_2O_3 and **(b)** PMMA coated Al_2O_3 surfaces.

Figure 5.6(a-d) show the typical AFM images of PTCDI-Ph surfaces grown at 30, 60, 90 and 120 °C substrate temperature, respectively. As substrate temperature increases, the size of grains at the top surface initially decreases up to 90 °C as shown in Figure 5.6(a-c). At the same time, the roughness of the films is successively decreased as one goes from Figure 5.6(a) to (c). Figure 5.6(c) is clearly showing the formation of small grains on top of a smooth film. However, formation of large mounds is observed at 120 °C substrate temperature as shown in Figure 5.6(d). These films are clearly showing discontinuity within the films by forming holes and leads to a rough film.

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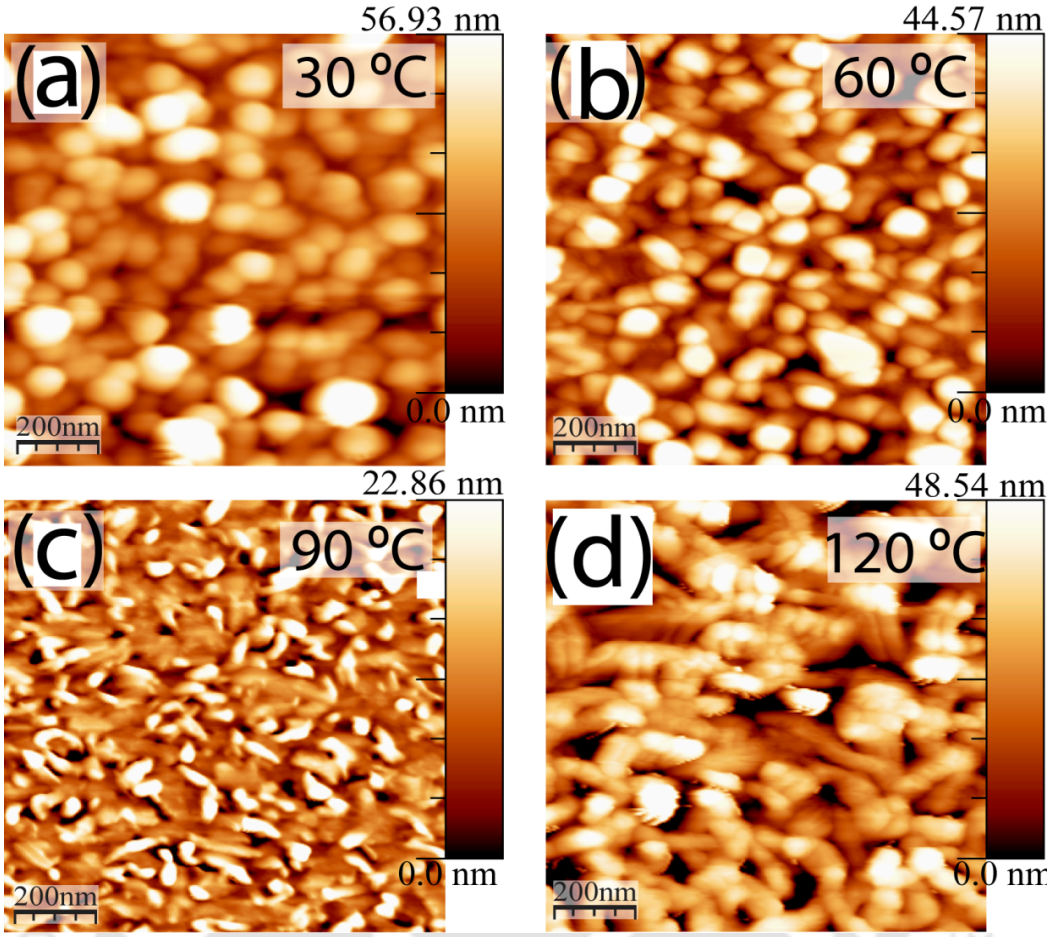

Figure 5.6: AFM topographic images of PTCDI-Ph thin films grown on hybrid dielectric at various substrate temperatures **(a)** 30 ºC, **(b)** 60 ºC, **(c)** 90 ºC and **(d)** 120 ºC.

5.3.2 Electrical Characterizations

Both SiO_2 and hybrid dielectric substrates were used for the fabrication of PTCDI-Ph based OFETs in order to study the charge transport through these films. The output and the transfer characteristics curves obtained from these devices are shown in Figure 5.7. We have extracted carrier mobility using equation described in *chapter I*. Figure 5.8 shows the summarized carrier mobility for all the OFETs fabricated using the PTCDI-Ph films grown on SiO_2 at four different substrate temperatures.

We have observed a reduction in threshold voltage (V_{TH}) as temperature increases from 30 to 90 °C (Table 5.1). This can be attributed to a better molecular self-assembly within the film due to enhanced diffusion of the molecules at higher substrate temperatures.

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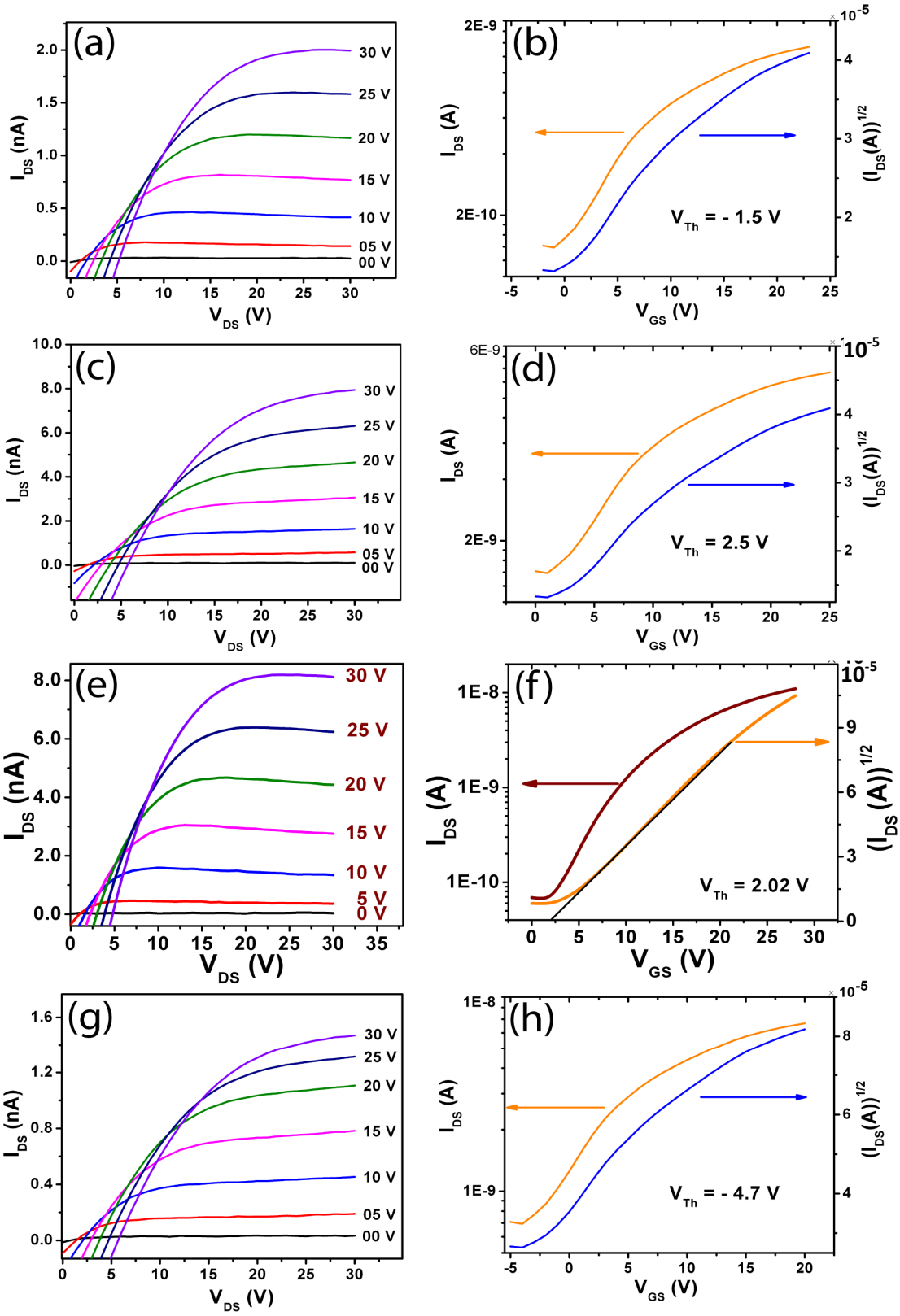

Figure 5.7: Output and transfer characteristics of PTCDI-Ph OFETs fabricated on SiO_2 substrate at different temperatures **(a-b)** 30 ºC; **(c-d)** 60 ºC; **(e-f)** 90 ºC and **(g-h)** 120 ºC.

As a result, the density of defects, grain boundaries and the crystallographic defects within the film reduces. It is also to be noted that the operating voltage of the OFETs fabricated with SiO_2 gate dielectric is about 30 V.

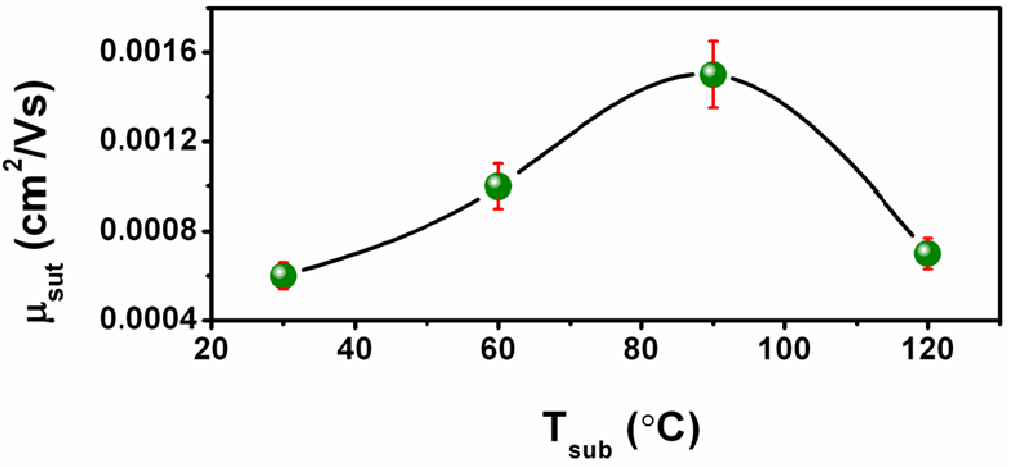

Figure 5.8: Carrier mobility variations with substrate temperature of PTCDI-Ph/SiO_2 based OFETs.

S. No.	Substrate Temperature (°C)	Threshold Voltage V_{Th}(V)	Carrier Mobility μ (cm^2/V-s)
1	30	- 1.5	0.0006
2	60	2.5	0.001
3	90	2.0	0.015
4	120	- 4.7	0.0007

Table 5.1: Summary of OFET parameters threshold voltage and carrier mobility of PTCDI-Ph/SiO_2 based device.

In order to reduce the operating voltage with enhanced carrier mobility we have fabricated OFETs using the PTCDI-Ph films grown on PMMA/Al_2O_3 bilayer dielectric system at four different substrate temperatures. Figure 5.9 shows the output and transfer characteristics of OFETs fabricated on PTCDI-Ph films grown at various substrate temperatures. We have observed a reduction in threshold voltage (V_{Th}) as temperature increases from 30 to 90°C, as observed from the devices fabricated with SiO_2 dielectric layer.

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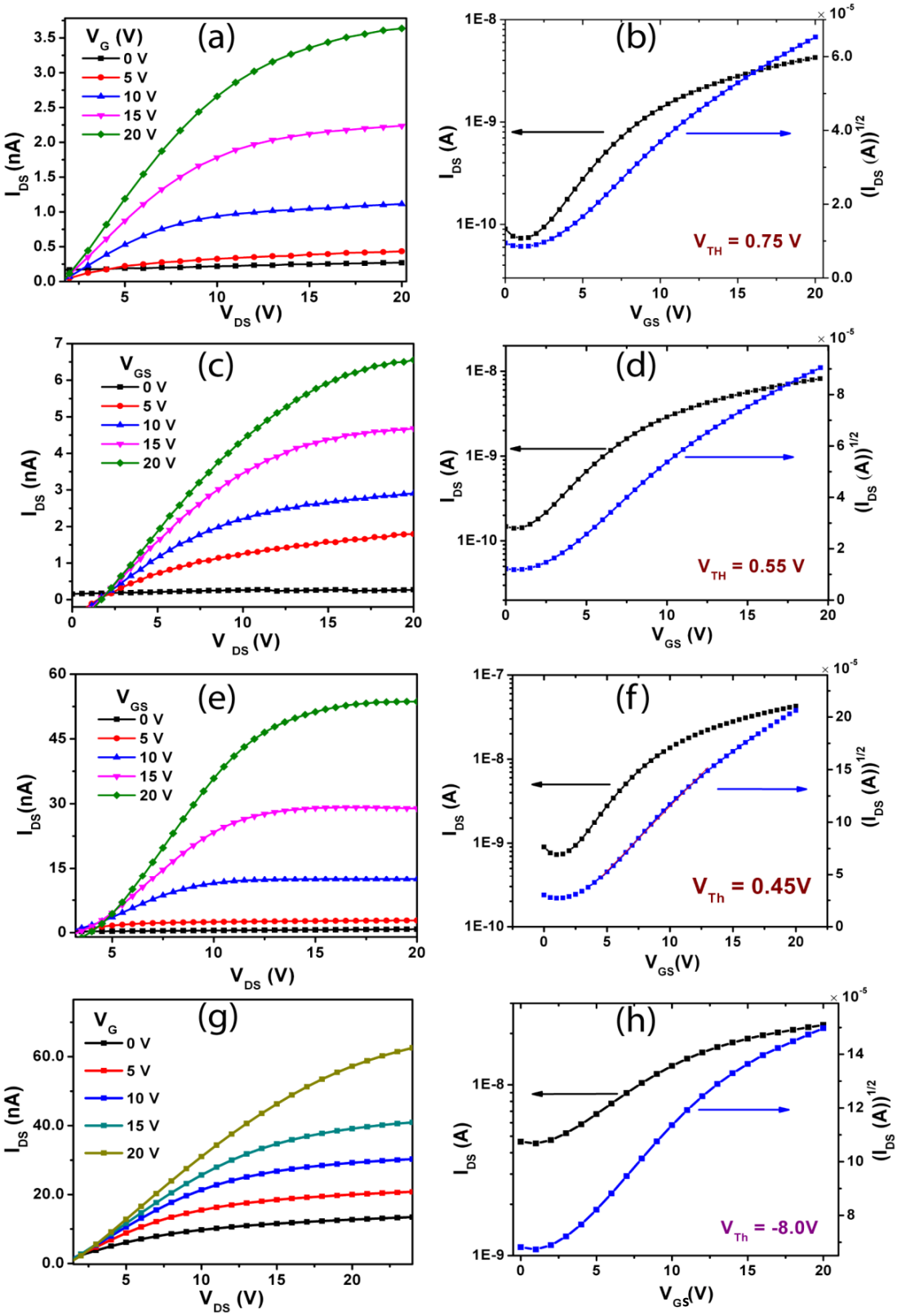

Figure 5.9: Output and transfer characteristics of PTCDI-Ph OFETs fabricated on bilayer dielectric at different temperatures **(a)-(b)** 30ºC, **(c)-(d)** 60ºC, **(e)-(f)** 90ºC and **(g)-(h)** 120ºC.

This can be attributed to reduction of the density of defects, grain boundaries and the crystallographic defects within the film. These defects act like trap states of the mobile carrier at the accumulation region of the OFETs. Therefore, the density of charge carriers at the interface of organic channel-dielectric layer reduces. A uniform film was formed at 90 °C substrate temperature as shown in Figure 5.9(e). However, we have observed the formation of discontinuous films due to larges mounds growth with pores at 120 °C substrate temperature, which is shown in Figure 5.9(f). The formation of pores could also be due to desorption of the molecules at higher substrate temperature. As a result carrier mobility observed in the OFETs fabricated with this film decreased. In this case, we have observed large negative threshold voltage of about -8.0 V. The highest carrier mobility observed is 0.021 cm^2/Vs from the OFETs fabricated with the film grown at 90°C substrate temperature.

The summarized values of carrier mobility and threshold voltage from the devices fabricated with bilayer dielectric have been given below (Table 5.2).

S.No.	Substrate Temperature (°C)	Threshold Voltage V_{Th}(V)	Carrier Mobility μ (cm^2/V-s)
1	30	0.75	0.0007
2	60	0.55	0.003
3	90	0.45	0.021
4	120	-8.0	0.0035

Table 5.2: Summarized parameters of threshold voltage and carrier mobility of PTCDI-Ph OFETs with bilayer dielectric.

We have observed the reduction in threshold voltage, which is about 0.45 V. The device operating voltage was found to be about 20 V, which is lower than the devices fabricated with SiO_2 as dielectric layer.

5.3.3 Film morphology and device properties

In order to correlate the observed variation of carrier mobility with morphology as the growth temperature PTCDI-Ph film increases, we have calculated height-height correlation

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function, *G(r),* which is defined as the mean square of height differences between two surface positions separated by a distance *r* as $G(r) = \left\langle [h(r) - h(0)]^2 \right\rangle$, where *h(r)* and *h(0)* are the heights of the surface at the locations separated by a distance *r* and the brackets signify an average over pairs of points [43-46]. For the small *r*, height-height correlation function $G(r) \sim (mr)^{2\alpha}$, with $r << \xi$, where, ξ is the characteristic in-plane correlation length, *m* is local surface slope and α is the roughness scaling exponent [47-49]. In-plane correlation lengths are the measure of the length beyond which surface heights are not significantly correlated. For the mounded surfaces, this is essentially the size of the mounds [49]. To determine ξ, we have calculated *G(r)* from AFM images following the procedure described in ref [50, 51]. In order to avoid sampling induced effect in the *G(r)* calculation, care has been taken to include many AFM images in the averaging of *G(r)* data. In our analysis, we have checked that 6 to 10 AFM images from each sample were enough to give statistically reliable data to obtain *G(r)* plot.

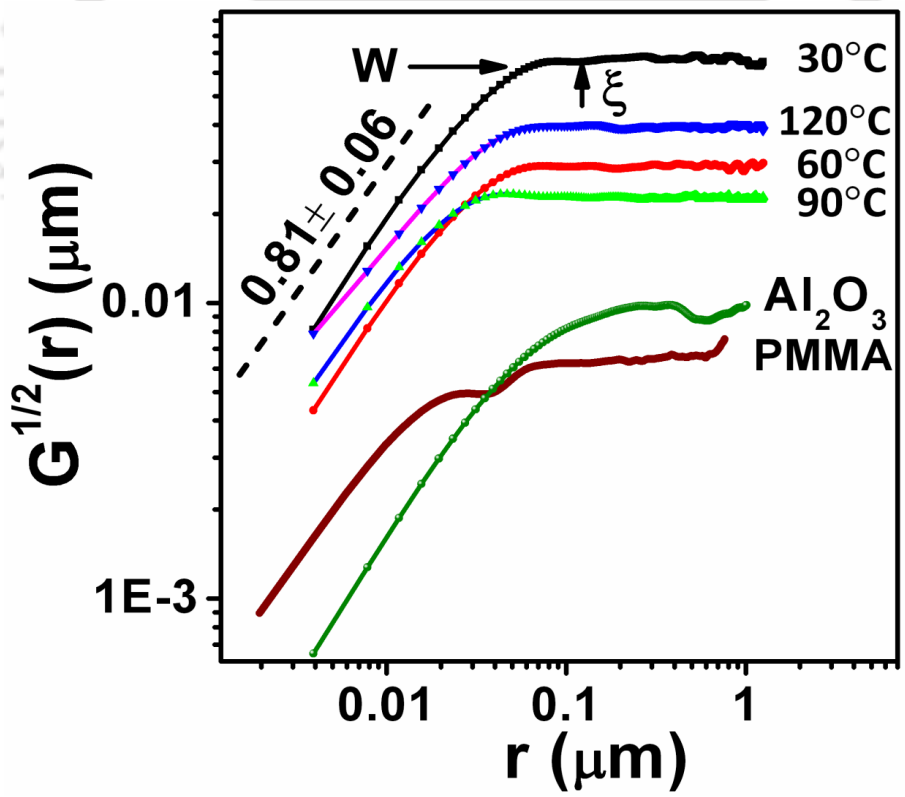

Figure 5.10: Square root of height−height correlation function calculated from AFM images of all the PTCDI-Ph films grown at various substrate temperatures, PMMA and Al_2O_3 surfaces. Roughness exponent (α) is calculated from the power fitting of the linear portion.

TH-1322_10612101

In order to understand the dynamics of growth as substrate temperature increases, we have studied how ξ and W evolve with substrate temperature since ξ estimates the lateral growth and W estimates the vertical growth of the film. W is the value of $G^{1/2}(r)$ at the first local maximum, as $W = G^{1/2}(\xi/2)$,where ξ marked by an upward arrow as shown in Figure 5.10, is the position of r at the first local minimum of $G^{1/2}(r)$ [51, 52]. The definition of roughness amplitude is preferred over the large r limit of G (r) because artifacts at large length scales can affect AFM data. Figure 5.10 summarizes the log-log variation of $G^{1/2}(r)$ vs r for all the surfaces. The value of ξ and W obtained for PMMA is less than Al_2O_3 surfaces. This revealed the formation of smooth PMMA surfaces.

The smooth dielectric surfaces are essential to achieve a better capacitive coupling between the gate and the active organic channel. The roughness exponent α was determined from a fit to the linear part of the log-log plot of $G^{1/2}(r)$ vs r. α essentially signifies the height fluctuation that corresponds to vertical growth of the film. Asymptotically, $\alpha = 1$, represents a morphology with very smooth local surfaces. We have observed the average value of α for all the PTCDI-Ph films as 0.81 ± 0.06. It is interesting to note that the roughness exponent, α for Al_2O_3 and PMMA surfaces are found to be 0.82 ± 0.03 which is similar to the PTCDI-Ph films within the measurement error. This signifies that the subsequently grown films of PMMA and PTCDI-Ph follow the same local surface properties of Al_2O_3 films and essentially follow the Al_2O_3 surfaces. In case of MBE growth, the theoretically predicted α considering for nonlinear growth equation is 0.66 [53]. If one consider the linear growth equation, the exponent will be α =1 [54]. In this system, the observed roughness exponent may be attributed to a crossover of linear and nonlinear regimes. Similar results were also reported for the growth of polymer films [55, 56]. The difference between the observed and predicted exponents indicates that the growth of organic films is different from the conventional MBE growth.

The evolution of the surface morphology can be quantified through the variation of ξ and W with substrate temperature. Though ξ and W are calculated from the morphology of the top surface layer, but variation of these parameters describes the kinetics of the growth process of the film. Smaller ξ characterizes the small grains formation, which makes the film continuous and smooth. Such films are expected to show a better charge transport

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mechanism. The variation of ξ and W obtained for the PTCDI-Ph surfaces grown at different substrate temperatures can be observed from the $G^{1/2}(r)$ vs r plot shown in the upper part of Figure 5.10. Shift of $G^{1/2}(r)$ is observed as the substrate temperature increases. This represents mounded growth when local surface slope changes as the film grows. This growth process is termed as non-stationary growth [47]. We have observed constant local surface slope of all the films is about m = 0.36. This again confirms that the local surfaces are independent of growth temperature.

In order to study how the carrier mobility depends on the film growth, we have plotted the variation of ξ, W and carrier mobility with substrate temperature as shown in Figure 5.11. When the substrate temperature increases, the value of ξ and W decreases up to 90°C and then again increases as shown in Figure 5.11(a). The minimum ξ and W were observed for the films grown at 90 °C substrate temperature. Figure 5.11(b) shows the variation of carrier mobility with substrate temperature. Significant enhancement of carrier mobility (~0.02 cm^2/Vs) has been observed for the device fabricated with the film grown at 90 °C substrate

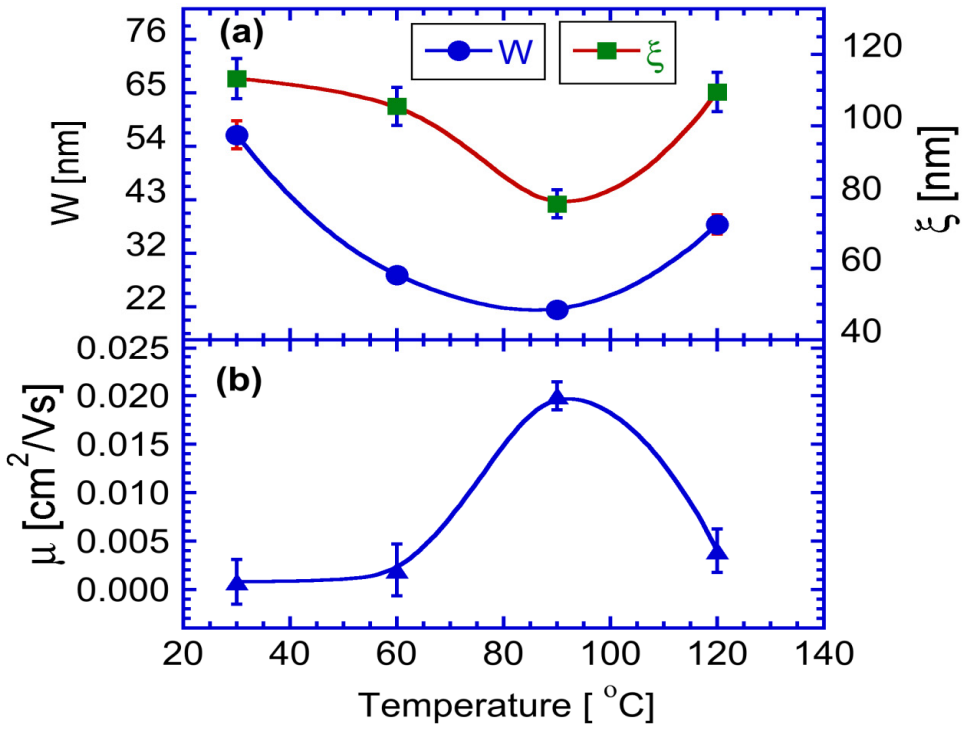

Figure 5.11: Variation of **(a)** In-plane correlation length (ξ), **(b)** Interface width (W) and **(c)** Carrier mobility (μ) with substrate temperature.

TH-1322_10612101

temperature. Substrate temperature essentially determines the growth kinetics by controlling diffusion of the molecules. The enhancement of the carrier mobility in this case may be attributed to a favorable molecular arrangement for efficient charge transport in the accumulation region at 90 °C substrate temperature. However, carrier mobility decreases as the substrate temperature increases to 120°C and the film becomes rough. Whether a film can be kinetically rough or smooth depends on the relative lateral and vertical growth rate.

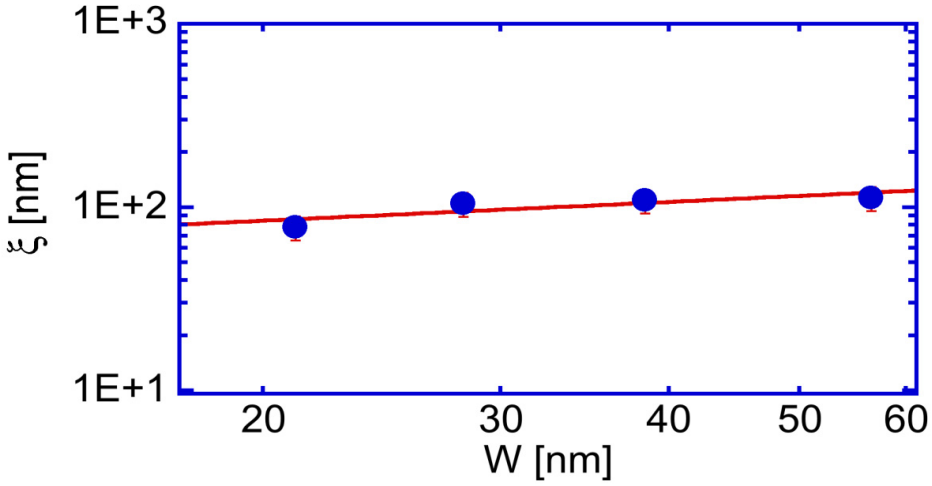

Figure 5.12: Log-log variation of interface width (W) with lateral correlation length (ξ). Solid curve represents the least-squares fit of the power equation to the data points as $\xi \sim W^{\gamma}$ with exponent $\gamma = 0.34 \pm 0.03$.

Figure 5.12 shows the variation of lateral correlation length (ξ) vs interface width (W) and found to follow a power law behavior as $\xi \sim W^{\gamma}$, with exponent $\gamma = 0.34 \pm 0.03$. Mounded surface formation depends on the upward diffusion of the molecule and the diffusion at step edge barrier (Ehrlich–Schwoebel barrier) [57]. However, the formation of smooth film is essentially guided by lateral diffusion of the molecules. Therefore, the competition between these two growth processes determines if the film to be smooth or rough. The diffusion activation energies along vertical and lateral growth direction are expected to be different. Power law behavior of ξ and W represents the relative growth that determines the film morphology. The parameter γ may be attributed to a factor relating to the diffusion activation energies along vertical and lateral diffusion of the molecules. It is to be noted that ξ and W do not follow Arrhenius behavior as the temperature increases within the

TH-1322_10612101

range of this measurements. This is the signature of smooth film growth since both the value of ξ and W decrease as temperature increases. However, the measured value of the ξ and W increased when substrate temperature increased to 120 °C. In this case, the crystalline quality of the film may be improved due to enhanced diffusion of the molecule, but at the same time, the film becomes rough and discontinuous due to the formation of large number of holes as shown in the AFM images in Figure 5.6(d). The rapid roughening by the formation of pores in the films at 120 °C substrate temperature may be attributed to lateral in-homogeneities in the molecular arrangement in the film at higher growth temperature. Desorption of the molecules at higher growth temperature may also destabilize the film. Therefore, OFETs fabricated at 120 °C substrate temperature is expected to showed poor carrier mobility as observed.

5.4 Summary & Conclusions

In this work, we have studied the growth of PTCDI-Ph films on both SiO_2 and bilayer dielectric of organic-inorganic combination. The substrate temperature during the growth has been varied. We observed higher carrier mobility of 0.021 cm^2/Vs for the OFETs fabricated with the PTCDI-Ph films grown at 90 °C substrate temperature. We have studied the evolution of surface morphology as the substrate temperature increases and observed a higher lateral diffusion that makes the film smooth. As a result, the carrier mobility improves with the growth temperature. However, very high substrate temperature makes the film rough and the carrier mobility reduces. We have demonstrated the correlation between carrier mobility and growth parameters. Reduction in operating voltage and enhancement in carrier mobility achieved by using bilayer dielectric in combination with anodized alumina for 90 °C grown PTCDI-Ph films based devices.

5.5 References

[1] S. Steudel, S. De Vusser, S. De Jonge, D. Janssen, S. Verlaak, J. Genoe, P. Heremans, Influence of the dielectric roughness on the performance of pentacene transistors, Appl. Phys. Lett., 85 (2004) 4400-4402.

TH-1322_10612101

[2] R.T. Weitz, K. Amsharov, U. Zschieschang, E.B. Villas, D.K. Goswami, M. Burghard, H. Dosch, M. Jansen, K. Kern, H. Klauk, Organic n-channel transistors based on core-cyanated perylene carboxylic diimide derivatives, J. Am. Chem. Soc., 130 (2008) 4637-4645.

[3] T. Neumann, D. Danilov, C. Lennartz, W. Wenzel, Modeling disordered morphologies in organic semiconductors, J. Comput. Chem., 34 (2013) 2716-2725.

[4] T.B. Singh, S. Gunes, N. Marjanovic, N.S. Sariciftci, R. Menon, Correlation between morphology and ambipolar transport in organic field-effect transistors, J. Appl. Phys., 97 (2005) 114508-5.

[5] J. Veres, S. Ogier, G. Lloyd, D. de Leeuw, Gate insulators in organic field-effect transistors, Chem. Mater., 16 (2004) 4543-4555.

[6] E. Lim, B.J. Jung, H.K. Shim, T. Taguchi, B. Noda, T. Karnbayashi, T. Mori, K. Ishikawa, H. Takezoe, L.M. Do, Nanoscale thin-film morphologies and field-effect transistor behavior of oligothiophene derivatives, Org. Electron., 7 (2006) 121-131.

[7] G.R. Dholakia, M. Meyyappan, A. Facchetti, T.J. Marks, Monolayer to multilayer nanostructural growth transition in N-type oligothiophenes on Au(111) and implications for organic field-effect transistor performance, Nano Lett., 6 (2006) 2447-2455.

[8] Y.D. Park, J.A. Lim, H.S. Lee, K. Cho, Interface engineering in organic transistors, Mater. Today, 10 (2007) 46-54.

[9] H.L. Cheng, W.Y. Chou, C.W. Kuo, Y.W. Wang, Y.S. Mai, F.C. Tang, S.W. Chu, Influence of electric field on microstructures of pentacene thin films in field-effect transistors, Adv. Funct. Mater., 18 (2008) 285-293.

[10] B.A. Jones, A. Facchetti, M.R. Wasielewski, T.J. Marks, Effects of arylene diimide thin film growth conditions on n-channel OFET performance, Adv. Funct. Mater., 18 (2008) 1329-1339.

[11] G. Scavia, W. Porzio, S. Destri, L. Barba, G. Arrighetti, S. Milita, L. Fumagalli, D. Natali, M. Sampietro, Effect of the silanization and annealing on the morphology of thin poly(3-hexylthiophene) (P3HT) layer on silicon oxide, Surf. Sci., 602 (2008) 3106-3115.

[12] M. Watanabe, K. Muro, T. Hamada, T. Tamai, A. Masuyama, H. Naito, K. Matsukawa, Surface Modification of Organic-Inorganic Hybrid Insulator for Printable Organic Field-effect Transistors, Chem. Lett., 38 (2009) 34-35.

TH-1322_10612101

[13] J. Sun, R. Devine, B.M. Dhar, B.J. Jung, K.C. See, H.E. Katz, Improved Morphology and Performance from Surface Treatments of Naphthalenetetracarboxylic Diimide Bottom Contact Field-Effect Transistors, ACS Appl. Mater. Interfaces, 1 (2009) 1763-1769.

[14] X.Y. Cheng, Y.Y. Noh, J.P. Wang, M. Tello, J. Frisch, R.P. Blum, A. Vollmer, J.P. Rabe, N. Koch, H. Sirringhaus, Controlling Electron and Hole Charge Injection in Ambipolar Organic Field-Effect Transistors by Self-Assembled Monolayers, Adv. Funct. Mater., 19 (2009) 2407-2415.

[15] C.A. Di, Y.Q. Liu, G. Yu, D.B. Zhu, Interface Engineering: An Effective Approach toward High-Performance Organic Field-Effect Transistors, Acc. Chem. Res., 42 (2009) 1573-1583.

[16] S.H. Kim, M. Jang, H. Yang, C.E. Park, Effect of pentacene-dielectric affinity on pentacene thin film growth morphology in organic field-effect transistors, J. Mater. Chem., 20 (2010) 5612-5620.

[17] H. Yang, C. Yang, S.H. Kim, M. Jang, C.E. Park, Dependence of Pentacene Crystal Growth on Dielectric Roughness for Fabrication of Flexible Field-Effect Transistors, ACS Appl. Mater. Interfaces, 2 (2010) 391-396.

[18] M.J. Kim, H.W. Heo, Y.K. Suh, C.K. Song, Morphology control of TIPS-pentacene grains with inert gas injection and effects on the performance of OTFTs, Org. Electron., 12 (2011) 1170-1176.

[19] N.B. Kolhe, R.N. Devi, S.P. Senanayak, B. Jancy, K.S. Narayan, S.K. Asha, Structure engineering of naphthalene diimides for improved charge carrier mobility: self-assembly by hydrogen bonding, good or bad?, J. Mater. Chem., 22 (2012) 15235-15246.

[20] S.S. Dharmapurikar, A. Arulkashmir, C. Das, P. Muddellu, K. Krishnamoorthy, Enhanced Hole Carrier Transport Due to Increased Intermolecular Contacts in Small Molecule Based Field Effect Transistors, ACS Appl. Mater. Interfaces, 5 (2013) 7086-7093.

[21] X.N. Zhang, E. Barrena, D. Goswami, D.G. de Oteyza, C. Weis, H. Dosch, Evidence for a Layer-Dependent Ehrlich-Schwobel Barrier in Organic Thin Film Growth, Phys. Rev. Lett., 103 (2009) 136101-4.

[22] Y. Zhang, E. Barrena, X.N. Zhang, A. Turak, F. Maye, H. Dosch, New Insight into the Role of the Interfacial Molecular Structure on Growth and Scaling in Organic Heterostructures, J. Phys. Chem. C, 114 (2010) 13752-13758.

TH-1322_10612101

[23] X.N. Zhang, E. Barrena, D.G. de Oteyza, H. Dosch, Transition from layer-by-layer to rapid roughening in the growth of DIP on SiO(2), Surf. Sci., 601 (2007) 2420-2425.

[24] C. Du, W.C. Wang, L.Q. Li, H. Fuchs, L.F. Chi, Growth of rubrene crystalline thin films using thermal annealing on DPPC LB monolayer, Org. Electron., 14 (2013) 2534-2539.

[25] X.X. Liu, X.Y. Qi, J.H. Gao, S.F. Zou, H.X. Zhang, W.L. Hao, Z.Z. Zang, H.X. Li, W.P. Hu, Dialkylated dibenzotetrathienoacene derivative as semiconductor for organic field effect transistors, Org. Electron., 15 (2014) 156-161.

[26] A. Dodabalapur, L. Torsi, H.E. Katz, Organic Transistors - 2-Dimensional Transport and Improved Electrical Characteristics, Science, 268 (1995) 270-271.

[27] R.P. Ortiz, A. Facchetti, T.J. Marks, High-k Organic, Inorganic, and Hybrid Dielectrics for Low-Voltage Organic Field-Effect Transistors, Chem. Rev., 110 (2010) 205-239.

[28] L.A. Majewski, R. Schroeder, M. Grell, Flexible high capacitance gate insulators for organic field effect transistors, J. Phys. D: Appl. Phys., 37 (2004) 21-24.

[29] C. Tanase, P.W.M. Blom, D.M. de Leeuw, E.J. Meijer, Charge carrier density dependence of the hole mobility in poly(p-phenylene vinylene), Phys Status Solidi A, 201 (2004) 1236-1245.

[30] G. Horowitz, Organic thin film transistors: From theory to real devices, J. Mater. Res., 19 (2004) 1946-1962.

[31] M.A. Alam, A. Dodabalapur, M.R. Pinto, A two-dimensional simulation of organic transistors, IEEE Trans. Electron Devices, 44 (1997) 1332-1337.

[32] L.A. Majewski, R. Schroeder, M. Grell, One volt organic transistor, Adv. Mater., 17 (2005) 192-196.

[33] J. Park, S.Y. Park, S.O. Shim, H. Kang, H.H. Lee, A polymer gate dielectric for high-mobility polymer thin-film transistors and solvent effects, Appl. Phys. Lett., 85 (2004) 3283-3285.

[34] S. Kobayashi, T. Nishikawa, T. Takenobu, S. Mori, T. Shimoda, T. Mitani, H. Shimotani, N. Yoshimoto, S. Ogawa, Y. Iwasa, Control of carrier density by self-assembled monolayers in organic field-effect transistors, Nat. Mater., 3 (2004) 317-322.

[35] C. Kim, A. Facchetti, T.J. Marks, Polymer gate dielectric surface viscoelasticity modulates pentacene transistor performance, Science, 318 (2007) 76-80.

TH-1322_10612101

[36] Y. Jang, D.H. Kim, Y.D. Park, J.H. Cho, M. Hwang, K.W. Cho, Low-voltage and high-field-effect mobility organic transistors with a polymer insulator, Appl. Phys. Lett., 88 (2006) 072101-072103.

[37] J. Puigdollers, C. Voz, A. Orpella, R. Quidant, I. Martin, M. Vetter, R. Alcubilla, Pentacene thin-film transistors with polymeric gate dielectric, Org. Electron., 5 (2004) 67-71.

[38] I. Horcas, R. Fernandez, J.M. Gomez-Rodriguez, J. Colchero, J. Gomez-Herrero, A.M. Baro, WSXM: A software for scanning probe microscopy and a tool for nanotechnology, Rev. Sci. Instrum., 78 (2007) 013705-013708.

[39] L.L. Chua, J. Zaumseil, J.F. Chang, E.C.W. Ou, P.K.H. Ho, H. Sirringhaus, R.H. Friend, General observation of n-type field-effect behaviour in organic semiconductors, Nature, 434 (2005) 194-199.

[40] D.J. Gundlach, K.P. Pernstich, G. Wilckens, M. Gruter, S. Haas, B. Batlogg, High mobility n-channel organic thin-film transistors and complementary inverters, J. Appl. Phys., 98 (2005) 064502-8.

[41] S.E. Fritz, T.W. Kelley, C.D. Frisbie, Effect of Dielectric Roughness on Performance of Pentacene TFTs and Restoration of Performance with a Polymeric Smoothing Layer, The Journal of Physical Chemistry B, 109 (2005) 10574-10577.

[42] Y. Jung, R.J. Kline, D.A. Fischer, E.K. Lin, M. Heeney, I. McCulloch, D.M. DeLongchamp, The Effect of Interfacial Roughness on the Thin Film Morphology and Charge Transport of High-Performance Polythiophenes, Adv. Funct. Mater., 18 (2008) 742-750.

[43] A.-L. Barabási, H.E. Stanley, Fractal Concepts in Surface Growth, Cambridge University Press, Cambridge, 1995.

[44] J. Lapujoulade, The roughening of metal surfaces, Surf. Sci. Reports . 20 (1994) 191-249.

[45] M. Pelliccione, T.-M. Lu, Evolution of thin film morphology: modeling and simulation, Springer-Verlag, New York, 2008.

[46] Y. Zhao, G.-C. Wang, T.-M. Lu, Characteriztion of Amorphus and Crystalline Rough Surface: Principles and Application, Academic Press, London, 2001.

[47] T.-M.L. M. Pelliccione, Evolution of thin film morphology: modeling and simulation, Springer-Verlag, New York, 2008.

TH-1322_10612101

[48] J.H. Jeffries, J.-K. Zuo, M.M. Craig, Instability of Kinetic Roughening in Sputter-Deposition Growth of Pt on Glass, Phys. Rev. Lett., 76 (1996) 4931-4934.

[49] M. Pelliccione, T. Karabacak, C. Gaire, G.-C. Wang, T.-M. Lu, Mound formation in surface growth under shadowing, Phys. Rev. B., 74 (2006) 125420-125410.

[50] D.P. Datta, T.K. Chini, Atomic force microscopy study of 60-keV Ar-ion-induced ripple patterns on Si(100), Physical Review B, 69 (2004) 235313-7.

[51] A. Pal, J.C. Mahato, B.N. Dev, D.K. Goswami, Roughening in electronic growth of ag on si(111)-(7x7) surfaces, ACS Appl Mater Interfaces, 5 (2013) 9517-9521.

[52] J. Kim, D.G. Cahill, R.S. Averback, Surface morphology of Ge(111) during etching by keV ions, Phys Rev B, 67 (2003) 045404-6.

[53] Z. Lai, S. Das Sarma, Kinetic growth with surface relaxation: Continuum versus atomistic models, Phys. Rev. Lett., 66 (1991) 2348-2351.

[54] D.E. Wolf, J. Villain, Growth with Surface-Diffusion, Europhys. Lett., 13 (1990) 389-394.

[55] F. Biscarini, P. Samori, O. Greco, R. Zamboni, Scaling behavior of anisotropic organic thin films grown in high vacuum, Phys. Rev. Lett., 78 (1997) 2389-2392.

[56] Y.P. Zhao, J.B. Fortin, G. Bonvallet, G.C. Wang, T.M. Lu, Kinetic roughening in polymer film growth by vapor deposition, Phys. Rev. Lett., 85 (2000) 3229-3232.

[57] M. Siegert, M. Plischke, Slope Selection and Coarsening in Molecular-Beam Epitaxy, Phys. Rev. Lett., 73 (1994) 1517-1520.

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TH-1322_10612101

Chapter VI

PTCDI-Ph Based Low – Operating Voltage OFETs with Metal – Oxide Gate Dielectrics

6.1 Introduction

One of the fundamental and powerful electronic devices in semiconductor electronic industry is field effect transistor (FET) since it is the elementary component for the fabrication of large-scale electronics. In organic electronics, integrated circuits (ICs) fabricated with OFETs offer the potential of enabling extremely cheap, adequately performing logic circuits with applications in mechanically flexible, postage stamps, radiofrequency identification (RFID) tags, smart cards and large-area electronic devices [1-5]. For successful integration of OFETs into ICs using both hole-transporting (*p*-type) and electron-transporting (*n*-type) organic semiconductors require achieving low-power complementary logic circuits [6-8]. The performance of *n*-type materials had fallen behind that of their p-type counterparts until recent years due to the less air stability and for high voltage operation [9, 10]. Nevertheless, the carrier mobility μ of *n*-type OFETs is generally much lower than that of *p*-type OFETs [11-14]. The *n*-type OFETs very often suffer from high threshold voltages, which is a serious disadvantage for the development of low-power-consuming organic complementary circuits. Therefore, in parallel to the effort of improving the carrier mobility of the conventional OFETs, it is necessary to work on the device architecture for successful implementation of low voltage operation. Few reports have been demonstrated the low-voltage-operating *n*-type OFETs by using high dielectric-constant insulators [15-18] or dielectric layers of ultrathin self-assembled monolayers [19-23]. However, although various high-performance *n*-type organic semiconducting materials have

TH-1322_10612101

been reported, most of them can only deliver OFETs that can be operated under vacuum or under an inert atmosphere. Only a few of them, that is, hexadeca-halogenated metal phthalocyanine, perylene and naphthalene diimides with electron-withdrawing groups, have been claimed to allow fabrication of devices that are relatively stable in air [24-27]. In this part of the thesis work, we have studied several *n*-type OFETs fabricated with PTCDI-Ph molecules as active channel and demonstrated their low voltage operation together with their highly air stability.

SiO_2 as gate dielectric layer is regularly being used for the fabrication of microelectronic devices [28, 29]. Being a material with low dielectric constant ($k \sim 3.9$) [30], the capacitance of the dielectric layer is lower. In order to increase the capacitance, one needs to decrease the thickness of the layer. However, thinner layer shows huge leakage current. On the other hand, the thicker SiO_2 layer shows poor field-effect properties. As a result, the operating voltage of the devices increases. In this chapter, we describe the fabrication of low operating voltage OFETs by using bilayer dielectric. The bilayer system is the combination of two metal oxide layers. These materials are of high dielectric constant and show exceptional field-effect in the OFETs [15, 16, 31-36]. In practice, the typical fabrication routes for high-*k* metal-oxide dielectrics are expensive growth techniques such as atomic layer deposition [37], radio-frequency magnetron sputtering [38] and chemical vapor deposition [39]. However, we have used chemical synthesis root together with anodization method for the fabrication of the dielectric layers of the OFETs.

There are numerous high-*k* inorganic metal-oxides are available. Among those metal-oxides, TiO_2, $BaTiO_3$, $SrTiO_3$ and $BaSrTiO_3$ are known to have the highest *k* values. However, the conduction band energies of these materials are very close to the Fermi energies of the contact materials (Ag and Al) that we used for the fabrication of the devices. Therefore, the defect states usually very close to band edge of the dielectric layers become easy access to the contact materials for electron conduction. As a result, a huge leakage current through metal-oxides alone as dielectric layer is expected. Therefore, we have chosen high band gap materials with conduction band edge away from contact Fermi energy of the contact materials as the second layer in the combination. Al_2O_3 has been used as this can be easily fabricated using anodization method as described before. The schematic of band

TH-1322_10612101

diagram for the bilayer dielectric used for the fabrication of the OFETs are shown in Figure 6.1. All other metal-oxide layers used in this work were fabricated using spin coating metal-oxide sols. In this chapter, we present our result on the fabrication of PTCDI-Ph based OFETs which exhibit a low operating voltage of about 1.5 V. In case of SiO_2 as dielectric layer, the operating voltage of the OFETs was about 30 V.

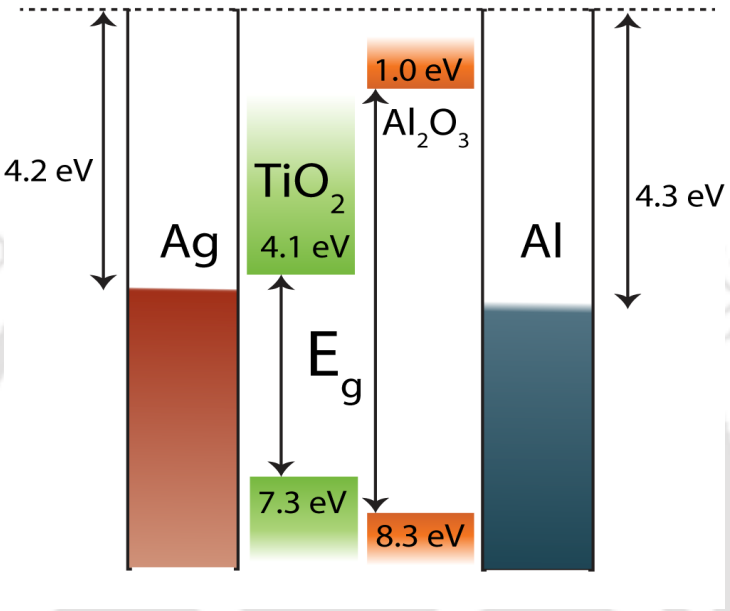

Figure 6.1: Energy band diagram of bilayer dielectric system of TiO_2/Al_2O_3 with silver (Ag) and aluminum (Al) electrodes.

6.2 Experimental Details

In this section, we described the procedure to synthesis of different solution processable metal-oxide by sol-gel method. We also elaborated the fabrication technique of PTCDI-Ph based OFETs.

6.2.1 Synthesis of Metal – Oxide Precursor Sols

TiO_x Precursor Sol Synthesis: A well known sol-gel method was followed to synthesis titanium oxide (TiO_x) sol [40]. It was prepared by dissolving titanium (IV) isopropoxide (TIP) ($Ti(OC_3H_7)_4$, 99.99%, Sigma-Aldrich) into a mixture of methanol and acetic acid in a concentration of about 0.1 mol/L, and then vigorously stirred for 24 h in ambient conditions.

TH-1322_10612101

The prepared final TiO_x sol then stored at room temperature for the further process. The maximum dielectric constant reported for TiO_2 film annealed at 700 ºC is 82 [41].

Synthesis of Barium Titanate ($BaTiO_X$; BTO) Precursor Sols: Barium acetate ($(CH_3COO)_2Ba$) and titanium (IV) isopropoxide (99.99%, Sigma-Aldrich) were used as precursor materials. Glacial acetic acid (99.8%, Merck Chemicals) and 2-methoxyethanol (>99 %, Merck Chemicals) were used as solvents, stabilizers, and chelating agents. Two stock solutions were made. A barium-acetate solution was prepared by dissolving barium acetate in acetic acid and subsequent refluxing at 120 °C for 8 h to remove all remaining water. The final concentration was adjusted to 1.0 mol/dm^3. The second stock solution was based on titanium iso-propoxide with 2-methoxyethanol as solvent, yielding a precursor concentration of 1.0 mol/dm^3. Both stock solutions were stirred at room temperature for 24 h. They were then stored at room temperature. We have followed the synthesis procedure describe in references [42-44]. Prior to the experiments, the stock solutions were mixed in 1:1 molar ratios and stirred for 10 min, yielding a concentration of 0.50 mol/dm^3 in the final $BaTiO_x$ (BTO) precursor solution. In the next step they were diluted with 2-methoxyethanol to reach a concentration of 0.1 mol/dm^3 in the final BTO precursor solution. BTO precursor sols of 0.1 mol/dm^3 were spin-cast onto Al_2O_3 substrates at 6000 rpm for 60 s. The as-prepared films were dried on a hot-stage at 200 °C for 15 min. The maximum reported value of dielectric constant for BTO film grown by solution process at 100 KHz frequency is 600 [45].

Synthesis of $SrTiO_x$ and $BaSrTiO_x$ Sols: The procedure for synthesizing $SrTiO_x$ (STO) (reported dielectric constant is 250 [46]) and $BaSrTiO_x$ (BST) sols (dielectric constant reported as 800 [47]) are similar as BTO sol preparation as described before. For STO synthesis, strontium acetate ($(CH_3COO)_2Sr$) has been used in place of barium acetate in BTO synthesis and for BST synthesis, both barium and strontium acetates were dissolved in 1:1 ratio [48]. The final precursor has been stored at room temperature for the further use.

6.2.2 OFET Fabrication

Prior to dielectric layer deposition, 300 nm aluminum (Al) was deposited on ultrasonically cleaned glass substrates and anodized to create 10 nm alumina (Al_2O_3) layers.

TH-1322_10612101

These surfaces were immediately spin-coated at 6000 rpm for 60 sec with freshly prepared metal-oxide sols. These films were heated to 200 ºC for 10 min. We have used a very slow rate of heating to achieve 200 ºC, which is about 2 hours to ensure the hydrolyzation and decomposition of the precursor.

After deposition of the dielectric layers, bottom gate, top contact OFETs were fabricated by vacuum deposition of PTCDI-Ph (80 ± 5 nm, ~ 10^{-6} mbar base pressure, 1.2 Å/s growth rate) onto the substrates at the substrate temperature of 90 ºC, followed by thermal evaporation of silver as source (*S*) – drain (*D*) electrodes (70 nm thick) through a shadow mask with dimensions of *L* (channel length) = 50 µm and *W* (channel width) = 1000 µm.

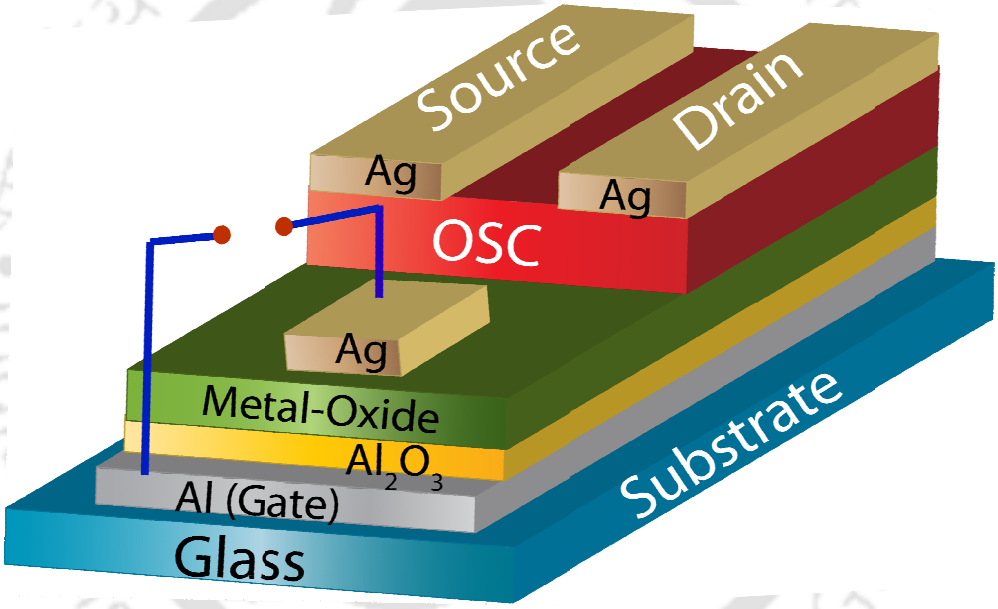

Figure 6.2: Typical design of OFET on bilayer gate dielectric system with metal-insulator-metal (MIM) capacitor.

As for leakage and capacitance characterizations, a metal-insulator-metal (MIM) capacitor was fabricated along with OFET by direct deposition of 70 nm thick rectangular silver electrode with dimensions of 1.0 × 0.5 mm^2 onto the single layer of metal–oxide and bilayer with Al_2O_3 dielectric system through a shadow mask. Both the capacitor and OFET fabrications were done on same substrate and the schematic representations of MIM and OFET with bilayer dielectric system is shown in Figure 6.2. The electrical characterizations like capacitance, leakage current, transistor output and transfer characteristics were carried

TH-1322_10612101

out by means of semiconductor parameter analyzer with micro-probe station. The surface morphology of the solution-processed dielectrics and PTCDI-Ph film was characterized by atomic force microscopy (AFM) in tapping mode.

6.3 Results and Discussions

6.3.1 Fabrication of OFETs using TiO_x /Al_2O_3 as bilayer gate dielectric

We have studied the morphology of the films during every steps of OFETs fabrication using bilayer dielectric system to understand the effect of the interface on the devices. Smooth interfaces are required for the better molecular packing within the films. Anodized Al_2O_3 surfaces are found to be very rough as shown in Figure 6.3(a). The observed rms roughness is ~ 5.4 nm. These surfaces are shown huge leakage current [14]. The single TiO_x layer grown on glass substrates (see Figure 6.3(b)) shows smooth film with rms roughness of ~0.2 nm., This surface is as smooth as that of the SiO_2 (rms roughness ~0.19 nm) and glass (rms roughness ~ 0.31 nm) substrates. However, TiO_x layer on Al_2O_3 exhibits rougher surface than single layer TiO_x and the rms roughness is 1.3 nm. Figure 6.3(c) is showing the morphology of TiO_x surface grown on Al_2O_3 surface. Since the surface roughness of anodized alumina is more, the roughness of TiO_x film grown on it appears to be little rougher than single TiO_x film grown on glass substrate. The roughness of the dielectric surfaces significantly influences the growth of the subsequent layer grown on top and this essentially affect the performance of the OFETs fabricated with such dielectric systems [49-52]. This induces physical traps for charge carriers [53], and the charge transport through the devices are affected. Nevertheless, smooth interfaces also enhance the capacitive coupling between gate and the active channel. This can reduce the threshold voltage of the devices. Therefore, the smooth surface of the hybrid dielectric layer TiO_x/Al_2O_3 is crucial for high performance OFETs. The surface morphology of PTCDI-Ph film on bilayer dielectric can be seen in Figure 6.3(d). The rms roughness of this surface is ~ 15.3 nm. We have observed interconnected grains forming percolated type structures. These films were used as active channel for the fabrication of OFETs. To characterize the electrical properties of the solution-processed dielectric, we have fabricated Ag/metal-oxides/Al (MIM) sandwiched structure to

TH-1322_10612101

estimate the leakage current and the variation of capacitance with increased frequency. A typical schematic structure is shown in Figure 6.2.

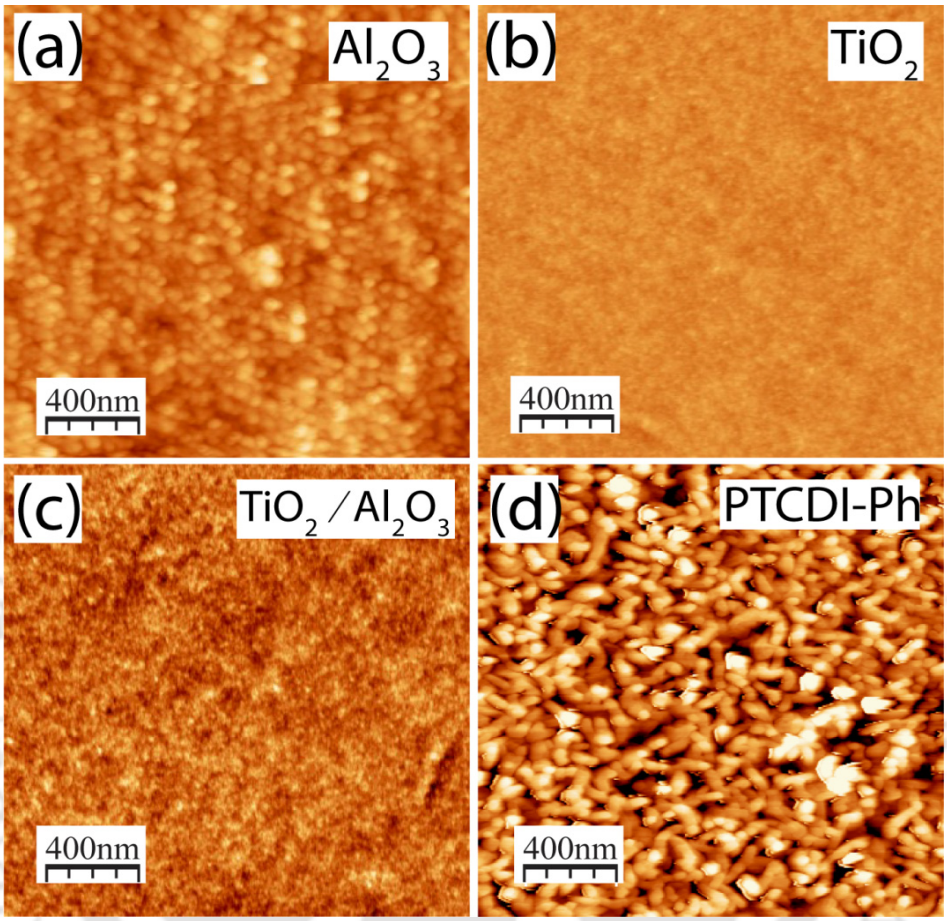

Figure 6.3: Tapping mode AFM images of **(a)** Anodized alumina (Al_2O_3), **(b)** Single layer of TiO_x, **(c)** TiO_x/Al_2O_3 bilayer and **(d)** PTCDI-Ph on bilayer dielectric surfaces.

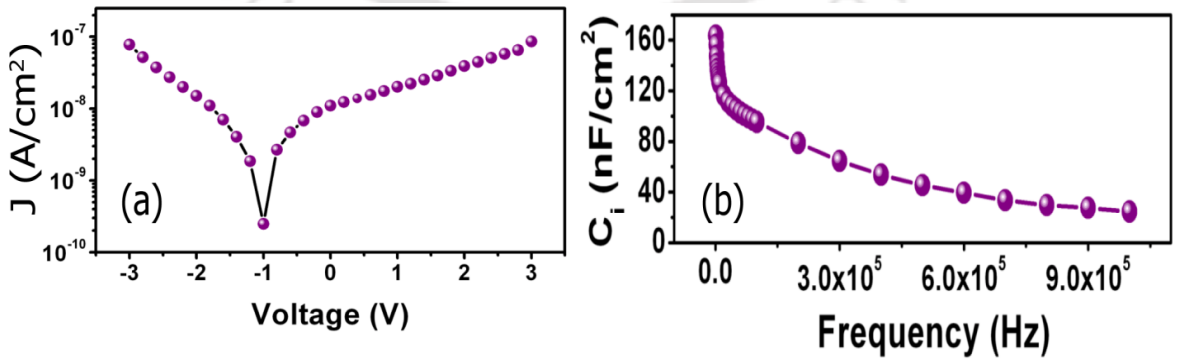

Figure 6.4: (a) Leakage current density and **(b)** Frequency dependent capacitance of parallel plate capacitor with TiO_x/Al_2O_3 bilayer dielectric system.

Figure 6.4(a) shows the typical leakage current density versus bias voltage plots of bilayer dielectric system containing 30nm TiO_x and 10 nm Al_2O_3. As can be seen from Figure 6.4, the bilayer dielectric system exhibits current density of $\sim 10^{-7}$ A/cm^2 at ±3 V. The variation of measured capacitance at 3 V bias is shown in Figure 6.3(b) for the frequency ranges from 10 kHz to 1 MHz. The typical capacitance used for the fabrication of the OFETs is 52 nF/cm^2 at 100 kHz.

We have used the same thickness of the dielectric layer as MIM system for the fabrication of OFETs. The active channel of PTCDI-Ph molecules were grown at 90 ºC substrate temperature and the typical thickness of the layer is 80 nm, which were optimized for better carrier mobility for the device as reported in the *chapter V*. Figure 6.5 shows the output and transfer characteristics of one of the OFETs fabricated with bilayer TiO_x/Al_2O_3 system as dielectric layer. We have observed significant reduction in operating and threshold voltages for these devices. It is to be noted that the observed operating and threshold voltages for OFETs fabricated with SiO_2 as dielectric layer are 30 V and 5 V, respectively (shown in *chapter V*, Figure 5.1). However, these values obtained from results shown in Figure 6.5 are 2.0 V and 0.55 V, respectively. The results are order of magnitude less than the earlier. The carrier mobility obtained is 0.012 cm^2/Vs.

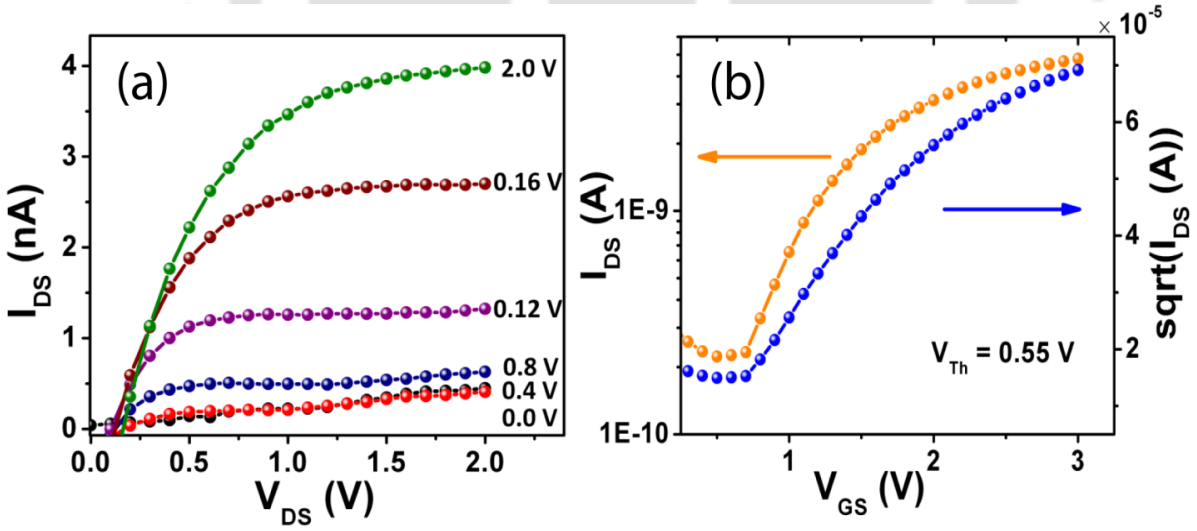

Figure 6.5: (**a**) Output and (**b**) transfer characteristics of OFET designed with TiO_x/Al_2O_3 bilayer dielectric.

TH-1322_10612101

6.3.2 OFETs based on $BaTiO_x$/ Al_2O_3 as dielectric layer

Barium titanate (BTO) was used for the fabrication of PTCDI-Ph based OFETs. BTO nanoparticle based sol was synthesized, the anodized Al_2O_3 layers were coated with this sol using spin coating technique. The thickness of this layer is about 30 nm. In this section we describe the fabrication and characterization of OFETs using BTO/Al_2O_3 as dielectric layer. Figure 6.6 is the representative tapping mode AFM topographic images of surfaces of BTO film grown on Al_2O_3. The rms roughness of this film is 0.42 nm. PTCDI-Ph films of 80 nm thicknesses were grown on this surface. We have observed the formation of islands, which make the films very rough with rms roughness 9.53 nm. As a result, charge transport through this film would be essentially through the wetting layer under the islands and the carrier mobility of the devices fabricated with this film is expected to be poor. In order to measure leakage current and capacitance through the BTO/Al_2O_3 dielectric layer, we fabricated MIM structures. The measured leakage current and capacitance densities for Ag/BTO/Al_2O_3/Al are ~10^{-8} A/cm^2 (see Figure 6.7) and 56 nF/cm^2, respectively.

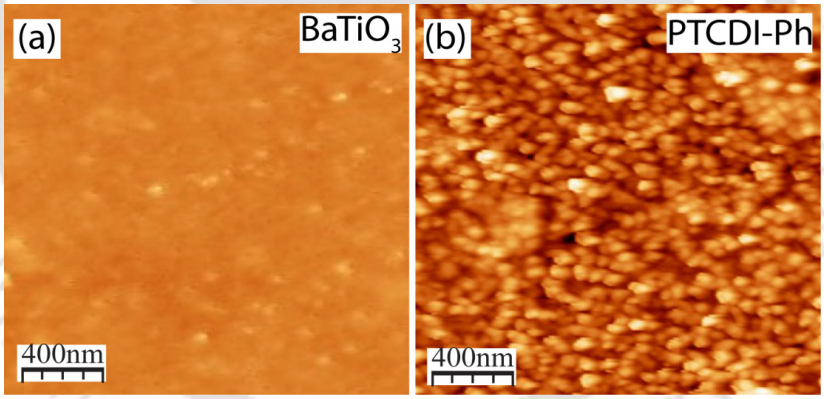

Figure 6.6: Tapping mode AFM topography of **(a)** BTO/Al_2O_3 and **(b)** PTCDI-Ph on BTO/Al_2O_3 bilayer system.

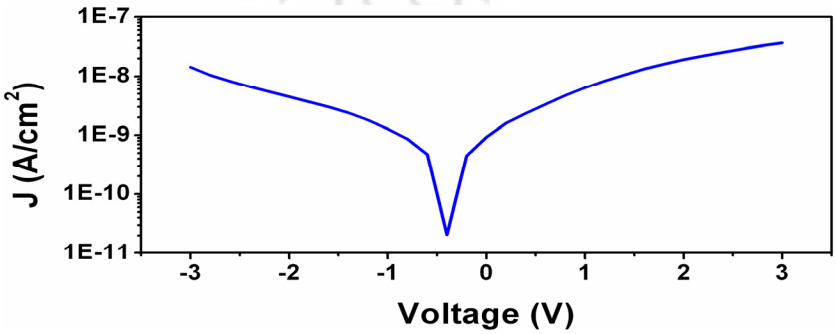

Figure 6.7: Leakage current response with applied voltage of Ag/BTO/Al_2O_3/Al capacitor.

The transistor output characteristics were measured for drain sweep voltages at different gate voltage steps are shown in Figure 6.8(a). Figure 6.8(b) shows the transfer characteristics of the designed device. The electron mobility (μ), operating voltage and threshold voltages (V_{TH}) are estimated from Figure 6.8 as 0.016 cm^2/V-s, 2.0 V and 0.7 V, respectively. We have not observed significant changes in the performance of the OFETs fabricated with TiO_x/Al_2O_3 and BTO/Al_2O_3 as dielectric layer. However, OFETs fabricated TiO_x/Al_2O_3 showed relatively lower threshold voltage. Though, the roughness of the TiO_x films is higher, the PTCDI-Ph film morphology on this surfaces showed percolated type growth forming a more uniform film. As a result, gate filed-effect improved in this case.

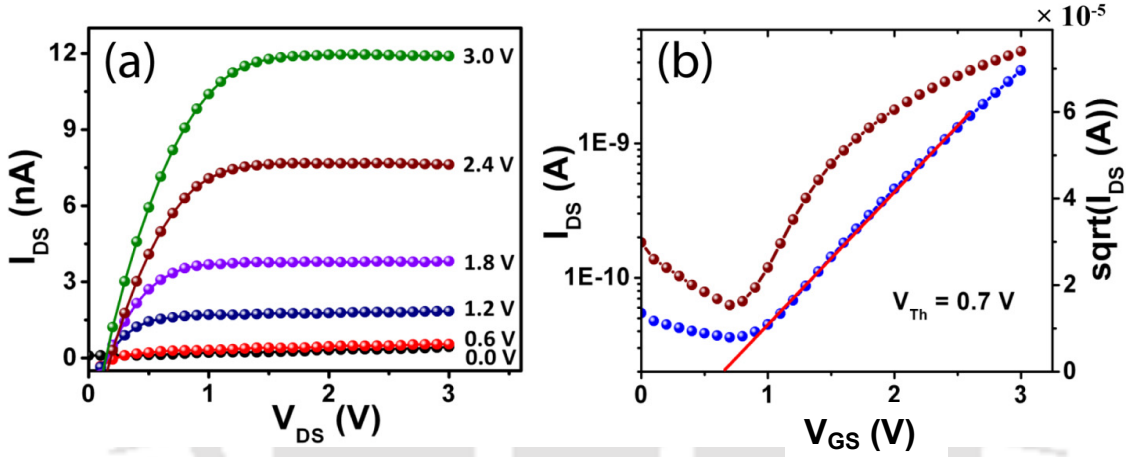

Figure 6.8: Transistor output and transfer characteristics of PTCDI-Ph OFET with BTO/Al_2O_3 bilayer dielectric system.

6.3.3 OFETs based on $SrTiO_x$/ Al_2O_3 as dielectric layer

In this section we report the fabrication of OFETs based on $SrTiO_x$ (STO)/Al_2O_3 as dielectric layer. The dielectric properties of the 40 ± 5 nm thick bilayer of STO (30nm)/Al_2O_3 (10nm) were characterized by using parallel plate capacitors of various plate areas. The capacitors were fabricated with Ag & Al electrodes patterned through a shadow mask. Figure 6.9 shows a typical design of parallel plate capacitors of both STO and bilayer of STO/ Al_2O_3. The capacitance density obtained for STO/Al_2O_3 bilayer system as 65.4nF/cm^2, it is almost constant over the frequencies ranging from 10 KHz – 1MHz (Figure 6.10(a)).

TH-1322_10612101

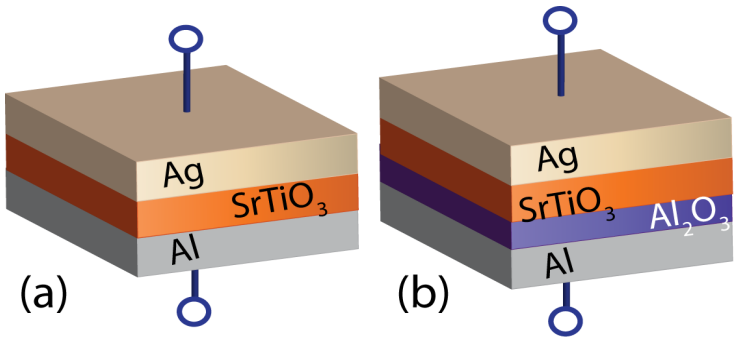

Figure 6.9: Typical designs of metal-insulator-metal (MIM) parallel plate capacitors based on dielectrics of **(a)** single layer STO and **(b)** STO/Al_2O_3 bilayer system.

The leakage current density of the STO/Al_2O_3 film was measured as less than 10^{-8} A/cm^2 whereas for single layer of STO, this value was more than 10^{-4} A/cm^2. A minute shift can be observed in leakage current curves shown in Figure 6.10(b), it might be attributed to the mismatch of Fermi-levels of both the electrodes of parallel plate capacitors. Less band gap of STO (E_g = 3.2eV) [54] causes the huge amount of leakage current through STO single layer and it is controlled due to the blocking of electron conduction path by the Al_2O_3 layer. The merits of Al_2O_3 are its large band gap [55] with excellent thermal stability [56]. This is the reason to have low leakage in bilayer system (4 orders of magnitude less) than single STO.

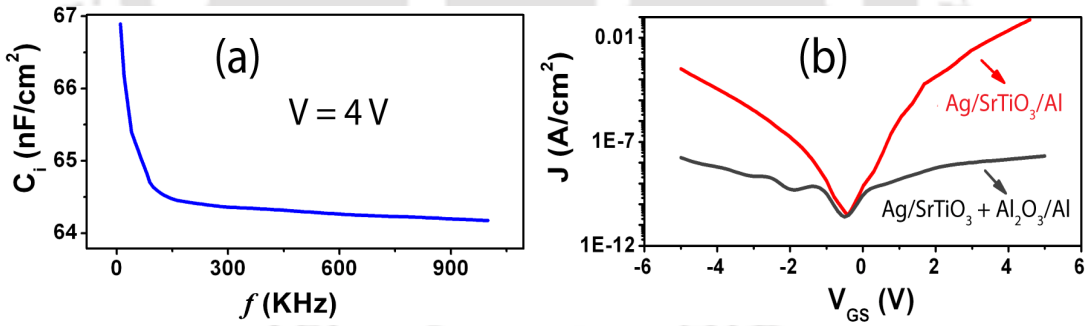

Figure 6.10: (a) Frequency dependent capacitance of STO/Al_2O_3 bilayer dielectric system and **(b)** leakage current plots of both single STO and bilayer dielectric systems.

Surface morphology images of STO/Al_2O_3 bilayer and PTCDI-Ph films grown on the bilayer dielectric system are shown in Figure 6.11 (a-b). The rms roughness of STO surfaces is 0.22 nm, which is very smooth in compare to the other two materials described above. Therefore, this system is expected to show better field-effect in OFETs. Figure 6.12 (a-b) shows the output and transfer characteristics of OFETs based on PTCDI-Ph film as active

TH-1322_10612101

channel with STO/Al_2O_3 bilayer layer as gate dielectric. A drastic improvement in output drain current is observed as shown in Figure 6.12(a). The linearity in the behavior of square root of drain current with gate voltage sweep, in transfer characteristics (see Figure 6.12(b)), reveals efficient performances of the devices.

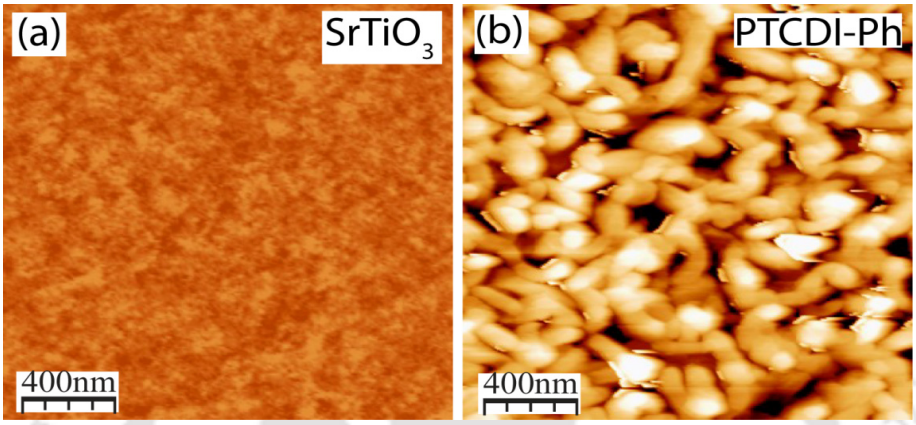

Figure 6.11: (a) STO/Al_2O_3 and **(b)** PTCDI-Ph on STO/Al_2O_3 film surface morphologies obtained from AFM in tapping mode.

The estimated carrier mobility, operating voltage, threshold voltage and on/off ratios obtained for these devices are 0.04 cm^2/V-s, 4 V, 0.31 V and 10^3, respectively. These devices show improved performance in compare to the devices described before. Though the PTCDI-Ph films were found to be rougher than before, but formation of larger grains can improve the crystalline quality of the film, which improves the charge transport through the devices.

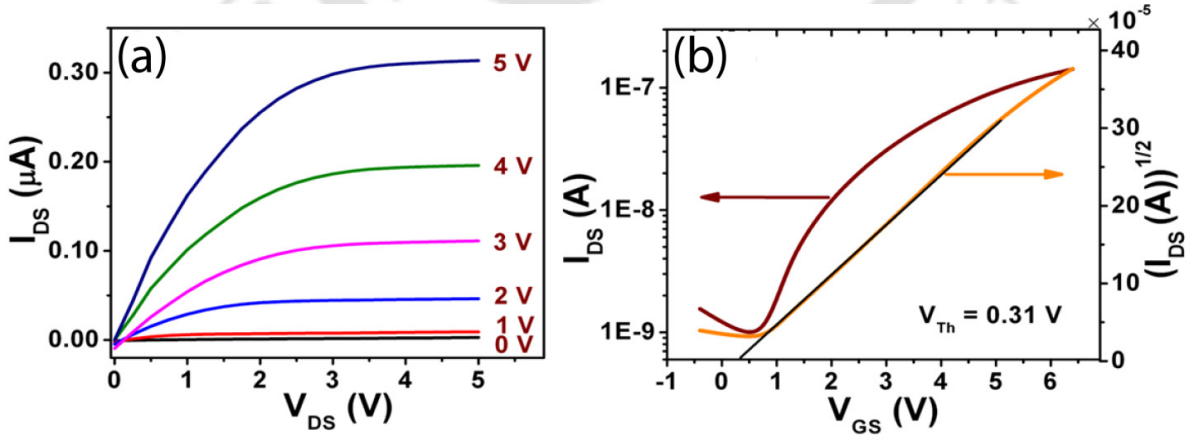

Figure 6.12: OFET (**a**) output and (**b**) transfer characters of device based on STO/Al_2O_3 bilayer system.

TH-1322_10612101

6.3.4 OFETs based on $BaSrTiO_x$ / Al_2O_3 as dielectric layer

In this section we described the results of the OFETs fabricated with $BaSrTiO_x$ (BST)/Al_2O_3 as dielectric layer. BST films were grown on Al_2O_3 films using spin coating technique and PTCDI-Ph films as active channel were grown on dielectric surfaces using thermal evaporation technique as before. The tapping mode topographic AFM images of these two surfaces are shown in Figure 6.13. Similar to BTO and STO, the BST films also found to form smooth surface with rms roughness ~0.35 nm as shown in Figure 6.13(a). Morphology of PTCDI-Ph film on BST dielectric surface can be seen in Figure 6.13(b). We have observed the formation of large grains, which makes the films very rough with rms roughness ~ 23 nm.

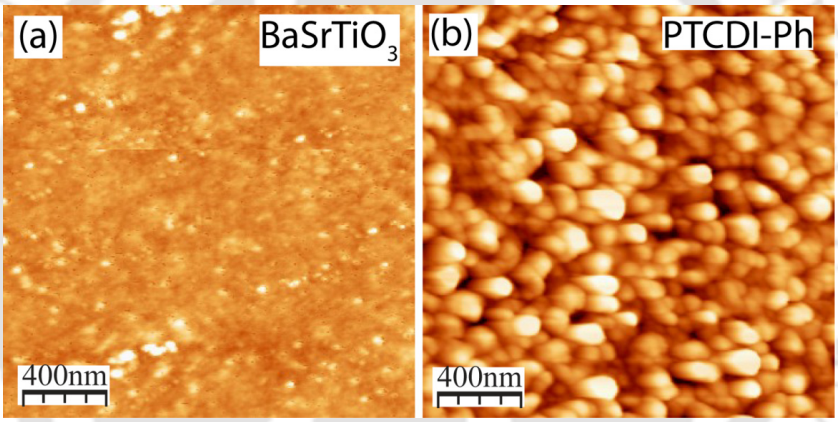

Figure 6.13: AFM tapping mode images of **(a)** BST/Al_2O_3 bilayer system and **(b)** organic molecule PTCDI-Ph thin film on bilayer system.

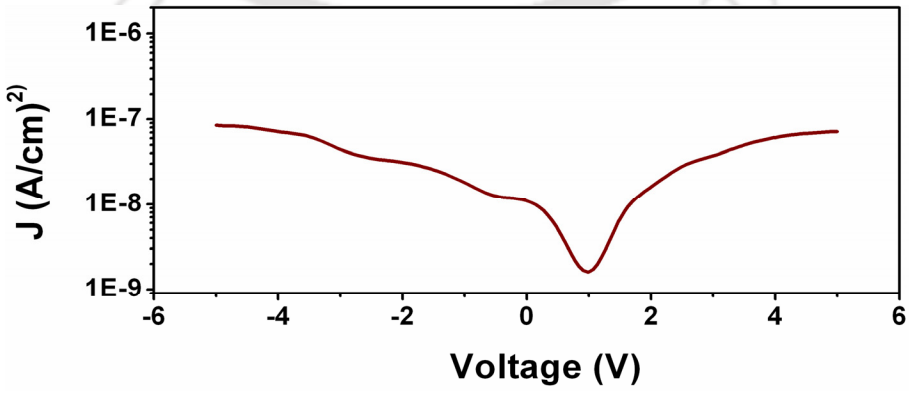

Figure 6.14: Leakage current plot of BST/Al_2O_3 bilayer dielectric systems.

TH-1322_10612101

We have fabricated OFETs using above bilayer system as gate dielectric. Figure 6.15 (a-b) shows the transistor output and transfer characteristic curves. As we can see, the operating voltage and threshold voltage of device are significantly lower and the values are 1.2 V and 0.4 V, which are further improved in compare to the devices reported before. The reduction of operating voltage is the due to high capacitive BST/Al_2O_3 bilayer with capacitance density of 63 nF/cm^2 and very low leakage current density of ~10^{-7} A/cm^2 (Figure 6.14). However, carrier mobility (0.022 cm^2/V-s) is lower than the device fabricated with STO/Al_2O_3 due to the extremely rough active channel.

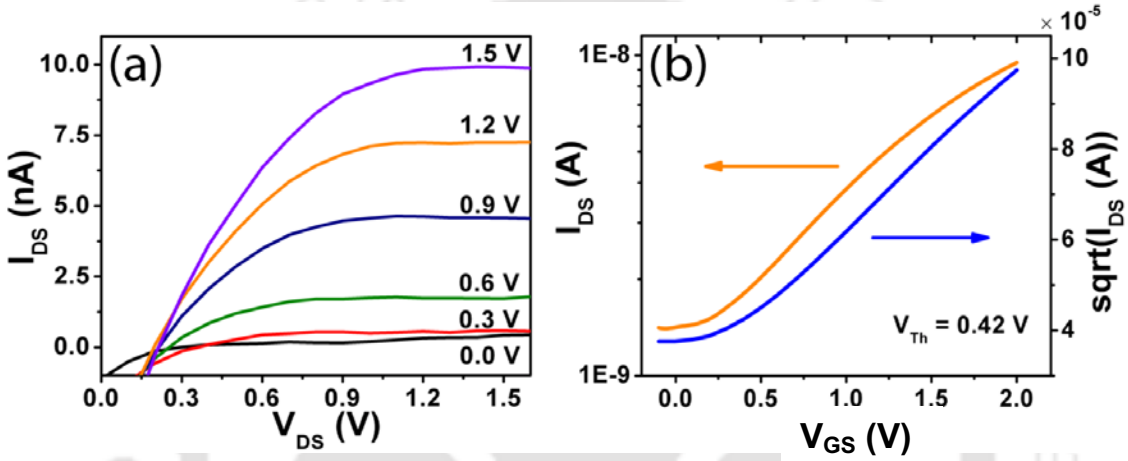

Figure 6.15: OFET **(a)** output and **(b)** transfer characteristics of device based on BST/Al_2O_3 bilayer system.

To demonstrate the effectiveness of our bilayer dielectric system, we have fabricated similar devices with SiO_2 and bilayer dielectrics. Figure 6.16(a) shows the tapping mode AFM image of SiO_2 substrate with root mean square roughness 0.19 nm and Figure 6.16(b) is showing surface morphology of PTCDI-Ph film grown on SiO_2/Si (B-doped, 0.001-0.005 Ω-cm). The film exhibits very rough surface with typical value of rms roughness calculated as 20.4 nm. Figure 6.17 shows the output and transfer characteristics of a PTCDI-Ph thin-film based OFET. From the output characteristics shown in Figure 6.17(a), the continuous shift of drain current near origin can be seen. This is attributed to carrier traps arises due to the rough surface of active layer [53]. The same phenomenon has been reflected in transfer characteristics (shown in Figure 6.17(b)) in terms of high threshold voltage (5 V). The extracted carrier mobility and operating voltages are 0.015 cm^2/V-s and 30 V respectively.

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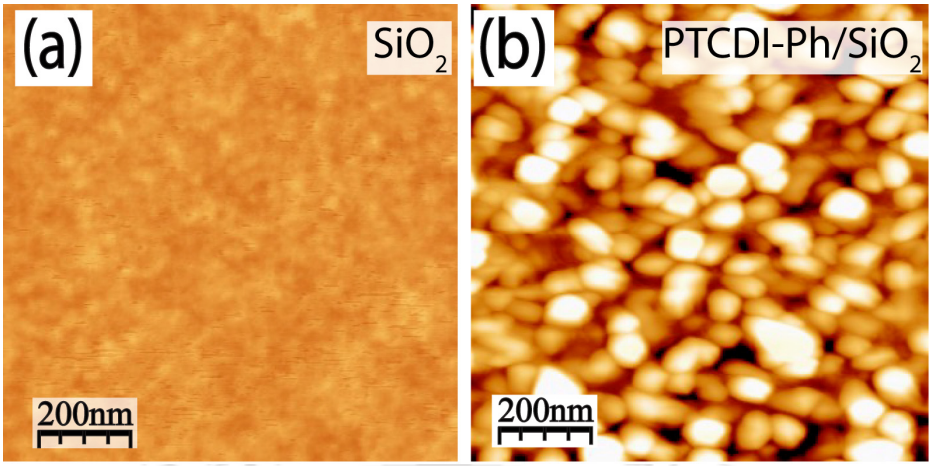

Figure 6.16: AFM topographies of (**a**) SiO_2 and (**b**) PTCDI-Ph on SiO_2 surfaces.

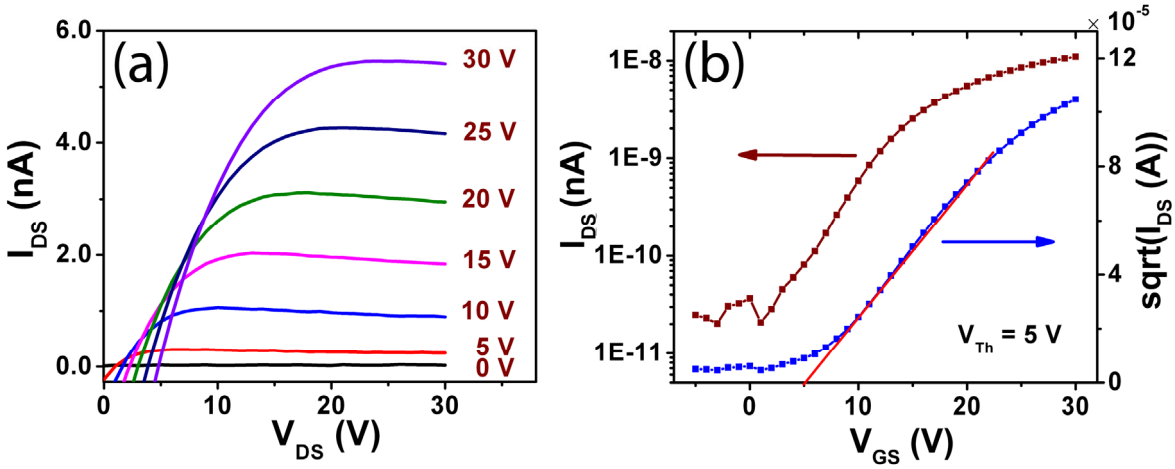

Figure 6.17: OFET **(a)** output and **(b)** transfer characteristics of device based PTCDI-Ph thin film on SiO_2/Si system.

6.4 Summary & Conclusions

In summary, we synthesized the high-*k* metal-oxide dielectrics by sol-gel process and used as a gate dielectric material in combination with anodized alumina. We have successfully achieved low-voltage OFETs by introducing solution-processed high-*k* bilayer systems as the gate dielectric. The bilayer dielectric systems exhibits very smooth surfaces with rms below 1nm, high capacitance about 65 nF/cm^2 and low leakage current densities. Upon using the high-*k* bilayers as the gate dielectrics, PTCDI-Ph based OFETs exhibit electron mobility as high as 0.04 cm^2/V-s and an operation voltage as low as 1.2 V. The

TH-1322_10612101

obtained results for all the transistors are much better than the transistor with traditional SiO_2 dielectric. The summary of transistor parameters has given in following Table 6.1.

S.No	Dielectric System	Surface rms Roughness	Capacitance C_i (nF/cm²)	Threshold Voltage V_{th} (V)	Operating Voltage (V)	Carrier Mobility (cm²/V-s)
01	SiO_2	0.19 nm	9.3	5.00	0 – 30	0.015
02	$BaTiO_3/Al_2O_3$	0.42 nm	56.3	0.71	0 – 2 V	0.012
03	TiO_2/Al_2O_3	1.32 nm	52.2	0.55	0 – 2 V	0.016
04	$SrTiO_3/Al_2O_3$	0.22 nm	64.5	0.31	0 – 4 V	**0.040**
05	$BaSrTiO_3/Al_2O_3$	0.35 nm	63.1	0.42	**0 – 1.2 V**	0.021

6.5 References

[1] G.H. Gelinck, H.E.A. Huitema, E. van Veenendaal, E. Cantatore, L. Schrijnemakers, J.B.P.H. van der Putten, T.C.T. Geuns, M. Beenhakkers, J.B. Giesbers, B.-H. Huisman, E.J. Meijer, E.M. Benito, F.J. Touwslager, A.W. Marsman, B.J.E. van Rens, D.M. de Leeuw, Flexible active-matrix displays and shift registers based on solution-processed organic transistors, Nat Mater, 3 (2004) 106-110.

[2] B. Crone, A. Dodabalapur, Y.Y. Lin, R.W. Filas, Z. Bao, A. LaDuca, R. Sarpeshkar, H.E. Katz, W. Li, Large-scale complementary integrated circuits based on organic transistors, Nature, 403 (2000) 521-523.

[3] H.E. Katz, Recent advances in semiconductor performance and printing processes for organic transistor-based electronics, Chem. Mater., 16 (2004) 4748-4756.

[4] B.J. de Gans, P.C. Duineveld, U.S. Schubert, Inkjet printing of polymers: State of the art and future developments, Adv. Mater., 16 (2004) 203-213.

[5] G. Horowitz, Organic thin film transistors: From theory to real devices, J. Mater. Res., 19 (2004) 1946-1962.

TH-1322_10612101

[6] H. Klauk, Organic thin-film transistors, Chem. Soc. Rev., 39 (2010) 2643-2666.

[7] F. Wurthner, M. Stolte, Naphthalene and perylene diimides for organic transistors, Chem. Commun., 47 (2011) 5109-5115.

[8] X.W. Zhan, A. Facchetti, S. Barlow, T.J. Marks, M.A. Ratner, M.R. Wasielewski, S.R. Marder, Rylene and Related Diimides for Organic Electronics, Adv. Mater., 23 (2011) 268-284.

[9] H. Usta, A. Facchetti, T.J. Marks, n-Channel Semiconductor Materials Design for Organic Complementary Circuits, Acc. Chem. Res., 44 (2011) 501-510.

[10] H.E. Katz, J. Huang, Thin-Film Organic Electronic Devices, Annu. Rev. Mater. Res., 39 (2009) 71-92.

[11] T. Marszalek, M. Wiatrowski, E. Dobruchowska, J. Jung, J. Ulanski, One-step technique for production of bi-functional low molecular semiconductor-polymer composites for flexible OFET applications, J. Mater. Chem. C., 1 (2013) 3190-3193.

[12] A. Petritz, A. Wolfberger, A. Fian, J.R. Krenn, T. Griesser, B. Stadlober, High performance p-type organic thin film transistors with an intrinsically photopatternable, ultrathin polymer dielectric layer, Org. Electron., 14 (2013) 3070-3082.

[13] M. Uno, T. Uemura, Y. Kanaoka, Z.H. Chen, A. Facchetti, J. Takeya, High-speed organic single-crystal transistors gated with short-channel air gaps: Efficient hole and electron injection in organic semiconductor crystals, Org. Electron., 14 (2013) 1656-1662.

[14] M. Gedda, N.V.V. Subbarao, S.M. Obaidulla, D.K. Goswami, High carrier mobility of CoPc wires based field-effect transistors using bi-layer gate dielectric, Aip Adv., 3 (2013) 112123-112127.

[15] A. Facchetti, M.H. Yoon, T.J. Marks, Gate dielectrics for organic field-effect transistors: New opportunities for organic electronics, Adv. Mater., 17 (2005) 1705-1725.

[16] R.P. Ortiz, A. Facchetti, T.J. Marks, High-k Organic, Inorganic, and Hybrid Dielectrics for Low-Voltage Organic Field-Effect Transistors, Chem. Rev., 110 (2010) 205-239.

[17] M. Kitamura, Y. Arakawa, Low-voltage-operating complementary inverters with C-60 and pentacene transistors on glass substrates, Appl. Phys. Lett., 91 (2007) 053505-3.

[18] H. Yan, H. Hanagata, T. Jo, H. Okuzaki, Low-Voltage Organic Field-Effect Transistors Fabricated on Self-Assembled-Monolayer-Free SrTiO3 Insulator, Jpn. J. Appl. Phys., 50 (2011) 01BC05-4.

TH-1322_10612101

[19] H. Klauk, U. Zschieschang, J. Pflaum, M. Halik, Ultralow-power organic complementary circuits, Nature, 445 (2007) 745-748.

[20] J.H. Schon, H. Meng, Z. Bao, Self-assembled monolayer organic field-effect transistors (Retracted article. See vol 422 pg 92 2003), Nature, 413 (2001) 713-716.

[21] Z.F. Li, J. Li, X.Y. Luo, Application of phosphonic acid self-assembled monolayer in organic field-effect transistors, Appl. Surf. Sci., 282 (2013) 487-491.

[22] A. Ringk, W.S.C. Roelofs, E.C.P. Smits, C. van der Marel, I. Salzmann, A. Neuhold, G.H. Gelinck, R. Resel, D.M. de Leeuw, P. Strohriegl, n-Type self-assembled monolayer field-effect transistors for flexible organic electronics, Org. Electron., 14 (2013) 1297-1304.

[23] H.Y. Chen, I.W. Wu, C.T. Chen, S.W. Liu, C.I. Wu, Self-assembled monolayer modification of silver source-drain electrodes for high-performance pentacene organic field-effect transistors, Org. Electron., 13 (2012) 593-598.

[24] T.M. Pappenfus, R.J. Chesterfield, C.D. Frisbie, K.R. Mann, J. Casado, J.D. Raff, L.L. Miller, A pi-stacking terthiophene-based quinodimethane is an n-channel conductor in a thin film transistor, J. Am. Chem. Soc., 124 (2002) 4184-4185.

[25] Y. Sakamoto, T. Suzuki, M. Kobayashi, Y. Gao, Y. Fukai, Y. Inoue, F. Sato, S. Tokito, Perfluoropentacene: High-performance p-n junctions and complementary circuits with pentacene, J. Am. Chem. Soc., 126 (2004) 8138-8140.

[26] A. Facchetti, M. Mushrush, H.E. Katz, T.J. Marks, n-type building blocks for organic electronics: A homologous family of fluorocarbon-substituted thiophene oligomers with high carrier mobility, Adv. Mater., 15 (2003) 33-38.

[27] X.K. Gao, C.A. Di, Y.B. Hu, X.D. Yang, H.Y. Fan, F. Zhang, Y.Q. Liu, H.X. Li, D.B. Zhu, Core-Expanded Naphthalene Diimides Fused with 2-(1,3-Dithiol-2-Ylidene)Malonitrile Groups for High-Performance, Ambient-Stable, Solution-Processed n-Channel Organic Thin Film Transistors, J. Am. Chem. Soc., 132 (2010) 3697- 3699.

[28] A.K. Diallo, L. Rapp, S. Nenon, A.P. Alloncle, P. Delaporte, F. Fages, C. Videlot-Ackermann, Top gate copper phthalocyanine thin film transistors with laser-printed dielectric, Synth. Met., 161 (2011) 888-893.

[29] D.B. Wolfe, J.C. Love, K.E. Paul, M.L. Chabinyc, G.M. Whitesides, Fabrication of palladium-based microelectronic devices by microcontact printing, Appl. Phys. Lett., 80 (2002) 2222-2224.

TH-1322_10612101

[30] P.R. Gray, P.J. Hurst, S.H. Lewis, R.G. Meyer, Analysis and Design of Analog Integrated Circuits Fifth ed., Wiley, New York, 2009.

[31] J. Veres, S. Ogier, G. Lloyd, D. de Leeuw, Gate insulators in organic field-effect transistors, Chem. Mater., 16 (2004) 4543-4555.

[32] Y.M. Park, A. Desai, A. Salleo, L. Jimison, Solution-Processable Zirconium Oxide Gate Dielectrics for Flexible Organic Field Effect Transistors Operated at Low Voltages, Chem. Mater., 25 (2013) 2571-2579.

[33] K.J. Baeg, S.W. Jung, D. Khim, J. Kim, D.Y. Kim, J.B. Koo, J.R. Quinn, A. Facchetti, I.K. You, Y.Y. Noh, Low-voltage, high speed inkjet-printed flexible complementary polymer electronic circuits, Org. Electron., 14 (2013) 1407-1418.

[34] Y.R. Su, W.G. Xie, Y. Li, Y. Shi, N. Zhao, J.B. Xu, A low-temperature, solution-processed high-k dielectric for low-voltage, high-performance organic field-effect transistors (OFETs), J. Phys. D. Appl. Phys., 46 (2013).

[35] X.H. Zhang, B. Kippelen, High-performance C-60 n-channel organic field-effect transistors through optimization of interfaces, J. Appl. Phys., 104 (2008).

[36] F.Y. Yang, K.J. Chang, M.Y. Hsu, C.C. Liu, Low-operating-voltage polymeric transistor with solution-processed low-k polymer/high-k metal-oxide bilayer insulators, Org. Electron., 9 (2008) 925-929.

[37] W. Li, O. Auciello, R.N. Premnath, B. Kabius, Giant dielectric constant dominated by Maxwell-Wagner relaxation in Al2O3/TiO2 nanolaminates synthesized by atomic layer deposition, Appl. Phys. Lett., 96 (2010) 162907-3.

[38] J. Lee, J.H. Kim, S. Im, Pentacene thin-film transistors with $Al2O_{3+x}$ gate dielectric films deposited on indium-tin-oxide glass, Appl. Phys. Lett., 83 (2003) 2689-2691.

[39] C. Maunoury, K. Dabertrand, E. Martinez, M. Saadoune, D. Lafond, F. Pierre, O. Renault, S. Lhostis, P. Bailey, T.C.Q. Noakes, D. Jalabert, Chemical interface analysis of as grown HfO2 ultrathin films on SiO2, J. Appl. Phys., 101 (2007).

[40] V.G. Kessler, G.I. Spijksma, G.A. Seisenbaeva, S. Hakansson, D.H.A. Blank, H.J.M. Bouwmeester, New insight in the role of modifying ligands in the sol-gel processing of metal alkoxide precursors: A possibility to approach new classes of materials, J. Sol-Gel Sci. Technol., 40 (2006) 163-179.

TH-1322_10612101

[41] M.J. Alam, D.C. Cameron, Preparation and characterization of TiO2 thin films by sol-gel method, J. Sol-Gel Sci. Technol., 25 (2002) 137-145.

[42] H. Nagata, S.W. Ko, E. Hong, C.A. Randall, S. Trolier-McKinstry, Microcontact printed BaTiO3 and LaNiO3 thin films for capacitors, J. Am. Ceram. Soc., 89 (2006) 2816-2821.

[43] J. Ihlefeld, B. Laughlin, A. Hunt-Lowery, W. Borland, A. Kingon, J.P. Maria, Copper compatible barium titanate thin films for embedded passives, J. Electroceram., 14 (2005) 95-102.

[44] T.M. Stawski, W.J.C. Vijselaar, O.F. Gobel, S.A. Veldhuis, B.F. Smith, D.H.A. Blank, J.E. ten Elshof, Influence of high temperature processing of sol-gel derived barium titanate thin films deposited on platinum and strontium ruthenate coated silicon wafers, Thin Solid Films, 520 (2012) 4394-4401.

[45] E.J.H. Lee, F.M. Pontes, E.R. Leite, E. Longo, J.A. Varela, E.B. Araujo, J.A. Eiras, Preparation and properties of ferroelectric BaTiO3 thin films produced by the polymeric precursor method, J. Mater. Sci. Lett., 19 (2000) 1457-1459.

[46] F.M. Pontes, E.J.H. Lee, E.R. Leite, E. Longo, J.A. Varela, High dielectric constant of SrTiO3 thin films prepared by chemical process, J Mater Sci, 35 (2000) 4783-4787.

[47] F.M. Pontes, E. Longo, J.H. Rangel, M.I. Bernardi, E.R. Leite, J.A. Varela, $Ba_{1-x}Sr_xTiO_3$ thin films by polymeric precursor method, Mater. Lett., 43 (2000) 249-253.

[48] S.M. Zanetti, E. Longo, J.A. Varela, E.R. Leite, Microstructure and phase evolution of SrTiO3 thin films on Si prepared by the use of polymeric precursors, Mater. Lett., 31 (1997) 173-178.

[49] S. Nam, J. Jang, J.J. Park, S.W. Kim, C.E. Park, J.M. Kim, High-Performance Low-Voltage Organic Field-Effect Transistors Prepared on Electro-Polished Aluminum Wires, ACS Appl. Mater. Interfaces, 4 (2012) 6-10.

[50] H.G. Min, E. Seo, J. Lee, N. Park, H.S. Lee, Behavior of pentacene molecules deposited onto roughness-controlled polymer dielectrics films and its effect on FET performance, Synth. Met., 163 (2013) 7-12.

[51] S.E. Fritz, T.W. Kelley, C.D. Frisbie, Effect of dielectric roughness on performance of pentacene TFTs and restoration of performance with a polymeric smoothing layer, J. Phys. Chem. B, 109 (2005) 10574-10577.

TH-1322_10612101

[52] C.S. Kim, S.J. Jo, S.W. Lee, W.J. Kim, H.K. Baik, S.J. Lee, D.K. Hwang, S. Im, Low-voltage organic transistors: the effect of a spin-coated smoothing layer on device performance, Semicond. Sci. Technol., 21 (2006) 1022-1025.

[53] J. Park, S.Y. Park, S.O. Shim, H. Kang, H.H. Lee, A polymer gate dielectric for high-mobility polymer thin-film transistors and solvent effects, Appl. Phys. Lett., 85 (2004) 3283-3285.

[54] K. van Benthem, C. Elsasser, R.H. French, Bulk electronic structure of SrTiO3: Experiment and theory, J. Appl. Phys., 90 (2001) 6156-6164.

[55] J. Robertson, High dielectric constant oxides, Eur. Phys. J. Appl. Phys., 28 (2004) 265-291.

[56] S. Duenas, H. Castan, H. Garcia, A. de Castro, L. Bailon, K. Kukli, A. Aidla, J. Aarik, H. Mandar, T. Uustare, J. Lu, A. Harsta, Influence of single and double deposition temperatures on the interface quality of atomic layer deposited Al2O3 dielectric thin films on silicon, J. Appl. Phys., 99 (2006) 054902-8.

TH-1322_10612101

Chapter VII

Stability of Low-Operating Voltage OFETs based on PTCDI-Ph

7.1 Introduction

In the *chapter VI*, we have fabricated OFETs using several bilayer dielectric systems and summarized their performance. We have successfully demonstrated the low-voltage operation of the OFETs. We achieved operating voltage as low as 1.2 V and threshold voltage 0.3 V. The carrier mobilities for these OFETs were relatively higher than the reported values. The best mobility we obtained is 0.04 cm^2/V-s for the OFETs fabricated with $SrTiO_x/Al_2O_3$ dielectric system. Though, the operating voltage for these OFETs is slightly higher (~ 4 V) than the OFETs fabricated with BST dielectric, we have chosen this devices due to their higher carrier mobility and lower threshold voltage for further study of the stability. We have essentially studied the hysteresis on voltage swing, bias stress and long-term air stability. The gate dielectric has an important influence on the device stability to overcome the hysteresis and reliability of OFETs. It is extremely important to select a proper gate dielectric with a high dielectric strength, low leakage current, and high breakdown strength. A high leakage current through the gate dielectric can degrade the organic semiconducting active channel [1]. In general, the hysteresis effect can be reduced by careful use of cross-link of polymers [2, 3] or by inserting an inorganic-barrier layer in contact with the gate electrode [4-6]. In our case, we have used inroganic-inorganic bilayer system as gate dielectric. The response of the devices under bias stress were also discussed. All the devices were tested in presence of ambient conditions and their stability over the time was examined under the same condition.

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7.2 Experimental Details

PTCDI-Ph based OFETs were fabricated using bilayer dielectric containing 30 nm STO and 10 nm thick Al_2O_3 layer. The details about preparation of the STO sols and fabrication of Al_2O_3 are described in earlier chapters. The fabrication of OFETs is also discussed in *chapter VI*. In this work, we have selected two different types of OFETs fabricated earlier for their stability study. The first one is based on SiO_2 (300 nm) as dielectric layer and the second one is based on STO/Al_2O_3 bilayer as dielectric system. The schematic designs of these two devices are shown in Figure 7.1, which includes the thickness of the individual layers. The SiO_2 based OFETs were considered in this work purely to compare the result with the STO based OFETs. The channel length of the OFETs was about 50 μm and width was about 700 μm.

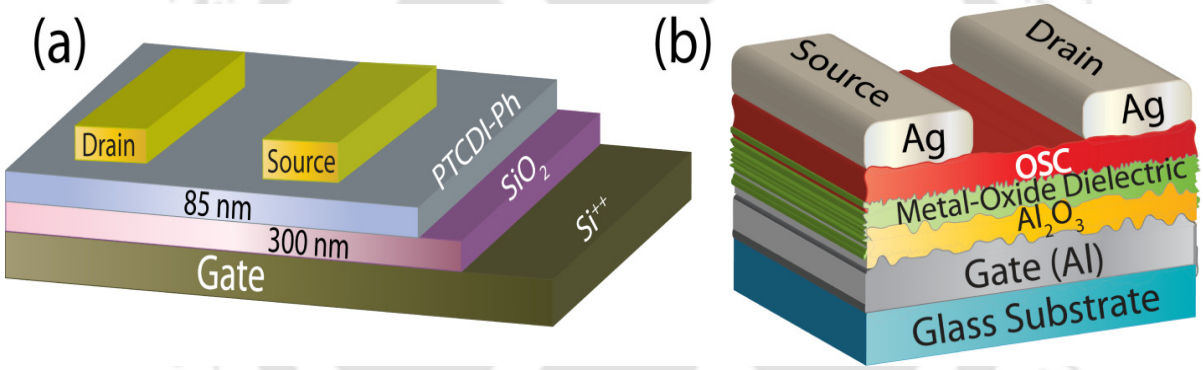

Figure 7.1: Schematic block diagrams of **(a)** OFET with SiO_2 gate dielectric and **(b)** OFET with STO/Al_2O_3 hybrid gate dielectric.

7.3 Results and Discussions

In order to study the stability of these devices, we have considered *(i)* hysteresis effect on the OFET output characteristics, *(ii)* effect of bias stress on OFET performances and *(iii)* degradation of the devices over time while exposing them in ambient for several days. Figure 7.2 (a) and (b) are showing the output and transfer characteristics curves obtained from SiO_2 based OFETs. Figure 7.2 (c) and (d) are showing the output and transfer characteristics curves for the devices fabricated with STO/Al_2O_3 as dielectric system.

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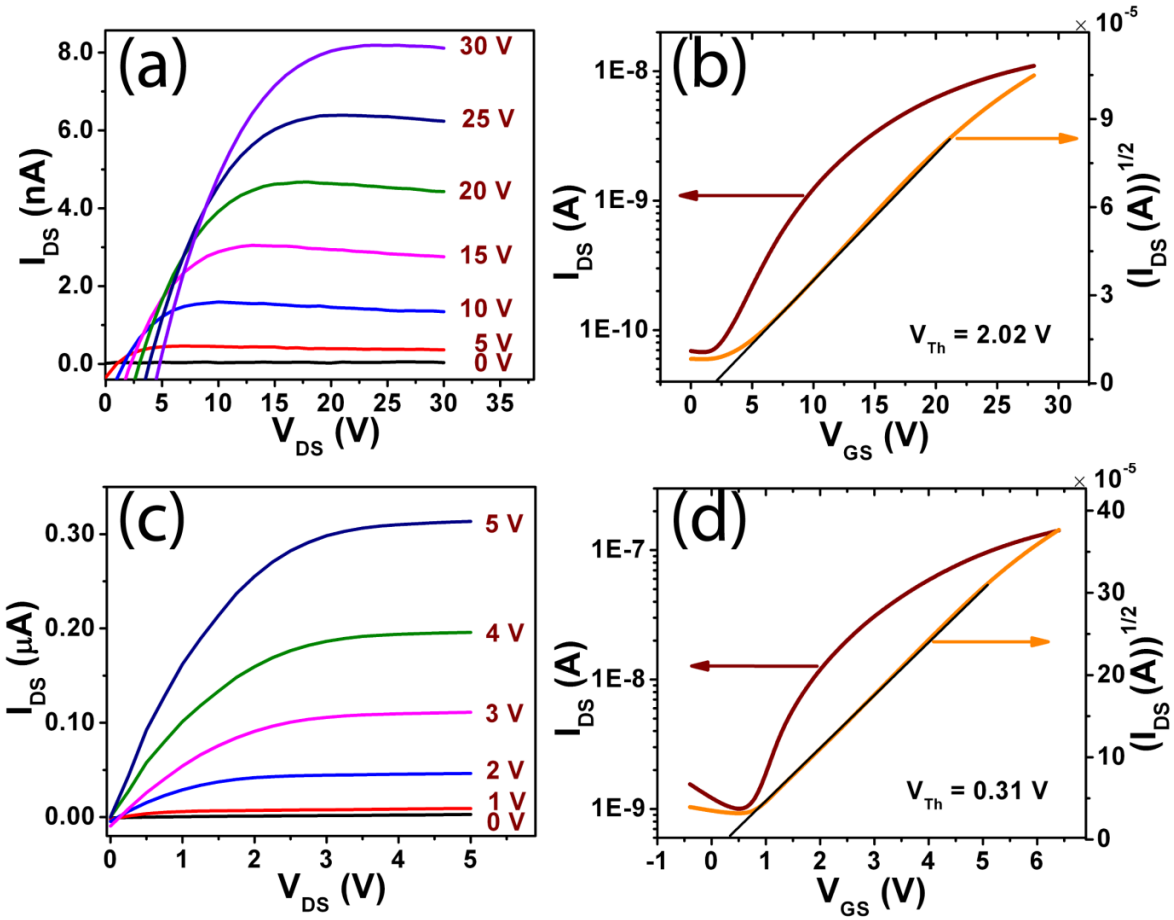

Figure 7.2: Output and transfer characteristics of OFET fabricated with 300 nm SiO_2 substrate (**(a)&(b)**) and with STO/Al_2O_3 bilayer (**(c)&(d)**).

The output curves show excellent linearity in the region with low V_{DS}. More than six STO/Al_2O_3 bilayer substrates were used and 10–15 devices on each substrate were fabricated and tested. The success rate of fabricating good devices is about 92%. As described in *chapter VI*, the operating voltage of OFETs using STO/Al_2O_3 gate dielectric is about 4 V, whereas, it is about 30 V for the OFETs based on SiO_2 dielectric layer. This is essentially due to the high capacitance of STO/Al_2O_3 combination layer. The threshold voltages were calculated from $(I_{DS})^{1/2}$ vs V_{GS} plot using the procedure describe in *chapter I*. To extract the electron mobility, we were used the average capacitance of 11.5 nF/cm^2 for SiO_2/Si and 65.4nF/cm^2 for bilayer STO/Al_2O_3 system. OFET parameters such as field-effect mobility (μ), on/off current ratio (I_{on}/I_{off}), threshold voltage (V_{Th}), and operating voltage, which were obtained from current-voltage characteristics of the drain current as a function of gate voltage

TH-1322_10612101

from both the devices are summarized in Table 7.1. *Chen et al.* [7] have reported the field effect mobility measured in glove box of OFET fabricated with PTCDI-Ph molecule grown on OTS treated SiO_2/Si substrate at 125 ºC substrate temperature during the growth is 0.017cm^2/Vs, operating voltage range is 0-100 V and threshold voltage range is 17-24 V. Even for SiO_2 dielectric based devices, we have observed threshold and operating voltages are very less. This may be due to the better quality of SiO_2 dielectric as well as quality of the PTCDI-Ph channel which was grown at 90 ºC substrate temperature. In case of OFETs based on STO/Al_2O_3, we observed the carrier mobility is doubled than the reported value and it is 0.04 cm^2/V-s. The threshold voltages were obtained in a range of 0.3 - 0.5 V. These values are the best reported parameters for the OFETs based on this molecule. In addition to that, there was no report found related to OFET fabrication on STO surfaces for *n*-type organic semiconducting molecules.

S. No.	Dielectric System	Operating Voltage (V)	Threshold Voltage (V)	Carrier Mobility cm^2/Vs	Reference
01	SiO_2	0 - 100	17 - 24	0.017	Ref. [7]
02	SiO_2	0 - 30	4 - 5	0.015	In This Work
03	$SrTiO_3/Al_2O_3$	0 - 4	0.3 – 0.5	0.04	In This Work

Table 7.1: Summarized parameters of SiO_2 and bilayer dielectric based OFETs with PTCDI-Ph as semiconducting channel.

7.3.1 Hysteresis in Transistor Output & Transfer Currents

A key parameter for device operation is, besides long term stability, the reproducibility in the current – voltage behavior, which may be affected by hysteresis phenomena. Hysteresis effects are often observed in organic transistors during sweeps of the gate voltage (V_{GS}).The origin of the hysteresis could be (*i*) effect of mobile charge at the channel, (*ii*) effect of resulting polarization in the gate dielectric or (*iii*) charge injection in the gate electrode [8]. For the successful integration of the OFETs into complex devices, hysteresis effects require to be less.

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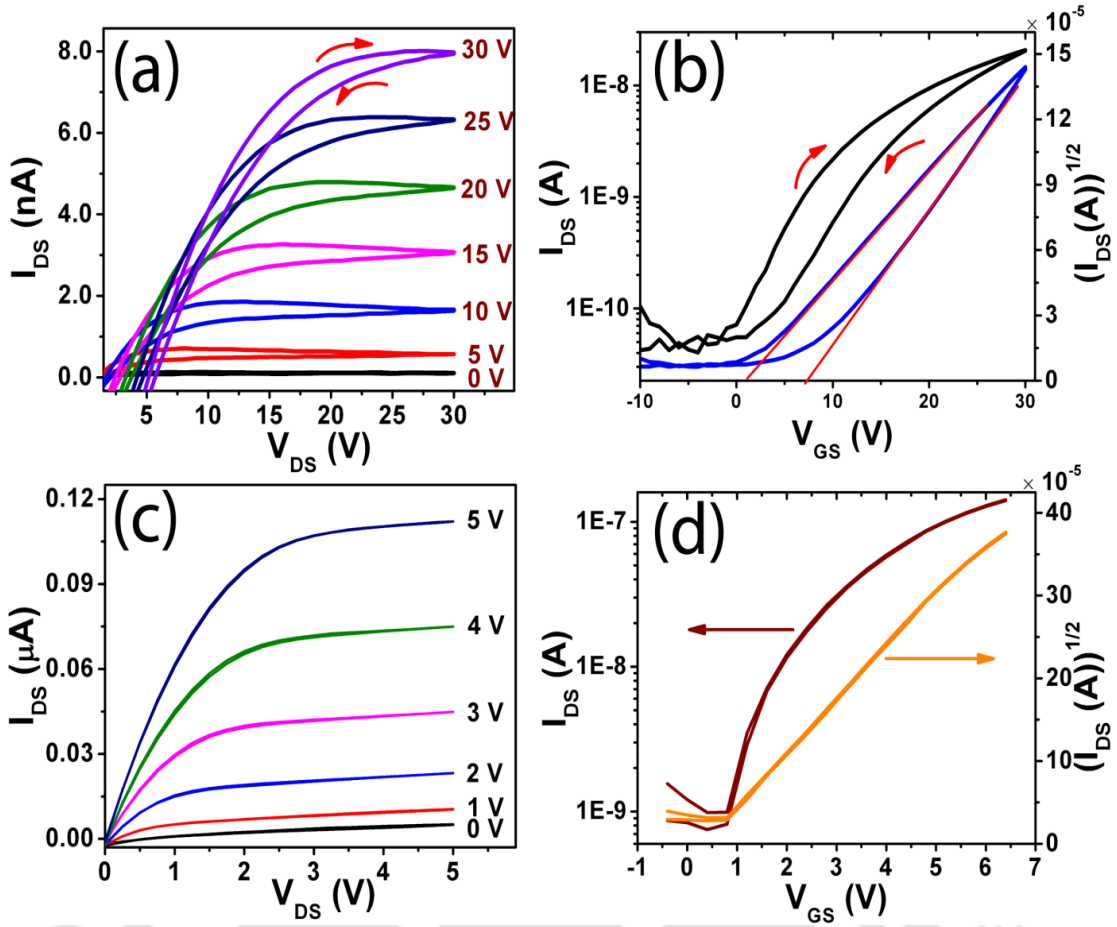

Figure 7.3: Output and transfer characteristics in dual sweep mode of OTFT fabricated with 300 nm SiO_2 substrate **((a)**, **(b))** and with $SrTiO_x/Al_2O_3$ bilayer **((c)**, **(d))**.

In order to study the hysteresis in our devices, we have performed the experiments on both the devices. Figure 7.3 is the representative hysteretic output and transfer electrical characteristics of PTCDI-Ph OFETs on SiO_2/Si and STO/Al_2O_3 bilayer, respectively. We observed that there is huge hysteresis in output & transfer characteristics curves existed in the OFETs fabricated with SiO_2/Si as dielectric layer as shown in Figures 7.3(a) & (b). Corresponding shift in threshold voltage was measured as 5.3 V. This hysteresis might be originating from charge trapping/de-trapping around the PTCDI-Ph and SiO_2 interface caused by interface hydroxyl groups [9, 10]. The devices on STO/Al_2O_3 bilayer (Figure 7.3(c) and 7.3(d)) were exhibiting almost no hysteresis when the gate bias is continuously swept from 0 V to 5 V at a step voltage of 0.1 V. The absence of hysteresis in the STO/Al_2O_3 bilayer-based devices are attributed to an improved dielectric layer with minimum trap states

arising from polar groups [11, 12], which usually give rise to slow polarization in STO/Al_2O_3 bulk or at the semiconductor- STO/Al_2O_3 bilayer interface [13]. The above results confirm that STO/Al_2O_3 as bilayer dielectric could be one of the options for the fabrication of OFETs with minimum hysteresis.

7.3.2 Reliability of Organic Field Effect Transistors

Optimization of material properties and device architecture has enabled rapid movement of OFETs towards their use in several applications. However, their reliability under atmospheric as well as electrical operating conditions is still impeding commercialization. Much of the effort in the past has focused on the development of materials having a high field-effect mobility and good environmental stability. To explore the environmental sensitivity, the OFETs fabricated on STO/Al_2O_3 bilayer dielectric was stored in air without any encapsulation; the ambient temperature was around 25 ºC and the relative humidity ranging between 60 –75%.

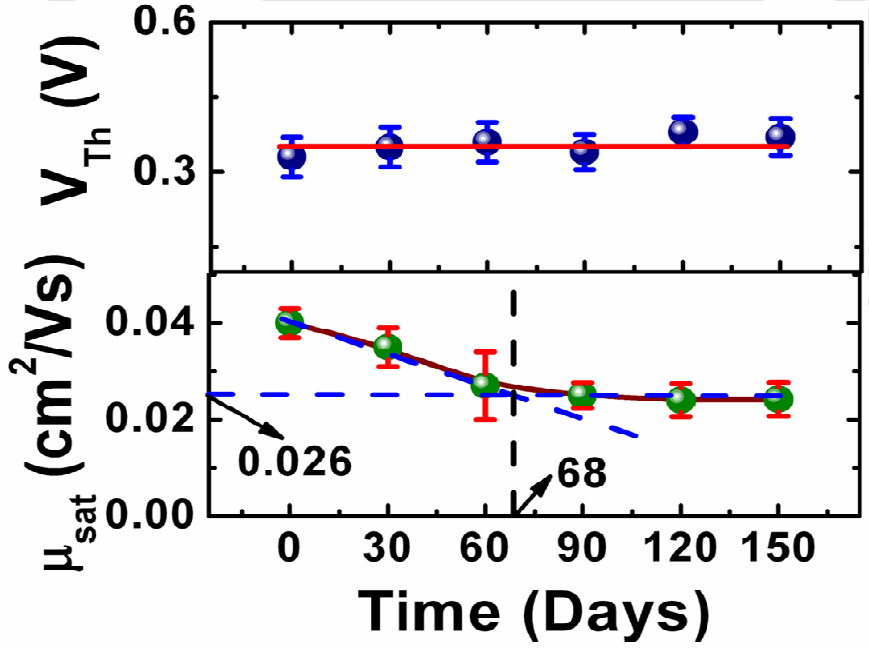

Figure 7.4: Carrier mobility variations with time of hybrid dielectric layered OFET after exposing with ambient.

The electrical characteristics were measured periodically for 150 days with a period of 30 days Figure 7.4 shows the variations in carrier mobility as well as threshold voltage with

exposing time under ambient condition. The carrier mobility of freshly fabricated device was 0.04 cm^2/V-s and this value reduces to 65 % of its original value to 0.026 in 68 days. After 68 days, though the devices were exposed in similar environmental conditions, the mobility was found to be almost constant at 0.026 cm^2/V-s. The representative plot for this behavior is shown in Figure 7.4(b). No significant variation in threshold voltage is observed. The threshold voltage is a measure of the applied gate bias at which a transistor switches to the on-state.

7.3.3 Bias – Stress Effect on Transistors

OFETs also display an electrical instability under application of a prolonged gate bias. Unlike environmental instability, the electrical instability in OFETs is reversible and is manifested only during application of a prolonged gate bias. During the operation, *i.e.* under application of a prolonged gate bias, the source-drain current decreases monotonically with time. Threshold voltage shift due to bias stress is observed regularly. Figure 7.5 shows the behavior of drain current while application of constant prolonged gate bias (more than 1hour) for both the devices. Most of the experimental works on the bias stress (BS) phenomenon have been focused on *p*-type organic transistors with silicon dioxide (SiO_2) layer as gate dielectric. For those devices, it has been proposed that, under the application of negative V_{GS}, the BS effect is due to a water-related charge trapping mechanism occurring at the SiO_2 surface (Proton Migration model) [14]. More recently, it was suggested that the proton migration model can be involved also in the BS effect occurring in *n*-type OFETs with SiO_2 gate dielectrics [15]. Nevertheless, the reports where the BS effect is systematically analyzed for *n*-type organic transistors are still only few [16, 17].

Indeed, it was found that $I_{DS}(t)$ decays over time for the OFETs based on SiO_2 dielectric when positive V_{GS} (inducing the formation of the electron accumulation layer at the PTCDI-Ph/SiO_2 interface) are applied. In particular, with V_{GS} = + 30 V, after 4000 s the I_{DS} decreased by 85% of its initial value. However, the reduction factor was only 9% for the OFETs based on STO/Al_2O_3 bilayer dielectric system. Our results revealed that the suitable high capacitive layer with low leakage current could significantly improve the device stability. The minimal shift in threshold voltage from 0.33 V to 0.42 V was observed. This further confirms the

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device stability. However, in case of OFETs based on SiO_2 as dielectric layer was 1.97 V to 6.22 V (see Figure 7.6). This is significantly higher in compare to earlier case.

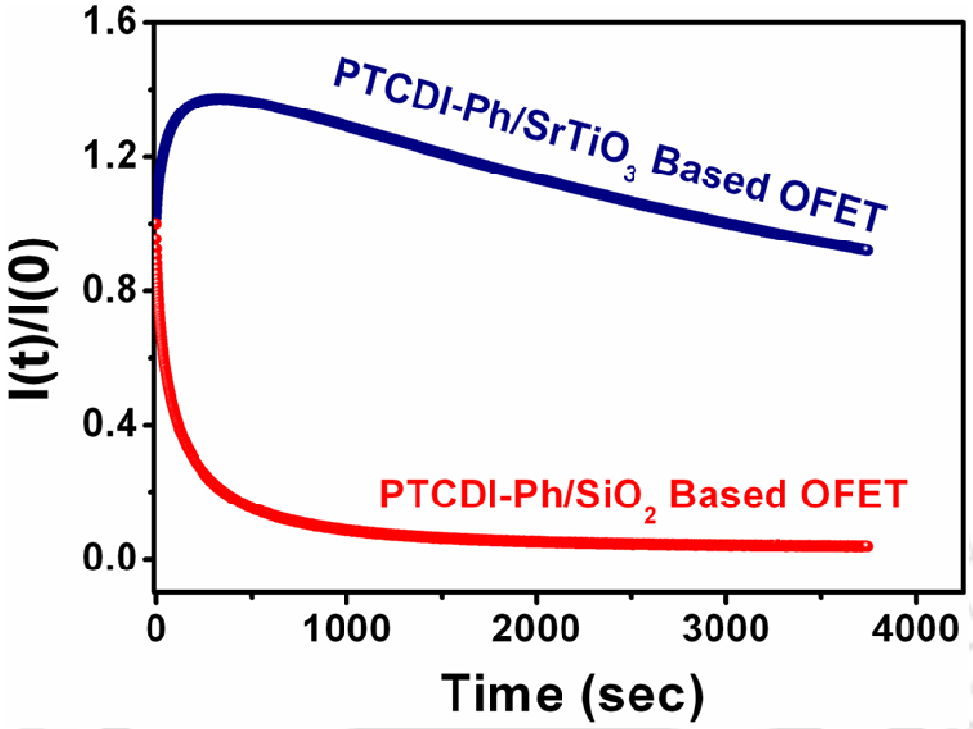

Figure 7.5: Time-dependent current decay under voltage stress for more than 1 h of OFET with SiO_2 and OFET with STO/Al_2O_3 bilayer dielectric systems.

Though the device stability is improved, there was an anomalous behavior in current variation in case of OFETs fabricated with bilayer dielectric. We have observed enhancement of current up to 25-30% as a result of bias stress initially and then current decreased monotonically. The decrease in I_{DS} during electrical bias stress is commenly related to the charge carrier trapping at the interface of insulator-semiconductor or in the semiconductor channel. However, increase of current under stress bias has been explain for *p*-type OFETs by proton migration model. The mechanism involves the exchange of holes in the semiconductor with protons in the gate dielectric in an electrolytic reaction involving water and the subsequent migration of these protons into the oxide [14]. In this case, we have *n*-type OFETs with STO as dielectric. STO is a provskite and the kinetics of water incorporation leading to provide extra electron in the active channel at the beginning of the stress bias could be more complex and requires further investigation. However, here we

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confirm the stability of the OFETs based on PTCDI-Ph fabricated with STO/Al_2O_3 as dielectric system.

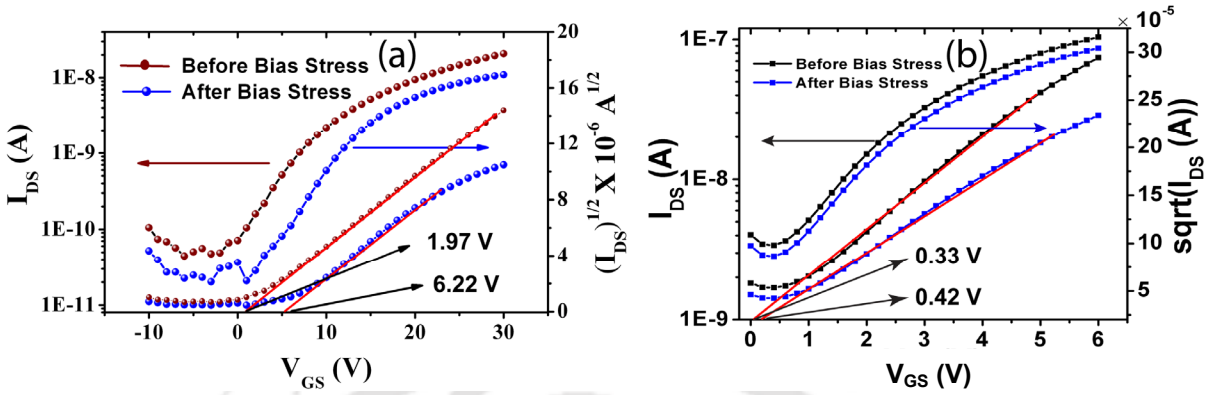

Figure 7.6: Transfer curves measured after 1h bias stress of OFETs with dielectric layers of **(a)** SiO_2 and **(b)** STO/Al_2O_3.

7.3.4 Stability after periodic application of bias-stress

In order to study the recovery of the devices after bias stress, we have systematically applied bias stress for some time and then switched off for a while and continued the cycle. The response of output current is shown in Figure 7.7 as the gate bias varied. At 4 V constant drain-source, V_{DS} and gate-source (V_{GS}) bias voltages, output drain-source current (I_{DS}) has been measured for periodic on/off states of V_{GS}. When device was biased, the current increases as observed before. However, when the bias is switched off, the current immediately reaches to current before bias stress was applied. As this continues to several cycles, device showed stable operation without further degradation in the performance due to periodic application of stress bias. This experiment confirms that these devices are highly stable under bias stress and the response of these devices is exceptionally reproducible. In general, the devices with huge trapped electron density are responsible for degradation of device performance with time. But in our case this problem has been solved successfully, this can be attributed to the high capacitance and better capacitive coupling of our bilayer dielectric system with the activation channel.

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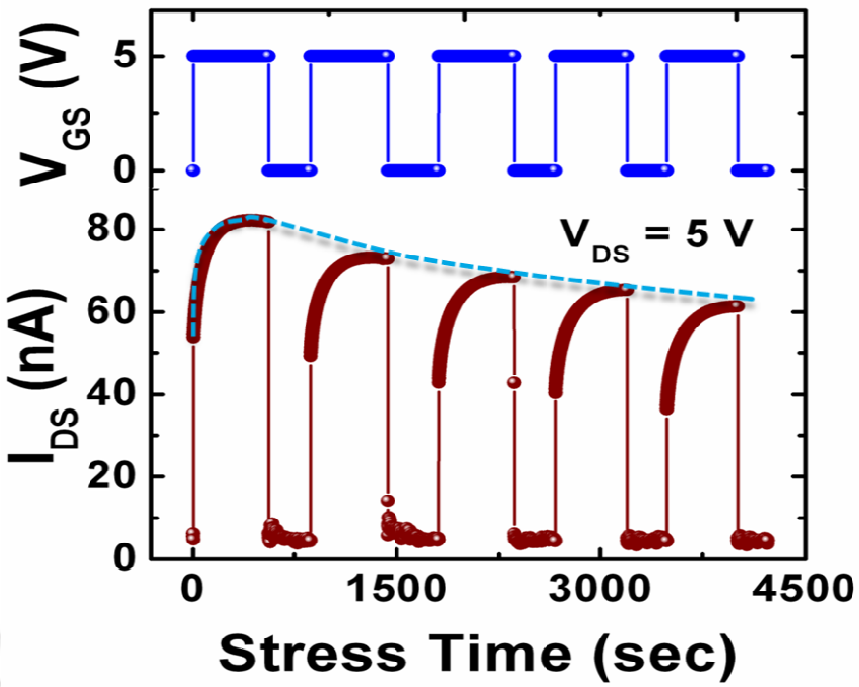

Figure 7.7: Response of active channel during stress-bias with on/off gate voltage bias.

7.4 Summary and conclusions

We have fabricated several OFETs based on metal oxide bilayer as dielectric layers. We have observed low voltage operation with enhanced carrier mobility. At the same time we have achieved very low threshold voltage. In this chapter, we have studied the stability and reliability of the devices, which were based on STO/Al_2O_3 dielectric system. These devices were chosen due to their higher carrier mobility and low threshold voltage operation. The air stability of the devices was studied for 150 days. We have observed slow decay process of carrier mobility for first 68 days. However, the devices were quite stable without showing any further decay in carrier mobility up to 150 days. Devices are highly stable under bias stress. We have observed 0.1 V minimal changes in the threshold voltage due to the bias stress when the threshold voltage was 0.3 V. The periodic application of bias stress also confirms that the devices are highly stable. We have observed anomalous increase in current during bias stress. In order to understand the origin of this anomalous effect requires further investigation.

TH-1322_10612101

7.5 References

[1] R.W.I. de Boer, N.N. Iosad, A.F. Stassen, T.M. Klapwijk, A.F. Morpurgo, Influence of the gate leakage current on the stability of organic single-crystal field-effect transistors, Appl. Phys. Lett., 86 (2005) 032103-3.

[2] C.A. Lee, D.W. Park, K.D. Jung, B.J. Kim, Y.C. Kim, J.D. Lee, B.G. Park, Hysteresis mechanism in pentacene thin-film transistors with poly(4-vinyl phenol) gate insulator, Appl. Phys. Lett., 89 (2006) 262120-3.

[3] D.K. Hwang, K. Lee, J.H. Kim, S. Im, J.H. Park, E. Kim, Comparative studies on the stability of polymer versus SiO2 gate dielectrics for pentacene thin-film transistors, Appl. Phys. Lett., 89 (2006) 093507-3.

[4] C.A. Lee, D.W. Park, S.H. Jin, I.H. Park, J.D. Lee, B.G. Park, Hysteresis mechanism and reduction method in the bottom-contact pentacene thin-film transistors with cross-linked poly(vinyl alcohol) gate insulator, Appl. Phys. Lett., 88 (2006) 252102-3.

[5] D.W. Park, C.A. Lee, K.D. Jung, B.G. Park, H. Shin, J.D. Lee, Low hysteresis pentacene thin-film transistors using SiO2/cross-linked poly(vinyl alcohol) gate dielectric, Appl. Phys. Lett., 89 (2006) 263507-3.

[6] J. Ficker, A. Ullmann, W. Fix, H. Rost, W. Clemens, Stability of polythiophene-based transistors and circuits, J. Appl. Phys., 94 (2003) 2638-2641.

[7] H.Z. Chen, M.M. Ling, X. Mo, M.M. Shi, M. Wang, Z. Bao, Air stable n-channel organic semiconductors for thin film transistors based on fluorinated derivatives of perylene diimides, Chem. Mater., 19 (2007) 816-824.

[8] M. Egginger, S. Bauer, R. Schwodiauer, H. Neugebauer, N.S. Sariciftci, Current versus gate voltage hysteresis in organic field effect transistors, Monatsh. Chem., 140 (2009) 735-750.

[9] J.B. Koo, C.H. Ku, S.C. Lim, S.H. Kim, J.H. Lee, Hysteresis and threshold voltage shift of pentacene thin-film transistors and inverters with Al2O3 gate dielectric, Appl. Phys. Lett., 90 (2007) 133503-3.

[10] L.L. Chua, J. Zaumseil, J.F. Chang, E.C.W. Ou, P.K.H. Ho, H. Sirringhaus, R.H. Friend, General observation of n-type field-effect behaviour in organic semiconductors, Nature, 434 (2005) 194-199.

TH-1322_10612101

[11] A. Wang, I. Kymissis, V. Bulovic, A.I. Akinwande, Engineering density of semiconductor-dielectric interface states to modulate threshold voltage in OFETs, IEEE Trans. Electron Devices, 53 (2006) 9-13.

[12] P. Balk, Dielectrics for Field-Effect Technology, Adv. Mater., 7 (1995) 703-710.

[13] D.K. Hwang, M.S. Oh, J.M. Hwang, J.H. Kim, S. Im, Hysteresis mechanisms of pentacene thin-film transistors with polymer/oxide bilayer gate dielectrics, Appl. Phys. Lett., 92 (2008) 013304-3.

[14] A. Sharma, S.G.J. Mathijssen, E.C.P. Smits, M. Kemerink, D.M. de Leeuw, P.A. Bobbert, Proton migration mechanism for operational instabilities in organic field-effect transistors, Phys. Rev. B., 82 (2010) 075322-11.

[15] H. Sirringhaus, Reliability of Organic Field-Effect Transistors, Adv. Mater., 21 (2009) 3859-3873.

[16] M. Barra, F.V. Di Girolamo, N.A. Minder, I.G. Lezama, Z. Chen, A. Facchetti, A.F. Morpurgo, A. Cassinese, Very low bias stress in n-type organic single-crystal transistors, Appl. Phys. Lett., 100 (2012) 133301-4.

[17] F.V. Di Girolamo, F. Ciccullo, M. Barra, A. Carella, A. Cassinese, Investigation on bias stress effects in n-type PDI8-CN2 thin-film transistors, Org. Electron., 13 (2012) 2281-2289.

TH-1322_10612101

Chapter VIII

Summary and Conclusions

The aim of this thesis was to fabricate low operating voltage and highly stable organic field-effect transistors (OFETs) using two different semiconducting materials as active channels. In order to achieve this, two strategies were followed. Firstly, we have considered gate dielectric materials with high-*k* dielectric constant for our study. Essentially, we have used bi-layer dielectric system considering different dielectric materials. The selection of the materials was based on the easy techniques available to grow the films and their different band energies. This enabled us to reduce the leakage current through the defects states. At the same time, the thicknesses of the dielectric layers were optimized to enhance the capacitance of the dielectric layer. In order to establish a better capacitance coupling between gate and organic semiconducting channel, the morphology of the dielectric layers were also studied to obtain smooth surface structure formation leading to minimum defect states. Secondly, we have studied the growth of organic active channel on top of the smooth dielectric surfaces to obtain the suitable growth parameters, which can enhance the performance of the devices. In one case, the organic active channel was in the form of single crystal wires like structures and in the other case, the active channel was in the form of thin film.

CoPc and PTCDI-Ph are the two molecules, which were used as the materials for active channel of the OFETs we fabricated in this thesis work. These two molecules are in the family of phthalocyanine and perylene derivatives, respectively. CoPc shows *p*-type semiconducting properties and PTCDI-Ph shows *n*-type semiconducting properties when devices are fabricated with these materials. To study the growth of thin films, we have used two solid substrate surfaces, such as SiO_2 and mica (001). SiO_2 is amorphous in nature, whereas, freshly cleaved mica (001) surfaces is atomically flat reconstructed surface. Growth of CoPc thin film was studied on both the surfaces. However, PTCDI-Ph films were

TH-1322_10612101

grown on different bi-layer dielectric systems. The bi-layer dielectric systems were fabricated using Al_2O_3 as one of the layers in combination with PVA, PMMA or any other metal oxides, such as TiO_x, $BaTiO_x$, $SrTiO_x$ and $BaSrTiO_x$ as second layer. These are the materials with high dielectric constant. Several OFETs were fabricated with these materials. The performances of the devices were studied optimizing different growth parameters. We successfully fabricated OFETs with high carrier mobility of the order 1.1 cm^2/Vs with CoPc as active materials. We have demonstrated the performance of the OFETs with operating voltage as low as 1.2 V for the devices based on PTCDI-Ph. The stability of the devices was also checked in terms of stress bias effect, hysteresis and exposing to ambient for several days.

CoPc films were found not suitable for the fabrication of OFETs. We have observed roughening in CoPc film due to instability in the growth mechanism induced by local diffusion of the molecules. Charge transport through the organic channel is essentially driven by the hopping conduction from molecules to molecules which are connected by very week π–π interaction. The rough films as channel would further reduce the charge transport by introducing defects and grain boundaries in the film. The roughening in CoPc films were characterized by calculating different scaling exponents such as α, β and $1/z$ determined from the height fluctuations obtained from atomic force microscopy images of the surface morphologies. We have observed equal diffusion activation energy for lateral and vertical diffusion of the molecules. However, it was found that local surface diffusion, which exists even at 120 °C growth temperatures and it plays crucial role for roughening in CoPc film growth. The reported scaling exponents do not belong to the existing models, which hold well for inorganic film growth. Therefore, the roughening behavior observed in the present study appears to belong to a different universality class. The growth kinetics of the CoPc films were also studied and obtain the diffusion activation energy $E_a = 0.35$eV for the growth laterally as well as vertically. This represents the molecular translational and rotational barrier on the surfaces. However, we observed different activation energy for the growth of CoPc on mica (001) surfaces. The film morphology also remains rough in this case and found not suitable to fabricate OFETs based on these films. In order to improve the molecular packing within the OFET active channel, we used physical vapor deposition (PVD)

TH-1322_10612101

technique exploiting the self-assembly of the CoPc molecules to grow CoPc micorstructures. The molecules self-assembled to form CoPc single crystal micron size wires in PVD growth technique. We have achieved to grow more than 100 μm long CoPc wires after optimizing the growth conditions on different substrates. XRD and TEM measurements confirm the crystallinity of the wires. These wires were further used for the fabrication of OFETs.

We have used poly(vinyl-alcohol) (PVA)/Al_2O_3 system as bi-layer dielectric for the fabrication of CoPc wires based OFETs. Al_2O_3 layers were grown using anodization of Al films. We have grown a very smooth film of PVA due to the lower surface free energy of PVA (~0.045 J/m^2) than Al_2O_3 (~1.7 J/m^2). In this process, we achieved a better capacitive coupling between CoPc wires and gate through the bi-layer dielectric system. The thickness of the individual layers was optimized for minimum leakage current at the same time enhanced capacitance in the system. We have observed significant enhancement of carrier mobility, which is 1.11 cm^2/Vs with on/off ratio ~10^4 and 20 V operating voltage. The observed carrier mobility of CoPc based OFETs is about one order of magnitude higher than the reported.

We have followed the same strategies to fabricate n-type OFETs based on PTCDI-Ph as active channel. The growth of PTCDI-Ph films on SiO_2 and polymer dielectric surfaces have been carried out in order to obtain the suitable growth conditions to fabricate efficient devices. In this case, we have also considered using bi-layer dielectric consisting layers of poly (methyl methacrylate) (PMMA) and Al_2O_3. The field-effect carrier mobility obtained from the devices designed at 90 °C substrate temperature showed the highest value of 0.02 cm^2/Vs. This has been attributed to the formation of smooth and uniform films of PTCDI-Ph on PMMA surfaces. In this process, we were able to enhance the carrier mobility. However, the operating voltage for these OFETs was about 30 V, which is still very high.

In order to fabricate the OFETs based on PTCDI-Ph as active channel with lower operating voltage, we have replaced the PMMA layers by the materials with higher dielectric constant. We have synthesized high-*k* metal-oxide gate dielectric sols like TiO_2, $BaTiO_3$, $SrTiO_3$ and $BaSrTiO_3$. The device parameters were optimized to obtain lower leakage current and formation of smooth dielectric surfaces. We have successfully achieved low operating

TH-1322_10612101

voltage OFETs by introducing solution-processed high-*k* bi-layer systems as the gate dielectric. The bilayer dielectric systems exhibits very smooth surfaces with rms roughness below 1 nm, high capacitance about 65 nF/cm^2 and low leakage current. PTCDI-Ph based OFETs exhibit an electron mobility about 0.04 cm^2/V-s and an operating voltage as low as 1.2 V with threshold voltage ranging from 0.3-0.5 V. The obtained results for all the transistors are much better than the transistors fabricated with the traditional SiO_2 dielectric. Most importantly, we demonstrated air stable *n*-type OFETs since all the measurements were performed under ambient condition. The observed parameters are highly reproducible and reliable.

In order to study the stability under bias stress and exposing into air, we have performed measurement on one of the best devices fabricated above. The stability of the devices was studied through hysteresis and bias-stress response. Negligible hysteresis in transfer characteristics have been observed for these devices in compare to the devices fabricated with SiO_2 dielectric. In that case, we observed huge hysteresis (corresponding threshold shift is > 4V). The air stability of the devices was studied for 150 days. We have observed slow decay process of carrier mobility to 0.02 cm^2/Vs in 68 days. However, these devices were found to be quite stable without showing any further decay in carrier mobility up to 150 days. This result conforms that the high reliability of the OFETs with high stability under bias stress. The periodic application of bias stress also confirms that the devices are extremely stable.

In this thesis, we have successfully fabricated OFETs based on CoPc and PTCDI-Ph molecules with better performances. Some of the open questions could be tackled within this work, but at the same time, new unsolved questions arose, which pave the way to interesting studies in the near future. In the following, some of the most intriguing issues are listed.

We have observed roughening in CoPc thin film growth even at elevated substrate temperature. Our experimental results confirmed that the local diffusion of the molecules is apparently reason for this roughening mechanism. The observed exponents do not satisfy any of the existing growth model for inorganic film growth. It would be interesting to propose a

TH-1322_10612101

simple solid on solid model including local diffusion of the molecules to get insight of the mechanism.

We have observed long CoPc structures formation on mica (001) surfaces. The effect of surface reconstruction on the growth of CoPc films on mica (001) surfaces needs more involved experimental study. X-ray surface diffraction study could be one of the appropriate studies to probe the molecular arrangement at the interfaces. In order to successfully implementation of the structures into electronic device fabrication, it would be very important to have the control on the growth of these structures with specific directionality. For further comprehensive description of the involved interactions might also be employed.

We have successfully fabricated *n*-type air stable PTCDI-Ph based OFETs with bi-layer dielectric system for low voltage operation. The stability of the devices is also very promising. The interaction of polymer or high-*k* dielectric surfaces with small molecules is more complex than the inorganic surfaces like SiO_2. It would be interesting to understand the molecular interactions, which lead to form different surface structures. The complete understanding of the growth, could guide to fabricate devices with enhanced performances.

We have observed an anomalous increase in current during bias stress measurement. More involved experiments require to understanding this effect. Though, proton migration model is proposed to explain this effect for *p*-type OFETs, but the mechanism could be different for *n*-type OFETs. Nevertheless, the interaction of water with STO surface is more complex. Moreover, the partial current flow through the STO layer cannot be ruled out. More controlled experiments are required to be short out these issues.

TH-1322_10612101

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List of Publications

1) **Murali Gedda,** Nimmakayala V. V. Subbarao and Dipak K. Goswami. "*High carrier mobility of CoPc wires based field effect transistors using bi-layer gate dielectric*" "***AIP Adv.*", 3, (2013)** 112123-112127**; doi: 10.1063/1.4834355.**

2) **Murali Gedda,** Nimmakayala V. V. Subbarao and Dipak K. Goswami. "*Local Diffusion Induced Roughening in CoPc Thin Film Growth*", **"*ACS Langmuir*", 30, (2014),** 8735-8740, **doi: 10.1021/la502108a.**

3) **Murali Gedda,** Nimmakayala V. V. Subbarao and Dipak K.Goswami "*Growth mechanism of Cobalt(II) Phthalocyanine(CoPc) thin films on SiO2 and muscovite substrates*" **"*AIP Conf. Proc". 1576*, (2014),** 152-154**; doi: 10.1063/1.4862007.**

4) Nimmakayala V. V. Subbarao, **Murali Gedda,** V. Suresh, Parameswar K. Iyer and Dipak K. Goswami. "*Effect of hybrid gate dielectric on perylenediimide based organic field effect transistors*", **"*Phys. Status Solidi A*",** 1–9 **(2014); doi: 10.1002/pssa.201431304.**

5) Nimmakayala V. V. Subbarao, **Murali Gedda,** Parameswar K. Iyer and Dipak K. Goswami. "*Enhanced environmental stability induced by effective polarization of a polar dielectric layer in tri-layer dielectric system of organic field-effect transistors: a quantitative study*" **"*ACS AMI*", 2015; doi: 10.1021/am507636k.**

6) Nimmakayala V. V. Subbarao, **Murali Gedda,** V. Suresh, D. Anamika, Parameswar K. Iyer and Dipak K. Goswami. "*Growth and Characterization of N, N'-Dioctadecyl -1, 7-Dibromo-3, 4, 9, 10-Perylenetetracarboxylic-Diimide Micron/Nano Wires for Organic Field Effect Transistors*" **"*AIP Conf. Proc".*, 1576, (2014);** 42-45**, doi: 10.1063/1.4861975.**

7) **Murali Gedda**, Arindam Pal, Nimmakayala V. V. Subbarao, M. Sharma, Parameswar K. Iyer and Dipak K. Goswami. *"Effect of substrate temperature on the growth of PTCDI-Ph films on a hybrid dielectric materials for organic field-effect transistors*", "***Organic Electronics*", 2014** (Submitted).

TH-1322_10612101

8) **Murali Gedda**, Nimmakayala V. V. Subbarao and Dipak K. Goswami, "*PTCDI-Ph based low-operating voltage organic field effect transistors with solution processable gate dielectrics*", ***"ACS AMI"***, **2015** (Submitted).

TH-1322_10612101

Conference Presentations

1) ***Murali Gedda**, Arindam Pal, P. Anand Kumar, and D.K.Goswami "Kinetics Of Flat Top Organic Nanostructure Growth",* Second International Conference on Advanced Nanomaterials and Nanotechnology ***(ICANN-2011)***, Dec 8-10, **2011**, IIT Guwahati. India.

2) ***Murali Gedda**, Arindam Pal, P. Anand Kumar, and D.K.Goswami "Kinetics Of Flat Top Organic Nanostructure Growth",* International Conference on Nano Science and Technology ***(ICONSAT 2012)***, January 20-23, **2012**, ARCI, Hyderabad. India.

3) ***Murali Gedda**, Arindam Pal and D.K.Goswami "Study of Growth of Organic Thin Films by X-ray Reflectivity Measurements"* "12th International Conference on Surface X-ray and Neutron Scattering ***(SXNS-12)"*** Saha Institute of Nuclear Physics, Kolkata, 25th to 28th July, **2012,** India .

4) ***Murali Gedda**, Arindam Pal, V. Suresh, P.K Iyer and D.K. Goswami, "Effect of Temperature on the Molecular Arrangement of Organic Nano-structure Growth"* 4th International conference on Advanced Nanomaterials ***(ANM 2012)*** IIT Madras, Chennai, October 17 –19, **2012,** India.

5) ***Murali Gedda**, Nimmakayala V. V. Subbarao and Dipak K. Goswami, "Growth kinetics of Cobalt Phthalocyanine (CoPc) Thin Films Grown by Molecular Beam Deposition Technique"* 2nd International conference on Optoelectronic Materials and Thin films for Advanced Technology ***(OMTAT 2013)***, CUSAT, Kochi January 3- 5, **2013**, India.

6) ***Murali Gedda**, Nimmakayala V. V. Subbarao and Dipak K. Goswami "Catalyst Directed Growth of Cobalt (II) Phthalocyanine Organic nanostructures",* Third International Conference on Advanced Nanomaterials and Nanotechnology ***(ICANN-2013)***, **2013,** Center for Nanotechnology, IIT Guwahati, India.

TH-1322_10612101

7) ***Murali Gedda**, Nimmakayala V. V. Subbarao and Dipak K. Goswami* "*Solution-processed metal-oxides as gate dielectrics for low-operating voltage of organic field-effect transistors",* 3rd International Conference on Physics at Surface and Interfaces (***PSI 2014***), Feb 24-28, 2014, Puri, India.

Schools & Workshops Attended

1) *"**International School on Nanoscience with X-Ray and Neutron Sources**"*, organized by Saha Institute of Nuclear Physics, Kolkata, from 23th to 24thJuly, **2012**, India.

2) *"**INUP Familiarization Workshop**"* especially for the North East at IIT-Guwahati" during 28-29 September **2012**, India.

3) ***"INUP Hands on training"*** organized by CeNSE, IISc Bangalore, from 24th Jun to 03rd July, **2014**, India.

TH-1322_10612101

Appendix

Height-height correlation function:

The simplest way to calculate the height-height correlation function for an isotropic surface is along the fast scan direction (assumed to be the *x* direction):

$$H(r) \approx H_S(p) = \frac{1}{N_y(N_x - p)} \sum_{l=1}^{N_y} \sum_{n=1}^{N_x - p} [h(p+n,l) - h(n,l)]^2.$$

An alternative is the circular average:

$$H(r) = H_S(\sqrt{p^2 + q^2})$$
$$= \frac{1}{(N_y - q)(N_x - p)} \sum_{l=1}^{N_y - q} \sum_{n=1}^{N_x - p} \left\{ [h(p+n,l+q) - h(n,l)]^2 + [h(N_x - p - n, l+q) - h(n,l)]^2 \right\}.$$

For an isotropic surface, the two-dimensional height-height correlation function can be calculated according to the following equation:

$$H(r) \approx H_S(p,q)$$
$$= \frac{1}{(N_y - q)(N_x - p)} \sum_{l=1}^{N_y - q} \sum_{n=1}^{N_x - p} [h(p+n,l+q) - h(n,l)]^2, \ \textit{and}$$

$$H(r) \approx H_S(-p,q)$$
$$= \frac{1}{(N_y - q)(N_x - p)} \sum_{l=1}^{N_y - q} \sum_{n=1}^{N_x - p} [h(N_x - p - n, l+q) - h(n,l)]^2.$$

[Adopted from Y. P. Zhao, G.C. Wang, and T.M. Lu "*Characterization of Amorphous and Crystalline Rough Surface: Principles and Applications*" Experimental Methods in the Physical Sciences, Volume 37 pp 27.]

TH-1322_10612101