# Abstract

Several studies on the applications of Recognition, Mining, and Synthesis (RMS) have been undertaken in recent years. The tasks executed by these applications don't require a golden answer or an outstanding numerical result. Instead, they must deliver products that are acceptable or sufficient in quality. These workloads have *inherent application resilience* or the capacity to deliver acceptable results even if a significant portion of their computations are executed in an imprecise or approximate manner. Intrinsic application resilience adds a whole new level to the optimization of computing platforms. However, the belief that every computation must be conducted with the same stringent idea of accuracy continues to govern the design of computing systems. With unrelenting demand for computing performance on one side and the power requirement from technology scaling on the other, it's essential to delve into a new source of efficiency. *Approximate Computing (AxC)* is a new design method that takes advantage of the flexibility given by intrinsic application resilience to optimise hardware or software implementations that are more energy or performance efficient. Several AxC techniques have been effectively developed for system architecture, software, storage elements, arithmetic circuits, and simulation in the last decade. In this thesis, we focus on Approximate Arithmetic Circuits, particularly *Approximate Adder*, which are the result of applying AxC techniques at the hardware level, and *Approximate Testing*, which is the process of approximating the conventional test procedure.

Recent techniques in approximate adder design revolve around two important principles: (1) reducing the carry chain and (2) tolerating

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inaccuracy at Least Significant Bits (LSBs). Using the first principle, a given n-bit adder is divided into a number of blocks to shorten the carry chain, and no modification is made to the Full Adders (FAs), which is the fundamental unit of an adder circuit. The next category of adders is based on the second principle. The approximation is achieved through employing Approximate Full Adder (AFA) in the LSB part of the adder circuit. The basic design principle is to partition the given n-bit adder into two segments: an inaccurate (inexact) segment and an accurate segment. The former consists of AFAs accepting the inputs from LSBs. The latter consists of conventional FAs receiving inputs from MSBs. The approximate adder design techniques discussed above are primarily applied to Ripple Carry Adder (RCA) circuits, where a carry-chain or a fundamental block such as FA is present in the design. However, complex adder designs such as Kogge Stone Adder (KSA), where no fundamental blocks or carry chain is available, require unique treatments to generate an approximation version. This thesis focuses on designing such adders using the Significance-based gate-level pruning (SGLP) technique. With this approach, a non-significant gate is identified and is removed from the actual architecture to achieve approximation. Following SGLP, the accuracy of the adder can be controlled using the error threshold provided by the designer.

Circuits that produce acceptable results can be used in applications like RMS that have error resilience qualities. To put it another way, a circuit that has a fault but nevertheless produces a decent outcome can be used in error-tolerant applications. These circuits are referred to as Acceptable Integrated Circuits (AcICs). However, when using the traditional testing process, we discovered no technique for identifying AcICs through testing. We can't overlook the fact that the faulty circuit discovered via traditional testing may generate error-free output for the majority of test patterns. This thesis proposes techniques to approximate the traditional test flow architecture (Approximate Testing) for distinguishing AcICs from rejected circuits.

The key idea is to classify the faults as benign or malignant (i.e., acceptable or unacceptable, respectively) based on an error threshold (i.e., the maximum tolerable amount of error). This classification provides two sets of faults (i.e., acceptable and unacceptable). Then, we employ an Automatic Test Pattern Generation (ATPG) system that is aware of the classification and generates test patterns only for unacceptable faults while minimizing detection of acceptable faults. The proposed approach has the considerable benefit of increasing yield. According to the proposed yield model, the effective yield gain will be between 10-20% on average.