Analog/RF Circuit Optimization using Adjoint Network Sensitivity Analysis and Metaheuristics

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DEEPAK JOSHI

DEPARTMENT OF ELECTRONICS AND ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI

GUWAHATI - 781 039, ASSAM, INDIA

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Certificate

This is to certify that the thesis entitled "**Analog/RF Circuit Optimization using Adjoint Network Sensitivity Analysis and Metaheuristics**", submitted by **DEEPAK JOSHI** (10610224), a research scholar in the *Department of Electronics and Electrical Engineering, Indian Institute of Technology Guwahati*, for the award of the degree of **Doctor of Philosophy**, is a record of an original research work carried out by him under our supervision and guidance. The thesis has fulfilled all requirements as per the regulations of the institute and in our opinion has reached the standard needed for submission. The results embodied in this thesis have not been submitted to any other University or Institute for the award of any degree or diploma.

Dated:
Guwahati.

Dr. Gaurav Trivedi
Assistant Professor
Dept. of Electronics and Electrical Engg.
Indian Institute of Technology Guwahati
Guwahati - 781 039, Assam, India.

Dated:
Guwahati.

Prof. Ratnajit Bhattacharjee
Professor
Dept. of Electronics and Electrical Engg.
Indian Institute of Technology Guwahati
Guwahati - 781 039, Assam, India.

To Mother Nature

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Abstract

The development of system-on-chip, consisting analog and digital circuits have become a crucial area of research due to the ever-increasing demand for miniaturization. The design of analog circuits consumes a significant part of resources (knowledge intensive design efforts) and time during the design flow. In order to reduce manual efforts in the analog design flow, automation of analog circuit design is gaining importance day-by-day.

The design methodology for analog and RF circuit sizing has evolved from "pen and paper" approach to an optimization-based methodology along with simulation-based approach. In general, analog circuit designers derive design equations and solve them for a given set of specifications. Nowadays, problem-solving has become efficient due to the advent of computational intelligence methods. In this thesis, different numerical methods are presented to optimize circuit performance. With the resurgence of optimization-based methodologies, efficient circuit sizing approach has become imperative for the analog design process. The circuit designers employ circuit simulators to iteratively modify design variables through optimization techniques for improving the performance of electronic circuits.

In this thesis, analog circuit optimization problem is presented in the form of a standard numerical optimization problem. However, such analytical representation of analog circuit optimization problem differs with the optimization methods used, equation-based single and multi-objective optimization methods have been proposed for the optimization of analog circuits in this thesis. The first method is based on sensitivity analysis and the classical optimization approach. The sensitivity of a response with respect to the circuit's

parameters is determined by applying adjoint network based sensitivity analysis (ANSA). In ANSA, to determine global solution, the optimization problem is formulated as convex problem. This approach is verified by optimizing basic test circuits, e.g., cascode amplifier and two-stage operational amplifier and, the optimized circuit performance has been compared with the results produced by a commercial EDA tool. Later, the analytical results have been verified by characterizing a two-stage OpAmp, fabricated with 180nm CMOS technology.

To generalize the analytical formulation over the different frameworks, the second technique is proposed using evolutionary algorithms for circuit sizing. In this method, a hybrid of particle swarm optimization and simulated annealing (HPSO) is developed. Further, HPSO is improved using Lévy flight search (l-HPSO) to optimize analog/RF circuits. The applicability and effectiveness of HPSO and l-HPSO are demonstrated on the test circuits and standard test functions.

Due to the presence of various competitive design objectives, analog circuit sizing is incomplete without the analysis of trade-offs between the performance specifications. Therefore, a multi-objective optimization method (MHPSO) is proposed for analog circuit optimization which is an multi-objective variant of HPSO. An improved version (MHPSO-CD) on the basis of archive maintenance (crowding distance), is also proposed to improve the efficiency. The effectiveness and applicability of these methods are verified by optimizing test circuits, namely two-stage operational amplifier, folded cascode amplifier, low noise amplifier and standard multi-objective benchmarks. The proposed methodologies have shown improved performance as compared to other well known standard methods while optimizing standard problems and analog/RF circuits.

Contents

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List of Acronyms

ACO	Ant Colony Optimization
ALC-PSO	Particle Swarm Optimization with Aging Leader and Challengers
AMS	Analog-Mixed Signal
ANSA	Adjoint Network based Sensitivity Analysis
BFD	Backward Finite Differences
CAD	Computer Aided Design
CFD	Central Finite Differences
CMOS	Complementary Metal Oxide Semiconductor
CRPSO	Craziness based Particle Swarm Optimization
DE	Differential Evolution
DMOPSO	Decomposition based Multiobjective Particle Swarm Optimization
DRC	Design Rule Check
EDA	Electronics Design Automation
FFD	Forward Finite Differences
GA	Genetic Algorithm
GBW	Gain Bandwidth Product
GD	Generational Distance
HPSO	Hybrid Particle Swarm Optimization
HV	Hypervolume
IC	Integrated Circuit
ICMR	Input Common Mode Ratio
IGD	Inverse Generational Distance

LNA	Low Noise Amplifier
l-HPSO	Lévy flight Hybrid Particle Swarm Optimization
LPSO	Lévy Particle Swarm Optimization
LVS	Layout Vs. Schematic
MHPSO	Multiobjective Hybrid Particle Swarm Optimization
MHPSO-CD	Multiobjective Hybrid Particle Swarm Optimization with Crowding Distance
MOO	Multiobjective Optimization
MOEA	Multiobjective Evolutionary Algorithm
MOPSO	Multiobjective Particle Swarm Optimization
MOSA	Multiobjective Simulated Annealing
NF	Noise Figure
NSGA-II	Nondominated Sorting Genetic Algorithm II
OTA	Operational Transconductance Amplifier
OpAmp	Operational Amplifier
PESA	Pareto Envelope-based Selection Algorithm
PF	Pareto Front
PM	Phase Margin
PSO	Particle Swarm Optimization
PSRR	Power Supply Rejection Ratio
RF	Radio Frequency
SA	Simulated Annealing
SADE	Self-Adaptive Differential Evolution
SMPSO	Speed-constrained Multiobjective Particle Swarm Optimization
SoC	System on Chip
SPEA	Strength Pareto Evolutionary Algorithm
SPICE	Simulation Program with Integrated Circuit Emphasis
SPSO	Standard Particle Swarm Optimization
SR	Slew Rate

UGW	Unity Gain Bandwidth
VLSI	Very Large Scale Integration

1

Introduction

Contents

1.1 Introduction

In the last few decades, Very Large Scale Integration (VLSI) technologies have experienced significant advancements. The competition of improving cost-effectiveness and minimizing time-to-market has become hard due to ever-increasing demand of miniaturization and integration in the form of System-on-Chip (SoC).

The designers, assisted by Computer Aided Design (CAD) tools, have enabled electronic systems to be extremely complex integrated circuits, comprising multi-million transistors. Many of these SoCs fall in the domain known as analog-mixed-signal (AMS) systems, which are composed of both analog and digital circuits.

Analog circuit design is more specific and complex than its digital counterpart. Hence, designers have been using digital electronics to replace the analog functions. However, there are some functions and applications which still remain analog, for example, the sensors handle analog signals and analog circuits are used to amplify these signals for further processing. The conversion of analog signals into digital or vice-versa requires a suitable electronic circuitry. Voltage and current reference circuits in any SoC are analog circuits. The SoCs incorporating the AMS and memory blocks are extensively being used in Internet of Things (IoT) products, medical applications and multimedia systems [2, 5].

The advances in fabrication technologies have increased device density and reduced device sizes. This resulted in increased variability and number of design constraints while improving the performance of analog blocks. Although analog blocks occupy a significantly smaller area in the SoC, design of analog blocks in the SoC is one of the deciding factor in productivity due to the lack of matured and well-defined procedures Figure 1.1.

The EDA tools available for digital circuit design are well matured, easy to reuse and easily upgradeable for the new technology. Most of the digital functionalities can be developed by reusing basic design blocks, whereas, analog blocks have distinct solutions and are difficult to reuse. Despite various efforts made in the area of analog EDA, distinct trade-offs and lack of well-defined rule-sets have made analog design a bottleneck in the development of any AMS systems. Therefore, in order to improve productivity in analog design, the development and improvement of CAD tools are essential

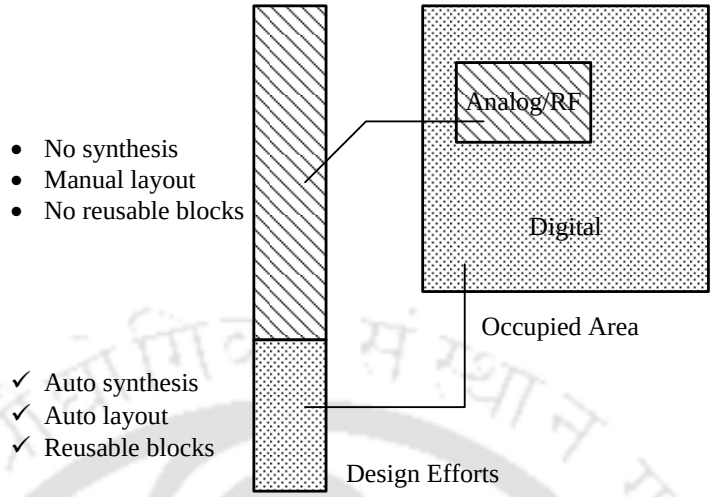

Figure 1.1: Comparison of analog and digital design [1]

requirements.

As we know, design flow of the analog circuit varies according to the applications, it can commonly be represented as shown in Figure 1.2. This is a circuit-level design flow which includes top-down flow from topology selection to circuit sizing and bottom-up flow from layout generation to extraction and verification.

The designer has to iteratively traverse through this design flow for every analog block in order to determine suitable physical sizes of all the devices. This task can further be divided into two steps: topology selection in which a suitable topology is selected for the given performance specifications and circuit sizing, where the aspect ratio of each transistor is determined under the conditions or constraints of the selected topology. Later, these sizes are verified using simulation tools, e.g., HSPICE [6] by analyzing optimized analog circuits.

These optimized devices are then accommodated in the chip area according to the topology with a suitable placement and routing plan either manually or by using the CAD tools or both. This stage is called layout generation. The layout is composed of a set of geometric structures which follows a set of rules defined by the process technology. Later, this layout is verified through the Design Rule Check (DRC) and the Layout-versus-Schematic (LVS) processes. There remains a significant difference in performance of an optimized circuit after simulation and the performance of the LVS process. This difference is generated because of the parasitic effects, produced by the layout. During

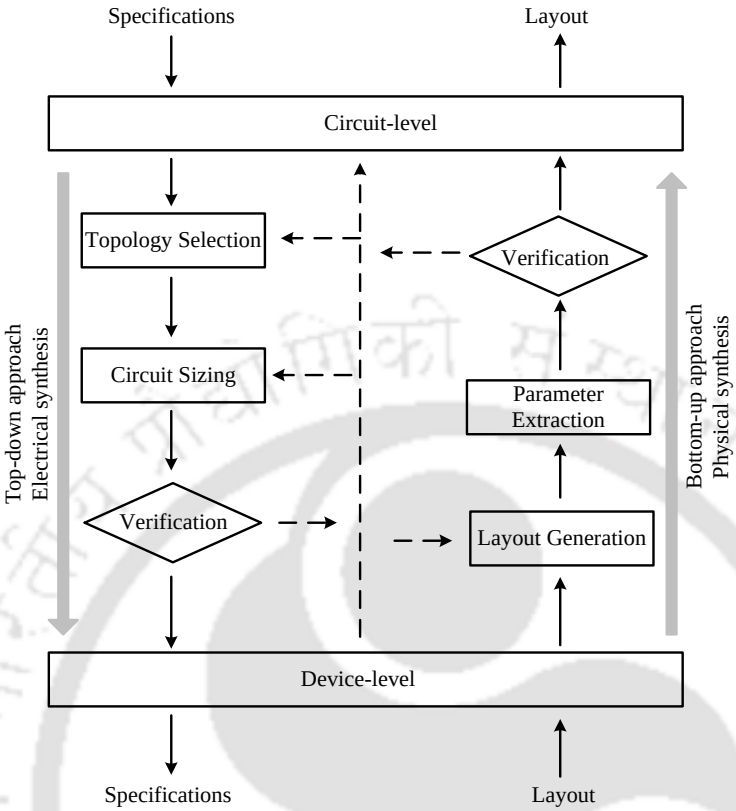

Figure 1.2: General flow of analog design at circuit-level [2]

parasitic extraction, these effects are modeled into the circuit components, which are simulated with the original circuit elements to determine the actual performance of the circuit. Here the importance of automation in the analog design flow, becomes important because of cumbersome and inefficient manual exploration of design space. Since analog design lacks a general systematic approach, it differs from its digital counterpart in applicability. The knowledge and experience of a designer are more crucial at every stage of the analog circuit design flow. In general, designers manually apply tools at every stage to achieve the design goals. The design goals have to satisfy performance specifications, and at the same time it has to be robust as well.

In order to perform circuit optimization, the analog circuit design is transformed into an optimization problem with design goals (DC gain, area, power, noise figure, etc.) as the cost or objective function subject to the design constraints. The design constraints are defined by the topology (biasing of transistors), input and output range of signals, performance specification (GBW, slew rate, input, output matching, etc.). These constraints confine the design space including various solutions. The

exploration of these multi-dimensional and irregular search spaces is frequently attempted while designing and optimizing analog circuits, and a review of these approaches is briefly discussed in chapter 2. Although these approaches are proven to be a fundamental aid to the designers, lack of generality and scalability are the issues which need to be addressed. Further, the transformation of analog circuit design problem into a suitable optimization problem depends on the applied optimization algorithm.

The work presented in this thesis is focused to address the issues related with the optimization-based analog circuit optimization.

1.2 Thesis Motivation and Objective

In analog circuit design, sensitivity analysis plays an important role in determining the critical design parameters. Analysis of sensitivity is an important mathematical measure of variations in the performance metrics due to the infinitesimally small perturbations of circuit parameters [7]. In this thesis, we employ adjoint network based sensitivity analysis (ANSA) to optimize analog circuit at a given topology. The main advantage of the adjoint network sensitivity analysis approach is low computational cost (i.e., of the order (N+1)). The CPU-time of adjoint sensitivity analysis is significantly low in comparison with finite-difference sensitivity approximations [8]. This approach has been employed to optimize different problems in microwave circuits [8, 9]. The application of this approach is extended in this thesis for the optimization of analog circuits.

The ANSA method requires a good initial operating point, and problem formulation in the form of convex optimization problem. Further, nature-inspired algorithms are developed for analog circuit optimization in the view of flexibility in their application in terms of initialization and problem formulation. The concept of *survival of the fittest* enables a detailed selection process for complete exploration of performance space to preserve the diversity of solutions. The cost functions can be optimized by using nature-inspired algorithms under a given set of conditions or constraints. Although particle swarm optimization (PSO) has been a popular method used for finding optimum solutions, it has issues of being trapped locally and slow convergence. On the other hand simulated annealing has a tendency to reach local optimum based on a serial stochastic search strategy [10]. Therefore, to improve the search performance of PSO, a metaheuristic combining both PSO and SA is proposed in

this thesis to attempt analog circuit optimization.

Since circuit modelling is often affected by uncertainties and errors at many levels, it is necessary to analyze tradeoffs among performance specifications to avoid inconsistent solutions during design. For addressing these problems, several multi-objective techniques have been proposed with an emphasis on nature-inspired algorithms because of their inherent ability and efficiency in handling uncertainty during circuit design flow. A multi-objective optimization framework is also aimed to be developed in this thesis.

The objective of this thesis is to develop methodologies for the optimization of analog/RF circuits by using sensitivity analysis and metaheuristics. In order to achieve these goals, key tasks which need to be accomplished, are given below.

- Design of a framework to compute sensitivity of analog circuit's response.
- Improvement of search strategy using the hybrid of PSO and SA.
- Formulation of temperature mapping scheme as an initialization scheme for SA in the hybrid framework.
- Development of multi-objective optimization scheme using the PSO-SA hybrid.

1.3 Thesis Contributions

Different methodologies are proposed to produce optimized circuit parameters for the given performance. These methods are validated by optimizing basic analog circuits. The work can be classified into two broader parts. In the first part, circuit optimization method is developed by using adjoint network based sensitivity calculation. Whereas, hybrid evolutionary algorithms are developed for analog/RF circuit optimization in the second part. Further, a multi-objective framework is also developed by using hybrid evolutionary algorithms to analyze the performance space of circuits as an aid to circuit designers. The key contributions of the thesis are as follows:

- A method of analog circuit optimization using adjoint network based sensitivity analysis is developed.

- A metaheuristics, hybrid evolutionary algorithm based on PSO and SA, is developed for analog/RF circuit optimization. An extension of this metaheuristic is proposed based on an improved search strategy.
- A multi-objective hybrid evolutionary algorithm is developed to study tradeoffs of various parameters related to performance optimization in analog/RF circuit design.
- Experimental results are verified by comparing them with the state-of-art optimization techniques for different test circuits and standard test functions. We report significant improvement by proposed methods over various existing approaches in this thesis.

1.4 Thesis Organization

The organization of rest of the thesis is presented as follows:

Chapter 2: Fundamentals of Optimization Techniques in Analog Circuit Sizing

In this chapter, evolution of various optimization methods for analog/RF circuits is discussed. Different existing methodologies for the performance optimization of analog/RF circuits, are reviewed. The fundamentals of problem formulation for analog/RF circuits along with the evolutionary algorithms are also discussed in this chapter.

Chapter 3: Sensitivity Analysis and Circuit Optimization

In this chapter, a gradient-based method for the optimization of analog circuits using adjoint network based sensitivity analysis (ANSA) is presented. By analyzing analog circuit and its adjoint transformation, sensitivities of the circuit response with respect to different parameters can be computed. The formulation of adjoint networks, calculation of sensitivity of circuit's response with respect to various design parameters and modification in the design parameters values in every iteration are described in this chapter. In order to verify the effectiveness of the proposed method it is employed to optimize the performance of a two-stage operational amplifier (OpAmp). Subsequently,

the OpAmp circuit is simulated using Cadence Virtuoso for optimized parameters and the results are validated with post fabrication measurement results as well.

Chapter 4: Analog Circuit Optimization using Metaheuristics

This chapter presents the development of evolutionary algorithms for analog circuit optimization. A metaheuristic (HPSO) based on PSO and SA is presented to optimize analog/RF circuits subject to a variety of design constraints. Here, convergence of PSO is improved by advancing through local solutions using SA to achieve the global optimum solution. PSO is applied to construct initial solutions for SA and these initial solutions are used to decompose the entire search space into different annealing regions. The results obtained by proposed method are compared with standard optimization methods to show the performance of the proposed method in terms of optimization quality and robustness. Further, HPSO is extended (l-HPSO) by incorporating Lévy flight principle to improve the convergence. The proposed optimization scheme is implemented for common analog/RF circuit optimization and the obtained result are compared with the results generated by standard test functions.

Chapter 5: Multi-objective Optimization of Analog Circuits using Metaheuristics

This chapter presents a hybrid multi-objective optimization framework (MHPSO) by combining particle swarm optimization and simulated annealing. In order to reduce manual efforts in the process of circuit design, tradeoffs among performance specifications are need to be analyzed using multi-objective optimization methodologies. The framework emphasizes on preserving nondominated solutions in an external archive. The multi-dimensional space excluding the archive is divided into several sub-spaces according to a velocity-temperature mapping scheme. Further, the solutions in each sub-space are optimized using simulated annealing for generation of a Pareto front. The framework is extended by incorporating crowding distance comparison operator (MHPSO-CD) to maintain non-dominated solutions in the archive. The effectiveness of proposed methodologies is demonstrated for performance space exploration of three electronic circuits, namely, a two-stage operational amplifier, a folded cascode operational amplifier and a low noise amplifier with inductive source degeneration.

Further, the performance of proposed algorithms (MHPSO, MHPSO-CD) are evaluated on various test functions and the results are compared with standard multi-objective evolutionary algorithms.

Chapter 6: Conclusions and Future Work

In this chapter, conclusions are drawn on the works reported in this thesis. Future scope along with the different possible applications is discussed in this chapter.

भारतीय प्रौद्योगिकी संस्थान गुवाहाटी
Indian Institute of Technology Guwahati

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Fundamentals of Optimization Techniques in Analog Circuit Sizing

Contents

In this chapter, a review of state-of-the-art methodologies for circuit optimization is presented along with the foundation for proposed methodologies in the following chapters. This chapter is organized as follows: Section 2.1 introduces the problem definition of analog circuit optimization. In section 2.2, a concise review of analog circuit sizing is presented. Analog circuit sizing methods can broadly be classified into knowledge-based and optimization-based methodologies. We have proposed optimization-based schemes in the consequent chapters. Backgrounds of the proposed techniques are discussed in section 2.3. Section 2.4 presents design examples used in the following chapters with discussion on generation of the global solutions. Section 2.5 summarizes the chapter.

2.1 Introduction

The applicability of integrated mixed analog-digital circuits in a system-on-chip (SoC) is surging due to more and more features to be provided in a single system itself ranging from Internet of Things (IoT) to smart and artificial intelligence based system. The accuracy and efficiency of an analog-mixed signal system are governed by the design of analog part, which depends upon the experience and ingenuity of the designer. With the advent of computer-aided circuit design tools, this knowledge-based dependency is reduced in the case of digital circuits. However, analog circuit design, due to the presence of tradeoffs or competitive design objectives, still remains dependent on manual efforts. A circuit design has to be iteratively improved in order to achieve the desired agreement between simulated and test results. Hence, optimization of the circuits has become one of the most critical part of the design process. The procedure of analog circuit design comprises of parameter-level design [12] and topological-level design [13]. In this thesis, the parameter-level design is explored keeping the topology fixed.

Analog circuit optimization or sizing problem can conveniently be expressed as a single or multi-objective optimization problem subject to a set of constraints. In chapters 3 and 4, single-objective circuit optimization is discussed, and chapter 5 presents multi-objective circuit optimization. It is to be noted that in this thesis, the terms *circuit sizing* and *circuit optimization* are interchangeable and used, whenever necessary as per the context. The single-objective optimization problem [63] can be generalized as,

$$\begin{aligned} \text{minimize} \quad & f(\mathbf{x}) \\ \text{subject to} \quad & g(\mathbf{x}) \leq 1 \\ & h(\mathbf{x}) = 0 \\ & x_{L_i} < x_i < x_{H_i} \\ & where\ i = 0, 1, ..., n \end{aligned} \tag{2.1}$$

where, vector **x** corresponds to the the n design variables [50] e.g., device dimensions, bias current, transconductances, etc.

$f(\mathbf{x})$ is the objective function to be minimized e.g., Area, Power, Noise Figure, etc.

$g(\mathbf{x})$ corresponds to the user defined performance specifications e.g., Slew rate, SNR, Gain-bandwidth product (GBW), etc.

$h(\mathbf{x})$ are equality constraints to be met e.g., KCL , KVL equations, output voltage swing, input range, biasing conditions, etc.

Unlike single-objective circuit optimization, multi-objective circuit optimization deals with multiple objective functions simultaneously. The solution of these problems consists of a set of optimized points (Pareto fronts) between objective functions. Multi-objective circuit optimization enables the circuit designer to explore trade-offs between different objectives under a given set of constraints. An example of such optimization problem [63] can be expressed as,

$$\begin{aligned} \text{minimize } f_i(\mathbf{x}), \quad & i = 1, 2, ..., q; \\ \text{subject to } g_j(\mathbf{x}) \leq 0, \quad & j = 1, 2, ..., m; \\ h_k(\mathbf{x}) = 0, \quad & k = 1, 2, ..., p; \\ \mathbf{x}_l \in X, \quad & l = 1, 2, ...n, \end{aligned} \tag{2.2}$$

where, **x** is a vector of n variables satisfying all the constraints $g_j(\mathbf{x})$ and $h_k(\mathbf{x})$. $f_i(\mathbf{x})$ is a set of q different objective functions that need to be minimized. Further, the problem formulation for multi-objective optimization is discussed in chapter 5.

2.2 Review of Analog Circuit Sizing Approaches

Automation of analog circuit optimization or sizing has been an interesting area of research in the view of the ever-increasing complexity of analog circuits. In this section, we have presented a brief survey of circuit sizing techniques while emphasizing the optimization-based approaches. A comparison of these tools/methods in the tabular form in summarized in Appendix A.

The analog circuit sizing techniques can broadly be classified as: the knowledge-based approaches and the optimization-based approaches [1], based on their fundamental principle. In the knowledge-based approaches, the circuit sizing is attempted by using a systematic design plan derived from the experts knowledge [14–17]. These design plans are developed with the design equations and a design strategy which provide the component sizes satisfying the desired performance. Although the derivation of a design plan consumes a lot of efforts and time, the execution of such approaches is fast. Further, the design plan needs to be maintained with the changing technology. The solutions produced by such approaches may not be global in nature, and are suitable only for the first-cut design.

In order to find the global solution, optimization techniques have been improvised and can be referred as next-generation methods for analog circuit optimization. Further, these methods can be divided into sub-classes: (a) equation-based and (b) simulation-based, depending upon the technique used for performance evaluation of a circuit. In equation-based methodologies, analytical expression or equation relate performance of the circuit as a function of design variables. For the optimal solutions these equations are analyzed with various algorithms which are either stochastic or deterministic in nature. Further, equation-based methods can be classified into two categories based on their problem formulation, (a) specific problem formulation and (b) generalized problem formulation.

(a) Specific problem formulation: The specific problem formulation depends upon the optimization strategy used to analyze it. The optimization strategies, i.e., steepest descent method, successive solution technique are employed in OPASYN [18] and STAIC [19], respectively. In Maulik et al. [20], analog sizing problems are defined as a constrained optimization problem and solved by employing sequential quadratic programming. In Matsukawa et al. [21], analog to digital converter is designed by solving the equations relating circuit's performance and component sizes via convex optimization

method. In GPCAD [22], circuit optimization problem is formulated in terms of posynomial functions and is solved via geometric programming method. However, GPCAD produces global solution efficiently, the derivation of posynomial equations introduces approximation errors. In Kuo-Hsuan et al. [23] and FASY [24], similar strategy is applied with simulated annealing (SA) and a simulation-based optimization strategy, respectively.

(b) Generalized problem formulation: Induction of heuristics for analog circuit sizing enables designers to generalize analytical formulation of the optimization problem. The application of simulated annealing to solve analytical models is demonstrated in OPTIMAN [25] and ASTRX/OBLX [26]. In DARWIN [27], genetic algorithm is applied for the optimization of electronic circuits. Further, applications of different heuristics in the circuit sizing are explained below.

As we know, the equation-based methods are superior to their knowledge-based counterparts in term of applicability and evaluation time, the analytical formulation of optimization problems introduces a deviation between the evaluated and actual performance. In general, all the device effects e.g., channel length modulation, velocity saturation, sub-threshold conduction, etc. cannot be accurately incorporated in the analytical models. Thus, reduction of the errors and variations induced by the above mentioned inaccuracies is a critical area of research. Further, solving the non-specific problem formulation using heuristics and iteratively refining the solutions using simulators, is another trend in the analog circuit optimization.

With the empowerment of computing resources simulation-based analog circuit optimization methods have become efficient and improvised. In DELIGHT.SPICE [28], equation-based optimization engine. DELIGHT [29] is used with the improved SPICE models to design an integrated circuit. In consonance with circuit simulators the optimization techniques, i.e., simulated annealing, swarm optimization, genetic algorithm, etc., can be implemented within the simulator to achieve an optimal solution more efficiently. In the following text, such sizing approaches are discussed based on the optimization scheme used. A few optimization methods are described briefly for completeness.

Simulated Annealing (SA): In Kuo-Hsuan et al. [23] and FASY [24], SA is used to refine solutions estimated by equation-based techniques. FRIDGE [30] uses SA optimization without having any dependency on initial point requirement. Cheng et al. [31] considers transistors biasing as one

of the design constraints to optimize circuit using SA. Similarly, SA is used in Castro et al. [32] to optimize the circuit.

Genetic Algorithm (GA): GA is an important optimization method based on the principle of natural evolution. The optimization problem is solved iteratively with the application of mutation and crossover operations. In Barros et al. [1, 33], the solution of optimization problem is obtained using GA. In Alpaydin et al. [34], a blend of an equation and simulation-based approaches is presented, where circuits performance is estimated by applying both GA and SA. With the application of parallel computing in ANACONDA [35], Santos-Tavares [36], MAELSTROM [37], etc., the optimization time is reduced.

Swarm Algorithms: The most popular swarm optimization algorithms [38] are Particle Swarm Optimization (PSO) and Ant Colony Optimization (ACO). PSO and ACO mimic natural phenomenon e.g., a swarm of bee searching for the best pollen areas and a swarm of ants searching for food, respectively. Since these algorithms require fewer variables in their implementation, the easy applicability makes them popular in analog circuit optimization. Various application of PSO [39, 40] and ACO [41, 42] in circuit optimization can be found in the literature.

In the view of circuit optimization, the works related to the iterative generation of component sizes and topologies are also present in literature. In Koza [43], Sripramong [44] and Hongying [45], generation of topologies are presented for the desired performance of circuit. It is to be noted that these methods could not earn proper attention due to their complexity and unusual designs.

Multi-objective Optimization: The design and optimization of an analog circuit may be treated as a multi-objective optimization (MOO) problem. A designer has to explore the feasible solution by analyzing the trade-offs among the competitive design objectives, e.g., minimizing power consumption while maximizing the gain, minimizing noise figure while maximizing the gain, etc. Due to the wider applicability of evolutionary algorithms to solve MOO problem, VLSI scientific community also employed these algorithms to the optimization of analog/RF circuits. GENOM-POF [46, 47] and MOJITO [48], the analog circuit optimization is attempted by multi-objective evolutionary algorithms. PSO is applied in [39] to solve circuit sizing problem via both single and multi-objective optimization methods. Multi-objective simulated annealing (MOSA) is proposed in [49] for the opti-

mization of electronic circuits.

Other than these approaches, the hybrid or combination of the heuristics (metaheuristics) have been proposed for both single and multi-objective circuit optimization. Such approaches are discussed in this thesis. However, development of circuit optimization methods is classified in a broader manner, the generalization and standardization of these methodologies for the domain of analog/RF circuit is yet to be sought. In the following section background of proposed algorithms are briefly explained.

2.3 Selected Optimization Methodologies

In general, a circuit design is iteratively improved in order to achieve the desired agreement between simulated and test results. To obtain the global solution, the circuit optimization problems can be formulated as a sub-class of convex optimization problems [50]. Although the analysis of convex optimization problems using gradient-based methods [51] and general heuristics [52], [53] are well-known in the domain of Electronic Design Automation (EDA), circuit optimization via mathematical programming is becoming increasingly difficult task with the rising level of circuit integration and complexity. The effectiveness and applicability of optimization methods [54] depend on their core strategies and structure. These methods are prone to errors with the increased number of variables thereby limiting their performance.

In this thesis, convex optimization problem is evaluated via sensitivity analysis using adjoint network approach. Further, the global solution can be produced from general formulation of optimization problem, using suitable heuristics, i.e., swarm algorithms, simulated annealing, evolutionary algorithms, etc. In this section, we present brief discussion of ANSA, PSO, SA and metaheuristics.

2.3.1 Adjoint Network based Sensitivity Analysis (ANSA)

The analytical model or equation-based problem formulation of an analog circuit sizing problem is evaluated via classical optimization scheme. Essence of ANSA is the reduction in computation cost of gradient calculation. The gradient of a cost function defines the direction of minimum cost and is calculated in steepest descent method. Sensitivities of circuits response with respect to circuit elements are simultaneously calculated by solving the original circuit and its adjoint transformation.

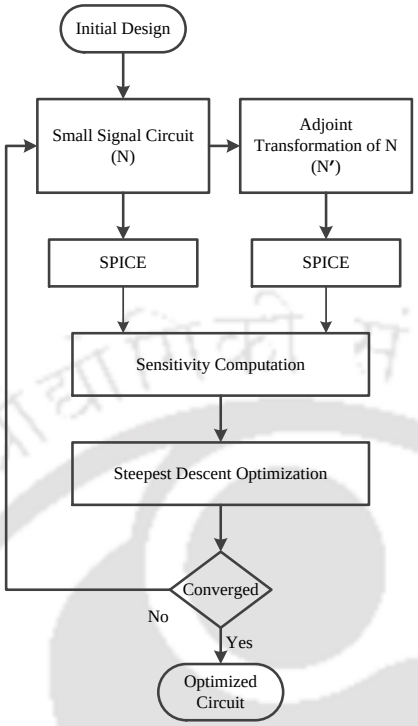


Figure 2.1: Optimization flow

These sensitivities provide the gradient vector of the cost function. Thus, with the help of SPICE simulations and sensitivity calculation the optimum solution can be obtained. The optimization process flow using ANSA is presented in Figure 2.1.

The optimization of two-port microwave networks has been proposed using adjoint network based sensitivity analysis [8], [55], which is further extended for the optimization of analog circuits. The proof of concept of proposed methodology has been demonstrated in [56] for basic analog circuits. The proposed methodology is discussed in detail in chapter 3.

2.3.2 Particle Swarm Optimization (PSO)

PSO is a population-based parallel stochastic search method which mimics the behavior of swarms to search for the global optimum through a multidimensional space [10]. Each swarm is considered as a particle in a multidimensional search space and the particles approach to the optimum solution based on their history and basic characteristics, such as position and velocity of current particles and their neighbors.

For optimization problem with n variables, a population size of N is generated randomly in the given variable range. In case of circuit optimization, these variables can be length (L), width (W), and transconductance (g_m) of a device (transistor). Fitness values are calculated for each particle and are tagged as $pbest$ and $gbest$ according to the personal and social performance of a particle. The position of a particle, updated iteratively, depends on the velocity of a particle. Particle velocity consists of present fitness value, random coefficients and previous velocity. For a particle in i^{th} iteration, if position and velocity are x_i and v_i respectively, the next position can be expressed as [57],

$$x_{(i+1)} = x_i + v_{(i+1)}, \tag{2.3}$$

and the velocity can be defined as,

$$v_{(i+1)} = wv_i + c_1r_1(gbest - x_i) + c_2r_2(pbest - x_i), \tag{2.4}$$

where, c_1 and c_2 are acceleration coefficients; r_1 and r_2 are random numbers generated uniformly between 0 and 1; and w denotes inertia. The trajectory of each particle towards personal and global best positions confirm the convergence to be globally optimum after satisfying specific design constraints. The details of PSO is described as a pseudocode in Algorithm 1. Figure 2.2 represents the movement of a particle in a search space using PSO.

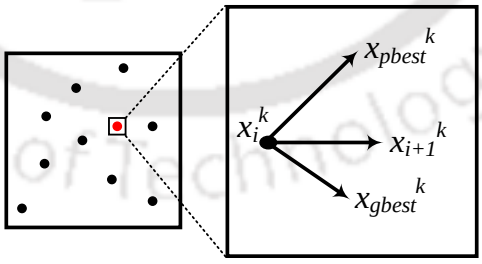


Figure 2.2: Performance of a particle in a 2D space using PSO.

2.3.3 Simulated Annealing (SA)

Simulated Annealing is based on the crystallization (annealing) process in metals. A local minimum of energy in a system is referred to different crystalline states. Similarly, randomly generated particles in multidimensional design space limited by a given set of circuit design variables are al-

Algorithm 1: Particle Swarm Optimization (PSO)

```
x_particle ← 0
x_pbest ← 0
for i ← 1, population_size do
    x_velocity ← random_velocity()
    x_position ← random_position()
    if f(x_pbest) > f(x_gbest) then
        x_gbest ← x_pbest
    end if
end for
while stoping_criteria do
    for x_particle ∈ population do
        x_velocity ← update_random_velocity()
        x_position ← update_random_position()
        fitness_value ← f(x_position)
        if fitness_value > f(x_pbest) then
            x_pbest ← x_position
            if f(x_pbest) > f(x_gbest) then
                x_gbest ← x_pbest
            end if
        end if
    end for
end while
return(x_pbest)
```

lowed to move towards a better solution or another local minimum, which exhibits a better cost function. A probability function controls acceptance of a solution with the cost in the next iteration. The probability of acceptance of such solutions decreases at every iteration. The selection of better solutions even with a lower probability enables SA to avoid getting trapped in local minimum. For i^{th} iteration, the value of cost function and the corresponding solution can be expressed as $f(x_i)$ and x_i, respectively. Solution in the next iteration (x_{i+1}) can be defined as,

$$x_{(i+1)} = x_i + \Delta x_i, \tag{2.5}$$

where, Δx_i is the difference between new cost function value and the current value, i.e., ($f(x_{i+1}) - f(x_i)$). In case of negative Δx_i, the probability of acceptance is unity ($p = 1$) and for the positive Δx_i, acceptance probability p is less than unity which can be expressed as,

$$p = e^{-\alpha \Delta f}, \tag{2.6}$$

where, α is the annealing parameter. In general, SA is used as a complement to other approaches for local refinement of the solutions [58]. The details of SA is described as pseudocode in Algorithm 2.

Algorithm 2: Simulated Annealing (SA)

```
initialize T by random()
prev_cost ← cost(solution)
TOL ← 1e − 06
initialize alpha
while T > TOL do
  generate points
  x ← points
  while x <= MAX do
    current_solution ← neighbor(solution)
    current_cost ← cost(current_solution)
    f(X) ← accept_probability(prev_cost, current_cost, T)
    if f(X) > R then
      sol ← new_sol
      old_cost ← new_cost
    end if
    x ← x + 1
    T ← alpha ∗ T
  end while
end while
```

Further, the random search of SA depends on the cooling effect of temperature. Let $T(x)$ be temperature at any instance x. Before starting SA, the initial temperature is computed by taking the mean of various randomized solutions. With the increase in time instance x, change in the temperature can be shown by using (2.7) [10].

$$T(x+1) = \alpha T(x) \tag{2.7}$$

where, α is a constant which is generated in the range $[0, 1]$. In each iteration, SA allows to search every step randomly based on the probability function f which leads to new states in solution space [10] and can be represented by using (2.8) [10].

$$f = \frac{1}{Z_T} \exp \frac{-\Delta E}{T} \tag{2.8}$$

where, $-\Delta E$ is difference between new and previous solution, Z_T is normalization factor, T denotes the cooling temperature ($\downarrow 0$). Again if $f > r_f$, the new solution is accepted, where r_f denotes a random number function, has random values in the range $[0, 1]$. r_f is generated using probability

density function [10].

$$r_f = \frac{1}{\sqrt{2\pi}\sigma} \exp \frac{-(x(i+1) - x(i))^2}{2\sigma^2} \tag{2.9}$$

where σ denotes standard deviation. The tendency to reach an optimum solution depends upon the choice of cooling function $T(t)$ and probability function f. During process of design using SA, if a step leads to a state having inefficient solution or no solution, the new state is allowed to have $f < 1$.

2.3.4 Metaheuristics

The PSO has a disadvantage of being trapped locally and having slow convergence. In comparison, SA has a tendency to avoid local optimum based on a serial stochastic search strategy [10]. Therefore to improve the search performance of PSO, a metaheuristic combining both PSO and SA is proposed in this thesis to analyze the analog circuit designing problem. Several metaheuristics of PSO have already been presented in literature, such as PSO-GA [59], PSO-ACO [60], PSO-SA [10] etc. The PSO-SA metaheuristic proposed in [10] makes use of cooling strategy of temperature to avoid local traps and pursue a global optimum solution for multiprocessor task scheduling problem in a multi-stage flow shop environment. In this thesis, different particles are allowed to move in the solution search space using PSO with random particle velocities. Then, the initial temperature is evaluated from velocity-temperature relation and multiple search spaces are chosen for different temperature ranges. Later the particles are allowed to move in those search spaces using SA to achieve the optimum solution for analog circuit designing problem. Further, the framework is extended to the improved search strategy based on Lévy flight method. In chapter 4, both the above mentioned methods are described in detail. These methods are extend to perform multi-objective optimization in chapter 5.

2.4 Design Examples

In the proposed work, some of the popular circuits are considered as design examples including a two-stage OpAmp [3], folded cascode OpAmp [3] and, LNA [61]. Although the details of these circuits are presented in the following chapters of the thesis, a generalized problem formulation is presented in this section.

In Hershenson et al. [50], the formulation of a circuit optimization problem is explained for a two-stage OpAmp. They have proposed the solution of optimization problem by using geometric programming. In the proposed work, similar formulation is employed with proposed methods in place of geometric programming. The design specifications of the test circuits are discussed in the chapters 3, 4 and 5. In the analytical formulations standard notations [3] are used.

2.4.1 Two-stage Operational Amplifier : OpAmp

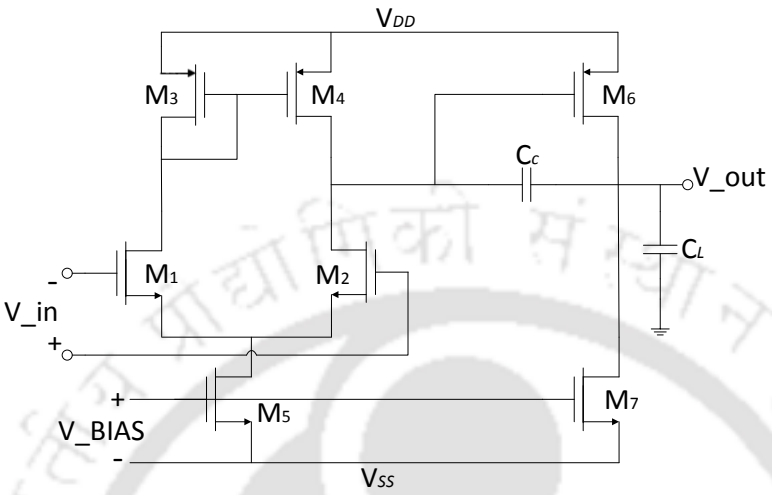


Figure 2.3: Two stage Operational Amplifier

$$
\begin{aligned}
\text{maximize} \quad & A_v = \frac{g_{m2} g_{m6}}{(g_{ds2} + g_{ds4})(g_{ds6} + g_{ds7})} \\
\text{subject to} \quad & L_{min} \leq L_i \leq L_{max}, \\
& SR = \frac{I_5}{C_c}, \\
& GB = \frac{g_{m1}}{C_c}, \\
& V_{in}\,(max) = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - |V_{T03}|\,(max) + V_{T1}\,(min)\,, \\
& V_{in}\,(min) = V_{SS} + \sqrt{\frac{I_5}{\beta_1}} + V_{T1}\,(max) + V_{DS5}\,(sat) \\
& g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_d}
\end{aligned}
$$

where, DC voltage gain is considered as objective function and the design space is bounded by performance specifications, i.e., slew rate, gain-bandwidth product, input voltage range, etc. Further, the choice of constraints varies according to the requirement of performance for a particular application.

2.4.2 Folded Cascode Operational Amplifier

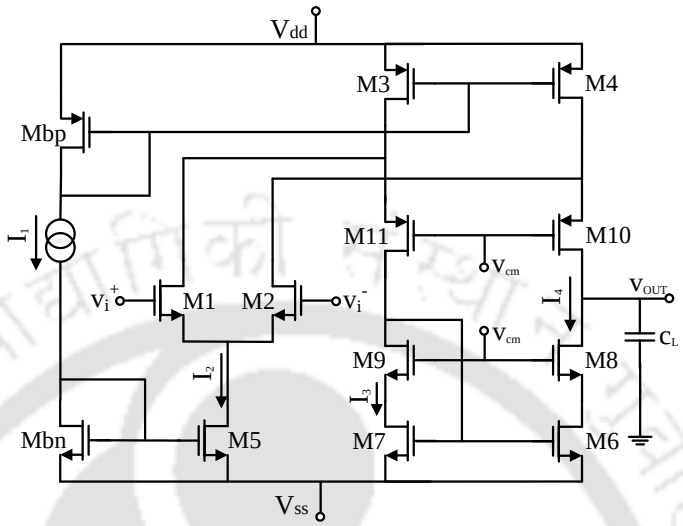


Figure 2.4: Folded Cascode Operational Amplifier circuit

$$
\begin{aligned}
\text{maximize} \quad & A_v = g_{m2}[g_{m8} r_{ds8} r_{ds6} \parallel (g_{m10} r_{ds10} (r_{o2} \parallel r_{o10}))] \\
\text{subject to} \quad & L_{min} \leq L_i \leq L_{max}, \\
& W_{min} \leq W_i \leq W_{max}, \\
& SR = \frac{I_b}{C_L}, \\
& GB = \frac{g_{m2}}{C_L}, \\
& V_{in}\,(max) = V_{DD} - V_{DS3} + V_{GS1} - V_{DS,sat1} \\
& V_{in}\,(min) = V_{SS} + V_{GS1} + V_{DS,sat5}, \\
& V_{out}\,(max) = V_{DD} - V_{DS4} - V_{DS,sat10}, \\
& V_{out}\,(min) = V_{SS} + V_{DS6} + V_{DS,sat8}
\end{aligned}
$$

Here, performance specifications such as gain-bandwidth product, slew rate, input voltage range and output voltage swing are employed as design constraints for maximum value of gain.

2.4.3 Low Noise Amplifier : LNA

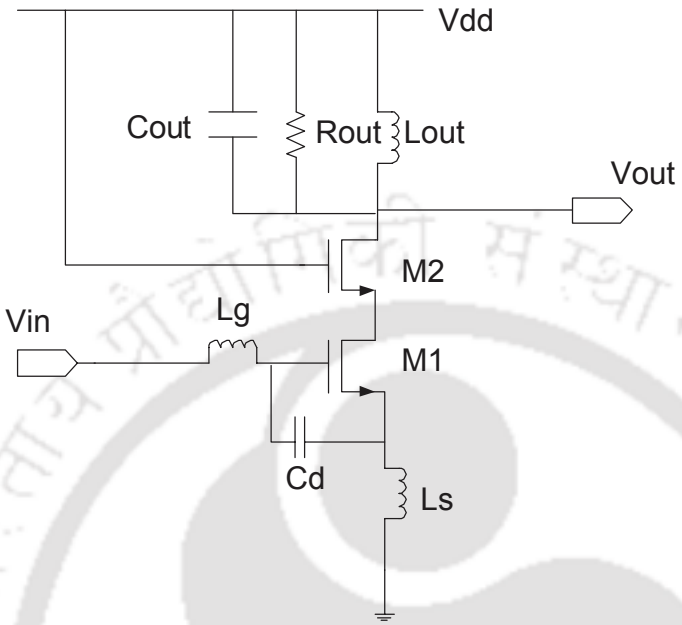


Figure 2.5: Low Noise Amplifier circuit

$$
\begin{aligned}
\text{minimize} \quad & F = 1 + \frac{4}{15}\frac{C_{gs}^2}{R_s g_m C_t^2} + \frac{4}{15}.\frac{C_{gs}^2\omega_0^2 R_s}{g_m} + \frac{2}{3}\frac{C_t^2\omega_0^2 R_s}{g_m} \\
\text{subject to} \quad & L_{min} \leq L \leq L_{max}, \\
& W_{min} \leq W \leq W_{max}, \\
& \left(\frac{g_m}{C_t}\right) L_s = 50, \\
& C_{gs} = \frac{2}{3} W L C_{ox}, \\
& \omega_0^2 = \frac{1}{L_t C_t}, \\
& g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L} I_d}
\end{aligned}
$$

Here, design constraints such as input impedance matching, tuning conditions and technology limitations are used as design constraints for minimizing the noise figure of LNA circuit.

2.4.4 Global Solutions

It is known that the solution generated by any optimization-based approach should be a global solution. It is quite possible that algorithm generates a local maximum or a local minimum resulting in an inferior design. In order to ensure the global solution, the analytical formulation of a circuit optimization problem can be transformed into a convex optimization formulation consisting of a set of posynomial expressions. Although the conversion into convex form introduces approximation errors, use of curve-fitting methods to model circuit's equations may improve the solutions as compared to approximated analytical formulae. The formulation of a two-stage operational amplifier is explained by Hershenson et al. in [50], and a general formulation of optimization problem can be expressed in the form given below.

$$\begin{aligned} & \text{minimize} && f_0(x) \\ \text{subject to } & f_i(\mathbf{x}) \leq 1\ , && i = 1, 2, ..., m, \\ & g_j(\mathbf{x}) = 1\ , && j = 1, 2, ..., p, \\ & x_k > 0\ , && k = 1, 2, ...n. \end{aligned}$$

where, f_0 is the objective (posynomial) function, f_i and g_j posynomials and monomials, respectively and **x** is vector of optimization variables. The objective function and constraints must be posynomial and it must be minimized. The examples of posynomials and monomials are given below.

- Posynomials: Let $(x_1, x_2, ..., x_n)$ be n real, positive variables. A function f is called posynomial function of x if it is in the form of,

$$f(x_1, x_2, ...x_n) = \sum_{k=1}^{t} c_k x_1^{\alpha_{1k}} x_2^{\alpha_{2k}} ... x_n^{\alpha_{nk}}$$

  where, $c_k \geq 0$ and the exponents $\alpha_{ik} \in \Re$, for $i = 1, 2, ..., n$.

- Monomials: When the posynomial consist of only one non-negative term in the summation, where $t = 1$ and $c_1 \geq 0$, then a monomial function is formed. A monomial is defined as a

function $g(x)$ which is expressed as,

$$g\left(x\right) = cx_1^{\alpha_1}x_2^{\alpha_2}...x_n^{\alpha_n}$$

where, the multiplicative constant $c \geq 0$ and the exponential constants $\alpha_i \in \Re$, for $i = 1, 2, ..., n$.

This type of problem formulation leads to the convex optimization problem, which upon solving provides the global solution. The design examples explained in this chapter are in the form of a convex formulation as square law model is used in the modelling of transistors. The expression of g_m is given in (2.10). The expression takes the non-posynomial form when the short-channel effects are included in the transistor model (2.11). Hence, this model can not be used for convex formulation. Further, the approximate analytical formulation as shown in (2.12) can be expressed in the posynomial/monomial form, after considering the short-channel effects.

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_d} = (2\mu_n C_{ox})^{0.5}W^{0.5}L^{-0.5}I_d^{0.5} \tag{2.10}$$

$$g_m = C_{ox}\mu_0 W\nu_{sat}.(1+\lambda V_{ds}).\frac{4m\nu_{sat}LV_{od} + (2m\nu_{sat}L\theta + \mu_0)V_{od}^2}{(2m\nu_{sat}L + (2m\nu_{sat}L\theta + \mu_0)V_{od})^2} \tag{2.11}$$

$$g_m = A_0 W^{A_1}L^{A_2}I_{ds}^{A_3} \tag{2.12}$$

In the thesis, to ensure global solutions, the square-law model is used for ANSA method. In case of heuristics (HPSO, l-HPSO, MHPSO, MHPSO-CD), the generation of a global solution is ensured by the combination of PSO and SA. Further, to avoid the complex analytical formulation, approximate model of g_m as shown in (2.12) is used to incorporate the short-channel effects and to make this solution more accurate.

2.5 Summary

A brief review of popular methods, which have been developed for the optimization of analog circuit is presented in this chapter. The approaches are broadly classified into the knowledge-based and optimization-based category on the basis of fundamental methods used to optimize the circuit. In the subsequent chapters, the proposed methods for analog circuit optimization are presented in detail.

3

Sensitivity Analysis and Circuit Optimization

Contents

This chapter presents the technique of analog circuit optimization by using adjoint network based sensitivity analysis (ANSA). In section 3.1, a brief introduction of classical approaches for sensitivity analysis (derivative estimation) is presented. These approaches include forward finite differences (FFD), backward finite differences (BFD), and central finite differences (CFD) formulation. ANSA is described in section 3.2, and the application of ANSA in analog circuit optimization is presented in section 3.3. The proposed methodology with the design examples is presented in section 3.4 and section 3.5, respectively. Section 3.6 summarizes the chapter.

3.1 Classical Methods for Sensitivity Analysis

Sensitivity analysis or derivative approximation holds a vital place in optimization theory. In general, finite difference methods are applied for the sensitivity analysis. In classical methods, each parameter is varied in turn leaving the others fixed at their nominal values. For a system response $f = f(\mathbf{p})$, the first-order sensitivities with respect to parameters ($\mathbf{p} = p_1, p_2, \ldots, p_n$) can be represented as,

$$\frac{\partial f}{\partial p_i} = \lim_{\Delta p_i \to 0} \frac{f(p_1, p_2, \ldots, p_i + \Delta p_i, \ldots, p_n) - f(p_1, p_2, \ldots, p_i, \ldots, p_n)}{\Delta p_i} \tag{3.1}$$

where, gradient vector can be represented as,

$$\bigtriangledown f = \left[\frac{\partial f}{\partial p_1}, \frac{\partial f}{\partial p_2}, \ldots \frac{\partial f}{\partial p_i}, \ldots, \frac{\partial f}{\partial p_n}\right] \tag{3.2}$$

The function f may be the noise figure of a low noise amplifier, the gain of an OpAmp, power dissipation or the chip area of a circuit. The (3.1) tells us how sensitive the function is with respect the parameter p_i, and the perturbation should be as small as possible to generate an accurate result. It can be approximated by the forward difference formula expressed in (3.3) as,

$$\frac{\partial f}{\partial p_i} \approx \frac{f(p_1, p_2, \ldots, p_i + \Delta p_i, \ldots, p_n) - f(p_1, p_2, \ldots, p_i, \ldots, p_n)}{\Delta p_i} \tag{3.3}$$

where, a finite small perturbation Δp_i is used. Other methods that can be utilized for approximating first-order derivatives including backward finite difference (BFD) and central finite difference (CFD) are given in (3.4) and (3.5), respectively.

$$\frac{\partial f}{\partial p_i} \approx \frac{f(p_1, p_2, \ldots, p_i, \ldots, p_n) - f(p_1, p_2, \ldots, p_i - \Delta p_i, \ldots, p_n)}{\Delta p_i} \tag{3.4}$$

$$\frac{\partial f}{\partial p_i} \approx \frac{f(p_1, p_2, \ldots, p_i + \Delta p_i, \ldots, p_n) - f(p_1, p_2, \ldots, p_i - \Delta p_i, \ldots, p_n)}{2\Delta p_i} \tag{3.5}$$

It can be observed from the expression of FFD and BFD that these approaches require one extra function evaluation for each parameter in forward and backward direction. Although CFD approach is more accurate when compared to FFD and BFD, it requires two extra function evaluation for each parameter. In order to estimate the sensitivity with respect to all n parameters, FFD and BFD require n extra function evaluations while CFD requires $2n$ extra function evaluations. For the perturbation of each parameter a complete circuit analysis is required, which makes sensitivity analysis computationally intensive. With scaling down of technology and increasing number of parameters, classical approaches of sensitivity analysis become counterproductive due to the increased computational cost.

Adjoint network sensitivity analysis offers an efficient approach for sensitivity estimation. Using at most one extra simulation of an adjoint system (or circuit), the first-order sensitivities of the desired response are evaluated with respect to all parameters in the circuit regardless of their number. These sensitivities can directly be used to derive the gradient of an objective function.

3.2 Adjoint Network Based Sensitivity Analysis

For describing the computation of adjoint network based sensitivity, relation between the original network and its adjoint transformation is discussed in this section. The adjoint network is derived using the original electrical network and is topologically identical to it. It exhibits a reciprocal direction of signal transmission (transmittance) when compared with the original network and has an incidence matrix equivalent to the transposition of incidence matrix of the original electrical network.

Let a set of linear system of equations to be $A\mathbf{x} = \mathbf{b}$. By performing absolute differentiation (neglecting higher order derivatives) on both sides, it can be written as,

$$A\delta\mathbf{x} + \delta A\mathbf{x} = \delta\mathbf{b} \quad \Rightarrow \; \delta\mathbf{x} = A^{-1}[\delta\mathbf{b} - \delta A\mathbf{x}] \tag{3.6}$$

Assuming a scalar performance function of $\Gamma(\mathbf{x})$,

$$\delta\Gamma = \left[\frac{\partial\Gamma}{\partial\mathbf{x}}\right]^T \delta\mathbf{x} \tag{3.7}$$

Using (3.6) and (3.7),

$$\delta\Gamma = \left[\frac{\partial\Gamma}{\partial\mathbf{x}}\right]^T A^{-1}[\delta\mathbf{b} - \delta A\mathbf{x}] \tag{3.8}$$

The adjoint network can be represented by the transpose of incidence matrix representing a system of equations. The sensitivity of the response of original network with respect to parameter **x** can be expressed by a vector $\boldsymbol{\eta}$ such that,

$$A^T\boldsymbol{\eta} = \left[\frac{\partial\Gamma}{\partial\mathbf{x}}\right] \Rightarrow \boldsymbol{\eta}^T = \left[\frac{\partial\Gamma}{\partial\mathbf{x}}\right]^T A^{-1} \tag{3.9}$$

Substituting (3.9) in (3.8),

$$\delta\Gamma = \boldsymbol{\eta}^T[\delta\mathbf{b} - \delta A\mathbf{x}] \tag{3.10}$$

The sensitivities of function Γ can be calculated by solving (3.10). The original electrical network where the transistors are represented by their small signal equivalent circuits, is analyzed using Modified Nodal Analysis (MNA) [62]. The system matrix generated during the analysis can be described as,

$$\begin{bmatrix} A_{rG}GA_{rG}^T & A_{rT'} \\ NA_{rT'}^T & M \end{bmatrix} \begin{bmatrix} \boldsymbol{v}_b \\ \boldsymbol{i}_{T'} \end{bmatrix} = \begin{bmatrix} -A_{rJ}i_J \\ S_{T'} \end{bmatrix} \tag{3.11}$$

where, $\boldsymbol{v}_b$ and $\boldsymbol{i}_{T'}$ denote a vector of node potentials and branch currents in T' type branches (which represent devices other than the conductances and current sources), respectively. A_r is reduced incidence matrix of the given network $(A\mathbf{i} = 0)$. Further, A_r is partitioned into three sub-matrices as,

$$A_r \equiv \left(A_{rG} \vdots A_{rT} \vdots A_{rJ}\right)$$

where, A_{rG}, A_{rJ}, and A_{rT} representing conductance, current sources and coefficients of elements other than conductances and current sources, respectively. The matrix $[M \;\; N]$ represents characteris-

tics of any device other than conductance and current sources. $S_{T'}$ can be expressed as,

$$\begin{bmatrix} M & N \end{bmatrix} \begin{bmatrix} \boldsymbol{i}_{T'} \\ \boldsymbol{v}_{T'} \end{bmatrix} = S_{T'} \tag{3.12}$$

The formulation in (3.11) can be applied to transistors, transformers and all linear components in the electronic circuit. The adjoint of this circuit can be represented by taking the transpose of the coefficient matrix as shown in (3.11).

$$\begin{bmatrix} (A_{rG}GA_{rG}^T)^T & -(NA_{rT'}^T)^T \\ -(A_{rT'})^T & M^T \end{bmatrix} \begin{bmatrix} \hat{\boldsymbol{v}_b} \\ \hat{\boldsymbol{i}_{T'}} \end{bmatrix} = \begin{bmatrix} \hat{I_j} \\ \hat{S_{T'}} \end{bmatrix} \tag{3.13}$$

where, vectors $\hat{\boldsymbol{v}_b}$ and $\hat{\boldsymbol{i}_{T'}}$ represent source excitations of adjoint network. By substituting (3.13) in (3.9), we obtain the adjoint variables as,

$$\boldsymbol{\eta} = \begin{bmatrix} \hat{\boldsymbol{v}_b} \\ \hat{\boldsymbol{i}_{T'}} \end{bmatrix} \tag{3.14}$$

3.3 Application of Sensitivity Analyses in Analog Circuit Optimization

In the proposed work, analog circuit optimization problem is formulated in the form of analytical models with objective function (e.g., gain and noise figure) being optimized under a set of constraints (e.g, biasing boundaries, area, power, and performance specifications). The solution of this such set of equations with constraints requires first order derivatives which can be provided by sensitivity analysis. In such derivative-based optimization techniques [63], new position is updated by using the following expression,

$$p(k+1) = p(k) + \alpha s(k), \tag{3.15}$$

where, $s(k)$ is search direction and α is the step taken in that direction. We utilize sensitivities computed by the analysis of original circuit and its adjoint transformation to determine the search direction $s(k)$ using steepest descent method [64] as,

$$s(k) = - \bigtriangledown f(p_k),$$

where, $\bigtriangledown f(p_k)$ is gradient (first-order sensitivities) of the objective function to be minimized.

3.4 Proposed Methodology

In this section, steps for optimization of an analog circuit using adjoint network based sensitivity analysis are presented. This method can be applied to compute gradient of the objective function without any topological changes in the circuit.

- **Step 1.** The original analog circuit is transformed into an equivalent electrical circuit by replacing MOSFETs with its small signal model and analyzed using SPICE [65]. It should be noted that we have experimented with the initial design of circuit parameters generated by using square law model of MOSFET to validate the proposed method. However, the accuracy of the solution can be improved by using higher level MOSFET models for small signal circuit analysis.

- **Step 2.** Later, adjoint of the equivalent electrical circuit obtained in **Step 1** is formulated. The small signal model of an NMOS transistor and its adjoint transformation are shown in Figure 3.1(a) and (b), respectively. The details of this transformation is discussed in [56] and [66]. The rules by which adjoint of an electrical circuit is transformed are described below for completeness.

  (i) Linear resistor nodes remain unchanged in the adjoint circuit.

  (ii) All independent voltage sources are short-circuited and all independent current sources are open-circuited.

  (iii) For a VCCS in Figure 3.1, the controlling and the controlled edges are exchanged in the adjoint circuit.

  (iv) A one ampere current source is added to the adjoint circuit in parallel where response needs to be determined.

Adjoint transformation of the original analog circuit is analyzed by SPICE to evaluate the DC operating point.

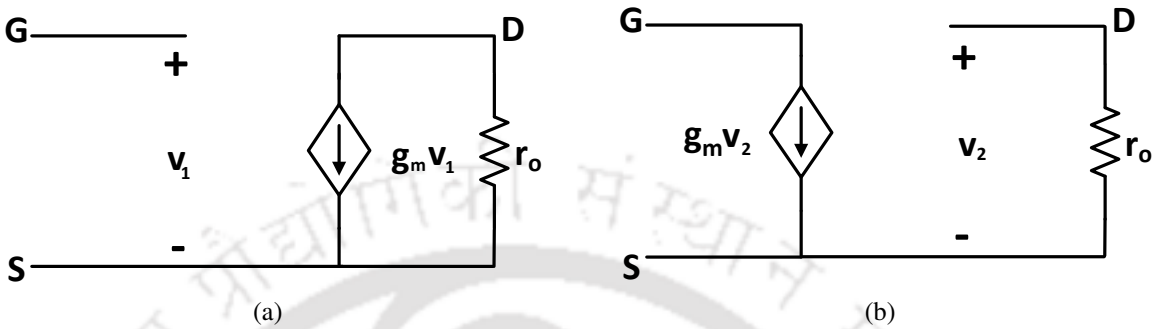


Figure 3.1: Small signal equivalent of an (a) NMOS transistor and (b) its adjoint transformation

An example of cascode amplifier is presented here to illustrate the rules of adjoint transformation. First, original circuit (Figure 3.2(a)) is represented into a small signal equivalent circuit (Figure 3.2(b)) and then it is transformed into its adjoint circuit (Figure 3.2(c)) according to the rules stated above. By the analysis of circuits in Figures 3.2(b) and 3.2(c) using SPICE sensitivity of V_{out} with respect to g_m and r_o is estimated.

- **Step 3.** Using initial values of the design parameters, adjoint network based sensitivity analysis is employed to evaluate the objective function in the optimum direction through various iterations. Let the objective function of electrical network be $F(V_{out}, \boldsymbol{\alpha})$ where, V_{out} denotes response of the network and $\boldsymbol{\alpha}$ denotes vector of the design parameters. In the i^{th} iteration, sensitivities of V_{out} with respect to $\boldsymbol{\alpha}$ can be expressed as,

$$\nabla F(\boldsymbol{\alpha}^i) = \frac{\partial F}{\partial \boldsymbol{\alpha}^i} = \beta \left[\frac{\partial V_{out}^i}{\partial \boldsymbol{\alpha}^i}\right] = \beta \left[\frac{\partial \Gamma^i}{\partial \boldsymbol{\alpha}^i}\right] \tag{3.16}$$

where, $\frac{\partial V_{out}^i}{\partial \boldsymbol{\alpha}^i}$ is equivalent to the expression given in (3.8) and β is a functional relation between the circuit response and objective function. From (3.11), (3.13), and (3.16), sensitivity of the output voltage [9] can be expressed as,

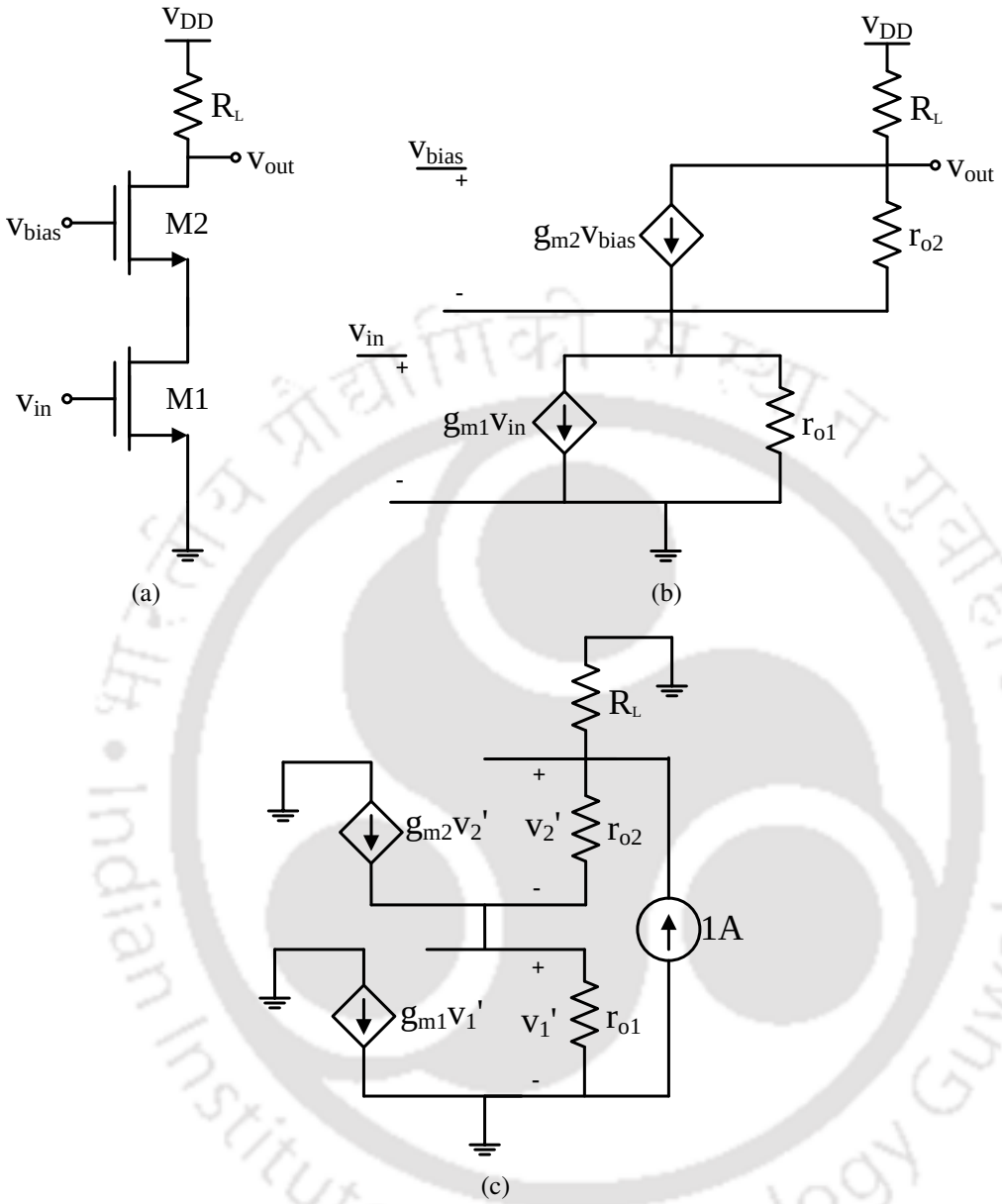


Figure 3.2: (a) Original circuit, (b) Small signal equivalent circuit, (c) Adjoint transformation

$$\left[\frac{\partial V_{out}^{i}}{\partial \boldsymbol{\alpha}^{i}}\right] = \begin{bmatrix} \boldsymbol{v}_b \\ \boldsymbol{i}_{T'} \end{bmatrix}^{T} \begin{bmatrix} \frac{\partial (A_{rG} G A_{rG}^{T})^{T}}{\partial \boldsymbol{\alpha}^{i}} & -\frac{\partial (N A_{rT'}^{T})^{T}}{\partial \boldsymbol{\alpha}^{i}} \\ -\frac{\partial (A_{rT'})^{T}}{\partial \boldsymbol{\alpha}^{i}} & \frac{\partial M^{T}}{\partial \boldsymbol{\alpha}^{i}} \end{bmatrix} \begin{bmatrix} \hat{\boldsymbol{v}}_b \\ \hat{\boldsymbol{i}}_{T'} \end{bmatrix} \tag{3.17}$$

For $\boldsymbol{\alpha} = \left[A_{rG} G A_{rG}^{T}\right]^{T}$ (perturbation across conductance elements), the gradient $\frac{\partial V_{out}^{i}}{\partial \boldsymbol{\alpha}^{i}}$ can be

formulated as,

$$\left[\frac{\partial V_{out}^{i}}{\partial \boldsymbol{\alpha}^{i}}\right] = \left[\boldsymbol{v}_b \hat{\boldsymbol{v}}_b\right]^T \tag{3.18}$$

Thus, the sensitivities of output response can be calculated by the solution (node voltages and branch currents) of original and adjoint circuits.

- **Step 4.** After evaluating all the sensitivities, design parameters are updated by applying steepest descent/ascent method (as per the requirement of cost function to be minimized/maximized) using $\boldsymbol{\alpha}^i = \boldsymbol{\alpha}^{i-1} \mp \theta^{i-1} \nabla F(\boldsymbol{\alpha}^{i-1})$, where θ is stepsize determined by BB method [67].

$$\theta^i = \frac{\left[\nabla F(\boldsymbol{\alpha}^{i+1}) - \nabla F(\boldsymbol{\alpha}^i)\right]\left[\boldsymbol{\alpha}^{i+1} - \boldsymbol{\alpha}^i\right]^T}{|\nabla F(\boldsymbol{\alpha}^{i+1}) - \nabla F(\boldsymbol{\alpha}^i)|^2} \tag{3.19}$$

The parameters are updated in both the original and adjoint transformed circuits. These steps are iterated until convergence is achieved as per the chosen criteria.

It is required to formulate the analytical model of the analog circuit in such a way that its solution leads to the global solution. In chapter 2, prerequisites for obtaining the global solution are discussed in section 2.4.4.

3.5 Design Examples

3.5.1 Cascode Amplifier

In this section, the proposed optimization approach is applied on a cascode amplifier circuit (as shown in Figure 3.2(a)) having two nMOS transistors M1 and M2 for the optimization of gain. Both transistors are assumed to be of same channel length.

The process parameters required for the experiment are extracted from $180nm$ CMOS bulk process technology. After forming a small signal circuit of the cascode amplifier, the proposed adjoint method can be applied to this circuit directly to form an equivalent adjoint circuit by following the rules explained in previous section. After constructing the adjoint circuit, objective function is formulated by variables transconductances (g_{m1} , g_{m2}) and drain to source resistances (r_{o1} , r_{o2}) of both the transistors. The experiment is performed for observing variation in the gain parameter of the amplifier

circuit. The absolute value of gain G of the amplifier circuit in Figure 3.2(a) can be approximated by the following mathematical equation.

$$|G| \approx g_{m1} g_{m2} r_{o1} r_{o2} \tag{3.20}$$

Table 3.1: Experimental steps of proposed approach till convergence

Steps	$\bigtriangledown f(\alpha^1)$	$\bigtriangledown f(\alpha^2)$	$\bigtriangledown f(\alpha^3)$	$\bigtriangledown f(\alpha^4)$	$\lvert\theta\rvert$	$g_{m1}(mS)$	$g_{m2}(mS)$	$r_{o1}(k\Omega)$	$r_{o2}(k\Omega)$	G
1	9.839e+03	1.36e+04	9.325e-06	1.902e-05	0	0.457	0.395	3.37	8.84	5.3
2	9.92e+03	1.37e+04	9.46e-06	1.9341e-05	3.57e-10	0.460	0.399	3.37	8.84	5.485
3	10.03e+03	1.382e+04	9.65e-06	1.976e-05	4.24e-10	0.464	0.405	3.37	8.84	5.5983
4	10.12e+03	1.394e+04	9.83e-06	2.021e-05	4.3219e-10	0.468	0.410	3.37	8.84	5.7339
5	10.23e+03	1.41e+04	10.013e-06	2.063e-05	4.0739e-10	0.472	0.415	3.37	8.84	5.84654
6	10.41e+03	1.4261e+04	10.332e-06	2.139e-05	6.579e-10	0.47872	0.4243	3.37	8.84	6.0506
7	10.524e+03	1.439e+04	10.546e-06	2.191e-05	4.269e-10	0.48316	0.4304	3.37	8.84	6.195
8	10.641e+03	1.452e+04	10.758e-06	2.2412e-05	4.23e-10	0.4876	0.4364	3.37	8.84	6.34062
9	10.768e+03	1.467e+04	11.00e-06	2.298e-05	4.263e-10	0.4921	0.443	3.37	8.84	6.4889
10	10.883e+03	1.48e+04	11.184e-06	2.35e-05	4.039e-10	0.4965	0.4489	3.37	8.84	6.64
11	11.022e+03	1.495e+04	11.474e-06	2.412e-05	4.8871e-10	0.502	0.4561	3.37	8.84	6.829
12	11.11e+03	1.512e+04	11.699e-06	2.457e-05	3.819e-10	0.506	0.461	3.37	8.84	6.9643
13	11.214e+03	1.516e+04	11.835e-06	2.49e-05	3.332e-10	0.511	0.466	3.37	8.84	7.0765
14	11.233e+03	1.516e+04	11.855e-06	2.504e-05	4.514e-11	0.509	0.467	3.37	8.84	7.08136
15	11.23e+03	1.52e+04	11.86e-06	2.51e-05	2.605e-18	0.5087	0.467	3.37	8.84	7.0814

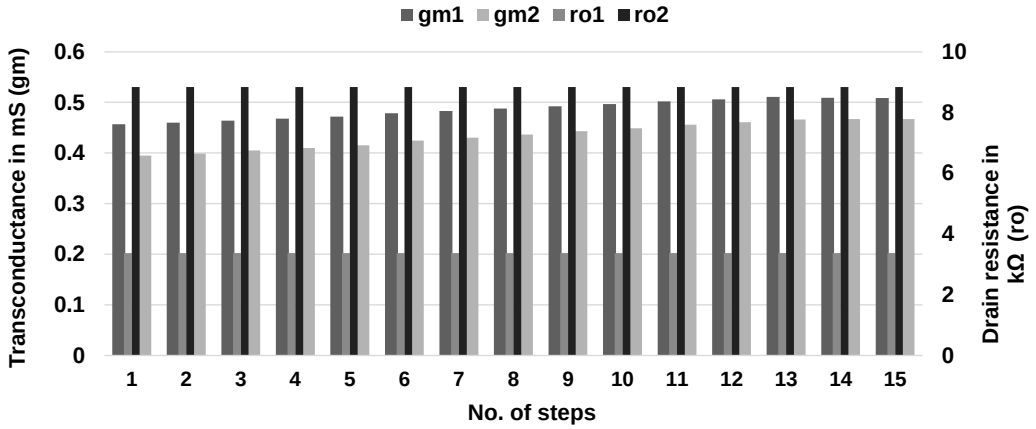


Figure 3.3: Values of design parameters g_{m1}, g_{m2} in mS and r_{o1} , r_{o2} in kΩ,

The iterative solutions of small signal analysis circuit and its adjoint show that there is an increase in the value of gain G which settles at 17 dB after 15 steps. All experimental results are listed in Table

3.1. The gradient of objective function $\bigtriangledown f(\alpha^i)$ having four elements $(i = 1,\ 2,\ 3,\ 4)$ listed in Table 3.1 is obtained by (3.16). It is found that the sensitivities with respect to r_{o1} and r_{o2} are negligible as compared to transconductances (g_{m1}, g_{m2}) as shown in Figure 3.3. The transconductances (g_{m1}, g_{m2}) play an important role in affecting the DC sensitivity of the cascode amplifier in a greater way than the drain to source resistances r_{o1} and r_{o2}. Figure 3.3 shows different values of circuit parameters g_{m1}, g_{m2}, r_{o1} and r_{o2} obtained during different steps of the analysis. It is evident from Figure 3.4 that the stepsize θ (as shown in **Step 4**) does not change very fast which causes design vector to move in an optimal direction very smoothly and precisely. This specific merit of proposed method empowers us to design complex analog circuits having multiple elements and to optimize these circuits for a variety of design parameters like gain, bandwidth, unity gain frequency etc. in a well-defined manner.

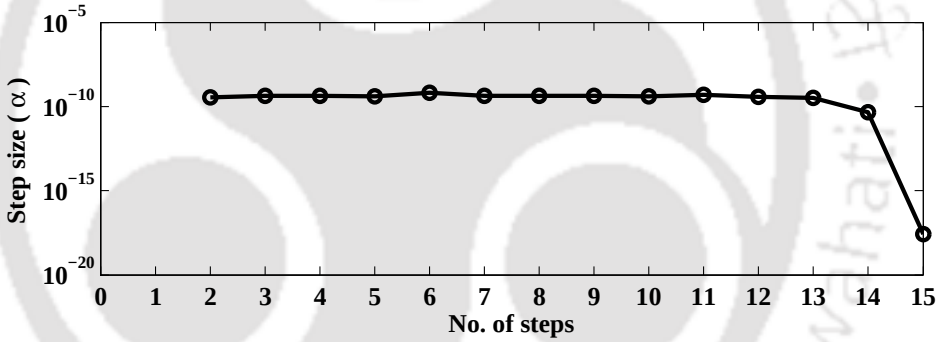


Figure 3.4: Variation of stepsize α in log-scale with respect to experimental steps.

The sensitivity of design parameters for the next iteration is obtained using the gradient of an objective function in every iteration. For the cascode amplifier circuit in Figure 3.2(a), the design parameters are transconductances and drain-to-source resistances. As both bandwidth and unity gain frequency can be derived mathematically from transconductance (g_m), it is now possible to optimize these two design parameters without even calculating the gradient of objective functions. These variations are shown in Figure 3.5. Hence, the proposed adjoint sensitivity method (ASM) can be applied only once to optimize multiple design parameters simultaneously which makes it an interesting approach to optimize analog circuits as per the given specifications.

For verification of the proposed approach, gain G of the cascode amplifier obtained by ASM is compared with the gain obtained by analyzing this circuit using Mentor Graphics's layout tool

Pyxis (Eldo) as shown in Figure 3.6. The relative error of the solutions obtained by using above mentioned methods is calculated by using (3.21). It is found that the error reported using this equation while comparing the solution of our proposed method with the solution provided by Pyxis (Eldo) is contained within 0.02%.

$$\%\ of\ error = \frac{G_{ASM} - G_{Mentor}}{G_{ASM}} \times 100 \tag{3.21}$$

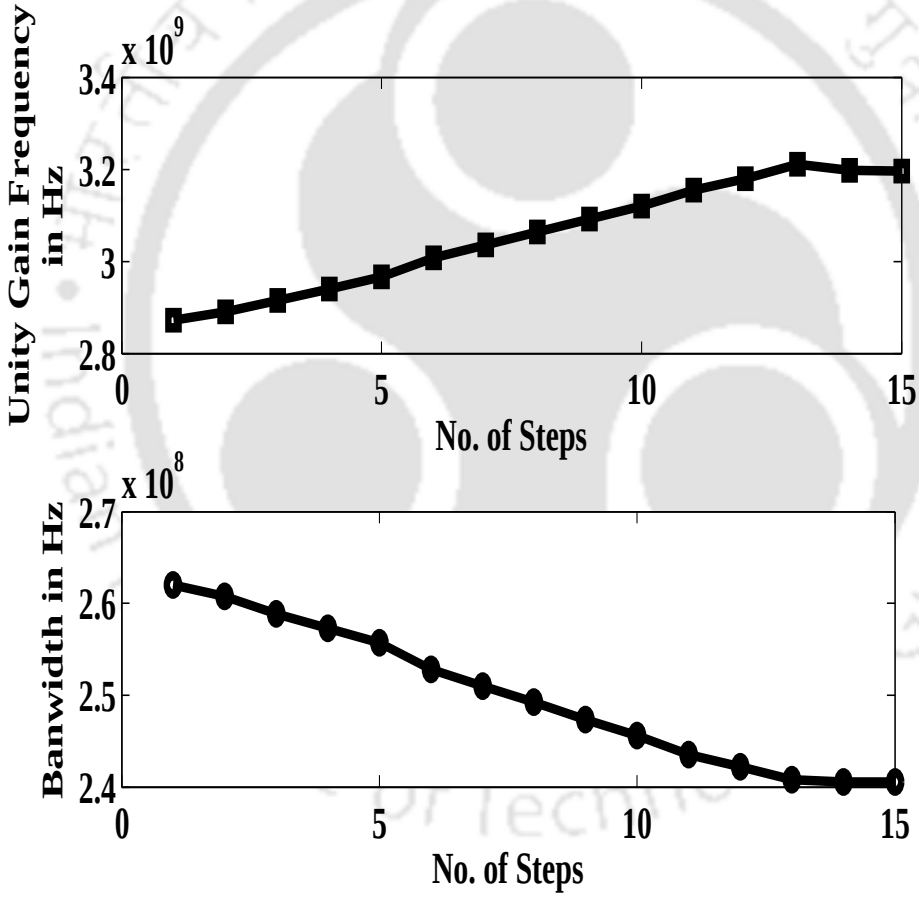


Figure 3.5: Variation of unity gain frequency and bandwidth of cascode amplifier circuit with respect to number of steps.

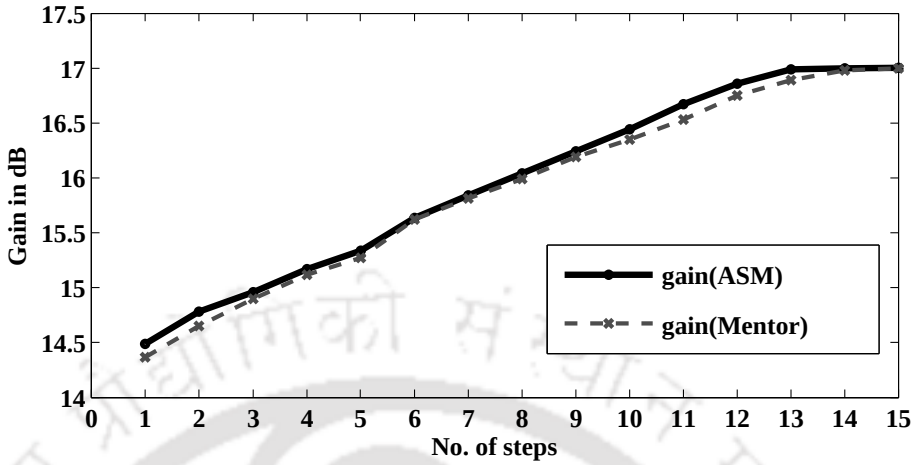


Figure 3.6: Variations of gain of adjoint sensitivity method (ASM) and gain obtained from Mentor Graphics in dB with respect to experimental steps.

3.5.2 Two-stage OpAmp Design Optimization

OpAmp is considered [50] one of the essential building block of analog electronics due to its versatile functionalities. A two-stage OpAmp shown in Figure 3.7(b) is considered as a test circuit to demonstrate the effectiveness of the proposed approach. The circuit shown in Figure 3.7(a) is a combination of startup circuit and voltage reference circuit. This circuit provides fixed biasing voltage to the OpAmp circuit. The OpAmp consists of a differential input stage with an active load as the first stage and common-source configuration with an active load as the second stage.

Assuming this OpAmp as a part of a system having capacitive load in the range of a few pico-farads.The capacitor C_c (Miller capacitance) and the resistor R_c are used for pole and zero compensation, respectively. V_{DD} and V_{SS} are positive and negative symmetrical supply voltages, respectively. In this circuit, V_{SS} is considered as grounded. V_{in}^{+} and V_{in}^{-} are differential voltage inputs which represents non-inverting and inverting voltage inputs, respectively. V_{out} denotes the output voltage at the second stage of the OpAmp. The transistor pairs M1-M2 and M3-M4 in OpAmp circuit are matched. The second stage of OpAmp consists of M5 and M6 transistors and the role of M7 is to provide required current to the differential stage. Voltage reference circuit is shown in Figure 3.7(a), which consists of NMOS matched pairs (Q1-Q2, Q3-Q4) and PMOS matched pairs (Q5-Q6, Q7-Q8).

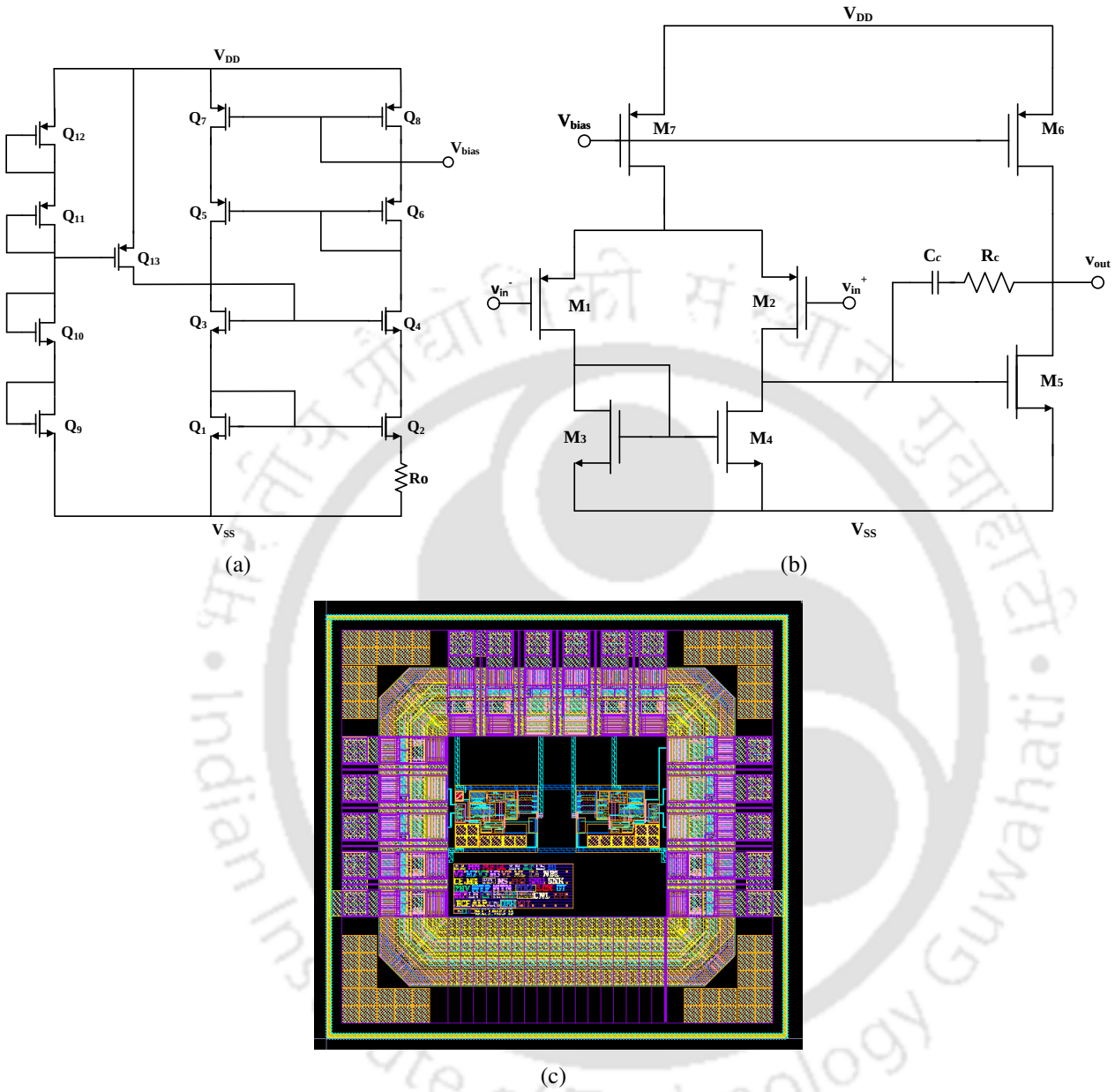


Figure 3.7: (a) Startup and voltage reference circuit, (b) Two-stage OpAmp circuit and (c) layout of the OpAmp circuit

Voltage output at the source of Q6 is fed to the OpAmp as a fixed biasing voltage V_{bias}. Startup circuit (Q9, Q10, Q11, Q12, and Q13) prevents effects of temperature variation on the generation of the fixed voltage reference. The analytical formulation of OpAmp circuit is represented in the form of convex functions of design variables (i.e., g_m and r_{ds}) and its design specifications. The design constraints are listed in Table 3.2.

Table 3.2: Desired design specifications of OpAmp

Design specifications	Constraints
Open loop voltage gain (A_v)	$\geq$ 70 dB
Unity gain bandwidth (UGB)	$\geq$ 2.5 MHz
Phase margin (PM)	$\geq 70°$
Power consumption	$\leq$ 15 mW
Slew rate	$\geq 2V/\mu s$

Table 3.3: Parameter values for OpAmp circuit

S.N.	Element name	Channel length (μm)	Channel width (μm)	Multiplying factor
1.	M1	1.2	9.15	2
2.	M2	1.2	9.15	2
3.	M3	3.6	6.1	4
4.	M4	3.6	6.1	4
5.	M5	3.6	28.35	10
6.	M6	2	6.1	6
7.	M7	2	3.7	1
8.	R0	10	4	4
9.	C0	30	30	4

3.5.2.1 Results and Discussion

Channel width (W) and channel length (L) etc. of the transistors are considered as design parameters for the optimization process. W and L obtained by the proposed method are listed in Table 3.3. MOS transistors used as compensation resistance and capacitance (R_0 and C_0) are also listed in Table 3.3. In order to validate performance of the proposed method, design specifications (i.e., slew rate, unity gain bandwidth (UGB), etc.) are calculated using Cadence Virtuoso [11]. The OpAmp circuit is designed by using optimal W and L values, and it is fabricated using $180nm$ bulk CMOS process technology. A layout of the designed OpAmp is shown in Figure 3.7(c). This layout was designed under the expert guidance of *Semiconductor Laboratory, Chandigarh, India*, and was fabricated at their facility. The chip was tested and characterized there. In Table 3.4, the design specifications obtained through simulations in the form of corner values are compared with the post-fabrication test results under different test conditions. Simulation results shown in Table 3.5 are generated by including the effect of process mismatch during corner analysis of the circuit. The typical value and the range of Monte Carlo simulation including process mismatch are presented in Table 3.5. For example UGB at TT corner denotes that 2.34 MHz is the typical value of UGB and it can vary over the range of 2.23 to 2.44 MHz. UGB of the circuit at SS corner is close to the measured UGB whereas, UGB of the circuit for TT and FF corners are close to the constraint value of UGB (Table 3.2). This indicates that the fabricated device lies near the SS corner. The difference between the measured and simulated

Table 3.4: Simulated and measured results (where, CL is load capacitance, G is unity gain, ACL is closed loop gain, and R2, R1 are the standard notation of feedback elements in closed loop)

Specification	Simulation Results	Test Inputs	Test Conditions (Typ.)	Test Results
Offset Voltage	771 - 804 μV	$V_{dd} = 3.3V$ $V_{in}^{+}(DC) = 1.65V$	G = +1	800 μV
Output Voltage High (V_{OH})	$V_{OH} \geq 3.18$ V	VDD = 3.3 V V_{in}^{+} (DC) = 1.65 V V_{in}^{-}(RAMP) = 1.65V + 0.1V_{pp} (f = 100kHz)	ACL = -10 R2/R1 = 1K/0.1K	3.27 V
Output Voltage Low (V_{OL})	$V_{OL} \leq 0.19$ V	VDD = 3.3 V V_{in}^{+} (DC) = 1.65 V V_{in}^{-}(RAMP) = 1.65V + 0.1V_{pp} (f = 100kHz)	ACL = -10 R2/R1 = 1K/0.1K	0.14 V
VOUT (PSRR)	56.13 dB - 108 dB	VDD = 3 V to 3.6 V V_{in}^{+} (DC) = 1.65 V	G = +1	63.52 dB
Input Voltage Range (ICMR)	$V_{IH} \geq 2.38$ V $V_{IL} \leq 0.098$	VDD = 3.3 V V_{in}^{+} (RAMP) = 1.65 V + 3.3 Vpp (f = 100kHz)	G = +1	2.760 V 0.08 V
Slew Rate (Rise)	2.9 - 3.79 V/μs	VDD = 3.3 V V_{in}^{+}(SQUARE) = 2 V_{pp} (f = 100kHz)	G = +1 CL = 10 pF	2.065 V/μs
Slew Rate (Fall)	3.1 - 3.81 V/μs	VDD = 3.3 V V_{in}^{+}(SQUARE) = 2 V_{pp} (f = 100kHz)	G = +1 CL = 10 pF	2.236 V/μs
Settling Time to 0.05% (Rise)	736 - 285 ns	V_{out} = 1 V STEP	G = +1 CL = 10 pF	590 ns
Unity Gain Bandwidth (UGB)	1.52 - 4.07 MHz	VDD = 3.3 V V_{in}^{+} (SINE) = 1.65 V + 1 V_{pp} (frequency sweep)	G = +1 CL = 10 pF	1.23 MHz

UGB (SS corner) may be due to the capacitances of bond wires and pads, the effects of which are not included in Monte Carlo analysis.

Table 3.5: Corner analysis of simulation results

Specification	Process Corners - value, (range)		
	FF	TT	SS
Offset Voltage (μV)	780.06, (771.3 - 790.4)	785.07, (776.85 - 794.2)	791.26, (780.9 - 804.2)
V_{OH} (V)	3.5, (3.47 - 3.54)	3.48, (3.41 - 3.52)	3.21, (3.18 - 3.31)
V_{OL} (V)	0.142, (0.135 - 0.146)	0.148, (0.138 - 0.153)	0.16, (0.12 - 0.19)
V_{IH} (V)	2.55, (2.518 - 2.567)	2.51, (2.47 - 2.516)	2.39, (2.388 - 2.434)
V_{IL} (V)	0.071, (0.062 - 0.0823)	0.076, (0.068 - 0.0903)	0.082, (0.077 - 0.098)
PSRR (dB)	84.1, (65.93 - 108.8)	79.9, (57.48 - 100)	71.75, (56.13 - 93.25)
Slew Rate (V/μs)	3.425, (3.152 - 3.796)	3.323, (2.989 - 3.633)	3.128, (3.043 - 3.562)
UGB (MHz)	3.75, (3.38 - 4.07)	2.34, (2.23 - 2.44)	1.56, (1.52 - 1.59)

Gain obtained after fabrication is $84dB$ with a unity gain bandwidth of $1.23MHz$. Power consumption is reported as $13mW$ under the supply voltage of $3.3V$. Further, ICMR is found to be

$0.08V - 2.76V$ with output swing of $3.27V - 0.14V$. PSRR of $63.52dB$ and phase margin of $> 70°$are measured. Load capacitance C_L of $10pF$ is considered for measurement of slew rate and unity gain bandwidth.

In the proposed work, a methodology based on analog network sensitivity analysis is presented to reduce manual effort in analog circuit design process. The main advantage of this approach is low computation cost (i.e., of the order (N+1)). The CPU-time of adjoint sensitivity analysis is significantly low when compared with direct forward/backward finite-difference sensitivity approximations [8]. The efforts made for the manual derivation of analytical expressions for the design specifications (objective function and constraints) can be reduced by automatic generation of design specification by various techniques illustrated in [68] and [69]. In the present form, the main disadvantage of the proposed approach is the requirement of initial design (properly biased transistors) to start the optimization process. The initial design, generated by g_m/I_D method [70] can provide better optimization results when compared with the design, obtained by square law equations model. Future scope of proposed methodology includes the development of an automated framework and incorporation of complex circuit models.

3.6 Summary

In this chapter, an adjoint network based sensitivity analysis (ANSA) method is presented for the optimization of analog circuits. This method enables the use of same simulation kernel for the evaluation of different sensitivities which reduces computational efforts significantly. The applicability of the proposed method is demonstrated by designing two basic analog circuits using the proposed methodologies. However, this approach may also be applied for the optimization of complex circuits/systems. Similarly, other design specifications of analog/RF circuits, e.g., Noise Figure, input/output impedance matching etc., can also be optimized using the proposed method. It can be integrated into circuit analysis tools for optimization of complex analog circuits in a natural way. The post-fabrication measurement results of a two-stage OpAmp circuit are reported along with the simulation results of optimized circuit parameters to validate the effectiveness of the proposed method.

भारतीय प्रौद्योगिकी संस्थान गुवाहाटी
Indian Institute of Technology Guwahati

4

Analog Circuit Optimization using Metaheuristics

Contents

The ANSA methodology described in the earlier chapter is an effective technique for analyzing circuits with reduced runtime and memory requirement. However, the proposed technique works better for convex problems. The analog circuit optimization problem can also be addressed very efficiently by using of metaheuristics. In section 4.1, a hybrid of PSO and SA (HPSO) is proposed. The improved version of HPSO based on Lévy Flight (l-HPSO) is presented in section 4.2. In section 4.3, design examples, namely two-stage OpAmp, OTA and LNA circuit are illustrated. To show the effectiveness of proposed methods, section 4.4 presents the comparison between the proposed techniques and the standard algorithms using test circuits and standard test functions. In section 4.5, a summary of this chapter is presented.

4.1 Proposed Hybrid Optimization Approach

This section depicts the proposed optimization approach (as shown in Figure 4.1) to design analog circuits for certain design parameters through a metaheuristic, which integrates the advantages of both PSO (fast convergence rate) and SA (avoid local traps). In the proposed approach, the process of annealing is utilized to pursue the search for an optimum solution so that premature convergence of PSO can be avoided. PSO contributes to this approach in a way to ensure that the random search converges faster within the solution space, while SA avoids local traps. If SA is employed at each iteration along with PSO, the cost of computations will increase arbitrarily and at the same time convergence rate of PSO may be declined. In order to have a better solution and to minimize the computational cost by integrating PSO with annealing process, SA is performed after the completion of PSO. Therefore, the proposed metaheuristic is able to sustain fast convergence rate of PSO with the aid of simulated annealing.

In this metaheuristic, each particle position x_i ($\in N$) is initialized with a random number given the value of any design constraint to start with. Later, the fitness value is evaluated according to the particle having personal best (x_{pbest}) and global best (x_{gbest}) positions. The fitness value is regarded as the objective function which serves as a solution for each displacement of a particle in the solution space. After each iteration, the particle moves within the solution space with a random velocity. After a single run of PSO, velocity values of different particles are encoded to evaluate different

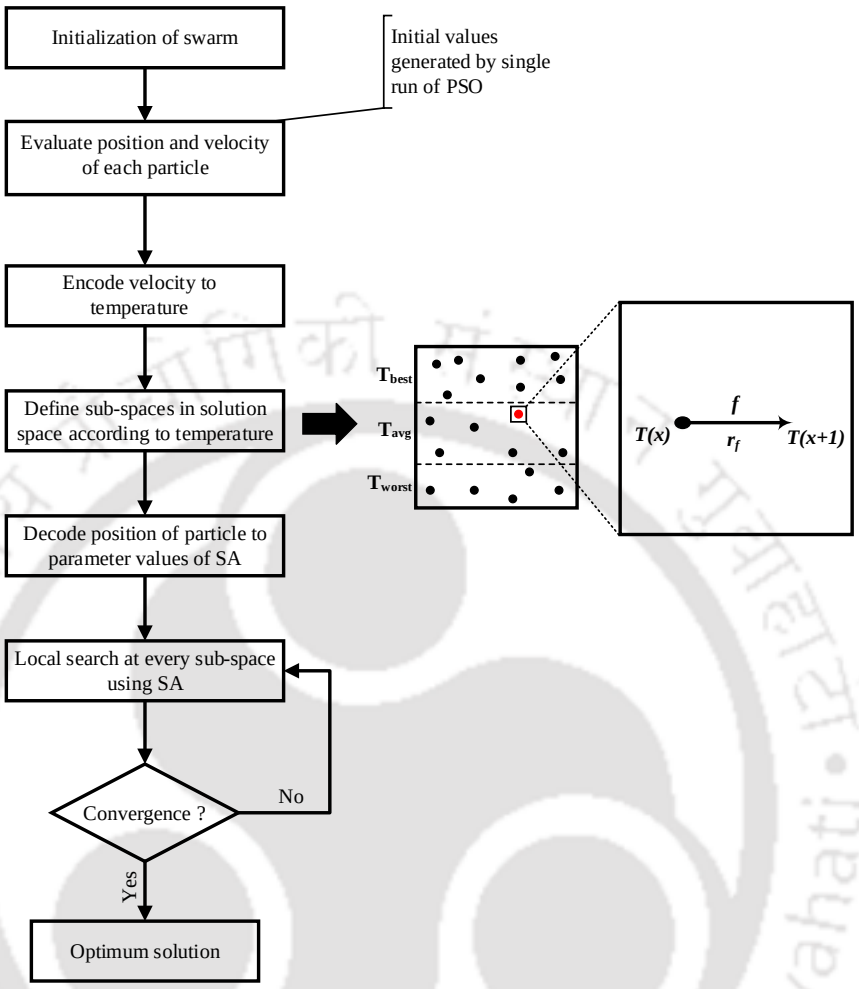


Figure 4.1: Block diagram representation of different steps in Hybrid PSO approach.

temperatures using (4.1) which is followed by the division of multidimensional search space into different sub-spaces according to initial temperatures associated with each particle.

$$T = \beta(V_{rms}^2) \tag{4.1}$$

Where, β is a constant which depends upon the crystal property ($\simeq$ metal conductivity mechanism) of particle and V_{rms} denotes the root mean square velocity of all particles of a sub-space and can be evaluated by using (4.2).

$$V_{rms} = \sqrt{(V_{x_1})^2 + (V_{x_2})^2 + ... + (V_{x_n})^2} \tag{4.2}$$

Later, the particles are allowed to move in each sub-space using the process of annealing (SA) to perform a local search for any traps and one global optimum solution is selected among the local

optimum solutions by analyzing the behavior of fitness values evaluated in each sub-space.

4.2 Hybrid Particle Swarm Optimization with Lévy Flight

Although different variants of PSO are reported in the literature, still behavior of PSO pertaining to premature convergence persists. The proposed l-HPSO approach aims to incorporate the advantages of both PSO (fast convergence rate) and SA (avoid local optima) along with the jump strategy of Lévy flight principle. Lévy flight principle is used to ensure the progressive movement of particles across the search space of PSO. l-HPSO starts by generating random particles across the search space. Each particle is allowed to move within the search space by altering its position with the random velocity. The next best position of the particle is decided in accordance with its global best position ($\vec{x}_{gbest}$) and personal best position ($\vec{x}_{pbest}$). The convergence time to achieve optimal position is improved by limiting the positions of particles within the search boundaries using Lévy flight principle. This jump strategy to shift the position of the particle can be reviewed by representing (2.3) as,

$$\vec{x}_i(t) = \vec{x}_i(t-1) + \phi \acute{L}(t) \tag{4.3}$$

$$\begin{aligned} \acute{L}(t) = \omega \vec{v}_i(t-1) + l_j Levy(\vec{x}_{pbest} - \vec{x}_i(t-1)) \\ + l_j Levy(\vec{x}_{gbest} - \vec{x}_i(t-1)) \end{aligned} \tag{4.4}$$

where $\phi \in (0,1)$ is step size; and $l_j \in \mathbb{R}, j = [1,2]$ are Lévy coefficients. l is defined as $u/v^{1/\beta}$, where u and v are the coefficients drawn from normal distribution. Here, $\acute{L}$ denotes the Lévy parameter evaluated from Lévy stable distribution.

Once optimal positions are evaluated using Lévy PSO approach, the entire search space is divided into different temperature regions based on the velocities of particles. Further, the particles in each temperature region are subjected to the annealing process to prolong the convergence rate in order for improving quality of the solution. The particles in the high-temperature region are more coherent to stiff annealing behavior than the particles in the lower temperature regions. There may be the cases where particles exist at room temperatures. In such cases, these particles are left out of the annealing

process to improve the convergence rate of l-HPSO. The objective of this course of action is to limit the number of particles getting into the process of annealing. Lévy flight is employed along with the annealing to facilitate PSO to sustain fast convergence rate in the presence of SA. Algorithm 3 differs from the implementation of HPSO (as shown in Figure 4.1) in terms of the search strategy. Since the annealing process is applied to a limited number of particles in higher temperature region the convergence of l-HPSO depends on the limitation imposed by the movement of particles using Lévy flight principle.

4.2.1 Convergence Analysis

The convergence analysis of l-HPSO is exhibited by analyzing the convergence of only Lévy PSO approach. The convergence of Lévy PSO is greatly affected by velocities of particle. The degree of randomness in theses velocities can be determined by position of a particle at different time instances and, can be represented as a linear system of equations shown below.

$$\begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} x_i(t+1) \\ x_i(t) \\ x_i(t-1) \end{bmatrix} = \begin{bmatrix} \phi \acute{L}(t) \\ \phi \acute{L}(t-1) \\ \phi \acute{L}(0) \end{bmatrix} \tag{4.5}$$

(4.5) denotes positional behavior of particles at three different time instances starting from time instant $(t-1)$. Here, $\acute{L}(0) = v_i(0)$; $\acute{L}(0) \in \mathbb{R}$ is called Lévy parameter representing initial state of the particle. It should be noted that the initial state is not considered as an equilibrium point, which is a state, achieved by the motion of particle without an external excitation. In this case, the position $x_i(t)$ at any time instant t of i^{th} particle can be represented as $x_i^{eq}(t) = l_j$; where l_j is derived from normal distribution. Further, convergence of the particle greatly depends upon the eigenvalues (λ_1, λ_2) of the coefficient matrix, which can be evaluated by solving the following equation.

$$\lambda^2 - (w - l_j + 1)\lambda + w = 0 \tag{4.6}$$

For a given particle, if the solution of (4.6) satisfies $(\lambda_1, \lambda_2) < 1$, particle is considered in the state of equilibrium. The state of equilibrium is the necessary and sufficient condition for l-HPSO to converge

Algorithm 3: Pseudocode of l-HPSO algorithm

Input : Problem size (P_{pop})
Output : Global solution (P_{gsol})

$P_{pop} \leftarrow \phi$
$P_{gbest} \leftarrow \phi$
for $i \leftarrow 1, P_{pop}$ **do**
  $P_{vel} \leftarrow \text{Levy}(\text{V}_\text{t})$
  $P_{pos} \leftarrow \text{Levy}(\text{X}_\text{t})$
  $P_{lbest} \leftarrow P_{pos}$
  if $(P_{lbest} \leq P_{gbest})$ **then**
    $P_{gbest} \leftarrow P_{lbest}$
  end if
end for
while Converge() **do**
  for $i \leftarrow 1, P_{pop}$ **do**
    $P_{vel} \leftarrow \text{UpdateLevy}(\text{V}_\text{t})$
    $P_{pos} \leftarrow \text{UpdateLevy}(\text{X}_\text{t})$
    if $(P_{pos} \leq P_{lbest})$ **then**
      $P_{lbest} \leftarrow P_{pos}$
    end if
    if $(P_{lbest} \leq P_{gbest})$ **then**
      $P_{gbest} \leftarrow P_{lbest}$
    end if
  end for
end while
$P_{temp} \leftarrow \text{Convert}(\text{P}_\text{Vel})$
$\text{Divide}(\text{P}_\text{temp})$
for $T_{pop} \leftarrow 1, P_{temp}$ **do**
  $S_{cur} \leftarrow \text{InitialSolution}(\text{T}_\text{pop})$
  $S_{best} \leftarrow S_{pop}$
  for $i \leftarrow 1, Max$ **do**
    $S_i \leftarrow \text{UpdateNeighbor}(\text{S}_\text{cur})$
    $T_{cur} \leftarrow \text{CalTemperature}(\text{i}, \text{T}_\text{pop})$
    if $(S_i \leq S_{cur})$ **then**
      $S_{cur} \leftarrow S_i$
    end if
    if $(S_i \leq S_{best})$ **then**
      $S_{best} \leftarrow S_i$
    end if
    if $\text{Exp}((S_i \leq S_{cur})/T_{cur}) > \text{Random}()$ **then**
      $S_{cur} \leftarrow S_i$
    end if
  end for
  $\text{Return}(\text{S}_\text{best})$
end for

to the global optimum solution.

4.3 Design Examples

4.3.1 Design Example 1 : Two-stage Operational Amplifier

A two-stage operational amplifier circuit [3] as shown in Figure 4.2 is taken as a benchmark to exhibit effectiveness of the proposed approach. The solutions obtained by using the proposed approach is verified with the solutions of Mentor Graphics layout tool Pyxis as shown in Figure 4.3. An average of 0.3% relative error is calculated by using (4.7) which is represented in Figure 4.4 for twenty various iterations before reaching the convergence.

$$\%\ of\ error = \frac{A_v^{hybridPSO} - A_v^{Mentor}}{A_v^{hybridPSO}} \times 100 \tag{4.7}$$

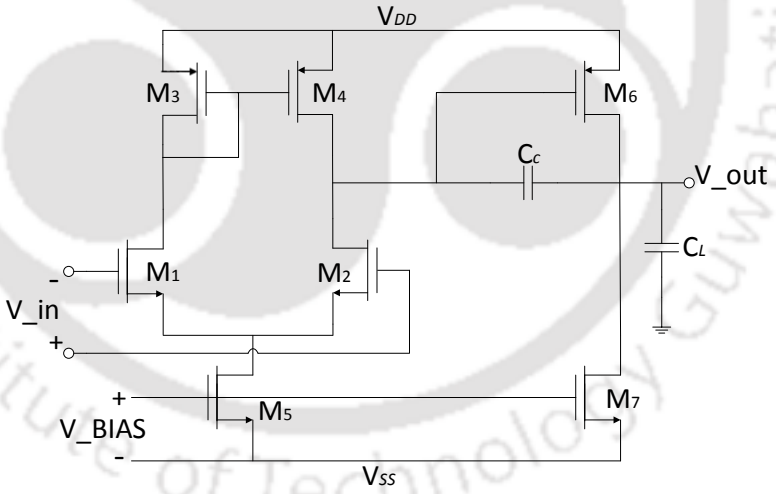


Figure 4.2: Two-stage operational amplifier circuit. [3]

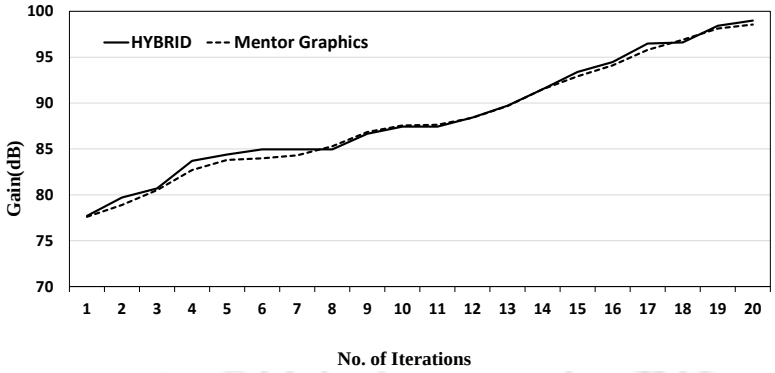


Figure 4.3: Design verification of proposed hybrid PSO approach with Mentor Graphics Pyxis tool for maximum gain of a two-stage operational amplifier circuit.

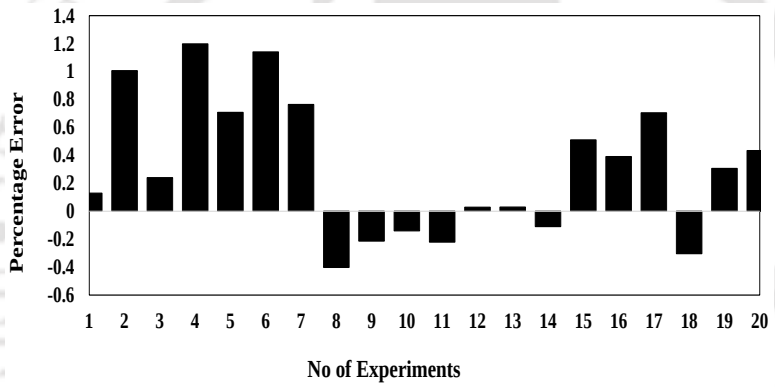


Figure 4.4: Percentage error for different experiments for the design of two-stage operational amplifier circuit.

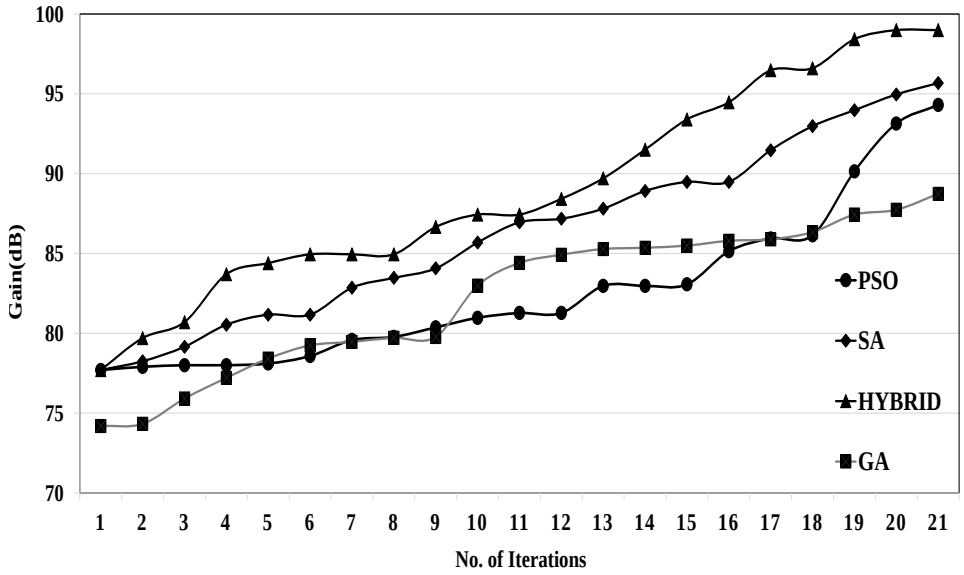


Figure 4.5: Comparison of different optimization techniques with proposed hybrid PSO approach for maximum gain of a two-stage operational amplifier circuit.

Table 4.1: Constraints and specification for two-stage operational amplifier. [3]

Constraints	Specification
Open-loop gain (A_{dc})	$Maximize$
Unity gain bandwidth (w_0)	$\geq 5\ MHz$
Slew rate (SR)	$>\ 10\ V/\mu s$
Input common-mode range ($ICMR$)	$-1\ to\ 2V$
Output voltage swing	$\pm\ 2V$
Load capacitance	$10\ pF$
Phase Margin	$\geq 60\,\text{deg}$

For designing of the two-stage operational amplifier, open-loop gain is taken as an objective function subject to constraints shown in Table 4.1. The objective function, i.e. gain A_v can be formulated as a function of transconductances ($g_{m1},\ g_{m2}, \ldots,\ g_{m7}$) and channel resistances ($r_{o1},\ r_{o2}, \ldots,\ r_{o7}$) of transistors of the two-stage operational amplifier circuit. The absolute value of voltage gain A_v [3] can be represented as,

$$|A_v| = \frac{g_{m2} \times g_{m6}}{(g_{ds2} + g_{ds4}) \times (g_{ds6} + g_{ds7})} \tag{4.8}$$

where, $g_{dsi} = 1/r_{oi}$, for $i = 2, 4, 6$ and 7.

The transconductance vector Gm ($g_{m1},\ g_{m2}$,g_{m5}) is treated as the position of particles for application of the proposed approach. Experiments are performed on the two-stage amplifier circuit to maximize gain subject to the design constraints listed in Table 4.1, using GA, PSO, SA and the proposed approach and the solutions are shown in Figure 4.5 in which it can be seen that the proposed metaheuristic performed better as compared to other methods for obtaining a quality solution. Since SA is employed in different temperature regions ($T_{best}, T_{avg}, T_{worst}$) simultaneously, the computational performance of proposed approach is not affected in a significant manner. For this design example, we have marked different temperature regions $T_{best}, T_{avg}\ and\ T_{worst}$ given in (4.9).

$$0 < T_{worst} < \frac{\delta T}{3}, \frac{\delta T}{3} < T_{avg} < \frac{2\delta T}{3}, \frac{2\delta T}{3} < T_{best} < \delta T \tag{4.9}$$

where, δT denotes $T_{max} - T_{min}$.

Table 4.2: Optimal gain obtained after execution of different heuristics for 20 experiments for the design of two-stage operational amplifier circuit and corresponding the execution time of different heuristics

Performance Parameters	SA	PSO	PSO_{hybrid}
A_v^{optmin} (dB)	83.9	85.33	88.67
A_v^{optavg} (dB)	89.87	88.84	92.99
A_v^{optmax} (dB)	96.67	94.30	99.00
t_{comp} (ms)	0.551	0.432	0.7095

In order to validate the proposed methodology twenty number of runs are performed till convergence for design of a two-stage operational amplifier circuit using PSO, SA and the proposed metaheuristic. The average solutions and computational time to perform various runs as listed in Table 4.2. It may be observed in Table 4.2 that the computational time consumed by proposed method is more as compared to SA and PSO but the solution obtained for the design of two-stage OpAmp circuit is much better as compared to SA and PSO.

4.3.2 Design Example 2 : Operational Transconductance Amplifier

Operational transconductance amplifiers (OTAs) have been used as one of the representatives of general purpose circuits due to high transconductance and voltage gain in moderate inversion region. For showing the effectiveness of the proposed approach a simple OTA circuit as shown in Figure 4.6 is taken as a design example to be operated in weak or moderate inversion region at long channel lengths. The proposed methods are employed to maximize voltage gain (A_v^{OTA}) of this OTA by transistors operating in high transconductance (g_m) and high drain-to-source (r_{ds}) regions.

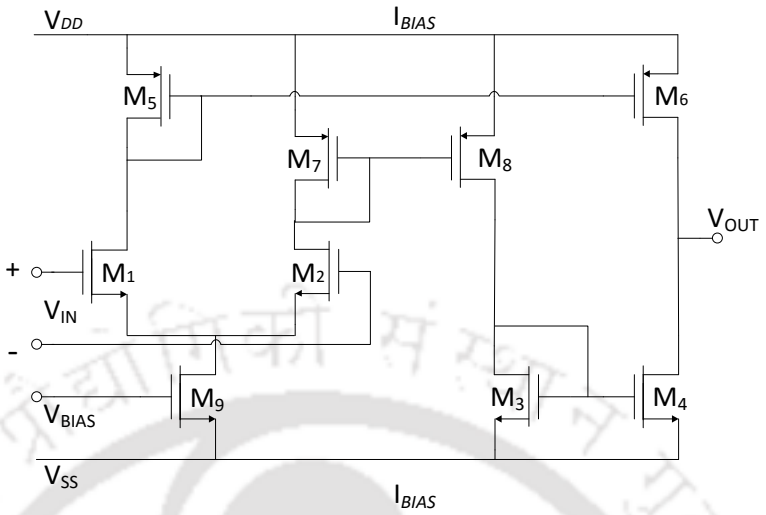


Figure 4.6: A simple operational transconductance amplifier circuit [4].

The voltage gain (A_v^{OTA}) of the OTA circuit can be approximated by (4.10) [4].

$$A_v^{OTA} = G_m^{OTA} \times R_{out}^{OTA} \tag{4.10}$$

where, G_m^{OTA} and R_{out}^{OTA} denote transconductance and output resistance of OTA respectively. It can be devised from the operation of OTA in inversion regions (weak or moderate) that A_v^{OTA} decreases with the increase in inversion coefficient regardless of the magnitude variation in OTA bias current (I_{bias}^{OTA}) and increases sub-linearly with increase in the transistor channel lengths (L_4 and L_6) [4]. Various runs are performed on OTA to maximize voltage gain subject to inversion coefficient and long channel lengths of transistors using PSO, SA and the proposed methods. Outcome of these runs is shown in Figure 4.7 which exhibits that the proposed metaheuristic is more efficient in optimizing (to achieve maximal gain in the temperature range of $500K < T < 1000K$) OTA circuit as compared to PSO and SA. This is due to the particles at high-temperature region taking more time to cool down as compared to the particles of other regions. In this way annealing process assists in search of finding out the local optimum. The proposed approach ensures to find a solution provided the design constraints and objective function chosen appropriately.

Figure 4.8 represents variation in gain of OTA with respect to change in channel lengths ($4\mu m - 14\mu m$) of transistors ($M_1 - M_4$) while performing experiments assuming inversion coefficient to be constant.

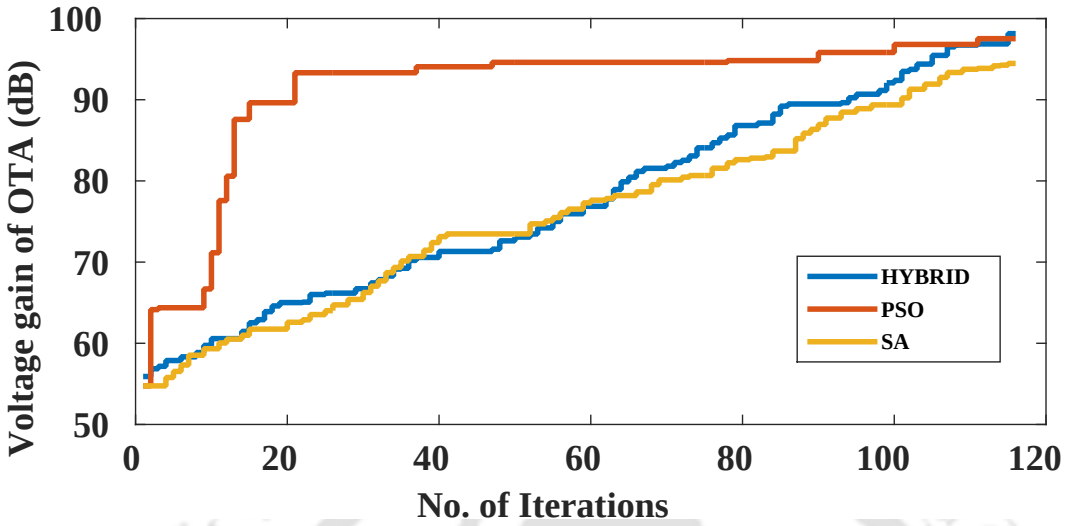


Figure 4.7: Comparison of different standard optimization techniques with hybrid PSO approach for maximum gain of a simple operational transconductance amplifier circuit.

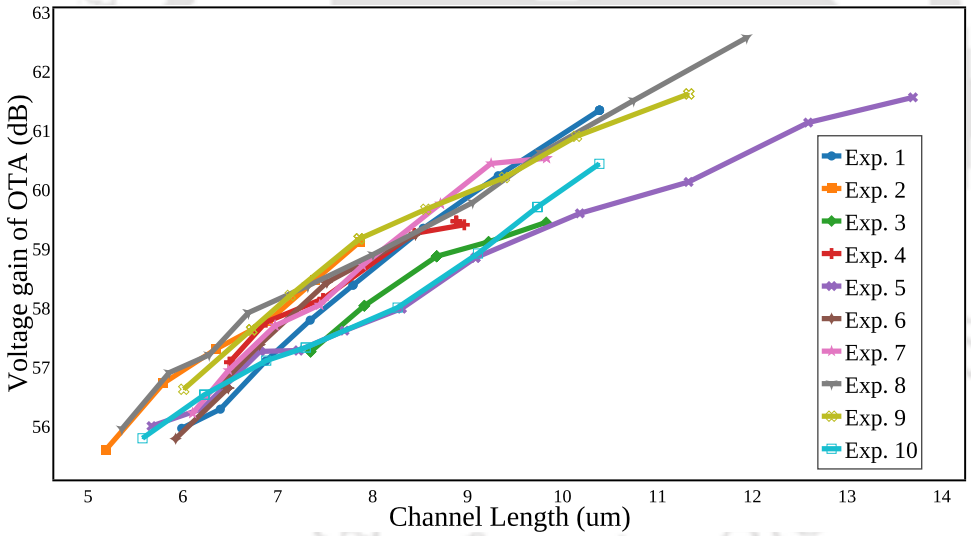
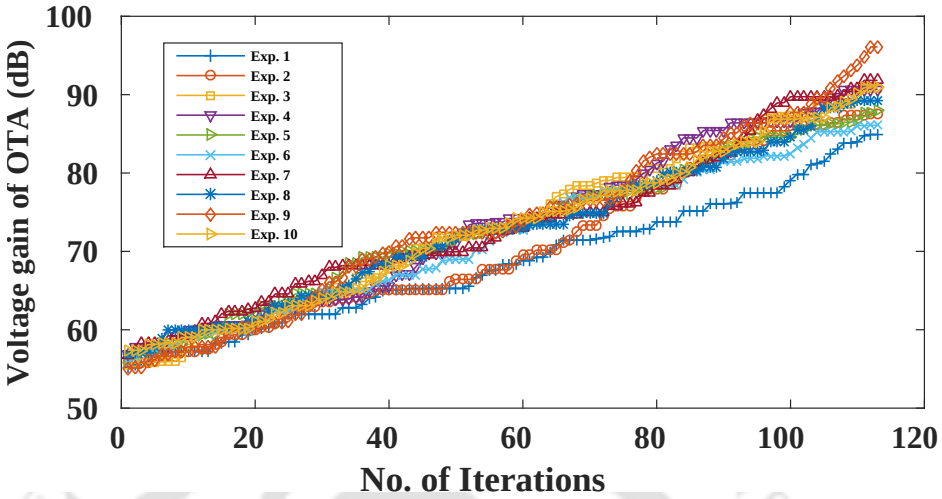
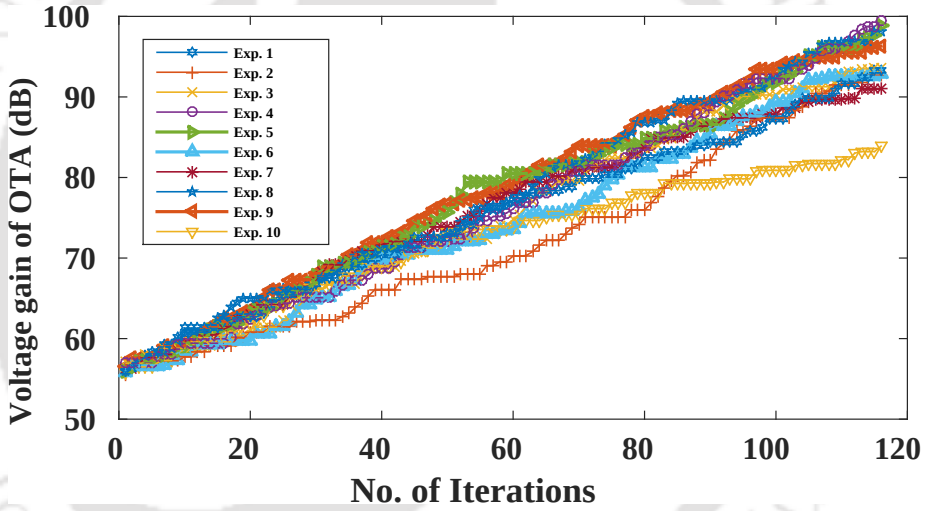


Figure 4.8: Variation of voltage gain in dB with respect to variation in long channel length using hybrid PSO approach for a simple operational transconductance amplifier circuit.

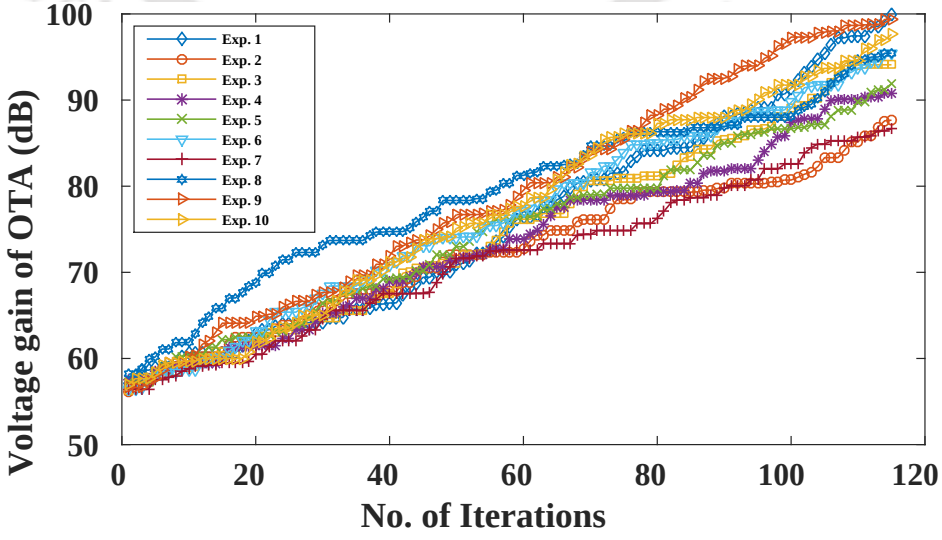
Figure 4.9 exhibits maximization of gain in three different temperature regions and it can be observed that a maximum gain of around 100dB is achieved by one of the searches done by proposed approach in the temperature region $500K < T < 1000K$. One of the reasons for this maximum gain is the impact of high temperature on the cooling strategy employed by SA approach. At high temperature, particles tend to move with a high velocity within the multidimensional search space which enables the search strategy of SA to find global solution avoiding local traps.



(a)



(b)



(c)

Figure 4.9: Optimization using proposed approach (HPSO) for maximum gain of a simple OTA circuit in three different temperature regions i.e., (a) $T < 200K$, (b) $200K < T < 500K$ and (c) $500K < T < 1000K$.

4.3.3 Design Example 3 : Low Noise Amplifier

A cascode LNA [61] is considered as a case study to demonstrate effectiveness of the proposed optimization technique. LNA consists of a common source amplifier with inductive source degeneration and a common gate load. The schematic of LNA, as shown in figure 4.10, contains two MOSFETs M_1 and M_2 and a tuning circuit (C_{out} and L_{out}) which is tuned at a center frequency of $2.4GHz$. Both inductors (L_g, L_s) are used for matching at an input end. The upper bound of NF is kept at 2.5 ($0.4dB$) with a power consumption of $8mW$. The quality factor of LNA is kept between 3 to 5.

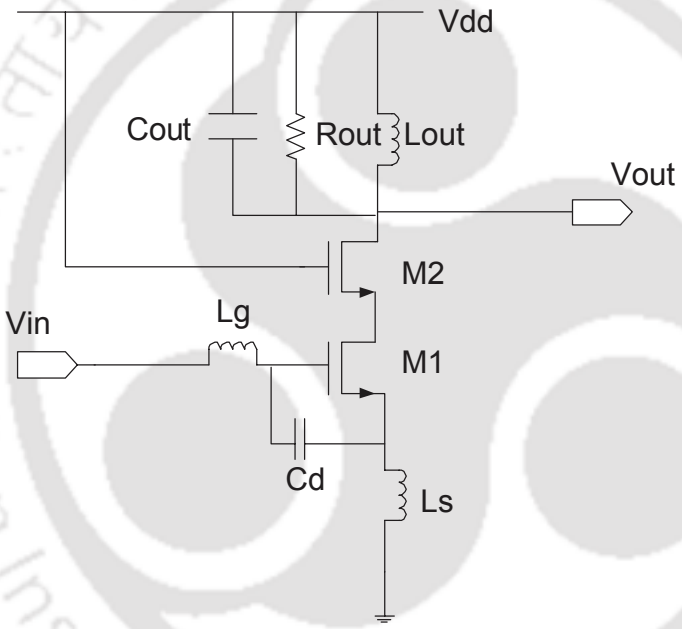


Figure 4.10: Low Noise Amplifier circuit

For optimization of LNA design, NF is taken as an objective function subject to the constraints as shown in Table 4.3. The problem formulation of LNA circuit is given in chapter 2. Here, approximated expressions of g_m and g_{do} are generated by curve-fitting [50] and can be expressed as follows,

$$\begin{aligned} g_m &= A_0 L^{A_1} W^{A_2} I_{ds}^{A_3} \\ g_{do} &= B_0 L^{B_1} W^{B_2} I_{ds}^{B_3} \end{aligned} \tag{4.11}$$

The values of constants are shown in Table 4.4.

Table 4.3: Constraints and values for LNA design

Constraints	Values
Gain (Av)	$\geq 10dB$
Length of Transistor (M1,M2 and M3)	$L = L_{featuresize}$
Input Matching	$\frac{g_m L_s}{C_{tot}} = 50\ \Omega$
Current through M1 and M2(I_{ds})	$0.1mA \leq I_{ds} \leq 4.5mA$
Width of Transistors M1 (W_{M1})	$60um \leq W_{M1} \leq 100um$
External Capacitor (C_{ext})	$0.08pF \leq C_{ext} \leq 0.15pF$

Table 4.4: Value of constants for calculating g_m and g_{do} for (4.11).

A_0	A_1	A_2	A_3
0.0463	-0.4489	0.5311	0.4689
B_0	B_1	B_2	B_3
0.0096	-0.5595	0.5194	0.4806

Design of LNA circuit is optimized for the minimum noise figure using state-of-the-art optimization techniques, such as PSO [71], SA [58], HPSO [72] and l-HPSO [73]. Several runs or experiments are carried out to demonstrate applicability of the proposed l-HPSO. Table 4.5 lists mean of the best values of NF and gain at different temperature regions. It can be observed from Table 4.5 that no particles are in the high-temperature region for both experiments 2 and 3. In these cases, SA is applied in rest of the temperature regions to search for an optimum solution. One of the probable reasons for the unavailability of particles in a particular temperature region is the clustering at specific locations across the feasible region. In such cases, the local best positions of each particle fall under specific dimensions to be accounted for a feasible solution. Another reason for the absence of particles in a particular temperature region is the distribution of temperature regions based on particle velocities. Adjacent particles place themselves in nearby regions while competing for a global best positions by following random velocities within a particular range.

Table 4.5: Best values Noise Figure and corresponding Gain in three temperature regions for different experiments

Exp.	Temperature Region 1 (K)		Temperature Region 2 (K)		Temperature Region 3 (K)	
	Gain (dB)	NF (dB)	Gain (dB)	NF (dB)	Gain (dB)	NF (dB)
1	0 - 734.59		734.59 - 1552.66		1552.66 - 2403.76	
	17.81	0.42	16.07	0.39	15.75	0.37
2	0 - 834.58		834.58 - 1669.17		1669.17 - 2503.76	
	14.98	0.39	15.32	0.37	-	-
3	0 - 1315.16		1315.16 - 2630.33		2630.33 - 3945.49	
	12.81	0.54	16.12	0.0.61	-	-
4	0 - 1037.29		1037.29 - 2074.58		2074.58 - 3111.87	
	16.55	0.59	15.71	0.56	19.57	0.73
5	0 - 1026.39		1026.39 - 2052.77		2052.77 - 3079.15	
	11.82	0.48	15.77	0.54	11.88	0.46
6	0 - 1320.31		1320.31 - 2640.63		2640.63 - 3960.95	
	11.76	0.48	12.71	0.52	13.46	0.50
7	0 - 385.44		385.44- 770.88		770.88 - 1156.32	
	14.96	0.55	13.07	0.51	15.36	0.58
8	0 - 985.20		985.20 - 1970.41		1970.41 - 2955.61	
	14.26	0.51	14.57	0.54	15.18	0.57

Figures 4.11 and 4.12 represent variations in the NF and gain, respectively, at different temperature regions for a single experiment. Since the objective is to minimize NF gain is maintained above $10dB$ and it can be seen from Figure 4.12 that at higher temperature regions the gain of LNA is higher. Figures 4.13 and 4.14 represent comparison among PSO, SA, HPSO and HPSO with l-HPSO. Further, it can be observed minimum NF is obtained by l-HPSO.

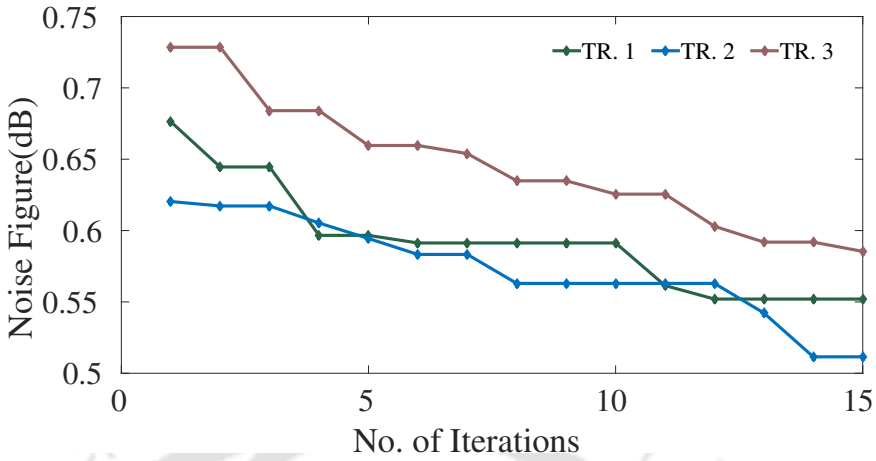


Figure 4.11: Variation of Noise Figure in a single experiment for different Temperature Regions(TR. 1, TR. 2, TR. 3)

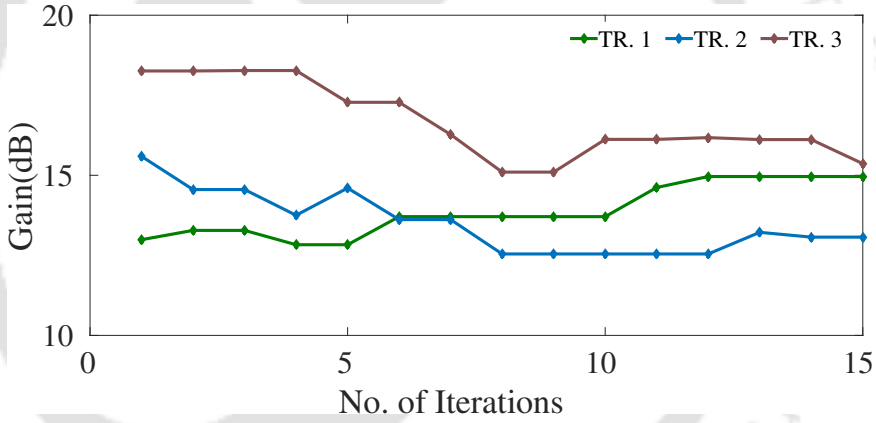


Figure 4.12: Variation of Gain in a single experiment for different Temperature Regions(TR. 1, TR. 2, TR. 3)

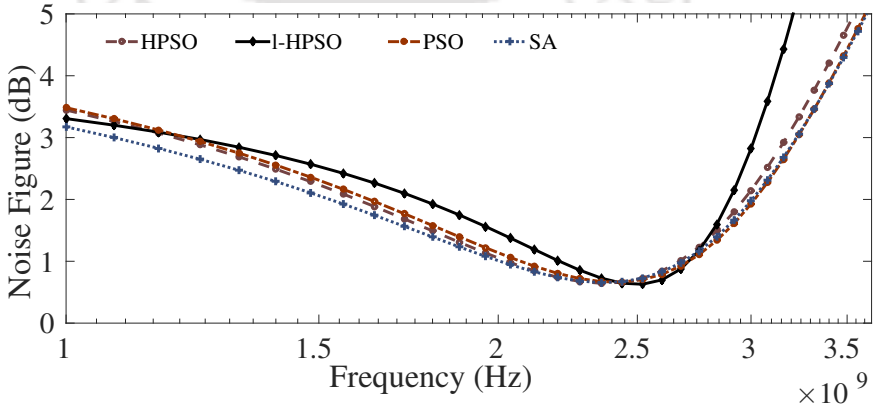


Figure 4.13: Comparison of noise figure for different techniques

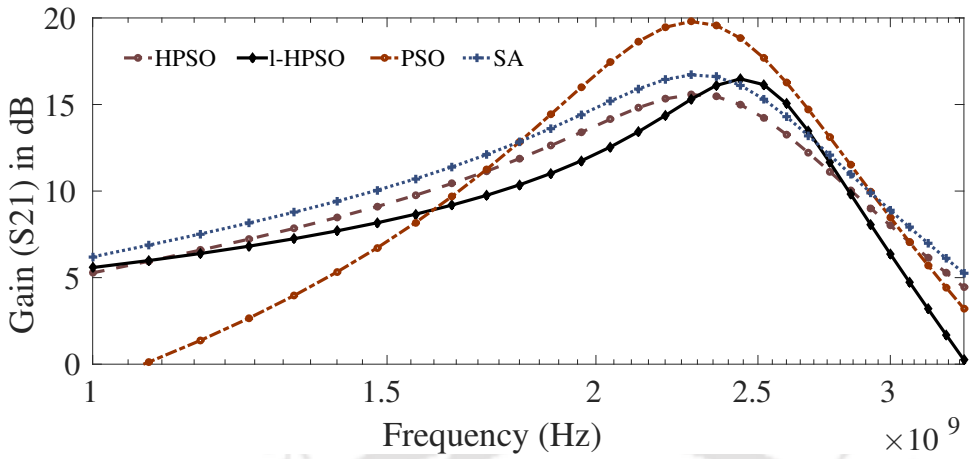


Figure 4.14: Comparison of gain for different techniques

4.4 Results

The comparison of performance of the proposed techniques with peer algorithms is tabulated in this section. Table 4.6 represents optimized cost function (Gain for amplifiers and NF in case of LNA) of analog/RF circuits. The peer algorithms includes swarm algorithms (SPSO [74], CRPSO [75, 76], LPSO [77, 78], ALCPSO [79]), differential evaluation (SADE [80]) and, genetic algorithm (gGA [81]). In Table 4.6, gain and noise figure are presented with the number of function evaluations. The smaller number of function evaluation indicates faster convergence of a particular algorithm. Therefore the smaller number of function evaluation and better value of cost function (larger gain or smaller NF) denote the superior performance.

The proposed algorithms are tested on standard benchmark functions[1] i.e., Rosenbrock-1, Rosenbrock-2, Mishra, Simionescu, g11, g12 and, g13. The comparison of proposed techniques and peer algorithms using standard benchmark functions are tabulated in Table 4.7. The proposed techniques, HPSO, and l-HPSO have performed better when compared to peer algorithms while analyzing circuit as well as benchmarks.

[1]These are standard single objective optimization test functions used in literature. They are also available at https://en.wikipedia.org/wiki/Test_functions_for_optimization and at http://www-optima.amp.i.kyoto-u.ac.jp/member/student/hedar/Hedar_files/TestGO_files/Page422.htm

Table 4.6: Comparison of Proposed HPSO and l-HPSO with different algorithms (Values shown are in format of cost of objective function (function evaluation))

Algorithms	Two-stage opamp	Folded cascode opamp	LNA
	Gain(dB)	Gain(dB)	NF(dB)
gGA	67.02(1200)	73(1000)	0.27(1220)
SADE	68(890)	73.01(800)	0.43(1150)
SPSO	68.96(1022)	73(1010)	0.35(1200)
CRPSO	68.99(1020)	73.56(1000)	0.38(1200)
LPSO	69.85(800)	72.85(750)	0.72(800)
ALCPSO	42.06(300)	75.04(220)	0.62(210)
HPSO	73.12(230)	**75.66(220)**	0.62(210)
l-HPSO	**75.12(220)**	75.03(220)	**0.67(200)**

Table 4.7: Comparison of Proposed HPSO and l-HPSO with different algorithms (Values shown are in format of cost of objective function (function evaluation))

Algorithms	Rosenbrock-1	Rosenbrock-2	Mishra	Simionescu	g11	g12	g13
gGA	–	5.94E-15(2.50E+06)	–	–	–	–	–
SADE	–	2.24E-20(2.48E+04)	-106.788(3.00E+04)	–	7.28E-01(1660)	0.99(3330)	5.06E-02(8520)
SPSO	–	3.59E-19(3.50E+02)	-106.788(150)	–	2.18E-12(400)	0.99(630)	5.06E-02(1800)
CRPSO	9.30E-05(9.00E+02)	5.94E-17(2.8E+02)	-106.788(150)	-0.15(1000)	2.80E-11(400)	0.99(602)	5.06E-02(1000)
LPSO	–	6.05E-18(2.50E+02)	-106.788(150)	-0.15(990)	1.78E-11(400)	0.99(620)	7.06E-02(1000)
ALCPSO	0(300)	0(220)	-106.788(100)	-0.15(500)	0(450)	1(500)	5.89E-02(900)
HPSO	1.60E-06(2.10E+02)	2.88E-17(2.20E+02)	**-106.788(110)**	-0.078(520)	0.74(500)	1(500)	**5.06E-02(900)**
l-HPSO	**1.12E-08(2.10E+02)**	**1.37E-18(2.20E+02)**	**-106.78(110)**	**-0.078(505)**	**0.74(400)**	**1(420)**	**5.06E-02(900)**

4.5 Summary

In this chapter, method of analog circuit optimization using hybrid of PSO and SA is presented. The effectiveness of the proposed method is demonstrated by verifying solution of a two-stage cascode amplifier circuit with the solutions of Mentor Graphics Pyxis (Eldo) tool. It is found that the solution of the proposed metaheuristic matches with the solutions provided by Mentor Graphics Pyxis tool with an average of 0.3% error. An extended version of HPSO (l-HPSO) is also presented with the improved search method (Lévy flight) and then applied to optimize a low noise amplifier circuit

designed for 2.4 GHz. In this design example, noise figure is minimized subjected to the constraints as input matching, bandwidth, biasing, etc. The results of HPSO and l-HPSO for Two-stage OpAmp, Folded cascode amplifier and LNA are compared with the standard algorithms. The proposed methods are also tested using standard benchmarks and the performance is compared with the peer algorithms.

5

Multi-objective Optimization of Analog Circuits using Metaheuristics

Contents

In this chapter multiobjective optimization techniques are applied for the analog circuit optimization. The proposed method provides a set of optimized solution subject to performance trade-off. In section 5.1 proposed approach is described. Section 5.2 presents the experimental setup for simulation including quality indicators, test functions and, peer algorithms, which are used to verify the proposed techniques. In section 5.3 analog circuit design examples are analyzed with the proposed method. The results of standard test functions are presented in section 5.4 and chapter is summarized in section 5.5.

5.1 Proposed Multi-objective Hybrid Particle Swarm Optimization (MHPSO)

Although PSO is one of the most popular algorithms for finding optimal regions of complex search spaces through the interaction of particles in a population, its search ability and convergence rate are not efficient [82]. Therefore, we propose to improve the performance of PSO by combining search strategy with SA to develop a hybrid framework for reducing manual efforts in the circuit design flow. In this chapter, we present a voltage-temperature mapping scheme to initiate the search of SA on nondominated solutions which are evaluated by using PSO.

Let the position of the particle at i^{th} generation is x^i_{pos} and it is allowed to move in a search space of dimension N. The first step is to initialize positions $\mathbf{X_{pos}}$ and velocities $\mathbf{V_x}$ of particles. Both local and global best positions of particles are assigned to their initial positions to start the optimization process. As each particle moves inside the search space, its velocity and position are updated. Consequently, the local best positions are updated and incorporated into the framework for evaluating next position and velocity. Later, particles having the best global positions are chosen as nondominated particles, and are stored in an external repository A. Once PSO is completed, annealing process is applied to the dominated particles after velocity-temperature mapping. The entire archive A is divided into sub-spaces having different temperature coefficients (T_1, T_2, T_3, etc.). Further, the annealing process is carried out in each subspace to improve the diversity of the solutions. Entire process flow of the framework is shown in Figure 5.1. Essential implementation steps of the framework are discussed as follows.

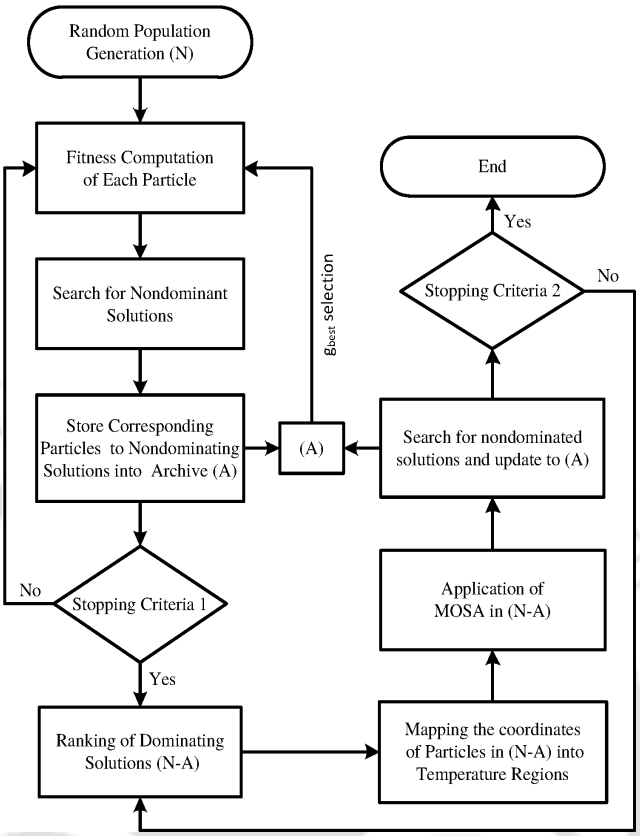


Figure 5.1: Proposed Framework

5.1.1 Initialization and Classification of Population

A population of N particles is randomly generated inside the multidimensional design space. The position of each particle, x^i_{pos}, is assigned with random values and the velocity of each particle, V^i_x, is initialized with zero. An external archive A is maintained to store nondominated particles and corresponding solutions. The selection procedure of identifying nondominated fronts is performed using normal dominance principle [83] till the size of $A \geq N$. If $|A| > N$, no further swarm operation is performed and annealing process is initiated.

5.1.2 Particle Movement and Finding Global-best

Once the positions of particles are initialized, each particle follows a series of trajectory inside the design space. The path of this trajectory is governed by a local search principle as described in Section 2.3.2. In this method, the stochastically weighted difference between the neighboring particle's local best position and individual's current position, $x^i_{lbest} - x^i_{pos}$, and difference between the best position

and individual's current position, $x_{gbest} - x^i_{pos}$, are added to individual's current velocity v^i_x to adjust the next time step. The global best position, x_{gbest}, is evaluated according to the new position obtained by particles in the design space and the expression for finding x_{gbest}, can be described by rewriting (2.3) as follows [82],

$$x_{gbest} \leftarrow \frac{c_1 r_1 (x^i_{lbest} - x^i_{pos}) + c_2 r_2 (x_{gbest} - x^i_{pos})}{c_1 r_1 + c_2 r_2}, \tag{5.1}$$

where, the value of x_{gbest} is regularly updated as the system moves towards an optimum solution. The procedure is presented in Algorithm 4. As there is a random weighting of the control parameters in (5.1), particles follow Brownian motion, preventing an explosion of design space, and supporting possible convergence to local optima in most of the cases.

Algorithm 4: Finding Nondominated Solutions using Swarm Search

Input: P_{pop}, MAX_GEN in
Output: P_{opt} out

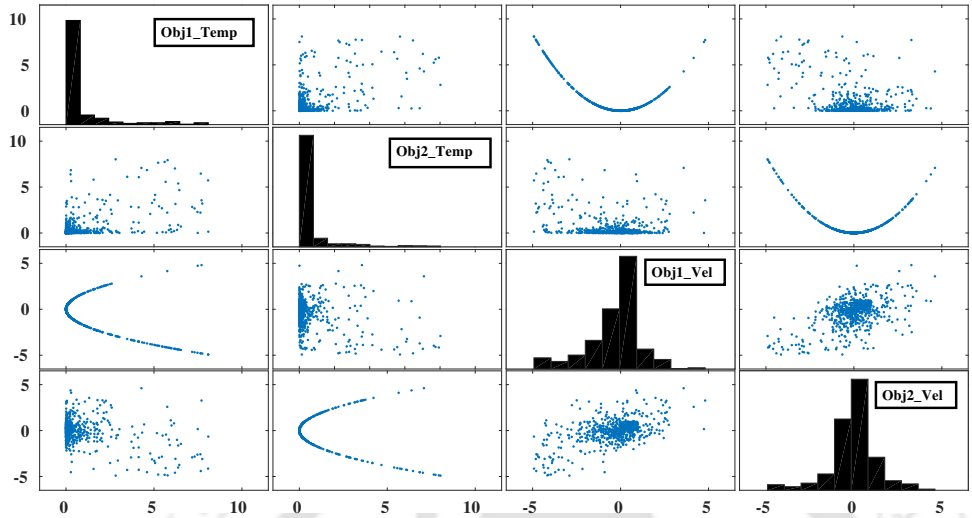
1: Generate random population P_{pop}
2: **for** $i \rightarrow 1$ to P_{size} **do**
3: Initialize $V_x[i]$
4: Initialize $X_{pos}[i]$
5: **end for**
6: Evaluate fitness P_x for each particle in P_{pop}
7: Store nondominated solutions to archive $A_{fitness}$
8: Initialize P_{gbest} and X_{gbest}
9: **for** $i \rightarrow 1$ to P_{size} **do**
10: $X_{lbest}[i] \rightarrow X_{pos}[i]$
11: **end for**
12: **for** $i \rightarrow 1$ to MAX_GEN **do**
13: **for** $i \rightarrow 1$ to P_{size} **do**
14: $V_x[i] \leftarrow w \times V_x[i] + C_1 \times (X_{lbest}[i] - X_{pos}[i]) + C_2 \times (X_{gbest} - X_{pos}[i])$
15: $X_{pos}[i] \leftarrow X_{pos}[i] + V_x[i]$
16: Check for out of bound solutions
17: Update $A_{fitness}$
18: Check and update local best particle $X_{lbest}[i]$
19: **end for**
20: Check and update global best particle X_{gbest} and solution P_{gbest}
21: **end for** ▷ *End of swarm search*

5.1.3 Ranking and Voltage-Temperature (V-T) Mapping Scheme

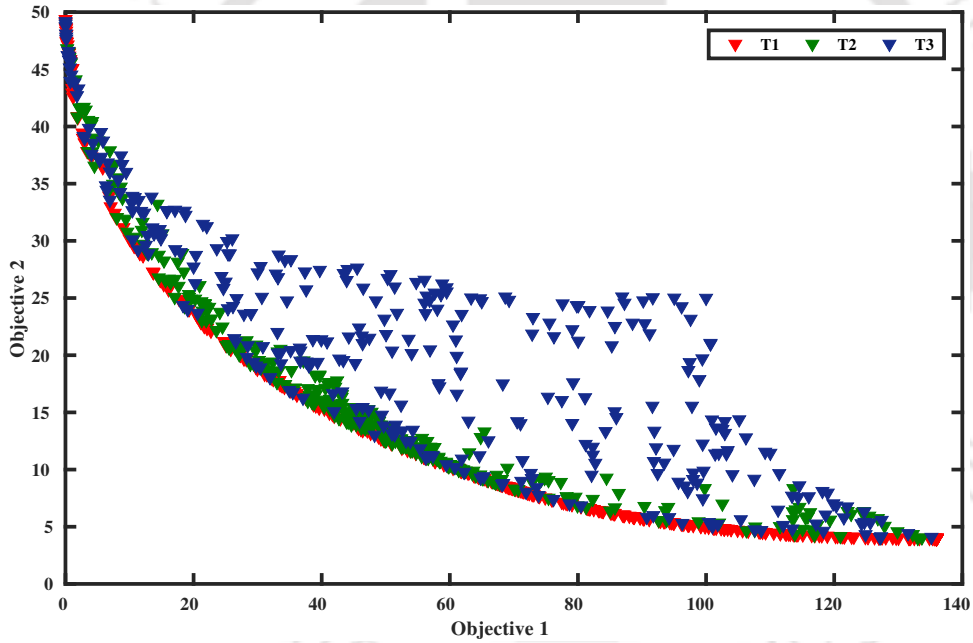
MHPSO uses an external archive A to store nondominated solutions obtained after swarm search operation. After the nondominated solutions (δ) are stored in A, rest of the solutions ($N-\delta$) are ranked according to the distance, evaluated by either Euclidean distance [84] or crowding distance [85] from nearest reference points in A, instead of discarding them. The results of both the methods are presented in following section in this chapter. In order to improve diversity, nondominated solutions in A are chosen as reference points for corresponding nearest dominated solutions. Once the ranking of dominated solutions is accomplished, corresponding particle is assigned a thermodynamic temperature depending upon the kinetic motion of that particle in three-dimensional search space. We analyze relationship between kinetic energy and velocity, i.e., $E_k = 1/2mv^2$, by analyzing the behavior of each particle whose velocity is modified in each step and also relate translational kinetic energy (E_k) to kinetic temperature (T_k) by,

$$E_k = \frac{3}{2} k_B T_k, \tag{5.2}$$

where, $k_B = 1.38065e$-23 J/K denotes the Boltzmann constant. At any instant, the proportion of particles moving at a calculated velocity within the search space can be evaluated by Maxwell-Boltzmann distribution. The Maxwell-Boltzmann distribution of particle velocities (for Binh2 function) with respect to corresponding temperature values for different objective functions are plotted as shown in Figure 5.2(a). It can be observed from Figure 5.2(b) that the particles having higher velocity (the normalized values ranging from 2 to 5 is evaluated from Figure 5.2(a)) comply with higher thermodynamic temperature. Once the particles corresponding to $N - \delta$ solutions are scaled according to the temperature, the solutions are identified according to their assigned ranks. The entire search space $S_{N-\delta}$ is divided into subspaces, s_t, where $t = 1, 2, 3, \ldots, M$. The cost functions having equal ranks are placed in the same subspace. The dominant solutions are considered in each step of the annealing process. However, diverged solutions that are far from the Pareto front are not critical. In the proposed method, we have analyzed up to three subspaces by keeping division of the ranks into three parts (i.e., $t = 1, 2$ and 3) and the solutions with higher ranks have been discarded.



(a)



(b)

Figure 5.2: (a) Maxwell Distribution of particles at any instant, relating temperature with velocity, and (b) representation of particles in objective space of Binh2 test function for different temperature regions, i.e., $T1 < T2 < T3$

5.1.4 Annealing Process

Further, the solutions in s_t are subjected to multi-objective annealing process to search any remaining nondominant solutions and obtaining a diverse Pareto front. The annealing process is described using pseudocode in Algorithm 5. It can be observed from Algorithm 5 that the annealing process

Algorithm 5: Annealing Process

Input: P_{pop}, MAX_GEN in
Output: S_{sa} out

Map particles to different temperature regions (T_1, T_2, T_3, etc.) in the solution space **S**
for $i \rightarrow 1$ to T_{num} **do**
  Initialize current solution P_x
  $step \leftarrow 0$
  while $true$ **do**
    $temp \leftarrow T_i \times e^{-step \times decayRate}$
    if $temp < minTemp$ **then**
      break
    end if
    for $j \rightarrow 1$ to n **do**
    $prob \leftarrow 1/\left(1 + e^{-\frac{\triangle X^i_{pos}}{temp}}\right)$
      if $rand() < prob$ **then**
        $X_{cur}[i] \leftarrow X_{pos}[i] + \triangle X^i_{pos}$
        if $X_{cur}[i] < X_{pos}[i]$ **then**
          $X_{pos}[i] \leftarrow X_{cur}[i]$
        end if
      end if
    end for
    Check and update current solution P_x
    $step \leftarrow step + 1$
  end while
end for

operates on probability evaluation, $prob = 1/\left(1 + e^{-(\triangle X^i_{pos}/temp)}\right)$, driven by cooling down of temperature in each step. Although annealing process becomes slower as it progresses, it firmly avoids the selection of any localized solutions and accounts for global optimum solutions. Since annealing process is applied to dominated solutions after swarm search, the proposed MHPSO procedure maintains a diversity in the space S_N at each generation. This enables the framework to solve problems having cost functions with different scales.

5.1.5 Niche Preservation

While constructing subspaces and performing annealing process in each subspace, it is worth noting that multiple particles (x_{count}) may have the same temperature values associated with them or no particles have the same temperature (t). As the particles with high-temperatures (t_{max}) require a

prolonged annealing process, it is necessary to have a niche count, ρ_j for the j^{th} subspace. The niche-preservation operation starts by identifying particle with the high-temperature ratings (minimum ρ_j) in any subspace s_j. The niching process is presented in Algorithm 6.

Algorithm 6: Niching Procedure

Input: ρ_j, s_j, $j \in S$ in
Output: $A_{N-\delta}$ out

for $i \rightarrow 1$ to β **do**
  for $j \rightarrow 1$ to s_j **do**
    Find t^j_{max} for each s_j
    Find x^j_{count} in each s_j
  end for
  for $j \rightarrow 1$ to s_j **do**
    while $x^j_{count} \neq \phi$ **do**
      choose x^j_s
      if $\rho_j \neq \phi$ **then**
        $A_{N-\delta} \rightarrow A_{N-\delta} \cup S_{sa}$
        $\rho_j \rightarrow \rho_j + 1$
        $x^j_{count} \rightarrow x^j_{count} - 1$
      end if
    end while
  end for
end for

In case of multiple particles having same high-temperatures, the particle (x^j_s) having the shortest Euclidean distance from the nearest nondominated particle is preferred. The annealing process in subspace s_j is carried out till the temperature associated with the chosen particle is cooled down to minimum temperature followed by incrementing niche count ρ_j by one. The subspace with the highest ρ count is subjected to annealing process to update the archive A. Only a few particles are subjected to annealing process in the subspace having a low ρ count, i.e., the particles having very low-temperature values are discarded. This procedure is repeated for β times after all niche counts are updated to fill the vacant spots in archive $A_{N-\delta}$.

5.1.6 Computational Complexity

The swarm search in Algorithm 4 of a population of size P_{size} having M-dimensional cost functions performed for a maximum generation of G requires $O(P_{size}MG)$ computations [86]. Ranking of dominated solutions in the statement 1 of Algorithm 5 requires Euclidean distance or crowding

distance evaluation on a number of population of size $P_{N-\delta}$. It requires $O(M(P_{N-\delta})log(P_{N-\delta}))$ and $O(M(N-\delta))$ computations to employ crowding distance and Euclidean distance in the ranking process [85]. Assigning particles to different subspaces (line 2 in Algorithm 5) according to the temperature values requires $O(M(N-\delta))$ computations. The annealing process starting from statement 3 – 20 in Algorithm 5 requires $O(tM(P_{s_t})G)$ computations for t number of subspaces (s_t) with a maximum generation of G. Assuming $\theta_j = |x^j_{count}|$ for subspace s_j, statement 7 requires $O(\theta_j)$ comparison. Considering a maximum of s subspaces and β generations, the worst case niching procedure requires $O(s\beta\theta^2)$, assuming maximum θ niching count for each subspace niche count evaluations.

5.2 Setup for Experiments

(i) **Peer Algorithms**: The performances of proposed MHPSO/MHPSO-CD are validated by choosing eight state-of-the-art multi-objective optimization algorithms NSGA-II [85], NSGA-II-DE [87], MOEA/D-DE [88], PESA-II [89], SPEA-II [90], DMOPSO [91], OMOPSO [92], and SMPSO [93] as peer algorithms. The implementations of these algorithms as provided in the respective references are considered to obtain solutions of the test functions. Algorithms such as MOEA/D-DE, SPEA-II and NSGA-II-DE are originally not developed to solve optimization problems subject to a set of constraints. In the proposed work, constraints handling mechanism proposed in NSGA-II is employed with MOEA/D-DE, SPEA-II and NSGA-II-DE to solve constrained optimization problems. A population size of 100 is considered to be evolved over 200 generations for NSGA-II, NSGA-II-DE, MOEA/D-DE, PESA-II, and SPEA-II and, 2000 function evaluations (generations) and the population size of 100 are considered for DMOPSO, OMOPSO, SMPSO, MHPSO and MHPSO-CD during the experiments. Further, Pareto fronts generated by the proposed MHPSO and MHPSO-CD are compared with these peer algorithms.

(ii) **Test Examples**: In order to evaluate the proposed MHPSO/MHPSO-CD for the application of analog circuit optimization, three analog circuits (i.e., two-stage operational amplifier, folded cascode operational amplifier, and low noise amplifier) are designed using 180 nm CMOS process technology. Further, various standard test functions ZDT*i* [94], SCH [95], FON [96],

KUR [97], BINH2 [98], CEX [85], OZY [99], and TNK [100] considered for the evaluation of proposed approaches. Here, ZDT*i* (*i* = 1, 2, 3, 4, 6), SCH , FON and KUR are unconstrained optimization problems whereas, BINH2, CEX, OZY and TNK are constrained optimization problems.

(iii) **Quality Indicators**: Multi-objective optimization algorithms are quantitatively analyzed by considering two factors. First is about finding closeness of the obtained solutions with the Pareto front and second is about finding diverse solutions with respect to the Pareto front. Therefore, in order to compare multi-objective evolutionary algorithms (MOEA), at least two performance metrics (one evaluating the closeness of the desired Pareto front, i.e., $\mathcal{P}^{\star}$, and the other evaluating the spread of Pareto front obtained) need to be used. Various performance metrics have been reported [94] in this regard for MOEAs.

The metric GD [101] is used to evaluate closeness with the Pareto-optimal front whereas, IGD [102] and hypervolume [94] provide combined quantitative information about closeness and diversity in the obtained Pareto-fronts. Quality indicators considered in the proposed work are as follows:

(a) Generational Distance (GD): GD calculates distance between the obtained Pareto front and the true Pareto front, and it can be expressed as,

$$GD = \frac{\sqrt{\sum_{i=1}^{n_{obtained}} (d_i)^2}}{n_{obtained}}, \tag{5.3}$$

where, $n_{obtained}$ is the number of solutions in obtained Pareto front, and d_i represents Euclidean distance between i^{th} obtained solution and the closest point of the true Pareto front. It should be noted that the Euclidean distance is calculated in objective space.

(b) Inverse Generational Distance (IGD): IGD can be expressed as,

$$IGD = \frac{\sqrt{\sum_{i=1}^{n_{true}} (d_i')^2}}{n_{true}}, \tag{5.4}$$

where, n_{true} is the number of solutions on true Pareto front, and d_i' represents Euclidean distance between the i^{th} solutions on the true Pareto front and the nearest solution on the

obtained front.

(c) Hypervolume: This metric is used for quantifying the convergence and diversity of MOEAs. The purpose is to calculate either area or volume of the objective space, which is covered by the obtained Pareto optimal solutions. Assuming an individual x_i in $\mathcal{P}^{\star}_{obtained}$ for a two-dimensional multi-objective optimization problem (MOO) defines a rectangular area, $a(x_i)$, bounded by an origin and $f(x_i)$. The union of such rectangular areas is referred as Hyperarea (hypervolume in the case of 3-D Pareto fronts), and in general it is called hypervolume of $\mathcal{P}^{\star}_{obtained}$,

$$HF(\mathcal{P}^{\star}_{obtained}) = \left\{ \bigcup_{i}^{n} a(x_i) | \forall x_i \in \mathcal{P}^{\star}_{obtained} \right\} \tag{5.5}$$

In [101], Hyperarea Ratio metric is expressed as:

$$HR = \frac{HF(\mathcal{P}^{\star}_{obtained})}{HF(\mathcal{P}^{\star}_{true})} \tag{5.6}$$

where, $HF(\mathcal{P}^{\star}_{true})$ is hyperarea or hypervolume covered by true Pareto front of the function. Hypervolume metric provides a qualitative measure of convergence as well as diversity. Nevertheless, it can be used along with GD or IGD metrics to get a better overview of the performance of an algorithm.

(iv) **Simulation Setup**: The parameters of peer and proposed algorithms are listed in Table 5.1, where, N, N_s, and A denote the population size, swarm size, and archive size, respectively. Maximum number of iteration is I and maximum number of evaluations is denoted by E. Mutation and crossover probabilities are represented by p_m and p_c, respectively. η_m is the distribution index of mutation and η_c is distribution index of crossover. Polynomial mutation and SBX crossover operators are used in the algorithms except for MOEAD/D-DE, where differential evaluation crossover operator is used. Binary Tournament selection strategy is used in NSGA-II, NSGA-II-DE, and SPEA-II. c_1, c_2, w, v_1, and v_2 are the parameters used to update velocity in DMOPSO, OMOPSO, SMPSO, and the proposed MHPSO.

Table 5.1: Simulation settings

Algorithm	Parameter settings
NSGA-II NSGA-II-DE	N = 300, E = 100000 $p_c = 0.9, p_m = 1.0, \eta_c = \eta_m = 20.0$
MOEA/D-DE	N = 300, E = 150000, CR = 1.0, F= 0.5, $p_m = 1.0, \eta_m = 20.0$
PESA-II	N = 10, A = 100, Bisection = 5, E = 10000, $p_c = 0.9, p_m = 1.0, \eta_c = \eta_m = 20.0$
SPEA-II	N = 100, A = 100, E = 10000, $p_c = 0.9, p_m = 1.0, \eta_c = \eta_m = 20.0$
DMOPSO	N_s = 1000, Max. age = 2, I = 25000, $c_1, c_2, w \in$ [0,1], v_1, v_2=-1.0
OMOPSO	N_s = 1000, A = 100, I = 250, η_p = 0.5 $p_m = 1.0, \eta_m = 20.0, c_1, c_2, w \in$ [0,1]
SMPSO	N_s = 100, A = 100, I = 250, p_m = 1.0, η_m = 20.0, $c_1, c_2, w \in$ [0,1], v_1, v_2=-1.0
MHPSO MHPSO-CD	N_s = 1000, A = 100, I = 250, α = 0.9 min. Temp. = 0.0001, $c_1, c_2, w \in$ [0,1]

5.3 Optimization of Analog Circuit Design

The proposed MHPSO method is applied for three analog circuit optimization problems. These test problems consist of multiple design variables, nonlinear constraints and objective functions confining a large search space. These circuits are represented in the form of multi-objective optimization problems as described in (4.11). Performance goals such as gain, power consumption, and noise figure are considered as objective functions, whereas, biasing conditions and circuit parameters (i.e., SR, GBW, etc.) are considered as constraints. The description of test circuits and generated Pareto fronts are presented as follows.

5.3.1 Two-stage OpAmp

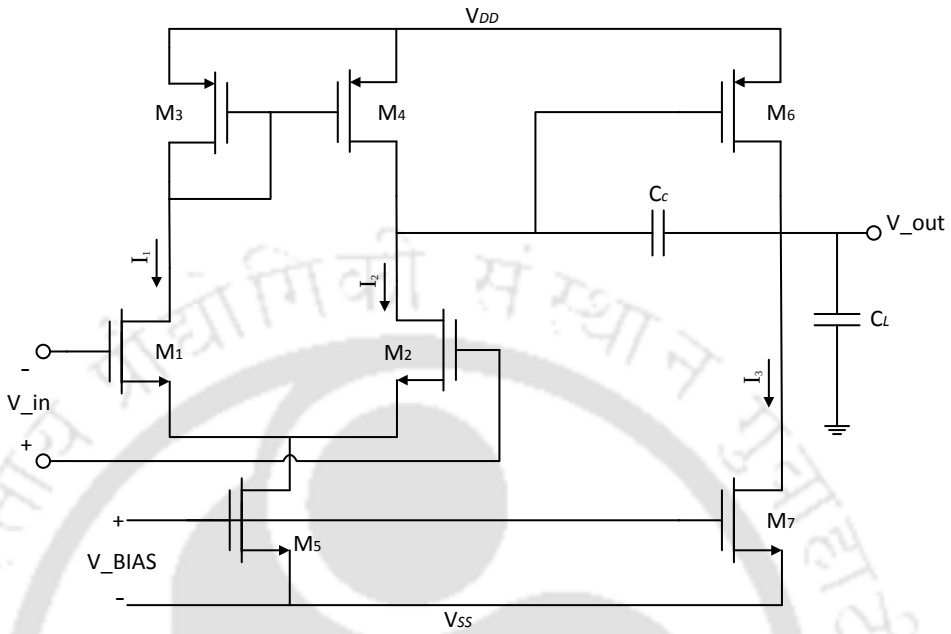


Figure 5.3: Operational Amplifier circuit

Operational amplifier is one of the fundamental elements in analog system design and frequently used as a test circuit for analog circuit design optimization. A two-stage OpAmp [3] is shown in Figure5.3 with the load capacitance C_L of 10 pF. As we know for the stable operation of the amplifier, relation between Miller capacitance (C_c) and load capacitance ($C_c > 2.2(g_{m2}/g_{m6})C_L$) need to be maintained. The circuit is designed using 0.18 μm CMOS process technology, and fixed power supply of 1.8V is used employed. W and L for all the transistors are kept within [0.24, 1000 μm] and [0.18, 10 μm], respectively. The variation of bias current in this circuit is kept between 1 μA – 2.5 mA. The appropriate differential operation and current biasing are ensured by the matching relations (e.g., M1≡M2, M3≡M4, and M5≡M7) between transistors. The analytical form of performance specifications [3] are expressed in (5.7). The design problem is formulated as a multi-objective optimization problem using the constraints shown in Table 5.2.

$$\begin{aligned} A_v &= \frac{g_{m1}g_{m6}}{(g_{ds2}+g_{ds4})(g_{ds6}+g_{ds7})} \\ P_{DC} &= v_{dd}(I_1+I_2+I_3) \\ GBW &= \frac{g_{m1}}{2\pi C_c} \end{aligned} \tag{5.7}$$

Table 5.2: OpAmp: constraints and specifications

Specifications	Description	Constraints
ϕ [degree]	Phase margin	≥ 60
P_{min} [μW]	Min. power consumption	≤ 300
SR [A/μF]	Slew rate	≥ 20
$ICMR$ [V]	Input common mode range	$[0.8, 1.6]$
GBW [MHz]	Gain bandwidth product	≥ 30
Y [mV]	$V_{in}^{min} - V_{ss} - \sqrt{\frac{I_5}{\beta}} - V_{T1}^{max}$	≥ 100

A population size of 100 particles is evolved over 200 generations in the course of optimization process. The Pareto fronts are generated to analyze tradeoff between gain and power consumption. Further, comparison between Pareto fronts, generated by proposed algorithms (MHPSO and MHPSO-CD) and other evolutionary algorithms are shown in Figure5.6. It can be observed from Figure 5.6 that the gain can be increased at the cost of power consumption. The Pareto front consists of two regions representing different rates of gain increment with respect to power consumption. In the first region, gain is increasing at a slower rate as compared to the rate in the second region. However, high gain at the cost of large power consumption may not usually be preferred. It can be further observed that the front generated by proposed MHPSO-CD is comparatively more diverse and dense than the fronts obtained by other standard algorithms.

5.3.2 Folded cascode OpAmp

As we know the folded cascode topology is commonly used to obtain improved input common-mode range, self-compensation, and high gain. A folded cascode OpAmp is shown in Figure5.4 which is used as a test case. In this circuit the load capacitance C_L is set to 5 pF. This circuit is designed using 0.18 μm CMOS process technology and a fixed power supply of 1.8V is used. The width (W) and length (L) of all the transistors are kept within [0.24, 1000 μm] and [0.18, 10 μm], respectively. The bias current in this circuit varies between 1 μA to 2.5 mA. The appropriate differential operation and current biasing are ensured by matching relations (e.g., M1≡M2, M3≡M4, and M5≡M7) between the transistors. The analytical form of performance specifications [3] are expressed in (5.8). The design problem is formulated as a multi-objective optimization problem using the constraints shown in Table. 5.3.

A population size of 100 particles is evolved over 200 generations in the course of optimization process. The Pareto fronts are generated to visualize the tradeoff between gain and power consumption. Further, the comparison between Pareto fronts generated by proposed algorithms (MHPSO and MHPSO-CD) and other evolutionary algorithms are shown in Figure5.7. It can be observed from Figure 5.7 that the higher gain is obtained at the cost of increased power dissipation. It should be noted that the front generated by MHPSO-CD is comparatively more diverse and dense as compared to the front generated by other standard algorithms.

$$\begin{aligned} A_v &= g_{m2}R_{out} \\ R_{out} &= (g_{m8}r_{ds8}r_{ds6}) \parallel [g_{m10}r_{ds10}(r_{ds2} \parallel r_{ds4})] \\ P_{DC} &= v_{dd}(I_1 + I_2 + I_3 + I_4) \\ GBW &= \frac{g_{m2}}{2\pi C_L} \\ SR &= \frac{I_2}{C_L} \end{aligned} \tag{5.8}$$

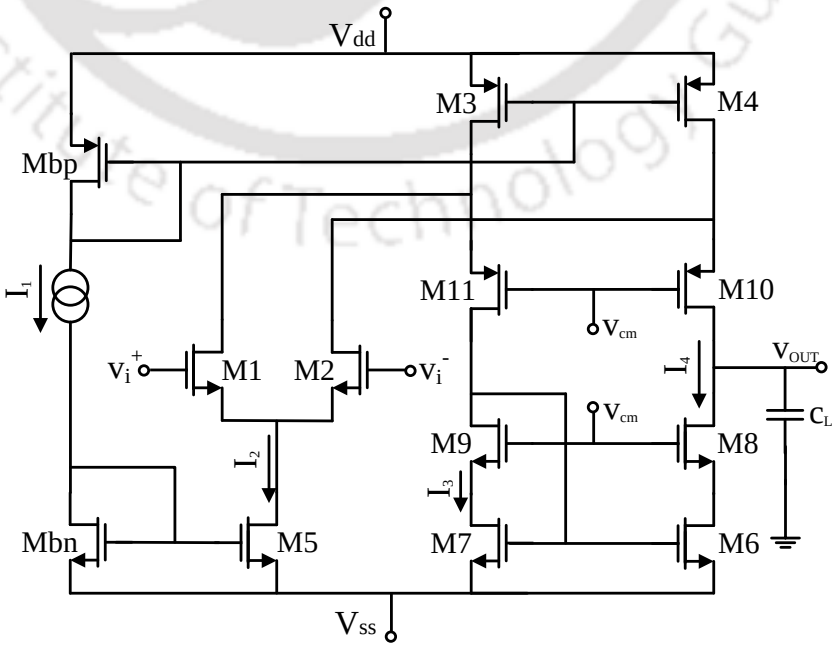


Figure 5.4: Folded Cascode Operational Amplifier circuit

Table 5.3: Folded cascode amplifier: constraints and specifications

Specifications	Constraints
DC gain (dB)	$\geq$55
GBW (MHz)	$\geq$2
Phase margin ($^\circ$)	$\geq$60
Output swing (V)	$\geq$1.2
Slew rate ($\frac{V}{\mu S}$)	$\geq$1

5.3.3 Low Noise Amplifier (LNA)

For demonstrating the effectiveness of the proposed optimization technique, a cascode LNA circuit [61] is employed as a case study. LNA consists of a common source amplifier with inductive source degeneration and a common gate load. The schematic of LNA, as shown in Figure 5.5, consists of two MOSFETs M_1 and M_2 and a tuning circuit (C_{out} and L_{out}), which is tuned at a center frequency of $2.4GHz$. Both inductors (L_g, L_s) are used for matching at the input end. The upper bound of the noise figure (NF) is kept at 2.5 (0.4dB) with a maximum power consumption of 8mW. The quality factor of LNA is kept between 3 to 5.

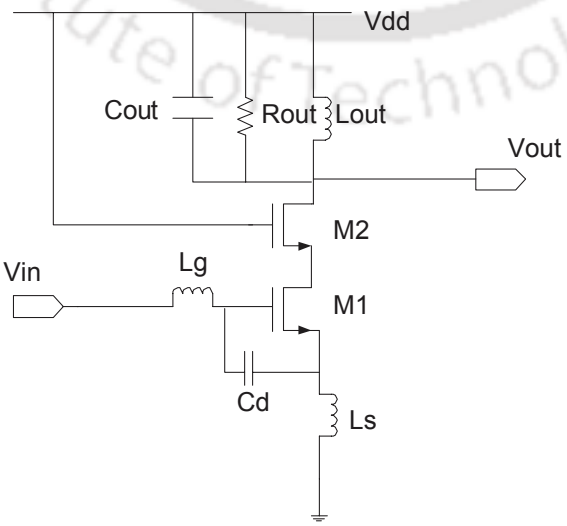


Figure 5.5: Low Noise Amplifier circuit

Table 5.4 summarizes variables and their ranges considered during the optimization of LNA. Details of different specifications and constraints during the optimization process are shown in Table 5.5.

Table 5.4: LNA: variables and ranges.

Variables	Description	Lower bound	Upper bound
W_1, W_2 [μm]	Width of M1 and M2	1	100
W_3[μm]	Width of M3	1	8
I_d[mA]	Forward drain current	0.1	4.5

Table 5.5: LNA: constraints and specifications.*Ratio of intrinsic gate capacitance of $M1$ to total capacitance ($C_{tot} = C_{gs} + C_{ext} + C_p$).

Specifications	Description	Constraints
$S11$[dB]	Input reflection coefficient @ 2.4GHz	≤ -20
$S12$[dB]	Reverse isolation @ 2.4GHz	≤ -50
$S21$[dB]	Forward power gain @ 2.4GHz	≥ 10
$S22$[dB]	Output reflection coefficient @ 2.4GHz	≤ -0.9
NF_{min}[dB]	Min. noise figure @ 2.4GHz	≤ 2.5
P_{min}[mW]	Min. power consumption @ 2.4GHz	≤ 8
f_{cf}[GHz]	Center frequency, span	$[2.4, 2.1 - 2.7]$
C_{gs}/C_{tot}	Capacitance ratio*	≤ 1
Q	Quality factor	$[3, 5]$
Z_{out}^{min}[Ω]	Min. output impedance (real part)	≥ 50

A total of 100 populations are evolved over 200 generations to obtain the Pareto front. Figure 5.8 shows various optimal Pareto fronts for minimum NF and maximum gain (S21 parameter) of LNA, obtained by different algorithms. It can be observed from these plots that with an increase in gain below $15dB$, NF increases slowly and after that NF starts to increase significantly at high gain values. LNAs with high NF deteriorates the performance of a receiver system significantly by transmitting input signals coupled with large noise to other blocks. Therefore, the feasible region having low noise figure and moderate gain can be considered to finalize the design.

Pareto fronts shown in Figures 5.6 – 5.8 are assessed qualitatively based on the hypervolume quality indicator (as shown in Table 5.6). Pareto fronts with higher hypervolume represent better quality of optimized solutions in terms of diversity of solutions. MHPSO and MHPSO-CD provide superior hypervolume for all three test circuits. In Table 5.6, b/e/w presents the number of test functions

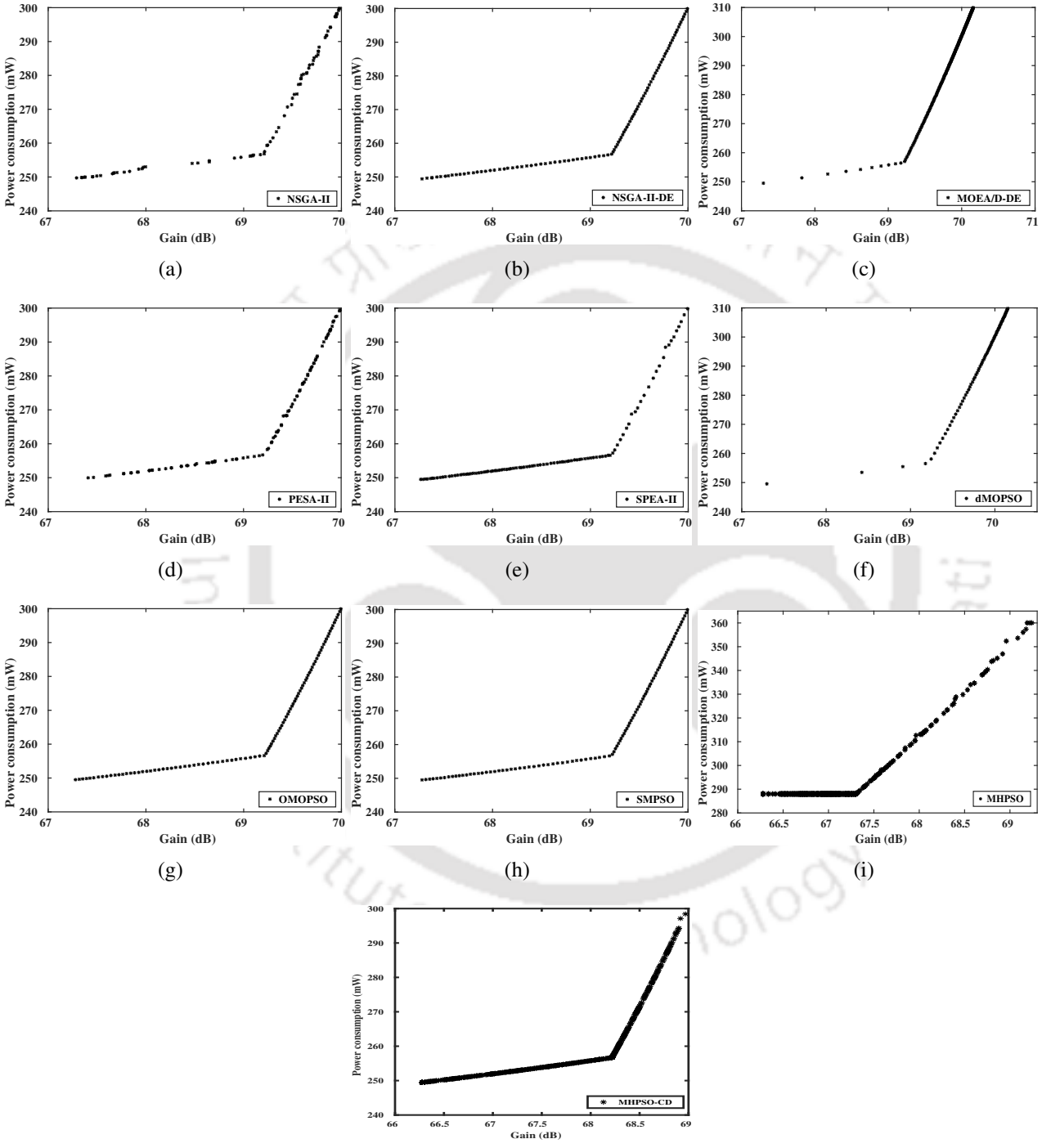


Figure 5.6: Pareto fronts generated for Two-stage OpAmp with (a) NSGA-II, (b) NSGA-II-DE, (c) MOEA/D-DE, (d) PESA-II, (e) SPEA-II, (f) DMOPSO, (g) OMOPSO, (h) SMPSO, (i) MHPSO, and (j) MHPSO-CD.

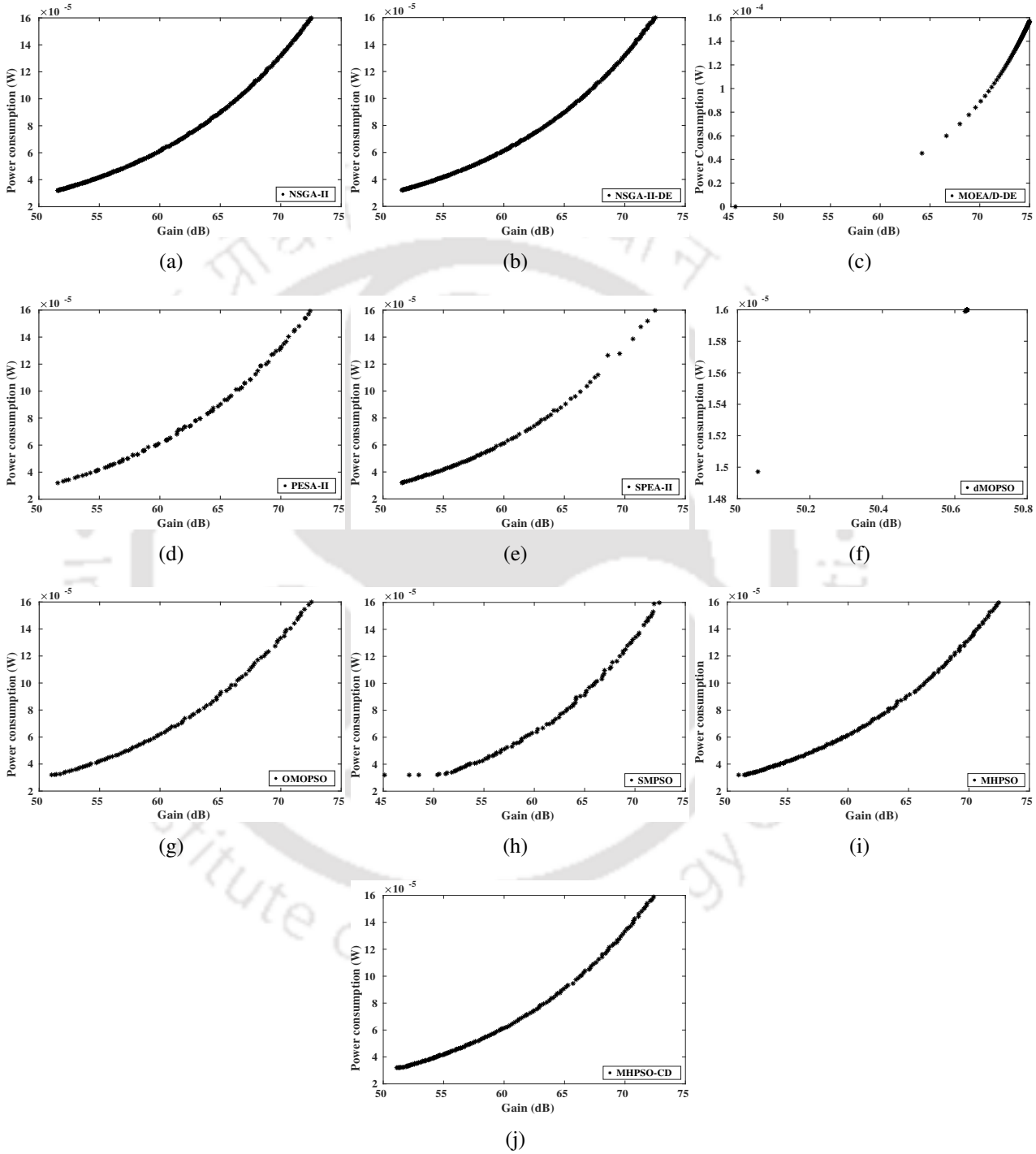


Figure 5.7: Pareto fronts generated for Folded cascode OpAmp with (a) NSGA-II, (b) NSGA-II-DE, (c) MOEA/D-DE, (d) PESA-II, (e) SPEA-II, (f) DMOPSO, (g) OMOPSO, (h) SMPSO, (i) MHPSO, and (j) MHPSO-CD.

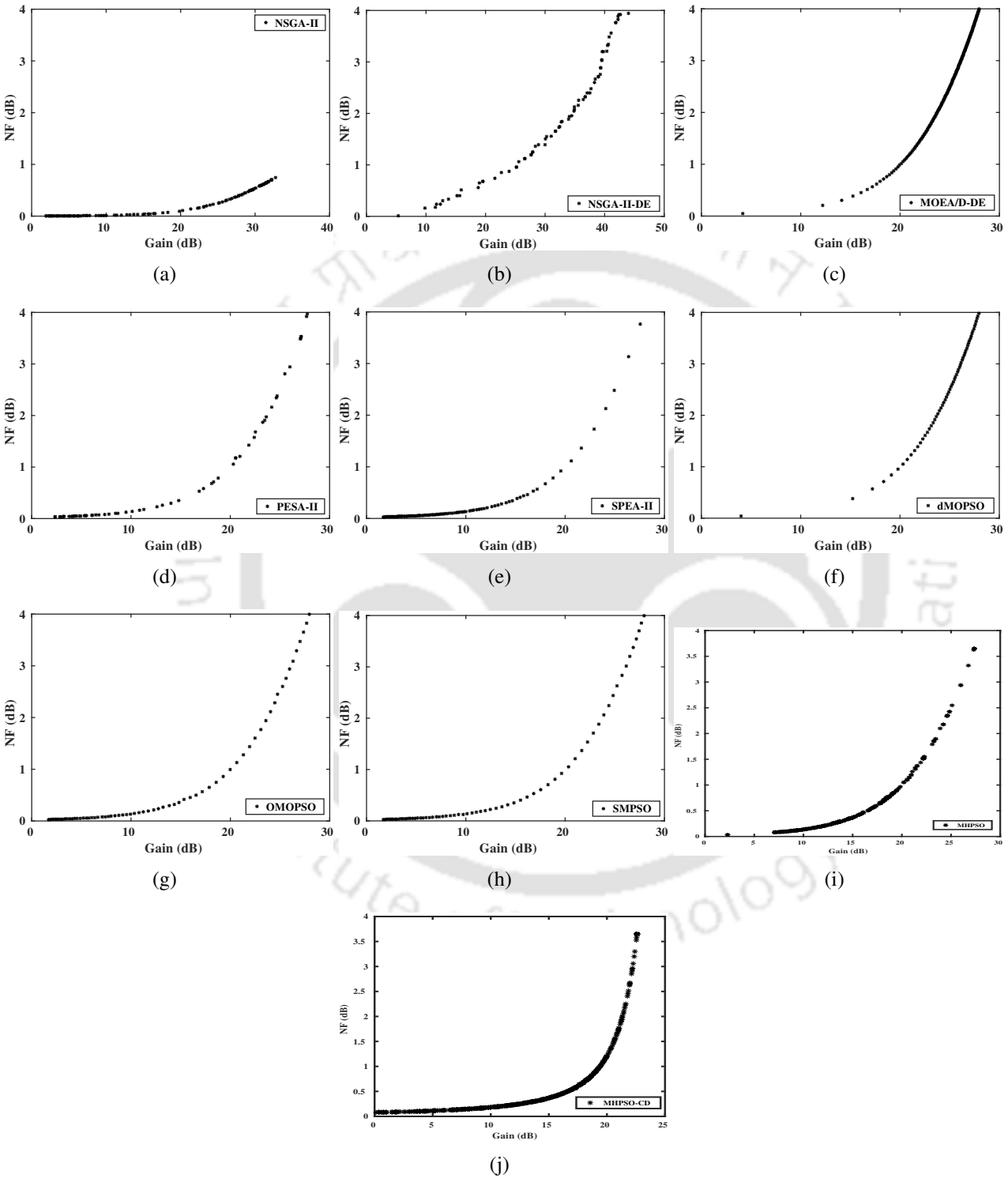


Figure 5.8: Pareto fronts generated for LNA with (a) NSGA-II, (b) NSGA-II-DE, (c) MOEA/D-DE, (d) PESA-II, (e) SPEA-II, (f) DMOPSO, (g) OMOPSO, (h) SMPSO, (i) MHPSO, and (j) MHPSO-CD.

where MHPSO and/or MHPSO-CD (any one) are better, equal to, or worse than the other cited methods with the significance level of 0.05, respectively. It may be noted that the proposed algorithms have produced better Pareto fronts for analog and RF circuits, in terms of diversity and density of nondominated solutions in the objective space.

Table 5.6: Hypervolume values for analog circuit optimization problems.

Algorithm	Two-stage opamp	Folded cascode opamp	LNA
NSGA-II	0.6045	0.8371	0.6012
NSGA-II-DE	0.6980	0.8461	0.6421
MOEA/D-DE	0.6494	0.7021	0.7256
PESA-II	0.5996	0.7433	0.5982
SPEA-II	0.6079	0.7312	0.6085
DMOPSO	0.6081	0.6086	0.5912
OMOPSO	0.7080	0.7997	0.7134
SMPSO	0.8029	0.8200	0.7465
MHPSO	0.8345	0.8361	0.7496
MHPSO-CD	**0.8556**	**0.8472**	**0.7782**
b/e/w	8/0/0	8/0/0	8/0/0

5.4 Benchmark Results and Analysis

In order to find out the competitiveness of MHPSO, it is compared with the state-of-the-art algorithms NSGA-II, NSGA-II-DE, MOEA/D-DE, PESA-II, SPEA-II, DMOPSO, OMOPSO, and SMPSO. As described earlier the performance of algorithms can quantitatively be analyzed by computing three quality metrics GD, IGD and HV.

GD, IGD and HV values for the test problems solved with different algorithms are listed in Table 5.7, where, numerical values represent the mean values of 30 runs of every algorithm for each problem, and the best performance shown by an algorithm is highlighted for each test problem. The comparison between proposed algorithms and peer algorithms is represented by b/e/w, where b, e, and w represent the number of occasions, when MHPSO and/or MHPSO-CD is performing better,

Table 5.7: GD, IGD and HV metrics standard test functions

Methods	ZDT1	ZDT2	ZDT3	ZDT4	ZDT6	SCH	FON	KUR	BINH2	CEX	OZY	TNK
GD metric:												
NSGA-II	1.1517e-01	2.0507e-01	9.6721e-02	4.0117e+01	0.2416e+01	1.1460e-02	2.4156e-03	7.3262e-02	18.1617	20.0060	0.0119	2.7255
NSGA-II-DE	2.3897e-03	2.0976e-01	2.3542e-01	7.2736e-02	2.3307e-01	8.4757e-01	2.0977e-01	1.7926e+01	2.7162e-03	3.4408e-03	2.1562e-03	6.0288e-03
MOEA/D-DE	3.2241e-03	2.7419e-01	1.7304e-01	1.7458e-03	2.8336e-01	8.5561e-01	2.7198e-01	1.7886e+01	2.2786e-03	3.2128e-04	2.4124e-03	6.0346e-03
PESA-II	0.8401e-04	2.7438e-04	5.7949e-04	7.8818e-03	7.8691e-03	1.9175e-01	5.3821e-04	2.4408e-04	2.4896e-02	4.2277e-04	1.4202e-03	7.3899e-04
SPEA-II	3.4137e-03	7.7292e-03	1.3506e-03	1.9055e-01	1.1563e-01	4.3401e-01	2.6145e-04	2.4346e-04	3.2894e-02	2.5679e-04	1.7636e-03	5.9922e-04
DMOPSO	1.0490e-04	4.9559e-05	9.8536e-05	8.9505e-05	4.1801e-05	2.2700e-04	1.2825e-04	4.1136e-04	9.6670e-03	1.8696e-02	0.5470	0.0952
OMOPSO	2.0610e-04	9.0625e-05	2.3206e-04	5.8820e-01	2.6670e-02	2.2756e-04	**1.1879e-04**	6.9291e-04	0.0258	2.1128e-04	1.7938e-03	8.3382e-04
SMPSO	1.0256e-04	4.8441e-05	1.1824e-04	7.4796e-05	1.6137e-03	2.2366e-04	1.2841e-04	2.4206e-04	2.7278e-02	2.0802e-04	1.6630e-03	9.0512e-04
MHPSO	**1.0330e-05**	4.5602e-05	**1.1728e-05**	**5.8226e-05**	**3.4366e-0**	1.2925e-04	4.0207e-04	2.4428e-04	0.11194e-03	3.9590e-03	1.6015e-03	4.6015e-04
MHPSO-CD	1.9838e-05	**4.3607e-05**	4.1766e-05	8.0437e-05	5.0003e-04	**1.1891e-04**	2.6807e-04	**1.8501e-04**	**0.2011e-04**	**1.8941e-04**	**1.0369e-03**	**4.5735e-04**
b/e/w	8/0/0	8/0/0	8/0/0	8/0/0	8/0/0	8/0/0	4/0/4	8/0/0	6/0/0	6/0/0	6/0/0	6/0/0
IGD metric:												
NSGA-II	7.9356e-02	1.4510e-01	7.2018e-03	1.4407e+01	8.4401e-01	2.2365e-03	7.8359e-04	1.2120e-02	3.8746e-02	2.6953e-03	1.3635e-03	0.6128
NSGA-II-DE	1.8796e-03	1.6733e-01	2.4908e-01	5.7595e-02	1.8216e-01	0.1467e+01	1.2627e-01	1.8181e+01	3.1612e-04	3.4915e-04	1.4290e-03	7.8635e-02
MOEA/D-DE	5.4652e-03	2.2529e-01	2.1255e-01	1.2372e-03	2.5408e-01	0.2560e+01	1.7374e-01	1.8290e+01	3.9562e-04	3.4630e-04	1.6056e-03	7.1737e-03
PESA-II	2.9049e-03	2.3787e-04	2.4666e-04	5.8863e-03	5.8600e-04	2.1274e-02	1.0119e-03	3.1286e-04	2.1411e-04	3.4398e-04	1.0047e-03	9.0237e-04
SPEA-II	1.0155e-03	1.5281e-02	5.7333e-04	3.3890e-02	1.3288e-02	3.1697e-02	2.3973e-04	**1.3727e-04**	1.5887e-04	5.0045e-04	8.8447e-03	6.1796e-04
DMOPSO	1.5926e-04	1.4076e-04	2.8151e-04	1.6759e-04	1.3987e-04	1.3766e-03	2.0804e-04	2.2666e-04	1.2544e-04	8.2293e-03	1.2335e-02	8.0866e-02
OMOPSO	1.4202e-04	1.4369e-04	1.2177e-04	1.6728e-01	1.3526e-04	3.3847e-04	**2.0799e-04**	1.6395e-04	1.1443e-04	1.9562e-04	1.0112e-02	4.9077e-04
SMPSO	1.3510e-04	1.3807e-04	1.0258e-04	1.3529e-04	1.3442e-04	3.5439e-04	2.4157e-04	1.5296e-04	1.1615e-04	1.9699e-04	1.0219e-02	6.2999e-04
MHPSO	1.3050e-05	1.0899e-05	4.1827e-05	9.8683e-04	**7.9775e-05**	3.8836e-04	7.4135e-03	1.3913e-04	1.0712e-04	2.4649e-03	1.1682e-03	4.1682e-04
MHPSO-CD	**1.2648e-05**	**1.0781e-05**	**3.1180e-05**	**7.0228e-04**	4.2758e-04	**2.7278e-04**	2.8085e-02	1.6301e-04	**1.0547e-04**	**1.2167e-04**	**1.8959e-04**	**4.0733e-04**
b/e/w	8/0/0	8/0/0	8/0/0	8/0/0	8/0/0	8/0/0	4/0/4	7/0/1	6/0/0	6/0/0	6/0/0	6/0/0
HV metric:												
NSGA-II	0.6575	0.3241	0.5131	0.6518	0.3773	0.6620	0.3079	0.3994	0.7249	0.7629	0.3765	0.3322
NSGA-II-DE	0.6362	0.4092	0.4856	0.4608	0.4679	0.6397	0.4092	0.4856	0.7287	0.7651	0.7472	0.4402
MOEA/D-DE	0.6644	0.3311	0.5161	0.6646	0.4047	0.7936	0.3155	0.4034	0.7239	0.7703	0.7243	0.4866
PESA-II	0.6313	0.3232	0.5037	0.5739	0.3761	0.7346	0.3045	0.3962	0.7215	0.7717	0.7066	0.3038
SPEA-II	0.6164	0.0528	0.4868	0.6577	0.0447	0.5504	0.3102	0.3996	0.7242	0.7752	0.7045	0.3047
DMOPSO	0.6615	0.3283	0.5136	0.6609	0.4013	0.8284	0.3118	0.3962	0.7283	0.8305	0.7567	0.7194
OMOPSO	0.6603	0.3278	0.5115	0.6547	0.4012	**0.8299**	0.3123	0.3972	0.7275	0.7759	0.7020	0.3060
SMPSO	0.6617	0.3286	0.5155	0.6615	0.4012	0.8208	0.3124	0.4001	0.7275	0.7756	0.6981	0.3047
MHPSO	0.6651	0.3321	0.7854	0.6658	0.2683	0.7265	0.4553	0.5219	0.8067	0.7457	0.7347	0.7303
MHPSO-CD	**0.6675**	**0.4351**	**0.7865**	**0.6708**	**0.4816**	0.8291	**0.5131**	**0.5367**	**0.8267**	**0.8709**	**0.7821**	**0.7416**
b/e/w	8/0/0	8/0/0	8/0/0	8/0/0	8/0/0	7/0/1	8/0/0	8/0/0	6/0/0	6/0/0	6/0/0	6/0/0

equal, and worse than the other algorithms, respectively. As evident from Table 5.7, GD values for MHPSO and/or MHPSO-CD are better for most of the test functions except FON. It indicates that the resulting Pareto fronts from MHPSO/MHPSO-CD are closer to the true Pareto fronts (standard solutions set) than the fronts generated by rest of the algorithms except one function FON. IGD metric indicates closeness to the actual front as well as diversity of the obtained Pareto front. The IGD values shows MHPSO is performing better for all functions except FON and KUR. The larger value of HV metric indicates better convergence and diversity of obtained Pareto front. The results obtained for HV metric exhibit that the performance of MHPSO better for all the functions except SCH.

It can be observed from the experiments (analog/RF circuits and test functions) that proposed methods provide superior Pareto fronts as compared to standard methods and is supported by quality metrics indicators to measure performance of all the methods.

5.5 Summary

In this chapter, a new algorithm based on the hybridization of PSO and SA is presented to evaluate multi-objective optimization problems. In this method, an archive of nondominated solutions is maintained during PSO followed by SA. Simulated annealing is applied on the reduced solution space (solutions excluding the archive, populated by PSO) to update archive with more nondominated solutions, hence, improving the quality of Pareto fronts in terms of diversity and density. Further, an extension of this approach incorporating crowding distance is also proposed. It is observed that the application of crowding distance during archive maintenance improves the diversity of obtained Pareto fronts.

The proposed scheme is applied for the optimization of two popular analog circuits and one RF circuit. Each circuit is tested for two competitive objectives, i.e., gain – power consumption in case of two-stage and folded cascode operational amplifiers, and gain – noise figure in case of LNA circuit. It is noticed that the proposed methods provide superior solutions as compared to other standard methods for an improved performance.

6

Conclusions and Future Work

In this chapter, we have summarized various methods for analog/RF circuit optimization. An electrical network based optimization method by employing adjoint network based sensitivity analysis is presented in this thesis to reduce manual efforts in the analog circuit design flow. As we know, due to huge manual efforts in the design of analog/RF circuits, search for new methods to reduce manual efforts is the need of hour. Therefore, the design of analog circuits requires electronic design automation tools, equipped with state-of-the-art efficient circuit analysis and optimization techniques. In this thesis, we have presented techniques for analog/RF circuit optimization based on adjoint network sensitivity analysis and metaheuristics employing classical and evolutionary algorithms. A brief discussion of these methods and scope of their extension are discussed as follows:

- Analog circuit sizing using adjoint network based sensitivity analysis (ANSA):

  In order to optimize the analog circuit, an objective function subject to various constraints needs to be optimized. This objective function is composed of various circuit parameters. Therefore, optimal behavior of the circuit depends on the optimal values of circuit parameters. For estimating optimal circuit parameters, we need to employ a suitable methodology which tradeoffs among these parameters to obtain optimal performance. The change in one parameter or sensitivity may affect performance of other parameter impacting circuit performance as well. Thus, circuit performance depends upon the sensitivities of circuit's response with respect to various parameters and in order to find optimal parameters for optimal circuit performance, we need to estimate sensitivities of various parameters in an efficient manner. It has been observed that with the large number of parameters, standard methods provide inefficient solutions. For optimizing the objective function, we need to calculate gradient of the objective function. By using the sensitivities, gradient of the objective function can be derived. It is known that the calculation of sensitivities of circuit parameters is a computationally intensive task. Therefore, we employ ANSA method to address this issue.

  In this method, an adjoint network of the original analog circuit is constructed by using small-signal model of the original circuit, in which MOS transistors are replaced by their small signal model. All the sensitivities can be calculated simultaneously by analyzing original circuit and

its adjoint transformation. For evaluating optimal circuit design the objective function is analyzed iteratively with respect to constraints until the convergence is achieved. In this process, we search for the solution in design space exhibiting optimal performance. Therefore, in each step a search direction is estimated by using steepest descent method. In this method, during gradient calculations, sensitivities of circuit's response with respect to various parameters are used. The calculation of sensitivities is performed by the analysis of original and its adjoint transformation of analog circuit in almost linear time. In steepest descent method, the step size is calculated by applying Barzilai and Borwein method [67]. In this way, our proposed method efficiently optimizes analog circuits using minimal number of steps. The applicability and effectiveness of the proposed method are demonstrated by designing the basic analog circuits, cascode amplifier and two-stage operational amplifier, and the results are verified by employing commercial EDA tool provided by Mentor Graphics. Further, a two-stage operational amplifier is designed using ANSA and fabricated with 180 nm CMOS bulk technology. The post fabrication measurement results of two-stage OpAmp are compared with the simulation results of optimal circuit obtained using the proposed method.

In the entire process of optimization, analog circuit optimization problem is represented in the convex formulation by using basic square-law model causing approximation error in the results. In future, this error can be reduced by using higher order analytical model [50]. Further, accuracy of proposed method depends on the selection of initial design (first-cut design), therefore, a better initial design can be produced by employing g_m/I_D method [70]. The proposed method offers scope for the parallelization. Thus, there will be an endeavor in future to employ efficient parallelization schemes to improve runtime efficiency of the proposed methodology using parallel computing platforms.

- Application of evolutionary algorithms for analog circuit optimization (HPSO):

  The requirement of convex formulation and a better initial guess limits the application of ANSA for wider range of circuits. In order to address these issues, we employ evolutionary algorithms for the optimization of analog/RF circuits. Evolutionary algorithms are very efficient in solv-

ing optimization problems bounded by constraints. Analog circuit optimization can suitably be attempted by employing such algorithms. In case of evolutionary algorithms or heuristics, convex problem formulation is not necessary to generate a global solution. In the recent literature different algorithms PSO, GA, SA, etc., have been effectively utilized for the optimization of analog/RF circuit. The issues with these individual algorithms, i.e., slow convergence (SA), premature convergence (PSO), trapping in local solutions (PSO), complicated application (GA) etc. can be attempted by combining them to form hybrid methods or metaheuristics.

In this thesis, a hybrid method (HPSO) using PSO followed by SA is proposed. In this method, the velocity of every particle in the initial population is mapped into temperatures and then based on the different temperature regions, SA is applied in these regions to search for the best solutions. Further, an extension of HPSO (l-HPSO) is proposed with the improved search strategy using Lévy flight method. Both HPSO and l-HPSO are experimented with standard test functions for single objective optimization, and are applied to the optimization of analog/RF circuits, namely two-stage OpAmp, OTA and LNA. These proposed methods are compared with other methods to showcase their effectiveness.

In future, considering HPSO as the base algorithm, different improvements in PSO can be implemented for better performance, namely ALC-PSO, PSO with state vector machines, heterogeneous PSO etc. Further, this extension can also be employed for the optimization of analog/RF circuits.

- Multi-objective optimization methods for analog circuit sizing (MHPSO):

  The various tradeoffs involved in analog circuit design can be analyzed by applying multi-objective optimization (MOO) algorithms. In this thesis, the proposed HPSO method is developed as a multi-objective approach for analog/RF circuit design. In MOO techniques, a set of optimum solutions is evaluated unlike its single-objective counterpart which is referred as Pareto front. Each member of a Pareto front represents an optimum circuit design. Pareto front enables designers to analyze behavior of the circuit in a broad manner.

  The method is based on the hybrid of PSO and SA with crowding distance scheme for archive

maintenance. By applying crowding distance scheme, diversity of the Pareto front is improved. Using these proposed methods, three analog/RF circuits, namely two-stage OpAmp, OTA and LNA have been optimized and the results of proposed methods are compared with other standard methods to showcase their effectiveness.

In future, the proposed methodology can be extended for the real life multi-objective optimization problems found in different technical fields. The application of proposed approach can further be extended to analyze yield of the designed circuit, and effect of process variation on the obtained Pareto front. Scope of the proposed methodology may be extended in other social and economic domains.

भारतीय प्रौद्योगिकी संस्थान गुवाहाटी
Indian Institute of Technology Guwahati

A

Summary of Sizing/Optimization Tools for Analog Circuits

A. Summary of Sizing/Optimization Tools for Analog Circuits

Table A.1: Summary of sizing/optimization tools for analog circuits

Tool/Authors	Methodology	Pros/Cons
IDAC [16]	Design plan followed by SA optimization	Based on equations hence fast, but design plan preparation was very time consuming.
DELIGHT.SPICE [28]	Equation based optimization with improved SPICE model	Setup time was moderate and simulation consumed several hours.
OPASYN [18]	Based on classical numerical technique	Topology specific simulation setup needed significant time and compilation consumed a few minutes
OPTIMAN [25]	Based on simulated annealing	Equation based optimization and time consumption is few minutes.
STAIC [19]	Based on successive solution techniques	Equation based optimization, setup time is large and solution time is a few minutes.
Maulik et. al. [20]	Based on sequential quadratic programming	Preparation time for BSIM and equation models was several months and, simulation time was a few minutes.
FRIDGE [30]	Based simulated annealing	Setup and simulation consumed about an hour
DARWIN [27]	Based on genetic algorithm	Small signal analytical model formation consumed a significant time and setup process is complex due to different parameters of GA.
FASY [24]	Based on simulated annealing combined with gradient methods	Simulation based optimization consumed a few hours for optimization.
ASTRX/OBLX [26]	Based on simulated annealing	Although asymptotic waveform evaluation (AWE) based equation solutions took a few seconds but the setup time was a few days
GPCAD [22]	Based on geometric programming	Formulation of a convex optimization problem introduced errors but a fast tool for circuit sizing.
MAELSTROM [37]	Based on genetic algorithm and simulated annealing	parallel computing reduced the simulation time to a few hours.
ANACONDA [35]	Based on stochastic pattern search	execution time was several hours.
Alpaydin [34]	Based on evolutionary strategies and simulated annealing	Fuzzy and NN trained simulation consumed a few days.
Barros [1]	Based on genetic algorithm	Simulation based optimization method consumed several minutes.
MOJITO [48]	Based on NSGA-II	Simulation based optimization method consumed several days.
Fakhfakh [39]	Based on multi-objective particle swarm optimization	Equation based solution by PSO made it quite fast and it consumed less than a minute.

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List of Publications

Journal Publications

- Published Papers:

  1. **Deepak Joshi**, Satyabrata Dash, HS Jatana, Ratnajit Bhattacharjee and Gaurav Trivedi, "Analog circuit optimization using adjoint network based sensitivity analysis", in *AEU - International Journal of Electronics and Communications*, Volume 82, 2017, Pages 221-225, ISSN 1434-8411, https://doi.org/10.1016/j.aeue.2017.08.053.

- Manuscripts Under Review

  1. **Deepak Joshi**, Satyabrata Dash, Y. Sushanth Reddy, M. Rahul Reddy, and Gaurav Trivedi, "Multi-objective Hybrid Particle Swarm Optimization and its Application to Analog and RF Circuit Optimization ", in *ACM Trans. Des. Autom. Electron. Syst.* (under review)

Conference and Workshop Publications

1. **Deepak Joshi**, Satyabrata Dash, Ayush Malhotra, Pulimi Venkata Sai, Rahul Das, Dikshit Sharma and Gaurav Trivedi, "Optimization of 2.4 GHz CMOS Low Noise Amplifier using Hybrid Particle Swarm Optimization with Lévy Flight", *30th International Conference on VLSI Design*, Hyderabad, 2017.

2. **Deepak Joshi**, Satyabrata Dash, Ujjawal Agarwal, Ratnajit Bhattacharjee and Gaurav Trivedi, "Analog Circuit Optimization Based on Hybrid Particle Swarm Optimization", *International Conference on Computational Science and Computational Intelligence*, Las Vegas, 2015.

3. **Deepak Joshi**, Satyabrata Dash, Ratnajit Bhattacharjee, Gaurav Trivedi, "A method of analog circuit optimization using adjoint sensitivity analysis", *25th International Conference on Radioelektronika*, CZ, 2015. (Student Best Oral Paper Award)