INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI
SHORT ABSTRACT OF THESIS

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Thesis Title:
Design and Implementation of Hardware-Efficient Architectures for FFT Algorithms

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SHORT ABSTRACT

The Fast Fourier Transform (FFT) holds significance across diverse applications in wireless communications, audio, and signal processing. This doctoral thesis addresses the imperative need to enhance hardware efficiency while concurrently minimizing area and power consumption in FFT processors. Extensive efforts by researchers have centered on optimizing FFT algorithms, determining the requisite number of multipliers, adders, and registers, all of which intricately influence power consumption and overall area. These considerations become pivotal constraints in FFT applications, necessitating a judicious trade-off between complexity and performance.

This research categorizes FFT architectures based on the level of parallelism: serial, parallel, or fully-parallel, each manifesting distinct computational and efficiency characteristics and aiming to realize hardware-efficient implementations with reduced complexity, thereby diminishing the demand for computational resources. The strategies employed encompass novel data flow graphs, specialized multipliers, and innovative memory-based approaches tailored to real-valued signals. Additionally, a fully parallel-pipelined split-radix based low-cost FFT architecture is proposed, addressing power consumption and latency challenges prevalent in existing fully-parallel FFTs. The comparative analysis substantiates the superior performance of the proposed design. This research not only contributes to the advancement of FFT architectures but also holds broader implications for signal processing applications, presenting directions for future research endeavors in pursuit of improved designs and methodologies.