DC-DC Converters with High Step-up/Step-down Conversion Ratio and Reduced Voltage Stress

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By

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Dedicated to

My Father

Mr. Nityananda Biswas

My Mother

Mrs. Kalpana Mandal Biswas

My Sister: Soumi Biswas and Cousin: Pankaj Biswas

My Uncle: Shribas Biswas

Certificate

This is to certify that the thesis entitled "**DC-DC Converters with High Step-up/Step-down Conversion Ratio and Reduced Voltage Stress**", submitted by **Mriganka Biswas** (146102032), a PhD student in the *Department of Electronics and Electrical Engineering, Indian Institute of Technology Guwahati*, for the award of the degree of **Doctor of Philosophy**, has been carried out by him under our supervision and guidance. The thesis has fulfilled all requirements as per the regulations of the Institute and in our opinion has reached the standard needed for submission. The results embodied in this thesis have not been submitted to any other university or institute for the award of any degree or diploma.

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"বিদ্যা বাহির হইতেই কেবল জমা করিলাম, ভিতর বইতে কিছু তো দিলাম না। কলসে কেবলই জল ভরিতে থাকিব, অথচ সে জল কোনোদিনই যথেষ্ট পরিমাণে দান-পানের উপযোগী ভরা হইবে না, এ যে বিষম বিপত্তি।

শিক্ষার এই শক্তিহীনতা আমরা স্পষ্টই বুঝিতেছি। আমাদের শিক্ষাকে আমাদের বাহন করিলাম না, শিক্ষাকে আমরা বহন করিয়াই চলিলাম, ইহারই পরম দুঃখ গোচরে অগোচরে আমাদের মনের মধ্যে জমিয়া উঠিতেছে।"

"শিক্ষা/অসন্তোষের কারণ"- রবীন্দ্রনাথ ঠাকুর

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Abstract

The thesis presents the design and implementation of DC-DC converters with improved step-up/step-down conversion ratio and reduced voltage stress. Firstly, a high step-down buck converter (HSDBuC) is proposed to produce a lower output voltage at a sufficiently higher duty ratio compared to the conventional buck converter (CBuC). The step-down voltage conversion ratio is modified by a series-parallel transition of two identical capacitors of a switch-capacitor cell. The cell consists of two parallel switches and two cross-connected identical capacitors. These identical capacitors are charged in series and discharged in parallel by producing a lower output voltage compared to CBuC at the same duty ratio. The modified voltage conversion ratio reduces the ripples in inductor currents and output voltage. This proposed HSDBuC utilizes a dual winding coupled inductor to reduce the ripples in inductor currents and output voltage even more. The voltage and current stresses of the semiconductor devices employed in HSDBuC are less. The switch-capacitor cell which is utilized to modify the voltage conversion ratio of HSDBuC is also used to modify the step-down conversion ratio of the conventional interleaved buck converter (CIBuC). The modified voltage conversion ratio helps to reduce the voltage and current stresses of the semiconductor devices of the proposed high step-down interleaved buck converter (HSDIBuC). The two single inductors at the output end of the HSDIBuC are replaced by a dual-winding coupled inductor (DWCI) to further improve the ripples in inductor currents and achieve a lower value of the output filter capacitor. A systematic step-by-step analysis is performed for the different cases of operations to investigate the effect of the coupling factor of the DWCI in the reduction of ripple and the size of the output filter capacitor of the high step-down interleaved buck converter with a dual-winding coupled inductor (HSDIBuC-DWCI). After modifying the step-down conversion ratio of CBuC and CIBuC using a switch-capacitor cell, a diode-capacitor cell is utilized to enhance the voltage conversion ratio of the conventional boost converter (CBoC) and conventional interleaved boost converters (CIBoC). The proposed high step-up boost converter (HSUBoC) reduces the ripples in input current, inductor current and output voltage with the help of the coupling factor of DWCI. Thereafter, the diode-capacitor cell is used to modify the voltage conversion ratio of CIBoC. The voltage and current stresses of the proposed high step-up interleaved boost converter (HSUIBoC) are less than the high output voltage. All the analyses and the subsequent design procedures of the proposed HSDBuC, HSDIBuC, HSDIBuC-DWCI, HSUBoC and HSUIBoC are accomplished in continuous conduction mode (CCM). In the voltage-mode control (VMC) framework, suitable controllers for each of these converters are designed to investigate the sensitivity to the load parameter variation and the performance under varying reference output voltage. Finally, the proposed converters are implemented in hardware and their performances are verified experimentally.

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Contents

List of Figures

List of Tables

List of Symbols and Abbreviations

$\mathbf{A_1}$, $\mathbf{A_2}$, $\mathbf{A_3}$, $\mathbf{A_4}$	State matrices
$\mathbf{A_{av}}$	Average state matrix
A_e	Cross-section area
$\mathbf{B_1}$, $\mathbf{B_2}$, $\mathbf{B_3}$, $\mathbf{B_4}$	Input matrices
$\mathbf{B_{av}}$	Average input matrix
B_{max}	Flux density
$C = C_1$, C_2	Identical capacitors
C_f	Output filter capacitor
D, D_1, D_2, D_3	Diodes
f_s	Switching frequency
$G_{v\alpha}(s)$	Output voltage to duty ratio transfer function
$G_{vg}(s)$	Output to input voltage transfer function
$G_c(s)$	Transfer function of controller
$G_{comp}(s)$	Compensated plant
I_L, I_{L_i}, I_{L_f}, I_{L_1}, I_{L_2}	Steady-state currents through inductors
$\hat{i}_L$, $\hat{i}_{L_i}$, $\hat{i}_{L_f}$, $\hat{i}_{L_1}$, $\hat{i}_{L_2}$	Perturbation in currents through inductors
i_L, i_{L_i}, i_{L_f}, i_{L_1}, i_{L_2}	Inductor currents with steady-state and perturbation
i_R	Load current
Δi_{in}	Ripple in input current
Δi_C	Ripple in input current of conventional buck
i_o	Output current
I_o	Steady-state output current
i_S, i_{S_1}, i_{S_2}, i_{S_3}	Currents through the switches
i_D, i_{D_1}, i_{D_2}, i_{D_3}	Currents through the diodes
i_C	Current through identical capacitors
i_{C_f}	Current through output filter capacitors
$I_{S_{rms}}$, $I_{S_{1rms}}$, $I_{S_{2rms}}$, $I_{S_{3rms}}$	Switch rms current
$I_{D_{rms}}$, $I_{D_{1rms}}$, $I_{D_{2rms}}$, $I_{D_{3rms}}$	Diode rms current
k	Coupling factor

K_p	Proportional constant
K_i	Integral constant
L, L_i, L_f, L_1, L_2	Inductors
L_r	Leakage inductance
M	Mutual inductance
M_p	Maximum peak overshoot
n	Turns ratio
N	Turns number of coupled inductor
P_o	Output power loss
P_{in}	Input power loss
$r_{DS(on)}$	Switch ON-state resistance
r_L, r_{L_i}, r_{L_f}	Parasitics of indcutors
r_{C_1}, r_{C_2}	Parasitics of identical capacitors
r_D, r_{D_1}, r_{D_2}, r_{D_3}	Diode conduction resistances
r_{C_f}	Equivalent series resistance (ESR)
R	Load resistance
S, S_1, S_2, S_3	Switches
t_s	Settling time
t_r	Rise time
T_s	Switching time period
V_{in}	Steady-state input voltage
$\hat{v}_{in}$	Perturbation in input voltage
v_{in}	Input voltage with steady-state and perturbation
V_o	Steady-state output voltage
$\hat{v}_o$	Perturbation in output voltage
v_o	Output voltage with steady-state and perturbation
V_C	Steady-state identical capacitive voltage
$\hat{v}_C$	Perturbation in identical capacitive voltage
v_C	Identical capacitive voltage with steady-state and perturbation
v_{fd}, v_{fd_1}, v_{fd_2}, v_{fd_3}	Forword bias voltages of diodes
V_{C_f}	Steady-state voltage across the output filter capacitor
$\hat{v}_{C_f}$	Perturbation in voltage across the output filter capacitor
v_{C_f}	Output capacitive voltage with steady-state and perturbation
V_{gs}, V_{gs_1}, V_{gs_2}, V_{gs_3}	Gate to source voltages
v_S, v_{S_1}, v_{S_2}, v_{S_3}	Switch voltage stresses
v_D, v_{D_1}, v_{D_2}, v_{D_3}	Diode voltage stresses
$v_{ref}(s)$	Reference voltage

$\mathbf{x}(t)$	State variables
$\hat{\mathbf{x}}(t)$	Perturbation in state variables
$\dot{\mathbf{x}}(t)$	Derivative of state variables
X	Steady-state value of state variables
$\mathbf{Z_1}$, $\mathbf{Z_2}$, $\mathbf{Z_3}$, $\mathbf{Z_4}$	Output matrices
$\mathbf{Z_{av}}$	Average output matrix
$\varphi_1 T_s$, $\varphi_2 T_s$, $\varphi_3 T_s$, $\varphi_4 T_s$	Switching instants
α	Duty ratio
Δi_L, Δi_{L_i}, Δi_{L_1}, Δi_{L_2}	Ripples in inductor currents
ΔV_o	Output voltage ripple
Δv_C	Voltage ripple in identical capacitors
ΔQ	Charge
η	Efficiency
$BESS$	Battery energy storage system
$CBuC$	Conventional buck converter
$CBoC$	Conventional boost converter
$CIBuC$	Conventional interleaved buck converter
$CIBoC$	Conventional interleaved boost converter
CCM	Continuous conduction mode
DCM	Discontinuous conduction mode
$DWCI$	Dual-winding coupled inductor
ESR	Equivalent series resistance
$HSDBuC$	High step-down buck converter
$HSDIBuC$	High step-down interleaved buck converter
$HSDIBuC - DWCI$	High step-down interleaved buck converter with DWCI
$HSUBoC$	High step-up boost converter
$HSUIBoC$	High step-up interleaved boost converter
$IBuC$	Interleaved buck converter
$IBoC$	Interleaved boost converter
OVR	Output voltage ripple
PI	Proportional-integral
VSB	Voltage second balance
VMC	Voltage mode controller

1

Introduction

The DC-DC buck converter is extensively used due to its simple structure and cost-effectiveness in a variety of non-isolated type applications such as voltage regulator modules for microprocessors, telecommunication, power systems, LED drivers and automotive applications. More often, such applications need DC-DC converter with high step-up/step-down voltage conversion ratio. Therefore, high-performance DC-DC converters have become emerging trends in the development of power converters. In this chapter, a brief introduction on conventional buck and boost converter is provided. Thereafter, a literature survey on other existing step-up/step-down converters is presented. Motivated by the literature survey, the purpose and the contribution of the thesis are explained. Finally, the organization of the thesis is provided at the end of this chapter.

Conventional energy resources like coal, gas and petroleum, apart from their fast depletion, contribute significantly to environmental degradation. Therefore, to address the drawbacks of such energy resources, an increasing number of researchers are attracted towards the exploration of the environment-friendly renewable energy sources such as photovoltaic, ocean and wind power generation [1, 2]. However, these non-conventional renewable energy resources suffer from two key issues which are variability and uncertainty. These unreliable power outputs can be remedied by a battery energy storage system (BESS). More often, the BESS is incapable of providing the desire output voltage or current. Generally, these problems are solved by using power converters which are capable of stepping-up/down the input voltage i.e. battery voltage and hence act as DC counterparts of transformers.

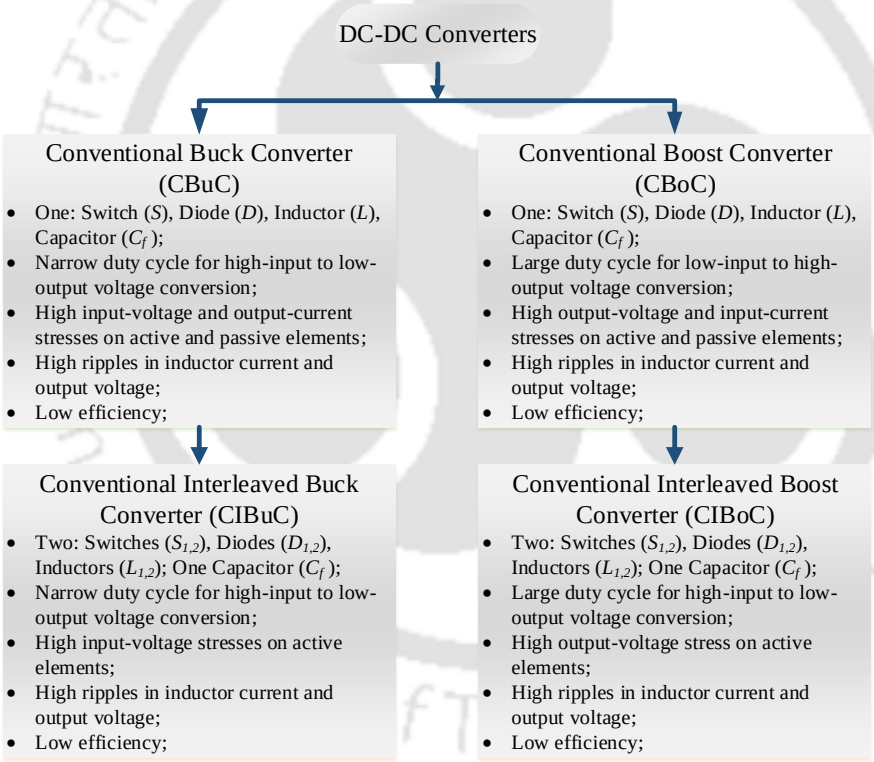


Figure 1.1: Classifications of conventional DC-DC buck and boost converters

This apart, power converters also find their usage in battery chargers, voltage regulator modules (VRMs) for microprocessors, telecommunication, power systems, light emitting diodes (LEDs) drivers, super-capacitor energy storage systems and automotive applications [3–6] in sectors as diverse as commercial, industrial, transportation and aeronautics. Among the power

converters, high-efficiency and high step-up/down converters in particular, are seeing an increasing demand in the aforementioned applications [7–9]. More specifically, due to intense market competition, the requirement is driven towards designing low-cost converter with high density for a better profit and performance.

Basically, there are two types of DC-DC converters namely, buck and boost converters. A tree of conventional step-up/down converters is shown in Figure 1.1 to understand the classifications of the conventional DC converters. To convert the high DC input voltage to a lower DC output voltage, the conventional buck converter (CBuC) is used as shown in Figure 1.2a. This converter is extensively popular due to its simple structure and cost-effectiveness in a variety of non-isolated type aforementioned applications. For very high voltage to low voltage applications, the CBuC needs an extremely narrow duty cycle. The semiconductor devices of the CBuC suffer the high current and input voltage stresses. Moreover, the efficiency of the CBuC is low and the current stresses in the passive elements are high as well.

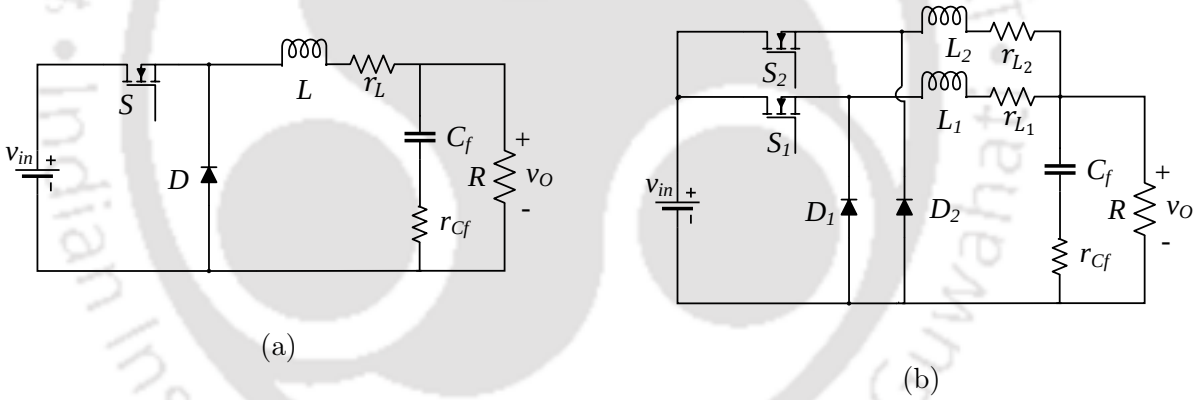


Figure 1.2: Circuit diagram of (a) Conventional buck converter (CBuC), and (b) Conventional interleaved buck converter (CIBuC)

Therefore, the CBuC can be used as an interleaving circuit configuration to reduce the current stresses of the active and passive elements as shown in Figure 1.2b. Due to its simple circuit configuration and low control complexity, conventional interleaved buck converter (CIBuC) is a current topic of research especially in the field of non-isolation applications with low output current ripple [10–12]. It should be noted though, that the active elements of CIBuC suffer from high input voltage which increases the voltage ratings of these components. This unwanted phenomenon gives rise to large voltage drop, high on-resistance and high cost. Apart from these shortcomings, in spite of using two CBuCs in parallel, the CIBuC shows no

improvement in voltage conversion ratio compared to the CBuC. Hence, only a very narrow duty cycle is permissible in the case of CIBuC for high input voltage to low output voltage conversion [13].

Now, on the other hand, conventional boost converter (CBoC) converts the low input voltage to a higher output voltage as shown in Figure 1.3a. For low voltage to high voltage conversion, the CBoC needs a very wide duty ratio. This wide duty ratio negatively impacts the efficiency resulting in more power loss. Apart from that, the semiconductor devices suffer high output voltage stress with undesirably high ripples in inductor current and output voltage. As in CBuC, the current stresses of the active and passive elements are also high in this case.

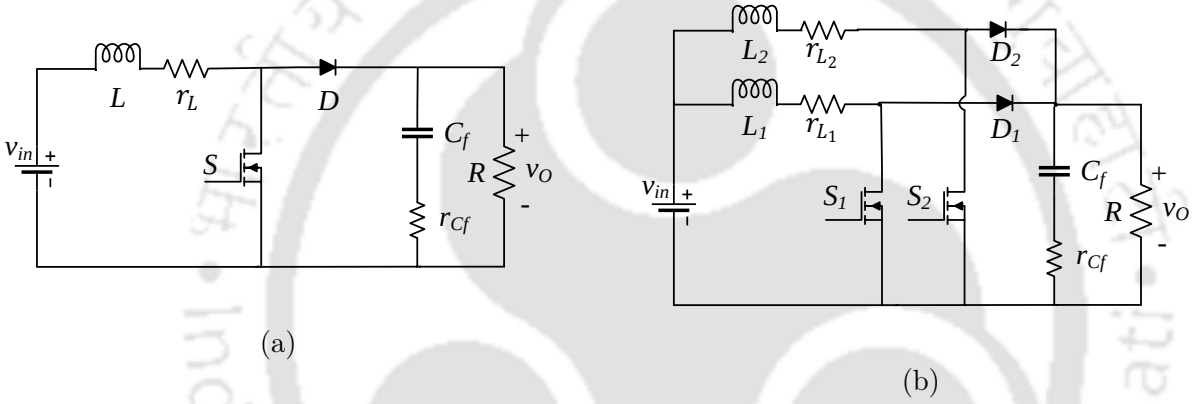


Figure 1.3: Circuit diagram of (a) Conventional boost converter (CBoC), and (b) Conventional interleaved boost converter (CIBoC)

The CBoC can be modified to operate as an interleaved boost converter combining two basic CBoCs in parallel so that the current rating of the components in the conventional interleaved boost converter (CIBoC) can be halved to that of the CBoC as shown in Figure 1.3b. Thus, the manufacturing of the CIBoC is quite economical as compared to other step-up converter topologies [14–16]. Moreover, the input and output current ripples can also be improved when compared with those of the conventional converter [14]. However, the voltage conversion ratio of the CIBoC is the same as the CBoC and the semiconductor devices still suffer high output voltage stress. In the following section, merits and demerits of the existing various DC-DC high step-up/down converters are discussed.

1.1 Literature Survey

The literature survey on existing DC-DC step-up/step-down converters is elaborated under the following five subsections. In the first subsection, various high step-down buck converters are reported. Thereafter, several topologies regarding interleaved buck converters (IBuC) are discussed in the second subsection. Survey on the effect of a coupled inductor in IBuC are presented in the third subsection. This is followed by a survey on high step-up topologies in the fourth subsection. In the last subsection, various high step-up converters with interleaving configurations are presented.

1.1.1 Existing step-down buck converters

For high voltage to very low voltage conversion, a type of switch-capacitor combination is used to enhance the voltage conversion ratio of a buck module in [17] forming a cascaded converter. Though a two-stage cascaded buck converter is a possible solution for high step-down voltage conversion [18], the overall efficiency decreases and the converter unit becomes bulkier. Several attempts to design single-stage buck converter with a larger step-down ratio have been reported. In [19], a buck converter is presented to achieve a wider conversion ratio by using a switched capacitor network. A transformer-less high step-down DC-DC converter is introduced in [20]. However, both the designs use a large number of active and passive components resulting in increased overall cost and size of the converters. A resonant high step-down ratio buck converter is designed by using a coupled inductor and one resonant energy-transferring capacitor in [21] with a very complex topology. In addition, the effect of the coupled inductor on ripple improvement is not discussed. A wider conversion ratio for a bidirectional buck/boost converter is reported in [22] with a large number of active and passive components. A non-isolated buck converter is presented in [23] to achieve a high step-down conversion ratio using a transformer and an energy transferring capacitor; though the switches are subjected to high input voltage stress. Another high step-down converter introduced in [24] has the demerit of a requirement of magnetic cores and components. In addition, the voltage step-down ratio of the converter depends on the turns ratio of a coupled inductor. A buck module with low source current ripple is introduced in [25]. This topology uses several semiconductor devices; however, it could not modify the conversion ratio. To get ultra-high step-down conversion ratio, the

use of a dual-winding or three winding tapped-inductor for buck module is reported in [26–28]. By using the coupled-inductor, the voltage conversion ratio is also modified to achieve high step-down output voltage in [29–31]. But, the voltage conversion ratio depends upon the turns ratio between the inductor windings. Moreover, requirements of active and passive elements are comparatively more in these topologies.

1.1.2 Existing step-down interleaved buck converters

In-spite of using two CBuCs, the voltage conversion ratio of CIBuC is the same as that of the former riddled with problems such as wider duty cycle, high ripples in current, high voltage drop, high on-resistance, high voltage and current stresses, and low efficiency. To deal with these problems, contemporary researches have tried to modify the circuit configuration of CIBuC and the relevant and significant attempts are discussed here. A high step-down ratio IBuC is introduced in [32]. Though the converter achieves larger step-down ratio, a large number of inductors are required that makes the circuit complex, bulky and costlier. An active-clamp IBuC with high step-down conversion ratio is introduced in [33]. Since the requirement of passive elements and active switches are more, it increases the manufacturing cost. In [29], a coupled inductor-based IBuC with high step-down conversion ratio is introduced. Although the voltage across the switches is reduced, the requirements of active switches are more causing an increment in cost and conduction loss. In [34], with an integrated inductor, a study on IBuC is carried out. The voltage conversion ratio of this IBuC is the same as that of CIBuC. At boundary condition, a synchronous IBuC is presented in [35] to achieve high step-down conversion ratio by using the turns ratio of a coupled inductor. The requirements of comparatively more semiconductor devices increase the total switching losses. An IBuC with a single-capacitor turn-off snubber is presented to reduce the switching loss in [36]. All the components are affected by the high-current stress causing more loss. Apart from this, the minimum voltage ratings of all the switches and the diodes of the converter are equal to the input voltage. Moreover, this IBuC operates only when the duty ratio is less than or equal to 0.50. An IBuC with zero current transition is introduced in [37]. The step-down ratio is not improved in this circuit configuration and it operates only when the duty cycle is less than 0.50. For LED drive, an IBuC is presented in [38]. It operates below 0.50 duty cycle and the voltage stresses of the semiconductor devices are equal to the input voltage. In [39], an IBuC

with a forward converter is introduced to achieve higher step-down ratio. The conversion ratio depends on the turns ratio of a transformer. The requirements of active and passive components are more. An IBuC with higher step-down conversion ratio is presented in [40]. This IBuC gains the conversion ratio by a pair of coupled inductors. The requirements of semiconductor devices and magnetizing cores are high. Thus, it increases the cost and size. The topology is complex. With a soft-switching technique, an IBuC is presented in [41]. The voltage conversion ratio depends upon the turns ratio of the transformer and does not achieve a high step-down conversion ratio. In [42], to achieve ultra-high step-down voltage conversion ratio, the tapped-inductor buck converter is designed in dual-phase interleaving configuration. To extend the duty cycle, series capacitors and transformers are applied in four-phase interleaving circuit configuration in [43]. However, both the topologies require a huge number of active and passive elements resulting in larger size and higher manufacturing cost.

1.1.3 Existing step-down interleaved buck converters with coupled inductor

CIBuC consists of two CBuCs in parallel. Thus, an extra inductor is required in the output-end to design CIBuC making the converter bulky. Therefore, these two output-end single inductors of CIBuC can be replaced by a dual-winding coupled inductor [44–48]. Use of coupled inductor in solving the other various issues of CIBuC is also very popular among the contemporary researchers which are discussed herein. To obtain a better transient response, a coupled inductor is used for a two-phase buck module in [49]. Moreover, it shows that strong coupling is more effective at reducing ripple if the proper magnetic topology is used. In [50], a multiphase buck converter with a coupled inductor is introduced. The coupled inductor improves dynamic behaviour and reduces steady-state power loss. A multiphase synchronous buck converter using a symmetrically coupled inductor is presented in [51]. The coupled inductor introduced in this paper improves efficiency and also reduces phase current ripple. In [52], to increase power density and efficiency of IBuC an ultra-thin coupled inductors is presented. To improve the resonant period of an interleaved critical current mode (CRM) bidirectional buck/boost converter, a coupled inductor is used in [53]. The coupled inductor also improves the soft-switching range and energy circulation. Inductor coupling effect in interleaved multiphase DC-DC converters is also demonstrated to avoid early inductor saturation and interference between phases in [54].

In [55], a comprehensive analysis of two-phase interleaved buck and boost converters including an inter-phase transformer/ coupled inductor is carried out in discontinuous conduction mode (DCM). To reduce the resistor and core loss, a compact lateral coupled inductor is designed and used for a two-phase IBuC module in [56]. To achieve high power density and high step-down conversion ratio, an IBuC is designed by a three winding coupled inductor in [47]. A four-phase inverse coupled-inductor is introduced for an interleaved bidirectional DC-DC buck-boost converter to reduce low current ripple and improve efficiency in [57]. A six-phase interleaved topology consisting of a coupled-inductor introduced in [58] utilizes variable coupling coefficient to reduce the ripple. But it does not explain the effect of the variable coupling coefficient of the coupled inductor on the output filter capacitor. At CCM/DCM boundary mode, a zero voltage switching mode synchronous interleaved buck converter is presented in [35]. A coupled inductor is used to improve the conversion ratio. In [59], the turns ratio of a coupled inductor is used to achieve high voltage gain for a bidirectional converter. A bidirectional interleaved DC-DC converter is introduced to achieve high power density and cancel the ripple by using a winding cross-coupled inductor (WCCI) in [60]. But the voltage conversion of this converter depends on the turns ratio of the WCCI. In [61], an interleaved bidirectional buck-boost converter is presented to achieve zero voltage switching (ZVS) by utilizing a coupled inductor with a variable coupling factor. But the semiconductor devices of this converter suffer high voltage stress. This converter also does not explain the effect of the variable coupling factor on the output filter capacitor. Four switches and a pair of coupled inductors are used to achieve high step-up/down conversion ratio for an interleaved bidirectional converter in [62]. This topology does not provide any analysis of the effect of the coupled inductor in improving the ripple. Input and output inductors of an interleaved buck-boost converter are magnetically coupled to improve current ripple, low power density, efficiency and voltage oscillation in [63].

The concept of coupled inductor is implemented successfully for the aforementioned various IBuC topologies to improve transient response efficiency, voltage conversion ratio, the ripple in current and power density, etc. However, there is a lack of proper work addressing any systematic analysis of ripples in output-end inductors for an IBuC. These works also do not provide the impact of the coupling factor of a coupled inductor for reducing the minimum capacitance value of the output filter capacitor.

1.1.4 Existing step-up boost converters

Normally, for low-input voltage to high-output voltage conversion, CBoC is extensively used due to its simple circuit configuration, less control complexity and acceptable efficiency. However, when a low-input to very high-output voltage conversion is required, utilization of CBoC can be disadvantageous as it requires wider duty ratio causing more conduction loss which renders less efficiency [64–67]. Apart from that, CBoC suffers from other issues such as high voltage and current stresses and high ripples in inductor current and output voltage [68–72]. Several techniques are applied to extend the voltage gain and deal with these other issues of CBoC. Some significant and relevant techniques are discussed here. Cascading of two boost converters can be a possible solution for high step-up voltage applications [73–75]. However, it increases the voluminosity and control complexity and deteriorates the overall efficiency of the converter unit [76, 77]. To overcome such problematic solutions, high step-up boost converters based on the coupled inductor can be a simpler and effective replacement [78–82]. Through voltage doubler circuit and coupled inductor, the step-up voltage conversion ratio is enhanced in [83,84]. However, these topologies are complex requiring a large number of active and passive elements. Thus, the power loss increases. Moreover, there are no ripple improvements in the inductor current. A non-isolated DC-DC step-up converter with higher step-up conversion ratio is presented in [85] to achieve low input current ripple using a total of two dual-winding coupled inductors making the converter costly and bulky. To cancel the input current ripple, a boost converter is introduced using a tapped inductor in [86]. But, the step-up ratio of this converter is the same as that of CBoC. Apart from the use of coupled inductor, some other techniques are also used to modify the voltage gain. Some relevant topologies are reported here. Based on the charge pump and boost converter, a high step-up converter is introduced in [87]. It uses two single inductors which are not coupled. Therefore, the voltage gain does not depend upon the turns ratio. A switch-inductor based step-up converter is reported in [88] to achieve high voltage gain employing a large number of active and passive elements. Requirements of a total of four single inductors make the system heavy and costly. Moreover, this work does not provide any clarity on ripple improvement. In [89], a DC-DC boost convert is designed to cancel the input current ripple. However, this converter uses two single inductors and a large number of semiconductor devices.

A high step-up DC-DC converter is presented in [90] [91]. Two single inductors and a diode-

capacitor cell are used to design this converter. The higher step-up ratio helps to reduce ripples in input and inductor current compared to that of CBoC. However, using two single inductors increases the size and cost of the converter. Replacement of these two single inductors by a directly coupled DWCI may further help to reduce the ripples in input current, inductor current and output voltage.

1.1.5 Existing step-up interleaved boost converters

Recently, step-up interleaved boost converters (IBoCs) are introduced based on the voltage doubler and passive snubber circuit [92–94]. The design procedures and implementations of these converters are complex and require a lot of components resulting in high switching losses. Generally, a cascade boost converter can produce a high step-up ratio but the circuit configuration is more complex and not cost-effective [95, 96]. The circuit configuration of the cascaded unit becomes bulky, complex and expensive, and leads to difficulty in manufacturing. A CBoC with a voltage multiplier cell and n-stage inductor capacitor-diode cell is presented to achieve higher step-up voltage gain [97–100]. Herein, VMC consists of diodes, capacitors and an inductor. The use of an extra inductor will increase the size and cost. Using coupled inductors, IBoCs produce a high step-up conversion ratio [75, 101–105]. The step-up voltage conversion ratios of these IBoCs depend on the turns ratio of the coupled inductor. However, a large number of coupled inductors increases the cost and complexity of these step-up IBoCs.

Transformers and active clamp circuits are also used to modify the step-up conversion ratio of IBoC [106]. Generally, higher number of magnetic cores makes the circuit bulkier and costlier. A zero current transition IBoC is presented [107]. This converter does not improve the voltage stress of the semiconductor devices. The topology is not cost-effective. An IBoC with one auxiliary switch is introduced [108]. But the voltage stress of the semiconductor devices is equal to the output voltage. An IBoC with zero current switching is presented [109]. The requirements of magnetics and semiconductor devices to design this converter are high which increase the size and cost. To achieve higher step voltage conversion ratio, a DC-DC converter is introduced using switch-capacitor cell to lower voltage stresses on the capacitor [110–113].

1.2 Motivation for the Thesis

From the above literature survey on existing various DC-DC step-up/down converters, the followings are found.

(i) CBuCs can be made to yield very low output voltage by operating at an extremely small duty cycle which leads to high power losses and low overall efficiency. Besides, it results in high ripple in inductor current as well as in output voltage which are not desirable; therefore achieving high step-down conversion ratio with lower ripple values is a problem worth exploring. Apart from CBuC, it is also seen from the other existing high step-up topologies that in-spite of providing high step-down voltage conversion ratio, voltage and current stresses of the semiconductor devices are high. Moreover, the ripple in inductor current and output voltage is also high in these existing high step-down topologies.

Therefore, a buck converter is required to be designed for - (a) a high step-down conversion ratio, (b) reduced ripples in input current, inductor current and output voltage, and (c) less current and voltage stresses in the semiconductor devices.

(ii) The maximum current ratings of the semiconductor devices and inductors in CIBuC are half of CBuC. However, in CIBuC, all the active devices are affected by high input voltage, which increases the voltage ratings of the devices. The high voltage rated devices come with a lot of disadvantages like large voltage drop, high on-resistance and high cost. Apart from these drawbacks, CIBuC requires a very small duty cycle when very high input to very low output voltage conversion is sought. From the literature survey, it is seen that there are some interleaving buck topologies which have modified step-down conversion ratio. However, these topologies are complex and costly. In these topologies some of which require a transformer or a coupled inductor to enhance the voltage conversion ratio, the constituent semiconductor devices are subjected to high voltage stresses. Moreover, many of these topologies are inoperable even over the entire duty ratio range $0 < \alpha \leq 1$ and require more number of active and passive elements.

Therefore, to deal with the problem of the small-duty cycle of CIBuC in high-input to low-output voltage applications, a high step-down duty ratio interleaved buck converter is required to be designed so that the proposed interleaved buck converter can produce a low-output voltage at sufficiently large duty ratio apart from rendering it operable over

the entire duty ratio range $0 < \alpha \leq 1$. While fulfilling these main motives, the proposed topology should be simpler with high efficiency and should have lower voltage stresses on the semiconductor devices.

(iii) Although CIBuC has benefits of high power capability, modularity, and improved reliability, it has few drawbacks. The interleaved converters achieve better performance by using an extra inductor, a power switch and a diode. Since the inductor is the heaviest and largest component in a power converter, the overall converter size becomes bulkier. Instead of using a number of single inductors, a single coupled inductor is a preferable solution because of its less core loss, transient improvement, and reduction of ripple in current [32, 46, 48, 114, 115]. Apart from CIBuC topology, there are other reported interleaving topologies which use a coupled inductor to improve ripple in inductor currents though they are complex and employ high number of active and passive elements.

The concept of coupled inductor is implemented successfully for the aforementioned various interleaved buck topologies to improve transient response, voltage conversion ratio, ripple in current and power density, etc. However, there is a lack of proper work in the existing literature on the systematic analysis of ripple in output-end inductors for an interleaved buck converter, nor do these works discuss the impact of the coupling factor of a coupled inductor for reducing the minimum capacitance value of the output filter capacitor.

(iv) Works on topologies regarding high step-up conversion may be found in abundance in the contemporary literature. For very low voltage to high voltage applications, CBoC is not suitable as it requires a large duty ratio causing more conduction loss affecting the overall efficiency. High ripple in inductor current and output voltage are other disadvantages of these converters. In case of IBoC, the current rating of the components is half of that of CBoC though the voltage conversion ratio is the same in both the cases. However, all these topologies expose the semiconductor devices to high output voltage stresses. It is worth noting that even though CBoCs and CIBoCs were not so expensive in past, recent trends show an increasing tendency in terms of both cost and complexity in these converters capable of addressing all the above-mentioned shortcomings.

Therefore, modifying step-up conversion ratio with reduced voltage stresses on constituent

semiconductor devices, cost, complexity, and ripples in inductor current and output voltage is a challenging problem in designing conventional and interleaved boost converters.

1.3 Contribution of the Thesis

Motivated by the aforementioned literature survey on the various step-up/down topologies, the DC-DC converters with improved step-up/down conversion ratio are proposed and implemented in this thesis. While fulfilling these main objectives, the proposed converters also demonstrate significant improvements in other features which are highlighted below under corresponding proposed converters.

(i) ***A high step-down buck converter (HSDBuC)***: The voltage conversion ratio of CBuC is modified by using a switch-capacitor cell to achieve the following:

- a larger step-down conversion ratio to avoid the narrow duty cycle for high voltage to very low voltage conversion
- a step-down conversion ratio which is independent of the effect of the turns ratio of coupled inductor or transformer
- reduced ripples in input current, inductor current and output voltage
- reduced voltage and current stresses in the semiconductor devices
- better efficiency
- two single inductors of HSDBuC are further coupled directly for lower ripple in input current, inductor current and output voltage.

(ii) ***A high step-down interleaved buck converter (HSDIBuC)***: The voltage conversion ratio of the CIBuC is modified by using a switch-capacitor cell to achieve the following:

- a high step-down voltage conversion ratio to produce a low-output voltage at sufficiently large duty ratio
- reduced voltage and current stresses of the switches and diodes
- a range of operation below and above 0.50 duty ratio
- reduced ripples in input, inductor current and output voltage using a dual-winding coupled inductor (DWCI)

- a lower value of the output filter capacitor by using DWCI
- better dynamic response
- fewer components compared to the existing topologies
- simpler interleaving topology compared to the existing topologies
- improved efficiency.

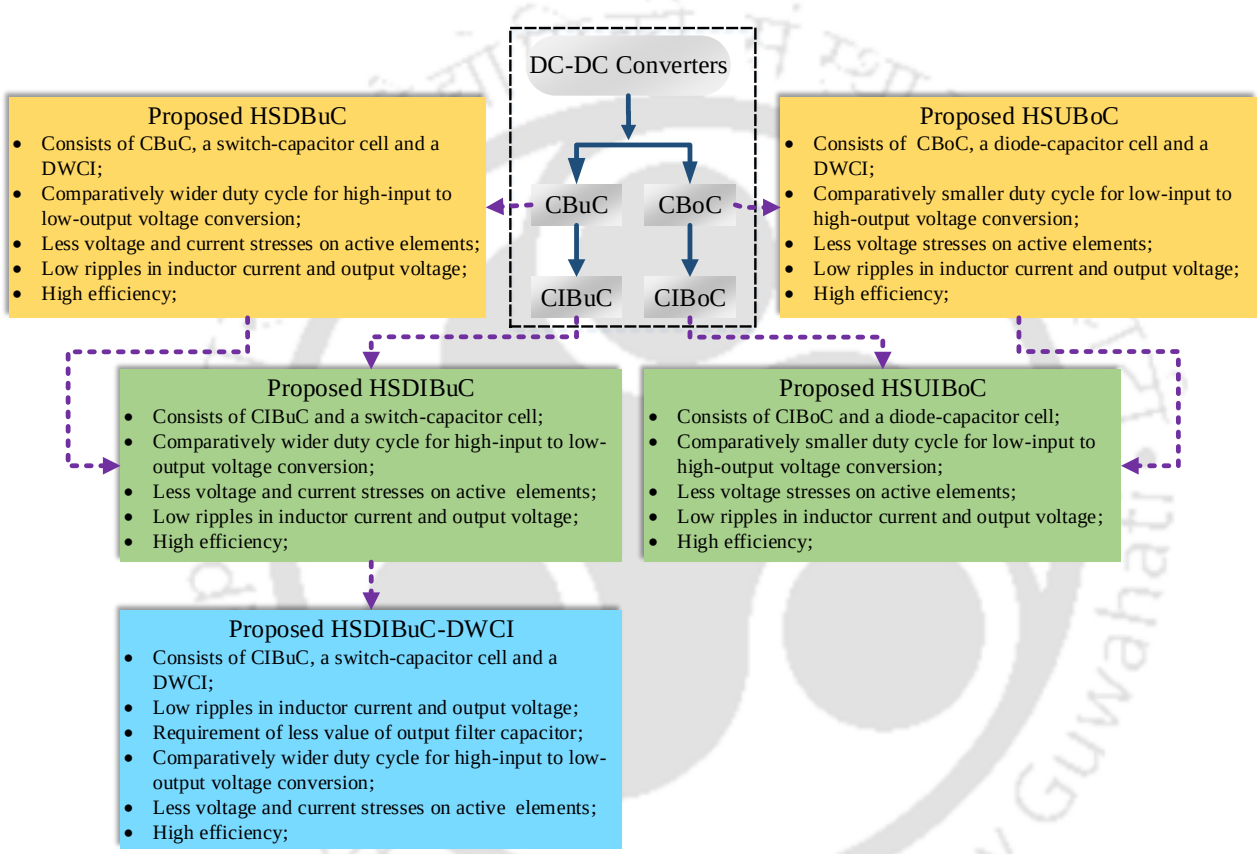


Figure 1.4: Flow chart of the development of proposed converters

(iii) ***A high step-up boost converter (HSUBoC)***: CBoC topology is modified by using a diode-capacitor cell and a coupled inductor to achieve the following:

- improved voltage conversion ratio to produce a high-output voltage at comparatively smaller duty ratio
- reduced voltage and current stresses of the semiconductor devices

- reduced ripples in input, inductor current and output voltage by using a coupled inductor
- improved efficiency.

(iv) ***A high step-up interleaved boost converter (HSUIBoC)***: The voltage conversion ratio of CIBoC is modified using a diode-capacitor cell to achieve the following:

- a high step-up conversion ratio by using a cross-connected diode-capacitor cell
- a conversion ratio independent of the turns ratio of a transformer or a coupled inductor
- reduced ripple in input current
- better efficiency
- reduced voltage stresses of the semiconductor devices
- simple circuit configuration compared to the existing topologies.

A tree-diagram of DC-DC converters highlighting the contribution of the thesis is shown in Figure 1.4. The conventional converters of Figure 1.1 are shown within the dotted rectangular box. The contribution of the author are shown within the coloured boxes.

1.4 Organization of the Thesis

Having laid the foundation of the thesis in the introduction, a brief organization is given below showing the glimpse of the subsequent chapters.

Chapter 2 proposes a high step-down buck converter (HSDBuC). The circuit topology of the high step-down interleaved buck converter (HSDIBuC) along with detailed analysis is provided in Chapter 3. Thereafter, the proposed high step-down interleaved buck converter with a dual-winding coupled inductor (HSDIBuC-DWCI) is presented in Chapter 4. In Chapter 5, a high step-up boost converter (HSUBoC) with a coupled inductor is proposed. After that, the proposed high step-up boost converter with interleaving configuration, namely high step-up interleaved boost converter (HSUIBoC) is discussed in Chapter 6. Section 7 concludes the works and provides future scope of the thesis.

2

High Step-down Buck Converter

This chapter presents a buck converter with a large step-down voltage conversion ratio, reduced ripple in inductor current and low semiconductor voltage stress. The proposed converter produces a lower output voltage at a sufficiently higher duty ratio compared to the conventional buck converter. The step-down voltage conversion ratio is modified by a series-parallel transition of two identical capacitors of a switch-capacitor cell. Two parallelly placed switches and two cross-connected identical capacitors are utilized to design the cell. An extra inductor is placed at the input side to oppose the sudden change in input current due to the series-parallel transition of the two capacitors. Therefore, two inductors are required to design the converter. These two inductors are coupled directly. The modified voltage conversion ratio reduces the ripple in inductor currents and output voltage. Direct coupling between the two inductors helps to further reduce the ripple in inductor currents and output voltage. The analysis of small-signal modelling is carried out and a voltage mode PI-controller is designed to enable the closed-loop operation. Finally, the proposed converter is implemented in hardware and the performance of the proposed converter is verified experimentally.

2.1 Introduction

Conventional buck converter (CBuC) requires a very narrow duty cycle for the high-input to very low-output voltage conversion which causes high power losses and overall low-efficiency. Besides, it results in high ripple in inductor current as well as in output voltage which is not desirable; therefore achieving a high step-down conversion ratio with lower ripple values is a notable development. A high step-down buck converter (HSDBuC) with a dual winding coupled inductor (DWCI) is proposed in this chapter. The proposed HSDBuC uses a switch-capacitor cell to achieve a larger step-down conversion ratio as well as the following.

- a larger step-down conversion ratio to avoid the narrow duty cycle for high voltage to very low voltage conversion;
- reduction of ripples in input current, inductor current and output voltage;
- reduction of voltage stresses in the semiconductor devices;
- improvement of efficiency;

The conversion ratio of the proposed HSDBuC is independent of the turns ratio of a coupled inductor or a transformer. The modified step-down conversion ratio reduces the ripple in input current and output voltage. But the use of a coupled inductor improves the ripple even more as the coils of the coupled inductor are directly coupled.

The chapter is organized as follows. Section 2.2 explains the operation principle. Ripple currents in inductor branches and input current are discussed in Sections 2.3 and 2.4 respectively. Section 2.5 discusses the minimum inductance value of the coupled inductor. The output voltage ripple and CCM/DCM boundary load conditions are determined in Sections 2.6 and 2.7 respectively. The voltage and current stresses are provided in Section 2.8. Section 2.9 discusses power losses and efficiency. Small-signal modelling and control scheme are described in Sections 2.10 and 2.11 respectively. Section 2.12 presents the simulation work. Experimental set-up and results are provided in Section 2.13. Finally, Section 2.14 gives a brief summary of the chapter.

2.2 Operating Principle

The proposed high step-down buck converter (HSDBuC), shown in Figure 2.1 combines a dual-winding coupled inductor (DWCI) and a switch-capacitor cell operating in continuous conduction mode (CCM). The input voltage v_{in} is applied to the L_i-winding of the coupled inductor. The r_{L_i} is the parasitic of the L_i-winding. Thereafter, a switch-capacitor cell is used and it consists of two switches S_1 and S_2 placed in parallel and two cross-connected identical capacitors C_1 and C_2.

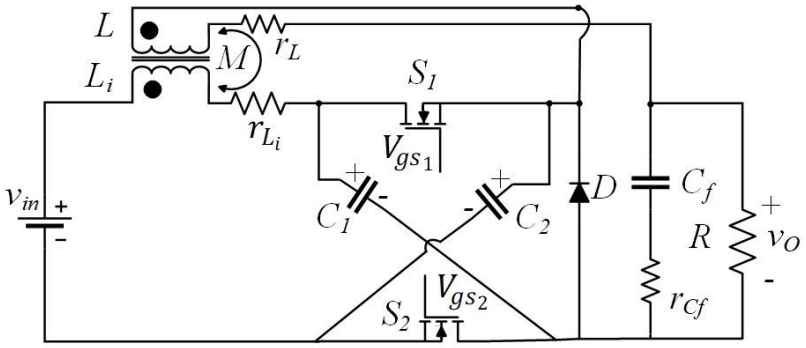


Figure 2.1: The proposed DC-DC high step-down buck converter (HSDBuC) with DWCI

The diode D is placed parallel to the switch-capacitor cell followed by the L-winding of the coupled inductor. Both the switches turn ON and OFF simultaneously. When both S_1 and S_2 are ON, the diode D is in reverse bias. Therefore, the two identical capacitors are parallel to each other and discharge their energy to the load side. When the switches are OFF simultaneously, the diode D is in forward bias because of which the two identical capacitors charge in series with the L_i-winding. Thus, the proposed converter produces lower output voltage at a sufficiently large duty cycle compared to the conventional buck converter. The modified conversion ratio helps to reduce ripple in input current, inductor current and in output voltage. To oppose the sudden change in the input current due to the series-parallel transition of the two identical capacitors, the L_i-winding is placed at the input side. Therefore, two inductors are required to design the proposed converter. These two inductors are coupled directly to reduce the ripple in input current, inductor current and in output voltage. The L_i- and L represent the two windings of the coupled inductor. C_f represents the output capacitor and r_{C_f} is the parasitic. v_o is the output voltage at output load resistance R. The r_L and r_{L_i} are negligible as $r_L, r_{L_i} \ll R$.

2.2.1 Generalized equations of coupled inductor

The schematic diagram of the directly-coupled dual-winding coupled inductor (DWCI) is shown in Figure 2.2. Two U/C-type cores are magnetically coupled.

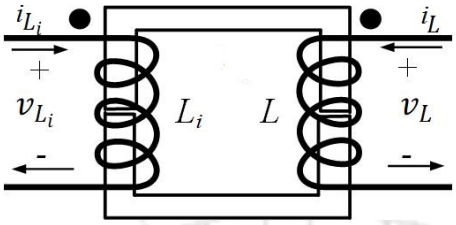


Figure 2.2: Schematic representation of the dual-winding coupled inductor (DWCI)

The generalized inductive voltages v_{L_i} and v_L across the L_i and L windings of the coupled inductor respectively are as follows.

$$v_{L_i} = L_i \frac{di_{L_i}}{dt} \pm M \frac{di_L}{dt} \tag{2.1}$$

$$v_L = L \frac{di_L}{dt} \pm M \frac{di_{L_i}}{dt} \tag{2.2}$$

Here i_{L_i} and i_L represent the currents flowing through the L_i and L windings respectively. Since the two windings of the coupled inductor have identical inductances, $L = L_i$. The mutual inductance, M, is defined as $M = k\sqrt{L_i L}$ where k is the coupling factor. The windings will be directly coupled or inversely coupled depending upon whether $k \in [0, 1]$ or $k \in [0, -1]$ respectively. The leakage inductance, L_r, is defined by $L_r = L(1 - k^2)$. The two inductor branches are coupled directly to reduce the ripple in current and output voltage for the proposed converter. Therefore, over a time period of T_s, Equations (2.1) and (2.2) can be expressed as

$$\int_0^{T_s} di_{L_i} = \frac{v_{L_i}}{(1-k^2)L_i} \int_0^{T_s} dt - \frac{v_L k \sqrt{\frac{L_i}{L}}}{(1-k^2)L_i} \int_0^{T_s} dt \tag{2.3}$$

$$\int_0^{T_s} di_L = \frac{v_L}{(1-k^2)L} \int_0^{T_s} dt - \frac{v_{L_i} k \sqrt{\frac{L}{L_i}}}{(1-k^2)L} \int_0^{T_s} dt \tag{2.4}$$

2.2.2 Switching modes

The converter, whose duty ratio is denoted by α, has one ON-state and one OFF-state, as both the switches S_1 and S_2 turn ON and OFF simultaneously over a time period of T_s as shown

in Figure 2.3. Here, $v_{S_{1,2}}$ represents drain to source voltage i.e. voltage stress for the switches, whereas v_D is the diode voltage stress. In the duration $0 < t < \alpha T_s$, both the inductor currents, i_{L_i} through L_i-winding and i_L through L-winding increase. In the next duration, $\alpha T_s < t < T_s$, both the inductor currents decrease. The switching operations are described below.

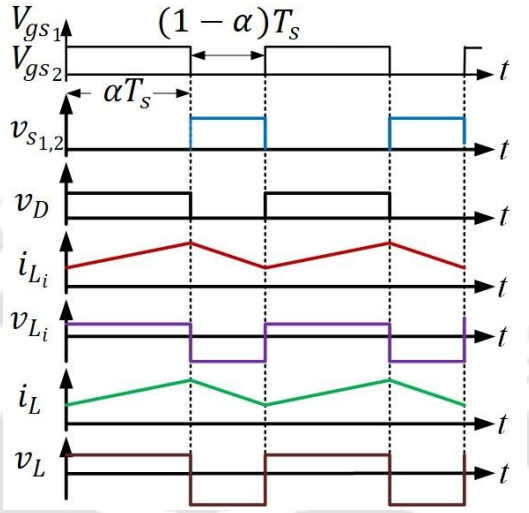


Figure 2.3: Idealized waveform of the proposed HSDBuC

2.2.2.1 ON-state $(0 < t \leq \alpha T_s)$ of HSDBuC

In this switching period, the S_1 and S_2 are simultaneously ON as shown in Figure 2.4. The diode D is in reverse bias. Therefore, the two identical capacitors are parallel to each other and the voltage across the capacitors is v_C.

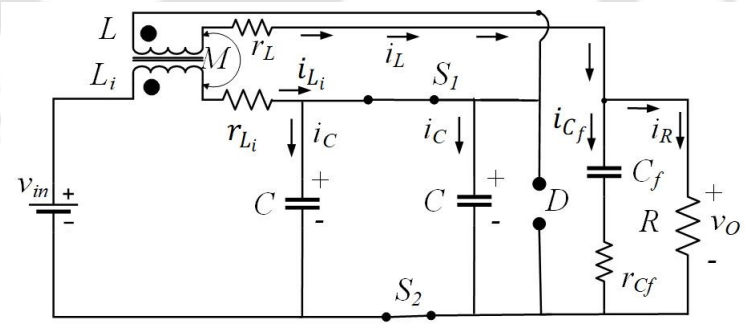


Figure 2.4: The circuit configuration of HSDBuC in ON-state

The voltage v_{L_i} across the L_i-winding and v_L across the L-winding are respectively as follows.

$$v_{L_i} = L_i \frac{di_{L_i}}{dt} + M \frac{di_L}{dt} = v_{in} - v_C \tag{2.5}$$

$$v_L = L \frac{di_L}{dt} + M \frac{di_{L_i}}{dt} = v_C - v_{C_f} - r_{c_f} i_{C_f} \tag{2.6}$$

where v_{C_f} is the voltage across the output capacitor C_f and i_{C_f} is the current flowing through C_f. The output voltage v_o is as follows.

$$v_o = v_{C_f} + r_{C_f} i_{C_f} = R i_R \tag{2.7}$$

where i_R is the current flowing through load R. The current through the identical capacitors, i_C, is provided as

$$2i_C(t) = i_{L_i}(t) - i_L(t) \tag{2.8}$$

The output load current is

$$i_R(t) = i_L(t) - i_{C_f}(t) \tag{2.9}$$

The state vectors are defined as $\mathbf{x}(t) = [i_{L_i}\ v_C\ i_L\ v_{C_f}]^T$ and the output vector as $\mathbf{y}(t) = v_o$. The state-space representation of the ON-state is as follows.

$$\dot{\mathbf{x}}(t) = \mathbf{A_1}\mathbf{x}(t) + \mathbf{B_1} v_{in}(t)$$

$$= \begin{bmatrix} 0 & \frac{-(M+L)}{LL_i - M^2} & \frac{MRr_{C_f}}{(LL_i - M^2)(R + r_{C_f})} & \frac{MR}{(LL_i - M^2)(R + r_{C_f})} \\ \frac{1}{2C} & 0 & \frac{-1}{2C} & 0 \\ 0 & \frac{L_i + M}{LL_i - M^2} & \frac{-L_i R r_{C_f}}{(LL_i - M^2)(R + r_{C_f})} & \frac{-L_i R}{(LL_i - M^2)(R + r_{C_f})} \\ 0 & 0 & \frac{R}{C_f(R + r_{C_f})} & \frac{-1}{RC_f(R + r_{C_f})} \end{bmatrix} \mathbf{x}(t) + \begin{bmatrix} \frac{L}{LL_i - M^2} \\ 0 \\ \frac{-M}{LL_i - M^2} \\ 0 \end{bmatrix} v_{in}(t) \tag{2.10}$$

$$\mathbf{y}(t) = \mathbf{Z_1}\mathbf{x}(t) = \begin{bmatrix} 0 & 0 & \frac{Rr_{C_f}}{R + r_{C_f}} & \frac{R}{R + r_{C_f}} \end{bmatrix} \mathbf{x}(t) \tag{2.11}$$

2.2.2.2 OFF-state ($\alpha T_s < t \leq T_s$) of HSDBuC

In this subsequent interval, both the switches are OFF and the diode D is in forward bias as shown in Figure 2.5. Therefore, these identical capacitors are in series with L_i-winding. The resultant voltage across the two capacitors becomes $v_C + v_C = 2v_C$. The voltage and current equations are as follows.

$$v_{L_i} = L_i \frac{di_{L_i}}{dt} + M \frac{di_L}{dt} = v_{in} - 2v_C \tag{2.12}$$

$$v_L = L\frac{di_L}{dt} + M\frac{di_{L_i}}{dt} = -v_{C_f} - r_{C_f} i_{C_f} \tag{2.13}$$

$$i_C(t) = i_{L_i}(t) \tag{2.14}$$

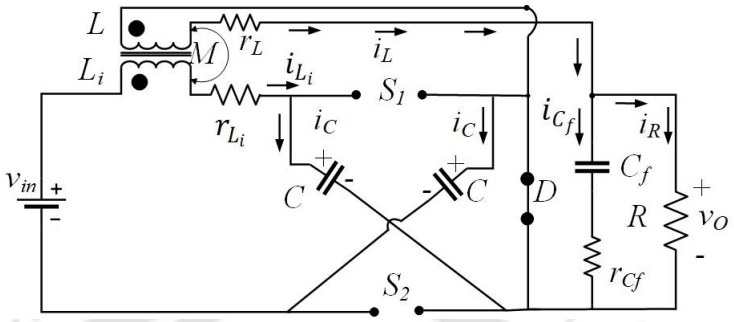


Figure 2.5: The circuit configuration of HSDBuC in OFF-state

The output voltage and load current are given in Equations (2.7) and (2.9) respectively. The state-space representation of the OFF-state is as follows.

$$\dot{\mathbf{x}}(t) = \mathbf{A_2}\mathbf{x}(t) + \mathbf{B_2}v_{in}(t)$$

$$= \begin{bmatrix} 0 & \frac{-2L}{LL_i - M^2} & \frac{MRr_{C_f}}{(LL_i - M^2)(R + r_{C_f})} & \frac{MR}{(LL_i - M^2)(R + r_{C_f})} \\ \frac{1}{C} & 0 & 0 & 0 \\ 0 & \frac{2M}{LL_i - M^2} & \frac{-L_i R r_{C_f}}{(LL_i - M^2)(R + r_{C_f})} & \frac{-L_i R}{(LL_i - M^2)(R + r_{C_f})} \\ 0 & 0 & \frac{R}{C_f(R + r_{C_f})} & \frac{-1}{RC_f(R + r_{C_f})} \end{bmatrix} \mathbf{x}(t) + \begin{bmatrix} \frac{L}{LL_i - M^2} \\ 0 \\ \frac{-M}{LL_i - M^2} \\ 0 \end{bmatrix} v_{in}(t) \tag{2.15}$$

$$\mathbf{y}(t) = \mathbf{Z_2}\mathbf{x}(t) = \begin{bmatrix} 0 & 0 & \frac{Rr_{C_f}}{R + r_{C_f}} & \frac{R}{R + r_{C_f}} \end{bmatrix} \mathbf{x}(t) \tag{2.16}$$

2.2.3 Voltage conversion ratio

At ideal case, by using Equations (2.5) and (2.12), the volt-second balance (VSB) equation of the L_i-winding is expressed as follows.

$$(v_{in} - v_C)\alpha + (v_{in} - 2v_C)(1 - \alpha) = 0$$

$$\frac{v_C}{v_{in}} = \frac{1}{2 - \alpha} \tag{2.17}$$

In the next stage, by using Equations (2.6) and (2.13), the VSB equation of the L-winding is written as

$$(v_C - v_o)\alpha - v_o(1-\alpha) = 0$$
$$v_o = \alpha v_C \tag{2.18}$$

Therefore, from Equations (2.17) and (2.18), the voltage conversion ratio of the proposed converter is derived as

$$\frac{v_o}{v_{in}} = \frac{\alpha}{2-\alpha} \tag{2.19}$$

The voltage conversion ratio of CBuC is $v_o/v_{in} = \alpha$. Therefore, the proposed HSDBuC produces less output voltage at the same duty ratio as compared to CBuC.

2.3 Ripple Current in Inductor Branches

By considering $L = L_i$, the ripple currents in L and L_i windings of the coupled inductor are determined. The effect of coupling factor k on ripple reduction is analysed.

2.3.1 Ripple current in L_i-winding

During the interval $(0 < t < \alpha T_s)$, the instantaneous inductor current $i_{L_i}(\alpha T_s)$ is derived by substituting Equations (2.5) and (2.6) into (2.3) as follows.

$$i_{L_i}(\alpha T_s) = \frac{(1-\alpha)T_s\alpha v_{in}}{(2-\alpha)(1+k)L_i} + i_{L_i}(0) \tag{2.20}$$

In the subsequent interval $(\alpha T_s < t < T_s)$, the instantaneous current $i_{L_i}(T_s)$ is determined by substituting Equations (2.12) and (2.13) into (2.3) as follows.

$$i_{L_i}(T_s) = i_{L_i}(\alpha T_s) - \frac{(1-\alpha)T_s\alpha v_{in}}{(2-\alpha)(1+k)L_i} \tag{2.21}$$

Therefore, the ripple current of L_i-winding is

$$\Delta i_{L_i} = i_{L_i}(\alpha T_s) - i_{L_i}(0) = \frac{(1-\alpha)\alpha T_s}{(2-\alpha)(1+k)L_i} v_{in} = \frac{(1-\alpha)T_s}{(1+k)L_i} v_o \tag{2.22}$$

2.3.2 Ripple current in L-winding

In the duration $(0 < t < \alpha T_s)$, the instantaneous current $i_L(\alpha T_s)$ is determined by substituting Equations (2.5) and (2.6) into (2.4) as follows.

$$i_L(\alpha T_s) = \frac{(1-\alpha)T_s \alpha v_{in}}{(2-\alpha)(1+k)L} + i_L(0) \tag{2.23}$$

In the next switching period $(\alpha T_s < t < T_s)$, by substituting Equations (2.12) and (2.13) into (2.4), the instantaneous current $i_L(T_s)$ is derived as

$$i_L(T_s) = i_L(\alpha T_s) - \frac{(1-\alpha)T_s \alpha v_{in}}{(2-\alpha)(1+k)L} \tag{2.24}$$

Therefore, the ripple in inductor current of L-winding is

$$\Delta i_L = i_L(\alpha T_s) - i_L(0) = \frac{(1-\alpha)\alpha T_s}{(2-\alpha)(1+k)L} v_{in} = \frac{(1-\alpha)T_s}{(1+k)L} v_o \tag{2.25}$$

2.4 Ripple in Input Current

The duty ratio and ripple in input current of CBuC are considered as α_b and Δi_b. The input ripple current of CBuC is as follows [116].

$$\Delta i_b = \frac{(1-\alpha_b)T_s}{L} v_o \tag{2.26}$$

The input ripple current (Δi_{in}) of the proposed HSDBuC is

$$\Delta i_{in} = \Delta i_{L_i} = \frac{(1-\alpha)T_s}{(1+k)L_i} v_o \tag{2.27}$$

While both converters have the same input and output voltages, the relation between two duty ratios is expressed as

$$\alpha = \frac{2\alpha_b}{1+\alpha_b} \tag{2.28}$$

Considering that both the converters have the same inductance value ($L = L_i$), the relation between Δi_b and Δi_{in} is as follows.

$$\frac{\Delta i_{in}}{\Delta i_b} = \frac{(1-\alpha)}{(1+k)(1-\alpha_b)} \tag{2.29}$$

Substituting the Equations (2.28) into (2.29), the following relation is obtained.

$$\frac{\Delta i_{in}}{\Delta i_b} = \frac{1}{(1+k)(1+\alpha_b)} \text{where } k \in [0,1] \tag{2.30}$$

Therefore, from the Equation (2.30), it can be said that the proposed HSDBuC has less input ripple current than the CBuC. The use of coupled inductor causes further ripple improvement in input current as shown in Equation (2.30).

2.5 Minimum Inductance Value of Coupled Inductor

The average input current i_{in} is determined by using Equation (2.22) as follows.

$$i_{in} = \frac{\Delta i_{L_i}}{2} = \frac{(1-\alpha)T_s}{2(1+k)L_i} v_o \tag{2.31}$$

The output current i_o is the same as the load current i_R. Now, at lossless condition $v_{in} i_{in} = v_o i_o$, the input current can be written by using Equation (2.19) as

$$i_{in} = i_o \frac{\alpha}{2-\alpha} \tag{2.32}$$

Therefore, by equating Equations (2.31) and (2.32), for a given load R, we get

$$R = \frac{v_o}{i_o} = \frac{2L_i\alpha(1+k)}{(2-\alpha)(1-\alpha)T_s} \tag{2.33}$$

Thus, the minimum inductance value can be written as

$$min\{L_i\} = \frac{(2-\alpha)(1-\alpha)T_s R}{2\alpha(1+k)} \tag{2.34}$$

Both the windings of the coupled inductor are considered to have equal inductance value ($L_i = L$).

2.6 Ripple in Output Voltage

In every cycle T_s, the output filter capacitor stores charge and the maximum increment, (ΔQ), of the charge is calculated as follows.

$$\Delta Q = \frac{\frac{T_s}{2}\frac{\Delta i_L}{2}}{2} = \frac{\Delta i_L T_s}{8} \tag{2.35}$$

Therefore, the peak to peak ripple voltage, Δv_o, in the proposed converter is given by

$$\Delta v_o = \frac{\Delta Q}{C_f} = \frac{(1-\alpha){T_s}^2 \alpha v_{in}}{8(1+k)(2-\alpha)LC_f} \tag{2.36}$$

The output ripple voltage of the CBuC is $\Delta v_o = \frac{\Delta Q}{C_f} = \frac{(1-\alpha){T_s}^2}{8LC_f}\alpha v_{in}$. In Figure 2.6, the ripple Δi_L of the proposed HSDBuC for different values of coupling factor k is compared with that of CBuC for the same input voltage. It is observed from the figure that the proposed HSDBuC has less ripple than CBuC in the entire range of α. As expected, the ripple decreases with increase in coupling factor. If the proposed converter utilizes two independent inductors instead of a coupled inductor, i.e. $k = 0$, the proposed HSDBuC still offers less ripple than CBuC.

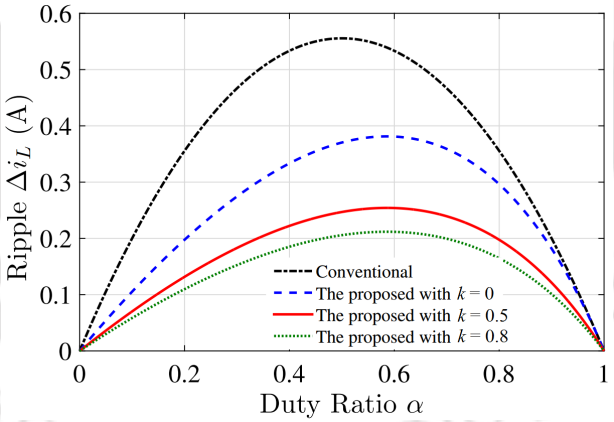


Figure 2.6: Plot of ripple in i_L versus duty ratio α at different values of k for equal v_{in}

2.7 CCM/DCM Boundary Load Condition

In this section, the load value at the boundary between the continuous conduction mode (CCM) and discontinuous conduction mode (DCM) is derived. The average input current (I_{in}) is the same as the current through the L_i-winding and calculated by using Equations (2.20)

and (2.21) as

$$I_{in} = \frac{i_{L_i}(0) + i_{L_i}(\alpha T_s)+}{2}\alpha + \frac{i_{L_i}(\alpha T_s) + i_{L_i}(T_s)}{2}(1-\alpha)$$
$$= \frac{(1-\alpha)T_s v_o}{2(1+k)L_i} + i_{L_i}(0) \tag{2.37}$$

At the boundary condition ($i_{L_i}(0) = i_{L_i}(T_s) = 0$),

$$I_{in} = \frac{(1-\alpha)v_o}{2(1+k)L_i f_s} \tag{2.38}$$

The average input current can be expressed by $I_{in} = \frac{\alpha}{2-\alpha} i_o$. Therefore, by substituting $I_{in} = \frac{\alpha}{2-\alpha} i_o$ into Equation (2.38), the boundary load R_{LB} is derived as

$$R_{LB} = \frac{v_o}{i_o} = \frac{2(1+k)L_i f_s \alpha}{(1-\alpha)(2-\alpha)} \tag{2.39}$$

The plot of normalized boundary load $R_{LB}/(2(1+k)L_i f_s)$ as a function of duty ratio α for the proposed buck converter is shown in Figure 2.7.

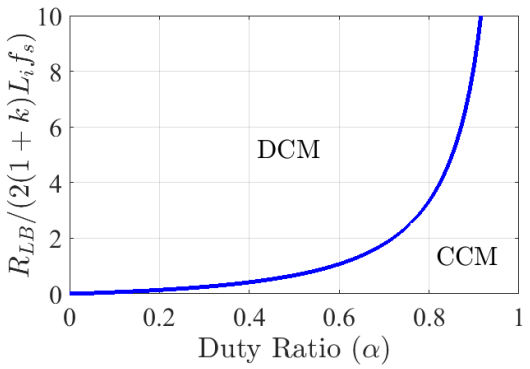


Figure 2.7: Plot of normalized load resistance of HSDBuC at CCM/DCM boundary

2.8 Voltage and Current Stresses

By neglecting the ripple in capacitor voltages, the voltage stresses of the switches and diode are determined. The switching voltage stresses v_{S_1} and v_{S_2} respectively of the switches S_1 and S_2 are provided as follows.

$$v_S = v_{S_1} = v_{S_2} = v_C = \frac{v_{in}}{2-\alpha} \tag{2.40}$$

The diode voltage stress v_D is as follows.

$$v_D = v_C = \frac{v_{in}}{2-\alpha} \tag{2.41}$$

The stresses of the switches and diode due to the current flow is determined by neglecting the ripple in inductor current. The approximation of the maximum switching current and diode current are carried out as

$$i_{S_1} = i_{S_2} = \begin{cases} i_o, & \text{for } 0 < t \leq \alpha T_s \\ 0, & \text{for } \alpha T_s < t \leq T_s \end{cases} \tag{2.42}$$

$$i_D = \begin{cases} 0, & \text{for } 0 < t \leq \alpha T_s \\ i_o, & \text{for } \alpha T_s < t \leq T_s \end{cases} \tag{2.43}$$

where i_o is the output load current. By using Equation (2.25), the maximum current stresses of the switches ($I_{S_{max}}$) and the diode current stress ($I_{D_{max}}$) are determined as follows.

$$I_{S_{max}} = I_{D_{max}} = i_o + \frac{\Delta i_L}{2} = i_o + \frac{(1-\alpha)T_s \alpha v_{in}}{2(1+k)(2-\alpha)L} \tag{2.44}$$

$I_{S_{1rms}}$ and $I_{S_{2rms}}$ are the root mean square (rms) currents flowing through the switches S_1 and S_2 respectively and are as follows.

$$I_{S_{1rms}} = I_{S_{2rms}} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_{S_1}^2 dt} = i_o\sqrt{\alpha} \tag{2.45}$$

The rms current $I_{D_{rms}}$ flowing through the diode is

$$I_{D_{rms}} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_D^2 dt} = i_o\sqrt{1-\alpha} \tag{2.46}$$

The average current, I_D, flowing through the diode is

$$I_D = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_D dt} = i_o(1-\alpha) \tag{2.47}$$

In Table 2.1, the ripple currents and output ripple voltage of the proposed HSDBuC are compared with CBuC for the same input and output voltages.

$$P_{r_{on}} = 2r_{DS(on)}\alpha i_o^2 = 2r_{DS(on)}\alpha\frac{P_o}{R} \tag{2.48}$$

Table 2.1: Comparison of ripple between the proposed HSDBuC and CBuC

Parameter	CBuC	Compare	Proposed HSDBuC
$\frac{v_o}{v_{in}}$	α	$>$	$\frac{\alpha}{2-\alpha}$
Δi_{in}	$\frac{(1-\alpha)T_s\alpha v_{in}}{L}$	$>$	$\frac{(1-\alpha)T_s\alpha v_{in}}{(1+k)(2-\alpha)L_i}$
Δi_L	$\frac{(1-\alpha)T_s\alpha v_{in}}{L}$	$>$	$\frac{(1-\alpha)T_s\alpha v_{in}}{(1+k)(2-\alpha)L}$
Δv_o	$\frac{(1-\alpha){T_s}^2\alpha v_{in}}{8LC_f}$	$>$	$\frac{(1-\alpha){T_s}^2\alpha v_{in}}{8(1+k)(2-\alpha)LC_f}$
v_s	v_{in}	$>$	$\frac{v_{in}}{2-\alpha}$
v_D	v_{in}	$>$	$\frac{v_{in}}{2-\alpha}$
I_{Smax}	$i_o + \frac{(1-\alpha)T_s\alpha v_{in}}{2L}$	$>$	$i_o + \frac{(1-\alpha)T_s\alpha v_{in}}{2(1+k)(2-\alpha)L}$
I_{Dmax}	$i_o + \frac{(1-\alpha)T_s\alpha v_{in}}{2L}$	$>$	$i_o + \frac{(1-\alpha)T_s\alpha v_{in}}{2(1+k)(2-\alpha)L}$

2.9 Analysis of Power Losses and Efficiency

The power loss in the proposed HSDBuC is mainly due to the semiconductor devices and the resistances of inductors. The loss analysis is carried out by assuming all the capacitors are ideal. The output power, P_o, can be written as $P_o = v_o i_o = i_o^2 R$. The switching conduction loss due to ON-state resistance, $r_{DS(on)}$, of the switches S_1 and S_2 is determined by using Equation (2.45) as follows. Assuming that the output capacitance, C_s, of the switches S_1 and S_2 is linear, the switching loss P_{sw} is expressed as

$$P_{sw} = 2f_s C_s v_C^2 = \frac{2f_s C_s v_C^2}{v_o^2} P_o \tag{2.49}$$

By using Equation (2.46), the conduction loss due to diode conduction resistance r_D is

$$P_{r_D} = r_D(1-\alpha)i_o^2 = r_D(1-\alpha)\frac{P_o}{R} \tag{2.50}$$

The bias loss, P_{v_D}, due to forward bias voltage, v_d, of the diode D is calculated by using Equation (2.47)

$$P_{v_{fd}} = v_d(1-\alpha)i_o = v_{fd}(1-\alpha)\frac{P_o}{v_o} \tag{2.51}$$

The losses due to the inductive resistances r_{L_i} and r_L of the L and L_i-windings respectively are as follows.

$$P_{r_{Li}} = r_{L_i}(\frac{\alpha}{2-\alpha})^2 i_o^2 = r_{L_i}(\frac{\alpha}{2-\alpha})^2\frac{P_o}{R} \tag{2.52}$$

$$P_{r_L} = r_L i_o^2 = r_L\frac{P_o}{R} \tag{2.53}$$

Therefore, the total power loss, P_{Loss}, is calculated as

$$P_{Loss} = P_{r_{(on)}} + P_{sw} + P_{r_D} + P_{v_{fd}} + P_{r_{Li}} + P_{r_L} \tag{2.54}$$

Thus, the efficiency, η, is derived as follows by using Equations (2.48)−(2.54).

$$\eta = \frac{1}{1+(P_{Loss}/P_o)} = \frac{1}{1+\frac{2r_{DS(on)}\alpha}{R}+\frac{2f_sC_oV_C^2}{v_o^2}+\frac{r_D(1-\alpha)}{R}+\frac{v_{fd}(1-\alpha)}{v_o}+\frac{r_{L_i}}{R}(\frac{\alpha}{2-\alpha})^2+\frac{r_L}{R}} \tag{2.55}$$

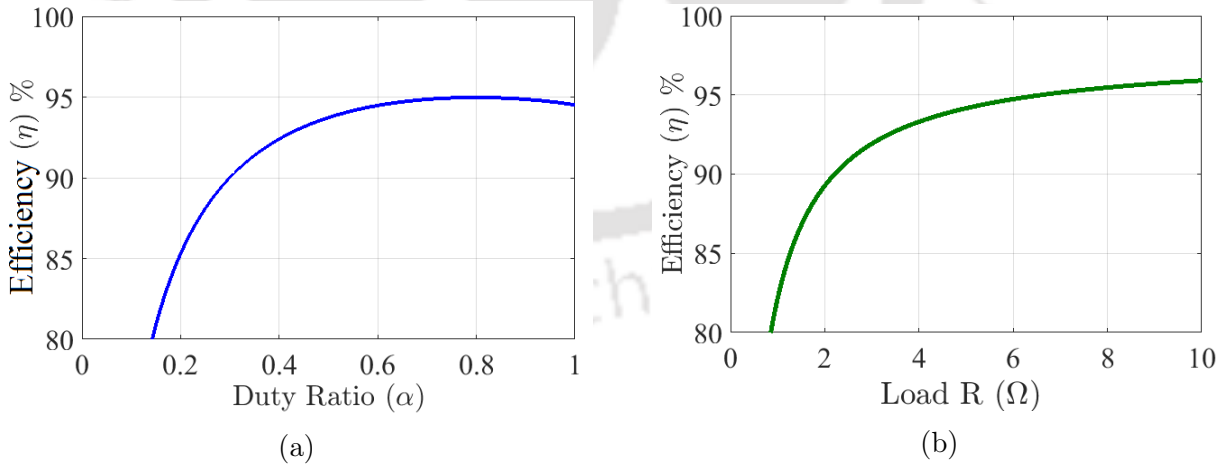


Figure 2.8: Theoretical efficiency of HSDBuC due to change of (a) α, and (b) Load R

The theoretical efficiencies of the proposed HSDBuC due to the variation of duty ratio (α) and load resistance (R) are shown in Figures 2.8a and 2.8b respectively.

2.10 Small Signal Modelling

In this section, followed by average state-space and steady-state analysis, power-stage transfer functions are determined to enable the closed-loop control systems.

2.10.1 Average state-space matrices

The general average state-space equations are written as follows.

$$\dot{\mathbf{x}}(t) = \mathbf{A_{av}}\mathbf{x}(t) + \mathbf{B_{av}}v_{in}(t) \tag{2.56}$$

$$\mathbf{y}(t) = \mathbf{Z_{av}}\mathbf{x}(t) \tag{2.57}$$

The average state matrices of Equations (2.56) and (2.57) are as follows.

$$\begin{aligned}\mathbf{A_{av}} &= (\mathbf{A_1} - \mathbf{A_2})\alpha + \mathbf{A_2} \\ &= \begin{bmatrix} 0 & \frac{\alpha(L-M)-2L}{LL_i - M^2} & \frac{MRr_{C_f}}{(LL_i - M^2)(R + r_{C_f})} & \frac{MRr_{C_f}}{(LL_i - M^2)(R + r_{C_f})} \\ \frac{2-\alpha}{2C} & 0 & \frac{-\alpha}{2C} & 0 \\ 0 & \frac{2M + \alpha(L_i - M)}{LL_i - M^2} & \frac{-LiRr_{C_f}}{(LL_i - M^2)(R + r_{C_f})} & \frac{-L_iRr_{C_f}}{(LL_i - M^2)(R + r_{C_f})} \\ 0 & 0 & \frac{R}{C_f(R + r_{C_f})} & \frac{-1}{RC_f(R + r_{C_f})} \end{bmatrix}\end{aligned} \tag{2.58}$$

$$\mathbf{B_{av}} = (\mathbf{B_1} - \mathbf{B_2})\alpha + \mathbf{B_2} = \begin{bmatrix} \frac{L}{LL_i - M^2} & 0 & \frac{-M}{LL_i - M^2} & 0 \end{bmatrix}^T \tag{2.59}$$

$$\mathbf{Z_{av}} = (\mathbf{Z_1} - \mathbf{Z_2})\alpha + \mathbf{Z_2} = \begin{bmatrix} 0 & 0 & \frac{Rr_{C_f}}{R + r_{C_f}} & \frac{R}{R + r_{C_f}} \end{bmatrix} \tag{2.60}$$

Now, considering a perturbation, $\hat{v}_{in}(t)$, in the steady state input voltage, V_{in}, the input voltage is expressed by $v_{in}(t) = V_{in} + \hat{v}_{in}(t)$. This perturbation in v_{in} affects the steady-state values of inductor currents and capacitor voltages. If the instantaneous state vector $\mathbf{x}(t)$ and output $\mathbf{v_o}(t)$ are $\mathbf{x}(t) = \mathbf{X} + \hat{\mathbf{x}}(t)$ and $\mathbf{v_o}(t) = \mathbf{V_o} + \hat{\mathbf{v}}_o(t)$, respectively, the state-space equation with the perturbation can be written as follows.

$$\dot{\mathbf{X}} + \dot{\hat{\mathbf{x}}}(t) = \mathbf{A_{av}}(\mathbf{X} + \hat{\mathbf{x}}(t)) + \mathbf{B_{av}}(V_{in} + \hat{v}_{in}(t)) \tag{2.61}$$

$$\mathbf{V_o} + \hat{\mathbf{v}}_o(t) = \mathbf{Z_{av}}(\mathbf{X} + \hat{\mathbf{x}}(t)) \tag{2.62}$$

This perturbation also affects the nominal duty cycle α that becomes $\alpha(t) + \hat{\alpha}(t)$. Substituting it into Equations (2.58) to (2.60), the average state-space matrices are expressed as follows.

$$\mathbf{A_{av}} = (\mathbf{A_1} - \mathbf{A_2})(\alpha(t) + \hat{\alpha}(t)) + \mathbf{A_2} \tag{2.63}$$

$$\mathbf{B_{av}} = (\mathbf{B_1} - \mathbf{B_2})(\alpha(t) + \hat{\alpha}(t)) + \mathbf{B_2} \tag{2.64}$$

$$\mathbf{Z_{av}} = (\mathbf{Z_1} - \mathbf{Z_2})(\alpha(t) + \hat{\alpha}(t)) + \mathbf{Z_2} \tag{2.65}$$

2.10.2 Steady-state analysis

Under ideal condition, the parasitics r_L, r_{L_i} and r_{C_f} are neglected as $r_L, r_{L_i}, r_{C_f} << R$ and the steady-state values of the state variables are

$$\mathbf{X} = [I_{L_i}\ V_C\ I_L\ V_{C_f}]^T = -\mathbf{A_{av}}^{-1}\mathbf{B_{av}}V_{in} = \left[\frac{\alpha^2 V_{in}}{R(2-\alpha)^2}\ \frac{V_{in}}{2-\alpha}\ \frac{\alpha V_{in}}{2R(2-\alpha)}\ \frac{\alpha V_{in}}{2-\alpha}\right]^T \tag{2.66}$$

2.10.3 Power-stage transfer function

The input-to-output voltage transfer function, $G_{vg}(s)$, can be determined by using Equations (2.56) to (2.60) as follows.

$$G_{vg}(s) = \frac{\hat{v}_o(s)}{\hat{v}_{in}(s)} = \mathbf{Z_{av}}(s\mathbf{I} - \mathbf{A_{av}})^{-1}\mathbf{B_{av}} = \frac{-n_3 s^3 - n_2 s^2 + n_1 s + n_0}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \tag{2.67}$$

The coefficients of the denominator of the $G_{vg}(s)$ and $G_{v\alpha}(s)$ are provided in Table 2.2. The numerators of the $G_{vg}(s)$ are $n_3 = \frac{MRr_{C_f}}{(LL_i - M^2)(R + r_{C_f})}$, $n_2 = \frac{MR}{(LL_i - M^2)(R + r_{C_f})C_f}$, $n_1 = \frac{(2-\alpha)\alpha MRr_{C_f}}{2(LL_i - M^2)(R + r_{C_f})C}$, $n_0 = \frac{\alpha(2-\alpha)R}{2(LL_i - M^2)(R + r_{C_f})CC_f}$. Since the coefficients of the numerator are negative, there is a zero on the right-half of the s-plane. Therefore, $G_{vg}(s)$ becomes non-minimum phase in nature. The Figure 2.9 shows the responses of the transfer function of $G_{vg}(s)$ for different values of α. The $G_{vg}(s)$ is tested with a step-signal of amplitude equal to $v_{in} = 20$ V. The undershoot in the responses of the proposed HSDBuC validates the non-minimum phase behaviour. The responses of $G_{vg}(s)$ of the proposed HSDBuC are com-

pared with $G_{vg}(s)$ of CBuC [117] which is not a non-minimum phase system and its response has no undershoot.

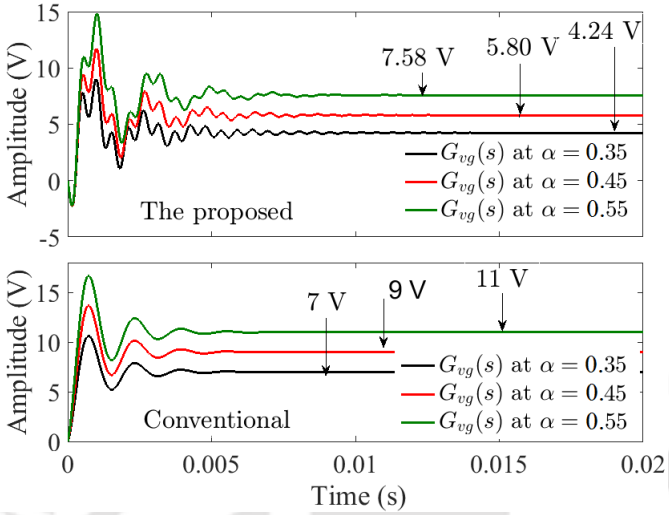


Figure 2.9: Step response of transfer function $G_{vg}(s)$ for the uncompensated proposed HSDBuC and CBuC at different α values

Table 2.2: The Coefficients of transfer functions $G_{vg}(s)$ and $G_{v\alpha}(s)$ of HSDBuC

Coefficient	**Expression**
a_3	$\dfrac{(L_i - M)Rr_{C_f}V_{in}}{(LL_i - M^2)(2-\alpha)(R + r_{C_f})}$
a_2	$\dfrac{(C(M - L_i)(\alpha - 2)R + C_f\alpha((M - L_i)\alpha - 2M)r_{C_f})V_{in}}{(LL_i - M^2)(2-\alpha)^2CC_f(R + r_{C_f})}$
a_1	$\dfrac{((C_fRr_{C_f} - L_i + M)\alpha^2 - (4C_fRr_{C_f} + 2M)\alpha + 4C_fRr_{C_f})V_{in}}{(LL_i - M^2)(2-\alpha)^2CC_f(R + r_{C_f})}$
a_0	$\dfrac{RV_{in}}{(LL_i - M^2)CC_f(R + r_{C_f})}$
b_4	1
b_3	$\dfrac{1}{C_fR(R + r_{C_f})} + \dfrac{L_iRr_{C_f}}{(LL_i - M^2)(R + r_{C_f})}$
b_2	$\frac{1}{2}\dfrac{((L_i + L - 2M)\alpha^2 + 4(M - L)\alpha + 4L)C_f(R + r_{C_f}) + 2L_iCR}{(LL_i - M^2)CC_f(R + r_{C_f})}$
b_1	$\dfrac{1}{2}\dfrac{(L_i + L - 2M + C_fRr_{C_f})\alpha^2 + 4(M - L - C_fRr_{C_f})\alpha + 4L + C_fRr_{C_f}}{(LL_i - M^2)CC_f(R + r_{C_f})}$
b_0	$\dfrac{1}{2}\dfrac{(\alpha - 2)^2R}{(LL_i - M^2)CC_f(R + r_{C_f})}$

By using Equations (2.56) to (2.66), the voltage to duty ratio transfer function $G_{v\alpha}(s)$ is derived as

$$G_{v\alpha}(s) = \frac{\hat{v}_o(s)}{\hat{\alpha}(s)} = \mathbf{Z_{av}}(s\mathbf{I} - \mathbf{A_{av}})^{-1}[(\mathbf{A_1} - \mathbf{A_2})\mathbf{X} + (\mathbf{B_1} - \mathbf{B_2})V_{in}] + (\mathbf{Z_1} - \mathbf{Z_2})\mathbf{X} \tag{2.68}$$

By using Equation (2.68), the following voltage to duty ratio transfer function is derived.

$$G_{v\alpha}(s) = \frac{a_3 s^3 + a_2 s^2 + a_1 s + a_0}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \tag{2.69}$$

The coefficients of $G_{v\alpha}(s)$ in terms of RLC-parameters are provided in Table 2.2. By substituting the parameter values provided in Table 2.3, the coefficients of $G_{v\alpha}(s)$ are determined. The coefficients of numerator are $a_3 = 9.7559 \times 10^3$, $a_2 = 1.2267 \times 10^8$, $a_1 = 1.5731 \times 10^{12}$, $a_0 = 2.3890 \times 10^{16}$. The coefficient of denominator are $b_4 = 1$, $b_3 = 2141$, $b_2 = 1.459 \times 10^8$, $b_1 = 1.832 \times 10^{11}$, $b_0 = 1.529 \times 10^{15}$. The bode diagram of $G_{v\alpha}(s)$ is provided in Figure 2.10. The gain margin and the phase margin of the transfer function are -15 dB and $-150°$, respectively. A PI controller is designed in the voltage mode framework to make the closed loop system stable and is described in the next section.

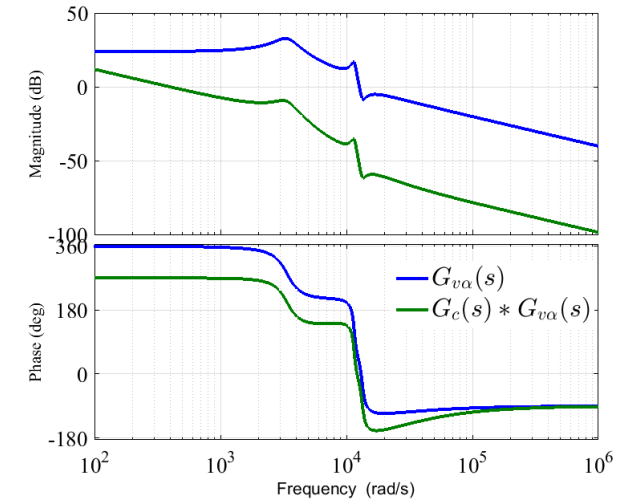


Figure 2.10: Bode diagrams of $G_{v\alpha}(s)$ with and without PI controller

2.11 Control Scheme

The block diagram representation of the closed loop system of the proposed HSDBuC is shown in Figure 2.11. In the voltage mode control (VMC) framework a PI controller is designed

and defined as

$$G_c(s) = K_p + \frac{K_i}{s} \tag{2.70}$$

Table 2.3: Circuit parameters of HSDBuC considered for CCM operation

Variable	Definition	Value
v_{in}	Input voltage	20 V
L_i	Inductance of L_i-winding	180 μH
L	Inductance of L-winding	180 μH
$r_{L_i} = r_L$	Parasitics of coupled-inductor	0.07 Ω
k	Coupling factor	0.5
$C_1 = C_2 = C$	Identical capacitors	100 μF
$r_{C_1} = r_{C_2}$	ESR of $C_1 = C_2$	0.32 ΩF
C_f	Output capacitor	330 μF
r_{C_f}	ESR of C_f	0.22 ΩF
R	Load resistance	5 Ω
f_s	Switching frequency	50 kHz
v_{fd}	Diode forward voltage	0.39 V
$r_{DS(on)}$	MOSFET on-resistance	0.040 Ω
C_s	MOSFET output-capacitance	295 pF
r_D	Diode Resistance	0.078 Ω

The coefficients of the controller $G_c(s)$ are $K_p = 0.001205$ and $K_i = 25$. The Figure 2.10 shows the bode diagram of the uncompensated, $G_{v\alpha}(s)$, and compensated plant ($G_c(s)G_{v\alpha}(s)$).

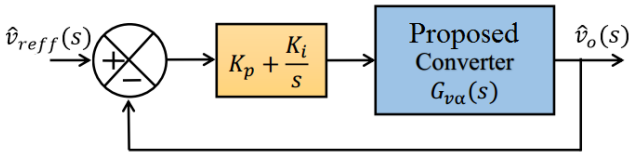


Figure 2.11: Block diagram representation of closed-loop system

The gain and phase margin of the compensated plant are 11.8 dB and 89.8° respectively. The closed-loop zeros are $z_1 = -1.37 \times 10^4$, $z_2 = -2.07 \times 10^4$, $z_3 = z_4 = 6.00 \times 10^2 \pm i1.33 \times 10^4$.

The closed-loop poles are $s_1 = -3.86 \times 10^2$, $s_2 = s_3 = -425.19 \pm i1.153 \times 10^4$, $s_4 = s_5 = -458.05 \pm i3.38 \times 10^3$. All the closed-loop poles are on left half of the s-plane. Therefore, the closed loop system is stable.

2.12 Simulation results

The MATLAB-Simscape platform is used to carry out the simulation work for the proposed HSDBuC using the parameters given in Table 2.3. At $\alpha = 0.40$ and $V_{in} = 20$ V, the steady-state output voltages of the proposed HSDBuC and CBuC are 4.9 V and 7.9 V respectively as shown in Figure 2.12. The simulation result of the proposed HSDBuC validates the step-down conversion ratio given in Equation (2.19). Thus, the proposed HSDBuC produces a lower output voltage at the same duty cycle. Both the converters have a 0.1 V steady-state error.

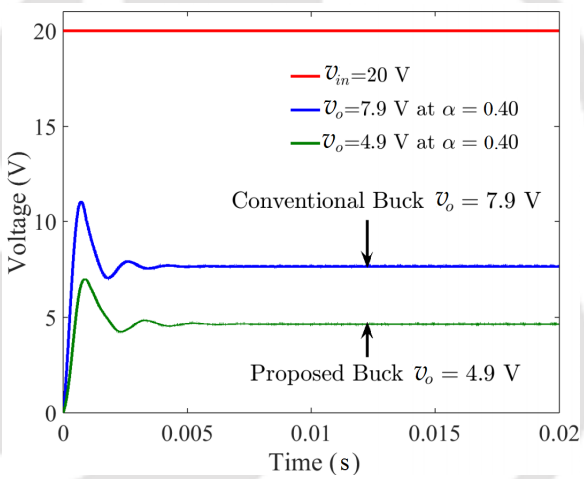


Figure 2.12: Response of the proposed HSDBuC and CBuC at $\alpha = 0.40$

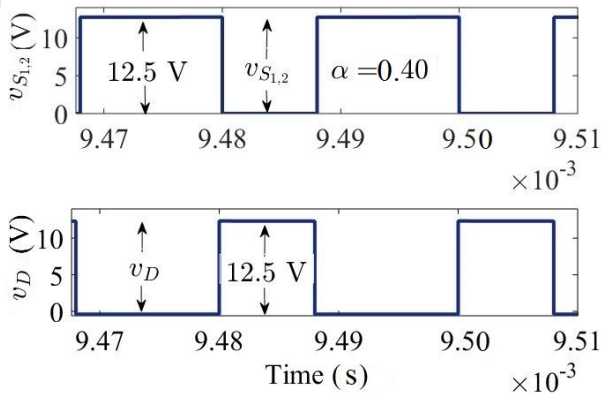


Figure 2.13: Voltage stresses of switches and diodes for $\alpha = 0.40$

The Figure 2.13 shows the voltage stress $v_{S_1} = v_{S_2} = v_{in}/(2-\alpha) = 12.5$ V and the diode stress $v_D = 12.5$ V at $\alpha = 0.40$. Therefore, it can be said that the stresses of the semiconductor devices are less than v_{in} i.e. 20 V. The effects of voltage conversion ratio and coupling factor on ripple reduction in i_L and v_o are shown in Figures. 2.14 and 2.15 respectively. The CBuC and the proposed HSDBuC are simulated in equal input-output voltage condition. Therefore, for $\alpha = 0.40$, the required duty ratio for CBuC is $\alpha_b = \alpha/(2-\alpha) = 0.25$. The Δi_L and Δv_o of the CBuC are 424.8 mA and 89.5 mV respectively. The Δi_L of the proposed HSDBuC with $k = 0$ is 339.5 mA and it is 226.3 mA when $k = 0.5$. The Δv_o of the proposed HSDBuC with $k = 0$ is 71.6 mV and it is 47.8 mV when $k = 0.5$.

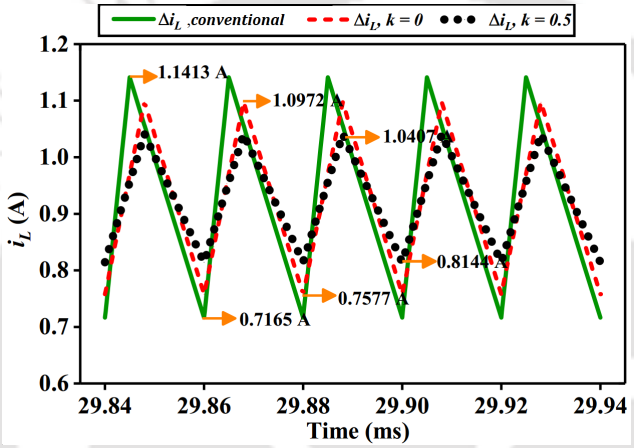


Figure 2.14: Ripple in inductor current i_L for CBuC and proposed HSDBuC with $k = 0$ and $k = 0.5$.

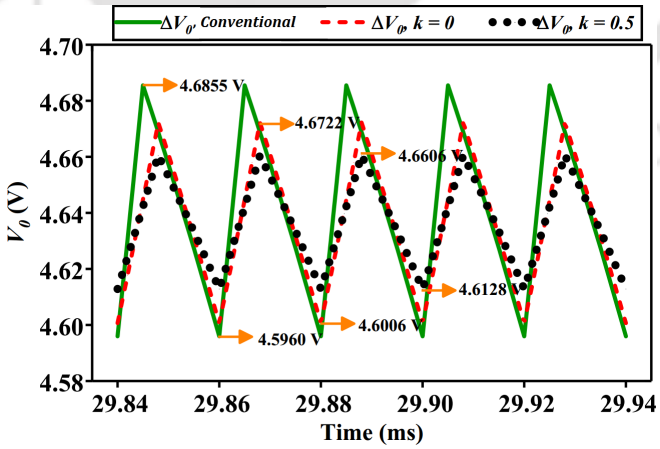


Figure 2.15: Ripple in output voltage v_o for CBuC and proposed HSDBuC with $k = 0$ and $k = 0.5$

2.13 Experimental setup and results

The schematic circuit diagram of the closed-loop control systems of the proposed HSDBuC is shown in Figure 2.16.

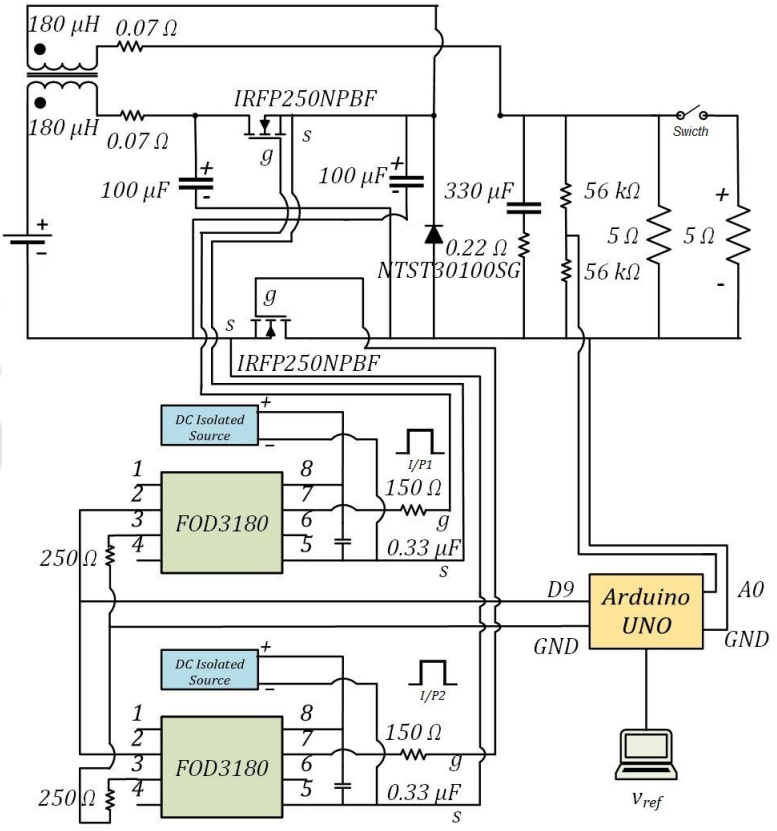
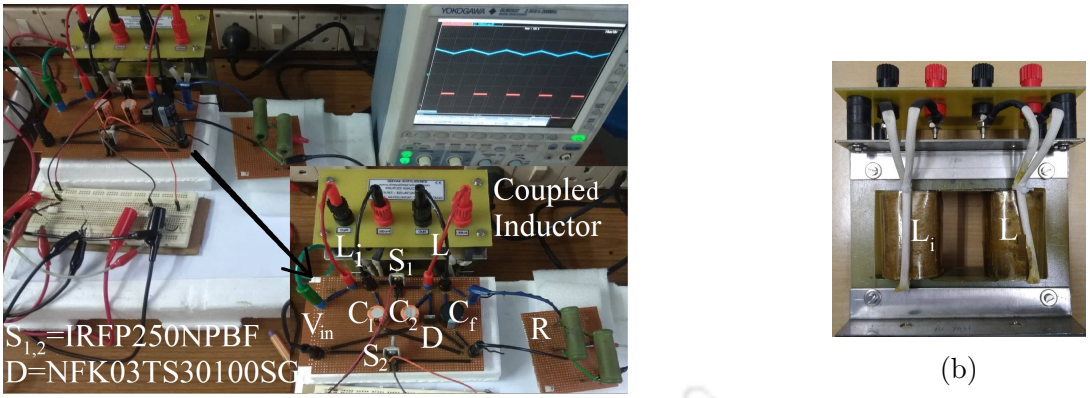


Figure 2.16: Schematic circuit of the closed-loop system of the proposed HSDBuC

To validate the mathematical expressions and simulation results, the proposed HSDBuC is designed by the parameters given in Table 2.3 and the setup is shown in Figure 2.17a. The switches S_1 and S_2 are implemented by power MOSFETs IRFP250NPBF and the diode D is implemented by NTST30100SG/NFK03TS30100SG. Two gate driver optocoupler ICs FOD3180 are used. The capacitors used here are electrolytic.

The coupled inductor is designed by two U/C type ferrite core as shown in Figure 2.17b. The flux density B_{max} of the ferrite core is 0.3 Tesla. Both the windings are identical having a maximum current rating (I_{pk}) of 8 A. The magnetic cross-section area (A_e) of the core is $A_e = 2.4$ cm^2. The turns number (N) can be determined by the equation $N = \frac{LI_{pk}}{B_{max}A_e}$ [118]. Therefore, the turns number are calculated as $N = 20$.

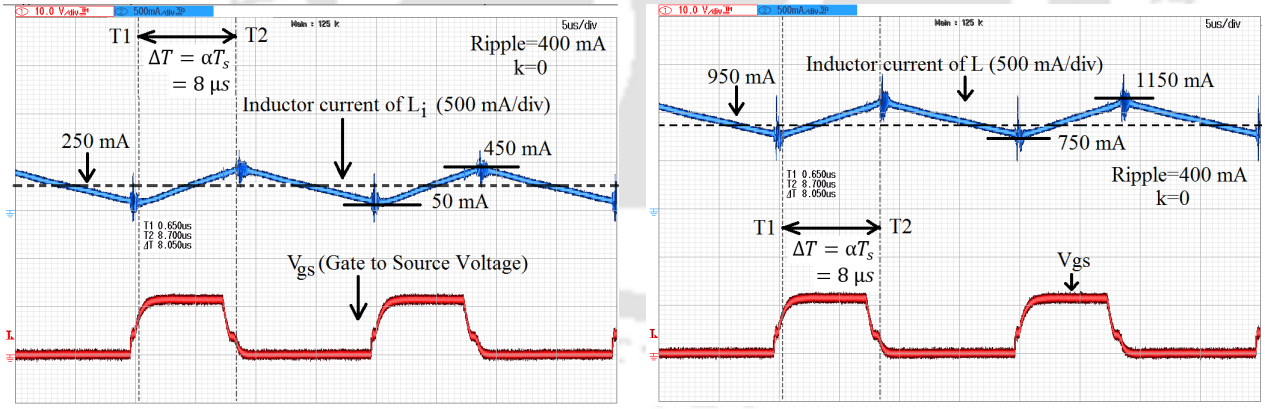


(a) (b)

Figure 2.17: Experimental setup (a) The proposed HSDBuC with DWCI, and (b) Dual winding coupled inductor (DWCI)

2.13.1 Ripple improvement

Initially, two single inductors i.e. coupling factor $k = 0$ are used to test the proposed converter. For $\alpha = 0.40$, Δi_{L_i} in L_i and Δi_L in L are 400 mA as observed in Figures 2.18a and 2.18b respectively. The ON-state duration of i_L and i_{L_i} is defined by $\Delta T = \alpha T_s = 0.4 \times (1/50000) = 8\ \mu$s.

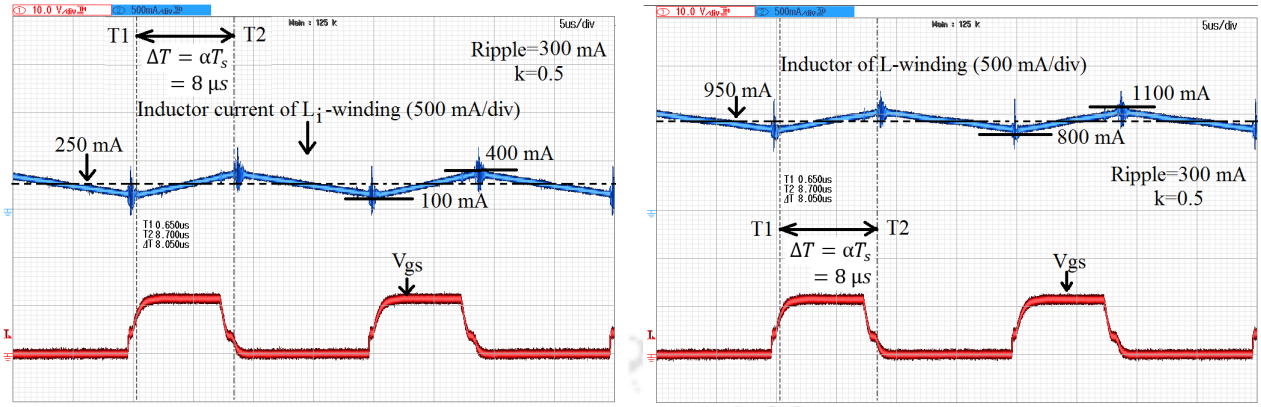


(a) (b)

Figure 2.18: Ripple in inductor current for $\alpha = 0.40$ and $k = 0$ (a) i_{L_i}, and (b) i_L

Next, a dual-winding coupled inductor with coupling factor $k = 0.5$ is used to test the proposed HSDBuC. The ripple in input current i.e. ripple current in L_i-winding is $\Delta i_{L_i} = 300$ mA at $\alpha = 0.40$ as shown in Figure 2.19a and the ripple current in L-winding is $\Delta i_L = 300$ mA as shown in Figure 2.19b. Therefore, the proposed HSDBuC with DWCI has better ripple

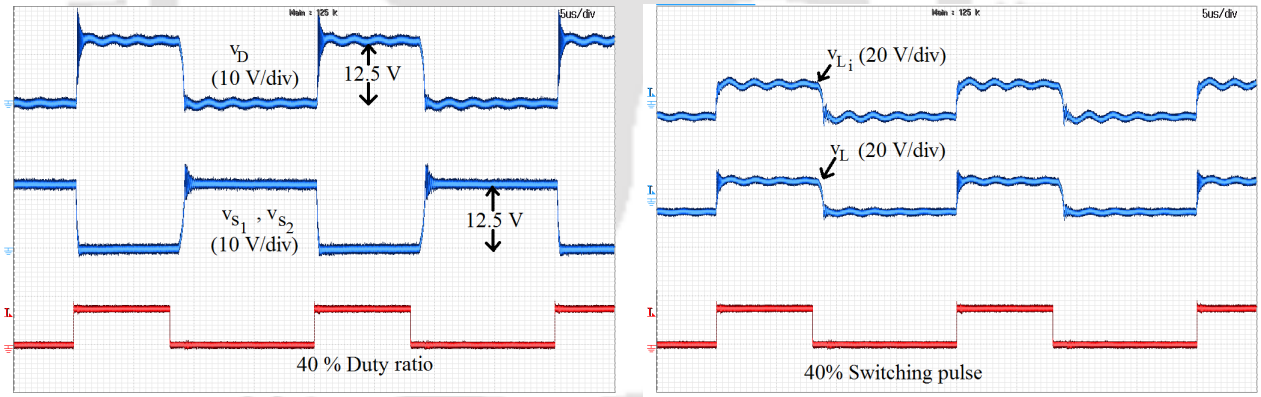
reduction performance.



(a) (b)

Figure 2.19: Ripple in inductor current for $\alpha = 0.40$ and $k = 0.5$ (a) i_{L_i}, and (b) i_L

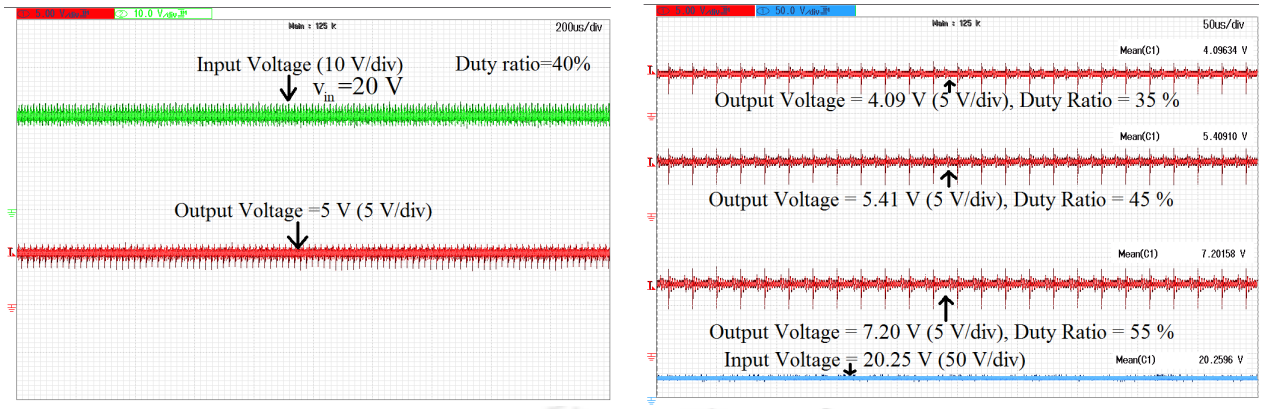
The voltage stresses of switches and diode are $v_s = v_D = 12.5$ V as shown in Figure 2.20a for $\alpha = 0.40$. The inductive voltages v_{L_i} and v_L are shown in Figure 2.20b. The Figures 2.19a-2.20b resemble the idealized waveform provided in Figure 2.3.



(a) (b)

Figure 2.20: Experimental results for $\alpha = 0.40$ and $k = 0.5$ (a) v_s, and (b) v_L, v_{L_i}

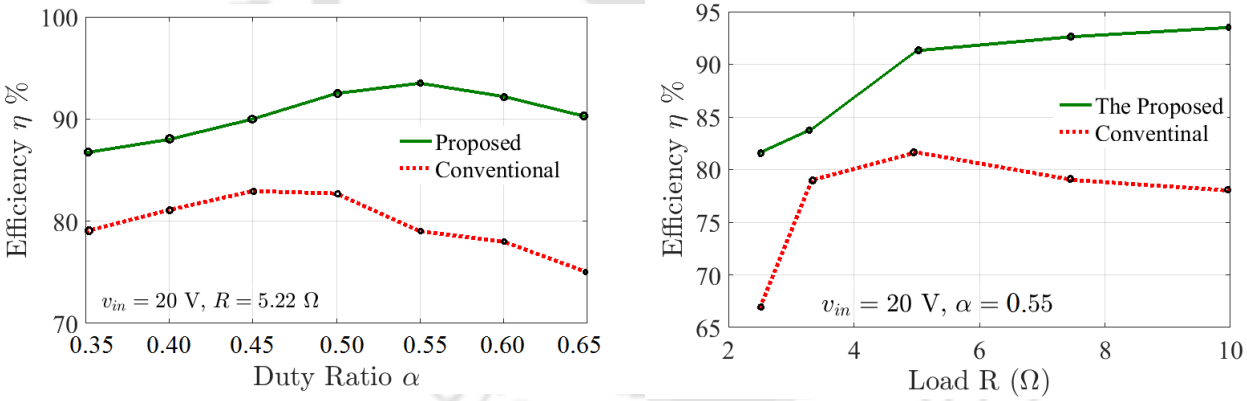
The output voltage of the proposed converter $v_o = 5$ V at $\alpha = 0.40$ is provided in Figure 2.21a. The ripple in output voltage is measured to be 50 mV. In Figure 2.21b, the steady-state output voltages for different values of α are shown. These results validate the voltage conversion ratio derived in Equation (2.19) and follow the simulated steady-state response shown in Figure 2.9.



(a) (b)

Figure 2.21: Output voltages of the proposed HSDBuC (a) $v_o = 5$ V for $\alpha = 0.40$ and $k = 0.5$, and (b) Steady-state v_o values for different values of α

The experimental results of efficiency versus duty ratio and load, R, for the proposed converter with the coupled inductor are shown in Figures 2.22a and 2.22b respectively. The experimental efficiencies are compared with the efficiencies of the conventional buck. A maximum efficiency of 93.5% is achieved at output power $P_o = 11.50$ W and $\alpha = 0.55\%$.



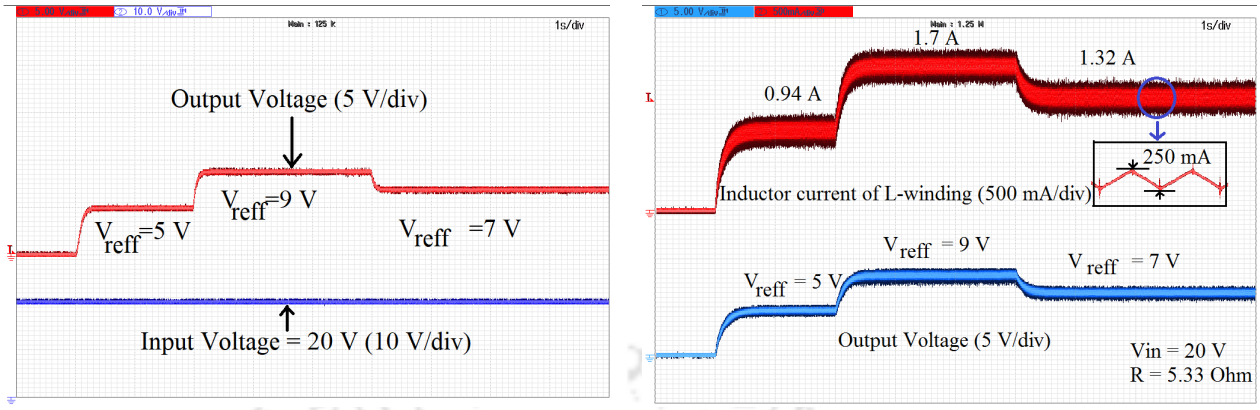
(a) (b)

Figure 2.22: Plots of experimental efficiency versus the variation in (a) α, and (b) Load R for CBuC and proposed HSDBuC

2.13.2 Closed-loop performance

In Figure 2.23a, output reference voltage V_{reff} is increased from 5 V to 9 V and then decreased from 9 V to 7 V. The output does not show any peak overshoot and the output voltage follows the reference change. The change of i_L due to reference change is shown in

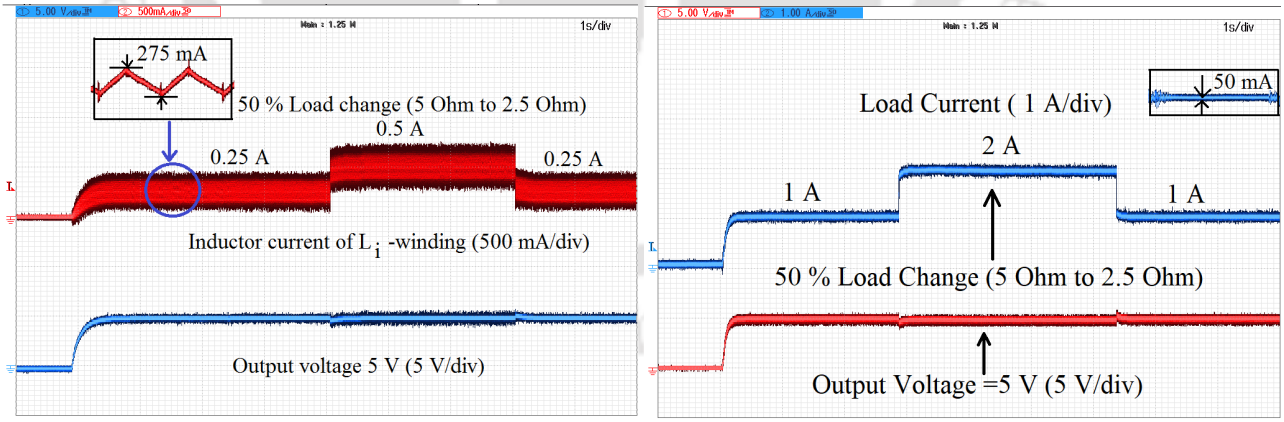
Figure 2.23b and it also follows the reference change. The ripple in i_L is $\Delta i_L = 250$ mA.



(a) (b)

Figure 2.23: Experimental results for reference voltage change on (a) v_o, and (b) i_L

50% load change is carried out to investigate the sensitivity to load parameter variation. Despite 50% load change the output voltage follows V_{reff} as shown in Figure 2.24. The change of input current i.e. i_{L_i} is shown and it is observed that i_{L_i} reaches 0.25 A to 0.5 A when the load is changed from 5 Ω to 2.5 Ω. i_{L_i} comes back to the previous state when the load is increased from 2.5 Ω to 5 Ω. The ripples in i_{L_i} and i_o are $\Delta i_{L_i} = 275$ mA $\Delta i_o = 50$ mA respectively.



(a) (b)

Figure 2.24: Experimental results of (a) i_{L_i}, and (b) Load current for 50 % load change

The load current due to 50% load change is shown in Figure 2.24b. Output load current increases from 1 A to 2 A when the load is reduced from 5 Ω to 2.5 Ω and decreases from 2 A to 1 A when the load is increased from 2.5 Ω to 5 Ω.

Table 2.4: Comparisons among the existing converters and the proposed HSDBuC

Topology	[21]	[22]	[23]	[37]	[38]	[119]	[120]	proposed
Voltage Gain $\frac{v_o}{v_{in}}$	$\frac{\alpha}{\alpha+\frac{n_1}{n_2}(1+\frac{L_r}{L_n})}$	$\frac{\alpha}{1+n-n\alpha}$	$\frac{(1-\alpha)\alpha}{n+1-\alpha}$	2α	α	α^2	α^2	$\frac{\alpha}{2-\alpha}$
$v_{S_{max}}$	v_{in}	v_{in}	v_{in}	v_{in}	v_{in}	v_{in}	$v_O+\sqrt{v_O v_{in}}$	$\frac{v_{in}}{2-\alpha}$
No of switches	3	3	4	2	2	4	4	2
No of diodes	0	1	0	2	2	0	0	1
No of inductors	2 *windings*	2 *windings*	2 *windings*	3	2	2	2	2 *windings*
No of capacitors	2	3	2	1	3	1	3	3

A comparison of the proposed HSDBuC with reported step-down topologies is shown in Table 2.4. Apart from the step-down ratios of the converters reported in [21], [22] and [23], the coupled inductor does not help in improving the ripple in current and output voltage in these topologies. These converters use more number of switches. The voltage conversion ratio of the converter presented in [21] depends upon the ratio of leakage inductance L_r to magnetizing inductance L_m. The step-down conversion ratio of the converters presented in [37, 38] is less than the proposed converter. A comparison plot for voltage conversion ratio is shown in Figure 2.25a by considering $n = 1$.

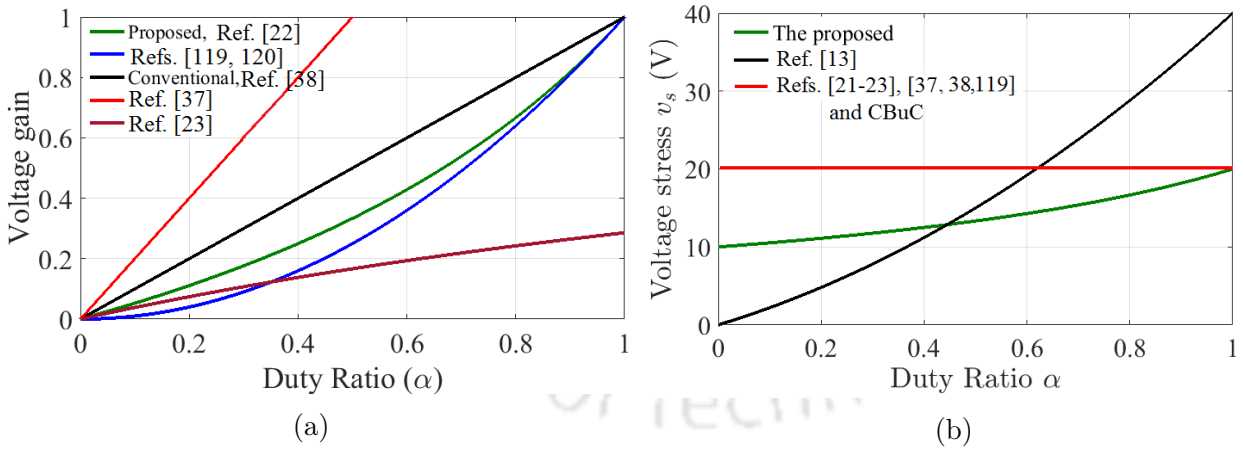


Figure 2.25: Comparison plots based on the theoretical expressions of (a) Voltage gain, and (b) Voltage stress against the duty ratio α, for the proposed HSDBuC, CBuC and reported buck converters

A comparison of voltage stress is shown in Figure 2.25b. The switches of these converters suffer high input voltage stress. Whereas, the proposed converter has voltage stress less than the input voltage v_{in} and it is possible to use switches with a lower voltage rating to implement the proposed HSDBuC. In addition, the proposed HSDBuC utilizes fewer active components

compared to the converters reported in [37, 38, 119, 120]. The proposed HSDBuC is less bulky as it utilizes a dual-winding coupled inductor.

2.14 Summary

In this chapter, a transformerless buck converter with large voltage step-down ratio is designed where the conversion ratio is independent of the turns ratio of the dual-winding coupled inductor. By comparing the proposed HSDBuC with CBuC, it is seen that the former produces less output voltage than the latter under the same condition. Hence, the proposed HSDBuC is suitable for applications requiring large step-down ratio while avoiding a narrow duty cycle to get a lower output voltage. Moreover, in case of the proposed topology, the coupled inductor reduces the ripples in inductor currents and in output voltage. It is also found that the voltage stresses of the semiconductor devices are less than the input voltage in this topology which has shown a maximum experimental efficiency of 93.5%. Small-signal modelling of the proposed HSDBuC with coupled inductor is carried out and a voltage mode PI-controller is designed to investigate the closed-loop performance. Closed-loop experiment shows a stable performance of the converter without any overshoot under a step-change in reference voltage and 50% load change.

3

High Step-down Interleaved Buck Converter

A two-phase interleaved buck converter providing high step-down conversion ratio is proposed in this chapter. The proposed high step-down interleaved buck converter (HSDIBuC) uses a switch-capacitor cell to achieve high step-down conversion ratio compared to the conventional interleaved buck converter (CIBuC). The cell consists of two parallel switches and two cross-connected identical capacitors. These identical capacitors are charged in series and discharged in parallel by producing lower output voltage compared to the CIBuC at the same duty ratio. The proposed HSDIBuC provides less voltage and current stresses. The operation principle is described, and the ripple and the average current through the inductors are determined in continuous conduction mode (CCM). The boundary load condition is also determined. By explaining the charging and discharging of the two identical capacitors of the cell, the capacitance value is determined. The losses and the efficiency are analyzed, and 96.33 % efficiency is achieved. Finally, the proposed HSDIBuC is implemented and experimental results are provided.

3.1 Introduction

In the previous chapter, to deal with the problem of very narrow duty cycle for high-input to low-output voltage conversion, the conversion ratio of the conventional buck converter (CBuC) has been improved using a switch-capacitor cell. Therefore, to overcome the similar problem in the conventional interleaved buck converter (CIBuC), the voltage conversion ratio can be modified using the same switch-capacitor cell. In this chapter, a high step-down conversion ratio interleaved buck converter (HSDIBuC) with the switch-capacitor cell is proposed to achieve higher step-down conversion ratio compared to CIBuC. The modified step-down ratio helps to achieve less ripples in inductor currents. The conversion ratio of the HSDIBuC does not depend upon the turns ratio of a transformer or a coupled inductor. The proposed HSDIBuC operates below and above 0.50 duty ratio. While fulfilling this main motive, the proposed HSDIBuC also shows less voltage and current stresses in the semiconductor devices reducing the voltage and current ratings of the active elements. In addition, the HSDIBuC topology is simpler and requires less components. Efficiency of the HSDIBuC is also high.

The chapter is organized as follows. The principle of operation is explained in Section 3.2. In Section 3.3, the voltage conversion ratio is derived. The average and the ripple currents through the inductors are analysed in Section 3.4. The boundary condition between CCM and DCM is determined in Section 3.5. In Section 3.6, the input ripple current is analysed. The capacitors are designed in Section 3.7. In Section 3.8, the voltage and the current stresses are provided. The power losses and the efficiency are illustrated in Section 3.9. The parameter values are selected in Section 3.10. Section 3.11 describes the simulation results. The experimental results are provided in Section 3.12. Finally a brief summary on the HSDIBuC is provided in Section 3.13.

3.2 Principle of Operation

Figure 3.1 shows the proposed HSDIBuC with a switch-capacitor cell operating in continuous conduction mode (CCM). The input voltage v_{in} is followed by an inductor L_i with parasitic r_{L_i}. Two parallel switches S_1 and S_2 of the cell are connected by two cross-connected identical capacitors C_1 and C_2. The parasitics of C_1 and C_2 are r_{C_1} and r_{C_2} respectively. These two switches operate simultaneously. When S_1 and S_2 do not conduct, the two identical capacitors

charge in series, and when S_1 and S_2 conduct, the capacitors discharge in parallel.

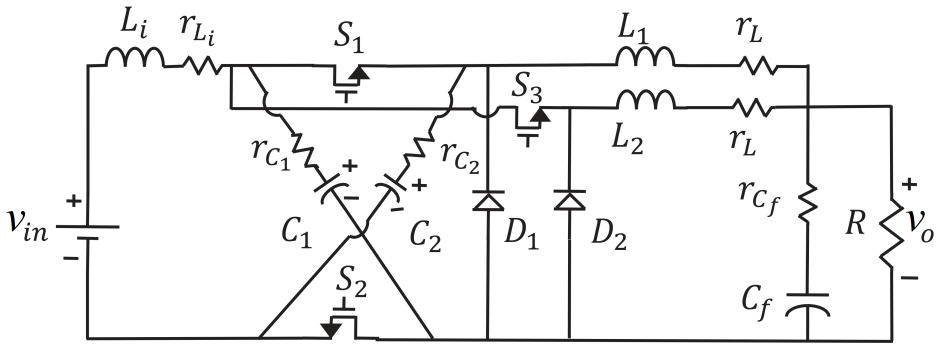


Figure 3.1: The proposed high step-down interleaved buck converter (HSDIBuC)

This series-parallel transition in the circuit configuration causes sudden change in the input current. To prevent this, L_i is placed in the input side. S_1 is followed by a diode D_1 and an inductor L_1 with parasitic r_L. The switch S_3 operates in 180° phase shift with respect to the switches S_1 and S_2. S_3 is followed by a diode D_2 and an inductor L_2 with parasitic r_L. The capacitor C_f with parasitic r_{C_f} is the output filter capacitor. v_o is the output voltage at the load resistance R.

Depending upon the range of duty ratio α, the switching modes of the proposed HSDIBuC are discussed. In order to illustrate the switching operations, capacitors $C_1 = C_2 = C$ and inductors $L_1 = L_2 = L$ are considered. The parasitics r_{L_i},r_{C_1}, r_{C_2}, r_L and r_{C_f} are negligible as $(r_{L_i},\ r_{C_1},\ r_{C_2},\ r_L,\ r_{C_f}) << R$. In steady state analysis, all the semiconductor devices are considered ideal. The value of C_f is considered large enough to keep the v_o constant.

3.2.1 Switching modes when $\alpha \in (0, 0.5]$

When the duty ratio α belongs to $(0, 0.5]$, all the three switches are OFF for two specific time durations of time period T_s as shown in Figure 3.2. The four switching modes of this case are described below.

3.2.1.1 Mode-I $(0 < t \leq \varphi_1 T_s)$

In this mode of operation, S_1 and S_2 conduct and S_3 does not conduct as shown in Figure 3.3. The diode D_1 is in reverse bias and D_2 is in forward bias. Therefore, the two identical capacitors are in parallel and the voltage across the identical capacitor (C) becomes v_C. The

currents $i_{L_i}(t)$ and $i_{L_1}(t)$ respectively through L_i and L_1 increase as shown in Figure 3.2. The current $i_{L_2}(t)$ through L_2 decreases during this mode as shown in Figure. 3.2.

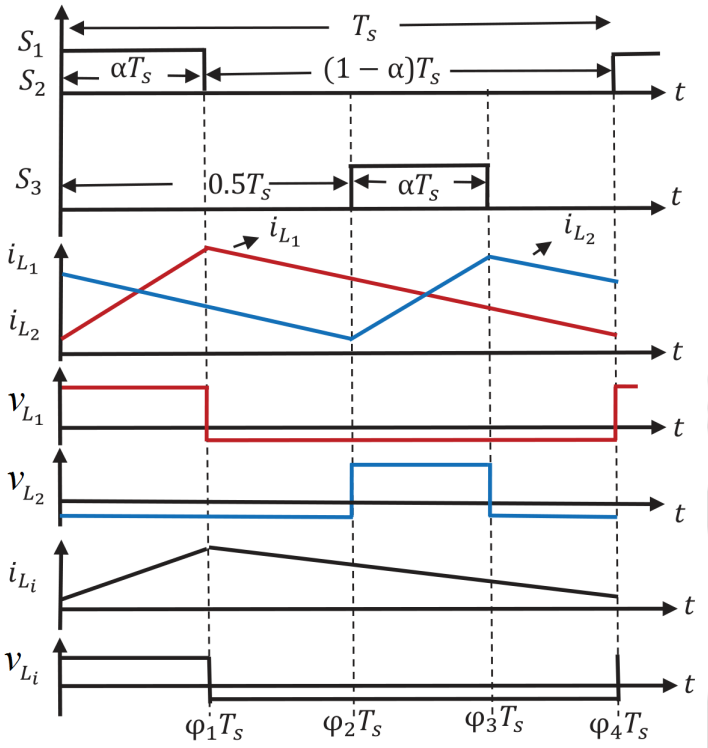


Figure 3.2: Idealized waveform of the proposed HSDIBuC when $\alpha \in (0, 0.5]$

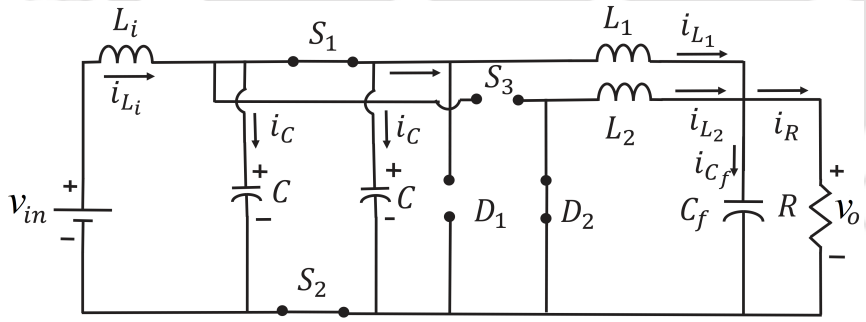


Figure 3.3: Mode-I operation of HSDIBuC

v_{L_i}, v_{L_1} and v_{L_2} are voltages across the inductors L_i, L_1 and L_2 respectively and are expressed as follows.

$$v_{L_i} = L_i \frac{di_{L_i}}{dt} = v_{in} - v_C \tag{3.1}$$

$$v_{L_1} = L_1 \frac{di_{L_1}}{dt} = v_C - v_o \tag{3.2}$$

$$v_{L_2} = L_2 \frac{di_{L_2}}{dt} = -v_o \tag{3.3}$$

The current $i_C(t)$ through the identical capacitors (C) is derived as follows.

$$2i_C(t) = i_{L_i}(t) - i_{L_1}(t) \tag{3.4}$$

The current $i_R(t)$ through the load R is determined as follows.

$$i_R(t) = i_{L_1}(t) + i_{L_2}(t) - i_{C_f}(t) \tag{3.5}$$

where $i_{C_f}(t)$ is the current flowing through the capacitor C_f. The voltage, v_{C_f}, across the capacitor C_f is

$$v_{C_f} = v_o = Ri_R(t) \tag{3.6}$$

The voltage, v_{S_3}, across the S_3 becomes the voltage across the identical capacitor and is expressed by

$$v_{S_3} = v_C \tag{3.7}$$

The voltage, v_{D_1}, across the D_1 is

$$v_{D_1} = v_C \tag{3.8}$$

3.2.1.2 Mode-II ($\varphi_1 T_s < t \leq \varphi_2 T_s$)

During this switching period, S_1 and S_2 do not conduct. Therefore, the two identical capacitors are in series through diode D_1 as shown in Figure 3.4. The resultant voltage across the capacitors becomes $v_C + v_C = 2v_C$. S_3 does not conduct and the current $i_{C_f}(t)$ free-wheels through the diode D_2.

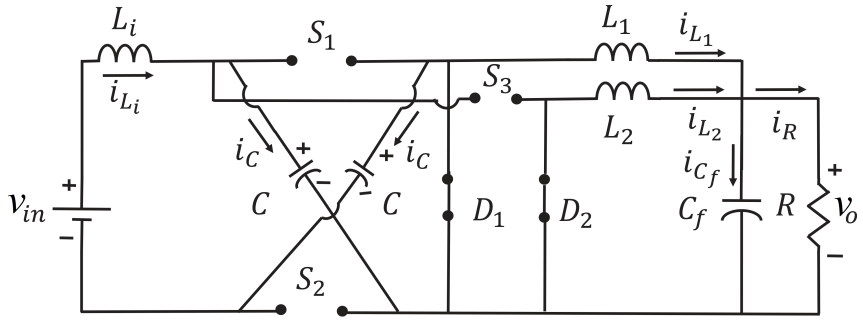


Figure 3.4: Mode-II operation of HSDIBuC

The voltage and current equations are as follows.

$$v_{L_i} = L_i \frac{di_{L_i}(t)}{dt} = v_{in} - 2v_C \tag{3.9}$$

$$v_{L_1} = v_{L_2} = -v_o \tag{3.10}$$

$$i_C(t) = i_{L_i}(t) \tag{3.11}$$

The equations of load current $i_R(t)$ and the output capacitor voltage v_{C_f} are the same as Equations (3.5) and (3.6) respectively. The equations of voltages v_{S_1}, v_{S_2} and v_{S_3} across the S_1, S_2 and S_3 respectively are the same as Equation (3.7).

3.2.1.3 Mode-III ($\varphi_2 T_s < t \leq \varphi_3 T_s$)

In this mode, S_1 and S_2 remain in non-conducting mode. Now, S_3 conducts and D_2 is in reverse bias as shown in Figure 3.5. The voltage, v_{L_i}, across L_i is the same as Equation (3.9). The equations of $i_R(t)$ and v_{C_f} are the same as Equations (3.5) and (3.6) respectively.

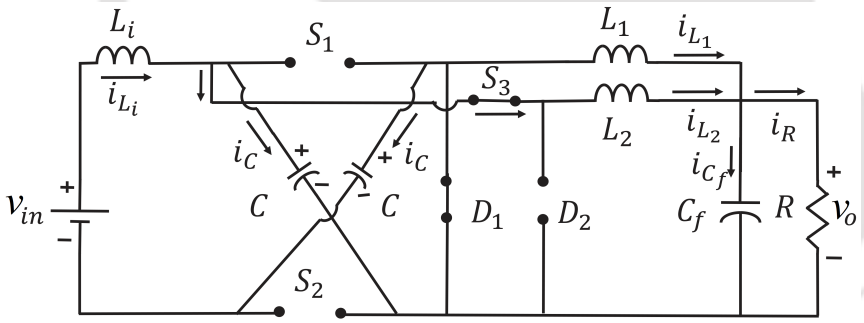


Figure 3.5: Mode-III operation of HSDIBuC

The voltages across L_1 and L_2 are as follows:

$$v_{L_1} = -v_o \tag{3.12}$$

$$v_{L_2} = v_C - v_o \tag{3.13}$$

The current, $i_C(t)$, through the identical capacitors is

$$i_C(t) = i_{L_i}(t) - i_{L_2}(t) \tag{3.14}$$

The equations of v_{S_1} and v_{S_2} are the same as Equation (3.7). The voltage v_{D_2} across D_2 is

$$v_{D_2} = v_C \tag{3.15}$$

3.2.1.4 Mode-IV ($\varphi_3 T_s < t \leq \varphi_4 T_s$)

In this duration, all the three switches are OFF. The voltage and current equations are the same as Mode-II operation when $\alpha \in (0, 0.5]$.

3.2.2 Switching modes when $\alpha \in (0.5, 1)$

When α belongs to $(0.5, 1)$, for two specific time durations, all the three switches conduct as shown in Figure 3.6. This case has also four switching intervals as in the case of $\alpha \in (0, 0.5]$, and are discussed below.

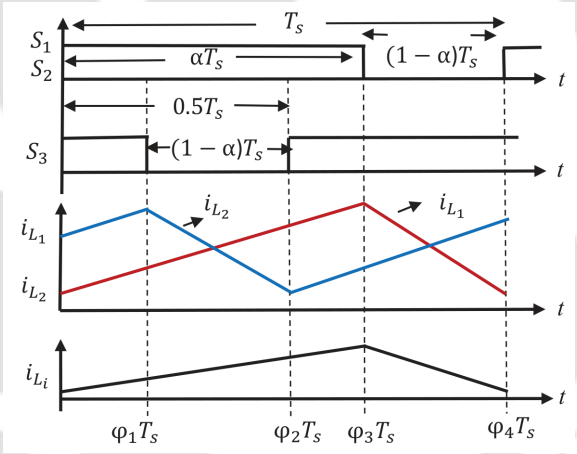


Figure 3.6: Idealized waveform of the proposed HSDIBuC when $\alpha \in (0.5, 1)$

3.2.2.1 Mode-1 ($0 < t \leq \varphi_1 T_s$)

During this switching interval, all the three switches conduct and the diodes D_1 and D_2 are in reverse bias as shown in Figure 3.7. The currents $i_{L_i}(t)$, $i_{L_1}(t)$ and $i_{L_2}(t)$ increase in this interval as shown in Figure 3.6. The voltage and current equations are as follows.

$$v_{L_1} = v_{L_2} = v_C - v_o \tag{3.16}$$

$$2i_C(t) = i_{L_i}(t) - i_{L_1}(t) - i_{L_2}(t) \tag{3.17}$$

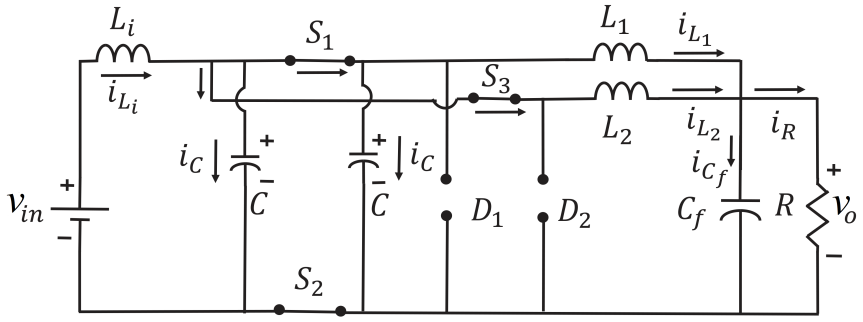


Figure 3.7: Mode-1 operation of HSDIBuC

The equation of v_{L_i} is the same as Equation (3.1). The equations of $i_R(t)$ and v_{C_f} are the same as Equations (3.5) and (3.6) respectively. The equations of v_{D_1} and v_{D_2} are the same as Equation (3.15).

3.2.2.2 Mode-2 ($\varphi_1 T_s < t \leq \varphi_2 T_s$)

In this switching interval, S_1 and S_2 conduct and S_3 does not conduct. During this interval, the switching operation is similar to Mode-I operation while $\alpha \in (0, 0.5]$.

3.2.2.3 Mode-3 ($\varphi_2 T_s < t \leq \varphi_3 T_s$)

During this interval, all the three switches conduct as shown in Figure 3.7 and the switching operation is as Mode-1 while $\alpha \in (0.5, 1)$.

3.2.2.4 Mode-4 ($\varphi_3 T_s < t \leq \varphi_4 T_s$)

In this switching interval, S_1 and S_2 do not conduct but S_3 conducts. The switching operation of this mode is similar to Mode-III while $\alpha \in (0, 0.5]$.

3.3 Voltage Conversion Ratio

As the conversion ratio is the same for the conditions $\alpha \in (0, 0.5]$ and $\alpha \in (0.5, 1)$, the analysis is done when for $\alpha \in (0, 0.5]$ only. By using the principle of inductor voltage second balance (VSB), the DC conversion ratio of the proposed converter is derived. The VSB equation of L_i is as follows.

$$\int_0^{\varphi_1 T_s} v_{L_i} dt + \int_{\varphi_1 T_s}^{\varphi_2 T_s} v_{L_i} dt + \int_{\varphi_2 T_s}^{\varphi_3 T_s} v_{L_i} dt + \int_{\varphi_3 T_s}^{\varphi_4 T_s} v_{L_i} dt = 0 \tag{3.18}$$

By solving Equation (3.18), it is found that $v_{in} = (2-\alpha)v_C$. Now, the VSB equation of L_1 is given by

$$\int_0^{\varphi_1 T_s} v_{L_1} dt + \int_{\varphi_1 T_s}^{\varphi_2 T_s} v_{L_1} dt + \int_{\varphi_2 T_s}^{\varphi_3 T_s} v_{L_1} dt + \int_{\varphi_3 T_s}^{\varphi_4 T_s} v_{L_1} dt = 0 \tag{3.19}$$

Equation (3.19) yields $v_o = \alpha v_C$. Thus, from Equations (3.18) and (3.19), the voltage conversion ratio of the proposed HSDIBuC is determined as

$$M = \frac{v_o}{v_{in}} = \frac{\alpha}{2-\alpha} \tag{3.20}$$

Thus, the proposed HSDIBuC has the higher step-down conversion ratio compared to the CIBuC which has $M = \alpha$ [121].

3.4 Average and Ripple Currents in Inductors

The currents through L_1, L_2 and L_i are expressed as $\int_0^{T_s} di_{L_1}(t) = \int_0^{T_s} \frac{v_{L_1}}{L_1} dt$, $\int_0^{T_s} di_{L_2}(t) = \int_0^{T_s} \frac{v_{L_2}}{L_2} dt$ and $\int_0^{T_s} di_{L_i} = \int_0^{T_s} \frac{v_{L_i}}{L_i} dt$. The average inductor current and the ripple are determined for the following two cases.

3.4.1 Case I, $\alpha \in (0, 0.5]$

In the switching interval $0 < t \leq \varphi_1 T_s$, as shown in Figure 3.2, the instantaneous values $i_{L_1}(\varphi_1 T_s)$, $i_{L_2}(\varphi_1 T_s)$ and $i_{L_i}(\varphi_1 T_s)$ are determined as

$$i_{L_1}(\varphi_1 T_s) = \frac{1}{L_1} \int_0^{\varphi_1 T_s} v_{L_1} dt + i_{L_1}(0) = \frac{(1-\alpha)T_s}{L_1} v_o + i_{L_1}(0) \tag{3.21}$$

$$i_{L_2}(\varphi_1 T_s) = i_{L_2}(0) + \frac{1}{L_2} \int_0^{\varphi_1 T_s} v_{L_2} dt = i_{L_2}(0) - \frac{\alpha T_s}{L_2} v_o \tag{3.22}$$

$$i_{L_i}(\varphi_1 T_s) = \frac{1}{L_i} \int_0^{\varphi_1 T_s} v_{L_i} dt + i_{L_i}(0) = \frac{(1-\alpha)T_s}{L_i} v_o + i_{L_i}(0) \tag{3.23}$$

where $i_{L_i}(0)$, $i_{L_1}(0)$ and $i_{L_2}(0)$ are the initial inductor currents at $t = 0$. In the next switching interval $\varphi_1 T_s < t \leq \varphi_2 T_s$, the instantaneous values $i_{L_1}(\varphi_2 T_s)$, $i_{L_2}(\varphi_2 T_s)$ and $i_{L_i}(\varphi_2 T_s)$ are

derived as follows.

$$\begin{aligned} i_{L_1}(\varphi_2 T_s) &= i_{L_1}(\varphi_1 T_s) + \frac{1}{L_1}\int_{\varphi_1 T_s}^{\varphi_2 T_s} v_{L_1} dt \\ &= i_{L_1}(\varphi_1 T_s) - \frac{(0.5-\alpha)T_s}{L_1} v_o = \frac{0.5T_s}{L_1} v_o + i_{L_1}(0) \end{aligned} \tag{3.24}$$

$$\begin{aligned} i_{L_2}(\varphi_2 T_s) &= i_{L_2}(\varphi_1 T_s) + \frac{1}{L_2}\int_{\varphi_1 T_s}^{\varphi_2 T_s} v_{L_2} dt \\ &= i_{L_2}(\varphi_1 T_s) - \frac{(0.5-\alpha)T_s}{L_2} v_o = i_{L_2}(0) - \frac{0.5T_s}{L_2} v_o \end{aligned} \tag{3.25}$$

$$\begin{aligned} i_{L_i}(\varphi_2 T_s) &= i_{L_i}(\varphi_1 T_s) + \frac{1}{L_i}\int_{\varphi_1 T_s}^{\varphi_2 T_s} v_{L_i} dt \\ &= i_{L_i}(\varphi_1 T_s) - \frac{(0.5-\alpha)T_s}{L_i} v_o = \frac{0.5T_s}{L_i} v_o + i_{L_i}(0) \end{aligned} \tag{3.26}$$

In the following interval $\varphi_2 T_s < t \leq \varphi_3 T_s$, the instantaneous values $i_{L_1}(\varphi_3 T_s)$, $i_{L_2}(\varphi_3 T_s)$ and $i_{L_i}(\varphi_3 T_s)$ are as follows.

$$\begin{aligned} i_{L_1}(\varphi_3 T_s) &= i_{L_1}(\varphi_2 T_s) + \frac{1}{L_1}\int_{\varphi_2 T_s}^{\varphi_3 T_s} v_{L_1} dt \\ &= i_{L_1}(\varphi_2 T_s) - \frac{\alpha T_s}{L_1} v_o = \frac{(0.5-\alpha)T_s}{L_1} v_o + i_{L_1}(0) \end{aligned} \tag{3.27}$$

$$\begin{aligned} i_{L_2}(\varphi_3 T_s) &= i_{L_2}(\varphi_2 T_s) + \frac{1}{L_2}\int_{\varphi_2 T_s}^{\varphi_3 T_s} v_{L_2} dt \\ &= i_{L_2}(\varphi_2 T_s) + \frac{(1-\alpha)T_s}{L_2} v_o = \frac{(0.5-\alpha)T_s}{L_2} v_o + i_{L_2}(0) \end{aligned} \tag{3.28}$$

$$\begin{aligned} i_{L_i}(\varphi_3 T_s) &= i_{L_i}(\varphi_2 T_s) + \frac{1}{L_i}\int_{\varphi_2 T_s}^{\varphi_3 T_s} v_{L_i} dt \\ &= i_{L_i}(\varphi_2 T_s) - \frac{\alpha T_s}{L_i} v_o = \frac{(0.5-\alpha)T_s}{L_i} v_o + i_{L_i}(0) \end{aligned} \tag{3.29}$$

During the subsequent interval $\varphi_3 T_s < t \leq \varphi_4 T_s$, the instantaneous values $i_{L_1}(\varphi_4 T_s)$, $i_{L_2}(\varphi_4 T_s)$ and $i_{L_f}(\varphi_4 T_s)$ are as follows.

$$\begin{aligned} i_{L_1}(\varphi_4 T_s) &= i_{L_1}(\varphi_3 T_s) + \frac{1}{L_1}\int_{\varphi_3 T_s}^{\varphi_4 T_s} v_{L_1} dt \\ &= i_{L_1}(\varphi_3 T_s) - \frac{(0.5-\alpha)T_s}{L_1} v_o = i_{L_1}(0) \end{aligned} \tag{3.30}$$

$$\begin{aligned} i_{L_2}(\varphi_4 T_s) &= i_{L_2}(\varphi_3 T_s) + \frac{1}{L_2}\int_{\varphi_3 T_s}^{\varphi_4 T_s} v_{L_2} dt \\ &= i_{L_2}(\varphi_3 T_s) - \frac{(0.5-\alpha)T_s}{L_2} v_o = i_{L_2}(0) \end{aligned} \tag{3.31}$$

$$\begin{aligned} i_{L_f}(\varphi_4 T_s) &= i_{L_i}(\varphi_3 T_s) + \frac{1}{L_i}\int_{\varphi_3 T_s}^{\varphi_4 T_s} v_{L_i} dt \\ &= i_{L_i}(\varphi_3 T_s) - \frac{(0.5-\alpha)T_s}{L_i} v_o = i_{L_i}(0) \end{aligned} \tag{3.32}$$

The average inductor current I_L through the inductors L_1 and L_2 is equal as these inductors are identical. By using Equations (3.21)−(3.32), I_L is derived as follows.

$$\begin{aligned} I_L &= \frac{i_{L_1}(0) + i_{L_1}(\varphi_1 T_s)}{2}\alpha + \frac{i_{L_1}(\varphi_1 T_s) + i_{L_1}(\varphi_2 T_s)}{2}(0.5-\alpha) \\ &\quad + \frac{i_{L_1}(\varphi_2 T_s) + i_{L_1}(\varphi_3 T_s)}{2}\alpha + \frac{i_{L_1}(\varphi_3 T_s) + i_{L_1}(\varphi_4 T_s)}{2}(0.5-\alpha) \\ &= \frac{(1-\alpha)T_s}{2L_1} v_o + i_{L_1}(0) \end{aligned} \tag{3.33}$$

Similarly, the average current I_{L_i} through the L_i is expressed as

$$I_{L_i} = \frac{(1-\alpha)T_s}{2L_i} v_o + i_{L_i}(0) \tag{3.34}$$

As the inductors L_1 and L_2 are identical ($L_1 = L_2 = L$), the ripple in inductor current, Δi_L, is determined as follows.

$$\Delta i_L = \frac{(1-\alpha)T_s}{L} v_o = \frac{(1-\alpha)\alpha T_s v_{in}}{(2-\alpha)L} \tag{3.35}$$

The ripple in inductor current, Δi_{L_i}, of L_i is derived as

$$\Delta i_{L_i} = \frac{(1-\alpha)T_s}{L_i} v_o = \frac{(1-\alpha)\alpha T_s v_{in}}{(2-\alpha)L} \tag{3.36}$$

3.4.2 Case II, $\alpha \in (0.5, 1)$

In this case of operation, the expressions of average inductor currents I_L and I_{L_i} are the same as in Equations (3.33) and (3.34) respectively. The ripple currents Δi_L and Δi_{L_i} are also the same as in Equations (3.35) and (3.36) respectively.

3.5 Boundary Load between CCM and DCM

3.5.1 Case I, $\alpha \in (0, 0.5]$

At the boundary condition ($i_{L_i}(0) = i_{L_i}(\varphi_4 T_s) = 0$), Equation (3.34) becomes $I_{L_i} = \frac{(1-\alpha)T_s}{2L_i} v_o$. The inductor current I_{L_i} is the same as the input current I_{in}. Therefore, it is defined by $I_{L_i} = i_{in} = \frac{v_o}{v_{in}} i_o = \frac{\alpha}{(2-\alpha)} i_o$. Therefore, the boundary load (R_{B_i}) equation for L_i is derived as follows.

$$R_{B_i} = \frac{v_o}{i_{OB}} = \frac{2L_i\alpha}{(1-\alpha)(2-\alpha)T_s} \tag{3.37}$$

where I_{OB} is the output boundary load current. By calculating the boundary load R_{B_i} from Equation (3.37), the minimum inductance value required for the two identical inductors at the output is determined. From Equation (3.33), I_L is expressed as $I_L = \frac{(1-\alpha)T_s}{2L} v_o$ at the boundary condition $i_{L_1}(0) = i_{L_1}(\varphi_4 T_s) = 0$. At the load R_{B_i}, the boundary current I_{OB} due to the inductor currents I_{L_1} and I_{L_2} is derived as

$$\begin{aligned} i_{OB} &= I_{L_1} + I_{L_2} = 2I_L = \frac{(1-\alpha)T_s}{L} v_o \\ R_{B_i} &= \frac{v_o}{i_{OB}} = \frac{L}{(1-\alpha)T_s} \end{aligned} \tag{3.38}$$

Therefore, from Equation (3.38), the minimum inductance value for the boundary load (R_{B_i}) is derived as follows.

$$min\{L = L_1 = L_2\} = R_{B_i}(1-\alpha)T_s \tag{3.39}$$

3.5.2 Case II, $\alpha \in (0.5, 1)$

The expression of the boundary load R_{B_i} is the same as Equation (3.37) and minimum inductance value ($L_1 = L_2 = L$) for the load (R_{B_i}) is the same as Equation (3.39).

3.6 Ripple in Input Current

Let us consider that the duty ratio and ripple in input current of CIBuC are α_b and Δi_b respectively. For the proposed HSDIBuC, duty ratio and input ripple are denoted by α and Δi respectively. The ripple in input current of CIBuC is as follows.

$$\Delta i_b = \frac{(1-\alpha_b)T_s}{L} v_o \tag{3.40}$$

The ripple in input current of the proposed HSDIBuC is as follows.

$$\Delta i = \frac{(1-\alpha)T_s}{L_i} v_o \tag{3.41}$$

Considering $L = L_i$, from Equations (3.40) and (3.41), the relation between ΔI_b and ΔI is derived as follows.

$$\frac{\Delta i}{\Delta i_b} = \frac{(1-\alpha)}{(1-\alpha_b)} \tag{3.42}$$

While both converter has equal input and output voltages, the relation between two duty ratios is

$$\alpha = \frac{2\alpha_b}{1+\alpha_b} \tag{3.43}$$

Now substituting Equations (3.43) into (3.42), the following relation is obtained.

$$\frac{\Delta i}{\Delta i_b} = \frac{1}{(1+\alpha_b)} \tag{3.44}$$

Equation (3.44) shows that the proposed HSDIBuC has less ripple in input current than that in CIBuC.

3.7 Design of Identical Capacitors ($C_1 = C_2 = C$)

The idealized waveform of charging and discharging of identical capacitors is shown in Figure 3.8. During the time interval $t_0 < t \leq t_3$, the switches S_1 and S_2 do not conduct. During this

entire interval, the two identical capacitors C_1 and C_2 are charged in series by the input voltage v_{in}, and the resultant voltage becomes $(v_C + v_C = 2v_C)$.

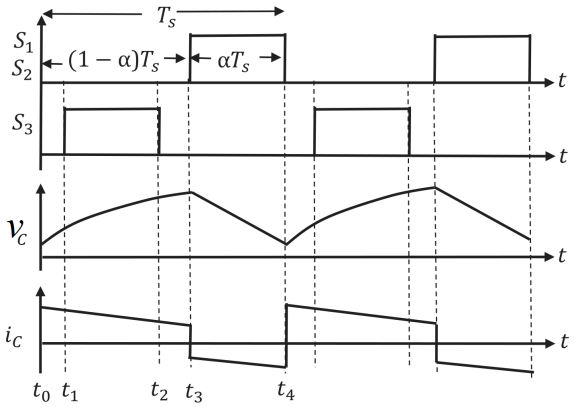


Figure 3.8: Charging and discharging of identical capacitors $(C_1 = C_2 = C)$ in ideal case

In the time interval $t_3 < t \leq t_4$, S_1 and S_2 conduct. In this duration, the identical capacitors are in parallel $(v_{C_1} = v_{C_2} = v_C)$ to each other and discharge their energies to the load side. Therefore, when S_1 and S_2 both conduct, the power released by these two capacitors is equal to the load power, and the energy equation is defined as follows.

$$\begin{aligned} \frac{1}{2}C(v_{Cmax}^2 - v_{Cmin}^2) &= \frac{1}{2}\frac{v_o^2}{R}\alpha T_s \\ \Longrightarrow \quad \frac{C(v_{Cmax} + v_{Cmin})(v_{Cmax} - v_{Cmin})}{\alpha T_s} &= \frac{v_o^2}{R} \end{aligned} \tag{3.45}$$

The average voltage of v_C is approximated as

$$\frac{v_{Cmax} + v_{Cmin}}{2} = v_C = \frac{v_o}{\alpha} \tag{3.46}$$

The peak-to-peak ripple voltage of identical capacitors is defined by

$$\Delta v_C = v_{Cmax} - v_{Cmin} \tag{3.47}$$

By substituting Equations (3.46) and (3.47) into (3.45), the minimum capacitance value required for identical capacitors is derived as

$$C_{min} = \frac{\alpha^2 T_s}{2\Delta v_C}\frac{v_o}{R} \tag{3.48}$$

3.8 Voltage and Current Stresses

To simplify the analysis of voltage stress, the capacitive ripple voltages are neglected. v_{S_1}, v_{S_2} and v_{S_3} are the voltage stresses of the switches S_1, S_2 and S_3 respectively. The maximum voltage stresses of the switches are defined as follows.

$$v_{S_1} = v_{S_2} = v_{S_3} = v_C = \frac{v_{in}}{2-\alpha} \tag{3.49}$$

Equation (3.49) shows that the proposed HSDIBuC can be implemented using switches with lower input voltage rating and higher ON resistance $r_{DS(on)}$. v_{D_1} and v_{D_2} are the diode voltage stresses of diodes D_1 and D_2 respectively. The maximum voltage stresses v_{D_1} and v_{D_2} are defined by

$$v_{D_1} = v_{D_2} = v_C = \frac{v_{in}}{2-\alpha} \tag{3.50}$$

To simplify the current stress analysis, the inductor ripple currents are neglected. The inductors L_1 and L_2 are carrying half of the output current as they are interleaved. Therefore, when $\alpha \in (0, 0.5]$, the switching current i_{S_1} can be approximated as

$$i_{S_1} = \begin{cases} \frac{i_o}{2}, & \text{for } 0 < t \leq \varphi_1 T_s \\ 0, & \text{for } \varphi_1 T_s < t \leq \varphi_4 T_s \end{cases} \tag{3.51}$$

$I_{S_{1rms}}$, $I_{S_{2rms}}$ and $I_{S_{3rms}}$ denote the root mean square (rms) currents of the switches S_1, S_2 and S_3 respectively. By using Equation (3.51), the rms current through the switch S_1 is determined as follows.

$$I_{S_{1rms}} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_{S_1}^2 dt} = \frac{i_o\sqrt{\alpha}}{2} \tag{3.52}$$

The expression of the $I_{S_{2rms}}$ and $I_{S_{3rms}}$ is the same as Equation (3.52). When $\alpha \in (0, 0.5]$, the diode current i_{D_1} through the diode D_1 is approximated as

$$i_{D_1} = \begin{cases} 0, & \text{for } 0 < t \leq \varphi_1 T_s \\ \frac{i_o}{2}, & \text{for } \varphi_1 T_s < t \leq \varphi_4 T_s \end{cases} \tag{3.53}$$

By using Equation (3.53), the rms current $I_{D_{1rms}}$ through diode D_1 is derived as follows.

$$I_{D_{1rms}} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_{D_1}^2 dt} = \frac{i_o\sqrt{(1-\alpha)}}{2} \tag{3.54}$$

The expression of rms current $I_{D_{2rms}}$ through the diode D_2 is the same as given in Equation (3.54). By using Equation (3.53), the average diode current I_{D_1} through D_1 is calculated as

$$I_{D_1} = \frac{1}{T_s}\int_0^{T_s} i_{D_1} dt = \frac{i_o(1-\alpha)}{2} \tag{3.55}$$

The average current I_{D_2} through the diode D_2 is given in Equation (3.55). The voltage and current stresses of the proposed HSDIBuC are compared among the existing interleaved topologies in Table 3.1. In Table 3.1, the switch S_3 of proposed HSDIBuC works in the same configuration as switch S_2 of the CIBuC and existing topologies.

Table 3.1: Comparisons of voltage and current stresses among the existing and the proposed IBuCs

Items	CIBuC	Compare	Proposed HSDIBuC	Compare	Existing [122]
Voltage gain	α	$>$	$\frac{\alpha}{2-\alpha}$	$>$	$\frac{\alpha}{2}$
Voltage stress v_{S_1}, v_{S_2}	v_{in}	$>$	$\frac{v_{in}}{2-\alpha}$	$>$	$\frac{v_{in}}{2}$
Voltage stress v_{S_3}	v_{in}	$>$	$\frac{v_{in}}{2-\alpha}$	$<$	v_{in}
Voltage stress v_{D_1}, v_{D_2}	v_{in}	$>$	$\frac{v_{in}}{2-\alpha}$	$>$	$\frac{v_{in}}{2}$
RMS current stress $I_{S_{rms}}$	$\frac{i_o}{2}\sqrt{\frac{\alpha}{2}}$	$<$	$\frac{i_o\sqrt{\alpha}}{2}$	$=$	$\frac{i_o\sqrt{\alpha}}{2}$
Average current stress I_{D_1}	$\frac{i_o}{2}(1-\frac{\alpha}{2})$	$>$	$\frac{i_o}{2}(1-\alpha)$	$=$	$\frac{i_o}{2}(1-\alpha)$
Average current stress I_{D_2}	$\frac{i_o}{2}(1-\frac{\alpha}{2})$	$>$	$\frac{i_o}{2}(1-\alpha)$	$<$	$\frac{i_o}{2}$
Ripple Δi_L	$\frac{(1-\alpha)\alpha T_s v_{in}}{L}$	$>$	$\frac{(1-\alpha)\alpha T_s v_{in}}{(2-\alpha)L}$	$<$	$\frac{(1-\alpha)\alpha T_s v_{in}}{L}$

3.9 Power Losses and Efficiency Analysis

The conduction losses are calculated by the resistances of semiconductor devices and parasitics of the inductors by assuming all the capacitors to be ideal [84]. Let us assume that all the three switches have equal ON-state resistance $r_{DS(on)}$. Therefore, by using Equation (3.52),

the conduction losses ($P_{r_{DS(on)}}$) due to the three switches are determined as follows [117].

$$P_{r_{DS(on)}} = r_{DS(on)} \left(I_{S_{1rms}}^2 + I_{S_{2rms}}^2 + I_{S_{3rms}}^2 \right) = r_{DS(on)} \frac{3 i_o^2 \alpha}{4} \tag{3.56}$$

Assuming the transistor output capacitance C_O to be linear, the switching loss is analyzed [116]. During the transistor *turn-off transition* the drain to source voltage rises from nearly zero to $v_C = v_{in}/(2-\alpha)$. Therefore, the *turn-off transition* switching power loss is derived as

$$P_{turn-off} = \frac{1}{2} \frac{C_O v_C^2}{T_s} \tag{3.57}$$

During the *turn-on* transition, the drain-to-source voltage falls from v_C to nearly zero. Therefore, the *turn-on* switching power loss is determined as follows.

$$P_{turn-on} = \frac{1}{2} \frac{C_O v_C^2}{T_s} \tag{3.58}$$

By using Equations (3.57) and (3.58), the total switching losses for the three switches are expressed as follows.

$$P_S = 3(P_{turn-off} + P_{turn-on}) = 3 \frac{C_O v_C^2}{T_s} = 3 \frac{C_O v_o^2}{\alpha^2 T_s} \tag{3.59}$$

It is assumed that the diode conduction resistance r_D is equal for D_1 and D_2. By using Equation (3.54), the conduction loss P_{r_D} due to r_D is calculated as

$$P_{r_D} = r_D \left(I_{D_{1rms}}^2 + I_{D_{2rms}}^2 \right) = r_D \frac{i_o^2 (1-\alpha)}{2} \tag{3.60}$$

The forward bias voltage of the diodes D_1 and D_2 is denoted by v_{fd}. By using Equation (3.55), the power losses associated with the diodes are determined as

$$P_{v_{fd}} = v_{fd} \left(I_{D_1} + I_{D_2} \right) = v_{fd} i_o (1-\alpha) \tag{3.61}$$

The input current of the proposed HSDIBuC at lossless condition is $i_{in} = \frac{\alpha}{2-\alpha} i_o$. Therefore, the loss $P_{r_{Li}}$ due to equivalent series resistance r_{L_i} of L_i is derived as

$$P_{r_{Li}} = r_{L_i} i_{in}^2 = r_{L_i} \left(\frac{\alpha}{2-\alpha} i_o \right)^2 \tag{3.62}$$

If the rms currents of L_1 and L_2 are approximated by $I_{L_{1rms}} = I_{L_{2rms}} = \frac{i_o}{2}$, the losses due to r_L of L_1 and L_2 are

$$P_{r_L} = r_L \frac{i_o^2}{2} \tag{3.63}$$

By using Equations (3.56) to (3.63), the total loss equation is provided as

$$P_{Loss} = P_{r_{DS(on)}} + P_S + P_{r_D} + P_{v_{fd}} + P_{r_{Li}} + P_{r_L} \tag{3.64}$$

The output power is denoted by P_O. From Equation (3.64), the efficiency η is determined as follows.

$$\eta = \frac{P_O}{P_O + P_{Loss}} = \frac{1}{1 + \frac{r_{DS(on)}3\alpha}{4R} + \frac{3C_O R}{\alpha^2 T_s} + \frac{r_D(1-\alpha)}{2R} + \frac{v_{fd}(1-\alpha)}{v_o} + \frac{r_{L_i}\alpha^2}{(2-\alpha)^2 R} + \frac{r_L}{2R}} \tag{3.65}$$

3.10 Selection of Parameters

To design HSDIBuC in CCM, $v_{in} = 20$ V, maximum $v_o = 12$ V, $i_{omax} = 6$ A, $i_{omin} = 0.5$ A and $f_s = 50$ kHz are specified. The range of duty ratio is considered as $0.2 \leq \alpha \leq 0.75$. To calculate the capacitance value of the identical capacitors, the ripple voltage is defined by $\Delta v_C = v_C \times 1\% = (v_o/\alpha) \times 1\%$. The maximum and minimum values of the output power are $P_{omax} = v_o \times I_{omax} = 72$ W and $P_{omin} = v_o \times i_{omin} = 6$ W respectively. The minimum and maximum load resistances are calculated as $R_{max} = v_o/i_{omin} = 24\ \Omega$ and $R_{min} = v_o/i_{omax} = 2\ \Omega$ respectively.

From Equation (3.48), it is seen that C_{min} is inversely proportional to the load resistance R and directly proportional to α. If the output voltage v_o is 12 V, the required duty ratio is $\alpha = 0.75$. Therefore, at $R_{max} = 24\ \Omega$, the minimum capacitance value of identical capacitors is $C_{min} = 17.57\ \mu$F. From Equation (3.37), the requirement of inductance for L_i is derived at $R_{B_i} = R_{min} = 2\ \Omega$ and $\alpha_{min} = 0.20$. Thus, the value of $L_{imin} = 144\ \mu$H. Substituting $R_{B_i} = R_{min} = 2\ \Omega$ and $\alpha_{min} = 0.2$ in Equation (3.39), the minimum inductance value is determined as $L_{min} = L_{1min} = L_{2min} = 32\ \mu$H. For the robust performance, the values of the parameters are taken higher than the minimum values as given in Table 3.2.

Table 3.2: Parameter values of HSDIBuC considered for CCM operation

Parameters	**Value**
Input Voltage (v_{in})	20 V
Switching Frequency (f_s)	50 kHz
Inductance ($L = L_1 = L_2$)	180 μH
Inductive Resistance (r_L)	0.07 Ω
Identical capacitance ($C = C_1 = C_2$)	220 μF
Resistances of C_1 and C_2 ($r_{C_1} = r_{C_2}$)	0.32 Ω
Input-side Inductance (L_i)	180 μH
Output capacitance (C_f)	330 μF
ESR of output capacitor (r_{C_f})	0.22 Ω
MOSFET drain to source on-resistance ($r_{DS(on)}$)	0.075 Ω
MOSFET output capacitance (C_O)	315 pF
Diode forward voltage ($v_D = v_{D_1} = v_{D_2}$)	0.39 V
Diode resistance ($r_D = r_{D_1} = r_{D_2}$)	0.078 Ω

3.11 Simulation Results

The simulation is carried out by using the MATLAB-Simscape tool. The value of the parameters are given in Table 3.2. Figure 3.9 shows the output voltage $v_o = 4.9$ V at $R = 3.33$ Ω and $v_o = 8.5$ V at $R = 5$ Ω respectively for $\alpha = 0.40$ and $\alpha = 0.60$. Figure 3.10 shows the phase shifted currents i_{L_1} and i_{L_2} for $\alpha = 0.40$ and $R = 3.33$ Ω. i_{L_1} and i_{L_2} are provided at ideal condition, i.e. all the parasitics are negligible. In Figure 3.11, capacitive voltage ($v_C = v_{in}/(2 - \alpha) = 12.5$ V) is shown at $\alpha = 0.40$. Figure 3.12 validates the voltage stress equation of the switches provided in Equation (3.49). In Figure 3.13, simulation result of diode voltage stress is provided. v_{D_1} and v_{D_2} validate Equation (3.50) at $\alpha = 0.40$. Figures 3.14 and 3.15 respectively show the variation of efficiency with respect to the load change and duty ratio (α) change. From these analyses, it is seen that the efficiency of HSDIBuC is high.

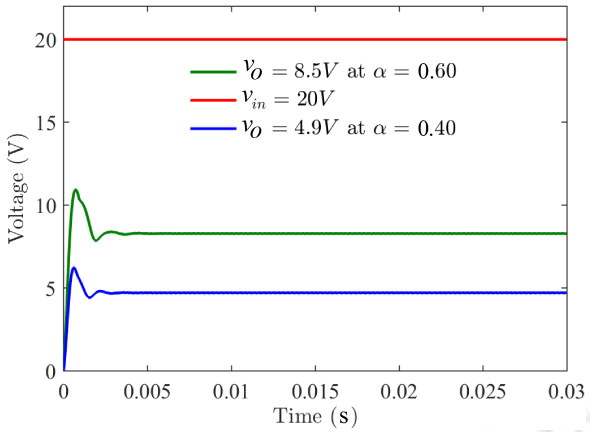


Figure 3.9: Simulation result of the output voltage of the proposed HSDIBuC

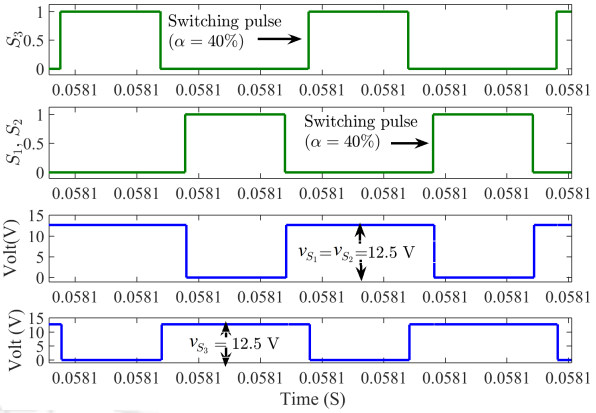


Figure 3.12: Simulation result of voltage stress of switches at $\alpha = 0.40$

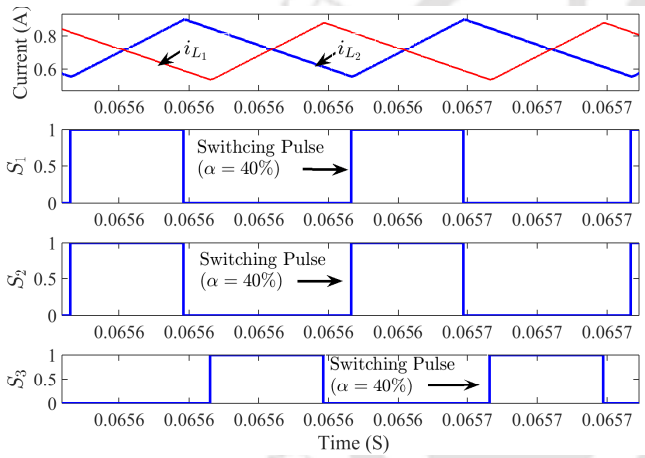


Figure 3.10: Simulation result of two phase shifted currents i_{L_1} and i_{L_2} at $\alpha = 0.40$

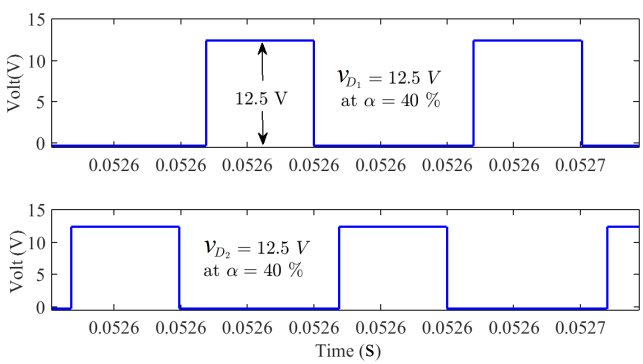


Figure 3.13: Simulation result of voltage stresses of diodes at $\alpha = 0.40$

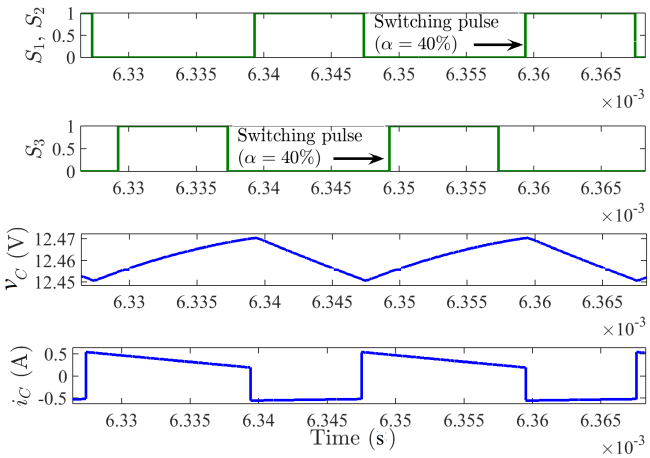


Figure 3.11: Simulation result of v_C at $\alpha = 0.40$

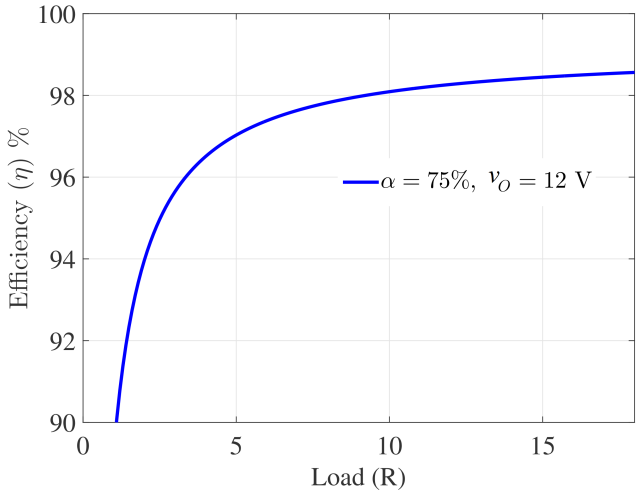


Figure 3.14: Efficiency of HSDIBuC due to change of load resistance R.

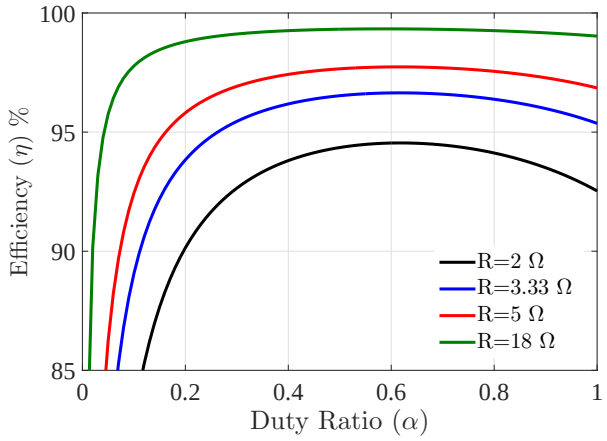


Figure 3.15: Efficiency of HSDIBC due to change of duty ratio α

3.12 Experimental Setup and Results

To verify the proposed HSDIBuC, an experiment is carried out as shown in Figure 3.16 by using the parameters given in Table 3.2. The switches S_1, S_2 and S_3 are implemented by MOSFET IRFP250NPBF. The Schottky diodes D_1 and D_2 are implemented by NTST30100SG/ NFK03TS30100SG. The results are provided for the following two cases.

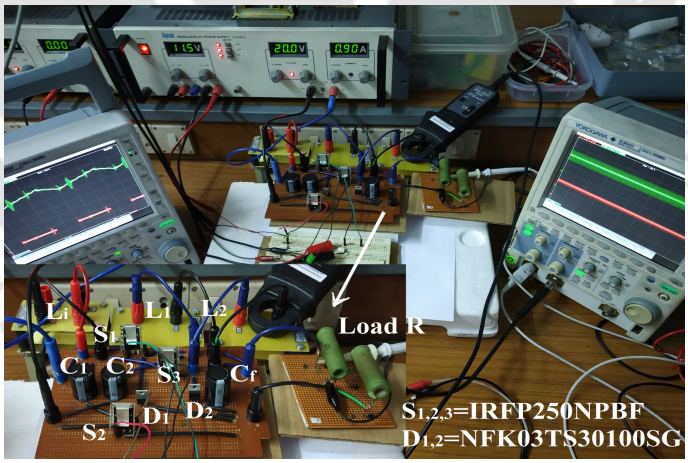
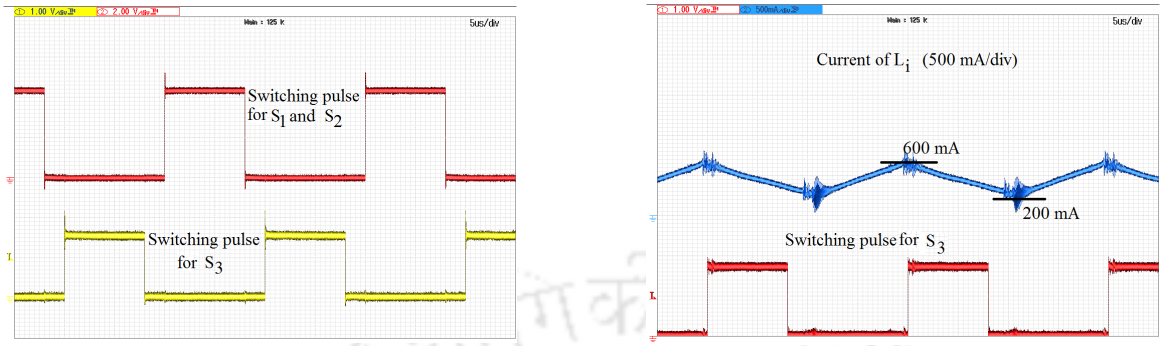


Figure 3.16: Experimental setup of the proposed HSDIBuC

3.12.1 Case I, $\alpha \in (0, 0.5]$

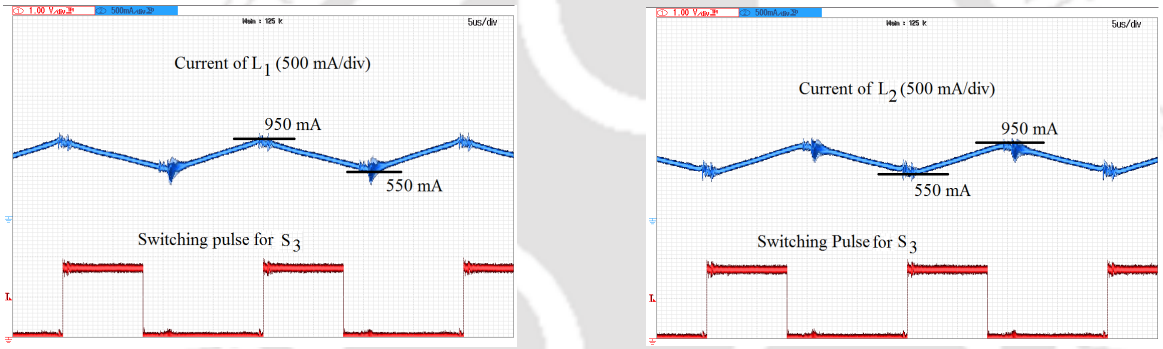
The two-phase shifted switching pulses for $\alpha = 0.40$ are shown in Figure 3.17a. In this experiment, the load resistance $R = 3.33\ \Omega$ is considered. The experimental current waveforms

of i_{L_i}, i_{L_1} and i_{L_2} are shown respectively in Figures 3.17b, 3.18a and 3.18b. The phase shifted waveforms of i_{L_1} and i_{L_2} are shown with respect to the switching pulse for S_3.



(a) (b)

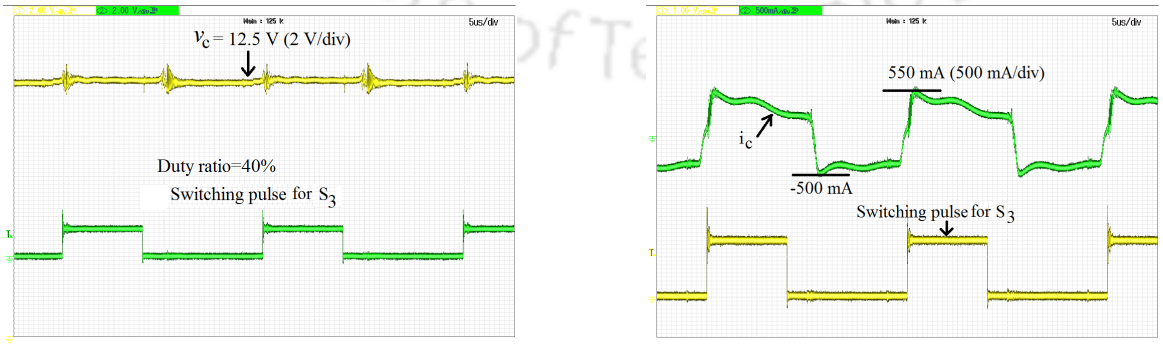
Figure 3.17: Experimental waveform for $\alpha = 0.40$ (a) Two-phase switching pulses, and (b) i_{L_i}



(a) (b)

Figure 3.18: Experimental result of inductor current for $\alpha = 0.40$ (a) i_{L_1}, and (b) i_{L_2}.

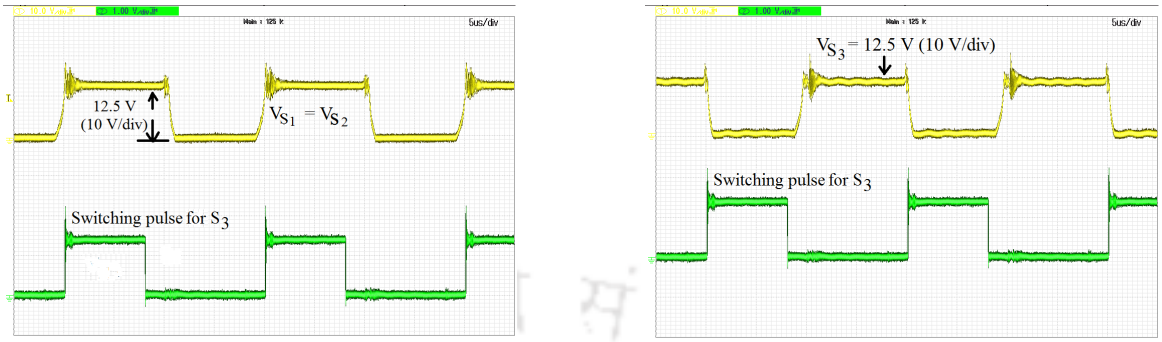
Figure 3.19a shows the capacitive voltage $v_C = 12.5$ V at $\alpha = 0.40$. This result satisfies Equation (3.18). In Figure 3.19b, the capacitive current is provided.



(a) (b)

Figure 3.19: Experimental results for the two identical capacitors for $\alpha = 0.40$ (a) $v_C = 12.5$ V, and (b) i_C

The experimental validation of voltage stresses of switches is shown in Figures 3.20a and 3.20b, and the results are consistent with Equation (3.49).



(a) (b)

Figure 3.20: Experimental switch voltage stresses for $\alpha = 0.40$ (a) $v_{S_1} = v_{S_2} = 12.5$ V, and (b) $v_{S_3} = 12.5$ V

The diode voltage stresses are given in Figure 3.21 and the results verify Equation (3.50). These experimental results verify that the voltage stresses of the switches and the diodes are less than the $v_{in} = 20$ V.

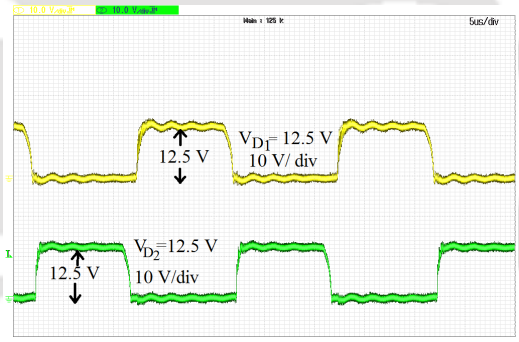
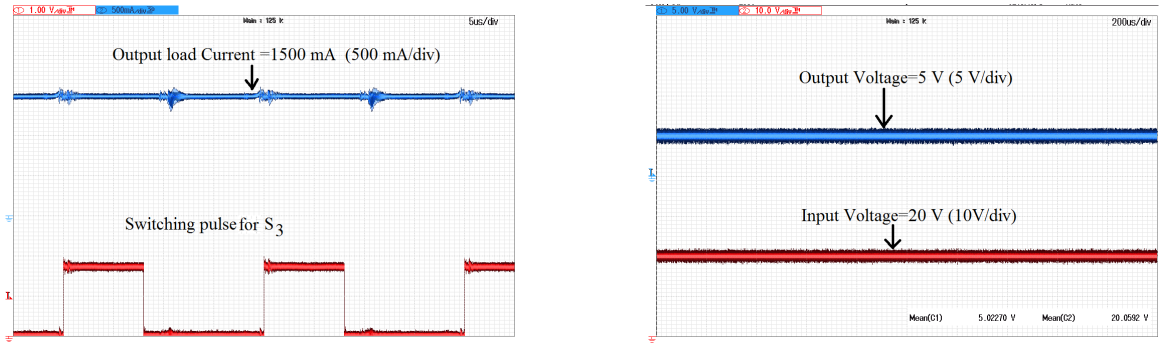


Figure 3.21: Experimental diode voltage stresses $v_{D_1} = v_{D_2} = 12.5$ V for $\alpha = 0.40$

At $R = 3.33\ \Omega$ and $\alpha = 0.40$, the output load current ($i_o = 1500$ mA) is shown in Figure 3.22a. The output voltage $v_o = 5$ V at $\alpha = 0.40$ duty ratio is seen in Figure 3.22b. Therefore, the output power becomes $P_O = 5 \times 1.50 = 7.5$ W. The measured experimental steady state value of i_{in} is 390 mA. Therefore, the input power is $P_{in} = 20 \times 0.39 = 7.8$ W. The efficiency is calculated as $\eta = P_O/P_{in} = 96.15\%$. The experimental result of efficiency due to load change is shown in Figure 3.26a. The load is varied up to 7.5 Ω as it is the boundary load in this case.



(a) (b)

Figure 3.22: Experimental results for $\alpha = 0.40$ (a) $i_o = 1.5$ A, and (b) $v_o = 5$ V

3.12.2 Case II, $\alpha \in (0.5, 1)$

In this experiment, the load resistance $R = 5\ \Omega$ is considered and the duty ratio is $\alpha = 0.60$. The experimental current waveforms of i_{L_i}, i_{L_1} and i_{L_2} are shown respectively in Figures 3.23, 3.24a and 3.24b. The phase shifted waveforms of i_{L_1} and i_{L_2} are shown with respect to the switching pulse for S_3.

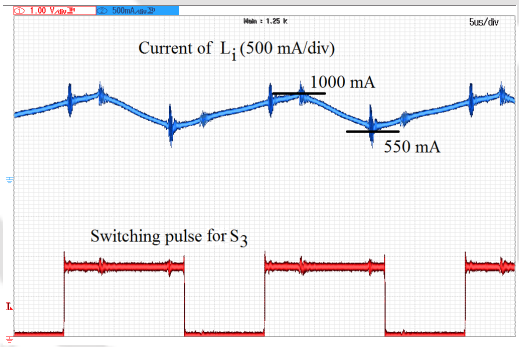
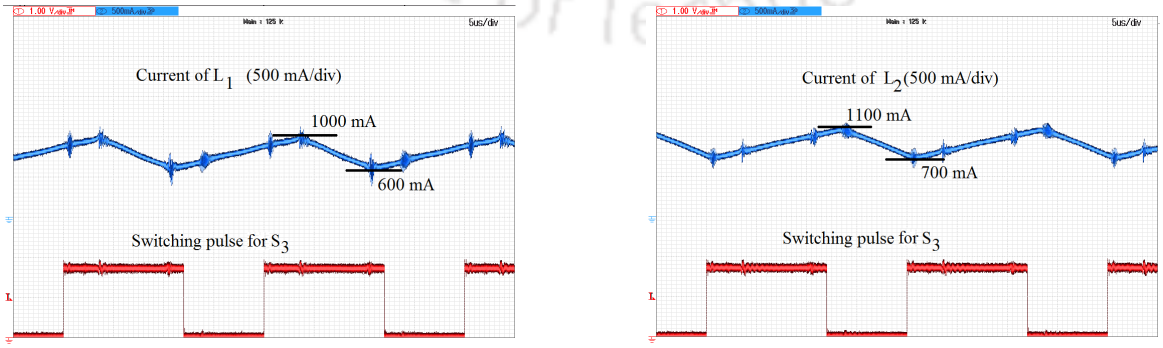


Figure 3.23: Experimental result of inductor current i_{L_i} for $\alpha = 0.60$



(a) (b)

Figure 3.24: Experimental results for $\alpha = 0.60$ (a) i_{L_1}, and (b) i_{L_2}

The output voltage $v_o = 8.5$ V at $\alpha = 0.60$ is shown in Figure 3.25. The experimental result of efficiency versus load change and duty ratio are shown in Figures 3.26a and 3.26b respectively. The efficiency is measured to be $\eta = P_O/P_{in} = 14.45/15 = 96.33\%$.

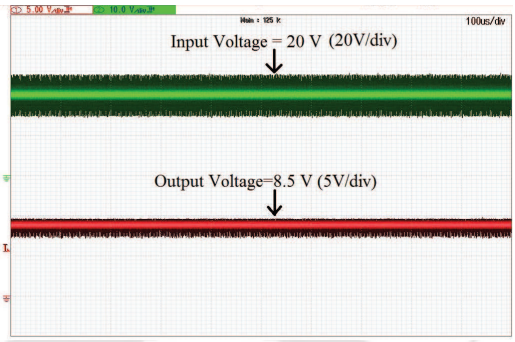


Figure 3.25: Experimental output voltage $v_o = 8.5$ V for $\alpha = 0.60$.

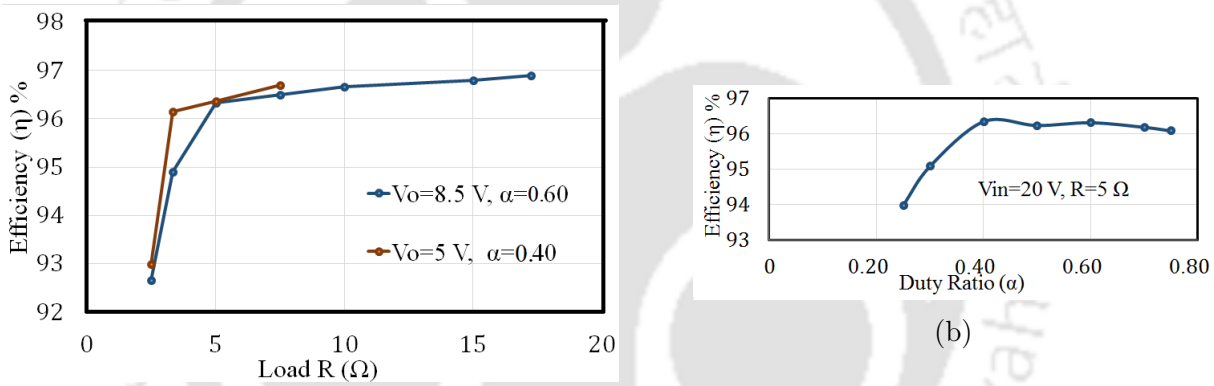


Figure 3.26: Experimental efficiency results of HSDIBuC due to change of (a) Load (R), and (b) Duty ratio (α)

The comparisons among the different topologies are provided in Table 3.3. The n depicts turns ratio of the transformers and coupled inductors. To achieve higher step-down ratio, the proposed HSDIBuC does not require any transformer or coupled inductor [35] [41]. The proposed HSDIBuC has higher step-down conversion ratio than the existing interleaved buck topologies [37]- [35], [41]. An interleaved buck converter (IBuC) with higher step-down conversion ratio is reported in [40]. This IBuC achieves the conversion ratio by a pair of coupled inductors. This coupled inductor is modeled by an ideal transformer. The requirements of semiconductor devices and magnetizing cores are high. Though the IBuCs presented in [32] and [40] have higher step-down conversion ratio, the requirement of inductors is very high.

Thus, it increases the cost and bulkiness. The IBuCs introduced in [37] and [38] operate only when the duty ratio is below 0.5. The proposed HSDIBuC operates in the range of $0 < \alpha \leq 1$.

Table 3.3: Comparisons among the existing and the proposed IBuCs

Topology	IBuC Introduced in [37]	IBuC Introduced in [38]	IBuC Introduced in [35]	IBuC Introduced in [32]	IBuC Introduced in [41]	IBuC Introduced in [40]	The Proposed HSDIBuC
$M = v_o/v_{in}$	2α	α	$\frac{\alpha}{n - n\alpha + \alpha}$	$\frac{\alpha}{4 - \alpha}$	$\frac{2\alpha}{n}$	$\frac{\alpha}{2(1+n)}$	$\frac{\alpha}{2 - \alpha}$
Quantities of switches	2	2	4	4	2	4	3
Quantities of diodes	2	2	4	4	3	2	2
Quantities of inductors	3	2	2 (4 windings)	5	1	4	3
Quantities of capacitors	1	3	5	5	3	4	3
Quantities of transformers	0	0	0	0	2	1	0

3.13 Summary

A DC-DC IBuC with improved step-down ratio namely HSDIBuC is proposed in this chapter. The proposed HSDIBuC has a simple circuit configuration and can produce low output voltage at sufficiently higher duty ratio by using a switch-capacitor cell. In input side, an inductor is placed to oppose the sudden change in the input current. The proposed HSDIBuC operates in the range of $0 < \alpha \leq 1$. The expressions for the high step-down conversion ratio, the ripple and the average current through the inductors are derived. The boundary load condition between CCM and DCM is determined. The semiconductor devices suffer less voltage stress. An efficiency of 96.33% has been achieved at $\alpha = 0.60$. Experimental results validate the proposed HSDIBuC. Small-signal modeling and the enabling of closed-loop control systems of the proposed HSDIBuC are extended in the next chapter.

4

High Step-down Interleaved Buck Converter with Dual-winding Coupled Inductor

This chapter proposes a dual-winding coupled inductor (DWCI) based high step-down interleaved buck converter (HSDIBuC) to reduce the ripples in inductor currents and to achieve lower value of the output filter capacitor. The proposed HSDIBuC-DWCI achieves a high step-down conversion ratio by using a switch-capacitor cell. In CCM, the systematic analysis of ripple currents in the windings of DWCI show the reduction of ripple in inductor current compared to the existing IBuCs. Further, the coupling factor of the DWCI reduces the minimum required value of the output filter capacitor. The operating principle of the proposed HSDIBuC-DWCI is analysed. Furthermore, the small-signal modelling is carried out. In the VMC framework, a PI-controller is designed to investigate the closed-loop performances. The proposed HSDIBuC-DWCI is implemented and experimental results are provided.

4.1 Introduction

In the previous chapter, a two-phase high-efficiency high step-down interleaved buck converter (HSDIBuC) with an improved step-down conversion ratio is presented using a switch-capacitor cell to avoid the problem of narrow duty cycle in CIBuC when a high-input to low-output voltage conversion is employed. The HSDIBuC as discussed previously also fulfills the objective of less voltage and current stresses for the semiconductor devices and less ripples in the inductor currents. However, the proposed HDIBuC uses two single inductors at the output-end and one single inductor. To reduce the size and weight, the two single inductors at the output-end can be replaced by a dual-winding coupled inductor (DWCI) whose units share magnetic core thus reducing the core size. The major technical performance benefit yielded by the DWCI is the further improvement of the ripples in inductor currents. Therefore, in this chapter, the two single inductors at the output-end of HSDIBuC are replaced by a DWCI utilizing all the advantages of HSDIBuC explained in previous chapter . The proposed high step-down interleaved buck converter with a dual-winding coupled inductor (HSDIBuC-DWCI) achieves less ripple in the inductor current without affecting the conversion ratio of HSDIBuC. Further, the analysis of the effect of the coupling factor on reducing the minimum capacitance value of the output filter capacitor is given.

The operation principle of the proposed HSDIBuC-DWCI is discussed in Section 4.2. In Section 4.3, a systematic analysis of the ripple current in DWCI for different cases is carried out. The effect of the coupling factor on the CCM/DCM boundary load is also developed. The minimum requirement of the crossly connected identical capacitors is carried out in Section 4.4. The equation for the minimum requirement of output filter capacitor value is derived in Section 4.5. Comparisons among the conventional and existing IBuCs are also discussed and necessary mathematical expressions are provided. The stresses of the semiconductor devices are provided in Section 4.6. The average state-space matrices and small-signal modelling analysis of the proposed IBuC with the DWCI are carried out respectively in Sections 4.7 and 4.8. A voltage mode PI controller is designed for the proposed IBC with DWCI in Section 4.9. To validate the claims, simulation and experimental results are provided in Section 4.10 and 4.11 respectively. Finally, in Section 4.12, summary of the chapter is provided.

4.2 Principle of Operation

A HSDIBuC is designed to improve the step-down conversion ratio operating in continuous conduction mode (CCM) as shown in Figure 3.1. This converter needs a total of three single inductors. Two single inductors are required at the output-end as shown in Figure 3.1. These two single inductors are replaced by a single dual-winding coupled inductor (DWCI) as shown in Figure 4.1.

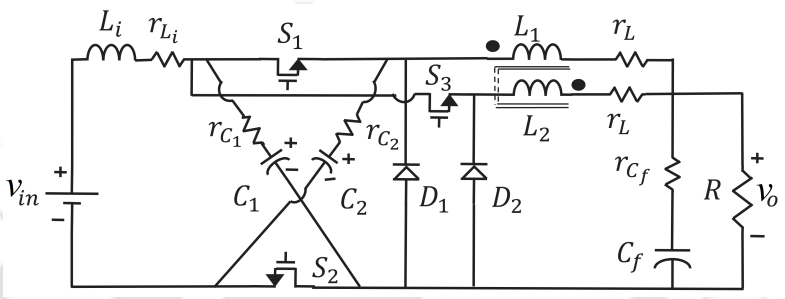


Figure 4.1: High step-down buck converter with a dual-winding coupled inductor (HSDIBuC-DWCI)

The input voltage v_{in} is followed by an single inductor L_i with parasitic r_{L_i}. Two identical capacitors C_1 and C_2 respectively with parasitics r_{C_1} and r_{C_2} are cross-connected with the two switches S_1 and S_2. The L_i is placed at the front side to oppose the sudden change of input current due to the series-parallel transition of these two identical capacitors. The diode D_1 is followed by the $L_1 - winding$ of the coupled inductor. The switch S_3 is followed by a diode D_2 and $L_2 - winding$ of the coupled inductor. r_L is the parasitic of the L_1 and L_2 windings. The two windings L_1 and L_2 are operating with 180^o phase shift in CCM. C_f with parasitic r_{C_f} is the output capacitor to the output v_o where R defines the output load resistance.

4.2.1 Dual-winding coupled inductor (DWCI)

The schematic diagram of DWCI is shown in Figure 4.2. The voltages across the L_1 and L_2 windings are denoted by v_{L_1} and v_{L_2}. The generalized equation of the coupled inductor is

$$v_{L_1} = L_1 \frac{di_{L_1}}{dt} \pm M \frac{di_{L_2}}{dt} \tag{4.1}$$

$$v_{L_2} = L_2 \frac{di_{L_2}}{dt} \pm M \frac{di_{L_1}}{dt} \tag{4.2}$$

where i_{L_1} and i_{L_2} are inductor currents. The mutual inductance M is defined as $M = k\sqrt{L_1 L_2}$.

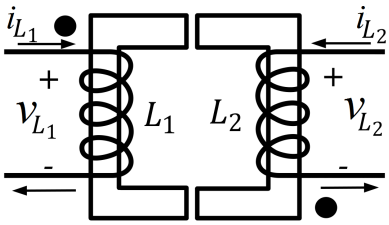


Figure 4.2: Schematic diagram of dual-winding coupled inductor (DWCI)

For inductors to be direct coupled, coupling coefficient $k \in [0, 1]$ and for inductors to be inverse coupled, $k \in [0, -1]$. The 180° phase shifting of inductor currents causes $i_{L_1} = -i_{L_2}$. Therefore, when the inductors are directly coupled, the inductive voltage becomes $v_{L_1} = (L_1 - M)\frac{di_{L_1}}{dt}$ and when the inductors are inversely coupled, the inductive voltage becomes $v_{L_1} = (L_1 + M)\frac{di_{L_1}}{dt}$. The $(L_1 - M)$ shows small inductance value with a bulky or larger size of the coupled inductor. Whereas, the $(L_1 + M)$ gives larger inductance value with the smaller size of the coupled inductor. Therefore, to reduce the bulkiness of the converter and to reduce the ripple in inductor current, the inductors are coupled inversely in a 180° phase-shifting condition. The two windings of the coupled inductor are considered to be equal $(L_1 = L_2 = L)$. The i_{L_1} and i_{L_2} represent the currents flowing through L_1 and L_2 windings respectively. By using Equations (4.1) and (4.2), the i_{L_1} and i_{L_2} over a time period T_s can be written as follows.

$$\int_0^{T_s} di_{L_1} = \frac{v_{L_1}}{(1-k^2)L_1}\int_0^{T_s} dt + \frac{v_{L_2} k\sqrt{\frac{L_1}{L_2}}}{(1-k^2)L_1}\int_0^{T_s} dt \tag{4.3}$$

$$\int_0^{T_s} di_{L_2} = \frac{v_{L_2}}{(1-k^2)L_2}\int_0^{T_s} dt + \frac{v_{L_1} k\sqrt{\frac{L_2}{L_1}}}{(1-k^2)L_2}\int_0^{T_s} dt \tag{4.4}$$

4.2.2 Switching modes when $\alpha \in (0, 0.5]$

The idealized waveform is shown in Figure 4.3 when the duty ratio α belongs to $(0, 0.5]$. At this case, there are four switching intervals over the time period T_s. The switching operations are described below. During the interval $(0 < t \leq \varphi_1 T_s)$, inductor current i_{L_1} through the L_1 increases and inductor current i_{L_2} through the inductor L_2 decreases. The currents i_{L_1} and i_{L_2} are out of phase. In the next interval $(\varphi_1 T_s < t \leq \varphi_2 T_s)$, all the three switches are OFF and both the inductor currents decrease. The currents i_{L_1} and i_{L_2} are in the same phase. In the subsequent interval $(\varphi_2 T_s < t \leq \varphi_3 T_s)$, S_1 and S_2 are still OFF but the S_3 is ON. Therefore, the i_{L_2} increases and i_{L_1} decreases.

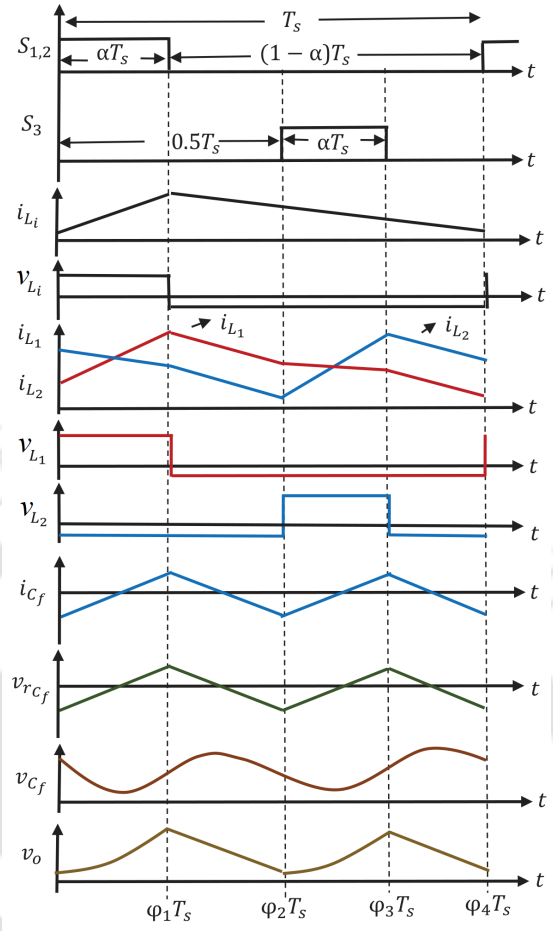


Figure 4.3: Idealized waveform of the proposed HSDIBuC-DWCI when $\alpha \in (0, 0.5]$

The i_{L_1} and i_{L_2} are out of phase. In the next interval ($\varphi_3 T_s < t \leq \varphi_4 T_s$), the nature of i_{L_1} and i_{L_2} is similar to that in the interval ($\varphi_1 T_s < t \leq \varphi_2 T_s$).

4.2.2.1 Interval $(0 < t \leq \varphi_1 T_s)$

In this duration, S_1 and S_2 are simultaneously ON and S_3 is OFF as shown in Figure 4.4. The diodes D_1 and D_2 become reverse and forward bias respectively. Therefore, the two identical capacitors become parallel and the voltage across these capacitor becomes v_C. The inductive voltages v_{L_i}, v_{L_1} and v_{L_2} across the L_i, L_1 and L_2 are expressed as follows.

$$v_{L_i} = v_{in} - v_C \tag{4.5}$$

$$v_{L_1} = L_1 \frac{di_{L_1}}{dt} - M \frac{di_{L_2}}{dt} = v_C - v_o \tag{4.6}$$

$$v_{L_2} = L_2 \frac{di_{L_2}}{dt} - M \frac{di_{L_1}}{dt} = -v_o \tag{4.7}$$

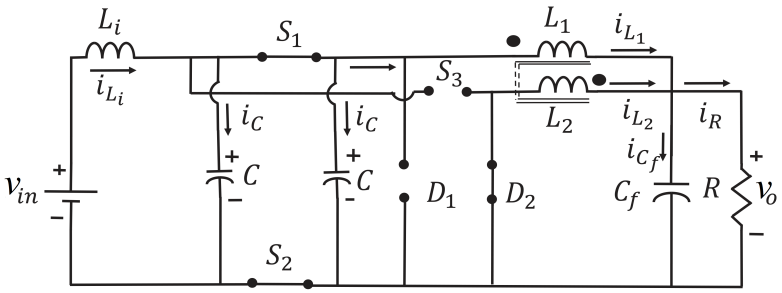


Figure 4.4: Schematic diagram of interval $(0 < t \leq \varphi_1 T_s)$

The current $i_C(t)$ through the two capacitors (C) is given by

$$2i_C(t) = i_{L_i}(t) - i_{L_1}(t) \tag{4.8}$$

The current $i_R(t)$ through the load R is determined as

$$i_R(t) = i_{L_1}(t) + i_{L_2}(t) - i_{C_f}(t) \tag{4.9}$$

where $i_{C_f}(t)$ is the current flowing through the capacitor C_f. The voltage, v_{C_f}, across the capacitor C_f is given by

$$v_{C_f} = v_o = Ri_R(t) \tag{4.10}$$

Let us define the state vector $\mathbf{x}(t) = [i_{L_i}\ v_C\ i_{L_1}\ i_{L_2}\ v_{C_f}]^T$ and the output vector $\mathbf{y}(t) = \mathbf{v_o}$. The state space equation in this duration $(0 < t \leq \varphi_1 T_s)$ is provided by

$$\dot{\mathbf{x}}(t) = \mathbf{A_1}\mathbf{x}(t) + \mathbf{B_1}v_{in}(t)$$

$$= \begin{bmatrix} \frac{-r_{L_i}}{L_i} & \frac{-1}{L_i} & 0 & 0 & 0 \\ \frac{1}{2C} & 0 & \frac{-1}{2C} & 0 & 0 \\ 0 & \frac{L_2}{L_1L_2 - M^2} & \frac{-r_L L_2}{L_1L_2 - M^2} & \frac{-Mr_L}{L_1L_2 - M^2} & \frac{-(L_2 + M)}{L_1L_2 - M^2} \\ 0 & \frac{M}{L_1L_2 - M^2} & \frac{-Mr_L}{L_1L_2 - M^2} & \frac{-r_L L_1}{L_1L_2 - M^2} & \frac{-(L_1 + M)}{L_1L_2 - M^2} \\ 0 & 0 & \frac{1}{C_f} & \frac{1}{C_f} & \frac{-1}{RC_f} \end{bmatrix} \mathbf{x}(t) + \begin{bmatrix} \frac{1}{L_i} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} v_{in}(t) \tag{4.11}$$

$$\mathbf{y}(t) = \mathbf{Z_1}\mathbf{x}(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \end{bmatrix} \mathbf{x}(t) \tag{4.12}$$

4.2.2.2 Interval ($\varphi_1 T_s < t \leq \varphi_2 T_s$)

During this interval, S_1, S_2 and S_3 are OFF. Both the diodes are in forward bias as represented in Figure 4.5.

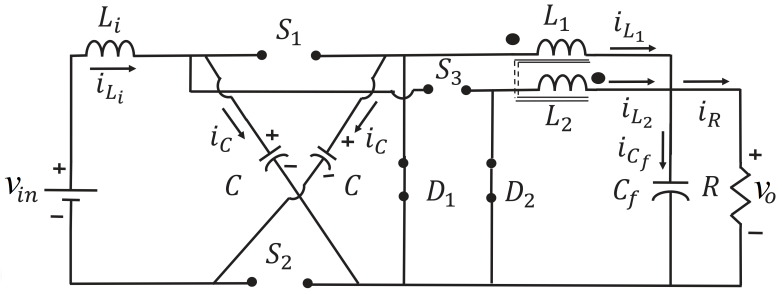


Figure 4.5: Schematic diagram of interval ($\varphi_1 T_s < t \leq \varphi_2 T_s$)

The two identical capacitors are in series through the diode D_1 and resultant voltage becomes $2v_C$. The voltages across the inductors are provided below.

$$v_{L_i} = v_{in} - 2v_C \tag{4.13}$$

$$v_{L_1} = L_1 \frac{di_{L_1}}{dt} - M \frac{di_{L_2}}{dt} = -v_o \tag{4.14}$$

$$v_{L_2} = L_2 \frac{di_{L_2}}{dt} - M \frac{di_{L_1}}{dt} = -v_o \tag{4.15}$$

The current through the capacitors is

$$i_C(t) = i_{L_i}(t) \tag{4.16}$$

The equations of load current $i_R(t)$ and the output capacitor voltage v_{C_f} are the same as Equations (4.9) and (4.10) respectively. The state-space equation is expressed by

$$\dot{\mathbf{x}}(t) = \mathbf{A_2}\mathbf{x}(t) + \mathbf{B_2} v_{in}(t)$$

$$= \begin{bmatrix} \frac{-r_{L_i}}{L_i} & \frac{-2}{L_i} & 0 & 0 & 0 \\ \frac{1}{C} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-r_L L_2}{L_1 L_2 - M^2} & \frac{-M r_L}{L_1 L_2 - M^2} & \frac{-(L_2 + M)}{L_1 L_2 - M^2} \\ 0 & 0 & \frac{-M r_L}{L_1 L_2 - M^2} & \frac{-r_L L_1}{L_1 L_2 - M^2} & \frac{-(L_1 + M)}{L_1 L_2 - M^2} \\ 0 & 0 & \frac{1}{C_f} & \frac{1}{C_f} & \frac{-1}{RC_f} \end{bmatrix} \mathbf{x}(t) + \begin{bmatrix} \frac{1}{L_i} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} v_{in}(t) \tag{4.17}$$

$$\mathbf{y}(t) = \mathbf{Z_2 x}(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \end{bmatrix} \mathbf{x}(t) \tag{4.18}$$

4.2.2.3 Interval ($\varphi_2 T_s < t \leq \varphi_3 T_s$)

In this duration, S_1 and S_2 are OFF and S_3 is ON as shown in Figure 4.6. The diode D_1 is in the reversed bias and D_2 is in the forward bias. The inductive voltage equations are provided as follows.

$$v_{L_i} = v_{in} - 2v_C \tag{4.19}$$

$$v_{L_1} = L_1 \frac{di_{L_1}}{dt} - M \frac{di_{L_2}}{dt} = -v_o \tag{4.20}$$

$$v_{L_2} = L_2 \frac{di_{L_2}}{dt} - M \frac{di_{L_1}}{dt} = v_C - v_o \tag{4.21}$$

The current, $i_C(t)$, through the capacitors is

$$i_C(t) = i_{L_i}(t) - i_{L_2}(t) \tag{4.22}$$

The equations of load current $i_R(t)$ and the output capacitor voltage v_{C_f} are the same as Equations (4.9) and (4.10) respectively.

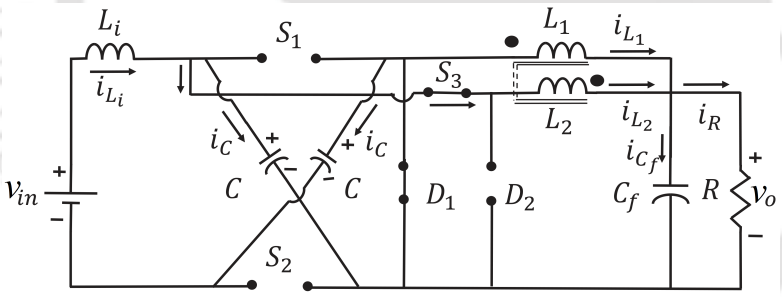


Figure 4.6: Schematic diagram of interval ($\varphi_2 T_s < t \leq \varphi_3 T_s$)

In this duration, the state-space equation is expressed by

$$\dot{\mathbf{x}}(t) = \mathbf{A_3 x}(t) + \mathbf{B_3} v_{in}(t)$$

$$= \begin{bmatrix} \frac{-r_{L_i}}{L_i} & \frac{-2}{L_i} & 0 & 0 & 0 \\ \frac{1}{C} & 0 & 0 & \frac{-1}{C} & 0 \\ 0 & \frac{M}{L_1L_2 - M^2} & \frac{-r_L L_2}{L_1L_2 - M^2} & \frac{-Mr_L}{L_1L_2 - M^2} & \frac{-(L_2 + M)}{L_1L_2 - M^2} \\ 0 & \frac{L_1}{L_1L_2 - M^2} & \frac{-Mr_L}{L_1L_2 - M^2} & \frac{-r_L L_1}{L_1L_2 - M^2} & \frac{-(L_1 + M)}{L_1L_2 - M^2} \\ 0 & 0 & \frac{1}{C_f} & \frac{1}{C_f} & \frac{-1}{RC_f} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_i} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} v_{in}(t) \tag{4.23}$$

$$\mathbf{y}(t) = \mathbf{Z_3 x}(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \end{bmatrix} \mathbf{x}(t) \tag{4.24}$$

4.2.2.4 Interval $(\varphi_3 T_s < t \leq \varphi_4 T_s)$

In this duration, the circuit configuration is the same as the Figure 4.5 and the operation is similar to that in the interval $(\varphi_1 T_s < t \leq \varphi_2 T_s)$.

4.2.3 Switching modes when $\alpha \in (0.5, 1)$

The idealized waveform is shown in Figure 4.7 when $\alpha \in (0.5, 1)$. In the intervals $(0 < t \leq \varphi_1 T_s)$ and $(\varphi_2 T_s < t \leq \varphi_3 T_s)$, all the switches are ON and the inductor currents i_{L_1} and i_{L_2} increase. The i_{L_1} and i_{L_2} are in phase during these two intervals. In the intervals $(\varphi_1 T_s < t \leq \varphi_2 T_s)$ and $(\varphi_3 T_s < t \leq \varphi_4 T_s)$, i_{L_1} and i_{L_2} are out of phase.

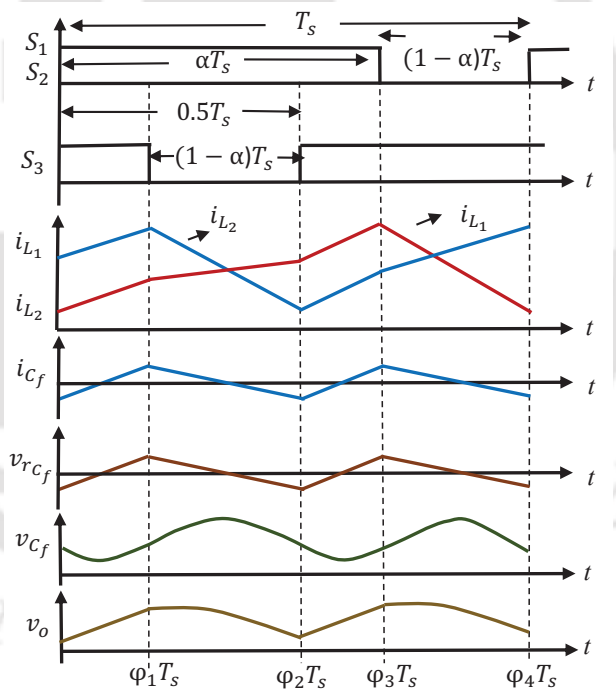


Figure 4.7: Idealized waveform of the proposed HSDIBuC-DWCI when $\alpha \in (0.5, 1)$

4.2.3.1 Interval $(0 < t \leq \varphi_1 T_s)$

In this interval all the three switches conduct and both the diodes are in reverse bias as shown in Figure 4.8. The voltages across the inductors are as follows.

$$v_{L_i} = v_{in} - v_C \tag{4.25}$$

$$v_{L_1} = L_1 \frac{di_{L_1}}{dt} - M \frac{di_{L_2}}{dt} = v_C - v_o \tag{4.26}$$

$$v_{L_2} = L_2 \frac{di_{L_2}}{dt} - M \frac{di_{L_1}}{dt} = v_C - v_o \tag{4.27}$$

The current through the two identical capacitors is given by

$$2i_C(t) = i_{L_i}(t) - i_{L_1}(t) - i_{L_2}(t) \tag{4.28}$$

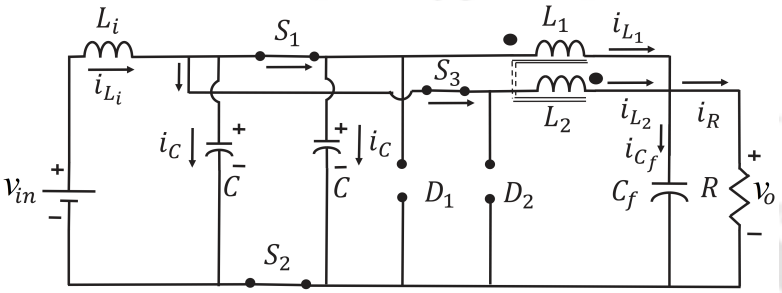


Figure 4.8: Schematic diagram of interval ($\varphi_1 T_s < t \leq \varphi_2 T_s$)

The equations of load current $i_R(t)$ and the output capacitor voltage v_{C_f} are the same as Equations (4.9) and (4.10) respectively. The state-space equation is provided as follows.

$$\dot{\mathbf{x}}(t) = \mathbf{A_4}\mathbf{x}(t) + \mathbf{B_4}v_{in}(t)$$

$$= \begin{bmatrix} \frac{-r_{L_i}}{L_i} & \frac{-1}{L_i} & 0 & 0 & 0 \\ \frac{1}{2C} & 0 & \frac{-1}{2C} & 0 & 0 \\ 0 & \frac{L_2+M}{L_1L_2-M^2} & \frac{-r_L L_2}{L_1L_2-M^2} & \frac{-Mr_L}{L_1L_2-M^2} & \frac{-(L_2+M)}{L_1L_2-M^2} \\ 0 & \frac{L_1+M}{L_1L_2-M^2} & \frac{-Mr_L}{L_1L_2-M^2} & \frac{-r_L L_1}{L_1L_2-M^2} & \frac{-(L_1+M)}{L_1L_2-M^2} \\ 0 & 0 & \frac{1}{C_f} & \frac{1}{C_f} & \frac{-1}{RC_f} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_i} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} v_{in}(t) \tag{4.29}$$

$$\mathbf{y}(t) = \mathbf{Z_4}\mathbf{x}(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \end{bmatrix} \mathbf{x}(t) \tag{4.30}$$

4.2.3.2 Interval ($\varphi_1 T_s < t \leq \varphi_2 T_s$)

During this interval, S_1 and S_2 are ON simultaneously, and S_3 is OFF. The operation principle is the same as the interval ($0 < t \leq \varphi_1 T_s$) operation while $\alpha \in (0, 0.5]$. The state-space equations are the same as provided in Equations (4.11) and (4.12).

4.2.3.3 Interval $(\varphi_2 T_s < t \leq \varphi_3 T_s)$

In this switching interval, all the three switches are ON and the operation principle is the same as in the interval $(0 < t \leq \varphi_1 T_s)$ while $\alpha \in (0.5, 1)$. The state-space equations are the same as provided in Equations (4.29) and (4.30).

4.2.3.4 Interval $(\varphi_3 T_s < t \leq \varphi_4 T_s)$

During this interval S_1 and S_2 are OFF, and S_3 is ON. The switching operation is the same as in the interval $(\varphi_2 T_s < t \leq \varphi_3 T_s)$ while $\alpha \in (0, 0.5]$. The state-space equations are the same as provided in Equations (4.23) and (4.24).

4.2.4 Voltage conversion ratio

The voltage second balance (VSB) equation of the input end inductor L_i is determined by using Equations (4.5), (4.13) and (4.19) as

$$v_C = \frac{v_{in}}{2 - \alpha} \tag{4.31}$$

The VSB equation of L_1 is derived by using Equations (4.6), (4.14) and (4.20) as

$$v_o = v_C \alpha \tag{4.32}$$

By using the Equations (4.31) and (4.32), the voltage conversion ratio is determined as

$$\frac{v_o}{v_{in}} = \frac{\alpha}{2 - \alpha} \tag{4.33}$$

Therefore, Equation (4.33) shows that the mutual inductance does not affect the conversion ratio of the proposed HSDIBuC discussed in chapter 3.

4.3 Ripple Current in DWCI

The ripples in the currents through the DWCI are determined for the following two cases.

4.3.1 Case I, $\alpha \in (0, 0.5]$

In the switching interval $(0 < t \leq \varphi_1 T_s)$, substituting Equations (4.6) and (4.7) into Equation (4.3), the instantaneous current $i_{L_1}(\varphi_1 T_s)$ is determined as follows.

$$i_{L_1}(\varphi_1 T_s) = \frac{(1 - \alpha - k\alpha) T_s v_o}{(1 - k^2) L_1} + i_{L_1}(0) \tag{4.34}$$

To determine the instantaneous current $i_{L_2}(\varphi_1 T_s)$ in this duration, Equations (4.6) and (4.7) are substituted into Equation (4.4) and is given by

$$i_{L_2}(\varphi_1 T_s) = \frac{(k - k\alpha - \alpha)T_s v_o}{(1-k^2)L_2} + i_{L_2}(0) \tag{4.35}$$

In the subsequent interval ($\varphi_1 T_s < t \leq \varphi_2 T_s$), the instantaneous current $i_{L_1}(\varphi_2 T_s)$ is determined by substituting Equations (4.14) and (4.15) into (4.3)

$$i_{L_1}(\varphi_2 T_s) = \frac{-(1+k)(0.5-\alpha)v_o T_S}{(1-k^2)L_1} + i_{L_1}(\varphi_1 T_s) = \frac{0.5 T_s v_o}{(1+k)L_1} + i_{L_1}(0) \tag{4.36}$$

In this interval, by substituting Equations (4.14) and (4.15) into Equation (4.4) the instantaneous current $i_{L_2}(\varphi_2 T_s)$ is calculated.

$$i_{L_2}(\varphi_2 T_s) = \frac{-(1+k)(0.5-\alpha)v_o T_S}{(1-k^2)L_2} + i_{L_2}(\varphi_1 T_s) = i_{L_2}(0) - \frac{0.5 T_s v_o}{(1+k)L_2} \tag{4.37}$$

In the next interval ($\varphi_2 T_s < t \leq \varphi_3 T_s$), the instantaneous current $i_{L_1}(\varphi_3 T_s)$ is determined by substituting Equations (4.20) and (4.21) into (4.3).

$$i_{L_1}(\varphi_3 T_s) = \frac{(k - k\alpha - \alpha)T_s v_o}{(1-k^2)L_1} + i_{L_1}(\varphi_2 T_s) = \frac{(0.5-\alpha)v_o T_s}{(1-k)L_1} + i_{L_1}(0) \tag{4.38}$$

The instantaneous current $i_{L_2}(\varphi_3 T_s)$ is the interval ($\varphi_2 T_s < t \leq \varphi_3 T_s$) is derived by substituting Equations (4.20) and (4.21) into Equation (4.4) as

$$i_{L_2}(\varphi_3 T_s) = \frac{(1 - \alpha - k\alpha)T_s v_o}{(1-k^2)L_2} + i_{L_2}(\varphi_2 T_s) = \frac{(0.5-\alpha)v_o T_s}{(1-k)L_2} + i_{L_2}(0) \tag{4.39}$$

In the subsequent interval ($\varphi_3 T_s < t \leq \varphi_4 T_s$), the instantaneous current $i_{L_1}(\varphi_4 T_s)$ is derived as

$$i_{L_1}(\varphi_4 T_s) = i_{L_1}(\varphi_3 T_s) - \frac{(0.5-\alpha)v_o T_s}{(1-k)L_1} = i_{L_1}(0) \tag{4.40}$$

In this interval, the instantaneous current $i_{L_2}(\varphi_4 T_s)$ is determined as follows.

$$i_{L_2}(\varphi_4 T_s) = i_{L_2}(\varphi_3 T_s) - \frac{(0.5-\alpha)v_o T_s}{(1-k)L_2} = i_{L_2}(0) \tag{4.41}$$

The average inductor current, I_L, flowing through the L_1 and L_2 windings of the coupled inductor is equal. Therefore, I_L is determined as follows.

$$\begin{aligned} I_L &= \frac{i_{L_1}(0) + i_{L_1}(\varphi_1 T_s)}{2}\alpha + \frac{i_{L_1}(\varphi_1 T_s) + i_{L_1}(\varphi_2 T_s)}{2}(0.5-\alpha) \\ &\quad + \frac{i_{L_1}(\varphi_2 T_s) + i_{L_1}(\varphi_3 T_s)}{2}\alpha + \frac{i_{L_1}(\varphi_3 T_s) + i_{L_1}(\varphi_4 T_s)}{2}(0.5-\alpha) \\ &= \frac{(1-\alpha-k\alpha)T_s}{2(1-k^2)L_1}v_o + i_{L_1}(0) \end{aligned} \tag{4.42}$$

The ripple in inductor windings L_1 and L_2 is as follows when $\alpha \in (0, 0.5]$.

$$\Delta i_{L_1} = \Delta i_{L_2} = \frac{(1-\alpha-k\alpha)T_s}{(1-k^2)L_1}v_o = \frac{(1-\alpha-k\alpha)\alpha v_{in}}{(1-k^2)(2-\alpha)L_1 f_s} \tag{4.43}$$

4.3.2 Case II, $\alpha \in (0.5, 1)$

In this case of operation, the expressions of the instantaneous inductor currents as shown in Figure 4.7, are provided in Table. 4.1.

Table 4.1: Instantaneous currents of L_1 and L_2 when $\alpha \in (0.5, 1)$

Instants	Instantaneous Current
$i_{L_1}(\varphi_1 T_s)$	$\frac{(1-\alpha)(\alpha-0.5)T_s v_o}{\alpha(1-k)L_1} + i_{L_1}(0)$
$i_{L_2}(\varphi_1 T_s)$	$\frac{(1-\alpha)(\alpha-0.5)T_s v_o}{\alpha(1-k)L_2} + i_{L_2}(0)$
$i_{L_1}(\varphi_2 T_s)$	$\frac{0.5(1-\alpha)v_o T_s}{\alpha(1+k)L_1} + i_{L_1}(0)$
$i_{L_2}(\varphi_2 T_s)$	$\frac{-0.5(1-\alpha)v_o T_s}{\alpha(1+k)L_2} + i_{L_2}(0)$
$i_{L_1}(\varphi_3 T_s)$	$\frac{(k\alpha+\alpha-k)(1-\alpha)T_s v_o}{\alpha(1-k^2)L_1} + i_{L_1}(0)$
$i_{L_2}(\varphi_3 T_s)$	$\frac{(k\alpha+\alpha-1)(1-\alpha)T_s v_o}{\alpha(1-k^2)L_2} + i_{L_2}(0)$
$i_{L_1}(\varphi_4 T_s)$	$i_{L_1}(0)$
$i_{L_2}(\varphi_4 T_s)$	$i_{L_2}(0)$

From the instantaneous values provided in Table 4.1, the average inductor current in this case is derived as follows.

$$I_L = \frac{(k\alpha + \alpha - k)(1-\alpha)T_s v_o}{2\alpha(1-k^2)L_1} + i_{L_1}(0) \tag{4.44}$$

The current ripple in the L_1 and L_2 windings are

$$\Delta i_{L_1} = \Delta i_{L_2} = \frac{(k\alpha + \alpha - k)(1-\alpha)v_{in}}{(2-\alpha)(1-k^2)L_1 f_s} \tag{4.45}$$

4.3.3 Ripple current in inductor L_i

The average current, I_{L_i}, through the inductor L_i is as follows.

$$I_{L_i} = \frac{(1-\alpha)T_s v_o}{2L_i} + i_{L_i}(0) \tag{4.46}$$

The ripple in i_{L_i} is determined as follows by using Equation (4.5).

$$\Delta i_{L_i} = i_{L_1}(\varphi_1 T_s) - i_{L_1}(0) = \frac{(1-\alpha)T_s v_o}{L_i} = \frac{(1-\alpha)\alpha T_s v_{in}}{(2-\alpha)L_i} \tag{4.47}$$

The ripple in input current is equal to the ripple in L_i inductor.

4.3.4 Minimum inductance value of DWCI

Minimum inductance value of DWCI is calculated for the following two cases.

4.3.4.1 Case I, $\alpha \in (0, 0.5]$

At the boundary condition, the input current can be written as follows by using Equation (4.46).

$$i_{in} = \frac{(1-\alpha)T_s v_o}{2L_i} + i_{L_i}(0) \tag{4.48}$$

At ideal lossless condition the relation between i_{in} and output current i_o is expressed as follows by using Equation (4.33).

$$i_{in} = \frac{\alpha}{2-\alpha} i_o \tag{4.49}$$

Therefore, by using Equations (4.48) and (4.49), the boundary load R_{B_i} is derived as

$$R_{B_i} = \frac{v_o}{i_{OB}} = \frac{2\alpha L_i}{(1-\alpha)(2-\alpha)T_s} \tag{4.50}$$

where i_{OB} is the boundary load current. At the boundary condition derived in Equations (4.50), output boundary load current i_{OB} is obtained as

$$i_{OB} = 2I_L = \frac{(1-\alpha-k\alpha)T_s}{(1-k^2)L_1} v_o \tag{4.51}$$

At this i_{OB}, the boundary load becomes

$$R_B = \frac{v_o}{i_{OB}} = \frac{(1-K^2)L_1}{(1-\alpha-k\alpha)T_s} \tag{4.52}$$

Therefore, minimum inductance value is derived as follows from Equation (4.52).

$$min\{L_1 = L_2\} = \frac{(1-\alpha-k\alpha)T_s R_B}{(1-k^2)} = \frac{(1-\alpha-k\alpha)R_B}{(1-k^2)f_s} \tag{4.53}$$

4.3.4.2 Case II, $\alpha \in (0.5, 1)$

Similarly the analysis is carried out as described above and this case the minimum requirement of inductance value is determined as

$$min\{L_1 = L_2\} = \frac{(k\alpha+\alpha-k)(1-\alpha)R_B}{\alpha(1-k^2)f_s} \tag{4.54}$$

4.4 Minimum Capacitance Value of ($C_1 = C_2 = C$)

The idealized waveforms of current through the identical capacitor i_C and the voltage across the identical capacitor v_C are shown in Figure 4.9. In the duration ($0 < t \leq \varphi_1 T_s$), the capacitors become parallel to each other and the voltage across the capacitor becomes v_C as shown in Figure 4.4. During this switching mode, the identical capacitors discharge energy to the load. In the remaining entire duration ($\varphi_1 T_s < t \leq T_s$), the two capacitors are charged in series by v_{in} and the resultant voltage across the two identical capacitors become $v_C + v_C = 2v_C$.

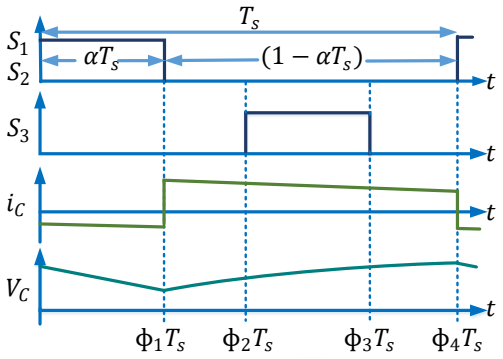


Figure 4.9: Idealized waveform of the capacitive current and voltage of the identical capacitors

The ripple voltage can be expressed by Δv_C and it is defined by $\Delta v_C = v_{C_{max}} - v_{C_{min}}$. The average capacitive voltage is approximated by using Equation (4.32) as follows.

$$\frac{v_{C_{max}} + v_{C_{min}}}{2} = v_C = \frac{v_o}{\alpha} \tag{4.55}$$

Now, in the duration $(0 < t \leq \varphi_1 T_s)$, the power released by these two identical capacitors is equal to the power delivered to the load. Therefore, the energy equation is written as follows.

$$\frac{C(v_{C_{max}} + v_{C_{min}})(v_{C_{max}} - v_{C_{min}})}{\alpha T_s} = \frac{v_o^2}{R} \tag{4.56}$$

Substituting, $\Delta v_C = v_{C_{max}} - v_{C_{min}}$ and Equation (4.55) into Equation (4.56), the minimum capacitance value for the identical capacitors is determined as

$$C_{min} = \frac{\alpha^2 T_s v_o}{2\Delta v_C R} \tag{4.57}$$

4.5 Minimum Capacitance value of C_f

Minimum capacitance value of C_f is calculated for the following two cases.

4.5.1 Case I, $\alpha \in (0, 0.5]$

The output filter capacitor is required to be designed so that the impedance of the capacitive branch is less than the load resistance R. The DC components of the two inductor currents (i_{L_1} and i_{L_2}) pass through the load (R) and the AC component passes through the capacitor (C_f). As the ripple in load current ($i_R = i_o$) is much less, it is neglected. Therefore, the current

passing through the output filter capacitor (C_f) is approximately equal to the resultant AC component of the two inductor currents. The idealized waveforms of the capacitive current i_{C_f}, AC component of the voltage across the r_{C_f}, ($v_{r_{C_f}}$), and AC component of output voltage, $\hat{v}_o$, are depicted as shown in Figure 4.3 when $\alpha \in (0, 0.5]$. Therefore, i_{C_f} is determined by the following equation.

$$i_{C_f} = \frac{\Delta total\ inductor\ current}{\Delta t} t \pm (\frac{\Delta I_{L_1}}{2} + \frac{\Delta I_{L_2}}{2}) \tag{4.58}$$

From Equation (4.42), the average ripple current ($\Delta I_L = \Delta I_{L_1} = \Delta I_{L_2}$) is determined as $\Delta I_L = \frac{(1-\alpha-k\alpha)T_s}{2(1-k^2)L} v_o$. In the interval ($0 < t \leq \varphi_1 T_s$) as shown in Figure 4.3, i_{C_f} is determined by substituting Equations (4.58), (4.34) and into Equation (4.35) as follows.

$$\begin{aligned} i_{C_f} &= \frac{[i_{L_1}(\varphi_1 T_s) - i_{L_1}(0)] - [i_{L_2}(0) - i_{L_2}(\varphi_1 T_s)]}{\varphi_1 T_s - 0} t - \Delta I_L \\ &= \frac{(1 - 2\alpha - 2k\alpha + k)v_o}{\alpha T_s (1-k^2) L f_s} t - \frac{(1 - \alpha - k\alpha)v_o}{2(1-k^2)Lf_s} \end{aligned} \tag{4.59}$$

The $v_{r_{C_f}}$ is determined by using Equation (4.59) as

$$v_{r_{C_f}} = \frac{(1 - 2\alpha - 2k\alpha + k)v_o r_{C_f}}{\alpha T_s (1-k^2) L f_s} t - \frac{(1 - \alpha - k\alpha)v_o r_{C_f}}{2(1-k^2)Lf_s} \tag{4.60}$$

The capacitive voltage v_{C_f} consists of DC component V_{C_f} and AC component v_{c_f}, i.e. $v_{C_f} = V_{C_f} + v_{c_f}$. In the output voltage, v_{c_f} contributes the ripple. Therefore, the v_{c_f} is derived as follows by using Equation (4.59).

$$\begin{aligned} v_{c_f} &= \frac{1}{C_f} \int_0^t i_{C_f}(t) dt + v_{c_f}(0) \\ &= \frac{(1 - 2\alpha - 2k\alpha + k)v_o}{C_f \alpha T_s (1-k^2) L f_s} \frac{t^2}{2} - \frac{(1 - \alpha - k\alpha)v_o}{C_f 2(1-k^2)Lf_s} t + v_{c_f}(0) \end{aligned} \tag{4.61}$$

The $v_{r_{C_f}}$ and v_{c_f} provide the AC component in the output voltage ($\hat{v}_o = v_{r_{C_f}} + v_{C_f}$). Therefore, AC component of the v_o can be written as follows by using Equations (4.60) and (4.61).

$$\begin{aligned} \hat{v}_o =& \frac{(1 - 2\alpha - 2k\alpha + k)v_o r_{C_f}}{\alpha T_s (1-k^2) L f_s} t - \frac{(1 - \alpha - k\alpha)v_o r_{C_f}}{2(1-k^2)Lf_s} \\ &+ \frac{(1 - 2\alpha - 2k\alpha + k)v_o}{C_f \alpha T_s (1-k^2) L f_s} \frac{t^2}{2} - \frac{(1 - \alpha - k\alpha)v_o}{C_f 2(1-k^2)Lf_s} t + v_{c_f}(0) \end{aligned} \tag{4.62}$$

To calculate the minimum capacitance value, the derivative of $\hat{v}_o$ in Equation (4.62) with respect to time ($d\hat{v}_o/dt$) is set to zero and the minimum capacitance value ($C_{f_{min(on-off)}}$) occurs at $t_{min} = 0$ as follows.

$$C_{f_{min(on-off)}} = \frac{(1 - \alpha_{max} - k\alpha_{max})\alpha_{max}}{2(1 - 2\alpha_{max})(1 + k)r_{C_f} f_s} \tag{4.63}$$

In the subsequent interval ($\varphi_1 T_s < t \leq \varphi_2 T_s$) as shown in Figure 4.3, by substituting Equations (4.36), (4.37) and into Equation (4.58) the i_{C_f} is derived as follows.

$$\begin{aligned} i_{C_f} =& \frac{[i_{L_1}(\varphi_2 T_s) - i_{L_1}(\varphi_1 T_s)] + [i_{L_2}(\varphi_2 T_s) - i_{L_2}(\varphi_1 T_s)]}{(0.5 - \alpha)T_s}(t - \alpha T_s) + \Delta I_L \\ =& \frac{-2(1 + k)v_o(t - \alpha T_s)}{T_s(1 - k^2)Lf_s} + \frac{(1 - \alpha - k\alpha)v_o}{(1 - k^2)Lf_s} \end{aligned} \tag{4.64}$$

By using Equation (4.64), $v_{r_{C_f}}$ is derived as follows.

$$v_{r_{C_f}} = \frac{-2(1 + k)v_o(t - \alpha T_s)r_{C_f}}{T_s(1 - k^2)Lf_s} + \frac{(1 - \alpha - k\alpha)v_o r_{C_f}}{(1 - k^2)Lf_s} \tag{4.65}$$

In this duration, the v_{c_f} is determined as follows.

$$\begin{aligned} v_{c_f} =& \frac{1}{C_f}\int_{\alpha T_s}^{t} i_{C_f}(t)dt + v_{c_f}(\alpha T_s) \\ =& \frac{-(1 + k)}{C_f T_s(1 - k^2)Lf_s}t^2 + \left(\frac{2(1 + k)\alpha T_s}{T_s} + \frac{1 - \alpha - k\alpha}{2}\right)\left(\frac{v_o}{C_f(1 - k^2)Lf_s}\right)t \\ & - \frac{(1 + k)\alpha^2 T_s^2}{C_f T_s(1 - k^2)Lf_s} - \frac{(1 - \alpha - k\alpha)\alpha T_s}{2C_f(1 - k^2)Lf_s} \end{aligned} \tag{4.66}$$

The AC component of the output voltage $\hat{v}_o$ is the sum of the $v_{r_{C_f}}$ and v_{c_f}, i.e $\hat{v}_o = v_{r_{C_f}} + v_{c_f}$. By setting the dv_o/dt to zero, the maximum value of $\hat{v}_o$ occurs at $t_{max} = \alpha T_s$. Therefore, the minimum capacitance ($C_{f_{min(off-off)}}$) value is derived as follows.

$$C_{f_{min(off-off)}} = \frac{(1 - \alpha_{min} - k\alpha_{min})}{4(1 + k)r_{C_f} f_s} \tag{4.67}$$

In the next duration ($\varphi_2 T_s < t \leq \varphi_3 T_s$), the minimum capacitance value ($C_{f_{min}}$) is the same as given in Equation (4.63). Similarly, the minimum capacitance value ($C_{f_{min}}$) is given by Equation (4.67) in the interval ($\varphi_3 T_s < t \leq \varphi_4 T_s$).

The peak-to-peak ripple voltage (V_r) does not depend upon the V_{C_f}. The V_r is determined only by the ripple voltage across the ESR (equivalent series resistance) r_{C_f} if

$$\begin{aligned} C_f \geq C_{f_{min}} &= max\left\{C_{f_{min(on-off)}}, C_{f_{min(off-off)}}\right\} \\ &= max\left\{\frac{(1-\alpha_{max}-k\alpha_{max})\alpha_{max}}{2(1-2\alpha_{max})(1+k)r_{C_f}f_s}, \frac{(1-\alpha_{min}-k\alpha_{min})}{4(1+k)r_{C_f}f_s}\right\} \end{aligned} \tag{4.68}$$

The extreme values of α_{min} and α_{max} are given as $\alpha_{min} = 0$ and $\alpha_{max} < 0.5$ respectively. Thus, the condition provided in Equation (4.68) is satisfied at the value of α if

$$C_f \geq C_{f_{min}} = \frac{1}{4(1+k)r_{C_f}f_s} \tag{4.69}$$

4.5.2 Case II, $\alpha \in (0.5, 1)$

The analysis to determine the capacitance value is carried out in the similar manner as described in Case I. The minimum capacitance values $C_{f_{min(on-on)}}$ and $C_{f_{min(on-off)}}$ respectively in the intervals $(0 < t \leq \varphi_1 T_s)$ and $(\varphi_1 T_s < t \leq \varphi_2 T_s)$ are provided as follows.

$$C_{f_{min(on-on)}} = \frac{(k\alpha_{max}+\alpha_{max}-k)}{4(1+k)r_{C_f}f_s} \tag{4.70}$$

$$C_{f_{min(on-off)}} = \frac{(k\alpha_{min}+\alpha_{min}-k)(1-\alpha_{min})}{2(2\alpha_{min}-1)(1+k)r_{C_f}f_s} \tag{4.71}$$

The output voltage ripple V_r can be calculated only by the r_{C_f} if

$$\begin{aligned} C_f \geq C_{f_{min}} &= max\left\{C_{f_{min(on-on)}}, C_{f_{min(on-off)}}\right\} \\ &= max\left\{\frac{(k\alpha_{max}+\alpha_{max}-k)}{4(1+k)r_{C_f}f_s}, \frac{(k\alpha_{min}+\alpha_{min}-k)(1-\alpha_{min})}{2(2\alpha_{min}-1)(1+k)r_{C_f}f_s}\right\} \end{aligned} \tag{4.72}$$

In the worst situation, the values of α_{min} and α_{max} are provided as $\alpha_{min} > 0.5$ and $\alpha_{max} = 1$ respectively. Thus, the condition provided in Equation (4.72) is satisfied at the value of α if

$$C_f \geq C_{f_{min}} = \frac{1}{4(1+k)r_{C_f}f_s} \tag{4.73}$$

Remarks: When the $\alpha = 0.5$, the peak to peak ripple output voltage (V_r) can be calculated

by the ripple voltage across the r_{C_f} if $C_f \geq \frac{0.5}{4r_{C_f}f_s}$. Now, when the $\alpha = 0.5$, the average ripple current in the L_1 and L_2 windings is $\Delta I_L = \frac{0.5v_o}{2(1+k)Lf_s}$.

4.5.3 Selection of parameters

The load resistance is considered as $R = 5\ \Omega$. The value of the coupling factor is $k = 0.5$. At $R_{B_i} = R = 5\ \Omega$ and $\alpha = 0.4$, the minimum inductance value is calculated as $L = L_1 = L_2 = 53.33\ \mu$H by using Equation (4.53). When two single inductors are used instead of the dual winding coupled inductor, i.e. $k = 0$, the minimum inductance value is 60 μH. At the values of $r_{C_f} = 0.22\ \Omega$, $f_s = 50$ kHz, $\alpha = 0.4$ and $k = 0.5$, the C_f is calculated as $C_f \geq max\{24.24, 6.06\}\mu\text{F} = 24.24\ \mu$F by the condition provided in Equation (4.68). At the same condition when k becomes zero ($k = 0$), the value of the C_f is calculated as $C_f \geq max\{54.54, 13.6\}\mu\text{F} = 54.54\ \mu$F. Therefore, it can be said that the values of the L_1, L_2 and C_f can be reduced by the coupling factor k. The parameter values are adopted from HSDIBuC [123] and provided in Table 4.2. The two output-end single inductors are replaced by a dual winding coupled inductor.

Table 4.2: Parameter values of HSDIBuC-DWCI considered for CCM operation

Parameters	**Value**
Input voltage (v_{in})	20 V
Switching frequency (f_s)	50 kHz
Inductance ($L = L_1 = L_2$)	180 μH
Coupling factor (k)	0.5
Inductive resistance (r_L)	0.07 Ω
Identical capacitance ($C = C_1 = C_2$)	220 μF
Resistances of C_1 and C_2 ($r_{C_1} = r_{C_2}$)	0.32 Ω
Input-side inductance (L_i)	180 μH
Output capacitance (C_f)	330 μF
Load resistance (R)	5 Ω
ESR of output capacitor (r_{C_f})	0.22 Ω

Table 4.3: Comparisons among the existing and the proposed IBuCs.

Items	CIBuC	Compare	The HSDIBuC	Compare	The HSDIBuC-DWCI
Voltage Gain ($\frac{v_o}{v_{in}}$)	α	$>$	$\frac{\alpha}{2-\alpha}$	$=$	$\frac{\alpha}{2-\alpha}$
$\Delta i_{L_1} = \Delta i_{L_2}\vert_{\alpha\in(0,0.5]}$	$\frac{(1-\alpha)\alpha v_{in}}{Lf_s}$	$>$	$\frac{(1-\alpha)\alpha v_{in}}{(2-\alpha)Lf_s}$	$>$	$\frac{(1-\alpha-k\alpha)\alpha v_{in}}{(1-k^2)(2-\alpha)Lf_s}$
$\Delta i_{L_1} = \Delta i_{L_2}\vert_{\alpha\in(0.5,1)}$	$\frac{(1-\alpha)\alpha v_{in}}{Lf_s}$	$>$	$\frac{(1-\alpha)\alpha v_{in}}{(2-\alpha)Lf_s}$	$>$	$\frac{(k\alpha+\alpha-k)(1-\alpha)v_{in}}{(2-\alpha)(1-k^2)L_1f_s}$
$\min\{L_1 = L_2\}\vert_{\alpha\in(0,0.5]}$	$\frac{(1-\alpha)R_B}{f_s}$	$>$	$\frac{(1-\alpha)R_B}{f_s}$	$>$	$\frac{(1-\alpha-k\alpha)R_B}{(1-k^2)f_s}$
$\min\{L_1 = L_2\}\vert_{\alpha\in(0.5,1)}$	$\frac{(1-\alpha)R_B}{f_s}$	$>$	$\frac{(1-\alpha)R_B}{f_s}$	$>$	$\frac{(k\alpha+\alpha-k)(1-\alpha)R_B}{\alpha(1-k^2)f_s}$
$C_{f_{min(on-off)}}\vert_{\alpha\in(0,0.5]}$	$\frac{(1-\alpha_{max})\alpha_{max}}{2(1-2\alpha_{max})r_{C_f}f_s}$	$=$	$\frac{(1-\alpha_{max})\alpha_{max}}{2(1-2\alpha_{max})r_{C_f}f_s}$	$>$	$\frac{(1-\alpha_{max}-k\alpha_{max})\alpha_{max}}{2(1-2\alpha_{max})(1+k)r_{C_f}f_s}$
$C_{f_{min(off-off)}}\vert_{\alpha\in(0,0.5]}$	$\frac{(1-\alpha_{min})}{4r_{C_f}f_s}$	$=$	$\frac{(1-\alpha_{min})}{4r_{C_f}f_s}$	$>$	$\frac{(1-\alpha_{min}-k\alpha_{min})}{4(1+k)r_{C_f}f_s}$
$C_{f_{min(on-off)}}\vert_{\alpha\in(0.5,1)}$	$\frac{(1-\alpha_{min})\alpha_{min}}{2(2\alpha_{min}-1)r_{C_f}f_s}$	$=$	$\frac{(1-\alpha_{min})\alpha_{min}}{2(2\alpha_{min}-1)r_{C_f}f_s}$	$>$	$\frac{(k\alpha_{min}+\alpha_{min}-k)(1-\alpha_{min})}{2(2\alpha_{min}-1)(1+k)r_{C_f}f_s}$
$C_{f_{min(on-on)}}\vert_{\alpha\in(0.5,1)}$	$\frac{\alpha_{max}}{4r_{C_f}f_s}$	$=$	$\frac{\alpha_{max}}{4r_{C_f}f_s}$	$>$	$\frac{(k\alpha_{max}+\alpha_{max}-k)}{4(1+k)r_{C_f}f_s}$

4.5.4 Comparisons among the existing and the proposed HSDIBuC-DWCI

The comparison among the existing and the proposed HSDIBuC-DWCI is shown in Table 4.3. In Figure 4.10, the change of ripple in inductor current ($\Delta i_L = \Delta i_{L_1} = \Delta i_{L_2}$) is shown with respect to α and it is seen that HSDIBuC introduced in Chapter 3 has less ripple than CIBuC in the entire range of $\alpha \in (0, 1)$. But, for a certain range of α, the proposed HSDIBuC-DWCI has less ripple (Δi_L) compared to the HSDIBuC described in Chapter 3. The curve of ripple Δi_L with $k = 0$ and Δi_L with $k = 0.5$ intersect at two points. In this region, Δi_L of the proposed HSDIBuC-DWCI is less than CIBuC and HSDIBuC introduced in Chapter 3. Therefore, it is necessary to find out the best operating range of α. In Equation (4.43), the v_{in}, L and f_s are positive constants. Therefore, to get the lower intersection point when $\alpha \in (0, 0.5]$, the Δi_L provided in chapter 3 and Equation (4.43) are equal and, written as

$$\frac{(1-\alpha)\alpha v_{in}}{(2-\alpha)Lf_s} = \frac{(1-\alpha-k\alpha)\alpha v_{in}}{(1-k^2)(2-\alpha)Lf_s} \tag{4.74}$$

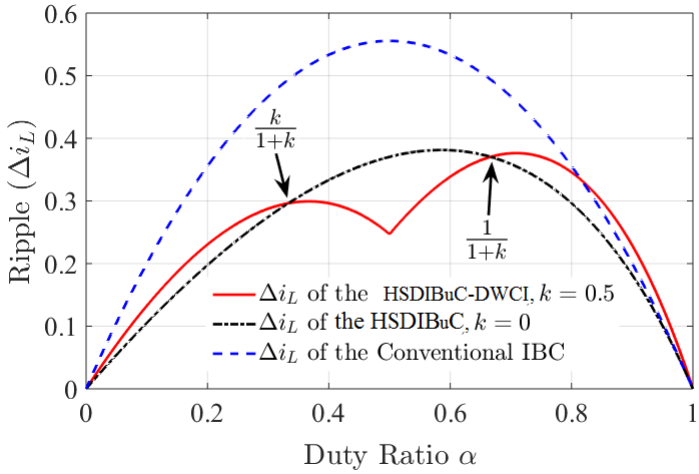


Figure 4.10: Ripple current Δi_L due to change of α

Since, $\alpha > 0$ and α can never be equal to 2, therefore, solving the Equation (4.74), the following intersection point is obtained.

$$\alpha = \frac{k}{1+k} \ , as \ k \neq 0 \tag{4.75}$$

Now, it is required to find out the higher value of intersection point when $\alpha \in (0.5, 1)$. Therefore, by equating the Δi_L provided in Equations (3.35) and (4.45), the upper limit of α is found as

$$\alpha = \frac{1}{1+k} \ , as \ k \neq 0 \tag{4.76}$$

Therefore, the ripple of the proposed converter is less than the CIBuC and HSDIBuC when $\alpha \in (\frac{k}{1+k}, \frac{1}{1+k})$.

The change in ripple in inductor currents due to change in coupling factor is shown in Figure 4.11. When $\alpha \in (0, 0.5]$, from Equation (4.74), the operating range of coupling factor is derived as $k \in (0, \frac{\alpha}{1-\alpha}]$. To get the minimum ripple for any provided α, the maximum coupling factor k is determined by equating the derivative of Δi_L with respect to k ($d\Delta i_L/dk$) to zero. Therefore, when $\alpha \in (0, 0.5]$, by doing the derivative of the Equation (4.43), k is determined as

$$k = \frac{1-\alpha}{\alpha} \pm \sqrt{(\frac{1-\alpha}{\alpha})^2 - 1} \tag{4.77}$$

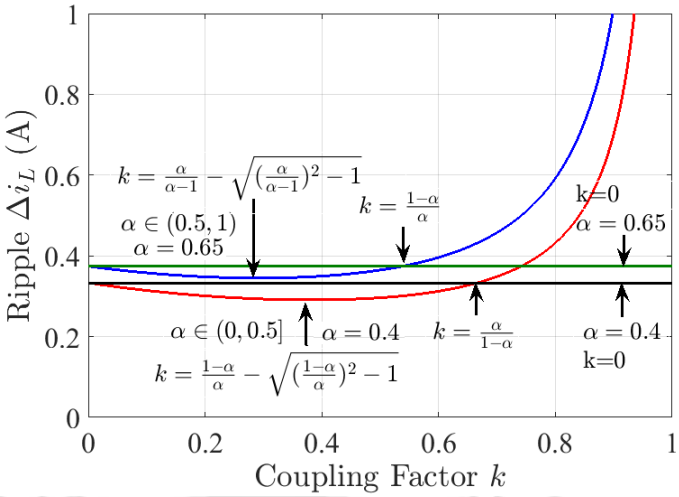


Figure 4.11: Ripple in inductor currents Δi_L due to change of k

As $k \not> 1$, the k becomes $k = \frac{1-\alpha}{\alpha} - \sqrt{(\frac{1-\alpha}{\alpha})^2 - 1}$. Now, when $\alpha \in (0.5, 1)$, the maximum k value to get the minimum ripple for any provided α is derived from Equation (4.45) as follows.

$$k = \frac{\alpha}{1-\alpha} \pm \sqrt{(\frac{\alpha}{1-\alpha})^2 - 1} \tag{4.78}$$

As $k \not> 1$, the k becomes $k = \frac{\alpha}{1-\alpha} - \sqrt{(\frac{\alpha}{1-\alpha})^2 - 1}$. The operating range of k for this case of operation is $k \in (0, \frac{1-\alpha}{\alpha}]$.

4.6 Stresses of the Semiconductor Devices

Maximum voltage and current stresses are determined as follows.

4.6.1 Maximum voltage stress

The voltage stresses of the switches S_1, S_2 and S_3 are denoted by v_{S_1}, v_{S_2} and v_{S_3} respectively. The maximum voltage stresses are approximated by neglecting the capacitive ripple voltages as follows.

$$v_{Smax} = v_{S_1} = v_{S_2} = v_{S_3} = v_C = \frac{v_{in}}{2-\alpha} = \frac{v_o}{\alpha} \tag{4.79}$$

The maximum diode voltage stresses v_{D_1} and v_{D_2} of the diodes D_1 and D_2 respectively are as follows.

$$v_{Dmax} = v_{D_1} = v_{D_2} = v_C = \frac{v_{in}}{2-\alpha} = \frac{v_o}{\alpha} \tag{4.80}$$

It is seen that the voltage stresses are equal to that in HSDIBuC. Therefore, compared to CIBuC, semiconductor devices of lower voltage rating can be used to design the proposed

converter.

4.6.2 Maximum current stress

The maximum current stresses of the switches S_1, S_2 and S_3 are defined by $I_{S_{1max}}$, $I_{S_{2max}}$ and $I_{S_{3max}}$ respectively. $I_{D_{max}}$ represents the maximum current flowing through the diodes D_1 and D_2. The currents flowing through the windings of DWCI are half of the output current. Therefore, the switch current stresses can be approximated as follows.

$$\begin{aligned} I_{Smax}\big|_{\alpha\in(0,0.5]} &= I_{D_{max}} = I_{S_{1max}} = I_{S_{2max}} = I_{S_{3max}} \\ &= \frac{i_o}{2} + \frac{\Delta i_L}{2} = \frac{i_o}{2} + \frac{(1-\alpha-k\alpha)\alpha v_{in}}{2(1-k^2)(2-\alpha)L_1 f_s} \end{aligned} \tag{4.81}$$

$$I_{Smax}\big|_{\alpha\in(0.5,1)} = I_{D_{max}} = \frac{i_o}{2} + \frac{(k\alpha+\alpha-k)(1-\alpha)v_{in}}{2(2-\alpha)(1-k^2)L_1 f_s} \tag{4.82}$$

4.7 Average State-space Matrices

The general average state space equation is as follows.

$$\dot{\mathbf{x}}(t) = \mathbf{A_{av}}\mathbf{x}(t) + \mathbf{B_{av}}v_{in}(t) \tag{4.83}$$

$$\mathbf{y}(t) = \mathbf{Z_{av}}\mathbf{x}(t) \tag{4.84}$$

The average state space matrices are as follows when $\alpha \in (0, 0.5]$.

$$\begin{aligned} \mathbf{A_{av}} &= (\mathbf{A_1} + \mathbf{A_3})\alpha + \mathbf{A_2}(1-2\alpha) \\ &= \begin{bmatrix} \frac{-r_{L_i}}{L_i} & \frac{\alpha-2}{L_i} & 0 & 0 & 0 \\ \frac{2-\alpha}{2C} & 0 & \frac{-\alpha}{2C} & \frac{-\alpha}{C} & 0 \\ 0 & \frac{(L_2+M)\alpha}{L_1L_2-M^2} & \frac{-r_L L_2}{L_1L_2-M^2} & \frac{-Mr_L}{L_1L_2-M^2} & \frac{-(L_2+M)}{L_1L_2-M^2} \\ 0 & \frac{(L_1+M)\alpha}{L_1L_2-M^2} & \frac{-Mr_L}{L_1L_2-M^2} & \frac{-r_L L_1}{L_1L_2-M^2} & \frac{-(L_1+M)}{L_1L_2-M^2} \\ 0 & 0 & \frac{1}{C_f} & \frac{1}{C_f} & \frac{-1}{RC_f} \end{bmatrix} \end{aligned} \tag{4.85}$$

$$\mathbf{B_{av}} = (\mathbf{B_1} + \mathbf{B_3})\alpha + \mathbf{B_2}(1 - 2\alpha) = \left[\frac{1}{L_i}\ 0\ 0\ 0\ 0\right]^T \tag{4.86}$$

$$\mathbf{Z_{av}} = (\mathbf{Z_1} + \mathbf{Z_3})\alpha + \mathbf{Z_2}(1 - 2\alpha) = [0\ 0\ 0\ 0\ 1] \tag{4.87}$$

4.8 Small Signal Modelling

Consider that the feedback control circuit is disabled and a perturbation $\hat{v}_{in}(t)$ appears in the steady state input voltage V_{in}. So the input voltage can be expressed as $v_{in}(t) = V_{in} + \hat{v}_{in}(t)$. It will cause a change (perturbation) in the steady state values of the inductor currents and capacitor voltages. Thus the instantaneous state-space variable vector $\mathbf{x}(t)$ and output $\mathbf{v_o}(t)$ become $\mathbf{x}(t) = \mathbf{X} + \hat{\mathbf{x}}(t)$ and $\mathbf{v_o}(t) = \mathbf{V_o} + \hat{\mathbf{v}}_o(t)$. After addition of perturbation, the state space equation becomes

$$\dot{\mathbf{X}} + \dot{\hat{\mathbf{x}}}(t) = \mathbf{A_{av}}(\mathbf{X} + \hat{\mathbf{x}}(t)) + \mathbf{B_{av}}(V_{in} + \hat{v}_{in}(t)) \tag{4.88}$$

$$\mathbf{V_o} + \hat{\mathbf{v}}_o(t) = \mathbf{Z_{av}}(\mathbf{X} + \hat{\mathbf{x}}(t)) \tag{4.89}$$

4.8.1 Steady-state analysis

Steady-state values of the state variables are denoted by I_{L_i}, V_C, I_{L_1}, I_{L_2}, V_{C_f}. The steady-state equation is provided by

$$\mathbf{X} = [I_{L_i}\ V_C\ I_{L_1}\ I_{L_2}\ V_{C_f}]^T = -\mathbf{A_{av}}^{-1}\mathbf{B_{av}}V_{in} \tag{4.90}$$

In ideal case the parasitics r_L and r_{L_i} are neglected as $r_L, r_{L_i} << R$. Therefore the steady-state values of the state variables are $\mathbf{X} = \left[I_{L_i}\ V_C\ I_{L_1}\ I_{L_2}\ V_{C_f}\right]^T = \left[\frac{3\alpha^2 V_{in}}{2R(2-\alpha)^2}\ \frac{V_{in}}{2-\alpha}\ \frac{\alpha V_{in}}{2R(2-\alpha)}\ \frac{\alpha V_{in}}{2R(2-\alpha)}\ \frac{\alpha V_{in}}{2-\alpha}\right]^T$.

4.8.2 Open loop transfer function

By substituting Equations (4.85), (4.86) and (4.87) into Equations (4.88) and (4.89) and doing the *Laplace* transformation of Equations (4.88) and (4.89), the voltage to duty ratio transfer function, $G_{v\alpha}(s)$, is derived by neglecting the steady-state and nonlinear parts, and

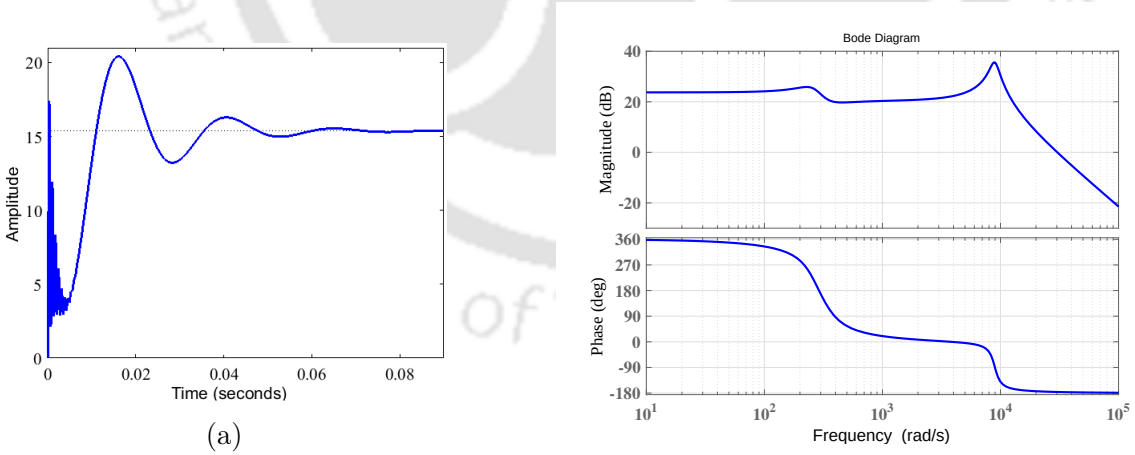
considering $\hat{v}_{in} = 0$.

$$G_{v\alpha}(s) = \frac{\hat{v}_o(s)}{\hat{\alpha}(s)} = \mathbf{Z_{av}}(s\mathbf{I} - \mathbf{A_{av}})^{-1}[(\mathbf{A_1} + \mathbf{A_3} - 2\mathbf{A_2})\mathbf{X} + (\mathbf{B_1} + \mathbf{B_3} - 2\mathbf{B_2})V_{in}] + (\mathbf{Z_1} + \mathbf{Z_3} - 2\mathbf{Z_2})\mathbf{X} \quad (4.91)$$

The required parameter values to design the HSDIBuC-DWCI are provided in Table 4.2. By using the value of these parameters and Equations (3.62), the following control power stage transfer function $G_{v\alpha}(s)$ is developed.

$$G_{v\alpha}(s) = \frac{a_3 s^3 + a_2 s^2 + a_1 s + a_0}{s^5 + b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \quad (4.92)$$

The coefficient of Equations (4.92) are provided as $a_3 = 8.4011 \times 10^8$, $a_2 = 4.8423 \times 10^{10}$, $a_1 = 4.32 \times 10^{13}$, $a_0 = 2.2585 \times 10^{16}$, $b_4 = 1.948 \times 10^3$, $b_3 = 8.0692 \times 10^7$, $b_2 = 3.2057 \times 10^{10}$, $b_1 = 8.5838 \times 10^{12}$, $b_0 = 1.4692 \times 10^{15}$. The step response of the uncompensated power stage transfer function ($G_{v\alpha}(s)$) is shown in Figure 4.12a. The rise time (t_r) and settling time (t_s) are 0.000175 s and 0.0555 s respectively. The bode diagram of the transfer function $G_{v\alpha}(s)$ is shown in Figure 4.12b. A pair of complex zero lies right-half of the s-plane. Thus, the open loop system is a non-minimum phase system and the phase margin is 3.85°.



(a) (b)

Figure 4.12: Time and frequency domain responses of $G_{v\alpha}(s)$ (a) Step response, and (b) Bode diagram

4.9 Control Scheme

In voltage mode control (VMC) framework, to improve the transient behaviour and to enable the feedback control circuit, a proportional integral (PI) controller is designed using frequency domain method. The block diagram representation of the closed loop system is shown in Figure 4.13. The controller is defined as

$$G_c(s) = K_p + \frac{K_i}{s} \tag{4.93}$$

where K_p and K_i are proportional and integral constants respectively and the values are $K_p = 0.001205$ and $K_i = 40$ respectively.

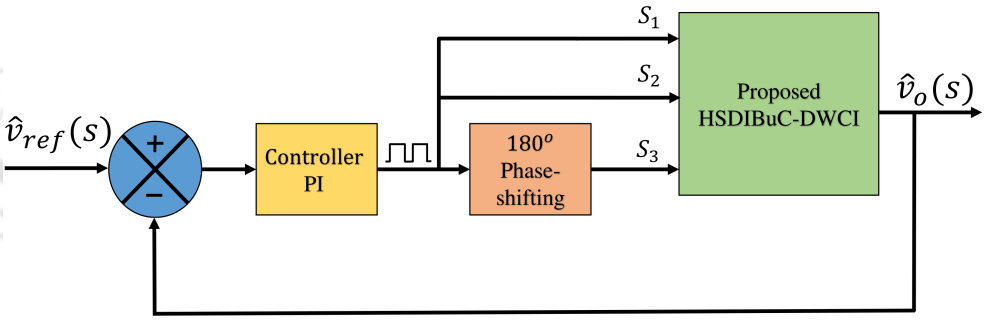


Figure 4.13: Block diagram representation of the closed-loop control system

4.10 Simulation Results

By using MATLAB-Simscape tools, the simulation is carried out. The results of the ripple, Δi_L, in i_{L_1} and i_{L_2} are shown in Figure 4.14. At $\alpha = 0.40$ and $k = 0.50$, the ripple is calculated to be $\Delta i_L = 296.29$ mA by using Equation (4.43). At the same α and k values, the simulation provides $\Delta i_L = 295.9$ mA closed to the calculated value of 296.29 mA. When $k = 0$, i.e. two single inductors are used, the ripple Δi_L is 333.33 mA for $\alpha = 0.40$. Thus, DWCI improves the ripple in inductor current. At $\alpha = 0.55$, the simulation provides $\Delta i_L = 297.7$ mA and $\Delta i_L = 380.3$ mA for the coupling factor $k = 0.5$ and $k = 0$ respectively. In Figure 4.15, the open loop transient response of the output voltage v_o is shown. The maximum peak overshoot (M_p) and settling time (t_s) of the HSDIBuC-DWCI are $M_p = 15.87$ % and $t_s = 0.00195$ s respectively. When the coupling factor $k = 0$, i.e. for HSDIBuC, the M_p and t_s are 30.82% and 0.00345 s respectively. It clearly shows that the DWCI improves the transient behaviour of the proposed HSDIBuC.

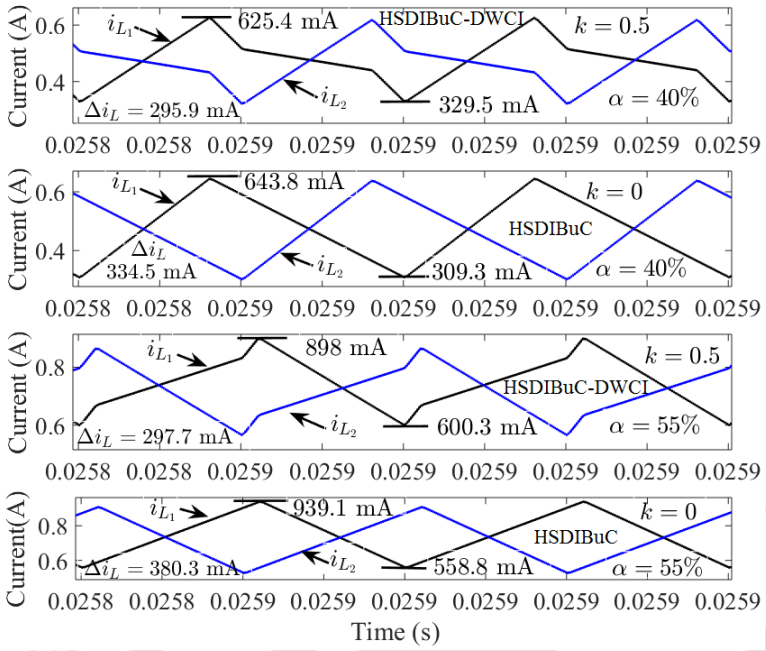


Figure 4.14: Simulations results for inductor current ripple Δi_L of i_{L_1} and i_{L_2} of (a) HSDIBuC at $\alpha = 0.40$, (b) HSDIBuC-DWCI at $\alpha = 0.40$, (c) HSDIBuC at $\alpha = 0.55$, (d) HSDIBuC-DWCI at $\alpha = 0.55$.

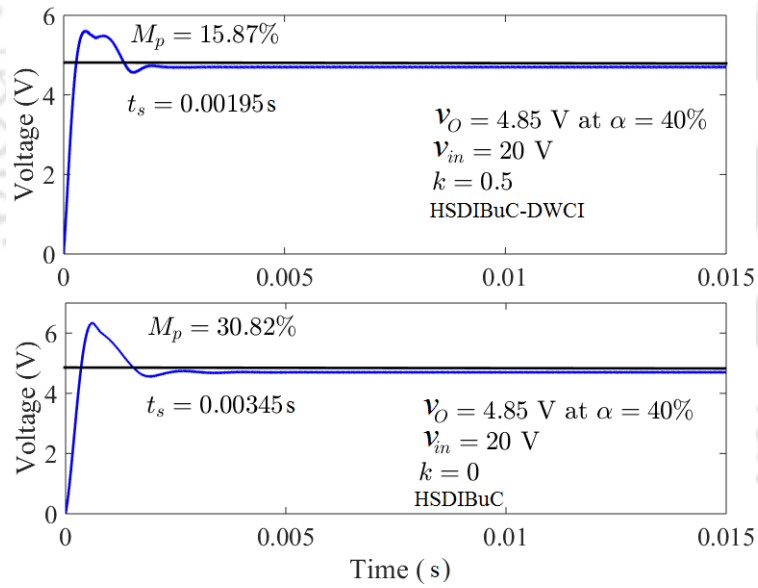


Figure 4.15: Open-loop transient response of output voltages for $\alpha = 0.40$ of HSDIBuC-DWCI with $k = 0.5$, and HSDIBuC.

4.11 Experimental Setup and Results

The schematic diagram of the closed-loop control systems of HSDIBuC-DWCI is shown in Figure 4.16. The switches S_1 and S_2 are turned ON and OFF simultaneously as described

in Section 4.2. Two 180° phase-shifted pulses are generated. One of the pulses is used to control S1 and S2 simultaneously, each driven through a MOSFET gate driver optocoupler, viz. FOD3180. The other pulse drives S3 through another FOD3180.

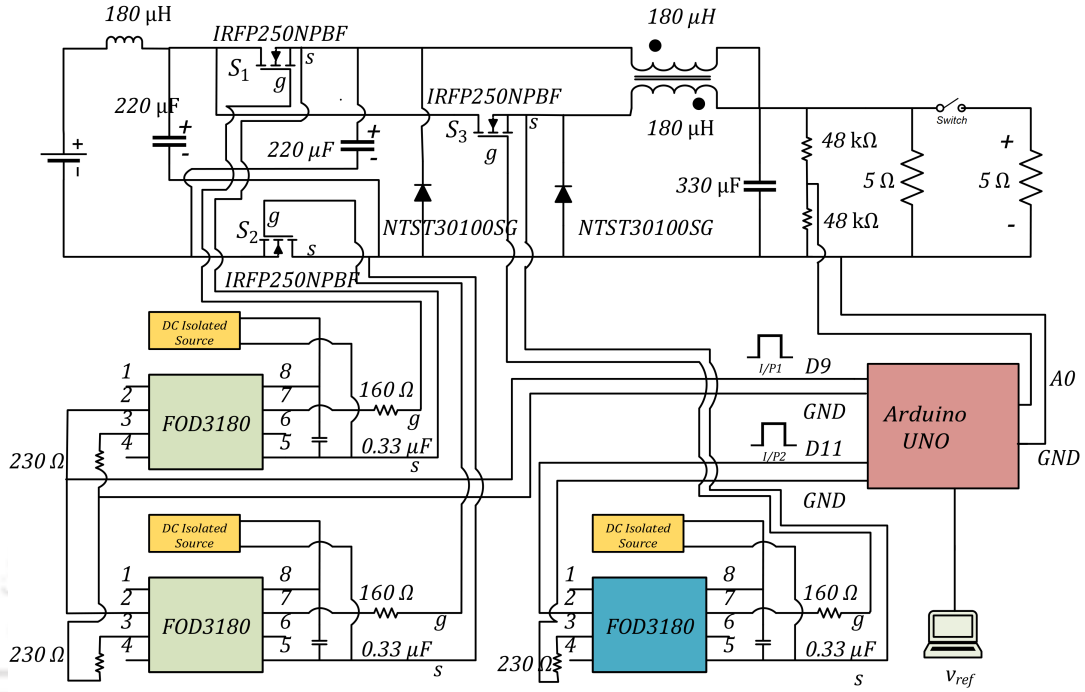


Figure 4.16: Schematic circuit diagram of the closed-loop control systems of HSDIBuC-DWCI

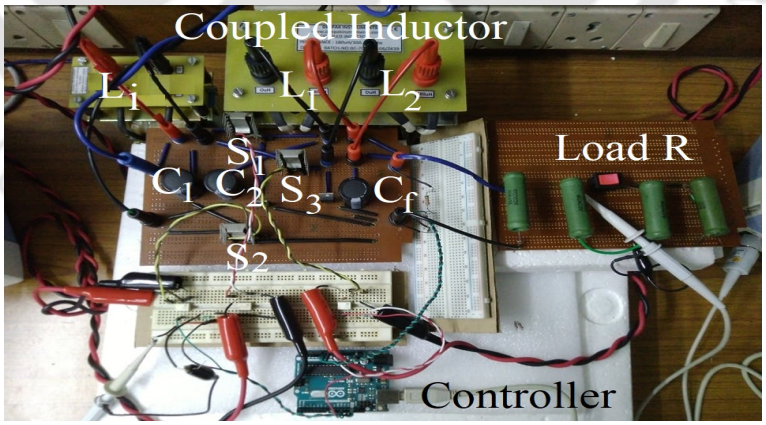


Figure 4.17: Experimental setup of the HSDIBuC-DWCI

The experimental setup is shown in Figure 4.17. The parameter values used to design the proposed HSDIBuC-DWCI are provided in Table 4.2. The switches S_1, S_2 and S_3 are implemented by n-channel MOSFETs IRF250NPBF. The diodes D_1 and D_2 are implemented

by NTST30100SG/ NFK03TS30100SG. As shown in Figure 4.18, DWCI is designed by using U/C-type ferrite core. The gap between the two cores is 0.1 mm. The maximum current rating of the coupled inductor is 8 A. The magnetic cross-section area of the core is 2.4 cm^2. There are 20 number of turns in each primary (N_p) and secondary (N_s) winding. The turns ratio is defined by $(N_p)/(N_s) = 1$.

The experiment is carried out in two stages. In the first stage, the ripple Δi_L in i_{L_1} and i_{L_2} is checked. In the second stage, the closed-loop part is enabled and the closed-loop performance is tested with the PI controller. The PI controller is implemented by Arduino Uno microcontroller board. HAMEG HZO50 AC/DC current probe is used to capture the current waveforms.

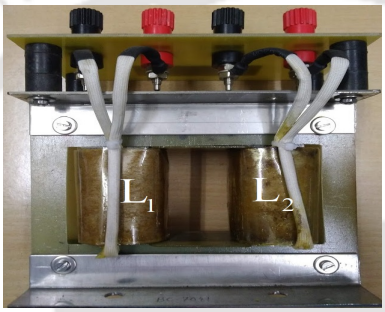


Figure 4.18: Dual-winding coupled inductor (DWCI)

4.11.1 Ripple improvement

In this stage of experiment, closed loop part is disabled and the proposed HSDIBuC is tested with DWCI at the output side. The input side inductor L_i is not affected by the coupling factor of DWCI and its current waveform is shown in Figure 4.19.

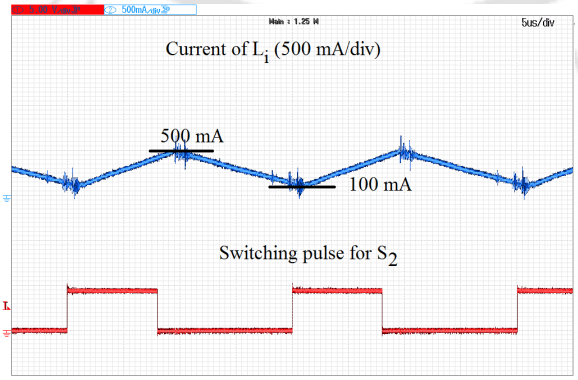
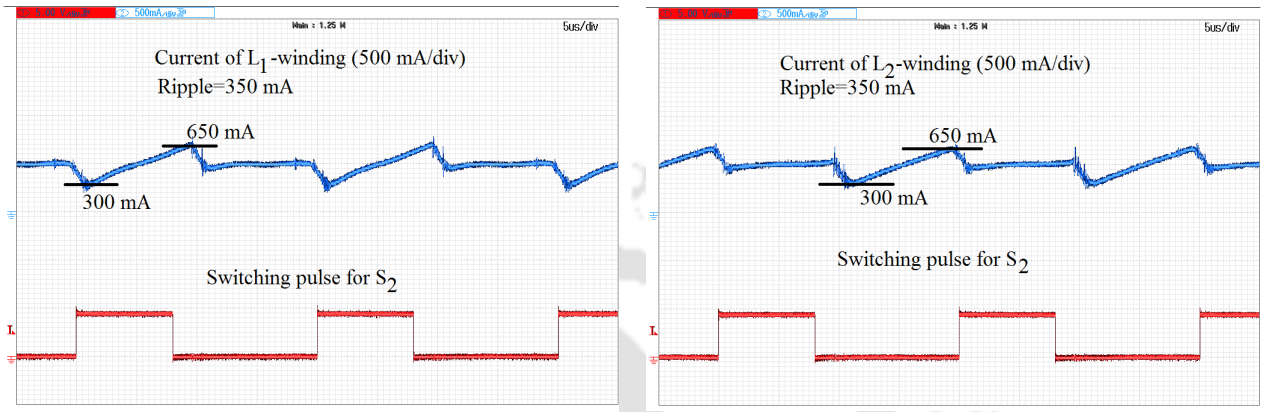


Figure 4.19: i_{L_i} through L_i- inductor for $\alpha = 0.40$

The currents through the L_1 and L_2 windings of DWCI are shown in Figures 4.20a and

4.20b respectively. When the duty ratio is 0.40, the ripple in i_{L_1} and i_{L_2} is Δi_L =350 mA for $k = 0.5$. The experimental ripple value is close to the theoretical and simulated values. The waveforms are plotted with respect to the switching pulse for S_2 and the phase shift between ripple waveforms of i_{L_1} and i_{L_2} is evident.



(a) (b)

Figure 4.20: Experimental results for $\alpha = 0.40$ and $k = 0.5$ (a) i_{L_1}, and (b) i_{L_2}.

When the α is 0.55, the ripple in L_2 winding is 350 mA as shown in Figure 4.21. The percentage of errors of Δi_L between simulation and experimental results are 18.28 % and 17.5 % respectively for $\alpha = 0.40$ and $\alpha = 0.55$.

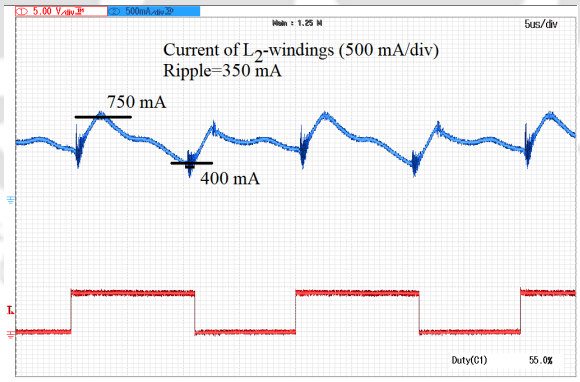
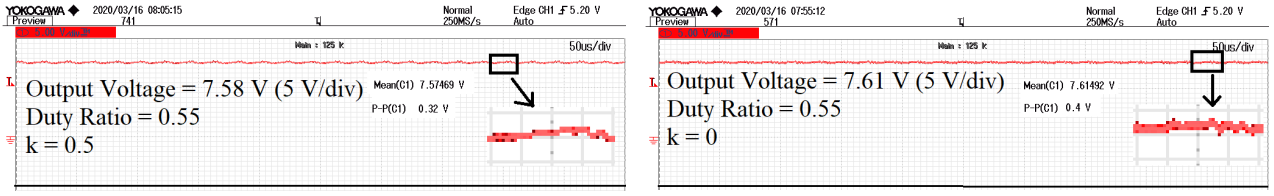


Figure 4.21: i_{L_2} through L_2-Winding for $\alpha = 0.55$

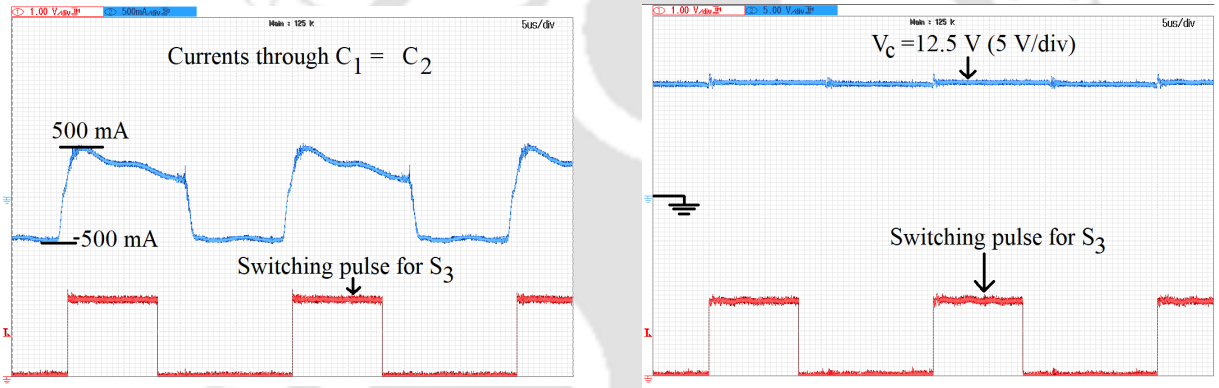
The output voltage v_o and ripple in output voltage are 7.58 V and 0.32 V for $\alpha = 0.55$ and $k = 0.5$ as shown in Figure 4.22a. When DWCI is replaced by two single inductors i.e. $k = 0$, the ripple in output voltage is 0.4 V as shown in Figure 4.22b. Thus, the coupled inductor reduces the ripple in v_o deducing that the value of output filter capacitor can be lower.



(a) (b)

Figure 4.22: Waveform of output voltage for $\alpha = 0.55$ (a) $v_o = 7.58$ V with 0.32 V ripple when $k = 0.5$, (b) $v_o = 7.61$ V with 0.40 V ripple when $k = 0$

The current flowing through the two identical capacitors is shown in Figure 4.23a for $\alpha = 0.40$. The voltage across the capacitors v_C is shown in Figure 4.23b. It shows that $v_C = 12.5$ V satisfies Equation (4.31) for $\alpha = 0.40$.

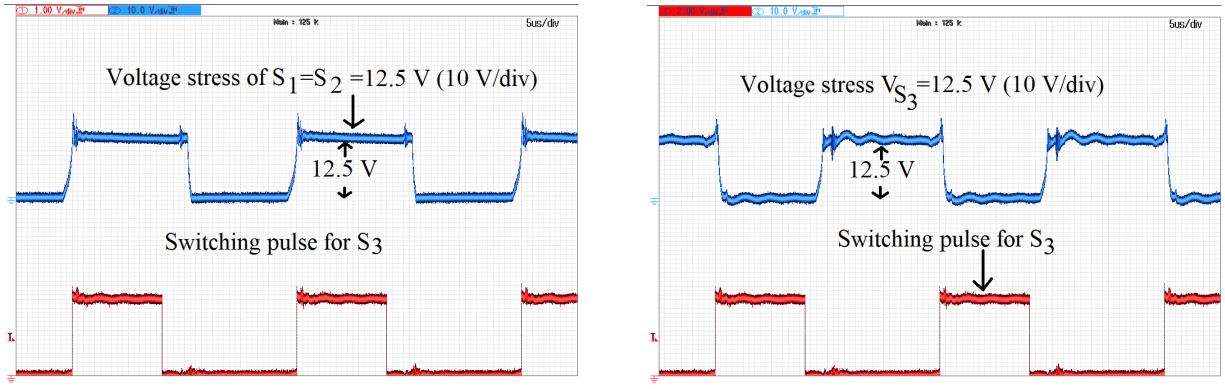


(a) (b)

Figure 4.23: Experimental results of identical capacitors ($C_1 = C_2$) for $\alpha = 0.40$ (a) i_c, and (b) v_C

4.11.2 Stresses of switches and diodes

The voltage stresses of S_1, S_2 and S_3 are shown in Figure 4.24a and Figure 4.24b respectively. The voltages stresses of the switches satisfy Equation (4.79) and which gives $v_S = v_{in}/(2-\alpha) = 12.50$ V for $\alpha = 0.40$. The diode voltage stress $v_D = v_{in}/(2-\alpha) = 12.50$ V for $\alpha = 0.40$ is shown in Figure 4.25. It is evident that the semiconductor devices suffer the voltage stress less than the input voltage $v_{in} = 20$ V.



(a) (b)

Figure 4.24: Voltage stress for $\alpha = 0.40$ (a) $v_{S_1} = v_{S_2} = 12.5$ V, (b) $v_{S_3} = 12.5$ V

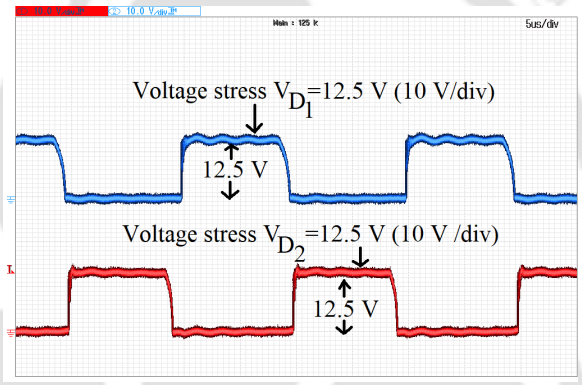
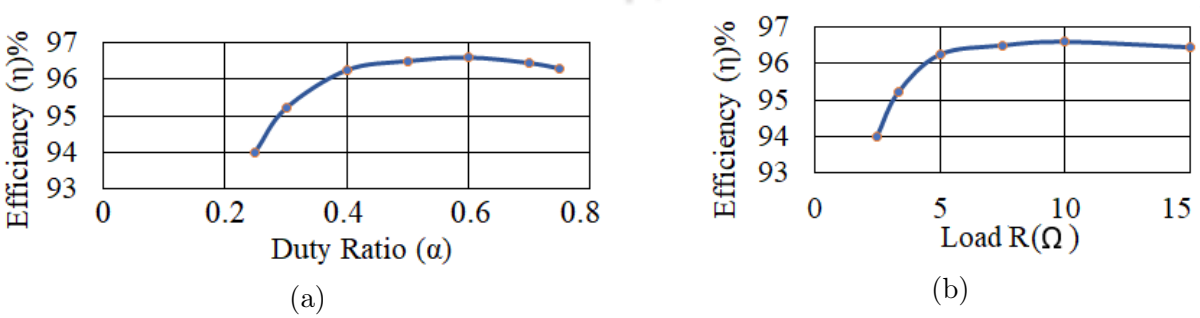


Figure 4.25: Voltage stress $v_{D_1} = v_{D_2} = 12.5$ V for $\alpha = 0.40$.

The experimental results of efficiency due to changes of duty ratio and load are shown in Figures 4.26a and 4.26b respectively. The comparisons of experimental results of HSDIBuC and HSDIBuC-DWCI are shown in Table 4.4. Efficiency of 96.4% is achieved at $\alpha = 0.55$, $v_{in} = 20$ V and $R = 5\ \Omega$.



(a) (b)

Figure 4.26: Experimental efficiency plots due to (a) Duty ratio change, and (b) Load R change

Table 4.4: Comparison of experimental results of HSDIBuC and HSDIBuC-DWCI

Items	The proposed HSDIBuC	The proposed HSDIBuC-DWCI
Efficiency $\eta\big\vert_{\alpha=0.55}$	96.2%	96.4%
Ripple $\Delta i_L\big\vert_{\alpha=0.40}$	400 mA	350 mA

4.11.3 Closed loop performance

In this stage, feedback part is enabled and closed loop performance is investigated. The designed PI controller makes the closed loop system stable. The change of input current i_{L_i} due to change in output voltage reference (v_{ref}) viz. 5 , 7 and 9 V is shown in Figure 4.27.

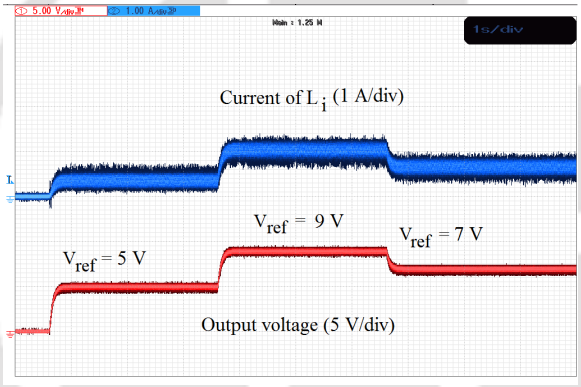


Figure 4.27: Change of i_{L_i} due to change in output voltage reference

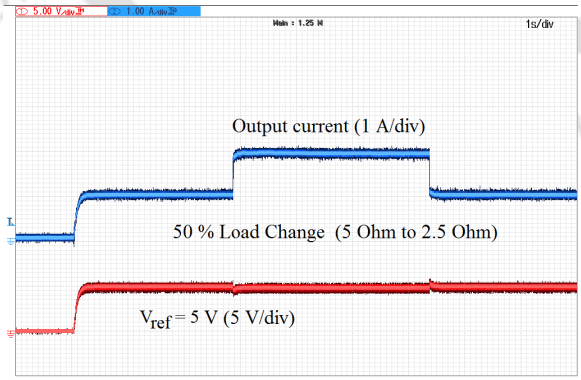


Figure 4.28: Output voltage and current waveforms for 50 % load change

It is seen that the there is no overshoot in the output voltage and the rise time t_r is 0.05 s. The output voltage follows the v_{ref} change. Now to check the sensitivity to the load parameter

variation, 50% output load (R) change is carried out as shown in Figure 4.28. During the load resistance change from 5 Ω to 2.5 Ω and 2.5 Ω to 5 Ω, the output voltage v_o follows the $v_{ref} = 5$ V.

4.12 Summary

A two-phase dc-dc HSDIBuC with a dual-winding coupled inductor (DWCI) is proposed to improve the ripple in current through the branches of DWCI. Two C/U cores are used to design the DWCI and are coupled inversely to improve the ripple. The coupling effect on the reduction of the minimum value of the output filter capacitor is derived and it shows that the coupling factor helps to reduce the capacitance value. The range of coupling factor for given conditions of duty ratio and ripple is developed. Simulations results are provided to validate the claims. Further, the effect of DWCI is shown to improve the transient behaviour of the proposed converter. At $\alpha = 0.40$ and $\alpha = 0.55\%$, experimental results are provided in an open-loop to observe the performance of the DWCI. The DWCI improves ripple and does not affect the steady-state output voltage. A voltage mode PI controller is designed to enable the closed-loop systems and experimental closed-loop results are provided.

5

High Step-up Boost Converter

In this chapter, a high step-up conversion ratio DC-DC boost converter with improved ripple is proposed using a diode capacitor cell and a dual-winding directly coupled coupled-inductor operating in continuous conduction mode (CCM). The proposed converter achieves step-up conversion ratio larger than the conventional boost converter by using a diode-capacitor cell. The cell consists of two cross-connected identical capacitors and two diodes placed in parallel. An inductor is required at the output-end to oppose the sudden change in load current due to series-parallel configuration of the two identical capacitors of the cell. Thus, the converter requires two inductors to implement the converter. These two inductors are replaced by a dual-winding directly-coupled coupled-inductor. This modification in the circuit improves the ripples in input current, inductor current and output voltage without affecting the conversion ratio. Apart from that, the reduction of size of magnetic core also reduces the cost and bulkiness of the proposed converter.

5.1 Introduction

In chapters 2, 3 and 4, the voltage conversion ratio of the conventional buck converter (CBuC) and conventional interleaved buck converter (CIBuC) are modified using a switch-capacitor cell to avoid the narrow duty cycle when a high-input to low-output voltage conversion is required. Similarly, when low-input to high-output voltage conversion is desired, the conventional boost converter (CBoC) needs a wide duty ratio causing more conduction loss which affects the overall efficiency of the converter. Moreover, the voltage stresses of the semiconductor devices of CBoC is equal to the high-output voltage causing increased voltage ratings of the active elements. These issues can be solved by enhancing the voltage conversion ratio of the CBoC using a diode-capacitor cell [90, 91]. The construction of the diode-capacitor cell is very similar to the switch-capacitor cell. In the diode-capacitor cell, the two diodes are placed in parallel and two identical capacitors are cross-connected. The high step-up gain of CBoC is achieved by the series-parallel transition of two identical capacitors. Due to these series-parallel transitions, a sudden directional change in output current-flow takes place. To prevent this sudden change, an extra inductor is required at the output end. Therefore, the high step-up boost converter (HSUBoC) requires two single inductors. These, two single inductors can be replaced by a directly-coupled dual-winding coupled inductor (DWCI) to further reduce the ripple in input current, inductor current and output voltage. Hence, in this chapter, a ripple improved HSUBoC with DWCI is proposed and the advantages are discussed with detailed analysis.

The chapter is organized as follows. In Section 5.2, the circuit configuration of the proposed HSUBoC with DWCI is explained. The reduction of ripple in the inductor currents is discussed in Section 5.3. In Section 5.4, the reduction of ripple in input current is determined. The reduction of output voltage ripple is analysed in Section 5.5. The voltage and current stresses analyses are provided in Section 5.6. In Section 5.7, power losses and efficiency are discussed. Small-signal modelling of HSUBoC with DWCI is provided in Section 5.8. Section 5.9 provides the simulation results. The experimental results are presented in Section 5.10. Finally, Section 5.11 summarises the chapter.

5.2 Circuit Configuration of Proposed Converter

Figure 5.1 shows circuit configuration of the proposed improved-ripple HSUBoC using a directly coupled DWCI operating in continuous conduction mode (CCM). The input voltage v_{in} is connected with the L-winding of the coupled inductor followed by a switch S. r_L is the parasitic of L-winding. Two identical capacitors C_1 and C_2 are placed in cross with diodes D_1 and D_2 in parallel. When the switch S does not conduct, the two capacitors are charged in parallel by the energy stored in the L-winding. When the switch S conducts, these two identical capacitors become in series through S. The L_f-winding of the coupled inductor is mounted to oppose the sudden change in output current caused by the series-parallel transition of the two capacitors. r_L and r_{L_f} are the parasitics of L-windings and L_f-windings respectively. Followed by L_f-winding, a capacitor C_f with parasitic r_{C_f} is placed at the output end. v_o is the output voltage at load resistance R. The parasitics $r_L, r_{L_f}, r_{C_f} << R$, thus, these are negligible. $C_1 = C_2 = C$ and $L = L_f$ are considered for further analysis.

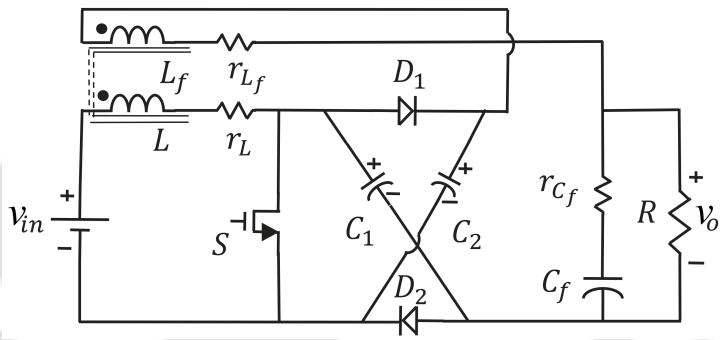


Figure 5.1: The proposed high step-up boost converter (HSUBoC) with dual-winding coupled inductor (DWCI)

5.2.1 Coupled inductor

The magnetic structure of the coupled inductor which is used to develop the converter is shown in Figure 5.2.

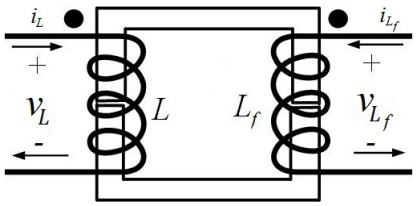


Figure 5.2: Magnetic structure of dual-winding coupled inductor (DWCI)

The generalized equation of the coupled inductor is

$$v_L = L\frac{di_L}{dt} \pm M\frac{di_{L_f}}{dt} \tag{5.1}$$

$$v_{L_f} = L_f\frac{di_{L_f}}{dt} \pm M\frac{di_L}{dt} \tag{5.2}$$

where i_L and i_{L_f} are currents through L and L_f windings respectively. v_L and v_{L_f} are the voltages across L and L_f windings respectively. The mutual inductance M is defined as $M = k\sqrt{LL_f}$. For inductor to be direct coupled, the coupling factor $k \in [0, 1]$, and to be inverse coupled, $k \in [0, -1]$. To improve the ripple, a directly coupled dual-windings coupled-inductor is used. Therefore, Equations (5.1) and (5.2) can be written as follows.

$$\int_0^{T_s} di_L = \frac{v_L}{(1-k^2)L}\int_0^{T_s} dt - \frac{v_{L_f}k\sqrt{\frac{L}{L_f}}}{(1-k^2)L}\int_0^{T_s} dt \tag{5.3}$$

$$\int_0^{T_s} di_{L_f} = \frac{v_{L_f}}{(1-k^2)L_f}\int_0^{T_s} dt - \frac{v_L k\sqrt{\frac{L_f}{L}}}{(1-k^2)L_f}\int_0^{T_s} dt \tag{5.4}$$

5.2.2 Switching modes

There are basic two switching states in one time period T_s as shown in Figure 5.3. α is denoted by duty ratio. The switching operations are described below.

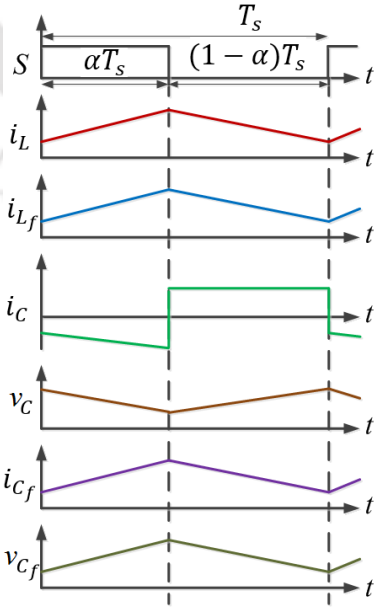


Figure 5.3: Idealized waveform of the proposed improved-ripple converter HSUBoC with DWCI

5.2.2.1 ON-state $(0 < t < \alpha T_s)$ of HSUBoC

In this duration the switch S is ON and the diodes D_1 and D_2 are in reversed biased as shown in Figure 5.4. The two identical capacitors are in series. Thus, the resultant voltage becomes $v_C + v_C = 2v_C$, where v_C is the voltage across the identical capacitors C. The voltage across the output capacitor is v_{C_f}. The voltage equations of inductors are as follows.

$$v_L = L\frac{di_L}{dt} + M\frac{di_{L_f}}{dt} = v_{in} \tag{5.5}$$

$$v_{L_f} = L_f\frac{di_{L_f}}{dt} + M\frac{di_L}{dt} = 2v_C - v_{C_f} \tag{5.6}$$

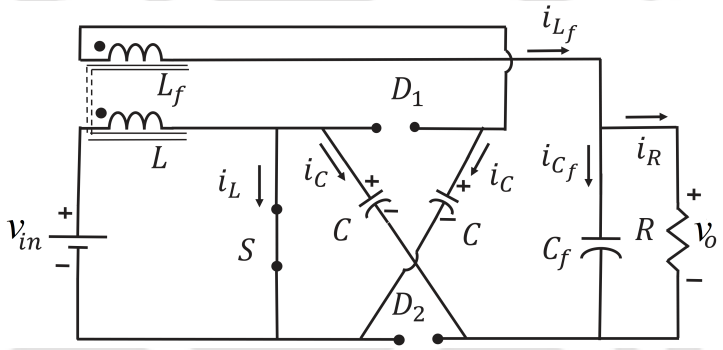


Figure 5.4: ON-state circuit configuration of HSUBoC with DWCI

The current i_C through the two identical capacitors is

$$i_C = C\frac{dv_C}{dt} = -i_{L_f} \tag{5.7}$$

The load current i_R is determined by

$$i_R = i_{L_f} - i_{C_f} \tag{5.8}$$

where i_{C_f} is the current flowing through the C_f and is defined by $i_{C_f} = C_f\frac{dv_{C_f}}{dt}$. The output voltage equation is given by

$$v_o = v_{C_f} = Ri_R \tag{5.9}$$

Let us define the state vector $\mathbf{x}(t) = [i_L\ v_C\ i_{L_f}\ v_{C_f}]^T$ and the output vector as $\mathbf{y}(t) = v_o$. The state-space representation of the ON-state is as follows.

$$\dot{\mathbf{x}}(t) = \mathbf{A_1}\mathbf{x}(t) + \mathbf{B_1}v_{in}(t)$$

$$= \begin{bmatrix} 0 & \frac{-2M}{LL_f - M^2} & 0 & \frac{M}{LL_f - M^2} \\ 0 & 0 & \frac{-1}{C} & 0 \\ 0 & \frac{2L}{LL_f - M^2} & 0 & \frac{-L}{LL_f - M^2} \\ 0 & 0 & \frac{1}{C_f} & \frac{-1}{RC_f} \end{bmatrix} \mathbf{x}(t) + \begin{bmatrix} \frac{L_f}{LL_f - M^2} \\ 0 \\ \frac{-M}{LL_f - M^2} \\ 0 \end{bmatrix} v_{in}(t) \tag{5.10}$$

$$\mathbf{y}(t) = \mathbf{Z_1}\mathbf{x}(t) = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \mathbf{x}(t) \tag{5.11}$$

5.2.2.2 OFF-state ($\alpha T_s < t < T_s$) of HSUBoC

During this interval, switch S is in OFF-state. D_1 and D_2 are in foreword biased. Thus, the two identical capacitors are in parallel as shown in Figure 5.5.

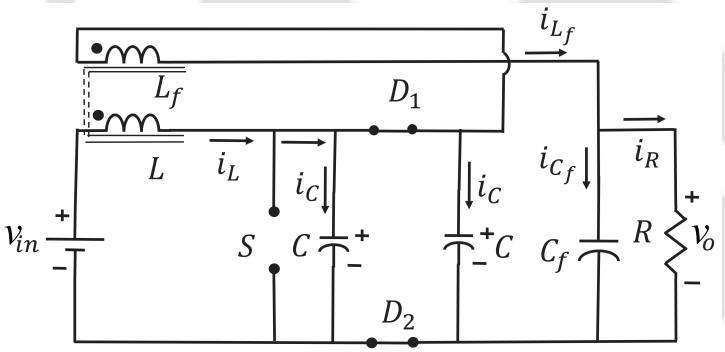


Figure 5.5: OFF-state circuit configuration of HSUBoC with DWCI

The voltage and current equations are derived as follows.

$$v_L = L\frac{di_L}{dt} + M\frac{di_{L_f}}{dt} = v_{in} - v_C \tag{5.12}$$

$$v_{L_f} = L_f\frac{di_{L_f}}{dt} + M\frac{di_L}{dt} = v_C - v_{C_f} \tag{5.13}$$

$$2i_C = i_L - i_{L_f} \text{where } i_C = C\frac{dv_C}{dt} \tag{5.14}$$

The equations for load current (i_R) and output voltage v_o are the same as Equations (5.8) and

(5.9) respectively. The state-space representation of the OFF-state is as follows.

$$\begin{aligned}\dot{\mathbf{x}}(t) &= \mathbf{A_2}\mathbf{x}(t) + \mathbf{B_2}v_{in}(t) \\ &= \begin{bmatrix} 0 & \frac{-(M+L_f)}{LL_f - M^2} & 0 & \frac{M}{LL_f - M^2} \\ \frac{1}{2C} & 0 & \frac{-1}{2C} & 0 \\ 0 & \frac{L+M}{LL_f - M^2} & 0 & \frac{-L}{LL_f - M^2} \\ 0 & 0 & \frac{1}{C_f} & \frac{-1}{RC_f} \end{bmatrix} \mathbf{x}(t) + \begin{bmatrix} \frac{L_f}{LL_f - M^2} \\ 0 \\ \frac{-M}{LL_f - M^2} \\ 0 \end{bmatrix} v_{in}(t) \end{aligned} \tag{5.15}$$

$$\mathbf{y}(t) = \mathbf{Z_2}\mathbf{x}(t) = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \mathbf{x}(t) \tag{5.16}$$

5.2.3 Voltage conversion ratio

By using the voltage second balance (VSB) equation, the steady-state voltage conversion ratio is determined. By using Equations (5.5) and (5.12), the VSB equation of inductor L is

$$\begin{aligned} \int_0^{\alpha T_s} v_L dt + \int_{\alpha T_s}^{T_s} v_L dt = 0 \\ \frac{v_C}{v_{in}} = \frac{1}{1-\alpha} \end{aligned} \tag{5.17}$$

The VSB equation of L_f is derived by using Equations (5.6) and (5.13) as follows.

$$\begin{aligned} \int_0^{\alpha T_s} v_{L_f} dt + \int_{\alpha T_s}^{T_s} v_{L_f} dt = 0 \\ \frac{v_o}{v_C} = 1 + \alpha \end{aligned} \tag{5.18}$$

Therefore, from Equations (5.17) and (5.18), the voltage conversion ratio is determined as

$$\frac{v_o}{v_{in}} = \frac{1+\alpha}{1-\alpha} \tag{5.19}$$

From Equation (5.19), it is seen that the mutual inductance of DWCI does not affect the steady-state step-up voltage conversion ratio.

5.3 Ripple in Inductor Current

The ripple in current through the the windings of DWCI is analyzed here in this section. Firstly, ripple current in L winding is analyzed followed by that in L_f winding.

5.3.1 Ripple current in L-winding

ON-state $(0 < t < \alpha T_s)$: During the switching interval $(0 < t < \alpha T_s)$, the instantaneous inductor current $i_L(\alpha T_s)$ can be derived by using Equation (5.3).

$$\begin{aligned}
\int_0^{\alpha T_s} di_L &= \frac{v_L}{(1-k^2)L}\int_0^{\alpha T_s} dt - \frac{v_{L_f} k\sqrt{\frac{L}{L_f}}}{(1-k^2)L}\int_0^{\alpha T_s} dt \\
i_L(\alpha T_s) - i_L(0) &= \frac{\alpha T_s}{(1-k^2)L}(v_{in} - k(2v_C - v_o)) \\
i_L(\alpha T_s) &= \frac{\alpha T_s v_{in}}{(1+k)L} + i_L(0)
\end{aligned} \tag{5.20}$$

OFF-state $(\alpha T_s < t < T_s)$: In the next switching interval $(\alpha T_s < t < T_s)$, the instantaneous current $i_L(T_s)$ through the L-winding is given by

$$\begin{aligned}
\int_{\alpha T_s}^{T_s} di_L &= \frac{v_L}{(1-k^2)L}\int_{\alpha T_s}^{0} dt - \frac{v_{L_f} k\sqrt{\frac{L}{L_f}}}{(1-k^2)L}\int_{\alpha T_s}^{0} dt \\
i_L(T_s) - i_L(\alpha T_s) &= \frac{(1-\alpha)T_s}{(1-k^2)L}((v_{in} - v_C) - k(v_C - v_o)) \\
i_L(T_s) &= \frac{\alpha T_s v_{in}}{(1+k)L} + i_L(\alpha T_s)
\end{aligned} \tag{5.21}$$

Therefore, the ripple in inductor current of the L-winding is

$$\Delta i_L = i_L(\alpha T_s) - i_L(0) = \frac{\alpha T_s v_{in}}{(1+k)L} \tag{5.22}$$

In the existing converter, the ripple in inductor L is $\Delta i_L = \frac{\alpha T_s v_{in}}{L}$ [90]. Therefore, it is seen that DWCI helps to reduce ripple in inductor current.

5.3.2 Ripple current in L_f-winding

ON-state $(0 < t < \alpha T_s)$: In this duration $(0 < t < \alpha T_s)$, the instantaneous inductor current $i_{L_f}(\alpha T_s)$ is determined by using Equation (5.4) as follows.

$$\begin{aligned} i_{L_f}(\alpha T_s) &= \frac{\alpha T_s((2v_C - v_o) - kv_{in})}{(1-k^2)L_f} + i_{L_f}(0) \\ &= \frac{\alpha T_s v_{in}}{(1+k)L_f} + i_{L_f}(0) \end{aligned} \tag{5.23}$$

In the next interval $(\alpha T_s < t < T_s)$, the instantaneous inductor current $i_{L_f}(T_s)$ is derived

$$i_{L_f}(T_s) = i_{L_f}(\alpha T_s) + \frac{(1-\alpha)T_s(v_C - v_{C_f} - k(v_{in} - v_C))}{(1-k^2)L_f} = i_{L_f}(0) \tag{5.24}$$

Therefore, the ripple current of L_f-winding is as follows.

$$\Delta i_{L_f} = i_{L_f}(\alpha T_s) - i_{L_f}(0) = \frac{\alpha T_s v_{in}}{(1+k)L_f} \tag{5.25}$$

5.4 Ripple in Input Current

Let us consider that the duty ratio and ripple in input current of the CBoC are α_c and Δi_c respectively. α and Δi_{in} are respectively the duty ratio and the ripple in input current of the proposed HSUBoC. The ripple in input current in CBoC is $\Delta i_c = \frac{\alpha_c T_s v_{in}}{L}$ [124]. The ripple in input current in the proposed HSUBoC is $\Delta i_{in} = \frac{\alpha T_s v_{in}}{(1+k)L}$. The relation between these two input currents is

$$\frac{\Delta i_{in}}{\Delta i_c} = \frac{\alpha}{(1+k)\alpha_c} \tag{5.26}$$

The voltage conversion ratio of CBoC is $\frac{v_o}{v_{in}} = \frac{1}{(1-\alpha_c)}$. It is seen that the two converters have equal output voltage when α and α_c are related as follows.

$$\alpha = \frac{\alpha_c}{2 - \alpha_c} \tag{5.27}$$

Substituting Equations (5.27) into (5.26), the following relation is developed.

$$\frac{\Delta i_{in}}{\Delta i_c} = \frac{1}{(1+k)(2-\alpha_c)} < 1 \quad \text{where } k \in \{0, 1\} \tag{5.28}$$

Therefore, the Equation (5.28) depicts that the use of directly-coupled DWCI can reduce the input current ripple more.

5.5 Output Voltage Ripple

The equation output voltage ripple Δv_o is provided as follows [90].

$$\Delta v_o = \frac{1}{C_f}\int_0^{\alpha\frac{T_s}{2}} \frac{\Delta i_{L_f}}{\alpha T_s} t dt + \frac{1}{C_f}\int_0^{(1-\alpha)\frac{T_s}{2}} (\frac{\Delta i_{L_f}}{2} - \frac{\Delta i_{L_f}}{(1-\alpha)t}) dt \tag{5.29}$$

By substituting $\Delta i_{L_f} = \dfrac{\alpha T_s v_{in}}{(1+k)L_f}$ into Equation (5.29), the output voltage ripple is determined as follows.

$$\Delta v_o = \frac{1}{8C_f}\frac{(1-\alpha)v_o \alpha {T_s}^2}{(1+k)(1+\alpha)L_f} \tag{5.30}$$

Therefore, output voltage ripple can be reduced using a DWCI. The summarized analytical development is shown in Table 5.1 and compared to the existing and CBoC.

Table 5.1: Comparison of the proposed HSUBoC with existing and CBoC

Items	Proposed HSUBoC	Existing [90] [91]	CBoC
v_o	$\frac{1+\alpha}{1-\alpha}v_{in}$	$\frac{1+\alpha}{1-\alpha}v_{in}$	$\frac{1}{1-\alpha}v_{in}$
Δi_L	$\frac{\alpha T_s v_{in}}{(1+k)L}$	$\frac{\alpha T_s v_{in}}{L}$	$\frac{\alpha T_s v_{in}}{L}$
Δi_{L_f}	$\frac{\alpha T_s v_{in}}{(1+k)L_f}$	$\frac{\alpha T_s v_{in}}{L_f}$	$\frac{\alpha T_s v_{in}}{L_f}$
v_S	$\frac{v_o}{1+\alpha}$	$\frac{v_o}{1+\alpha}$	v_o
Δv_o	$\frac{1}{8C_f}\frac{(1-\alpha)v_o\alpha {T_s}^2}{(1+k)(1+\alpha)L_f}$	$\frac{1}{8C_f}\frac{(1-\alpha)v_o\alpha {T_s}^2}{(1+\alpha)L_f}$	$\frac{v_o \alpha T_s}{RC_f}$

By varying the duty ratio α, the improvement of current ripple Δi_L in the L-winding is provided in Figure 5.6. It clearly shows that the ripple current in the proposed HSUBoC is less than the conventional and existing boost converters. It also shows that the ripple reduces as the coupling factor increases.

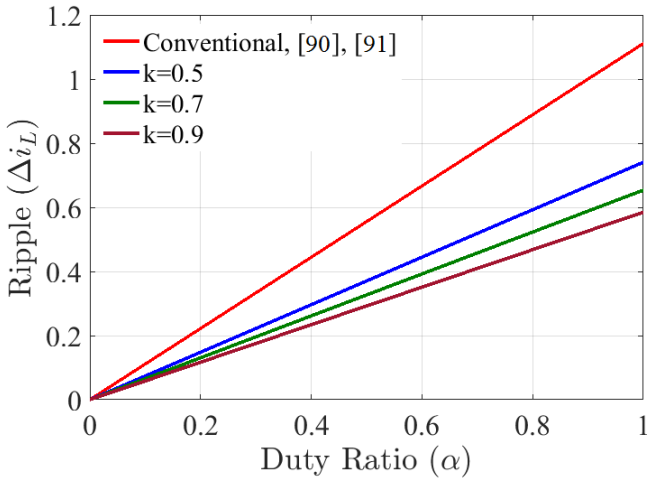


Figure 5.6: Plot of ripple current Δi_L versus duty ratio α

5.6 Voltage and Current Stresses

The voltage stresses of the semiconductor devices are expressed by neglecting the capacitive ripple voltages. The voltage stress, v_S, of the switch S and voltage stress, v_D, of the diodes D_1 and D_2 are as follows.

$$v_S = v_D = \frac{v_o}{1+\alpha} \tag{5.31}$$

Therefore, below the output voltage rated semiconductor devices with low ON-state switching resistance can be used to implement the converter. The switching current i_S through S is approximated as follows.

$$i_S = \begin{cases} \frac{(1+\alpha)i_o}{1-\alpha}, & \text{for } 0 < t \leq \alpha T_s \\ 0, & \text{for } \alpha T_s < t \leq T_s \end{cases} \tag{5.32}$$

By using Equation (5.32), the root mean square (rms) current, $I_{S_{rms}}$, through S is determined as

$$I_{S_{rms}} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_S^2 dt} = \frac{\sqrt{\alpha}(1+\alpha)i_o}{1-\alpha} \tag{5.33}$$

The diode currents i_{D_1} through D_1 and i_{D_2} through D_2 are approximated as follows.

$$i_{D_1} = \begin{cases} 0, & \text{for } 0 < t \leq \alpha T_s \\ \frac{(1+\alpha)i_o}{1-\alpha}, & \text{for } \alpha T_s < t \leq T_s \end{cases} \tag{5.34}$$

$$i_{D_2} = \begin{cases} 0, & \text{for } 0 < t \leq \alpha T_s \\ i_o, & \text{for } \alpha T_s < t \leq T_s \end{cases} \tag{5.35}$$

By using Equation (5.34), the rms current $I_{D_{1rms}}$ and average current I_{D_1} are determined as follows.

$$I_{D_{1rms}} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_{D_1}^2 dt} = \frac{(1+\alpha)i_o}{\sqrt{1-\alpha}} \tag{5.36}$$

$$I_{D_1} = \frac{1}{T_s}\int_0^{T_s} i_{D_1} dt = (1+\alpha)i_o \tag{5.37}$$

By using Equation (5.35), the rms current $I_{D_{2rms}}$ and average current I_{D_2} are derived as follows respectively.

$$I_{D_{2rms}} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_{D_2}^2 dt} = i_o\sqrt{(1-\alpha)} \tag{5.38}$$

$$I_{D_2} = \frac{1}{T_s}\int_0^{T_s} i_{D_2} dt = (1-\alpha)i_o \tag{5.39}$$

5.7 Power Losses and Efficiency

Conduction losses are analyzed by the resistances of the semiconductor devices and the inductors. By using Equation (5.33), the power loss ($P_{r_{DS}}$) due to the ON-state switching resistance $r_{DS(on)}$ is calculated as follows.

$$P_{r_{DS}} = \frac{\alpha(1+\alpha)^2 i_o^2 r_{DS(on)}}{(1-\alpha)^2} \tag{5.40}$$

The diode conduction resistance of diodes D_1 and D_2 are denoted by r_D. By using Equations (5.36) and (5.38), the total conduction loss P_{r_D} of the diodes is determined as follows.

$$P_{r_D} = r_D(I_{D_{1rms}}^2 + I_{D_{2rms}}^2) = 2\frac{(1+\alpha^2)i_o^2}{1-\alpha} r_D \tag{5.41}$$

By using Equations (5.37) and (5.39), the power loss ($P_{v_{fd}}$) due to diode forward bias voltage v_{fd} is derived as

$$P_{v_{fd}} = v_D(I_{D_1} + I_{D_2}) = 2v_{fd}i_o \tag{5.42}$$

The inductor current i_L through L-winding is expressed as $i_L = i_{in} = \frac{(1+\alpha)i_o}{(1-\alpha)}$. The inductor current i_{L_f} through L_f-winding is approximated as $i_{L_f} = i_o$. Due to the inductive parasitics ($r_L = r_{L_f}$), the total power loss (P_{r_L}) due to the inductors are as follows.

$$P_{r_L} = r_L \frac{2i_o^2(1+\alpha^2)}{(1-\alpha)^2} \tag{5.43}$$

By using Equations (5.40) to (5.43), the total loss (P_{Loss}) is determined as follows.

$$P_{Loss} = P_{r_{DS}} + P_{r_D} + P_{v_{fd}} + P_{r_L} \tag{5.44}$$

The output power is denoted by P_O. From Equation (5.44), the efficiency η is determined as

$$\eta = \frac{P_O}{P_O + P_{Loss}} = \frac{1}{1 + \frac{2r_{DS(on)}\alpha(1+\alpha)^2}{(1-\alpha)^2 R} + \frac{2(1+\alpha^2)r_D}{(1-\alpha)R} + \frac{2v_{fd}}{V_O} + \frac{2(1+\alpha^2)r_L}{(1-\alpha)^2 R}} \tag{5.45}$$

The simulation of efficiency curve of HSUBoC with improved ripple against duty ratio change is shown in Figure 5.7.

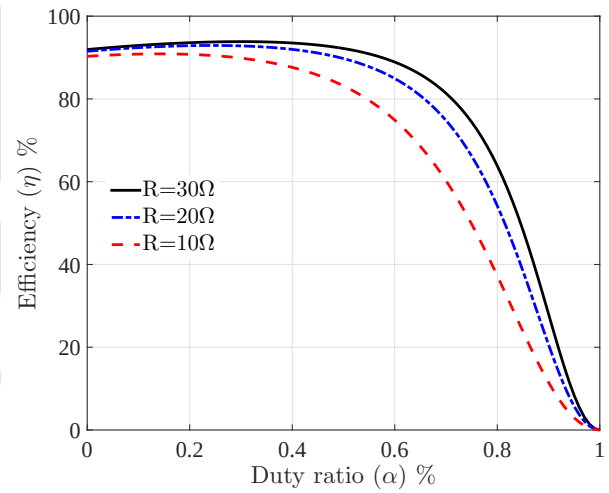


Figure 5.7: Simulation result of efficiency due to variation of α

5.8 Small-signal Modelling

In this section, following the average state-space equations and steady-state analysis, transfer function is determined to enable the closed-loop control systems.

5.8.1 Average state-space equation

The general average state-space equations are written as follows.

$$\dot{\mathbf{x}}(t) = \mathbf{A_{av}}\mathbf{x}(t) + \mathbf{B_{av}}v_{in}(t) \tag{5.46}$$

$$\mathbf{y}(t) = \mathbf{Z_{av}}\mathbf{x}(t) \tag{5.47}$$

The average state matrices of the Equations (5.46) and (5.47) are as follows.

$$\begin{aligned}\mathbf{A_{av}} &= (\mathbf{A_1} - \mathbf{A_2})\alpha + \mathbf{A_2} \\ &= \begin{bmatrix} 0 & \dfrac{(\alpha-1)L_f - M(\alpha+1)}{LL_f - M^2} & 0 & \dfrac{M}{LL_f - M^2} \\ \dfrac{1-\alpha}{2C} & 0 & \dfrac{-(1+\alpha)}{2C} & 0 \\ 0 & \dfrac{(1-\alpha)M + (1+\alpha)L}{LL_f - M^2} & 0 & \dfrac{-L_f}{LL_f - M^2} \\ 0 & 0 & \dfrac{1}{C_f} & \dfrac{-1}{RC_f} \end{bmatrix}\end{aligned} \tag{5.48}$$

$$\mathbf{B_{av}} = (\mathbf{B_1} - \mathbf{B_2})\alpha + \mathbf{B_2} = \begin{bmatrix} \dfrac{L_f}{LL_f - M^2} & 0 & \dfrac{-M}{LL_f - M^2} & 0 \end{bmatrix}^T \tag{5.49}$$

$$\mathbf{Z_{av}} = (\mathbf{Z_1} - \mathbf{Z_2})\alpha + \mathbf{Z_2} = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \tag{5.50}$$

Now, considering a perturbation $\hat{v}_{in}(t)$ in the steady state input voltage V_{in}, the input voltage becomes $v_{in}(t) = V_{in} + \hat{v}_{in}(t)$. This perturbation in v_{in} affects the steady-state values of inductor currents and capacitor voltages. Therefore, the instantaneous state vector $\mathbf{x}(t)$ and output $\mathbf{v_o}(t)$ become $\mathbf{x}(t) = \mathbf{X} + \hat{\mathbf{x}}(t)$ and $\mathbf{v_o}(t) = \mathbf{V_o} + \hat{\mathbf{v}}_o(t)$. The state-space equation with the perturbation can be written as follows.

$$\dot{\mathbf{X}} + \dot{\hat{\mathbf{x}}}(t) = \mathbf{A_{av}}(\mathbf{X} + \hat{\mathbf{x}}(t)) + \mathbf{B_{av}}(V_{in} + \hat{v}_{in}(t)) \tag{5.51}$$

$$\mathbf{V_o} + \hat{\mathbf{v}}_o(t) = \mathbf{Z_{av}}(\mathbf{X} + \hat{\mathbf{x}}(t)) \tag{5.52}$$

5.8.2 Steady-state analysis

At ideal case, the steady-state values of the state variables are determined as follows.

$$\mathbf{X} = [I_{L_i}\ V_C\ I_L\ V_{C_f}]^T = -\mathbf{A_{av}}^{-1}\mathbf{B_{av}}V_{in} = \left[\frac{(1+\alpha)^2 V_{in}}{(1-\alpha)^2 R}\ \frac{V_{in}}{1-\alpha}\ \frac{(1+\alpha)V_{in}}{(1-\alpha)R}\ \frac{(1+\alpha)V_{in}}{1-\alpha}\right]^T \tag{5.53}$$

5.8.3 Open-loop transfer function

By using the Equations (5.46) to (5.47), the voltage to duty ratio transfer function $G_{v\alpha}(s)$ is derived as follows.

$$G_{v\alpha}(s) = \frac{\hat{v}_o(s)}{\hat{\alpha}(s)} = \mathbf{Z_{av}}(s\mathbf{I} - \mathbf{A_{av}})^{-1}[(\mathbf{A_1} - \mathbf{A_2})\mathbf{X} + (\mathbf{B_1} - \mathbf{B_2})V_{in}] + (\mathbf{Z_1} - \mathbf{Z_2})\mathbf{X} \tag{5.54}$$

By using the Equation (5.54), the following voltage to duty ratio transfer function is derived.

$$G_{v\alpha}(s) = \frac{a_2 s^2 + a_1 s + a_0}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \tag{5.55}$$

The coefficients of $G_{v\alpha}(s)$ are provided in terms of RLC-parameters in Table 5.2. By using the parameter value provided in Table 5.3, the $G_{v\alpha}$ is determined as follows.

$$G_{v\alpha}(s) = \frac{1.6033 \times 10^8 s^2 - 1.4888 \times 10^1 1 s + 5.6684 \times 10^1 5}{s^4 + 101 s^3 + 7.447 \times 10^7 s^2 + 5.255 \times 10^9 s + 1.389e14} \tag{5.56}$$

The gain and phase margin of the uncompensated plant $G_{v\alpha}(s)$ are -29.7 dB and 4.92°. Therefore, the closed-loop systems is unstable and a suitable controller will be required.

5.8.4 Control scheme

A PI controller is designed to check the closed loop performance [116]. The expression of the PI controller is as follows.

$$G_c(s) = K_p + \frac{K_i}{s} \tag{5.57}$$

where K_p and K_i are the proportional and integral constants. The parameters of the controller are $K_p = 1.5559 \times 10^{-5}$ and $K_i = 0.6617$.

Table 5.2: The coefficients of transfer function $G_{v\alpha}(s)$

Coefficient	Expression
a_2	$\frac{(L-M)V_{in}}{C_f(LL_f-M^2)(1-\alpha)}$
a_1	$\frac{-((L-M)\alpha+L+M)(1+\alpha)V_{in}}{C_f(LL_f-M^2)(\alpha-1)^2RC}$
a_0	$\frac{-V_{in}((\alpha-1)L^2+((1-\alpha)M-L_f(\alpha+1))L+M(2M+(\alpha-1)L_f))}{2C_fC(LL_f-M^2)^2}$
b_4	1
b_3	$\frac{1}{C_fR}$
b_2	$\frac{(\alpha^2(L-M)+L+M)C_f+L_fC}{(LL_f-M^2)CC_f}$
b_1	$\frac{(L-M)\alpha^2+L+M}{RC_f(LL_f-M^2)C}$
b_0	$\frac{((1-\alpha)M^2+(L-L_f)(\alpha+1)M+LL_f(\alpha-1))(\alpha-1)}{2C_fC(LL_f-M^2)^2}$

Block diagram representation of the closed-loop control system is shown in Figure 5.8. The transfer function of compensated system is calculated as follows.

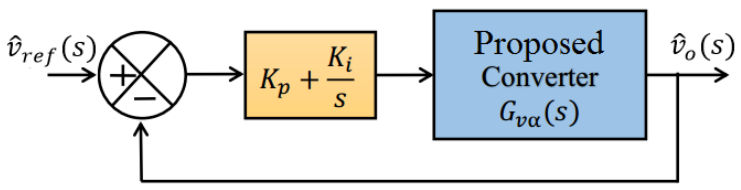


Figure 5.8: Block diagram representation of the closed-loop control systems

$$G_{comp}(s) = G_c(s)G(s) = \frac{2495s^3 + 1.038 \times 10^8 s^2 - 1.032 \times 10^1 s + 3.751 \times 10^{15}}{s^5 + 101s^4 + 7.447 \times 10^7 s^3 + 5.255 \times 10^9 s^2 + 1.389 \times 10^{14} s} \quad (5.58)$$

The phase and gain margin of the compensated system ($G_{comp}(s)$) are 89.9° and 8.71 dB. As, both the gain and phase margins of the compensated system are positive, the closed-loop system will be stable. The closed loop zeros are $z_1 = z_2 = 0.0464 \times 10^4 \pm i0.5928 \times 10^4$, $z_3 = -4.2528 \times 10^4$. The closed loop poles are $s_1 = -27$, $s_2 = s_3 = -0.0143 \times 10^3 \pm i8.5180 \times 10^3$,

$s_4 = s_5 = -0.0227 \times 10^3 \pm i1.3829 \times 10^3$. It is also seen that all the closed loop poles are in left half of the s-plane. Therefore, this also validates the closed-loop system stability.

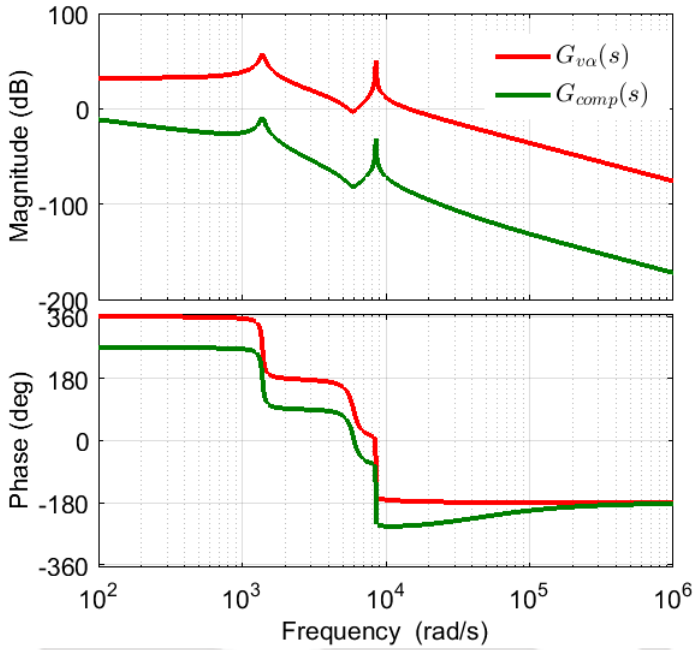


Figure 5.9: Bode plot of uncompensated and compensated systems

5.9 Simulation Results

The simulation is carried out in the MATLAB-Simscape platform by using the parameters given in Table 5.3.

Table 5.3: Parameter values of HSUBoC considered for CCM operation

Parameters	**Values**
Power (P_O)	18.14 W
Input Voltage v_{in}	10 V
Switching Frequency f_s	50 kHz
Inductance L	180 μH
Inductance L_f	180 μH
Coupling factor k	0.5
Capacitor $C_1 = C_2 = C$	220 μF
Output Capacitor C_f	330 μF
Load Resistance R	30 Ω
Diode forward voltage (v_D)	0.39 V
MOSFET drain to source on-resistance ($r_{DS_{on}}$)	0.075 Ω
Duty Ratio α	0.40

At first, steady-state results i.e. open-loop simulation results will be discussed and thereafter, to investigate the closed-performances, closed-loop simulation will be carried out.

5.9.1 Open-loop performance

Figure 5.10a shows the ripple in inductor current for $\alpha = 0.40$. When the coupling factor $k = 0$, i.e. uncoupled inductors, the ripple currents through the inductors L and L_f are $\Delta i_L = \Delta i_{L_f} = 0.45$ A as shown in Figure 5.10a. After replacing these two single inductors by a DWCI with coupling factor $k = 0.5$, the ripple currents through $L-winding$ and $L_f-winding$ become $\Delta i_L = \Delta i_{L_f} = 0.3$ A as shown in Figure 5.10a. The inductance values of the single inductors L and L_f are equal to $L-winding$ and $L_f-winding$ of DWCI respectively. In Figure 5.10b, the output voltage ripple is shown. With the single inductors, the output voltage ripple is Δv_o =97.3 mV. By using the DWCI the output voltage ripple Δv_o is reduced into 64.9 mV as shown in Figure 5.10b. The steady state value of the output voltage $v_o = 22.415$ V is not affected by the coupling factor.

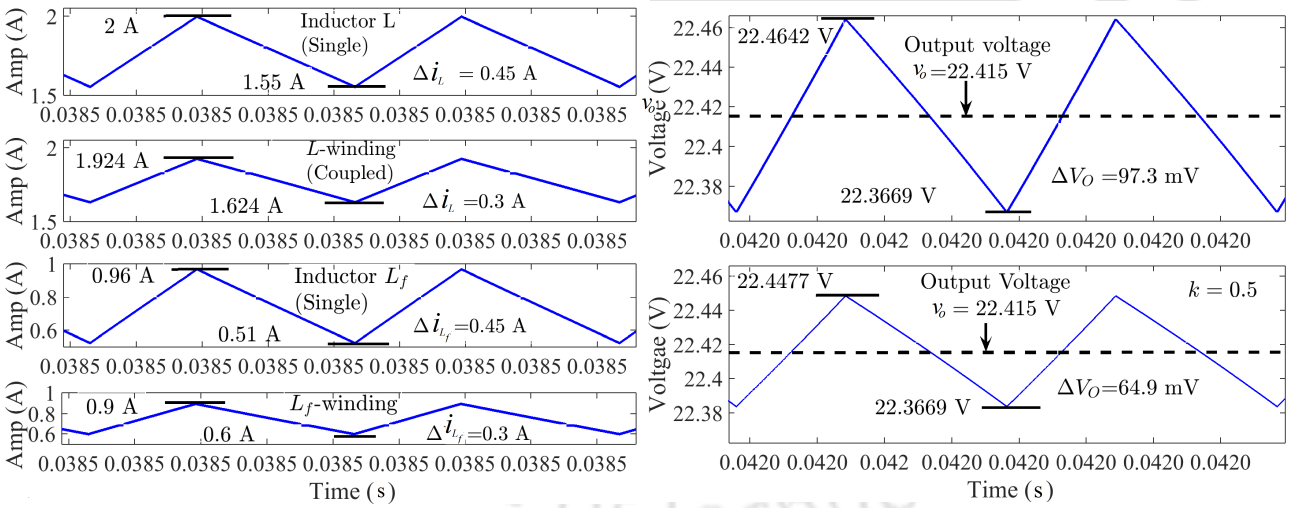


Figure 5.10: Ripples in (a) Inductor currents, and (b) Output voltage for $\alpha = 0.40$

5.9.2 Closed-loop performance

Figure 5.11a shows the simulation results of the closed-loop systems due to reference voltage v_{ref} change. The v_{ref} is set to be 26 V, 18 V and 22 V. From the results, it can be seen that the output voltage (v_o) and inductor currents (i_L and i_{L_f}) follow the reference. To investigate

the sensitivity to load parameter variation, 50% load change is carried out as shown in Figure 5.11b. At 0.2 s, the load is changed from 30 Ω to 15 Ω. Therefore, the output load current increases from 0.733 A to 1.46 A. At 0.4 s, the load is again 30 Ω, therefore the load current decreases from 1.46 A to 0.733 A.

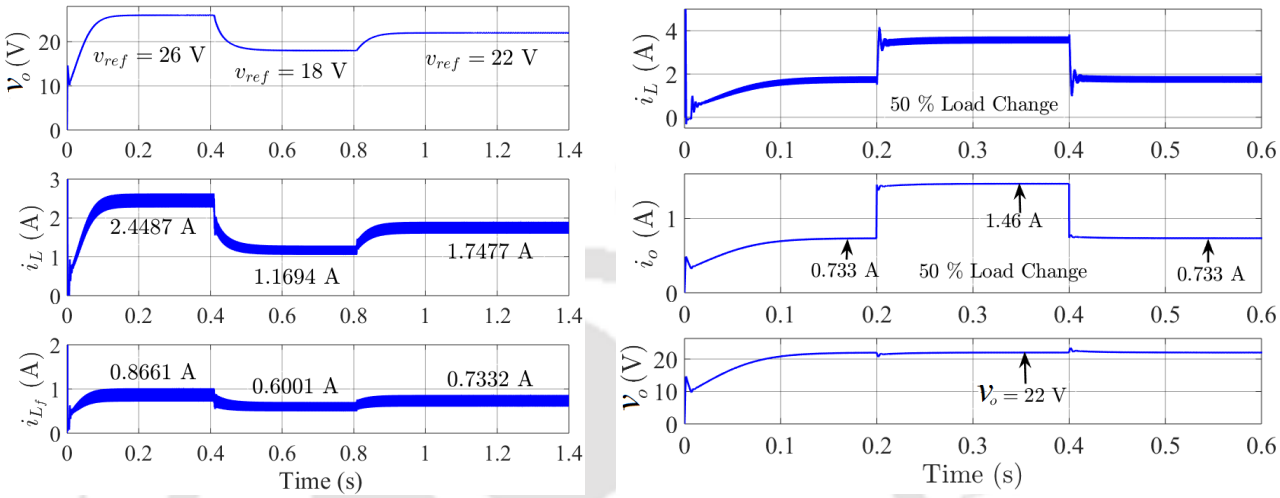


Figure 5.11: Simulation results for (a) Reference change, and (b) 50 % load change

5.10 Experimental Setup and Results

Only open-loop steady-state experiment is done. The proposed HSUBoC is tested in two stages. At first, the converter is tested with two single inductors and later those two single inductors have been replaced by the directly-coupled DWCI. The experimental set-up with two single indcutors is shown in Figure 5.12.

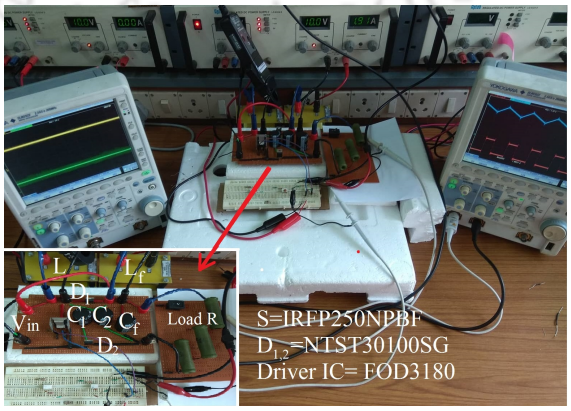
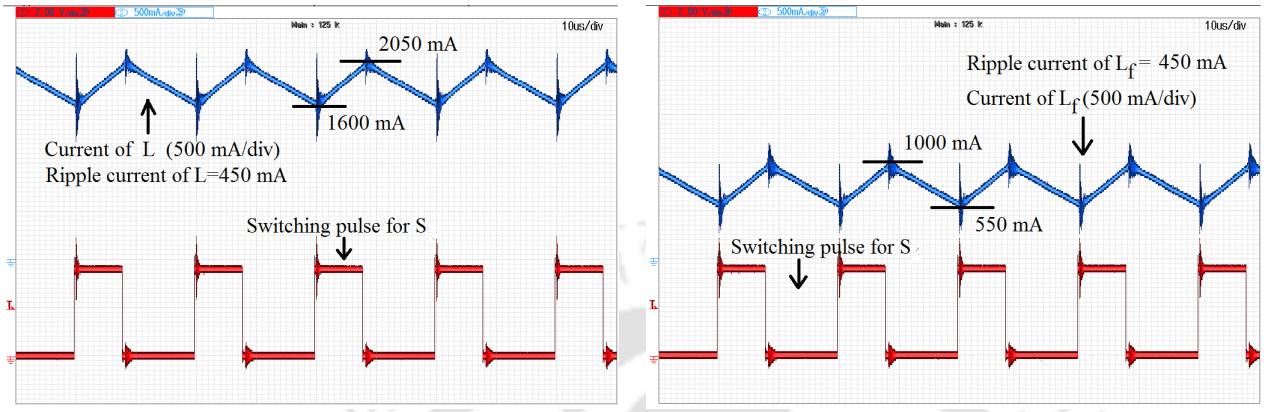


Figure 5.12: Experimental setup of the converter (HSUBoC) with single inductors

For the real-time validation, the proposed HSUBoC with improved-ripple is designed with the parameters given in Table 5.3. The switch S is implemented by MOSFET IRFP250NPBF. The diodes D_1 and D_2 are implemented by NTST30100SG.



(a) (b)

Figure 5.13: Experimental result of inductor currents for $\alpha = 0.40$ and $k = 0$ (a) i_L, and (b) i_{L_f}

The ripple current Δi_L in inductor L is 0.45 A for $\alpha = 0.40$ as shown in Figure 5.13a and the ripple current Δi_{L_f} in inductor L_f is 0.45 A for $\alpha = 0.40$ as shown in Figure 5.13b.

Subsequently, the two single inductors are replaced by a DWCI as shown in Figure 5.14. The experimental schematic diagram of the proposed HSUBoC is shown in Figure 5.15.

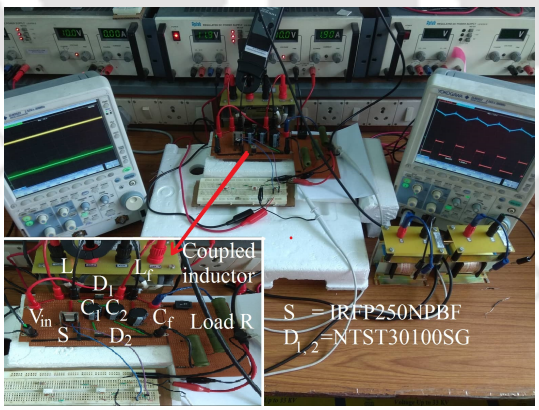


Figure 5.14: Experimental setup of the converter (HSUBoC) with DWCI

The DWCI is designed by using U-type core [125]. The ripple current in $L-winding$ of the coupled inductor is $\Delta i_L = 0.3$ A as shown in Figure 5.16a. The ripple current in $L_f-winding$ of the coupled inductor is $\Delta i_{L_f} = 0.3$ A as shown in Figure 5.16b. Thus, these experimental results of ripple improvement validate the Equations (5.22) and (5.25). With

more tight coupling factor, the ripple can be reduced more.

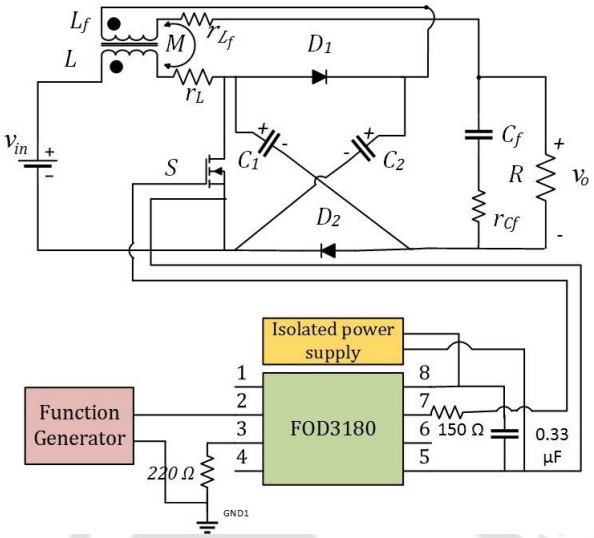
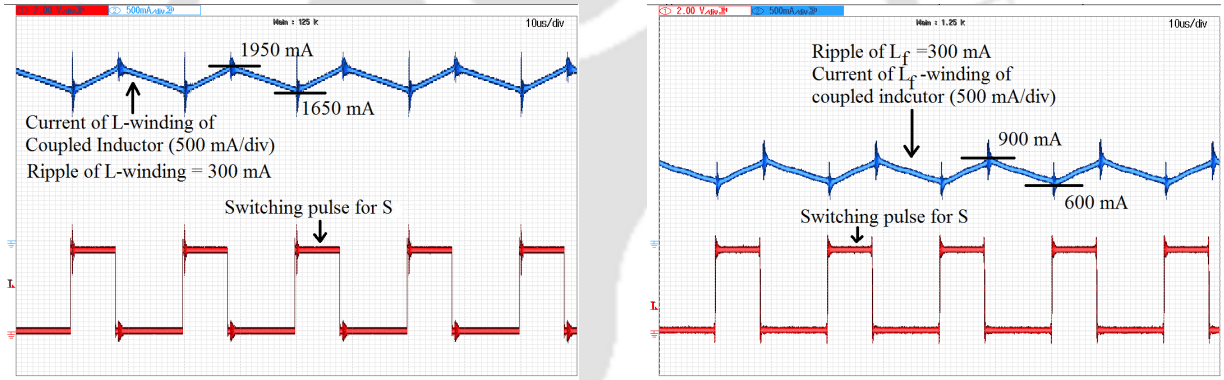
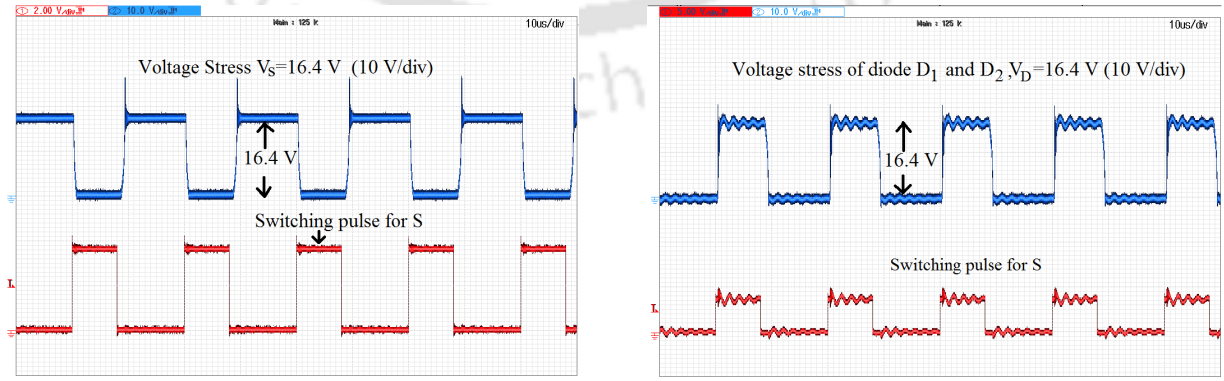


Figure 5.15: Schematic diagram of the experimental setup of the converter (HSUBoC) with DWCI



(a) (b)

Figure 5.16: Experimental result of inductor currents (a)i_L, and (b)i_{L_f} for $\alpha = 0.40$ and $k = 0.5$



(a) (b)

Figure 5.17: Experimental result of voltage stresses (a) v_S, and (b) v_D for $\alpha = 0.40$

The diode and switch voltage stresses are $v_S = 16.4$ V and $v_D = 16.4$ V, respectively shown in Figure 5.17a and in Figure 5.17b. The output voltage is shown in Figure 5.18. The steady-state value of the output voltage is 22.7 V and the output ripple voltage is $\Delta v_o = 70$ mV. The experimental waveform of efficiency for duty ratio change is shown in Figure 5.19. Maximum 94.15% efficiency is achieved at $\alpha = 0.30$.

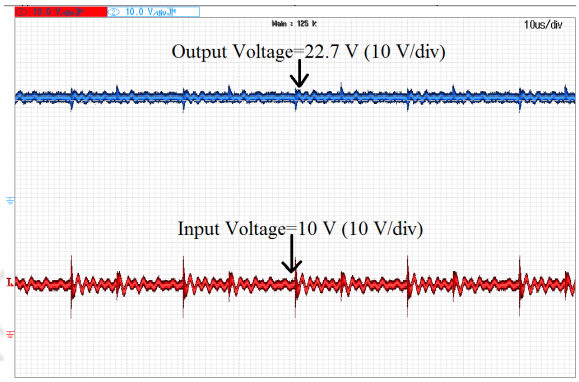


Figure 5.18: Experimental result of output voltage v_o for $\alpha = 0.40$

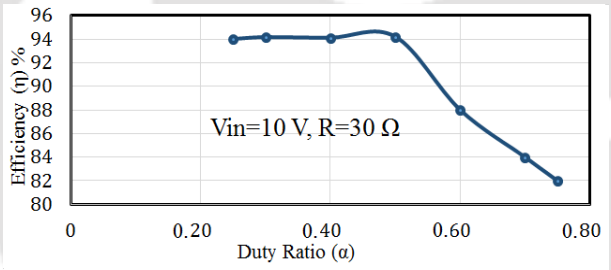


Figure 5.19: Plot of efficiency versus duty ratio (α)

5.11 Summary

A HSUBoC with DWCI having a larger step-up conversion ratio and improved-ripple is presented in this chapter. The role of the DWCI is to reduce ripples in inductor current, input current and output voltage. It also reduces the size of magnetic cores as both the windings of the coupled inductor share cores. Thus, it reduces the cost and bulk of the system. The mutual inductance does not affect the steady-state value of the output voltage. The experimental results are provided to verify the physical realizability of the proposed converter. An experimental efficiency of 94.58% has been achieved. Followed by small-signal modelling analysis, a closed-loop control is enabled and simulated closed-loop results are provided.

6

High Step-up Interleaved Boost Converter

The chapter presents a two-phase interleaved boost converter (IBoC) providing higher step-up conversion ratio compared to CIBoC. The circuit consists of a cross-connected diode-capacitor cell which provides the extra boost up. The two identical capacitors of the cell are charged in parallel and discharged in series providing high voltage gain at considerably low duty ratio. Switching operations, ripple and average currents through inductors are analysed in continuous conduction mode (CCM). Ripple in input current is also improved. The voltage stress across the semiconductor devices is less in the proposed converter. Also, boundary load condition is derived. Small-signal modelling is carried out and a control circuit is enabled in the voltage mode control framework. Power losses are analysed and 96.53 % efficiency is achieved. Finally, the proposed converter is designed and implemented, and experimental results are provided.

6.1 Introduction

In the previous chapter, the voltage conversion ratio of the conventional boost converter (CBoC) is enhanced utilizing a diode-capacitor cell to overcome the problem of a wide duty ratio when a very low-input to high-output voltage conversion is required. The same technique can be applied for the conventional interleaved boost converter (CIBoC) as the step-up voltage conversion ratio is the same as CBoC. Therefore, in this chapter, the diode-capacitor cell is used to modify the conversion ratio of CIBoC. The proposed high step-up interleaved boost converter (HSUIBoC) achieves a modified voltage gain, less voltage stresses in the active elements, and less ripple in input and inductor currents compared to CIBoC. From the efficiency analysis it is also seen that the efficiency of the proposed HSUIBoC is higher as well.

This chapter is organized as follows. Section 6.2 discusses the operation principle of the proposed HSUIBoC in the continuous conduction mode (CCM) framework. In Section 6.3, the voltage conversion ratio is determined. The inductor average and ripple currents are analysed in Section 6.4. Section 6.5 explains the boundary load condition between CCM and DCM. The analysis of ripple in input current is provided in Section 6.6. In Section 6.7, the design of identical capacitors is explained. The design of the output filter capacitor is provided in Section 6.8. Voltage and current stress are explained in Section 6.9. Section 6.10 discusses about the selection of parameters value. The small-signal modelling and the closed-loop control are provided in Section 6.11 and 6.12 respectively. The simulation result is provided in Section 6.13. The experimental results on the performance of the proposed converter are discussed in Section 6.14. Section 6.15 provides brief summary on the chapter.

6.2 Operation Principle

Figure 6.1 shows the circuit configuration of the proposed two-phase high step-up interleaved boost converter (HSUIBoC). Followed by input voltage v_{in}, two identical inductors L_1 and L_2 with parasitic r_L are connected to the switches S_1 and S_2 respectively. Two identical capacitors C_1 and C_2 are connected in cross through two parallel diodes D_1 and D_2 with S_1. When S_1 does not conduct, the two capacitors are charged in parallel by the L_1. When the S_1 conducts, the capacitors are connected in series through the S_1 and they provide the stored energy to the output part. The switch S_2 is followed by a diode D_3 and connected to output side inductor

L_f. The L_f is used to oppose the sudden change in output current when those two identical capacitors switch from a parallel connection to a series configuration. The inductor L_f is followed by an output capacitor C_f with parasitic r_{C_f}. R is the load resistance at output v_o. Parasitics r_L and r_{C_f} are negligible as $r_L, r_{C_f} << R$.

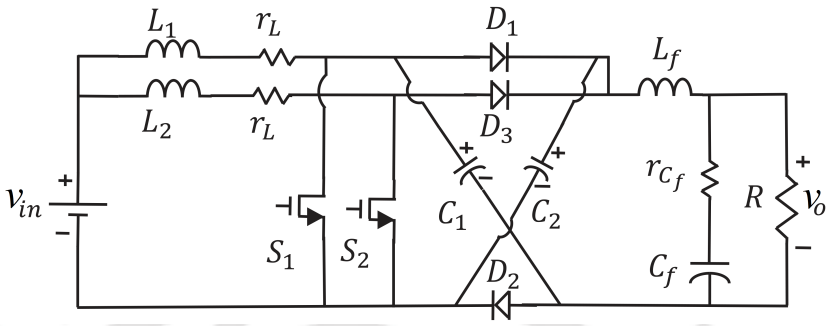


Figure 6.1: Proposed high step-up interleaved boost converter (HSUIBoC)

6.2.1 Switching operations

The proposed HSUIBoC operates in four basic switching modes depending upon the value of the duty ratio α. When the duty ratio α is in the interval $\alpha \in (0, 0.5]$, both the switches are OFF for two specific durations of the time period T_s as shown in Figure 6.2a.

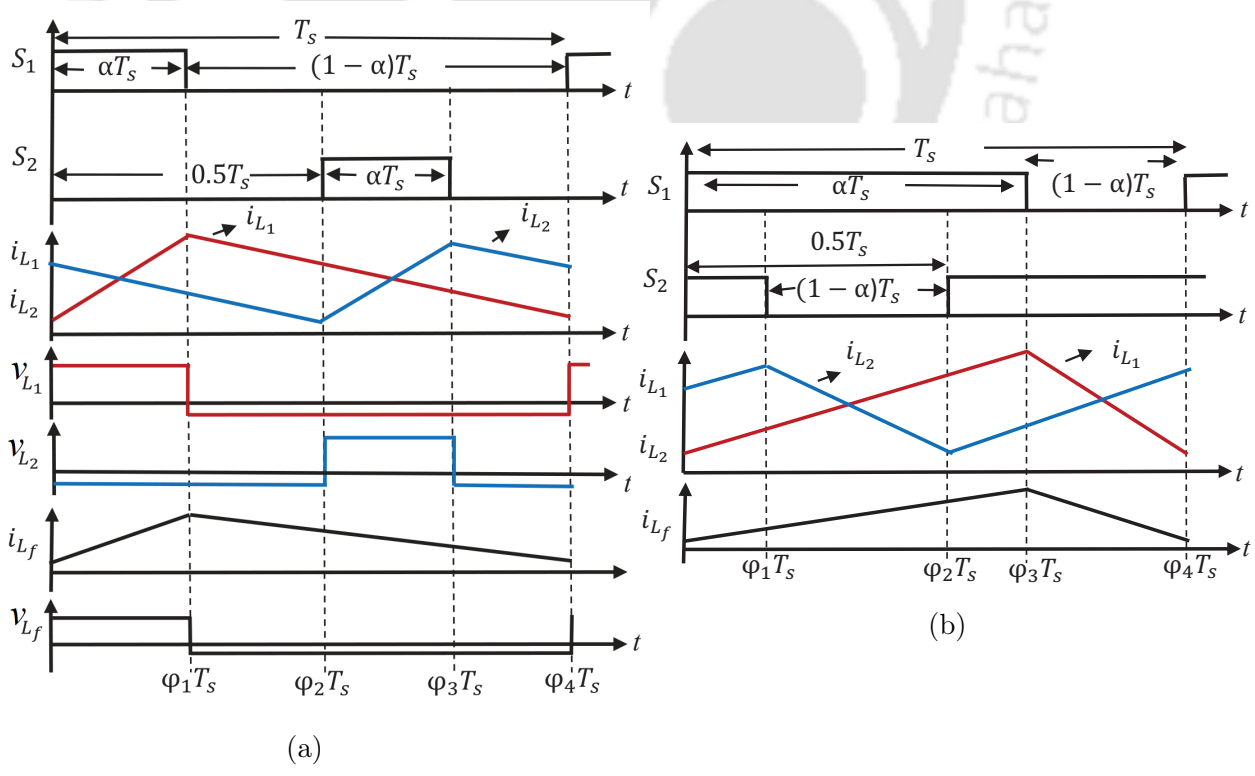


Figure 6.2: Idealized waveform of the proposed HSUIBoC when (a) $\alpha \in (0, 0.5]$, and (b) $\alpha \in (0.5, 1)$

During these intervals, inductor currents i_{L_1} and i_{L_2} through L_1 and L_2 respectively decrease. In other condition, while $\alpha \in (0.5, 1)$, both the switches are ON for two particular durations as shown in Figure 6.2b. During these periods, i_{L_1} and i_{L_2} increase. In the both idealized waveforms, it is shown that the inductor currents i_{L_1} and i_{L_2} are in 180° phase shift. The current i_{L_f} is through the inductor L_f. All the four basic switching modes of operation are described by assuming $C_1 = C_2 = C$.

6.2.1.1 Mode-I

During this mode of operation, switch S_1 conducts and S_2 does not conduct as shown in Figure 6.3. This causes D_1 and D_2 to be in reverse bias and D_3 in forward bias. Therefore, two identical capacitors, C, are in series through S_1 and the resultant capacitive voltage becomes $v_C + v_C = 2v_C$. The switching operation of Mode-I occurs during $0 < t \leq \varphi_1 T_s$ for the case of $\alpha \in (0, 0.5]$ as shown in Figure 6.2a and the same switching operation occurs for the case of $\alpha \in (0.5, 1)$ during $\varphi_1 T_s < t \leq \varphi_2 T_s$ as shown in Figure 6.2b.

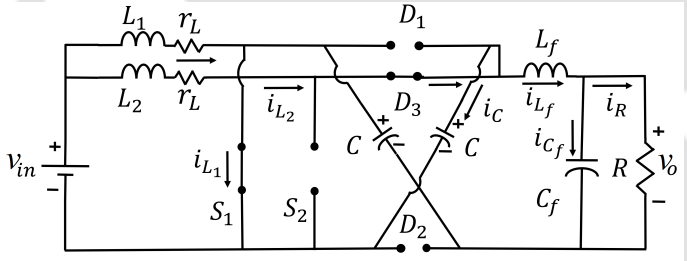


Figure 6.3: Mode-I operation while $S_1 = ON$ and $S_2 = OFF$

The equations of voltages v_{L_1}, v_{L_2} and v_{L_f} across L_1, L_2 and L_f are expressed as

$$v_{L_1} = L_1 \frac{di_{L_1}(t)}{dt} = v_{in} - r_L i_{L_1} \tag{6.1}$$

$$v_{L_2} = L_2 \frac{di_{L_2}(t)}{dt} = v_{in} - v_C - r_L i_{L_2} \tag{6.2}$$

$$v_{L_f} = L_f \frac{di_{L_f}(t)}{dt} = 2v_C - v_o \tag{6.3}$$

The current through the identical capacitors, $i_C(t)$, and load current, $i_R(t)$, are described by

$$i_C(t) = i_{L_2}(t) - i_{L_f}(t) \tag{6.4}$$

$$i_R(t) = i_{L_f}(t) - i_{C_f}(t) \tag{6.5}$$

where $i_{C_f}(t)$ is the current flowing through the output capacitor C_f. The voltage, v_{C_f}, across C_f is

$$v_{C_f} = v_o = Ri_R(t) \tag{6.6}$$

The voltage, v_{S_2}, across the switch S_2 is given by

$$v_{S_2} = v_{in} - v_{L_2} = v_C \tag{6.7}$$

The voltages v_{D_1} and v_{D_2} across D_1 and D_2 respectively are as follows.

$$v_{D_1} = v_{D_2} = v_C \tag{6.8}$$

The state vectors are defined by $\mathbf{x}(t) = [i_{L_1}\ i_{L_2}\ v_C\ i_{L_f}\ v_{C_f}]^T$ and the output vector $\mathbf{v_o}(t)$. The state space equation of this mode of operation is expressed

$$\begin{aligned}\dot{\mathbf{x}}(t) &= \mathbf{A_1}\mathbf{x}(t) + \mathbf{B_1}v_{in}(t) \\ &= \begin{bmatrix} \frac{-r_L}{L_1} & 0 & 0 & 0 & 0 \\ 0 & \frac{-r_L}{L_2} & \frac{-1}{L_2} & 0 & 0 \\ 0 & \frac{1}{C} & 0 & \frac{-1}{C} & 0 \\ 0 & 0 & \frac{2}{L_f} & 0 & \frac{-1}{L_f} \\ 0 & 0 & 0 & \frac{1}{C_f} & \frac{-1}{RC_f} \end{bmatrix} \mathbf{x}(t) + \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_{in}(t)\end{aligned} \tag{6.9}$$

$$\mathbf{v_o}(t) = \mathbf{Z_1}\mathbf{x}(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \end{bmatrix} \mathbf{x}(t) \tag{6.10}$$

6.2.1.2 Mode-II

In this mode both the switches are OFF and all the three diodes are in forward bias as shown in Figure 6.4. Therefore, the two identical capacitors C are parallel to each other. This switching operation takes place during $\varphi_1 T_s < t \leq \varphi_2 T_s$ and $\varphi_3 T_s < t \leq \varphi_4 T_s$ only if $\alpha \in (0, 0.5]$ as shown in Figure 6.2a. The inductive voltage equation of L_2 is as Equation (6.2).

The inductive voltage equations of L_1 and L_f are as follows.

$$v_{L_1} = v_{in} - v_C - r_L i_{L1} \tag{6.11}$$

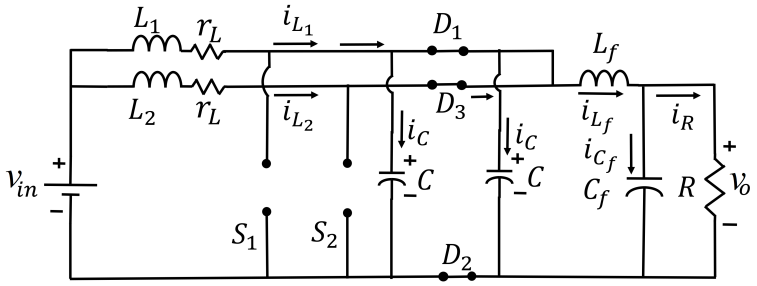


Figure 6.4: Mode-II operation while $S_1 = OFF$ and $S_2 = OFF$

$$v_{L_f} = v_C - v_o \tag{6.12}$$

The output load current and voltage equations are the same as Equations (6.5) and (6.6) respectively. The $i_C(t)$ can be defined as follows.

$$2i_C(t) = i_{L_1}(t) + i_{L_2}(t) - i_{L_f}(t) \tag{6.13}$$

The voltage, v_{S_1}, across the switch S_1 is as follows.

$$v_{S_1} = v_{in} - v_{L_1} = v_C \tag{6.14}$$

The voltage v_{S_2} is the same as given in Equation (6.7). The state space equation of this mode of operation is expressed as follows

$$\begin{aligned}\dot{\mathbf{x}}(t) &= \mathbf{A_2}\mathbf{x}(t) + \mathbf{B_2}v_{in}(t) \\ &= \begin{bmatrix} \frac{-r_L}{L_1} & 0 & \frac{-1}{L_1} & 0 & 0 \\ 0 & \frac{-r_L}{L_2} & \frac{-1}{L_2} & 0 & 0 \\ \frac{1}{2C} & \frac{1}{2C} & 0 & \frac{-1}{2C} & 0 \\ 0 & 0 & \frac{1}{L_f} & 0 & \frac{-1}{L_f} \\ 0 & 0 & 0 & \frac{1}{C_f} & \frac{-1}{RC_f} \end{bmatrix} \mathbf{x}(t) + \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_{in}(t)\end{aligned} \tag{6.15}$$

$$\mathbf{v_o}(t) = \mathbf{Z_2}\mathbf{x}(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \end{bmatrix} \mathbf{x}(t) \tag{6.16}$$

6.2.1.3 Mode-III

During this switching mode, the switch S_1 does not conduct and the switch S_2 conducts. Therefore, the diodes D_1 and D_2 are in forward bias but D_3 is in reverse bias as shown in Figure 6.5. Thus, the two identical capacitors C are parallel to each other. When $\alpha \in (0, 0.5]$, the Mode-III takes place during $\varphi_2 T_s < t \leq \varphi_3 T_s$ as shown in Figure 6.2a and when $\alpha \in (0.5, 1)$, the same mode occurs during $\varphi_3 T_s < t \leq \varphi_4 T_s$ as shown in Figure 6.2b.

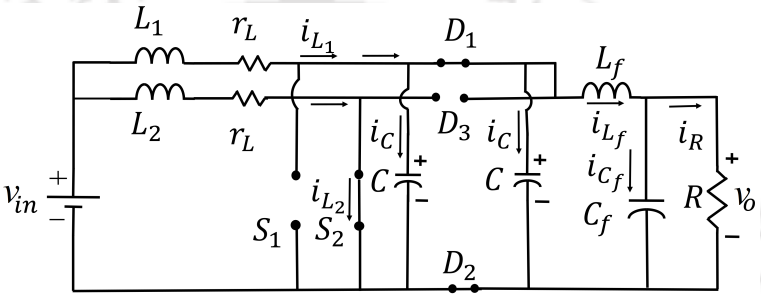


Figure 6.5: $Mode - III$ operation while $S_1 = OFF$ and $S_2 = ON$

The voltage across L_1 and L_f are as in Equations (6.11) and (6.12) respectively. The v_{L_2} is

$$v_{L_2} = v_{in} - r_L i_{L_2} \tag{6.17}$$

The output load current and voltage are as provided in Equations (6.5) and (6.6) respectively. The $i_C(t)$ is expressed by

$$2i_C(t) = i_{L_1}(t) - i_{L_f}(t) \tag{6.18}$$

The voltage v_{S_1} is the same as given in Equation (6.14) and the voltage, v_{D_3}, across the D_3 is as follows.

$$v_{D_3} = v_C \tag{6.19}$$

The state space equation of this mode of operation is given by

$$\dot{\mathbf{x}}(t) = \mathbf{A_3}\mathbf{x}(t) + \mathbf{B_3}v_{in}(t)$$

$$= \begin{bmatrix} \frac{-r_L}{L_1} & 0 & \frac{-1}{L_1} & 0 & 0 \\ 0 & \frac{-r_L}{L_2} & 0 & 0 & 0 \\ \frac{1}{2C} & 0 & 0 & \frac{-1}{2C} & 0 \\ 0 & 0 & \frac{1}{L_f} & 0 & \frac{-1}{L_f} \\ 0 & 0 & 0 & \frac{1}{C_f} & \frac{-1}{RC_f} \end{bmatrix} \mathbf{x}(t) + \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_{in}(t) \tag{6.20}$$

$$\mathbf{v_o}(t) = \mathbf{Z_3}\mathbf{x}(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \end{bmatrix} \mathbf{x}(t) \tag{6.21}$$

6.2.1.4 Mode-IV

In this mode, both the switches conduct and all the three diodes are in reverse bias as shown in Figure 6.6. The two identical capacitors C are in series through switch S_1. This mode of operation occurs during $0 < t \leq \varphi_1 T_s$ and $\varphi_2 T_s < t \leq \varphi_3 T_s$ only if $\alpha \in (0.5, 1)$ as shown in Figure 6.2b.

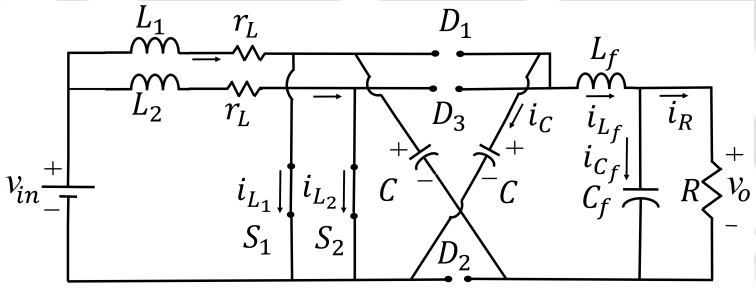


Figure 6.6: Mode-IV operation while $S_1 = ON$ and $S_2 = ON$

The voltages across L_1, L_2 and L_f are as derived in Equations (6.1), (6.17) and (6.3) respectively. The capacitor current $i_C(t)$ is given by

$$i_C(t) = -i_{L_f}(t) \tag{6.22}$$

The output load current and voltage are as in Equations (6.5) and (6.6) respectively. The state

space equation of this mode of operation is given by

$$\dot{\mathbf{x}}(t) = \mathbf{A_4}\mathbf{x}(t) + \mathbf{B_4}v_{in}(t) = \begin{bmatrix} \frac{-r_L}{L_1} & 0 & 0 & 0 & 0 \\ 0 & \frac{-r_L}{L_2} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{C} & 0 \\ 0 & 0 & \frac{2}{L_f} & 0 & \frac{-1}{L_f} \\ 0 & 0 & 0 & \frac{1}{C_f} & \frac{-1}{RC_f} \end{bmatrix} \mathbf{x}(t) + \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_{in}(t) \quad (6.23)$$

$$\mathbf{v_o}(t) = \mathbf{Z_4}\mathbf{x}(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \end{bmatrix} \mathbf{x}(t) \quad (6.24)$$

6.3 Voltage conversion ratio

The voltage conversion ratio is determined when $(0 < \alpha \leq 0.5)$. The conversion ratio is the same for the conditions $\alpha \in (0, 0.5]$ and $\alpha \in (0.5, 1)$. By using principle of inductor voltage second balance (VSB), the DC conversion ratio of the proposed converter can be derived. The VSB equation of L_1 is as follows.

$$\left(\int_0^{\varphi_1 T_s} v_{L_1} + \int_{\varphi_1 T_s}^{\varphi_2 T_s} v_{L_1} + \int_{\varphi_2 T_s}^{\varphi_3 T_s} v_{L_1} + \int_{\varphi_3 T_s}^{\varphi_4 T_s} v_{L_1} \right) dt = 0 \quad (6.25)$$

By solving Equation (6.25), it is found that $v_{in} = (1 - \alpha)v_C$. Now, the VSB equation of L_f is

$$\left(\int_0^{\varphi_1 T_s} v_{L_f} + \int_{\varphi_1 T_s}^{\varphi_2 T_s} v_{L_f} + \int_{\varphi_2 T_s}^{\varphi_3 T_s} v_{L_f} + \int_{\varphi_3 T_s}^{\varphi_4 T_s} v_{L_f} \right) dt = 0 \quad (6.26)$$

The Equation (6.26) yields to $v_o = (1 + \alpha)v_C$. Thus, from Equations (6.25) and (6.26), the voltage conversion ratio of the proposed HSUIBoC is determined as follows.

$$M = \frac{v_o}{v_{in}} = \frac{1 + \alpha}{1 - \alpha} \quad (6.27)$$

Thus, the proposed HSUIBoC has higher conversion ratio than the CIBoC $(M = 1/(1 - \alpha))$ as provided in [126]. The change of voltage gain of the proposed HSUIBoC with respect to α is

shown in Figure 6.7.

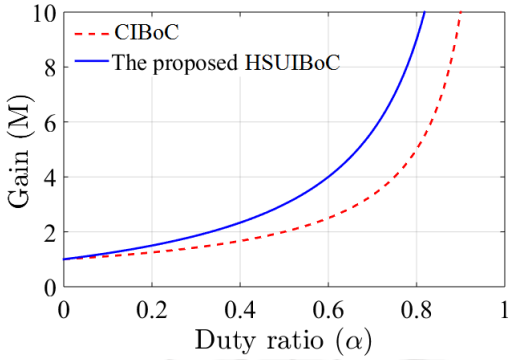


Figure 6.7: Voltage gain (M) versus duty ratio (α)

6.4 Average and Ripple Currents in Inductor

To determine inductor average and ripple current, the currents through L_1, L_2 and L_f are expressed as $\int_0^{T_s} di_{L_1}(t) = \int_0^{T_s} \frac{v_{L1}}{L_1} dt$, $\int_0^{T_s} di_{L_2}(t) = \int_0^{T_s} \frac{v_{L2}}{L_2} dt$ and $\int_0^{T_s} di_{L_f} = \int_0^{T_s} \frac{v_{L_f}}{L_f} dt$ respectively.

6.4.1 Case I, $\alpha \in (0, 0.5]$

In the interval $0 < t \leq \varphi_1 T_s$, shown in Figure 6.2a, the $i_{L_1}(\varphi_1 T_s)$, $i_{L_2}(\varphi_1 T_s)$ and $i_{L_f}(\varphi_1 T_s)$ are derived by neglecting the parasitics of inductors.

$$\int_0^{\varphi_1 T_s} di_{L_1}(t) = \frac{1}{L_1} \int_0^{\varphi_1 T_s} v_{L_1} dt$$
$$i_{L_1}(\varphi_1 T_s) = \frac{1}{L_1} v_{L_1}(\varphi_1 T_s - 0) + i_{L_1}(0) = \frac{\alpha T_s}{L_1} v_{in} + i_{L_1}(0) \tag{6.28}$$

$$\int_0^{\varphi_1 T_s} di_{L_2}(t) = \frac{1}{L_2} \int_0^{\varphi_1 T_s} v_{L_2} dt$$
$$i_{L_2}(\varphi_1 T_s) = i_{L_2}(0) + \frac{1}{L_2} v_{L_2}(\varphi_1 T_s - 0) = i_{L_2}(0) + \frac{1}{L_2}(v_{in} - v_C)\alpha T_s$$
$$= i_{L_2}(0) + \frac{1}{L_2}(v_{in} - \frac{v_{in}}{1-\alpha})\alpha T_s = i_{L_2}(0) - \frac{\alpha^2 T_s}{L_2(1-\alpha)} v_{in} \tag{6.29}$$

$$\int_0^{\varphi_1 T_s} di_{L_f}(t) = \frac{1}{L_f}\int_0^{\varphi_1 T_s} v_{L_f} dt$$
$$i_{L_f}(\varphi_1 T_s) = \frac{1}{L_f} v_{L_f}(\varphi_1 T_s - 0) + i_{L_f}(0) = \frac{1}{L_f}(2v_C - v_o)\alpha T_s + i_{L_f}(0)$$
$$= \frac{1}{L_f}(2\frac{v_{in}}{1-\alpha} - \frac{(1+\alpha)v_{in}}{1-\alpha})\alpha T_s + i_{L_f}(0) = \frac{\alpha T_s}{L_f} v_{in} + i_{L_f}(0) \quad (6.30)$$

where $i_{L_1}(0)$, $i_{L_2}(0)$ and $i_{L_f}(0)$ are the initial inductor current at $t = 0$.

Next switching interval $\varphi_1 T_s < t \leq \varphi_2 T_s$: By using Equation (6.11), the instantaneous current $i_{L_1}(\varphi_2 T_s)$ is determined as follows.

$$\int_{\varphi_1 T_s}^{\varphi_2 T_s} di_{L_1}(t) = \frac{1}{L_1}\int_{\varphi_1 T_s}^{\varphi_2 T_s} v_{L_1} dt$$
$$i_{L_1}(\varphi_2 T_s) = i_{L_1}(\varphi_1 T_s) + \frac{1}{L_1}(v_{in} - v_C)(\varphi_2 - \varphi_1)T_s$$
$$= i_{L_1}(\varphi_1 T_s) + \frac{1}{L_1}(v_{in} - \frac{v_{in}}{1-\alpha})(0.5 - \alpha)T_s$$
$$= \frac{0.5\alpha T_s}{L_1(1-\alpha)} v_{in} + i_{L_1}(0) \quad (6.31)$$

The instantaneous current $i_{L_2}(\varphi_2 T_s)$ is derived by using Equation (6.2) as

$$\int_{\varphi_1 T_s}^{\varphi_2 T_s} di_{L_2}(t) = \frac{1}{L_2}\int_{\varphi_1 T_s}^{\varphi_2 T_s} v_{L_2} dt$$
$$i_{L_2}(\varphi_2 T_s) = i_{L_2}(\varphi_1 T_s) + \frac{1}{L_2}(v_{in} - v_C)(\varphi_2 - \varphi_1)T_s$$
$$= i_{L_2}(\varphi_1 T_s) + \frac{1}{L_2}(v_{in} - \frac{v_{in}}{1-\alpha})(0.5 - \alpha)T_s$$
$$= i_{L_2}(0) - \frac{0.5\alpha T_s}{L_2(1-\alpha)} v_{in} \quad (6.32)$$

By using Equation (6.12), instantaneous current $i_{L_f}(\varphi_2 T_s)$ is determined as follows.

$$\int_{\varphi_1 T_s}^{\varphi_2 T_s} di_{L_f}(t) = \frac{1}{L_f}\int_{\varphi_1 T_s}^{\varphi_2 T_s} v_{L_f} dt$$
$$i_{L_f}(\varphi_2 T_s) = i_{L_f}(\varphi_1 T_s) + \frac{1}{L_f}(v_C - v_o)(\varphi_2 - \varphi_1)T_s$$
$$= i_{L_f}(\varphi_1 T_s) + \frac{1}{L_f}(\frac{v_{in}}{1-\alpha} - \frac{(1+\alpha)v_{in}}{1-\alpha})(0.5 - \alpha)T_s$$
$$= \frac{\alpha T_s}{L_f} v_{in} + i_{L_f}(0) - \frac{(0.5-\alpha)\alpha T_s}{L_f(1-\alpha)} v_{in} = \frac{0.5\alpha T_s}{L_f(1-\alpha)} v_{in} + i_{L_f}(0) \quad (6.33)$$

In the subsequent duration $\varphi_2 T_s < t \leq \varphi_3 T_s$, the instantaneous $i_{L_1}(\varphi_3 T_s)$ is determined as

$$\begin{aligned}
\int_{\varphi_2 T_s}^{\varphi_3 T_s} di_{L_1}(t) &= \frac{1}{L_1}\int_{\varphi_2 T_s}^{\varphi_3 T_s} v_{L_1} dt \\
i_{L_1}(\varphi_3 T_s) &= i_{L_1}(\varphi_2 T_s) + \frac{1}{L_1}(v_{in} - v_C)(\varphi_3 - \varphi_2)T_s \\
&= i_{L_1}(\varphi_2 T_s) + \frac{1}{L_1}(v_{in} - \frac{v_{in}}{1-\alpha})\alpha T_s \\
&= \frac{0.5\alpha T_s}{L_1(1-\alpha)} v_{in} + i_{L_1}(0) - \frac{\alpha^2 T_s}{L_1(1-\alpha)} v_{in} = \frac{(0.5-\alpha)\alpha T_s}{L_1(1-\alpha)} v_{in} + i_{L_1}(0)
\end{aligned} \tag{6.34}$$

By using Equation (6.17), The instantaneous $i_{L_2}(\varphi_3 T_s)$ is derived as follows.

$$\begin{aligned}
\int_{\varphi_2 T_s}^{\varphi_3 T_s} di_{L_2}(t) &= \frac{1}{L_2}\int_{\varphi_2 T_s}^{\varphi_3 T_s} v_{L_2} dt \\
i_{L_2}(\varphi_3 T_s) &= i_{L_2}(\varphi_2 T_s) + \frac{1}{L_2} v_{in}(\varphi_3 - \varphi_2)T_s \\
&= i_{L_2}(0) - \frac{0.5\alpha T_s}{L_2(1-\alpha)} v_{in} + \frac{\alpha T_s}{L_2} v_{in} = \frac{(0.5-\alpha)\alpha T_s}{L_2(1-\alpha)} v_{in} + i_{L_2}(0)
\end{aligned} \tag{6.35}$$

The instant $i_{L_f}(\varphi_3 T_s)$ is derived by using Equation (6.12) as follows.

$$\begin{aligned}
\int_{\varphi_2 T_s}^{\varphi_3 T_s} di_{L_f}(t) &= \frac{1}{L_f}\int_{\varphi_2 T_s}^{\varphi_3 T_s} v_{L_f} dt \\
i_{L_f}(\varphi_3 T_s) &= i_{L_f}(\varphi_2 T_s) + \frac{1}{L_f}(v_C - v_o)(\varphi_3 - \varphi_2)T_s \\
&= i_{L_f}(\varphi_2 T_s) + \frac{1}{L_f}(\frac{v_{in}}{1-\alpha} - \frac{(1+\alpha)v_{in}}{1-\alpha})\alpha T_s \\
&= \frac{0.5\alpha T_s}{L_f(1-\alpha)} v_{in} + i_{L_f}(0) - \frac{\alpha^2 T_s}{L_f(1-\alpha)} v_{in} = \frac{(0.5-\alpha)\alpha T_s}{L_f(1-\alpha)} v_{in} + i_{L_f}(0)
\end{aligned} \tag{6.36}$$

In the following interval $\varphi_3 T_s < t \leq \varphi_4 T_s$, the instantaneous currents are $i_{L_1}(\varphi_4 T_s)$, $i_{L_2}(\varphi_4 T_s)$ and $i_{L_f}(\varphi_4 T_s)$. Using Equation (6.11), the $i_{L_1}(\varphi_4 T_s)$ is derived as

$$\begin{aligned}
\int_{\varphi_3 T_s}^{\varphi_4 T_s} di_{L_1}(t) &= \frac{1}{L_1}\int_{\varphi_3 T_s}^{\varphi_4 T_s} v_{L_1} dt \\
i_{L_1}(\varphi_4 T_s) &= i_{L_1}(\varphi_3 T_s) + \frac{1}{L_1}(v_{in} - v_C)(\varphi_3 - \varphi_4)T_s \\
&= i_{L_1}(\varphi_3 T_s) + \frac{1}{L_1}(v_{in} - \frac{v_{in}}{1-\alpha})(0.5-\alpha)T_s \\
&= \frac{(0.5-\alpha)\alpha T_s}{L_1(1-\alpha)} v_{in} + i_{L_1}(0) - \frac{(0.5-\alpha)\alpha T_s}{L_1(1-\alpha)} v_{in} = i_{L_1}(0)
\end{aligned} \tag{6.37}$$

By using Equation (6.2), the $i_{L_2}(\varphi_4 T_s)$ is determined as follows.

$$\int_{\varphi_3 T_s}^{\varphi_4 T_s} di_{L_2}(t) = \frac{1}{L_2}\int_{\varphi_3 T_s}^{\varphi_4 T_s} v_{L_2} dt$$

$$\begin{aligned} i_{L_2}(\varphi_4 T_s) &= i_{L_2}(\varphi_3 T_s) + \frac{1}{L_2}(v_{in} - v_C)(\varphi_3 - \varphi_4)T_s \\ &= i_{L_2}(\varphi_3 T_s) + \frac{1}{L_2}(v_{in} - \frac{v_{in}}{1-\alpha})(0.5-\alpha)T_s \\ &= \frac{(0.5-\alpha)\alpha T_s}{L_2(1-\alpha)} v_{in} + i_{L_2}(0) - \frac{(0.5-\alpha)\alpha T_s}{L_2(1-\alpha)} v_{in} = i_{L_2}(0) \end{aligned} \tag{6.38}$$

The $i_{L_f}(\varphi_4 T_s)$ is derived by using Equation (6.12) as follows.

$$\int_{\varphi_3 T_s}^{\varphi_4 T_s} di_{L_f}(t) = \frac{1}{L_f}\int_{\varphi_3 T_s}^{\varphi_4 T_s} v_{L_f} dt$$

$$\begin{aligned} i_{L_f}(\varphi_4 T_s) &= i_{L_f}(\varphi_3 T_s) + \frac{1}{L_f}(v_C - v_o)(\varphi_3 - \varphi_4)T_s \\ &= i_{L_f}(\varphi_3 T_s) + \frac{1}{L_f}(\frac{v_{in}}{1-\alpha} - \frac{(1+\alpha)v_{in}}{1-\alpha})(0.5-\alpha)T_s \\ &= \frac{(0.5-\alpha)\alpha T_s}{L_f(1-\alpha)} v_{in} + i_{L_f}(0) - \frac{(0.5-\alpha)\alpha T_s}{L_f(1-\alpha)} v_{in} = i_{L_f}(0) \end{aligned} \tag{6.39}$$

Now, the average currents (I_L) of L_1 and L_2 are equal and it is determined in terms of i_{L_1} as follows.

$$\begin{aligned} I_L &= \frac{i_{L_1}(0) + i_{L_1}(\varphi_1 T_s)}{2}\alpha + \frac{i_{L_1}(\varphi_1 T_s) + i_{L_1}(\varphi_2 T_s)}{2}(0.5-\alpha) \\ &+ \frac{i_{L_1}(\varphi_2 T_s) + i_{L_1}(\varphi_3 T_s)}{2}\alpha + \frac{i_{L_1}(\varphi_3 T_s) + i_{L_1}(\varphi_4 T_s)}{2}(0.5-\alpha) \\ &= \frac{(1-\alpha)\alpha T_s}{2L_1(1+\alpha)} v_o + i_{L_1}(0) \end{aligned} \tag{6.40}$$

In a similar fashion, the average current I_{L_f} of L_f is derived as

$$I_{L_f} = \frac{(1-\alpha)\alpha T_s}{2L_f(1+\alpha)} v_o + i_{L_f}(0) \tag{6.41}$$

Moving to the analysis for *Case II:* $\alpha \in (0.5, 1)$, the expressions of average inductor currents I_L and I_{L_f} are the same as Equations (6.40) and (6.41) and are not repeated herein for brevity. The ripple in inductor current, Δi_L, of the two identical inductors is as follows.

$$\Delta i_L = \Delta i_{L_1} = \Delta i_{L_2} = \frac{\alpha T_s}{L} v_{in} = \frac{\alpha T_s}{L}\frac{(1-\alpha)}{(1+\alpha)} v_o \tag{6.42}$$

The ripple in output end inductor, Δi_{L_f}, is expressed as

$$\Delta i_{L_f} = \frac{\alpha T_s}{L_f} v_{in} = \frac{\alpha T_s}{L_f} \frac{(1-\alpha)}{(1+\alpha)} v_o \tag{6.43}$$

6.4.2 Case II, $\alpha \in (0.5, 1)$

The expressions of average inductor currents I_L and I_{L_f} are the same as given in Equations (6.40) and (6.41) respectively. The expressions of Δi_L and Δi_{L_f} are the same as provided in Equations (6.42) and (6.43) respectively.

6.5 CCM/DCM Boundary Load Condition

In Case I: $\alpha \in (0, 0.5]$, at boundary condition between CCM and DCM, $i_{L_1}(0) = i_{L_1}(\varphi_4 T_s) = 0$, and the average inductor current I_L is

$$I_L = \frac{(1-\alpha)\alpha T_s}{2L_1(1+\alpha)} v_o \tag{6.44}$$

In the proposed HSUIBoC, the steady-state input current is given by

$$i_{in} = I_{L_1} + I_{L_2} = 2I_L = \frac{(1-\alpha)\alpha T_s}{L_1(1+\alpha)} v_o \tag{6.45}$$

In ideal condition, the relation between output boundary current i_{OB} and input current i_{in} of the proposed HSUIBoC is $\frac{v_o}{v_{in}} = \frac{i_{in}}{i_{OB}} = \frac{1+\alpha}{1-\alpha}$. Hence, the output boundary current, i_{OB}, is derived as

$$i_{OB} = \frac{1-\alpha}{1+\alpha} i_{in} = \frac{(1-\alpha)^2 \alpha T_s}{L_1(1+\alpha)^2} v_o \tag{6.46}$$

Therefore, from Equation (6.46) the boundary load, R_B, between CCM and DCM is calculated as follows.

$$R_B = \frac{v_o}{i_{OB}} = \frac{L_1(1+\alpha)^2}{(1-\alpha)^2 \alpha T_s} \tag{6.47}$$

The minimum requirement of inductance value for a given load R is determined by

$$min\{L = L_1 = L_2\} = \frac{R_B(1-\alpha)^2 \alpha T_s}{(1+\alpha)^2} \tag{6.48}$$

Now, the average inductor current I_{L_f} of L_f is equal to the output current i_o as the ripple current passes through the output filter capacitor C_f. Therefore, at boundary condition ($i_{L_f}(0) = 0$), Equation (6.41) can be written as follows.

$$I_{L_f} = i_o = \frac{v_o}{R_B} = \frac{(1-\alpha)\alpha T_s}{2L_f(1+\alpha)} v_o \tag{6.49}$$

Therefore, for a given load R, the minimum requirement of inductance value is derived as follows.

$$min\{L_f\} = \frac{(1-\alpha)\alpha T_s R_B}{2(1+\alpha)} \tag{6.50}$$

Case II, $\alpha \in (0.5, 1)$: Similarly, it can be shown that R_B is the same as given in Equation (6.47) and the minimum requirements of inductance value ($L = L_1 = L_2$) and L_f for a given load R are the same as provided in Equations (6.48) and (6.50) respectively.

6.6 Ripple in Input Current

The duty ratio and the ripple in input current of CIBoC are denoted by α_c and Δi_c. The ripple in input current of CIBoC is $\Delta i_c = \frac{\alpha_c T_s v_{in}}{L}$. The ripple in input current of the proposed HSUIBoC is $\Delta i_{in} = \frac{\alpha T_s v_{in}}{L}$. The relation between the two input currents yields $\frac{\Delta i_{in}}{\Delta i_c} = \frac{\alpha}{\alpha_c}$. It is seen that the two converters have the same output voltage when α and α_c are related as follows.

$$\alpha = \frac{\alpha_c}{2 - \alpha_c} \tag{6.51}$$

Therefore, the relation of ripple in input current between the CIBoC and proposed HSUIBoC is as follows.

$$\frac{\Delta i_{in}}{\Delta i_c} = \frac{1}{2 - \alpha_c} < 1 \tag{6.52}$$

From the above relation, it is seen that the proposed HSUIBoC converter reduces ripple in input current for the CIBoC.

6.7 Design of Identical Capacitors ($C_1 = C_2 = C$)

When the switch S_1 conducts, the two identical capacitors ($C_1 = C_2 = C$) are connected in series and the superimposed capacitor voltage is fed to the output load. Therefore, when S_1

conducts the power released by these two identical capacitors is equal to the load power and the energy equation is defined by follows.

$$\frac{1}{2}\frac{C}{2}(2v_C)^2 = \frac{v_o^2}{R}T_s$$
$$C(v_{Cmax}^2 - v_{Cmin}^2) = \frac{C(v_{Cmax} + v_{Cmin})(v_{Cmax} - v_{Cmin})}{T_s} = \frac{v_o^2}{R} \tag{6.53}$$

The peak-to-peak ripple of capacitive voltage v_C is defined by

$$\Delta v_C = v_{Cmax} - v_{Cmin} \tag{6.54}$$

The average voltage of v_C is approximated by $\frac{(v_{Cmax}+v_{Cmin})}{2} = v_C$ and hence,

$$v_{Cmax} + v_{Cmin} = 2v_C = 2\frac{v_o}{1+\alpha} \tag{6.55}$$

Therefore, by using Equations (6.53)-(6.55), the minimum requirement of capacitance value of identical capacitors is derived as follows.

$$C_{min} = \frac{(1+\alpha)T_s}{2\Delta V_C}\frac{v_o}{R} \tag{6.56}$$

6.8 Design of Output Filter Capacitor (C_f)

The maximum peak-to-peak value of the AC (alternating current) component of the voltage across the capacitor C_f is as follows.

$$V_{C_{fpp}} = \frac{\Delta Q}{C_f} = \frac{i_o \alpha T_s}{C_f} = \frac{v_o \alpha T_s}{RC_f} \tag{6.57}$$

where ΔQ is the charge decrease during the interval $(0 < t < \varphi_1 T_s)$ while $\alpha \in (0, 0.5]$ and $(0 < t < \varphi_3 T_s)$ while $\alpha \in (0.5, 1)$. The requirement of C_f can be calculated by assuming $V_r = V_{C_{fpp}}$ where V_r is the output voltage ripple (OVR). Hence, the minimum requirement of output capacitor is expressed by

$$C_{fmin} = \frac{v_{omax}\alpha_{max}T_s}{R_{min}V_r} \tag{6.58}$$

The effect of equivalent series resistance (ESR) on OVR is required to analyse [127]. Therefore, the peak-to-peak voltage V_{rcfpp} across the ESR r_{C_f} is determined as follows.

$$V_{rcfpp} = r_{C_f}\Delta i_{L_f} = r_{C_f}\frac{\alpha T_s}{L_f}\frac{(1-\alpha)}{(1+\alpha)}v_o \tag{6.59}$$

The accurate ripple equation $V_r = V_{C_{fpp}} + V_{rcfpp}$ cannot be used as the r_{C_f} is unknown [117]. With C_f already designed by Equation (6.58), the expression ($r_{C_f} = V_{C_{fpp}}/i_o$) shall be evaluated to get maximum ESR value [14]. Therefore, in this way, the accurate OVR can be calculated. Moreover, considering the hold-up time ($t_{hold-up}$), output capacitor value can be decided and it is as follows [14], [117].

$$C_f \geq \frac{i_o \times t_{hold-up}}{0.01 \times v_o} = \frac{i_o}{0.01 \times v_o}\frac{1}{0.1 \times f_s} \tag{6.60}$$

6.9 Voltage and Current Stresses

The capacitor ripple voltage is neglected to simplify the analysis of the voltage stress of the semiconductor devices of the proposed converter. The maximum voltage stresses on the switches are derived as

$$v_S = v_{S_1} = v_{S_2} = v_C = \frac{v_o}{1+\alpha} \tag{6.61}$$

Equation (6.61) explains that below the output voltage rated switches can be used to design the converter. The maximum voltage stresses on the diodes D_1, D_2 and D_3 are as follows.

$$v_D = v_{D_1} = v_{D_2} = v_{D_3} = v_C = \frac{v_o}{1+\alpha} \tag{6.62}$$

The inductor ripple current is ignored to simplify the current stress analysis. The dc current flowing through the inductor is half of the input current. The rms (root mean square) currents flowing through the switches are derived as

$$I_{S_{rms}} = I_{S_{1rms}} = I_{S_{2rms}} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_{S_{1,2}}^2 dt} = \frac{i_o(1+\alpha)\sqrt{\alpha}}{2(1-\alpha)} \tag{6.63}$$

The rms currents of diodes D_1, D_3 and D_2 are as follows.

$$I_{D_{rms}} = I_{D_{1rms}} = I_{D_{3rms}} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_{D_{1,3}}^2 dt} = \frac{i_o(1+\alpha)}{2\sqrt{(1-\alpha)}} \tag{6.64}$$

$$I_{D_{2rms}} = i_o\sqrt{(1-\alpha)} \tag{6.65}$$

The features of the proposed HSUIBoC is compared with CIBoC in Table 6.1.

Table 6.1: Comparison between HSUIBoC and CIBoC

Items	CIBoC	Comparison	Proposed HSUIBoC
Voltage Gain	$\frac{1}{1-\alpha}$	$<$	$\frac{1+\alpha}{1-\alpha}$
Ripple current Δi_L	$\frac{(1-\alpha)\alpha T_s}{L} v_o$	$>$	$\frac{\alpha T_s}{L}\frac{(1-\alpha)}{(1+\alpha)} v_o$
Ripple voltage V_{rcfpp}	$r_{C_f}\frac{(1-\alpha)\alpha T_s}{L} v_o$	$>$	$r_{C_f}\frac{\alpha T_s}{L_f}\frac{(1-\alpha)}{(1+\alpha)} v_o$
min$\{L = L_1 = L_2\}$	$R_B(1-\alpha)^2\alpha T_s$	$>$	$\frac{R_B(1-\alpha)^2\alpha T_s}{(1+\alpha)^2}$
Voltage stress v_S	v_o	$>$	$\frac{v_o}{1+\alpha}$
Voltage stress v_D	v_o	$>$	$\frac{v_o}{1+\alpha}$
Current stress $I_{S_{rms}}$	$\frac{i_o\sqrt{\alpha}}{2(1-\alpha)}$	$<$	$\frac{i_o(1+\alpha)\sqrt{\alpha}}{2(1-\alpha)}$
Current stress $I_{D_{rms}}$	$\frac{i_o}{2\sqrt{(1-\alpha)}}$	$<$	$\frac{i_o(1+\alpha)}{2\sqrt{(1-\alpha)}}$

6.10 Power Losses and Efficiency Analysis

By assuming all the capacitors are ideal, conduction losses are analyzed by resistances of semiconductor devices and parasitic of inductors [84], [128]. The conduction losses due to both switches are defined by

$$P_{r_{DS(on)}} = r_{DS(on)}(I_{S_{1rms}}^2 + I_{S_{2rms}}^2) = r_{DS(on)}\frac{i_o^2(1+\alpha)^2\alpha}{2(1-\alpha)^2} \tag{6.66}$$

To analyse the switching loss, the transistor output capacitance C_{os} is assumed to be linear. During the turn-off period of the transistor, the drain to source voltage of the transistor rises from nearly zero to $v_C = v_o/(1+\alpha)$. Therefore, the switching losses for the two switches are as follows.

$$P_S = 2\frac{C_{os}v_C^2}{T_S} = 2\frac{C_{os}v_o^2}{T_S(1+\alpha)^2} \tag{6.67}$$

The resistance r_{D_1} of the D_1 and r_{D_3} of D_3 are equal as $r_D = r_{D_1} = r_{D_3}$. The losses due to these resistances are determined as

$$P_{r_{D_{1,3}}} = r_{D_1} I^2_{D_{1rms}} + r_{D_3} I^2_{D_{3rms}} = r_D \frac{i_o^2(1+\alpha)^2}{2(1-\alpha)} \tag{6.68}$$

The loss due to the resistance r_{D_2} of D_2 is calculated as

$$P_{r_{D_2}} = r_{D_2} I^2_{D_{2rms}} = r_{D_2} i_o^2 \sqrt{(1-\alpha)} \tag{6.69}$$

The average currents through the diodes D_1 and D_3 are derived as

$$I_{D_1} = I_{D_3} = \frac{1}{T_s}\int_0^{T_s} i_{D_{1,3}} dt = \frac{i_o(1+\alpha)}{2} \tag{6.70}$$

The forward voltages v_{fd_1} of D_1, v_{fd_2} of D_2 and v_{fd_3} of D_3 are equal ($v_{fd} = v_{fd_1} = v_{fd_2} = v_{fd_3}$). The power losses associated with the forward voltages v_{fd_1} and v_{fd_3} are determined as follows.

$$P_{v_{fd_{1,3}}} = v_{fd_1} \frac{i_o(1+\alpha)}{2} + v_{fd_3} \frac{i_o(1+\alpha)}{2} = v_{fd} i_o (1+\alpha) \tag{6.71}$$

The average current through the diode D_2 is derived as follows.

$$I_{D_2} = \frac{1}{T_s}\int_0^{T_s} i_{D_2} dt = i_o(1-\alpha) \tag{6.72}$$

Therefore, the power loss associated with the forward voltage v_{fd_2} of D_2 is

$$P_{v_{fd_2}} = v_{fd} i_o (1-\alpha) \tag{6.73}$$

The rms current flowing through the two identical inductors ($L_1 = L_2$) is expressed as follows.

$$I_{L_{1rms}} = I_{L_{2rms}} = \frac{i_o(1+\alpha)}{2(1-\alpha)} \tag{6.74}$$

The conduction losses due to the resistance r_L of both the inductor L_1 and L_2 are as follows.

$$P_{r_L} = r_L (I^2_{L_{1rms}} + I^2_{L_{2rms}}) = r_L \frac{i_o^2(1+\alpha)^2}{2(1-\alpha)^2} \tag{6.75}$$

By using Equations (6.66)-(6.69), (6.71), (6.73) and (6.75), the overall loss in the proposed HSUIBoC is determined as

$$P_{Loss} = P_{r_{DS(on)}} + P_S + P_{r_{fd_{1,3}}} + P_{r_{fd_2}} + P_{v_{fd_{1,3}}} + P_{v_{fd_2}} + P_{r_L} \tag{6.76}$$

Therefore, the efficiency of HSUIBoC is expressed as

$$\eta = \frac{1}{1 + \frac{P_{Loss}}{P_O}} = \frac{1}{1 + \frac{(1+\alpha)^2((r_{DS(on)} - r_D)\alpha + r_D + r_L)}{2(1-\alpha)^2 R} + \frac{2C_O R}{T_S(1+\alpha)^2} + \frac{2v_{fd}}{v_o} + \frac{r_{D_2}\sqrt{(1-\alpha)}}{R}} \tag{6.77}$$

6.11 Selection of Parameters

To calculate the minimum requirement of parameters, input voltage $v_{in} = 10$ V and a maximum output current $i_o = 1$ A are taken into consideration. The specification of the output voltage ripple is $V_r/V_O = 1\%$. To calculate the identical capacitance value the capacitive ripple voltage is determined by $\Delta V_C = v_C \times 1\% = [v_o/(1+\alpha)] \times 1\%$. The load resistance has been varied from 20 Ω to 120 Ω. The duty ratio is chosen in the range of 20 % to 80 %.

From Equation (6.48), it is seen that the values of L_1 and L_2 are inversely proportional to the duty ratio (α) and directly proportional to the load resistance (R). Therefore, at $R_{max} = 120$ Ω and duty ratio $\alpha_{min} = 20$ %, the inductances of L_1 and L_2 are 213.33 μH. From Equation (6.56), it is seen that the capacitance values of the identical capacitors are directly proportional to α and inversely proportional to R. Hence, at $\alpha_{max} = 80$ % and $R_{min} = 20$ Ω, the minimum capacitance values of the identical capacitors are 129.6 μF. By using Equation (6.60), at maximum $i_o = 1$ A and maximum output voltage $v_o = 90$ V at $\alpha_{max} = 80$ %, the minimum value of C_f is 222.22 μF. Specially, the values of L_1, L_2 and L_f are also provided for both the following cases in CCM.

Case I, $\alpha \in (0, 0.5]$: At 0.40 duty ratio, the output voltage v_o is 23.3 V. The load resistance $R = 30$ Ω is considered. By using Equation (6.48), the minimum requirement of inductance $L = L_1 = L_2$ is determined as 44.08 μH. The minimum requirement of the inductance value of L_f is calculated as 51.42 μH by using Equation (6.50).

Case II, $\alpha \in (0.5, 1)$: At this case, to get the output voltage $v_o = 40$ V, the required duty ratio is 0.60 and load resistance $R = 60$ Ω is considered. The minimum inductance value of $L = L_1 = L_2 = 45$ μH is determined by Equation (6.48).

For the robust performances of the proposed converter, the values of the inductors and the capacitors are chosen to be higher than the minimum values as given in Table 6.2. By using Equation (6.50), the minimum requirement of $L_f = 90$ μH is calculated.

Table 6.2: Parameter values of HSUIBoC considered for CCM operation

Parameters	**Value**
Input Voltage (v_{in})	10 V
Switching frequency (f_s)	50 kHz
Inductance ($L = L_1 = L_2$)	180 μH
Inductive resistance (r_L)	0.07 Ω
Identical capacitance ($C = C_1 = C_2$)	220 μF
Output-end inductance (L_f)	180 μH
Output capacitance (C_f)	330 μF
ESR of output capacitor (r_{C_f})	0.22 Ω
MOSFET drain-to-source on-resistance ($r_{DS(on)}$)	0.075 Ω
MOSFET output capacitance (C_{os})	315 pF
Diode forward voltage (v_{fd})	0.39 V
Diode resistance ($r_D = r_{D_1} = r_{D_2} = r_{D_3}$)	0.078 Ω

6.12 Small Signal Modelling Analysis

The state-space equation of this mode of operation is given by

$$\dot{\mathbf{x}}(t) = \mathbf{A_{av}}\mathbf{x}(t) + \mathbf{B_{av}}\mathbf{v_{in}}(t) \tag{6.78}$$

$$\mathbf{v_o}(t) = \mathbf{Z_{av}}\mathbf{x}(t) \tag{6.79}$$

where $\mathbf{A_{av}}$, $\mathbf{B_{av}}$ and $\mathbf{Z_{av}}$ are state average matrices. The average matrices are determined at

the switching operation $\alpha \in (0, 0.5]$ as follows.

$$\mathbf{A_{av}} = \mathbf{A_1}\alpha + \mathbf{A_2}(0.5-\alpha) + \mathbf{A_3}\alpha + \mathbf{A_2}(0.5-\alpha) \tag{6.80}$$

$$= (\mathbf{A_1} + \mathbf{A_3} - 2\mathbf{A_2})\alpha + \mathbf{A_2} = \begin{bmatrix} \frac{-r_L}{L_1} & 0 & \frac{\alpha-1}{L_1} & 0 & 0 \\ 0 & \frac{-r_L}{L_2} & 0 & \frac{\alpha-1}{L_2} & 0 \\ \frac{1-\alpha}{2C} & \frac{1}{2C} & 0 & \frac{-1-\alpha}{2C} & 0 \\ 0 & 0 & \frac{1+\alpha}{L_f} & 0 & \frac{-1}{L_f} \\ 0 & 0 & 0 & \frac{1}{C_f} & \frac{-1}{RC_f} \end{bmatrix} \tag{6.81}$$

$$\mathbf{B_{av}} = (\mathbf{B_1} + \mathbf{B_3} - 2\mathbf{B_2})\alpha + \mathbf{B_2} = \mathbf{B_1} = \begin{bmatrix} \frac{1}{L_1} & \frac{1}{L_2} & 0 & 0 & 0 \end{bmatrix}^T \tag{6.82}$$

$$\mathbf{Z_{av}} = (\mathbf{Z_1} + \mathbf{Z_3} - 2\mathbf{Z_2})\alpha + \mathbf{Z_2} = \mathbf{Z_1} = [0\ 0\ 0\ 0\ 1] \tag{6.83}$$

By using the state-space small signal modelling analysis procedure provided in [117], and Equations (6.80), (6.82) and (6.83), the voltage to duty ratio power stage transfer function is derived as

$$G_{v\alpha}(s) = \frac{\hat{v}_o(s)}{\hat{\alpha}(s)} = \mathbf{Z_{av}}(s\mathbf{I} - \mathbf{A_{av}})^{-1}(\mathbf{A_1} + \mathbf{A_3} - 2\mathbf{A_2})\mathbf{X} \tag{6.84}$$

where $\mathbf{X}$ is the steady part and defined by $\mathbf{X} = -{\mathbf{A_{av}}}^{-1}\mathbf{B_{av}}V_{in}$. By using the parameters provided in Table 6.2 and Equation (6.84), the following power stage transfer function is determined.

$$G_{v\alpha}(s) = \frac{2.7925 \times 10^8 s^3 + 1.3945 \times 10^{11} s^2 + 1.1265 \times 10^{16} s + 4.3761 \times 10^{18}}{s^5 + 878.788 s^4 + 5.393 \times 10^7 s^3 + 4.079 \times 10^{10} s^2 + 2.127 \times 10^{14} s + 7.974 \times 10^{16}} \tag{6.85}$$

The bode diagram of the uncompensated plant $G_{v\alpha}(s)$ is shown in Figure 6.8. The phase margin of $G_{v\alpha}(s)$ is 1.29° and the gain margin is infinity. All the poles and zeros are in the left-half of

s-plane. In the following section, a voltage mode single-integral-lead controller is designed.

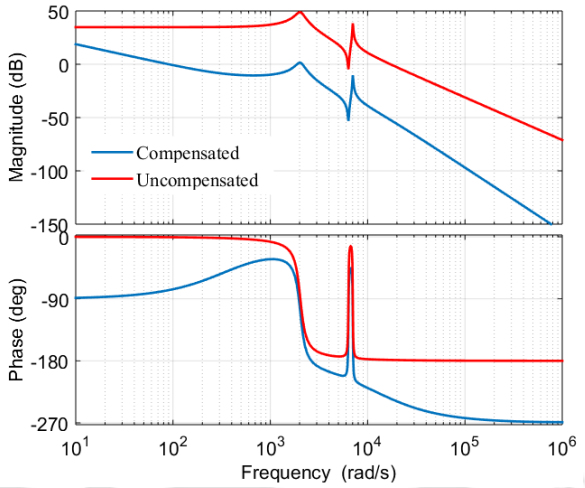


Figure 6.8: Bode diagram of uncompensated power stage transfer function ($G_{v\alpha}(s)$) as provided in Equation (6.85) and compensated power stage transfer function ($G_{comp}(s)$) as provided in Equation (6.87)

6.13 Closed-loop Control System

To investigate the closed loop performance, a suitable controller is required. To enable to the controller circuit and to check the closed loop performance, a compensator is designed based on the voltage to duty ratio transfer function $G_{v\alpha}(s)$. The block diagram representation of the closed loop control circuit is shown in Figure 6.9. Bode design tool is used to design a Type-II based (single-integral-lead) controller for the interleaved boost converter [116].

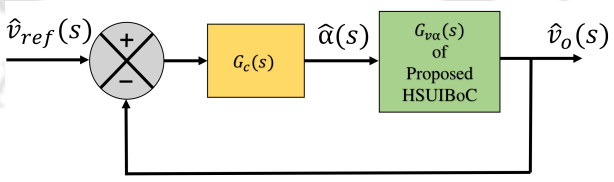


Figure 6.9: Block diagram representation of closed-loop control systems

The $k-$factor based transfer function of the compensator is as follows.

$$G_c(s) = \frac{B(1+\frac{s}{\omega_{zc}})}{q^2 s(1+\frac{s}{\omega_{pc}})} \tag{6.86}$$

where $q = \sqrt{\frac{\omega_{pc}}{\omega_{zc}}}$. The parameters of the controller are $\omega_{pc} = 12086.46$, $\omega_{zc} = 375.793$ and

$B = 51.309$. Therefore, the transfer function of compensated plant is calculated as follows.

$$G_{comp}(s) = G_c(s)G_{v\alpha}(s) = \frac{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0}{s^7 + b_6 s^6 + b_5 s^5 + b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s} \tag{6.87}$$

The coefficients of the $G_{comp}(s)$ are provided as $a_4 = 1.433 \times 10^{10}$, $a_3 = 1.254 \times 10^{13}$, $a_2 = 5.807 \times 10^{17}$, $a_1 = 4.417 \times 10^{20}$, $a_0 = 8.438 \times 10^{22}$, $b_6 = 1.297 \times 10^4$, $b_5 = 6.456 \times 10^7$, $b_4 = 6.927 \times 10^{11}$, $b_3 = 7.058 \times 10^{14}$, $b_2 = 2.651 \times 10^{18}$, $b_1 = 9.637 \times 10^{20}$.

The phase and gain margins of the compensated plant ($G_{comp}(s)$) are 43.3° and 10.3 dB. As, both the gain and phase margins of the compensated plant are positive, the closed-loop system will be stable. The closed loop zeros are $z_1 = z_2 = -5.5245 \times 10^1 \pm i6.3477 \times 10^3$, $z_3 = -3.8888 \times 10^2$, $z_4 = -3.7579 \times 10^2$. The closed loop poles are $s_1 = -71.6752$, $s_2 = -1.2176 \times 10^4$, $s_3 = -3.8888 \times 10^2$, $s_4 = s_5 = -4.0333 \times 10^1 \pm i7.0532 \times 10^3$, $s_6 = s_7 = -1.2399 \times 10^2 \pm i2.2320 \times 10^3$. It is also seen that all the closed loop poles are in left half of the s-plane. Therefore, it also validates the closed-loop system stability.

6.14 Simulation Results

In the MATLAB-Simscape platform, a simulation is carried out by using the parameters given in Table 6.2. The simulation performance is investigated in two stages, viz. open loop and closed loop.

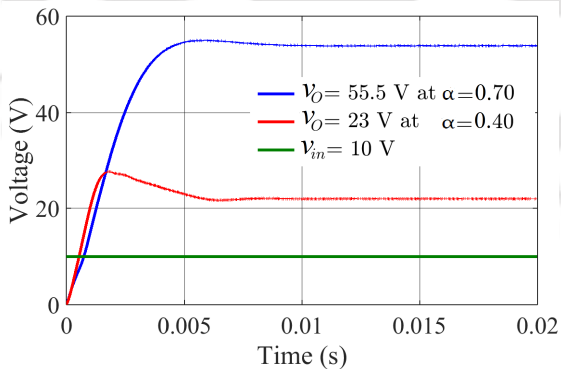
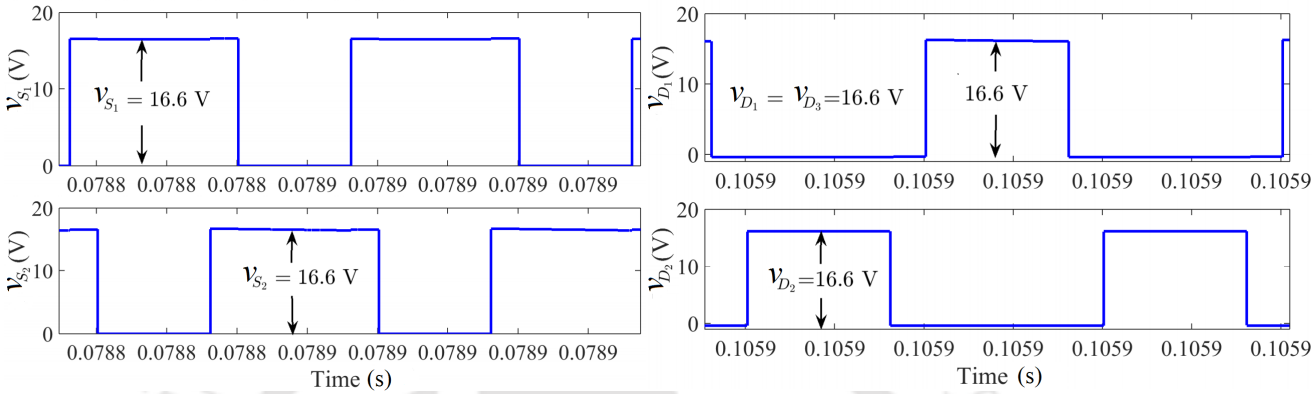


Figure 6.10: Simulation result of output voltage of the proposed HSUIBoC

6.14.1 Open-loop performance

At duty ratio 0.40 and 0.70, the output voltages are 23.3 V and 55.5 V respectively as shown in Figure 6.10. The results satisfy the conversion ratio developed in Equation (6.27). At 0.40

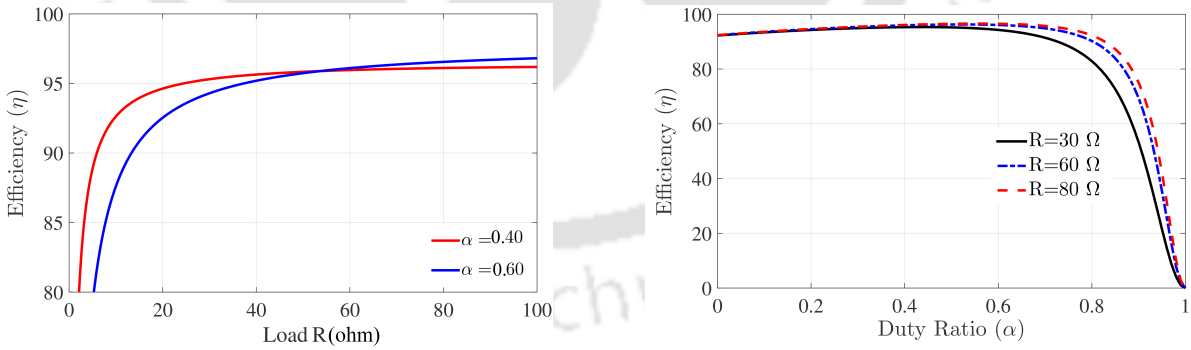
duty ratio, the simulation result of the voltage stress of the switches S_1 and S_2 is shown in Figure 6.11a. The result validates Equation (6.61). At 0.40 duty ratio, the simulation result of the voltage stress of the diodes D_1, D_2 and D_3 is shown in Figure 6.11b, and the result validates Equation (6.62).



(a) (b)

Figure 6.11: Simulation results for $\alpha = 0.40$ showing (a) Switch voltage stress $v_S = 16.6$, and (b) Diode voltage stress $v_D = 16.6$ V

The variation of efficiency with respect to the load resistance is shown in Figure 6.12a by using Equation (6.77). The change of efficiency due to the increment of duty ratio (α) is shown in Figure 6.12b also by using Equation (6.77).



(a) (b)

Figure 6.12: Simulation results of efficiency due to (a) Change of R, and (b) Change of α

6.14.2 Closed-loop performance

The closed-loop simulation model of the proposed HSUIBoC is shown in Figure 6.13. The load parameter uncertainties and reference input voltage variation are checked. Figure 6.14a

shows the output voltage along with the corresponding output current of the proposed HSUIBoC due to reference voltage change.

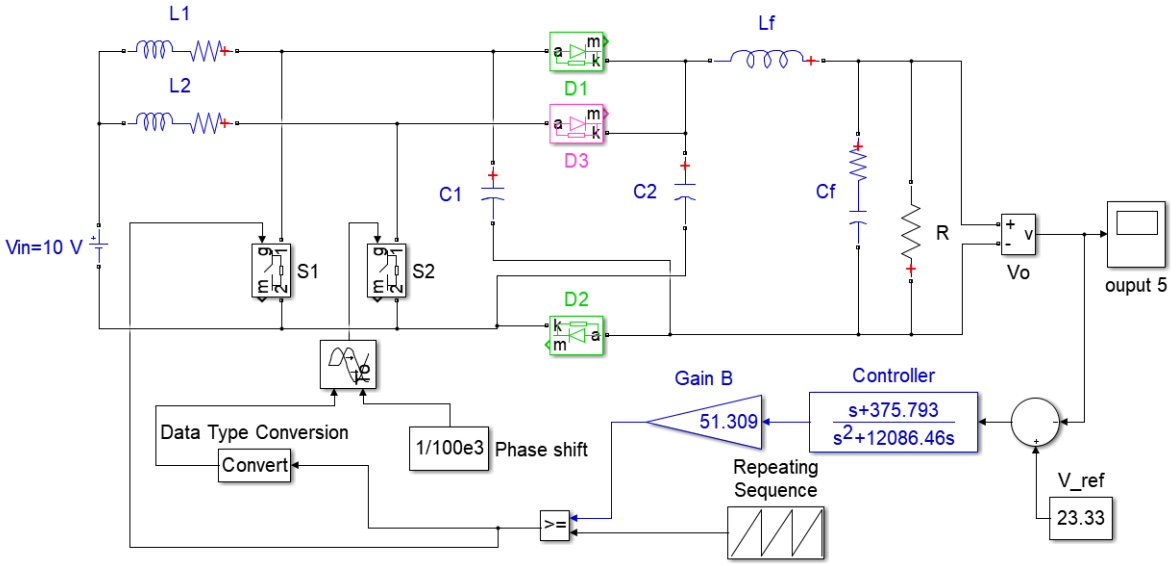
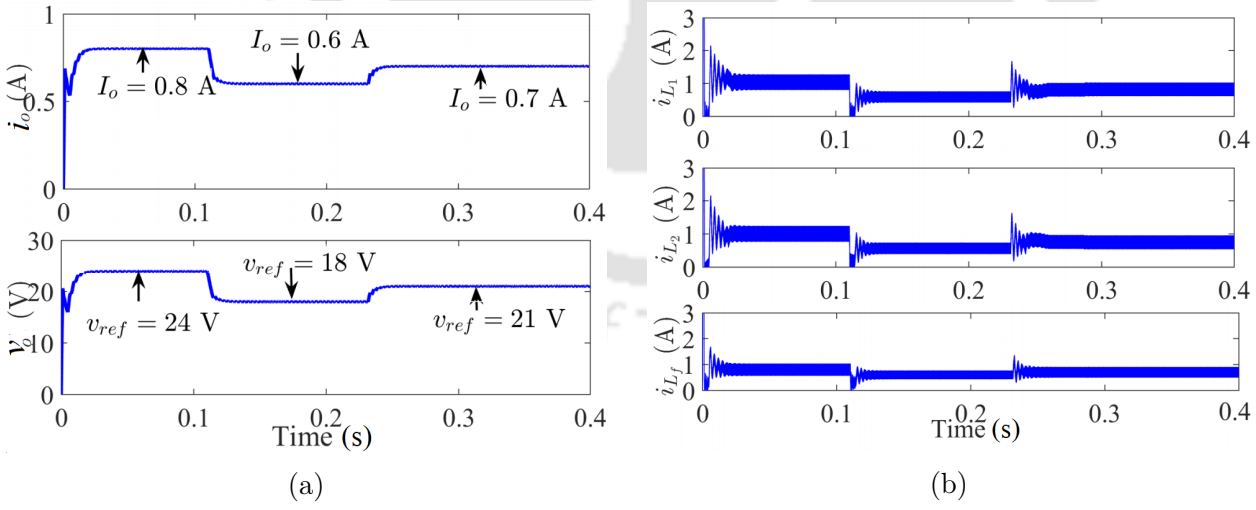


Figure 6.13: Diagram of the Matlab closed-loop model simulation

The output voltage follows the reference voltages 24 V, 18 V and 21 V. It can be seen that the output voltage does not have overshoot during the change of v_{ref}. Figure 6.14b shows the change of currents through the inductors due to reference change.



(a) (b)

Figure 6.14: Simulation results of reference change (a) Output voltage and current, and (b) Currents through the inductors

To check the load parameter uncertainties, 50 % load change takes place at $t = 0.14$ s and $t = 0.26$ s as shown in Figure 6.15a. The output voltage follows the reference in spite of load

change. The currents through the inductors due to load change are shown in Figure 6.15b.

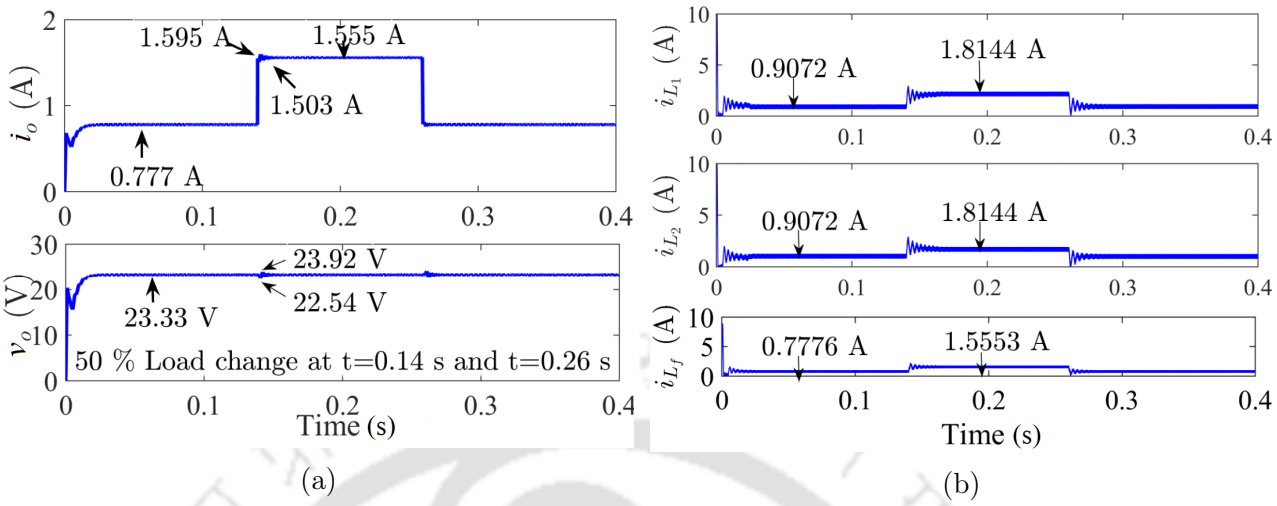


Figure 6.15: Simulation results due to 50 % load change (a) Output voltage, and (b) Currents through the inductors

6.15 Experimental Setup and Results

The schematic diagram of open-loop HSUIBoC is shown in Figure 6.16. The experimental setup of the proposed HSUIBC is shown in Figure 6.17.

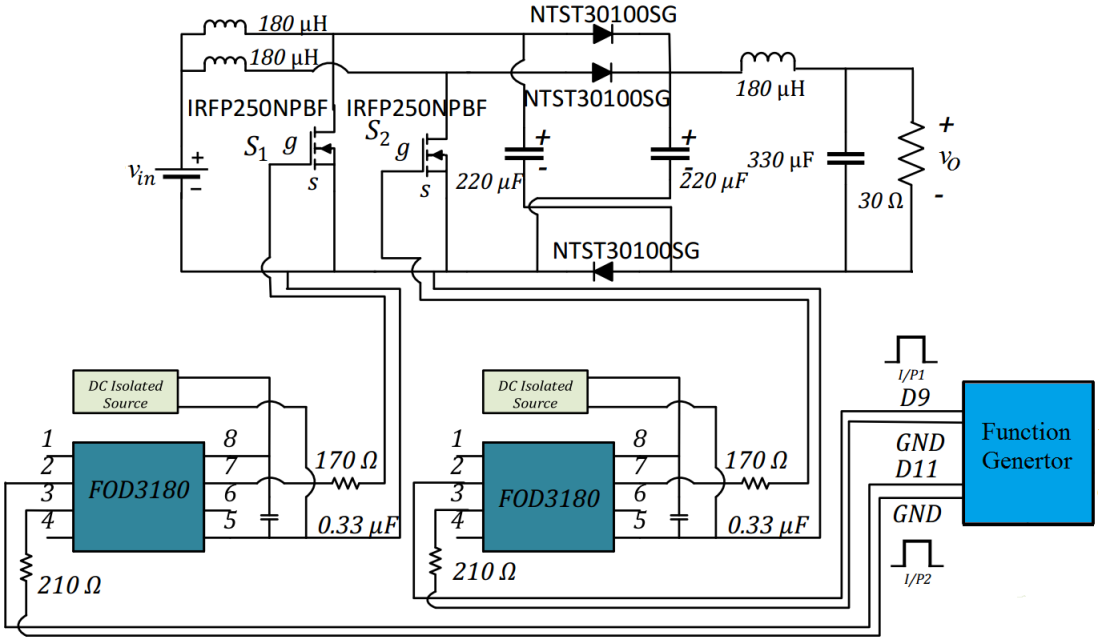


Figure 6.16: Open-loop schematic diagram of the proposed HSUIBoC

The proposed HSUIBoC is implemented in CCM by using the parameters given in Table 6.2. The switches S_1 and S_2 are implemented by the MOSFET IRFP250NPBF. FOD3180 MOSFET gate driver ICs are used for the switches. The diodes D_1, D_2 and D_3 are implemented by NFK03TS30100SG (equivalent to NTST30100SG and NTSB30100S-1G).

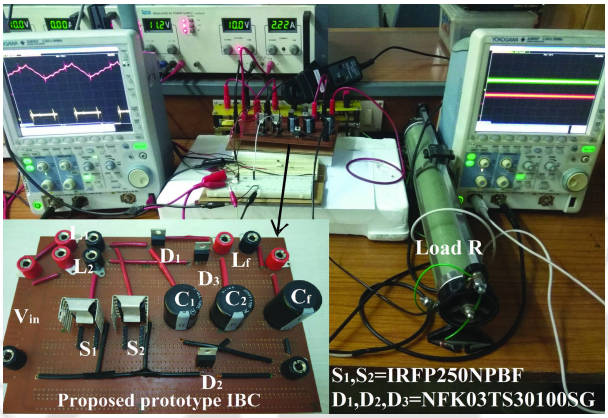
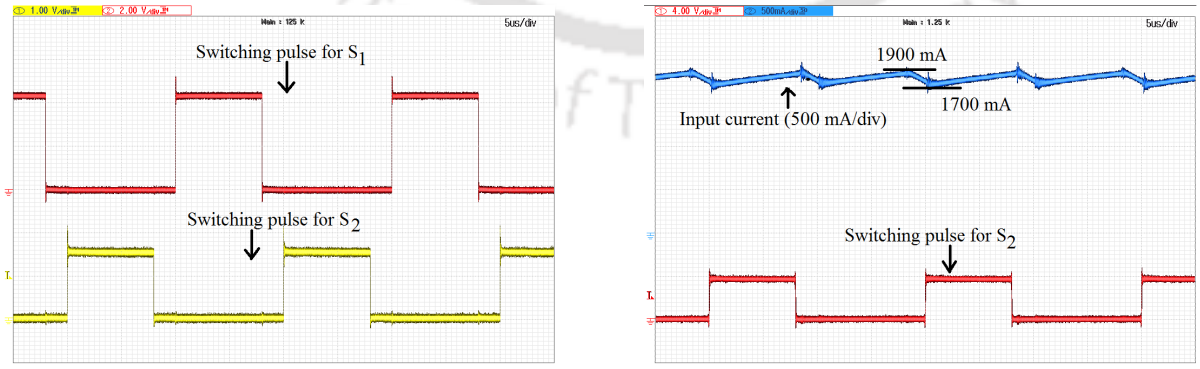


Figure 6.17: Experimental set-up of the proposed HSUIBoC

These diodes have considerably low forward voltage $v_{fd} = 0.39$ V at a forward current of 5 A. The porpoised converter can be used for PV cell or LED driver circuit. Here, only open-loop experimental results are provided. The experimental implementation of closed-loop control will be conducted in future. The open-loop results are provided for the following two cases.

6.15.1 Case I, $\alpha \in (0, 0.5]$

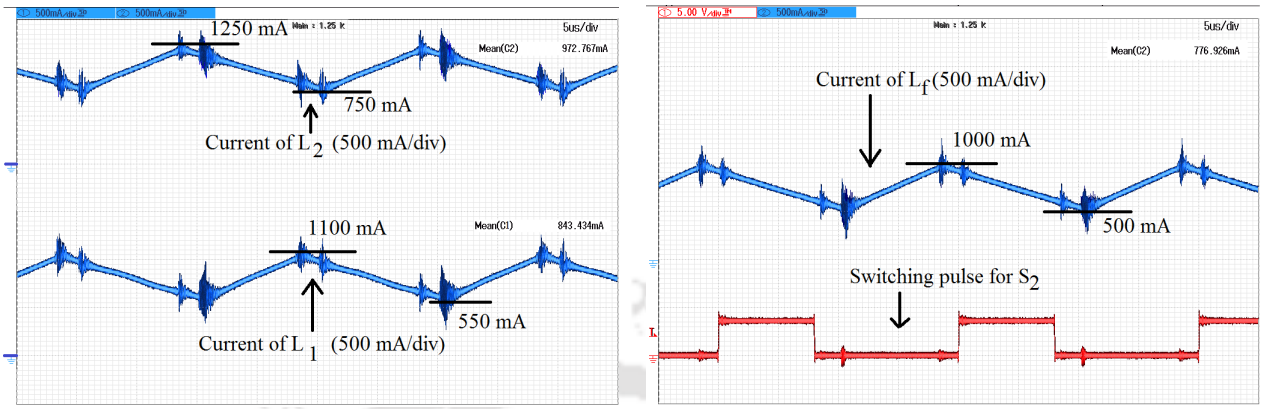
In this case, the experiment is performed with duty ratio α of 0.40 and load resistance R of 30 Ω. The two phase-shifted switching pulses are shown in Figure 6.18a. The waveform of the input current is shown in Figure 6.18b.



(a) (b)

Figure 6.18: Experimental waveforms of (a) Two-phase switching pulses, and (b) Input current i_{in} for $\alpha = 0.40$

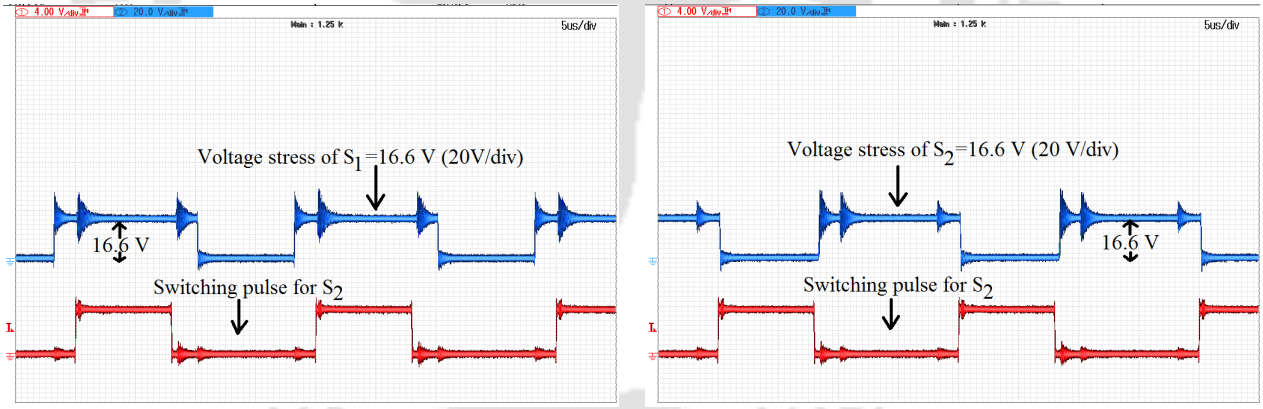
The phase shifted currents i_{L_1} and i_{L_2} are shown in Figure 6.19a. The current i_{L_f} is provided in Figure 6.19b.



(a) (b)

Figure 6.19: Experimental results of inductor currents (a) i_{L_1}, i_{L_2}, and (b) i_{L_f} for $\alpha = 0.40$

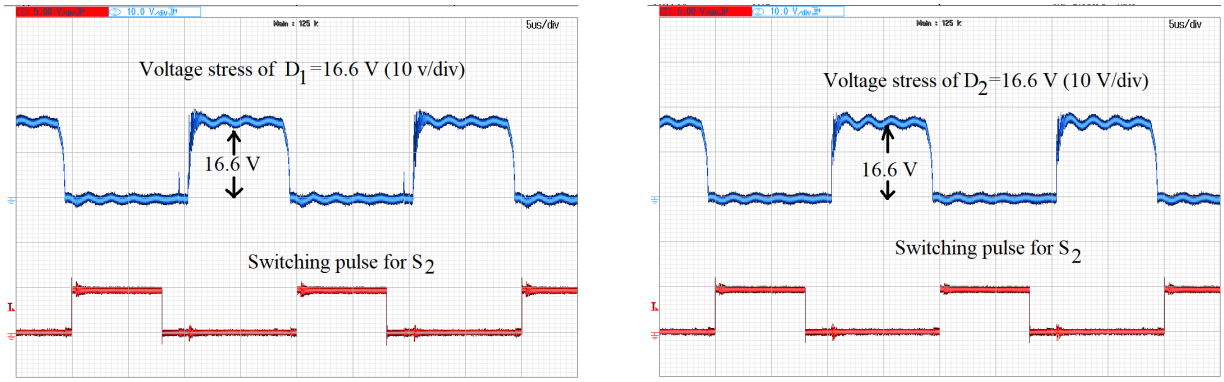
The waveforms of voltage stresses of the switches S_1 and S_2 are shown in Figure 6.20a and Figure 6.20b respectively. The voltage stress satisfies Equation (6.61).



(a) (b)

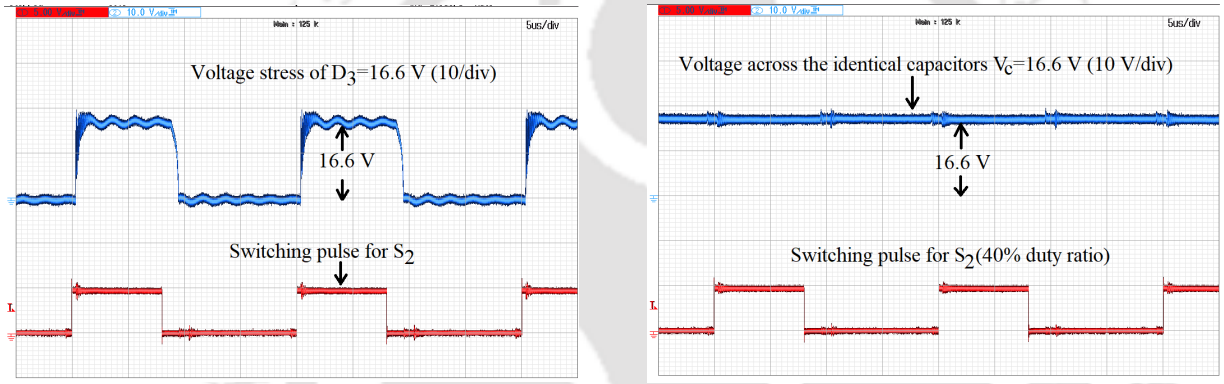
Figure 6.20: Experimental result of voltage stresses (a) v_{S_1}, and (b) v_{S_2} for $\alpha = 0.40$

The diode voltage stresses v_{D_1}, v_{D_1} and v_{D_3} are shown in Figures 6.21a, 6.21b and 6.22a respectively. The diode voltage stress satisfies Equation (6.62). The voltage across the identical capacitors is $v_C = v_{in}/(1-\alpha) = 16.6$ V as shown in Figure 6.22b. The output load current i_o is provided in Figure 6.23a. From Figure 6.23b, it is seen that the output voltage $v_o = 23$ V at 0.40 duty ratio satisfies the conversion ratio as derived in Equation (6.27).



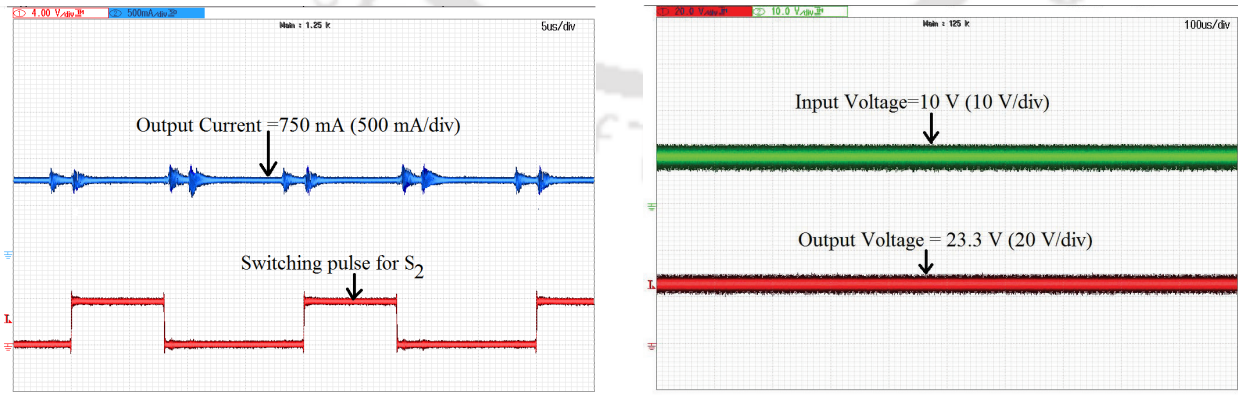
(a) (b)

Figure 6.21: Experimental result of voltage stresses (a) v_{D_1}, and (b) v_{D_2} for $\alpha = 0.40$



(a) (b)

Figure 6.22: Experimental results of (a) v_{D_3}, and (b) v_C for $\alpha = 0.40$

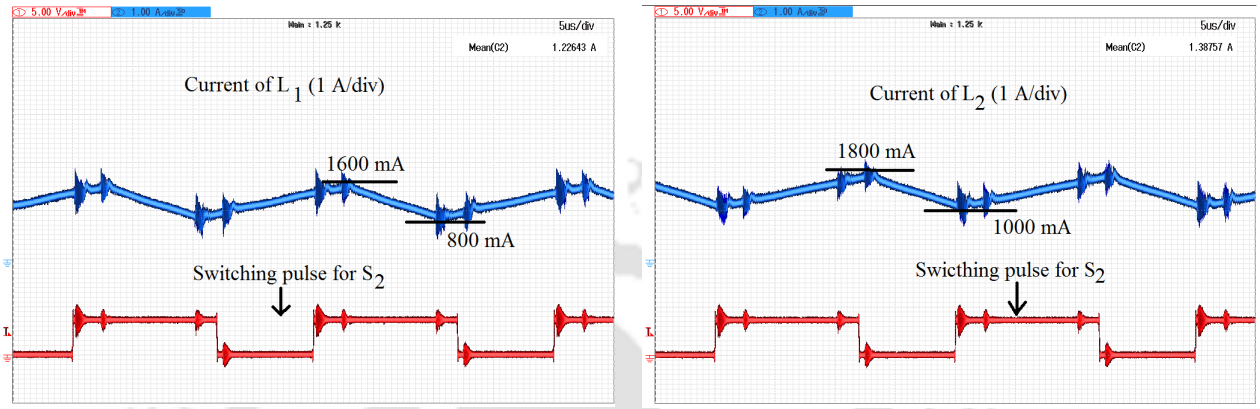


(a) (b)

Figure 6.23: Experimental results of (a) Output current $i_o = 750$ mA, and (b) Output voltage $v_o = 23.3$ V for $\alpha = 0.40$

6.15.2 Case II, $\alpha \in (0.5, 1)$

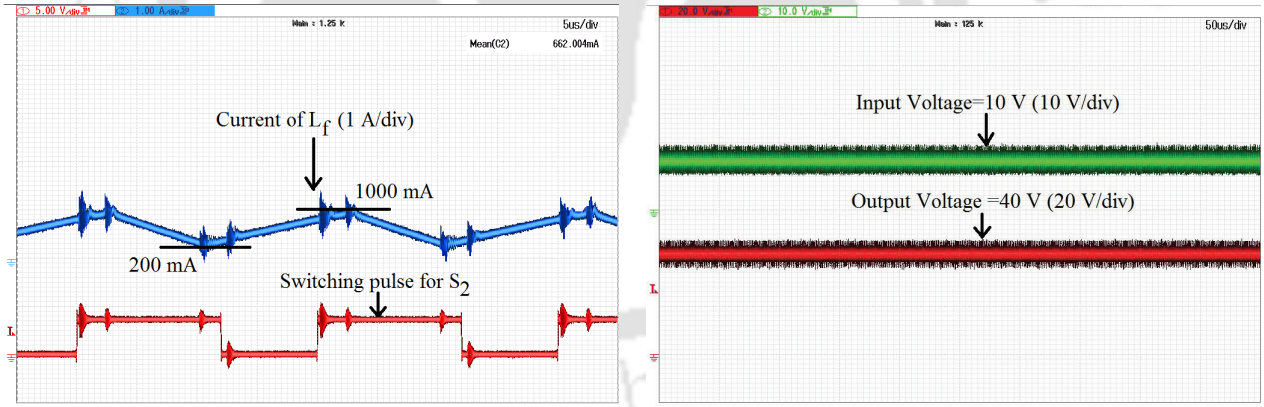
In this case, the load resistance, R, is considered 60 Ω and duty ratio is 0.60. The two phase-shifted inductor currents i_{L_1} and i_{L_2} with respect to the switching pulse for S_2 are provided in Figures 6.24a and 6.24b respectively.



(a) (b)

Figure 6.24: Experimental result of inductor current (a) i_{L_1}, and (b) i_{L_2} for $\alpha = 0.60$

The current i_{L_f} is shown in Fig. 6.25a. The desired output voltage $v_o = 40$ V at 0.60 duty ratio is shown in Fig. 6.25b. It also satisfies the conversion ratio provided in Equation (6.27).



(a) (b)

Figure 6.25: Experimental results of (a) Inductor current i_{L_f}, and (b) $v_o = 40$ V for $\alpha = 0.60$

In the first stage, by varying the load R and keeping $\alpha = 0.40$ and $v_{in} = 10$ V constant, the efficiency of the proposed converter is checked and the experimental data are provided in Table 6.3a. In the second stage, the experimental results of the efficiency are provided by varying the load R and fixing the $\alpha = 0.60$ and $v_{in} = 10$ V and the experimental data are provided in

Table 6.3a. The efficiency curves with respect to load change are shown in Figure 6.26a.

By varying α and keeping R constant, the efficiency is checked and experimental data are provided in Table 6.3b. The efficiency curve with respect to duty ratio change is shown in Figure 6.26b.

Table 6.3: Experimental results of HSUIBoC

(a) With load parameter R (Ω) variation

α	R	i_{in}(A)	v_o (V)	i_o (A)	η (%)
0.40	20	3.010	21.68	1.250	90.03
0.40	30	1.780	22.32	0.735	92.16
0.40	40	1.350	22.58	0.565	94.50
0.40	50	1.080	22.82	0.441	93.18
0.40	60	0.925	22.97	0.375	93.12
0.40	70	0.812	23.07	0.327	92.90
0.40	80	0.700	23.14	0.280	92.56
0.60	30	5.00	37.00	1.182	87.00
0.60	40	3.85	37.92	0.935	92.09
0.60	50	3.02	38.57	0.750	95.78
0.60	60	2.65	38.97	0.643	94.55
0.60	70	2.30	39.14	0.560	95.29
0.60	80	2.01	39.44	0.492	96.53

(b) With variation of duty ratio α

R	α	i_{in}(A)	v_o (V)	i_o (A)	η (%)
30	0.20	0.773	14.50	0.495	92.85
30	0.25	0.952	16.00	0.552	92.77
30	0.30	1.180	17.80	0.615	92.77
30	0.35	1.460	19.89	0.688	93.72
30	0.40	1.850	22.30	0.777	93.66
30	0.45	2.320	25.00	0.856	92.94
30	0.50	2.990	28.27	0.965	91.23
60	0.20	0.373	14.95	0.237	94.99
60	0.25	0.477	16.63	0.273	95.17
60	0.30	0.585	18.27	0.308	96.19
60	0.35	0.747	20.67	0.347	96.01
60	0.40	0.927	23.13	0.385	96.06
60	0.45	1.170	26.05	0.431	95.96
60	0.50	1.487	29.72	0.473	94.53

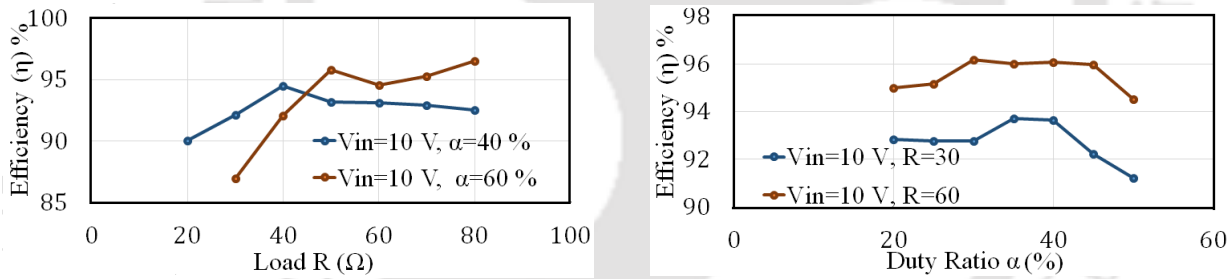


Figure 6.26: Plots of experimental efficiency versus (a) Load R, and (b) α

Together Tables 6.4 and 6.5 show the comparison among the existing IBoCs and the converter proposed in this chapter. The IBoC presented in [14] operates for $\alpha < 0.5$. The IBoCs presented in [92] and [129] operate for $\alpha > 0.5$. But the proposed HSUIBoC operates for $0 < \alpha < 1$. As shown in Tables 6.4 and 6.5, the constant n is the turns ratio in the existing converters [92], [101], [106]. It is observed that the voltage conversion ratio of the existing HSUIBoC depends on either the turns ratio of a coupled inductor or a transformer. But the proposed HSUIBoC can achieve the voltage gain without a coupled inductor or a transformer. The requirements of the passive and active components in existing converters are high. The

voltage conversion ratio of the converter presented in [106] is $\frac{2+n}{(1-\alpha)}$. Therefore, at $n = 2$ and $\alpha = 0.60$, the voltage gain is 10. The voltage gain of the proposed IBC is grater than the IBCs presented [129], [130]. With equal number winding i.e. N=1, the IBoC behaves as a conventional IBoC [101]. The proposed HSUIBoC has better efficiency. The requirements of semiconductor devices and passive components are less than the existing converters given in Table. 6.4 and 6.5. The converter presented in [131], works for $\alpha > 0.5$. A high step-up interleaved converter is introduced by utilizing two coupled inductors in [132]. The voltage gain of this converter is $v_o/v_{in} = (2n + 4)/(1 - \alpha)$. Therefore, at the same duty cycle and input voltage, the output voltage will be more compared to the proposed one. But the number of active and passive elements is comparatively larger. Another high step-up converter with interleaved technique is introduced in [133]. The voltage conversion ratio is $v_o/v_{in} = (2(n + 1))/(1 - \alpha)$. Herein, the requirement of the total passive and active components are more.

Table 6.4: Part-1: Comparison among the existing high step-up converters and the proposed HSUIBoC.

Topology	IBoC introduced in [14]	IBoC introduced in [92]	IBoC introduced in [101]	IBoC introduced in [106]	IBoC introduced in [129]
Voltage Gain	$\frac{1}{1-2\alpha}$	$\frac{2}{1-\alpha} + n\alpha$	$\frac{n}{1-\alpha}$	$\frac{2+n}{1-\alpha}$	$\frac{1}{1-\alpha}$
v_s	Not provided	$\frac{v_o}{2}\frac{n\alpha v_{in}}{2}$	$\frac{v_o}{n}$	$\frac{v_o}{2+n}$	Not provided
v_D	Not provided	$v_o - n\alpha v_{in}$	$v_o(2 - \frac{1}{n})$	$\frac{2v_o}{2+n}$	Not provided
Switches	3	2	2	2	2
Diodes	2	4	2	4	4
Inductors	1 coupled (2 windings)1 single	3 single	2 coupled (6 windings)1 single	2 single	3 single
Capacitors	1	3	4	3	3
Transformers	0	1	0	1	0
α Range	$\alpha < 0.5$	$\alpha > 0.5$	$0 < \alpha < 1$	$0 < \alpha < 1$	$\alpha > 0.5$
Efficiency	95.12%	95.8%	92.7%	94.65%	84.5%

Table 6.5: Part-2: Comparison among the existing high step-up converters and the proposed HSUIBoC

Topology	IBoC introduced in [130]	IBoC introduced in [131]	IBoC introduced in [132]	IBoC introduced in [133]	The proposed IBoC
Voltage Gain	$\frac{1}{1-\alpha}$	$\frac{1+n}{1-\alpha}$	$\frac{2n+4}{1-\alpha}$	$\frac{2(n+1)}{1-\alpha}$	$\frac{1+\alpha}{1-\alpha}$
v_s	Not provided	$\frac{(1+2n)V_O}{1+n}$	$\frac{v_o}{2n+4}$	$\frac{v_o}{2(n+1)}$	$\frac{v_o}{1+\alpha}$
v_D	Not provided	Not provided	$\frac{(n+1)v_o}{n+2}$	$\frac{v_o}{n+1}$	$\frac{v_o}{1+\alpha}$
Switches	4	4	2	2	2
Diodes	0	0	4	4	3
Inductors	1 coupled 2 single	1 coupled (3 windings), 2 single	2 (4 windings)	2 (4 windings)	3 single
Capacitors	1	3	4	4	3
Transformers	0	0	0	0	0
α Range	$0 < \alpha < 1$	$\alpha > 0.5$	$0 < \alpha < 1$	$0 < \alpha < 1$	$0 < \alpha < 1$
Efficiency	97.5%	Not Provided	95%	96%	96.53%

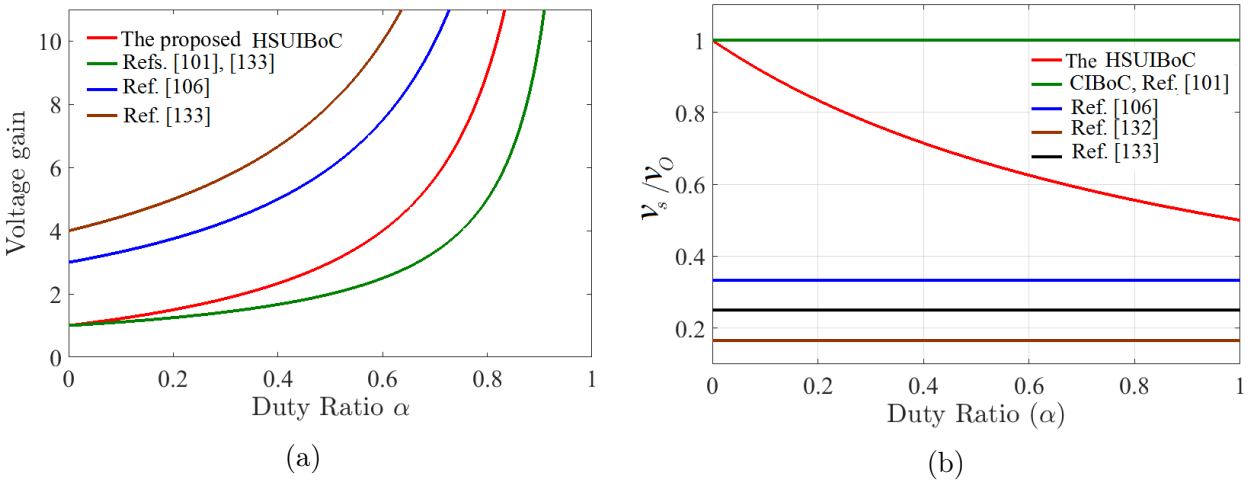


Figure 6.27: Comparison with existing topologies in terms of (a) Voltage gain, and (b) Voltage stress.

A graphical comparisons of voltage gain and voltage stress among the existing and proposed

converter are shown in Figures 6.27a and 6.27b respectively as the operation range for these topologies is $0 < \alpha < 1$. Figure 6.27b shows the voltage stress as a function of v_S/v_o.

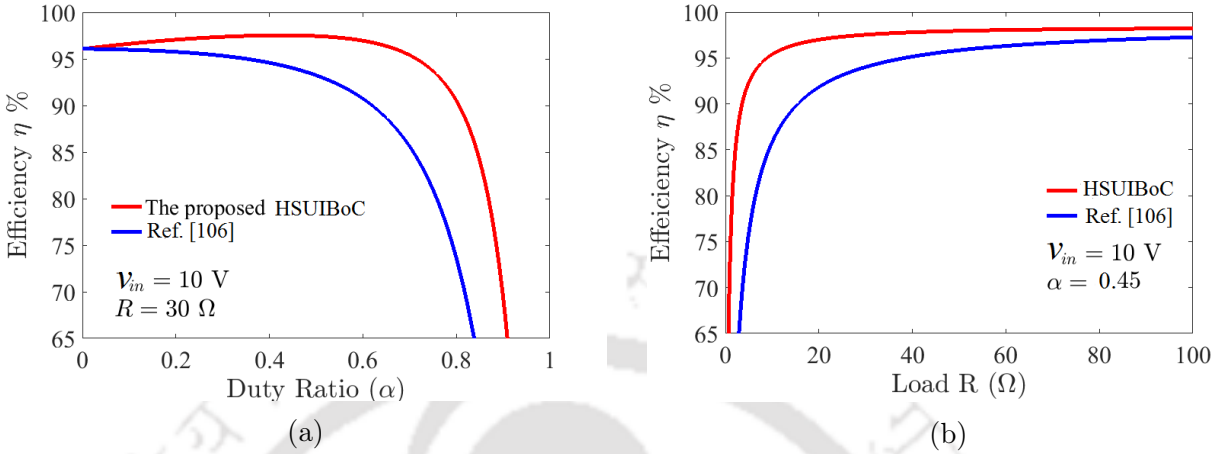


Figure 6.28: Efficiency comparison with existing topologies for (a) Duty ratio change, and (b) Load change.

A comparisons of efficiency between the proposed converter and Ref. [106] are carried out for duty ratio and load change as shown in Figures 6.28a and 6.28b respectively.

6.16 Summary

This chapter presents the operating principle, circuit parameter analysis and mathematical expressions of an IBoC proposed to achieve a high step-up conversion ratio. The proposed HSUIBoC circuit is capable of producing higher output voltage compared to CIBoC at the same duty cycle. As the on-time duty ratio is smaller, the conduction loss also reduces. The expressions for high step-up conversion ratio, ripple and average currents in inductors, minimum requirement of identical capacitors, minimum requirement of output filter capacitor and boundary load condition between CCM and DCM are derived. Small-signal modelling followed by design of a voltage mode k-factor-based controller is accomplished. Simulation results of the closed-loop control systems are provided. The hardware implementation of the proposed converter is successfully carried out. Power loss is analysed and 96.53% efficiency is achieved. The components required in the proposed converter are compared with existing converters to examine the cost-effectiveness of the former.

7

Conclusions and Future Work

Substantial work has been published on the development of high step-up/step-down DC-DC converters. However, in this thesis work, the author has made an effort on some different approaches to design high step-up/down converters which have some advantages over the ones in the existing literature. Therefore, in this thesis, five novel DC-DC converters viz. HSDBuC, HSDIBuC, HSDIBuC-DWCI, HSUBoC, HSUIBoC have been designed. This chapter reflects the overall contributions and provides the conclusion of the thesis. Finally, a vision on the future scope of this thesis is suggested to carry the work forward.

7.1 Conclusions

The thesis presents the design and implementation of DC-DC converters with improved step-up/step-down conversion ratio. A switch-capacitor cell has been used to modify the step-down voltage conversion ratio of CBuC and CIBuC, whereas the step-up conversion ratios of CBoC and CIBoC have been improved using a diode-capacitor cell. In this thesis, a total of five converters namely HSDBuC, HSDIBuC, HSDIBuC-DWCI, HSUBoC and HSUIBoC have been proposed in chapters 2, 3, 4, 5 and 6 respectively.

HSDBuC independent of the turns ratio of transformer or coupled inductor has been proposed in **chapter 2**. The proposed HSDBuC achieves less output voltage at the same duty cycle compared to CBuC using a switch-capacitor cell. Hence, the proposed HSDBuC is suitable for applications requiring large step-down ratio while avoiding a narrow duty cycle to obtain a lower output voltage. The modified conversion ratio reduces the current and voltage stresses of the semiconductor devices. Thus, active elements with less voltage and current ratings can be used to implement HSDBuC. Apart from this, the modified conversion ratio of HSDBuC helps to achieve less ripple in input current, inductor current and output voltage. Further, the two inductors of HSDBuC are replaced by a directly-coupled DWCI helping in the reduction of ripples in input current, inductor current as well as output voltage. Maximum efficiency 93.5% has been achieved experimentally. The closed-loop experiment shows a stable performance of the converter without any overshoot under a step-change in reference voltage and 50% load change.

As CIBuC suffers from the same problem of narrow duty cycle like CBuC when a very high-input to low-output voltage conversion is required, the voltage conversion ratio of the former has been improved using the switch-capacitor cell. HSDIBuC introduced in **chapter 3** has a simple circuit configuration and can produce a low-output voltage at a sufficiently higher duty ratio. The ripples in input current, inductor current and output voltage have been reduced by the newly developed conversion ratio. Active elements with comparatively lower voltage and current ratings can be used as these ratings have been reduced by the newly developed conversion ratio. HSDIBuC operates in the range of $0 < \alpha \leq 1$ achieving maximum efficiency of 96.33% at $\alpha = 0.60$. Finally, HSDIBoC has been designed and experimental results have been provided to validate the claims.

A total of three inductors are required to design HSDIBuC in which two single inductors

have been placed in the output-end resulting in larger size and weight. Therefore, these two single inductors have been replaced by a DWCI reducing the volume of HSDIBuC as the windings of DWCI share the cores as presented in **chapter 4**. The addition of DWCI not only reduces the converter size and weight but also it provides a few advantageous technical features such as reduction of ripples in the inductor currents through the windings of DWCI without affecting the step-down voltage conversion ratio. In addition, the coupling effect on the reduction of the minimum value of the output filter capacitor has been derived through step-by-step analysis which shows that the coupling factor is capable of reducing the capacitance value. At $\alpha = 0.40$ and $\alpha = 0.55$, experimental results have been provided in an open-loop to validate the performance of DWCI. It is also observed from experimental as well as simulation results that DWCI does not affect the steady-state output voltage. A voltage mode PI controller has been designed to enable the closed-loop system.

After modifying the voltage conversion ratio of CBuC and CIBuC using a switch-capacitor cell, the voltage conversion ratio of CBoC has been improved using a diode-capacitor cell in **chapter 5**. Two single inductors of the proposed HSUBoC have been replaced by a DWCI to reduce the ripples in inductor current and output voltage. It is seen that the voltage conversion ratio of HSUBoC is independent of the turns ratio of DWCI. DWCI also reduces the size of magnetic cores as both the windings of DWCI share cores. The voltage stresses of the semiconductor devices are less than the output voltage. The experimental results are provided to see the physical realizability of the proposed HSUBoC. A maximum efficiency of 94.58% has been achieved experimentally for HSUBoC.

In **chapter 6**, the diode-capacitor cell which has been used to improve the step-up conversion ratio of HSUBoC, is also utilized to improve the step-up voltage conversion ratio of a CIBoC. Thus, the proposed HSUIBoC is capable of producing higher output voltage compared to CIBoC at the same duty cycle reducing the conduction losses as the on-time duty ratio is less. The ripples in input current, inductor current and output voltage have been reduced. The voltage stress of the active elements are less compared to the conventional and ones in existing topologies. Open-loop experimental results of these quantities have been provided to validate the claims. Followed by small-signal modelling, a voltage mode k-factor-based controller has been designed and the simulated results on the closed-loop performances have been given. A maximum efficiency of 96.53% is achieved experimentally.

Table 7.1: Summary of work done and scope for future work

Converters	Features	Advantages	Scope for future work

HSDBuC	• Made of
	  • A CBoC
	  • A switch-capacitor cell
	  • A DWCI
	• Designed in CCM
	• Hard-switching
	• Operating range: $0 < \alpha \leq 1$
		• High step-down ratio
		• Less ripples in
		  • Input and indcutor currents
		  • Output voltage
		• Active elements:
		  • Less voltage stress
		  • Less current stress
		• High efficiency ($\eta_{max} = 93.5\%$)
			• DCM operation
			• Soft-switching

HSDIBuC	• Made of
	  • A CIBoC
	  • A switch-capacitor cell
	• Designed in CCM
	• Hard-switching
	• Operating range: $0 < \alpha \leq 1$
		• High step-down ratio
		• Less ripples in
		  • Input and inductor currents
		• Active elements:
		  • Less voltage stress
		  • Less current stress
		• High efficiency ($\eta_{max} = 96.33\%$)
			• DCM operation
			• Soft-switching
			• Output voltage ripple

HSDIBuC-DWCI	• Made of
	  • A HSDIBuC
	  • DWCI
	• Designed in CCM
	• Hard-switching
	• Operating range: $0 < \alpha \leq 1$
		• Less ripples in
		  • In currents of DWCI
		  • Output voltage
		• Lower capacitance
		• Active elements:
		  • Less current stress
			• DCM operation
			• Soft-switching

HSUBoC	• Made of
	  • A CBoC
	  • A diode-capacitor cell
	  • DWCI
	• Designed in CCM
	• Hard-switching
	• Operating range: $0 < \alpha \leq 1$
		• High step-up ratio
		• Less ripples in DWCI
		• Less output ripple voltage
		• Less voltage stress
		• High Efficiency ($\eta_{max} = 94.58\%$)
			• DCM operation
			• Closed-loop experiment
			• Soft-switching

HSUIBoC	• Made of
	  • A CIBoC
	  • A diode-capacitor cell
	• Designed in CCM
	• Hard-switching
	• Operating range: $0 < \alpha \leq 1$
		• High step-up ratio
		• Less ripples in DWCI
		• Less output ripple voltage
		• Less voltage stress
		• High efficiency ($\eta_{max} = 96.53\%$)
			• Use of DWCI
			• Closed-loop experiment
			• DCM operation
			• Soft-switching

7.2 Suggestions for Future Work

(i) In this work, the proposed HSDBuC, HSDIBuC, HSDIBuC-DWCI, HSUBoC and HSUIBoC DC-DC converters in the continuous conduction mode (CCM), have been designed. Therefore, designing of these converters in discontinuous conduction mode (DCM) remains to be an important research work.

(ii) The proposed converters may be implemented with soft switching techniques to reduce switching loss and switch stress.

(iii) Chapter 5 presented closed-loop performance of HSUBoC in simulation. The work may be extended to verify the results experimentally.

(iv) A high step-up interleaved boost converter (HSUIBoC) has been presented in chapter 6. The work can be extended by employing DWCI to reduce ripple in HSUIBoC and by conducting experiment to test realizability and close loop performance.

List of Publications

Journal publications

1. **Biswas M.**, Majhi S. and Nemade H., *Design and Analysis of a High-Efficiency Two-Phase Interleaved Boost Converter with Modified Conversion Ratio and Low Voltage Stress*, J. Circuits, Syst. Comput., Vol. 30, No. 9, July, 2021.*(Chapter 6)*

2. **Biswas M.**, Majhi S. and Nemade H., *A High Step-Down DC-DC Converter with Reduced Inductor Current Ripple and Low Voltage Stress*, IEEE Transaction on Industry Applications Vol. 57, Issue 2, 2021 *(Chapter 2)*

3. **Biswas M.**, Majhi S. and Nemade H., *Performance of a Coupled Inductor for Interleaved Buck Converter with Improved Step-down Conversion Ratio*, IET Power Electronics., Vol. 14, Issue 2, 2021, p. 239-256. *(Chapter 4)*

4. **Biswas M.**, Majhi S. and Nemade H., *Two-phase high efficiency interleaved buck converter with improved step-down conversion ratio and low voltage stress*, IET Power Electronics., Vol. 12, Issue 15, 2019, p. 3942 – 3952. *(Chapter 3)*

Conference publications

1. **Biswas M.**, Majhi S. and Nemade H., A Larger Step-down Ratio Buck Converter with Reduced Ripple in Input Current and Output Voltage, *The IEEE International conference on "Power Electronics, Smart Grid and Renewable Energy" (IEEE PESGRE)*, Kerala, India, January, 2020. *(Chapter 2)*

2. **Biswas M.**, Majhi S. and Nemade H., Ripple Improvement and Steady State Analysis of a Boost Converter with Higher Step-up Ratio, *The 10^{th} International Conference on Power Electronics, Machines and Drives (IET PEMD)*, Nottingham, December, 2020.*(Chapter 5)*

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