INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI
SHORT ABSTRACT OF THESIS

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SHORT ABSTRACT

The video coding standards are used to compress the video before transmission and revert back into the normal format at the receiving end. High-Efficiency Video Coding (HEVC) is the state of the art video coding standard developed by motion picture expert group (MPEG) as well as video coding expert group (VCEG). This standard supports a wide range of video resolutions, but mainly developed for high-resolution videos. It reduces the bit-rate requirement around 50% as compared to H.264/AVC video coding standard. However, the reduction in bit-rate achieved at the cost of the increase in computational complexity. Motion estimation (ME) is one of the most important and computationally extensive blocks in all the video coding standards. Hence, there is a great demand towards the development of efficient algorithms and architectures for ME. In this thesis, we have made an attempt to develop power-efficient ME algorithms and architectures for HEVC.

To begin with, a detailed study of the ME algorithm is carried out at the integer level. The techniques such as pixel truncation, sub-sampling and removing of the prediction unit part sizes are used to reduce the computational complexity of the ME at integer level without much degradation in the video quality. We also examined the effect of these techniques in term of bit-rate and PSNR on HEVC. In order to reduce complexity further, using these techniques, we proposed an algorithm which uses hexagonal search pattern with a fixed number of search points at each grid and labelled as hexagonal grid search (HGS).

The second part of the thesis emphasizes in the design of low-power architecture for the HGS algorithm. Towards this, we first modified motion vector (MV) prediction processes such that it is more suitable for hardware implementation. It is not the proposed process, but we used this with the proposed integer ME algorithm. In order to reduce computational power, in the proposed architecture, we used a few techniques such as data reuse, 4:2 and 3:2 compressors. We also replaced multiplication circuit with the look-up table and employed suitable adder in our design.

The final part of the thesis focuses on the new fractional ME (FME) algorithm and its corresponding architecture. The proposed algorithm is developed based on the fact that most of the final MVs lies either nearer to the integer MV position or have either horizontal or vertical movements. Simulation studies revealed that the amount of degradation depends on the types of search pattern used. So, we proposed three different search patterns. All three proposed pattern required fewer search points compared to the conventional method. We also highlighted the designing of the scalable architecture for Hadamard Transform (HT) which is used to compute a sum of absolute transform difference (SATD) operation involved in FME of HEVC. The proposed architecture is based on the decomposition of larger size HT into smaller HTs. The proposed architecture is capable to compute the HTs of all sizes supported by HEVC.