LOW-FREQUENCY RIPPLE ANALYSIS AND MITIGATION OF SINGLE-PHASE SWITCHED BOOST INVERTER AND REDUCED-SWITCH CURRENT-FED SWITCHED INVERTER

Pramit Nandi

LOW-FREQUENCY RIPPLE ANALYSIS AND MITIGATION OF SINGLE-PHASE SWITCHED BOOST INVERTER AND REDUCED-SWITCH CURRENT-FED SWITCHED INVERTER

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by

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To my loving parents and sister

For their endless love, support and encouragement

CERTIFICATE

This is to certify that the thesis entitled **"Low-frequency ripple analysis and mitigation of Single-phase Switched Boost Inverter and Reduced-Switch Current-Fed Switched Inverter"**, submitted by **Pramit Nandi** (166102001), a research scholar in the Department of Electronics and Electrical Engineering, Indian Institute of Technology Guwahati, for the award of the degree of Doctor of Philosophy, has been carried out by him under my supervision and guidance. The thesis has fulfilled all requirements as per the regulations of the institute and, in my opinion, has reached the standard needed for submission. The results embodied in this thesis have not been submitted to any other University or Institute for the award of any degree or diploma.

Dated:

Guwahati.

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ABSTRACT

Single-phase converters are mainly preferred to connect systems that work with relatively low-power range, viz., uninterruptible power supply (UPS), distributed generation (fuel cell, photovoltaic (PV), wind, etc.), battery or super-capacitor energy storage, electric vehicles, adjustable-speed drives, etc. In such applications, the Z-Source Inverter (ZSI) and quasi-ZSI (qZSI) can be employed, which can boost input dc voltages to achieve better dc-ac gain and can also offer better EMI noise immunity. The active-front-end impedance-source inverters (AFE-ISIs), such as Switched Boost Inverter (SBI), Current-Fed Switched Inverter (CFSI), etc., can replace ZSI and qZSI, as AFE-ISIs reduce the passive component count and achieve better efficiency than ZSI and qZSI. Compared to SBI, CFSI has a higher gain while having the same component count as SBI. Also, unlike SBI, the CFSI provides a continuous input current. Thus, CFSI is more suitable for renewable energy and fuel cell applications.

In order to improve the efficiency of CFSI by reducing the number of switches, this thesis proposes a new topology named as Reduced-Switch CFSI (RSCFSI). It retains all advantages of SBI and CFSI while removing one switch. Hence, the proposed inverter can achieve improved efficiency compared to SBI and CFSI. In this thesis, the steady-state analysis of the RSCFSI is illustrated, and the conventional simple boost control-based PWM (SBC-PWM) is modified for RSCFSI. Furthermore, this thesis proposes another PWM strategy, namely Enhanced Boost Control-based PWM (EBC-PWM), which can achieve a higher boost factor and dc-ac voltage gain compared to SBC-PWM. In this thesis, a comparison between RSCFSI and other existing AFE-ISIs is presented to highlight the advantages and limitations of the RSCFSI. The RSCFSI is also implemented in hardware to verify the theoretical analysis.

This thesis also deals with the low-frequency ripple problem in single-phase AFE-ISIs, which is one of the most troublesome issues in any single-phase inverter. If this low-frequency ripple is not diminished below an engineering tolerance limit, the passive elements of the active-front-end network are impacted by the low-frequency ripples, which eventually distorts the output voltage. In this thesis, the low-frequency ripple of both SBI and RSCFSI is analyzed, which outlines the presence of the second harmonic component. In the case of

RSCFSI, the low-frequency ripple problem becomes more severe than that of SBI as it contains an additional fundamental component. Based on the analysis, the amount of low-frequency ripple present in the active-front-end network parameters is estimated for both SBI and RSCFSI, which reveals that significantly larger passive components are required to maintain smaller ripples, resulting in poor power density for both SBI and RSCFSI.

As a solution to the low-frequency ripple problem in SBI, this thesis proposes the Active Power Decoupling (APD)-integrated SBI to deflect the low-frequency ripple to an auxiliary capacitor. Three independent APD-integrated SBI topologies are explored and compared, which indicates the boost-type topology is the most advantageous in reducing the low-frequency ripple in the active-front-end network. As a result, smaller passive elements are required in the active-front-end network. In order to properly mitigate the low-frequency ripple for varying ac loads of the SBI and also to avoid overcharging of the auxiliary capacitor, a closed-loop control strategy is developed for the APD-integrated SBI. A hardware prototype is built for the boost-type APD-integrated SBI, and the advantages of APD integration are corroborated by the experimental results.

In the case of the APD-integrated SBI, it is observed the extra switches and passive elements introduce additional losses, which brings down efficiency. Therefore, this thesis explores more efficient alternate solutions for the RSCFSI and further introduces the APD-integrated RSCFSI (APDRSCFSI). Since the low-frequency ripple energy is deflected to an auxiliary capacitor without adding extra switches, the inverter can employ smaller passive elements. It is observed when APDRSCFSI is operated with SBC-PWM, the dc-ac gain of the inverter is lowered. As a solution, EBC-PWM is extended for APDRSCFSI to improve its dc-ac gain. A comparison between RSCFSI and APDRSCFSI with SBC-PWM and EBC-PWM is also presented in this thesis. The fundamental and second harmonic ripples in RSCFSI pose additional challenges for the APD integration and corresponding closed-loop controllers. So, this thesis illustrates a closed-loop control strategy, which incorporates dc-ac power conversion as well as APD operation. The APDRSCFSI is also implemented in hardware to verify the theoretical analysis with experimental results.

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

Single-phase converters are mainly preferred to connect systems that work with relatively low-power range applied to small consumers. A wide class of single-phase applications can be achieved by using such converters [1, 2], viz., standby power supplies, uninterruptible power supply (UPS), distributed generation (fuel cell, photovoltaic (PV), wind, etc.), battery or super-capacitor energy storage, electric vehicles, distributed dc power systems, avionics, adjustable-speed drives, flywheel energy storage systems, electronic loads, dc circuit breaker, power factor correction (PFC), micro-inverters, line voltage regulators, universal active power filters (APFs), etc. Generally, in such applications, a conventional single-phase voltage source inverter (VSI), as shown in Fig. 1.1, can be employed. However, the conventional VSI has some drawbacks as listed below:

(a) The upper and lower switches of each phase leg cannot be turned on simultaneously either by purpose or by electromagnetic interference (EMI) noise. Otherwise, the inverter phase leg(s) will be shorted, which is known as shoot-through. As a result of the shoot-through, the switches would be destroyed. Generally, the shoot-through problem arises from unintentional turning on of the switches owing to EMI noise. The

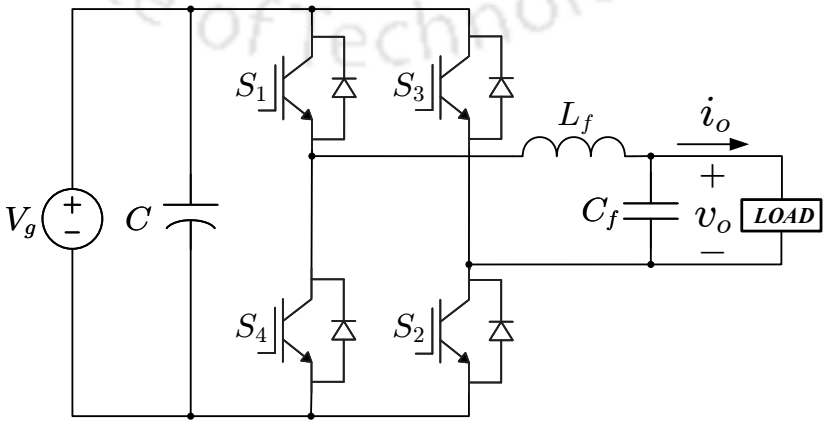


Fig. 1.1 Voltage Source Inverter (VSI).

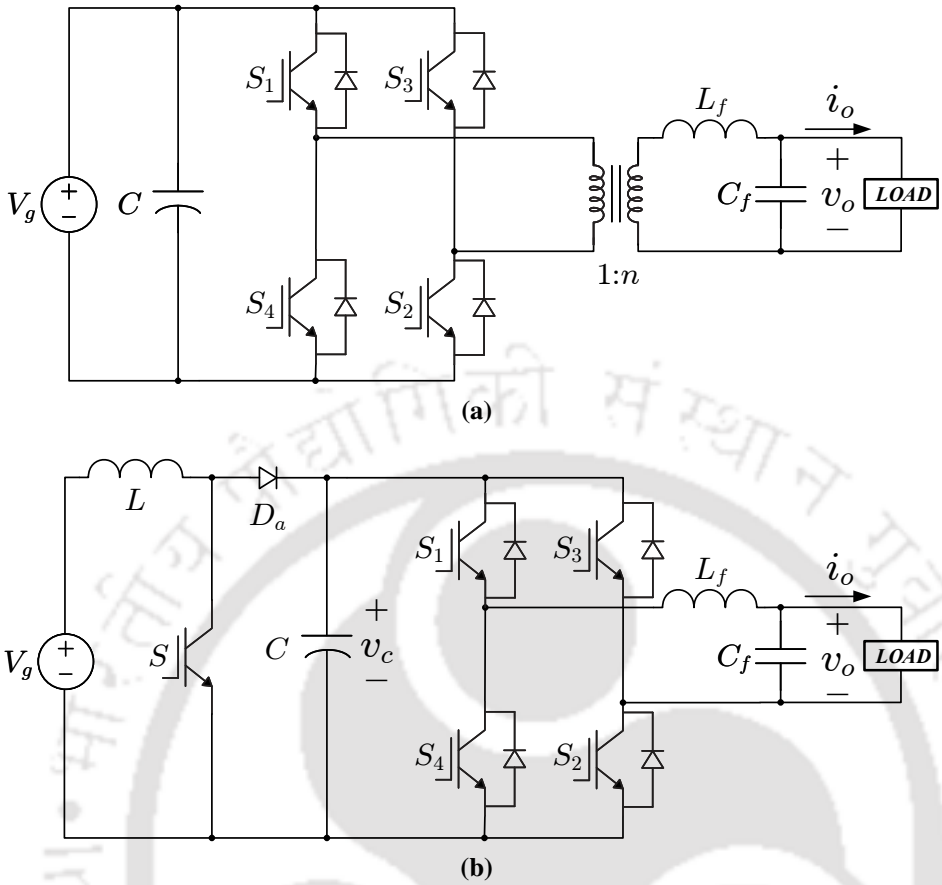


Fig. 1.2 Examples of two-stage system: (a) combination of a VSI and a step-up transformer and (b) combination of a boost converter and a VSI.

shoot-through is a major factor affecting the reliability and overall lifetime of the VSI [3, 4].

(b) To prevent the occurrence of shoot-through, a dead-time is added to the gate pulses of the upper and lower switches of each phase leg of the VSI. However, the implementation of the dead-time introduces a complex circuitry, which causes waveform distortion and other issues [5, 6].

(c) For VSI, the peak ac output voltage is limited below and cannot exceed the dc-link voltage. Although energy and environmental considerations encourage the increased use of the renewable energy sources, these sources generally provide significantly low dc voltages at the VSI input. Therefore, either a step-up transformer should be placed after the VSI, or an additional boost converter ought to be present before the VSI, in

order to boost the output voltage of the renewable sources. But these solutions bring additional issues [7].

(d) In Fig. 1.2(a), a step-up transformer is placed after the inverter output to boost the output voltage of the renewable energy source. Here, to achieve high gain, the turns ratio of the step-up transformer has to be high, which results in a bulky and noisy transformer. As a result, the cost and size of the whole system is increased, and the overall efficiency is hampered [8].

(e) Alternatively, an additional dc-dc boost converter can be employed before the inverter input as shown in Fig. 1.2(b). However, in order to attain very high gain, the conventional boost converters must be operated at a duty ratio (D) close to unity, which indicates that the diode and the output capacitor must be conducted for a very narrow pulsewidth while maintaining a high current [9]. This results in severe reverse recovery of the diode, which increases the conduction loss and creates EMI noise. This issue is exacerbated at high switching frequencies, as the reverse-recovery time of the diode may be longer than the time available during $(1 - D)$ interval. Furthermore, a boost converter can only achieve a gain of 4 to 5 times [10].

In order to overcome the issues in traditional VSI, a family of impedance source inverters (ISIs) are proposed in the literature [11–27]. In [11], the Z-source inverter (ZSI) has been proposed to overcome the conceptual and theoretical barriers and limitations of the VSI, which can boost input dc voltages to achieve better dc-ac gain and can also offer better EMI noise immunity. The three-phase ZSI is proposed in [11], and its single-phase equivalent is illustrated in [12]. As shown in Fig. 1.3, the single-phase ZSI is made up of an X-shaped impedance network that connects the VSI with the dc source. The X-shaped impedance network is composed of two inductors L_1 and L_2, two capacitors C_1 and C_2, and one diode D_a.

However, the typical ZSI architecture has the drawback of having the diode D_a, which disconnects the impedance network from the source. Hence, the input current of the ZSI

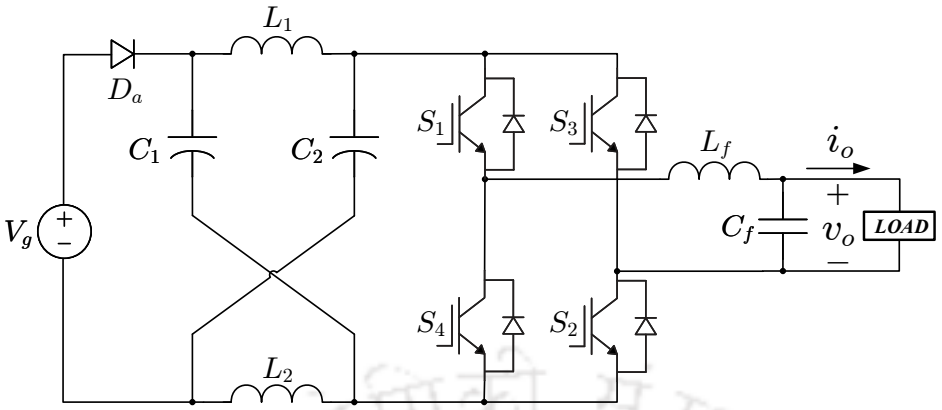


Fig. 1.3 Z-source Inverter (ZSI).

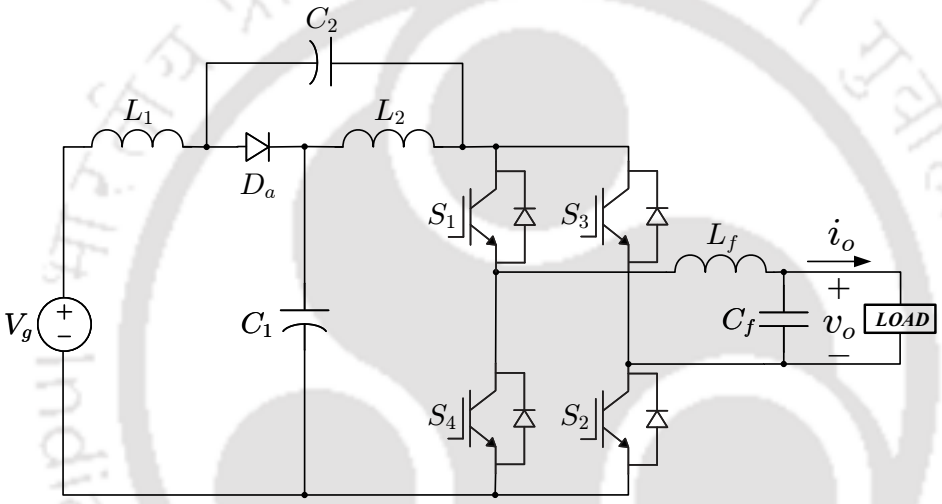


Fig. 1.4 Quasi-Z-source Inverter (qZSI).

becomes discontinuous, which may be undesirable for some sources such as solar cells and fuel cells [28]. Also, the negative terminals of the input source and the dc-link of the inverter are not shared, which may introduce common-mode noise.

In order to obtain additional advantages over the ZSI, four quasi-ZSIs (qZSIs) have been proposed in [13]. A qZSI with continuous input current is shown in Fig. 1.4. The qZSI has lower component rating compared to ZSI as the impedance-source network capacitor voltages are lower than those in case of the ZSI. Unlike ZSI, the negative terminal of the input source and the negative terminal of the dc-link of the qZSI are also connected together, which reduces the common-mode noise in the system. It has one more advantage over the ZSI, i.e., continuous input current owing to the presence of an input inductor.

In literature, significant amount of discussions can be found on the applications of ZSI and qZSI in grid-connected photovoltaic systems [29–32], electric vehicles [33, 34], electric motor drives [35, 36], distributed power generation [37], fuel cell power conversion [38, 39], etc. However, both ZSI and qZSI are vulnerable to the following issues:

(a) The impedance networks of both ZSI and qZSI employ two inductors and two capacitors, which greatly increase the power converter's size and expense lowering its energy density and efficiency. As a result, both architectures may not be appropriate for low power applications where size, weight, and cost are major considerations [26].

(b) Generally, the impedance networks of ZSI and qZSI theoretically require two inductors of equal size and two capacitors of equal size, which is extremely hard to achieve in a hardware setup. Any kind of mismatch in the LC values in the impedance network can result in a dynamic stability problem [40, 41].

Several other impedance-source inverter topologies are derived from the basic principles of ZSI and with a goal of increasing the boost factor, such as Extended-boost qZSI [14], Switched Inductor ZSI/qZSI [15, 16], Enhanced-boost ZSI/qZSI [17–19], etc. However, all of these topologies use quite higher number of inductors and capacitors, which makes them practically unsuitable for low power applications. Furthermore, the single-phase variants of these topologies would be heavily plagued with low-frequency ripples, which will then require large passive elements in a huge quantities impacting power density, cost, efficiency, reliability and lifetime of the overall system.

As a solution, another power converter is proposed in [24], known as Switched Boost Inverter (SBI), shown in Fig. 1.5. The SBI was proposed by preserving the same dynamic states as ZSI but reducing the passive component count by replacing the X-shaped impedance network with an active-front-end (AFE) network. Therefore, the SBI can be termed as an active-front-end impedance-source inverter (AFE-ISI). When compared to the original ZSI, the SBI employs an additional active component and less number of inductors and capacitors, while preserving its operating benefits [21, 23]. Having only one LC pair, the SBI does not

face the dynamic stability problem arising from mismatch in LC values, thereby making it a compact solution. Also, the SBI is capable of supplying both dc and ac loads from a single dc input. As a result, it can realize both the dc-to-dc converter and the dc-to-ac converter in a single stage. This reduces the total size and expense of the system.

However, the gain of the SBI is $(1 - D)$ times that of ZSI and qZSI. As a result, it is not suitable for very high boost inversion. Also, similar to the ZSI, the input current of the SBI is discontinuous because of the diode D_a, which makes it unsuitable for applications involving renewable energy sources.

As a solution, another AFE-ISI topology, called Current-Fed Switched Inverter (CFSI), is proposed in [25], as shown in 1.6(a). Although CFSI has the same number of components as the SBI, the components of the AFE network are rearranged so that the inductor L is connected in series with the input voltage source V_g. Therefore, if a sufficiently large inductor is chosen to provide operation in continuous conduction mode (CCM), the CFSI draws continuous input current from the dc source, which makes it more suitable for renewable energy applications. Also, the change in position of L helps CFSI to continuously charge L resulting in improved gain, which is same as that of ZSI and qZSI. As a result, CFSI does not require extreme duty ratio operation to achieve high voltage boost. Therefore, CFSI combines the gain advantage of ZSI, manages to reduce passive elements like SBI and provides a continuous input current like qZSI. However, the voltage stress on the capacitor is still equal to the dc-link voltage, same as that in SBI.

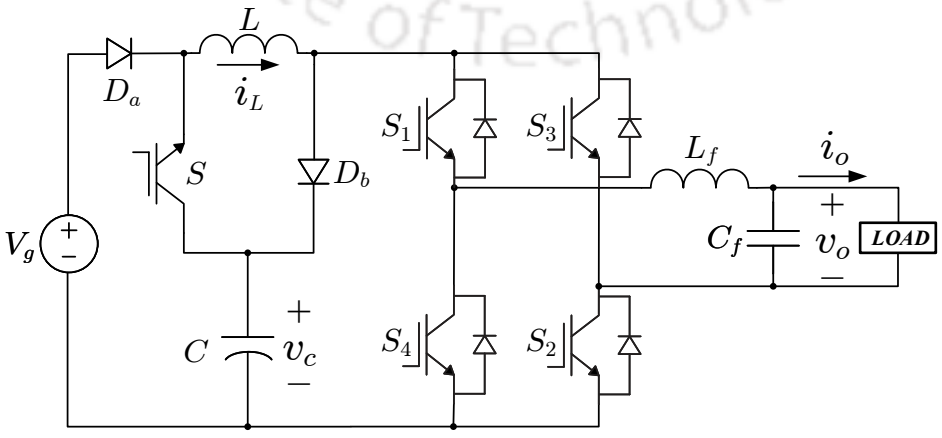


Fig. 1.5 Switched Boost Inverter (SBI).

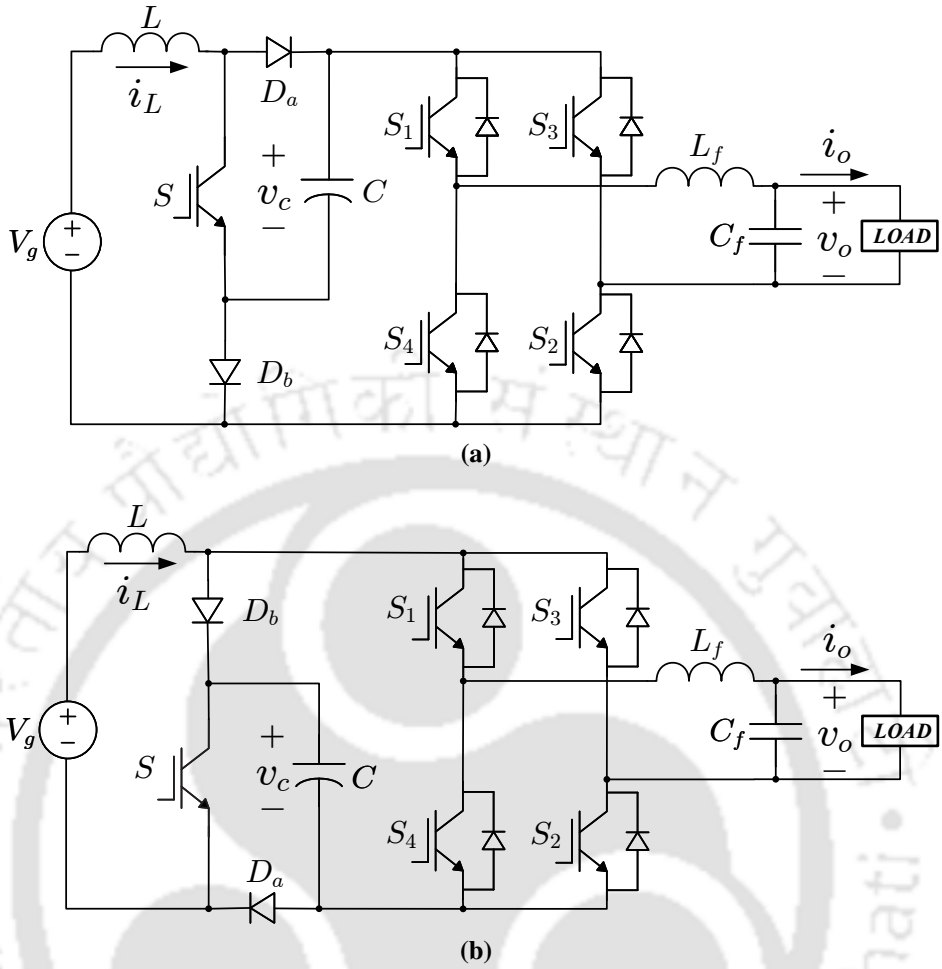


Fig. 1.6 (a) Current-Fed Switched Inverter (CFSI) / Embedded type-2 quasi-SBI (qSBI). (b) Embedded type-1 qSBI.

The CFSI is termed as the embedded type-2 quasi-SBI (qSBI) by M. K. Nguyen et al. in [26], which presents a family of qSBIs. One such inverter is the embedded type-1 qSBI, as shown in 1.6(b). In CFSI, the negative terminal of the input voltage and the negative rail of the inverter bridge share a common point of connection. However, in embedded type-1 qSBI topology, the negative terminal of the input voltage is only connected with the negative rail of the inverter bridge, when the inverter acts as a conventional VSI, and both diodes are forward-biased. However, in the shoot-through state, the switch S is on, and both diodes are reverse-biased. Thus, the capacitor of the active-front-end network occurs across the the negative terminal of the input voltage and the negative rail of the inverter bridge. Because of this voltage difference, the embedded type-1 qSBI might face common-mode noise issues.

This thesis proposes one more AFE-ISI topology, called Reduced-Switch CFSI (RSCFSI). It retains all advantages of SBI and CFSI, while removing one switch. Hence, the proposed inverter can achieve improved efficiency compared to SBI and CFSI. In this thesis, the steady-state analysis of the RSCFSI is illustrated, and the conventional simple boost control-based PWM (SBC-PWM) is modified for RSCFSI. Furthermore, this thesis proposes another PWM strategy, namely Enhanced Boost Control-based PWM (EBC-PWM), which can achieve a higher boost factor and dc-ac voltage gain compared to SBC-PWM. In this thesis, a comparison between RSCFSI and other existing AFE-ISIs is presented to highlight the advantages and limitations of the RSCFSI. The RSCFSI is also implemented in hardware to verify the theoretical analysis with experimental results.

In addition to the drawbacks of single-phase VSI mentioned in pages 1-3, it also suffers due to low-frequency ripple problem in all practical applications, where the input voltage source V_g is not a stiff voltage source [5]. Any system having a single-phase inverter, viz., photovoltaic (PV) system, light-emitting diode (LED) lighting etc. is affected due to low-frequency ripple. Therefore, all single-phase ISIs and AFE-ISIs are plagued with low-frequency ripples. If this low-frequency ripple is not diminished below an engineering tolerance limit, the impedance-source network and active-front-end network components are impacted by the low-frequency ripples, which eventually distorts the output voltage. Moreover, the power from PV array shows oscillation around maximum power point (MPP) reducing efficiency [42]. This ripple results in light flicker in LED lighting applications [43]. If a battery or fuel cell is utilized with single-phase inverter, significant low-frequency current will be going into battery because of very small internal resistance of the battery resulting in overheating [44] or considerable shortening of the lifetime of the fuel cell [45]. The low-frequency ripple of both SBI and RSCFSI is analyzed, which outlines the presence of the double-line frequency ($2\omega_o$) component. In the case of RSCFSI, the low-frequency ripple problem becomes more severe than that of SBI as it contains an additional line frequency (ω_o) component. Based on the analysis, the amount of low-frequency ripple present in the active-front-end network parameters is estimated for both SBI and RSCFSI. A common solution

to reduce the aforementioned low-frequency ripple is to employ bulky passive elements. However, this leads to increased volume, weight and cost affecting power density, efficiency, reliability and lifetime of the system [46]. Based on the low-frequency ripple analysis, the design procedures for the selection of the passive elements of the active-front-end networks of both SBI and RSCFSI are illustrated in this thesis.

Since significantly larger passive components are required to maintain smaller ripples, resulting in poor power density for both SBI and RSCFSI. As an alternative, active power decoupling (APD) based solutions are explored in literature, which are mostly limited to single-phase VSI. Therefore, it remains to be explored for the AFE-ISIs. Although a few APD solutions are also found for the ZSI and qZSI, these solutions cannot be directly applied to the AFE-ISIs owing to their topological differences. As a solution to the low-frequency ripple problem in SBI, this thesis proposes the Active Power Decoupling (APD)-integrated SBI to deflect the low-frequency ripple to an auxiliary capacitor. Three independent APD-integrated SBI topologies are explored and compared, which indicates the boost-type topology is the most advantageous in reducing the low-frequency ripple in the active-front-end network. As a result, smaller passive elements are required in the active-front-end network. In order to properly mitigate the low-frequency ripple for varying ac loads of the SBI and also to avoid overcharging of the auxiliary capacitor, a closed-loop control strategy is developed for the APD-integrated SBI. A hardware prototype is built for the boost-type APD-integrated SBI, and the advantages of APD integration are corroborated by the experimental results.

In the case of the APD-integrated SBI, it is observed the extra switches and passive elements introduce additional losses, which brings down efficiency. Therefore, this thesis explores more efficient alternate solutions for the RSCFSI and further introduces the APD-integrated RSCFSI (APDRSCFSI). Since the low-frequency ripple energy is deflected to an auxiliary capacitor without adding extra switches, the inverter can employ smaller passive elements. It is observed when APDRSCFSI is operated with SBC-PWM, the dc-ac gain of the inverter is lowered. As a solution, EBC-PWM is extended for APDRSCFSI to improve its dc-ac gain. A comparison between RSCFSI and APDRSCFSI with SBC-PWM and EBC-

PWM is also presented in this thesis. The ω_o and $2\omega_o$ ripples in RSCFSI pose additional challenges for the APD integration and corresponding closed-loop controllers. So, this thesis illustrates a closed-loop control strategy, which incorporates dc-ac power conversion as well as APD operation. The APDRSCFSI is also implemented in hardware to verify the theoretical analysis with experimental results.

The remaining part of this chapter is organized as follows: in **Section 1.2**, a brief review of AFE-ISIs and their advantages over ISIs are presented. **Section 1.3** elucidates the low-frequency ripple problem and describes potential solutions found in literature. In **Section 1.4**, the motivation and the objectives of the thesis are illustrated. **Section 1.5** presents the contributions of this thesis are presented. In **Section 1.6**, the organization of the thesis is explained, followed by the conclusion of this chapter in **Section 1.7**.

1.2 REVIEW OF AFE-ISIS

In literature, the active-front-end impedance-source inverters (AFE-ISIs) are explored as alternatives to the VSI and ISIs. Generally, an impedance network is present at the front-end of the ISIs, which is replaced with an active-front-end network in AFE-ISIs. This helps to reduce the number of passive elements in AFE-ISIs, resulting in improved efficiency and power density. The most researched AFE-ISIs are SBI, CFSI and the family of qSBI topologies, which are reviewed in this section.

In [24], the SBI is introduced as an alternative to the VSI and ZSI, which can retain the advantages of the ZSI while reducing the number of passive elements. The circuit diagram of SBI is shown in Fig. 1.5. Similar to the ZSI, the SBI has extra zero states in the form of shoot-through switching states that are prohibited in the conventional VSI. The SBI utilizes shoot-through states to improve dc-link voltage by turning on both upper and lower switches of a phase leg. By effectively leveraging the shoot-through states of the inverter bridge, the SBI has the benefit of stepping up the dc input voltage before the dc-ac power inversion, unlike the conventional VSI. As a result, depending on the situation, the converter's output voltage

may be either greater or less than the input voltage, which accomplishes the functionality of the two-stage system, mentioned in pages 2-3, in a single-stage.

The SBI preserves the same dynamic states as ZSI but reducing the passive component count by replacing the X-shaped impedance network with an active-front-end network. As shown in Fig. 1.5, SBI employs an additional active component and less number of inductors and capacitors, compared to the original ZSI, while preserving its operating benefits [21, 23]. Having only one LC pair, the SBI does not face the dynamic stability problem arising from mismatch in LC values, thereby making it a compact solution.

Moreover, the inverter's dependability is substantially enhanced since any kind of occurrence of shoot-through no longer has the capacity to ruin the circuit. By enabling the shoot-through of the inverter phase leg switches, the SBI has a strong tolerance to EMI noise. Also, the SBI does not require complex dead-time circuitry for the prevention of unwanted shoot-through state used in VSI, which also helps to avoid output waveform distortion caused by the dead-time. As a result, it provides a low-cost, dependable, and high-efficiency single-stage structure for buck and boost power conversion.

Also, the SBI is capable of supplying both dc and ac loads from a single dc input. As a result, it can realize both the dc-to-dc converter and the dc-to-ac converter in a single stage. This reduces the total size and expense of the system.

However, the SBI's main disadvantages are:

(a) The boost factor of SBI is $\left(\frac{1-D}{1-2D}\right)$, and the boost factor of both ZSI and qZSI is $\left(\frac{1}{1-2D}\right)$. Therefore, the dc input voltage boosted by the SBI is $(1-D)$ times that of ZSI and qZSI.

(b) Similar to the ZSI, the input current of SBI is also discontinuous due to the diode D_a.

As a solution, Current-Fed Switched Inverter (CFSI) is proposed in [25], as shown in 1.6(a). CFSI combines the advantages of both ZSI and SBI. Similar to SBI, the CFSI preserves the same dynamic states as ZSI but reduces the passive component count by replacing the X-shaped impedance network with an active-front-end network while keeping the same

component count as the SBI. In CFSI, the input current profile is much improved than that of SBI and ZSI, and a continuous current is drawn from the dc source, similar to that of qZSI. Also, the boost factor of CFSI is $\left(\frac{1}{1-2D}\right)$, same as ZSI and qZSI, which indicates that CFSI has a higher boost factor than SBI. In [26], CFSI is mentioned as a part of the quasi-switched boost inverter (qSBI) family, and termed as the embedded type-2 qSBI. A similar topology, named as Active Switched Capacitor qZSI (ASC-qZSI), is introduced in [47], which is mentioned as the embedded type-1 qSBI in [26], as shown in Fig. 1.6(b).

As the name suggests, both types of embedded qSBI are similar in topological architecture and features. However, there is a drawback of the embedded type-1 qSBI owing to a topological difference, as the negative terminal of the dc source is disconnected by the diode D_b from the negative rail of the inverter bridge. As a result, the dc-link capacitor voltage occurs across the negative terminal of the dc source and the negative rail of the inverter bridge when the shoot-through states take place, and the switch S is turned on while the diodes are reverse-biased. The voltage between the negative terminal of the dc source and the negative rail of the inverter bridge only becomes zero when both diodes are forward-biased during conventional inverter operation. Owing to this voltage difference, the embedded type-1 qSBI may face additional common-mode noises.

Similar to SBI, in qSBIs, the voltage stress of the capacitor of the active-front-end network is equal to the dc-link voltage. To reduce the voltage stress, four qSBIs are presented in [26], which are called dc-linked-type qSBIs, as shown in Fig. 1.7. In these converters, the dc source is inserted between the active-front-end network and the dc-ac power conversion stage. In dc-linked-type qSBI positive bus type-1 and type-2, the input source is inserted between the active-front-end network and the positive terminal of the dc-link, where the positive terminal of the input voltage is shared with the positive rail of the inverter bridge. In dc-linked-type qSBI negative bus type-1 and type-2, the input source is inserted between the active-front-end network and the negative terminal of the dc-link, where the negative terminal of the source voltage is shared with the negative rail of the inverter bridge.

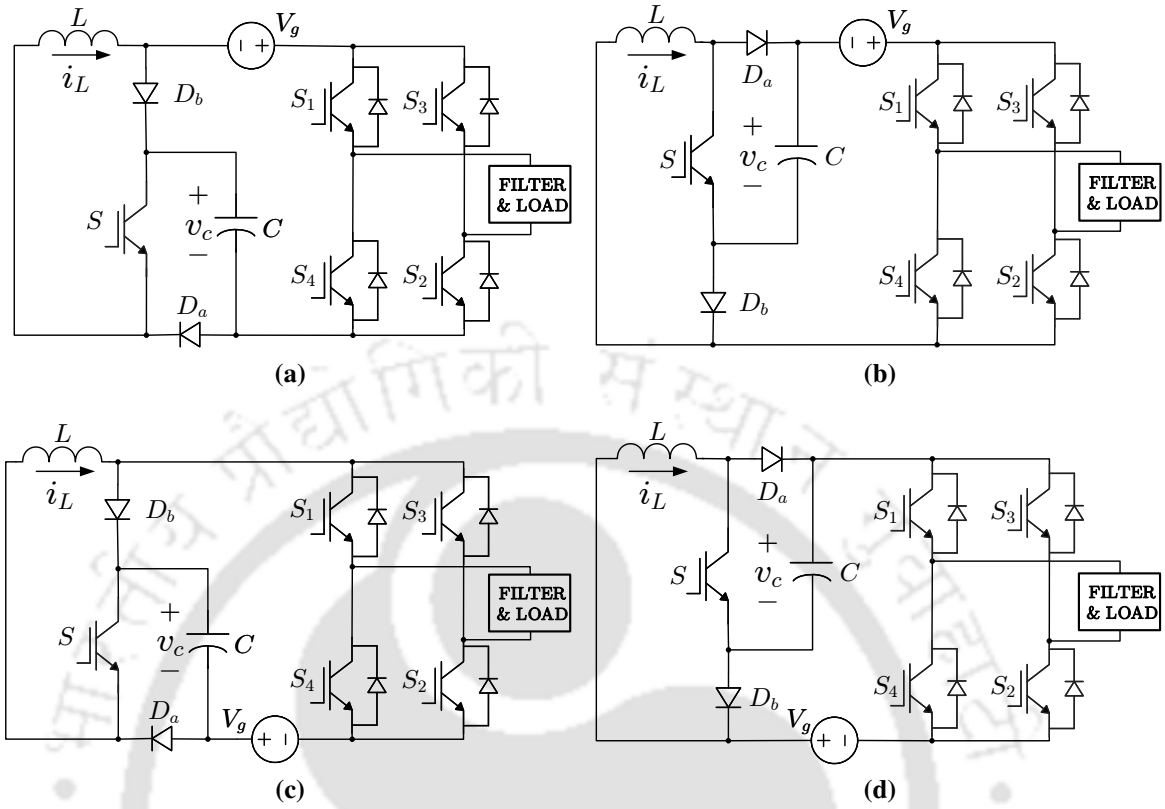


Fig. 1.7 Examples of dc-linked-type qSBIs: (a) positive bus type-1, (b) positive bus type-2, (c) negative bus type-1 and (d) negative bus type-2.

However, the boost factor of the dc-linked-type qSBIs reduces to $\left(\frac{1-D}{1-2D}\right)$, which is same as that of SBI. The dc-linked-type qSBIs, introduced alongside the embedded-type qSBIs, is less favored mainly because of their low voltage gain and high input current ripple [48]. Note that in embedded-type-1 and all dc-linked-type qSBIs, the negative terminals of the input source and the dc-link are not shared because of the diode, which may increase common-mode noises in the overall system.

In literature, the efficiency of AFE-ISIs is also researched. Generally, CFSI and qSBIs are reported to achieve better efficiency compared to qZSI [49, 50]. Several PWM methods are proposed for the qSBIs, which not only improve voltage gain but also better the efficiency [51–53]. In [52, 53], a power loss distribution of various components of the CFSI is presented. Similarly, in [49], a power loss distribution of various components of the embedded type-1 qSBI is exhibited. Generally, it is observed that the switching loss and the conduction loss of the switches are the most significant contributors to the overall power losses. Therefore, in an

effort to improve efficiency by reducing one of the switches, a new topology is derived from CFSI and named as Reduced-Switch CFSI (RSCFSI) in this thesis.

1.3 LOW-FREQUENCY RIPPLE PROBLEM IN AFE-ISIS AND ITS TRADITIONAL SOLUTIONS

The low-frequency ripple in the dc-link severely impacts the operation of the single-phase AFE-ISIs. Similar to a traditional single-phase VSI, the elements of the active-front-end network of the single-phase AFE-ISIs has to endure the low-frequency ripple power generated from the ac load side. So, the dc capacitor voltage and inductor current of the active-front-end network contain low-frequency ripple. In order to prevent distortion of the output voltage of the inverter, this low-frequency ripple ought to be mitigated or at least limited within an engineering tolerant range. Also, any single-phase AFE-ISI-integrated system, e.g., photovoltaic (PV) system, light-emitting diode (LED) lighting, battery, fuel cell, etc. is affected due to low-frequency ripple. The power from PV array shows oscillation around maximum power point (MPP) reducing efficiency [54, 42]. This ripple results in light flicker in LED lighting applications [43]. If a battery is utilized with single-phase AFE-ISIs, high low-frequency current will be going into battery because of very small internal resistance of the battery resulting in overheating [44]. Similarly, using a fuel cell with single-phase AFE-ISIs will significantly reduce the fuel cell's lifespan due to the high low-frequency current flowing into the fuel cell as a result of the fuel cell's low internal resistance [45]. Therefore, it can be observed that there are numerous use cases where suppressing dc-side power oscillation is a priority.

So, it becomes necessary for the inverters to have the ability to process the ripple power and protect the application from receiving an improper signal quality so that the ripple power does not propagate through the converter. In order for the inverter to handle ripple power, it must be able to store it. As a result, the most prevalent approach to eliminate low-frequency ripple is to utilize large capacitor and inductor in the active-front-end network to store the

ripple power. However, this leads to increased volume, weight and cost affecting power density, efficiency, reliability and lifetime of the system [46, 55, 56].

1.3.1 Low-frequency ripple problem

One of the basic requirements of single-phase AFE-ISIs is that the output voltage and/or output current need to be filtered or controlled to be sinusoidal. The expressions of sinusoidal output voltage (v_o) and output current (i_o) can be considered as

$$\begin{aligned} v_o(t) &= \sqrt{2}V_o \sin \omega_o t \\ i_o(t) &= \sqrt{2}I_o \sin(\omega_o t - \varphi) \end{aligned} \tag{1.1}$$

where ω_o is the fundamental frequency, φ is the phase difference between v_o and i_o. Therefore, the output power (p_o) can be obtained as

$$\begin{aligned} p_o(t) &= v_o(t) \cdot i_o(t) \\ &= V_o I_o \cos\varphi - V_o I_o \cos(2\omega_o t - \varphi) \\ &= P_o + p'_r(t) \end{aligned} \tag{1.2}$$

which contains two components: the constant active power (P_o) and the low-frequency ripple power (p'_r). In Fig. 1.5, the input power is coming from the source is constant. In order to balance the input and output power, the low-frequency ripple power must be supplied by the capacitor C and inductor L of the active-front-end network. This results in large voltage ripple on the capacitor and large current ripple on the inductor of the active-front-end network, which can be analyzed with the determination of the ripple energy of single-phase AFE-ISIs. Because p'_r comprises the second harmonic ($2\omega_o$) ripple, the low-frequency ripples of the active-front-end network parameters contain the $2\omega_o$ ripple. As a result, the dc-link voltage has low-frequency ripples. The presence of low-frequency ripple on the dc-link voltage distorts the output voltage.

As a solution, large capacitors and inductors are used in the active-front-end network to facilitate suppression of the low-frequency ripple. Thus, the minimization of the voltage variation in the dc-link are achieved so that output voltage distortion can be prevented. Also, the capacitors help to provide energy storage during hold up time.

In ISIs, the inductors and capacitors of the impedance network are utilized to buffer the ripple power by designing suitable inductance and capacitance [29, 57–59]. In a similar manner, for the qSBI, the passive elements of the active-front-end network are designed in [49]. However, such impedance design is not explored for other AFE-ISIs, in particular for SBI, in the literature. This thesis presents the low-frequency ripple analysis of the SBI. The same analysis is also extended for RSCFSI. Based on the analysis, the design procedures for the passive elements of the active-front-end network are illustrated. It is also shown that if the components are chosen according to the analysis given in this thesis, the low-frequency ripple in SBI and RSCFSI can be limited below the preferred engineering tolerance level.

1.3.2 Large capacitors as a potential solution

The type of capacitors used in AFE-ISIs depends on the various factors [60], viz., required capacitance value, voltage rating, maximum operating temperature, frequency characteristics, cost, size, reliability, etc. Fig. 1.8 illustrates the ranges of capacitance and voltage ratings of various types of capacitors for power electronics applications [61]. There are two types of electrolytic capacitors: aluminum and solid tantalum. Aluminum electrolytic capacitors can be used in AFE-ISIs for applications of nearly 1 kV while providing a high capacitance value. Solid tantalum capacitors are used primarily for low dc voltage applications below 100 V. Plastic film and ceramic capacitors can also be used in AFE-ISIs. However, they cannot achieve a high capacitance value. The double-layer capacitors are unsuitable for AFE-ISIs because their maximum achievable voltage rating is quite low despite having a very high capacitance value.

The three types of capacitors, electrolytic, film and ceramic capacitors, which are suitable for AFE-ISIs, exhibit specific advantages and shortcomings, as shown in Table 1.1 [62].

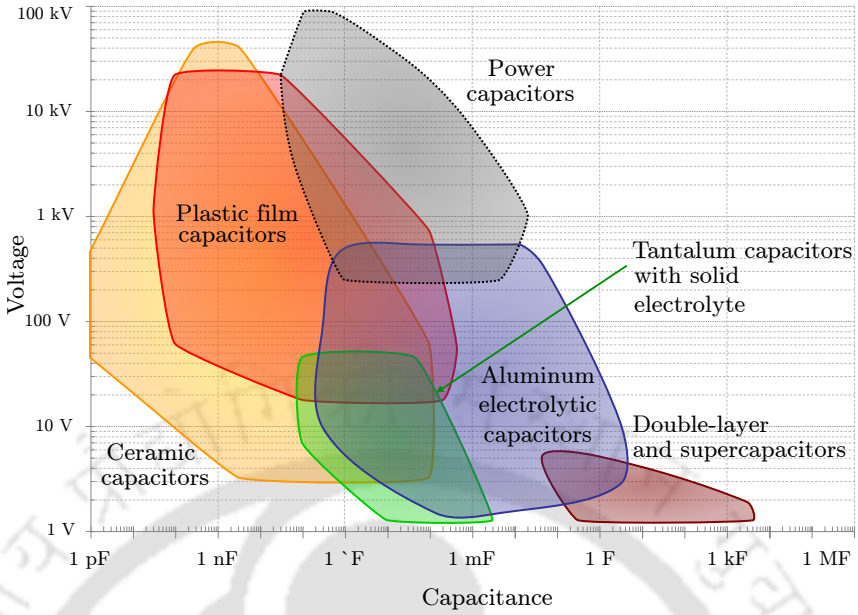


Fig. 1.8 Application of different types of capacitors [61].

Electrolytic capacitors could achieve the highest energy density and lowest cost per joule but with relatively high ESRs, low ripple current ratings, and wear-out issues due to the evaporation of electrolytes. Film capacitors provide a well-balanced performance for high-voltage applications (e.g., above 500 V) in terms of cost and ESR, capacitance, ripple current, and reliability. Nevertheless, they have the shortcomings of large volume and moderate upper operating temperature. Ceramic capacitors have a smaller size, wider frequency range, and higher operating temperatures of up to 200^{o}C. However, they suffer from higher costs and mechanical sensitivity.

All of these three types of capacitors can fail due to intrinsic and extrinsic factors, such as design defects, material wear-out, operating temperature, voltage, current, moisture, mechanical stress, and so on. Generally, the failures can be divided into catastrophic failures due to single-event overstress and wear-out failures due to the long-term degradation of capacitors [62]. The most important reliability feature of film capacitors is their self-healing capability. Initial dielectric breakdowns (e.g., due to overvoltage) at local weak points will be cleared, and the capacitor will regain its full ability except for a negligible capacitance reduction. With the increase of these isolated weak points, the capacitance of the capacitor is gradually reduced to reach the end-of-life.

Table 1.1 Performance comparisons of three types of capacitors [62]

Attributes	Electrolytic	Film	Ceramic
Capacitance	+++	++	+
Voltage	++	+++	+
Ripple Current	+	+++	+++
Equivalent Series Resistance	+	+++	+++
Dissipation Factor	+	+++	+++
Frequency Range	+	++	+++
Capacitor Stability	++	+++	+
Overvoltage capability	++	+++	+
Temperature Range	++	+	+++
Energy density	+++	+	++
Reliability under stresses	+	+++	+++
Cost per joule	+++	++	+

+++ Superior ++ Intermediate + Inferior

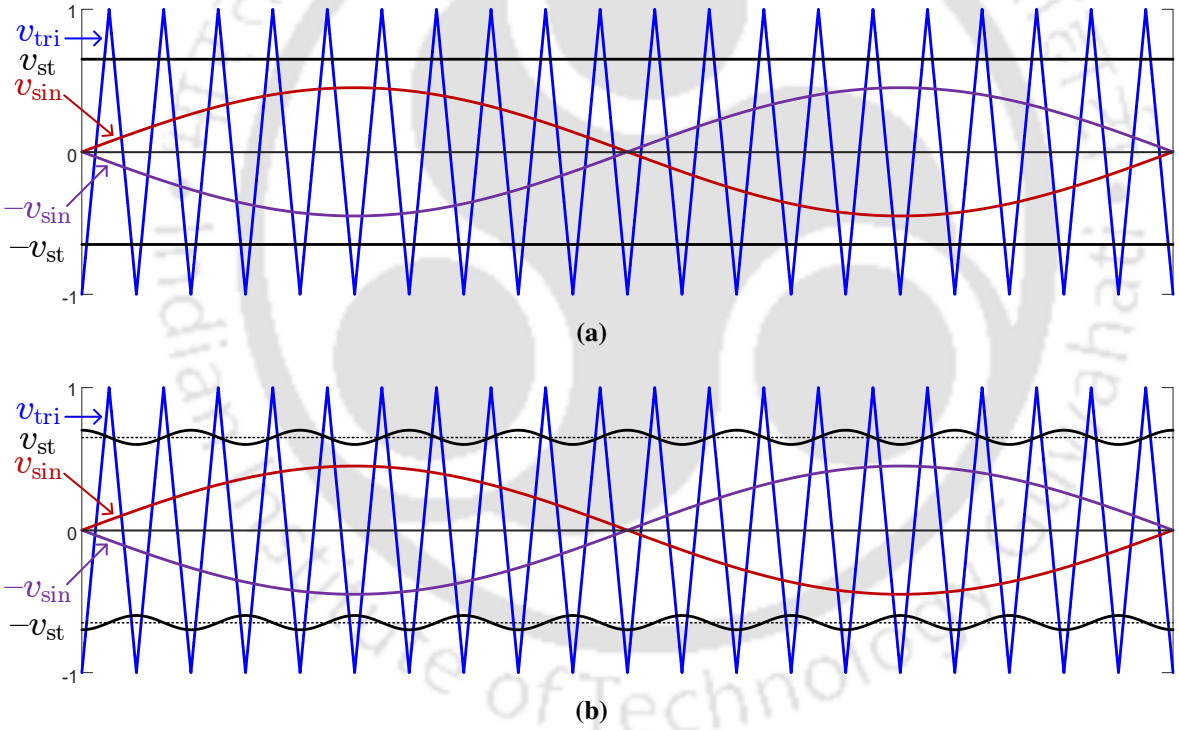


Fig. 1.9 Low-frequency ripple reduction using PWM strategies: (a) simple boost control-based PWM (SBC-PWM) strategy for ISIs and (b) modified modulation signals in SBC-PWM.

The total lifespan of the system is impeded because electrolytic dc capacitors are commonly employed in AFE-ISIs to minimize low-frequency ripples. The greater the amount of capacitors, the worse the system dependability. As a result, ISIs with a large number of capacitors are regarded unreliable for single-phase applications.

1.3.3 Other existing solutions found in literature

Although the solution of employing large passive elements is simple and straightforward, the designed value of capacitances and inductances turned out to be significantly large, which increases the volume, weight, and cost of single-phase AFE-ISIs. As a solution, another different kind of approach to mitigate low-frequency ripples is explored in literature, which is illustrated in Fig. 1.9. The modulation and carrier signals of the conventional simple boost control-based pulse-width modulation (SBC-PWM), employed in ISIs, are shown in Fig. 1.9(a), where the shoot-through signals are generated using the constant voltages $\pm v_{\text{st}}$. In Fig. 1.9(b), $\pm v_{\text{st}}$ are modified to contain the low-frequency ripples while generating the shoot-through signals to damp the low-frequency ripples of capacitor voltages and inductor currents of the ISIs. This approach can be executed in open-loop [30, 31] and in closed-loop [32, 63] without needing any extra hardware components. In ISIs, it is observed that a reduction in passive elements is achieved, but the values are still large. Although a similar solution is explored for the CFSI in [64], such kind of solutions are not explored for other AFE-ISIs in the literature. In CFSI, this approach can only reduce the input inductor size, and the capacitor of the active-front-end network still remains significantly large.

In literature, a hybrid design solution composed of both electrolytic and film capacitors instead of using only electrolytic capacitors is proposed [65], as illustrated in Fig. 1.10(a). A dc-link composed of a 40 mF electrolytic capacitor bank and a 2 mF film capacitor is designed for a 250 kW inverter by taking advantage of their different frequency characteristics. By adopting this solution, the reliability of the capacitor bank is to be improved due to reduced current stresses.

Another research direction is to reduce the energy storage requirement in the dc-link so that electrolytic capacitors could be replaced by film capacitors to achieve a higher level of reliability without considerably increasing the cost and volume. For example, the concept of Fig. 1.10(b) is to synchronize the current i_{DC1} and i_{DC2} by an additional control scheme to reduce the ripple current flowing through the dc-link capacitor [66]. However, this method is not generalized, and the control strategy changes with changes in the connected converters.

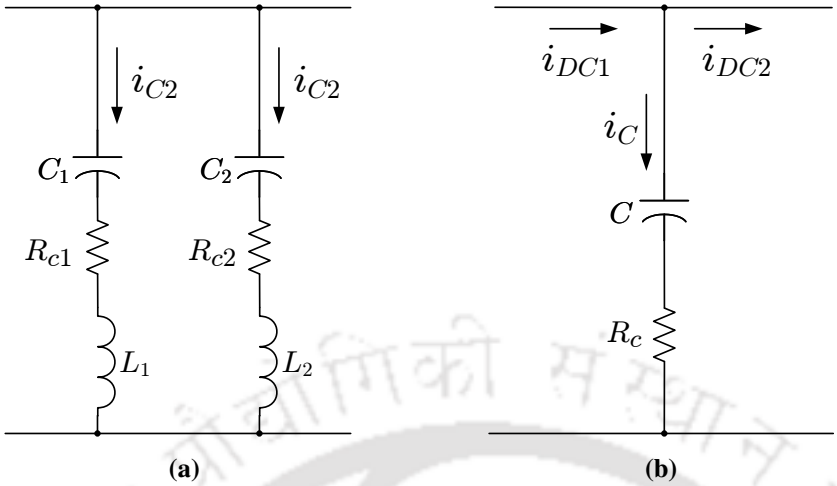


Fig. 1.10 Some types of capacitive dc-link design solutions [65, 66]: (a) hybrid dc-link bank design and (b) by an additional control scheme.

In recent times, more research efforts have been put in to find generalized solutions so that more reliable film capacitors can replace their electrolytic counterparts. As a more generalized solution, Active power decoupling (APD) networks are explored in the literature and are discussed in the following section.

1.4 ACTIVE POWER DECOUPLING NETWORKS

The APD networks are integrated with the converters and utilize additional energy storage components, such as capacitors or inductors, to deflect and store the low-frequency ripple energy from the dc-link so that the size of the dc-link capacitor in VSI or the size of the passive elements of the impedance-source network in ISIs can be significantly lowered [67–99]. Generally, the capacitive energy storage has been paid more attention due to the factors such as volume and cost compared to the inductive energy storage. So, in this literature survey, only the capacitive APD networks are explored. The APD topologies are divided into two categories: (a) independent and (b) dependent.

1.4.1 Operating principles of APD

In Section 1.3, the output power of the VSI contains a constant and a ripple part, according to (1.2). The schematic diagram of an APD circuit with a VSI is shown in Fig. 1.11(a). Note

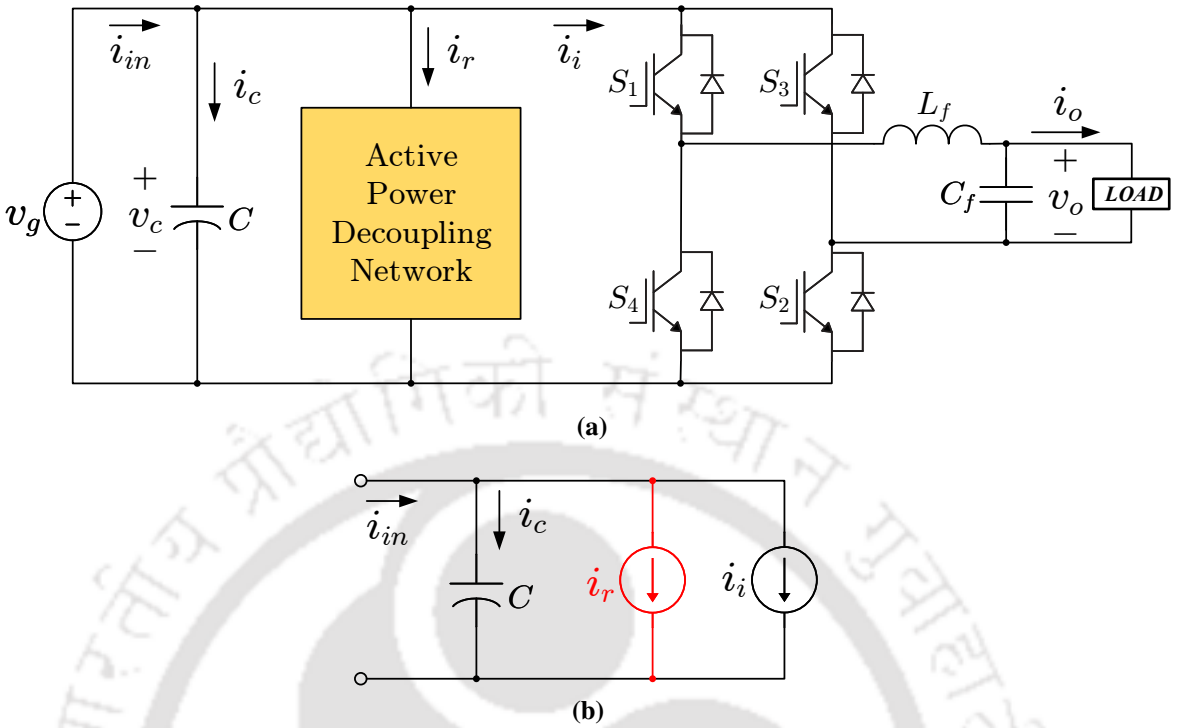


Fig. 1.11 Voltage source converter with an APD circuit [67]: (a) schematic diagram and (b) equivalent circuit.

that the input voltage is denoted by v_g indicating that it is not a stiff source. When the APD circuit is disabled, the input power of the inverter is

$$p_i(t) = v_g(t) \cdot i_{in}(t) = v_c(t) \cdot i_i(t) \tag{1.3}$$

where v_c is the dc-link voltage of the VSI. For simplicity, the effects of power losses and input filters are neglected. According to power balance, using (1.2), one can write

$$p_i(t) = p_o(t) = P_o + p'_r(t) \tag{1.4}$$

Thus, the current drawn by the inverter bridge, i_i, is expressed as follows:

$$i_i(t) = \frac{P_o}{V_c} + \frac{p'_r(t)}{V_c} = \frac{V_o I_o}{V_c} \cos\varphi + \frac{V_o I_o}{2V_c} \cos(2\omega_o t - \varphi) \tag{1.5}$$

where V_c is the average value of v_c. In (1.5), it is assumed that $v_c \approx V_c$. Note that i_i has a dc component and a second harmonic component.

Fig. 1.11(b) shows the equivalent circuit diagram. When the APD network is not active, the dynamic equation of the dc-link is

$$\begin{aligned} i_c(t) = C \cdot \frac{dv_c(t)}{dt} &= i_{in}(t) - i_i(t) \\ \implies \frac{dv_c(t)}{dt} &= \frac{1}{C} \cdot \{i_{in}(t) - i_i(t)\} \end{aligned} \tag{1.6}$$

which indicates that in order to minimize the amount of voltage fluctuations in the dc-link voltage, a significantly high value of C is needed. Therefore, the dc-link capacitor of the VSI is required to be large, as it is utilized as the low-frequency ripple energy storage devices.

When the APD network shown in Fig. 1.11(a) is activated, its equivalent circuit can be drawn as shown in Fig. 1.11(b), and the dynamic equation of the dc-link is

$$i_c(t) = C \cdot \frac{dv_c(t)}{dt} = i_{in}(t) - i_i(t) - i_r(t) \tag{1.7}$$

where i_r is the ripple current drawn by the APD network. In (1.7), if i_r becomes equal to the ripple part of i_i, one can write

$$\begin{aligned} \frac{dv_c(t)}{dt} &= \frac{1}{C} \cdot \left\{ i_{in}(t) - \frac{V_o I_o}{v_c} \cos\varphi \right\} \\ i_r(t) &= \frac{V_o I_o}{2V_c} \cos(2\omega_o t - \varphi) \end{aligned} \tag{1.8}$$

Thus, the low-frequency ripple arising due to the pulsating output power is diminished, and the goal of the active power decoupling will come true. Since a large fluctuation range is allowed in the energy storage component in the APD network, a much smaller energy storage device is required in the dc-link [67, 68].

1.4.2 Independent APD topologies

As the name suggests, in the independent decoupling topologies, the single-phase inverters and the APD networks operate independently. Usually, the APD network is connected to the dc-link of the single-phase inverters in parallel or series. The basic idea of the parallel decou-

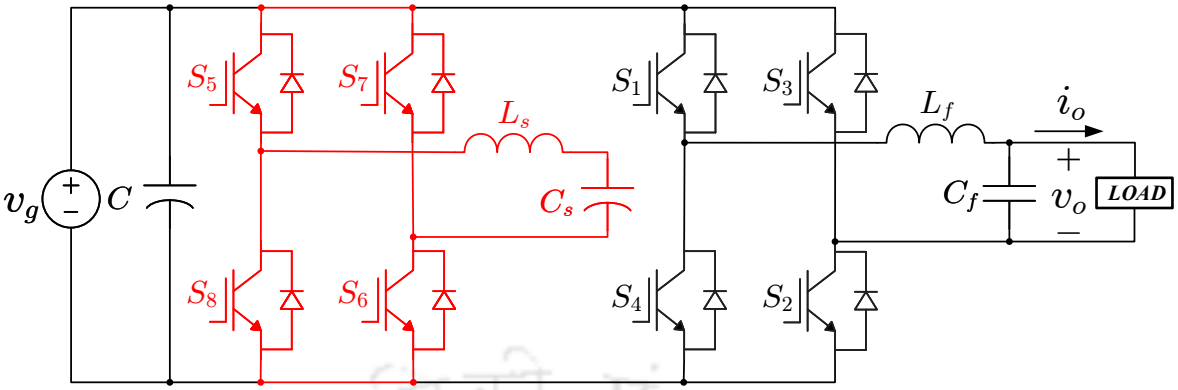


Fig. 1.12 Single-phase VSI with full-bridge APD network connected in parallel [69–72].

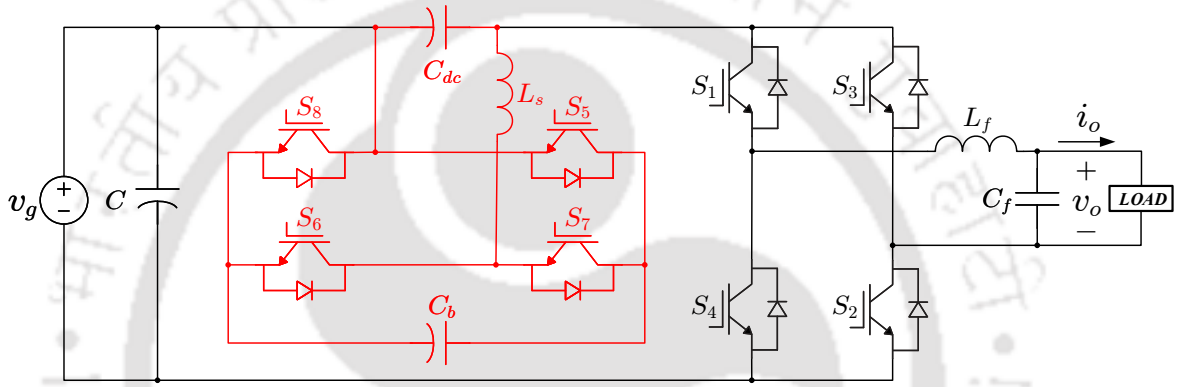


Fig. 1.13 Single-phase VSI with full-bridge APD network connected in series [73–76].

pling concept is to inject compensation current to the coupling point, preventing the ripple current from flowing into the dc capacitor. Similarly, the basic idea of the series decoupling concept is to inject the compensation voltage in series to mitigate dc-link voltage ripple. The single-phase inverter is responsible for the regulation of the dc-link voltage/current, and the APD network's task is to absorb the ripple power. The introduction of the additional APD network will not change the operating point of the original single-phase inverter. Meanwhile, the control methods and modulation strategies for the original single-phase inverter and the APD network can be designed independently. Some of the existing independent APD networks are briefly reviewed in the following paragraphs.

Fig. 1.12 shows a single-phase VSI with the full-bridge APD network, which is connected in parallel with the dc link [69–72]. The APD network consists of an energy storage capacitor C_s, an auxiliary inductor L_s, and a full-bridge power module with switches S_5-S_8. In this circuit, the full-bridge power module regulates the voltage on the capacitor C_s in such a way

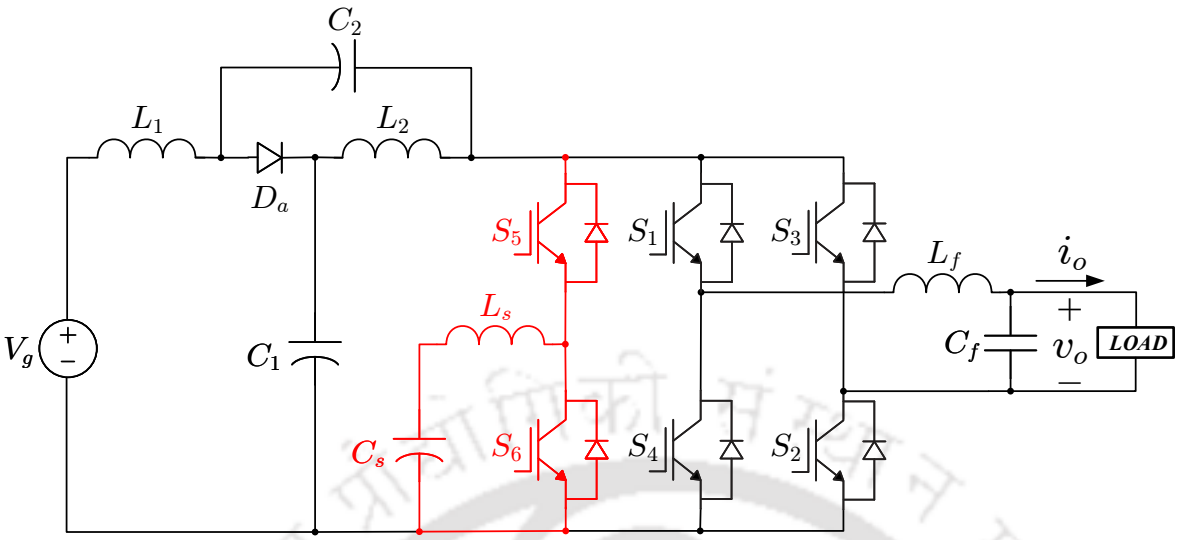


Fig. 1.14 Single-phase qZSI with buck-type APD network [78–80].

that the power flow cancels out the low-frequency. The purpose of the inductor L_s just to smooth the switching frequency. Thus, L_s can be small as it is not utilized as a energy storage device. The APD network has low voltage stress but may need a capacitor with relatively large capacitance. The peak capacitor voltage of C_s may be determined by the design, and as a result, the capacitor value can be made smaller. S. Harb et al., 2013, studied and further developed the ripple decoupling concept above for PV system with isolated transformer cases [72]. Another full-bridge APD network, as shown in Fig. 1.13, can be connected in series with the dc-link capacitor [73–76]. The APD network, which is a capacitor-supported full-bridge power module without an external dc source, is connected between the positive terminal of the dc-link and the positive rail of the inverter bridge. The APD network generates an ac voltage that counteracts the ripple voltage on the dc-link. Thus, the input of the grid-connected inverter is a dc voltage equal to the average value of the voltage v_c, i.e., devoid of low-frequency ripple, across the dc-link capacitor C. While the APD network has to suffer high voltage stress but only needs a capacitor with relatively small capacitance. Note that in both full-bridge APD networks, the presence of four additional switches impacts overall system efficiency [67, 68].

M. Saito et al., 2003, proposed the single-phase VSI with the buck-type APD network in [77]. The buck-type APD network is also integrated with qZSI in [78–80], as shown in Fig. 1.14. The APD network consists of an auxiliary capacitor C_s, an auxiliary inductor L_s,

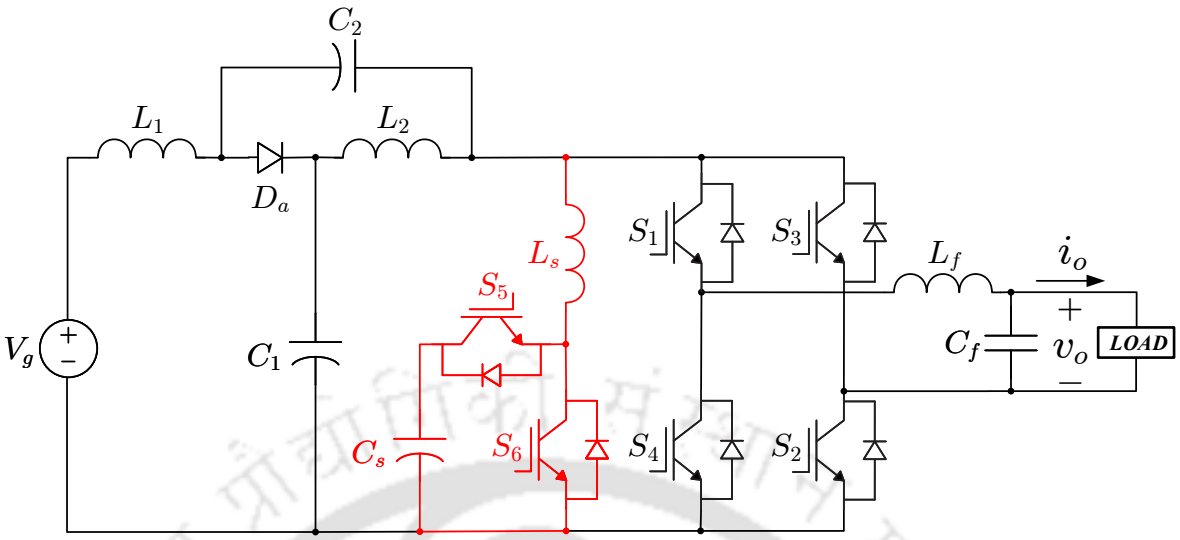


Fig. 1.15 Single-phase qZSI with boost-type APD network [89].

and a half-bridge power module containing two additional switches S_5 and S_6. The auxiliary capacitor C_s is utilized as the energy storage component, and the auxiliary inductor L_s is employed to transfer the ripple energy between the auxiliary capacitor and the dc-link. The inverter bridge is still in charge of regulating the dc-link voltage, whilst the APD network is in charge of regulating the ripple power that originates from the ac side. The auxiliary capacitor voltage should be lower than the dc-link voltage, which makes it suitable for cases where the dc-link voltage is relatively high. The APD network has been further investigated in terms of operating principles, operational modes and control strategies in [81, 82].

The integration of the boost-type APD network with the single-phase VSI is well-studied [83–88]. The boost-type APD network is also integrated with the qZSI in [89], as illustrated in Fig. 1.15. The components of the buck-type APD network are reorganized to obtain the boost-type APD network. Similar to the buck-type APD network, C_s serves as the energy storage element, while L_s is used to facilitate the transfer of ripple energy between the auxiliary capacitor and the dc-link. The responsibility of controlling the dc-link voltage lies with the inverter bridge, while the APD network is responsible for compensating the low-frequency ripple power. It should be noted that the voltage of the auxiliary capacitor must be adjusted to a level that exceeds the voltage of the dc-link. This characteristic makes it particularly suitable for situations where the dc-link voltage is relatively low. The boost-type bidirectional

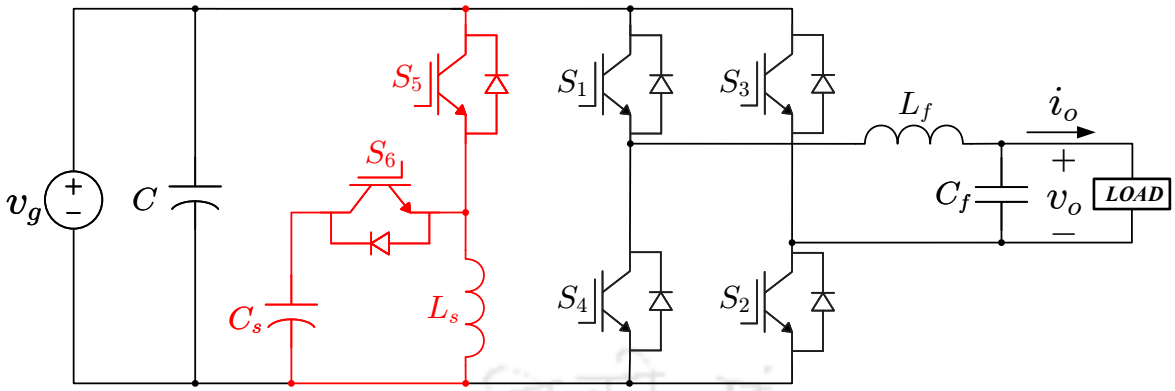


Fig. 1.16 Single-phase VSI with buck-boost-type APD network [90].

power converter has the capability to draw a continuous input current. Therefore, in contrast to the buck-type APD network, the boost-type APD network has the capability to provide a continuous compensating current to the dc-link.

In buck-type or boost-type APD network, the auxiliary capacitor voltage is limited to be either lower or higher than the dc-link voltage. This limitation can be relaxed by using the buck-boost-type APD network shown in Fig. 1.16. This widens the potential applications of the APD network [90]. The components of the buck-type APD network are reorganized to obtain the buck-boost-type APD network, and its functionality is similar to buck-type and boost-type APD network. However, the drawbacks are reduced efficiency and increased volume of the auxiliary inductor L_s. As the injected current is discontinuous, this APD network is not an option for high power applications.

1.4.3 Dependent APD topologies

When an independent APD network is integrated with any single-phase inverter, the introduction of extra active switches in the circuit results in more switching loss. Hence, the overall efficiency of the system is reduced. The total device rating and weight of the system are also increased without any additional increase in power transfer, meaning the system power density is poorer. As a solution, the dependent APD networks are explored in the literature. In dependent APD networks, the APD network can share power semiconductor devices with the original converter partially or fully. The shared bridge leg has to undertake

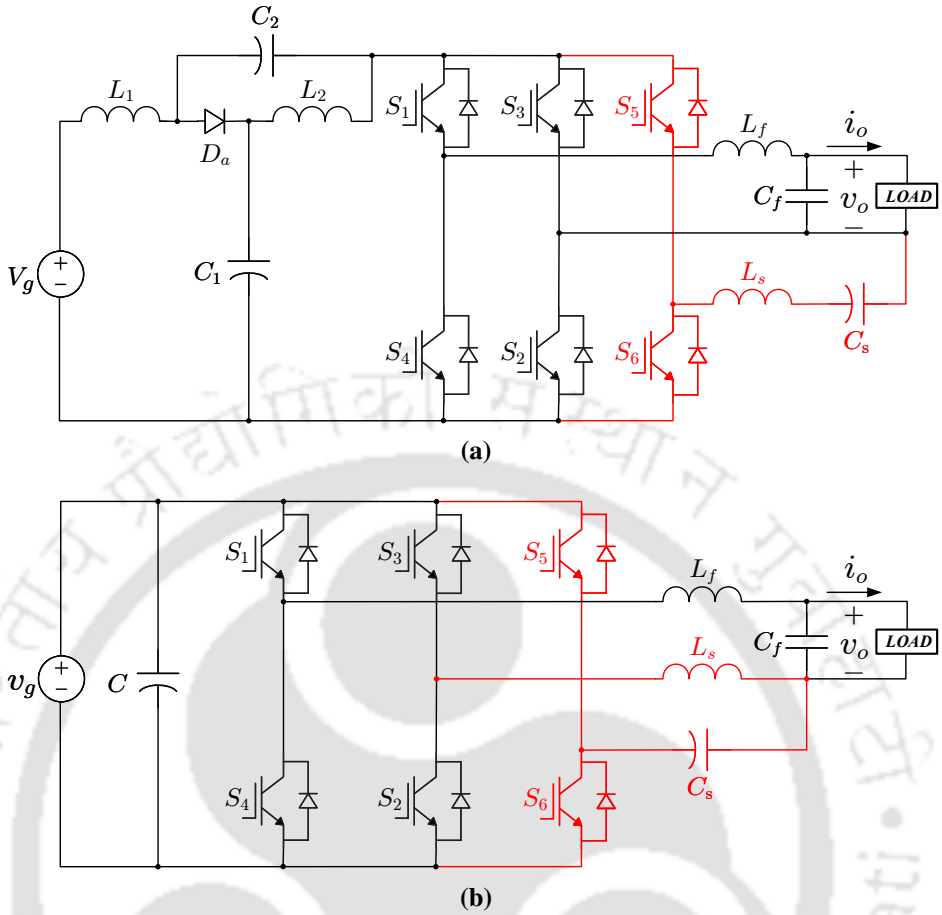


Fig. 1.17 Dependent APD network based on Fig. 1.12 [94]: (a) integrated with single-phase qZSI [95] and (b) modified version with single-phase VSI [96].

two tasks simultaneously: dc-ac power conversion and ripple power buffering. The obvious advantages are better power density and increased efficiency due to fewer active switches compared to the independent topologies. However, there are also some demerits. Some of the existing dependent APD networks are reviewed in the following paragraphs.

In [94], a dependent APD network has been derived from the converter shown in Fig. 1.12. In [95], the same APD network is integrated with the single-phase qZSI, as shown in Fig. 1.17(a). The middle bridge leg, consisting of S_3-S_2, is shared by the original converter and the APD network. As the auxiliary inductor L_s is only utilized to smooth high-frequency, it can be taken quite small so that the voltage across it can be neglected. Thus, another configuration, shown in Fig. 1.17(b), can be obtained by a trivial modification [96]. However, in Fig. 1.17(b), the output current dynamics are coupled with the voltage across the energy storage capacitor C_s, which complicates controller design. Although two active switches are

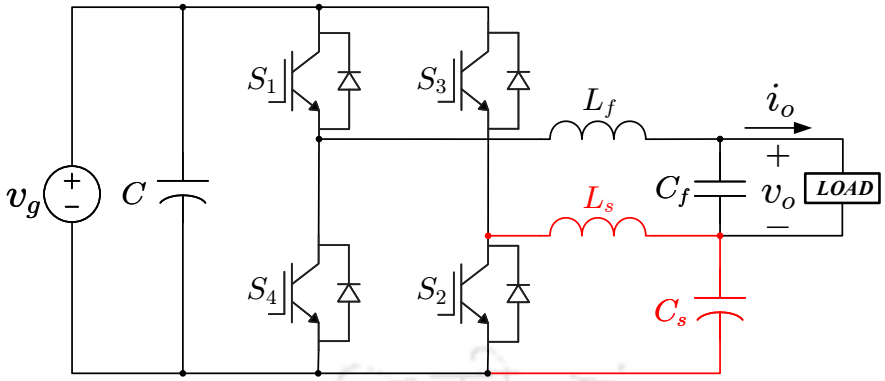


Fig. 1.18 Dependent APD network based on Fig. 1.14.

saved, smaller operating range of the dc-link voltage and higher voltage stresses are some of the disadvantages.

Fig. 1.18 shows a dependent APD network derived from the converter in Fig. 1.14 [98, 99]. This decoupling topology achieves a significant minimization of switches as no additional switches are added. In [99], an automatic power decoupling control concept is applied, which significantly improves the transient performances of the system, and the computational complexity of the controller can be simplified. However, in this APD network, the output voltage becomes restricted.

Thus, it can be observed that a lot of research has been carried out to solve the low-frequency ripple problem by integrating APD topologies with VSI and ISIs. However, the application of APD topologies to the single-phase AFE-ISIs, in particular to SBI and RSCFSI, is not explored in literature. In this thesis, the low-frequency ripple problem of single-phase SBI is mitigated by integration of independent APD networks. Furthermore, a dependent APD-integrated RSCFSI is proposed in this thesis to mitigate the low-frequency ripples of RSCFSI.

1.5 RESEARCH MOTIVATION AND OBJECTIVES OF THE THESIS

As discussed in Section 1.2, several AFE-ISIs are proposed in the literature as an alternative to the conventional VSI. The AFE-ISIs can operate in a wide range of voltages and protect the inverter switches against shoot-through. Among AFE-ISIs, SBI reduces passive

component count and achieves better efficiency than ZSI and qZSI. However, the application of SBI is restricted because of its lower voltage gain. Also, the input current profile of SBI is discontinuous, which makes it less appropriate for several applications. The CFSI can solve the problems of SBI as it improves voltage gain and provides a continuous input current. In the literature, the efficiency analysis of AFE-ISIs reveals that switching and conduction loss of the switches are the most significant contributors to the overall power losses. Therefore, the efficiency improvement of AFE-ISIs via topological modifications can be explored.

As discussed in Section 1.3, in the single-phase AFE-ISIs, a low-frequency ripple power is generated from the ac load side. Since the input power is coming from the dc source is constant, to balance the input and output power, the passive elements of the active-front-end network must supply the low-frequency ripple power. On the dc side, this mismatch in power results in a large voltage ripple on the capacitor and a large current ripple on the inductor. In order to prevent distortion of the output voltage of the inverter, this low-frequency ripple ought to be mitigated or at least limited within an engineering tolerant range. The low-frequency ripple analysis and the design of passive elements of the active-front-end network for low-frequency ripple mitigation for the single-phase AFE-ISIs, in particular for SBI, are not researched in the literature.

The commonly employed solution to reduce low-frequency ripple is to use a bulky capacitor in the dc-link. As large capacitors, electrolytic capacitors are conventionally utilized due to their availability and cost, but they have a limited lifetime, which affects system reliability. As a solution to the low-frequency ripple problem, the APD networks have been explored in literature, as discussed in Section 1.4. The APD networks are kept in parallel to the dc-link and utilize additional energy storage devices to store the ripple energy of the dc-link, thereby reducing the size of the dc-link capacitor in VSI or the size of the passive elements of the impedance-source network in ISIs. A lot of research has been carried out to mitigate the low-frequency ripple problem by integrating APD networks with VSI and ISIs. However, the application of APD networks to the single-phase AFE-ISIs, in particular for SBI, is not explored in the literature.

Based on the above research motivations, the objectives of the thesis are listed as follows:

(1) To perform the low-frequency ripple analysis of the single-phase SBI, and to formulate a procedure to design suitable capacitance and inductance for the active-front-end network to achieve minimization of the low-frequency ripple.

(2) To derive an APD-integrated single-phase SBI so that low-frequency ripple can be mitigated and overall system lifetime can be improved.

(3) To derive an AFE-ISI topology from SBI achieving better voltage gain, continuous input current and better efficiency than SBI.

(4) To propose a PWM strategy for the derived topology achieving better voltage gain.

(5) To perform the low-frequency ripple analysis of the proposed single-phase AFE-ISI topology, and to formulate a procedure to design suitable capacitance and inductance for the active-front-end network to achieve minimization of the low-frequency ripple.

(6) To integrate an APD topology with the proposed topology mitigating low-frequency ripple and improving overall system lifetime.

(7) To perform a detailed comparison of single-phase SBI with and without APD, the proposed topology with existing AFE-ISIs, and the proposed topology with and without APD.

1.6 CONTRIBUTIONS OF THE THESIS

Based on the objectives listed in Section 1.5, the contributions of the thesis are listed below:

(1) The low-frequency ripple of single-phase SBI is analyzed. Based on the analysis, the amount of low-frequency ripple present in the dc-link capacitor voltage and inductor current is estimated for the SBI. When the information about the low-frequency ripple of the active-front-end network parameters is combined with the estimated high-frequency

ripple, a selection procedure for the passive elements is formulated so that both low- and high-frequency ripple is minimized.

(2) The APD-integrated single-phase SBI is proposed so that low-frequency ripple is minimized without requiring large passive elements. As a result, the electrolytic capacitors is replaced with film capacitors and overall system lifetime is improved. A comparative analysis of the SBI with the APD-integrated SBI is also presented to point out the advantages and disadvantages of the proposed topology.

(3) An AFE-ISI topology, named as Reduced-Switch Current-Fed Switched Inverter (RSCFSI), is derived from SBI and CFSI. The RSCFSI can achieve better voltage gain, continuous input current and better efficiency than SBI. A comparative analysis of RSCFSI with other AFE-ISIs is presented to highlight its advantage in terms of efficiency.

(4) The Simple Boost Control-based PWM (SBC-PWM) is modified and extended for the RSCFSI. Another PWM strategy is also proposed for the RSCFSI, known as Enhanced Boost Control-based PWM (EBC-PWM), which can help produce higher voltage gain.

(5) The low-frequency ripple analysis is extended for the single-phase RSCFSI. Based on the analysis, the amount of low-frequency ripple present in the active-front-end network parameters is estimated for RSCFSI, and a selection procedure for the passive elements of the active-front-end network is formulated.

(6) The APD-integrated RSCFSI (APDRSCFSI) is also proposed mitigating low-frequency ripple and improving overall system lifetime. A comparative analysis of the RSCFSI with the APDRSCFSI is also presented to point out the advantages and disadvantages of the proposed topology.

(7) All of the above contributions are implemented in hardware, and the experimental validations are performed for all of the proposed topologies and PWM strategies.

1.7 ORGANIZATION OF THE THESIS

The thesis is organized into five chapters. **Chapter 1** presents a background of the thesis and a brief review of the single-phase AFE-ISIs. Next, a discussion about inherent low-frequency ripple issues of single-phase AFE-ISIs is demonstrated. The motivation is presented to fill the research gaps found in the literature survey about the AFE-ISIs and the low-frequency ripple problem of the AFE-ISIs. Based on the motivation, a set of objectives is established. The organization of the thesis is given at the end of Chapter 1.

In **Chapter 2**, a brief introduction to single-phase SBI is illustrated, and its steady-state analysis is presented. The low-frequency ripple of SBI is analyzed. Based on the analysis, the amount of low-frequency ripple present in the active-front-end network parameters is estimated for the SBI, and a selection procedure for the passive elements of the active-front-end network is formulated. As a solution to the low-frequency ripple problem, the integration of the single-phase SBI with an independent APD topology is proposed to deflect the low-frequency ripple to an auxiliary capacitor. Three independent APD topologies are explored and compared to select the appropriate topology. Apart from the auxiliary capacitor, the APD topology contains two switches and one auxiliary inductor. The passive element selection procedure is modified for the active-front-end network, and the same is also extended to the passive elements of the APD topology. A comparative analysis of the SBI with the APD-integrated SBI is also presented to point out the advantages and disadvantages of the proposed topology. In order to properly mitigate the low-frequency ripple for varying ac loads of the SBI and also to avoid overcharging of the auxiliary capacitor, a closed loop control strategy is developed for the APD topology. A hardware prototype is built for the APD-integrated SBI, and the advantages of the APD integration is corroborated with the experimental results.

In **Chapter 3**, the Reduced-Switch Current-Fed Switched Inverter (RSCFSI) is introduced, which has reduced one switch and has improved dc-dc voltage gain and efficiency over SBI. The derivation and steady-state analysis of the RSCFSI are explained. The conventional SBC-PWM of ISIs is modified for RSCFSI to incorporate simultaneous functionality of the the shoot-through operation and the dc-ac power conversion for the generation of the gate

pulses. A new PWM strategy, namely Enhanced Boost Control-based PWM (EBC-PWM), is proposed, which can achieve more boost factor and dc-ac voltage gain compared to SBC-PWM. A comparative analysis of RSCFSI with other AFE-ISIs is presented to highlight its advantage in terms of efficiency. The hardware prototype is built for the single-phase RSCFSI to validate the theoretical analysis with experimental results.

In **Chapter 4**, the low-frequency ripple problem of the single-phase RSCFSI is investigated. The amount of low-frequency ripple present in the active-front-end network parameters is estimated for the RSCFSI, and a selection procedure for the passive elements of the active-front-end network is formulated. Furthermore, an APD-integrated RSCFSI (APDRSCFSI) is introduced as a solution that deflects the aforementioned low-frequency ripple energy to an auxiliary capacitor without adding more active switches. As a result, the inverter can employ smaller passive elements. In addition, the EBC-PWM strategy is also extended for APDRSCFSI. As a result, the dc-ac voltage gain of the APDRSCFSI is improved, and the voltage stresses of the switches are reduced. A comparative analysis of the RSCFSI with the APDRSCFSI is also presented. A closed-loop control technique that combines output voltage control and APD functionality is also illustrated. The APDRSCFSI is validated to illustrate the advantages with the help of experimental results.

In **Chapter 5**, the concluding remarks of the thesis are presented. Based on the concluding remarks, the future scopes of research are proposed.

1.8 CONCLUDING REMARKS

This chapter provides the background information on the thesis, as well as a comprehensive review of the single-phase AFE-ISIs. Further, a discussion of the inherent low-frequency ripple problem of single-phase AFE-ISIs is presented. The motivation of this thesis is to address the research gaps discovered in the literature survey about AFE-ISIs and the low-frequency ripple problem associated with AFE-ISIs. A list of objectives is defined based on the motivation. The organization of the thesis is provided at the end of this chapter.

CHAPTER 2

SWITCHED BOOST INVERTER: ANALYSIS AND MITIGATION OF LOW-FREQUENCY RIPPLE

2.1 INTRODUCTION

In Chapter 1, the drawbacks of the conventional VSI are explained, viz., lower peak ac output voltage compared to dc input voltage, essential requirement of dead-time for prevention of shoot-through in the legs of inverter bridge, etc. The Switched Boost Inverter (SBI) can eliminate these drawbacks using its active-front-end network. The shoot-through zero states are introduced into the inverter's switching operation to boost the dc input voltage so that the effective input voltage to the inverter bridge is higher. As a result, higher ac output voltage can be achieved compared to conventional VSI. SBI can function with both dc and ac loads simultaneously and shows superior electromagnetic interference (EMI) noise immunity and more reliability. With the variation of shoot-through zero state duration, the ac output voltage can be varied widely. In this chapter, the circuit diagram and the steady-state analysis of SBI are presented.

Similar to a conventional single-phase VSI, the elements of the active-front-end network of the single-phase SBI have to endure the low-frequency ripple power generated from the ac load side. So, the capacitor voltage and inductor current of the active-front-end network contain low-frequency ripple. As a result, the dc-link voltage contains low-frequency ripple, which distorts the waveform of the output voltage. Furthermore, any single-phase SBI-integrated system, viz., photovoltaic system, light-emitting diode (LED) lighting, fuel cell, battery, etc., is affected due to low-frequency ripple. Therefore, this low-frequency ripple should be mitigated or limited within an engineering tolerant range.

The solution to the inherent low-frequency ripple issue in single-phase SBI is not explored in the literature. However, a lot of research has been carried out to solve this ripple problem for VSI and impedance-source inverters. The low-frequency ripple analysis and mitigation

of SBI and impedance-source inverters are not the same due to their topological differences. However, since they share some similar operational features, the low-frequency ripple reduction techniques for impedance-source inverters may be extended for SBI with appropriate modifications.

A common solution to reduce low-frequency ripple is to use bulky capacitor and inductor in the active-front-end network. In this chapter, the ripple energy of SBI is analyzed, and the amount of low-frequency ripple present in the active-front-end network parameters is estimated. Based on the analysis, a selection procedure for the passive elements of the active-front-end network is illustrated. However, the utilization of bulky passive elements leads to increased volume, weight and cost affecting power density, efficiency, reliability and lifetime of the system.

As a solution, active power decoupling (APD) topologies have been explored in the literature. In the traditional single-phase converters, additional active energy storage networks are connected in parallel to the dc-link to store the ripple energy, thereby, reducing size and weight of passive elements in the active-front-end network. As APD topologies can entirely eliminate low-frequency ripple power, it is highly effective for the single-phase SBI with battery or fuel cells. Among the existing techniques, the independent APD networks generally work independent of the inverter, which makes the control strategy much easier to implement. In this chapter, three independent APD topologies are integrated with SBI to minimize the passive elements of the active-front-end network. A comparison between three APD networks is also presented, and the independent Boost-type is chosen for implementation in hardware, because this topology can draw ripple current continuously and has higher auxiliary capacitor voltage, which results in lower capacitance and less complexity.

The ripple energy analysis of boost-type APD-integrated SBI is performed to estimate the amount of ripple to be diminished. The passive elements of the active-front-end network and APD topology are selected based on this analysis. The magnitude of the low-frequency ripple on capacitor voltage and inductor current is dependent on the load current. Also, the voltage across the auxiliary capacitor is required to be regulated to prevent over-voltage, as the

auxiliary capacitor stores the ripple energy. Therefore, to achieve these two objectives, closed-loop control is employed. Two different types of current controllers, proportional-integral (PI) and proportional-resonant (PR) controllers, are compared, and the PR current controller is chosen due to its superior steady-state error accuracy in tracking ac signals [100]. With the help of the small signal analysis of the APD topology, the parameters of the PR controller are designed, and a study is presented in this chapter. In order to validate the theoretical analysis, both single-phase SBI and boost-type APD-integrated SBI are fabricated in hardware. In the prototype of the proposed system, the gate pulses for the APD topology and SBI switches, as well as closed-loop control and PR controller, are implemented using TMS320F28335 digital signal processor (DSP). A sine-triangle pulse width modulation-based technique described in [20] is used for the gate-pulse generation of the SBI. Both the steady-state and transient performance of the system are demonstrated in the experimental results.

This chapter is organized as follows: **Section 2.2** focuses on single-phase SBI topology and its steady-state analysis. In **Section 2.3**, the low-frequency ripple analysis and the design of passive elements of the active-front-end network of SBI are illustrated. The mitigation of the low-frequency ripple of SBI is explained in **Section 2.4** with the help of APD integration. In **Section 2.5**, the low-frequency ripple analysis of APD-integrated topologies are illustrated, and a design procedure for passive elements of active-front-end network and APD topology is also presented. **Section 2.6** demonstrates the comparison between three APD-integrated SBI topologies. In **Section 2.7**, a closed-loop control strategy for ripple current compensation is described. The experimental studies are discussed in **Section 2.8**. Finally, **Section 2.9** concludes this chapter with a summary.

2.2 STEADY-STATE ANALYSIS OF SBI

The circuit diagram of the single-phase SBI is shown in Fig. 2.1. In SBI, the active switch S is essential to step up the dc input voltage (V_g). Apart from V_g and S, the dc-side comprises of the input inductor (L), the dc-link capacitor (C) and two diodes (D_a and D_b). The four switches ($S_{1\text{-}4}$) with anti-parallel diodes ($D_{1\text{-}4}$) are responsible for the dc-ac power

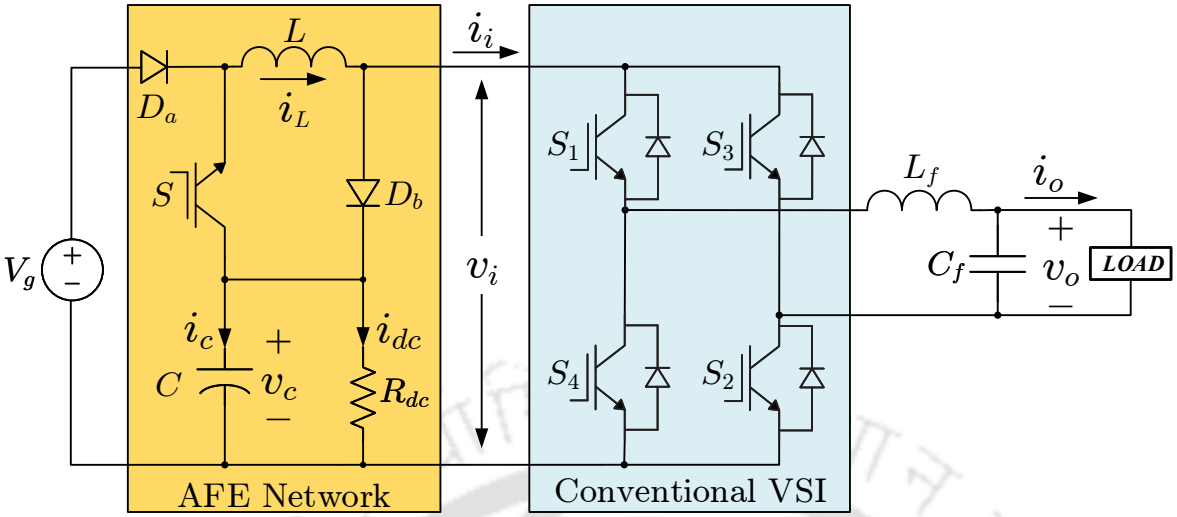


Fig. 2.1 Circuit diagram of a single-phase Switched Boost Inverter (SBI).

conversion. As shown in Fig. 2.1, the single-phase SBI utilizes the active-front-end network to boost the input dc voltage by the additional shoot-through zero switching states. As a result, higher ac output voltage can be achieved compared to classical VSI. SBI can function with both dc and ac loads simultaneously and shows superior electromagnetic interference (EMI) noise immunity and more reliability. With the variation of shoot-through zero state duration, the ac output voltage can be varied widely. A resistance R_{dc} is connected across capacitor C as the dc load. In absence of R_{dc}, a relatively large inductor L will be required to maintain continuous conduction mode. The shoot-through duty ratio D can be expressed as $D = T_{sh}/T_s$, where T_{sh} is the total duration of the shoot-through time interval, and T_s is the total switching time period.

For the circuit analysis of the single-phase SBI during shoot-through and nonshoot-through intervals, it is assumed that the SBI consists of all ideal elements and is operating in a continuous conduction mode. In the shoot-through interval, it is considered that the switches are turned on simultaneously without any dead time, and the fundamental frequency (f) of output ac voltage is much smaller than the switching frequency (f_s) of the inverter switches.

Fig. 2.2 shows two operational states of the SBI, i.e., shoot-through and nonshoot-through, with respective equivalent circuits. In shoot-through, there are two modes, and in nonshoot-

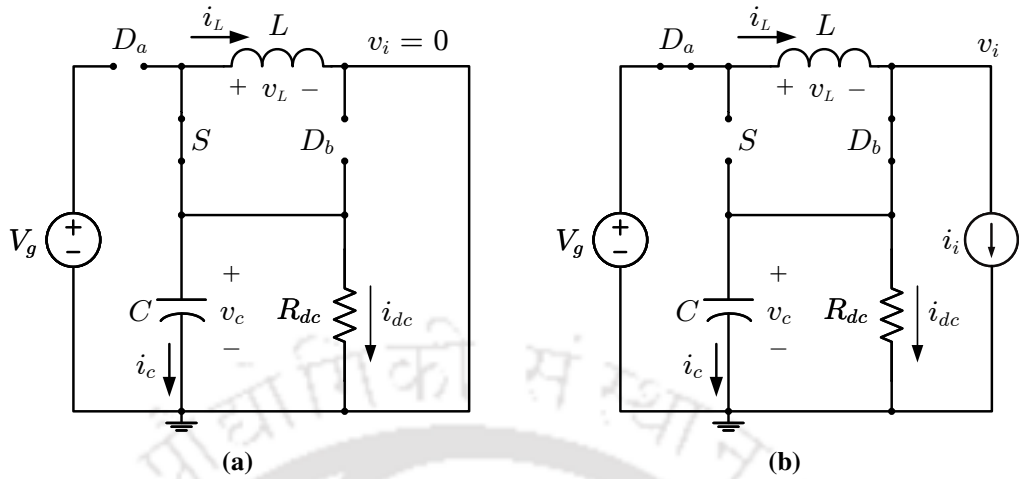


Fig. 2.2 Different states of operation of SBI: (a) shoot-through and (b) nonshoot-through.

Table 2.1 Switching states and inverter output voltage in different modes

State	Mode	ON Elements	OFF Elements	v_{ab}
Shoot-through	1	S, S_1, S_4	S_2, S_3, D_a, D_b	0
	2	S, S_2, S_3	S_1, S_4, D_a, D_b	0
Nonshoot--through	3	S_1, S_3, D_a, D_b	S_2, S_4	0
	4	S_2, S_3, D_a, D_b	S_1, S_4	$-v_c$
	5	S_1, S_4, D_a, D_b	S_2, S_3	v_c
	6	S_2, S_4, D_a, D_b	S_1, S_3	0

through, there are four modes, based on the switching states of the active switches and diodes as mentioned in Table 2.1.

During the shoot-through interval $D \cdot T_s$, either one of the inverter legs is shorted simultaneously with the switch S. In mode-1, S, S_1 and S_4 are turned on together, and in mode-2, S, S_2 and S_3 are turned on together. Note that SBI can also go into this state by tuning on all five switches simultaneously. The diode D_a is reverse-biased as a voltage of $(V_g - v_c)$ appears across it, where v_c is the dc-link capacitor voltage, and V_g is less than v_c. Similarly, the other diode D_b is reverse-biased as the dc capacitor C appears across it. Thus, the mathematical equations of the inverter in this interval can be written as:

$$\begin{aligned} v_L(t) &= v_c(t) \\ i_c(t) &= -i_L(t) - i_{dc}(t) \\ v_i(t) &= 0 \end{aligned} \tag{2.1}$$

where v_L and i_L are the inductor voltage and current, respectively; i_c is the capacitor current; v_i is the effective input voltage to the inverter; i_{dc} is the current drawn by the dc load R_{dc}.

During the nonshoot-through interval $(1-D)\cdot T_s$, the inverter is indicated by a current source i_i, because the SBI operates as a classical VSI. The switch S is turned off, and the diodes are forward-biased. The mathematical equations in this time interval are obtained as:

$$\begin{aligned} v_L(t) &= V_g - v_c(t) \\ i_c(t) &= i_L(t) - i_i(t) - i_{dc}(t) \\ v_i(t) &= v_c(t) \end{aligned} \tag{2.2}$$

where i_i is the current drawn by the inverter in the nonshoot-through interval.

Applying small ripple approximation to (2.1) and (2.2), one can obtain

$$v_L(t) = \begin{cases} V_c, & \text{if } 0 < t < D\cdot T_s \\ V_g - V_c, & \text{if } D\cdot T_s < t < T_s \end{cases} \tag{2.3}$$

$$i_c(t) = \begin{cases} -I_L; & \text{if } 0 < t < D\cdot T_s \\ I_L - I_i - I_{dc}; & \text{if } D\cdot T_s < t < T_s \end{cases} \tag{2.4}$$

where V_c, I_L, I_{dc} and I_i are the dc components of v_c, i_L, i_{dc} and i_i, respectively. In steady-state, over one switching cycle, the average voltage across the inductor $\langle v_L\rangle_{T_s}$ and average current through the capacitor $\langle i_c\rangle_{T_s}$ should be zero. Thus, using volt-second balance, one can write

$$\langle v_L(t)\rangle_{T_s} = D\cdot V_c + (1-D)\cdot(V_g - V_c) = 0. \tag{2.5}$$

From (2.5), the average value of v_c is determined as:

$$V_c = \left(\frac{1-D}{1-2D}\right)\cdot V_g = B_F V_g \tag{2.6}$$

where B_F signifies the boost factor.

Similarly, using capacitor amp-second balance, one can obtain

$$\langle i_c(t)\rangle_{T_s} = D\cdot(-I_L - I_{dc}) - (1-D)\cdot(I_L - I_i - I_{dc}) = 0 \tag{2.7}$$

From (2.7), the average value of i_L is derived as:

$$I_L = \left(\frac{1-D}{1-2D}\right)\cdot I_i + \left(\frac{1}{1-2D}\right)\cdot I_{dc}. \tag{2.8}$$

2.3 LOW-FREQUENCY RIPPLE ANALYSIS OF SBI AND DESIGN OF PASSIVE ELEMENTS OF ACTIVE-FRONT-END NETWORK

The elements of the active-front-end network of the single-phase SBI has to endure the low-frequency ripple because of the power mismatch between the constant dc input power and the pulsating power generated from the ac load side. As a result, the capacitor voltage and inductor current of the active-front-end network contain low-frequency ripple. In Subsection 2.3.1, a low-frequency ripple analysis is illustrated to estimate the amount of the low-frequency ripple in the active-front-end network. In order to prevent distortion of the SBI's output voltage, this low-frequency ripple ought to be mitigated or at least limited within an engineering tolerant range. Thus, a design procedure for the passive elements of the active-front-end network is described in Subsection 2.3.2 to limit the low-frequency ripple.

2.3.1 Low-frequency ripple analysis of SBI

The output voltage and/or output current of single-phase SBI should be sinusoidal. The expressions of sinusoidal output voltage (v_o) and output current (i_o) can be considered as

$$\begin{aligned} v_o(t) &= \sqrt{2}V_o \sin\omega_o t \\ i_o(t) &= \sqrt{2}I_o \sin(\omega_o t - \varphi) \end{aligned} \tag{2.9}$$

where ω_o is the fundamental frequency, and φ is the phase difference between v_o and i_o.

Therefore, the output power (p_o) can be obtained as

$$p_o(t) = v_o(t) \cdot i_o(t) = V_o I_o \cos\varphi - V_o I_o \cos(2\omega_o t - \varphi) = P_o + p'_r(t) \tag{2.10}$$

which contains two components: the constant active power (P_o) and the low-frequency ripple power (p'_r). In Fig. 2.1, the input power is coming from the source is constant. In order to balance the input and output power, the low-frequency ripple power must be supplied by the capacitor C and inductor L of the active-front-end network. This results in large voltage ripple on the capacitor and large current ripple on the inductor of the active-front-end network, which can be analyzed with the determination of the ripple energy of single-phase SBI. Because p'_r mostly includes second harmonic ($2\omega_o$) ripples, the low-frequency ripples of the active-front-end network parameters primarily contain $2\omega_o$ ripples. As a result, the dc-link voltage has low-frequency ripples. The presence of low-frequency ripple on the dc-link voltage distorts the output voltage.

For the computation of the total ripple power, the effect of the output filter inductor (L_f) and the output filter capacitor (C_f) should also be taken into account. Note that C_f is connected across the load as shown in Fig. 2.1. Thus, the voltage across C_f is the output voltage v_o. Therefore, the current through C_f is

$$i_{Cf}(t) = C_f \frac{dv_o(t)}{dt} = \sqrt{2}\omega_o C_f V_o \cos\omega_o t \tag{2.11}$$

Thus, the power drawn by C_f is expressed as,

$$p_{Cf}(t) = v_o(t) \cdot i_{Cf(t)} = \omega_o C_f V_o^2 \sin 2\omega_o t \tag{2.12}$$

Similarly, from Fig. 2.1, it can be noticed that the current through L_f is

$$i_{Lf}(t) = i_o(t) - i_{Cf}(t) = \sqrt{2} I_o \sin(\omega_o t - \varphi) - \sqrt{2}\omega_o C_f V_o \cos\omega_o t \tag{2.13}$$

Therefore, the voltage across L_f is

$$v_{Lf}(t) = L_f \frac{di_{Lf}(t)}{dt} = \sqrt{2}\omega_o L_f I_o \cos(\omega_o t - \varphi) - \sqrt{2}\omega_o^2 L_f C_f V_o \sin \omega_o t \tag{2.14}$$

Thus, the power drawn by L_f is expressed as,

$$\begin{aligned} p_{Lf}(t) &= v_{Lf}(t) \cdot i_{Lf}(t) \\ &= \omega_o L_f I_o^2 \sin(2\omega_o t - 2\varphi) - \omega_o^2 L_f C_f \{\omega_o C_f V_o^2 \sin 2\omega_o t - 2V_o I_o \cos(2\omega_o t - \varphi)\} \end{aligned} \tag{2.15}$$

In (2.15), the second term can be ignored, because it is significantly smaller than the first term. Therefore, (2.15) can be approximately written as

$$p_{Lf}(t) \approx \omega_o L_f I_o^2 \sin(2\omega_o t - 2\varphi) \tag{2.16}$$

Thus, the total ripple power (p_r) becomes,

$$\begin{aligned} p_r(t) &= p_r'(t) + p_{Lf}(t) + p_{Cf}(t) \\ &= -V_o I_o \cos(2\omega_o t - \varphi) + \omega_o L_f I_o^2 \sin(2\omega_o t - 2\varphi) + \omega_o C_f V_o^2 \sin 2\omega_o t \\ &= R_0 \sin(2\omega_o t - \psi) \end{aligned} \tag{2.17}$$

where

$$\begin{aligned} R_0 &= \sqrt{(V_o I_o \, cos\varphi + \omega_o L_f I_o^2 \sin 2\varphi)^2 + (\omega_o C_f V_o^2 + \omega_o L_f I_o^2 \cos 2\varphi - V_o I_o \sin \varphi)^2} \\ \psi &= \tan^{-1}\left(\frac{V_o I_o \, cos\varphi + \omega_o L_f I_o^2 \sin 2\varphi}{\omega_o C_f V_o^2 + \omega_o L_f I_o^2 \cos 2\varphi - V_o I_o \sin \varphi}\right) \end{aligned}$$

The ac modeling approach, as explained in [3], is applied to (2.1) and (2.2) to derive the average over one switching cycle as follows:

$$\begin{aligned} L\frac{d}{dt}\langle i_L(t)\rangle_{T_s} &= V_g - \{1 - 2d(t)\} \cdot \langle v_c(t)\rangle_{T_s} \\ C\frac{d}{dt}\langle v_c(t)\rangle_{T_s} &= \{1 - 2d(t)\} \cdot \langle i_L(t)\rangle_{T_s} - \{1 - d(t)\} \cdot \langle i_i(t)\rangle_{T_s} \end{aligned} \tag{2.18}$$

where $\langle i_L(t)\rangle_{T_s}$, $\langle v_c(t)\rangle_{T_s}$ and $\langle i_i(t)\rangle_{T_s}$ are the average of i_L, v_c and i_i, receptively, over one switching period. It is assumed that the dc input voltage is purely dc. The dc load R_{dc} is also ignored. The small-signal perturbations are considered for the rest of the parameters around their respective average values and are represented by '$\sim$' above these variables as follows:

$$\begin{aligned}\langle i_L(t)\rangle_{T_s} &= I_L + \tilde{i}_L(t);\\ \langle v_c(t)\rangle_{T_s} &= V_c + \tilde{v}_c(t);\\ \langle i_i(t)\rangle_{T_s} &= I_i + \tilde{i}_i(t).\end{aligned} \tag{2.19}$$

Note that the objective here is to derive a relationship between $\tilde{i}_L$, $\tilde{v}_c$ and $\tilde{i}_i$, Hence, the shoot-through duty ratio is also taken as constant so that $d(t) = D$. Thus, (2.18) is perturbed and linearized to construct the small-signal equations of SBI as

$$\begin{aligned}L\frac{d}{dt}\{I_L + \tilde{i}_L(t)\} &= V_g - (1-2D)\cdot\{V_c + \tilde{v}_c(t)\}\\ C\frac{d}{dt}\{V_c + \tilde{v}_c(t)\} &= (1-2D)\cdot\{I_L + \tilde{i}_L(t)\} - (1-D)\cdot\{I_i + \tilde{i}_i(t)\}\end{aligned} \tag{2.20}$$

Equating the first order ac terms on both sides, the dynamic equations are obtained as

$$\begin{aligned}L\frac{d\tilde{i}_L(t)}{dt} &= -(1-2D)\cdot\tilde{v}_c(t)\\ C\frac{d\tilde{v}_c(t)}{dt} &= (1-2D)\cdot\tilde{i}_L(t) - (1-D)\cdot\tilde{i}_i(t)\end{aligned} \tag{2.21}$$

Using Laplace transform, (2.21) is taken into s-domain, and is presented as

$$\begin{aligned}sL\tilde{i}_L(s) &= -(1-2D)\cdot\tilde{v}_c(s)\\ sC\tilde{v}_c(s) &= (1-2D)\cdot\tilde{i}_L(s) - (1-D)\tilde{i}_i(s).\end{aligned} \tag{2.22}$$

Solving (2.22), the relationship among $\tilde{i}_i$, $\tilde{v}_c$ and $\tilde{i}_L$ in s-domain is obtained as

$$\begin{aligned}\tilde{v}_c(s) &= -\frac{sL(1-D)}{(1-2D)^2 + s^2LC}\cdot\tilde{i}_i(s)\\ \tilde{i}_L(s) &= \frac{(1-D)(1-2D)}{(1-2D)^2 + s^2LC}\cdot\tilde{i}_i(s)\end{aligned} \tag{2.23}$$

At frequency $2\omega_o$, from (2.23) one can obtain

$$\begin{aligned}\tilde{v}_c(j2\omega_o) &= -\frac{j2\omega_o L(1-D)}{(1-2D)^2 - 4\omega_o^2 LC} \cdot \tilde{i}_i(j2\omega_o) \\ \tilde{i}_L(j2\omega_o) &= \frac{(1-D)(1-2D)}{(1-2D)^2 - 4\omega_o^2 LC} \cdot \tilde{i}_i(j2\omega_o)\end{aligned} \tag{2.24}$$

which can be rewritten using phasor notations as

$$\begin{aligned}\overrightarrow{\tilde{v}}_{c\,2\omega_o} &= -\frac{j2\omega_o L(1-D)}{(1-2D)^2 - 4\omega_o^2 LC} \cdot \overrightarrow{\tilde{i}}_{i\,2\omega_o} \\ \overrightarrow{\tilde{i}}_{L\,2\omega_o} &= \frac{(1-D)(1-2D)}{(1-2D)^2 - 4\omega_o^2 LC} \cdot \overrightarrow{\tilde{i}}_{i\,2\omega_o}\end{aligned} \tag{2.25}$$

where $\overrightarrow{\tilde{i}}_{i\,2\omega_o}$, $\overrightarrow{\tilde{v}}_{c\,2\omega_o}$ and $\overrightarrow{\tilde{i}}_{L\,2\omega_o}$ are the second harmonic ripples of $\tilde{i}_i$, $\tilde{v}_c$ and $\tilde{i}_L$, respectively, expressed using phasor notations.

During the shoot-through interval, power is not transferred from input to output of the inverter, and the current drawn by the inverter i_i is also zero. So, the power is coming from the dc side only in the nonshoot-through interval and is equal to the output power p_o as follows

$$p_i(t) = (1-D) \cdot v_i(t) \cdot i_i(t) = p_o(t) \tag{2.26}$$

which can be expanded with respective low-frequency ripples as follows

$$(1-D) \cdot \{V_c + \tilde{v}_c(t)\} \cdot \{I_i + \tilde{i}_i(t)\} = P_o + p_r(t) \tag{2.27}$$

In (2.27), equating the dc parts on both sides, one can obtain

$$(1-D) \cdot V_c \cdot I_i = P_o \tag{2.28}$$

The fundamental component of the voltage across the terminals a-b can be expressed as

$$v_{ab1}(t) = v_o(t) + v_{Lf}(t) = A_x \sin(\omega_o t + \varphi_x) \tag{2.29}$$

where

$$\begin{aligned} A_x &= \sqrt{2\{(V_o + \omega_o L_f I_o \sin\varphi)^2 + (\omega_o L_f I_o \cos\varphi)^2\}} \\ \varphi_x &= \tan^{-1}\left(\frac{\omega_o L_f I_o \cos\varphi}{V_o + \omega_o L_f I_o \sin\varphi}\right) \end{aligned} \tag{2.30}$$

Also, the peak fundamental output ac voltage is

$$\hat{v}_{ab1} = M \cdot V_c = A_x \tag{2.31}$$

where M is the modulation index of the inverter. Using (2.10) and (2.31) in (2.28), the average value of i_i is obtained as

$$I_i = \frac{V_o I_o}{1-D} \cdot \frac{M}{A_x} \cos\varphi \tag{2.32}$$

In (2.29), v_{Lf} can be ignored as it is much smaller than v_o so that one can approximately obtain the following

$$v_{ab1}(t) \approx v_o(t) \tag{2.33}$$

and (2.31) is approximated as

$$V_c = \frac{\sqrt{2}V_o}{M} \tag{2.34}$$

So, (2.32) is approximated as

$$I_i \approx \frac{M I_o}{\sqrt{2}(1-D)} \cos\varphi \tag{2.35}$$

In (2.27), taking only the low-frequency ripple part and assuming $V_c >> \tilde{v}_c$, one can write

$$(1-D) \cdot V_c \cdot \tilde{i}_i(t) = p_r(t) \tag{2.36}$$

Therefore, the expression of $\tilde{i}_i$ can be derived as

$$\tilde{i}_i(t) = -\frac{M I_o}{\sqrt{2}(1-D)} \cos(2\omega_o t - \varphi) \tag{2.37}$$

which can be expressed using phasor notations as

$$\overrightarrow{\tilde{i}}_{i\ 2\omega_o} = -\frac{MI_o}{\sqrt{2}(1-D)}\angle -\varphi \tag{2.38}$$

Thus, (2.25) and (2.38) and are solved to obtain low-frequency part of i_L and v_c, i.e., $\tilde{i}_L$ and $\tilde{v}_c$, respectively, as follows

$$\begin{aligned}\overrightarrow{\tilde{v}}_{c\,2\omega_o} &= \frac{\sqrt{2}\omega_o LMI_o}{[4\omega_o^2 LC-(1-2D)^2]}\angle(90^{\text{o}}+\varphi)\\ \overrightarrow{\tilde{i}}_{L\,2\omega_o} &= \frac{(1-2D)MI_o}{\sqrt{2}[4\omega_o^2 LC-(1-2D)^2]}\angle -\varphi\end{aligned} \tag{2.39}$$

which can be rewritten in time-domain as follows:

$$\begin{aligned}\tilde{v}_c(t) &= \frac{\sqrt{2}\omega_o LMI_o}{[4LC\omega_o^2-(1-2D)^2]}\sin(2\omega_o t-\varphi)\\ \tilde{i}_L(t) &= \frac{(1-2D)MI_o}{\sqrt{2}[4LC\omega_o^2-(1-2D)^2]}\cos(2\omega_o t-\varphi)\end{aligned} \tag{2.40}$$

It is clear from (2.40), both L and C need to be very large in order to maintain smaller values of $\tilde{v}_c$ and $\tilde{i}_L$.

2.3.2 Design of passive elements of the active-front-end network of SBI

The passive components in the active-front-end network are chosen in such a manner so that both high- and low-frequency ripple are limited within a specified tolerant range. Thus, (2.1) can be approximated as

$$\begin{aligned}L\frac{\Delta i_L}{DT_s} &= V_c\\ C\frac{\Delta v_c}{DT_s} &= |-I_L|\end{aligned} \tag{2.41}$$

Using (2.6) in (2.41), the capacitor requirement for the mitigation of high-frequency ripple is

$$C \geq \frac{DT_s MI_o cos\varphi}{\sqrt{2}a(1-D)V_g} \tag{2.42}$$

where a is the preferred allowance of high-frequency ripples of v_c as follows:

$$a \geq \frac{\Delta v_c}{V_c} \times 100\% \tag{2.43}$$

Similarly, the required inductor to restrict the high-frequency current ripple is obtained as

$$L \geq \frac{\sqrt{2}D(1-D)T_s V_g}{bMI_o cos\varphi} \tag{2.44}$$

where b is the preferred allowance of high-frequency ripple of i_L as follows:

$$b \geq \frac{\Delta i_L}{I_L} \times 100\% \tag{2.45}$$

However, these values of capacitor and inductor may not be sufficient for mitigation of low-frequency ripple within required limit. The peak-to-peak low-frequency ripple of the capacitor voltage v_c is

$$(\tilde{v}_c)_{\text{p-p}} = 2\hat{\tilde{v}}_c = \frac{2\sqrt{2}\omega_o LMI_o}{[4LC\omega_o^2 - (1-2D)^2]} \tag{2.46}$$

Similarly, the peak-to-peak low-frequency ripple of the inductor current i_L can be expressed as

$$(\tilde{i}_L)_{\text{p-p}} = 2\hat{\tilde{i}}_L = \frac{2(1-2D)MI_o}{\sqrt{2}[4LC\omega_o^2 - (1-2D)^2]} \tag{2.47}$$

Let x be the desired low-frequency ripples of v_c as follows:

$$x \geq \frac{2\hat{\tilde{v}}_c}{V_c} \times 100\% \tag{2.48}$$

Similarly, let y be the desired low-frequency ripple of i_L as follows:

$$y \geq \frac{2\hat{\tilde{i}}_L}{I_L} \times 100\% \tag{2.49}$$

Table 2.2 Simulation parameters and component values

Parameter/Component	Attributes
Input voltage (V_g)	100 V
Modulation index (M)	0.5
Shoot-through duty ratio (D)	0.4
Fundamental frequency (f_o)	50 Hz
Inverter switching frequency (f_s)	10 kHz
Inductor (L)	2.75 mH
DC-link capacitor (C)	100 µF
DC Load (R_{dc})	400 Ω, 250 W
Output filter inductor (L_f)	1 mH
Output filter capacitor (C_f)	11 µF
AC Load (R_o)	36 Ω, 250 W

Thus, the minimum capacitor requirement for limiting low-frequency ripple using the selected inductor value in (2.44) is obtained as

$$C \geq \frac{(1-2D)MI_o}{\sqrt{2}x\omega_o(1-D)V_g} + \frac{(1-2D)^2}{4\omega_o^2 L} \tag{2.50}$$

In order to mitigate both high- and low-frequency ripple, the capacitor must be chosen larger than both the values of C obtained in (2.42) and (2.50). Based on the value of chosen capacitor, y needs to be calculated again to check whether it matches ripple limit.

$$y \geq \frac{2(1-2D)^2}{[4LC\omega_o^2 - (1-2D)^2]\cos\varphi} \tag{2.51}$$

If it is not within limit, a larger inductor is selected and capacitor value is again calculated. This procedure is continued until all ripples are within tolerance limit.

In this work, taking x = 2.5%, C is chosen as 570 µF, and considering y = 25%, L is selected as 2.75 mH. The design of passive elements is verified in simulation with parameters given in Table 2.2. The simulation results are shown in Fig. 2.3, where the waveforms of the dc-link capacitor voltage v_c, the inductor current i_L of active-front-end network, the output voltage v_o and the output current i_o are plotted. The peak-to-peak ripple of v_c is found to be 6 V, and the average value of v_c is observed to be 300 V. Thus, the calculated value of x = 2%. Similarly, the peak-to-peak ripple of i_L is found to be 2 A, and the average value of

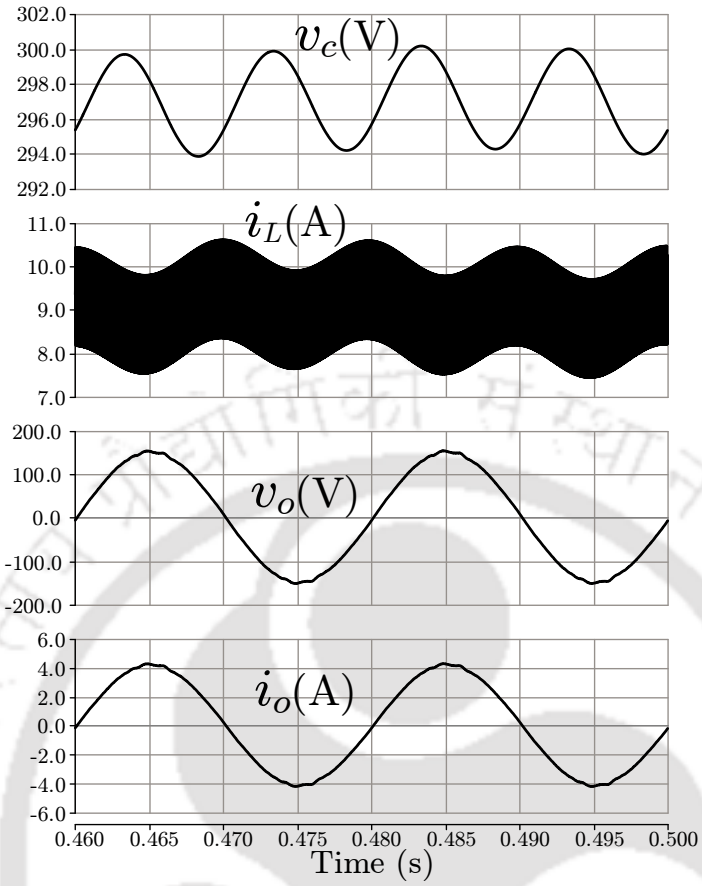


Fig. 2.3 Simulation results of single-phase SBI to verify the design of passive elements. v_c: dc-link capacitor voltage, i_L: inductor current of active-front-end network, v_o: output voltage and i_o: output current.

i_L is observed to be 9 A. Therefore, the calculated value of y = 22.2%. Note that the peak amplitude of v_o is 150 V, and the peak amplitude of i_o is 4 A. So, it can be concluded that the designed values of passive elements of the active-front-end network can satisfactorily restrict the low-frequency ripples below desired limitations.

2.4 LOW-FREQUENCY RIPPLE MITIGATION IN SBI

As discussed in Chapter 1, the integration of APD and ISIs are found in literature, in which the independent APD networks are connected across the dc-link to suppress the low-frequency ripple [77–90]. The same connection can be used for SBI, and the general circuit diagram of an APD-integrated SBI topology can be derived as shown in Fig. 2.4. Alternatively, the independent APD networks can be connected across the dc-link capacitor to suppress the low-frequency ripple as shown in Fig. 2.5. Three most common independent APD topologies,

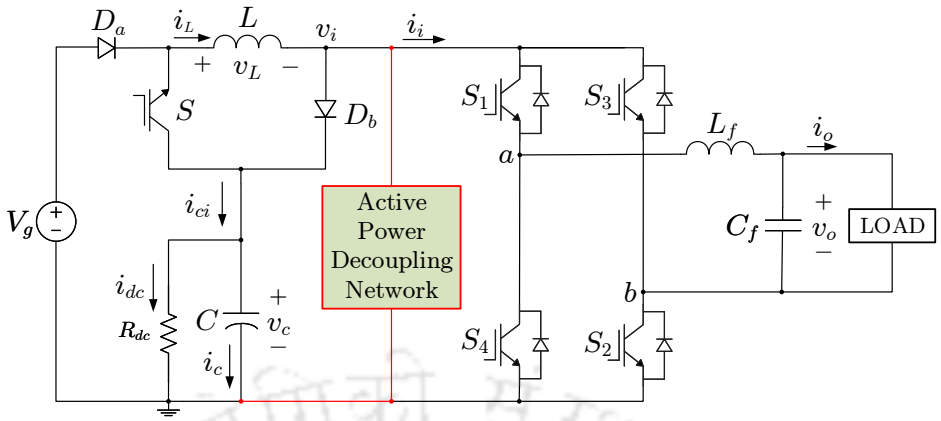


Fig. 2.4 Circuit diagram of a single-phase SBI with APD networks connected across the dc-link.

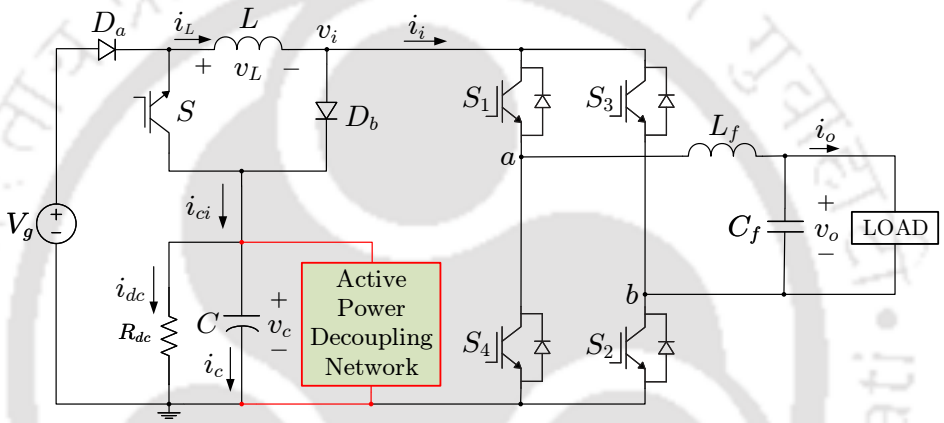


Fig. 2.5 Circuit diagram of a single-phase SBI with APD networks connected across the dc-link capacitor.

namely buck, boost and buck-boost-type are illustrated in Fig. 2.6. Any of these APD topologies can be integrated with the single-phase SBI in accordance with the circuit diagrams shown in Fig. 2.4 and 2.5. All of these topologies comprise of two switches (Q_1, Q_2), one auxiliary capacitor (C_s) for the storage of low-frequency ripple energy and one auxiliary inductor (L_s) for facilitation of low-frequency ripple energy transfer from C to C_s. Note that L_s does not store any energy over a switching cycle. Depending on the value of the ripple current i_r, the amount of ripple reduction in the capacitor voltage and inductor current of the active-front-end network is determined.

However, the connection of the APD network across the dc-link in any ISI and AFE-ISI topology has a considerable issue arising from the APD operation during shoot-through state, and this behavior is also observed in APD-integrated SBI. During shoot-through state, the dc-link voltage becomes zero in SBI, because any one of the inverter leg is shorted. Consequently,

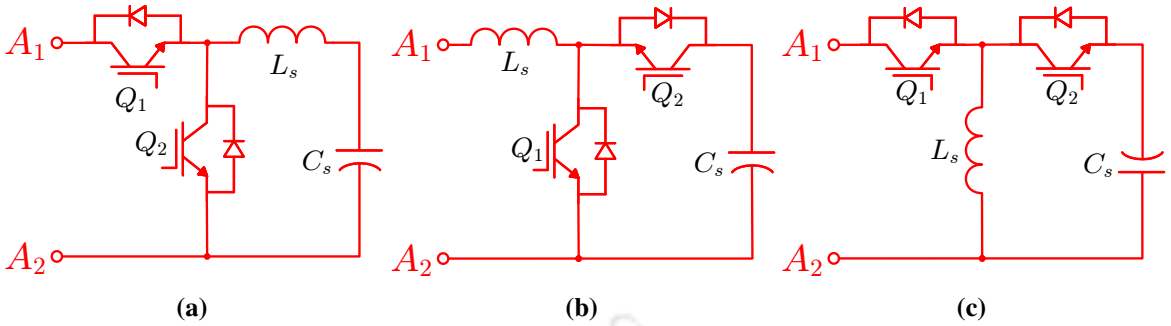


Fig. 2.6 Different types of APD networks: (a) buck, (b) boost and (c) buck-boost.

the APD network is also shorted during shoot-through state of the SBI. This is explained for each of the buck, boost and buck-boost APD networks in the following with the help of equivalent circuit diagrams. Since the connection of the APD network across the dc-link in SBI possesses unintentional issues in different ways in all three APD topologies owing to the shoot-through state of the SBI, the low-frequency ripple reduction functionality of the APD networks is significantly hampered. To prevent this, in this chapter, the APD networks are connected across the dc-link capacitor C instead of the dc-link as shown in Fig. 2.5. In the following sections, both connections are explored for all three APD topologies to explain the benefit of connecting the APD network across the dc-link capacitor instead of the dc-link.

2.4.1 Buck-type APD

As the name suggests, the auxiliary capacitor voltage v_{cs} in this APD topology is maintained to be lower than the capacitor voltage v_c.

A) Buck-type APD network connected across the dc-link

The circuit diagram of the single-phase SBI with buck-type APD network connected across the dc-link is illustrated in Fig. 2.7. The equivalent circuit diagrams in different operational modes are shown in Fig. 2.8.

Mode-1: As shown in Fig. 2.8(a), in this mode, Q_1 is turned on and Q_2 is turned off, while the SBI is in shoot-through state. The auxiliary inductor L_s is discharged, and the auxiliary capacitor C_s are charged by L_s. The APD operation becomes hampered in this mode, because

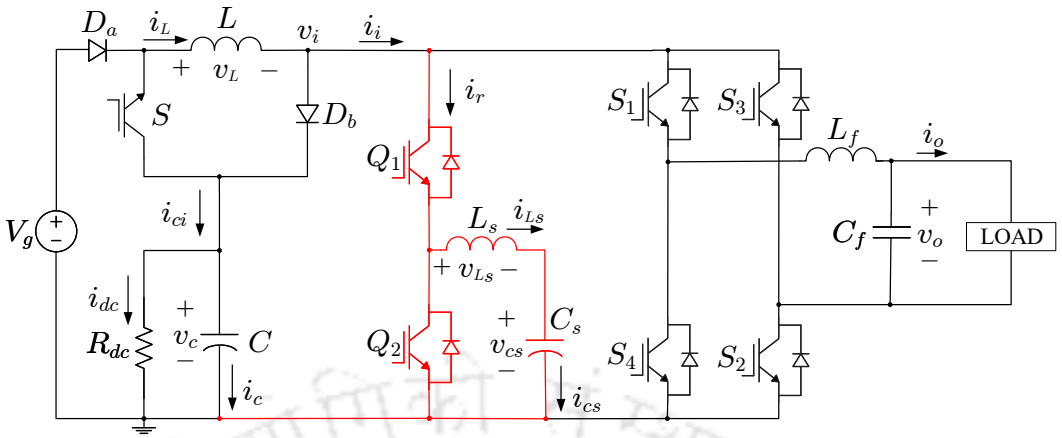


Fig. 2.7 Circuit diagram of SBI with buck-type APD connected across the dc-link.

one of the inverter leg is shorted. As the APD functionality becomes dependent on the inverter in this mode, this is an undesired mode of operation.

Mode-2: In this mode, Q_1 turned off and Q_2 is turned on, L_s is discharged and C_s is charged by L_s as observed in Fig. 2.8(b). Although the SBI is in shoot-through state, the APD network is disconnected from the inverter in this mode. Therefore, the APD functionality remains independent of the inverter.

Mode-3: This mode is similar to the operation of APD when it is connected across the dc-link of a conventional VSI, because the SBI operates in the nonshoot-through state. In this mode, C charges both L_s and C_s by turning on the switch Q_1, as shown in Fig. 2.8(c). In this mode, the ripple energy of C is transferred to L_s and C_s. As L_s is not utilized as a ripple energy storage device over a switching period, the energy stored by L_s in this mode is discharged in modes 1, 2 and 4. In this mode, the APD functionality remains independent of the inverter, because the ripple energy of C is only transferred without affecting the steady-state operation.

Mode-4: Similar to mode-2, in this mode, Q_1 turned off and Q_2 is turned on, L_s is discharged and C_s is charged by L_s. The SBI operates in nonshoot-through, but the APD network is disconnected from the inverter in this mode, as observed in Fig. 2.8(d). Therefore, the APD functionality remains independent of the inverter.

The undesired mode of operation is also verified in simulation with the parameters given in Table 2.2. The auxiliary inductor L_s is taken as 1 mH, and the auxiliary capacitor C_s is chosen

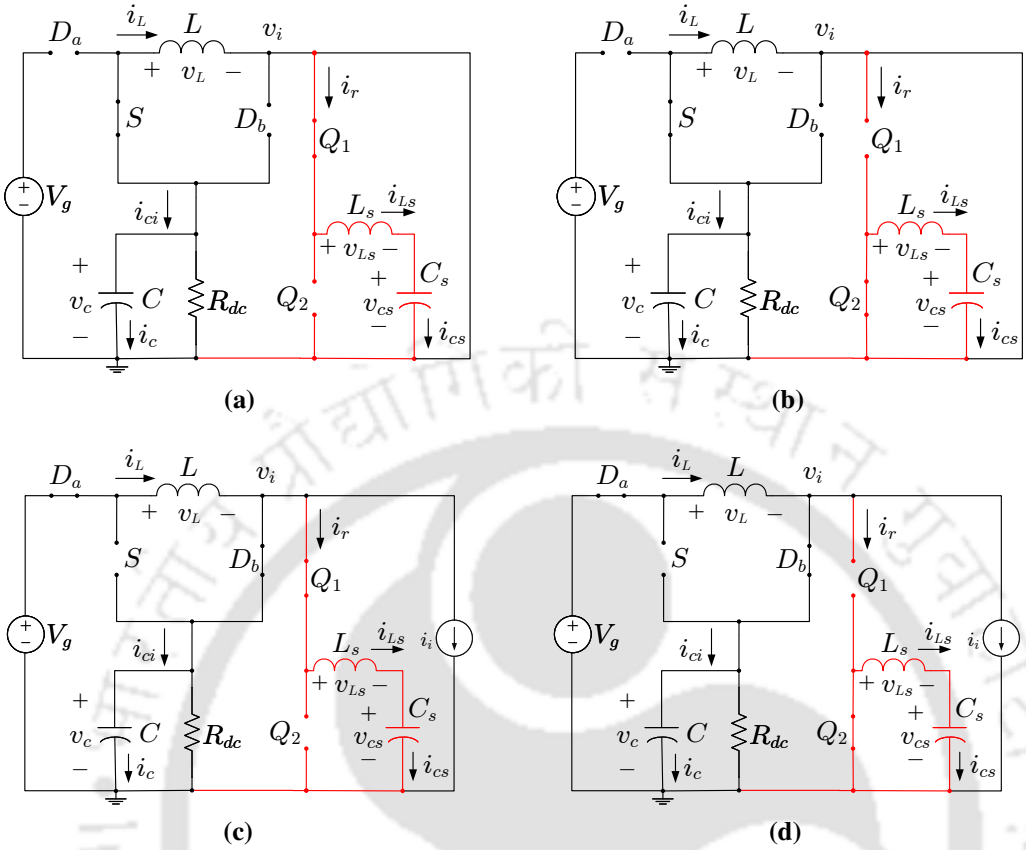


Fig. 2.8 Different modes of operation of single-phase SBI with buck-type APD network connected across the dc-link: (a) mode-1: SBI is in shoot-through state, Q_1 is on; (b) mode-2: SBI is in shoot-through state, Q_2 is on; (c) mode-3: SBI is in nonshoot-through state, Q_1 is on; (d) mode-4: SBI is in nonshoot-through state, Q_2 is on.

as 220 μF. The APD switching frequency is 20 kHz. The simulation results are shown in Fig. 2.9. The auxiliary inductor voltage v_{Ls}, the auxiliary inductor current i_{Ls}, the gate signals of the switches S, Q_1 and Q_2, i.e., G_S, G_{Q1} and G_{Q2}, respectively, are plotted in Fig. 2.9(a). It is observed that during shoot-through state, when G_S and G_{Q1} are high simultaneously, i_{Ls} has a negative slope, which indicates the discharging of L_s. In the nonshoot-through state, when G_S is low, and G_{Q1} is high, i_{Ls} has a positive slope, which shows the charging of L_s. Therefore, the charging of L_s is facilitated by turning on of the switch Q_1. But this is interrupted, when S turns on, impacting the transfer of the ripple energy from C to C_s. Irrespective of the shoot-through or nonshoot-through state of SBI, when G_{Q2} is high, L_s is discharged as indicated by the negative slope of i_{Ls}.

In Fig. 2.9(b), the waveforms of the dc-link capacitor voltage v_c, the active-front-end network inductor current i_L and the auxiliary capacitor voltage v_{cs} are plotted. The average

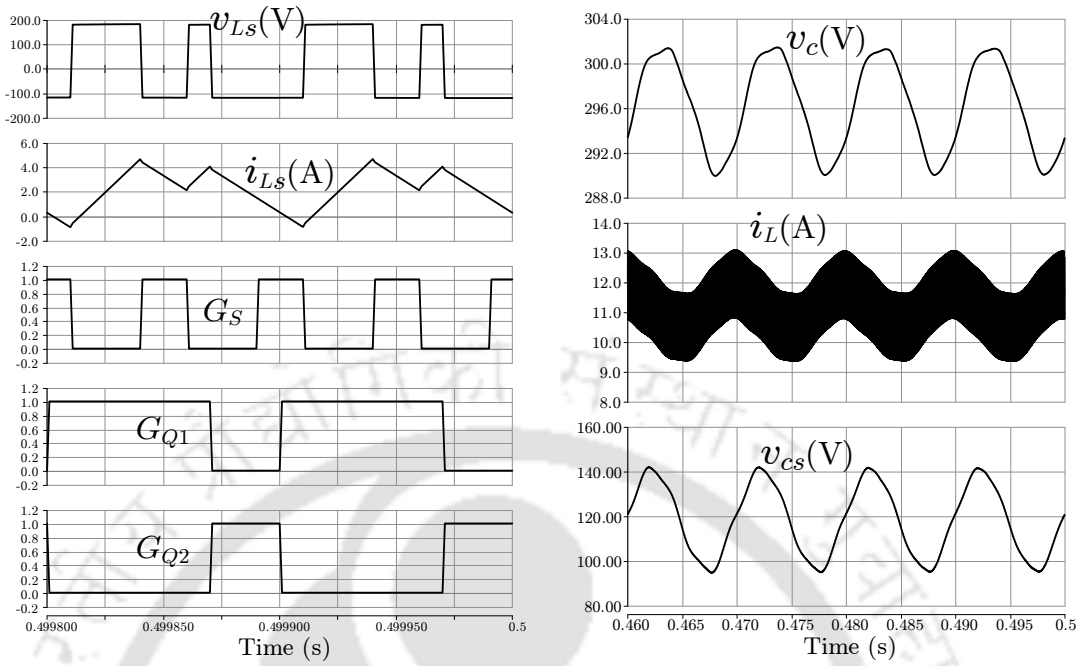


Fig. 2.9 Simulation results of single-phase SBI with buck-type APD connected across the dc-link.

value of v_c is 296 V, and the average value of v_{cs} is 120 V, which indicates the APD functions in buck-mode. The peak-to-peak ripple of v_c is 12 V, and the peak-to-peak ripple of i_L is 4 A. The amount of ripple can be reduced further if the APD network is connected across the dc-link capacitor.

B) Buck-type APD network connected across the dc-link capacitor

The circuit diagram of the single-phase SBI with buck-type APD network connected across the dc-link capacitor C is illustrated in Fig. 2.10. The equivalent diagrams are shown in Fig. 2.11. The main advantage of connecting the buck-type APD network across the dc-link capacitor is that the undesired mode-1 of the buck-type APD network connected across the dc-link is avoided.

As shown in Fig. 2.11, the SBI is in shoot-through state in modes 1 and 2, and is in nonshoot-through state in modes 3 and 4. However, the state of the inverter does not impact the APD functionality. In modes 1 and 3, when Q_1 is turned on, and Q_2 is turned off, both auxiliary inductor L_s and the dc-link capacitor C charge the auxiliary capacitor C_s. Thus, the

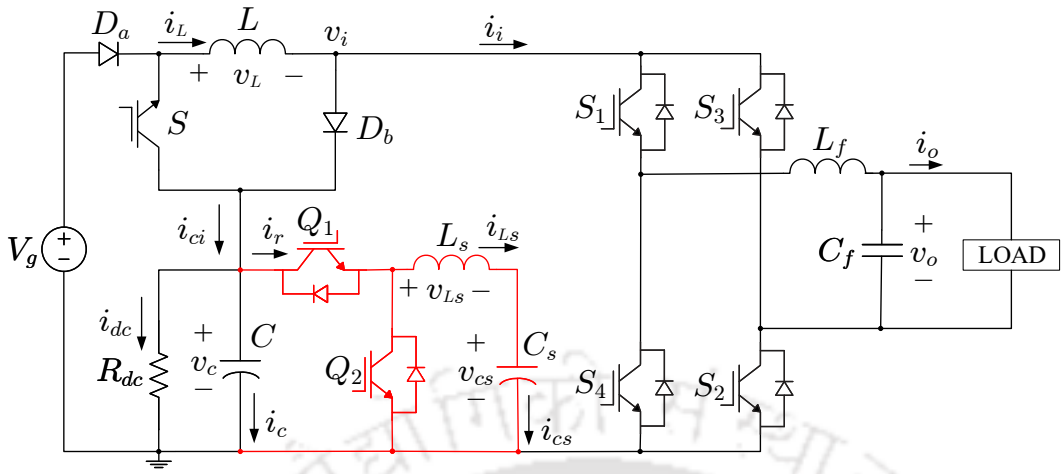


Fig. 2.10 Circuit diagram of SBI with buck-type APD connected across the dc-link capacitor.

ripple energy is deflected from C and gets stored in C_s. So, C_s is the ripple energy storage device. Note that the ripple current i_r is same as the auxiliary inductor current i_{Ls} and the auxiliary capacitor current i_{cs}. Therefore, the mathematical equations during this time interval can be obtained as:

$$\begin{aligned} v_{Ls}(t) &= v_c(t) - v_{cs}(t) \\ i_{cs}(t) &= i_{Ls}(t) \\ i_r(t) &= i_{Ls}(t) \end{aligned} \tag{2.52}$$

In modes 2 and 4, when Q_1 is turned off, and Q_2 is turned on, the auxiliary capacitor C_s is charged by the auxiliary inductor L_s. In these modes, L_s transfers the energy stored in the modes 1 and 3 to C_s. Thus, the ripple energy is transferred from C to C_s via L_s. Here, L_s is not used as a energy storage device in buck-type APD, and it is only employed to transfer the ripple energy from C to C_s. Therefore, the mathematical equations during this time interval are expressed as:

$$\begin{aligned} v_{Ls}(t) &= -v_{cs}(t) \\ i_{cs}(t) &= i_{Ls}(t) \\ i_r(t) &= 0 \end{aligned} \tag{2.53}$$

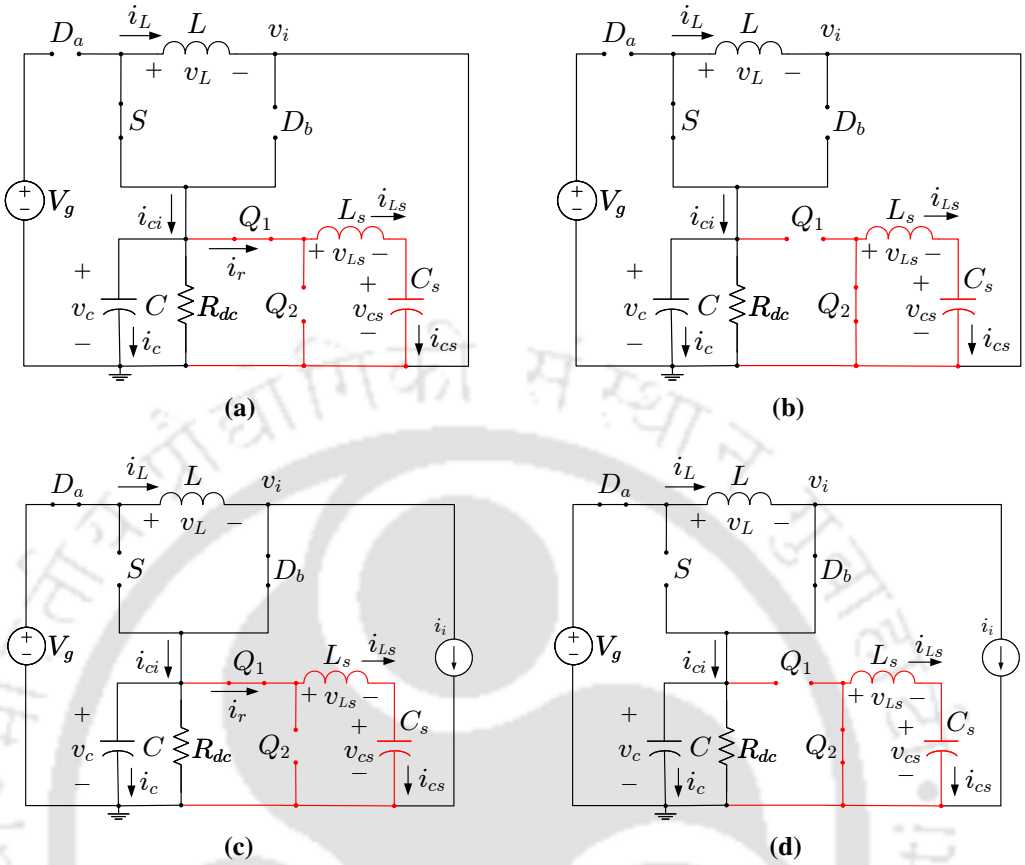


Fig. 2.11 Different modes of operation of single-phase SBI with buck-type APD network connected across the dc-link capacitor: (a) mode-1: SBI is in shoot-through state, Q_1 is on; (b) mode-2: SBI is in shoot-through state, Q_2 is on; (c) mode-3: SBI is in nonshoot-through state, Q_1 is on; (d) mode-4: SBI is in nonshoot-through state and Q_2 is on.

During shoot-through, the analytical equations are given in (2.1), which is modified as:

$$\begin{aligned} v_L(t) &= v_c(t) \\ i_c(t) &= -i_L(t) - i_{dc}(t) - i_{Ls}(t) \\ v_i(t) &= 0 \end{aligned} \tag{2.54}$$

During nonshoot-through, the analytical equations are given in (2.2), which is modified as:

$$\begin{aligned} v_L(t) &= V_g - v_c(t) \\ i_c(t) &= i_L(t) - i_i(t) - i_{dc}(t) - i_{Ls}(t) \\ v_i(t) &= v_c(t) \end{aligned} \tag{2.55}$$

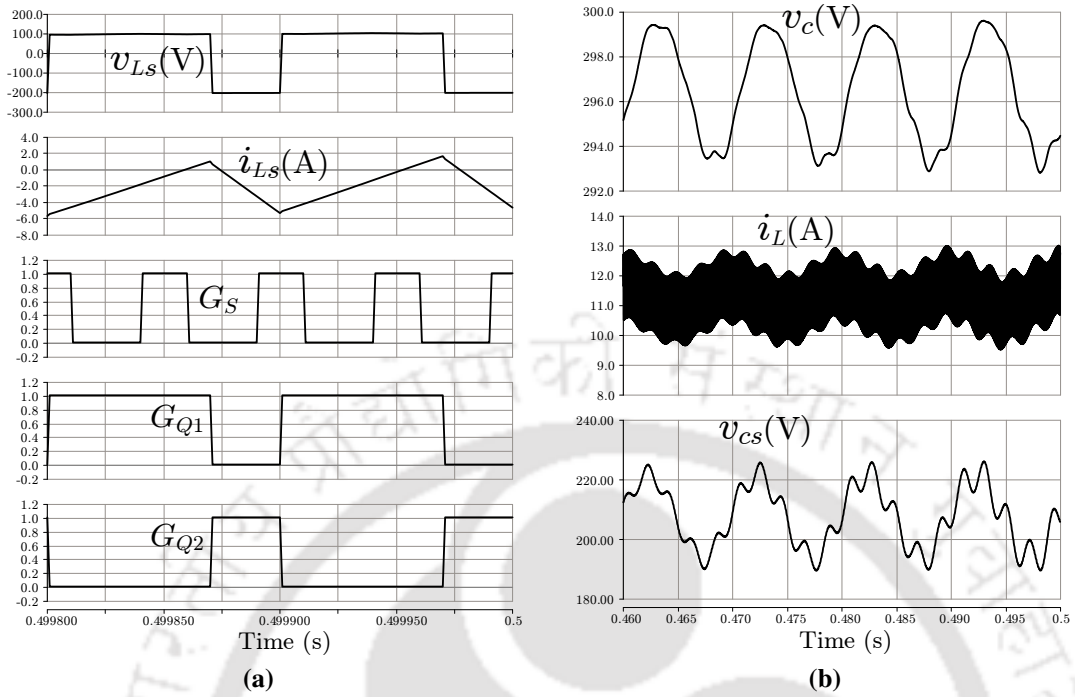


Fig. 2.12 Simulation results of single-phase SBI with buck-type APD network connected across the dc-link capacitor.

However, (2.54) is valid in mode-1, and (2.55) is valid in mode-3 of buck-type APD-integrated SBI. In modes 2 and 4, (2.1) and (2.2) are valid, because turning off the switch Q_1 disconnects the APD network from the SBI.

The theoretical analysis is verified in simulation with the parameters given in Table 2.2. The auxiliary inductor L_s is taken as 1 mH, and the auxiliary capacitor C_s is chosen as 220 µF. The APD switching frequency is 20 kHz. The simulation results are shown in Fig. 2.12. The auxiliary inductor voltage v_{Ls}, the auxiliary inductor current i_{Ls}, the gate signals of the switches S, Q_1 and Q_2, i.e., G_S, G_{Q1} and G_{Q2}, respectively, are plotted in Fig. 2.12(a). It is observed when G_{Q1} is high, and G_{Q2} is low, L_s is charged as the slope of i_{Ls} is positive. The approximate voltage across L_s is 100 V, which is equal to $(v_c - v_{cs})$. Similarly, when G_{Q1} is low, and G_{Q2} is high, L_s is discharged as the slope of i_{Ls} is negative. The approximate voltage across L_s is -200 V, which is equal to $-v_{cs}$. When G_S becomes high, both charging and discharging of L_s remains unaffected by the shoot-through state, unlike the buck-type APD network connected across the dc-link as shown in Fig. 2.9(a).

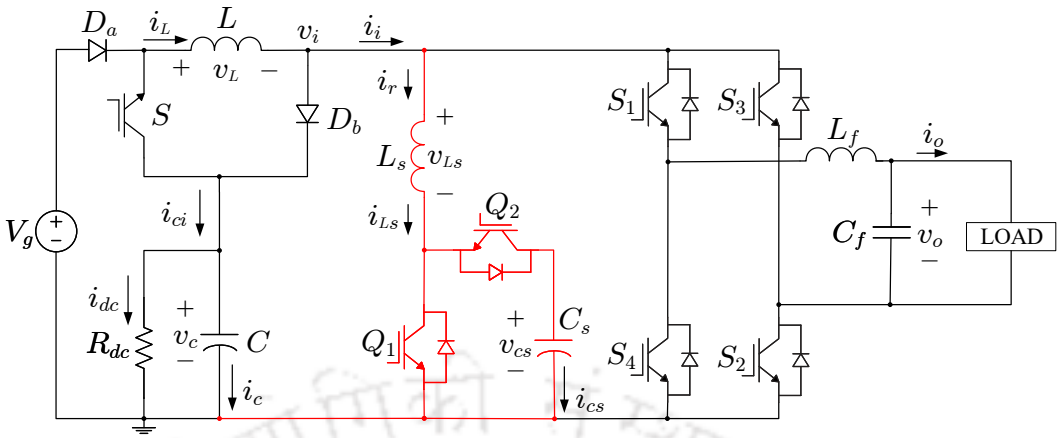


Fig. 2.13 Circuit diagram of SBI with boost-type APD connected across the dc-link.

In Fig. 2.12(b), the waveforms of the dc-link capacitor voltage v_c, the active-front-end network inductor current i_L and the auxiliary capacitor voltage v_{cs} are plotted. The average value of v_c is 296 V, and the average value of v_{cs} is 205 V, which indicates the APD functions in buck-mode. The peak-to-peak ripple of v_c is 6 V, and the peak-to-peak ripple of i_L is 3 A, which suggests the amount of ripple is reduced compared to the buck-type APD network connected across the dc-link as shown in Fig. 2.9(b).

2.4.2 Boost-type APD

As the name suggests, the auxiliary capacitor voltage v_{cs} is maintained above the dc-link capacitor voltage v_c in this APD topology.

A) Boost-type APD network connected across the dc-link

The circuit diagram of the single-phase SBI with boost-type APD network connected across the dc-link is illustrated in Fig. 2.13. The equivalent circuit diagrams of different operational modes are shown in Fig. 2.14.

Mode-1: As shown in Fig. 2.14(a), in this mode, Q_1 is turned on and Q_2 is turned off, while the SBI is in shoot-through state. The auxiliary inductor L_s is shorted, and the auxiliary capacitor C_s is open-circuited. So, both L_s and C_s are neither charged nor discharged in this mode. Thus, the APD network does not function as intended in this mode, because one of the

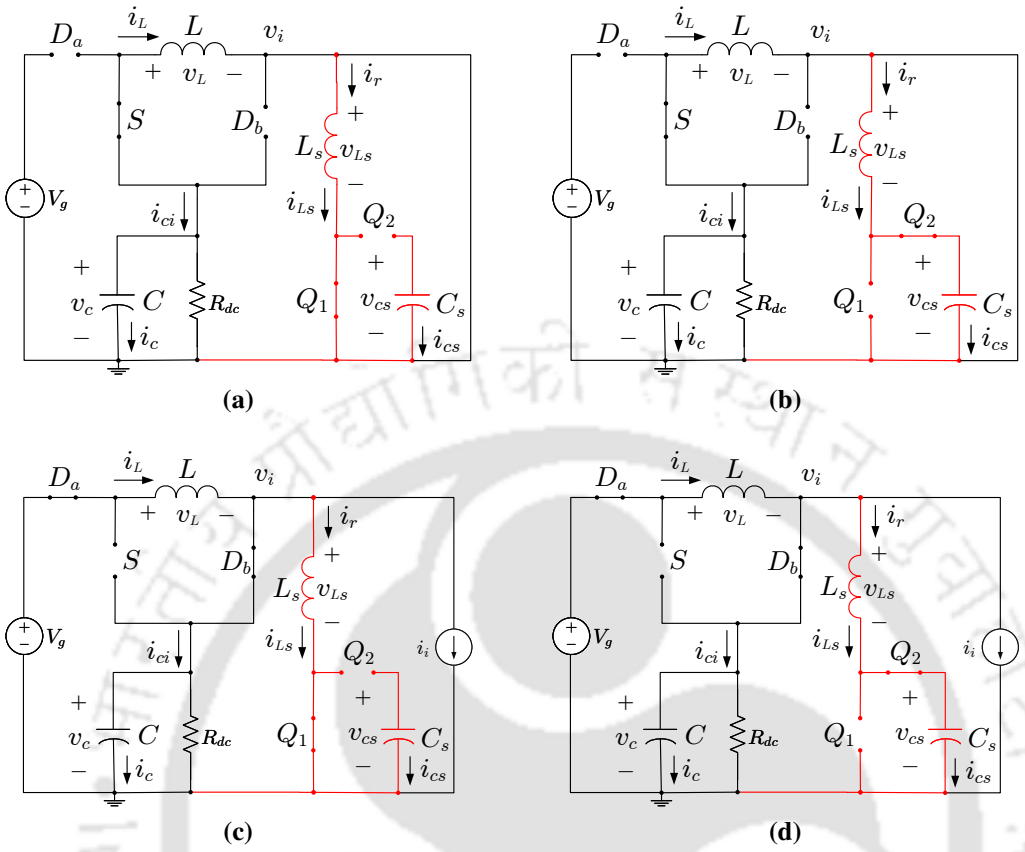


Fig. 2.14 Different modes of operation of single-phase SBI with boost-type APD network connected across the dc-link: (a) mode-1: SBI is in shoot-through state, Q_1 is on; (b) mode-2: SBI is in shoot-through state, Q_2 is on; (c) mode-3: SBI is in nonshoot-through state, Q_1 is on; (d) mode-4: SBI is in nonshoot-through state, Q_2 is on.

inverter leg is shorted. Since the APD functionality becomes dependent on the inverter in this mode, this is an undesired mode of operation.

Mode-2: In this mode, Q_1 turned off and Q_2 is turned on, L_s is discharged and C_s is charged by L_s as observed in Fig. 2.14(b). As the SBI is in shoot-through state, the APD network goes into this mode. Therefore, the APD functionality remains dependent of the inverter, similar to mode-1. Hence, this is also an undesired mode of operation. This indicates during the complete shoot-through interval, the APD network cannot function as intended.

Mode-3: This mode is similar to the operation of APD when it is connected across the dc-link of a conventional VSI, because the SBI operates in the nonshoot-through state. In this mode, C charges L_s by turning on the switch Q_1, as shown in Fig. 2.14(c). In this mode, the ripple energy of C is transferred to L_s. As L_s is not utilized as a ripple energy storage device over a switching period, the energy stored by L_s in this mode is discharged to C_s in mode-4.

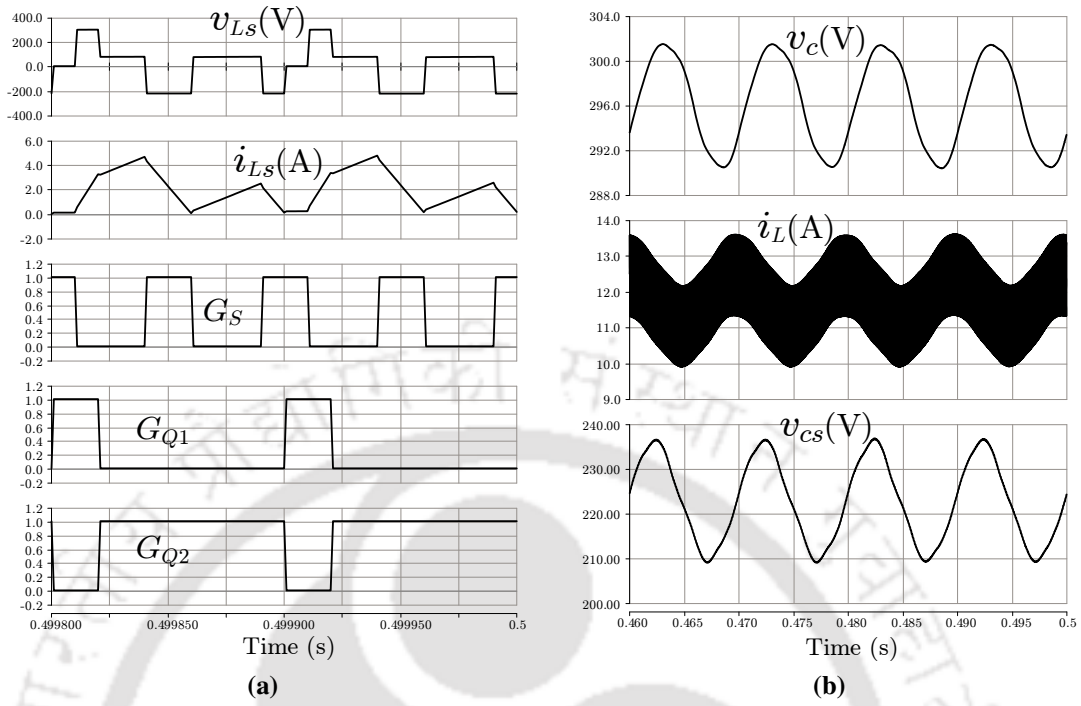


Fig. 2.15 Simulation results of single-phase SBI with boost-type APD connected across the dc-link.

In this mode, the APD functionality remains independent of the inverter, because the ripple energy of C is only transferred without affecting the steady-state operation.

Mode-4: Similar to mode-3, the SBI operates in nonshoot-through. The ripple energy of C is deflected to C_s as it is charged by both C and L_s, as observed in Fig. 2.14(d). Similar to mode-3, the APD functionality also remains independent of the inverter in this mode, because the ripple energy of C is only transferred without affecting the steady-state operation.

The undesired modes of operation are also verified in simulation with the parameters given in Table 2.2. The auxiliary inductor L_s is taken as 1 mH, and the auxiliary capacitor C_s is chosen as 220 µF. The APD switching frequency is 20 kHz. The simulation results are shown in Fig. 2.15. The auxiliary inductor voltage v_{Ls}, the auxiliary inductor current i_{Ls}, the gate signals of the switches S, Q_1 and Q_2, i.e., G_S, G_{Q1} and G_{Q2}, respectively, are plotted in Fig. 2.15(a). It is observed that during shoot-through state, when G_S and G_{Q1} are high simultaneously, v_{Ls} is zero, and the slope of i_{Ls} does not change, indicating that L_s is neither charged nor discharged. Conventionally, in boost-type APD, Q_1 is turned on to charge

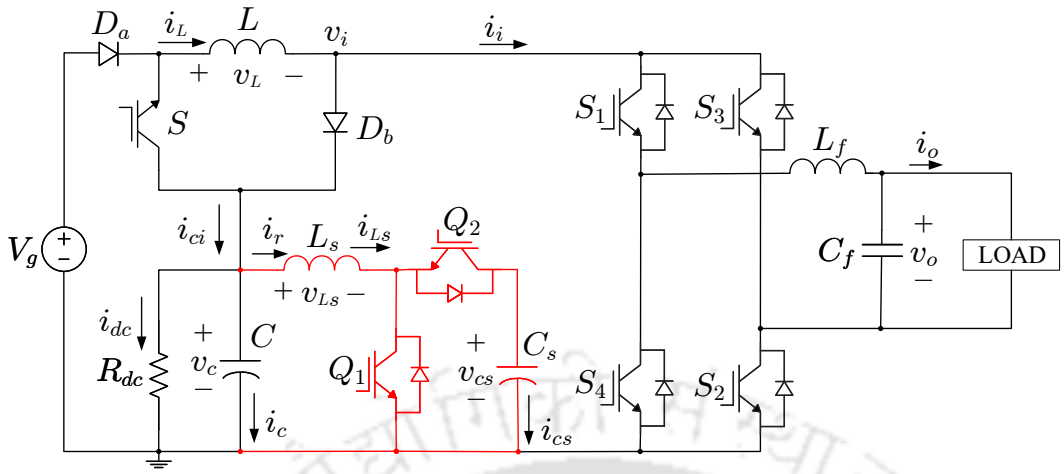


Fig. 2.16 Circuit diagram of SBI with boost-type APD connected across the dc-link capacitor.

L_s with the deflected ripple energy of C. But the shoot-through state of SBI interrupts the charging of L_s indicating that the operation of APD is impacted by the inverter operation.

Similarly, when G_S and G_{Q2} are high, L_s is discharged, as i_{Ls} has a negative slope. Conventionally, in boost-type APD, Q_2 is turned on to facilitate the charging of C_s by both C and L_s. However, due to the interruptions caused by the shoot-through states, v_{cs} actually could not boosted. A lower v_{cs} results in charging of L_s when Q_2 is turned on. Thus, the APD fails to function as intended owing to interaction with the shoot-through state of SBI.

In Fig. 2.15(b), the waveforms of the dc-link capacitor voltage v_c, the active-front-end network inductor current i_L and the auxiliary capacitor voltage v_{cs} are plotted. The average value of v_c is 296 V, and the average value of v_{cs} is 222 V, which indicates the APD actually functions in buck-mode instead of operating in the boost-mode, because of the interruptions caused by the shoot-through states of SBI. The peak-to-peak ripple of v_c is 10 V, and the peak-to-peak ripple of i_L is 3.5 A. The amount of ripple can be reduced further if the boost-type APD network is connected across the dc-link capacitor.

B) Boost-type APD network connected across the dc-link capacitor

The circuit diagram of the single-phase SBI with boost-type APD network connected across the dc-link capacitor C is illustrated in Fig. 2.16. As shown in Fig. 2.17, the SBI is in shoot-through state in modes 1 and 2, and is in nonshoot-through state in modes 3 and 4.

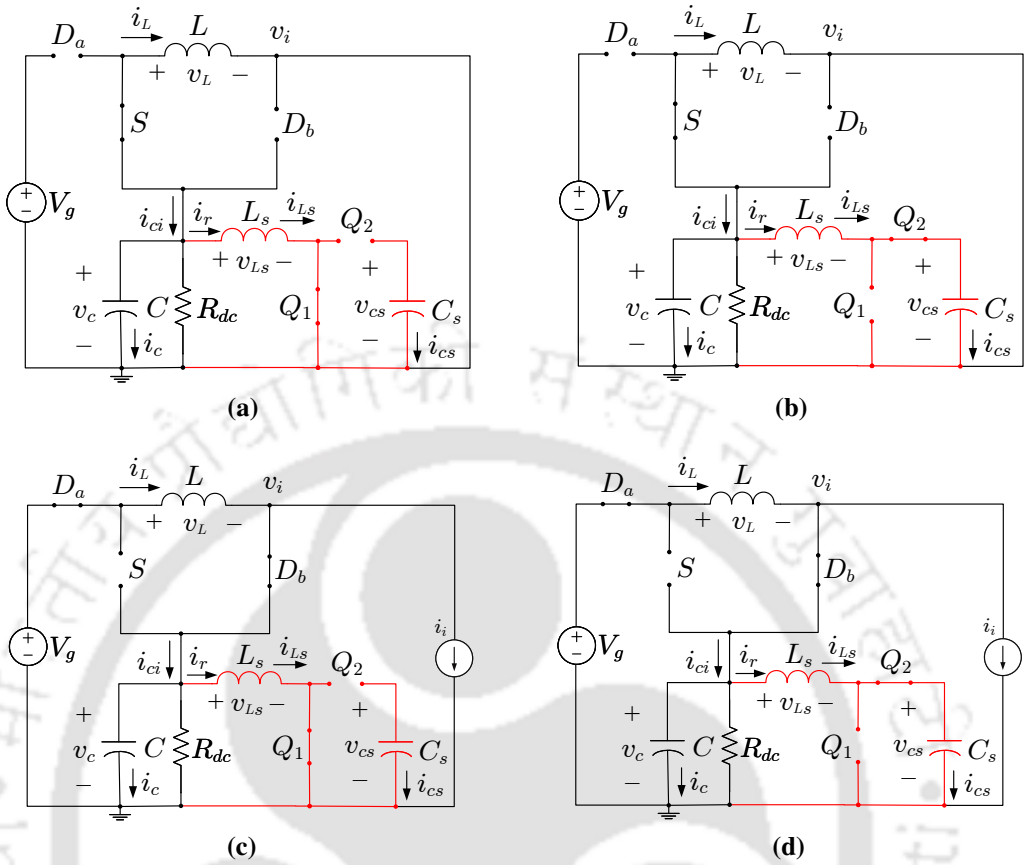


Fig. 2.17 Different modes of operation of single-phase SBI with boost-type APD network connected across the dc-link capacitor: (a) mode-1: SBI is in shoot-through state, Q_1 is on; (b) mode-2: SBI is in shoot-through state, Q_2 is on; (c) mode-3: SBI is in nonshoot-through state, Q_1 is on; (d) mode-4: SBI is in nonshoot-through state, Q_2 is on.

However, the state of the inverter does not impact the APD functionality. In modes 1 and 3, when Q_1 is turned on, and Q_2 is turned off, L_s is charged by C. Hence, i_r is same as i_{Ls}. Note that i_{cs} becomes zero indicating no change in the voltage across C_s. The ripple energy is stored in L_s in this interval. So, the mathematical equations are obtained as:

$$\begin{aligned} v_{Ls}(t) &= v_c(t) \\ i_{cs}(t) &= 0 \\ i_r(t) &= i_{Ls}(t) \end{aligned} \tag{2.56}$$

In modes 2 and 4, when Q_1 is turned off, and Q_2 is turned on, C_s is charged by both C and L_s, which indicates ripple energy discharge of L_s stored from C during previous interval.

Here, i_r is same as i_{Ls} and i_{cs}. Thus, the ripple energy is deflected from C to C_s and is stored in C_s, while L_s does not store any energy over a complete switching period. The mathematical equations during this time interval are written as:

$$\begin{aligned} v_{Ls}(t) &= v_c(t) - v_{cs}(t) \\ i_{cs}(t) &= i_{Ls}(t) \\ i_r(t) &= i_{Ls}(t) \end{aligned} \tag{2.57}$$

During shoot-through, the analytical equations are given in (2.1), which is modified as:

$$\begin{aligned} v_L(t) &= v_c(t) \\ i_c(t) &= -i_L(t) - i_{dc}(t) - i_{Ls}(t) \\ v_i(t) &= 0 \end{aligned} \tag{2.58}$$

During nonshoot-through, the analytical equations are given in (2.2), which is modified as:

$$\begin{aligned} v_L(t) &= V_g - v_c(t) \\ i_c(t) &= i_L(t) - i_i(t) - i_{dc}(t) - i_{Ls}(t) \\ v_i(t) &= v_c(t) \end{aligned} \tag{2.59}$$

Note that (2.58) is valid for modes 1 and 2 of boost-type APD-integrated SBI. Similarly, for modes 3 and 4, (2.59) is valid.

The theoretical analysis is verified in simulation with the parameters given in Table 2.2. The auxiliary inductor L_s is taken as 1 mH, and the auxiliary capacitor C_s is chosen as 220 µF. The APD switching frequency is 20 kHz. The simulation results are shown in Fig. 2.18. The auxiliary inductor voltage v_{Ls}, the auxiliary inductor current i_{Ls}, the gate signals of the switches S, Q_1 and Q_2, i.e., G_S, G_{Q1} and G_{Q2}, respectively, are plotted in Fig. 2.18(a). It is observed when G_{Q1} is high, and G_{Q2} is low, L_s is charged as the slope of i_{Ls} is positive. The approximate voltage across L_s is 300 V, which is equal to v_c. Similarly, when G_{Q1} is low, and G_{Q2} is high, L_s is discharged as the slope of i_{Ls} is negative. The approximate voltage across

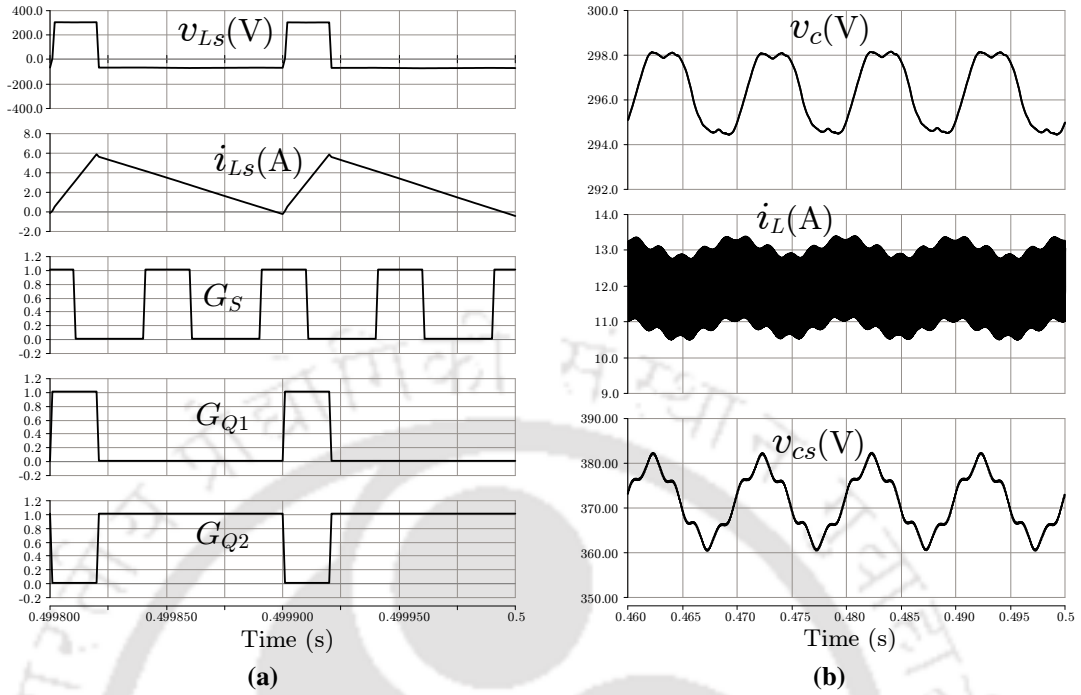


Fig. 2.18 Simulation results of single-phase SBI with boost-type APD connected across the dc-link capacitor.

L_s is -100 V, which is equal to $(v_c - v_{cs})$. Since v_{cs} is more than v_c in boost-type APD, v_{Ls} becomes negative in this case. When G_S becomes high, both charging and discharging of L_s remains unaffected by the shoot-through state, unlike the boost-type APD network connected across the dc-link as shown in Fig. 2.15(a).

In Fig. 2.18(b), the waveforms of the dc-link capacitor voltage v_c, the active-front-end network inductor current i_L and the auxiliary capacitor voltage v_{cs} are plotted. The average value of v_c is 296 V, and the average value of v_{cs} is 372 V, which indicates the APD functions in boost-mode. The peak-to-peak ripple of v_c is 3.5 V, and the peak-to-peak ripple of i_L is 3 A, which suggests the amount of ripple is reduced compared to the boost-type APD network connected across the dc-link as shown in Fig. 2.15(b).

2.4.3 Buck-boost-type APD

As the name suggests, the auxiliary capacitor voltage v_{cs} can be maintained above or below the dc-link capacitor voltage v_c, depending on the duty ratio of the switch Q_1, in this APD topology.

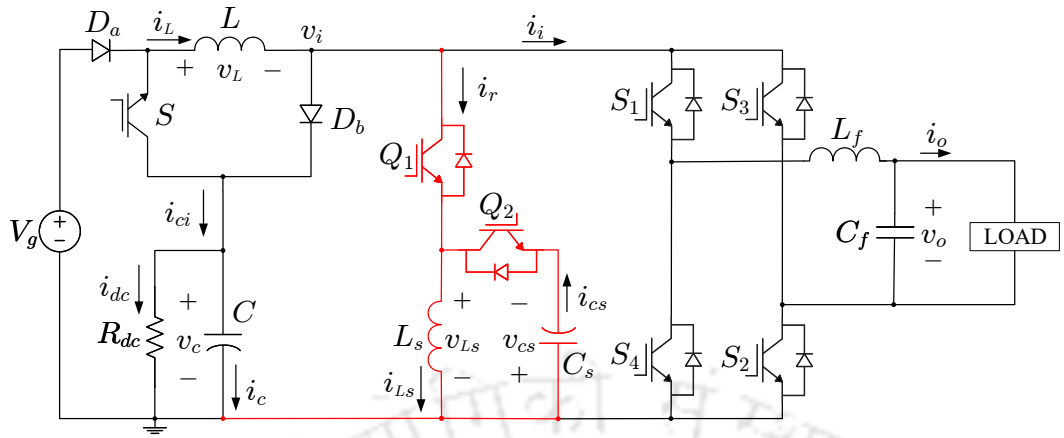


Fig. 2.19 Circuit diagram of SBI with buck-boost-type APD connected across the dc-link.

A) Buck-boost-type APD network connected across the dc-link

The circuit diagram of the single-phase SBI with buck-boost-type APD network connected across the dc-link is illustrated in Fig. 2.19. The equivalent circuit diagrams of different operational modes are shown in Fig. 2.20.

Mode-1: As shown in Fig. 2.20(a), in this mode, Q_1 is turned on and Q_2 is turned off, while the SBI is in shoot-through state. The auxiliary inductor L_s is shorted, and the auxiliary capacitor C_s is open-circuited. So, both L_s and C_s are neither charged nor discharged in this mode. Thus, the APD network does not function as intended in this mode, because one of the inverter leg is shorted. Since the APD functionality becomes dependent on the inverter in this mode, this is an undesired mode of operation.

Mode-2: In this mode, Q_1 turned off and Q_2 is turned on, L_s is discharged and C_s is charged by L_s as observed in Fig. 2.20(b). Although the SBI is in shoot-through state, the APD network is disconnected from the inverter in this mode. Therefore, the APD functionality remains independent of the inverter.

Mode-3: This mode is similar to the operation of APD when it is connected across the dc-link of a conventional VSI, because the SBI operates in the nonshoot-through state. In this mode, C charges L_s by turning on the switch Q_1, as shown in Fig. 2.20(c). In this mode, the ripple energy of C is transferred to L_s. As L_s is not utilized as a ripple energy storage device over a switching period, the energy stored by L_s in this mode is discharged to C_s in modes 2

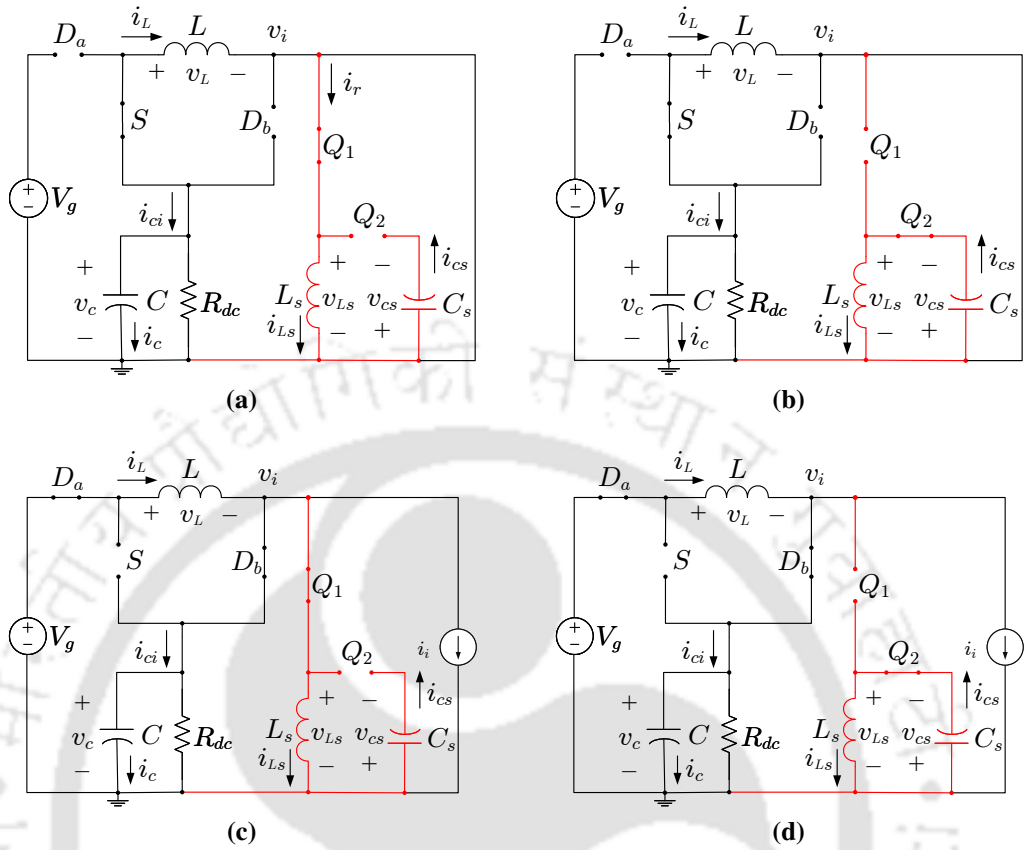


Fig. 2.20 Different modes of operation of single-phase SBI with buck-boost-type APD network connected across dc-link: (a) mode-1: SBI is in shoot-through state, Q_1 is on; (b) mode-2: SBI is in shoot-through state, Q_2 is on; (c) mode-3: SBI is in nonshoot-through state, Q_1 is on; (d) mode-4: SBI is in nonshoot-through state, Q_2 is on.

and 4. In this mode, the APD functionality remains independent of the inverter, because the ripple energy of C is only transferred without affecting the steady-state operation.

Mode-4: Similar to mode-2, in this mode, Q_1 turned off and Q_2 is turned on, L_s is discharged and C_s is charged by L_s. The SBI operates in nonshoot-through, but the APD network is disconnected from the inverter in this mode, as observed in Fig. 2.20(d). Therefore, the APD functionality remains independent of the inverter.

The undesired modes of operation are also verified in simulation with the parameters given in Table 2.2. The auxiliary inductor L_s is taken as 1.5 mH, and the auxiliary capacitor C_s is chosen as 220 µF. The APD switching frequency is 20 kHz. The simulation results are shown in Fig. 2.21. The auxiliary inductor voltage v_{Ls}, the auxiliary inductor current i_{Ls}, the gate signals of the switches S, Q_1 and Q_2, i.e., G_S, G_{Q1} and G_{Q2}, respectively, are plotted in Fig. 2.21(a). It is observed that during shoot-through state, when G_S and G_{Q1} are

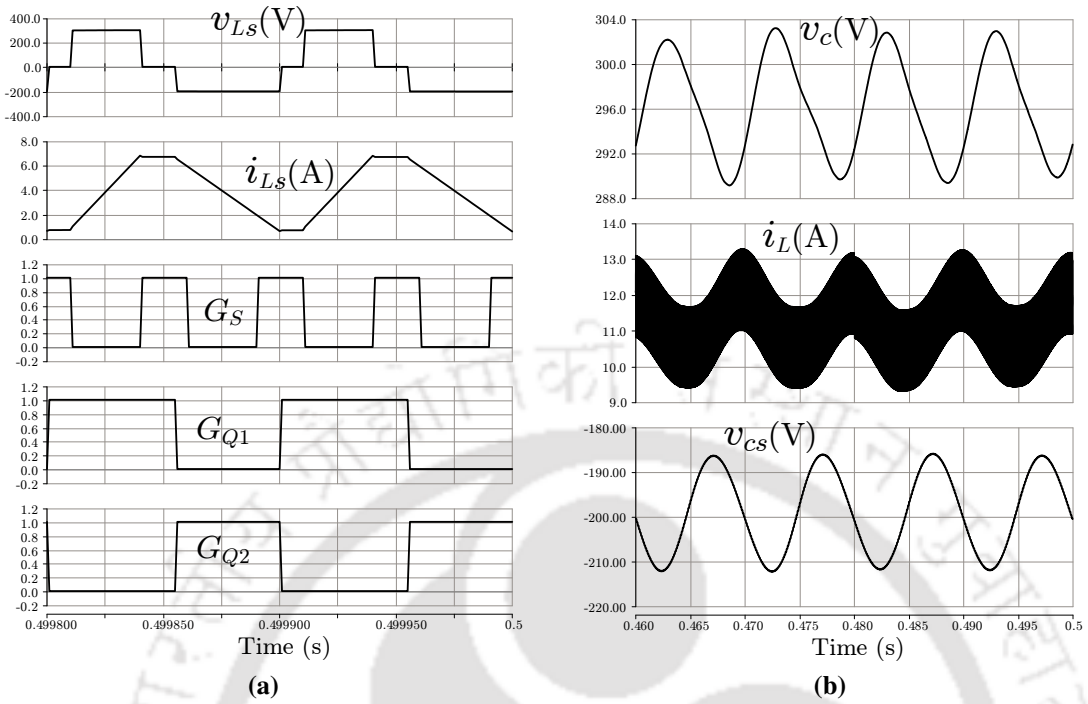


Fig. 2.21 Simulation results of single-phase SBI with buck-boost-type APD connected across the dc-link.

high simultaneously, v_{Ls} is zero, and the slope of i_{Ls} does not change, indicating that L_s is neither charged nor discharged. Conventionally, in boost-type APD, Q_1 is turned on to charge L_s with the deflected ripple energy of C. But the shoot-through state of SBI interrupts the charging of L_s indicating that the operation of APD is impacted by the inverter operation.

Similarly, when G_S and G_{Q2} are high, L_s is discharged, as i_{Ls} has a negative slope. Conventionally, in boost-type APD, Q_2 is turned on to facilitate the charging of C_s by both C and L_s. However, due to the interruptions caused by the shoot-through states, v_{cs} actually could not be boosted. A lower v_{cs} results in charging of L_s when Q_2 is turned on. Thus, the APD fails to function as intended owing to interaction with the shoot-through state of SBI.

In Fig. 2.21(b), the waveforms of the dc-link capacitor voltage v_c, the active-front-end network inductor current i_L and the auxiliary capacitor voltage v_{cs} are plotted. The average value of v_c is 296 V, and the average value of v_{cs} is 120 V, which indicates the APD functions in buck-mode, because of the interruptions caused by the shoot-through states of SBI. As the duty ratio of Q_1 is taken as 0.55, the APD should have operated in boost-mode. The peak-to-peak ripple of v_c is 12 V, and the peak-to-peak ripple of i_L is 4 A. The amount of

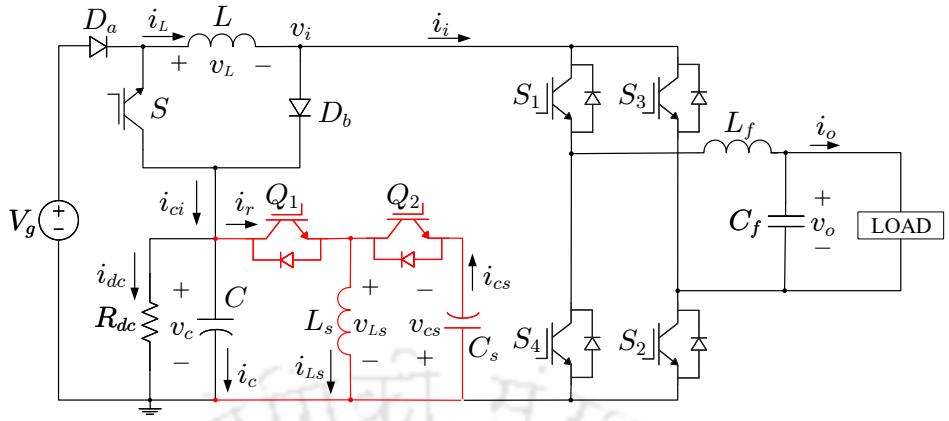


Fig. 2.22 Circuit diagram of SBI with buck-boost-type APD connected across the dc-link capacitor.

ripple can be reduced further if the APD network is connected across the dc-link capacitor as discussed in the following.

B) Buck-Boost-type APD network connected across the dc-link capacitor

The circuit diagram of the single-phase SBI with buck-boost-type APD network connected across the dc-link capacitor C is illustrated in Fig. 2.22. As shown in Fig. 2.17, the SBI is in shoot-through state in modes 1 and 2, and is in nonshoot-through state in modes 3 and 4. However, the state of the inverter does not impact the APD functionality. In modes 1 and 3, when Q_1 is turned on, and Q_2 is turned off, L_s is charged by C, and i_r is same as i_{Ls}. Since i_{cs} is zero, there is no change in v_{cs}. The mathematical equations during this time interval can be obtained as:

$$\begin{aligned} v_{Ls}(t) &= v_c(t) \\ i_{cs}(t) &= 0 \\ i_r(t) &= i_{Ls}(t) \end{aligned} \tag{2.60}$$

In modes 2 and 4, when Q_1 is turned off, and Q_2 is turned on, the auxiliary capacitor C_s is charged by the auxiliary inductor L_s. As Q_1 is turned off, the APD network is essentially disconnected from SBI. In this interval, L_s transfers the ripple energy to C_s, which was stored from C in the previous interval. Thus, the ripple energy is transferred from C to C_s via L_s.

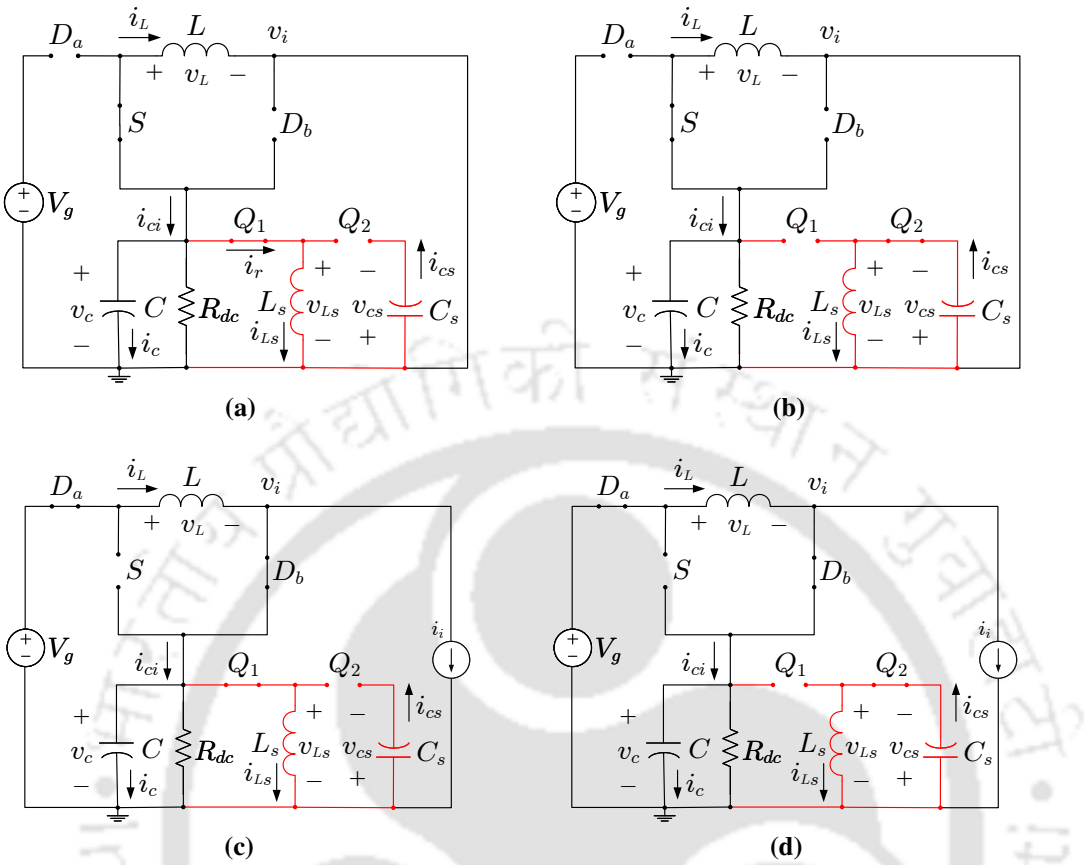


Fig. 2.23 Different modes of operation of single-phase SBI with buck-boost-type APD network connected across the dc-link capacitor: (a) mode-1: SBI is in shoot-through state, Q_1 is on; (b) mode-2: SBI is in shoot-through state, Q_2 is on; (c) mode-3: SBI is in nonshoot-through state, Q_1 is on; (d) mode-4: SBI is in nonshoot-through state and Q_2 is on.

Therefore, the mathematical equations in this time interval are obtained as:

$$\begin{aligned} v_{Ls}(t) &= -v_{cs}(t) \\ i_{cs}(t) &= i_{Ls}(t) \\ i_r(t) &= 0 \end{aligned} \tag{2.61}$$

During shoot-through, the analytical equations are given in (2.1), which is modified as:

$$\begin{aligned} v_L(t) &= v_c(t) \\ i_c(t) &= -i_L(t) - i_{dc}(t) - i_{Ls}(t) \\ v_i(t) &= 0 \end{aligned} \tag{2.62}$$

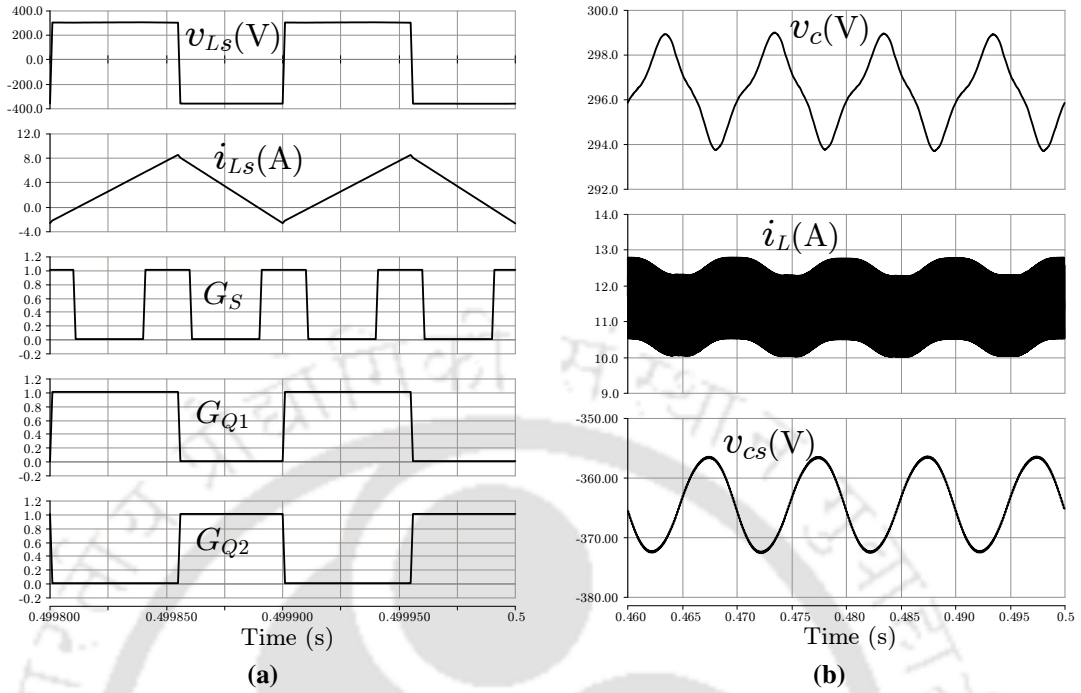


Fig. 2.24 Simulation results of single-phase SBI with buck-boost-type APD network connected across the dc-link capacitor.

During nonshoot-through, the analytical equations are given in (2.2), which is modified as:

$$\begin{aligned} v_L(t) &= V_g - v_c(t) \\ i_c(t) &= i_L(t) - i_i(t) - i_{dc}(t) - i_{Ls}(t) \\ v_i(t) &= v_c(t) \end{aligned} \tag{2.63}$$

However, (2.62) is valid in mode-1, and (2.63) is valid in mode-3 of buck-boost-type APD-integrated SBI. In modes 2 and 4, (2.1) and (2.2) are valid, because turning off the switch Q_1 disconnects the APD network from the SBI.

The theoretical analysis is verified in simulation with the parameters given in Table 2.2. The auxiliary inductor L_s is taken as 1.5 mH, and the auxiliary capacitor C_s is chosen as 220 µF. The APD switching frequency is 20 kHz. The simulation results are shown in Fig. 2.24. The auxiliary inductor voltage v_{Ls}, the auxiliary inductor current i_{Ls}, the gate signals of the switches S, Q_1 and Q_2, i.e., G_S, G_{Q1} and G_{Q2}, respectively, are plotted in Fig. 2.24(a). It is observed when G_{Q1} is high, and G_{Q2} is low, L_s is charged as the slope of i_{Ls} is positive. The

approximate voltage across L_s is 300 V, which is equal to v_c. Similarly, when G_{Q1} is low, and G_{Q2} is high, L_s is discharged as the slope of i_{Ls} is negative. The approximate voltage across L_s is -365 V, which is equal to $-v_{cs}$. When G_S becomes high, both charging and discharging of L_s remains unaffected by the shoot-through state, unlike the buck-boost-type APD network connected across the dc-link as shown in Fig. 2.21(a).

In Fig. 2.24(b), the waveforms of the dc-link capacitor voltage v_c, the active-front-end network inductor current i_L and the auxiliary capacitor voltage v_{cs} are plotted. The average value of v_c is 296 V, and the average value of v_{cs} is 365 V, which indicates the APD functions in boost-mode. The peak-to-peak ripple of v_c is 5 V, and the peak-to-peak ripple of i_L is 2.75 A, which suggests the amount of ripple is reduced compared to the buck-boost-type APD network connected across the dc-link as shown in Fig. 2.21(b).

2.5 LOW-FREQUENCY RIPPLE ANALYSIS AND DESIGN OF PASSIVE ELEMENTS OF APD-INTEGRATED SBI

As discussed in Section 2.4, the connection of the APD network across the dc-link in SBI possesses unintentional issues in different ways in all three APD topologies owing to the shoot-through state of the SBI. Therefore, the low-frequency ripple reduction functionality of the APD networks is significantly hampered. As a solution, the APD networks are connected across the dc-link capacitor. In this section, the low-frequency ripple analysis of APD-integrated SBI topologies is illustrated, considering the APD networks are connected across the dc-link capacitor.

2.5.1 Low-frequency ripple analysis

A) With buck-type APD

Fig. 2.10 shows the circuit diagram of the single-phase SBI with buck-type APD network connected across the dc-link capacitor. Similar to Section 2.3, the ac modeling approach is also applied to (2.52) and (2.53) so that the small-signal equations of the APD network can

be obtained as follows:

$$\begin{aligned} L_s\frac{d}{dt}\{I_{Ls}+\tilde{i}_{Ls}(t)\} &= D_a\cdot\{V_c+\tilde{v}_c(t)\}-\{V_{cs}+\tilde{v}_{cs}(t)\} \\ C_s\frac{d}{dt}\{V_{cs}+\tilde{v}_{cs}(t)\} &= I_{Ls}+\tilde{i}_{Ls}(t) \\ I_r+\tilde{i}_r(t) &= D_a\cdot\{I_{Ls}+\tilde{i}_{Ls}(t)\} \end{aligned} \tag{2.64}$$

where the turn on duration of Q_1 is $D_a\cdot T_s$. Here, D_a is considered as constant. It is assumed that the switching frequencies of the APD switches and the switch S are the same. Also, R_{dc} is not considered as it does not contribute to the low-frequency ripple. In steady-state, the following expressions are obtained

$$\begin{aligned} V_{cs} &= D_a\cdot V_c \\ I_r &= D_a\cdot I_{Ls}=0 \end{aligned} \tag{2.65}$$

The dynamic equations of the APD network are found to be

$$\begin{aligned} L_s\frac{d\tilde{i}_{Ls}(t)}{dt} &= D_a\cdot\tilde{v}_c(t)-\tilde{v}_{cs}(t) \\ C_s\frac{d\tilde{v}_{cs}(t)}{dt} &= \tilde{i}_{Ls}(t) \\ \tilde{i}_r(t) &= D_a\cdot\tilde{i}_{Ls}(t) \end{aligned} \tag{2.66}$$

Also, the dynamic equations of SBI from (2.21) are modified as

$$\begin{aligned} L\frac{d\tilde{i}_L(t)}{dt} &= -(1-2D)\cdot\tilde{v}_c(t) \\ C\frac{d\tilde{v}_c(t)}{dt} &= (1-2D)\cdot\tilde{i}_L(t)-(1-D)\cdot\tilde{i}_i(t)-D_a\cdot\tilde{i}_{Ls}(t) \end{aligned} \tag{2.67}$$

Following the procedure presented in Section 2.3, $\tilde{i}_L$ and $\tilde{v}_c$ of the buck-type APD-integrated SBI are derived as

$$\begin{aligned} \tilde{i}_L(t) &= \frac{(1-2D)MI_o}{\sqrt{2}[4LC\omega_o^2-(1-2D)^2+k_t]}\cos(2\omega_o t-\varphi) \\ \tilde{v}_c(t) &= \frac{\sqrt{2}\omega_o LMI_o}{[4LC\omega_o^2-(1-2D)^2+k_t]}\sin(2\omega_o t-\varphi) \end{aligned} \tag{2.68}$$

where

$$k_t = \frac{4\omega_o^2 L C_s D_a^2}{1 - 4\omega_o^2 L_s C_s}. \tag{2.69}$$

The auxiliary capacitor voltage ripple $\tilde{v}_{cs}$ is generally in phase with low-frequency ripple component $\tilde{v}_c$ indicating transfer of ripple energy from C to C_s. The expression of $\tilde{v}_{cs}$ can be written for buck-type APD topology as follows:

$$\tilde{v}_{cs}(t) = \frac{D_a}{1 - 4\omega_o^2 L_s C_s} \cdot \tilde{v}_c(t). \tag{2.70}$$

The ripple current i_r, which is generally in phase with inductor current ripple $\tilde{i}_L$, is expressed for buck-type APD topology as follows:

$$i_r(t) = \tilde{i}_r(t) = \frac{4\omega_o^2 L C_s D_a^2}{\sqrt{2}(1 - 4\omega_o^2 L_s C_s)} \cdot \tilde{i}_L(t). \tag{2.71}$$

B) with boost-type APD

Fig. 2.16 shows the circuit diagram of the single-phase SBI with boost-type APD network connected across the dc-link capacitor. The ac modeling approach is applied to (2.56) and (2.57) so that the small-signal equations of the APD network can be obtained as follows:

$$\begin{aligned} L_s \frac{d}{dt}\{I_{Ls} + \tilde{i}_{Ls}(t)\} &= \{V_c + \tilde{v}_c(t)\} - (1 - D_a) \cdot \{V_{cs} + \tilde{v}_{cs}(t)\} \\ C_s \frac{d}{dt}\{V_{cs} + \tilde{v}_{cs}(t)\} &= (1 - D_a) \cdot \{I_{Ls} + \tilde{i}_{Ls}(t)\} \\ I_r + \tilde{i}_r(t) &= I_{Ls} + \tilde{i}_{Ls}(t) \end{aligned} \tag{2.72}$$

Here, D_a is considered as constant. It is assumed that the switching frequencies of the APD switches and the switch S are the same. Also, R_{dc} is not considered as it does not contribute to the low-frequency ripple. In steady-state, the following expressions are obtained

$$\begin{aligned} V_{cs} &= \frac{V_c}{1 - D_a} \\ I_{Ls} &= I_r = 0 \end{aligned} \tag{2.73}$$

The dynamic equations of the APD network are found to be

$$\begin{aligned} L_s\frac{d\tilde{i}_{Ls}(t)}{dt} &= \tilde{v}_c(t) - (1-D_a)\cdot\tilde{v}_{cs}(t) \\ C_s\frac{d\tilde{v}_{cs}(t)}{dt} &= (1-D_a)\cdot\tilde{i}_{Ls}(t) \\ \tilde{i}_r(t) &= \tilde{i}_{Ls}(t). \end{aligned} \tag{2.74}$$

Also, the dynamic equations of SBI from (2.21) are modified as

$$\begin{aligned} L\frac{d\tilde{i}_L(t)}{dt} &= -(1-2D)\cdot\tilde{v}_c(t) \\ C\frac{d\tilde{v}_c(t)}{dt} &= (1-2D)\cdot\tilde{i}_L(t) - (1-D)\cdot\tilde{i}_i(t) - \tilde{i}_{Ls}(t). \end{aligned} \tag{2.75}$$

Following the procedure presented in Section 2.3, $\tilde{i}_L$ and $\tilde{v}_c$ of the boost-type APD-integrated SBI are derived as

$$\begin{aligned} \tilde{i}_L(t) &= \frac{(1-2D)MI_o}{\sqrt{2}[4LC\omega_o^2-(1-2D)^2+k_t]}\cos(2\omega_o t-\varphi) \\ \tilde{v}_c(t) &= \frac{\sqrt{2}\omega_o LMI_o}{[4LC\omega_o^2-(1-2D)^2+k_t]}\sin(2\omega_o t-\varphi) \end{aligned} \tag{2.76}$$

where

$$k_t = \frac{4\omega_o^2 LC_s}{(1-D_a)^2-4\omega_o^2 L_sC_s}. \tag{2.77}$$

The auxiliary capacitor voltage ripple $\tilde{v}_{cs}$ is generally in phase with low-frequency ripple component $\tilde{v}_c$ indicating transfer of ripple energy from C to C_s. The expression of $\tilde{v}_{cs}$ can be written for boost-type APD topology as follows:

$$\tilde{v}_{cs}(t) = \frac{D_a}{(1-D_a)^2-4\omega_o^2 L_sC_s}\cdot\tilde{v}_c(t). \tag{2.78}$$

The ripple current i_r, which is generally in phase with inductor current ripple $\tilde{i}_L$, is expressed for boost-type APD topology as follows:

$$i_r(t) = \tilde{i}_r(t) = \frac{4\omega_o^2 LC_s}{\sqrt{2}\{(1-D_a)^2-\omega_o^2 L_sC_s\}}\cdot\tilde{i}_L(t). \tag{2.79}$$

C) with buck-boost-type APD

Fig. 2.22 shows the circuit diagram of the single-phase SBI with buck-boost-type APD network connected across the dc-link capacitor. Similar to Section 2.3, the ac modeling approach is applied to (2.60) and (2.61) so that the small-signal equations of the APD network can be obtained as follows:

$$\begin{aligned} L_s\frac{d}{dt}\{I_{Ls}+\tilde{i}_{Ls}(t)\} &= D_a\cdot\{V_c+\tilde{v}_c(t)\}-(1-D_a)\cdot\{V_{cs}+\tilde{v}_{cs}(t)\} \\ C_s\frac{d}{dt}\{V_{cs}+\tilde{v}_{cs}(t)\} &= (1-D_a)\cdot\{I_{Ls}+\tilde{i}_{Ls}(t)\} \\ I_r+\tilde{i}_r(t) &= D_a\cdot\{I_{Ls}+\tilde{i}_{Ls}(t)\} \end{aligned} \tag{2.80}$$

Here, D_a is considered as constant. It is assumed that the switching frequencies of the APD switches and the switch S are the same. Also, the dc load R_{dc} is not considered, because it does not contribute to the low-frequency ripple. Therefore, in steady-state, the following expressions are obtained

$$\begin{aligned} V_{cs} &= \frac{D_a}{1-D_a}\cdot V_c \\ I_{Ls} &= D_a\cdot I_r = 0 \end{aligned} \tag{2.81}$$

The dynamic equations of the APD network are found to be

$$\begin{aligned} L_s\frac{d\tilde{i}_{Ls}(t)}{dt} &= D_a\cdot\tilde{v}_c(t)-(1-D_a)\cdot\tilde{v}_{cs}(t) \\ C_s\frac{d\tilde{v}_{cs}(t)}{dt} &= (1-D_a)\cdot\tilde{i}_{Ls}(t) \\ \tilde{i}_r(t) &= D_a\cdot\tilde{i}_{Ls}(t). \end{aligned} \tag{2.82}$$

Also, the dynamic equations of SBI from (2.21) are modified as

$$\begin{aligned} L\frac{d\tilde{i}_L(t)}{dt} &= -(1-2D)\cdot\tilde{v}_c(t) \\ C\frac{d\tilde{v}_c(t)}{dt} &= (1-2D)\cdot\tilde{i}_L(t)-(1-D)\cdot\tilde{i}_i(t)-D_a\cdot\tilde{i}_{Ls}(t) \end{aligned} \tag{2.83}$$

Following the procedure presented in Section 2.3, $\tilde{i}_L$ and $\tilde{v}_c$ of the buck-boost-type APD-integrated SBI are derived as

$$\begin{aligned}\tilde{i}_L(t) &= \frac{(1-2D)MI_o}{\sqrt{2}[4LC\omega_o^2-(1-2D)^2+k_t]}\cos(2\omega_o t-\varphi)\\ \tilde{v}_c(t) &= \frac{\sqrt{2}\omega_o LMI_o}{[4LC\omega_o^2-(1-2D)^2+k_t]}\sin(2\omega_o t-\varphi)\end{aligned} \tag{2.84}$$

where

$$k_t = \frac{4\omega_o^2 LC_s D_a^2}{(1-D_a)^2-4\omega_o^2 L_s C_s}. \tag{2.85}$$

The auxiliary capacitor voltage ripple $\tilde{v}_{cs}$ is generally in phase with low-frequency ripple component $\tilde{v}_c$ indicating transfer of ripple energy from C to C_s. The expression of $\tilde{v}_{cs}$ can be written for buck-boost-type APD topology as follows:

$$\tilde{v}_{cs}(t) = \frac{D_a(1-D_a)}{(1-D_a)^2-4\omega_o^2 L_s C_s}\cdot\tilde{v}_c(t). \tag{2.86}$$

The ripple current i_r, which is generally in phase with inductor current ripple $\tilde{i}_L$, is expressed for buck-boost-type APD topology as follows:

$$i_r(t) = \tilde{i}_r(t) = \frac{4\omega_o^2 LC_s D_a^2}{\sqrt{2}\{(1-D_a)^2-\omega_o^2 L_s C_s\}}\cdot\tilde{i}_L(t). \tag{2.87}$$

2.5.2 Design of passive elements

The auxiliary capacitor C_s can be selected based on the ripple energy of the dc-link capacitor C. If ripple energy E_r is assumed to be constant, it can be derived from low-frequency ripple power, given in (2.17), as follows:

$$E_r = \frac{\text{Peak-to-peak vale of } p_r}{2\omega_o} = \frac{R_0}{\omega_o} \approx \frac{I_o\sqrt{V_o^2+(\omega_o L_f I_o)^2}}{\omega_o} \tag{2.88}$$

Here, it is assumed that the output voltage v_o and the output current i_o, given in (2.9), are in phase, i.e., φ = 0. To design the auxiliary capacitor C_s, the ripple energy stored in C_s corresponding to the allowable peak-to-peak voltage ripple of auxiliary capacitor is required,

which is expressed as

$$p_{cs} = \frac{1}{2}C_s v_{cs\text{-Max}}^2 - \frac{1}{2}C_s v_{cs\text{-Min}}^2 = \frac{1}{2}C_s(V_{cs} + \hat{\tilde{v}}_{cs})^2 - \frac{1}{2}C_s(V_{cs} - \hat{\tilde{v}}_{cs})^2 = C_s V_{cs}(2\hat{\tilde{v}}_{cs}) \quad (2.89)$$

where $\hat{\tilde{v}}_{cs}$ is the peak value of $\tilde{v}_c s$, as expressed for three different types of APD networks in the following

$$\begin{aligned}
\text{For Buck:} \quad & \hat{\tilde{v}}_{cs} = \frac{D_a}{1 - 4\omega_o^2 L_s C_s} \cdot \frac{\sqrt{2}\omega_o L M I_o}{[4LC\omega_o^2 - (1-2D)^2 + k_t]} \\
\text{For Boost:} \quad & \hat{\tilde{v}}_{cs} = \frac{D_a}{(1-D_a)^2 - 4\omega_o^2 L_s C_s} \cdot \frac{\sqrt{2}\omega_o L M I_o}{[4LC\omega_o^2 - (1-2D)^2 + k_t]} \\
\text{For Buck-Boost:} \quad & \hat{\tilde{v}}_{cs} = \frac{D_a(1-D_a)}{(1-D_a)^2 - 4\omega_o^2 L_s C_s} \cdot \frac{\sqrt{2}\omega_o L M I_o}{[4LC\omega_o^2 - (1-2D)^2 + k_t]}
\end{aligned} \quad (2.90)$$

This energy storage must be more than the total ripple energy (E_r) expressed in (2.88). Therefore, C_s can be chosen as follows:

$$C_s \geq \frac{I_o\sqrt{V_o^2 + (\omega_o L_f I_o)^2}}{\omega_o V_{cs}(2\hat{\tilde{v}}_{cs})} \quad (2.91)$$

The auxiliary capacitor voltage V_{cs} and the corresponding peak-to-peak voltage ripple $2\hat{\tilde{v}}_{cs}$, both have inverse relationship with C_s, according to (2.91). Therefore, with the help of controller tuning, more ripple can be allowed in C_s or higher V_{cs} can be selected, so that C_s can be reduced.

It is clear that buck-type APD is ideal for devices with lower rating as voltage stress on the switches and capacitor are minimum. However, this limits its capability to reduce the ripple, because higher voltage can reduce more ripple as well as capacitor size. Therefore, in boost-type APD or buck-boost-type APD in boost mode, by allowing higher voltage, smaller capacitors can be employed due to more reduction in ripple.

Since the auxiliary inductor L_s is not used as a ripple energy storage device, it does not store any energy over a switching period. Therefore, the estimation of L_s does not involve the calculation of stored energy; instead, the allowable peak current through L_s needs to be

calculated. The peak auxiliary inductor current ($\hat{i}_{Ls}$) for different APD networks, considering both low- and high-frequency ripples, are found to be:

$$\begin{aligned} \text{For Buck:} \quad & \hat{i}_{Ls} = \frac{\hat{i}_r}{D_a} + \Delta i_{Ls} \\ \text{For Boost:} \quad & \hat{i}_{Ls} = \hat{i}_r + \Delta i_{Ls} \\ \text{For Buck-Boost:} \quad & \hat{i}_{Ls} = \frac{\hat{i}_r}{D_a} + \Delta i_{Ls} \end{aligned} \tag{2.92}$$

where Δi_{Ls} is the high-frequency ripple component, expressed in the following for three different types of APD networks as:

$$\begin{aligned} \text{For Buck:} \quad & \Delta i_{Ls} = \frac{(V_c - V_{cs}) D_a T_s}{2L_s} \\ \text{For Boost:} \quad & \Delta i_{Ls} = \frac{V_c D_a T_s}{2L_s} \\ \text{For Buck-Boost:} \quad & \Delta i_{Ls} = \frac{V_c D_a T_s}{2L_s}. \end{aligned} \tag{2.93}$$

Based on C_s, the selection of L_s is carried out, which depends on maximum allowable current stress through the switches I_{DSS}. Note that L_s is not storing any energy and is being used to charge and discharge the auxiliary capacitor C_s by deflecting ripple energy from C. The values of $\hat{i}_{Ls}$ found in (2.92) must not exceed I_{DSS}. Therefore, L_s for all three types of APD networks can be chosen as follows:

$$\begin{aligned} \text{Buck: } L_s &= \frac{(1-D_a)T_s \left\{ V_{cs} + \frac{I_o}{2\omega_o C_s V_{cs}} \sqrt{V_o^2 + (\omega_o L_f I_o)^2} \right\}}{I_{DSS} - \frac{I_o}{V_{cs}} \sqrt{V_o^2 + (\omega_o L_f I_o)^2}} \\ \text{Boost: } L_s &= \frac{D_a(1-D_a)T_s \left\{ V_{cs} + \frac{I_o}{2\omega_o C_s V_{cs}} \sqrt{V_o^2 + (\omega_o L_f I_o)^2} \right\}}{I_{DSS} - \frac{I_o}{(1-D_a)V_{cs}} \sqrt{V_o^2 + (\omega_o L_f I_o)^2}} \\ \text{Buck-boost: } L_s &= \frac{(1-D_a)T_s \left\{ V_{cs} + \frac{I_o}{2\omega_o C_s V_{cs}} \sqrt{V_o^2 + (\omega_o L_f I_o)^2} \right\}}{I_{DSS} - \frac{I_o}{(1-D_a)V_{cs}} \sqrt{V_o^2 + (\omega_o L_f I_o)^2}} \end{aligned} \tag{2.94}$$

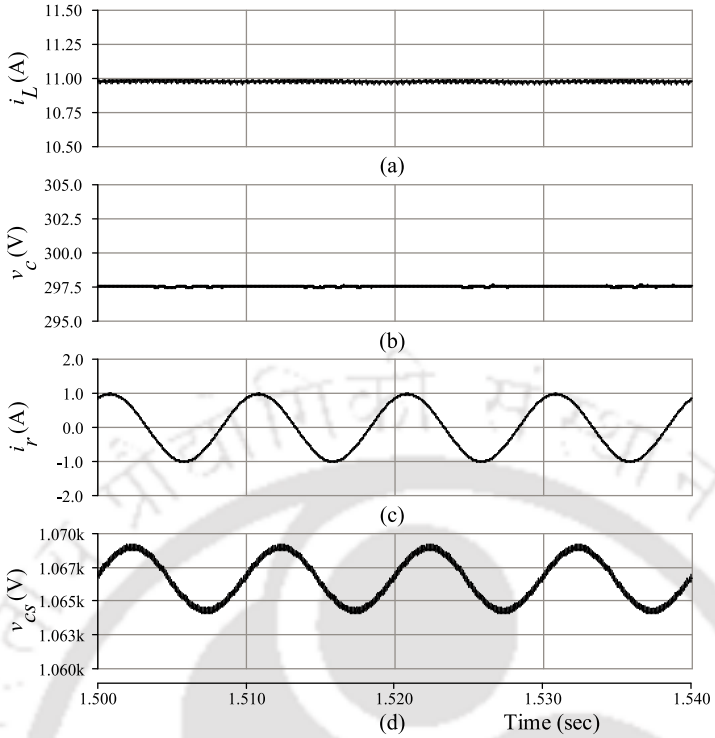


Fig. 2.25 Waveforms of single-phase SBI with boost-type APD. (a) i_L: inductor current of active-front-end network, (b) v_c: capacitor voltage of active-front-end network, (c) i_r: ripple current and (d) v_{cs}: auxiliary capacitor voltage.

There is another way to achieve complete elimination of voltage and current ripple, i.e., $\tilde{i}_L = 0$ and $\tilde{v}_c = 0$. For example, in boost-type APD-integrated SBI, according to (2.76), the design target should be

$$(1 - D_a)^2 = 4\omega_o^2 L_s C_s \tag{2.95}$$

This requires D_a to be close to 1, which results in very high V_{cs} according to (2.73). As an example, the simulation results are shown in Fig. 2.25 for $D_a = 0.72$, $C_s = 200$ μF and $L_s = 1$ mH in accordance with (2.95) with the parameters mentioned in Table 2.2. It is observed that v_c and i_L do not contain any low-frequency ripple while v_{cs} and i_r contain low-frequency ripple. It is to be noted that V_{cs} is nearly 1070 V which is very high as $D_a = 0.72$. Choosing a smaller D_a would result in much larger L_s and C_s. For example, for D_a = 0.2, L_s = 4 mH and C_s = 405 μF.

Therefore, in order to completely eliminate of the low-frequency ripple, auxiliary passive elements L_s and C_s need to be larger, and this affects overall power density of the system.

Alternatively, the APD network can be utilized to store a part of the low-frequency ripple energy instead of the complete ripple energy. In that case, the required C_s and L_s would be much smaller. At the same time, the reduction in the low-frequency ripple energy would also help reduce dc-link capacitor. Thus, the design target is chosen such that the capacitor voltage ripple and inductor current ripple are reduced by a factor k as follows:

$$\begin{aligned} \frac{(\hat{v}_c)_{\text{SBI}}}{(\hat{v}_c)_{\text{SBI\_APD}}} &\geq k \\ \frac{(\hat{i}_L)_{\text{SBI}}}{(\hat{i}_L)_{\text{SBI\_APD}}} &\geq k \end{aligned} \tag{2.96}$$

where $(\hat{v}_c)_{\text{SBI}}$ and $(\hat{i}_L)_{\text{SBI}}$ can be obtained from (2.40); $(\hat{v}_c)_{\text{SBI\_APD}}$ and $(\hat{i}_L)_{\text{SBI\_APD}}$ are given in (2.68), (2.76) and (2.84) for buck-type, boost-type and buck-boost-type APD topologies, respectively.

For a certain amount of ripple energy E_r, the auxiliary capacitor voltage V_{cs} and the voltage ripple Δv_{cs} are both inversely proportional to the value of C_s. So, by allowing more ripple in the C_s or by selecting higher V_{cs}, power density can be improved.

$$C_s \geq \frac{k-1}{k} \cdot \frac{I_o\sqrt{V_o^2 + (\omega_o L_f I_o)^2}}{\omega_o V_{cs}(2\hat{\tilde{v}}_{cs})} \tag{2.97}$$

Once C_s is chosen, L_s can be designed based on (2.94).

Although APD topology is handling most of the low-frequency content, the active-front-end network is still required to keep high-frequency and low-frequency within a limit. The required capacitor to limit the high-frequency ripple is given in (2.42). However, this capacitor may not be sufficient for mitigation of low-frequency ripple within the limit. If the low-frequency ripple in v_c is considered to be $2\hat{\tilde{v}}_c \leq xV_c$, the minimum capacitor requirement for limiting low-frequency ripple using the selected inductor value in (2.44) is obtained as

$$C \geq \frac{(1-2D)MI_o}{\sqrt{2}kx\omega_o(1-D)V_g} + \frac{(1-2D)^2}{4\omega_o^2 L} \tag{2.98}$$

In order to mitigate both high- and low-frequency ripple, C must be chosen larger than both the values obtained in (2.42) and (2.98). If the low-frequency ripple in i_L is considered to be $2\hat{\tilde{i}}_L \leq yI_L$, based on the value of chosen capacitor, y needs to be calculated again to check whether it matches ripple limit. If it is not within limit, a larger inductor is selected and capacitor value is again calculated. This procedure is continued until all ripples are within a limit.

According to $k = 5$, $a = 2\%$, $b = 40\%$, $x = 5\%$ and $y = 20\%$, the chosen values of C, L, C_s and L_s are 100 µF, 2.75 mH, 220 µF and 1 mH respectively. As C is smaller, conventional electrolytic capacitors can be replaced with film capacitors, thereby, significantly enhancing overall reliability and lifetime of the system [46].

2.6 COMPARISON OF THREE APD-INTEGRATED SBI TOPOLOGIES

In this section, a comparison of three APD-integrated SBI topologies is presented, considering the APD networks are connected across the dc-link capacitor. The average auxiliary capacitor voltages V_{cs} for different APD topologies are expressed as follows:

$$\begin{aligned} \text{For Buck:} \quad & V_{cs} = D_a \cdot V_c \\ \text{For Boost:} \quad & V_{cs} = \frac{V_c}{1 - D_a} \\ \text{For Buck-Boost:} \quad & V_{cs} = \frac{D_a}{1 - D_a} \cdot V_c. \end{aligned} \tag{2.99}$$

In buck-type APD topology, the voltage stress across the switches are equal to the peak of the dc-link voltage v_c, which indicates that the switching voltage stress is comparatively less than other two topologies. In boost-type APD topology, the voltage stress across the switches is observed to be peak of the auxiliary capacitor voltage v_{cs}, which is comparatively higher than buck-type APD, and comparatively lower than buck-boost-type APD. In buck-boost-type topology, the voltage across the switches can be as high as the sum of peak of the auxiliary capacitor voltage v_{cs} and peak of the dc-link voltage v_c. Therefore, the voltage stress in switches in buck-boost-type is comparatively higher than both buck- and boost-type APD.

Table 2.3 Comparison of component values for three APD-integrated SBI topologies

	SBI	w. Buck	w. Boost	w. Buck-boost
D_a	NA	0.75	0.2	0.55
V_{cs}	NA	225 V	375 V	367 V
C	570 μF	100 μF	100 μF	100 μF
L	2.75 mH	2.75 mH	2.75 mH	2.75 mH
C_s	NA	220 μF	135 μF	135 μF
L_s	NA	0.6 mH	0.6 mH	1.9 mH
Loss	65W	5 W	3 W	10 W
η	87%	86%	86.4%	85%

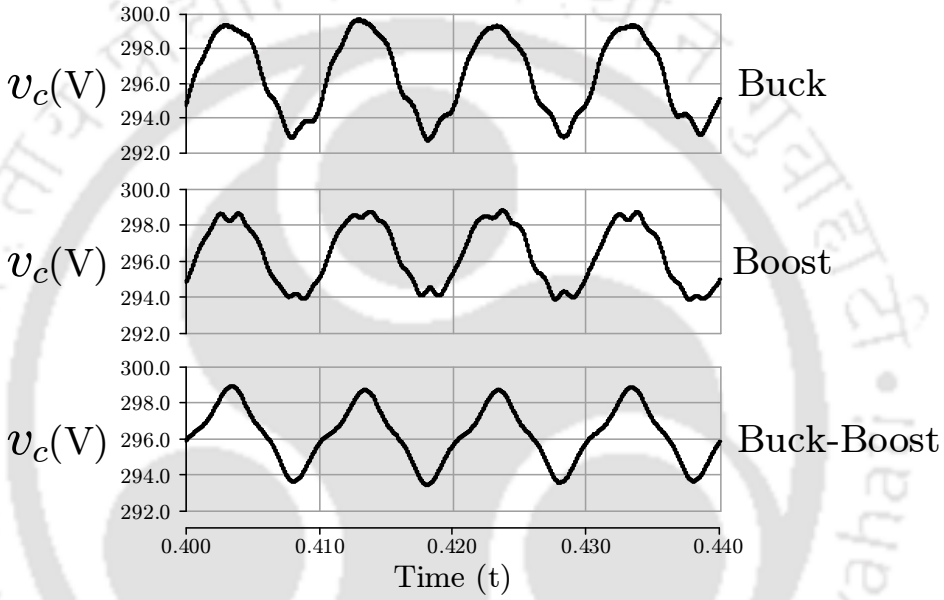


Fig. 2.26 Comparison of dc-link capacitor voltage ripple of three APD-integrated SBI topologies.

Table 2.3 shows a comparison of the selected values of C_s and L_s, which indicates minimum C_s can be chosen for boost-type as well as buck-boost-type, and minimum L_s can be selected for buck-type and boost-type. The auxiliary capacitor voltage V_{cs} are chosen as 225 V, 375 V and 367 V for buck, boost and buck-boost, respectively, whereas allowable peak-to-peak ripple across the auxiliary capacitor C_s is kept as 20 V for all APDs. Although buck-type APD has less voltage stress on switches, it requires more C_s. The buck-boost can operate as either buck-type or boost-type, but it has the highest voltage stress across switches, and it requires more L_s, thereby making it the least favorable choice. As both minimum capacitor and inductor can be found for boost-type APD, it is clearly the most favorable APD in terms of power density with the conditions used for this analysis.

Note that reduction of ripple using APD topologies will reduce efficiency. However, this compromise will be overcome by the fact that reduction in ripple will facilitate the use of film capacitor, which in turn improve overall system lifetime and reliability. Therefore, the most favorable APD topology should result in the least reduction in efficiency. The superiority of the boost-type APD is further affirmed in the efficiency analysis, where SBI with boost-type APD shows the least amount of reduction of efficiency. Note that the integration of APD topologies with SBI reduces capacitor requirement in the active-front-end network by nearly 6 times.

From the simulation results of three APD-integrated SBI topologies as shown in Fig. 2.26, it is observed that the amount of ripple achieved with buck, boost and buck-boost-type APD are 6.5 V, 4.5 V and 6 V respectively. Therefore, maximum ripple reduction is achieved with boost-type APD.

As a conclusion, this comparison clearly indicates that the integration of the boost-type APD network with the single-phase SBI is the most advantageous among all three APD topologies. Therefore, a closed-loop control is proposed for the boost-type APD-integrated SBI, where the boost-type APD is connected across the dc-link capacitor, as shown in Fig. 2.16, and it is implemented in hardware.

2.7 CLOSED-LOOP CONTROL STRATEGY OF APD

The schematic diagram of the closed-loop control strategy for boost-type APD is shown in Fig. 2.27. The main objective of the closed-loop control of the APD topology is to deflect the second harmonic ripple energy from the dc-link capacitor C to the auxiliary capacitor C_s. This involves two steps: the generation of the reference ripple current by extracting the low-frequency ripple from the dc-link capacitor voltage and tracking this reference. As C_s is utilized as a ripple energy storage device, the voltage across C_s might become too high if it is not discharged properly. Therefore, the closed-loop control also needs to prevent any over-voltage situation of C_s. Additionally, the closed-loop control is also required to compensate for low-frequency ripple current accurately against any load changes.

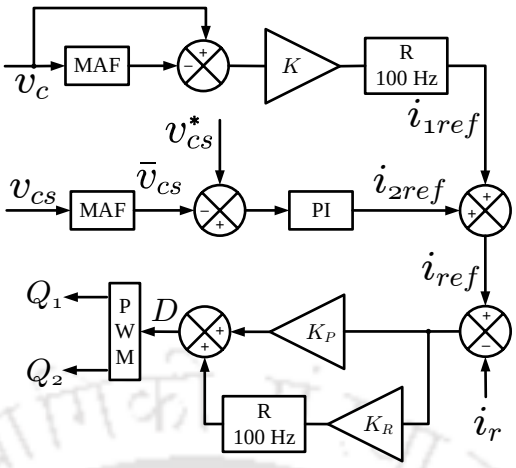


Fig. 2.27 Control strategy of boost-type APD.

2.7.1 Generation of reference ripple current

In order to generate the average value, the measured v_c is passed through a moving average filter (MAF), as shown in Fig. 2.27. The average value V_c is subtracted from v_c to obtain the complete harmonic content which is passed through a resonant filter to extract the dominant second harmonic part i_{1ref}. Generally, i_{1ref} can be taken as the reference ripple current. However, the auxiliary capacitor C_s will be over-charged as it is now storing the ripple content. As a result, the voltage across C_s will increase dangerously. Therefore, the closed-loop control must regulate the auxiliary capacitor voltage v_{cs} to prevent its over-voltage. Hence, an additional dc bias current i_{2ref} is added to i_{1ref} so that

$$i_{ref} = i_{1ref} + i_{2ref} \tag{2.100}$$

Thus, it is ensured that a constant average auxiliary capacitor voltage V_{cs} is maintained.

2.7.2 Tracking the reference ripple current

The current through the auxiliary inductor needs to track the reference ripple current, i_{ref}. The current controller should ensure zero steady-state error, good attenuation at second harmonic as well switching frequency and good transient performance. To achieve this, proportional-integral (PI) and proportional-resonant (PR) are considered as current controllers.

For designing of the parameters of the current controller, the control to ripple current transfer function is required. So, small-signal analysis of the boost-type APD topology, as shown in Fig. 2.16, is carried out, and the following expressions are obtained as

$$\begin{aligned} L_s\frac{d\tilde{i}_r(t)}{dt} &= \tilde{v}_c(t) - (1-D_a)\cdot\tilde{v}_{cs}(t) + \tilde{d}_a(t)\cdot V_{cs} \\ C\frac{d\tilde{v}_c(t)}{dt} &= -\frac{\tilde{v}_c(t)}{R_{dc}} - \tilde{i}_r(t) - \tilde{i}_{ci}(t) \\ C_s\frac{d\tilde{v}_{cs}(t)}{dt} &= (1-D_a)\cdot\tilde{i}_r(t) \end{aligned} \tag{2.101}$$

The transfer function of ripple current to capacitor voltage can be derived as

$$\left.\frac{\tilde{v}_c(s)}{\tilde{i}_r(s)}\right|_{\tilde{i}_{ci}(s)=0} = -\frac{R_{dc}}{sCR_{dc}+1} \tag{2.102}$$

The transfer function of ripple current to auxiliary capacitor voltage can be expressed as

$$\left.\frac{\tilde{v}_{cs}(s)}{\tilde{i}_r(s)}\right|_{\tilde{d}_a(s)=0} = \frac{1-D_a}{sC_s} \tag{2.103}$$

The control parameter is the duty ratio, d_a, of the switch Q_1. So, the transfer function of control to the ripple current can be obtained as

$$G_i(s) = \left.\frac{\tilde{i}_r(s)}{\tilde{d}_a(s)}\right|_{\tilde{v}_{cs}(s)=0,\ \tilde{i}_{ci}(s)=0} = \frac{V_{cs}}{R_{dc}}\cdot\frac{R_{dc}(sCR_{dc}+1)}{s^2L_sCR_{dc}+sL_s+R_{dc}} \tag{2.104}$$

The current loop gain can be written as

$$T_i(s) = G_{ci}(s)\cdot G_i(s) = \left(K_P + \frac{K_I}{s}\right)\cdot G_i(s) \tag{2.105}$$

where $G_{ci}(s)$ is a PI controller. As the reference signal contains ac components, it is difficult to eliminate steady-state error, and the error further increases with increase in the frequency. So, the controller can be modified for ac reference signals [100].

$$G_{cm}(s) = \frac{1}{2}[G_{ci}(s+j2\omega_o) + G_{ci}(s-j2\omega_o)] \tag{2.106}$$

Table 2.4 Simulation parameters and component values

Parameter/Component	Attributes
Input voltage (V_g)	100 V
Modulation index (M)	0.5
Shoot-through duty ratio (D)	0.4
Fundamental frequency (f_o)	50 Hz
Inverter switching frequency (f_s)	10 kHz
Inductor (L)	2.75 mH
DC-link capacitor (C)	100 µF
APD switching frequency (f_s)	20 kHz
APD inductor (L_s)	1 mH
APD capacitor (C_s)	220 µF
DC load (R_{dc})	400 Ω, 250 W
Output filter inductor (L_f)	1 mH
Output filter capacitor (C_f)	11 µF
AC load (R_o)	36 Ω, 250 W

which can be written in the form of a PR controller as follows

$$G_{cm}(s) = K_P + K_R \cdot \frac{2s}{s^2 + (2\omega_o)^2} \tag{2.107}$$

Instead of using the structure of (2.107), an additional damping can be included. The damping factor, ξ, can be taken between 0.01 and 0.02 [100]. Thus, (2.107) becomes

$$G_{cm}(s) = K_P + K_R \cdot \frac{4\xi\omega_o s}{s^2 + 4\xi\omega_o s + (2\omega_o)^2} \tag{2.108}$$

The single-phase SBI with boost-type APD network connected across the dc-link capacitor, shown in Fig. 2.16, is simulated to compare the performance of PI and PR current controllers with parameters mentioned in Table 2.4. As shown in Fig. 2.28(a) and (b), the PR controller tracks the reference current better than the PI controller, which corroborates with the previous analysis. This is also evident from the steady-state error plot of both controllers in Fig. 2.28(c). The steady-state error calculation is based on RMS values of reference and actual current waveforms. The steady-state error is nearly three times in the case of PI compared to PR, as the PR controller introduces a very high gain at the second harmonic, making the steady-state error close to zero.

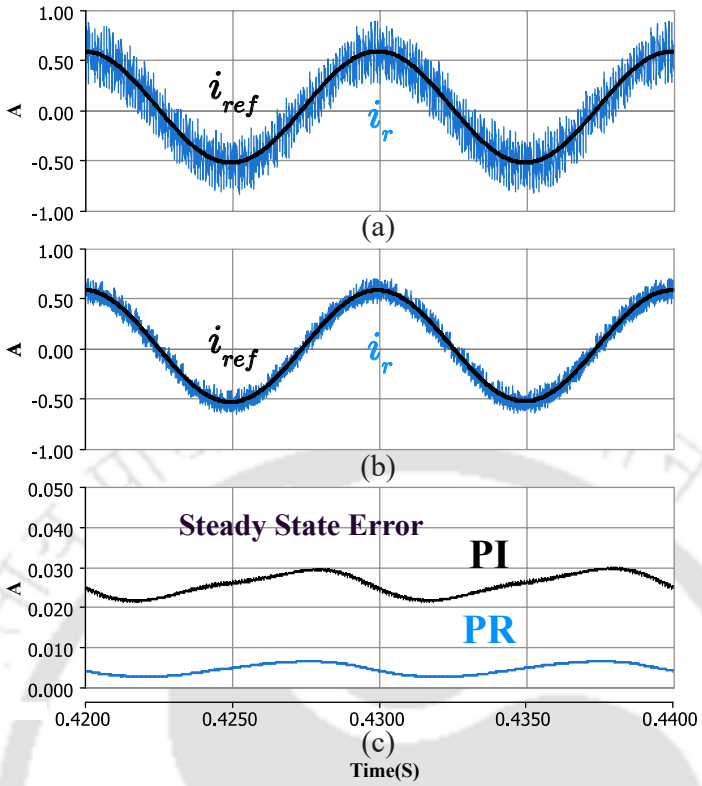


Fig. 2.28 Tracking performance of different current controllers: (a) proportional-integral (PI) controller, (b) proportional-resonant (PR) controller and (c) steady-state error using PI and PR controllers.

Further study has been carried out for the selection of the parameters K_P and K_R based on stability and transient performance as well as several other constraints as the APD topology is working primarily for ripple reduction. A high gain must be available at the second harmonic ripple frequency, i.e., 100 Hz for accurate tracking of the ripple current in order to achieve proper mitigation. Generally, a gain of 20dB or higher is recommended for a good design. However, while designing the loop gain, enough phase margin (φ_m) must be present to ensure relative stability.

Since the current loop should have fast dynamics, high bandwidth is essential. As the APD switching frequency (f_s) is 20 kHz, the crossover frequency (f_c) of the current loop should be below 10 kHz in order to provide adequate attenuation at f_s. The lower limit of f_c is set based on the second harmonic, i.e., 100 Hz ripple. In order to avoid interaction with the 100 Hz, a separation of at least half decade must be present [101]. So, f_c should be more than 500 Hz. The system performance with the variation of K_P and K_R has been tabulated in

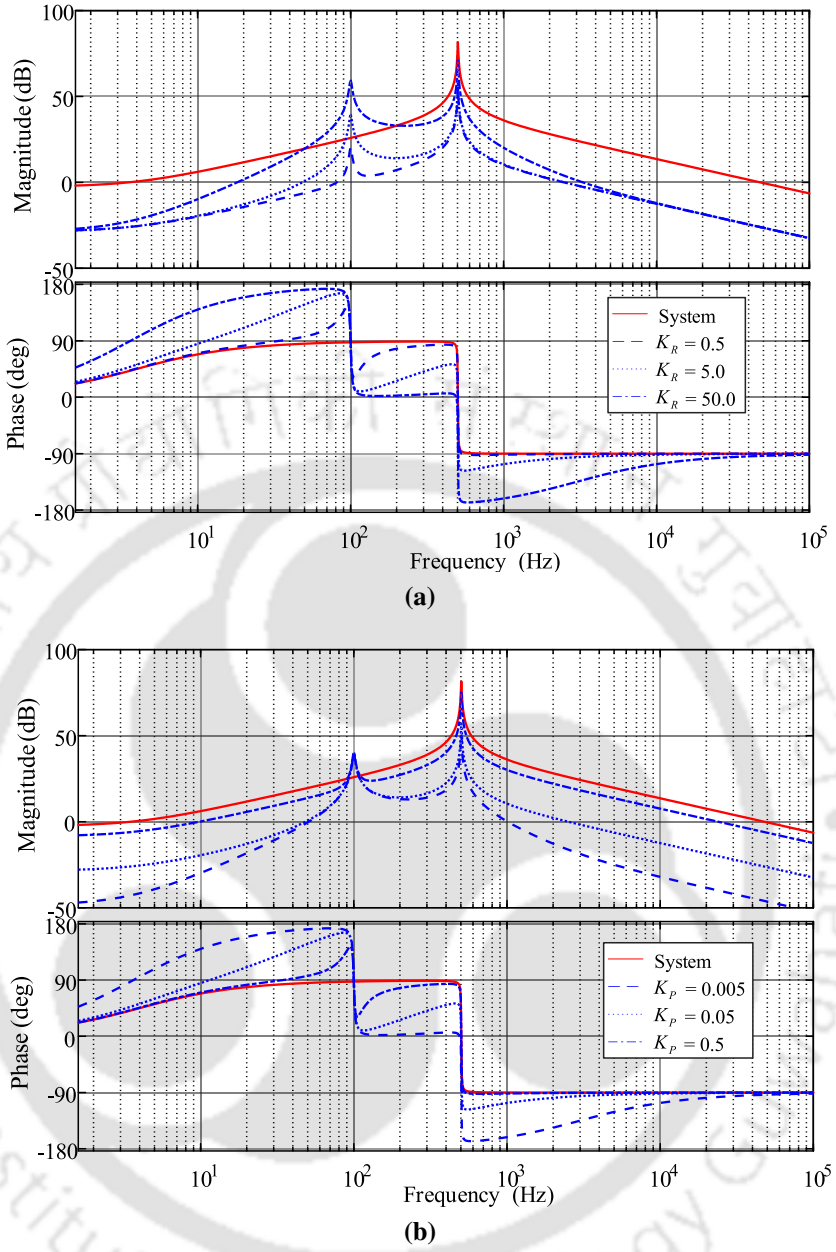


Fig. 2.29 Bode diagram of open-loop gain for current control loop. (a) variation of K_R from 0.5 to 50.0 while keeping K_P = 0.05 and (b) variation of K_P from 0.005 to 0.5 while keeping K_R = 5.0.

Table 2.5 from which it is found that the selection of K_P = 0.05 and K_R = 5.0 results in f_c = 2510 Hz , φ_m = 83.2^o, gain at 100 Hz = 40 dB and attenuation at switching frequency = 18.4 dB, which is satisfying all aforementioned criteria.

A bode plot is given in Fig. 2.29(a), where K_R is varied from 0.5 to 50.0 while keeping K_P = 0.05. As K_R is increased, gain at 100 Hz has also increased. However, with more increment, a reduction of φ_m is also observed. So, K_R = 5.0 is chosen. Another bode plot is

Table 2.5 Effect of variation of K_R and K_P

K_P	K_R	f_c (Hz)	φ_m	Gain@100 Hz	Gain@20 kHz
0.005	0.5	653	65.4^o	19.8 dB	–38.4 dB
0.05	0.5	2490	89.3^o	19.8 dB	–18.4 dB
0.5	0.5	23900	90^o	25.8 dB	1.52 dB
0.005	5.0	1010	18.6^o	40.7 dB	–38.2 dB
0.05	5.0	2510	83.2^o	40.7 dB	–18.4 dB
0.5	5.0	23900	89.9^o	40.7 dB	1.54 dB
0.005	50.0	2730	5.26^o	59.9 dB	–33.3 dB
0.05	50.0	3300	47.8^o	59.9 dB	–18.4 dB
0.5	50.0	23900	89.3^o	59.9 dB	1.59 dB

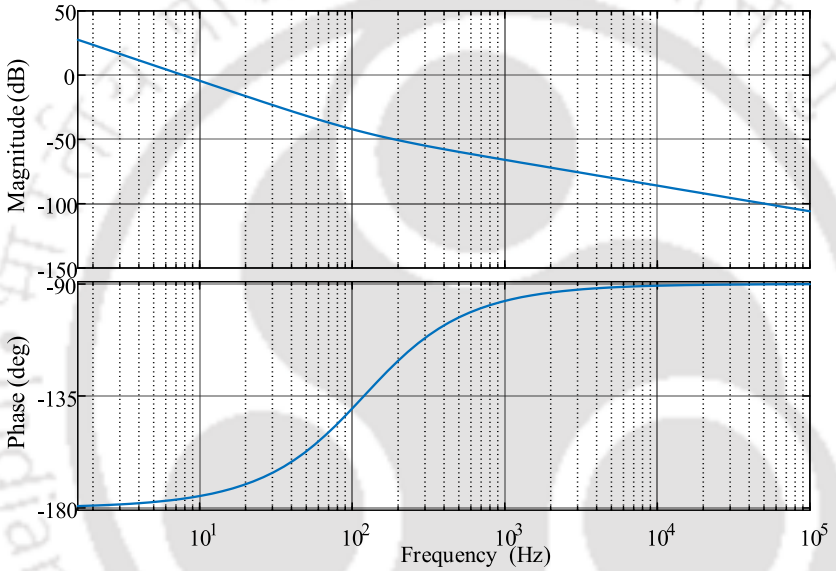


Fig. 2.30 Bode diagram in closed-loop for voltage control loop.

shown in Fig. 2.29(b), where K_P is varied from 0.005 to 0.5 while keeping K_R = 5.0. As K_P is increased, φ_m has increased, and f_c has also increased which results in less attenuation at f_s. So, K_P = 0.05 is chosen.

2.7.3 Control of auxiliary capacitor voltage

As discussed earlier, v_{cs} is required to be regulated, and it is achieved with a voltage controller added in the form of a PI controller. As shown in Fig. 2.27, the measured v_{cs} is passed through a moving average filter (MAF) so that the dc component V_{cs} can be extracted. Then V_{cs} is compared with the reference value V_{cs}^* and the error is given to the PI controller.

In the voltage loop, the bandwidth can be relatively lower compared to the current controller. So, the closed-loop gain of the current controller can be taken as unity. Thus, the voltage loop gain can be written as

$$T_v(s) = G_{cv}(s) \cdot G_v(s) = \left(K_P + \frac{K_I}{s}\right) \cdot \left(\frac{1 - D_a}{sC_s}\right) \tag{2.109}$$

where G_{cv} is a PI controller and G_v is taken from (2.103).

In order to avoid interaction with 100 Hz current ripple, the crossover frequency should be set at least half decade separated from 100 Hz. Hence, the crossover frequency in the voltage loop is recommended to be lower than 20 Hz. It should be chosen such that enough attenuation can be achieved at 100 Hz. In this work, the crossover frequency is selected as 8 Hz. As a result, more than 40 dB attenuation is provided at 100 Hz, as shown in Fig. 2.30, which should adequately mitigate the second harmonic ripple.

2.8 EXPERIMENTAL RESULTS

In the hardware fabrication of the SBI, the gate pulses for the switches are implemented using TMS320F28335 digital signal processor (DSP) [102]. A sine-triangle pulse width modulation-based technique described in [20] is used for the gate-pulse generation of the SBI. A hardware prototype of single-phase APD-integrated SBI has been built which is shown in Fig. 2.31. The experimental results of the single-phase SBI without APD topology is presented in Fig. 2.32(a) and (b). All parameters are the same as the value used in simulation and are mentioned in Table 2.4. The components used in the hardware setup are listed in Table 2.6.

The input dc voltage V_g is kept at 100 V. The average capacitor voltage V_c of the active-front-end network is observed to be 265 V. As the shoot-through duty ratio D is taken as 0.4, the calculated V_c is 300 V, according to (2.6). The drop in boosted voltage is due to non-idealities present in the hardware circuit. The average inductor current I_L is observed to be 7.5 A, which is in accordance with (2.8). As shown in Fig. 2.32(a), the peak-to-peak ripple

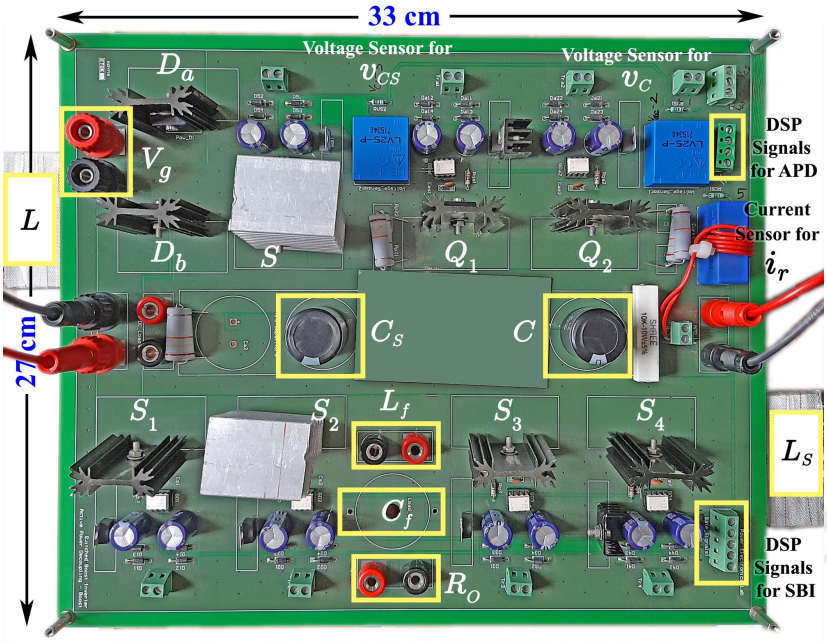


Fig. 2.31 Hardware prototype of single-phase APD-integrated SBI.

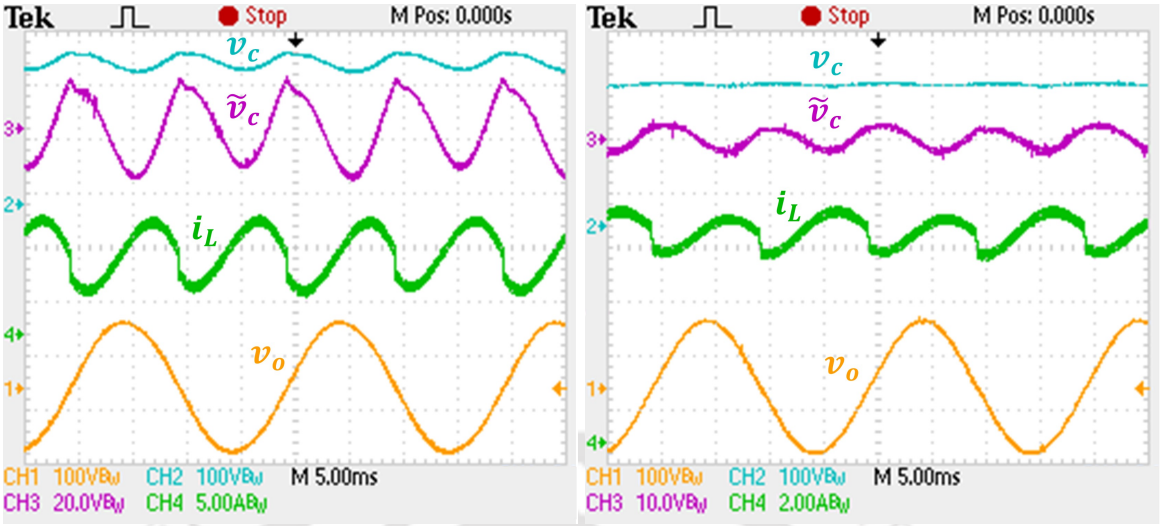
Table 2.6 Components used in hardware setup

Component	Part No. and Manufacturer
S_1, S_2, S_3, S_4	IRG7PH42UDPBF (International Rectifier)
S	IRG7PH42UPBF (International Rectifier)
D_a, D_b	DSEI60-06A (IXYS)
Gate Driver	FOD3180 (Fairchild)
Inductor Core	E 100/60/28 (EPCOS)
Voltage Transducer	LV 25-P (LEM)
Current Transducer	LA 55-P (LEM)

Table 2.7 Comparison of low-frequency ripples obtained from experimental results

	SBI without any APD		SBI with boost-type APD	
Fig. No.	2.32(a)	2.32(b)	2.33(a)-(b)	2.33(c)-(d)
DC-link capacitor C	100 µF	570 µF	100 µF	100 µF
Peak-to-peak ripple in v_c	40 V	8 V	8 V	5.6 V
Peak-to-peak ripple in i_L	8 A	1.6 A	1.6 A	1.4 A
Peak-to-peak ripple in v_{cs}	NA		10 V	12 V

in v_c is 40 V, and the peak-to-peak ripple in i_L is 8 A, when the dc capacitor C is only 100 µF. When C is increased to 570 µF, the peak-to-peak ripple in v_c is reduced to 8 V, and the peak-to-peak ripple in i_L has decreased to 1.6 A as evident from Fig. 2.32(b). The amount of low-frequency ripples are consistent with (2.40). The filter ac output voltage is 90 V RMS, although the waveform is found to be slightly distorted when C is 100 µF.



(a) **(b)**

Fig. 2.32 Experimental results of single-phase SBI without APD: (a) C = 100 µF without APD and (b) C = 570 µF without APD. DC input voltage V_g = 100 V, v_c: capacitor voltage of active-front-end network, $\tilde{v}_c$: low-frequency ripple of v_c, i_L: inductor current of active-front-end network, $\tilde{i}_L$: low-frequency ripple of i_L, v_{cs}: auxiliary capacitor voltage, $\tilde{v}_{cs}$: low-frequency ripple of v_{cs}, v_o: load voltage.

Fig. 2.33(a)-(d) show experimental results of single-phase SBI with APD. Note that as mentioned in Section 2.5, for the complete elimination of ripple in v_c and i_L, as shown in Fig. 2.25, very high auxiliary capacitor voltage v_{cs} or very large auxiliary capacitor C_s and inductor L_s are required. In order to prevent this, the design target is chosen such that the voltage ripple is reduced by a factor k. Hence, k is chosen as 5 so that similar levels of ripple reduction as Fig. 2.33(b) can be achieved. So, according to (2.97) and (2.94), C_s and L_s are selected as 220 µF and 1 mH respectively with allowed peak-to-peak voltage ripple across C_s taken as 10 V. The reference for auxiliary capacitor voltage (V_{cs}^*) is taken as 300 V. As shown in Fig. 2.33(a), similar peak-to-peak ripple in v_c as Fig. 2.33(b) have been attained, when the SBI is operating with the APD and C is 100 µF. The APD is operated in closed-loop, and the current and voltage controller parameters are same as those designed in the previous section. The average auxiliary capacitor voltage (V_{cs}) is found to be around 300 V, which means the voltage controller in closed-loop is working. The waveform of v_o has improved due to reduced ripple in v_c. The ripple content of v_c, v_{cs} and i_L are observed separately with ac coupling mode in the oscilloscope. As shown in Fig. 2.33(b), a reduction of 80% in voltage ripple has been achieved as the peak-to-peak ripple in v_c is observed to be 8 V, and a reduction

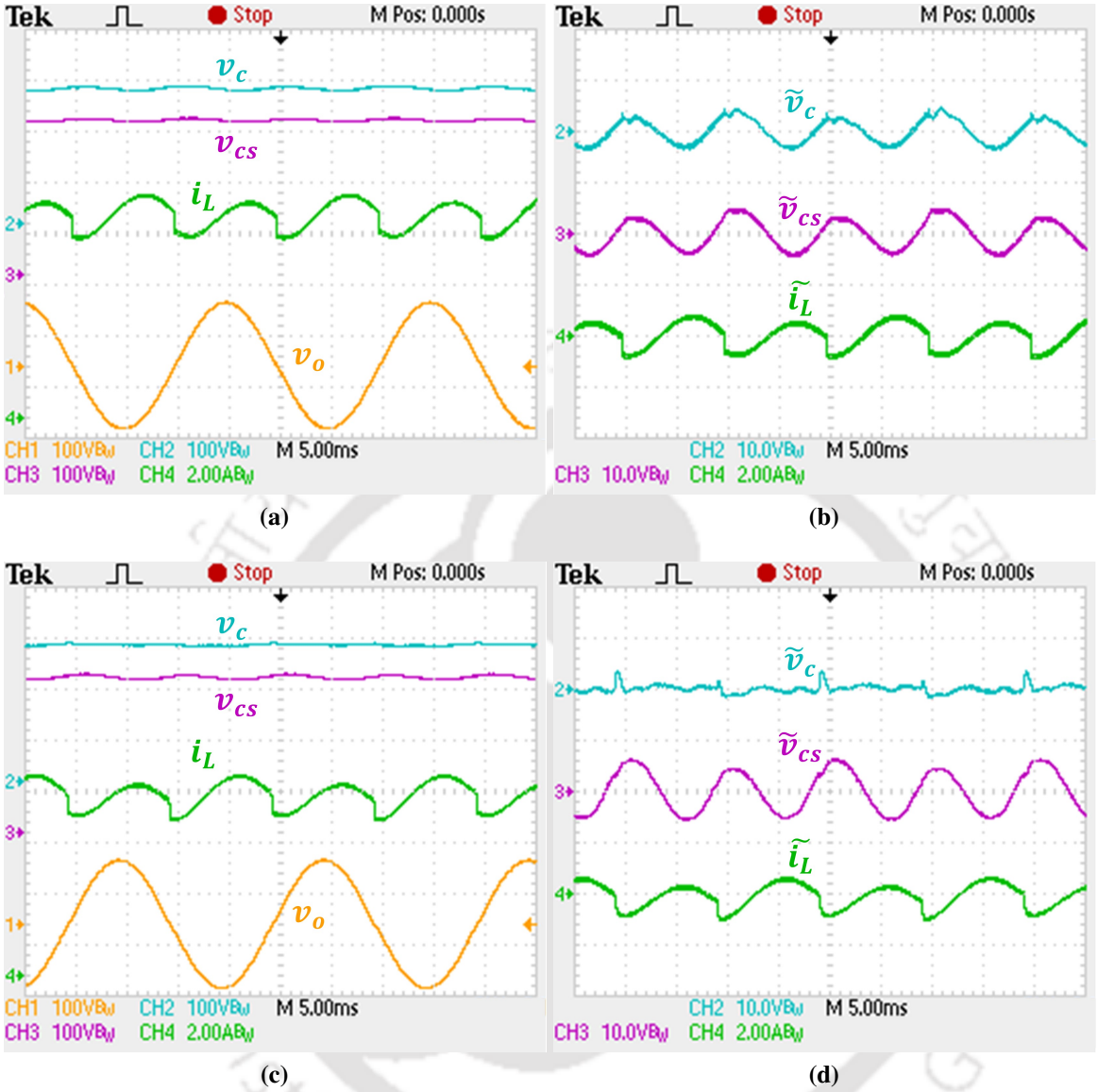
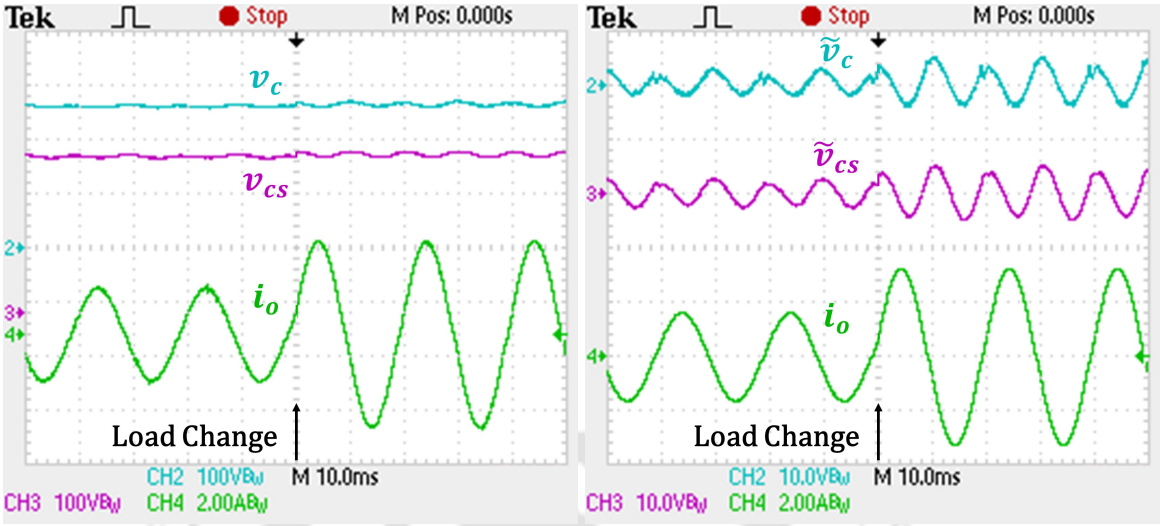


Fig. 2.33 Experimental results of single-phase APD-integrated SBI: (a) k = 5, C = 100 µF with APD when v_{cs} = 10 V, (b) low-frequency ripple of v_c, v_{cs} and i_L in (a), (c) k = 7, C = 100 µF with APD when v_{cs} = 12 V and (d) low-frequency ripple of v_c, v_{cs} and i_L in (c). dc input voltage V_g = 100 V, v_c: capacitor voltage of active-front-end network, $\tilde{v}_c$: low-frequency ripple of v_c, i_L: inductor current of active-front-end network, $\tilde{i}_L$: low-frequency ripple of i_L, v_{cs}: auxiliary capacitor voltage, $\tilde{v}_{cs}$: low-frequency ripple of v_{cs}, v_o: load voltage.

of 80% in current ripple is obtained as the peak-to-peak ripple in i_L has been found to be 1.6 A. The amount of low-frequency ripples are consistent with (2.76). Therefore, a reduction of 82.5% in capacitor requirement in the active-front-end network and a reduction of 45% in overall capacitor requirement have been achieved in the system.

As shown in Fig. 2.33(c) and (d), by allowing more voltage ripple across C_s, k can be further increased to 7, which indicates the peak-to-peak ripple in v_c is reduced 7 times, while



(a) **(b)**

Fig. 2.34 Transient response of single-phase APD-integrated SBI: (a) change in voltage ripple with change in load current i_o and (b) low-frequency ripples of v_c and v_{cs} in (a). v_c: capacitor voltage of active-front-end network, $\tilde{v}_c$: low-frequency ripple of v_c, v_{cs}: auxiliary capacitor voltage, $\tilde{v}_{cs}$: low-frequency ripple of v_{cs}, i_o: load current.

keeping values of both C_s and L_s unchanged. The ripple content of v_c, v_{cs} and i_L are observed separately with ac coupling mode in the oscilloscope. It is observed from Fig. 2.33(d), since the allowed peak-to-peak voltage ripple across C_s has increased to 12 V, the peak-to-peak ripple in v_c has reduced to 5.6 V, and the peak-to-peak ripple in i_L has suppressed to 1.4 A. Table 2.7 presents the low-frequency ripples in v_c and i_L for single-phase SBI with and without APD.

The transient performance of the single-phase APD-integrated SBI is demonstrated in Fig. 2.34. As shown in Fig. 2.34(a), with a reduction in load current from 3.25 A (p-p) to 6.5 A (p-p), the ripple content in both v_c and v_{cs} have also decreased. It can also be observed in Fig. 2.34(a) that the auxiliary capacitor voltage V_{cs} is regulated to its reference V_{cs}^* during the change in load. The ripple in v_c has increased from 4 V to 8 V and the ripple in v_{cs} has increased from 5 V to 10 V as observed in Fig. 2.34(b). Thus, the single-phase APD-integrated SBI shows satisfactory steady-state and transient performances.

A comparison of the efficiency of the single-phase SBI with 100 µF, with 570 µF and with APD is presented in Fig. 2.35. It is observed that system efficiency is decreasing with more output power. In general, more efficiency has been achieved with larger capacitance due to

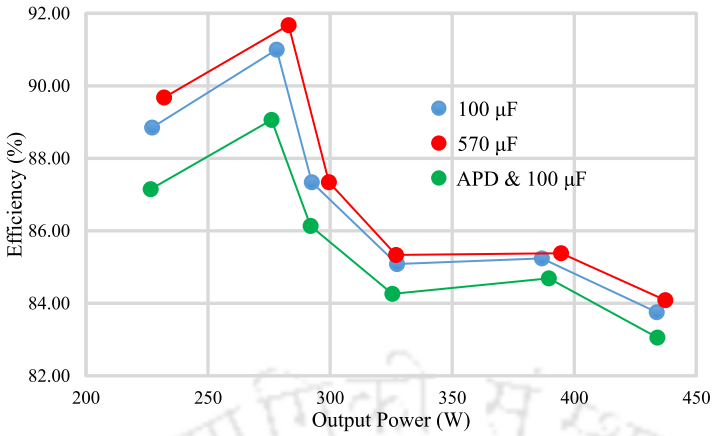


Fig. 2.35 Efficiency comparison for single-phase SBI: C = 100 µF without APD, C = 570 µF without APD and C = 100 µF with APD.

smaller ripples when APD is not operational. When single-phase SBI is operated with APD, a slight drop in efficiency is observed due to additional switches and passive elements. The reduced efficiency is considered a compromise to achieve better reliability and lifetime of the system. Since the dc-link capacitor used in the system is reduced, and the auxiliary capacitor is also relatively small, film capacitors can be employed instead of conventional electrolytic ones for all of the capacitors in the boost-type APD-integrated SBI. Since film capacitors have significantly better reliability and lifetime than electrolytic capacitors, overall system reliability and lifetime are improved with the compromise of slightly reduced efficiency.

2.9 SUMMARY

In this chapter, the steady-state analysis of the single-phase SBI is presented, and the low-frequency ripple problem of the single-phase SBI is illustrated. Based on the low-frequency ripple analysis, the passive elements of the active-front-end network of the SBI are designed, which reveals that significantly large passive elements are required to restrict the low-frequency ripple. As a solution, the single-phase SBI is integrated with three independent APD networks in order to transfer low-frequency ripple power directly from the ac load to an auxiliary capacitor. A low-frequency ripple analysis of the APD-integrated SBI has been carried out, and it is observed that significantly less ripple on the capacitor voltage and the inductor current of the active-front-end network has been achieved. Owing to the additional

APD network, a reduction in both capacitor and inductor requirements is achieved. Based on the analysis, a design procedure for the passive elements of the active-front-end network and APD topology has been presented. A comparison between three APD networks suggests the boost-type APD network is the most suitable type for integration with single-phase SBI. Hence, the boost-type APD-integrated SBI is chosen for hardware implementation. A closed-loop control strategy for accurate low-frequency ripple mitigation has been presented. The proportional-resonant (PR) is chosen as the current controller as a very low steady-state error has been observed for PR while tracking reference ripple current. The parameters of the PR controller have been chosen based on the small-signal analysis of the APD topology. The system is fabricated in hardware, and the presented experimental results for steady-state operation and transient performance of the system due to ac load change are consistent with the analysis. When single-phase SBI is operated with APD, a slight drop in efficiency is observed due to additional switches and passive elements. The reduced efficiency is considered a compromise to achieve better reliability and the lifetime of the system because more reliable film capacitors can be employed instead of conventional electrolytic ones for all of the capacitors in the boost-type APD-integrated SBI.

CHAPTER 3

REDUCED-SWITCH CURRENT-FED SWITCHED INVERTER

3.1 INTRODUCTION

Chapter 1 presented several drawbacks of the conventional single-phase VSI, viz., lower peak ac output voltage compared to dc input voltage, essential requirement of dead-time for prevention of shoot-through in the legs of inverter bridge etc. The AFE-ISIs can eliminate these drawbacks using the active-front-end network. Several AFE-ISIs are proposed in the literature as an alternative to the conventional VSI. The AFE-ISIs can operate in wide range of voltages as well as protect the inverter switches against shoot-through. Among AFE-ISIs, the SBI reduces the number of passive elements and achieves improved power density than ZSI and qZSI. In Chapter 2, the circuit diagram and steady-state analysis of SBI are presented. Note that the voltage gain of SBI is lower than ZSI and qZSI as observed in Chapter 2. Thus, the application of SBI becomes restricted. Also, the input current profile of the SBI is discontinuous, which makes it less appropriate for renewable energy applications. The CFSI can solve the problems of the SBI as it improves voltage gain as well as provides a continuous input current. However, the lower efficiency is still an issue in existing AFE-ISIs. Therefore, better topological solutions are explored in this chapter, and as a result, the Reduced-Switch Current-Fed Switched Inverter (RSCFSI) is proposed. The RSCFSI has one less switch than SBI and CFSI, while retaining all features of CFSI.

In this chapter, the RSCFSI topology is derived from the complimentary current-fed dc-dc topology. The operating principles, the boost factor and the dc-to-ac gain of the RSCFSI depends on the PWM strategy. To achieve a boost factor that is same as the CFSI, the gate pulses of RSCFSI are generated using the simple boost control-based PWM (SBC-PWM) strategy. In this chapter, with SBC-PWM, the operating principles of RSCFSI are explained, and its boost factor and the dc-to-ac voltage gain are derived. Furthermore, the enhanced boost

control PWM (EBC-PWM) is proposed to improve the boost factor of the inverter. Similarly, with EBC-PWM, the operating principles of RSCFSI is illustrated, and its boost factor and the dc-to-ac voltage gain are derived in this chapter. A comparison between SBC-PWM and EBC-PWM is also presented. In order to illustrate the advantages of RSCFSI, it is compared with SBI and CFSI. A closed-loop control strategy is proposed to regulate its output voltage and the dc-link voltage.

This chapter is organized as follows: in **Section 3.2**, the derivation of RSCFSI topology is explained along with the complete circuit diagram. In **Section 3.3**, the operating principles of the single-phase RSCFSI are explained with the SBC-PWM strategy. **Section 3.4** describes the EBC-PWM strategy. Both PWM strategies are compared in **Section 3.5**. A comparison of the RSCFSI topology with the existing AFE-ISI topologies is presented in **Section 3.6**. A closed-loop control for the RSCFSI is illustrated in **Section 3.7**. The RSCFSI and the PWM strategies are validated with the help of hardware prototype, and the corresponding experimental results are illustrated in **Section 3.8**. Finally, the summary of this chapter is given in **Section 3.9**.

3.2 DERIVATION OF SINGLE-PHASE RSCFSI TOPOLOGY

The circuit diagram of the current-fed dc-dc topology is shown in Fig. 3.1(a). In D interval, both switches are in position '1', and the equivalent circuit is shown in Fig. 3.1(b). The instantaneous voltage across L is:

$$v_L(t) = V_g - v_c(t) \tag{3.1}$$

In $(1 - D)$ interval, both switches are in position '0', and the equivalent circuit is shown in Fig. 3.1(c). The instantaneous voltage across L is:

$$v_L(t) = V_g + v_c(t) \tag{3.2}$$

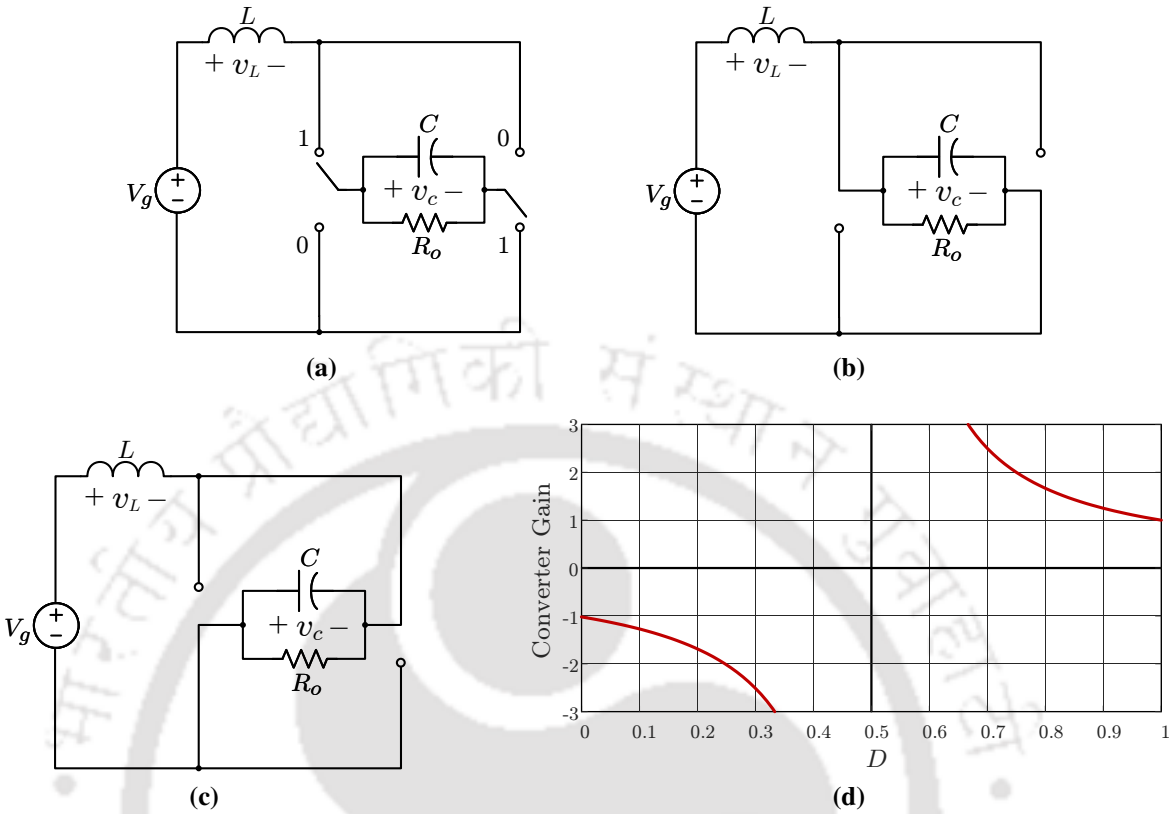


Fig. 3.1 (a) Circuit diagram of the current-fed dc/dc topology, (b) with switch at position 1, (c) with switch at position 0 and (d) conversion ratio.

From the volt-second balance of the inductor L, the average voltage across L over one switching cycle is zero, which gives:

$$\langle v_L(t) \rangle_{T_s} = D \cdot (V_g - V_c) + (1 - D) \cdot (V_g + V_c) = 0. \tag{3.3}$$

where V_c is the average value of the output capacitor.

Therefore, the conversion ratio of current-fed topology can be obtained as follows:

$$\frac{V_c}{V_g} = \frac{1}{2D - 1} \tag{3.4}$$

The conversion ratio of current-fed topology is plotted in Fig. 3.1(d). It is noted that the converter gain is negative when the duty ratio (D) of the converter is between 0 and 0.5, and the gain is positive when D is beyond 0.5. If the gain is desired to be positive when D is in

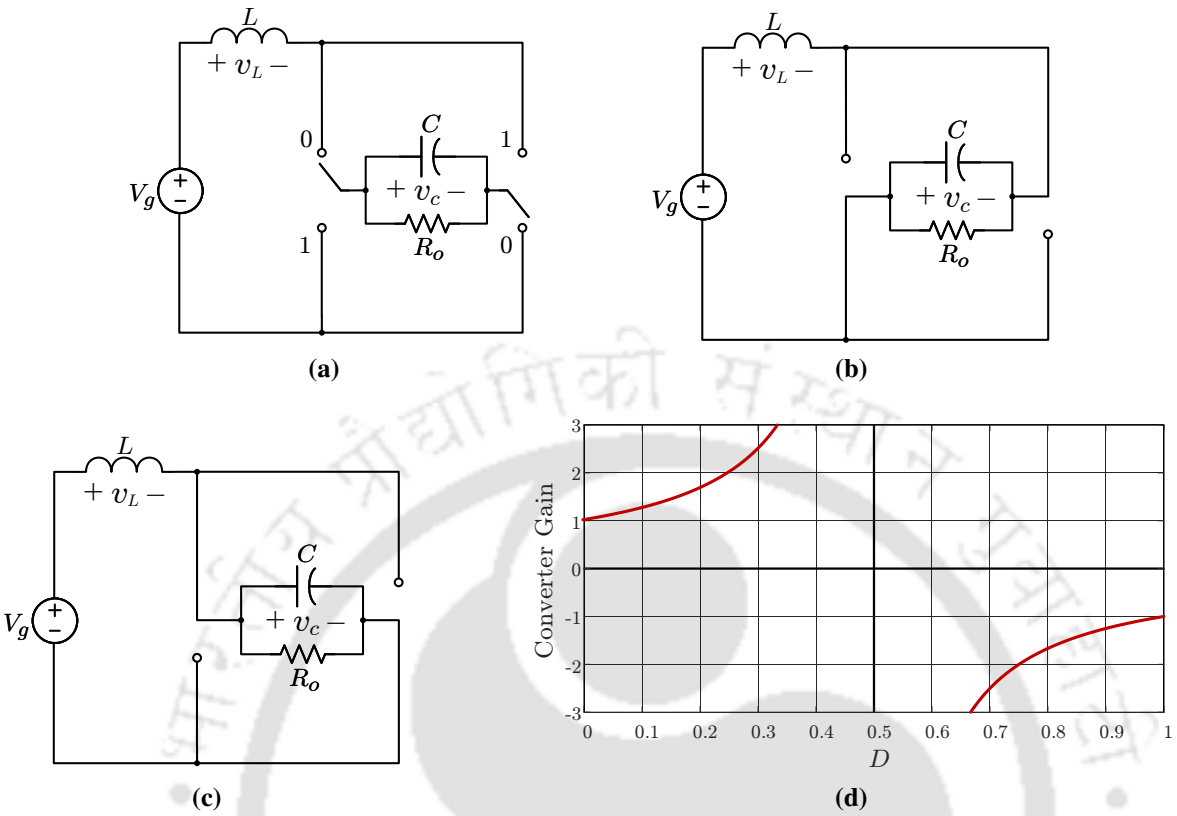


Fig. 3.2 (a) Circuit diagram of the complementary current-fed dc/dc topology, (b) with switch at position 1, (c) with switch at position 0 and (d) conversion ratio.

between 0 and 0.5, the D and $(1-D)$ intervals of current-fed topology must be interchanged [25]. Thus, the complementary current-fed dc/dc topology is obtained as shown in Fig. 3.2(a), which is derived by interchanging the positions '1' and '0' in current-fed dc/dc topology.

In D interval, the switches are kept at position '1', and the equivalent circuit is shown in Fig. 3.2(b). The instantaneous voltage across L is:

$$v_L(t) = V_g + v_c(t) \tag{3.5}$$

In $(1-D)$ interval, the switches are placed at position '0', and the equivalent circuit is shown in Fig. 3.2(c). The instantaneous voltage across L is:

$$v_L(t) = V_g - v_c(t) \tag{3.6}$$

From the volt-second balance of the inductor L, the average voltage across L over one switching cycle is zero, which gives:

$$\langle v_L(t) \rangle_{T_s} = D \cdot (V_g + V_c) + (1 - D) \cdot (V_g - V_c) = 0. \tag{3.7}$$

Thus, the conversion ratio of complimentary current-fed dc/dc topology is obtained as

$$\frac{V_c}{V_g} = \frac{1}{1 - 2D} \tag{3.8}$$

The conversion ratio is plotted in Fig. 3.2(d). When $D < 0.5$, the output of the converter is positive. For $D > 0.5$, the output polarity becomes negative. In this chapter, $D < 0.5$ is only considered as a valid region of operation to make switch realization easier.

Fig. 3.3(a) shows the realization of Fig. 3.2(a) using active and passive switches, i.e., two switches, S_a and S_b, and two diodes, D_a and D_b. The load is realized using a resistor R_o. The switch S_a can be replaced with two switches, S_1, S_4. Similarly, the switch S_b can be replaced with two switches, S_3, S_2. With four switches, the modified circuit is depicted in Fig. 3.3(b). The circuit is redrawn with a different orientation in Fig. 3.3(c). Instead of connecting the load across the capacitor, if it is connected across the terminals a-b, an alternate circuit is realized as shown in Fig. 3.3(d). In this circuit, the inverter is realized using existing four switches S_1-S_4. However, in this circuit, the voltage across R_o contains both dc component and ac component. To offset this dc component, an offset capacitor is added in series with the load as shown in Fig. 3.3(e).

This topology is called Reduced-Switch Current-Fed Switched Inverter (RSCFSI) in this thesis. Its complete circuit diagram is illustrated in Fig. 3.4. Note that one inductor (L), one capacitor (C) and two diodes (D_a, D_b) complete the active-front-end network. In this thesis, the active devices in RSCFSI are realized using insulated gate bipolar transistors (IGBTs). In Chapter 2, the inverter input voltage v_i has been used in the circuit analysis for SBI. However, in RSCFSI, the same voltage cannot be defined in a similar manner owing to the topological difference between RSCFSI and SBI. Alternatively, the voltage across the series combination

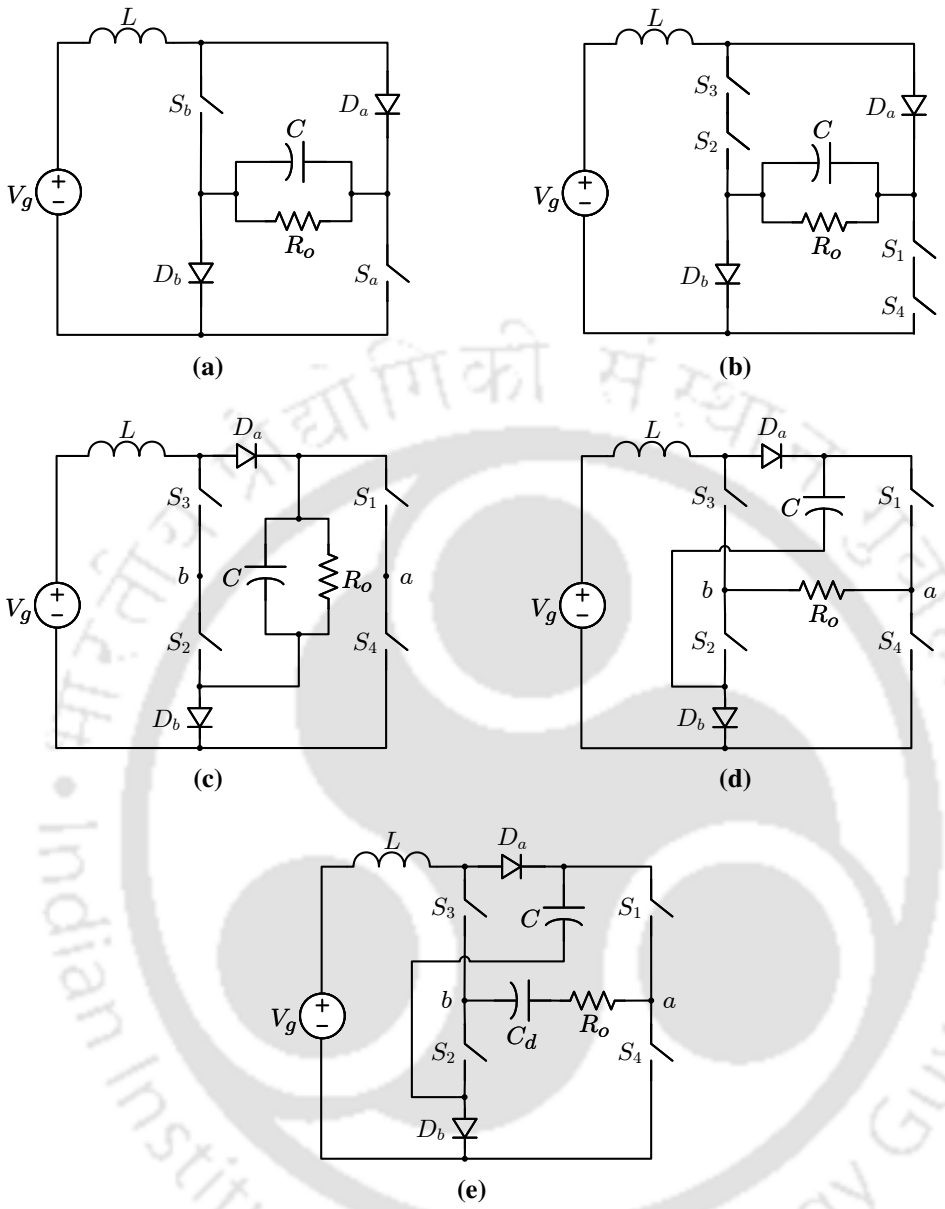


Fig. 3.3 Derivation of RSCFSI topology from complimentary current-fed topology: (a) realization using active and passive devices, (b) redrawing (a) using four switches instead of two, (c) redrawing (b), (d) shifting of load to the switching terminals and (e) addition of the offset capacitor to form the complete RSCFSI topology.

of switches S_1, S_4 is taken as v_{i1}, and the voltage across the series combination of the switches S_3, S_2 is taken as v_{i2} as shown in Fig. 3.4. In SBI, $v_{i1} = v_{i2} = v_i$, but in RSCFSI, v_{i1} and v_{i2} are different because of the position of the diodes D_a and D_b.

The main topological difference between the RSCFSI and the CFSI is the presence of an additional active switch S in the CFSI, shown in Fig. 3.5. This switch is essential for the shoot-through state in CFSI so that the dc input voltage (V_g) can be stepped up and applied as

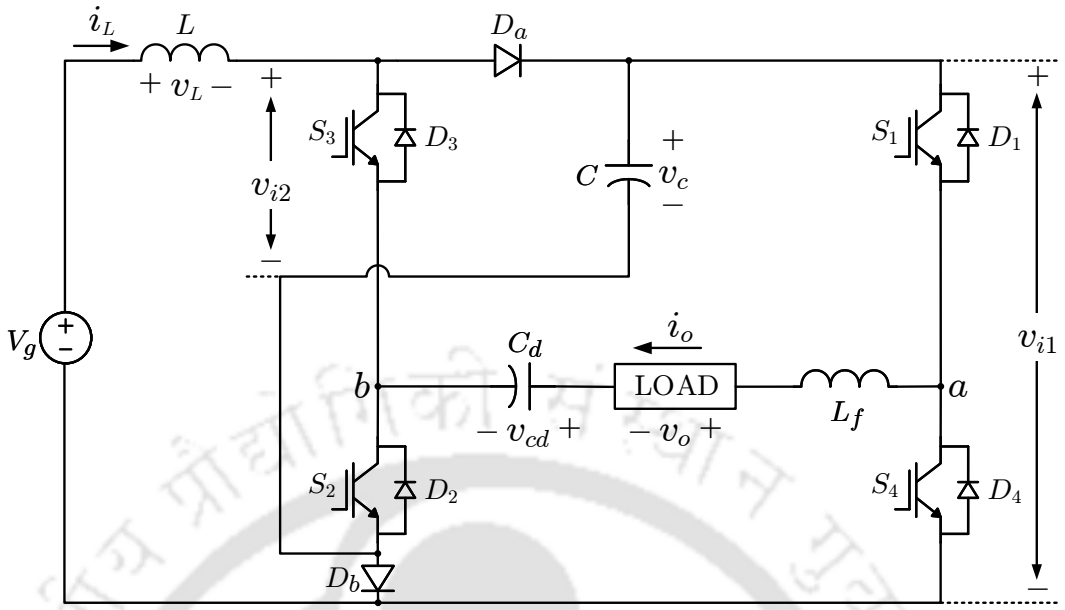


Fig. 3.4 Circuit diagram of Reduced-Switch Current-Fed Switched Inverter (RSCFSI).

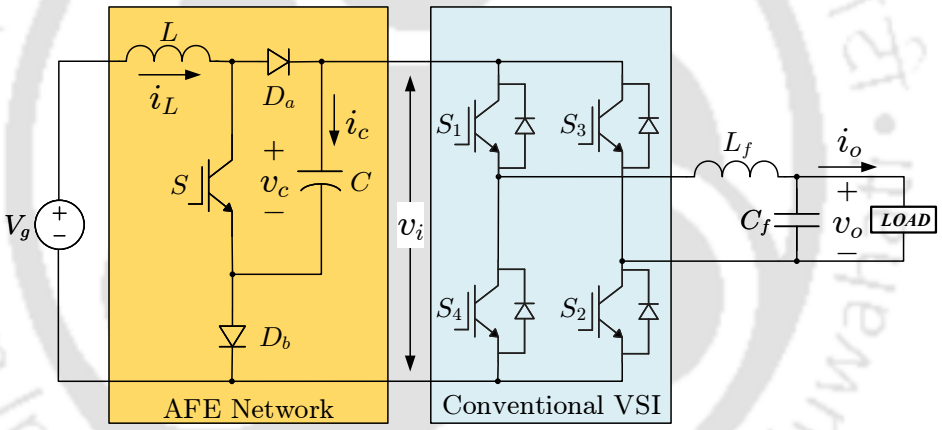


Fig. 3.5 Circuit diagram of Current-Fed Switched Inverter (CFSI).

the effective input voltage of the inverter bridge. However, the RSCFSI does not require this additional switch for the shoot-through state. Instead, the shoot-through of the both inverter legs is part of its operation, when S_1, S_2, S_3 and S_4 are turned on at the same time. Therefore, the RSCFSI provides single-stage dc-ac inversion as well as buck and boost capabilities. In the nonshoot-through interval of the inverter, either S_1, S_2 or S_3, S_4 are turned on together to transfer power to the load. In a VSI structure, shoot-through in any of the inverter leg is not permitted due to the potential damage to switches. Therefore, a dead-time between complementary switching signals is always in place. As turning on of both switches of an inverter leg is a valid state, RSCFSI has better EMI noise immunity, similar to SBI and CFSI.

Table 3.1 Possible operational states of RSCFSI with switching conditions and inverter output voltage

State	ON Elements	OFF Elements	v_{ab}
Shoot-through 1	S_1, S_2, S_3, S_4	D_a, D_b	v_c
Shoot-through 2	S_2, S_3, S_4, D_b	S_1, D_a	0
Shoot-through 3	S_1, S_2, S_3, D_b	S_4, D_a	v_c
Shoot-through 4	S_1, S_2, S_4, D_a	S_3, D_b	v_c
Shoot-through 5	S_1, S_3, S_4, D_a	S_2, D_b	0
Nonshoot-through 1	S_1, S_2, D_a, D_b	S_3, S_4	v_c
Nonshoot-through 2	S_3, S_4, D_a, D_b	S_1, S_2	$-v_c$
Nonshoot-through 3	S_1, S_3, D_a, D_b	S_2, S_4	0
Nonshoot-through 4	S_2, S_4, D_a, D_b	S_1, S_3	0

The operating principles, boost factor and dc-to-ac gain of RSCFSI depend on the PWM strategies. The possible operational states are presented in Table 3.1, where five shoot-through states and four nonshoot-through states are shown with switching conditions. In shoot-through state-1, all four switches of RSCFSI are turned on simultaneously. In shoot-through states 2-5, three switches are turned on at the same time. The nonshoot-through states 1-4 are similar to the switching states of a conventional VSI.

Based on the possible operational states, two PWM strategies are illustrated in this chapter as follows: (i) simple boost control-based PWM (SBC-PWM) and (ii) enhanced boost control-based PWM (EBC-PWM). In SBC-PWM, shoot-through state-1 and nonshoot-through states 1-4 are utilized from all the possible states described in Table 3.1. With this PWM strategy, the boost factor and dc-ac voltage gain of RSCFSI are the same as that of CFSI. To further improve the boost factor and dc-ac voltage gain, the EBC-PWM strategy is proposed. In EBC-PWM strategy, shoot-through states 1-3 and nonshoot-through states 1-4 are utilized from all the possible states described in Table 3.1. The detailed operating principles of RSCFSI with SBC-PWM and EBC-PWM are described in Section 3.3 and Section 3.4, respectively.

3.3 SIMPLE BOOST CONTROL-BASED PWM STRATEGY

3.3.1 Operating principles of RSCFSI using SBC-PWM

For the circuit analysis of the single-phase RSCFSI during shoot-through and non-shoot-through interval, it is assumed that the RSCFSI consists of all ideal elements and is operating

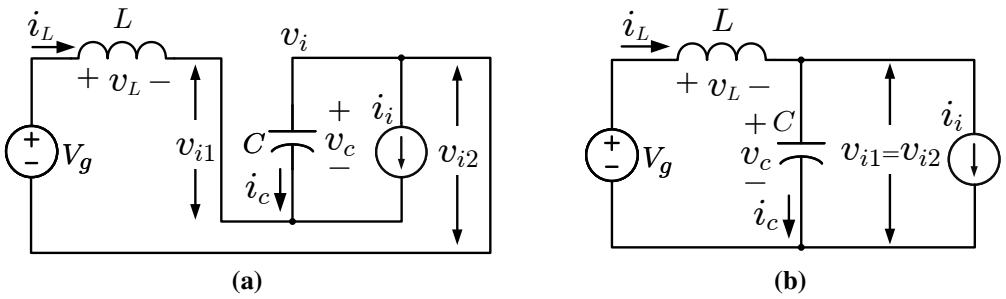


Fig. 3.6 Equivalent circuit diagrams of RSCFSI: (a) shoot-through state-1 and (b) nonshoot-through states 1-4.

in a continuous conduction mode. The equivalent circuit diagram of the RSCFSI during the shoot-through state is shown in Fig. 3.6(a). In the shoot-through state, all four switches are turned on together. The diodes D_a, D_b becomes reverse biased, because the capacitor C is placed parallel to them. As shown in Fig. 3.6(a), the inductor L is charged by the input voltage V_g and the capacitor C together during this interval. As observed in Fig. 3.6(a), both v_{i1} and v_{i2} are zero, because all four switches are turned on. The inverter output voltage v_{ab} is equal to v_c. However, in SBI and CFSI, v_{ab} remains zero during the shoot-through interval, and the power coming from the dc side is considered as zero. Owing to a non-zero v_{ab}, the power delivered to the ac side is non-zero for RSCFSI in this interval. Therefore, the inverter is represented as a current source i_i. The duration of the shoot-through time interval is $D \cdot T_s$, where D is shoot-through duty ratio, and T_s is the total switching time period. Following this analysis, the mathematical equations are expressed as:

$$\begin{aligned} v_L(t) &= V_g + v_c(t) \\ i_c(t) &= -i_L(t) - i_i(t) \\ v_{i1}(t) &= 0 \\ v_{i2}(t) &= 0 \\ v_{ab}(t) &= v_c(t) \end{aligned} \tag{3.9}$$

The equivalent circuit diagram of the RSCFSI during the nonshoot-through state is shown in Fig. 3.6(b). During the nonshoot-through interval, the RSCFSI operates similar to the conventional single-phase VSI. The diodes D_a and D_b become forward-biased, because none

of the inverter legs are shorted in this interval. Therefore, both v_{i1} and v_{i2} becomes equal to v_c. Hence, in the equivalent circuit shown in Fig. 3.6(b), the inverter can be represented as a current source i_i during the nonshoot-through interval. Note that the duration of this interval is $(1-D)\cdot T_s$. In this interval, the input inductor L is discharged, and the dc-link capacitor C is charged by the input voltage source V_g along with L. Also, the power is delivered to the ac load through the inverter. Hence, the mathematical equations can be written as:

$$\begin{aligned} v_L(t) &= V_g - v_c(t) \\ i_c(t) &= i_L(t) - i_i(t) \\ v_{i1}(t) &= v_{i2}(t) = v_c(t) \end{aligned} \tag{3.10}$$

3.3.2 Determination of dc-dc gain with SBC-PWM

Applying small ripple approximation to (3.9) and (3.10), the voltage across inductor L and the current through capacitor C in one switching period of T_s are obtained as:

$$v_L(t) = \begin{cases} V_g + V_c, & \text{if } 0 < t < D\cdot T_s \\ V_g - V_c, & \text{if } D\cdot T_s < t < T_s \end{cases} \tag{3.11}$$

$$i_c(t) = \begin{cases} -I_L - I_i; & \text{if } 0 < t < D\cdot T_s \\ I_L - I_i; & \text{if } D\cdot T_s < t < T_s \end{cases} \tag{3.12}$$

In steady-state, over one switching cycle, the average voltage across the inductor $\langle v_L(t)\rangle_{T_s}$ and the average current through the capacitor $\langle i_c(t)\rangle_{T_s}$ should be zero. Therefore, using inductor volt-second balance, one can write

$$\langle v_L(t)\rangle_{T_s} = D\cdot(V_g + V_c) + (1-D)\cdot(V_g - V_c) = 0. \tag{3.13}$$

From (3.13), the average value of v_c is determined as:

$$V_c = \left(\frac{1}{1-2D}\right) \cdot V_g = B_F V_g \tag{3.14}$$

where B_F is the dc-dc gain or boost factor of RSCFSI. Similarly, using capacitor amp-second balance, one can obtain

$$\langle i_c(t) \rangle_{T_s} = D \cdot (-I_L - I_i) + (1-D) \cdot (I_L - I_i) = 0 \tag{3.15}$$

From (3.15), the average value of i_L is derived as:

$$I_L = \left(\frac{1}{1-2D}\right) \cdot I_i \tag{3.16}$$

where I_i is the average value of i_i.

3.3.3 Determination of dc-ac gain with SBC-PWM

The relationship between the peak value of the fundamental ac output voltage of the inverter v_{ab} and input dc source voltage V_g is,

$$\hat{v}_{ab1} = M \cdot V_c = M \cdot \left(\frac{1}{1-2D}\right) \cdot V_g \tag{3.17}$$

where M is the modulation index of the inverter. Furthermore, the relationship between the output voltage (v_o) and v_{ab}

$$v_{ab}(t) = v_o(t) - v_{cd}(t) + v_{Lf}(t) \tag{3.18}$$

For sinusoidal output voltage (v_o) and current (i_o), the expressions can be taken as

$$\begin{aligned} v_o(t) &= \sqrt{2} V_o \sin \omega_o t \\ i_o(t) &= \sqrt{2} I_o \sin(\omega_o t - \varphi) \end{aligned} \tag{3.19}$$

where ω_o is the fundamental frequency and φ is the phase difference between v_o and i_o. In Fig. 3.4, it can be noticed that i_o flows through L_f. Thus, the voltage across L_f is

$$v_{Lf}(t) = L_f \frac{di_o(t)}{dt} = \sqrt{2} I_o \omega L_f \cos(\omega t - \varphi) \tag{3.20}$$

In the shoot-through states, as v_{ab} cannot always be deemed zero, a dc offset will be reckoned in v_{ab}. The duration of the shoot-through state is $D \cdot T_s$, and v_{ab} is equal to v_c in this state. Therefore, the dc offset in v_{ab} becomes

$$V_{\text{off}} = D \cdot V_c = \frac{D}{1 - 2D} \cdot V_g. \tag{3.21}$$

Consequently, a dc capacitor C_d is essential to counter the dc offset at the output so that the average voltage across C_d becomes

$$V_{cd} = V_{\text{off}} = D \cdot V_c \tag{3.22}$$

which ensures that v_o remains entirely ac. As the current i_o is flowing through the offset capacitor C_d, one can write

$$C_d \cdot \frac{dv_{cd}(t)}{dt} = i_o(t) \tag{3.23}$$

Therefore, the voltage across C_d can be derived as

$$v_{cd}(t) = D \cdot V_c - \frac{\sqrt{2} I_o}{\omega_o C_d} \cos(\omega_o t - \varphi) = V_{cd} + \tilde{v}_{cd}(t) \tag{3.24}$$

where V_{cd} and $\tilde{v}_{cd}$ are average and low-frequency components of v_{cd}, respectively.

Therefore, the relationship between the v_o and v_{ab1} becomes

$$\begin{aligned} v_{ab1}(t) &= v_o(t) + \tilde{v}_{cd}(t) + v_{Lf}(t) \\ &= \sqrt{2} V_o \sin \omega t - \sqrt{2} I_o \left(\frac{1}{\omega C_d} - \omega L_f \right) \cos(\omega t - \varphi) \\ &= \sqrt{2} V_o \sin \omega t - \sqrt{2} I_o X_f \cos(\omega t - \varphi) \end{aligned} \tag{3.25}$$

where $X_f = \left(\frac{1}{\omega C_d} - \omega L_f\right)$. Considering the output load as

$$\begin{aligned} Z_o &= R_o + jX_o \\ |Z_o| &= \sqrt{R_o^2 + X_o^2} \\ \varphi &= \tan^{-1}\left(\frac{X_o}{R_o}\right) \end{aligned} \tag{3.26}$$

where R_o and X_o are considered to be the resistive and the inductive part of the load, respectively, connected at the output. From (3.26), one can write

$$I_o = \frac{V_o}{R_o}\cos\varphi \tag{3.27}$$

Using (3.27) in (3.25),

$$v_{ab1}(t) = \sqrt{2}V_o\{\sin\omega t - \frac{X_f}{R_o}\cos\varphi\cos(\omega t - \varphi)\} = \sqrt{2}V_o A_1 \sin(\omega t - \lambda_1) \tag{3.28}$$

where

$$A_1 = \left[\sqrt{\left\{1 + \frac{X_f}{R_o}\sin\varphi\cos\varphi\right\}^2 + \left\{\frac{X_f}{R_o}\cos^2\varphi\right\}^2}\right]$$

$$\lambda_1 = \tan^{-1}\frac{\left\{\frac{X_f}{R_o}\cos^2\varphi\right\}}{\left\{1 + \frac{X_f}{R_o}\sin\varphi\cos\varphi\right\}}$$

Considering $\varphi = 0$, the peak output ac voltage is derived by solving (3.17) and (3.28) as

$$\hat{v}_o = \sqrt{2}V_o = \frac{M}{A_1} = \frac{M}{\sqrt{1 + (X_f/R_o)^2}} \cdot V_c = M' \cdot \left(\frac{1}{1 - 2D}\right) \cdot V_g \tag{3.29}$$

Since $R_o >> X_f$, one can write $M' \approx M$, which indicates

$$\hat{v}_o \approx \hat{v}_{ab1} = M \cdot V_c = M \cdot \left(\frac{1}{1 - 2D}\right) \cdot V_g \tag{3.30}$$

Using (3.19), one can express the output power (p_o) as follows

$$p_o(t) = v_o(t) \cdot i_o(t) = V_o I_o \cos\varphi - V_o I_o \cos(2\omega_o t - \varphi) = P_o + p'_r(t) \tag{3.31}$$

which contains two components: the constant active power (P_o) and the low-frequency ripple power (p'_r). Hence, due to the presence of p'_r, low-frequency ripples will occur in the dc side. The low-frequency ripple problem of RSCFSI will be discussed separately in detail in Chapter 4. As mentioned previously, power is transferred from input to output of the inverter in both shoot-through and nonshoot-through states for RSCFSI. Therefore, p_o must be equal to the input power of the inverter (p_i) as follows:

$$p_i(t) = v_c(t) \cdot i_i(t) = p_o. \tag{3.32}$$

which can be expanded as

$$\{V_c + \tilde{v}_c(t)\} \cdot \{I_i + \tilde{i}_i(t)\} = P_o + p'_r(t) \tag{3.33}$$

where $\tilde{v}_c$ and $\tilde{i}_i$ are the ac component of v_c and i_i, respectively. Equating the dc components on both sides, the following expression can be obtained

$$V_c \cdot I_i = V_o I_o \cos\varphi \tag{3.34}$$

Using (3.30) in (3.34), I_i is expressed as:

$$I_i = \frac{M I_o}{\sqrt{2}} \cos\varphi \tag{3.35}$$

Therefore, putting (3.35) in (3.16), the average value of i_L is derived as:

$$I_L = \left(\frac{1}{1-2D}\right) \cdot \frac{M I_o}{\sqrt{2}} \cos\varphi \tag{3.36}$$

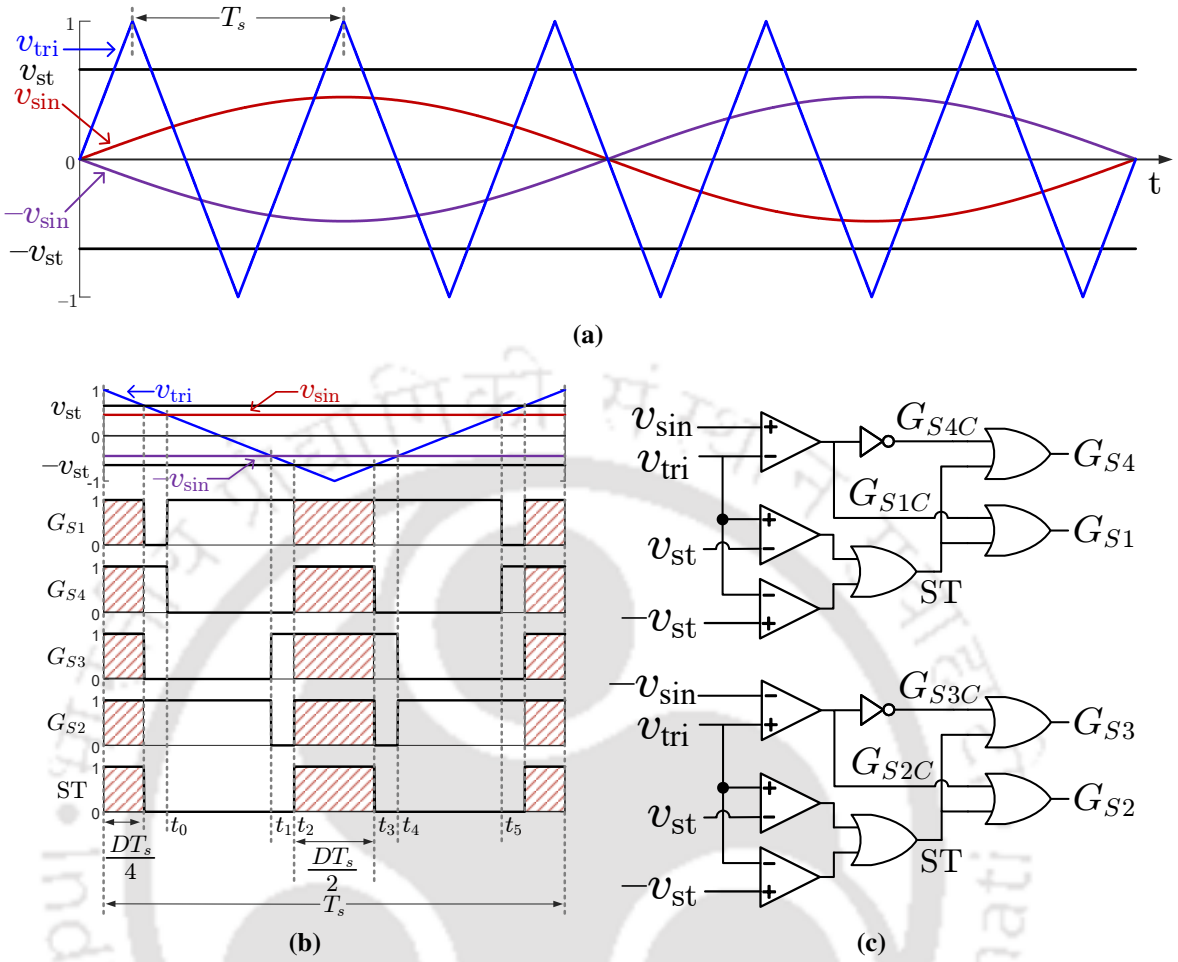


Fig. 3.7 SBC-PWM for RSCFSI: (a) sinusoidal modulation and triangular carrier signals, (b) generation of gate control signals and (c) PWM control scheme.

3.3.4 Generation of gate pulses using SBC-PWM

To incorporate the shoot-through state in the PWM control, the traditional PWM technique for VSI needs to be modified accordingly. The modified PWM scheme for RSCFSI is developed based on the traditional sine-triangle PWM with unipolar voltage switching as exhibited in Fig. 3.7(a), where the sinusoidal modulation signals $\pm v_{\text{sin}}$ and triangular carrier signal v_{tri} are shown. Note that the carrier signal frequency is much higher than the modulation signal frequency ($f_{\text{tri}} >> f_{\text{sin}}$), but for demonstration purposes, it is shown to be very less. The gate pulses for the switches S_1, S_2, S_3 and S_4 are G_{S1}, G_{S2}, G_{S3} and G_{S4}, respectively, which are demonstrated in Fig. 3.7(b). Further, the schematic of the switching strategy for RSCFSI is illustrated in Fig. 3.7(c).

In conventional sine-triangle PWM, the gate pulse for switch S_1, denoted as G_{S1C}, is generated from a triangular carrier signal v_{tri} and a sinusoidal modulation signal v_{sin}. The gate pulse for switch S_4 is the complementary signal of G_{S1C} and is denoted as G_{S4C}. Similarly, the gate pulse for S_2 is generated from v_{tri} and $-v_{\text{sin}}$, which is denoted as G_{S2C}. The gate pulse for switch S_3 is the complementary signal of G_{S2C} and is denoted as G_{S3C}. Therefore, G_{S1C}, G_{S2C}, G_{S3C} and G_{S4C} are the gate signals to be used when the conventional sine-triangle PWM is applied to the inverter as shown in Fig. 3.7(c). The shoot-through duty ratio D can be varied by changing the shoot-through control voltages v_{st} and $-v_{\text{st}}$, as seen from Fig. 3.7(b). In order to insert shoot-through, the shoot-through signal ST, generated by comparing v_{st} and $-v_{\text{st}}$ with v_{tri}, is logically added with G_{S1C}, G_{S2C}, G_{S3C} and G_{S4C} to obtain the final gate signals G_{S1}, G_{S2}, G_{S3} and G_{S4} using the following logic as shown in Fig. 3.7(c).

$$\begin{aligned} G_{S1} &= G_{S1C} + \text{ST} \\ G_{S4} &= G_{S4C} + \text{ST} \\ G_{S3} &= G_{S3C} + \text{ST} \\ G_{S2} &= G_{S2C} + \text{ST} \end{aligned} \tag{3.37}$$

3.3.5 Limitation of modulation index

The shoot-through duty ratio D can be varied by changing the shoot-through control voltages v_{st} and $-v_{\text{st}}$, as seen from Fig. 3.7(b). To derive the mathematical relation between D and v_{st} consider the equations for the triangular carrier signal, which can be written as:

$$v_{\text{tri}}(t) = \begin{cases} -\dfrac{\hat{v}_{\text{tri}}}{\left(\frac{T_s}{4}\right)} \cdot \left(t - \dfrac{T_s}{4}\right) & \text{if } 0 < t < \dfrac{T_s}{2} \\ \dfrac{\hat{v}_{\text{tri}}}{\left(\frac{T_s}{4}\right)} \cdot \left(t - \dfrac{3T_s}{4}\right) & \text{if } \dfrac{T_s}{2} < t < T_s \end{cases} \tag{3.38}$$

From Fig. 3.7(b), it can be observed that at time t_0, the sinusoidal signal v_{sin} becomes equal to the triangular signal v_{tri}, and the switch S_1 is turned on. Further, $-v_{\text{sin}}$ becomes equal to v_{tri} at time t_1, and the switch S_1 is turned off. Also, between time t_0 and t_1, $v_{\text{tri}} > v_{\text{sin}}$,

which indicates that the switch S_2 is turned on. So, both S_1 and S_2 remains on between time t_0 and t_1, indicating occurrence of an active state. Therefore, at time t_0 and t_1 one can write

$$\begin{aligned} v_{\text{tri}}(t_0) &= v_{\text{sin}}(t_0) \\ v_{\text{tri}}(t_1) &= -v_{\text{sin}}(t_1) \end{aligned} \tag{3.39}$$

The limiting value of v_{sin} occurs at the peak, i.e., the modulation index M, which can be used in (3.39) to obtain the following

$$\begin{aligned} v_{\text{tri}}(t_0) &= M \\ v_{\text{tri}}(t_1) &= -M \end{aligned} \tag{3.40}$$

From (3.40), the expressions of t_0 and t_1 can be written as

$$\begin{aligned} t_0 &= \frac{T_s}{4} \cdot \left(1 - \frac{M}{\hat{v}_{\text{tri}}}\right) \\ t_1 &= \frac{T_s}{4} \cdot \left(1 + \frac{M}{\hat{v}_{\text{tri}}}\right) \end{aligned} \tag{3.41}$$

Therefore, the time interval between t_0 and t_1 is

$$t_1 - t_0 = \frac{M}{\hat{v}_{\text{tri}}} \cdot \frac{T_s}{2} \tag{3.42}$$

Hence, the total duration of active state becomes

$$T_{\text{active}} = \frac{M}{\hat{v}_{\text{tri}}} \cdot \frac{T_s}{2} \cdot 2 = \frac{M}{\hat{v}_{\text{tri}}} \cdot T_s \tag{3.43}$$

Therefore, the duration of the zero state is

$$T_{\text{zero}} = T_s - T_{\text{active}} = T_s - \frac{M}{\hat{v}_{\text{tri}}} \cdot T_s = \left(1 - \frac{M}{\hat{v}_{\text{tri}}}\right) \cdot T_s \tag{3.44}$$

In Fig. 3.7(b), it can be observed that the shoot-through signal ST is high between t_2 and t_3, where $-v_{\text{st}} > v_{\text{tri}}$. Therefore, one can write

$$v_{\text{tri}}(t_2) = v_{\text{tri}}(t_3) = -v_{\text{st}} \tag{3.45}$$

Therefore, from (3.38) and (3.45), the expressions of t_1 and t_2 can be written as

$$\begin{aligned} t_2 &= \frac{T_s}{4} \cdot \left(1 + \frac{v_{\text{st}}}{\hat{v}_{\text{tri}}}\right) \\ t_3 &= \frac{T_s}{4} \cdot \left(3 - \frac{v_{\text{st}}}{\hat{v}_{\text{tri}}}\right) \end{aligned} \tag{3.46}$$

Since shoot-through occurs twice in a switching cycle, the time interval between t_2 and t_3 is also expressed as,

$$t_3 - t_2 = \frac{DT_s}{2} \tag{3.47}$$

Solving (3.46) and (3.47), the total of shoot-through state is given by,

$$T_{\text{sh}} = D \cdot T_s = \left(1 - \frac{v_{\text{st}}}{\hat{v}_{\text{tri}}}\right) \cdot T_s \tag{3.48}$$

In order to ensure that the shoot-through interval does not overlap with the power interval of the inverter, D should be chosen such that the total width of the shoot-through interval does not exceed the total available width for zero interval in any switching cycle as follows:

$$T_{\text{zero}} > T_{\text{sh}} \tag{3.49}$$

which gives

$$\left(1 - \frac{M}{\hat{v}_{\text{tri}}}\right) \cdot T_s > DT_s \tag{3.50}$$

Using (3.48) in (3.50),

$$v_{\text{st}} = (1 - D) \cdot \hat{v}_{\text{tri}} > M \cdot \hat{v}_{\text{tri}} \tag{3.51}$$

In this chapter, $\hat{v}_{\text{tri}} = 1$. So, one can write

$$v_{\text{st}} = (1 - D) \tag{3.52}$$

From which, the limitation of M is found to be

$$M < (1 - D) \tag{3.53}$$

There is another limitation of the modulation index, which is needed to be taken into consideration owing to the presence of the offset capacitor C_d placed in series with the load. When the switches S_3 and S_4 are turned on together, one can write

$$v_c(t) = v_o(t) + v_{cd}(t) + v_{Lf}(t) \tag{3.54}$$

Since v_{Lf} is generally quite small, it can be ignored. Using (3.24) and (3.30) in (3.54), one can obtain the following inequality:

$$\begin{aligned} V_c &> M \cdot V_c + D \cdot V_c \\ \implies M &< (1 - D) \end{aligned} \tag{3.55}$$

which is same as (3.53). Therefore, the selection of the modulation index is limited by the shoot-through duty ratio. Thus, the dc-ac gain of RSCFSI with SBC-PWM becomes

$$B_{\text{AC}} = \frac{\hat{v}_o}{V_g} = \frac{MV_c}{V_g} < \left(\frac{1 - D}{1 - 2D}\right). \tag{3.56}$$

3.4 ENHANCED BOOST CONTROL-BASED PWM STRATEGY

In order to improve the boost factor and dc-ac gain of RSCFSI, another PWM strategy is proposed in this chapter, which is known as enhanced boost control-based PWM (EBC-PWM). In the SBC-PWM strategy, 5 states, which are one shoot-through and four nonshoot-through,

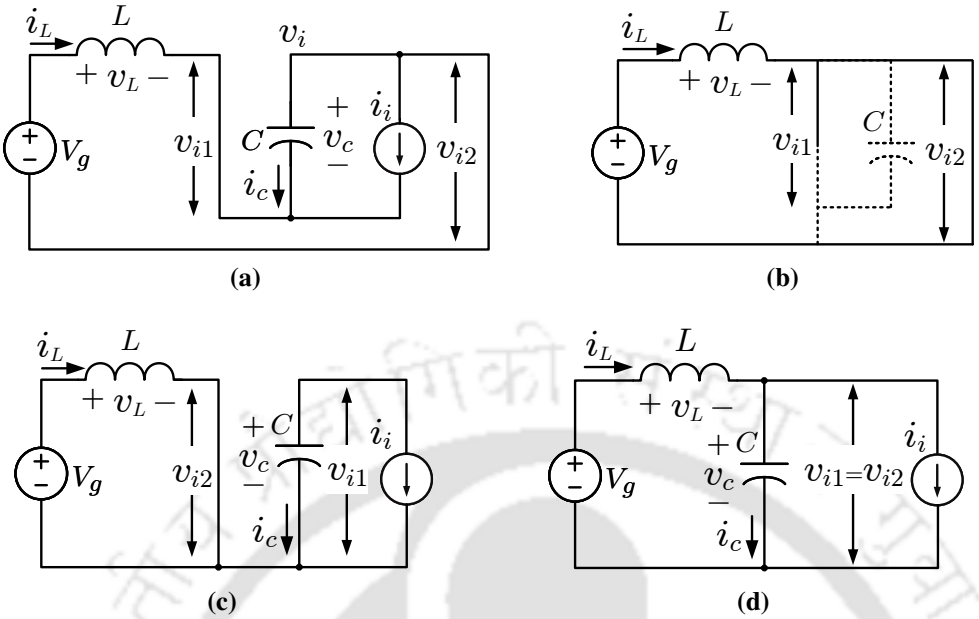


Fig. 3.8 Different states of operation of RSCFSI in EBC-PWM: (a) shoot-through state-1, (b) shoot-through state-2, (c) shoot-through state-3 and (d) nonshoot-through states 1-4.

are utilized from Table 3.1. With EBC-PWM, two additional shoot-through states are utilized to improve the boost factor of RSCFSI, compared to SBC-PWM.

3.4.1 Operating principles of RSCFSI using EBC-PWM

For the circuit analysis of the single-phase RSCFSI during shoot-through and non-shoot-through intervals, all the previous assumptions mentioned in Section 3.3 are again considered. The equivalent circuit diagram of the RSCFSI during the shoot-through state-1 is shown in Fig. 3.8(a). In the shoot-through state-1, all four switches are turned on together. The diodes D_a, D_b becomes reverse biased, because the capacitor C is placed parallel to them. The inductor L is charged by the input voltage V_g and the capacitor C together during this interval. In this state, the mathematical equations are same as (3.9). The rest of the duration of $(1-D)\cdot T_s$ is utilized for the shoot-through states 2-3 and the nonshoot-through state.

The equivalent circuit diagram of the RSCFSI during the shoot-through state-2 is shown in Fig. 3.8(b). This state is achieved by the inverter by turning on three switches at the same time. Both switches of the leg-2, i.e., S_2 and S_3 as well as S_1 should be turned on simultaneously. In this state, the diode D_b becomes forward-biased. The other diode D_a is reverse-biased as a

voltage of $(V_c - V_g)$ appears across it. Hence, the inductor L is charged by the input voltage V_g as observed in Fig. 3.8(b). The capacitor is disconnected from the rest of the circuit in this state. Since both S_2 and S_3 are turned on, v_{i2} is zero in this interval. At the same time, v_{i1} is equal to v_c, because S_4 and D_a are turned off. So, the mathematical equations in this state are

$$\begin{aligned} v_L(t) &= V_g \\ i_c(t) &= 0 \\ v_{i1}(t) &= v_c(t) \\ v_{i2}(t) &= 0 \\ v_{ab}(t) &= 0. \end{aligned} \tag{3.57}$$

The equivalent circuit diagram of the RSCFSI during the shoot-through state-3 is shown in Fig. 3.8(c). Similar to the shoot-through state-2, this state is also achieved by turning on three switches at the same time. Both switches of the leg-2, i.e., S_2 and S_3 as well as S_4 can be turned on together to achieve this state of operation. In this state, the diode D_a is reverse-biased, because a voltage of $(V_c - V_g)$ appears across it. The other diode D_b becomes forward-biased. Thus, L is charged by V_g as observed in Fig. 3.8(c). Since both S_2 and S_3 are turned on, v_{i2} is zero in this interval. At the same time, v_{i1} is equal to v_c, because S_1 is turned on, and D_a are turned off. The inverter output voltage v_{ab} is equal to v_c in shoot-through state-3. Similar to shoot-through state-1, owing to a non-zero v_{ab}, the power is transferred from the dc-side to the ac side in this state. Therefore, the inverter is represented as a current source i_i. Thus, the mathematical equations in this state are expressed as

$$\begin{aligned} v_L(t) &= V_g \\ i_c(t) &= -i_i(t) \\ v_{i1}(t) &= v_c(t) \\ v_{i2}(t) &= 0 \\ v_{ab}(t) &= v_c(t). \end{aligned} \tag{3.58}$$

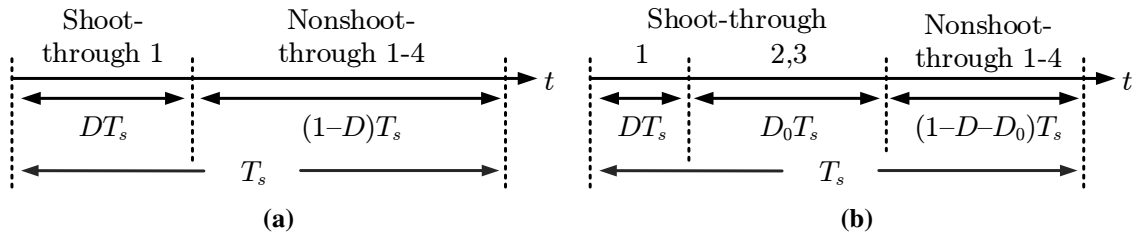


Fig. 3.9 Duration of shoot-through and nonshoot-through states (a) in SBC-PWM and (b) in EBC-PWM.

In SBC-PWM, the entire switching period is divided by shoot-through state-1 of duration $D \cdot T_s$ and nonshoot-through states 1-4 of duration $(1 - D) \cdot T_s$ as shown in 3.9(a). In EBC-PWM, because the inductor voltage is equal to V_g in both states, the duration of each of the shoot-through states 2 and 3 is taken as $D_0 \cdot T_s/2$, where D_0 is taken as

$$D_0 = \frac{1 - D}{2} \tag{3.59}$$

As shown in 3.9(b), the $(1 - D) \cdot T_s$ interval is equally between the shoot-through states 2, 3 and the nonshoot-through states 1-4.

Considering that both switches of the leg-2, i.e., S_2 and S_3 are turned on together in both shoot-through states 2 and 3, the shoot-through duty ratio of S_2 and S_3 becomes

$$D + D_0 = D + \left(\frac{1 - D}{2}\right) = \left(\frac{1 + D}{2}\right) \tag{3.60}$$

The equivalent circuit diagram of the RSCFSI during the nonshoot-through state is shown in Fig. 3.6(b). The nonshoot-through states 1-4 can be considered as a single state, because the RSCFSI operates similar to the conventional single-phase VSI. Hence, in the equivalent circuit shown in Fig. 3.6(b), the inverter can be represented as a current source i_i during the nonshoot-through interval. Note that the duration of this interval is $(1 - D - D_0) \cdot T_s = (1 - D) \cdot T_s/2$. In this interval, the input inductor L is discharged, and the dc-link capacitor C is charged by the input voltage source V_g along with L. Also, the power is delivered to the ac load through the inverter. Hence, the mathematical equations are same as (3.10) in this state.

3.4.2 Determination of dc-dc gain with EBC-PWM

Applying small ripple approximation to (3.9), (3.10), (3.57) and (3.58), the voltage across inductor L and the current through capacitor C in one switching period of T_s are obtained as:

$$v_L(t) = \begin{cases} V_g + V_c, & \text{if } 0 < t < D \cdot T_s \\ V_g, & \text{if } D \cdot T_s < t < \left(\frac{1+D}{2}\right) \cdot T_s \\ V_g - V_c, & \text{if } \left(\frac{1+D}{2}\right) \cdot T_s < t < T_s \end{cases} \tag{3.61}$$

$$i_c(t) = \begin{cases} -I_L - I_i; & \text{if } 0 < t < D \cdot T_s \\ 0; & \text{if } D \cdot T_s < t < \left(\frac{3D+1}{4}\right) \cdot T_s \\ -I_i; & \text{if } \left(\frac{3D+1}{4}\right) \cdot T_s < t < \left(\frac{1+D}{2}\right) \cdot T_s \\ I_L - I_i; & \text{if } \left(\frac{1+D}{2}\right) \cdot T_s < t < T_s \end{cases} \tag{3.62}$$

In steady-state, over one switching cycle, the average voltage across the inductor $\langle v_L(t)\rangle_{T_s}$ and average current through the capacitor $\langle i_c(t)\rangle_{T_s}$ should be zero. Therefore, using inductor volt-second balance, one can write

$$\langle v_L(t)\rangle_{T_s} = D \cdot (V_g + V_c) + \frac{(1-D)}{2} \cdot V_g + \frac{(1-D)}{2} \cdot (V_g - V_c) = 0. \tag{3.63}$$

From (3.63), the average value of v_c is determined as:

$$V_c = \left(\frac{2}{1-3D}\right) \cdot V_g = B_F V_g \tag{3.64}$$

which indicates the boost factor is significantly more than that achieved by RSCFSI with SBC-PWM strategy for same shoot-through duty ratio.

Similarly, using capacitor amp-second balance, one can obtain

$$\langle i_c(t)\rangle_{T_s} = D\cdot(-I_L - I_i) + \frac{(1-D)}{4}\cdot(-I_i) + \frac{(1-D)}{2}\cdot(I_L - I_i) = 0 \tag{3.65}$$

From (3.65), the average value of i_L is derived as:

$$I_L = \frac{1}{2}\cdot\left(\frac{D+3}{1-3D}\right)\cdot I_i \tag{3.66}$$

3.4.3 Determination of dc-ac gain with EBC-PWM

In EBC-PWM, the power is delivered in the shoot-through states 1 and 3 along with the nonshoot-through state for RSCFSI. Therefore, p_o must be equal to the power at the input of the inverter (p_i) as follows:

$$p_i(t) = \left\{1 - \left(\frac{1-D}{4}\right)\right\}\cdot v_c(t)\cdot i_i(t) = \left(\frac{D+3}{4}\right)\cdot v_c(t)\cdot i_i(t) = p_o(t). \tag{3.67}$$

Equating the dc components on both sides, one can obtain

$$\left(\frac{D+3}{4}\right)\cdot V_c\cdot I_i = V_o I_o\cos\varphi \tag{3.68}$$

Using (3.30) in (3.68), I_i is expressed as:

$$I_i = \left(\frac{4}{D+3}\right)\cdot\frac{MI_o}{\sqrt{2}}\cos\varphi \tag{3.69}$$

Therefore, putting (3.69) in (3.66), the average value of i_L is derived as:

$$I_L = \left(\frac{2}{1-3D}\right)\cdot\frac{MI_o}{\sqrt{2}}\cos\varphi \tag{3.70}$$

During shoot-through states 1 and 3, v_{ab} is equal to v_c, because of which, an offset voltage occurs at the output. The duration of shoot-through state-3 is $(1-D)\cdot T_s/4$, according to (3.59). Also, the duration of shoot-through state-1 is $D\cdot T_s$. Therefore, the dc offset in v_{ab}

becomes

$$V_{\text{off}} = \left(D + \frac{1-D}{4}\right) \cdot V_c = \left(\frac{3D+1}{4}\right) \cdot V_c = D_1 \cdot V_c. \tag{3.71}$$

where $D_1 = \left(\frac{3D+1}{4}\right)$. Similar to SBC-PWM, a dc capacitor C_d is essential to counter the dc offset at the output so that the average voltage across C_d becomes

$$V_{cd} = V_{\text{off}} = D_1 \cdot V_c \tag{3.72}$$

which ensures that v_o remains entirely ac. Therefore, (3.24) becomes modified as

$$v_{cd}(t) = D_1 V_c - \frac{\sqrt{2} I_o}{\omega_o C_d} \cos(\omega_o t - \varphi) = V_{cd} + \tilde{v}_{cd}(t) \tag{3.73}$$

In (3.53), the limitation of the modulation index M is established for SBC-PWM, which is same for EBC-PWM. However, in (3.55), another limitation of M is dictated by the presence of the offset capacitor C_d placed in series with the load, which needs to be modified for EBC-PWM. Using (3.30) and (3.73) in (3.54), one can obtain the following inequality:

$$\begin{aligned} V_c &> M \cdot V_c + D_1 \cdot V_c \\ \implies M &< (1 - D_1) \end{aligned} \tag{3.74}$$

Therefor, the dc-ac gain of RSCFSI with EBC-PWM becomes

$$B_{\text{AC}} = \frac{\hat{v}_o}{V_g} = \frac{M V_c}{V_g} < \left\{\frac{2(1-D_1)}{1-3D}\right\} = \frac{3}{2} \cdot \left(\frac{1-D}{1-3D}\right) \tag{3.75}$$

which is significantly more than the dc-ac gain achieved by RSCFSI with SBC-PWM strategy for same shoot-through duty ratio.

3.4.4 Generation of gate pulses using EBC-PWM

To incorporate the additional shoot-through states along with previously implemented shoot-through state-1 and nonshoot-through states 1-4 in the PWM control, the SBC-PWM

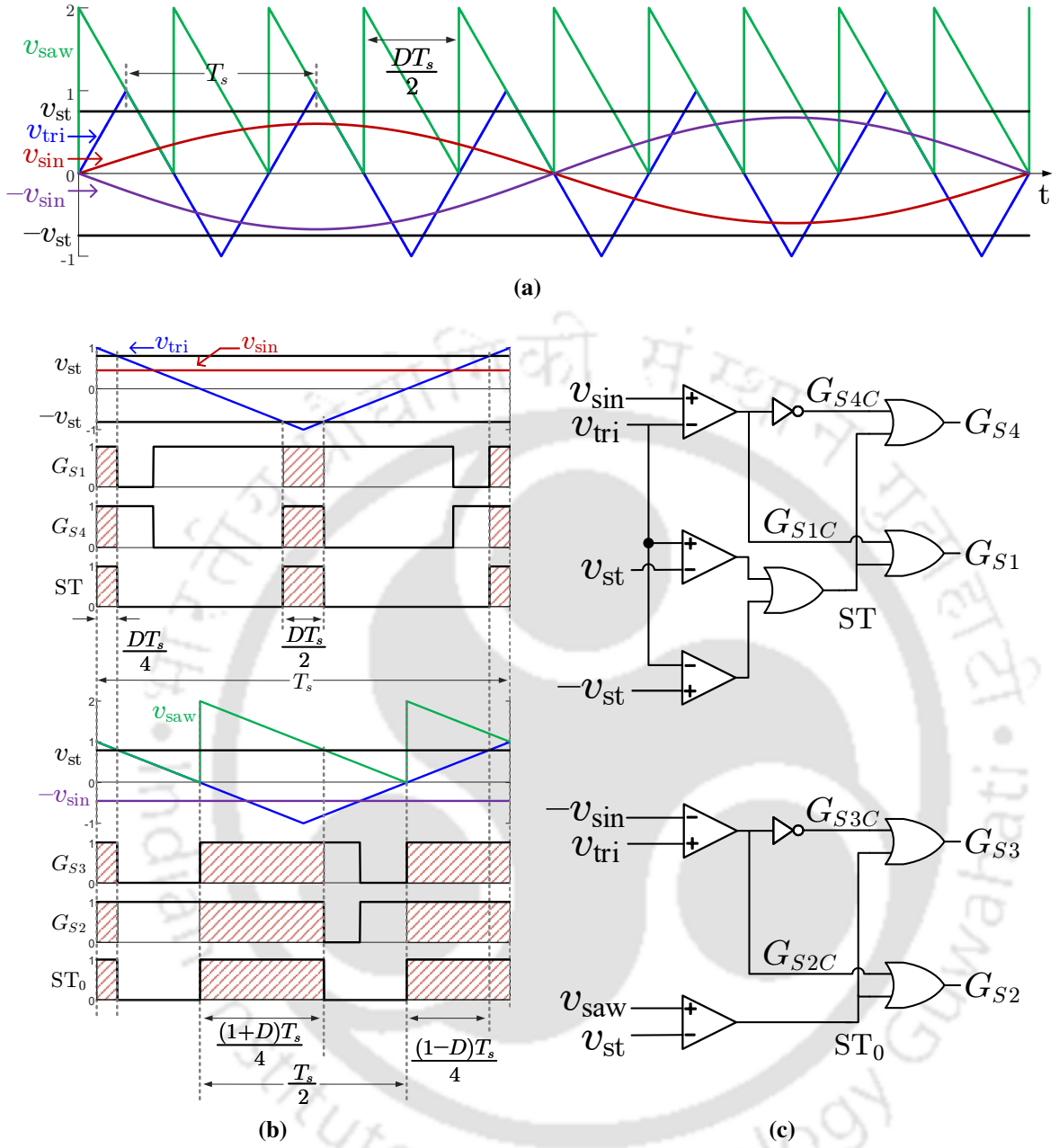


Fig. 3.10 EBC-PWM for RSCFSI: (a) sinusoidal modulation and triangular carrier signals, (b) generation of gate control signals and (c) PWM control scheme.

technique of Fig. 3.7 needs to be modified accordingly. The EBC-PWM scheme for RSCFSI is developed based on the traditional sine-triangle PWM with unipolar voltage switching as exhibited in Fig. 3.10(a), where the modulation and carrier signals are shown. The gate pulses for the switches S_1, S_2, S_3 and S_4 are G_{S1}, G_{S2}, G_{S3} and G_{S4}, respectively, which are demonstrated in Fig. 3.10(b). Further, the schematic of the switching strategy for RSCFSI is illustrated in Fig. 3.10(c).

As explained previously, G_{S1C}, G_{S2C}, G_{S3C} and G_{S4C} are the gate signals to be used when the conventional sine-triangle PWM is applied to the inverter. The method of generation and insertion of shoot-through to the gate signals for the switches S_1 and S_4 is same as SBC-PWM. The shoot-through signal ST is generated by comparing v_{st} and $-v_{\text{st}}$ with v_{tri}, and it is logically added with G_{S1C} and G_{S4C} to obtain the final gate signals G_{S1} and G_{S4} using the following logic as shown in Fig. 3.10(c).

$$\begin{aligned} G_{S1} &= G_{S1C} + \text{ST} \\ G_{S4} &= G_{S4C} + \text{ST} \end{aligned} \tag{3.76}$$

However, the method of generation and insertion of shoot-through to the gate signals for the switches S_2 and S_3 differs from SBC-PWM. A shoot-through signal ST_0, which is different than ST, is generated by comparing v_{st} with v_{saw}, and it is logically added with G_{S2C} and G_{S3C} to obtain the final gate signals G_{S2} and G_{S3} using the following logic as shown in Fig. 3.10(c).

$$\begin{aligned} G_{S3} &= G_{S3C} + \text{ST}_0 \\ G_{S2} &= G_{S2C} + \text{ST}_0 \end{aligned} \tag{3.77}$$

3.5 COMPARISON BETWEEN SBC-PWM AND EBC-PWM

To compare the boost factor and dc-ac gain of RSCFSI with SBC-PWM and EBC-PWM, the expression of v_c is reevaluated after considering the effect of parasitic resistance r_l of input inductor L. So, with the consideration of r_l, realized in series with L, the inductor voltage v_L using SBC-PWM, expressed in (3.11), is modified as

$$v_L(t) = \begin{cases} V_g + V_c - I_L r_l; & \text{if } 0 < t < D \cdot T_s \\ V_g - V_c - I_L r_l; & \text{if } D \cdot T_s < t < T_s \end{cases} \tag{3.78}$$

Applying small ripple approximation to (3.78) and using inductor volt-second balance, one can obtain

$$\langle v_L(t)\rangle_{T_s} = V_g - (1-2D)\cdot V_c - I_L r_l = 0. \tag{3.79}$$

Using (3.16) and (3.35) in (3.79), and assuming the ac load as a resistor R_o, the boost factor of RSCFSI, when SBC-PWM is applied, can be modified as:

$$\frac{V_c}{V_g} = \frac{1}{(1-2D) + M^2 \cdot \dfrac{1}{2(1-2D)} \cdot \dfrac{r_l}{R_o}} \tag{3.80}$$

Similarly, the inductor voltage v_L using EBC-PWM, expressed in (3.61), is modified as

$$v_L(t) = \begin{cases} V_g + V_c - I_L r_l; & \text{if } 0 < t < D\cdot T_s \\ V_g - I_L r_l; & \text{if } D\cdot T_s < t < \left(\dfrac{1+D}{2}\right)\cdot T_s \\ V_g - V_c - I_L r_l; & \text{if } \left(\dfrac{1+D}{2}\right)\cdot T_s < t < T_s \end{cases} \tag{3.81}$$

Applying small ripple approximation to (3.81) and using inductor volt-second balance, one can obtain

$$\langle v_L(t)\rangle_{T_s} = V_g + \left(D - \frac{1-D}{2}\right)\cdot V_c - I_L r_l = 0. \tag{3.82}$$

Using (3.66) and (3.35) in (3.82), and assuming the ac load as a resistor R_o, the boost factor of RSCFSI, when EBC-PWM is applied, can be modified as:

$$\frac{V_c}{V_g} = \frac{2}{(1-3D) + M^2 \cdot \dfrac{2}{(1-3D)} \cdot \dfrac{r_l}{R_o}} \tag{3.83}$$

Based on (3.75) and (3.56), the plots of change in boost factor and dc-ac gain vs. D are given in Fig. 3.11 and compared for both PWM strategies. Note that the ac load R_o = 40 Ω and r_l = 0.22 Ω. It can be observed that, the inverter can achieve significantly better boost factor as well as dc-ac gain for same D with the proposed EBC-PWM strategy. However, the

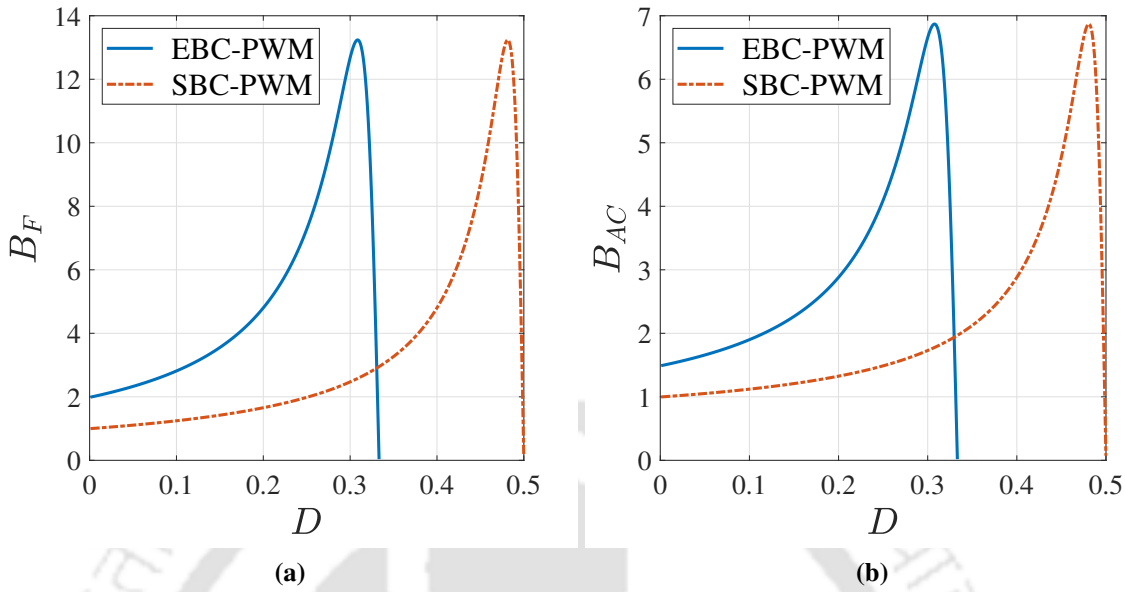


Fig. 3.11 Change in (a) boost factor, B_F, vs. shoot-through duty ratio, D, and (b) dc-ac voltage gain, B_{AC}, vs. D for EBC-PWM and SBC-PWM strategies.

maximum boost factor and the highest possible dc-ac gain remain unchanged in case of both PWM strategies.

3.6 COMPARISON OF RSCFSI WITH EXISTING AFE-ISIS

In this section, RSCFSI is compared with existing AFE-ISI topologies such as SBI and CFSI. The advantages and disadvantages of RSCFSI are discussed in the following.

A) Conversion Ratio

The boost factor ($B_F = V_c/V_g$) of the RSCFSI with SBC-PWM is the same as that of the CFSI, which is $1/(1-2D)$. Compared to RSCFSI, SBI offers a lower voltage conversion ratio, which is $(1-D)/(1-2D)$. In a practical scenario, considering maximum boost converter gain to be 5 and loss-less inversion, the overall RMS ac output voltage to input dc conversion ratio ($B_{\text{AC}} = \sqrt{2}V_o/V_g$) for the SBI topology is about 2 [23]. The experimentally obtained overall conversion ratio for RSCFSI is 4.23 (145 V RMS ac output voltage from a 50 V dc input voltage), which can be further improved with EBC-PWM.

Table 3.2 Comparison of RSCFSI with SBI and CFSI

	SBI	**CFSI**	**RSCFSI**
No. of active switches	5	5	4
No. of passive switches	6	6	6
No. of capacitors	2	2	3
No. of inductors	2	2	2
Input current	Discontinuous	Continuous	
Inverter input voltage	$\frac{1-D}{1-2D} \cdot V_g$	$\frac{1}{1-2D} \cdot V_g$	$\frac{1}{1-2D} \cdot V_g$
Boost factor (B_F)	$\frac{1-D}{1-2D}$	$\frac{1}{1-2D}$	
Modulation index (M)	$0 < M < (1-D)$		
Capacitor voltage	$V_c = \frac{1-D}{1-2D} \cdot V_g$	$V_c = \frac{1}{1-2D} \cdot V_g$	$V_c = \frac{1}{1-2D} \cdot V_g; \quad V_{cd} = DV_c$
Inductor current	$I_L = \frac{MI_o \cos\varphi}{\sqrt{2}(1-2D)}$		
Voltage stress on switches $S_{1\text{-}4}$, $D_{1\text{-}4}$	$V_c = \frac{1-D}{1-2D} \cdot V_g$	$V_c = \frac{1}{1-2D} \cdot V_g$	
Voltage stress on switch S	$V_c - V_g$	V_c	NA
Voltage stress on diode D_a	$V_c - V_g$	V_c	V_c
Voltage stress on switch D_b	V_c	V_c	V_c
Current stress on switches $S_{1\text{-}4}$	I_L		
Current stress on diode D_a	I_L		$2DI_L$
Current stress on diode D_b	$\frac{DI_L}{1-D}$		$2DI_L$
Total Device Rating	$P_o B_{F\text{-SBI}} \cdot \frac{4-D}{(1-D)^2}$	$P_o B_{F\text{-CFSI}} \cdot \frac{6-5D}{1-D}$	$4P_o B_{F\text{-RSCFSI}} \cdot (1+D)$

B) Component Count

The complete break-up of various components for SBI, CFSI and RSCFSI is illustrated in Table 3.2. The number of active switches required in SBI and CFSI is 5, which includes 4 IGBTs with anti-parallel diodes and one IGBT without anti-parallel diode. RSCFSI requires 4 active switches as it reduces the IGBT without anti-parallel diode. Considering the power diodes of the active-front-end network and the anti-parallel diodes of the active switches, the number of passive switches required in SBI and CFSI is 6, which remains same for RSCFSI. The number of capacitors used by the SBI and CFSI is 2, of which, one is used in

Table 3.3 Quantitative comparison of parameters, voltage stress and current stress

	SBI	**CFSI**	**RSCFSI**
Boost factor (B_F)	5.708	5.263	
Shoot-through duty ratio (D)	0.452	0.405	
Modulation index (M)	0.548	0.595	
Output voltage (v_o)	110 V RMS for V_g = 50 V		
Output current (i_o)	2.2 A RMS taking load resistance as 50 Ω		
Capacitor voltages	V_c = 285.4 V	V_c = 263.15 V	V_c = 263.15 V; V_{cd} = 106.575 V
Inductor current (I_L)	8.8 A	4.87 A	
Voltage stress on switches $S_{1\text{-}4}$, $D_{1\text{-}4}$	285.4 V	263.15 V	
Voltage stress on switch S	235.4 V	263.15 V	NA
Voltage stress on diode D_a	235.4 V	263.15 V	
Voltage stress on switch D_b	285.4 V	263.15 V	
Current stress on switches $S_{1\text{-}4}$	8.8 A	4.87 A	
Current stress on diode D_a	8.8 A	4.87 A	3.945 A
Current stress on diode D_b	7.258 A	3.31 A	3.945 A
Total Device Rating	16.32 kVA	8.509 kVA	7.157 kVA

the active-front-end network and another one is used as the filter capacitor. In addition to those two capacitors, RSCFSI needs one more as the offset capacitor. All of SBI, CFSI and RSCFSI use two inductors, of which one is required in the active-front-end network, and the other one serves as the output filter inductor. Although the total component count remains the same for SBI, CFSI and RSCFSI, due to the elimination of one switch, the RSCFSI is expected to achieve better efficiency than other two topologies.

C) Input Current

The discontinuous nature of the input current of SBI from the supply is attributed to the diode present in series with the DC source. In certain renewable energy applications, such as solar photovoltaic and fuel cell systems, the incorporation of an input filter stage is imperative. This is due to the fact that discontinuous input current has the potential to cause a reduction in the lifespan of the renewable sources. Conversely, the continuous input current drawn by CFSI and RSCFSI is associated with the existence of an inductor between the input source and the active-front-end network. Therefore, the necessity for an additional input filter stage is significantly reduced.

D) Voltage Stress of Switching Devices

A comparison of voltage stresses of the switches is presented in Table 3.2. From the table, it can be seen that all of the switches of all three topologies have to withstand a voltage equal to the dc-link voltage, except for the diode D_a and switch S of SBI, which have to withstand voltage stress of $(V_c - V_g)$. Note that the low-frequency is not considered for voltage stress calculation. As the boost factor of SBI is lower than that of both CFSI and RSCFSI, to achieve the same dc-ac gain B_{AC}, SBI needs to be operated with a much higher shoot-through duty ratio D. This results in higher dc-link voltage V_c, which indicates higher voltage stress across . A quantitative comparison is presented in Table 3.3. To obtain a 110 V RMS as ac output voltage for a 50 V as dc input voltage, the dc-link voltage V_c of SBI needs to be 285.4 V. At the same scenario, V_c of both CFSI and RSCFSI need to be 263.15 V. As the boost factor is less, SBI requires a higher D of 0.452 compared to 0.405 of CFSI and RSCFSI. As the modulation index M is also limited by D, SBI has a reduced M of 0.548. At the same time, CFSI and RSCFSI have a higher M of 0.595. Because of the combined impact of the low boost factor and the limitation of modulation index by the shoot-through duty ratio increases the required V_c for SBI, which increases the voltage stress level in some of the switches.

E) Current Stress of Switching Devices

A comparison of the current stresses of the switches is illustrated in Table 3.2. From the table, it can be seen that most of the switches of all topologies have to withstand a current equal to the inductor current I_L. Note that the low-frequency is not considered for the current stress calculation. In SBI and CFSI, the diode D_b has to withstand a current stress of $(I_L - I_i) = DI_L/(1-D)$. In RSCFSI, both diodes have a current stress of $(I_L - I_i) = 2DI_L$.

The input current i_{in} of SBI is not same as i_L, and the expression of i_{in} of SBI is

$$i_{\text{in}}(t) = \begin{cases} 0; & \text{if } 0 < t < D \cdot T_s \\ I_L; & \text{if } D \cdot T_s < t < T_s \end{cases} \tag{3.84}$$

which means the relation between I_{in},the average value of i_{in}, and I_L is

$$I_L = \frac{1}{1-D} \cdot I_{\text{in}} \tag{3.85}$$

At the same time, for CFSI and RSCFSI, $I_{\text{in}} = I_L$. Therefore, for same input current as CFSI and RSCFSI, the inductor current of SBI becomes significantly higher. Furthermore, the boost factor of SBI is lower than that of both CFSI and RSCFSI, and, to achieve same dc-ac gain B_{AC}, SBI needs to be operated with much higher shoot-through duty ratio. The combination of both these factors results in higher inductor current I_L, which indicates higher current stress through the switches S_1, S_2, S_3, S_4 and D_a. A quantitative comparison is presented in Table 3.3. To obtain a 110 V RMS as ac output voltage for a 50 V as dc input voltage and a load resistor of 50 Ω, the input current of all three topologies needs to be 4.87 A, which means I_L of both CFSI and RSCFSI ought to be 4.87 A. As the boost factor is less, SBI requires a shoot-through duty ratio of 0.452 compared to 0.405 of CFSI and RSCFSI. Therefore, I_L of SBI becomes 8.8 A, according to (3.85). Since I_L is higher, the current stress of D_b also increases to 7.258 A. At the same time, for CFSI and RSCFSI, the current stress of D_b are 3.31 A and 3.945 A, respectively.

F) Total device rating

The Total Device Rating (TDR) is a mathematical expression that represents the summation of the individual device ratings of all switching devices [25]. This rating is obtained by multiplying the peak voltage across the device with the peak current through the device. The TDR expressions for three topologies are given in Table 3.2. Note that the low-frequency is not considered for TDR calculation. A quantitative comparison is also presented in Table 3.3, where the dc input voltage is 50 V, the ac output voltage is 110 V RMS, a resistor of 50 Ω is considered as the load. From this comparison, it is clear that among three topologies, the RSCFSI has the least TDR of 7.157 kVA and the SBI has the highest TDR of 16.32 kVA. Note that the CFSI has a TDR of 8.509 kVA, which is slightly more than that of RSCFSI

Table 3.4 Parameters of the components of SBI, CFSI and RSCFSI for power loss calculation

	SBI/CFSI	RSCFSI
Switch	IRG7PH42UDPBF, 1200V, 45A, r_s = 62.5mΩ	
Diode	DSEI60-06A, 600V, 60A, r_D = 16.7mΩ	
Capacitor	400μF 160mΩ	C: 1160μF; r_c = 56mΩ C_d: 470μF; r_{cd} = 130mΩ
DC-side Inductor	2.75mH, 0.15Ω	
Filter Inductor	4mH, 0.2Ω	
Inductor Core	E 100/60/28, N97, 6800nH/N^2	

owing to the additional switch S. The TDR of SBI is significantly higher than other two topologies owing to much higher voltage stress and current stress as explained previously.

G) Efficiency and power loss

In order to compare operational efficiencies, the power loss of SBI, CFSI and RSCFSI are calculated using same switches, power diodes and inductor core as shown in Table 3.4. Note that the voltage rating of all capacitors is 400 V and the current rating of all inductors is 10 A. The operating conditions are same as the parameters mentioned in Table 3.3. Using the parameters mentioned in Table 3.4, an efficiency comparison for all three inverters is presented in Fig. 3.12(a), in which the output power P_o is varied between 50 W and 350 W. In Fig. 3.12(b), a power loss comparison for all three inverters are illustrated for a P_o = 350 W. The method for power loss and efficiency calculation used in [49] is followed in this chapter. Note that output filter losses are included in the power loss and efficiency calculation. Also, any low- or high-frequency ripple are not considered for the dc-side parameters, and only average values are used in this comparative analysis.

In Fig. 3.12(a), it is observed that RSCFSI has better efficiency than both SBI and CFSI. Since SBI has a lower boost factor, to achieve a similar dc-to-ac voltage gain, SBI is operated at a much higher shoot-through duty ratio. Hence, it is demonstrated to have the lowest efficiency among the three inverters. Compared to CFSI, RSCFSI has about 1%-2% better efficiency. A breakdown of the losses brings out the main reason behind the better efficiency of RSCFSI. Owing to one less switch, RSCFSI has lower switching loss among all three inverters. In both SBI and CFSI, the inductor current I_L flows through the dc-link capacitor

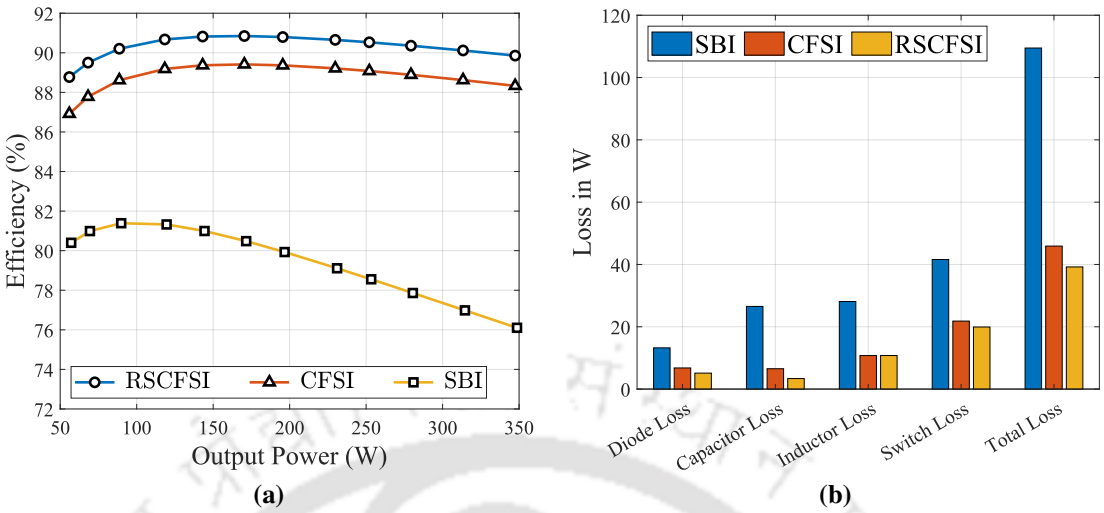


Fig. 3.12 Comparison between RSCFSI, CFSI and SBI in terms of (a) calculated efficiency and (b) calculated power loss at output power = 350 W.

during the shoot-through state. Consequently, the dc-link capacitor only takes a current of $(I_L - i_o)$ in RSCFSI during shoot-through. Also, for the same voltage ripple at the dc-link, RSCFSI uses a larger capacitor compared to SBI and CFSI. A larger capacitor has lower equivalent series resistance. Because of these two factors, the dc-link capacitor loss of RSCFSI is also the lowest among the three inverters. However, RSCFSI has an additional capacitor C_d, which adds more capacitor loss. Although at P_o = 350 W, overall capacitor loss is lowest for RSCFSI, at higher output power, a higher output current will flow through C_d, and the capacitor loss will be higher, resulting in an overall higher loss for the RSCFSI. The diode loss is more for CFSI because conducting current through one of the diodes is I_L and through the other diode is $(I_L - i_o)$, whereas conducting currents through both diodes of the RSCFSI are $(I_L - i_o)$. Thus, the RSCFSI also has the lowest diode loss among the three inverters.

H) Control to output response

The control to output transfer function of CFSI [25] is

$$\frac{\tilde{v}_c(s)}{\tilde{d}(s)} = \frac{-b_1 s - b_0}{a_2 s^2 + a_1 s + a_0} \tag{3.86}$$

where

$$a_0 = R_{dc}R_i(1-2D)^2; \quad a_1 = L\{R_i + (1-D)R_{dc}\}; \quad a_2 = LCR_{dc}R_i;$$
$$b_0 = 2R_{dc}R_iV_c(2D-1); \quad b_1 = LR_{dc}R_i\left(2I_L - \frac{V_c}{R_i}\right) \tag{3.87}$$

Note that the control to output transfer function of SBI [23] is also given by (3.86) and (3.87). The expression for the control to output transfer function of RSCFSI remains same as (3.86) while the expressions of the coefficients are given as follows:

$$a_0 = R_{dc}R_i(1-2D)^2; \quad a_1 = L(R_i + R_{dc}); \quad a_2 = LCR_{dc}R_i;$$
$$b_0 = 2R_{dc}R_iV_c(2D-1); \quad b_1 = 2LR_{dc}R_iI_L \tag{3.88}$$

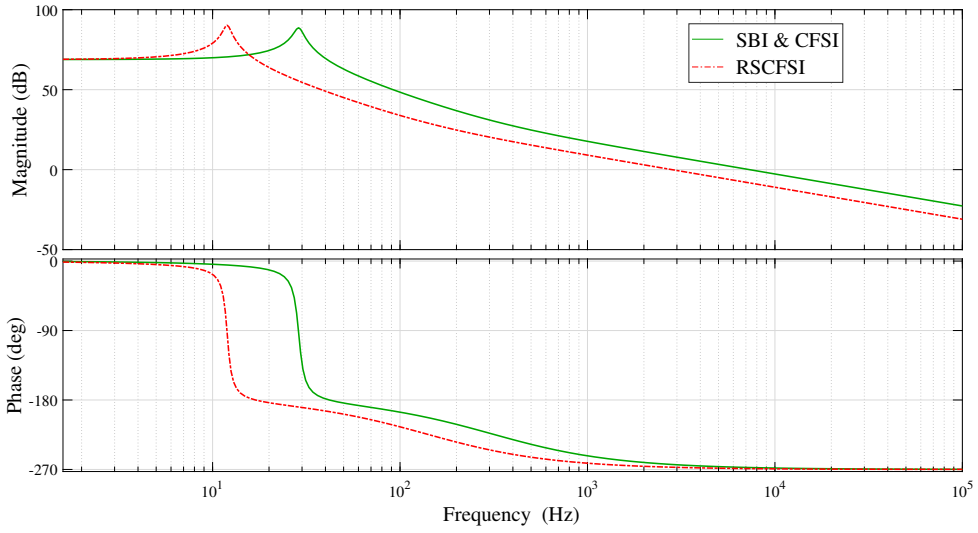


Fig. 3.13 The control to output response of SBI, CFSI and RSCFSI

The control to output response of SBI, CFSI and RSCFSI is given in Fig. 3.13. Since the expressions of the transfer functions are very similar, it is expected that three inverters will have quite similar control to output response. However, the additional fundamental component in the low-frequency ripple requires larger passive elements to be used for RSCFSI considering same amount of ripple. Thus, RSCFSI seems to be having a smaller bandwidth compared to both SBI and CFSI.

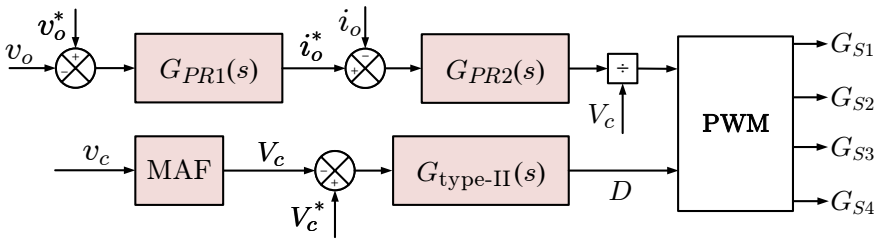


Fig. 3.14 Closed-loop control strategy.

3.7 CLOSED-LOOP CONTROL OF RSCFSI

The objective of the control strategy in standalone mode is to track a reference output voltage and control the dc-link voltage. Therefore, the output voltage controller must track the reference output voltage (v_o^*), which generates the reference output current (i_o^*) for the current controller. A separate voltage controller is used to track the desired dc-link voltage given as a reference, which also prevents over-charging of the dc-link capacitor. The complete closed-loop control strategy is presented in Fig. 3.14.

3.7.1 Tracking the reference output voltage

The output voltage (v_o) is compared to its reference v_o^*, and the error is passed through a proportional-resonant (PR) controller as shown in Fig. 3.14. The PR controller has been chosen due to its accurate tracking. The overall transfer function of the controller, which should track the fundamental component, is chosen as

$$G_{PR1}(s) = K_{p1} + K_{r1}\frac{2\xi\omega_o s}{s^2 + 2\xi\omega_o s + \omega_o^2} \tag{3.89}$$

The damping factor ξ can be taken between 0.01 and 0.02 [100]. The transfer function from v_o to i_o is given by

$$G_{vi}(s) = \frac{v_o(s)}{i_o(s)} = \frac{R_o}{sR_oC_f + 1} \tag{3.90}$$

where the ac load is R_o, and a filter capacitor C_f is connected across R_o.

With K_{p1} = 0.05 and K_{r1} = 1.0, the compensated bode diagram is shown in Fig. 3.15. In order to maintain steady-state error close to zero, the PR controllers must have high gain at

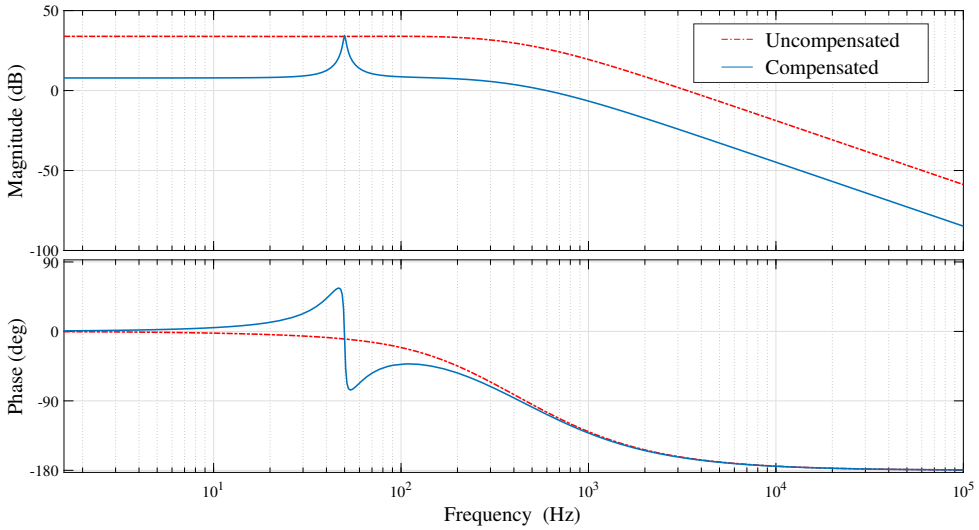


Fig. 3.15 Bode diagram of output voltage control loop.

the desired (in this case, fundamental) frequency of 50 Hz, and the gain crossover frequency (f_c) has to be more than half a decade separated from the switching frequency f_s so that enough attenuation can be achieved at f_s. It is found the phase margin is 72.5°, and f_c is 600 Hz, which is more than a decade separated from f_s of 10 kHz. A gain of 33 dB is achieved at 50 Hz, and an attenuation of 45 dB is observed at f_s.

3.7.2 Tracking the reference output current

The output current i_o has a monotonic relationship with the switching states. So, when switches S_1 and S_2 are on, one can write

$$v_{Lf}(t) = L_f \frac{di_o(t)}{dt} = v_c(t) - v_{cd}(t) - v_o(t) = v_c(t) - v_{cd}(t) - i_o(t)R_o \tag{3.91}$$

which indicates

$$\frac{di_o(t)}{dt} > 0 \tag{3.92}$$

Similarly, when switches S_3 and S_4 are on, one can obtain

$$v_{Lf}(t) = L_f \frac{di_o(t)}{dt} = -v_c(t) - v_{cd}(t) - v_o(t) = -v_c(t) - v_{cd}(t) - i_o(t)R_o \tag{3.93}$$

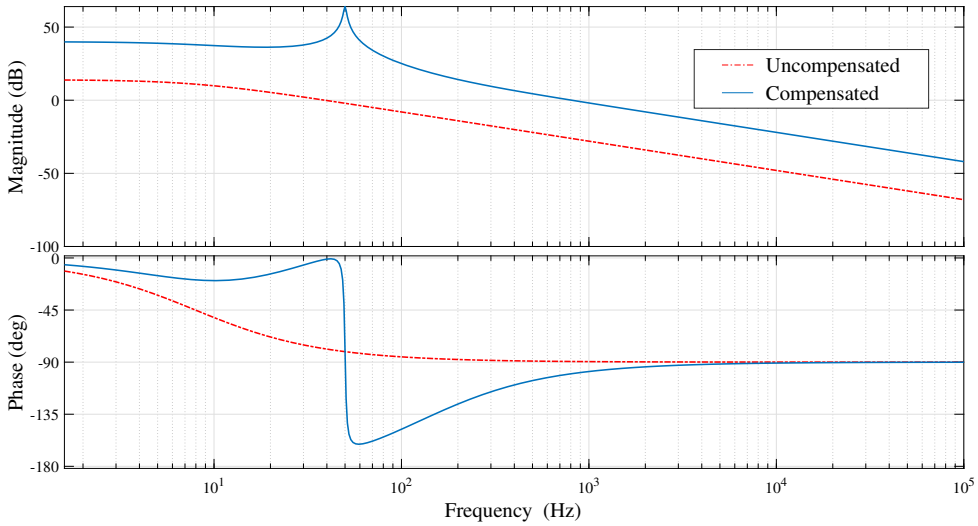


Fig. 3.16 Bode diagram of output current control loop.

which indicates

$$\frac{di_o(t)}{dt} < 0 \tag{3.94}$$

Thus, in order to control i_o, the switches require regulation through the control variable v_{Lf}. Therefore, the current through the filter inductor L_f is compared to the reference generated by the voltage controller, and the error is passed through a PR controller as shown in Fig. 3.14. The transfer function from i_o to v_{Lf} is obtained as:

$$G_{io}(s) = \frac{i_o(s)}{v_{Lf}(s)} = \frac{1}{sL_f + R_{Lf}}. \tag{3.95}$$

considering R_{Lf}, the parasitic resistance of L_f. The current controller, which should also contain ω_o as the resonant frequency, is selected as:

$$G_{PR2}(s) = K_{p2} + K_{r2}\frac{2\xi\omega_o s}{s^2 + 2\xi\omega_o s + \omega_o^2}. \tag{3.96}$$

With K_{p2} = 20 and K_{r2} = 2000, the compensated bode diagram is shown in Fig. 3.16. The phase margin is 80^o, and crossover frequency is 815 Hz, which is more than a decade

separated from the switching frequency of 10 kHz. A gain of 64 dB is observed at the fundamental frequency, and an attenuation of 22 dB is achieved at the switching frequency.

3.7.3 Control of dc-link capacitor voltage

In order to design the controller for the regulation of the dc-link capacitor voltage, the control to output transfer function is required. Applying ac modeling approach, as explained in [3], to (3.9) and (3.10) one can write,

$$\begin{aligned} L\frac{d}{dt}\langle i_L(t)\rangle_{T_s} &= V_g - \{1-2d(t)\}\cdot\langle v_c(t)\rangle_{T_s} - \langle i_L(t)\rangle_{T_s} r_l \\ C\frac{d}{dt}\langle v_c(t)\rangle_{T_s} &= \{1-2d(t)\}\cdot\langle i_L(t)\rangle_{T_s} - \{1-d(t)\}\cdot\langle i_i(t)\rangle_{T_s} \end{aligned} \tag{3.97}$$

where r_l is the parasitic resistance of the input inductor L. Here, $\langle v_c(t)\rangle_{T_s}$, $\langle i_L(t)\rangle_{T_s}$, and $\langle i_i(t)\rangle_{T_s}$ are the average values of v_c, i_L and i_i, respectively, over one switching period. Note that V_c, I_L and I_i is obtained in Section 3.3 considering small ripple approximation. The above-mentioned equations are perturbed and linearized to construct the small-signal model of the converter. In this model, the input voltage V_g is considered to be stiff, and it does not have any perturbation. As explained in Section 3.6, the voltage stress of the switching devices are equal to either V_c or $(V_c - V_g)$, and the current stress of the switching devices are either equal to I_L or $(I_L - I_i)$. Also, the relationship between V_g and V_c as well as the relationship between I_L and I_i depend on D. Therefore, the chosen quiescent point (Q-point) or the operating point of a device, should be V_c, I_L, I_i and D. Therefore, $\tilde{i}_L(t)$, $\tilde{i}_i(t)$, $\tilde{v}_c(t)$, and $\tilde{d}(t)$ are the small ac variations with respect to the chosen Q-points, i.e., the average values I_L, I_i, V_c, and D, respectively, and are expressed as follows:

$$\begin{aligned} \langle v_c(t)\rangle_{T_s} &= V_c + \tilde{v}_c(t); \\ \langle i_L(t)\rangle_{T_s} &= I_L + \tilde{i}_L(t); \\ \langle i_i(t)\rangle_{T_s} &= I_i + \tilde{i}_i(t); \\ d(t) &= D + \tilde{d}(t). \end{aligned} \tag{3.98}$$

Using (3.98) in (3.97), one can obtain

$$\begin{aligned} L\frac{d}{dt}\left\{I_L+\tilde{i}_L(t)\right\} &= V_g-\left[1-2\left\{D+\tilde{d}(t)\right\}\right]\cdot\left\{V_c+\tilde{v}_c(t)\right\}-\left\{I_L+\tilde{i}_L(t)\right\}r_l \\ C\frac{d}{dt}\left\{V_c+\tilde{v}_c(t)\right\} &= \left[1-2\left\{D+\tilde{d}(t)\right\}\right]\cdot\left\{I_L+\tilde{i}_L(t)\right\}-\left[1-\left\{D+\tilde{d}(t)\right\}\right]\cdot\left\{I_i+\tilde{i}_i(t)\right\} \end{aligned} \tag{3.99}$$

The dc terms contain dc quantities only. The first-order ac terms contain a single ac quantity, usually multiplied by a constant coefficient such as a dc term. These terms are linear functions of the ac variations. The second-order ac terms contain the products of ac quantities. Hence, they are relatively small and can be ignored. Thus, the small-signal dynamic equations of the RSCFSI can be written as follows:

$$\begin{aligned} L\frac{d}{dt}\tilde{i}_L(t) &= -(1-2D)\cdot\tilde{v}_c(t)-r_l\cdot\tilde{i}_L(t)+2V_c\cdot\tilde{d}(t) \\ C\frac{d}{dt}\tilde{v}_c(t) &= (1-2D)\cdot\tilde{i}_L(t)+(I_i-2I_L)\cdot\tilde{d}(t)+(1-D)\cdot\tilde{i}_i(t) \end{aligned} \tag{3.100}$$

By transforming (3.100) into s-domain, the control to output transfer function can be derived as follows

$$G_{\text{vd}}(s)=\left.\frac{\tilde{v}_c(s)}{\tilde{d}(s)}\right|_{\tilde{i}_i(s)=0}=\frac{2V_c(1-2D)+(sL+r_l)(I_i-2I_L)}{s^2LC+sr_lC+(1-2D)^2} \tag{3.101}$$

which indicates that the transfer function G_{vd} of RSCFSI is a nonminimum phase transfer function with a real zero in the right half of the s-plane, which is also observed in SBI and CFSI [23, 25].

The regulation of the dc-link capacitor voltage v_c is achieved with a voltage controller added in the form of a type-II compensator. As shown in Fig. 3.14, the measured v_c is passed through a moving average filter (MAF) so that the dc component V_c can be extracted. Then V_c is compared with the reference value V_c^* and the error is given to the type-II compensator as follows:

$$G_{\text{type-II}}(s)=G_{\text{MB}}\cdot\frac{\left(1+\dfrac{s}{\omega_z}\right)}{s\left(1+\dfrac{s}{\omega_p}\right)} \tag{3.102}$$

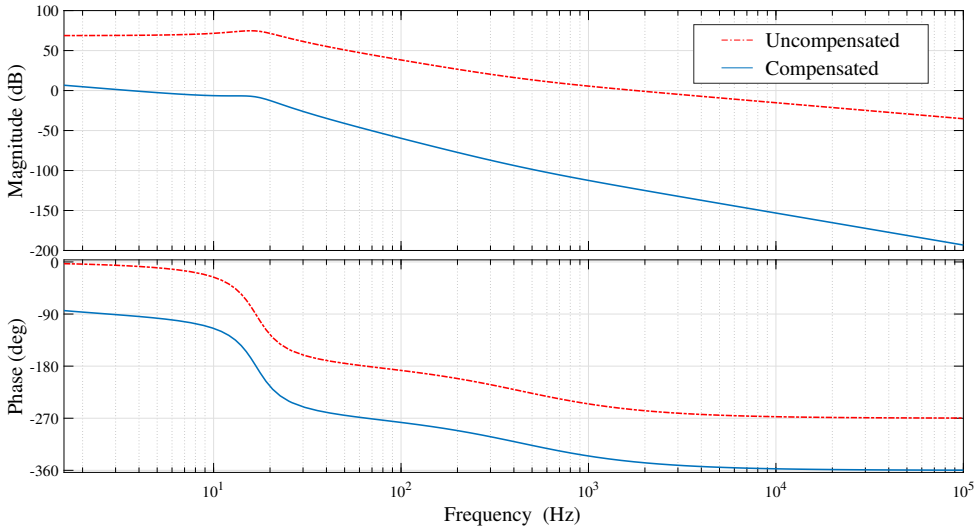


Fig. 3.17 Bode diagram of dc-link voltage controller.

where G_{MB}, ω_p and ω_z are the gain, pole and zero of the compensator, respectively.

Thus, the voltage loop gain can be written as

$$T_v(s) = G_{\text{type-II}}(s) \cdot G_{\text{vd}}(s) \tag{3.103}$$

The crossover frequency needs to be less than 5 Hz, because of the significant low-frequency ripples at 50 Hz and 100 Hz, which will be discussed in Chapter 4 in detail. Therefore, the crossover frequency should be more than a decade separated than both 50 and 100 Hz so that sufficient attenuation is available for both 50 and 100 Hz. To achieve this, G_{MB} = 0.005; ω_p = 0.02 rad/s; and ω_z = 1.59 rad/s, so that the crossover frequency becomes 3.57 Hz. The phase margin is 87^{o}, and the gain margin is 8 dB. The attenuation at 50 Hz is 40 dB, and the attenuation at 100 Hz is 60 dB, indicating the voltage controller remains unaffected by the low-frequency ripples.

3.8 VERIFICATION OF RSCFSI

The hardware prototype of single-phase RSCFSI has been built to perform experimental verification of the theoretical analysis presented in this chapter. Fig. 3.18 shows the

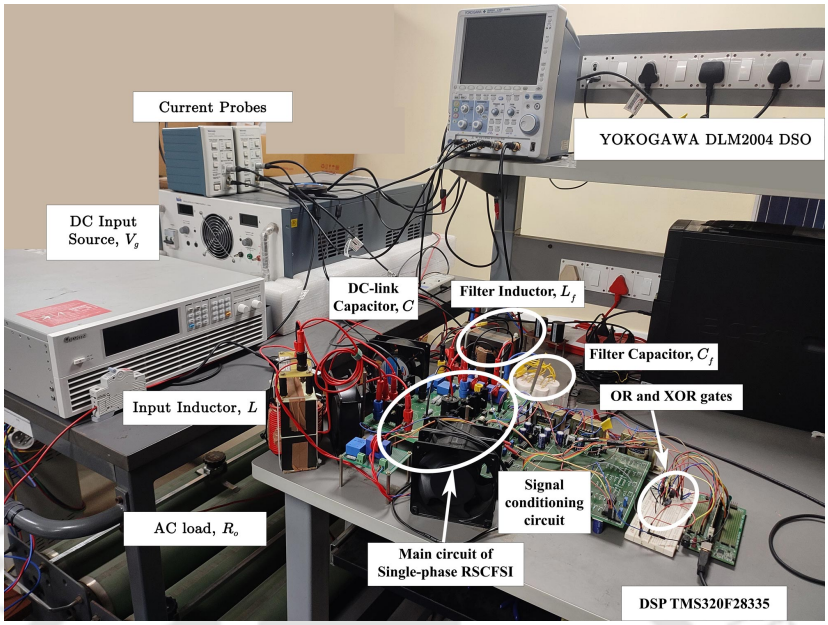


Fig. 3.18 Experimental setup of single-phase RSCFSI.

Table 3.5 Components used in hardware setup

Component	Part No. and Manufacturer
S_1, S_2, S_3, S_4	IRG7PH42UDPBF (International Rectifier)
D_a, D_b	DSEI60-06A (IXYS)
Gate Driver	FOD3180 (Fairchild)
Inductor Core	E 100/60/28 (EPCOS)
Voltage Transducer	LV 25-P (LEM)
Current Transducer	LA 55-P (LEM)

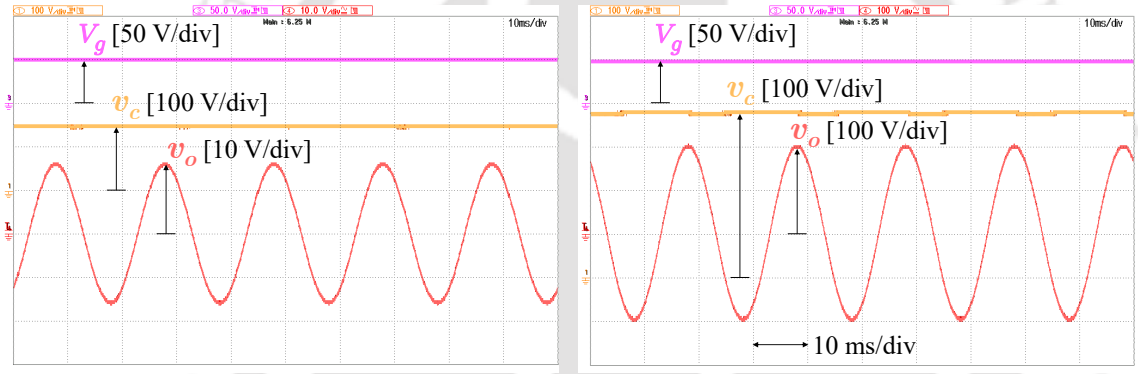
photograph of the hardware setup. The input dc voltage V_g is 50 V. The output voltage v_o is 110 V RMS. The system operation with an ac load of 50 Ω is verified. Table 3.6 lists the parameters and component values used to perform the experiments. A TMS320F28335 Digital Signal Processor (DSP) is used to implement the proposed PWM switching strategies and the closed-loop control technique. The components used in the hardware setup are listed in Table 3.5.

3.8.1 Verification of buck-boost capability of RSCFSI

One of the main advantages of RSCFSI over the conventional VSI is that it can generate an ac output voltage that is either higher or lower than the dc source voltage V_g. To verify this experimentally, the RSCFSI is tested for different conversion ratios, and the corresponding

Table 3.6 Parameters and component values for experiment

Parameter/Component	Attributes
Input Voltage (V_g)	50 V
Shoot-through duty ratio (D)	0.425
Peak value of output voltage (v_o)	110 V RMS
Fundamental Frequency (f_o)	50 Hz
Inverter Switching Frequency (f_s)	10 kHz
Input inductor (L)	2.75 mH
dc-link capacitor (C)	1160 µF
Bleeding Resistance (R_d)	10 kΩ
Filter Inductor (L_f)	4 mH
Offset capacitor (C_d)	470 µF
AC Load (R_o)	50 Ω
Output Filter capacitor (C_f)	10 µF



(a) **(b)**

Fig. 3.19 Experimental results of the RSCFSI with different conversion ratios: (a) buck mode and (b) boost mode.

experimental results are given in Fig. 3.19. The buck capability of RSCFSI is shown in Fig. 3.19(a). It can be observed that the dc input voltage V_g is 50.4 V, which is boosted to the dc-link voltage V_c = 148.8 V. The output voltage v_o is observed to be 11.6 V RMS. Therefore, the ac-to-dc voltage gain B_{AC} is 0.33. In Fig. 3.19(b), the boost capability of the RSCFSI is explored. Note that for a V_g of 48.2 V, V_c is stepped up to 375.7 V, whereas v_o is 144.25 V RMS. Therefore, the ac-to-dc voltage gain B_{AC} is 4.23. From these results, it is clear that the ac-to-dc conversion ratio can vary between 0.33 and 4.23. This verifies the buck-boost capability of the RSCFSI.

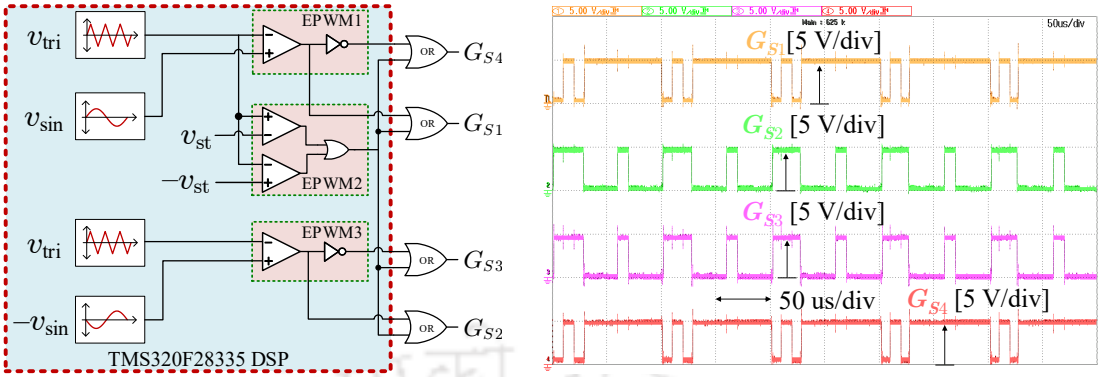


Fig. 3.20 (a) Implementation of SBC-PWM using DSP and OR gates and (b) gate pulses generated by SBC-PWM. $\pm v_{sin}$: sinusoidal modulation signals, $\pm v_{tri}$: triangular carrier signals, $\pm v_{st}$: shoot-through constant voltages, $G_{S1\text{-}4}$: gate pulses of $S_{1\text{-}4}$.

3.8.2 Verification of RSCFSI with SBC-PWM

A) Generation of gate pulses using SBC-PWM

As shown in Fig. 3.20(a), the gate pulses are generated through the DSP and four OR logic gates. A total of four EPWM modules are utilized in DSP [103]. A 74HC32 quad 2-Input OR gate IC is used to realize four OR logic gates, which are employed at the DSP output. The gate signals of S_1 and S_2 are generated in the EPWM1 module. The shoot-through signals for S_1 and S_2 are generated in EPWM2 module. Using a pair of OR gates, the shoot-through signals are inserted into the final gate signals of S_1 and S_2. Similarly, the gate signals for S_3 and S_4 are generated in EPWM3, and the shoot-through signals generated in EPWM2 is added to those signals using another pair of OR gates obtaining the final gate signals of S_3 and S_4. Note that the modulation signals v_{sin} and $-v_{sin}$ are generated in the DSP in open loop. In closed loop, the modulation signals are obtained from the output of the current controller as illustrated in Fig. 3.14.

The gates pulses for the switches $S_{1\text{-}4}$ are shown in Fig. 3.20(b), which are generated using the aforementioned process. It can also be noted that these gate pulses are consistent with the pulses illustrated in Fig. 3.7(b).

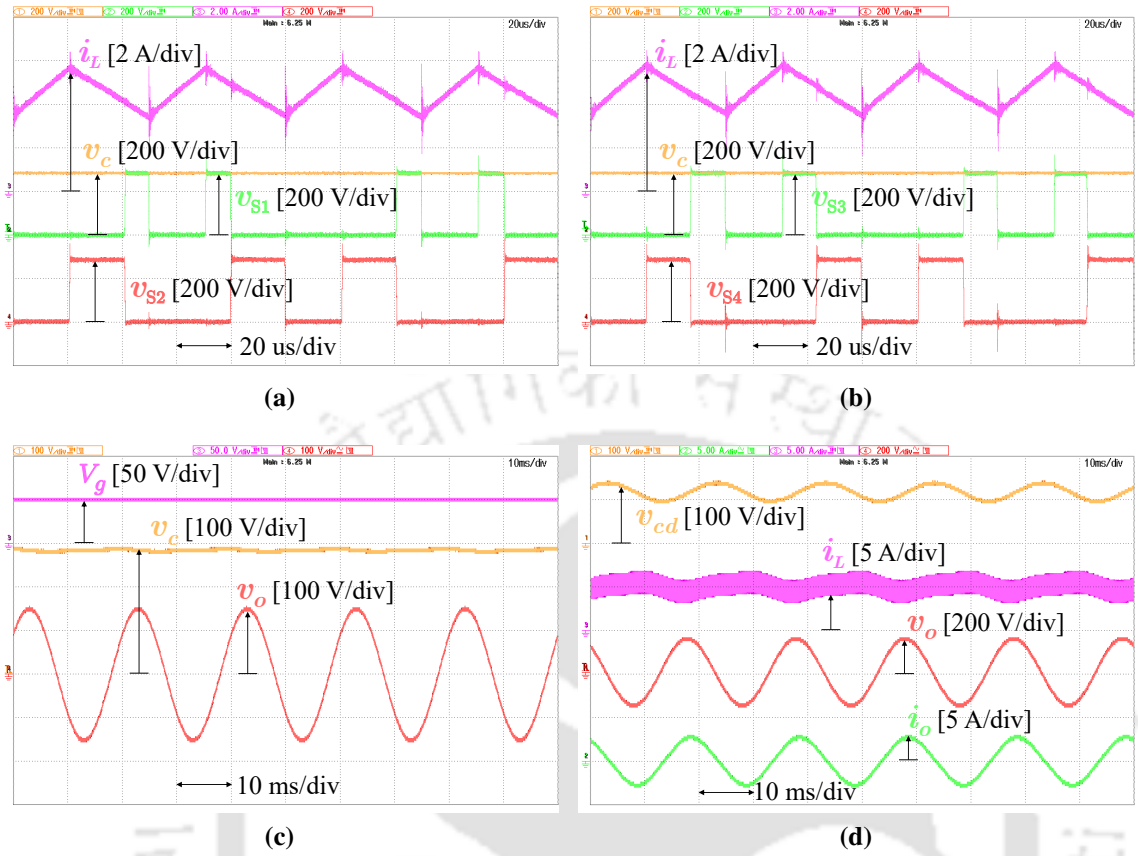


Fig. 3.21 (a)-(b) switch node voltage waveforms and (c)-(d) steady-state performance of the RSCFSI with SBC-PWM. i_L: input inductor current, v_c: dc-link capacitor voltage, $v_{S1\text{-}4}$: voltages across $S_{1\text{-}4}$, V_g: input voltage, v_o: output voltage, i_o: output current, v_{cd}: offset capacitor voltage.

B) Steady-state performance of RSCFSI using SBC-PWM

Fig. 3.21 shows the experimental results of RSCFSI using the SBC-PWM strategy. The dc-link capacitor voltage v_c, the inductor current i_L, and the switch node voltages are shown in Fig. 3.21(a) and (b), where v_{s1}, v_{s2}, v_{s3} and v_{s4} are the voltage across the switches S_1, S_2, S_3 and S_4, respectively. When the switches are turned on, the voltage across it becomes zero, and when the switch is turned off, the voltage across it becomes equal to the dc-link capacitor voltage v_c as shown in Fig. 3.21(a) and (b). In the shoot-through state, when all four switches are turned on together, the inductor is charged, which can be verified from the positive slope of i_L in Fig. 3.21(a) and (b). Similarly, in the nonshoot-through state, the inductor is discharged, which is supported by the negative slope of i_L.

Fig. 3.21(c) and (d) demonstrate the steady-state performance of the RSCFSI using the SBC-PWM strategy. Fig. 3.21(c) depicts the waveforms of the input voltage V_g, the dc-link voltage v_c and the output voltage v_o for 5 cycles. Note that a lower boost factor B_F and a lower dc-to-ac gain B_{AC} are chosen for further experimental results owing to several limitations of the experimental setup. In this way, the output current i_o can be taken higher. In Fig. 3.21(c), V_g is taken as 50 V, and the average value of v_c is measured to be 287 V, which indicates B_F = 5.74. The shoot-through duty ratio D is taken as 0.425, for which the theoretical value of B_F is calculated as 6.67, according to (3.14). So, it is concluded that there is a drop in B_F as per experimental results. This is observed due to non-idealities present in the hardware, such as the parasitic resistance of the input inductor L and the filter inductor L_f, the equivalent series resistance of the dc-link capacitor C and the filter capacitor C_f, the turn-on resistance of the switches and the diodes, etc. The peak-to-peak ripple of v_c is 8 V. The RMS value of v_o is 110 V.

Fig. 3.21(c) shows the waveforms of the input inductor current i_L, the offset capacitor voltage v_{cd}, the output voltage v_o and the output current i_o. The average value of i_L is 5 A, and its peak-to-peak ripple is 3.6 A. The average value of v_{cd} is measured to be 118 V, which is calculated as 121 V, according to (3.24). The peak-to-peak ripple of v_{cd} is 52 V as a 470 µF capacitor used as the offset capacitor C_d. Since the load resistor is 50 Ω, the RMS value of i_o is measured to be 2.2 A for a v_o of 110 V RMS, and it is in phase with v_o.

C) Transient performance of RSCFSI using SBC-PWM

In Fig. 3.22, the transient performance of RSCFSI with SBC-PWM is demonstrated, where the waveforms of dc-link capacitor voltage v_c, input inductor current i_L, output voltage v_o and output current i_o are presented. Fig. 3.22(a) depicts the transient performance for a 40% step-up change in load. Fig. 3.22(b) demonstrates the transient performance for a 40% step-down change in load. Note that v_o is maintained at 110 V RMS in both changes of step-up and step-down in load.

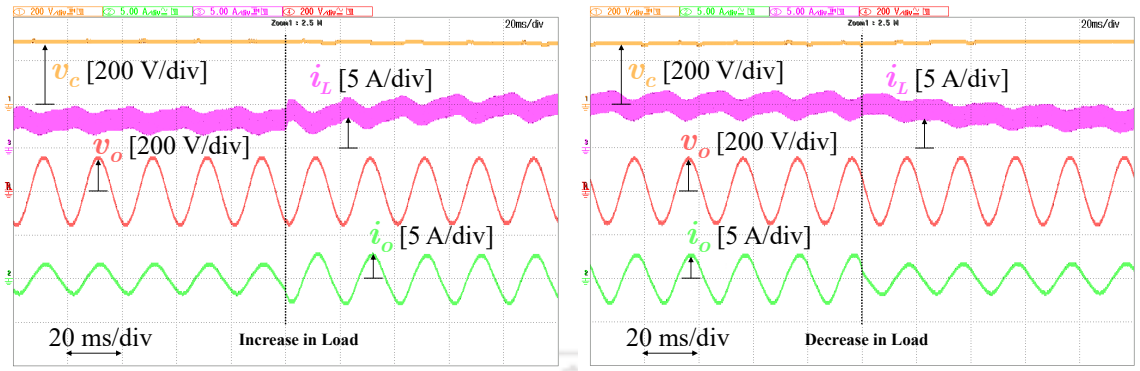


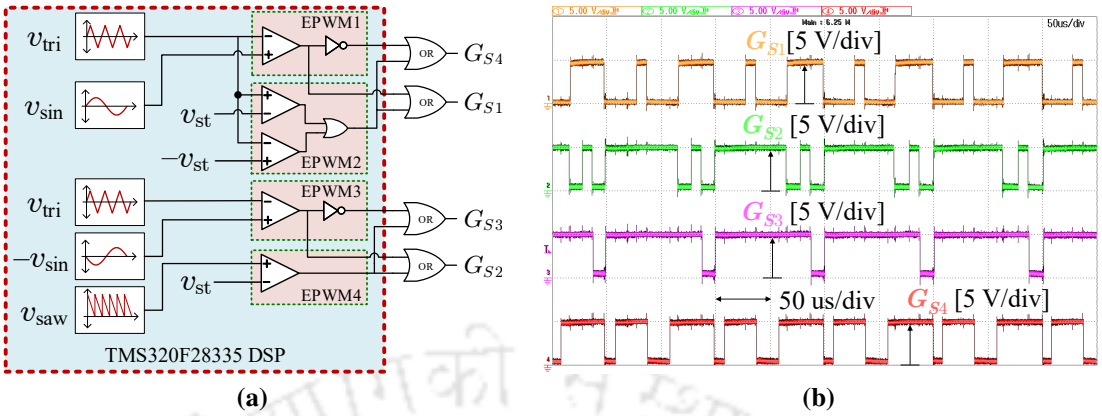
Fig. 3.22 Transient performance of RSCFSI with SBC-PWM: (a) for a 40% step-up change in load and (b) for a 40% step-down change in load. v_c: dc-link capacitor voltage, i_L: input inductor current, v_o: output voltage, i_o: output current.

As shown Fig. 3.22(a), i_o is decreased from 2.2 A RMS to 1.4 A RMS so that the average value of i_L is stepped down from 5 A to 3 A. The average value of v_c remains unchanged at 287 V, which indicates the dc-link voltage controller is working satisfactorily. However, a reduction in low-frequency ripple is observed for both v_c and i_L as the load is reduced. Similarly, in Fig. 3.22(b), i_o is increased from 1.4 A RMS to 2.2 A RMS so that the average value of i_L is stepped up from 3 A to 5 A. The average value of v_c remains unaltered at 287 V, which demonstrates that the dc-link voltage controller is functioning adequately. However, an increment in low-frequency ripple is observed for both v_c and i_L as the load is increased. Therefore, both transitions in load display acceptable transient responses. Note that although i_L is not controlled, its waveform is included in Fig. 3.22 to show changes on the input side when a change in load occurs.

3.8.3 Verification of RSCFSI with EBC-PWM

A) Generation of gate pulses using EBC-PWM

As shown in Fig. 3.23(a), the gate pulses are generated through the DSP and four OR logic gates. A total of four EPWM modules are utilized in DSP [102]. A 74HC32 quad 2-Input OR gate IC is used to realize four OR logic gates, which are employed at the DSP output. The gate signals of S_1 and S_2 are generated in the EPWM1 module. The shoot-through signals



(a) (b)

Fig. 3.23 (a) Implementation of EBC-PWM using DSP and OR gates and (b) gate pulses generated by EBC-PWM. $\pm v_{\text{sin}}$: sinusoidal modulation signals, $\pm v_{\text{tri}}$: triangular carrier signals, $\pm v_{\text{st}}$: shoot-through constant voltages, v_{saw}: sawtooth signal, $G_{S1\text{-}4}$: gate pulses of $S_{1\text{-}4}$.

for S_1 and S_2 are generated in EPWM2 module. Using a pair of OR gates, the shoot-through signals are inserted into the final gate signals of S_1 and S_2. Similarly, the gate signals and the shoot-through signals for S_3 and S_4 are generated in EPWM3 and EPWM4, respectively. Two more OR gates are employed to include the shoot-through signals into the final gate signals of S_3 and S_4. Similar to SBC-PWM strategy, the modulation signals v_{sin} and $-v_{\text{sin}}$ are generated in the DSP in open loop. In closed loop, the modulation signals are obtained from the output of the current controller as illustrated in Fig. 3.14.

The gates pulses for the switches $S_{1\text{-}4}$, generated using the aforementioned process, are shown in Fig. 3.23(b). It can also be noted that these gate pulses are consistent with the pulses illustrated in Fig. 3.10(b).

B) Steady-state performance of RSCFSI using EBC-PWM

Fig. 3.24 shows the steady-state experimental results of RSCFSI using the EBC-PWM strategy. The dc-link capacitor voltage v_c, the inductor current i_L, and the switch node voltages are shown in Fig. 3.24(a) and (b), where v_{s1}, v_{s2}, v_{s3} and v_{s4} are the voltage across the switches S_1, S_2, S_3 and S_4, respectively. When the switches are turned on, the voltage across it becomes zero, and when the switch is turned off, the voltage across it becomes equal to the dc-link capacitor voltage v_c as shown in Fig. 3.24(a) and (b). In the shoot-through

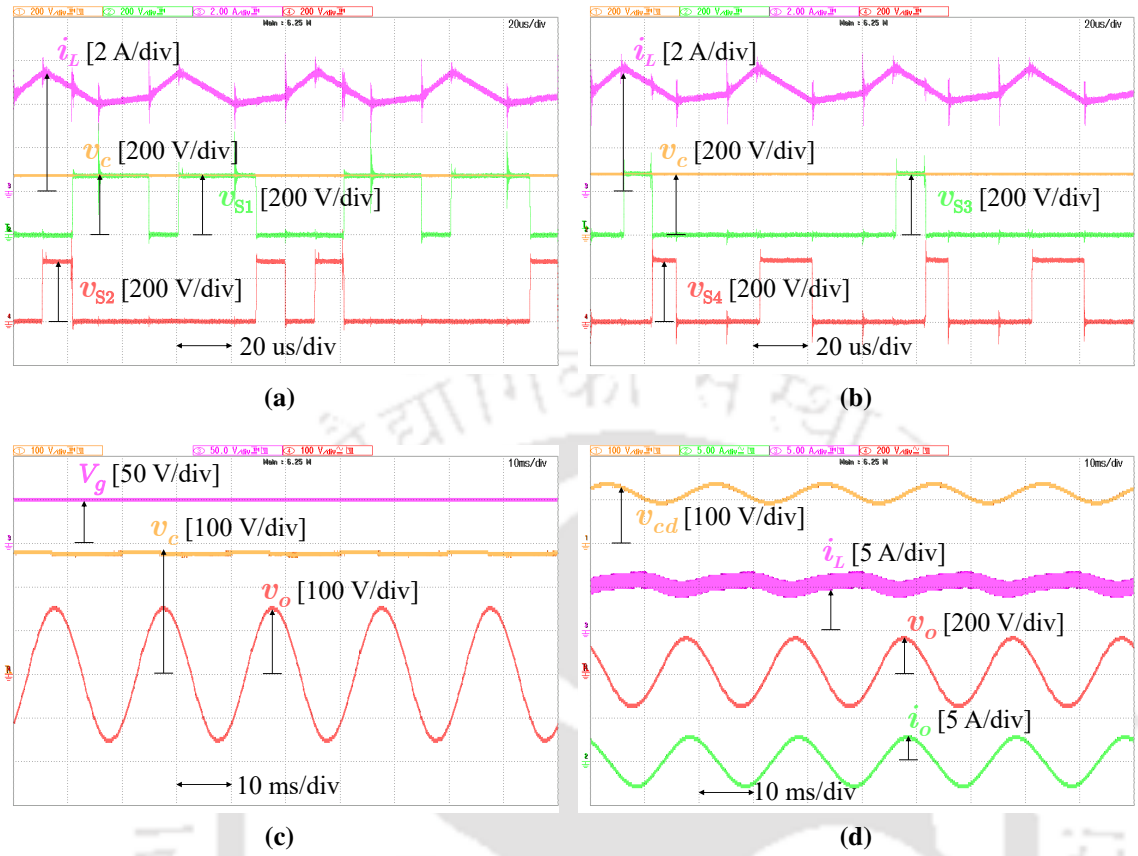


Fig. 3.24 (a)-(b) switch node voltage waveforms and (c)-(d) steady-state performance of the RSCFSI with EBC-PWM. i_L: input inductor current, v_c: dc-link capacitor voltage, $v_{S1\text{-}4}$: voltages across $S_{1\text{-}4}$, V_g: input voltage, v_o: output voltage, i_o: output current, v_{cd}: offset capacitor voltage.

state-1, when all four switches are turned on together, the inductor is charged with a steeper slope of $(V_g + V_c)/L$, which can be verified from the positive slope of i_L in Fig. 3.21(a) and (b). Similarly, it is noticed that In the shoot-through state 2, when three switches are turned on together, the inductor is charged with a slope of V_g/L, which can be verified from the less steep, positive slope of i_L. Similar to SBC-PWM, in the nonshoot-through state, the inductor is discharged as supported by the negative slope of i_L.

Fig. 3.24(c) and (d) demonstrate the steady-state performance of the RSCFSI using the EBC-PWM strategy. Fig. 3.24(c) depicts the waveforms of the input voltage V_g, the dc-link voltage v_c and the output voltage v_o for five cycles. Similar to SBC-PWM, in Fig. 3.24(c), V_g is taken as 50 V, and the average value of v_c is measured to be 278 V, which indicates B_F = 5.56. The shoot-through duty ratio D is taken as 0.225, for which the theoretical value of B_F is calculated as 6.15, according to (3.14). The reduction in the boost factor is observed due to

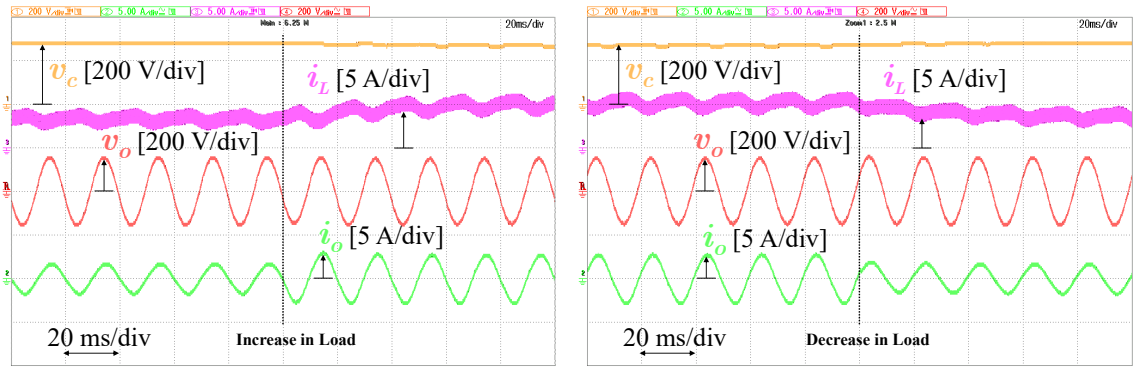


Fig. 3.25 Transient performance of RSCFSI with EBC-PWM: (a) for a 40% step-up change in load and (b) for a 40% step-down change in load. v_c: dc-link capacitor voltage, i_L: input inductor current, v_o: output voltage, i_o: output current.

non-idealities in the hardware setup. The peak-to-peak ripple of v_c is 8 V. The RMS value of v_o is 110 V.

Fig. 3.24(c) shows the waveforms of the input inductor current i_L, the offset capacitor voltage v_{cd}, the output voltage v_o and the output current i_o. The average value of i_L is 5 A, and its peak-to-peak ripple is 3 A, which is less than that of SBC-PWM. The average value of v_{cd} is measured to be 114 V, which is calculated as 116 V, according to (3.73). The peak-to-peak ripple of v_{cd} is 52 V as a 470 µF capacitor used as the offset capacitor C_d. Since the load resistor is 50 Ω, the RMS value of i_o is measured to be 2.2 A for a v_o of 110 V RMS, and it is in phase with v_o.

C) Transient performance of RSCFSI using EBC-PWM

In Fig. 3.25, the transient performance of RSCFSI with EBC-PWM is demonstrated, where the waveforms of dc-link capacitor voltage v_c, input inductor current i_L, output voltage v_o and output current i_o are presented. Fig. 3.25(a) depicts the transient performance for a 40% step-up change in load. Fig. 3.25(b) demonstrates the transient performance for a 40% step-down change in load. Note that v_o is maintained at 110 V RMS in both changes of step-up and step-down in load.

As shown Fig. 3.25(a), i_o is decreased from 2.2 A RMS to 1.4 A RMS so that the average value of i_L is stepped down from 5 A to 3 A. The average value of v_c remains unchanged at 278 V, which indicates the dc-link voltage controller is working satisfactorily. However, a reduction in low-frequency ripple is observed for both v_c and i_L as the load is reduced. Similarly, in Fig. 3.25(b), i_o is increased from 1.4 A RMS to 2.2 A RMS so that the average value of i_L is stepped up from 3 A to 5 A. The average value of v_c remains unaltered at 278 V, which demonstrates that the dc-link voltage controller is functioning adequately. However, an increment in low-frequency ripple is observed for both v_c and i_L as the load is increased. Therefore, both transitions in load display acceptable transient responses. Note that although i_L is not controlled, its waveform is included in Fig. 3.25 to show changes on the input side when a change in load occurs.

3.9 SUMMARY

In this chapter, the single-phase RSCFSI topology is derived from the complimentary current-fed dc/dc topology, and the steady-state analysis of the RSCFSI is presented. The implementation of the SBC-PWM strategy is illustrated, for which the RSCFSI can achieve same boost factor as the CFSI. To improve the proposed inverter's boost factor for the same shoot-through duty ratio, the EBC-PWM strategy is proposed. A comparison of the RSCFSI with SBI and CFSI is also performed in this chapter, which shows the RSCFSI requires lower total device rating (TDR) and achieves better efficiency among the three inverters. A closed-loop control strategy is also illustrated for the RSCFSI to control the output voltage and the dc-link voltage. The proposed inverter is fabricated in hardware, and the presented experimental results for steady-state operation and transient performance of the inverter due to ac load change are consistent with the analysis.

CHAPTER 4

LOW-FREQUENCY RIPPLE ANALYSIS AND MITIGATION IN RSCFSI

4.1 INTRODUCTION

In Chapter 3, the circuit diagram of RSCFSI is introduced, and its operating principles are presented with SBC-PWM and EBC-PWM strategies. A performance comparison of RSCFSI with SBI and CFSI is also presented in Chapter 3. As discussed in Chapter 2, the low-frequency ripple analysis of the single-phase SBI underlines the requirement of notably large inductors and capacitors to subdue the second harmonic ripple. In a similar manner, the low-frequency ripple problem is explored for the RSCFSI in this chapter. A low-frequency ripple analysis for the RSCFSI is performed, which reveals the existence of an additional fundamental frequency ripple as a part of the low-frequency ripple problem, which is not found in SBI. Based on the analysis, a design procedure for the selection of the passive elements of the active-front-end network of the RSCFSI is demonstrated. However, to mitigate both fundamental and second harmonic ripples in RSCFSI, even larger electrolytic capacitors and inductors are required, which significantly hinders the reliability and power density of the overall system [46].

In SBI, the low-frequency ripple problem is mitigated by the integration of independent APD networks with the SBI, as explained in Chapter 2. A similar solution would also work for RSCFSI. However, it is observed that the independent APD solutions bring down efficiency as they employ additional switches and passive elements. Also, because of the combined operation of the switches and the presence of the additional fundamental frequency component, the mitigation of low-frequency ripple in the RSCFSI poses more challenges. Recent developments in ripple reduction approaches have focused on dependent APD networks, which only include additional auxiliary passive elements to store the low-frequency ripple

energy redirected from the dc-side. Here, the inverter leg switches simultaneously handle the APD functionality and dc-ac power conversion.

Following this research, the APD-integrated RSCFSI (APDRSCFSI) topology is proposed in this chapter. Compared to RSCFSI, the changes in the proposed topology involve the inclusion of one auxiliary dc capacitor (C_s) and the splitting of the ac output filter inductor (L_f) in two (L_{f1} and L_{f2}). Also, APDRSCFSI does not add more active switches than RSCFSI, and the existing inverter switches S_3 and S_4 are utilized for APD functionality. A closed-loop control technique is also illustrated in this chapter, which integrates output voltage control and APD functionality. The closed-loop control strategy extensively utilizes multiple resonant controllers to appropriately deal with the additional fundamental frequency component alongside the second harmonic ripple.

The rest of this chapter is organized as follows: in **Section 4.2**, the low-frequency ripple of RSCFSI is analyzed with SBC-PWM, and a selection procedure for the passive elements of the active-front-end network of RSCFSI is formulated. In **Section 4.3**, the APDRSCFSI is introduced to facilitate low-frequency ripple mitigation in RSCFSI. **Section 4.3** further presents the low-frequency ripple analysis and the design of passive elements for the APDRSCFSI. Furthermore, the boundary condition of APDRSCFSI with SBC-PWM strategy is explained in **Section 4.3**. In **Section 4.4**, the low-frequency ripple of RSCFSI is analyzed with EBC-PWM, and the design of passive elements for the RSCFSI is extended for EBC-PWM strategy. In **Section 4.5**, the low-frequency ripple analysis for the APDRSCFSI with EBC-PWM is illustrated along with the design of passive elements. A comparison between SBC-PWM and EBC-PWM, applied to APDRSCFSI, is presented in **Section 4.6**. The closed-loop control strategy is illustrated in **Section 4.7**. The experimental verification of the APDRSCFSI is demonstrated in **Section 4.8**. The concluding remarks are presented at the end of this chapter.

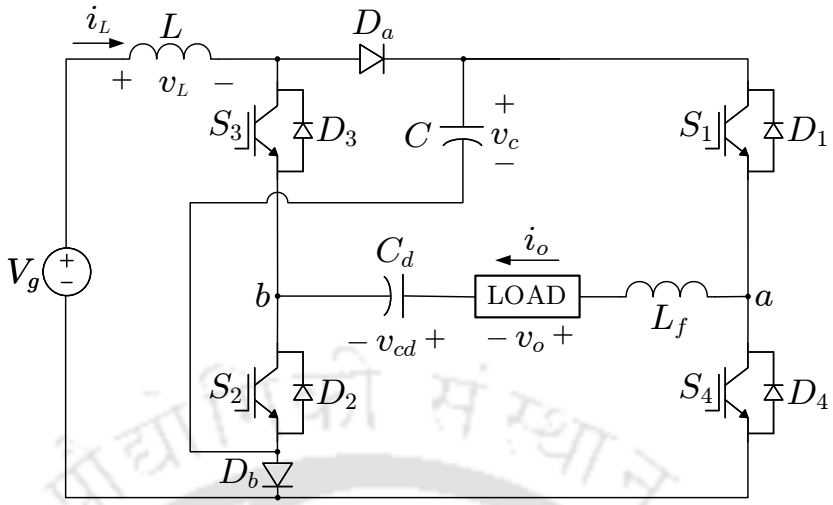


Fig. 4.1 Circuit diagram of RSCFSI.

4.2 LOW-FREQUENCY RIPPLE ANALYSIS AND DESIGN OF PASSIVE ELEMENTS OF RSCFSI WITH SBC-PWM

The circuit diagram of RSCFSI is shown in Fig. 4.1. In Chapter 2, the low-frequency analysis of SBI is described, which involves the estimation of the output and input power. The same analysis is extended for RSCFSI. However, the analysis requires modification owing to the topological differences between SBI and RSCFSI. Also, the analysis depends on the PWM strategy used to generate the gate pulses. In this section, the low-frequency ripple analysis of RSCFSI with SBC-PWM strategy is presented. Based on the analysis, the design of passive elements is also formulated in this section.

4.2.1 Low-frequency ripple analysis of RSCFSI with SBC-PWM

The output voltage and current of single-phase RSCFSI should be sinusoidal. The expressions of sinusoidal output voltage (v_o) and output current (i_o) can be considered as

$$\begin{aligned} v_o(t) &= \sqrt{2}V_o \sin \omega_o t \\ i_o(t) &= \sqrt{2}I_o \sin(\omega_o t - \varphi) \end{aligned} \tag{4.1}$$

where ω_o is the fundamental frequency, φ is the phase difference between v_o and i_o.

Therefore, the output power (p_o) can be obtained as

$$p_o(t) = v_o(t) \cdot i_o(t) = V_o I_o \cos\varphi - V_o I_o \cos(2\omega_o t - \varphi) = P_o + p_{or}(t) \tag{4.2}$$

which contains two components: the constant active power (P_o) and the low-frequency ripple power (p_{or}). In Fig. 4.1, the input power is coming from the source is constant. In order to balance the input and output power, the low-frequency ripple power must be supplied by the capacitor C and inductor L of the active-front-end network. This results in large voltage ripple on the capacitor and large current ripple on the inductor of the active-front-end network, which can be analyzed with the determination of the ripple energy of single-phase RSCFSI. However, p_{ab} signifies the power received at the inverter output, and it is observed that p_o is not same as p_{ab} because of the presence of the offset capacitor C_d and the output filter inductor L_f.

In Section 3.3, the voltage across C_d, i.e., v_{cd}, is expressed in (3.24), which is given below

$$v_{cd}(t) = D \cdot V_c - \frac{\sqrt{2} I_o}{\omega_o C_d} \cos(\omega_o t - \varphi) = V_{cd} + \tilde{v}_{cd}(t) \tag{4.3}$$

where V_{cd} and $\tilde{v}_{cd}$ are average and low-frequency components of v_{cd}, respectively. It is observed that the voltage ripple $\tilde{v}_{cd}$ contains a fundamental or ω_o ripple. Since the output current i_o is flowing through C_d, as shown in Fig. 4.1, the power drawn by C_d is

$$p_{cd}(t) = v_{cd}(t) \cdot i_o(t) = \sqrt{2} D V_c I_o \sin(\omega_o t - \varphi) - \frac{I_o^2}{\omega_o C_d} \sin(2\omega_o t - 2\varphi). \tag{4.4}$$

which also contains a fundamental component along with the second harmonic component. As shown in Fig. 4.1, i_o is flowing through the output filter inductor L_f. Therefore, v_{Lf}, the voltage across L_f, is expressed as:

$$v_{Lf}(t) = L_f \frac{di_o(t)}{dt} = \sqrt{2} \omega_o L_f I_o \cos(\omega_o t - \varphi) \tag{4.5}$$

So, the power drawn by L_f is

$$p_{Lf}(t) = v_{Lf}(t) \cdot i_o(t) = \omega_o L_f I_o^2 \sin(2\omega_o t - 2\varphi). \tag{4.6}$$

Therefore, p_{ab} is expressed as:

$$p_{ab}(t) = P_o + p_{or}(t) + p_{cd}(t) + p_{Lf}(t) = P_o + p_r(t). \tag{4.7}$$

where p_r denotes the overall low-frequency ripple power of RSCFSI. Since C_d and L_f are passive elements, they only contribute to the reactive power. Thus, p_{cd} and p_{Lf} cannot be ignored in the low-frequency ripple analysis of RSCFSI, as they constitute a considerable part of p_r. Hence, the complete expression of p_r is reckoned as:

$$p_r(t) = p_{or}(t) + p_{cd}(t) + p_{Lf}(t) = R_1 \sin(\omega_o t - \varphi) + R_2 \sin(2\omega_o t - 2\varphi + \psi) \tag{4.8}$$

where R_1 and R_2 are the peaks of the fundamental and second harmonic components of the low-frequency ripple power of RSCFSI, expressed in the following

$$\begin{aligned} R_1 &= \sqrt{2} D V_c I_o = \sqrt{2} \left(\frac{D}{1-2D} \right) V_g I_o \\ R_2 &= -\sqrt{(V_o I_o \cos\varphi)^2 + (I_o^2 X_f - V_o I_o \sin\varphi)^2} \\ X_f &= \left(\frac{1}{\omega_o C_d} - \omega_o L_f \right) \quad \psi = \tan^{-1} \frac{V_o I_o \cos\varphi}{I_o^2 X_f - V_o I_o \sin\varphi}. \end{aligned} \tag{4.9}$$

Therefore, p_r contains both fundamental and second harmonic ripple, unlike SBI or CFSI. Hence, owing to p_r, the dc-side parameters will be affected by the low-frequency ripples.

In Section 3.7, the small-signal dynamic equations are obtained in (3.100). Ignoring the parasitic resistance of the input inductor, (3.100) can be modified as:

$$\begin{aligned} L \frac{d\tilde{i}_L(t)}{dt} &= -(1-2D) \cdot \tilde{v}_c(t) \\ C \frac{d\tilde{v}_c(t)}{dt} &= (1-2D) \cdot \tilde{i}_L(t) - \tilde{i}_i(t). \end{aligned} \tag{4.10}$$

where $\tilde{i}_i$, $\tilde{i}_L$ and $\tilde{v}_c$ are the low-frequency parts of i_i, i_L and v_c, respectively. Using Laplace transform, (4.10) is taken into s-domain, and is presented as

$$\begin{aligned} sL\tilde{i}_L(s) &= -(1-2D)\cdot\tilde{v}_c(s) \\ sC\tilde{v}_c(s) &= (1-2D)\cdot\tilde{i}_L(s) - \tilde{i}_i(s). \end{aligned} \tag{4.11}$$

Solving (4.11), the relationship among $\tilde{i}_i$, $\tilde{v}_c$ and $\tilde{i}_L$ in s-domain is obtained as

$$\begin{aligned} \tilde{v}_c(s) &= -\frac{sL}{(1-2D)^2 + s^2LC}\cdot\tilde{i}_i(s) \\ \tilde{i}_L(s) &= \frac{1-2D}{(1-2D)^2 + s^2LC}\cdot\tilde{i}_i(s) \end{aligned} \tag{4.12}$$

At frequency ω_o, from (4.12) one can obtain

$$\begin{aligned} \tilde{v}_c(j\omega_o) &= -\frac{j\omega_oL}{(1-2D)^2 - \omega_o^2LC}\cdot\tilde{i}_i(j\omega_o) \\ \tilde{i}_L(j\omega_o) &= \frac{1-2D}{(1-2D)^2 - \omega_o^2LC}\cdot\tilde{i}_i(j\omega_o) \end{aligned} \tag{4.13}$$

which can be rewritten using phasor notations as

$$\begin{aligned} \overrightarrow{\tilde{v}}_{c\,\omega_o} &= -\frac{j\omega_oL}{(1-2D)^2 - \omega_o^2LC}\cdot\overrightarrow{\tilde{i}}_{i\,\omega_o} \\ \overrightarrow{\tilde{i}}_{L\,\omega_o} &= \frac{1-2D}{(1-2D)^2 - \omega_o^2LC}\cdot\overrightarrow{\tilde{i}}_{i\,\omega_o} \end{aligned} \tag{4.14}$$

where $\overrightarrow{\tilde{i}}_i$, $\overrightarrow{\tilde{v}}_{c\,\omega_o}$ and $\overrightarrow{\tilde{i}}_{L\,\omega_o}$ are the fundamental ripples of $\tilde{i}_i$, $\tilde{v}_c$ and $\tilde{i}_L$, respectively, expressed in phasor form.

Similarly, at frequency $2\omega_o$, from (4.12), one can obtain

$$\begin{aligned} \tilde{v}_c(j2\omega_o) &= -\frac{j2\omega_oL}{(1-2D)^2 - 4\omega_o^2LC}\cdot\tilde{i}_i(j2\omega_o) \\ \tilde{i}_L(j2\omega_o) &= \frac{1-2D}{(1-2D)^2 - 4\omega_o^2LC}\cdot\tilde{i}_i(j2\omega_o) \end{aligned} \tag{4.15}$$

which can be rewritten using phasor notations as

$$\begin{aligned}\overrightarrow{\tilde{v}}_{c\,2\omega_o} &= -\frac{j2\omega_o L}{(1-2D)^2 - 4\omega_o^2 LC} \cdot \overrightarrow{\tilde{i}}_{i\,2\omega_o} \\ \overrightarrow{\tilde{i}}_{L\,2\omega_o} &= \frac{1-2D}{(1-2D)^2 - 4\omega_o^2 LC} \cdot \overrightarrow{\tilde{i}}_{i\,2\omega_o}\end{aligned} \tag{4.16}$$

where $\overrightarrow{\tilde{i}}_{i\,2\omega_o}$, $\overrightarrow{\tilde{v}}_{c\,2\omega_o}$ and $\overrightarrow{\tilde{i}}_{L\,2\omega_o}$ are the second harmonic ripples of $\tilde{i}_i$, $\tilde{v}_c$ and $\tilde{i}_L$, respectively, expressed in phasor form.

As explained in Section 3.2, power is transferred from the dc-side to the ac-side in both shoot-through and nonshoot-through states for RSCFSI. Hence, p_{ab}, the output power of the inverter at the terminals a-b, should be equal to p_i, the input power of the inverter, as follows:

$$p_i(t) = V_c \cdot i_i(t) = p_{ab}(t). \tag{4.17}$$

where it can be assumed that $v_c \approx V_c$. Thus, the expression of i_i is derived as

$$i_i(t) = \frac{MI_o}{\sqrt{2}}\cos\varphi + \frac{R_1}{V_c}\sin(\omega_o t - \varphi) + \frac{R_2}{V_c}\sin(2\omega_o t - 2\varphi + \psi) \tag{4.18}$$

From (4.18), $\overrightarrow{\tilde{i}}_{i\,\omega_o}$ and $\overrightarrow{\tilde{i}}_{i\,2\omega_o}$ can be obtained as

$$\begin{aligned}\overrightarrow{\tilde{i}}_{i\,\omega_o} &= \frac{R_1}{V_c}\angle -\varphi \\ \overrightarrow{\tilde{i}}_{i\,2\omega_o} &= \frac{R_2}{V_c}\angle(-2\varphi + \psi)\end{aligned} \tag{4.19}$$

Therefore, (4.14), (4.16) and (4.18) are solved to obtain $\overrightarrow{\tilde{i}}_{L\,\omega_o}$ and $\overrightarrow{\tilde{i}}_{L\,2\omega_o}$ as follows

$$\begin{aligned}\overrightarrow{\tilde{i}}_{L\,\omega_o} &= \frac{R_1(1-2D)}{V_c[(1-2D)^2 - \omega_o^2 LC]}\angle -\varphi \\ \overrightarrow{\tilde{i}}_{L\,2\omega_o} &= \frac{R_2(1-2D)}{V_c[(1-2D)^2 - 4\omega_o^2 LC]}\angle(-2\varphi + \psi)\end{aligned} \tag{4.20}$$

Thus, $\tilde{i}_L$ can be expressed in time-domain as follows:

$$\tilde{i}_L(t) = I_{L1}\sin(\omega_o t - \varphi) + I_{L2}\sin(2\omega_o t - 2\varphi + \psi) \tag{4.21}$$

where I_{L1} and I_{L2} are the peaks of ω_o and $2\omega_o$ ripple of $\tilde{i}_L$, respectively, which are

$$\begin{aligned} I_{L1} &= \frac{R_1(1-2D)}{V_c[(1-2D)^2 - \omega_o^2 LC]} \\ I_{L2} &= \frac{R_2(1-2D)}{V_c[(1-2D)^2 - 4\omega_o^2 LC]} \end{aligned} \tag{4.22}$$

Similarly, (4.14), (4.16) and (4.18) are solved to obtain $\overrightarrow{\tilde{v}_{c\,\omega_o}}$ and $\overrightarrow{\tilde{v}_{c\,2\omega_o}}$ as follows

$$\begin{aligned} \overrightarrow{\tilde{v}_{c\,\omega_o}} &= -\frac{\omega_o L R_1}{V_c[(1-2D)^2 - \omega_o^2 LC]}\angle(90^\text{o} - \varphi) \\ \overrightarrow{\tilde{v}_{c\,2\omega_o}} &= -\frac{2\omega_o L R_2}{V_c[(1-2D)^2 - 4\omega_o^2 LC]}\angle(90^\text{o} - 2\varphi + \psi) \end{aligned} \tag{4.23}$$

Thus, $\tilde{v}_c$ can be expressed in time-domain as

$$\tilde{v}_c(t) = V_{c1}\cos(\omega_o t - \varphi) + V_{c2}\cos(2\omega_o t - 2\varphi + \psi) \tag{4.24}$$

where V_{c1} and V_{c2} are the peaks of ω_o and $2\omega_o$ ripple of $\tilde{v}_c$, respectively, which are

$$\begin{aligned} V_{c1} &= -\frac{\omega_o L R_1}{V_c[(1-2D)^2 - \omega_o^2 LC]} \\ V_{c2} &= -\frac{2\omega_o L R_2}{V_c[(1-2D)^2 - 4\omega_o^2 LC]} \end{aligned} \tag{4.25}$$

Therefore, an additional fundamental component as well as the second harmonic component is observed in both $\tilde{i}_L$ and $\tilde{v}_c$, unlike SBI or CFSI.

4.2.2 Design of passive elements

The offset capacitor C_d needs to withstand a substantial quantity of low-frequency voltage ripple because the output current i_o is passing through it, as observed in (3.24) in the expression

of v_{cd}. Let x_d be the allowable peak-to-peak voltage ripple in the following

$$x_d \geq \frac{2\hat{\tilde{v}}_{cd}}{V_{cd}} \times 100\% \tag{4.26}$$

Thus, the desired C_d should be selected as

$$C_d \geq \frac{2\sqrt{2}(1-2D)I_o}{\omega_o x_d D V_g} \tag{4.27}$$

The dc-link capacitor C and input inductor L must be able to mitigate low- and high-frequency ripples. When L and C are designed to mitigate high-frequency ripples, (3.9) is approximated as

$$L\frac{\Delta i_L}{DT_s} = V_g + V_c = (1-2D)\cdot V_c + V_c \tag{4.28}$$

$$C\frac{\Delta v_c}{DT_s} = |-I_L - I_i| = I_L + (1-2D)\cdot I_L \tag{4.29}$$

Using (3.14) and (3.35) in (4.28) and (4.29), the inductor requirement for high-frequency ripple constraint is obtained as follows:

$$L \geq \frac{2\sqrt{2}D(1-2D)T_s V_g}{bMI_o cos\varphi} \tag{4.30}$$

where b is the preferred allowance of high-frequency ripple of i_L as follows:

$$b \geq \frac{\Delta i_L}{I_L} \times 100\% \tag{4.31}$$

Similarly, the capacitor requirement to limit the high-frequency ripple is derived as follows:

$$C \geq \frac{\sqrt{2}D(1-2D)T_s MI_o cos\varphi}{aV_g}. \tag{4.32}$$

where a is the preferred allowance of high-frequency ripples of v_c as follows:

$$a \geq \frac{\Delta v_c}{V_c} \times 100\% \tag{4.33}$$

Although L and C, given in (4.30) and (4.32), respectively, are adequate for mitigation of the high-frequency ripples, larger passive elements are necessary for mitigation of the low-frequency ripple. Let x be the desired low-frequency ripples of v_c as follows:

$$\begin{aligned} x &\geq \frac{2V_{c1}}{V_c} \times 100\% \\ x &\geq \frac{2V_{c2}}{V_c} \times 100\% \end{aligned} \tag{4.34}$$

Similarly, let y be the desired low-frequency ripple of i_L as follows:

$$\begin{aligned} y &\geq \frac{2I_{L1}}{I_L} \times 100\% \\ y &\geq \frac{2I_{L2}}{I_L} \times 100\% \end{aligned} \tag{4.35}$$

Thus, the minimum capacitor requirements for mitigation of low-frequency ripple, using the specified inductor value in (4.30), are:

$$\begin{aligned} C_{\omega_o} &\geq \frac{2\sqrt{2}D(1-2D)I_o}{x\omega_o V_g} + \frac{(1-2D)^2}{\omega_o^2 L} \\ C_{2\omega_o} &\geq \frac{(1-2D)MR_2}{\sqrt{2}x\omega_o V_o V_g} + \frac{(1-2D)^2}{4\omega_o^2 L} \end{aligned} \tag{4.36}$$

Therefore, for mitigation of both low-frequency and high-frequency ripple, the preferred C must be larger than all the values of capacitance acquired in (4.32) and (4.36). After C is estimated, fundamental and second harmonic ripples, i.e., y_{ω_o} and $y_{2\omega_o}$, respectively, are estimated to review if it falls within y according to (4.37). If it exceeds the limit, a larger L is selected, and C is again estimated. This procedure is repeated until every ripple is brought down below the desired constraints.

$$\begin{aligned} y_{\omega_o} &= \frac{4D(1-2D)^2}{[\omega_o^2 LC - (1-2D)^2]M\cos\varphi} \leq y \\ y_{2\omega_o} &= \frac{2(1-2D)R_2}{[4\omega_o^2 LC - (1-2D)^2]V_o I_o \cos\varphi} \leq y \end{aligned} \tag{4.37}$$

Table 4.1 Parameters of RSCFSI used for design of passive elements

Parameter	Attributes
Input Voltage (V_g)	40 V
Peak output voltage (v_o)	120 V
Peak output current (i_o)	3 A
Output power (P_o)	180 W
Fundamental Frequency	50 Hz
Inverter Switching Frequency (f_s)	10 kHz

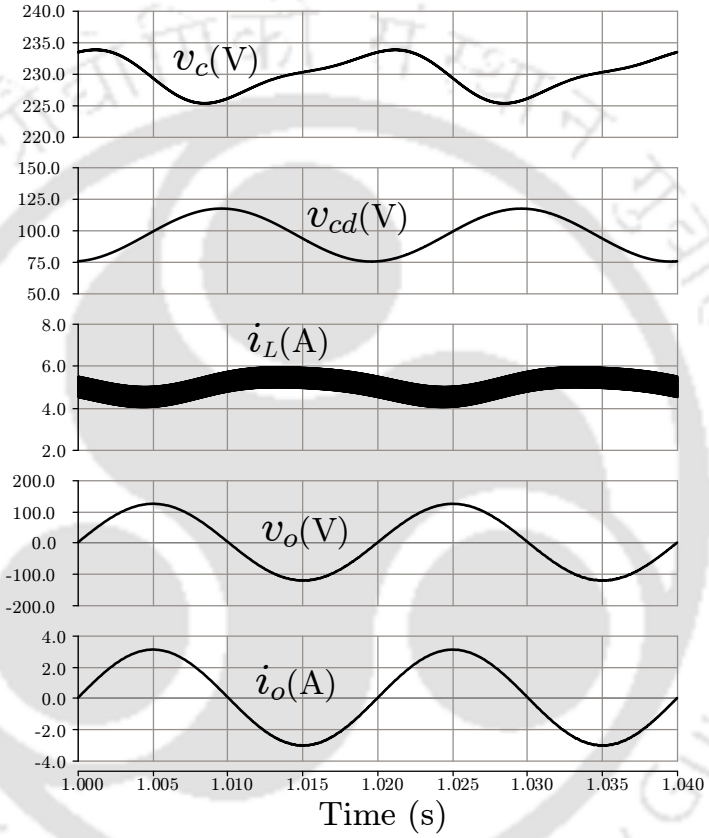


Fig. 4.2 Simulation results of single-phase RSCFSI with SBC-PWM to verify the design of passive elements. v_c: dc-link capacitor voltage, i_L: inductor current of active-front-end network, v_{cd}: offset capacitor voltage, v_o: output voltage, and i_o: output current.

In this work, taking x = 5%, C is chosen as 1160 µF; considering y = 40%, L is selected as 3.5 mH; taking x_d = 40%, C_d is chosen as 470 µF. The design of passive elements is verified in simulation with parameters given in Table 4.1. The simulation results are shown in Fig. 4.2, where the waveforms of the dc-link capacitor voltage v_c, the inductor current i_L of active-front-end network, the output voltage v_o and the output current i_o are plotted. The peak-to-peak ripple of v_c is found to be 9 V, and the average value of v_c is observed to be 230 V. Thus, the calculated value of x = 4%. Similarly, the peak-to-peak ripple of i_L is found to

be 2 A, and the average value of i_L is observed to be 5 A. Therefore, the calculated value of y = 40%. The peak-to-peak ripple of v_{cd} is found to be 40 A, and the average value of v_{cd} is observed to be 100 V. Therefore, the calculated value of x_d = 40%. Note that the peak amplitude of v_o is 120 V, and the peak amplitude of i_o is 3 A. So, it can be concluded that the designed values of passive elements of the active-front-end network can satisfactorily mitigate the low-frequency ripples below desired limitations.

4.3 LOW-FREQUENCY RIPPLE MITIGATION IN RSCFSI WITH SBC-PWM

In SBI, the low-frequency ripple problem is mitigated by integration of independent APD networks with the SBI, as explained in Chapter 2. A similar solution would also work for RSCFSI. However, it is observed that the independent APD solutions bring down efficiency as they employ additional switches and passive elements. Also, because of the combined operation of the switches and the presence of the additional fundamental frequency component, the mitigation of low-frequency ripple in the RSCFSI poses more challenges. Recent developments in ripple reduction approaches have focused on dependent APD networks, which only include additional auxiliary passive elements to store the low-frequency ripple energy redirected from the dc-side. Here, the inverter leg switches handle both APD functionality and dc-ac power conversion. Following this research, the APD-integrated RSCFSI (APDRSCFSI) topology is proposed in this section.

4.3.1 Introduction to APDRSCFSI

For low-frequency ripple mitigation, the topology of RSCFSI is altered with the addition of a dependent APD network. The modifications involve the inclusion of one auxiliary dc capacitor C_s and the ac output filter inductor L_f being halved in L_{f1} and L_{f2}, as shown in Fig. 4.3. The switches S_3 and S_2 are utilized for APD functionality. The resultant topology is named APD-integrated RSCFSI (APDRSCFSI). Alongside acting as a filter for the output current, L_{f2} helps the transfer of the low-frequency ripple from C to C_s. Thus, the current

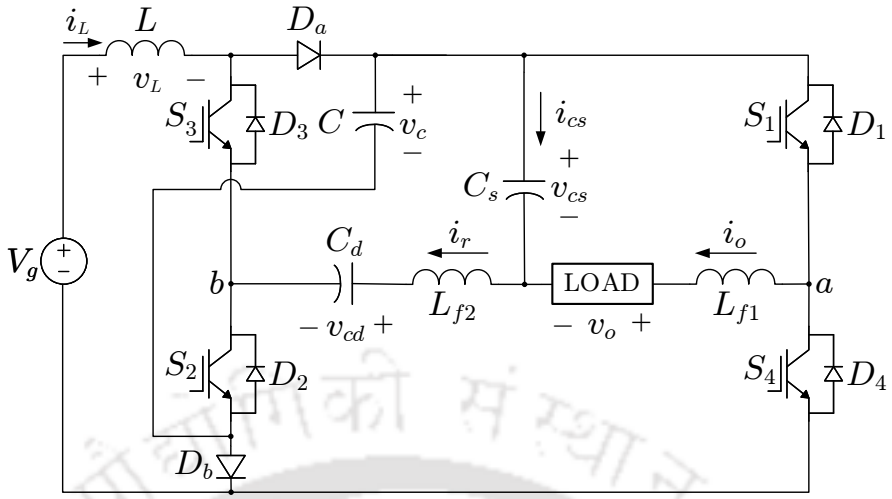


Fig. 4.3 Circuit Diagram of APDRSCFSI.

through L_{f2} is denoted as the ripple current (i_r). Like the RSCFSI, the switches S_1 and S_4 carry out the shoot-through process and facilitate the conversion of dc-ac power. At the same time, S_3 and S_2 facilitate the transfer and storage of low-frequency ripple energy in C_s and also carry out the shoot-through process and facilitate the conversion of dc-ac power.

4.3.2 Low-frequency ripple analysis of APDRSCFSI with SBC-PWM

Since the auxiliary capacitor C_s stores both fundamental and second harmonic ripple energies, the expression of the auxiliary capacitor voltage v_{cs} can be considered as

$$v_{cs}(t) = V_{cs} + V_{cs1}\cos(\omega_o t - \varphi_1) + V_{cs2}\cos(2\omega_o t - \varphi_2) \tag{4.38}$$

where V_{cs}, V_{cs1} and V_{cs2} are the average value, the peaks of fundamental and second harmonic ripple of v_{cs}, respectively. Thus, the auxiliary capacitor current i_{cs} is derived from (4.38) as

$$i_{cs}(t) = C_s\frac{dv_{cs}(t)}{dt} = -\omega_o C_s V_{cs1}\sin(\omega_o t - \varphi_1) - 2\omega_o C_s V_{cs2}\sin(2\omega_o t - \varphi_2) \tag{4.39}$$

For simplicity, one can consider $\varphi_1 \approx \varphi$, and (4.39) becomes

$$i_{cs}(t) = -\omega_o C_s V_{cs1}\sin(\omega_o t - \varphi) - 2\omega_o C_s V_{cs2}\sin(2\omega_o t - \varphi_2) \tag{4.40}$$

Therefore, the fundamental ripple of i_{cs} is shifted by a phase of 180^{o} from i_o. Thus, the expression of ripple current i_r can be written as:

$$\begin{aligned} i_r(t) &= i_o(t) + i_{cs}(t) \\ &= \{(\sqrt{2}I_o - \omega_o C_s V_{cs1})\sin(\omega_o t - \varphi) - 2\omega_o C_s V_{cs2}\sin(2\omega_o t - \varphi_2)\} \\ &= (\sqrt{2}I_o + I_{cs1})\sin(\omega_o t - \varphi) + I_{cs2}\sin(2\omega_o t - \varphi_2) \end{aligned} \tag{4.41}$$

where $I_{cs1} = -\omega_o C_s V_{cs1}$ and $I_{cs2} = -2\omega_o C_s V_{cs2}$. Thus, i_r is less than i_o, which indicates lower current stress for S_2, S_3, C_d and L_{f2}. Since i_r is flowing through C_d, $\tilde{v}_{cd}$ is also lowered, which reduces capacitor requirement.

For RSCFSI, the power received at the inverter output p_{ab} is given in (4.7). Alongside previous considerations, p_{ab} of APDRSCFSI must also consider the power stored by the auxiliary capacitor, p_{cs}, expressed in the following

$$p_{cs}(t) = v_{cs}(t)\cdot i_{cs}(t) \approx V_{cs}\{I_{cs1}\sin(\omega_o t - \varphi) + I_{cs2}\sin(2\omega_o t - \varphi_2)\} \tag{4.42}$$

In (4.42), the terms containing frequencies higher than $2\omega_o$ and other higher order terms are ignored. In RSCFSI, i_o is flowing through C_d, and the expressions of v_{cd} and p_{cd} are calculated accordingly in (4.3) and (4.4), respectively. In APDRSCFSI, i_r is flowing through C_d, as shown in Fig. 4.3, which indicates

$$C_d \cdot \frac{dv_{cd}(t)}{dt} = i_r(t) \tag{4.43}$$

Therefore, the expression of v_{cd} is modified as follows:

$$v_{cd}(t) = D\cdot V_c - \frac{\sqrt{2}I_o + I_{cs1}}{\omega_o C_d}\cos(\omega_o t - \varphi) - \frac{I_{cs2}}{2\omega_o C_d}\cos(2\omega_o t - \varphi_2). \tag{4.44}$$

From which, the expression of p_{cd} can be also altered as follows:

$$p_{cd}(t) = v_{cd}(t)\cdot i_r(t) \approx V_{cd}\{(\sqrt{2}I_o + I_{cs1})\sin(\omega_o t - \varphi) + I_{cs2}\sin(2\omega_o t - \varphi_2)\} \tag{4.45}$$

In (4.45), the terms containing frequencies higher than $2\omega_o$ and other higher order terms are ignored. Thus, p_{ab} should be modified as:

$$p_{ab}(t) = P_o + p_{or}(t) + p_{Lf}(t) + p_{cd}(t) + p_{cs}(t) = P_o + p_r(t) \tag{4.46}$$

where p_r is the low-frequency ripple power of APDRSCFSI. Assuming $\varphi_2 \approx (2\varphi - \psi)$, p_r can be expressed as

$$p_r(t) = p_{or}(t) + p_{Lf}(t) + p_{cd}(t) + p_{cs}(t) = R_1' \sin(\omega_o t - \varphi) + R_2' \sin(2\omega_o t - 2\varphi + \psi). \tag{4.47}$$

where R_1' and R_2' are the peaks of fundamental and second harmonic ripples of the low-frequency ripple power of APDRSCFSI, respectively, expressed in the following

$$\begin{aligned} R_1' &= R_1 - \omega_o C_s V_{cs1}(V_{cd} + V_{cs}) \\ R_2' &= R_2 - 2\omega_o C_s V_{cs2}(V_{cd} + V_{cs}) \end{aligned} \tag{4.48}$$

As R_1' and R_2' of APDRSCFSI are significantly lower than R_1 and R_2 of RSCFSI, respectively, both fundamental and second harmonic components of the low-frequency ripple power of APDRSCFSI are much smaller than that of RSCFSI.

Following a similar procedure, described for RSCFSI in Section 4.2, i_i for APDRSCFSI can be derived from (4.17) and (4.46) as follows:

$$i_i(t) = I_i + \frac{R_1'}{V_c} \sin(\omega_o t - \varphi) + \frac{R_2'}{V_c} \sin(2\omega_o t - 2\varphi + \psi). \tag{4.49}$$

For RSCFSI, the low-frequency parts of i_L and v_c, i.e., $\tilde{i}_L$ and $\tilde{v}_c$, respectively, are presented in (4.21) and (4.24), respectively. Similarly, for APDRSCFSI, solving (4.14), (4.16) and (4.49), the expression of $\tilde{i}_L$ is obtained as follows:

$$\tilde{i}_L(t) = I_{L1} \sin(\omega_o t - \varphi) + I_{L2} \sin(2\omega_o t - 2\varphi + \psi) \tag{4.50}$$

where

$$I_{L1} = \frac{R_1'(1-2D)}{V_c[(1-2D)^2 - \omega_o^2 LC]}$$
$$I_{L2} = \frac{R_2'(1-2D)}{V_c[(1-2D)^2 - 4\omega_o^2 LC]} \tag{4.51}$$

Similarly, solving (4.14), (4.16) and (4.49), the expression of $\tilde{v}_c$ is derived as follows:

$$\tilde{v}_c(t) = V_{c1}\cos(\omega_o t - \varphi) + V_{c2}\cos(2\omega_o t - 2\varphi + \psi) \tag{4.52}$$

where

$$V_{c1} = -\frac{\omega_o L R_1'}{V_c[(1-2D)^2 - \omega_o^2 LC]}$$
$$V_{c2} = -\frac{2\omega_o L R_2'}{V_c[(1-2D)^2 - 4\omega_o^2 LC]} \tag{4.53}$$

Since R_1' and R_2' are significantly lower than R_1 and R_2, respectively, both $\tilde{i}_L$ and $\tilde{v}_c$ for APDRSCFSI are also significantly reduced, compared to RSCFSI.

4.3.3 Design of passive elements

The design of passive elements, described in Section 4.2.2, is extended for APDRSCFSI. The selection of C_s and L_{f2} involves consideration of both ω_o and $2\omega_o$ frequencies because the low-frequency ripple power contains both, according to (4.47). In order to make the low-frequency ripple of v_c completely zero, i.e., $V_{c1,2} = 0$, the required minimum values of C_s at different frequencies are

$$C_{s\text{-}\omega_o} \geq \frac{R_1}{\omega_o V_{cs1}(V_{cd} + V_{cs})}$$
$$C_{s\text{-}2\omega_o} \geq \frac{R_2}{2\omega_o V_{cs2}(V_{cd} + V_{cs})} \tag{4.54}$$

where $C_{s\text{-}2\omega_o}$ and $C_{s\text{-}2\omega_o}$ are the required capacitances at ω_o and $2\omega_o$, respectively. Thus, the final value of C_s should be chosen as

$$C_s \geq \text{Max}(C_{s\text{-}\omega_o}, C_{s\text{-}2\omega_o}) \tag{4.55}$$

If C_s is designed to completely diminish $\tilde{v}_c$, the required C would be very small, as it is only required to mitigate high-frequency ripple. However, this results in a considerably large value of C_s. If both C and C_s are small enough, film capacitors can replace conventional electrolytic capacitors, significantly improving the lifetime and overall system reliability. So, the design goal is to lessen the amount of voltage ripple by a factor of k as

$$\frac{(\tilde{v}_c)_{p\text{-}p} \text{ in RSCFSI}}{(\tilde{v}_c)_{p\text{-}p} \text{ in APDRSCFSI}} \geq k \tag{4.56}$$

which can be approximated as $\dfrac{R_1}{R_1'} \geq k; \quad \dfrac{R_2}{R_2'} \geq k$. Hence, the respective capacitance requirements at ω_o and $2\omega_o$ are

$$\begin{aligned} C_{s\text{-}\omega_o} &\geq \frac{k-1}{k} \cdot \frac{R_1}{\omega_o V_{cs1}(V_{cd}+V_{cs})} \\ C_{s\text{-}2\omega_o} &\geq \frac{k-1}{k} \cdot \frac{R_2}{2\omega_o V_{cs2}(V_{cd}+V_{cs})} \end{aligned} \tag{4.57}$$

The auxiliary capacitor C_s must be selected higher than both $C_{s\text{-}\omega_o}$ and $C_{s\text{-}2\omega_o}$. As both V_{cs} and its ripple $V_{cs1,2}$ are inversely proportional to C_s, greater V_{cs} or $V_{cs1,2}$ facilitates smaller C_s. Moreover, the dc-link capacitor C is only required to diminish the low-frequency ripples reduced by k, because rest of the ripple energy is now deflected to C_s. Therefore, the minimum capacitor requirements as obtained in (4.36) are modified as

$$\begin{aligned} C_{\omega_o} &\geq \frac{2R_1'}{\omega_o x V_c^2} + \frac{(1-2D)^2}{\omega_o^2 L} \\ C_{2\omega_o} &\geq \frac{R_2'}{\omega_o x V_c^2} + \frac{(1-2D)^2}{(2\omega)^2 L}. \end{aligned} \tag{4.58}$$

In order to mitigate both low-frequency and high-frequency ripple, the preferred C must be larger than all the values of capacitance acquired in (4.32) and (4.58).

Choosing k = 6, V_{cs} = 0.375 · V_c, V_{cs1}/V_{cs} = 0.16, both of C and C_s are selected as 220 μF. Therefore, C is reduced by a factor of 6 compared to RSCFSI.

After C is estimated, the procedure to select L, given in Section 4.2.2, is again performed as per the following:

$$\begin{aligned} y_{\omega_o} &= \frac{2R_1'(1-2D)}{[(1-2D)^2-\omega_o^2 LC]V_o I_o \cos\varphi} \times 100\% \leq y \\ y_{2\omega_o} &= \frac{2R_2'(1-2D)}{[(1-2D)^2-4\omega_o^2 LC]V_o I_o \cos\varphi} \times 100\% \leq y \end{aligned} \tag{4.59}$$

Taking y = 40%, L is chosen as 2.75 mH.

Since L_{f2} is not used as a ripple energy storage device, the ripple current i_r does not contain any dc part. Therefore, L_{f2} ought to be designed from the peak auxiliary inductor currents at ω_o and $2\omega_o$, which are:

$$\begin{aligned} \hat{i}_{r\text{-}\omega_o} &= \sqrt{2}I_o + I_{cs1} + \Delta i_r \\ \hat{i}_{r\text{-}2\omega_o} &= I_{cs2} + \Delta i_r \end{aligned} \tag{4.60}$$

where the expression of Δi_r is given as

$$\Delta i_r = \frac{D_s T_s (V_c - V_{cs} - V_{cd})}{L_{f2}} \tag{4.61}$$

The turn on duration of S_2 is taken as $D_s \cdot T_s$. The current stresses of the switches S_3 and S_4 at ω_o and $2\omega_o$ are $\hat{i}_{r\text{-}\omega_o}$ and $\hat{i}_{r\text{-}2\omega_o}$, respectively, which must be within I_{max}, the maximum allowable continuous conducting current. Therefore, L_{f2} should be estimated as:

$$L_{f2} \geq \max\left\{ \frac{D_s T_s (V_c - V_{cs} - V_{cd})}{I_{\text{max}} - \sqrt{2}I_o - I_{cs1}}, \frac{D_s T_s (V_c - V_{cs} - V_{cd})}{I_{\text{max}} - I_{cs2}} \right\} \tag{4.62}$$

Choosing I_{Max} = 6 A, L_{f2} is selected as 2 mH.

As i_r is flowing through C_d in APDRSCFSI, and $i_r < i_o$, according to (4.41), the minimum requirement of C_d is also modified as follows:

$$C_d \geq \frac{2(1-2D)(\sqrt{2}I_o - \omega_o C_s V_{cs1})}{\omega_o x_d D V_g} \tag{4.63}$$

Taking x_d = 40%, C_d is selected as 220 μF, which shows a reduction by approximately 53% compared to RSCFSI.

4.3.4 Boundary condition of APDRSCFSI

In Table 3.1, different operational states of RSCFSI with SBC-PWM are given according to switching conditions of different active elements. Considering similar operational states for APDRSCFSI with SBC-PWM, the equivalent circuit diagrams for each states are shown in Fig. 4.4. As explained in Chapter 3, the duration of the shoot-through state 1 is $D \cdot T_s$, and the overall duration of the nonshoot-through states are $(1-D) \cdot T_s$. In each state, the voltage across the inductor L_{f2} is expressed as follows:

$$v_{Lf2}(t) = \begin{cases} -v_{cs}(t) - v_{cd}(t) + v_c(t); & \text{in shoot-through state 1} \\ -v_{cs}(t) - v_{cd}(t) + v_c(t); & \text{in nonshoot-through states 1, 2, 4} \\ -v_{cs}(t) - v_{cd}(t); & \text{in nonshoot-through state 3} \end{cases} \tag{4.64}$$

Using small ripple approximation, averaging (4.64) over the entire switching period T_s and using inductor volt-second balance, one can obtain:

$$\langle v_{Lf2}(t) \rangle_{T_s} = \left(D + \frac{1-D}{2} \right) \cdot V_c - V_{cs} - V_{cd} = 0. \tag{4.65}$$

Since $V_{cd} = D \cdot V_c$, according to (4.3), the average value of v_{cs} is determined as:

$$V_{cs} = \left(\frac{1-D}{2} \right) \cdot V_c. \tag{4.66}$$

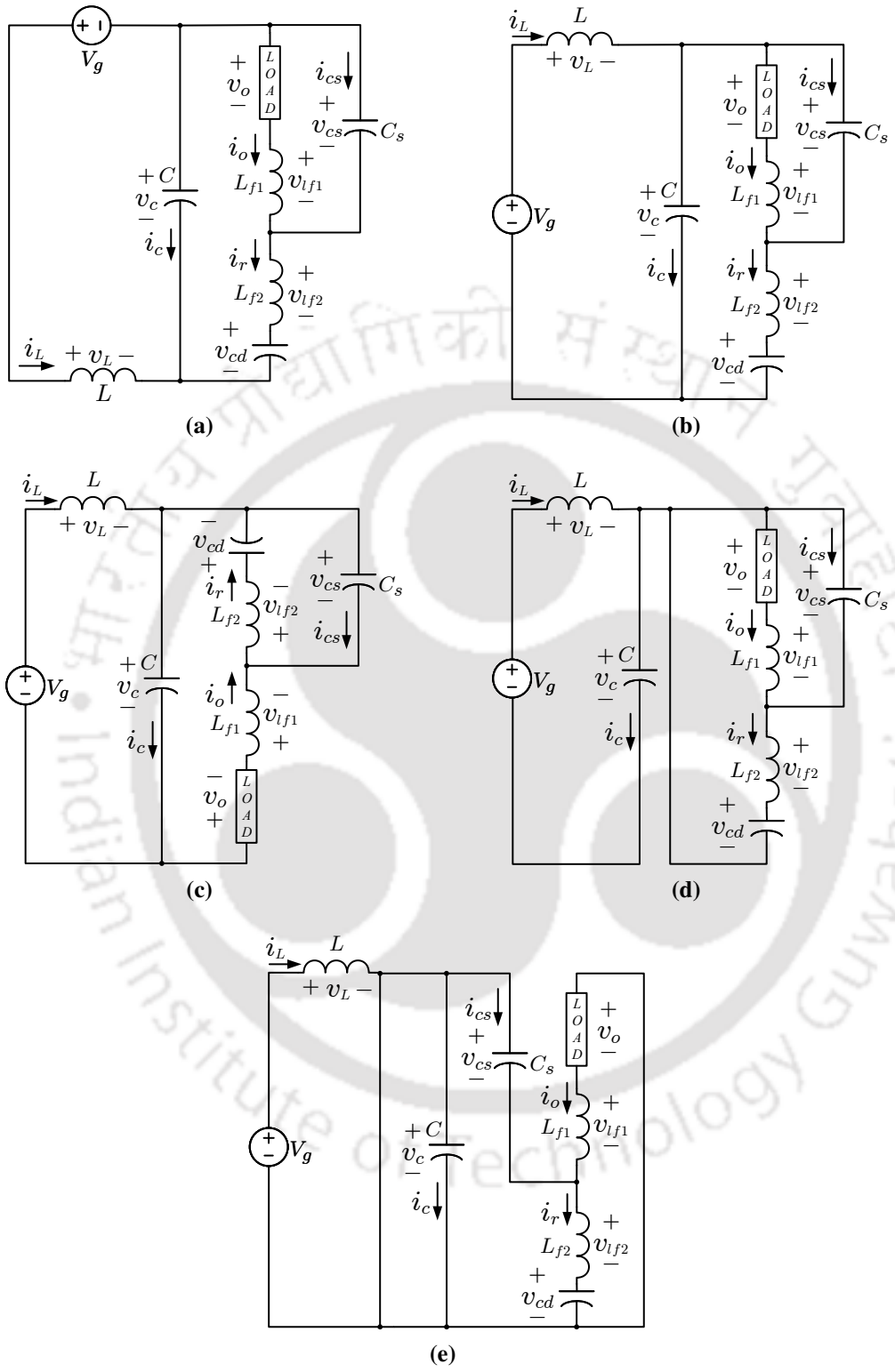


Fig. 4.4 Different operational states of APDRSCFSI with SBC-PWM: (a) shoot-through state-1, (b) nonshoot-through state-1, (c) nonshoot-through state-2, (d) nonshoot-through state-3 and (e) nonshoot-through state-4.

Furthermore, in all operational states, except nonshoot-through states 2 and 4, as shown in Fig. 4.4, one can write

$$v_o(t) + v_{Lf1}(t) = v_{cs}(t) \tag{4.67}$$

where v_{Lf1} is the voltage across L_{f1}. As the output current i_o flows through L_{f1}, the expression of v_{Lf1} can be derived as

$$v_{Lf1}(t) = L_{f1}\frac{di_o(t)}{dt} = \sqrt{2}\omega_o L_{f1} I_o \cos(\omega_o t - \varphi) \tag{4.68}$$

Using (4.1), (4.38), (4.39) in (4.67), while considering only fundamental component, the expression for the highest possible peak output voltage is obtained as follows:

$$\hat{v}_o = V_{cs} + V_{cs1}\sin\varphi_1 - \sqrt{2}\omega_o L_{f1} I_o \sin\varphi \tag{4.69}$$

If the ac load is considered to be unity power factor, i.e., φ = 0, one can write

$$\hat{v}_o \approx V_{cs} = \left(\frac{1-D}{2}\right)\cdot V_c. \tag{4.70}$$

Hence, with SBC-PWM strategy, the dc-ac gain of APDRSCFSI becomes

$$\frac{\hat{v}_o}{V_g} = \frac{MV_c}{V_g} \leq \left(\frac{1-D}{2}\right)\cdot\left(\frac{1}{1-2D}\right). \tag{4.71}$$

So, compared to the dc-ac gain of RSCFSI, given in (3.56), the dc-ac gain of APDRSCFSI is reduced, which is a limitation of APDRSCFSI. In Chapter 3, to improve the dc-ac gain of RSCFSI for the same shoot-through duty ratio, EBC-PWM is applied to RSCFSI. In the following section, EBC-PWM is also applied to APDRSCFSI to improve its dc-ac gain.

4.4 LOW-FREQUENCY RIPPLE ANALYSIS AND DESIGN OF PASSIVE ELEMENTS OF RSCFSI WITH EBC-PWM

4.4.1 Low-frequency ripple analysis of RSCFSI with EBC-PWM

The low-frequency ripple analysis is extended for EBC-PWM strategy. In this case, some modifications are required for the equations derived for SBC-PWM. With EBC-PWM, the offset capacitor voltage v_{cd} is derived in (3.73), which is

$$v_{cd}(t) = D_1 \cdot V_c - \frac{\sqrt{2}I_o}{\omega_o C_d}\cos(\omega_o t - \varphi) = V_{cd} + \tilde{v}_{cd} \tag{4.72}$$

Thus, the power drawn by C_d is

$$p_{cd}(t) = v_{cd}(t) \cdot i_o(t) = \sqrt{2}D_1 V_c I_o \sin(\omega_o t - \varphi) - \frac{I_o^2}{\omega_o C_d}\sin(2\omega_o t - 2\varphi). \tag{4.73}$$

With EBC-PWM, p_{or} and p_{Lf} remain unchanged in the expression of p_r, given in (4.8), but p_{cd} is modified. Thus, p_r is modified as follows:

$$p_r(t) = R_1 \sin(\omega_o t - \varphi) + R_2 \sin(2\omega_o t - 2\varphi + \psi) \tag{4.74}$$

where R_1 is modified as

$$R_1 = \sqrt{2}D_1 V_c I_o = \frac{1}{\sqrt{2}} \cdot \left(\frac{1+3D}{1-3D}\right) \cdot V_g I_o \tag{4.75}$$

The rest of the parameters, given in (4.9), remain unchanged. Following a similar procedure, described for RSCFSI with SBC-PWM in Section 4.2, i_i for RSCFSI with EBC-PWM can be derived from (4.17) and (4.74) as follows:

$$i_i(t) = \left(\frac{4}{3+D}\right) \cdot \left[\frac{MI_o}{\sqrt{2}}\cos\varphi + \frac{R_1}{V_c}\sin(\omega_o t - \varphi) + \frac{R_2}{V_c}\sin(2\omega_o t - 2\varphi + \psi)\right] \tag{4.76}$$

Similar to the process followed in Section 4.2, the dynamic equations of RSCFSI with EBC-PWM are obtained as:

$$\begin{aligned} L\frac{d\tilde{i}_L(t)}{dt} &= -\left(\frac{1-3D}{2}\right)\cdot\tilde{v}_c(t) \\ C\frac{d\tilde{v}_c(t)}{dt} &= \left(\frac{1-3D}{2}\right)\cdot\tilde{i}_L(t) - \left(\frac{3+D}{4}\right)\cdot\tilde{i}_i(t). \end{aligned} \tag{4.77}$$

Using Laplace transform, (4.10) is taken into s-domain, and is presented as

$$\begin{aligned} sL\tilde{i}_L(s) &= -\left(\frac{1-3D}{2}\right)\cdot\tilde{v}_c(s) \\ sC\tilde{v}_c(s) &= \left(\frac{1-3D}{2}\right)\cdot\tilde{i}_L(s) - \left(\frac{3+D}{4}\right)\tilde{i}_i(s). \end{aligned} \tag{4.78}$$

Solving (4.78), the relationship among $\tilde{i}_i$, $\tilde{v}_c$ and $\tilde{i}_L$ in s-domain is obtained as

$$\begin{aligned} \tilde{v}_c(s) &= -\frac{sL(3+D)}{(1-3D)^2+4s^2LC}\cdot\tilde{i}_i(s) \\ \tilde{i}_L(s) &= \frac{(1-3D)(3+D)}{2[(1-3D)^2+4s^2LC]}\cdot\tilde{i}_i(s) \end{aligned} \tag{4.79}$$

At frequency ω_o, from (4.79) one can obtain

$$\begin{aligned} \tilde{v}_c(j\omega_o) &= -\frac{j\omega_oL(3+D)}{(1-3D)^2-4\omega_o^2LC}\cdot\tilde{i}_i(j\omega_o) \\ \tilde{i}_L(j\omega_o) &= \frac{(1-3D)(3+D)}{2[(1-3D)^2-4\omega_o^2LC]}\cdot\tilde{i}_i(j\omega_o) \end{aligned} \tag{4.80}$$

which can be rewritten using phasor notations as

$$\begin{aligned} \overrightarrow{\tilde{v}_{c\,\omega_o}} &= -\frac{j\omega_oL(3+D)}{(1-3D)^2-4\omega_o^2LC}\cdot\overrightarrow{\tilde{i}_{i\,\omega_o}} \\ \overrightarrow{\tilde{i}_{L\,\omega_o}} &= \frac{(1-3D)(3+D)}{2[(1-3D)^2-4\omega_o^2LC]}\cdot\overrightarrow{\tilde{i}_{i\,\omega_o}} \end{aligned} \tag{4.81}$$

Similarly, at frequency $2\omega_o$, from (4.79) one can obtain

$$\begin{aligned}\tilde{v}_c(j\omega_o) &= -\frac{j2\omega_o L(3+D)}{(1-3D)^2-16\omega_o^2 LC}\cdot\tilde{i}_i(j\omega_o)\\ \tilde{i}_L(j\omega_o) &= \frac{(1-3D)(3+D)}{2[(1-3D)^2-16\omega_o^2 LC]}\cdot\tilde{i}_i(j\omega_o)\end{aligned} \tag{4.82}$$

which can be rewritten using phasor notations as

$$\begin{aligned}\overrightarrow{\tilde{v}}_{c\,\omega_o} &= -\frac{j2\omega_o L(3+D)}{(1-3D)^2-16\omega_o^2 LC}\cdot\overrightarrow{\tilde{i}}_{i\,\omega_o}\\ \overrightarrow{\tilde{i}}_{L\,\omega_o} &= \frac{(1-3D)(3+D)}{2[(1-3D)^2-16\omega_o^2 LC]}\cdot\overrightarrow{\tilde{i}}_{i\,\omega_o}\end{aligned} \tag{4.83}$$

Therefore, (4.81), (4.83) and (4.76) are solved to obtain $\tilde{i}_L$ as follows:

$$\tilde{i}_L(t) = I_{L1}\sin(\omega_o t-\varphi) + I_{L2}\sin(2\omega_o t-2\varphi+\psi) \tag{4.84}$$

where

$$\begin{aligned}I_{L1} &= \frac{2R_1(1-3D)}{V_c[(1-3D)^2-4\omega_o^2 LC]}\\ I_{L2} &= \frac{2R_2(1-3D)}{V_c[(1-3D)^2-16\omega_o^2 LC]}\end{aligned} \tag{4.85}$$

Similarly, (4.81), (4.83) and (4.76) are solved to obtain are solved to obtain $\tilde{v}_c$ as

$$\tilde{v}_c(t) = V_{c1}\cos(\omega_o t-\varphi) + V_{c2}\cos(2\omega_o t-2\varphi+\psi) \tag{4.86}$$

where

$$\begin{aligned}V_{c1} &= -\frac{4\omega_o LR_1}{V_c[(1-3D)^2-4\omega_o^2 LC]}\\ V_{c2} &= -\frac{8\omega_o LR_2}{V_c[(1-3D)^2-16\omega_o^2 LC]}\end{aligned} \tag{4.87}$$

Similar to SBC-PWM, both fundamental and second harmonic ripples are observed in both $\tilde{i}_L$ and $\tilde{v}_c$, when EBC-PWM is applied to RSCFSI.

4.4.2 Design of passive elements

The offset capacitor C_d needs to withstand a substantial quantity of low-frequency voltage ripple because the output current i_o is passing through it, as observed in (3.24) in the expression of v_{cd}. If x_d is regarded as the allowable peak-to-peak voltage ripple, defined as a percentage of average capacitor voltage V_{cd} as follows:

$$x_d \geq \frac{2\tilde{v}_{cd(p\text{-}p)}}{V_{cd}} \times 100\% \tag{4.88}$$

Thus, the desired C_d should be selected as

$$C_d \geq \frac{4\sqrt{2}I_o(1-3D)}{\omega_o x_d(3D+1)V_g} \tag{4.89}$$

Taking x_d = 40%, C_d is chosen as 470 μF.

The dc-link capacitor C and input inductor L are designed to mitigate high-frequency ripples, (3.58) is approximated as

$$L\frac{\Delta i_L}{DT_s} = V_g + V_c = \left(\frac{1-3D}{2}\right)\cdot V_c + V_c \tag{4.90}$$

$$C\frac{\Delta v_c}{DT_s} = |-I_L - I_i| = I_L + 2\cdot\left(\frac{1-3D}{3+D}\right)\cdot I_L \tag{4.91}$$

Using (3.64) and (3.66) in (4.90) and (4.91), the inductor and capacitor requirements for high-frequency ripple constraint are obtained as follows:

$$L \geq \frac{3DT_sV_g}{\sqrt{2}bMI_o cos\varphi} \tag{4.92}$$

$$C \geq \frac{3D(1-D)T_sMI_o cos\varphi}{2\sqrt{2}aV_g} \tag{4.93}$$

where a and b are the preferred allowance of high-frequency ripples of v_c and i_L expressed in (4.33) and (4.31), respectively. Although C and L, given in (4.93) and (4.92), respectively, are adequate for mitigation of the high-frequency ripple, larger C and L are necessary for mitigation of the low-frequency ripple.

Considering x and y as the desired low-frequency ripples of v_c and i_L, given in (4.34) and (4.35), respectively, the minimum capacitor requirements for mitigation of low-frequency ripple, using the specified inductor value in (4.30), are:

$$\begin{aligned} C_{\omega_o} &\geq \frac{2R_1}{\omega_o x V_c^2} + \frac{(1-3D)^2}{4\omega_o^2 L} \\ C_{2\omega_o} &\geq \frac{2R_2}{2\omega_o x V_c^2} + \frac{(1-3D)^2}{16\omega_o^2 L} \end{aligned} \tag{4.94}$$

Therefore, for mitigation of both low-frequency and high-frequency ripple, the preferred C must be larger than all the values of capacitance acquired in (4.93) and (4.94). After C is estimated, fundamental and second harmonic ripples, i.e., y_{ω_o} and $y_{2\omega_o}$, respectively, are estimated to review if it falls within y according to (4.95). If it exceeds the limit, a larger L is selected, and C is again estimated. This procedure is repeated until every ripple is brought down below the desired constraints.

$$\begin{aligned} y_{\omega_o} &= \frac{4R_1(1-3D)}{[(1-3D)^2 - 4\omega_o^2 LC]V_o I_o \cos\varphi} \times 100\% \leq y \\ y_{2\omega_o} &= \frac{4R_2(1-3D)}{[(1-3D)^2 - 4(2\omega)^2 LC]V_o I_o \cos\varphi} \times 100\% \leq y \end{aligned} \tag{4.95}$$

In this work, taking x = 5%, C is chosen as 1160 µF; considering y = 40%, L is selected as 3.5 mH; taking x_d = 40%, C_d is chosen as 470 µF. The design of passive elements is verified in simulation with parameters given in Table 4.1. The simulation results are shown in Fig. 4.5, where the waveforms of the dc-link capacitor voltage v_c, the inductor current i_L of active-front-end network, the output voltage v_o and the output current i_o are plotted. The peak-to-peak ripple of v_c is found to be 7 V, and the average value of v_c is observed to be 220 V. Thus, the calculated value of x = 3%. Similarly, the peak-to-peak ripple of i_L is found to

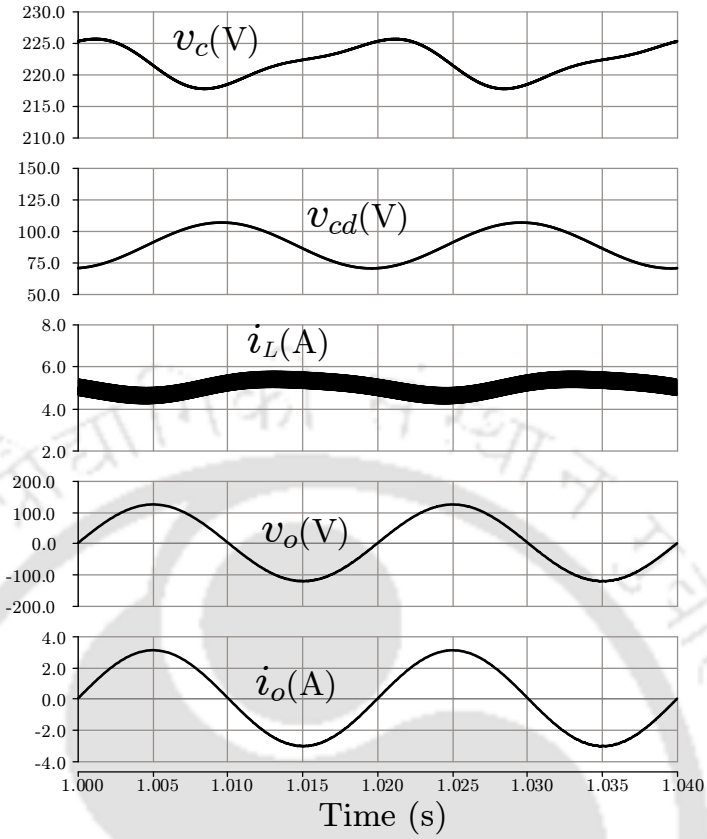


Fig. 4.5 Simulation results of single-phase RSCFSI with EBC-PWM to verify the design of passive elements. v_c: dc-link capacitor voltage, i_L: inductor current of active-front-end network, v_{cd}: offset capacitor voltage, v_o: output voltage, and i_o: output current.

be 1.5 A, and the average value of i_L is observed to be 5 A. Therefore, the calculated value of y = 30%. The peak-to-peak ripple of v_{cd} is found to be 30 V, and the average value of v_{cd} is observed to be 90 V. Therefore, the calculated value of x_d = 33%. Note that the peak amplitude of v_o is 120 V, and the peak amplitude of i_o is 3 A. So, it can be concluded that the designed values of passive elements of the active-front-end network can satisfactorily mitigate the low-frequency ripples below desired limitations.

4.5 LOW-FREQUENCY RIPPLE MITIGATION IN RSCFSI WITH EBC-PWM

4.5.1 Low-frequency ripple analysis of APDRSCFSI with EBC-PWM

For SBC-PWM, the expressions of the auxiliary capacitor voltage v_{cs}, the auxiliary capacitor current i_{cs} and the ripple power stored by the auxiliary capacitor C_s are obtained in

(4.38), (4.39) and (4.42), respectively, which remain same for APDRSCFSI with EBC-PWM. The relationship between the ripple current i_o and the output current i_o is established in (4.41), which also remains unchanged.

In APDRSCFSI, i_r is flowing through C_d, as shown in Fig. 4.3, which indicates

$$C_d \cdot \frac{dv_{cd}(t)}{dt} = i_r(t) \tag{4.96}$$

Therefore, the expression of v_{cd} is modified as follows:

$$v_{cd}(t) = D_1 \cdot V_c - \frac{\sqrt{2}I_o + I_{cs1}}{\omega_o C_d}\cos(\omega_o t - \varphi) - \frac{I_{cs2}}{2\omega_o C_d}\cos(2\omega_o t - \varphi_2). \tag{4.97}$$

From which, the expression of p_{cd} can be also altered as follows:

$$p_{cd}(t) = v_{cd}(t) \cdot i_r(t) \approx D_1 V_c\{(\sqrt{2}I_o + I_{cs1})\sin(\omega_o t - \varphi) + I_{cs2}\sin(2\omega_o t - \varphi_2)\} \tag{4.98}$$

The low-frequency ripple power of APDRSCFSI with SBC-PWM is derived in (4.47). Following a similar set of steps and approximations, the low-frequency ripple power of APDRSCFSI with EBC-PWM, p_r can be obtained, which is rearranged to obtain the following:

$$p_r(t) = R_1' \sin(\omega_o t - \varphi) + R_2' \sin(2\omega_o t - 2\varphi + \psi) \tag{4.99}$$

where

$$\begin{aligned} R_1' &= R_1 - \omega_o C_s V_{cs1}(V_{cd} + V_{cs}) \\ R_2' &= R_2 - 2\omega_o C_s V_{cs2}(V_{cd} + V_{cs}) \end{aligned} \tag{4.100}$$

Following a similar procedure, described for RSCFSI with EBC-PWM in Section 4.4, i_i for APDRSCFSI with EBC-PWM can be derived as follows:

$$i_i(t) = \left(\frac{4}{3+D}\right) \cdot \left[\frac{MI_o}{\sqrt{2}}\cos\varphi + \frac{R_1'}{V_c}\sin(\omega_o t - \varphi) + \frac{R_2'}{V_c}\sin(2\omega_o t - 2\varphi + \psi)\right]. \tag{4.101}$$

Therefore, (4.81), (4.83) and (4.101) are solved to obtain $\tilde{i}_L$, the low-frequency components of i_L, as follows:

$$\tilde{i}_L(t) = I_{L1}\sin(\omega_o t - \varphi) + I_{L2}\sin(2\omega_o t - 2\varphi + \psi) \tag{4.102}$$

where

$$\begin{aligned} I_{L1} &= \frac{R_1'(1-2D)}{V_c[(1-2D)^2 - \omega_o^2 LC]} \\ I_{L2} &= \frac{R_2'(1-2D)}{V_c[(1-2D)^2 - 4\omega_o^2 LC]} \end{aligned} \tag{4.103}$$

Similarly, (4.81), (4.83) (4.101) are solved to obtain $\tilde{v}_c$, the low-frequency components of v_c, as follows:

$$\tilde{v}_c(t) = V_{c1}\cos(\omega_o t - \varphi) + V_{c2}\cos(2\omega_o t - 2\varphi + \psi) \tag{4.104}$$

where

$$\begin{aligned} V_{c1} &= -\frac{4\omega_o L R_1'}{V_c[(1-3D)^2 - 4\omega_o^2 LC]} \\ V_{c2} &= -\frac{8\omega_o L R_2'}{V_c[(1-3D)^2 - 16\omega_o^2 LC]} \end{aligned} \tag{4.105}$$

It can be observed that R_1' and R_2' are significantly lower than R_1 and R_2, respectively. Thus, with the application of EBC-PWM, both $\tilde{i}_L$ and $\tilde{v}_c$ for APDRSCFSI are also significantly reduced, compared to RSCFSI.

4.5.2 Design of passive elements

The design of passive elements, described in Section 4.4.2, is extended for APDRSCFSI. The selection of C_s and L_{f2} involves consideration of both ω_o and $2\omega_o$ frequencies because the low-frequency ripple power contains both, according to (4.47). In order to make the low-frequency ripple of v_c completely zero, i.e., $V_{c1\text{-}2} = 0$, the required minimum values of C_s at different frequencies can be obtained from (4.54). Although the expression remains same, the estimated value changes because of the changed R_1'.

If C_s is designed to completely diminish $\tilde{v}_c$, the required C would be very small, as it is only required to mitigate high-frequency ripple. However, this results in a considerably large value of C_s. If both C and C_s are small enough, film capacitors can replace conventional electrolytic capacitors, significantly improving the lifetime and overall system reliability. So, the design goal is to lessen the amount of voltage ripple by a factor of k as given in (4.56). Hence, the respective capacitance requirements at ω_o and $2\omega_o$ can be derived from (4.57). Although the expression remains same as (4.57), the estimated value changes because of the changed R_1 owing to EBC-PWM.

The auxiliary capacitor C_s must be selected higher than both $C_{s\text{-}\omega_o}$ and $C_{s\text{-}2\omega_o}$. As both V_{cs} and its ripple $V_{cs1,2}$ are inversely proportional to C_s, greater V_{cs} or $V_{cs1,2}$ facilitates smaller C_s. Moreover, the dc-link capacitor C is only required to diminish the low-frequency ripples reduced by k, because rest of the ripple energy is now deflected to C_s. Therefore, the minimum capacitor requirements as obtained in (4.94) are modified as

$$\begin{aligned} C_{\omega_o} &\geq \frac{2R_1'}{\omega_o x V_c^2} + \frac{(1-3D)^2}{4\omega_o^2 L} \\ C_{2\omega_o} &\geq \frac{R_2'}{\omega_o x V_c^2} + \frac{(1-3D)^2}{16\omega_o^2 L} \end{aligned} \tag{4.106}$$

In order to mitigate both low-frequency and high-frequency ripple, the preferred C must be larger than all the values of capacitance acquired in (4.32) and (4.106).

Choosing k = 6, V_{cs} = 0.375 · V_c, V_{cs1}/V_{cs} = 0.16, both of C and C_s are selected as 220 µF. Therefore, C is reduced by a factor of 6 compared to RSCFSI.

After C is estimated, the procedure to select L, given in Section 4.4.2, is again performed as per the following:

$$\begin{aligned} y_{\omega_o} &= \frac{4R_1'(1-3D)}{[(1-3D)^2 - 4\omega_o^2 LC]V_o I_o \cos\varphi} \times 100\% \leq y \\ y_{2\omega_o} &= \frac{4R_2'(1-3D)}{[(1-3D)^2 - 16\omega_o^2 LC]V_o I_o \cos\varphi} \times 100\% \leq y \end{aligned} \tag{4.107}$$

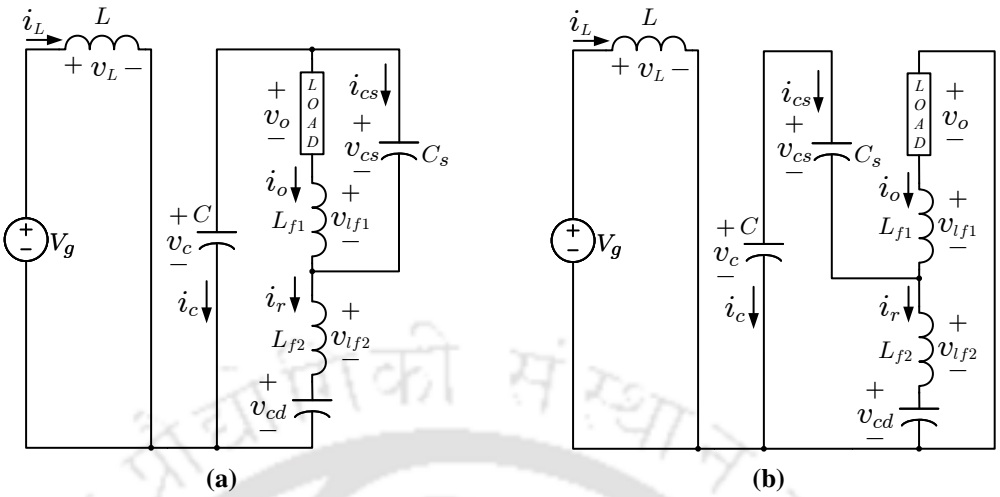


Fig. 4.6 Additional operational states of APDRSCFSI with EBC-PWM: (a) shoot-through state-2 and (b) shoot-through state-3.

Taking $y = 40\%$, L can be chosen as 1.5 mH, which indicates a reduction by approximately 46% compared to RSCFSI.

Since L_{f2} is not used as a ripple energy storage device, the ripple current i_r does not contain any dc part. Therefore, L_{f2} ought to be designed from (4.62) with a slight modification owing to changed value of V_{cd}. as follows:

$$L_{f2} \geq \max\left\{\frac{D_s T_s(V_c - V_{cs} - V_{cd})}{I_{\max} - \sqrt{2}I_o - I_{cs1}}, \frac{D_s T_s(V_c - V_{cs} - V_{cd})}{I_{\max} - I_{cs2}}\right\} \tag{4.108}$$

Choosing $I_{\max} = 6$ A, L_{f2} is selected as 2 mH.

As i_r is flowing through C_d in APDRSCFSI, the minimum requirement of C_d is also modified as follows:

$$C_d \geq \frac{4(\sqrt{2}I_o - \omega_o C_s V_{cs1})(1 - 3D)}{\omega_o x_d (1 + 3D) V_g} \tag{4.109}$$

Taking $x_d = 40\%$, C_d is selected as 220 μF, which shows a reduction by approximately 53% compared to RSCFSI.

4.5.3 Improvement of boundary condition of APDRSCFSI

In Table 3.1, different operational states of RSCFSI with EBC-PWM are given according to switching conditions of different active elements. Considering similar operational states

for APDRSCFSI with EBC-PWM, the equivalent circuit diagrams for each state are shown in Fig. 4.6. As explained in Section 3.4, the duration of the shoot-through state 1 is $D \cdot T_s$. Since the overall duration of both the shoot-through state 2 and the nonshoot-through state are $(1-D) \cdot T_s/2$, the duration of each of the states 2-5 is taken as $(1-D) \cdot T_s/4$. In each state, the voltage across the inductor L_{f2} is expressed as follows:

$$v_{Lf2}(t) = \begin{cases} -v_{cs}(t) - v_{cd}(t) + v_c(t); & \text{in shoot-through states 1-3} \\ -v_{cs}(t) - v_{cd}(t) + v_c(t); & \text{in nonshoot-through states 2, 3, 5} \\ -v_{cs}(t) - v_{cd}(t); & \text{in nonshoot-through state 4} \end{cases} \tag{4.110}$$

Using small ripple approximation, averaging (4.110) over T_s and using volt-second balance, one can obtain:

$$\langle v_{Lf2}(t) \rangle_{T_s} = \left(\frac{3+D}{4} \right) V_c - V_{cs} - V_{cd} = 0. \tag{4.111}$$

Since $V_{cd} = D_1 \cdot V_c$, according to (4.72), the average value of v_{cs} is determined as:

$$V_{cs} = \left(\frac{1-D}{2} \right) \cdot V_c. \tag{4.112}$$

which is same as (4.66), derived for SBC-PWM. Furthermore, it can be observed in several operational states shown in Fig. 4.6 that

$$v_o(t) + v_{Lf1}(t) = v_{cs}(t) \tag{4.113}$$

Using (4.1), (4.38), (4.39) in (4.113), while considering only fundamental component, the expression for the highest possible peak output voltage is obtained as follows:

$$\hat{v}_o = V_{cs} + V_{cs1} \sin\varphi - \sqrt{2}\omega_o L_{f1} I_o \sin\varphi \tag{4.114}$$

If the ac load is considered to be unity power factor, i.e., $\varphi = 0$, and $\varphi_1 \approx \varphi$, one can write

$$\hat{v}_o \approx V_{cs} = \left(\frac{1-D}{2}\right) \cdot V_c. \tag{4.115}$$

which is unchanged for both SBC-PWM and EBC-PWM. Hence, with both PWM strategies, the dc-ac gain of APDRSCFSI becomes

$$\frac{\hat{v}_o}{V_g} = \frac{MV_c}{V_g} \leq \left(\frac{1-D}{2}\right) \cdot \left(\frac{2}{1-3D}\right). \tag{4.116}$$

So, compared to the dc-ac gain of APDRSCFSI, with SBC-PWM, given in (4.71), the dc-ac gain of APDRSCFSI is improved.

4.6 COMPARISON OF APDRSCFSI WITH SBC-PWM AND EBC-PWM

In this section, the advantages of the operation of APDRSCFSI with EBC-PWM compared to SBC-PWM is illustrated in terms of dc-ac voltage gain and voltage stress.

The maximum possible output voltage $\hat{v}_o$ is established in (4.115), which can be combined with (3.56) and (3.75) to obtain

$$M = \frac{\hat{v}_o}{V_c} = \frac{1}{2} \cdot (1-D)|_{\text{EBC-PWM}} = \frac{4}{3} \cdot \frac{1}{2} \cdot (1-D)|_{\text{SBC-PWM}}. \tag{4.117}$$

Therefore, in the APDRSCFSI, for the same V_c, a 33.33% improvement in maximum possible $\hat{v}_o$ is achieved with EBC-PWM compared to SBC-PWM.

Based on (3.75), (3.56) and (4.116), the dc-ac voltage gain of RSCFSI is plotted vs. the variation of D in Fig. 4.7. It can be observed that there is a significant reduction in dc-ac gain of APDRSCFSI compared to the RSCFSI, when EBC-PWM is used. However, as shown in (4.53), the input inductor current ripple of APDRSCFSI is reduced, which also diminishes input inductor L requirement, resulting in a reduced parasitic resistance r_l. In Fig. 4.7, r_l = 0.22 Ω for RSCFSI as L = 2.75 mH. In APDRSCFSI, L can be reduced to 1.5 mH,

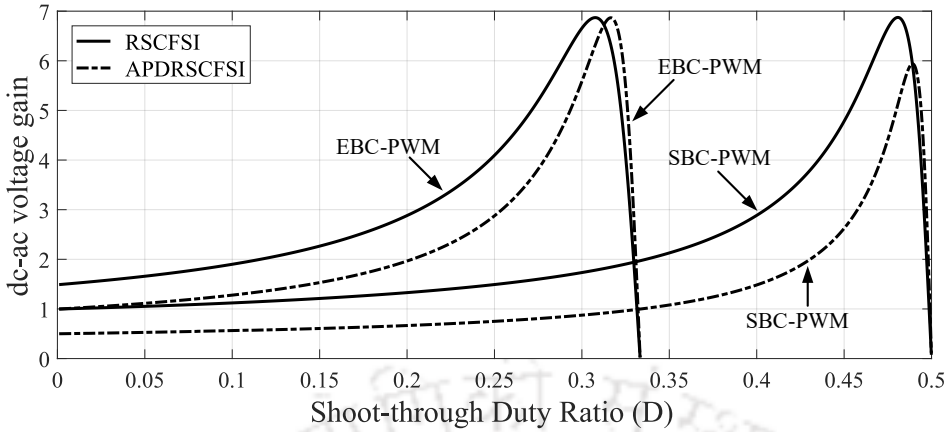


Fig. 4.7 Comparison of dc-ac gain vs. shoot-through duty ratio of APDRSCFSI with SBC-PWM and EBC-PWM.

Table 4.2 Quantitative comparison of parameters of APDRSCFSI with SBC-PWM and EBC-PWM

	APDRSCFSI	
PWM strategies →	**SBC-PWM**	**EBC-PWM**
Shoot-through duty ratio, D	0.4545	0.25
Modulation index, M	0.278	0.375
Boost Factor, B_F	11	8
Avg. dc-link capacitor voltage, V_c (V)	440	320
Voltage Stress (V) across $S_{1\text{-}4}$, $D_{a\text{-}b}$	440	320
Avg. offset capacitor voltage, V_{cd} (V)	200	140

which reduces r_l to 0.15 Ω. Therefore, APDRSCFSI can still achieve approximately similar maximum dc-ac gain, compared to RSCFSI.

It is also observed that the APDRSCFSI with EBC-PWM can achieve better maximum dc-ac gain than APDRSCFSI with SBC-PWM as shown in Fig. 4.7. Also, APDRSCFSI with EBC-PWM can obtain similar maximum dc-ac gain compared to RSCFSI with SBC-PWM because of smaller r_l.

A quantitative comparison of APDRSCFSI with both PWM strategies are shown in Table 4.2. The inverter specifications given in Table 4.1 are used for the quantitative analysis. The values of D are calculated to maintain a peak output voltage of 120 V for a input voltage of 40 V, indicating a dc-ac gain of three.

From Table 4.2, it is observed that all parameters except D remain the same for RSCFSI whether SBC-PWM or EBC-PWM is applied. In comparison, APDRSCFSI with SBC-PWM

Table 4.3 Parameters and component values for simulation

Parameter/Component	Attributes
Input voltage (V_g)	40 V
Shoot-through duty ratio (D)	0.25
Peak value of output voltage ($\hat{v}_o$)	120 V
Fundamental frequency (f_o)	50 Hz
Inverter switching frequency (f_s)	10 kHz
Input inductor (L)	2.75 mH
DC-link capacitor (C)	220 µF
Bleeding resistance (R_d)	10 kΩ
APDRSCFSI filter inductors ($L_{f1,2}/R_{lf1,2}$)	2 mH / 0.5 Ω
APDRSCFSI auxiliary capacitor (C_s)	220 µF
APDRSCFSI offset capacitor (C_d)	220 µF
AC load (R_o)	40 Ω
Output filter capacitor (C_f)	10 µF

requires higher V_c to achieve the same dc-ac gain, which needs higher D to obtain a higher B_F. When EBC-PWM is applied, V_c can be reduced, owing to reduced B_F. Because of reduced V_c, the voltage stress across the switches and diodes is also reduced by 27.3%. Note that V_{cd} is also reduced by 30% owing to smaller D required with EBC-PWM.

The theoretical analysis is verified with simulation results as shown in Fig. 4.8. The dc-link capacitor voltage v_c, offset capacitor voltage v_{cd}, auxiliary capacitor voltage v_{cs}, output voltage v_o and output current i_o are plotted for APDRSCFSI with SBC-PWM and EBC-PWM in Fig. 4.8(a) and 4.8(b), respectively. The simulation parameters are given in Table 4.3. In both cases, the input voltage V_g is taken as 40 V; the peak of the output voltage is considered to be 120 V, and the peak of the output current is reckoned as 3 A while the load resistance is 40 Ω. With SBC-PWM, the average dc-link required is 458 V, which reduces to 323 V with EBC-PWM. Therefore, to achieve same dc-ac voltage gain, when the APDRSCFSI is operated with SBC-PWM and EBC-PWM, the APDRSCFSI is expected to lower dc-link voltage with EBC-PWM. Thus, the voltage stress across the switches and the diodes are less with EBC-PWM, which is consistent with the theoretical comparison given in Table 4.2. Also, a lower dc-link voltage owing to EBC-PWM reduces the offset capacitor voltage v_{cd}. With both SBC-PWM and EBC-PWM, the average value of v_{cs} is observed to be 125 V, as seen in Fig. 4.8(a) and 4.8(b), respectively, which also verifies (4.66) and (4.112). The average

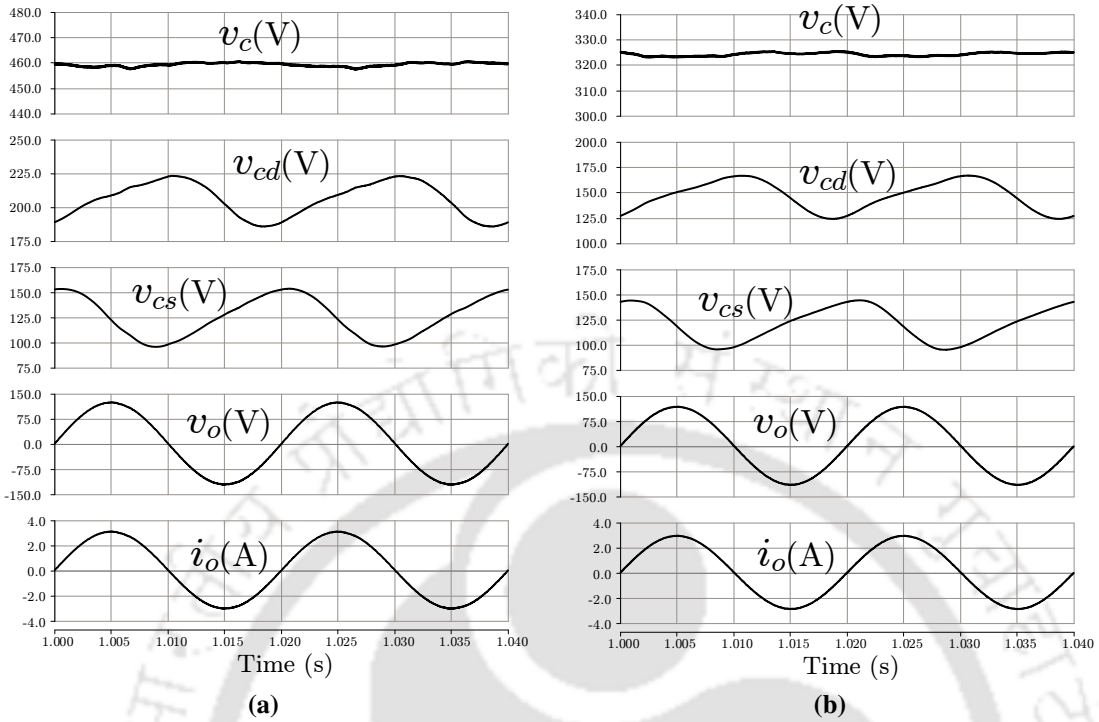


Fig. 4.8 Simulation results of APDRSCFSI: (a) with SBC-PWM and (b) with EBC-PWM.

value of v_{cd} is observed to be 205 V with SBC-PWM and 145 V with EBC-PWM, as seen in Fig. 4.8(a) and 4.8(b), respectively. Thus, the voltage stress across the offset capacitor C_d is reduced with EBC-PWM.

In this section, a comparison of APDRSCFSI with SBC-PWM and EBC-PWM is presented. As a conclusion, it can reckoned that the EBC-PWM is more advantageous compared to SBC-PWM. Following this study, in the implementation of the closed-loop control and in the hardware prototype, the EBC-PWM is applied to APDRSCFSI.

4.7 CLOSED-LOOP CONTROL TECHNIQUE

Fig. 4.10 shows the schematic diagram of the complete closed-loop control technique, which involves a total of three controllers and one ripple extractor. As RSCFSI is chosen to operate in standalone mode, the closed-loop control technique's objectives are to maintain the reference output voltage and facilitate deflection of the low-frequency ripple energy. The additional fundamental frequency ripple poses more difficulty, which is solved using resonant

controllers. Two controllers are utilized to maintain the output voltage and current, where the output voltage controller operates in the external loop and the output current controller functions in the internal loop. In order to compensate for the low-frequency ripple, a separate current controller is employed to follow the reference ripple current after extraction of the voltage ripple from the dc-link capacitor voltage. In APDRSCFSI, the amount of the low-frequency ripple in the active-front-end network parameters are reduced with the help of the APD functionality, which facilitates the use of smaller passive elements. As a result, the bandwidth of APDRSCFSI is improved, as shown in Fig. 4.9.

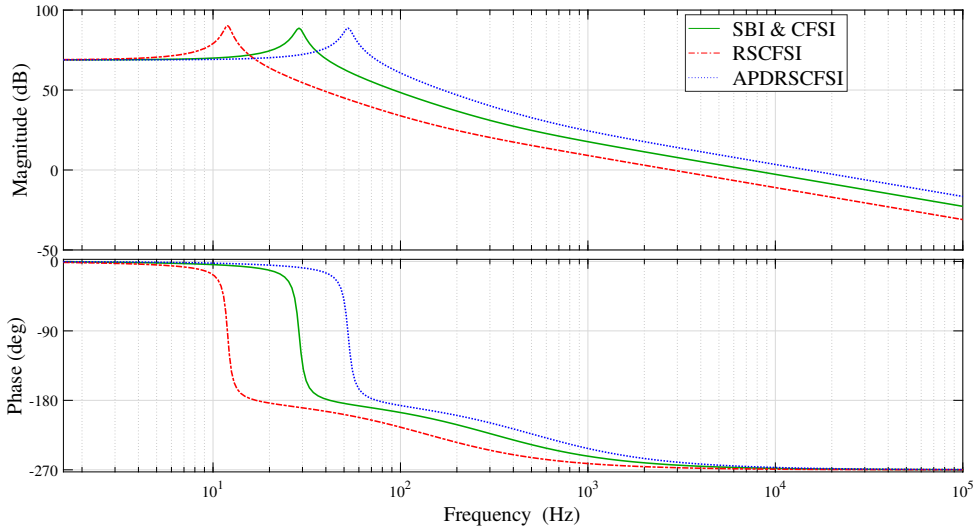


Fig. 4.9 The control to output response of SBI, CFSI, RSCFSI and APDRSCFSI

4.7.1 Output voltage controller

Due to its precise tracking performance, the proportional-resonant (PR) controller is preferred as the output voltage controller. As shown in Fig. 4.10, the PR controller $G_{PR1}(s)$ should regulate v_o to follow its reference v_o^*. The resonant part of the controller contains only the fundamental frequency so that the overall transfer function becomes:

$$G_{PR1}(s) = K_{p1} + K_{r1}\frac{2\xi\omega_o s}{s^2 + 2\xi\omega_o s + \omega_o^2} \tag{4.118}$$

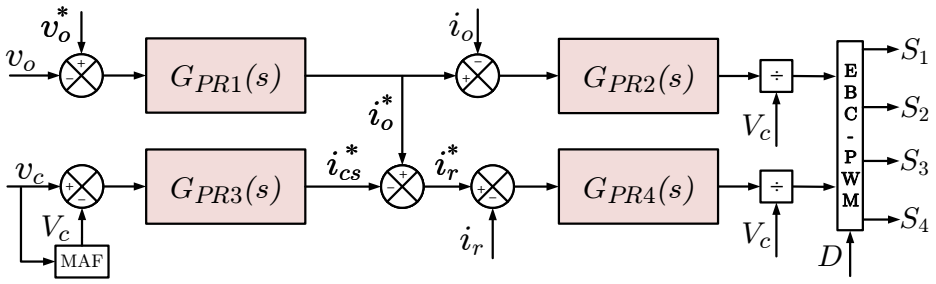


Fig. 4.10 Schematic diagram of the closed-loop control technique for APDRSCFSI.

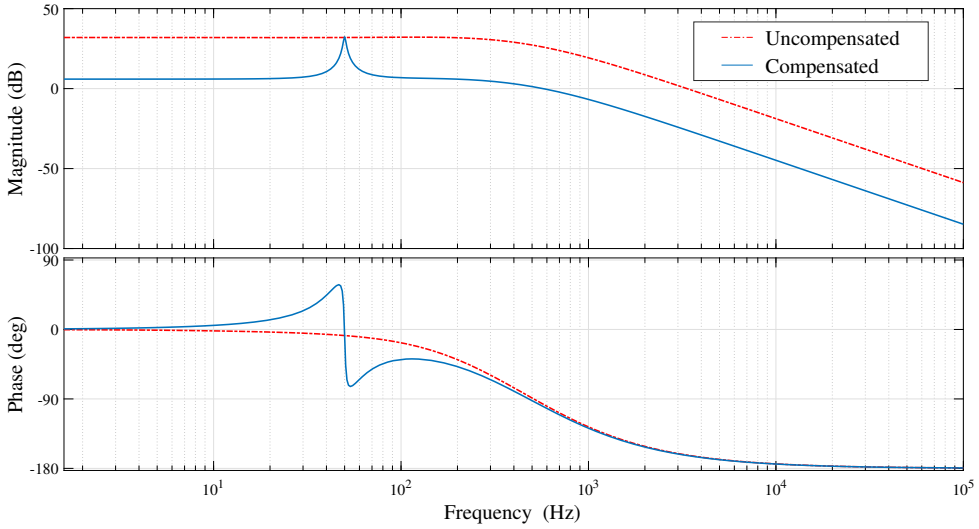


Fig. 4.11 Bode diagram of output voltage control loop.

where K_{p1} and K_{r1} are the output voltage controller parameters; ξ is the damping factor and can be chosen as between 0.01 and 0.02 [100]. The transfer function of the external voltage loop, from v_o to i_o, is given by

$$G_{vi}(s) = \frac{v_o(s)}{i_o(s)} = \frac{R_o}{sR_oC_f + 1} \tag{4.119}$$

where C_f is the filter capacitor attached across the ac load resistor R_o.

With K_{p1} = 0.05 and K_{r1} = 1.0, the compensated bode diagram is shown in Fig. 4.11. In order to maintain steady-state error close to zero, the PR controllers must have high gain at the desired (in this case, fundamental) frequency of 50 Hz, and the gain crossover frequency (f_c) has to be more than half a decade separated from the switching frequency f_s so that enough attenuation can be achieved at f_s. It is found the phase margin is 80^o, and f_c is 572 Hz, which

is more than a decade separated from f_s of 10 kHz. A gain of 32 dB is achieved at 50 Hz, and an attenuation of 45 dB is observed at f_s.

4.7.2 Output current controller

The voltage across L_{f1} is expressed as:

$$v_{Lf1}(t) = L_{f1}\frac{di_o(t)}{dt} = -s_a v_c(t) + v_{cs}(t) - v_o(t). \tag{4.120}$$

where s_a is the phase-a leg switching states. When switch S_4 is on, $s_a = 1$ and $\frac{di_o(t)}{dt} < 0$ and vice versa. So, the output current i_o has a monotonic relationship with s_a. Thus, i_o can be controlled when the phase-a leg switches are regulated via the control variable v_{Lf1}.

The reference for i_o is obtained from the output voltage controller as i_o^*. As shown in Fig. 4.10, another PR controller $G_{PR2}(s)$, where the resonant part of the controller contains only the fundamental frequency similar to the voltage controller, is employed for the regulation of i_o as follows:

$$G_{PR2}(s) = K_{p2} + K_{r2}\frac{2\xi\omega_o s}{s^2 + 2\xi\omega_o s + \omega_o^2}. \tag{4.121}$$

where K_{p2} and K_{r2} are the output current controller parameters. Considering the parasitic resistance of L_{f1} as r_{lf1}, the transfer function of the internal current control loop is:

$$G_{io}(s) = \frac{v_{Lf1}(s)}{i_o(s)} = \frac{1}{sL_{f1} + r_{lf1}}. \tag{4.122}$$

With K_{p2} = 20 and K_{r2} = 2000, the compensated bode diagram is shown in Fig. 4.12. The phase margin is 80^o, and crossover frequency is 815 Hz, which is more than a decade separated from the switching frequency of 10 kHz. A gain of 64 dB is observed at the fundamental frequency, and an attenuation of 22 dB is achieved at the switching frequency.

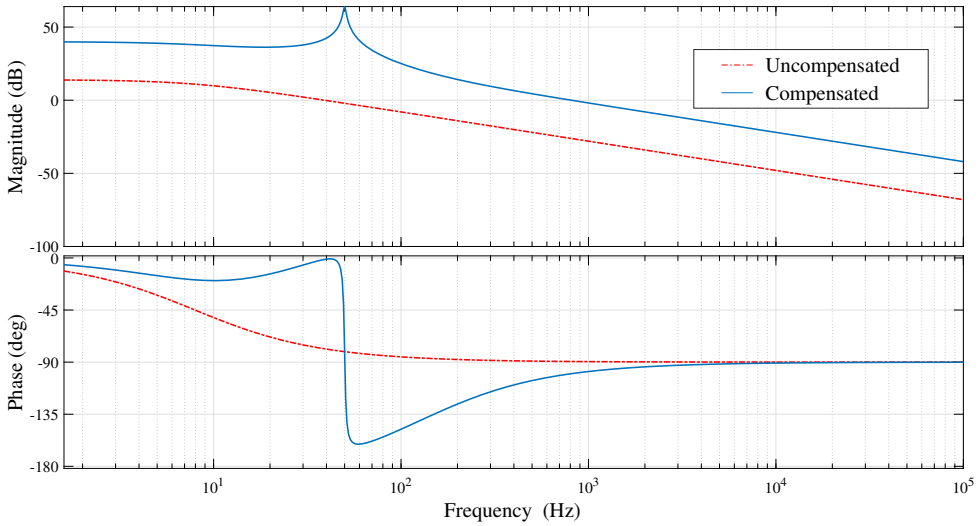


Fig. 4.12 Bode diagram of output current control loop.

4.7.3 Low-frequency ripple extraction

As the auxiliary capacitor C_s stores the low-frequency ripple energy, the capacitor current, i_{cs}, must be regulated to compensate for the low-frequency ripple of C. As shown in Fig. 4.10, the low-frequency ripple extraction includes a moving average filter (MAF), which generates the dc value V_c from the measured value of v_c. The complete harmonic content is obtained when V_c is subtracted from v_c. Since fundamental and second harmonic frequencies are the dominant harmonics, for precise extraction, another PR controller $G_{PR3}(s)$ is used, as indicated in Fig. 4.10, and its transfer function is:

$$G_{PR3}(s) = K_{p3} + \sum_{n=1,2} K_{r3n} \frac{2\xi n\omega_o s}{s^2 + 2\xi n\omega_o s + (n\omega)^2}. \tag{4.123}$$

where K_{p3} and K_{r3n} are the controller parameters. Assuming the turn on duration of S_2 is $D_s \cdot T_s$, the transfer function from v_c to i_r is obtained as:

$$G_{vr}(s) = \frac{v_c(s)}{i_r(s)} = \frac{D_s R_d}{sR_dC + 1}. \tag{4.124}$$

where R_d is the bleeding resistance connected across the dc-link capacitor C.

4.7.4 Ripple current controller

As i_o and i_r are regulated through a-phase and b-phase switching legs, respectively, i_{cs} is controlled indirectly. The reference i_{cs}^* generated by the ripple extraction block. The reference of the ripple current i_r is generated from i_{cs}^*. As shown in Fig. 4.10, the relationship among i_{cs}, i_o and i_r is utilized for the reference as follows

$$i_r^*(t) = i_o^*(t) + i_{cs}^*(t). \tag{4.125}$$

Similar to i_o and s_a, there exists a monotonic relationship between i_r and phase-b leg switching states (s_b) as follows

$$v_{Lf2}(t) = L_{f2}\frac{di_r(t)}{dt} = s_b v_c(t) - v_{cs}(t) - v_{cd}(t). \tag{4.126}$$

According to (4.126), when switch S_2 is on, s_b = 1 and $\frac{di_r(t)}{dt} > 0$ and vice versa. Therefore, i_r can be regulated by controlling the phase-b leg switches. Since i_r^* contains both fundamental and second harmonic frequencies, the chosen PR controller $G_{PR4}(s)$, as indicated in Fig. 4.10, should provide high gain at those frequencies, as follows:

$$G_{PR4}(s) = K_{p4} + \sum_{n=1,2} K_{r4n} \cdot \frac{2\xi n\omega_o s}{s^2 + 2\xi n\omega_o s + (n\omega)^2}. \tag{4.127}$$

where K_{p4} and K_{r4n} are the ripple current controller parameters. Considering the parasitic resistance of L_{f2} as r_{lf2}, the transfer function from i_r to v_{Lf2} is given by:

$$G_{ir}(s) = \frac{v_{Lf2}(s)}{i_r(s)} = \frac{1}{sL_{f2} + r_{lf2}}. \tag{4.128}$$

With K_{p4} = 12, K_{r41} = 2000 and K_{r42} = 200, the compensated bode diagram is shown in Fig. 4.13. The phase margin is 76°, and crossover frequency is 990 Hz, which is a decade separated from the switching frequency of 10 kHz. A gain of 67 dB is observed at the

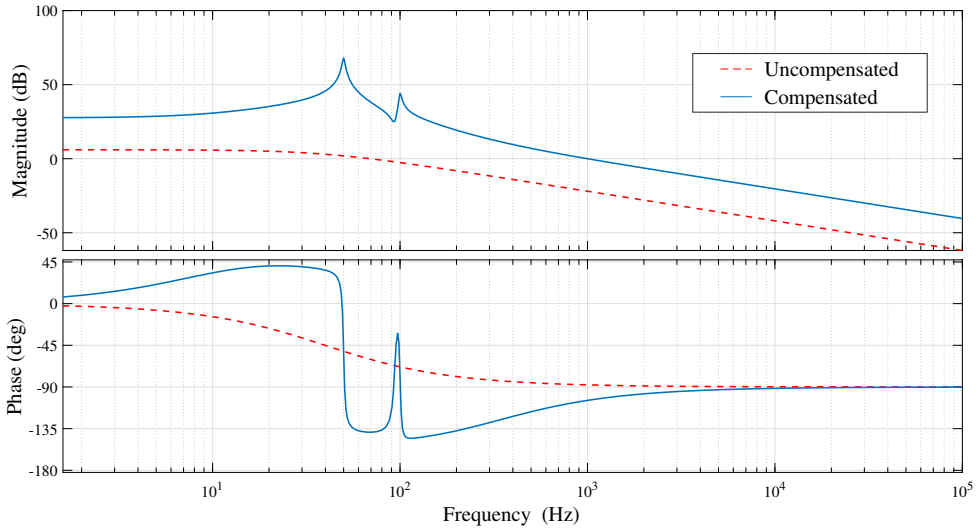


Fig. 4.13 Bode diagram of ripple current control loop.

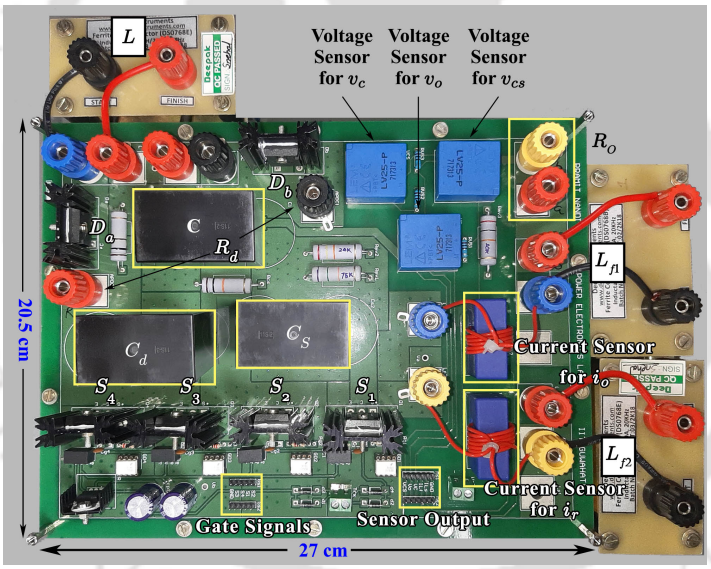


Fig. 4.14 Hardware prototype of APDRSCFSI.

fundamental frequency; a gain of 45 dB is obtained at the second harmonic frequency, and an attenuation of 21 dB is achieved at the switching frequency.

4.8 EXPERIMENTAL RESULTS

The hardware prototype of single-phase APDRSCFSI has been built to perform experimental verification. Fig. 4.14 shows the photograph of the hardware prototype. Table 4.3 lists the parameters and component values are given, which are used to perform the experiments.

Table 4.4 Components used in hardware setup

Component	Part No. and Manufacturer
S_1, S_2, S_3, S_4	IRG7PH42UDPBF (International Rectifier)
D_a, D_b	DSEI60-06A (IXYS)
Gate Driver	FOD3180 (Fairchild)
Inductor Core	E 100/60/28 (EPCOS)
Voltage Transducer	LV 25-P (LEM)
Current Transducer	LA 55-P (LEM)

The input dc voltage V_g is 40 V. The reference output voltage v_o^* is a 50 Hz sinusoidal signal, and its peak is 120 V in order to achieve a dc-ac gain of three. The system operation with an ac load of 40 Ω is verified. Rest of the parameters are mentioned in Table 4.3. Although L can be reduced to 1.5 mH as mentioned in Subsection 4.4.2, due to the unavailability of a 1.5mH inductor, it is taken as 2.75 mH for APDRSCFSI, same as RSCFSI. Note that the output filter inductor L_f is 4 mH for RSCFSI, which is split into two filter inductors as L_{f1} = L_{f2} = 2 mH for APDRSCFSI. Because EBC-PWM is the superior PWM strategy than SBC-PWM, as discussed in Section 4.6, it is used in the hardware implementation of APDRSCFSI. The EBC-PWM strategy and the closed-loop control of APDRSCFSI are implemented in DSP [102]. The components used in the hardware setup are listed in Table 4.4.

4.8.1 Steady-state performance of RSCFSI without APD

Fig. 4.15 shows the experimental results for the steady-state performance of RSCFSI without APD. Fig. 4.15(a) and (b) demonstrates the waveforms of input voltage V_g, dc-link capacitor voltage v_c and its low-frequency ripple $\tilde{v}_c$, and input inductor current i_L. In Fig. 4.15(a), C = 220 µF and L = 5.5 mH. In Fig. 4.15(a), C = 1160 µF and L = 2.75 mH. As observed in Fig. 4.15(a) and (b), the input voltage V_g is 40 V, and the dc-link capacitor voltage v_c has an average of approximately 290 V, achieving a boost factor B_F of 7.25. According to (3.64), B_F should be 8. The drop in B_F is observed due to non-idealities present in the circuit. For RSCFSI, the peak-to-peak low-frequency voltage ripple $\tilde{v}_c$ is observed to be 40 V in Fig. 4.15(a) and 8 V in Fig. 4.15(a), respectively, which verifies (4.86). Note that the dc-link capacitor requirement of 1160 µF is fulfilled by electrolytic capacitors. In Fig. 4.15(b),

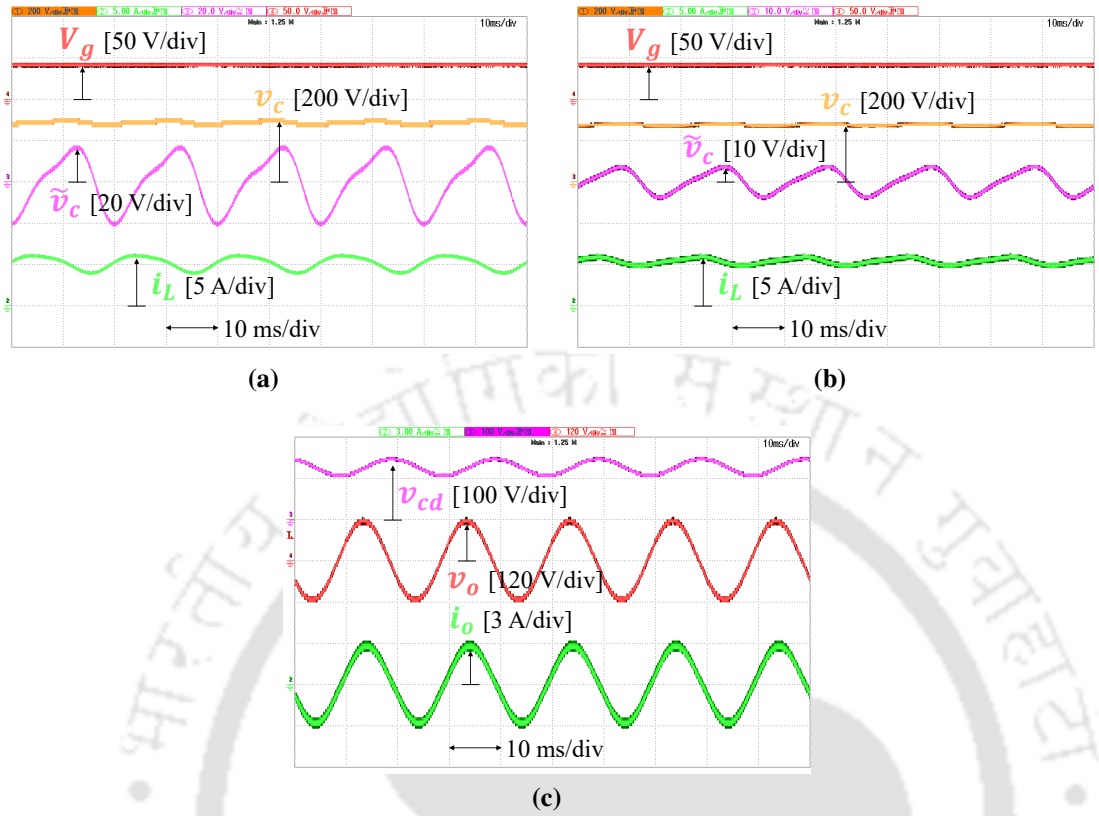


Fig. 4.15 Steady-state performance of the RSCFSI using EBC-PWM: (a) with C = 220 µF, L = 5.5 mH, (b) with C = 1160 µF, L = 2.75 mH. Input voltage (V_g), dc-link capacitor voltage (v_c) and its ripple ($\tilde{v}_c$), input inductor current (i_L) and (c) offset capacitor voltage (v_{cd}), output voltage (v_o), output current (i_o).

it is also noticed that the inductor current i_L has an average of 5 A, which matches (3.66). The peak-to-peak low-frequency ripple of i_L is found to be 2.6 A in Fig. 4.15(a) and 2 A in Fig. 4.15(b), which is in accordance with (4.84).

Fig. 4.15(c) illustrates the waveforms of output voltage v_o, output current i_o and offset capacitor voltage v_{cd}. It is observed that v_o accurately tracks the reference v_o^*, and its peak $\hat{v}_o$ is 120 V. Since the ac load R_o is 40 Ω, the output current i_o has a peak of 3 A, which indicates the output power P_o is 180 W. In Fig. 4.15(c), it is also observed that the average of v_{cd} is 125 V, which verifies (4.72). Since i_o is flowing through C_d, a capacitor of 470 µF is used as C_d. Thus, a peak-to-peak low-frequency voltage ripple of 50 V is observed in v_{cd}, which is in agreement with (4.72).

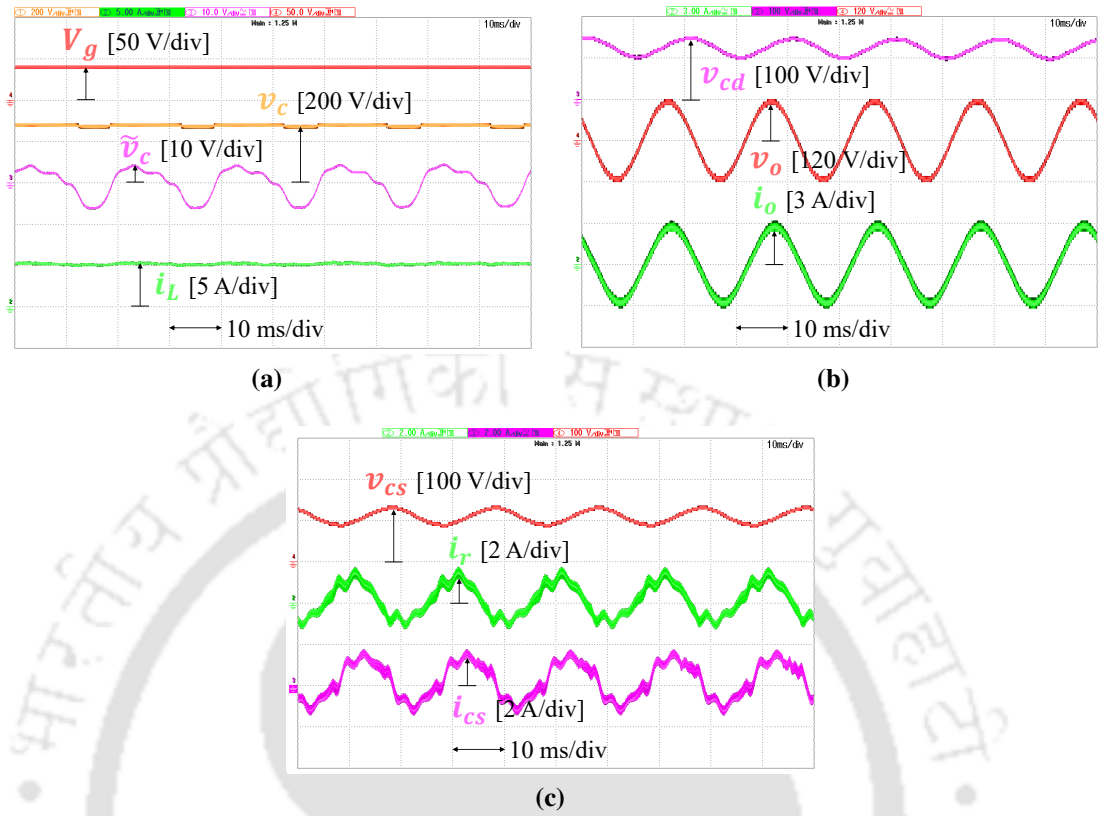


Fig. 4.16 Steady-state performance of the APDRSCFSI using EBC-PWM with C = 1160 µF, L = 2.75 mH: (a) Input voltage (V_g), dc-link capacitor voltage (v_c) and its ripple ($\tilde{v}_c$), input inductor current (i_L), (b) offset capacitor voltage (v_{cd}), output voltage (v_o), output current (i_o) and (c) auxiliary capacitor voltage and current (v_{cs}, i_{cs}), ripple current (i_r).

4.8.2 Steady-state performance of APDRSCFSI

The steady-state performance of the RSCFSI with APD, i.e., APDRSCFSI, is illustrated in Fig. 4.16. Fig. 4.16(a) presents the waveforms of input voltage V_g, dc-link capacitor voltage v_c and its low-frequency ripple $\tilde{v}_c$, and input inductor current i_L. Similar to RSCFSI, V_g is kept at 40 V; V_c remains at 290 V, and I_L is measured to be 5 A. In APDRSCFSI, a film capacitor of 220 µF is employed as the dc-link capacitor. The peak-to-peak low-frequency voltage ripple $\tilde{v}_c$ is 10 V, which is similar to that of RSCFSI, and is consistent with (4.104). Thus, the dc-link capacitor requirement is downsized by six compared to RSCFSI. In Fig. 4.16(a), it is also noted that the peak-to-peak low-frequency ripple of i_L is reduced significantly to 0.67 A, indicating a reduction by a factor of three, which also matches with (4.104).

Table 4.5 Comparison of low-frequency ripples

	RSCFSI without APD		**APDRSCFSI**
Fig. No.	4.15(a)	4.15(b)	4.16
DC-link capacitor C	220 µF	1160 µF	220 µF
Offset capacitor C_d	470 µF	470 µF	220 µF
Input inductor L	5.5 mH	2.75 mH	2.75 mH
Peak-to-peak ripple in v_c	40 V	8 V	8 V
Peak-to-peak ripple in i_L	2.6 A	2 A	0.6 A
Peak-to-peak ripple in v_{cd}	50 V	50 V	50 V

Fig. 4.16(b) demonstrates the waveforms of output voltage v_o, output current i_o and offset capacitor voltage v_{cd}. In Fig. 4.16(b), v_o is observed to be meticulously following the reference v_o^*, and its peak $\hat{v}_o$ is 120 V. Similar to RSCFSI, the peak of i_o is 3 A, and P_o is 180 W, as R_o is 40 Ω. Fig. 4.16(b) also shows that V_{cd} is 125 V, which is similar to that of RSCFSI. As shown in Fig. 4.16(b), the peak-to-peak low-frequency ripple of v_{cd} remains unchanged at 50 V, which is same as that of RSCFSI and is consistent with (4.97).

Fig. 4.16(c) illustrates the waveforms of auxiliary capacitor voltage v_{cs}, auxiliary capacitor current i_{cs} and ripple current i_r. As shown in Fig. 4.16(c), the average value of v_{cs} is around 110 V, which verifies (4.112) and (4.114). Also, the peak value of both i_{cs} and i_r are found to be around 1.5 A.

As shown in Fig. 4.3, the ripple current i_r flows through C_d. In Fig. 4.16(c), the peak value of i_r is found to be around 1.5 A, which clearly indicates i_r is less than i_o, in line with (4.41). Owing to smaller i_r, C_d is reduced to 220 µF facilitating use of a film capacitor. This indicates a 53% reduction of C_d compared to RSCFSI. Table 4.5 presents the low-frequency ripples in v_c, i_L and v_{cd} for single-phase RSCFSI with and without APD.

4.8.3 Transient performance of APDRSCFSI

In Fig. 4.17, the transient performance of APDRSCFSI is demonstrated, where the waveforms of dc-link capacitor voltage v_c, input inductor current i_L, output voltage v_o and output current i_o are presented. Note that $\hat{v}_o$ is maintained at 150 V. At first, the ac load R_o is reduced from 72 Ω to 36 Ω so that the peak magnitude of i_o is stepped up from 3.75 A to 7.5 A. It is observed that both transitions in load display acceptable transient responses. Note that

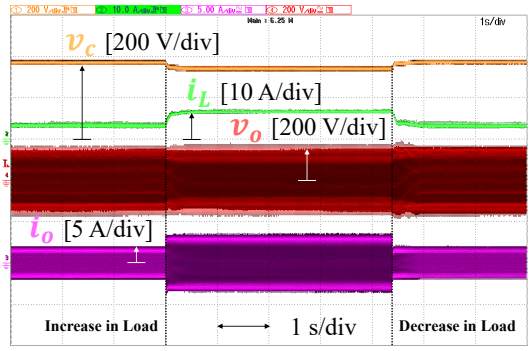


Fig. 4.17 Transient performance of the APDRSCFSI using EBC-PWM: dc-link capacitor voltage (v_c), input inductor current (i_L), output voltage (v_o) and output current (i_o).

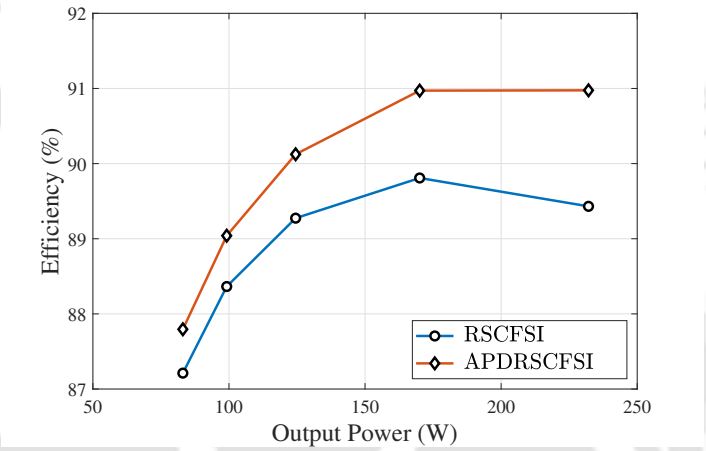


Fig. 4.18 Comparison of measured efficiencies of RSCFSI and APDRSCFSI.

although both v_c and i_L are not controlled, they are included in Fig. 4.17 to show changes on the input side when a change in load occurs.

4.8.4 Comparison of measured efficiencies

The measured efficiencies of RSCFSI and APDRSCFSI at different output powers are plotted in Fig. 4.18. The efficiency of RSCFSI is measured with C = 1160 µF. An improvement in efficiency is observed with APDRSCFSI operation with 220 µF compared to RSCFSI operation with 1160 µF because losses are reduced in C_d and L_{f2} as well as the switches S_3 and S_4 due to reduction in current i_r as explained previously in Section 4.3. Moreover, use of film capacitors in APDRSCFSI has helped reduce losses further.

4.9 SUMMARY

In this chapter, the low-frequency ripple of the single-phase RSCFSI is analyzed, and based on the analysis, a selection procedure for the passive elements of the active-front-end network of the RSCFSI is formulated. Similar to the single-phase SBI, the RSCFSI requires significantly large passive elements to mitigate the low-frequency ripples, which hampers power density and overall system reliability. As a solution to the low-frequency ripple problem of RSCFSI, this chapter further presents the APD-integrated RSCFSI, which reduces dc-link capacitor requirement by six when compared to the RSCFSI. The input inductor ripple is reduced by a factor of three, and the required offset capacitor is also halved. One of the drawbacks of the APDRSCFSI is the reduction of the dc-ac gain, which is improved because of the EBC-PWM switching strategy. As a result, the peak output voltage is improved by 33%, and the voltage stress across the switches and diodes is reduced by 27.3%, compared to when the SBC-PWM strategy is employed. This work also elucidates a closed-loop control technique for the APDRSCFSI that maintains the output voltage as well as facilitates the APD functionality. The APDRSCFSI is implemented in hardware, and the experimental results demonstrate steady-state and transient responses that validate the analysis.

CHAPTER 5

CONCLUDING REMARKS AND FUTURE SCOPE OF RESEARCH

5.1 CONCLUDING REMARKS

In this thesis, the low-frequency ripple analysis of the single-phase SBI is performed, and a procedure to design suitable capacitance and inductance for the active-front-end network is formulated to achieve minimization of the low-frequency ripple. The low-frequency ripple analysis is validated with the help of a hardware prototype.

This thesis also derives an APD-integrated single-phase SBI so that low-frequency ripple can be mitigated and overall system lifetime can be improved. A comparison between single-phase SBI and APD-integrated SBI is presented to show the advantages of the APD integration. The APD-integrated SBI is verified in hardware.

This thesis has derived another AFE-ISI topology, named RSCFSI, achieving better voltage gain, continuous input current and better efficiency than SBI. The proposed topology is compared with existing AFE-ISIs. Two PWM strategies, namely SBC-PWM and EBC-PWM, are proposed for the derived topology. With SBC-PWM, the RSCFSI can achieve more voltage gain than SBI and same voltage gain as CFSI. The voltage gain of RSCFSI can be improved further with EBC-PWM. With the help of a hardware prototype, the operating principle of RSCFSI and the proposed PWM strategies are validated.

This thesis has also extended the low-frequency ripple analysis of the proposed RSCFSI, and a procedure to design suitable capacitance and inductance for the active-front-end network is formulated to achieve minimization of the low-frequency ripple. The analysis and the procedure are validated in hardware.

The thesis has further proposed APDRSCFSI, which mitigates low-frequency ripple and improves overall system lifetime. A comparison between RSCFSI and APDRSCFSI has been carried out. The APDRSCFSI has been verified in hardware.

The detailed conclusions drawn from the individual chapters are given below.

In **Chapter 2**, the steady-state analysis of the single-phase SBI is presented, and the low-frequency ripple problem of the single-phase SBI is illustrated. Based on the low-frequency ripple analysis, the passive elements of the active-front-end network of the SBI are designed, which reveals significantly large passive elements are required to restrict the low-frequency ripple. As a solution, the single-phase SBI is integrated with three independent APD networks, viz., buck, boost and buck-boost, in order to transfer low-frequency power ripple directly from the ac load to an auxiliary capacitor. A low-frequency ripple analysis of the overall system has been carried out and it is observed that significantly less ripple on the capacitor voltage and the inductor current of the active-front-end network has been achieved with the additional APD topology reducing both capacitor and inductor requirement. Based on the analysis, a design procedure for the passive elements of active-front-end network and APD topology has been presented. A comparison between three APD networks suggests the boost-type APD network is the most suitable for integration with single-phase SBI. Hence, the boost-type APD-integrated SBI is chosen for hardware implementation. Compared to SBI, a reduction of 82.5% in capacitor requirement in the active-front-end network and a reduction of 45% in overall capacitor requirement have been achieved in APD-integrated SBI. A closed loop control strategy for accurate low-frequency ripple mitigation has been presented. The proportional-resonant (PR) is chosen as the current controller as very low steady-state error has been observed for PR while tracking reference ripple current. The parameters of the PR controller have been chosen based on the small-signal analysis of the APD topology. The system is fabricated in hardware and the presented experimental results for steady-state operation and transient performance of the system due to ac load change are consistent with the analysis.

In **Chapter 3**, the single-phase RSCFSI is derived from complimentary current-fed topology, and the steady-state analysis of the RSCFSI is presented. The implementation of the SBC-PWM strategy is illustrated, for which the RSCFSI can achieve same boost factor as the CFSI. To improve the proposed inverter's boost factor for same shoot-through duty

ratio, the EBC-PWM strategy is proposed. A comparison of the RSCFSI with SBI and CFSI is also demonstrated in this chapter, which shows the RSCFSI requires lower total device rating (TDR) and achieves better efficiency among the three inverters. A closed-loop control strategy is also illustrated for the RSCFSI to control the output voltage and the dc-link voltage. The proposed inverter is fabricated in hardware, and the presented experimental results for steady-state operation and transient performance of the inverter due to ac load change are consistent with the analysis.

In **Chapter 4**, the low-frequency ripple of the single-phase RSCFSI is analyzed, and based on the analysis, a selection procedure for the passive elements of the active-front-end network of the RSCFSI is formulated. Similar to the single-phase SBI, the RSCFSI requires significantly large passive elements to restrict the low-frequency ripples, which hampers power density and overall system reliability. As a solution to the low-frequency ripple problem of RSCFSI, this chapter further presents the APD-integrated RSCFSI (APDRSCFSI), which reduces dc-link capacitor requirement by six when compared to the RSCFSI. The input inductor ripple is reduced by a factor of three, and the required offset capacitor is also halved. One of the drawbacks of the APDRSCFSI is the reduction of the dc-ac gain, which is improved because of the EBC-PWM switching strategy. As a result, the peak output voltage is improved by 33%, and the voltage stress across the switches and diodes is reduced by 27.3%, compared to when the SBC-PWM strategy is employed. This chapter also elucidates a closed-loop control technique for the APDRSCFSI that maintains the output voltage as well as facilitates the APD functionality. The APDRSCFSI is implemented in hardware, and the experimental results demonstrate steady-state and transient responses that validate the analysis.

5.2 FUTURE SCOPE OF RESEARCH

The work presented in this thesis can be further extended in the future. Some of the future scopes of research that can be further explored from this thesis are given as follows:

(1) The three-phase RSCFSI can be conceptualized from the single-phase RSCFSI.

(2) The RSCFSI can be utilized in a grid-connected system with solar energy or other renewable energy sources, which should be further researched.

(3) The presence of the offset capacitor in RSCFSI adds a fundamental component to the low-frequency ripple problem. The removal of this capacitor without hampering the basic functionality of the inverter can be explored.

(4) The gain of RSCFSI is limited, which can be increased further using additional power electronics. Also, the APDRSCFSI's limited output voltage can be improved using other APD topologies, which can be explored in the future.

(5) The non-zero discontinuous current mode (NZ-DCM) is one of the issues that exist in AFE-ISIs, when the inverters are operated at a low boost factor to achieve a high modulation index. It remains unexplored in RSCFSI, which is one of the future works.

(6) The zero voltage switching is an attractive solution explored in literature, which can improve efficiency. However, it is not explored for RSCFSI, which can be further researched in the future.

LIST OF PUBLICATIONS

Journals

1. **Pramit Nandi** and Ravindranath Adda, "Integration of Boost-type Active Power Decoupling Topology with Single-Phase Switched Boost Inverter," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11965–11975, Nov. 2020.

2. **Pramit Nandi** and Ravindranath Adda, "An Active Power Decoupling-integrated Reduced-Switch Current-Fed Switched Inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 2, pp. 1929–1942, Apr. 2023.

Conferences

1. **Pramit Nandi** and Ravindranath Adda, "Generation of Switching Pulses for Three-Phase Switched Boost Inverter using Space Vector Modulation," *in Proc. 8th IEEE Int. Conf. Power Electron. Drives Energy Syst. (PEDES)*, Chennai, India, Dec. 2018, pp. 1–6.

2. **Pramit Nandi** and Ravindranath Adda, "Three-Phase Grid-connected Photovoltaic Switched Boost Inverter with Low-Voltage Ride-Through Capability," *in Proc. 8th IEEE Int. Conf. Power Electron. Drives Energy Syst. (PEDES)*, Chennai, India, Dec. 2018, pp. 1–6.

3. **Pramit Nandi** and Ravindranath Adda, "Reduction of Low-Frequency Ripples in Single-Phase Switched Boost Inverter using Active Power Decoupling," *in Proc. 11th IEEE Energy Convers. Congr. Expo. (ECCE)*, Baltimore, MD, USA, Sep.-Oct. 2019, pp. 6981–6988.

4. **Pramit Nandi** and Ravindranath Adda, "An Active Power Decoupling-integrated Four-Switch quasi-Switched Boost Inverter," *in Proc. 12th IEEE Energy Convers. Congr. Expo. (ECCE)*, Detroit, MI, USA, Oct. 2020, pp. 5215–5222.

5. **Pramit Nandi** and Ravindranath Adda, "Reduction of Capacitance in Four-Switch quasi-Switched Boost Inverter using Low-frequency Ripple Damping Scheme," *in Proc. 12th*

IEEE Energy Convers. Congr. Expo. (ECCE), Detroit, MI, USA, Oct. 2020, pp. 6285–6292.

6. **Pramit Nandi** and Ravindranath Adda, "A comprehensive overview of Active Power Decoupling-integrated Switched Boost Inverters," *in Proc. 9th IEEE Int. Conf. Power Electron. Drives Energy Syst. (PEDES)*, Jaipur, India, Dec. 2020, pp. 1–6.

7. **Pramit Nandi** and Ravindranath Adda, "Discontinuous Conduction Mode analysis of Single-phase Switched Boost Inverter with a dc load," *in Proc. 9th IEEE Int. Conf. Power Electron. Drives Energy Syst. (PEDES)*, Jaipur, India, Dec. 2020, pp. 1–6.

8. **Pramit Nandi** and Ravindranath Adda, "Discontinuous Conduction Mode analysis of Single-phase Switched Boost Inverter with a dc load," in *in Proc. 10th Nat. Power Electron. Conf. (NPEC)*, Bhubaneswar, India, Dec. 2021, pp. 1–6.

9. **Pramit Nandi** and Ravindranath Adda, "Comparison of two different configurations of independent Active Power Decoupling networks in Active-Front-End Impedance Source Inverters," *in Proc. 11th Nat. Power Electron. Conf. (NPEC)*, Guwahati, India, Dec. 2023, pp. 1–6.

10. **Pramit Nandi** and Ravindranath Adda, "Reduced-Switch Current-Fed Switched Inverter: Steady-state analysis and PWM control," *in Proc. 11th Nat. Power Electron. Conf. (NPEC)*, Guwahati, India, Dec. 2023, pp. 1–6.

Under Preparation

1. **Pramit Nandi** and Ravindranath Adda, "A PWM-based Ripple Damping Technique for Reduced-Switch Current-Fed Switched Inverter."

2. **Pramit Nandi** and Ravindranath Adda, "An APD approach for Reduced-Switch Current-Fed Switched Inverter with improved gain."

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