Ripple Minimization of Input and Inductor Currents in Coupled Inductor Single Input Dual Output DC-DC Converters

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By

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To my mother **Mrs. Anita Prasad** and my father **Prof. Ram Kailash Prasad**, for their sacrifices, unconditional love, and constant support

Certificate

This is to certify that the thesis entitled "**Ripple Minimization of Input and Inductor Currents in Coupled Inductor Single Input Dual Output DC-DC Converters** ", submitted by **Nupur** (156302007), a research scholar in the *Department of Electronics and Electrical Engineering, Indian Institute of Technology Guwahati*, for the award of the degree of **Doctor of Philosophy**, is a record of an original research work carried out by her under my supervision and guidance. The thesis has fulfilled all the requirements as per the regulations of the institute and, in my opinion, has reached the standard needed for submission. The results embodied in this thesis have not been submitted to any other University or Institute for the award of any degree or diploma.

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Abstract

The single input multiple outputs (SIMO) DC-DC converters with two outputs are called single input dual output (SIDO) DC-DC converters. The SIDO converters can generate two different DC voltage levels from only one available DC voltage level with the reduced component count, reduced losses, reduced physical size and increased efficiency. The introduction of an inversely coupled inductor further reduces the physical size as the flux due to the two windings cancels each other, resulting in a reduced flux in the core. Therefore, the coupled inductor single input dual output (CI-SIDO) buck, boost, and buck-boost converters are analyzed in this thesis.

The analysis of CI-SIDO converters depends on the inductor current patterns. Due to the presence of inversely coupled inductors, the inductor current patterns depend on both the output voltages, input voltage, and the coupled inductor parameters. The slopes of the inductor currents change depending on the input, output voltages, duty ratios and the coupled inductor parameters. If a shift in gate pulse is introduced between the two gate pulses, the waveform patterns change further, thereby increasing the number of inductor current patterns. The change in the inductor current patterns also affects the CCM/DCM boundary of the CI-SIDO converters, as the boundary depends on the inductor current patterns. The presence of coupled inductors affects the DCM operations of the CI-SIDO converters. In DCM, the converter has so many different operating modes due to numerous possibilities of inductor currents. Furthermore, the turning ON of the body diode due to coupling further adds to the feasible operating modes. Also, the variation of input voltage affects both the converters of the CI-SIDO converter because of the common input.

The analysis of each CI-SIDO converter for all possible values of the coupled inductor parameters, duty ratios, and the gate pulse shift is very tedious and repetitive. An approach to unify inductor current waveforms and inductor current ripples in CI-SIDO converters is presented by forming sectors of duty ratios. The CI-SIDO converters have two MOSFETs with two gate pulses. It is found that the shift of one gate pulse with respect to the starting point of another gate pulse reduces the ripples in two inductor currents and input currents. The ripples in inductor currents reduce up to 92.46% with respect to the zero shifting. The condition of the ripple-free input current is also proposed. This work also proposes a unified coupled inductor design with reduced inductor current ripples. An approach to design a CI-SIDO boost converter is also proposed such that the ripple in input current is either zero or less than the maximum specified ripple limit. It is further found that there is no undesirable effect of gate pulse shifting on any of the variables of the CI-SIDO converter, such as the average value of inductor current, input current, and output voltage ripples. Also, the range of CCM operation increases as the shifting is introduced by decreasing the CCM/DCM boundary. The discontinuous conduction mode (DCM) of the CI-SIDO boost converter is also analysed. The input-output voltage relations of DCM are found, and the effect of change in load currents, input voltages and duty ratios are analysed for all possibilities of the CI-SIDO boost converter.

Hence, the CI-SIDO converters can efficiently generate two different DC voltage levels from only one available input voltage level with reduced physical size and reduced ripples. The shifting of gate pulse is advantageous for CI-SIDO converters without any extra circuit elements and control schemes. This simple and low-cost method can achieve ripple-free input current with an assured reduction in the inductor current ripples and also increases the load range of CCM operation in CI-SIDO converters.

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List of Acronyms

CCM	Continuous conduction mode
DCM	Discontinuous conduction mode
SISO	Single input single output
MIMO	Multiple input multiple output
MISO	Multiple input single output systems
SIDO	Single input dual output
CI	Coupled inductor
TPC	Triple port converter
CI-SIDO	Coupled inductor single input dual output
CI-SITO	Coupled inductor single input triple output
PCB	Printed Circuit Board
SMPS	Switched Mode Power Supplies

List of Symbols

S_{t1}, S_{t2}	Two MOSFETs of CI-SIDO converter
S_{d1}, S_{d2}	Two diodes of CI-SIDO converter
g_1, g_2	Gate pulses of S_{t1}, S_{t2}
D_1, D_2	Duty ratios of g_1, g_2
C_1, C_2	Output capacitors
R_1, R_2	Load resistances
L_1, L_2	Coupled inductor windings
k	Coefficient of coupling
M	Mutual inductance
V_{in}, V_{o1}, V_{o2}	Input, output voltages
Δv_{o1}, Δv_{o2}	Ripples in V_{o1}, V_{o2}
v_{L1}, v_{L2}	Voltages across L_1, L_2
D_1, D_2	Duty ratios of two MOSFETs
T_s	Switching time period
NN	State of CI-SIDO when S_{t1} ON and S_{t2} ON
FF	State of CI-SIDO when S_{t1} OFF and S_{t2} OFF
NF	State of CI-SIDO when S_{t1} ON and S_{t2} OFF
FN	State of CI-SIDO when S_{t1} OFF and S_{t2} ON
G_{NNw}, G_{FFw}, G_{NFw}, G_{FNw}	$\frac{di_w}{dt}$ in states NN, FF, NF, FN where $w = 1$ for i_{L1}, $w = 2$ for i_{L2}, $w = in$ for i_{in}

D_t	Shifting of D_2 from starting point of D_1
$\mathbf{D}_{min}$	Range of D_t where Δi_{in} is minimum for given values of L_1, L_2, k, D_1, D_2
i_{L1}, i_{L2}, i_{in}	Inductor currents and input current
i_{d1}, i_{d2}	Diode currents
i_{t1}, i_{t2}	MOSFET currents
i_{C1}, i_{C2}	Capacitor currents
i_{o1}, i_{o2}	Load currents
I_{o1}, I_{o2}	Average values of i_{o1}, i_{o2}
I_{L1}, I_{L2}, I_{in}	Average values of i_{L1}, i_{L2}, i_{in}
$\Delta i_{L1}, \Delta i_{L2}, \Delta i_{in}$	Ripples in inductor and input currents
$\underline{\Delta i_{L1}}, \underline{\Delta i_{L2}}, \underline{\Delta i_{in}}$	Minimum values of $\Delta i_{L1}, \Delta i_{L2}, \Delta i_{in}$
$\widehat{\Delta i_{in}}, \widehat{\Delta i_{L1}}, \widehat{\Delta i_{L2}}$	Maximum specified ripple limits in i_{L1}, i_{L2}, i_{in}
L_{cr1}, L_{cr2}	L_1, L_2 at CCM/DCM boundary
I_{LwB}	Average value of i_{Lw} at CCM/DCM boundary for $D_t = 0$
I'_{LwB}	Average value of i_{Lw} at CCM/DCM boundary for $D_t \neq 0$
$I'_{LwB_{mn}}$	Minimum value of I'_{LwB}
i_{owB}	Load currents at CCM/DCM boundary
D_m	D_t corresponding to $I'_{LwB_{mn}}$
V_{in}, V_{o1}, V_{o2}	Input, output voltages
r_{NF1}, r_{NF2}	D_2 at which $G_{NF1} = 0, G_{NF2} = 0$
r_{FN1}, r_{FN2}	D_1 at which $G_{FN1} = 0, G_{FN2} = 0$
NN_0, FF_0, NF_0, FN_0	States of converter where N, F denote ON and OFF states of S_{t1} and S_{t2}, respectively for $i_{L1} = 0, i_{L2} > 0$

NN_{bD}, FF_{bD}	States of converter where N, F denote ON and OFF states of S_{t1} and S_{t2}, respectively for $i_{L1} < 0$, $i_{L2} > 0$
G_{NNw}, G_{FFw}, G_{NFw}, G_{FNw}, G_{NNw_0}, G_{FFw_0}, G_{NFw_0}, G_{FNw_0}, $G_{NNw_{bD}}$, $G_{FFw_{bD}}$	$\frac{di_w}{dt}$ in states NN, FF, NF, FN, NN_0, FF_0, NF_0, FN_0, NN_{bD}, FF_{bD}, respectively, where $w = 1$ for i_{L1}, $w = 2$ for i_{L2}
t_{NN}, t_{FF}, t_{NF}, t_{FN}, t_{NN_0}, t_{FF_0}, t_{NF_0}, t_{FN_0}, $t_{NN_{bD}}$, $t_{FF_{bD}}$	Duration of states NN, FF, NF, FN, NN_0, FF_0, NF_0, FN_0, NN_{bD}, FF_{bD} divided by T_s
r_{FN1}, r_{FN2},	D_1 at which $G_{FN1} = 0$, $G_{FN2} = 0$ in CCM
r_{NF1}, r_{NF2}	D_2 at which $G_{NF1} = 0$, $G_{NF2} = 0$ in CCM
rd_{FN1}, rd_{FN2},	$\frac{V_{in}}{V_{o1}}$ at which $G_{FN1} = 0$, $G_{FN2} = 0$ in DCM
rd_{NF1}, rd_{NF2}	$\frac{V_{in}}{V_{o2}}$ at which $G_{NF1} = 0$, $G_{NF2} = 0$ in DCM

1

Introduction

Contents

1.1 Introduction

With the extensive use of microprocessors, electric vehicles, hybrid energy sources and portable electronic devices, the requirement for efficient DC-DC converters which can supply multiple voltage levels has increased tremendously. There are two ways by which multiple voltage levels can be generated. The first method is to use multiple single input single output (SISO) converters depending on the number of outputs, as shown in Fig. 1.1(a). The second method is to use a single input multiple output (SIMO) converter, as shown in Fig. 1.1(b). The SIMO converters are of great interest in the literature for converting single DC voltage level to multiple DC voltage levels [3–14]. The SIMO converters are a better option to generate multiple DC voltage levels because of the reduced component, lower losses associated with each component, and increased efficiency [14–17]. For example, various functionalities of electric vehicles like wipers, horns, headlights, microprocessors require different DC voltage levels, as shown in Fig. 1.2. The generation of multiple DC voltage levels from only one available battery requires different DC-DC converters. Alternatively, the SIMO DC-DC converters can supply all the applications from only one available battery.

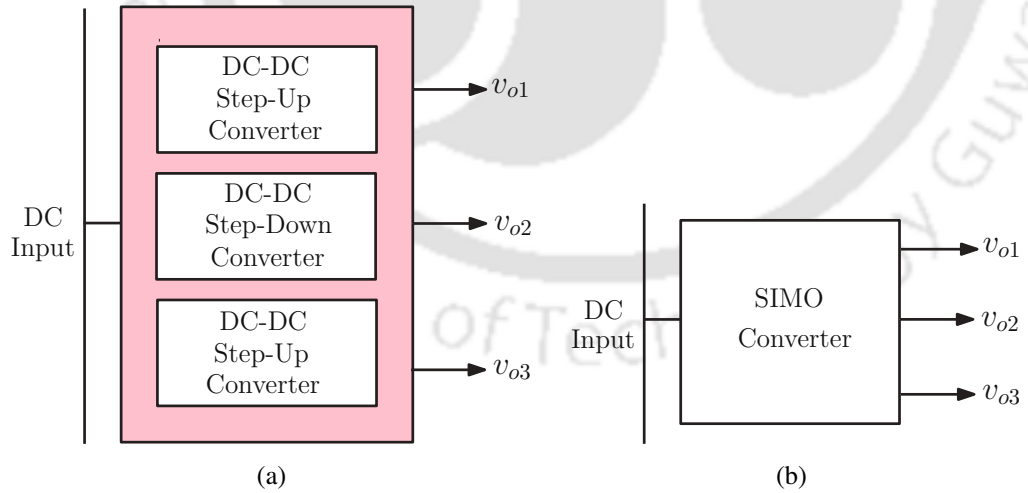

Figure 1.1: (a) Multiple single input single output (SISO) converter, and (b) single input multiple output (SIMO) converter.

Owing to the advantages of the SIMO converters, there are constant improvements in the SIMO topologies to increase their power density, reduce their physical size, improve their voltage regulations, and increase their efficiency. The SIMO converters with two outputs are called single input

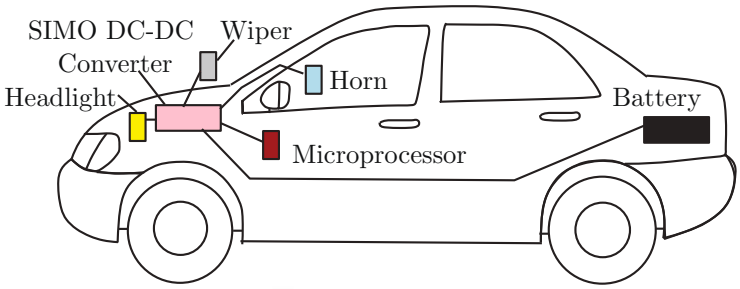

Figure 1.2: The SIMO DC-DC converter in electric vehicles.

dual output (SIDO) converters. This thesis presents the analysis of SIDO converters. The main topologies for SIDO converters are– single inductor SIDO [1, 3–8, 12, 18] and coupled inductor SIDO [10, 11, 14, 19, 20]. The most widely used SIDO topologies are derived from a single inductor as shown in Fig. 1.3 [1, 18]. The two outputs of these converters are derived from the single inductor. The single inductor SIDO has a smaller physical size, weight, and volume. However, due to the presence of only one inductor, the problem of cross-regulation and cross-coupling is very high [1, 18]. In addition, the inductor current ripple is also very high. Several control methods have been proposed in the literature to reduce the effects of these issues [3, 4, 6–8, 12].

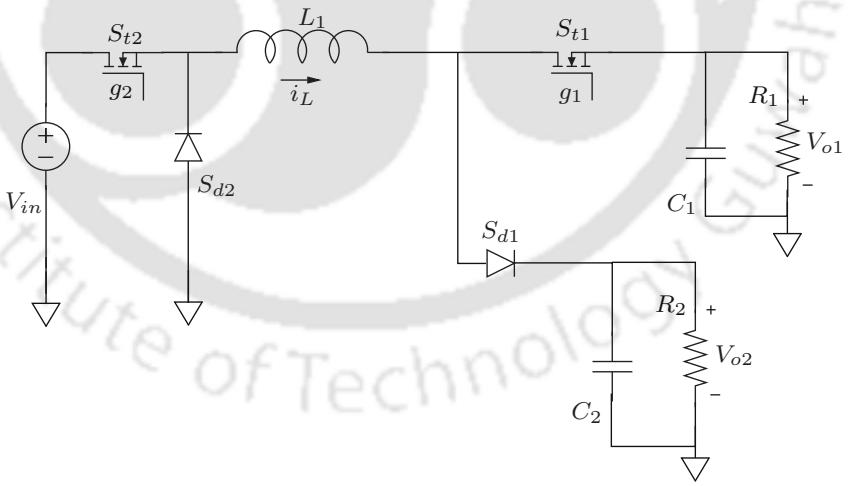

Figure 1.3: The topology of single inductor SIDO [1].

The other widely used topologies are the coupled inductor SIDO (CI-SIDO) converters, as shown in Fig. 1.4. In CI-SIDO, the two outputs are derived using a coupled inductor [14, 19, 20]. These converters have reduced current ripples and reduced cross-regulation and cross-coupling problems. There are two types of coupled inductor SIDO (CI-SIDO) topologies – one with inverse and the other with direct magnetic coupling [13]. The inversely coupled inductor is such that the flux due to one

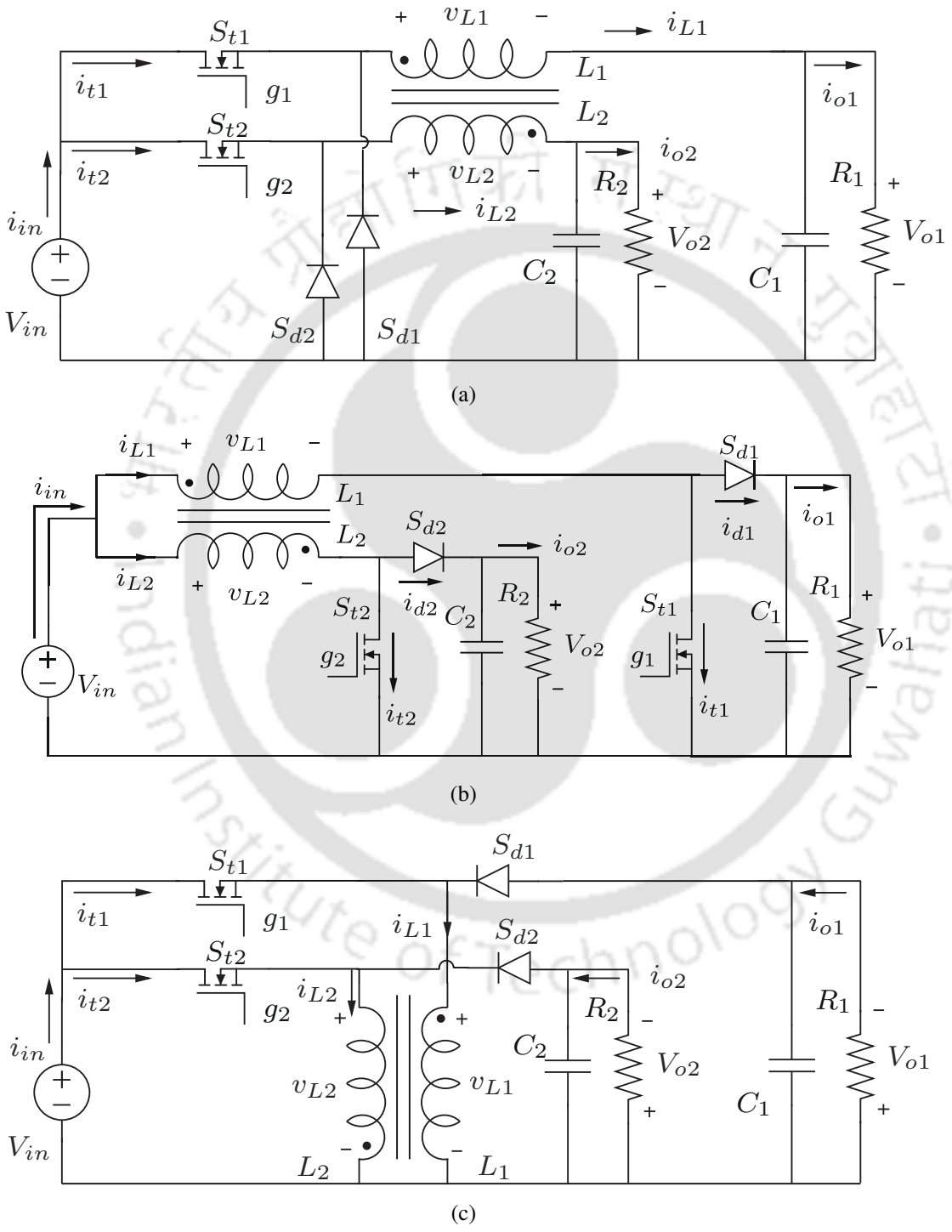

Figure 1.4: CI-SIDO DC-DC converters– (a) Buck, (b) Boost, and (c) Buck-boost.

winding opposes the flux due to another winding. Due to this inversely coupled inductor, the size of the inductor core is reduced [20,21]. So, the overall physical size, weight, and volume of the converter reduce compared to the uncoupled inductors [20]. Also, the inductor current ripples are reduced in CI-SIDO converters [20]. The advantages of the inverse coupling in the SIDO converters are–

- *Reduces flux in core*: In the inversely coupled inductor, the DC flux due to one winding cancels the DC flux due to the other windings. This reduces the flux in the core of the coupled inductor.
- *Avoids magnetic saturation at high currents*: When operated at a high current, the directly coupled inductors saturate the core more readily than inversely coupled inductors due to reduced flux in the core.
- *Inversely coupled inductors are a better choice for high power DC applications*: Due to its flux cancellation characteristics, inversely coupled power converters are superior for high power DC applications.
- *Reduces physical size of CI-SIDO boost converter*: Due to the reduced flux in the core, the volume and weight of the magnetic components reduce. This reduces the overall physical size of the CI-SIDO boost converter.

Therefore, the SIDO converters with inverse magnetic coupling are the topology of interest in this research work and are shown in Fig. 1.4. The CI-SIDO converters can be used in many practical applications like photovoltaics, fuel cells, micro-grids, DC drives, consumer electronics, communication systems, etc. [22–25].

The CI-SIDO converters are generally compared to the interleaved converters. The topology of the interleaved boost converter is shown in Fig. 1.5. However, the CI-SIDO converters are very different from the interleaved converters. In CI-SIDO boost, the values of two output voltages and loads are unequal. The values of the two inductances of coupled windings are also different. The patterns of inductor current waveforms are very different from those in interleaved boost converters. The simplified and special cases of CI-SIDO converters can be compared with interleaved converters when both output voltages, loads and inductances are equal. However, this simplification eliminates the real advantage of SIDO topologies supplying different types of loads.

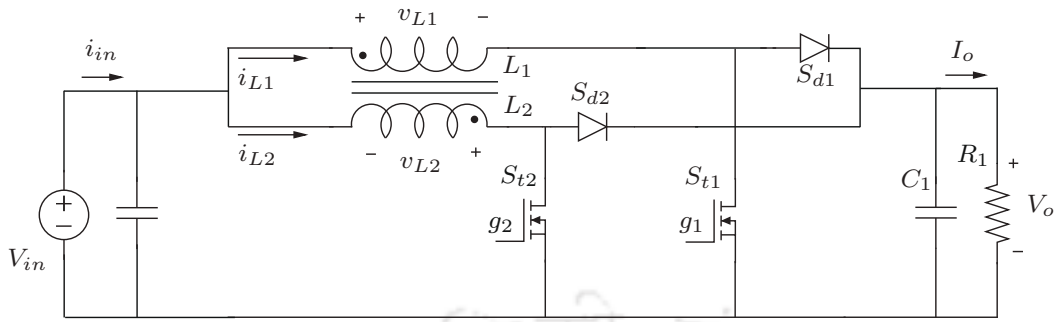

Figure 1.5: The interleaved boost converter [2].

1.2 Advantages of Ripple Reduction

The current ripples in DC-DC converters is an important factor to be considered while designing converters [11, 24, 26–35]. Lower input current ripples reduce the requirement of input filters [24, 26, 28, 33, 34]. The input filters are added in DC-DC converters to suppress noise and attenuate the switching harmonics present in the input current [31, 32, 36, 37]. Applications like fuel cell, photovoltaic generation systems, uninterrupted power systems, electric traction have strict restriction on input current ripples [24, 33, 38, 39]. High current ripples also cause large stress on switching devices, and high electromagnetic interference [11, 24, 26, 28, 33, 34]. Also, a smaller ripple reduces the peak current, thereby reducing switching loss [26]. Higher ripples in currents increase the ratings of inductors and capacitors. The advantages of the ripple reduction are summarised as–

- *Avoids bulky electrolytic capacitors at the input:* The most commonly used method of current ripple reductions is the use of bulky electrolytic capacitors. However, the electrolytic capacitors reduce the lifespan of the systems and also make the system bulky and unreliable. According to [40], an electrolytic capacitor of 2650 μF is required to keep the voltage ripples below 2 V for 100 W, 60 V PV system connected to 50 Hz grid. It is found that the lifespan of electrolytic capacitors gets halved with 10°C increase in temperature [40].

- *Requirement of reduced ripples in PV systems:* The output power capabilities of the PV panels get affected by the ripples in the PV output current. According to [25], the power loss of 6% occurs when the PV current ripples of 2% are allowed. Therefore, reducing current ripples is important for increasing the efficiency of PV systems.

- *Requirement of reduced ripples in fuel cells:* Current ripples affect the fuel cell capacity, life span of fuel cells, and fuel consumption rate. It is found that the proton-exchange membrane (PEM) fuel cells remain dominant in medium power applications like fuel cell vehicles [41]. However, its lifespan, reliability, performance are adversely affected when low-frequency current ripples below 400 Hz are encountered [42]. According to [43], the fuel cells exhibit hysteresis at around 100 Hz. This causes additional losses to the fuel cell system. Therefore, the ripples reduction in a fuel cell is a major issue for fuel cell converter design [41–43].

- *Area of minor B-H loop of filter inductance depends on the inductor current ripples:* The B-H curve of the filter inductance of the DC-DC converters depends on the inductor current ripples. This area of the minor B-H loop decides the core loss of the converter. Therefore, the inductor current ripples should be reduced to decrease the core loss of the DC-DC converters [44].

- *Ratings of devices increase if current ripples are higher:* The peak current through the semiconductor device decides the current ratings. If the ripples are higher, the current ratings of the semiconductor devices like MOSFETs, diodes increase.

- *Avoids the input filters with additional semiconductor devices:* The input filters are added in DC-DC converters to suppress noise and to attenuate the switching harmonics present in the input current [31, 32, 36, 37]. If the ripples are reduced, the requirements of the input filters reduce. This reduces the additional semiconductor devices in the converters, thus reducing the complexity and cost of the converters.

1.3 Literature Review

This section covers the available ripple reduction methods for DC-DC converters. A unified approach of ripple reductions and the methods to obtain zero input currents in DC-DC converters are discussed. The literature on CCM/DCM boundary analysis and the DCM analysis of DC-DC converters are also presented.

1.3.1 Ripple Reduction Methods

Different ripple reduction techniques for various DC-DC converter topologies are available in the literature. The first among them is shifting one gate pulse with respect to another. This method has been widely used in interleaved converters [45, 46]. In interleaved boost with multiple phases, input current ripple is reduced by shifting the gate pulse of each phase with respect to the other by T_s/n, where T_s is the switching time period, and n is the number of phases. Ripples can be reduced further by the use of coupled inductors [47, 48]. Shifting of gate pulses has also been used in SIDO buck converters to reduce ripples [11, 14]. However, in all these converters, the duty ratios of all switches are kept equal. Moreover, ripple reduction has been made by considering equal inductances in all phases. However, in CI-SIDO converters, the two output voltages V_{o1}, V_{o2} and so the duty ratios D_1, D_2 are not equal, as shown in Fig. 1.4. The inductances L_1, L_2 cannot be assumed to be equal as the two loads R_1, R_2 can be different from each other. So, the shift of T_s/n cannot minimize ripple in CI-SIDO converters like the interleaved converters.

The use of an additional passive network is another method for ripple reduction in DC-DC converters. Ripple cancellation networks with additional inductors (L) and capacitors (C), tapped inductors, LL-LC filters have been proposed in [47,49,50]. Active ripple cancellation techniques eliminate harmonics to reduce ripple by injecting additional currents or using control schemes based on frequency [27, 30, 51]. On the other hand, passive ripple cancellation networks make the system bulky and more complex and reduce reliability by using additional elements. Active and passive cancellation techniques are compared in [52]. Although active cancellation does not need additional passive elements, it increases the control complexity and reduces robustness and reliability. New topologies have also been proposed in the literature with reduced ripple [53, 54]. However, these topologies are not standard, and their suitability for different applications needs to be explored more. Reference [55] proposed a method to keep ripple fixed with a change in load by changing switching frequency. So, this method can only be used where the variable switching frequency is allowed.

Amongst all the available methods, the shifting of gate pulse is the most suitable method as it does not involve any additional circuit elements.

1.3.2 Ripple Cancellations & Zero Ripple input Currents in DC-DC converters

The ripple cancellation in input current means the ripple in input current is less than the sum of inductor current ripples. The ripple cancellation is again widely generated for the interleaved boost converters [24, 33, 34]. In these converters, the ripple decreases with the increase in the number of phases and by shifting the gate pulses by T_s/n, where n is the number of phases [24, 33, 56]. Interleaved boost converters have one common output with equal duty ratios for each phase. As gate pulses are shifted by T_s/n, inductor currents also get shifted. So, the addition of shifted currents always causes ripple cancellation [39].

In the converter where direct ripple cancellation is not possible, the reduction of input current ripple by ripple cancellation is obtained by adding an interleaved converter at the input [39,39,57,58]. A flyback-type converter in [57] proposes maximum ripple cancellation by introducing an auxiliary circuit for pulsating input currents, [58] presents a current fed resonant converter with an interleaved converter at the input. However, in all the above methods, the addition of auxiliary circuits and increasing the conversion stages complicate the system by increasing the component count, cost, and volume. The modelling of the interleaved converter is done in [59], which finds the new approach to ripple cancellation in the frequency domain. However, the frequency domain approach makes the system complex to analyze and implement.

Different strategies are adopted in DC-DC converters to obtain zero ripple input currents. The addition of an electrolytic capacitor at the input side is one of them. However, this capacitor reduces the life span of the converter and increases the physical size [60]. There are cases where the interleaving technique is introduced at the input side of the DC-DC converters to get zero ripple input current [47]. Also, zero ripple input currents are obtained for various converters like SEPIC [22, 61], flyback [57] by the introduction of auxiliary circuits. The extra conversion stage and the auxiliary circuit contain additional inductors, capacitors, and switches. Also, several new topologies are proposed in the literature to obtain zero ripple input currents, such as [19].

The most important considerations in the design of DC-DC converters are the input current ripples. The ripples are reduced by introducing slope cancellations in all the DC-DC converters. The most efficient and economical way to introduce slope cancellation is the shift of gate pulse [11, 14]. Hence,

the gate pulse shift is generally introduced to reduce current ripples in DC-DC converters wherever feasible. The attempts to propose a unified approach to ripple reduction in DC-DC converters further add to its advantages.

1.3.3 Existing CCM/DCM Boundary Analysis in DC-DC Converters

The DC-DC converters are preferred to be operated in CCM. This is because the output-input voltage relations and the control of converters are not dependent on the loads in CCM. The CCM/DCM boundary analysis is essential to ensure the CCM operation of the converter. For any DC-DC converter to operate in CCM, the inductance values are required to be kept higher than the critical inductances at CCM/DCM boundary.

The converter operates at CCM/DCM boundary when the inductor currents become zero at the switching time period, T_s. This depends on the waveforms of the inductor currents. Generally, the expressions of inductor currents in CCM are known for the DC-DC converters. CCM/DCM boundary conditions are found by making the starting point of inductor current expressions in CCM to zero. Using this approach, the critical inductance values at CCM/DCM is calculated for converters like a buck-boost [62], a boost [63], etc. In [64], the boundary is calculated by considering the fact that the voltage gain expressions of the converter in CCM and DCM are equal at CCM/DCM boundary.

There are cases where operating the DC-DC converters at CCM/DCM boundary is actually advantageous [65–67]. In [65], a tapped inductor buck converter is proposed, which operates at CCM/DCM boundary. This converter provides a low-cost high step down to obtain an output voltage of about 20 V from the line voltage. In [66], a flyback inverter operates in hybrid operating mode, i.e., the converter operates in DCM or at boundary depending on the input voltage levels. In [67], a forward-flyback converter is described, which operates at CCM/DCM boundary and processes the power efficiently. Therefore, the CCM/DCM boundary analysis of the converter is equally important for the complete analysis of DC-DC converters.

1.3.4 Discontinuous Conduction Mode of DC-DC Converters

The literature presents the DCM analysis of converters like two-phase interleaved boost converter with coupled inductor [68–71]. In [68], two CCM and three DCM operating modes are analysed,

including the current, voltage ripples and DC voltage gain analysis of interleaved boost converter with inversely coupled inductors. In [69], more operating modes of interleaved boost converters are added compared to [68]. The DCM and boundary analysis of ten operating modes are discussed with discrete and coupled inductors. However, few operating modes are still ignored. In [70], the dual interleaved buck and boost converters with interphase transformers are analysed, and major DCM operating regions are presented depending on the voltage ratios and duty cycles. In [71], the complete analysis of interleaved boost converters is presented with all possible operating modes in DCM. The DCM analysis gives rise to many different modes of operation because the forced turn ON of body diodes of the MOSFETs takes place in DCM. Also, the forced conduction of the forward diode takes place due to the presence of coupled inductors.

This research focuses on the coupled inductor SIDO (CI-SIDO) boost converter in DCM. Power electronic converter is usually designed for rated conditions. So, the values of different passive elements (like L_1, L_2, etc.) are chosen at the design stage according to the rating of the converter. However, the converter may not always operate in rated conditions. The load of the converter may reduce while operating, leading to the DCM of the converter. Therefore, this research work evaluates the performance of the CI-SIDO boost converter in DCM.

The CI-SIDO converters have two different duty ratios, output voltages, loads, and inductance values for each of the two phases. In interleaved boost converter, the duty ratios of two phases are equal, inductance values are also equal, and the load is common. The number of DCM operating modes of CI-SIDO boost converter is much more than the coupled inductor interleaved boost [71]. So, the DCM approach adopted for interleaved boost does not apply to the CI-SIDO boost converter.

1.4 Gaps in Existing Literature and Problem Formulation

The following are the research gaps in existing literature–

(i) Among all the existing ripple reduction methods, shifting one gate pulse with respect to another is the most preferred one - due to its simplicity, low cost and no additional network elements. However, minimization of ripple neither by shifting of gate pulses nor by any other methods has been explored in the literature for CI-SIDO converters. The shifting method has been

investigated only for simplified and special cases of SIDO converters with $L_1 = L_2$ and $D_1 = D_2$. But CI-SIDO converters are targeted for a wide range of applications with different output voltages and inductances.

(ii) The conditions of ripple cancellation adopted for interleaved converters are again not valid for CI-SIDO converters, i.e. T_s/n does not give minimum input currents in CI-SIDO converters.

(iii) The methods to obtain zero ripple input current by adding auxiliary circuits reduces the efficiency by increasing the power loss. The weight of the converter also increases, thus reducing its power density.

(iv) The CCM/DCM analysis of the CI-SIDO converters is not available in the literature. The analysis presented for other DC-DC converters is not feasible for CI-SIDO converters. In many applications, the CCM/DCM boundary analysis is also useful.

(v) The DCM analysis of CI-SIDO converters is different from other DC-DC converters. The unequal inductance values and output voltages make the analysis of CI-SIDO converters complex compared to the other converters like interleaved topologies.

Based on the available literature, it is found that the analysis of CI-SIDO converters is not available in the literature till now. The available analysis presented for other DC-DC converters like interleaved converters is not applicable to CI-SIDO converters. The ripples reduction methods for CI-SIDO converters need to be explored. A design method is required for the coupled inductors of the CI-SIDO converters. Also, the CCM/DCM boundary analysis and the DCM analysis for the CI-SIDO converters need to be analysed.

The CI-SIDO converters are shown in Fig. 1.4. The detailed analysis of each CI-SIDO converter is presented in Chapter 2. The analysis shows that due to the presence of inversely coupled inductors, the inductor current patterns depend on both the output voltages, input voltage, and the coupled inductor parameters of the CI-SIDO converters. The slopes of the inductor currents change depending on the output voltages, duty ratios and the coupled inductor parameters. The states of the converter, the ripples expressions, the inductor current slope possibilities for each case are different. The analysis

changes completely as the CI-SIDO converters are changed. The CCM/DCM boundary analysis and the DCM analysis also change as the input, output voltages, and coupled inductor parameters change. Based on the analysis and shortcomings, the following are the problem formulation of the thesis–

(i) A unified approach of analysis is required for converters of this type like CI-SIDO buck, CI-SIDO boost and CI-SIDO buck-boost.

(ii) The effect of gate pulse shift on the inductor current ripples and the input current ripples need to be found for all possible duty ratios and inductance values.

(iii) The design of coupled inductor is needed for reduced inductor current ripples and input current ripples. The design of coupled inductor for zero ripple input current is also required.

(iv) The effect of gate pulse shift on other circuit variables such as the average inductor currents, input current, and output voltage ripples is required.

(v) The effect of gate pulse shift on the CCM/DCM boundary of the CI-SIDO converters needs analysis.

(vi) The effect of coupling and the gate pulse shift on the DCM analysis of the CI-SIDO converters also requires analysis.

1.5 Contribution of the Thesis

Following are the contributions of the thesis:

(i) *Analysis of CI-SIDO Converters:* Detailed analysis and operation of CI-SIDO buck, CI-SIDO boost and CI-SIDO buck-boost converters are presented. The four states of the converters and the current slopes in each state are discussed, along with the factors affecting the current ripples. The CCM/DCM boundary analysis and the DCM analysis of CI-SIDO boost converters are also included in the thesis. It is found that as the converter enters DCM, the body diode of the MOSFETs turns ON, and the ratings of the MOSFETs, output capacitors and diodes change.

(ii) *Unifying Inductor Current Ripples, Finding Zero Ripple Input Current, and Inductor Design by Forming Sectors of Duty Ratios:* To avoid the repetitive analysis of CI-SIDO converters, this thesis presents an approach to unify inductor current patterns and inductor current ripples by forming sectors of duty ratios. In each sector, the inductor current patterns and the inductor current ripples are different from other sectors. The formation of sectors of duty ratios is valid for all three CI-SIDO converters. We have also found the condition for zero ripple input current. The design of coupled inductor for zero ripple input current in the CI-SIDO boost converter is also proposed. For the cases where zero ripple input current is not possible, the coupled inductors are designed such that the input current ripples are less than the maximum specified ripple limit.

(iii) *Effect of Gate Pulse Shift:* The shift of gate pulse is introduced in CI-SIDO converters to reduce ripples in inductor currents and input current. It is found that for a range of gate pulse shifts, the ripples in CI-SIDO converters reduce. We have found that the gate pulse shift reduced the inductor current ripples up to 92.46% without adding extra circuit elements and any extra complex control scheme. The condition for ripple minimizations in input current is also found. The shift in gate pulse is reducing the CCM/DCM boundary of the CI-SIDO boost converter, which increases the CCM operating range of the CI-SIDO boost converter. It is also found that the gate pulse shift has no undesirable effect on the average inductor currents, input currents, and output voltage ripples.

(iv) *Concept Extension to Other Topologies:* The concept of gate pulse shift to reduce the current ripples are also extended to coupled inductor single input triple output (CI-SITO) converters in addition to the CI-SIDO buck, CI-SIDO boost, CI-SIDO buck-boost converters.

1.6 Organization of the Thesis

This thesis has been organized into nine chapters as follows:

- Chapter 2 presents the introduction to the CI-SIDO converters. This chapter covers the detailed operations of the CI-SIDO converters, their four operating states, and the factors affecting the

current ripples in CCM. The possible inductor current slope possibilities and patterns are also presented.

- Chapter 3 presents the basis of sector formation and their advantages. The chapter also presents the effect of coupled inductor parameters on the sector formation of CI-SIDO converters. A unified approach to analyse the CI-SIDO converters are also presented.

- Chapter 4 finds the gate pulse shift where inductor current ripples are minimum for CI-SIDO converters as well as CI-SITO converters.

- Chapter 5 presents the gate pulse shift where input current ripples are minimum. The sector and sub-sector formations with input current ripples are also presented. The conditions of maximum ripple cancellations in input currents are found, and a design method is proposed to achieve maximum ripple cancellation. The condition of zero ripple input current in the CI-SIDO boost converter is also found, and a design method is proposed to achieve zero ripple input current. The practical design considerations in the proposed design method are also presented.

- Chapter 6 presents the effect of gate pulse shift on the average inductor and input currents and on the output voltage ripples of the CI-SIDO boost converter.

- Chapter 7 presents the effect of gate pulse shift on the average inductor currents at CCM/DCM boundaries. The gate pulse shift is found where the average values of inductor currents at CCM/DCM boundaries are minimum.

- Chapter 8 evaluates the effect of coupling on the DCM of the CI-SIDO boost converter. This chapter covers the conditions to turn ON the body diode and the effect of turning ON body diodes on the circuit parameters. The patterns of inductor currents when both boost converters are in DCM are also evaluated.

- Chapter 9 presents the conclusions of the research work and provides the future scope of this research.

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2

CI-SIDO Converters - Analysis of Inductor Currents

Contents

2.1 Introduction

[1] The DC-DC converters have applications in regulated switched mode power supplies (SMPS) which can convert unregulated DC voltages to regulated DC outputs at desired DC voltage levels. The CI-SIDO converters have added advantages of providing two regulated DC outputs from only one unregulated DC input voltage. This thesis presents the following DC-DC converters–

(i) CI-SIDO buck converter

(ii) CI-SIDO boost converter

(iii) CI-SIDO buck-boost converter

The converters are analysed in steady state. All the switches are considered ideal and the losses in inductors and capacitors are neglected. The DC input voltage is considered to have a zero internal impedance with a zero ripple DC voltage. The converters are assumed to supply resistive loads. The output capacitors are assumed to be very large such that constant output voltages are obtained. The aim of this chapter is to analyse all the possible states and the operations of the converter.

2.2 Four States of CI-SIDO Converters

The circuit diagram of CI-SIDO buck converter is shown in Fig. 1.4(a). The two DC output voltages are lower than the common DC input voltage. When the switches are ON, the corresponding diodes are reversed biased and the input supply energy to the loads as well as inductors. When the switches are OFF, the inductor currents flows through the diodes and transfer some portion of its stored energy to the loads.

The circuit diagram of CI-SIDO boost converter is shown in Fig. 1.4(b). The two DC output voltages are greater than the common DC input voltage. When the switches are ON, the corresponding

[1]Major part of this chapter is reproduced from my publications: (i) Nupur and S. Nath, "Minimizing Ripples of Inductor Currents in Coupled SIDO Boost Converter by Shift of Gate Pulses," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1217–1226, Feb. 2020. (ii) Nupur and S. Nath, "Inductor Current Ripples Minimization in Coupled SIDO Buck and Buck-Boost Converter by Gate Pulse Shifting," in *Proc. Int. Conf. Power Electron., Drives Energy Syst.*, Dec. 2020, pp. 1-6.

diodes are reversed biased and the input supply energy to the inductors. When the switches are OFF, the outputs receive energy from the input as well as the inductor.

The circuit diagram of CI-SIDO buck-boost converter is shown in Fig. 1.4(c). The CI-SIDO buck-boost converter generates negative regulated DC output voltages with respect to the common input and output voltage terminals. The two DC output voltages can be either lower or higher than the common DC input voltage. When the switches are ON, the corresponding diodes are reversed biased and the input provide energy to the inductors. When the switches are OFF, the stored energy of the inductors is transferred to the loads.

The two MOSFETs of CI-SIDO buck converter, CI-SIDO Boost converter, and CI-SIDO buck boost converter give rise to four different operating states of the converter which is named as NN, FF, NF and FN where N denotes the ON state and F denotes the OFF state of S_{t1} and S_{t2}, respectively. Therefore, NN means S_{t1} ON and S_{t2} ON, FF means S_{t1} OFF and S_{t2} OFF, NF means S_{t1} ON and S_{t2} OFF, and FN means S_{t1} OFF and S_{t2} ON. The equivalent circuits of CI-SIDO buck, CI-SIDO boost and CI-SIDO buck-boost converters in all the four states are shown in Fig. 2.9, Fig. 2.10 and Fig. 2.11, respectively. The respective slopes, $\frac{di_{Lw}}{dt}$ of all the converter are denoted by G_{NNw}, G_{FFw}, G_{NFw}, G_{FNw} where $w = 1$ for i_{L1} and $w = 2$ for i_{L2}.

2.3 Circuit Analysis to Find Factors Affecting Current Ripples in CCM

In this section, CI-SIDO converters are analysed to find out the factors that affect the ripples of the inductor currents. The scope of the analysis is limited to CCM (DCM analysis is performed in Chapter-8). To find these factors, different conditions of output voltages, load currents and output powers need to be considered. These different possible conditions are presented in Table 2.1. The columns of this table represents the voltage conditions, load demands and the load currents of the two outputs. The rows represent the relative voltages of the two outputs. The table represents the possible load demands, load current and voltage possibilities of CI-SIDO converters.

Here, the analysis is shown for one condition of the CI-SIDO boost converter. For all other conditions, the analysis is similar. The conditions chosen for the CI-SIDO boost converter are $V_{o1} > V_{o2}$ and $P_{o1} < P_{o2}$. The waveforms of gate pulses g_1, g_2; output voltages V_{o1}, V_{o2}; load currents I_{o1},

Table 2.1: Different possible conditions of output voltages, load currents and output powers

Voltage Conditions	Load Demands	Load Currents
$V_{o1} = V_{o2}$	$P_{o1} < P_{o2}$	$I_{o1} < I_{o2}$
	$P_{o1} = P_{o2}$	$I_{o1} = I_{o2}$
	$P_{o1} > P_{o2}$	$I_{o1} > I_{o2}$
$V_{o1} > V_{o2}$	$P_{o1} < P_{o2}$	$I_{o1} < I_{o2}$
	$P_{o1} = P_{o2}$	$I_{o1} < I_{o2}$
	$P_{o1} > P_{o2}$	$I_{o1} > I_{o2}$
$V_{o1} < V_{o2}$	$P_{o1} < P_{o2}$	$I_{o1} < I_{o2}$
	$P_{o1} = P_{o2}$	$I_{o1} > I_{o2}$
	$P_{o1} > P_{o2}$	$I_{o1} > I_{o2}$

I_{o2}, inductor current waveforms i_{L1}, i_{L2}; diode currents i_{d1}, i_{d2} are shown in Fig. 2.1. We observe that the converter goes through states $NN \rightarrow NF \rightarrow FF$. Voltage and branch currents are analysed for each of the three states.

For state NN with duration D_2T_s:

$$\begin{aligned} v_{L1} &= V_{in} \\ i_{C1} &= -\tfrac{V_{o1}}{R_1} \\ v_{L2} &= V_{in} \\ i_{C2} &= -\tfrac{V_{o2}}{R_2} \end{aligned} \tag{2.1}$$

For state NF with duration $(D_1 - D_2)T_s$:

$$\begin{aligned} v_{L1} &= V_{in} \\ i_{C1} &= -\tfrac{V_{o1}}{R_1} \\ v_{L2} &= V_{in} - V_{o2} \\ i_{C2} &= I_{L2} - \tfrac{V_{o2}}{R_2} \end{aligned} \tag{2.2}$$

For state FF with duration $(1 - D_1)T_s$:

$$\begin{aligned} v_{L1} &= V_{in} - V_{o1} \\ i_{C1} &= I_{L1} - \tfrac{V_{o1}}{R_1} \\ v_{L2} &= V_{in} - V_{o2} \\ i_{C2} &= I_{L2} - \tfrac{V_{o2}}{R_2} \end{aligned} \tag{2.3}$$

Output-Input Voltage Relations: The voltage across v_{L1} are given by (2.4).

$$v_{L1} = \begin{cases} V_{in} \text{ if } S_{t1} \text{ ON}, \\ V_{in} - V_{o1} \text{ if } S_{t1} \text{ OFF}. \end{cases} \tag{2.4}$$

Applying the volt-sec balance across v_{L1}, we obtain:

$$V_{in}D_1T_s + (V_{in} - V_{o1})(1 - D_1)T_s = 0, \tag{2.5a}$$

$$\implies \frac{V_{o1}}{V_{in}} = \frac{1}{(1 - D_1)}. \tag{2.5b}$$

Similarly, it is true for V_{o2}. Therefore, the input-output voltage relations are given by:

$$\frac{V_{o1}}{V_{in}} = \frac{1}{(1 - D_1)}, \quad \frac{V_{o2}}{V_{in}} = \frac{1}{1 - D_2} \tag{2.6}$$

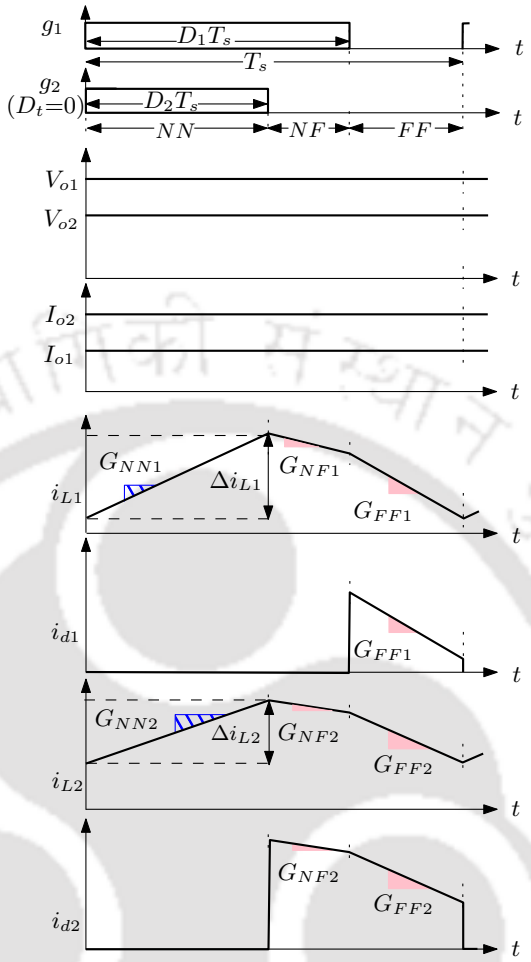


Figure 2.1: Waveforms of the CI-SIDO boost converter.

where, D_1 and D_2 are duty ratios of S_{t1} and S_{t2} respectively.

Average Inductor Current: The DC component of the inductor current is derived by applying capacitor charge balance for both the capacitors.

$$\begin{aligned} &\int_0^{T_s} i_{C1}(t)dt = 0 \\ &\implies \left(-\tfrac{V_{o1}}{R_1}\right) D_1 T_s + \left(I_{L1} - \tfrac{V_{o1}}{R_1}\right)(1-D_1)T_s \\ &\implies I_{L1} = \tfrac{V_{o1}}{(1-D_1)R_1} \end{aligned} \tag{2.7}$$

Also, load current $I_{o1}-$

$$I_{o1} = \frac{V_{o1}}{R_1} = I_{L1}(1-D_1) \tag{2.8}$$

Similarly, applying capacitor charge balance for second capacitor, we get

$$I_{L2} = \frac{V_{o2}}{(1-D_2)R_2} \tag{2.9}$$

Also, load current I_{o2}–

$$I_{o2} = \frac{V_{o2}}{R_2} = I_{L2}(1 - D_2) \tag{2.10}$$

Therefore, the average value of inductor currents depend on the load currents. It does not depend on the coupled inductor parameters.

Average Input Current: For ideal CI-SIDO converter, input power and output power are equal. Therefore, we can write

$$V_{in}I_{in} = V_{o1}I_{o1} + V_{o2}I_{o2} \tag{2.11}$$

Using (2.6), the equation reduces to

$$\begin{aligned} V_{in}I_{in} &= \tfrac{V_{in}}{(1-D_1)}I_{o1} + \tfrac{V_{in}}{(1-D_2)}I_{o2} \\ \implies I_{in} &= I_{L1} + I_{L2} \end{aligned} \tag{2.12}$$

Inductor Current Ripples: As the slopes of the currents are known, the ripple is calculated by the product of slope magnitude and its duration as presented below:

$$\Delta i_{Lw} = \Sigma\{|\text{+ve slope}| \times (\text{slope's time interval})\} = \Sigma\{|\text{-ve slope}| \times (\text{slope's time interval})\} \tag{2.13}$$

The expressions of inductor currents are derived by applying KVL to each boost converters. The detailed derivations are presented below.

Applying KVL in the first boost converter of state NN, we get

$$\begin{aligned} (1-k^2)L_1\tfrac{di_{L1}}{dt} &= V_{in} + k\sqrt{\tfrac{L_1}{L_2}}v_{L2} \\ (1-k^2)L_1\tfrac{di_{L1}}{dt} &= \left(1 + k\sqrt{\tfrac{L_1}{L_2}}\right)V_{in} \\ \tfrac{di_{L1}}{dt} &= \tfrac{\Delta i_{L1\ NN}}{D_2T_s} = \tfrac{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)V_{in}}{(1-k^2)L_1} \end{aligned} \tag{2.14}$$

The ripple expressions in this state is given by-

$$\Delta i_{L1\ NN} = \frac{\left(1 + k\sqrt{\frac{L_1}{L_2}}\right)V_{in}}{(1-k^2)L_1}D_2T_s \tag{2.16}$$

We can observe that this ripple expression is > 0 always.

Applying KVL in the second boost converter of state NN, we get

$$\begin{aligned} (1-k^2)L_2\tfrac{di_{L2}}{dt} &= V_{in} + k\sqrt{\tfrac{L_2}{L_1}}v_{L1} \\ (1-k^2)L_2\tfrac{di_{L2}}{dt} &= \left(1 + k\sqrt{\tfrac{L_2}{L_1}}\right)V_{in} \\ \tfrac{di_{L2}}{dt} &= \tfrac{\Delta i_{L2\ NN}}{D_2T_s} = \tfrac{\left(1+k\sqrt{\frac{L_2}{L_2}}\right)V_{in}}{(1-k^2)L_2} \end{aligned} \tag{2.15}$$

The ripple expressions in this state is given by-

$$\Delta i_{L2\ NN} = \frac{\left(1 + k\sqrt{\frac{L_2}{L_2}}\right)V_{in}}{(1-k^2)L_2}D_2T_s \tag{2.17}$$

We can observe that this ripple expression is > 0 always.

Similarly, applying KVL in the first boost converter of state NF, we get

$$(1-k^2)L_1\frac{di_{L1}}{dt} = V_{in} + k\sqrt{\frac{L_1}{L_2}}v_{L2}$$
$$(1-k^2)L_1\frac{di_{L1}}{dt} = V_{in} + k\sqrt{\frac{L_1}{L_2}}(V_{in}-V_{o2})$$
$$\frac{di_{L1}}{dt} = \frac{\Delta i_{L1\ NF}}{(D_1-D_2)T_s} = \frac{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)V_{in}-k\sqrt{\frac{L_1}{L_2}}V_{o2}}{(1-k^2)L_1} \quad (2.18)$$

The ripple expressions in this state is given by-

$$\Delta i_{L1\ NF} = \frac{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)V_{in}-k\sqrt{\frac{L_1}{L_2}}V_{o2}}{(1-k^2)L_1}(D_1-D_2)T_s \quad (2.20)$$

We can observe that this ripple expression can be > 0 or < 0, or $= 0$.

Applying KVL in the second boost converter of state NF, we get

$$(1-k^2)L_2\frac{di_{L2}}{dt} = V_{in} - V_{o2} + k\sqrt{\frac{L_2}{L_1}}v_{L1}$$
$$(1-k^2)L_2\frac{di_{L2}}{dt} = V_{in} - V_{o2} + k\sqrt{\frac{L_2}{L_1}}V_{in}$$
$$\frac{di_{L2}}{dt} = \frac{\Delta i_{L2\ NF}}{(D_1-D_2)T_s} = \frac{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)V_{in}-V_{o2}}{(1-k^2)L_2} \quad (2.19)$$

The ripple expressions in this state is given by-

$$\Delta i_{L2\ NF} = \frac{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)V_{in}-V_{o2}}{(1-k^2)L_2}(D_1-D_2)T_s \quad (2.21)$$

We can observe that this ripple expression can be > 0 or < 0, or $= 0$.

Applying KVL in the first boost converter of state FF, we get

$$(1-k^2)L_1\frac{di_{L1}}{dt} = V_{in} - V_{o1} + k\sqrt{\frac{L_1}{L_1}}v_{L2}$$
$$(1-k^2)L_1\frac{di_{L1}}{dt} = V_{in} - V_{o1} + k\sqrt{\frac{L_1}{L_1}}(V_{in}-V_{o2})$$
$$\frac{di_{L1}}{dt} = \frac{\Delta i_{L1\ FF}}{(1-D_1)T_s} = \frac{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)V_{in}-V_{o1}-k\sqrt{\frac{L_1}{L_2}}V_{o2}}{(1-k^2)L_1} \quad (2.22)$$

The ripple expressions in this state is given by-

$$\Delta i_{L1\ FF} = \frac{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)V_{in}-V_{o1}-k\sqrt{\frac{L_1}{L_2}}V_{o2}}{(1-k^2)L_1}(1-D_1)T_s \quad (2.24)$$

We can observe that this ripple expression is < 0 always.

Applying KVL in the second boost converter of state FF, we get

$$(1-k^2)L_2\frac{di_{L2}}{dt} = V_{in} - V_{o2} + k\sqrt{\frac{L_2}{L_1}}v_{L1}$$
$$(1-k^2)L_2\frac{di_{L2}}{dt} = V_{in} - V_{o2} + k\sqrt{\frac{L_2}{L_1}}(V_{in}-V_{o1})$$
$$\frac{di_{L2}}{dt} = \frac{\Delta i_{L2\ FF}}{(1-D_1)T_s} = \frac{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)V_{in}-V_{o2}-k\sqrt{\frac{L_2}{L_1}}V_{o1}}{(1-k^2)L_2} \quad (2.23)$$

The ripple expressions in this state is given by-

$$\Delta i_{L2\ FF} = \frac{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)V_{in}-V_{o2}-k\sqrt{\frac{L_2}{L_1}}V_{o1}}{(1-k^2)L_2}(1-D_1)T_s \quad (2.25)$$

We can observe that this ripple expression is < 0 always.

If (2.20) and (2.21) are negative, the ripples are given by-

$$\Delta i_{L1} = \Delta i_{L1\ NN} = \frac{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)V_{in}}{(1-k^2)L_1}D_2T_s = |\Delta i_{L1\ NF}| + |\Delta i_{L1\ FF}|$$
$$\Delta i_{L2} = \Delta i_{L2\ NN} = \frac{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)V_{in}}{(1-k^2)L_2}D_2T_s = |\Delta i_{L2\ NF}| + |\Delta i_{L2\ FF}| \quad (2.26)$$

Similarly, if (2.20) and (2.21) are positive, the ripples are given by-

$$\begin{aligned}\Delta i_{L1} &= \Delta i_{L1\ NN} + \Delta i_{L1\ NF} = \frac{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)V_{in}}{(1-k^2)L_1}D_2T_s + \frac{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)V_{in}-k\sqrt{\frac{L_1}{L_2}}V_{o2}}{(1-k^2)L_1}(D_1-D_2)T_s = |\Delta i_{L1\ FF}| \\ \Delta i_{L2} &= \Delta i_{L2\ NN} + \Delta i_{L2\ NF} = \frac{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)V_{in}}{(1-k^2)L_2}D_2T_s + \frac{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)V_{in}-V_{o2}}{(1-k^2)L_2}(D_1-D_2)T_s = |\Delta i_{L2\ FF}|\end{aligned} \tag{2.27}$$

If (2.20) is negative and (2.21) is positive, the ripples are given by-

$$\begin{aligned}\Delta i_{L1} &= \Delta i_{L1\ NN} = \frac{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)V_{in}}{(1-k^2)L_1}D_2T_s = |\Delta i_{L1\ NF}| + |\Delta i_{L1\ FF}| \\ \Delta i_{L2} &= \Delta i_{L2\ NN} + \Delta i_{L2\ NF} = \frac{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)V_{in}}{(1-k^2)L_2}D_2T_s + \frac{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)V_{in}-V_{o2}}{(1-k^2)L_2}(D_1-D_2)T_s = |\Delta i_{L2\ FF}|\end{aligned} \tag{2.28}$$

From the above analysis, we observe that inductor current ripples depend on:

- Input and output voltages
- Duty ratios
- Pattern of the gate pulse
- Values of the coupled inductor

It does not depend on the load currents/output power/load demands. Also, from above analysis, we observe that pattern of inductor currents depend on slope of inductor currents, which in turn depend on the coupled inductor parameters and input-output voltages. The pattern of inductor current waveforms also does not depend on the load currents/output power/load demands. Output powers are proportional to average values of inductor current. For the same average values of inductor currents, different patterns of inductor current waveforms and ripples can be obtained. This is shown by the simulation results in Fig. 2.2 with $V_{in} = 8\ V$, $D_1 = D_2 = 0.3$, $I_{o1} = 1.47\ A$, $I_{o2} = 0.98\ A$, $k = 0.73$, $L_1 = 131\ \mu H$, $L_2 = 95\ \mu H$.

2.4 Problems of Numerous, Variable and Unforeseeable Patterns of Inductor Current Waveforms in CI-SIDO Converters

2.4.1 Fixed Pattern of Waveforms in Interleaved Converters

In the interleaved boost converter, $D_1 = D_2 = D$ and $L_1 = L_2 = L$, resulting in equal slopes of i_{L1} and i_{L2}. Therefore, a limited number of waveform patterns are possible. The waveforms of

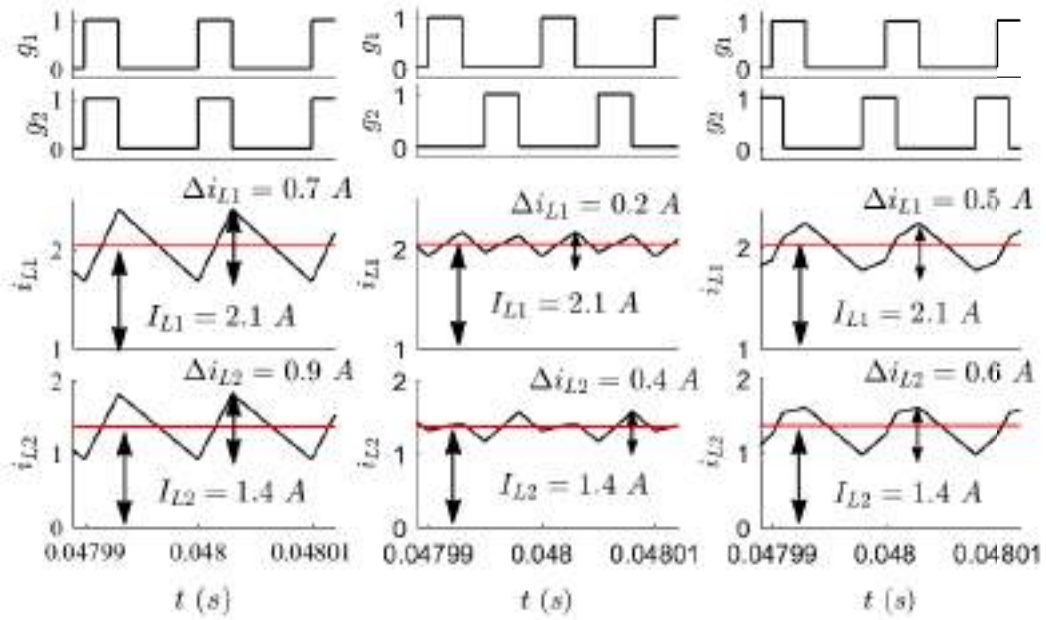


Figure 2.2: Simulation results to show that for same average values of inductor currents, different patterns of inductor current waveforms and ripples can be obtained for CI-SIDO converters.

the inductor currents remain same even if the gate pulses are shifted, as shown in Fig. 2.3. Even if the coupled inductors are added to the interleaved converters, the number of waveforms are limited because of the equal duty ratios, and equal windings. Here, the values of gate pulse shift for minimum current ripples are a fixed value. The slope cancellations of the inductor currents always takes place. Also, the slope cancellations always lead to ripple cancellation.

In the CI-SIDO boost, the values of two output voltages and loads are unequal. The values of two inductances of coupled windings are also different. The patterns of inductor current waveforms are very different than that in interleaved boost converters (or other topologies where shifting of gate pulses is used to reduce ripple). Therefore, this article presents a detailed analysis of the CI-SIDO converters.

2.4.2 Variable Patterns of Current Waveforms in CI-SIDO Converters - Without Shifting Gate Pulse

This section presents the possible inductor current waveforms of the CI-SIDO boost converter with no gate pulse shift. In Fig. 2.4, different patterns are observed by varying the duty ratios such that $D_1 < D_2$ keeping the coupled inductor parameters as $k = 0.73$, $L_1 = 100\ \mu H$, $L_2 = 150\ \mu H$. In Fig. 2.5, different patterns are observed by varying the duty ratios such that $D_1 > D_2$ keeping the

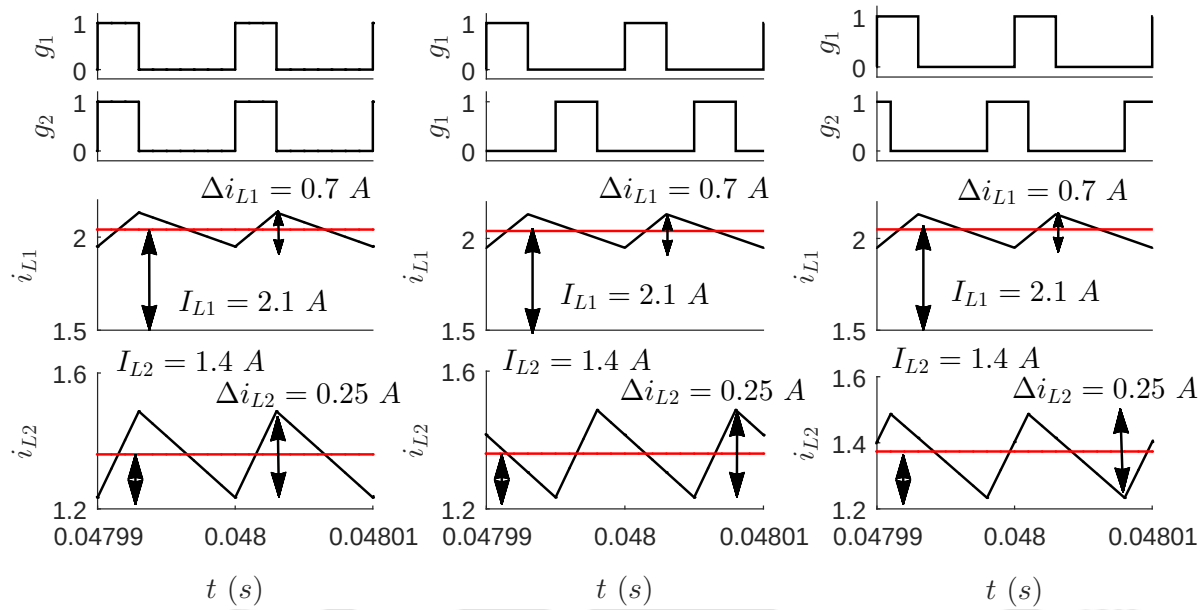


Figure 2.3: In interleaved converters, the inductor current waveforms remain same even if the gate pulses are shifted.

coupled inductor parameters as $k = 0.73$, $L_1 = 100\ \mu H$, $L_2 = 150\ \mu H$. In Fig. 2.6, the effect of change in coupled inductor parameters are shown for $V_{in} = 8\ V$, $R_1 = 8\ \Omega$, $R_2 = 12\ \Omega$, $D_1 = 0.4$, $D_1 = 0.5$. The three coupled inductor parameters chosen are- (i) $k = 0.73$, $L_1 = 100\ \mu H$, $L_2 = 1000\ \mu H$, (ii) $k = 0.73$, $L_1 = 150\ \mu H$, $L_2 = 100\ \mu H$, (iii) $k = 0.73$, $L_1 = 100\ \mu H$, $L_2 = 200\ \mu H$.

2.4.3 Numerous Patterns of Current Waveforms in CI-SIDO Converters - With Shift in Gate Pulse

The simulation results of inductor currents by varying shift in gate pulse for $D_1 + D_2 > 1$ and $D_1 > D_2$ are shown in Fig.2.7 and Fig. 2.8. The simulations are shown for $V_{in} = 8\ V$, $k = 0.73$, $L_1 = 100\ \mu H$, $L_2 = 150\ \mu H$, $R_1 = 8\ \Omega$, $R_2 = 20\ \Omega$, $D_1 = 0.8$, $D_2 = 0.5$. The gate pulse shift that is considered here are 0.1, 0.3, 0.5, 0.7, 0.8, 0.9. As the gate pulse shift varies, the inductor current patterns are changing.

Thus, we observe that the pattern of inductor currents in CI-SIDO converters are variable in nature. Numerous patterns are possible. For a given condition, the pattern of current waveform is unforeseeable without theoretical calculations or simulation. As the pattern of inductor currents depend on the slope of inductor currents, analysis of slopes of inductor currents are performed in next section.

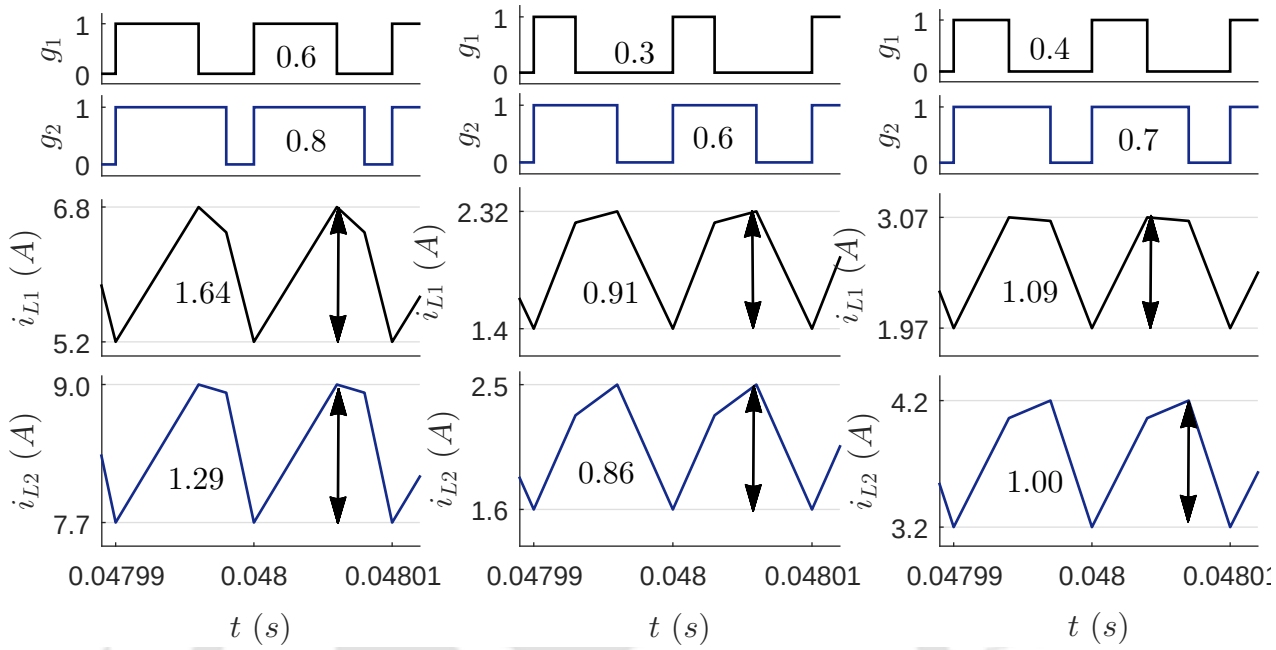


Figure 2.4: Simulation results to show the effect of change in output voltages on patterns of inductor current waveforms for $D_1 < D_2$. The parameters are – $V_{in} = 8\ V$, $k = 0.73$, $L_1 = 100\ \mu H$, $L_2 = 150\ \mu H$, $R_1 = 8\ \Omega$, $R_2 = 24\ \Omega$.

2.5 Derivation of Inductor Current Slopes

Each converter has a single input V_{in} and two outputs– V_{o1}, V_{o2}. The two MOSFETs S_{t1}, S_{t2} have two gate pulses g_1, g_2 with duty ratios D_1, D_2. The load resistances are R_1, R_2 and load currents are i_{o1}, i_{o2}. The coupled inductor has two windings L_1, L_2, and coefficient of coupling k. The inductors are inversely coupled such that the flux due to two windings oppose each other in the core. The voltage across the coupled inductor windings are v_{L1}, v_{L2} and current through them are i_{L1}, i_{L2}. Due to the coupling, the voltages and currents are related as (2.29) where $M = k\sqrt{L_1 L_2}$.

$$v_{L1} = L_1 \frac{di_{L1}}{dt} - M\frac{di_{L2}}{dt}, \tag{2.29a}$$

$$v_{L2} = L_2 \frac{di_{L2}}{dt} - M\frac{di_{L1}}{dt} \tag{2.29b}$$

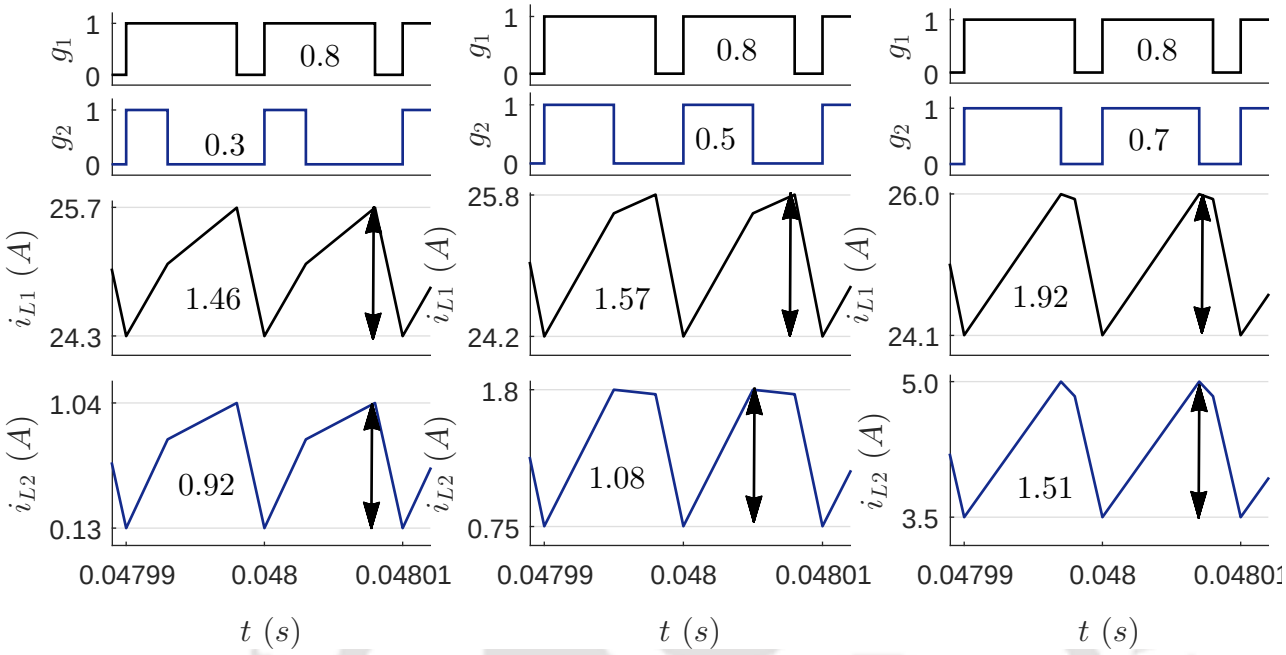


Figure 2.5: Simulation results to show the effect of change in output voltages on patterns of inductor current waveforms for $D_1 > D_2$. The parameters are – $V_{in} = 8\ V$, $k = 0.73$, $L_1 = 100\ \mu H$, $L_2 = 150\ \mu H$, $R_1 = 8\ \Omega$, $R_2 = 20\ \Omega$.

The voltage and current relations in (2.29) can be reduced to (2.30) to find the slopes of inductor currents.

$$\frac{di_{L1}}{dt} = \frac{v_{L1} + k\sqrt{\frac{L_1}{L_2}}v_{L2}}{(1-k^2)L_1}, \tag{2.30a}$$

$$\frac{di_{L2}}{dt} = \frac{v_{L2} + k\sqrt{\frac{L_2}{L_1}}v_{L1}}{(1-k^2)L_2}. \tag{2.30b}$$

2.5.1 Slopes of Inductor Currents in CI-SIDO Buck Converter

The detailed discussions on the four operating states of CI-SIDO buck converter is presented in this section.

NN: The equivalent circuit in this state is shown in Fig. 2.9(a). In this state, S_{t1} and S_{t2} both are ON simultaneously. The voltage across the inductor windings are presented in (2.31).

$$v_{L1} = V_{in} - V_{o1}, \tag{2.31a}$$

$$v_{L2} = V_{in} - V_{o2} \tag{2.31b}$$

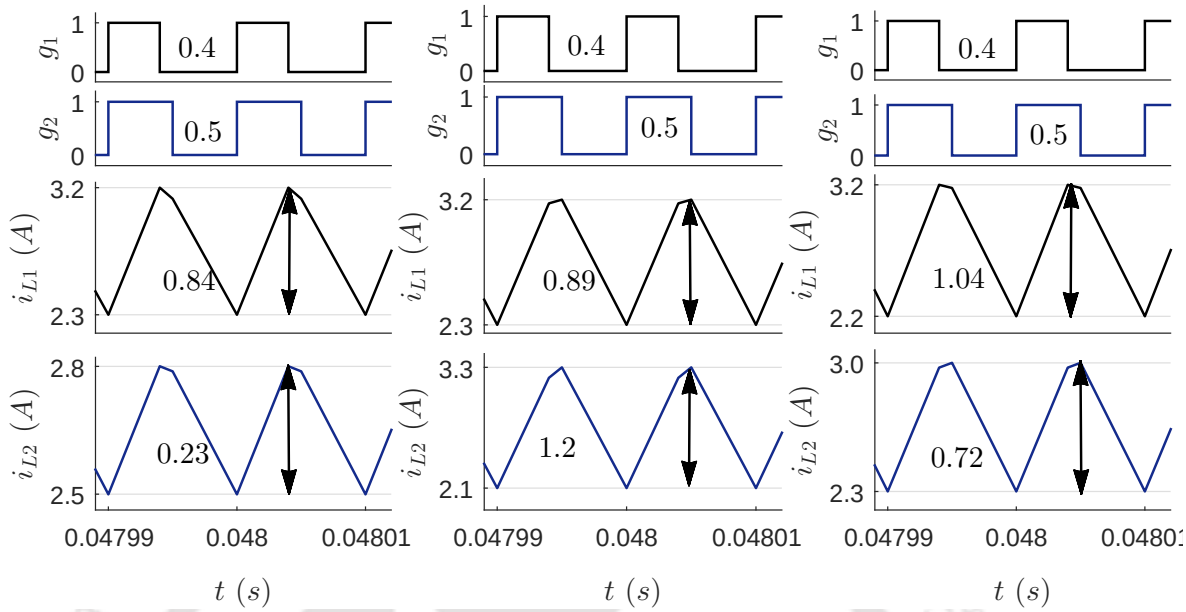


Figure 2.6: Simulation results to show the effect of changing k, L_1, L_2 on patterns of inductor current waveforms. The coupled inductor parameters chosen are $k = 0.73$, $L_1 = 100\ \mu H$, $L_2 = 1000\ \mu H$, $k = 0.73$, $L_1 = 150\ \mu H$, $L_2 = 100\ \mu H$, $k = 0.73$, $L_1 = 100\ \mu H$, $L_2 = 200\ \mu H$

The slope of inductor currents in this state can be formulated by combining (2.30) and (2.31). The obtained slopes in this state are obtained in (2.32).

$$G_{NN1} = \frac{(1 + k\sqrt{\frac{L_1}{L_2}})V_{in} - V_{o1} - k\sqrt{\frac{L_1}{L_2}}V_{o2}}{(1 - k^2)L_1}, \tag{2.32a}$$

$$G_{NN2} = \frac{(1 + k\sqrt{\frac{L_2}{L_1}})V_{in} - k\sqrt{\frac{L_2}{L_1}}V_{o1} - V_{o2}}{(1 - k^2)L_2} \tag{2.32b}$$

FF: The equivalent circuit in this state is shown in Fig. 2.9(b). In this state, S_{t1} and S_{t2} both are OFF simultaneously. The voltage across the inductor windings are presented in (2.33).

$$v_{L1} = -V_{o1}, \tag{2.33a}$$

$$v_{L2} = -V_{o2} \tag{2.33b}$$

The slope of inductor currents in this state can be formulated by combining (2.30) and (2.33). The

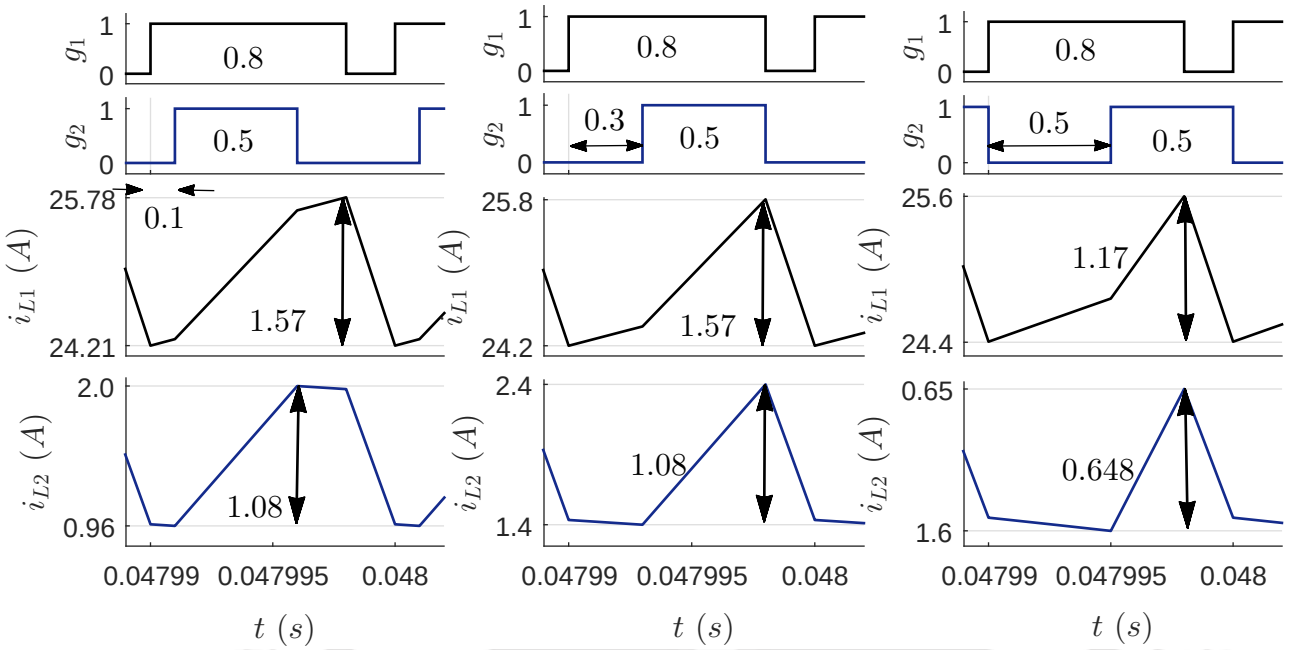


Figure 2.7: Simulation results to show the effect of gate pulse shift on patterns of inductor current waveforms. The simulations are done for $V_{in} = 8\ V$, $k = 0.73$, $L_1 = 100\ \mu H$, $L_2 = 150\ \mu H$, $R_1 = 8\ \Omega$, $R_2 = 20\ \Omega$, $D_1 = 0.8$, $D_2 = 0.5$. The gate pulse shifts change from 0.1, 0.3 to 0.5.

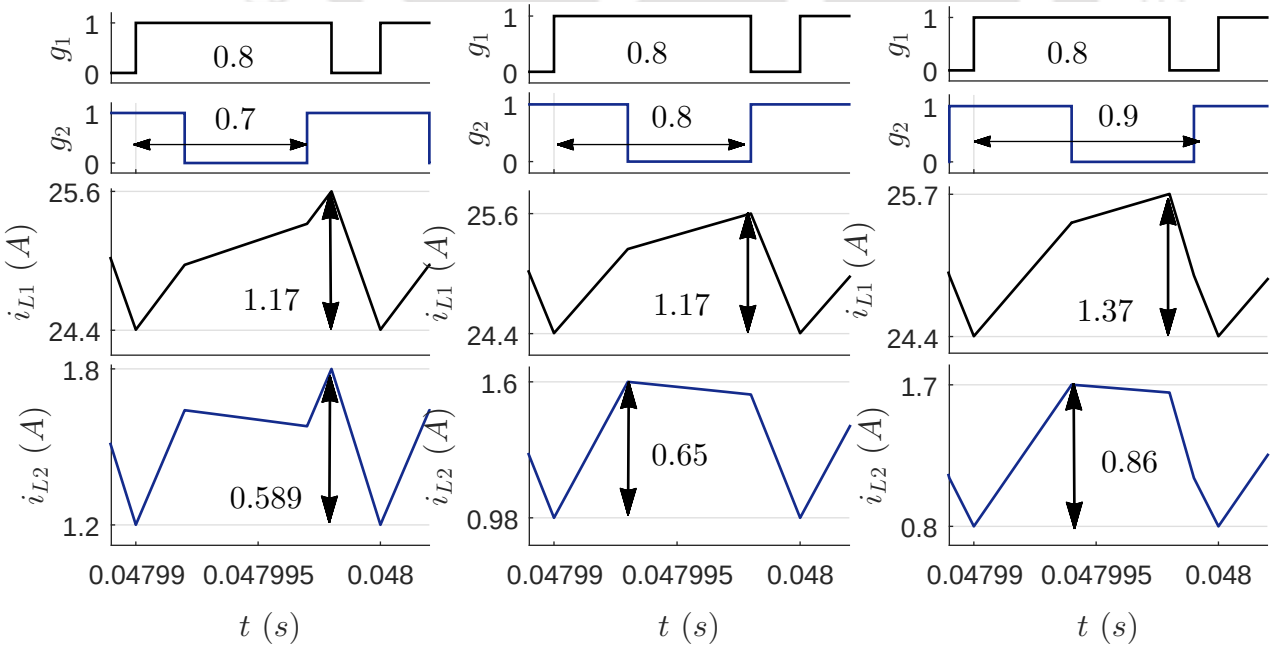


Figure 2.8: Simulation results to show the effect of gate pulse shift on patterns of inductor current waveforms. The simulations are done for $V_{in} = 8\ V$, $k = 0.73$, $L_1 = 100\ \mu H$, $L_2 = 150\ \mu H$, $R_1 = 8\ \Omega$, $R_2 = 20\ \Omega$, $D_1 = 0.8$, $D_2 = 0.5$. The gate pulse shifts change from 0.7, 0.8 to 0.9.

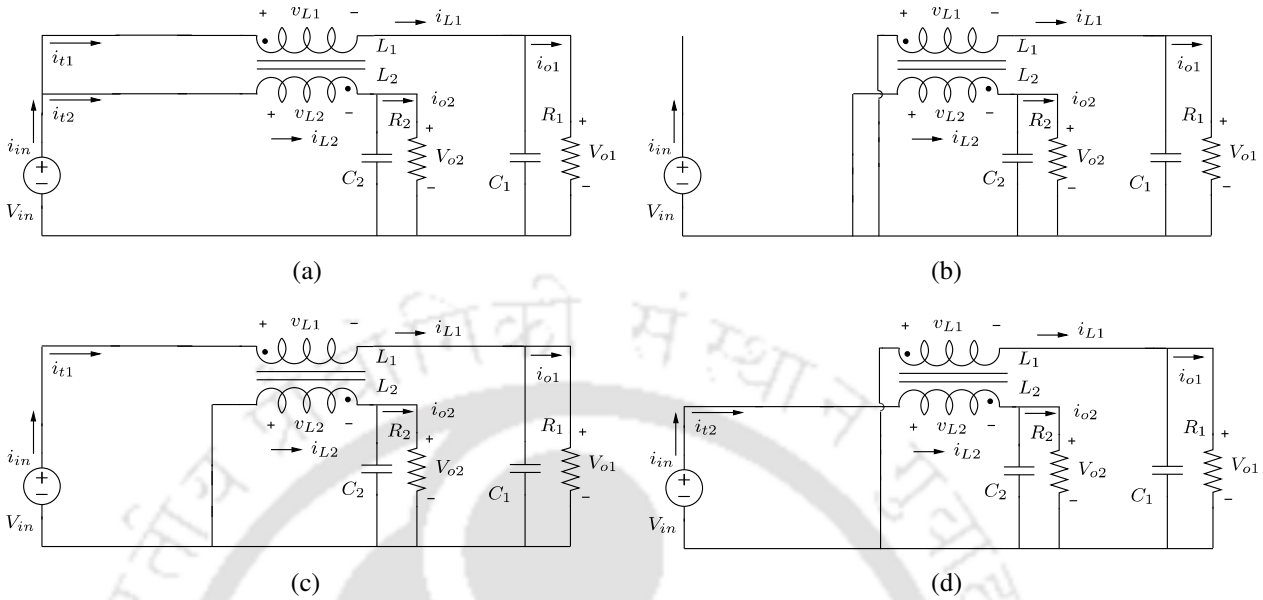


Figure 2.9: Equivalent circuits of CI-SIDO buck in different states: (a) NN, (b) FF, (c) NF and (d) FN.

obtained slopes in this state are obtained in (2.34).

$$G_{FF1} = \frac{-V_{o1} - k\sqrt{\frac{L_1}{L_2}}V_{o2}}{(1-k^2)L_1}, \tag{2.34a}$$

$$G_{FF2} = \frac{-k\sqrt{\frac{L_2}{L_1}}V_{o1} - V_{o2}}{(1-k^2)L_2} \tag{2.34b}$$

NF: The equivalent circuit in this state is shown in Fig. 2.9(c). In this state, S_{t1} is ON and S_{t2} is OFF. The voltage across the inductor windings are presented in (2.35).

$$v_{L1} = V_{in} - V_{o1}, \tag{2.35a}$$

$$v_{L2} = -V_{o2} \tag{2.35b}$$

The slope of inductor currents in this state can be formulated by combining (2.30) and (2.35). The

obtained slopes in this state are obtained in (2.36).

$$G_{NF1} = \frac{V_{in} - V_{o1} - k\sqrt{\frac{L_1}{L_2}}V_{o2}}{(1-k^2)L_1}, \tag{2.36a}$$

$$G_{NF2} = \frac{k\sqrt{\frac{L_2}{L_1}}V_{in} - k\sqrt{\frac{L_2}{L_1}}V_{o1} - V_{o2}}{(1-k^2)L_2} \tag{2.36b}$$

FN: The equivalent circuit in this state is shown in Fig. 2.9(d). In this state, S_{t1} is OFF and S_{t2} is ON. The voltage across the inductor windings are presented in (2.37).

$$v_{L1} = -V_{o1}, \tag{2.37a}$$

$$v_{L2} = V_{in} - V_{o2} \tag{2.37b}$$

The slope of inductor currents in this state can be formulated by combining (2.30) and (2.37). The obtained slopes in this state are obtained in (2.38).

$$G_{FN1} = \frac{k\sqrt{\frac{L_1}{L_2}}V_{in} - V_{o1} - k\sqrt{\frac{L_1}{L_2}}V_{o2}}{(1-k^2)L_1}, \tag{2.38a}$$

$$G_{FN2} = \frac{V_{in} - k\sqrt{\frac{L_2}{L_1}}V_{o1} - V_{o2}}{(1-k^2)L_2} \tag{2.38b}$$

The slopes of the inductor currents in all the four states are presented in Table 2.2. The rows of the table represent the three CI-SIDO converters and the columns represent the four states of the CI-SIDO converters. In continuous conduction mode (CCM), making the average voltage across inductors zero over switching time period T_s, we obtain:

$$V_{o1} = D_1 V_{in}, \tag{2.39a}$$

$$V_{o2} = D_2 V_{in} \tag{2.39b}$$

where, D_1 and D_2 are duty ratios of S_{t1} and S_{t2} respectively. It can be seen from (2.39) that output voltage V_{o1} and V_{o2} are not coupled i.e. unaffected by each other in CCM. So, duty ratios D_1 and D_2 also are not affected by mutual coupling in CCM.

Table 2.2: Inductor current slopes for CI-SIDO Buck, Boost, and Buck-Boost Converters

CI-SIDO converter	Inductor current	*NN*	*FF*	*NF*	*FN*
Buck	i_{L1}	$\frac{(1+k\sqrt{\frac{L_1}{L_2}})V_{in}-V_{o1}-k\sqrt{\frac{L_1}{L_2}}V_{o2}}{(1-k^2)L_1}$	$\frac{-V_{o1}-k\sqrt{\frac{L_1}{L_2}}V_{o2}}{(1-k^2)L_1}$	$\frac{V_{in}-V_{o1}-k\sqrt{\frac{L_1}{L_2}}V_{o2}}{(1-k^2)L_1}$	$\frac{k\sqrt{\frac{L_1}{L_2}}V_{in}-V_{o1}-k\sqrt{\frac{L_1}{L_2}}V_{o2}}{(1-k^2)L_1}$
	i_{L2}	$\frac{(1+k\sqrt{\frac{L_2}{L_1}})V_{in}-k\sqrt{\frac{L_2}{L_1}}V_{o1}-V_{o2}}{(1-k^2)L_2}$	$\frac{-k\sqrt{\frac{L_2}{L_1}}V_{o1}-V_{o2}}{(1-k^2)L_2}$	$\frac{k\sqrt{\frac{L_2}{L_1}}V_{in}-k\sqrt{\frac{L_2}{L_1}}V_{o1}-V_{o2}}{(1-k^2)L_2}$	$\frac{V_{in}-k\sqrt{\frac{L_2}{L_1}}V_{o1}-V_{o2}}{(1-k^2)L_2}$
Boost	i_{L1}	$\frac{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)V_{in}}{(1-k^2)L_1}$	$\frac{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)V_{in}-\left(V_{01}+k\sqrt{\frac{L_1}{L_2}}V_{02}\right)}{(1-k^2)L_1}$	$\frac{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)V_{in}-k\sqrt{\frac{L_1}{L_2}}V_{02}}{(1-k^2)L_1}$	$\frac{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)V_{in}-V_{01}}{(1-k^2)L_1}$
	i_{L2}	$\frac{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)V_{in}}{(1-k^2)L_2}$	$\frac{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)V_{in}-\left(V_{02}+k\sqrt{\frac{L_2}{L_1}}V_{01}\right)}{(1-k^2)L_2}$	$\frac{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)V_{in}-V_{02}}{(1-k^2)L_2}$	$\frac{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)V_{in}-k\sqrt{\frac{L_2}{L_1}}V_{01}}{(1-k^2)L_2}$
Buck -boost	i_{L1}	$\frac{(1+k\sqrt{\frac{L_1}{L_2}})V_{in}}{(1-k^2)L_1}$	$\frac{-V_{o1}-k\sqrt{\frac{L_1}{L_2}}V_{o2}}{(1-k^2)L_1}$	$\frac{V_{in}-k\sqrt{\frac{L_1}{L_2}}V_{o2}}{(1-k^2)L_1}$	$\frac{-V_{o1}+k\sqrt{\frac{L_1}{L_2}}V_{in}}{(1-k^2)L_1}$
	i_{L2}	$\frac{(1+k\sqrt{\frac{L_2}{L_1}})V_{in}}{(1-k^2)L_2}$	$\frac{-k\sqrt{\frac{L_2}{L_1}}V_{o1}-V_{o2}}{(1-k^2)L_2}$	$\frac{k\sqrt{\frac{L_2}{L_1}}V_{in}-V_{o2}}{(1-k^2)L_2}$	$\frac{V_{in}-k\sqrt{\frac{L_2}{L_1}}V_{o1}}{(1-k^2)L_2}$

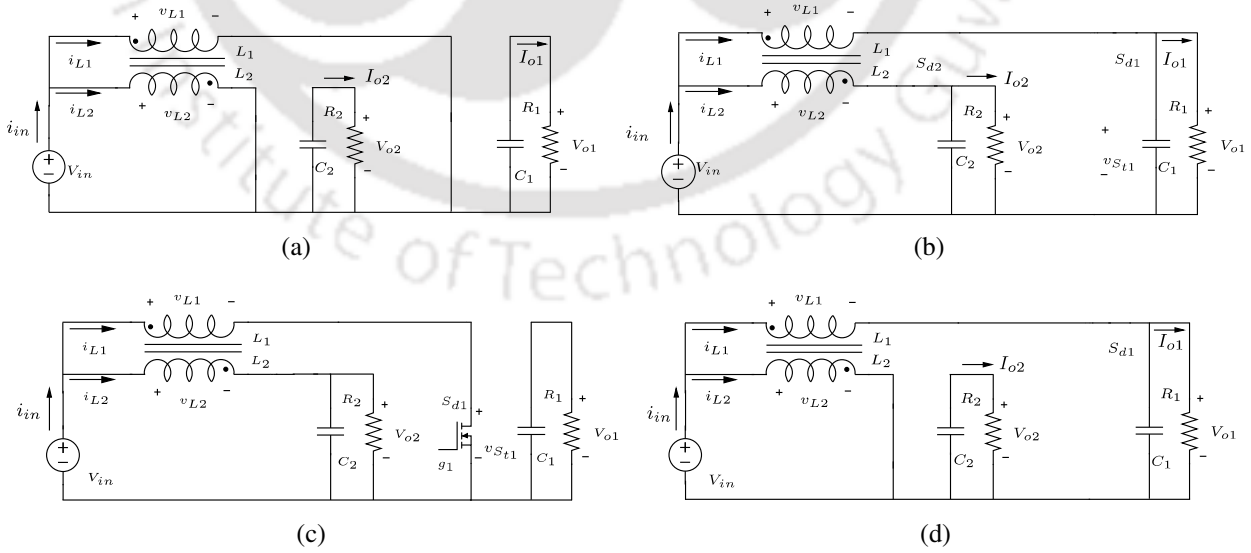


Figure 2.10: Equivalent circuits of CI-SIDO boost in different states: (a) NN, (b) FF, (c) NF and (d) FN.

2.5.2 Slopes of Inductor Currents in CI-SIDO Boost Converter

The detailed discussions on the four operating states of CI-SIDO boost converter is presented in this section.

NN: The equivalent circuit in this state is shown in Fig. 2.10(a). In this state, S_{t1} and S_{t2} both are ON simultaneously. The voltage across the inductor windings are presented in (2.40).

$$v_{L1} = V_{in}, \tag{2.40a}$$

$$v_{L2} = V_{in} \tag{2.40b}$$

The slope of inductor currents in this state can be formulated by combining (2.30) and (2.40). The obtained slopes in this state are obtained in (2.41).

$$G_{NN1} = \frac{\left(1 + k\sqrt{\frac{L_1}{L_2}}\right) V_{in}}{(1 - k^2) L_1}, \tag{2.41a}$$

$$G_{NN2} = \frac{\left(1 + k\sqrt{\frac{L_2}{L_1}}\right) V_{in}}{(1 - k^2) L_2} \tag{2.41b}$$

FF: The equivalent circuit in this state is shown in Fig. 2.10(b). In this state, S_{t1} and S_{t2} both are OFF simultaneously. The voltage across the inductor windings are presented in (2.42).

$$v_{L1} = V_{in} - V_{o1}, \tag{2.42a}$$

$$v_{L2} = V_{in} - V_{o2} \tag{2.42b}$$

The slope of inductor currents in this state can be formulated by combining (2.30) and (2.42). The obtained slopes in this state are obtained in (2.43).

$$G_{FF1} = \frac{\left(1 + k\sqrt{\frac{L_1}{L_2}}\right) V_{in} - \left(V_{01} + k\sqrt{\frac{L_1}{L_2}} V_{02}\right)}{(1 - k^2) L_1}, \tag{2.43a}$$

$$G_{FF2} = \frac{\left(1 + k\sqrt{\frac{L_2}{L_1}}\right) V_{in} - \left(V_{02} + k\sqrt{\frac{L_2}{L_1}} V_{01}\right)}{(1 - k^2) L_2} \tag{2.43b}$$

NF: The equivalent circuit in this state is shown in Fig. 2.10(c). In this state, S_{t1} is ON and S_{t2} is OFF. The voltage across the inductor windings are presented in (2.44).

$$v_{L1} = V_{in}, \tag{2.44a}$$

$$v_{L2} = V_{in} - V_{o2} \tag{2.44b}$$

The slope of inductor currents in this state can be formulated by combining (2.30) and (2.44). The obtained slopes in this state are obtained in (2.45).

$$G_{NF1} = \frac{\left(1 + k\sqrt{\frac{L_1}{L_2}}\right)V_{in} - k\sqrt{\frac{L_1}{L_2}}V_{02}}{(1-k^2)L_1}, \tag{2.45a}$$

$$G_{NF2} = \frac{\left(1 + k\sqrt{\frac{L_2}{L_1}}\right)V_{in} - V_{02}}{(1-k^2)L_2} \tag{2.45b}$$

FN: The equivalent circuit in this state is shown in Fig. 2.10(d). In this state, S_{t1} is OFF and S_{t2} is ON. The voltage across the inductor windings are presented in (2.46).

$$v_{L1} = V_{in} - V_{o1}, \tag{2.46a}$$

$$v_{L2} = V_{in} \tag{2.46b}$$

The slope of inductor currents in this state can be formulated by combining (2.30) and (2.46). The obtained slopes in this state are obtained in (2.47).

$$G_{FN1} = \frac{\left(1 + k\sqrt{\frac{L_1}{L_2}}\right)V_{in} - V_{01}}{(1-k^2)L_1} \tag{2.47a}$$

$$G_{FN2} = \frac{\left(1 + k\sqrt{\frac{L_2}{L_1}}\right)V_{in} - k\sqrt{\frac{L_2}{L_1}}V_{01}}{(1-k^2)L_2} \tag{2.47b}$$

The slopes of the inductor currents in all the four states are presented in Table 2.2. Thus, the voltage across v_{L1} are given by (2.48).

$$v_{L1} = \begin{cases} V_{in} \text{ if } S_{t1} \text{ ON}, \\ V_{in} - V_{o1} \text{ if } S_{t1} \text{ OFF}. \end{cases} \tag{2.48}$$

Applying the volt-sec balance across v_{L1}, we obtain:

$$V_{in}D_1T_s + (V_{in} - V_{o1})(1 - D_1)T_s = 0, \tag{2.49a}$$

$$\implies \frac{V_{o1}}{V_{in}} = \frac{1}{(1 - D_1)}. \tag{2.49b}$$

In the CI-SIDO boost converter, the output voltage depends on the input voltage and the duty ratio only, as presented in (2.49). The coupling does not affect the output voltages. Similarly, it is true for V_{o2}. Therefore, the input-output voltage relations are given by:

$$V_{o1} = \frac{V_{in}}{1 - D_1}, \tag{2.50a}$$

$$V_{o2} = \frac{V_{in}}{1 - D_2} \tag{2.50b}$$

where, D_1 and D_2 are duty ratios of S_{t1} and S_{t2} respectively. It can be seen from (2.50) that output voltage V_{o1} and V_{o2} are not coupled i.e. unaffected by each other in CCM. So, duty ratios D_1 and D_2 also are not affected by mutual coupling in CCM.

2.5.3 Slopes of Inductor Currents in CI-SIDO Buck-Boost

The detailed discussions on the four operating states of CI-SIDO buck-boost converter is presented in this section. *NN*: The equivalent circuit in this state is shown in Fig. 2.11(a). In this state, S_{t1} and S_{t2} both are ON simultaneously. The voltage across the inductor windings are presented in (2.51).

$$v_{L1} = V_{in}, \tag{2.51a}$$

$$v_{L2} = V_{in} \tag{2.51b}$$

The slope of inductor currents in this state can be formulated by combining (2.30) and (2.51). The obtained slopes in this state are obtained in (2.52).

$$G_{NN1} = \frac{(1 + k\sqrt{\frac{L_1}{L_2}})V_{in}}{(1 - k^2)L_1}, \tag{2.52a}$$

$$G_{NN2} = \frac{(1 + k\sqrt{\frac{L_2}{L_1}})V_{in}}{(1 - k^2)L_2} \tag{2.52b}$$

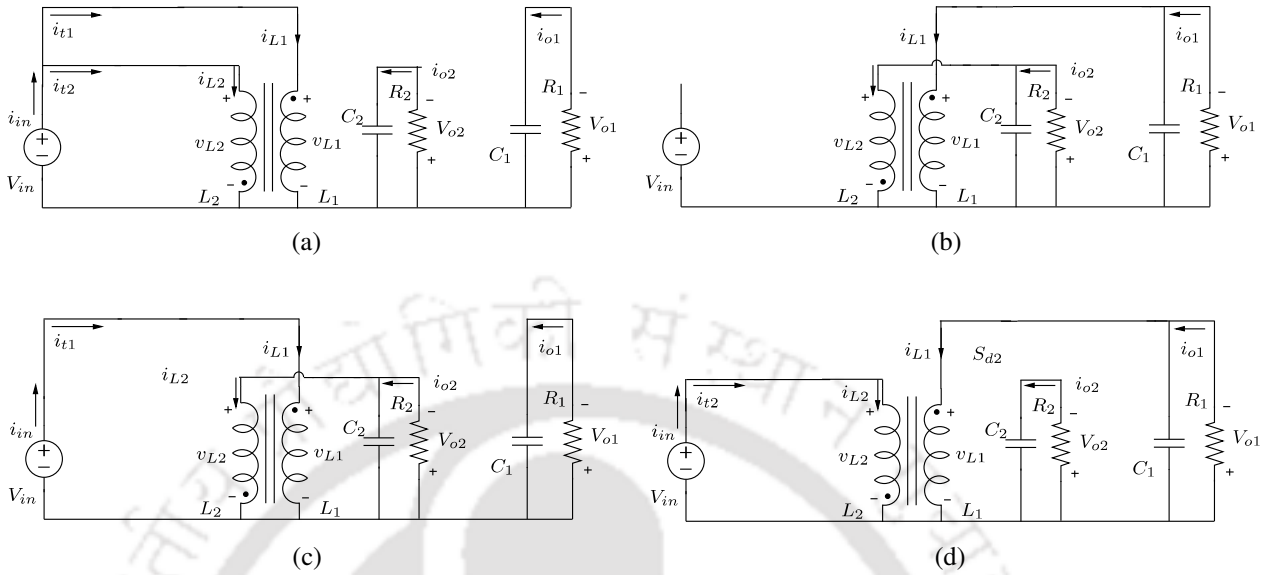


Figure 2.11: Equivalent circuits of CI-SIDO buck-boost in different states: (a) NN, (b) FF, (c) NF and (d) FN.

FF: The equivalent circuit in this state is shown in Fig. 2.11(b). In this state, S_{t1} and S_{t2} both are OFF simultaneously. The voltage across the inductor windings are presented in (2.53).

$$v_{L1} = -V_{o1}, \tag{2.53a}$$

$$v_{L2} = -V_{o2} \tag{2.53b}$$

The slope of inductor currents in this state can be formulated by combining (2.30) and (2.53). The obtained slopes in this state are obtained in (2.54).

$$G_{FF1} = \frac{-V_{o1} - k\sqrt{\frac{L_1}{L_2}}V_{o2}}{(1-k^2)L_1}, \tag{2.54a}$$

$$G_{FF2} = \frac{-k\sqrt{\frac{L_2}{L_1}}V_{o1} - V_{o2}}{(1-k^2)L_2} \tag{2.54b}$$

NF: The equivalent circuit in this state is shown in Fig. 2.11(c). In this state, S_{t1} is ON and S_{t2} is OFF. The voltage across the inductor windings are presented in (2.55).

$$v_{L1} = V_{in}, \tag{2.55a}$$

$$v_{L2} = -V_{o2} \tag{2.55b}$$

The slope of inductor currents in this state can be formulated by combining (2.30) and (2.55). The obtained slopes in this state are obtained in (2.56).

$$G_{NF1} = \frac{V_{in} - k\sqrt{\frac{L_1}{L_2}}V_{o2}}{(1-k^2)L_1}, \tag{2.56a}$$

$$G_{NF2} = \frac{k\sqrt{\frac{L_2}{L_1}}V_{in} - V_{o2}}{(1-k^2)L_2} \tag{2.56b}$$

FN: The equivalent circuit in this state is shown in Fig. 2.11(d). In this state, S_{t1} is OFF and S_{t2} is ON. The voltage across the inductor windings are presented in (2.57).

$$v_{L1} = -V_{o1}, \tag{2.57a}$$

$$v_{L2} = V_{in} \tag{2.57b}$$

The slope of inductor currents in this state can be formulated by combining (2.30) and (2.57). The obtained slopes in this state are obtained in (2.58).

$$G_{FN1} = \frac{-V_{o1} + k\sqrt{\frac{L_1}{L_2}}V_{in}}{(1-k^2)L_1}, \tag{2.58a}$$

$$G_{FN2} = \frac{V_{in} - k\sqrt{\frac{L_2}{L_1}}V_{o1}}{(1-k^2)L_2} \tag{2.58b}$$

The slopes of the inductor currents in all the four states are presented in Table 2.2. In continuous conduction mode (CCM), making the average voltage across inductors zero over switching time period T_s, we obtain:

$$V_{o1} = \frac{D_1 V_{in}}{1 - D_1}, \tag{2.59a}$$

$$V_{o2} = \frac{D_2 V_{in}}{1 - D_2} \tag{2.59b}$$

where, D_1 and D_2 are duty ratios of S_{t1} and S_{t2} respectively. It can be seen from (2.59) that output voltage V_{o1} and V_{o2} are not coupled i.e. unaffected by each other in CCM. Also, duty ratios D_1 and D_2 are not affected by mutual coupling in CCM.

2.6 36 Possible Conditions in Either Inductor Current

All the slope expressions of CI-SIDO converters are analysed and following can be noted:

(i) The slopes, of either of the inductor currents, are different in different states.

(ii) For any particular state, the slope of inductor current i_{L1} is different than the slope of i_{L2}.

(iii) For any values of duty ratios D_1, D_2: $G_{NNw} > 0$ and $G_{FFw} < 0$, as $0 < V_{in} < \{V_{o1}, V_{o2}\}$.

(iv) In steady state, the change in the inductor current over a switching period is zero. The inductor current waveform is periodic, i.e., $i_{Lw}(nT_s) = i_{Lw}((n+1)T_s)$. The inductor current waveforms are not feasible where the periodic waveforms are not possible.

(v) From above, it is also summarised below–

$$\text{When } G_{NFw} > 0,\ G_{FNw} > 0 \text{ then } D_1 + D_2 < 1 \tag{2.60a}$$

$$\text{When } G_{NFw} < 0,\ G_{FNw} < 0 \text{ then } D_1 + D_2 > 1 \tag{2.60b}$$

$$\text{When } G_{NFw} = 0,\ G_{FNw} > 0 \text{ then } D_1 + D_2 < 1 \tag{2.60c}$$

$$\text{When } G_{NFw} = 0,\ G_{FNw} < 0 \text{ then } D_1 + D_2 > 1 \tag{2.60d}$$

$$\text{When } G_{NFw} > 0,\ G_{FNw} = 0 \text{ then } D_1 + D_2 < 1 \tag{2.60e}$$

$$\text{When } G_{NFw} < 0,\ G_{FNw} = 0 \text{ then } D_1 + D_2 > 1 \tag{2.60f}$$

(vi) It can also be shown that $G_{NNw} > G_{NFw}$ if $G_{NFw} > 0$. For example, if $w = 1$, we observe that

$$k\sqrt{\frac{L_1}{L_2}}V_{o2} > 0 \implies -k\sqrt{\frac{L_1}{L_2}}V_{o2} < 0 \tag{2.61a}$$

$$\implies \left(1 + k\sqrt{\frac{L_1}{L_2}}\right)V_{in} - k\sqrt{\frac{L_1}{L_2}}V_{o2} < \left(1 + k\sqrt{\frac{L_1}{L_2}}\right)V_{in} \tag{2.61b}$$

$$\implies G_{NF1} < G_{NN1} \tag{2.61c}$$

Table 2.3: 36 possible conditions in either inductor currents

Sl. No.	$D_1 + D_2$	Relation of D_1, D_2	Slope possibilities
1	< 1	$D_1 < D_2$	$G_{NFw} > 0, G_{NFw} > 0$
2			$G_{NFw} > 0, G_{NFw} < 0$
3			$G_{NFw} < 0, G_{NFw} > 0$
4			$G_{NFw} = 0, G_{NFw} > 0$
5			$G_{NFw} > 0, G_{NFw} = 0$
6	< 1	$D_1 > D_2$	$G_{NFw} > 0, G_{NFw} > 0$
7			$G_{NFw} > 0, G_{NFw} < 0$
8			$G_{NFw} < 0, G_{NFw} > 0$
9			$G_{NFw} = 0, G_{NFw} > 0$
10			$G_{NFw} > 0, G_{NFw} = 0$
11	< 1	$D_1 = D_2$	$G_{NFw} > 0, G_{NFw} > 0$
12			$G_{NFw} > 0, G_{NFw} < 0$
13			$G_{NFw} < 0, G_{NFw} > 0$
14			$G_{NFw} = 0, G_{NFw} > 0$
15			$G_{NFw} > 0, G_{NFw} = 0$
16	> 1	$D_1 < D_2$	$G_{NFw} < 0, G_{NFw} < 0$
17			$G_{NFw} > 0, G_{NFw} < 0$
18			$G_{NFw} < 0, G_{NFw} > 0$
19			$G_{NFw} = 0, G_{NFw} < 0$
20			$G_{NFw} < 0, G_{NFw} = 0$
21	> 1	$D_1 > D_2$	$G_{NFw} < 0, G_{NFw} < 0$
22			$G_{NFw} > 0, G_{NFw} < 0$
23			$G_{NFw} < 0, G_{NFw} > 0$
24			$G_{NFw} = 0, G_{NFw} < 0$
25			$G_{NFw} < 0, G_{NFw} = 0$
26	> 1	$D_1 < D_2$	$G_{NFw} < 0, G_{NFw} < 0$
27			$G_{NFw} > 0, G_{NFw} < 0$
28			$G_{NFw} < 0, G_{NFw} > 0$
29			$G_{NFw} = 0, G_{NFw} < 0$
30			$G_{NFw} < 0, G_{NFw} = 0$
31	$= 1$	$D_1 < D_2$	$G_{NFw} > 0, G_{NFw} < 0$
32			$G_{NFw} < 0, G_{NFw} > 0$
33	$= 1$	$D_1 > D_2$	$G_{NFw} > 0, G_{NFw} < 0$
34			$G_{NFw} < 0, G_{NFw} > 0$
35	$= 1$	$D_1 = D_2$	$G_{NFw} > 0, G_{NFw} < 0$
36			$G_{NFw} < 0, G_{NFw} > 0$

Similarly, it can be proved for other slope expressions as–

$$G_{NNw} > G_{NFw} \text{ if } G_{NFw} > 0 \tag{2.62a}$$

$$G_{NNw} > G_{FNw} \text{ if } G_{FNw} > 0 \tag{2.62b}$$

$$|G_{FFw}| > |G_{NFw}| \text{ if } G_{NFw} < 0 \tag{2.62c}$$

$$|G_{FFw}| > |G_{FNw}| \text{ if } G_{FNw} < 0 \tag{2.62d}$$

From the analysis of CI-SIDO converters, we found that–

(i) D_1 can be >, < or = D_2,

(ii) $(D_1 + D_2)$ can be >, < or = 1,

(iii) G_{NFw} and G_{FNw} can be >, <, or = 0, depending on the values of V_{o1}, V_{o2}, V_{in}, L_1, L_2 and k chosen to design the CI-SIDO converters.

Based on the values of $(D_1 + D_2)$ and relative values of D_1 and D_2, $3 \times 3 = 9$ conditions are possible. And including the signs of G_{NFw} and G_{FNw}, a total of $9 \times 9 = 81$ conditions are possible. Using (2.60), 45 out of 81 conditions are excluded from the analysis as:

(i) when $(D_1 + D_2) < 1$ then $G_{NFw} < 0$, $G_{FNw} < 0$, $G_{NFw} = 0$, $G_{FNw} < 0$, or $G_{NFw} < 0$, $G_{FNw} = 0$ are not possible

(ii) when $(D_1 + D_2) > 1$ then $G_{NFw} > 0$, $G_{FNw} > 0$, $G_{NFw} = 0$, $G_{FNw} > 0$, or $G_{NFw} > 0$, $G_{FNw} = 0$ are not possible

(iii) when $(D_1 + D_2) = 1$ then G_{NFw} and G_{FNw} both cannot be < or > 0 and either G_{NFw} and G_{FNw} = 0 is not possible

Therefore, 36 conditions are possible for either inductor current i_{Lw}, as presented in Table 2.3. The rows of the table represent all the 36 possibilities and the columns of the table represent all the possibilities of D_1, D_2 and the slope possibilities. The table lists all the possible inductor current waveforms possibilities. It is found that with change in any parameters of the converter like D_1,

D_2, D_t, L_1, L_2, k, the inductor current waveform patterns change. As the pattern of waveforms are changed, the ripple expressions change as well. The same scenario repeats as the topology of CI-SIDO converter changes.

2.7 Challenges in Minimizing Current Ripples in CI-SIDO Converters

It is observed that the inductor current ripples depend on the input and output voltages, duty ratios, pattern of the gate pulse and the values of the coupled inductor. The ripples do not depend on the load currents/output power/load demands. It can be observed from (2.39), (2.50), (2.59) that V_{o1} and V_{o2} are independent of the relative arrangement of gate pulses g_1 and g_2. So, relative shift between g_1 and g_2 does not affect the outputs. The relative shift is denoted by ratio D_t, and it varies between 0 and 1.

From the above analysis, we came across the following challenges –

(i) 36 inductor current possibilities are formed for either inductor current depending on $D_1 + D_2 >$, $<$, $= 1$, $D_1 > D_2$, $D_1 < D_2$, $D_1 = D_2$ and slope conditions, in each of the three CI-SIDO converters.

(ii) Different patterns of inductor currents are observed in different conditions. Inductor current pattern change with change in value of coupled inductors.

(iii) Numerous patterns and sequence of states are obtained when D_2 is shifted w.r.t. D_1 by D_t.

(iv) Expressions of inductor current ripples vary and depend on the pattern of inductor current.

(v) Separate analysis is required for each CI-SIDO converter and different values of D_1, D_2, D_t, L_1, L_2 and k.

(vi) It is not known which pattern of inductor current and values of D_1, D_2, D_t, L_1, L_2 and k are suitable for converters operation, among the numerous possibilities.

Therefore, a unified approach is required for CI-SIDO converters which simplifies and reduces the tedious analysis of numerous cases.

2.8 Summary of the Chapter

The following are the summary of the chapter:

(i) The CI-SIDO boost, buck, buck-boost converters have four different operating states in CCM, namely NN, FF, NF, FN.

(ii) The slopes of either inductor currents are different in different states.

(iii) In particular state, the slope of i_{L1} is different from the slope of i_{L2}.

(iv) For each CI-SIDO converter, 36 conditions are possible for either inductor current.

(v) The inductor current ripples depend on the input and output voltages, duty ratios, pattern of the gate pulse and the values of the coupled inductor.

(vi) The inductor current ripples do not depend on the load currents/output power/load demands.

3

Unifying Inductor Current Ripples by Forming Sectors of Duty Ratios

Contents

3.1 Introduction

[1] To evaluate the performance of each CI-SIDO converter, a separate analysis of all 36 cases is required. Moreover, inductor current patterns also depend on the pattern of gate pulses. If a shift in gate pulse is introduced between the two gate pulses, the waveform patterns change further. Thus, increasing the number of inductor current patterns. A separate analysis of each pattern is required for different values of output-input voltages, i.e., duty ratios and coupled inductor parameters for all three CI-SIDO converters. The separate analysis of each pattern is very tedious, which restricts the usage of CI-SIDO converters. Amongst the numerous inductor current patterns, which pattern is more suitable for the operation of the CI-SIDO converters is also not known. Therefore, a unified approach is required for CI-SIDO converters which simplifies and reduces the tedious analysis.

3.2 Basis of Sector Formations

Main idea behind forming sectors of duty ratios is to find different ranges of duty ratios D_1 and D_2 in terms of coupled inductor parameters k, L_1, L_2; such that in one particular range, pattern of inductor current waveforms remain same even if duty ratios vary. These different ranges of duty ratios are called as sectors. The formation of sectors make the pattern of inductor current waveforms foreseeable. Using the values of coupled inductor parameters, first it has to be determined that a given set of duty ratios lay in which sector. Once the sector is known, the pattern of waveforms of both i_{L1} and i_{L2} are evident from the sector diagram. The formation of sectors of duty ratios simplifies and reduces the tedious analysis of numerous cases. As numerous patterns of inductor currents are possible for these CI-SIDO converters depending on the coupled inductor parameters and duty ratios, it is difficult to analyze the numerous possibilities individually. The inductor current patterns also depend on the gate pulse patterns. With the change in the patterns, inductor current ripples change. The separate analysis of each pattern is very tedious, which restricts the usage of CI-SIDO converters.

[1]Major part of this chapter is reproduced from my publications: (i) Nupur and S. Nath, "Minimizing Ripples of Inductor Currents in Coupled SIDO Boost Converter by Shift of Gate Pulses," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1217–1226, Feb. 2020. (ii) Nupur and S. Nath, "Inductor Current Ripples Minimization in Coupled SIDO Buck and Buck-Boost Converter by Gate Pulse Shifting," in *Proc. Int. Conf. Power Electron., Drives Energy Syst.*, Dec. 2020, pp. 1-6. (iii) Nupur and S. Nath, "Unifying Inductor Current Ripples and Inductor Design in Coupled SIDO Converters by Forming Sectors of Duty Ratios," in *IEEE Trans. Ind. Appl.*, vol. 58, no. 3, pp. 3830-3839, May-Jun. 2022.

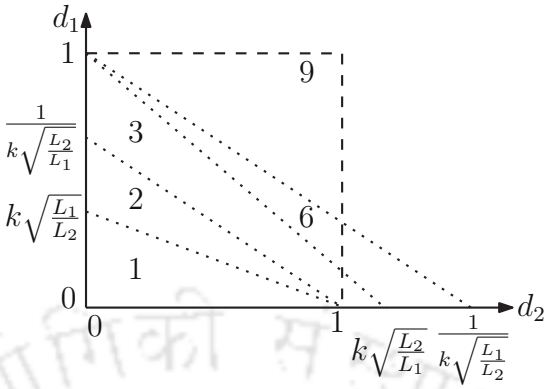


Figure 3.1: Sector diagram of CI-SIDO buck converter for $k\sqrt{\frac{L_1}{L_2}} < 1$ and $k\sqrt{\frac{L_2}{L_1}} > 1$.

Hence, a unified approach is required for the CI-SIDO converters which simplifies and reduces the tedious analysis. The proposed sectors of duty ratios unifies –

- the patterns of inductor currents.
- the expressions of current ripples for any values of D_1, D_2, L_1, L_2 and k.
- the shift that gives the minimum inductor current ripples.
- the design of coupled inductors.

3.3 Proposed Unified Current Ripples by Forming Sectors of Duty Ratios

We propose 9 sectors of duty ratios for CI-SIDO converters such that the slope conditions, the minimum inductor current ripple expressions, the shift in gate pulse for the minimum inductor current ripples, and the design of coupled inductors get unified for CI-SIDO buck, boost, and buck-boost. The proposed sector diagrams for CI-SIDO buck is shown in Fig. 3.1 and CI-SIDO boost as well as buck-boost is shown in Fig. 3.2 where Table 3.1 holds true. The rows of the table represents the four slope conditions and the columns represent the conditions when the corresponding slope conditions are positive for CI-SIDO buck, and boost, buck-boost. The condition presented in the table is required to obtain the sector formation of CI-SIDO converters. For all the 9 sectors, the conditions of the unified slope are given in Table 3.2, the unified minimum inductor current ripple expressions are given by Table 3.3. The rows of Table 3.2 represents the 9 sectors and columns represent the signs of slopes

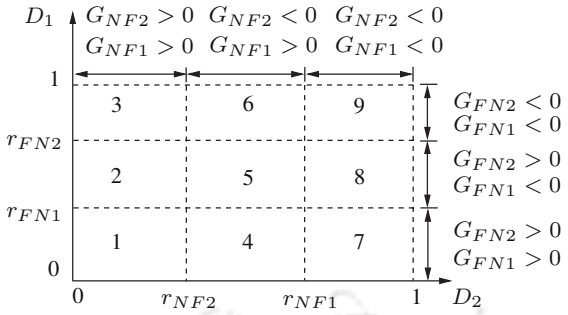


Figure 3.2: Nine sectors of CI-SIDO boost converter and CI-SIDO buck-boost converter (Dotted line represents $G_{NFw} = 0$ or $G_{FNw} = 0$).

G_{NF1}, G_{NF2}, G_{FN1}, G_{FN2}. If the duty ratios are known, this table helps to find the sector in which the CI-SIDO converter is operating. The rows of Table 3.3 represents the values of $D_1 + D_2$ and the columns represent the sign of G_{NF_w}, G_{NF_w} and the inductor current ripple expressions. The minimum inductor current ripple expressions presented in the table helps to get the percentage reduction in the inductor current ripples.

The sector diagram for boost converter is shown in Fig. 3.2 which is a D_1 versus D_2 graph. Fig. 3.2 shows the different ranges of D_1 and D_2 in which the slopes G_{NFw} and G_{FNw} are positive and negative. Depending on the slopes being $<$ or $>$ 0, the values of D_1 and D_2 can be divided in 9 different sectors. In each sector the combination of signs of slopes G_{NFw} and G_{FNw} is different from that in other sectors. Further, the patterns of both inductor current waveforms i_{L1} and i_{L2} may be same or different depending on the signs of slopes. So, in sectors 1, 3, 7, and 9, the patterns of waveforms of i_{L1} and i_{L2} are going to be same, and they are different in sectors 2, 4, 5, 6 and 8. A sector diagram for the CI-SIDO buck converter is drawn in Fig. 3.1 which is D_1 versus D_2 graph. The sector diagram is presented for $k\sqrt{\frac{L_1}{L_2}} < 1$ and $k\sqrt{\frac{L_2}{L_1}} > 1$. The sector diagram shows the ranges of D_1 and D_2 in which the slopes G_{NFw} and G_{FNw} are positive and negative. Depending on the slopes being $<$ or $>$ or $= 0$, the values of D_1 and D_2 can be divided into different sectors. In each sector the combination of signs of slopes G_{NFw} and G_{FNw} is different from that in other sectors. It is found that only five sectors are formed for this values of coupled inductor parameters. Only sectors 1, 2, 3, 6, and 9 are formed for $k\sqrt{\frac{L_1}{L_2}} < 1$ and $k\sqrt{\frac{L_2}{L_1}} > 1$. In sectors 1, 3, and 9, the patterns of waveforms of i_{L1} and i_{L2} are going to be same, and they are different in sectors 2 and 6. It can also be noted that the signs of G_{NFw} and G_{FNw} in sectors 1, 2, 3, 6, and 9 are same as CI-SIDO boost converter.

Table 3.1: Conditions for G_{NFw} and G_{FNw} to be positive

Slope	CI-SIDO		
condition	buck	boost	buck-boost
$G_{NF1} > 0$	$D_1 + k\sqrt{\frac{L_1}{L_2}}D_2 < 1$	$D_2 < r_{NF1}$	
$G_{NF2} > 0$	$k\sqrt{\frac{L_2}{L_1}}D_1 + D_2 < k\sqrt{\frac{L_2}{L_1}}$	$D_2 < r_{NF2}$	
$G_{FN1} > 0$	$D_1 + k\sqrt{\frac{L_1}{L_2}}D_2 < k\sqrt{\frac{L_1}{L_2}}$	$D_1 < r_{FN1}$	
$G_{FN2} > 0$	$k\sqrt{\frac{L_2}{L_1}}D_1 + D_2 < 1$	$D_1 < r_{FN2}$	

where, $r_{NF1} = \frac{1}{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)}$, $r_{NF2} = \frac{k\sqrt{\frac{L_2}{L_1}}}{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)}$

$r_{FN1} = \frac{k\sqrt{\frac{L_1}{L_2}}}{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)}$, $r_{FN2} = \frac{1}{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)}$

Table 3.2: Unified slope conditions for each sector of CI-SIDO buck, boost, buck-boost converters

Sector	Slopes sign			
No.	G_{NF1}	G_{NF2}	G_{FN1}	G_{FN2}
1	> 0	> 0	> 0	> 0
2	> 0	> 0	< 0	> 0
3	> 0	> 0	< 0	< 0
4	> 0	< 0	> 0	> 0
5	> 0	< 0	< 0	> 0
6	> 0	< 0	< 0	< 0
7	< 0	< 0	> 0	> 0
8	< 0	< 0	< 0	> 0
9	< 0	< 0	< 0	< 0

Table 3.3: Unified minimum expressions of Δi_{Lw} for CI-SIDO buck, boost, buck-boost

$D_1 + D_2$	G_{NFw}	G_{FNw}	Δi_{Lw}
$<$	$+$	$+$	$\max\{G_{NFw}D_1T_s, G_{FNw}D_2T_s\}$
	$+$	$-$	$G_{NFw}D_1T_s$
	$-$	$+$	$G_{FNw}D_2T_s$
$>$	$-$	$-$	$\max\{\lvert G_{NFw}\rvert(1 - D_2)T_s, \lvert G_{FNw}\rvert(1 - D_1)T_s\}$
	$+$	$-$	$G_{NNw}(D_1 + D_2 - 1)T_s + G_{NFw}(1 - D_2)T_s$
	$-$	$+$	$G_{NNw}(D_1 + D_2 - 1)T_s + G_{FNw}(1 - D_1)T_s$
$=$	$+$	$-$	$G_{NFw}D_1T_s$
	$-$	$+$	$G_{FNw}D_2T_s$

3.4 Proof of Unified Current Ripples by Using the Proposed Sectors of Duty Ratios

3.4.1 Unified Patterns of Inductor Currents

Suppose we select a waveform from Sector 6 such that $D_1 + D_2 > 1$ and $D_1 > D_2$. From Table 3.2, the slope conditions are $G_{NF1} > 0$, $G_{FN1} < 0$, $G_{NF2} < 0$, and $G_{FN2} < 0$. From Fig. 3.2 and Table 3.1, the condition for $G_{NF1} > 0$ in CI-SIDO boost is–

$$D_2 < \frac{1}{\left(1 + k\sqrt{\frac{L_1}{L_2}}\right)} \tag{3.1}$$

Using (2.6), this equation reduces to–

$$\left(1 + k\sqrt{\frac{L_1}{L_2}}\right) V_{in} - k\sqrt{\frac{L_1}{L_2}} V_{02} > 0 \tag{3.2}$$

Dividing the above expression by $\left(1 - k^2\right) L_1$, we get $G_{NF1} > 0$. Similarly, the slope conditions $G_{FN1} < 0$, $G_{NF2} < 0$, and $G_{FN2} < 0$ are proved. Therefore, the obtained waveform for CI-SIDO boost is presented in Fig. 3.3(a).

Likewise from Fig. 3.1 and Table 3.1, the condition for $G_{NF1} > 0$ in CI-SIDO buck converter is–

$$D_1 + k\sqrt{\frac{L_1}{L_2}} D_2 < 1 \tag{3.3}$$

Using (2.39), this equation reduces to–

$$V_{in} - V_{o1} - k\sqrt{\frac{L_1}{L_2}} V_{o2} > 0 \tag{3.4}$$

Dividing the above expression by $\left(1 - k^2\right) L_1$, we get $G_{NF1} > 0$ for CI-SIDO buck converter. Similarly, the slope conditions $G_{FN1} < 0$, $G_{NF2} < 0$, and $G_{FN2} < 0$ are proved. Therefore, the obtained waveform for CI-SIDO buck converter is presented in Fig. 3.3(a).

Thus, we observe that the same waveform is obtained for CI-SIDO buck and boost. Also, the sector diagrams of CI-SIDO buck-boost are the same as CI-SIDO boost. Therefore, the same waveform of Fig. 3.3(a) is obtained for Sector 6 of all the CI-SIDO converters.

Similarly, the waveform shown in Fig. 3.3(b) operates in Sector 8 for all the CI-SIDO converters.

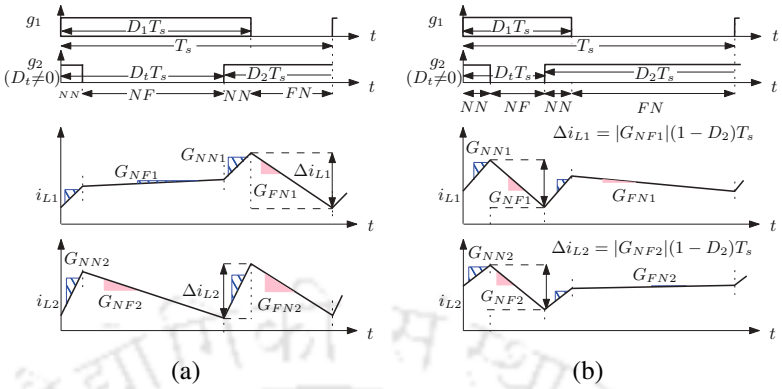


Figure 3.3: The inductor current waveforms for (a) $G_{NF1} > 0$, $G_{FN1} < 0$, $G_{NF2} < 0$, and $G_{FN2} < 0$ and (b) $G_{NF1} < 0$, $G_{FN1} < 0$, $G_{NF2} < 0$, and $G_{FN2} > 0$.

Thus, we obtain the unified inductor current patterns for all CI-SIDO converters.

3.4.2 Unified Minimum Inductor Current Ripple Expressions

For the waveform shown in Fig. 3.3(a), the minimum inductor current ripple expressions are given by–

$$\begin{aligned} \Delta i_{L1} &= G_{NN1}(D_1 + D_2 - 1)T_s + G_{NF1}(1 - D_2)T_s, \\ \Delta i_{L2} &= |G_{FN2}|(1 - D_1)T_s. \end{aligned} \tag{3.5}$$

These ripple expressions are matching with the ripple expressions presented in Table 3.3. Similarly, the minimum inductor current ripple expressions for Fig. 3.3(b) is given by–

$$\begin{aligned} \Delta i_{L1} &= |G_{NF1}|(1 - D_2)T_s, \\ \Delta i_{L2} &= G_{NN2}(D_1 + D_2 - 1)T_s + G_{FN2}(1 - D_1)T_s. \end{aligned} \tag{3.6}$$

These ripple expressions are also matching with the ripple expressions presented in Table 3.3. Therefore, the unified minimum ripple expressions for all the possibilities of CI-SIDO converters are presented in Table. 3.3.

3.4.3 Unified Gate Pulse Shift for Minimum Inductor Current Ripples

As the sector formations unifies the inductor current patterns, the inductor current ripples, and the expressions of the minimum inductor current ripples, the gate pulse patterns where inductor current ripples are minimum also get unified. This detailed analysis on the unified gate pulse shift for

minimum inductor current ripples are discussed in Chapter-4.

3.4.4 Unified Design of Coupled Inductors

It is found that the CI-SIDO converter are best to operate in sector 5. The detailed discussion on the unified design of coupled inductor in Sector 5 for the CI-SIDO converters are presented in Chapter-4.

3.5 Examples on Advantages of Sector Formation

The sectors are actually decided by the designer. The designer can design the CI-SIDO converter to operate it in a particular sector.

Example 1: CI-SIDO boost converter has to maintain output voltages of $V_{o1} = 10V$ and $V_{o2} = 8V$. If $V_{in} = 4V$, maximum load is 100 W on either output, and maximum ripple is 0.8% of maximum load current; find suitable values of k, L_1 and L_2. The converter needs to be designed to operate inside (a) sector 5, (b) sector 3.

Solution: $D_1 = 0.6$, $D_2 = 0.5$, $D_1 + D_2 > 1$ and $D_1 > D_2$.

(a) For the converter to operate inside sector 5, $r_{FN1} < D_1 < r_{FN2}$ and $r_{NF2} < D_2 < r_{NF1}$. Using the expressions of r_{NF1}, r_{NF2}, r_{FN1}, r_{FN2}, the condition obtained is shown in (3.7).

$$\frac{k\sqrt{\frac{L_1}{L_2}}}{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)} < 0.6 < \frac{1}{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)} \tag{3.7a}$$

$$\frac{k\sqrt{\frac{L_2}{L_1}}}{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)} < 0.5 < \frac{1}{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)} \tag{3.7b}$$

Solving (3.7), we obtain (3.8).

$$2.25k^2 < \frac{L_1}{L_2} < \frac{1}{k^2} \tag{3.8}$$

We observe that the choice of k and L_1/L_2 are dependent on each other. From the given condition of maximum ripple, $\Delta i_{Lwmax} = 0.1A$. If we choose $k = 0.7$, then $L_1/L_2 = 1.44$. Writing expressions of

$\underline{\Delta i_{Lw}}$ for condition $(D_1 + D_2) > 1$, $D_1 > D_2$ and sector 5 (as given in Table A.5), we obtain (3.9).

$$\underline{\Delta i_{L1}} = G_{NN1}(D_1 + D_2 - 1)T_s + G_{NF1}(1 - D_2)T_s \tag{3.9a}$$

$$\underline{\Delta i_{L2}} = G_{NN2}(D_1 + D_2 - 1)T_s + G_{FN2}(1 - D_1)T_s \tag{3.9b}$$

Two solution of L_1 and L_2 are possible. Substituting V_{in}, V_{o1}, V_{o2}, k, L_1/L_2 in expressions of G_{NN1}, G_{NF1}, G_{NN2} and G_{FN2} we obtain

(*i*) If $\underline{\Delta i_{L1}} = 0.1A$ then $L_1 = 206.7\mu H \Rightarrow L_2 = L_1/1.44 \Rightarrow L_2 = 143.5\mu H \Rightarrow \underline{\Delta i_{L2}} = 0.11A$

(*ii*) If $\underline{\Delta i_{L2}} = 0.1A$ then $L_2 = 164.9\mu H \Rightarrow L_1 = 1.44L_2 \Rightarrow L_1 = 237.5\mu H \Rightarrow \underline{\Delta i_{L1}} = 0.09A$

Since, second case keeps both $\underline{\Delta i_{L1}}$ and $\underline{\Delta i_{L2}}$ within specification of Δi_{Lwmax}, we choose $L_1 = 237.5\mu H$ and $L_2 = 164.9\mu H$.

(b) For the converter to operate inside sector 3, $r_{FN2} < D_1 < 1$ and $0 < D_2 < r_{NF2}$. Using expressions of r_{FN2}, r_{NF2}, the condition obtained is shown in (3.11).

$$\frac{1}{\left(1 + k\sqrt{\frac{L_2}{L_1}}\right)} < 0.6 < 1 \tag{3.11a}$$

$$0 < 0.5 < \frac{k\sqrt{\frac{L_2}{L_1}}}{\left(1 + k\sqrt{\frac{L_2}{L_1}}\right)} \tag{3.11b}$$

Solving (3.11), we obtain (3.12).

$$\frac{1}{k^2} < \frac{L_2}{L_1} \tag{3.12}$$

From the given condition of maximum ripple, $\Delta i_{Lwmax} = 0.1A$. If we choose $k = 0.8$, then $L_1/L_2 = 0.5$. Writing expressions of $\underline{\Delta i_{Lw}}$ for condition $(D_1 + D_2) > 1$, $D_1 > D_2$ and sector 5 (as given in Table A.5), we obtain (3.13).

$$\underline{\Delta i_{L1}} = G_{NN1}(D_1 + D_2 - 1)T_s + G_{NF1}(1 - D_2)T_s \tag{3.13a}$$

$$\underline{\Delta i_{L2}} = G_{NN2}(D_1 + D_2 - 1)T_s + G_{NF2}(1 - D_2)T_s \tag{3.13b}$$

Two solution of L_1 and L_2 are possible. Substituting V_{in}, V_{o1}, V_{o2}, k, L_1/L_2 in expressions of G_{NN1},

G_{NF1}, G_{NN2} and G_{FN2} we obtain

$$(i)\ \text{If } \underline{\Delta i_{L1}} = 0.1A \text{ then } L_1 = 400\mu H \Rightarrow L_2 = L_1/0.5 \Rightarrow L_2 = 800\mu H \Rightarrow \underline{\Delta i_{L2}} = 0.04A \quad (3.14a)$$

$$(ii)\ \text{If } \underline{\Delta i_{L2}} = 0.1A \text{ then } L_2 = 300\mu H \Rightarrow L_1 = 0.5L_2 \Rightarrow L_1 = 150\mu H \Rightarrow \underline{\Delta i_{L1}} = 0.28A \quad (3.14b)$$

Since, first case keeps both $\underline{\Delta i_{L1}}$ and $\underline{\Delta i_{L2}}$ within specification of Δi_{Lwmax}, we choose $L_1 = 400\mu H$ and $L_2 = 800\mu H$. Therefore, it can be observed that the sectors are decided by the designer. For same converter parameters, we can design the CI-SIDO converters to operate in different sectors. For any energy considerations (specific to input and output voltage/current/load demands....etc), we can design the CI-SIDO converters to choose the nature of the current waveforms. This is explained using the following examples.

Example 2: The CI-SIDO converter has to maintain the output voltages of 1.0 V, 1.5 V. The converter should be such that the operation is in sector 1 with available input voltage, V_{in} of 4.5 V.

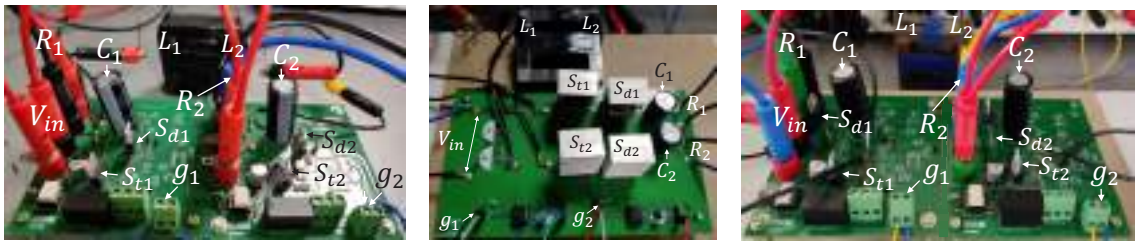
Solution: As the required DC voltages are smaller than V_{in}, the CI-SIDO buck converter is designed. For $V_{o1} = 1.0$ and $V_{o2} = 1.5$, the duty ratios obtained are $D_1 = 0.3$, $D_2 = 0.4$ using (2.39). If $k = 0.8$, $k\sqrt{\frac{L_1}{L_2}} < 1$ and $k\sqrt{\frac{L_2}{L_1}} < 1$, the range of $\frac{L_1}{L_2}$ obtained are $0.14 < \frac{L_1}{L_2} < 4$ using Fig. 3.1. The experimental result for $\frac{L_1}{L_2} = 0.64$ is shown in Fig. 3.6(a). From Table 4.7, the shift $0.5 \subset \mathbf{D}_{min}$. Here, $R_1 = 2.5\ \Omega$ and $R_1 = 4.0\ \Omega$.

Example 3: The CI-SIDO converter has to maintain the output voltages of 10.25 V, 10.0 V. The converter needs to be designed in sector 1 with available input voltage of 8.0 V.

Solution: Here $V_{o1} = 10.25$ and $V_{o2} = 10.0$ which is higher than the available V_{in} of 8 V. Therefore, the CI-SIDO boost converter is designed. The duty ratios obtained are $D_1 = 0.3$, $D_2 = 0.3$ using (2.50). Again, if $k = 0.8$, the range of $\frac{L_1}{L_2}$ obtained are $0.24 < \frac{L_1}{L_2} < 4.2$ using Fig. 3.2. The experimental result with $\frac{L_1}{L_2} = 2.56$ is shown in Fig. 3.6(b). From Table 4.7, the shift $0.5 \subset \mathbf{D}_{min}$. Here, $R_1 = 23\ \Omega$ and $R_1 = 12\ \Omega$.

Example 4: For the available input voltage of 6 V, the CI-SIDO converter has to maintain the output voltages of 1.0 V, 1.8 V. Design the converter in sector 1.

Solution: Here $V_{o1} = 1.0$ and $V_{o2} = 1.8$ and V_{in} of 6 V. Here, the CI-SIDO buck-boost converter is designed. The duty ratios obtained are $D_1 = 0.2$, $D_2 = 0.3$ using (2.59). Again, if $k = 0.8$, the range



(a) (b) (c)

Figure 3.4: Experimental setup of CI-SIDO (a) buck, (b) boost, and (c) buck-boost converters.

Table 3.4: Experimental details

Fig. No.	V_{in} (V)	L_1 (μH)	L_2 (μH)	k	R_1 (Ω)	R_2 (Ω)	D_1	D_2	D_t
3.6(a)	4.5	100	155	0.80	3.0	4.0	0.3	0.4	0.5
3.6(b)	8.0	230	90	0.88	27.0	13.5	0.3	0.3	0.5
3.6(c)	6.0	100	155	0.80	5.0	12.0	0.2	0.3	0.5
3.7(a)	4.5	100	154	0.80	3.0	4.0	0.3	0.3	0.5
3.7(b)	8.0	230	90	0.88	27.0	13.5	0.7	0.6	0.5
3.7(c)	6.0	100	155	0.80	30.0	92.0	0.6	0.8	0.5

of $\frac{L_1}{L_2}$ obtained are $0.1 < \frac{L_1}{L_2} < 4.2$. The experimental result with $\frac{L_1}{L_2} = 2.56$ is shown in Fig. 3.6(c). To maintain CCM operation, $R_1 = 4.0\ \Omega$ and $R_2 = 3.0\ \Omega$. It is to be noted that the obtained V_{o1}, V_{o2} are negative because of the buck-boost converters.

3.6 Experimental Verifications of Unified Inductor Current Patterns and Inductor Current Ripples

The analysis presented in this chapter is verified in laboratory using a prototype of CI-SIDO buck, boost and buck-boost converter as shown in Figs. 3.4(a), 3.4(b), 3.4(c), respectively. The CI-SIDO buck, boost, and buck-boost converters are designed using different values of L_1, L_2, k, V_{in}, R_1, R_2 with $C_1 = C_2 = 100\,\mu F$ and $T_s = 10\,\mu s$. The parameters are presented in Table 3.4. The input voltage is supplied using a regulated DC supply which can supply $64\ V$, $20\ A$. The gate pulses, voltage and the current waveforms are observed and measured in mixed signal oscilloscope (MSO) with differential probes and current probes. The converter parameters are selected based on the availability in our laboratory. However, the analysis presented in this thesis is valid for all the practical parameters of the CI-SIDO converters.

The gate pulses g_1 and g_2 are generated using FPGA kit - NI sbRIO 9637 and programmed in

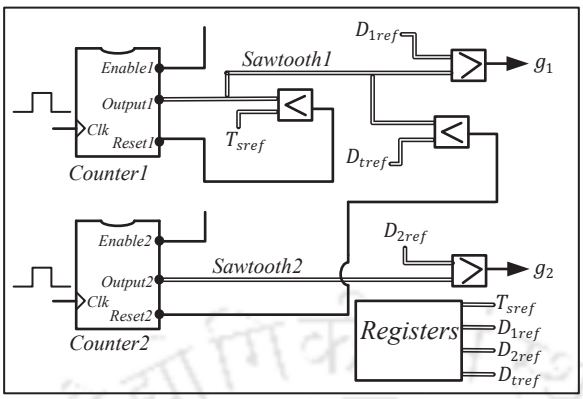


Figure 3.5: Controller block diagram.

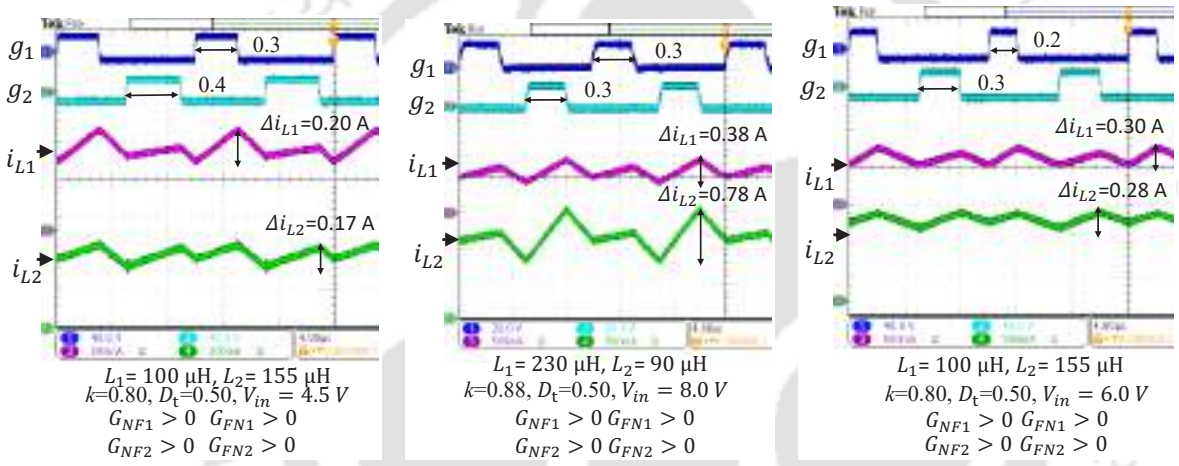


Figure 3.6: Experimental results of CI-SIDO (a) buck, (b) boost, and (c) buck-boost converters in sector 1. Inductor current patterns are same irrespective of different coupled inductors, output and input voltages.

LabVIEW platform. The controller's diagram is shown in Fig. 3.5. As can be seen in figure, the controller is implemented in FPGA mainly using registers, counters and discrete comparators. The control logic generates two sawtooth carrier waveforms which have a relative delay D_{tref} with respect to each other. The gate pulses are generating by comparing D_{1ref} and D_{2ref} with the two sawtooth waveforms.

In Fig. 3.6 even if the coupled inductors are different, the loads, output and input voltages are also different, the patterns of i_{L1}, i_{L2} are same. For all the three converters the unified slope conditions are $G_{NN1} > 0$, $G_{NF1} > 0$, $G_{FN1} > 0$, $G_{FF1} < 0$, $G_{NN2} > 0$, $G_{NF2} > 0$, $G_{FN2} > 0$, $G_{FF2} < 0$, resulting in a unified inductor current patterns. As presented in Table 3.2, this is the condition for Sector 1.

Similarly, a unified pattern of inductor currents are obtained for Sector 9 in Fig. 3.7. The slope

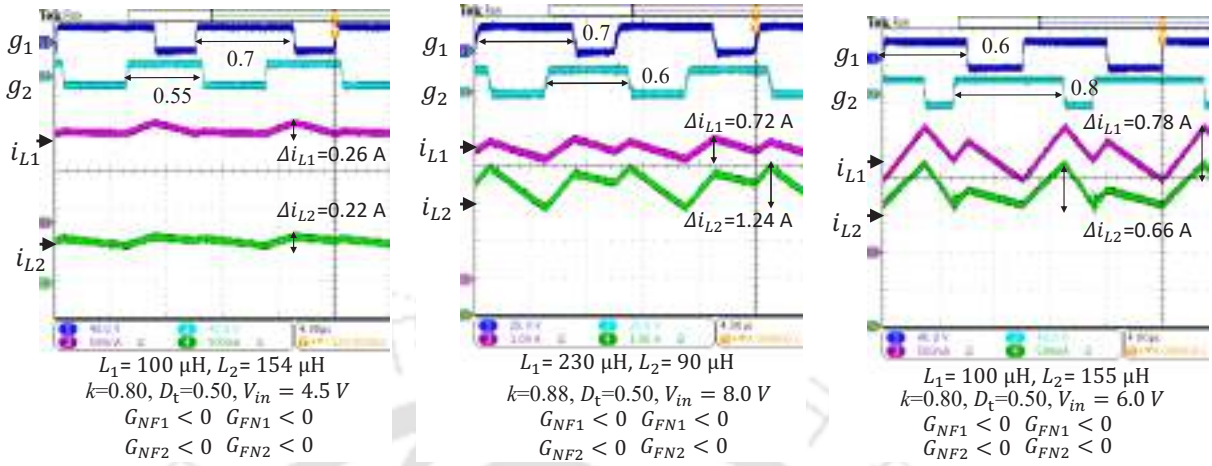


Figure 3.7: Experimental results of CI-SIDO (a) buck, (b) boost, and (c) buck-boost converters in sector 9. Inductor current patterns are same irrespective of different coupled inductors, output and input voltages.

conditions for all the three CI-SIDO converters are $G_{NN1} > 0$, $G_{NF1} < 0$, $G_{FN1} < 0$, $G_{FF1} < 0$, $G_{NN2} > 0$, $G_{NF2} < 0$, $G_{FN2} < 0$, $G_{FF2} < 0$ (Table 3.2).

3.7 Derivation of Conditions to Form Sectors of Duty Ratios

The slope expressions of the CI-SIDO converters are presented in Chapter-2. Each slope expressions are analysed in details.

3.7.1 Condition to be satisfied by duty ratios - for inductor current slope $G_{NF1} > 0$

CI-SIDO Buck	CI-SIDO Boost	CI-SIDO Buck-Boost
The slope expression of G_{NF1} is given by–		
$G_{NF1} = \frac{V_{in} - V_{o1} - k\sqrt{\frac{L_1}{L_2}}V_{o2}}{(1-k^2)L_1}$	$G_{NF1} = \frac{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)V_{in} - k\sqrt{\frac{L_1}{L_2}}V_{02}}{(1-k^2)L_1}$	$G_{NF1} = \frac{V_{in} - k\sqrt{\frac{L_1}{L_2}}V_{o2}}{(1-k^2)L_1}$
Depending on the values of k, L_1, L_2, V_{in}, V_{o1}, V_{o2}, the slope expression of G_{NF1} can take positive as well as negative values. For $G_{NF1} > 0$, we have		
$\frac{V_{in} - V_{o1} - k\sqrt{\frac{L_1}{L_2}}V_{o2}}{(1-k^2)L_1} \geq 0$	$\frac{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)V_{in} - k\sqrt{\frac{L_1}{L_2}}V_{02}}{(1-k^2)L_1} \geq 0$	$\frac{V_{in} - k\sqrt{\frac{L_1}{L_2}}V_{o2}}{(1-k^2)L_1} \geq 0$
Rearranging the expression, we have		
$V_{o1} + k\sqrt{\frac{L_1}{L_2}}V_{o2} \leq V_{in}$	$\frac{V_{in}}{V_{o2}} \geq \frac{k\sqrt{\frac{L_1}{L_2}}}{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)}$	$\frac{V_{in}}{V_{o2}} \geq k\sqrt{\frac{L_1}{L_2}}$
Using (2.39)–	Using (2.50)–	Using (2.59)–
$D_1 + k\sqrt{\frac{L_1}{L_2}}D_2 \leq 1$	$D_2 \leq r_{NF1}$	$D_2 \leq r_{NF1}$

3.7.2 Condition to be satisfied by duty ratios - for inductor current slope $G_{NF2} > 0$

CI-SIDO Buck	CI-SIDO Boost	CI-SIDO Buck-Boost
The slope expression of G_{NF2} is given by–		
$G_{NF2} = \frac{k\sqrt{\frac{L_2}{L_1}}V_{in} - k\sqrt{\frac{L_2}{L_1}}V_{o1} - V_{o2}}{(1-k^2)L_2}$	$G_{NF2} = \frac{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)V_{in} - V_{02}}{(1-k^2)L_2}$	$G_{NF2} = \frac{k\sqrt{\frac{L_2}{L_1}}V_{in} - V_{o2}}{(1-k^2)L_2}$
Depending on the values of k, L_1, L_2, V_{in}, V_{o1}, V_{o2}, the slope expression of G_{NF2} can take positive as well as negative values. For $G_{NF2} > 0$, we have		
$\frac{k\sqrt{\frac{L_2}{L_1}}V_{in} - k\sqrt{\frac{L_2}{L_1}}V_{o1} - V_{o2}}{(1-k^2)L_2} \geq 0$	$\frac{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)V_{in} - V_{02}}{(1-k^2)L_2} \geq 0$	$\frac{k\sqrt{\frac{L_2}{L_1}}V_{in} - V_{o2}}{(1-k^2)L_2} \geq 0$
Rearranging the expression, we have		
$V_{o2} + k\sqrt{\frac{L_2}{L_1}}V_{o1} \leq k\sqrt{\frac{L_2}{L_1}}V_{in}$	$\frac{V_{in}}{V_{o2}} \geq \frac{1}{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)}$	$\frac{V_{in}}{V_{o2}} \geq \frac{1}{k\sqrt{\frac{L_2}{L_1}}}$
Using (2.39)–	Using (2.50)–	Using (2.59)–
$D_2 + k\sqrt{\frac{L_2}{L_1}}D_1 < k\sqrt{\frac{L_2}{L_1}}$	$D_2 \leq r_{NF2}$	$D_2 \leq r_{NF2}$

3.7.3 Condition to be satisfied by duty ratios - for inductor current slope $G_{FN1} > 0$

CI-SIDO Buck	CI-SIDO Boost	CI-SIDO Buck-Boost
The slope expression of G_{FN1} is given by–		
$G_{FN1} = \frac{k\sqrt{\frac{L_1}{L_2}}V_{in} - V_{o1} - k\sqrt{\frac{L_1}{L_2}}V_{o2}}{(1-k^2)L_1}$	$G_{FN1} = \frac{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)V_{in} - V_{01}}{(1-k^2)L_1}$	$G_{FN1} = \frac{-V_{o1} + k\sqrt{\frac{L_1}{L_2}}V_{in}}{(1-k^2)L_1}$
Depending on the values of k, L_1, L_2, V_{in}, V_{o1}, V_{o2}, the slope expression of G_{FN1} can take positive as well as negative values. For $G_{FN1} > 0$, we have		
$\frac{k\sqrt{\frac{L_1}{L_2}}V_{in} - V_{o1} - k\sqrt{\frac{L_1}{L_2}}V_{o2}}{(1-k^2)L_1} \geq 0$	$G_{FN1} = \frac{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)V_{in} - V_{01}}{(1-k^2)L_1} \geq 0$	$\frac{-V_{o1} + k\sqrt{\frac{L_1}{L_2}}V_{in}}{(1-k^2)L_1} \geq 0$
Rearranging the expression, we have		
$V_{o1} + k\sqrt{\frac{L_1}{L_2}}V_{o2} \leq k\sqrt{\frac{L_1}{L_2}}V_{in}$	$\frac{V_{in}}{V_{o1}} \geq \frac{1}{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)}$	$\frac{V_{in}}{V_{o1}} \geq \frac{1}{k\sqrt{\frac{L_1}{L_2}}}$
Using (2.39)–	Using (2.50)–	Using (2.59)–
$D_1 + k\sqrt{\frac{L_1}{L_2}}D_2 < k\sqrt{\frac{L_1}{L_2}}$	$D_1 \leq r_{FN1}$	$D_1 \leq r_{FN1}$

3.7.4 Condition to be satisfied by duty ratios - for inductor current slope $G_{FN2} > 0$

CI-SIDO Buck	CI-SIDO Boost	CI-SIDO Buck-Boost
The slope expression of G_{FN2} is given by–		
$G_{FN2} = \frac{V_{in} - k\sqrt{\frac{L_2}{L_1}}V_{o1} - V_{o2}}{(1-k^2)L_2}$	$G_{FN2} = \frac{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)V_{in} - k\sqrt{\frac{L_2}{L_1}}V_{o1}}{(1-k^2)L_2}$	$G_{FN2} = \frac{V_{in} - k\sqrt{\frac{L_2}{L_1}}V_{o1}}{(1-k^2)L_2}$
Depending on the values of k, L_1, L_2, V_{in}, V_{o1}, V_{o2}, the slope expression of G_{FN2} can take positive as well as negative values. For $G_{FN2} > 0$, we have		
$\frac{V_{in} - k\sqrt{\frac{L_2}{L_1}}V_{o1} - V_{o2}}{(1-k^2)L_2} \geq 0$	$\frac{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)V_{in} - k\sqrt{\frac{L_2}{L_1}}V_{o1}}{(1-k^2)L_2} \geq 0$	$\frac{V_{in} - k\sqrt{\frac{L_2}{L_1}}V_{o1}}{(1-k^2)L_2} \geq 0$
Rearranging the expression, we have		
$k\sqrt{\frac{L_2}{L_1}}V_{o1} + V_{o2} \leq V_{in}$	$\frac{V_{in}}{V_{o1}} \geq \frac{k\sqrt{\frac{L_2}{L_1}}}{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)}$	$\frac{V_{in}}{V_{o1}} \geq k\sqrt{\frac{L_2}{L_1}}$
Using (2.39)–	Using (2.50)–	Using (2.59)–
$k\sqrt{\frac{L_2}{L_1}}D_1 + D_2 < 1$	$D_1 \leq r_{FN2}$	$D_1 \leq r_{FN2}$

3.7.5 Relation between r_{NF1} and r_{NF2}; and r_{FN1} and r_{FN2} in CI-SIDO Boost and Buck-Boost Converters

Suppose we assume that $r_{NF2} \leq r_{NF1}$, we have

$$\frac{k\sqrt{\frac{L_2}{L_1}}}{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)} \leq \frac{1}{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)} \Rightarrow k^2 \leq 1 \Rightarrow 0 \leq k \leq 1 \tag{3.15}$$

Therefore, we conclude that $r_{NF2} \leq r_{NF1}$. Suppose we assume that $r_{FN1} \leq r_{FN2}$, we have

$$\frac{k\sqrt{\frac{L_1}{L_2}}}{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)} \leq \frac{1}{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)} \Rightarrow k^2 \leq 1 \Rightarrow 0 \leq k \leq 1 \tag{3.16}$$

Therefore, we conclude that $r_{FN1} \leq r_{FN2}$.

3.8 Effect of Change in Coupled Inductors on Sector Formation

As discussed in the previous section, the sector formation of CI-SIDO buck (Fig. 3.1), CI-SIDO boost (Fig. 3.2) and CI-SIDO buck-boost (Fig. 3.2) converters depend on whether G_{NF1}, G_{NF2}, G_{FN1}, G_{FN2} is >, <, or = 0. For given duty ratios, we observed from Table 3.1 that the signs of slopes depend on the coupled inductor parameters. For CI-SIDO boost and buck-boost, the slope conditions depend on r_{NF1}, r_{NF2}, r_{FN1}, r_{FN2}. For CI-SIDO buck, the slope conditions depend on $k\sqrt{\frac{L_1}{L_2}}$. As the coupled

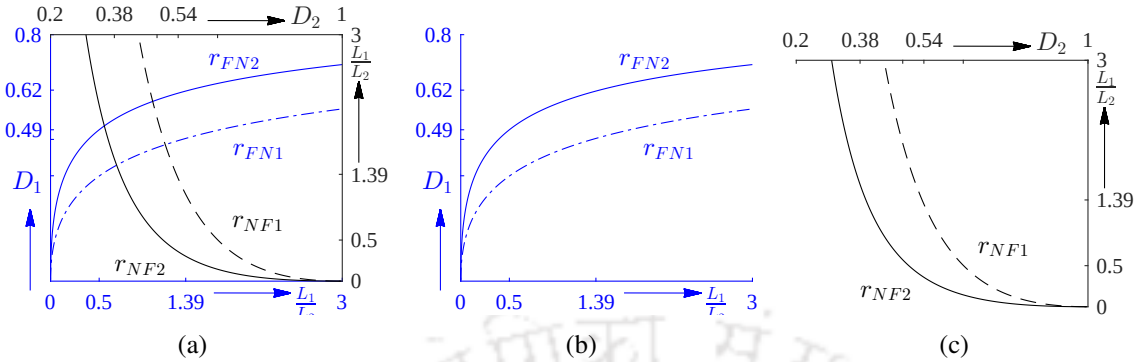


Figure 3.8: (a) Plot of r_{NF1}, r_{NF2}, r_{FN1} and r_{FN2} for different $\frac{L_1}{L_2}$, (b) D_1 versus $\frac{L_1}{L_2}$ separated, (c) D_2 versus $\frac{L_1}{L_2}$ separated.

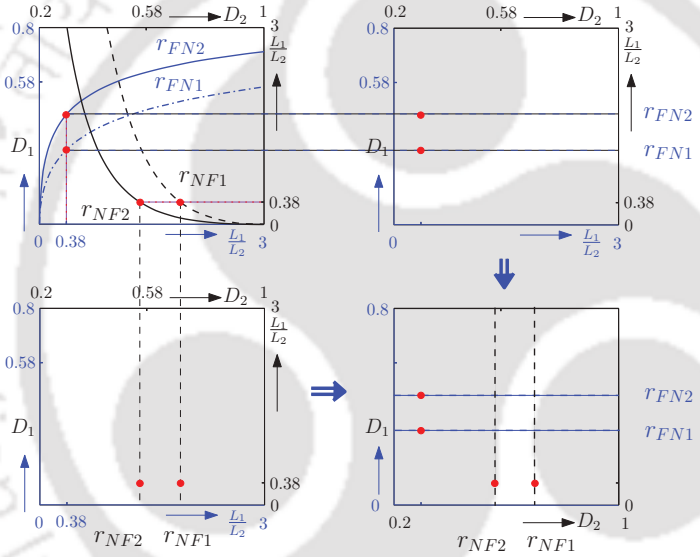


Figure 3.9: Formation of sector using the plots of r_{NF1}, r_{NF2}, r_{FN1} and r_{FN2} for $\frac{L_1}{L_2} = 0.38$

inductor parameters change, the dimensions of the sectors change. The effect of change in coupled inductor parameters on sector formation is discussed in this section. As the sectors of CI-SIDO boost and CI-SIDO buck-boost is same, it is discussed together, followed by CI-SIDO buck converter.

3.8.1 CI-SIDO Boost and CI-SIDO Buck-Boost Converter

The sector diagram of CI-SIDO boost and CI-SIDO buck-boost converters in Fig. 3.2 shows that its dimensions depend on the values of r_{NF1}, r_{NF2}, r_{FN1}, r_{FN2}. The plots of r_{NF1}, r_{NF2}, r_{FN1}, r_{FN2} for $\frac{L_1}{L_2}$ ranging from 0 to 3 is shown in Fig. 3.8(a) for $k = 0.73$. r_{FN1} and r_{FN2} is plotted in blue with respect to $\frac{L_1}{L_2}$ and D_1. Similarly, r_{NF1} and r_{NF2} is plotted in black with respect to $\frac{L_1}{L_2}$ and D_2. To make the plot of r_{NF1}, r_{NF2}, r_{FN1}, r_{FN2} more clear, the plots in Fig. 3.8(a) is separated into two different

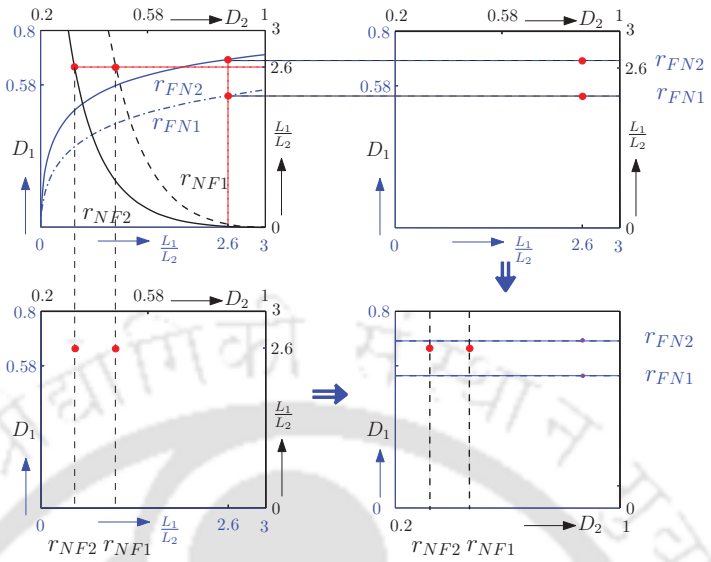
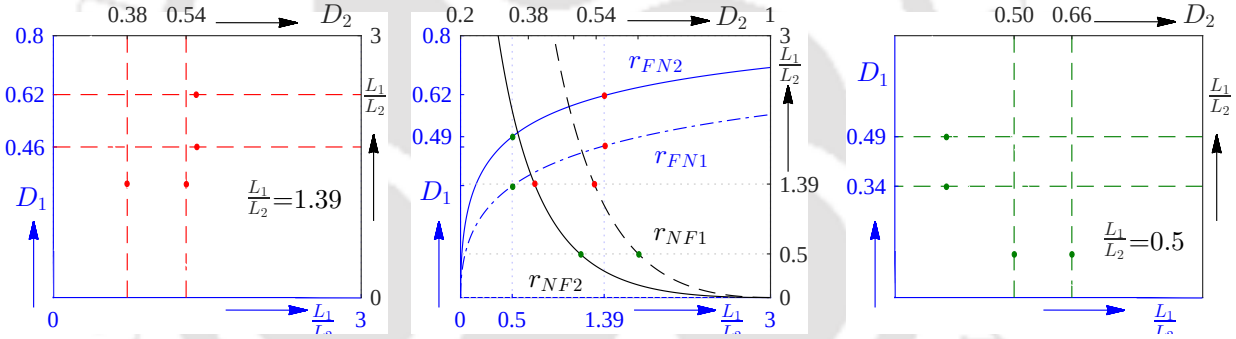


Figure 3.10: Formation of sector using the plots of r_{NF1}, r_{NF2}, r_{FN1} and r_{FN2} for $\frac{L_1}{L_2} = 2.6$



(a) (b) (c)

Figure 3.11: (a) Sector formation for $\frac{L_1}{L_2} = 1.39$, (b) Plot of r_{NF1}, r_{NF2}, r_{FN1} and r_{FN2} for different $\frac{L_1}{L_2}$, and (c) Sector formation for $\frac{L_1}{L_2} = 0.5$.

plots of D_1 versus $\frac{L_1}{L_2}$ in blue colour and D_2 versus $\frac{L_1}{L_2}$ in black colour. The waveforms in Fig. 3.8(a) is the combination of D_1 versus $\frac{L_1}{L_2}$ (Fig. 3.8(b)) and D_2 versus $\frac{L_1}{L_2}$ (Fig. 3.8(c)). The x-axis of D_2 versus $\frac{L_1}{L_2}$ is shifted upward and y-axis is shifted to the right side. In the plot, $\frac{L_1}{L_2}$ is the independent variable and D_1, D_2 are the dependent variables.

The plots of r_{NF1}, r_{NF2}, r_{FN1} and r_{FN2} helps to find the sector diagram as shown in Figs. 3.9 and 3.10. These plots also help to find the effect of change in coupled inductor parameters on the sector formation.

For different values of $\frac{L_1}{L_2}$, the value of r_{NF1}, r_{NF2}, r_{FN1} and r_{FN2} are different. The change in $\frac{L_1}{L_2}$, changes the size of sectors. For example, in Fig. 3.11(a), the sector formation is shown for $\frac{L_1}{L_2} = 1.39$

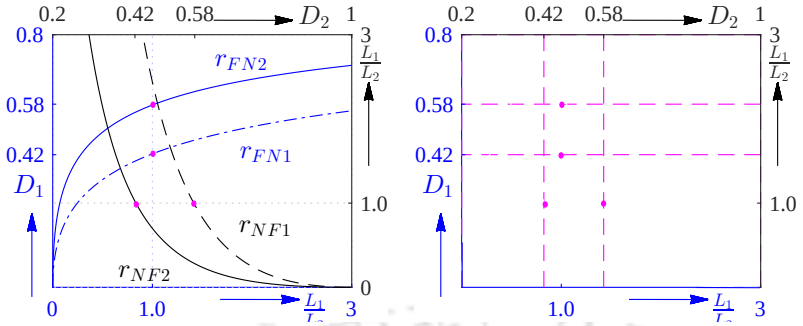


Figure 3.12: (a) Plot of r_{NF1}, r_{NF2}, r_{FN1} and r_{FN2} for different $\frac{L_1}{L_2}$, and (b) Sector formation for $\frac{L_1}{L_2} = 1.0$.

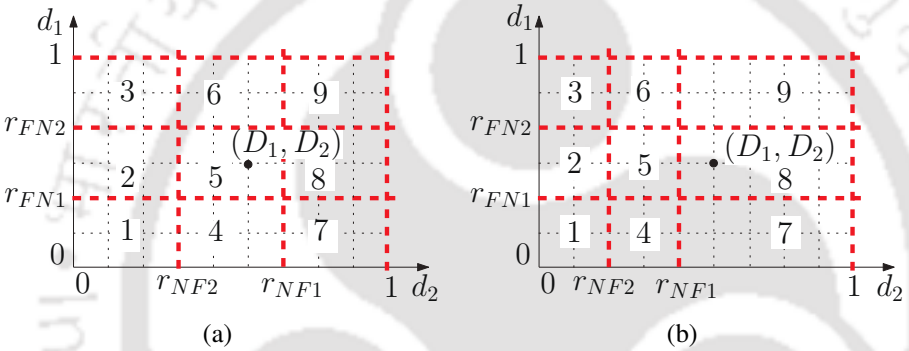


Figure 3.13: Effect of variations in coupled inductor parameters on sector formation of CI-SIDO boost when (a) D_1, D_2 in sector 5, and (b) D_1, D_2 in sector 8.

and in Fig. 3.11(c), the sector formation is shown for $\frac{L_1}{L_2} = 0.5$. The number of sectors are same but the size changes. For same value of D_1 and D_2, the change in $\frac{L_1}{L_2}$ changes the slope condition and hence, the current patterns. The sector formation for $\frac{L_1}{L_2} = 1.0$, is shown in Fig. 3.12.

The change in L_1, L_2, k changes the dimensions of sectors in CI-SIDO boost converter as shown in Fig. 3.13. The duty ratios D_1, D_2 lying in sector 5 changes to sector 8 if the coupled inductor parameters L_1, L_2, k change.

3.8.2 CI-SIDO Buck Converter

The sector formation for buck converter depends on both D_1, D_2, in addition to k, L_1, L_2. It can be observed in Fig. 3.14. Fig. 3.14(a) is shown when D_1 varies with $\frac{L_1}{L_2}$ when D_2 is given. Similarly, Fig. 3.14(b) is shown when D_2 varies with $\frac{L_1}{L_2}$ when D_1 is given.

As the values of L_1, L_2, k change, the sectors of CI-SIDO buck converter changes. Depending on the values of $k\sqrt{\frac{L_2}{L_1}}$ and $k\sqrt{\frac{L_1}{L_2}}$, the feasible sectors of CI-SIDO buck converters change as shown

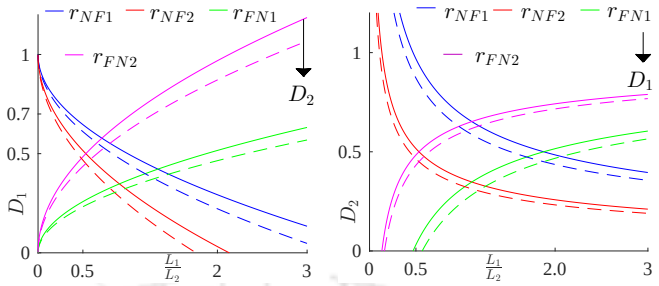


Figure 3.14: The effect of change in $\frac{L_1}{L_2}$ on the sector formation of buck converter.

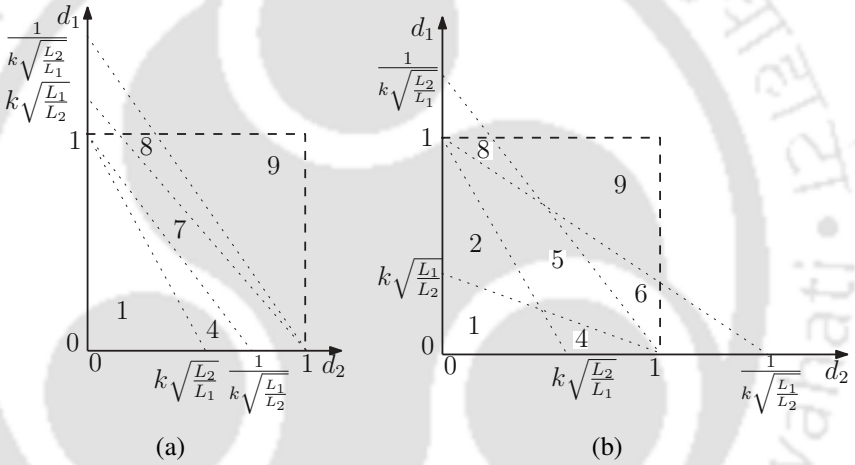


Figure 3.15: Effect of coupled inductor parameters on sector formation in CI-SIDO buck converter (a) $k\sqrt{\frac{L_1}{L_2}} > 1$ and $k\sqrt{\frac{L_2}{L_1}} < 1$, and (b) $k\sqrt{\frac{L_1}{L_2}} < 1$ and $k\sqrt{\frac{L_2}{L_1}} < 1$.

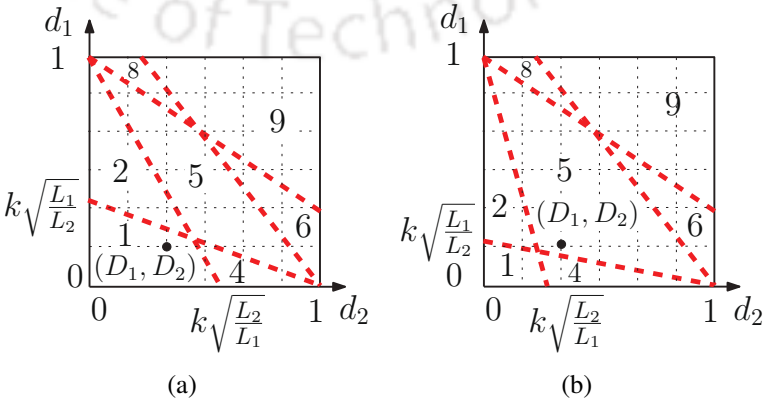


Figure 3.16: Effect of variations in coupled inductor parameters on sector formation of CI-SIDO buck (a) D_1, D_2 in sector 1, and (b) D_1, D_2 in sector 5.

in Fig. 3.15. For $k\sqrt{\frac{L_2}{L_1}} > 1$ and $k\sqrt{\frac{L_1}{L_2}} < 1$, sectors 1, 2, 3, 6, and 9 are possible. For $k\sqrt{\frac{L_2}{L_1}} < 1$ and $k\sqrt{\frac{L_1}{L_2}} > 1$, sectors 1, 4, 7, 8, and 9 are possible. For $k\sqrt{\frac{L_2}{L_1}} < 1$ and $k\sqrt{\frac{L_1}{L_2}} < 1$, sectors 1, 2, 4, 5, 6, 8, and 9 are possible. Furthermore, even if the values of L_1, L_2, k changes keeping $k\sqrt{\frac{L_2}{L_1}} < 1$, $k\sqrt{\frac{L_1}{L_2}} < 1$, the dimension of each sectors change as shown in Fig. 3.16. In the figure, it is found that if duty ratios D_1, D_2 lies in sector 1 and then if L_1, L_2, k changes, the same duty ratios D_1, D_2 changes its sector to sector 5.

3.9 Summary of the Chapter

The following are the summary of the chapter:

(i) Numerous patterns of inductor currents are possible for these CI-SIDO converters depending on the coupled inductor parameters and duty ratios. It is difficult to analyze the numerous possibilities of inductor current patterns for all the CI-SIDO converters. An approach is presented to unify inductor current patterns and inductor current ripples in CI-SIDO converters by forming sectors of duty ratios.

(ii) Sectors are formed by grouping inductor currents based on similar inductor current slope conditions.

(iii) The sector formation unifies the patterns of inductor currents, the expressions of current ripples for any values of D_1, D_2, L_1, L_2, k.

(iv) The sector formations of CI-SIDO boost and CI-SIDO buck-boost converters are same. These converters always form nine sectors irrespective of the coupled inductor parameter values. The dimensions of nine sectors depend on the values of L_1, L_2, k.

(v) In CI-SIDO buck converter, all the nine sectors are not formed simultaneously. Amongst nine sectors, which sector gets formed depend on the coupled inductor parameter values.

(vi) If the coupled inductors are changed, the dimensions of nine sectors change in CI-SIDO boost and CI-SIDO buck-boost converter.

(vii) If the coupled inductor parameters are changed in CI-SIDO buck converter, the sector which gets formed also change, in addition to the change in the dimension of the sectors.

4

Inductor Current Ripple Minimization in CI-SIDO Converters by Shift of Gate Pulse

Contents

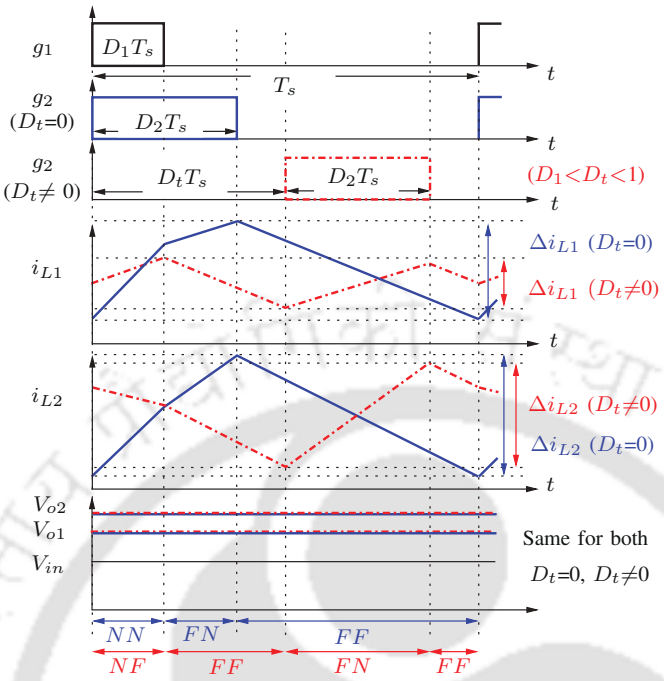


Figure 4.1: Effect of shift in g_2 by D_tT_s with respect to g_1 on ripples Δi_{L1} and Δi_{L2} (N and F denote ON and OFF states of switches).

4.1 Introduction

[1] The input-output voltage relations in (2.39), (2.50), and (2.59) show that V_{o1} and V_{o2} are independent of the relative arrangement of gate pulses g_1 and g_2. So, relative shift between g_1 and g_2 does not affect the outputs. The relative shift is denoted by ratio D_t, and it varies between 0 and 1.

Fig. 4.1 shows the output voltages V_{o1}, V_{o2}, input voltage V_{in}, and inductor currents i_{L1}, i_{L2}; for zero and a non-zero shift D_tT_s between g_1 and g_2. We observe from Fig. 4.1, due to shifting of g_2:

- The ripples in inductor currents, Δi_{L1}, Δi_{L2} change.
- For the same shift D_t of g_2, the change in Δi_{L1} is different than the change in Δi_{L2}.
- The ripples Δi_{L1}, Δi_{L2} depend on the values of duty ratios D_1, D_2, and the slopes of i_{L1}, i_{L2}, i.e., in turn on the values of inductances L_1, L_2.

[1]Major part of this chapter is reproduced from my publications: (i) Nupur and S. Nath, "Minimizing Ripples of Inductor Currents in Coupled SIDO Boost Converter by Shift of Gate Pulses," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1217-1226, Feb. 2020. (ii) Nupur and S. Nath, "Inductor Current Ripples Minimization in Coupled SIDO Buck and Buck-Boost Converter by Gate Pulse Shifting," in *Proc. Int. Conf. Power Electron., Drives Energy Syst.*, Dec. 2020, pp. 1-6. (iii) Nupur and S. Nath, "Inductor Current Ripples Minimization in Coupled Inductor Single Input Triple Output Boost Converter by Gate Pulse Shifting," in *Proc. Int. Conf. Power Electron., Drives Energy Syst.*, Dec. 2020, pp. 1-6.

This chapter aims to find the values of D_t at which the ripples of both inductor currents Δi_{L1}, Δi_{L2} are minimum; for any given values of inductances L_1, L_2 and duty ratios D_1, D_2. The scope of this work is limited to CCM of CI-SIDO converters. The range of values of D_t, at which minimum ripple is obtained, is denoted by $\mathbf{D}_{min}$. Bold letter $\mathbf{D}$ is used to represent the range of values of D_t throughout the thesis. Least or minimum values of ripples Δi_{L1} and Δi_{L2} are denoted by $\underline{\Delta i_{L1}}$ and $\underline{\Delta i_{L2}}$, respectively. While finding $\mathbf{D}_{min}$, the following challenges are encountered:

- $\mathbf{D}_{min}$ for all the 36 conditions are different depending on the values of L_1, L_2, k, D_1 and D_2. All conditions need to be found.
- $\mathbf{D}_{min}$ need to be obtained in each condition.
- $\mathbf{D}_{min}$ for $\underline{\Delta i_{L1}}$ can be different than $\mathbf{D}_{min}$ for $\underline{\Delta i_{L2}}$.

4.2 Commonly Used Terminologies for CI-SIDO Converters

The subsequent chapters of the thesis discusses the CI-SIDO converters in details. The most common terms and nomenclatures that are used in the thesis is presented in Fig. 4.2 for reference.

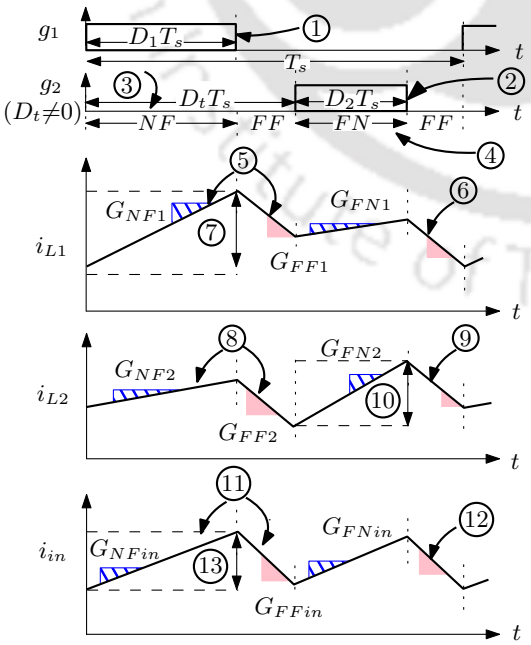


Figure 4.2: Diagram of current waveforms and gate pulses to explain the terminologies used.

1. Gate pulse with duty ratio D_1
2. Gate pulse with duty ratio D_2
3. Gate pulse shift D_t
4. Sequence of states
5. Slopes of first inductor current
6. First inductor current waveform
7. Ripple of first inductor current
8. Slopes of second inductor current
9. Second inductor current waveform
10. Ripple of second inductor current
11. Slopes of input current
12. Input current waveform
13. Ripple of input current

4.3 Gate Pulse Shift for Minimum Inductor Current Ripples in CI-SIDO Boost Converter

To obtain $\mathbf{D}_{min}$ for each of the conditions identified in Chapter 2, at first the relative shift D_t is varied from 0 to 1, irrespective of the signs of G_{NFw} and G_{FNw}. Then the ripple expressions are obtained and compared for each D_t.

Taking example of condition $(D_1 + D_2) < 1$ and $D_1 < D_2$, it is observed that the sequences of states obtained are $NN \rightarrow FN \rightarrow FF$ when $D_t = 0$ (Fig. 4.3(a)). The states NN, FN and FF occur for the time intervals D_1T_s, $(D_2 - D_1)T_s$ and $(1 - D_2)T_s$, respectively, and can be denoted as $D_1T_s \rightarrow (D_2-D_1)T_s \rightarrow (1-D_2)T_s$. Further, the sequences of states obtained are $NF \rightarrow NN \rightarrow FN \rightarrow FF$ and are for the corresponding time intervals $D_tT_s \rightarrow (D_1 - D_t)T_s \rightarrow (D_2 + D_t - D_1)T_s \rightarrow (1 - D_2 - D_t)T_s$, when $0 < D_t < D_1$ (Fig. 4.3(b)). Similarly, D_t is varied further for all possible range of values under the condition set $(D_1 + D_2) < 1$ and $D_1 < D_2$, and the obtained different sequence of states are shown in Fig. 4.3. Each different sequence of states is denoted by a name (e.g. D-I, B-I), as shown on the right side of the figure. It is pertinent to mention that Fig. 4.3 is drawn considering one out of the nine conditions of D_1, D_2. For conciseness, only one figure is shown out of nine figures corresponding to the nine conditions. The remaining eight figures are drawn similarly and shown in Appendix A.

For each sequence of states, there can be four different patterns of waveforms, depending on G_{NF_w} and G_{FN_w} being positive or negative, for either inductor currents i_{Lw}. The number further increases if G_{NF_w} and G_{FN_w} becomes zero. Fig. 4.3 also shows the patterns of waveforms i_{Lw}, for $(D_1 + D_2) < 1$ and $D_1 < D_2$ (i.e. SR-2), when $G_{NF_w} > 0$, $G_{FN_w} > 0$ (red solid lines), $G_{NF_w} > 0$, $G_{FN_w} < 0$ (blue dashed lines) and $G_{NF_w} < 0$, $G_{FN_w} > 0$ (black dash-dotted lines). Note that, Fig. 4.3 shows patterns of i_{Lw} waveforms for three conditions out of 36 conditions. Similarly, the remaining figures are drawn in Figs. A.1 to A.14.

4.3.1 Finding Series Name, Sequence, Sequence of States, and Time Durations of Each State Using Table 4.2 and Table 4.3

From the above analysis associated with Fig. 4.3, it is clear that different sequence of states occur for different ranges of shift D_t. Series of sequences are obtained for different conditions of D_1, D_2.

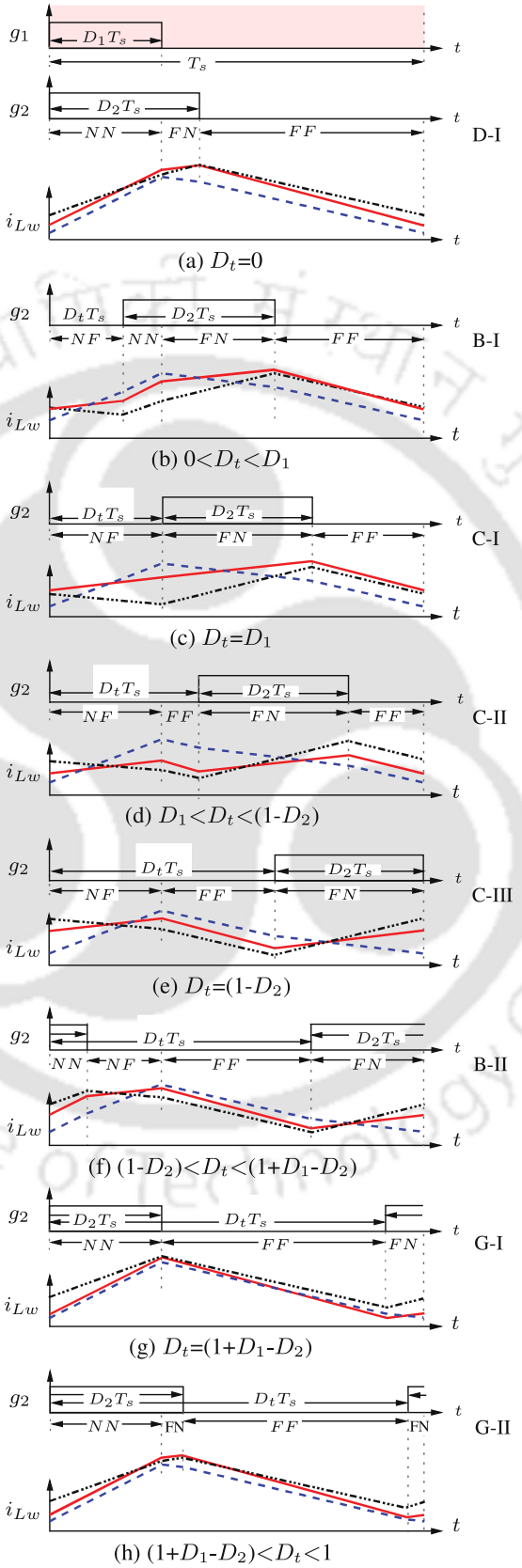


Figure 4.3: Different sequences (D-I, B-I,...) of states and different patterns of i_{Lw} waveforms for (i) $G_{NF_w} > 0$, $G_{FN_w} > 0$ (red solid lines), (ii) $G_{NF_w} > 0$, $G_{FN_w} < 0$ (blue dashed lines), (iii) $G_{NF_w} < 0$, $G_{FN_w} > 0$ (black dash-dotted lines); when $(D_1 + D_2) < 1$ and $D_1 < D_2$ as D_t varied from 0 to 1.

Table 4.1: The sequence, sequence of states, and time durations of each state for series *SR-2* ($D_1 + D_2 < 1$ and $D_1 < D_2$).

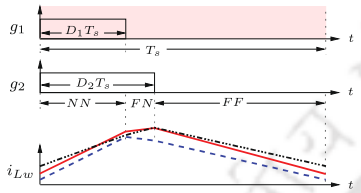
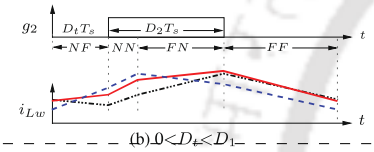
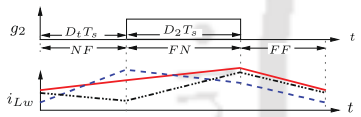
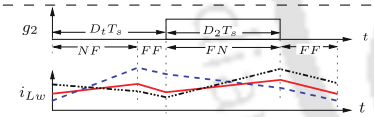
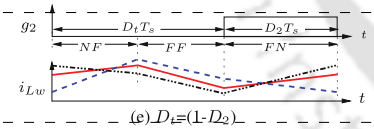
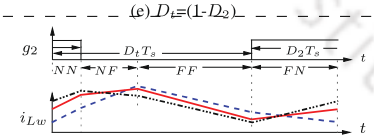
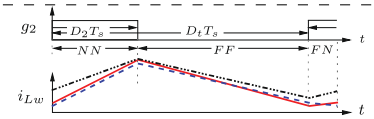
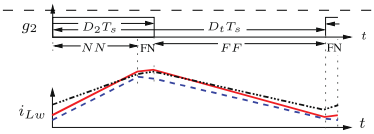
Series Name: *SR-2*	Shift D_t	Seq.	Sequence of states	Time duration of each state
 D-I (a) D_t=0	$D_t = 0$	D-I	$NN \rightarrow$ $FN \rightarrow$ FF	$D_1T_s \rightarrow$ $(D_2 - D_1)T_s \rightarrow$ $(1 - D_2)T_s$
 B-I (b) $0<D_t<D_1$	$0 < D_t < D_1$	B-I	$NF \rightarrow$ $NN \rightarrow$ $FN \rightarrow$ FF	$D_tT_s \rightarrow$ $(D_1 - D_t)T_s \rightarrow$ $(D_2 + D_t - D_1)T_s$ $\rightarrow (1 - D_2 - D_t)T_s$
 C-I (c) D_t=D_1	$D_t = D_1$	C-I	$NF \rightarrow$ $FN \rightarrow$ FF	$D_1T_s \rightarrow$ $D_2T_s \rightarrow$ $(1 - D_1 - D_2)T_s$
 C-II (d) $D_1<D_t<(1-D_2)$	$D_1 < D_t$ $< (1 - D_2)$	C-II	$NF \rightarrow$ $FF \rightarrow$ $FN \rightarrow$ FF	$D_1T_s \rightarrow$ $(D_t - D_1)T_s \rightarrow$ $D_2T_s \rightarrow$ $(1 - D_2 - D_t)T_s$
 C-III (e) D_t=(1-D_2)	$D_t = (1 - D_2)$	C-III	$NF \rightarrow$ $FF \rightarrow$ FN	$D_1T_s \rightarrow$ $(1 - D_1 - D_2)T_s$ $\rightarrow D_2T_s$
 B-II (f) $(1-D_2)<D_t<(1+D_1-D_2)$	$(1 - D_2) < D_t$ $< (1 + D_1 - D_2)$	B-II	$NN \rightarrow$ $NF \rightarrow$ $FF \rightarrow$ FN	$(D_t + D_2 - 1)T_s \rightarrow$ $(D_1 - D_t - D_2 + 1)T_s$ $\rightarrow (D_t - D_1)T_s$ $\rightarrow (1 - D_t)T_s$
 G-I (g) D_t=(1+D_1-D_2)	$D_t = (1 + D_1 - D_2)$	G-I	$NN \rightarrow$ $FF \rightarrow$ FN	$D_1T_s \rightarrow$ $(1 - D_2)T_s \rightarrow$ $(D_2 - D_1)T_s$
 G-II (h) $(1+D_1-D_2)<D_t<1$	$(1 + D_1 - D_2)$ $< D_t < 1$	G-II	$NN \rightarrow$ $FN \rightarrow$ $FF \rightarrow$ FN	$D_1T_s \rightarrow$ $(D_t + D_2 - 1 - D_1)T_s$ $\rightarrow (D_t - D_1)T_s$ $\rightarrow (1 - D_t)T_s$

Table 4.2: Series of occurrence of sequences in 9 conditions of D_1 and D_2 (Sequence of states shown in Table 4.3 and corresponding figures in Appendix A)

	$(D_1 + D_2) < 1$			$(D_1 + D_2) > 1$			$(D_1 + D_2) = 1$		
Relative shift D_t	$D_1 > D_2$	$D_1 < D_2$	$D_1 = D_2$	$D_1 > D_2$	$D_1 < D_2$	$D_1 = D_2$	$D_1 > D_2$	$D_1 < D_2$	$D_1 = D_2$
$D_t = 0$ $0 < D_t < (D_1 - D_2)$ $D_t = (D_1 - D_2)$	A-I A-II A-III	D-I	D-II	A-I A-II A-III	D-I	D-II	A-I A-II A-III	D-I	D-II
$Max\{0, D_1 - D_2\} < D_t < Min\{D_1, 1 - D_2\}$	B-I	B-I	B-I	B-I	B-I	B-I	B-I	B-I	B-I
$D_t = D_1$ $D_1 < D_t < (1 - D_2)$ $D_t = (1 - D_2)$	C-I C-II C-III	C-I C-II C-III	C-I C-II C-III						
$D_t = (1 - D_2)$ $(1 - D_2) < D_t < D_1$ $D_t = D_1$				E-I E-II E-III	E-I E-II E-III	E-I E-II E-III	F	F	F
$Max\{D_1, 1 - D_2\} < D_t < \{(1 + D_1 - D_2)\ if\ D_2 > D_1,\ else\ 1\}$	B-II	B-II	B-II	B-II	B-II	B-II	B-II	B-II	B-II
$D_t = (1 + D_1 - D_2)$ $(1 + D_1 - D_2) < D_t < 1$		G-I G-II			G-I G-II			G-I G-II	
Series name	*SR-1*	*SR-2*	*SR-3*	*SR-4*	*SR-5*	*SR-6*	*SR-7*	*SR-8*	*SR-9*

Depending on the signs of slopes G_{NF_w}, G_{FN_w}, either of the inductor currents i_{Lw} has numerous patterns of waveforms possible.

The waveforms presented in Fig. 4.3 is again explained using Table 4.1. Different columns of the table represents all the informations presented in the figure. In column 1, Table 4.1 shows different patterns of i_{Lw} waveforms for (i) $G_{NF_w} > 0$, $G_{FN_w} > 0$ (red solid lines), (ii) $G_{NF_w} > 0$, $G_{FN_w} < 0$ (blue dashed lines), (iii) $G_{NF_w} < 0$, $G_{FN_w} > 0$ (black dash-dotted lines), when $(D_1 + D_2) < 1$ and $D_1 < D_2$ as D_t varied from 0 to 1. The range of gate pulse shift for each waveform is presented in column 2. The sequence name is presented in column 3 which is also written in right side of each waveform. The sequence of states and the time duration of each state is also presented in column 4 and column 5 of the table, respectively. The table is added to explain the usage of Table 4.2 and Table 4.3 and its relation with Fig. 4.3.

This type of analysis is done for other 8 cases of the CI-SIDO converters. To make the presentation compact and to reduce the unnecessary repetitions, the series of sequences obtained for all the nine conditions are listed in Table 4.2, and the occurrence of states under each sequence are listed in Table 4.3. The series of sequences is named as SR-1 to SR-9, as shown in Table 4.2. The time duration of states in each sequence are listed in Table 4.3.

The above analysis is done for all 9 conditions of D_1, D_2. The series of sequences obtained for all

Table 4.3: Occurrence of states in each sequence

Seq.	Sequence of states	Time duration of each state
A-I	$NN \rightarrow NF \rightarrow FF$	$D_2T_s \rightarrow (D_1 - D_2)T_s \rightarrow (1 - D_1)T_s$
A-II	$NF \rightarrow NN \rightarrow NF \rightarrow FF$	$D_tT_s \rightarrow D_2T_s \rightarrow (D_1 - D_2 - D_t)T_s \rightarrow (1 - D_1)T_s$
A-III	$NF \rightarrow NN \rightarrow FF$	$(D_1 - D_2)T_s \rightarrow D_2T_s \rightarrow (1 - D_1)T_s$
B-I	$NF \rightarrow NN \rightarrow FN \rightarrow FF$	$D_tT_s \rightarrow (D_1 - D_t)T_s \rightarrow (D_2 + D_t - D_1)T_s \rightarrow (1 - D_2 - D_t)T_s$
B-II	$NN \rightarrow NF \rightarrow FF \rightarrow FN$	$(D_t + D_2 - 1)T_s \rightarrow (D_1 - (D_t + D_2 - 1))T_s \rightarrow (D_t - D_1)T_s \rightarrow (1 - D_t)T_s$
C-I	$NF \rightarrow FN \rightarrow FF$	$D_1T_s \rightarrow D_2T_s \rightarrow (1 - D_1 - D_2)T_s$
C-II	$NF \rightarrow FF \rightarrow FN \rightarrow FF$	$D_1T_s \rightarrow (D_t - D_1)T_s \rightarrow D_2T_s \rightarrow (1 - D_2 - D_t)T_s$
C-III	$NF \rightarrow FF \rightarrow FN$	$D_1T_s \rightarrow (1 - D_1 - D_2)T_s \rightarrow D_2T_s$
D-I	$NN \rightarrow FN \rightarrow FF$	$D_1T_s \rightarrow (D_2 - D_1)T_s \rightarrow (1 - D_2)T_s$
D-II	$NN \rightarrow FF$	$D_1T_s \rightarrow (1 - D_1)T_s$
E-I	$NF \rightarrow NN \rightarrow FN$	$(1 - D_2)T_s \rightarrow (D_1 + D_2 - 1)T_s \rightarrow (1 - D_1)T_s$
E-II	$NN \rightarrow NF \rightarrow NN \rightarrow FN$	$(D_t + D_2 - 1)T_s \rightarrow (1 - D_2)T_s \rightarrow (D_1 - D_t)T_s \rightarrow (1 - D_1)T_s$
E-III	$NN \rightarrow NF \rightarrow FN$	$(D_1 + D_2 - 1)T_s \rightarrow (1 - D_2)T_s \rightarrow (1 - D_1)T_s$
F	$NF \rightarrow FN$	$D_1T_s \rightarrow (1 - D_1)T_s$
G-I	$NN \rightarrow FF \rightarrow FN$	$D_1T_s \rightarrow (1 - D_2)T_s \rightarrow (D_2 - D_1)T_s$
G-II	$NN \rightarrow FN \rightarrow FF \rightarrow FN$	$D_1T_s \rightarrow (D_t + D_2 - 1 - D_1)T_s \rightarrow (D_t - D_1)T_s \rightarrow (1 - D_t)T_s$

the nine conditions are listed in Table 4.2, and the occurrence of states under each sequence are listed in Table 4.3. We named the series of sequences as SR-1 to SR-9, as shown in Table 4.2. The time duration of states in each sequence are listed in Table 4.3.

4.3.2 Finding Gate Pulse for Minimum Inductor Current Ripples

The steps followed to find minimum ripple are: (1) $\mathbf{D}_{min}$ is obtained for minimum ripple in either inductor currents $\underline{\Delta i_{Lw}}$, by comparing ripple Δi_{Lw} in each of the 36 conditions, (2) As $\mathbf{D}_{min}$ for $\underline{\Delta i_{L1}}$ can be different than that for $\underline{\Delta i_{L2}}$, the common range of $\mathbf{D}_{min}$ is found where both $\underline{\Delta i_{L1}}$ and $\underline{\Delta i_{L2}}$ are achieved together.

Finding $\mathbf{D}_{min}$

The approach used to find the value of $\mathbf{D}_{min}$ for all the possible slope conditions are as follows:

(i) For the selected duty ratio and slope conditions, the expressions for ripple Δi_{Lw} are formed using (2.13), and are shown in Tables A.1 to A.9.

(ii) By comparing all the expressions of Δi_{Lw}, we find the minimum of Δi_{Lw}.

(iii) We found that Δi_{Lw} remains same and is minimum for a range of D_t which is called $\mathbf{D}_{min}$.

Table 4.4: Comparing Δi_{Lw} at different D_t to find $\mathbf{D}_{min}$ for *SR-2* ($D_1 + D_2 < 1$ and $D_1 < D_2$) with $G_{NFw} > 0$ and $G_{FNw} > 0$.

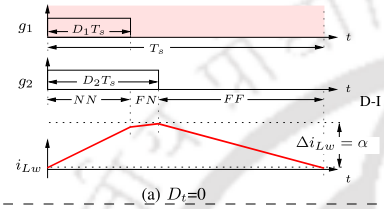
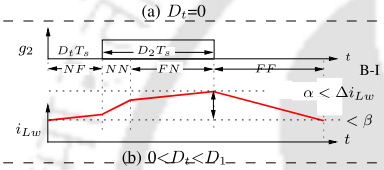
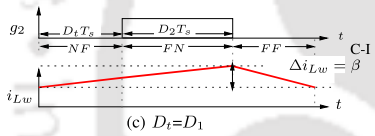
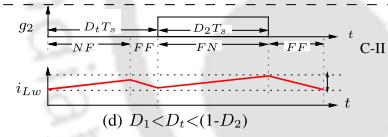
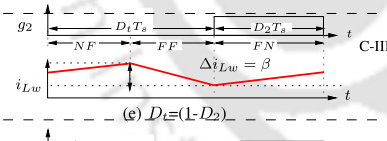
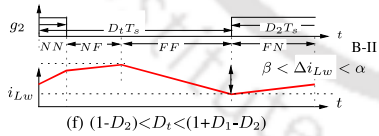
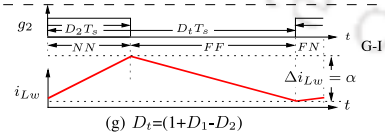
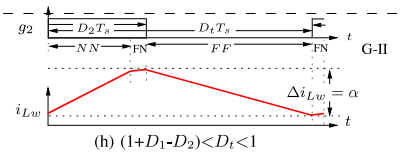
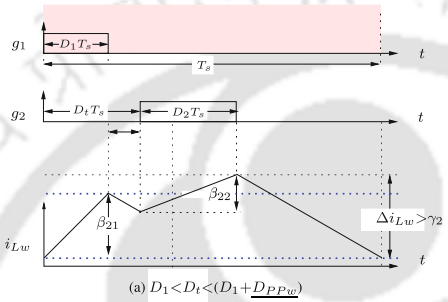
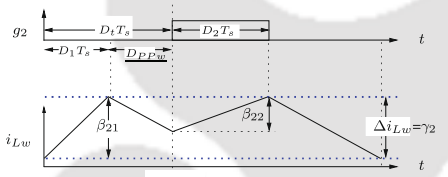
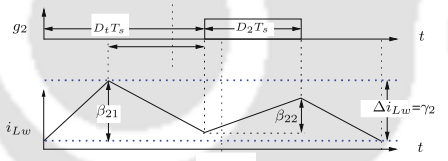
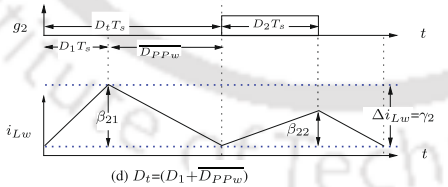
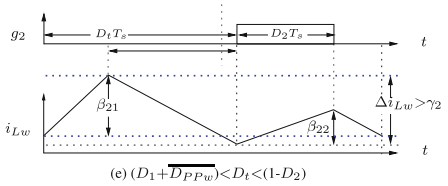
Series Name: *SR-2*	Shift D_t	Seq.	Δi_{Lw}	Notations
 (a) D_t=0	$D_t = 0$	D-I	α	$\alpha = G_{NN_w} D_1 T_s + G_{FN_w}(D_2 - D_1)T_s$
 (b) 0<D_t<D_1	$0 < D_t < D_1$	B-I	$\alpha < \Delta i_{Lw} < \beta$	$G_{NF_w} D_t T_s + G_{NN_w}(D_1 - D_t)T_s + G_{FN_w}(D_2 + D_t - D_1)T_s$
 (c) D_t=D_1	$D_t = D_1$	C-I	β	$\beta = G_{NF_w} D_1 T_s + G_{FN_w} D_2 T_s$
 (d) D_1<D_t<(1-D_2)	$D_1 < D_t < (D_1 + \underline{D_{PPw}})$ $(D_1 + \underline{D_{PPw}}) \le D_t \le (D_1 + \overline{D_{PPw}})$ $(D_1 + \overline{D_{PPw}}) < D_t < (1 - D_2)$	C-II	Table 4.5	Table 4.5
 (e) D_t=(1-D_2)	$D_t = (1 - D_2)$	C-III	β	$\beta = G_{NF_w} D_1 T_s + G_{FN_w} D_2 T_s$
 (f) (1-D_2)<D_t<(1+D_1-D_2)	$(1 - D_2) < D_t < (1 + D_1 - D_2)$	B-II	$\beta < \Delta i_{Lw} < \alpha$	$G_{NN_w}(D_t + D_2 - 1)T_s + G_{NF_w}(D_1 - D_t - D_2 + 1)T_s + G_{FN_w}(1 - D_t)T_s$
 (g) D_t=(1+D_1-D_2)	$D_t = (1 + D_1 - D_2)$	G-I	α	$G_{NN_w} D_1 T_s + G_{FN_w}(D_2 - D_1)T_s$
 (h) (1+D_1-D_2)<D_t<1	$(1 + D_1 - D_2) < D_t < 1$	G-II	α	$G_{NN_w} D_1 T_s + G_{FN_w}(D_2 - D_1)T_s$

Table 4.5: Variations of inductor current patterns within C-II such that $D_1 < D_t < (1 - D_2)$.

Shift	Fig.	Δi_{Lw}	Notations
$D_1 < D_t < (D_1 + \underline{D_{PPw}})$	 (a) $D_1 < D_t < (D_1 + \underline{D_{PPw}})$	$\beta > \Delta i_{Lw} > \gamma_2$	$\beta = G_{NF_w} D_1 T_s + G_{FN_w} D_2 T_s$ $\beta_{21} = G_{NF_w} D_1 T_s$ $\beta_{22} = G_{FN_w} D_2 T_s$ $\gamma_2 = Max\{G_{NF_w} D_1 T_s, G_{FN_w} D_2 T_s\}$
$D_t = (D_1 + \underline{D_{PPw}})$	 (b) $D_t = (D_1 + \underline{D_{PPw}})$	γ_2	$\gamma_2 = Max\{G_{NF_w} D_1 T_s, G_{FN_w} D_2 T_s\}$
$(D_1 + \underline{D_{PPw}}) < D_t < (D_1 + \overline{D_{PPw}})$	 (c) $(D_1 + \underline{D_{PPw}}) < D_t < (D_1 + \overline{D_{PPw}})$	γ_2	$\gamma_2 = Max\{G_{NF_w} D_1 T_s, G_{FN_w} D_2 T_s\}$
$D_t = (D_1 + \overline{D_{PPw}})$	 (d) $D_t = (D_1 + \overline{D_{PPw}})$	γ_2	$\gamma_2 = Max\{G_{NF_w} D_1 T_s, G_{FN_w} D_2 T_s\}$
$(D_1 + \overline{D_{PPw}}) < D_t < (1 - D_2)$	 (e) $(D_1 + \overline{D_{PPw}}) < D_t < (1\text{-}D_2)$	$\gamma_2 < \Delta i_{Lw} < \beta$	$\beta = G_{NF_w} D_1 T_s + G_{FN_w} D_2 T_s$ $\beta_{21} = G_{NF_w} D_1 T_s$ $\beta_{22} = G_{FN_w} D_2 T_s$ $\gamma_2 = Max\{G_{NF_w} D_1 T_s, G_{FN_w} D_2 T_s\}$

(iv) The range of D_t corresponding to minimum ripples are found from Tables A.1 to A.9.

Taking example of condition $(D_1 + D_2) < 1$, $D_1 < D_2$ (i.e. SR-2) for $G_{NF_w} > 0$, $G_{FN_w} > 0$ (shown in Fig. 4.3), the expressions for ripple Δi_{Lw} are formed using (2.13), and are shown in Table 4.4. The column-1 of the table presents the selected waveforms with slope conditions $G_{NF_w} > 0$, $G_{FN_w} > 0$. The column-2 presents the variations in D_t from 0 to 1. The column-3 presents the sequence name and column-4 presents the ripple expressions for each D_t as it varies from 0 to 1. As the ripple expressions are repeating, it is presented in terms of α, β, γ_2 and the corresponding notations is presented in column-5. The aim of this table is to show the effect of gate pulse shift on the inductor current patterns, sequence of states, and the ripple expressions.

It can be seen that Δi_{Lw} remains constant in sequences D-I, C-I, C-III, G-I, G-II and varies in sequences B-I, C-II, B-II. In the sequence B-I and B-II, Δi_{Lw} remains within the values $G_{NNw}D_1T_s + G_{FNw}(D_2 - D_1)T_s$ and $G_{NFw}D_1T_s + G_{FNw}D_2T_s$. However, Δi_{Lw} reduces within C-II. The variations of Δi_{Lw} within C-II is presented in Table 4.5. The column-1 of table presents the possible values of gate pulse shift. The inductor current patterns are presented in column-2. The inductor current ripple expressions in terms of β, γ_2 are presented in column-3 with the notations in column-4. The table is presented to show the effect of gate pulse shift within sequence C-II.

By comparing all the expressions of Δi_{Lw}, we observe that the minimum of Δi_{Lw} is $\max\{G_{NF_w}D_1T_s, G_{FN_w}D_2T_s\}$. Further we note that Δi_{Lw} remains same and is minimum for a range of D_t. This range occurs in the sub-range of sequence C-II. Therefore, for series SR-2 and slope condition $G_{NF_w} > 0$, $G_{FN_w} > 0$, we get,

$$\mathbf{D}_{min} := \{D_t \,\big|\, (D_1 + \underline{D_{PP_w}}) \le D_t \le (D_1 + \overline{D_{PP_w}})\} \quad \equiv \mathbf{D}_{PPw} \tag{4.1}$$

where

$$\underline{D_{PP_w}} = \frac{Min\{G_{NF_w}D_1, G_{FN_w}D_2\}}{|G_{FF_w}|}, \quad \overline{D_{PP_w}} = \frac{Max\{G_{NF_w}D_1, G_{FN_w}D_2\}}{|G_{FF_w}|}.$$

Similar to Table 4.4 and Table 4.5, other tables can be drawn for different slope conditions and duty ratios. Ripples for all other conditions are analyzed and compared similarly as described above for one condition. The rest of the tables are shown in Tables A.1 to A.15. The $\mathbf{D}_{min}$ obtained for all

Table 4.6: $\mathbf{D}_{min}$ in 36 conditions of i_{Lw}

$(D_1 + D_2)$	$G_{NF_w} > 0$ $G_{FN_w} > 0$	$G_{NF_w} > 0$ $G_{FN_w} < 0$	$G_{NF_w} < 0$ $G_{FN_w} > 0$	$G_{NF_w} < 0$ $G_{FN_w} < 0$	$G_{NF_w} = 0$ $G_{FN_w} < 0$	$G_{NF_w} = 0$ $G_{FN_w} > 0$	$G_{NF_w} > 0$ $G_{FN_w} = 0$	$G_{NF_w} < 0$ $G_{FN_w} = 0$
$D_1 > D_2$ < 1 $D_1 < D_2$ $D_1 = D_2$	$\mathbf{D}_{PPw}$	$\mathbf{D}_L$	$\mathbf{D}_L$	X	X	$\mathbf{D}_L$	$\mathbf{D}_L$	X
$D_1 > D_2$ > 1 $D_1 < D_2$ $D_1 = D_2$	X	$\mathbf{D}_G$	$\mathbf{D}_G$	$\mathbf{D}_{NNw}$	$\mathbf{D}_G$	X	X	$\mathbf{D}_G$
$D_1 > D_2$ $= 1$ $D_1 < D_2$ $D_1 = D_2$	X	D_1	D_1	X	X	X	X	X

36 conditions are summarized in Table 4.6. The rows of the table represent the possibilities of duty ratios and the columns of the table represent the possible slope conditions for either inductor current. The aim of this table is to present the value of $\mathbf{D}_{min}$ for all 36 inductor current possibilities of CI-SIDO converters. The different ranges $\mathbf{D}_L$, $\mathbf{D}_G$, $\mathbf{D}_{PPw}$ and $\mathbf{D}_{NNw}$ used in Table 4.6 are given by

$$\mathbf{D}_{min} := \{D_t \,\big|\, D_1 \leq D_t \leq (1 - D_2)\} \quad \equiv \mathbf{D}_L \tag{4.2}$$

$$\mathbf{D}_{min} := \{D_t \,\big|\, (1 - D_2) \leq D_t \leq D_1\} \quad \equiv \mathbf{D}_G \tag{4.3}$$

$$\mathbf{D}_{min} := \{D_t \,\big|\, (D_1 - \overline{D_{NN_w}}) \leq D_t \leq (D_1 - \underline{D_{NN_w}})\}, \quad \equiv \mathbf{D}_{NNw} \tag{4.4}$$

where

$$\underline{D_{NN_w}} = \frac{Min\{|G_{NF_w}|(1 - D_2), |G_{FN_w}|(1 - D_1)\}}{G_{NN_w}}, \quad \overline{D_{NN_w}} = \frac{Max\{|G_{NF_w}|(1 - D_2), |G_{FN_w}|(1 - D_1)\}}{G_{NN_w}} \tag{4.5}$$

Gate Pulse Shift for Minimum Ripples of Both Inductor Currents Together

The range of shifts D_t where both Δi_{L1} and Δi_{L2} are minimum, is the intersection of $\mathbf{D}_{min}$ for $\underline{\Delta i_{L1}}$ and $\mathbf{D}_{min}$ for $\underline{\Delta i_{L2}}$ in each of the nine sectors. From (4.1), (4.2), (4.3), (4.4), we observe that $\mathbf{D}_{PPw} \subset \mathbf{D}_L$ and $\mathbf{D}_{NNw} \subset \mathbf{D}_G$. Table 4.7 shows the $\mathbf{D}_{min}$ obtained by intersection of all $\mathbf{D}_{min}$ for $\underline{\Delta i_{L1}}$ and $\underline{\Delta i_{L2}}$. The rows of the table represent the 9 sectors and the column represent the possible values of duty ratios and the values of $\mathbf{D}_{min}$ for each sectors.

For sectors 1 and 9 in Table 4.7, we can observe that the intersections $\mathbf{D}_{PP1} \cap \mathbf{D}_{PP2}$ and $\mathbf{D}_{NN1} \cap \mathbf{D}_{NN2}$, always exist and is explained as follows. From Table 4.5 we note that $\mathbf{D}_{PP1}$, $\mathbf{D}_{PP2}$ are sub-ranges in

Table 4.7: $\mathbf{D}_{min}$ in 9 sectors for both minimum ripples

Sector No.	$(D_1 + D_2)$	$\mathbf{D}_{min}$
1	< 1	$\mathbf{D}_{PP1} \cap \mathbf{D}_{PP2}$
2	< 1	$\mathbf{D}_L \cap \mathbf{D}_{PP2} = \mathbf{D}_{PP2}$
3	< 1 > 1 $= 1$	$\mathbf{D}_L$ $\mathbf{D}_G$ D_1
4	< 1	$\mathbf{D}_{PP1} \cap \mathbf{D}_L = \mathbf{D}_{PP1}$
5	< 1 > 1 $= 1$	$\mathbf{D}_L$ $\mathbf{D}_G$ D_1
6	> 1	$\mathbf{D}_G \cap \mathbf{D}_{NN2} = \mathbf{D}_{NN2}$
7	< 1 > 1 $= 1$	$\mathbf{D}_L$ $\mathbf{D}_G$ D_1
8	> 1	$\mathbf{D}_{NN1} \cap \mathbf{D}_G = \mathbf{D}_{NN1}$
9	> 1	$\mathbf{D}_{NN1} \cap \mathbf{D}_{NN2}$

sequence C-II. The sequence C-II has states $NF \rightarrow FF \rightarrow FN \rightarrow FF$ with corresponding durations $D_1T_s \rightarrow (D_t - D_1)T_s \rightarrow D_2T_s \rightarrow (1 - D_2 - D_t)T_s$, as shown in Table 4.3. The total duration of state FF, $(D_t - D_1)T_s + (1 - D_2 - D_t)T_s = (1 - D_1 - D_2)T_s$ always remain same in all sub-ranges of C-II. From Fig. 4.3(d) we can note that, $\underline{D_{PPw}} + \overline{D_{PPw}} = (1 - D_1 - D_2)$. From which, we conclude that

$$\text{If } \underline{D_{PP1}} < \underline{D_{PP2}} \text{ then } \overline{D_{PP1}} > \overline{D_{PP2}} \Rightarrow \mathbf{D}_{PP2} \subset \mathbf{D}_{PP1}$$

$$\text{If } \underline{D_{PP1}} > \underline{D_{PP2}} \text{ then } \overline{D_{PP1}} < \overline{D_{PP2}} \Rightarrow \mathbf{D}_{PP1} \subset \mathbf{D}_{PP2}$$

Therefore, $\mathbf{D}_{PP1} \cap \mathbf{D}_{PP2}$ always exist. Similarly we can show that $\mathbf{D}_{NN1} \cap \mathbf{D}_{NN2}$ also always exist. To summarize the method of finding $\mathbf{D}_{min}$ that is presented in this section, a flowchart is added in Fig. 4.4. The flowchart explains that the input required is the input-output voltages and coupled inductor parameters. The duty ratios and the slopes are found using the available input. Then Table 4.2 and Table 4.3 are referred to find the series name and sequences. For each series, these tables represent sequence of states and its time durations as D_t varies from 0 to 1. Then tables of Appendix A are referred to find the $\mathbf{D}_{min}$ and $\underline{\Delta i_{Lw}}$. For each series, these tables represent and compare the ripple expressions as D_t varies from 0 to 1. The $\mathbf{D}_{min}$ for all 36 inductor current possibilities are presented in Table 4.6. The $\mathbf{D}_{min}$ corresponding to both $\underline{\Delta i_{L1}}$ and $\underline{\Delta i_{L2}}$ are presented in Table 4.7.

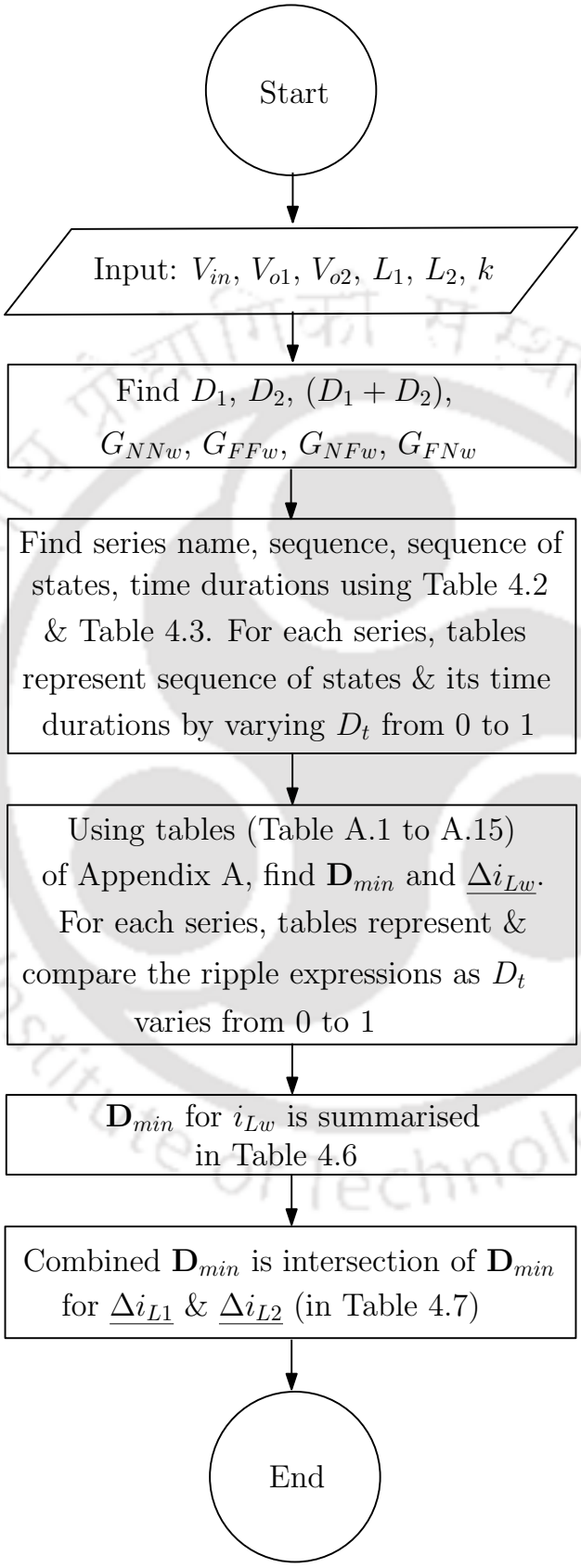
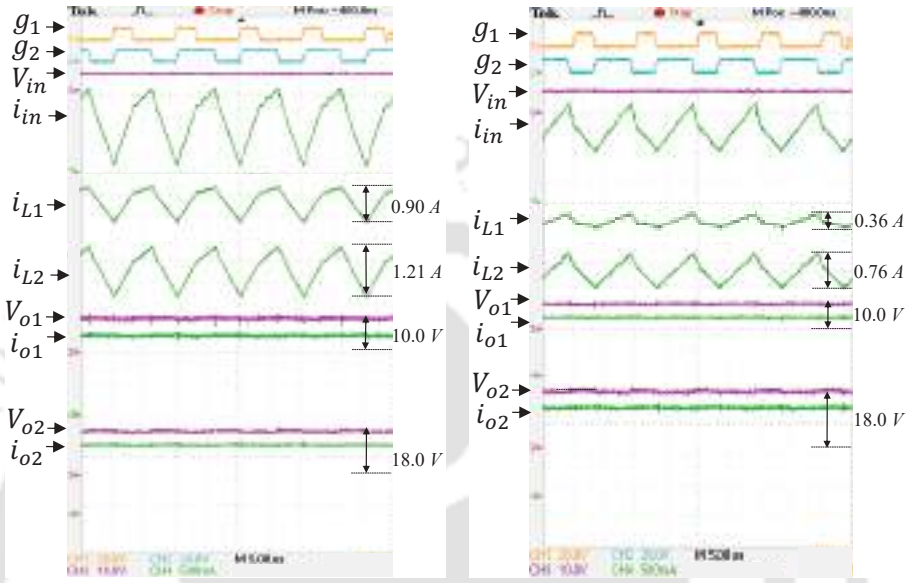


Figure 4.4: A flowchart to summarize the method of finding $\mathbf{D}_{min}$.

Table 4.8: Parameters

V_{in}	8 V	L_1	131.24 μH	L_2	94.61 μH	k	0.73
T_s	10 μs	C_1, C_2	100 μF	R_1	8 Ω	R_2	12 Ω



(a) $D_t = 0$ (b) $D_t = 0.3$

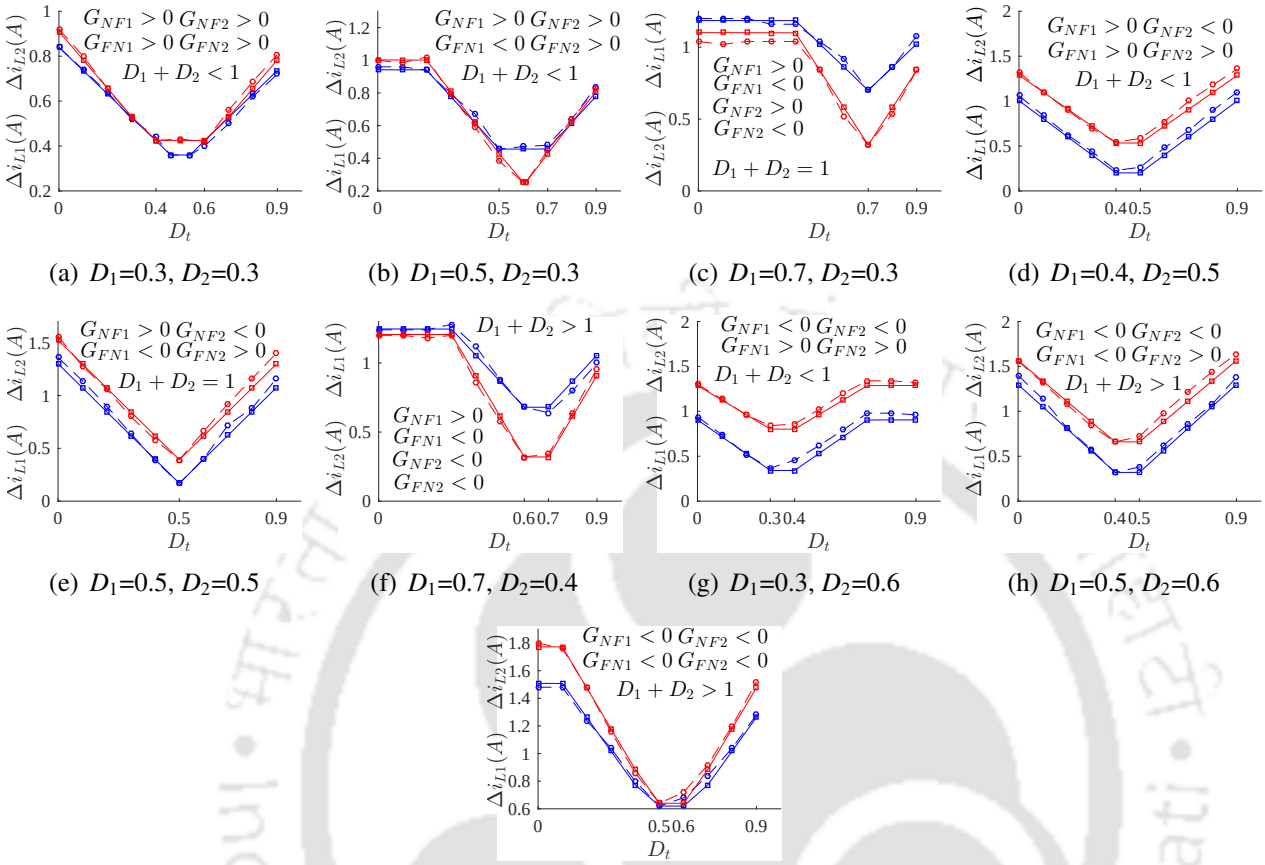
Figure 4.5: Experimental results for $D_1 = 0.3$, $D_2 = 0.6$.

4.3.3 Simulation and Experimental Results

The $\mathbf{D}_{min}$ derived for each condition is verified by developing a 100 W laboratory prototype of CI-SIDO boost (Fig. 3.4(b)). The design parameters are shown in Table 4.8. MOSFETs and diodes used are IRFP90N20DPBF and RHRP30120, respectively. $\mathbf{D}_{min}$ are also verified by simulating the CI-SIDO boost converter with same parameters in Matlab/Simulink environment. All the different conditions explained in Chapter 2 are generated by: first, computing the ratios r_{NF1}, r_{NF2}, r_{FN1}, r_{FN2} using Table 3.2 for chosen L_1, L_2; second, Fig. 3.2 is used to choose the duty ratios D_1, D_2 for which different slope conditions of i_{L1} and i_{L2} can be obtained.

The waveforms of g_1, g_2, V_{in}, i_{in}, i_{L1}, i_{L2}, V_{o1}, V_{o2}, i_{o1}, i_{o2} obtained experimentally, are presented in Fig. 4.5(a) and 4.5(b) for $D_1 = 0.3, D_2 = 0.6$. Fig. 4.5(a) and 4.5(b) show the results for $D_t = 0$ and $D_t = 0.3 \in \mathbf{D}_{min}$, respectively. It can be seen that V_{o1}, V_{o2}, i_{o1}, i_{o2} are unaffected by shift in g_2. However, there is significant reduction in Δi_{L1} and Δi_{L2}.

All the nine sectors are generated by choosing different values of D_1 and D_2. In each sector, $\mathbf{D}_{min}$



(a) D_1=0.3, D_2=0.3 (b) D_1=0.5, D_2=0.3 (c) D_1=0.7, D_2=0.3 (d) D_1=0.4, D_2=0.5

(e) D_1=0.5, D_2=0.5 (f) D_1=0.7, D_2=0.4 (g) D_1=0.3, D_2=0.6 (h) D_1=0.5, D_2=0.6

(i) D_1=0.7, D_2=0.6

Figure 4.6: Plots of measured Δi_{L1} (blue) and Δi_{L2} (red) vs D_t using simulation (square) and experimental (circle) data for sector no. : (a) 1 (b) 2 (c) 3 (d) 4 (e) 5 (f) 6 (g) 7 (h) 8 (i) 9.

shown in Table 4.7 is verified by varying shift D_t from 0 to 1 and measuring the ripples Δi_{L1} and Δi_{L2}. Simulated and experimental measurements of Δi_{L1}, Δi_{L2} for nine sectors are plotted in Fig. 4.6.

Table 4.9 compares the $\mathbf{D}_{min}$ obtained by - (i) analytically using Table 4.7, (ii) simulation, and (iii) experimental measurements corresponding to Fig. 4.6. It can be noted from Table 4.9 that $\mathbf{D}_{min}$ obtained by analytical, simulations and experimental measurements match for almost all the conditions. However, in Fig. 4.6(d) there is a slight mismatch in $\mathbf{D}_{min}$ obtained experimentally and from simulations. This is due to precision errors in calculating G_{NN_w}, G_{FF_w}, G_{NF_w}, G_{FN_w} as precision of values L_1, L_2 and k are limited.

Table 4.9 also tabulates the percentage reduction in ripples Δi_{L1} and Δi_{L2} when gate pulse g_2 is shifted by $\mathbf{D}_{min}$. The percentage is calculated with respect to the zero shifting. The percentage reduction is different for different conditions, and also different for Δi_{L1} and Δi_{L2}. The minimum

Table 4.9: Comparison of analytical, simulation and experimental $\mathbf{D}_{min}$, % reduction in Δi_{Lw} and % change in ΔI_{Lw}.

Fig. No.	$\mathbf{D}_{min}$			Reduction (%)		ΔI_{Lw} (%)	
	Analytical	Simulation	Experiment	Δi_{L1}	Δi_{L2}	ΔI_{L1}	ΔI_{L2}
4.6(a)	0.46-0.54	0.46-0.54	0.46-0.54	66.04	54.66	5.29	7.29
4.6(b)	0.59-0.61	0.59-0.61	0.59-0.61	53.85	78.24	5.01	13.95
4.6(c)	0.7	0.7	0.7	45.46	76.19	3.76	17.46
4.6(d)	0.43-0.46	0.43-0.46	0.4-0.5	87.35	58.48	7.75	10.25
4.6(e)	0.5	0.5	0.5	92.46	76.53	8.60	11.84
4.6(f)	0.62-0.68	0.62-0.68	0.62-0.68	49.30	79.34	2.88	16.17
4.6(g)	0.3-0.4	0.3-0.4	0.3-0.4	60.00	37.62	10.53	7.55
4.6(h)	0.44-0.46	0.44-0.46	0.42-0.48	87.54	58.48	9.16	10.67
4.6(i)	0.48-0.61	0.48-0.61	0.48-0.61	60.38	63.77	3.85	13.57

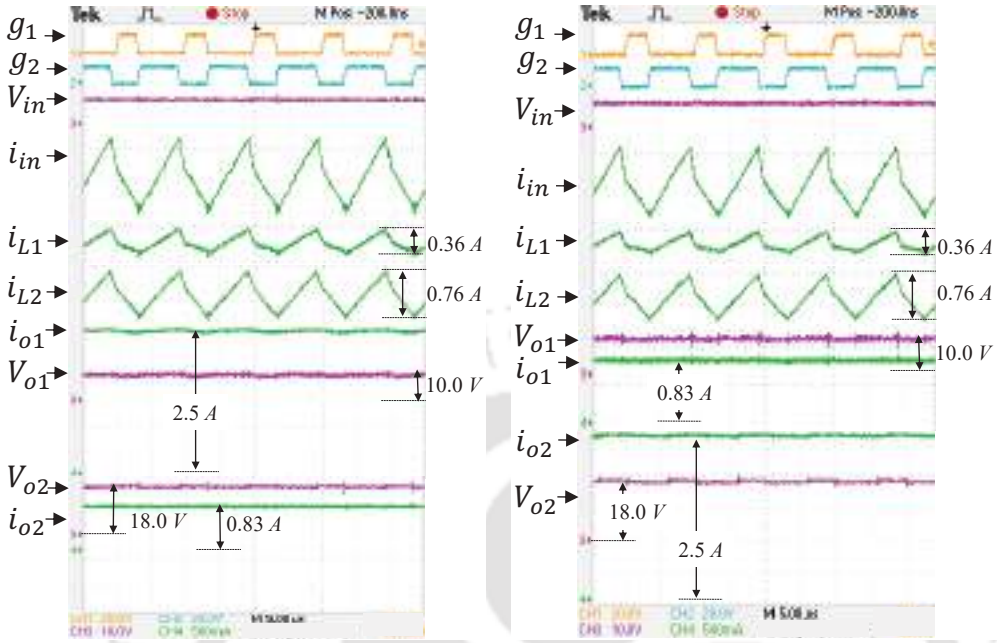
reductions for Δi_{L1} and Δi_{L2} are 45.46% and 37.62%, respectively. The maximum reductions for Δi_{L1} and Δi_{L2} are 92.46% and 79.34%, respectively. So, inductor current ripples are reduced significantly by shifting g_2 using $\mathbf{D}_{min}$ derived in this chapter.

The percentage change in average value of i_{Lw} ($\%\Delta I_{Lw}$) is also shown in Table 4.9. Note that, currents at any instant are denoted by i and average value of i over T_s is denoted by I. We observe a small change in I_{Lw} as D_t is varied, for the same values of I_{o1}, I_{o2}, D_1, D_2. This is because, the average values of diode currents (I_{dw}) are equal to I_{ow} and at any instant $i_{Lw} = i_{tw} + i_{dw}$ (Fig. 1.4(b)). As pattern of i_{tw} changes with variation in D_t, the value of i_{Lw} also changes such that i_{dw} obtains unchanged I_{dw} over T_s. $\%\Delta I_{Lw}$ is calculated with respect to the maximum value of I_{Lw}.

Although in Table 4.9, ΔI_{Lw} increases slightly for some values of $\mathbf{D}_{min}$, the maximum of i_{Lw} does not increase due to reduced ripples. The ratio of maximum i_{Lw} at $D_t = \mathbf{D}_{min}$ and $D_t = 0$ is found to be smaller than 1, for all cases.

The experimental results for $D_1 = 0.3$, $D_2 = 0.6$ and $D_t = 0.3$ with two sets of load currents $I_{o1} = 0.75I_{o1_{max}}$, $I_{o2} = 0.25I_{o2_{max}}$ and $I_{o1} = 0.25I_{o1_{max}}$, $I_{o2} = 0.75I_{o2_{max}}$ are shown in Fig. 4.7. It can be seen that the values of V_{o1}, V_{o2} are same for both the cases since output voltages are not affected by load currents in CCM. The values of Δi_{L1}, Δi_{L2} also are same for both the cases. It is because, as it can be seen from the analysis presented in Chapter 2, Δi_{Lw} depends on D_t and the sector in which D_1, D_2 lies. However, it is not affected by change in load currents, for same values of D_1, D_2 and D_t.

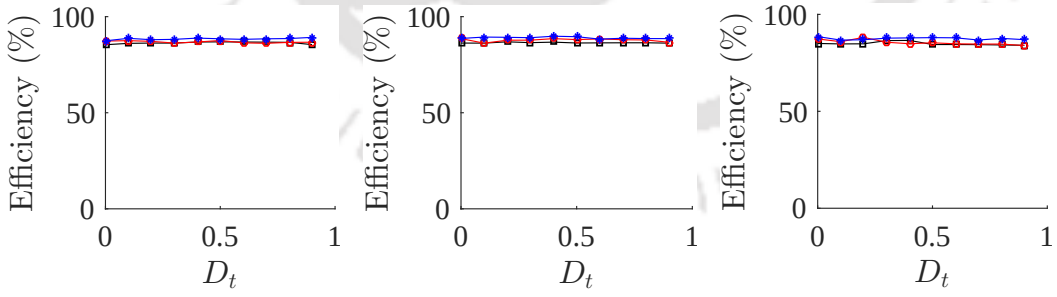
The efficiency of the converter is shown in Fig. 4.8 for different values of D_1 and D_2 as D_t is



(a) $I_{o1} = 0.75I_{o1_{max}}$, $I_{o2} = 0.25I_{o2_{max}}$ (b) $I_{o1} = 0.25I_{o1_{max}}$, $I_{o2} = 0.75I_{o2_{max}}$

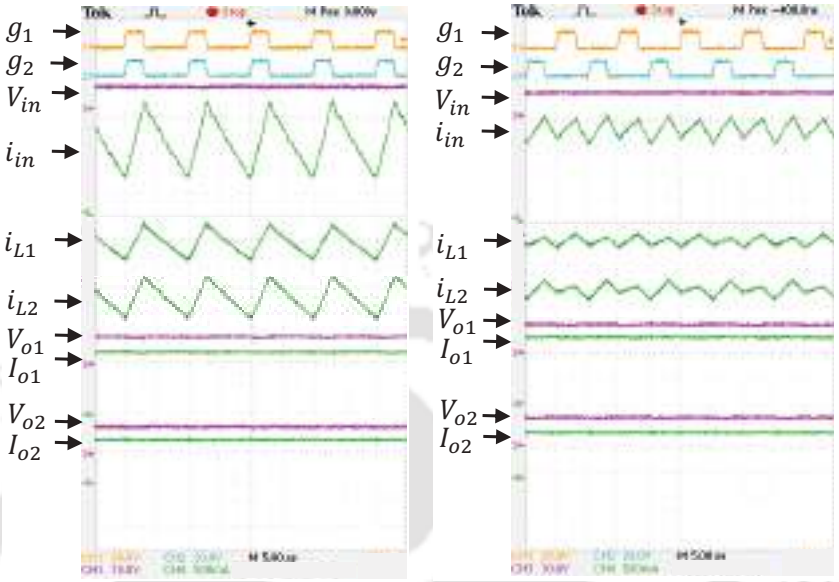
Figure 4.7: Experimental results for $D_1 = 0.3$, $D_2 = 0.6$, $D_t = 0.3$. $I_{ow_{max}}$ are values of I_{ow} at full load.

varied from 0 to 1. The results are also shown for different values of load currents. We observe that D_t does not have significant effect on efficiency. The waveforms of g_1, g_2, V_{in}, i_{L1}, i_{L2} V_{o1}, V_{o2}, I_{o1}, I_{o2} obtained experimentally in Fig. 4.9 for $D_1 = D_2 = 0.3$ and for $D_1 = 0.6$, $D_2 = 0.5$ in Fig. 4.10. Fig. 4.11(a) to Fig. 4.11 (h) show the experimental waveforms of g_1, g_2, i_{L1}, i_{L2} for $D_t = 0$ and $D_t \in \mathbf{D}_{min}$.



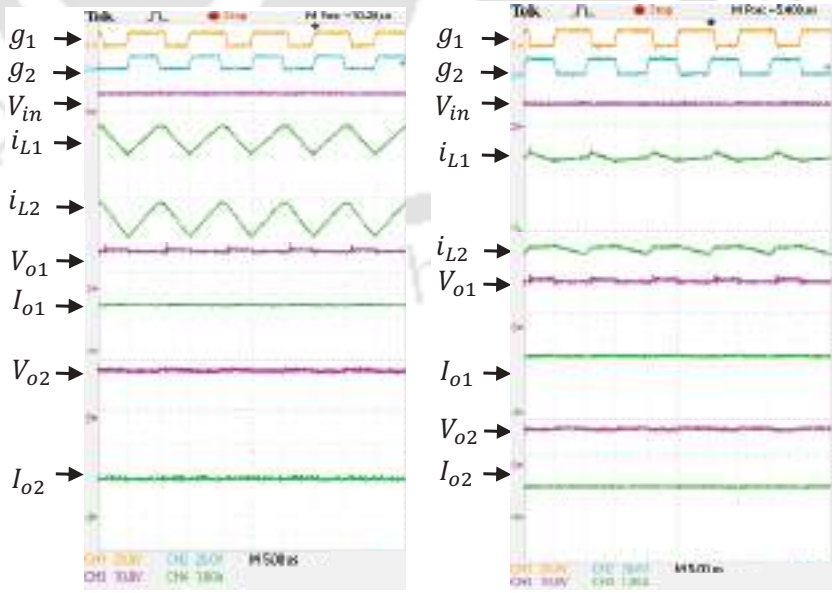
(a) D_1=0.3, D_2=0.3 (b) D_1=0.3, D_2=0.4 (c) D_1=0.5, D_2=0.4

Figure 4.8: Efficiency of converter as D_t is varied from 0 to 1 for $R_1 = 8\ \Omega$, $R_2 = 12\ \Omega$ (black square), $R_1 = 10\ \Omega$, $R_2 = 22\ \Omega$ (red circle) and $R_1 = 15\ \Omega$, $R_2 = 27\ \Omega$ (blue star).



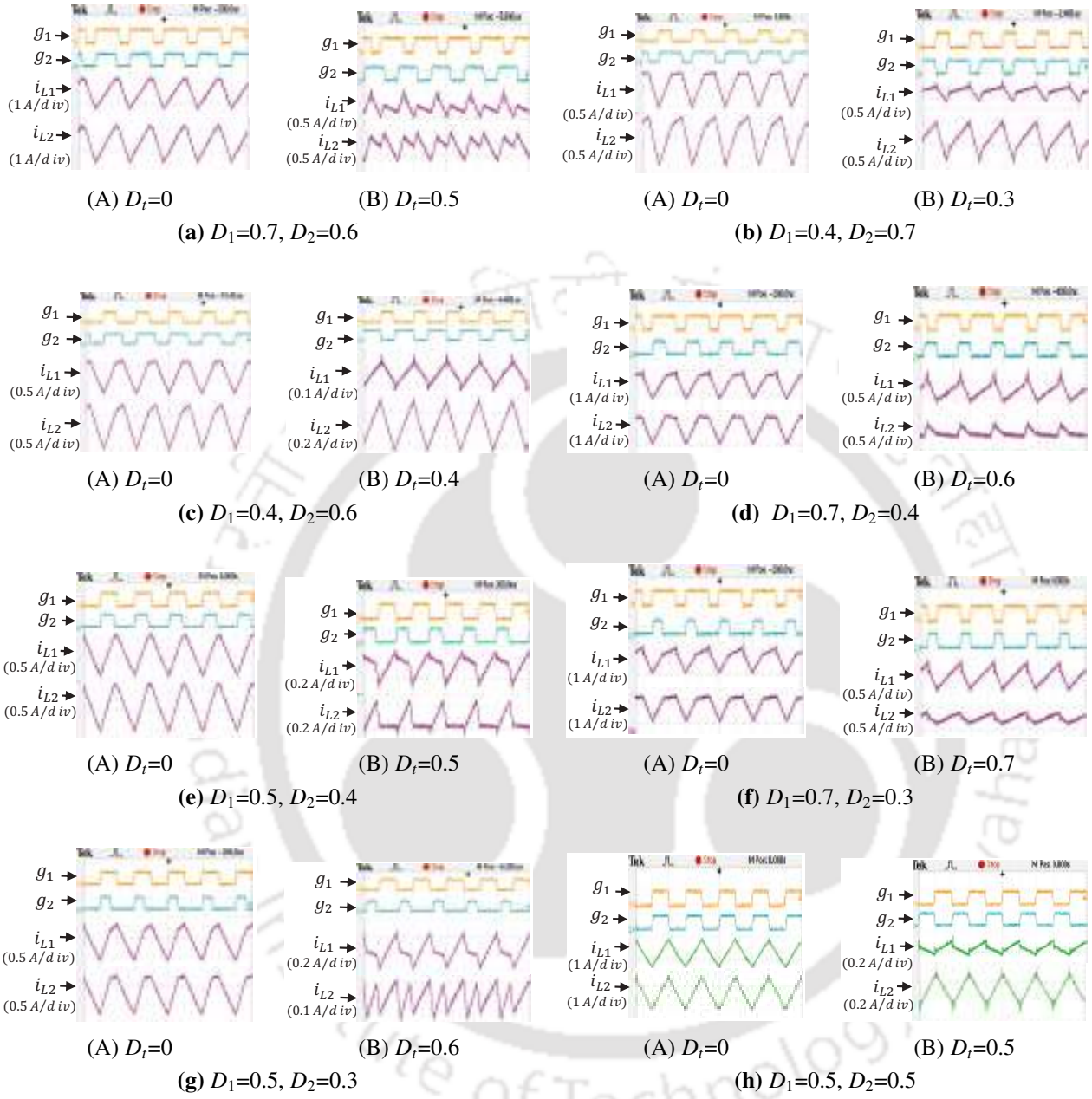
(a) $D_t = 0$ (b) $D_t = 0.5$

Figure 4.9: Experimental results for $D_1 = D_2 = 0.3$.



(a) $D_t = 0$ (b) $D_t = 0.5$

Figure 4.10: Experimental results for $D_1 = 0.6$, $D_2 = 0.5$.



(A) D_t=0 (B) D_t=0.5 (A) D_t=0 (B) D_t=0.3

(a) D_1=0.7, D_2=0.6 **(b)** D_1=0.4, D_2=0.7

(A) D_t=0 (B) D_t=0.4 (A) D_t=0 (B) D_t=0.6

(c) D_1=0.4, D_2=0.6 **(d)** D_1=0.7, D_2=0.4

(A) D_t=0 (B) D_t=0.5 (A) D_t=0 (B) D_t=0.7

(e) D_1=0.5, D_2=0.4 **(f)** D_1=0.7, D_2=0.3

(A) D_t=0 (B) D_t=0.6 (A) D_t=0 (B) D_t=0.5

(g) D_1=0.5, D_2=0.3 **(h)** D_1=0.5, D_2=0.5

Figure 4.11: Experimental results for different values of D_1 and D_2, at (A) $D_t = 0$ and (B) $D_t \in \mathbf{D}_{min}$.

It is to be noted that the theoretical waveforms presented in this chapter are for the analysis of the converter. These theoretical waveforms help to analyse the inductor current possibilities and the effect of gate pulse shift on the inductor current ripples. Each theoretical waveforms can be reproduced in simulations and experiments. For example, Fig. 4.12 presents the theoretical, experimental and simulation waveforms for $(D_1 + D_2) = 1$ and $D_1 = D_2$.

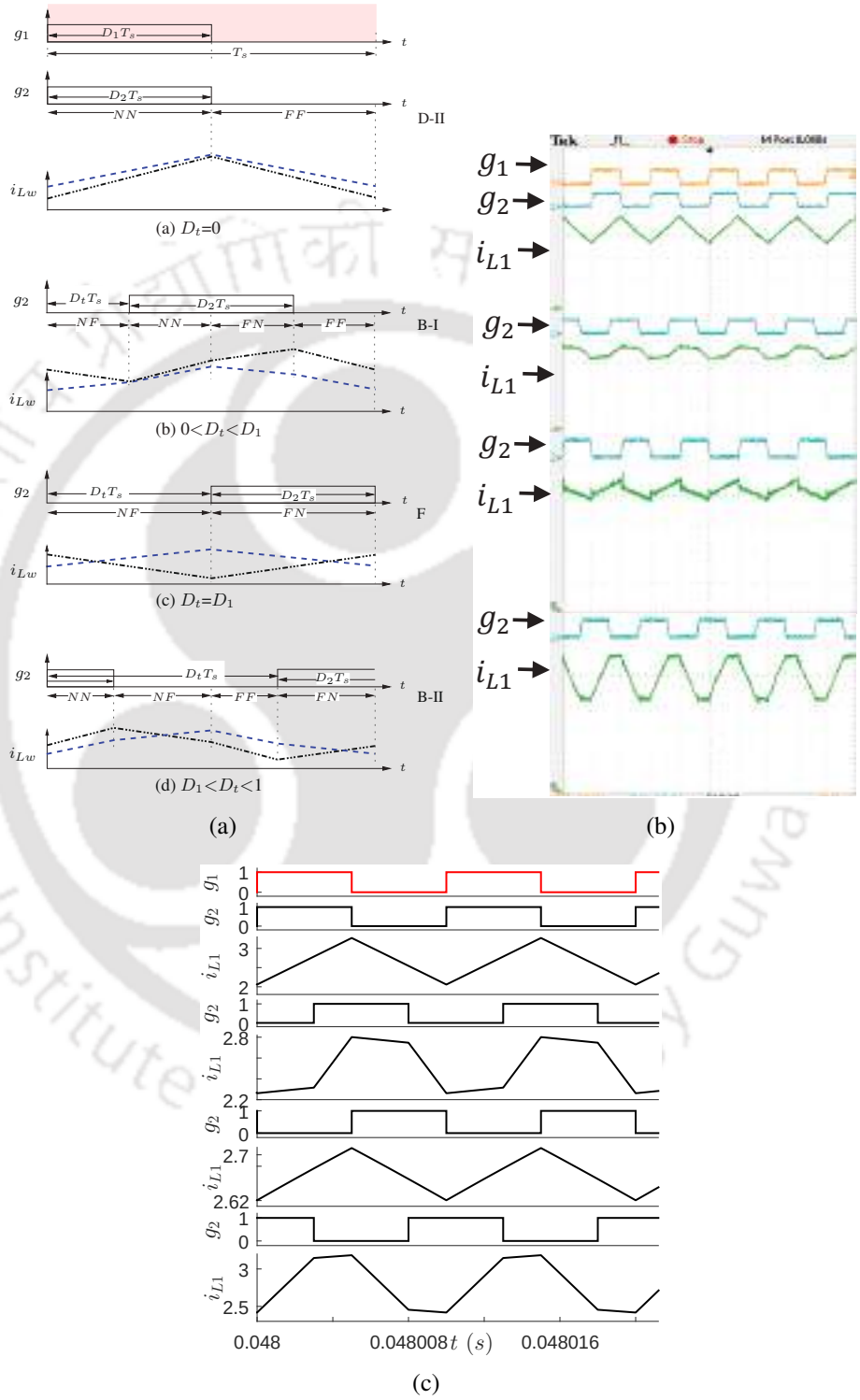


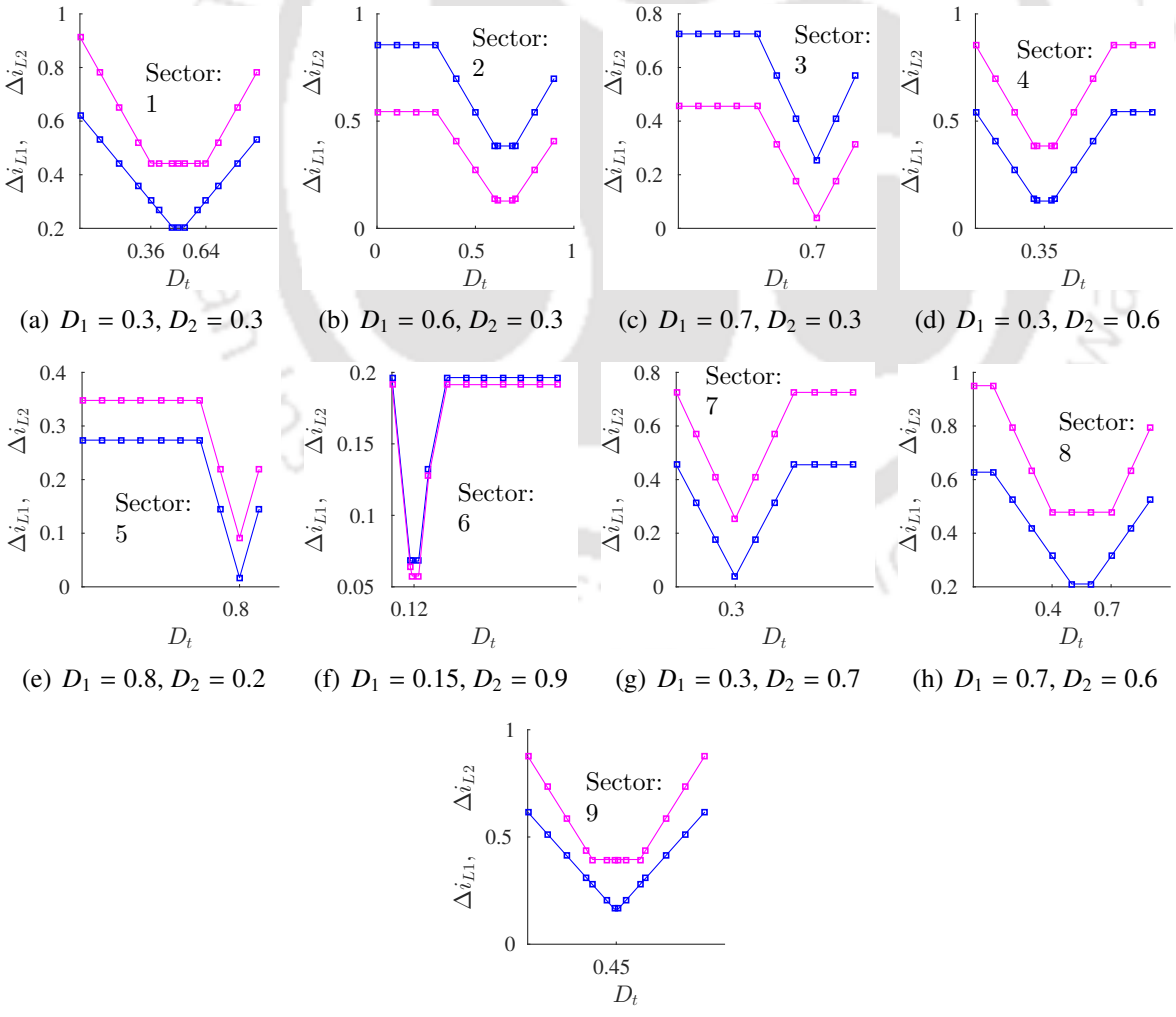
Figure 4.12: Different sequences D-II, B-I,... and different patterns of i_{Lw} waveforms for (i) $G_{NF_w} > 0$, $G_{FN_w} < 0$ (blue dashed lines), (ii) $G_{NF_w} < 0$, $G_{FN_w} > 0$ (black dash-dotted lines) when $(D_1 + D_2) = 1$ and $D_1 = D_2$ (i.e. SR-9) as D_t varied from 0 to 1 (a) theoretical, (b) experiments, and (c) simulations.

4.4 Extension of Gate Pulse Shift Methods to CI-SIDO Buck, CI-SIDO Buck-Boost and CI-SITO Boost

The values of $\mathbf{D}_{min}$ obtained in Table 4.7, is verified for CI-SIDO buck, CI-SIDO buck-boost for all the nine sectors. The analysis is similar to CI-SIDO boost converter. The simulation results are presented in the following sections.

4.4.1 Gate Pulse Shift for Minimum Inductor Current Ripples of CI-SIDO Buck

In CI-SIDO buck converter, formation of all nine sectors are not possible simultaneously, for one coupled inductor. First, the inductor values are selected, and sector diagrams are formed. Then D_1, D_2 are varied so as to generate each sector.



(a) $D_1 = 0.3, D_2 = 0.3$ (b) $D_1 = 0.6, D_2 = 0.3$ (c) $D_1 = 0.7, D_2 = 0.3$ (d) $D_1 = 0.3, D_2 = 0.6$

(e) $D_1 = 0.8, D_2 = 0.2$ (f) $D_1 = 0.15, D_2 = 0.9$ (g) $D_1 = 0.3, D_2 = 0.7$ (h) $D_1 = 0.7, D_2 = 0.6$

(i) $D_1 = 0.6, D_2 = 0.7$

Figure 4.13: Δi_{L1} (blue), Δi_{L2} (pink) vs. D_t for all 9 sectors of CI-SIDO buck converter.

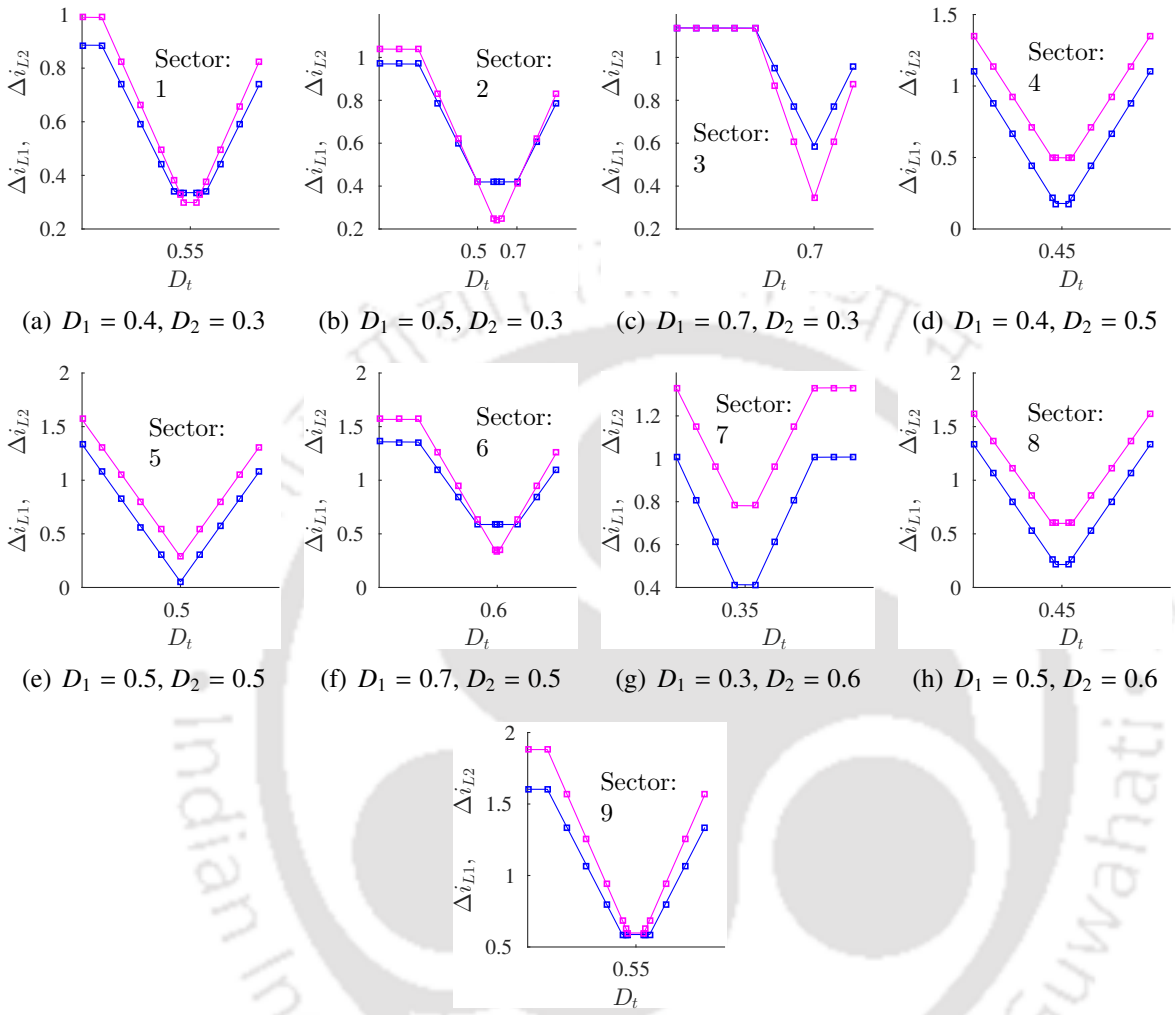
For $L_1 = 200.00\,\mu H$, $L_2 = 100.00\,\mu H$, $k = 0.8$, $\frac{1}{k\sqrt{\frac{L_1}{L_2}}} < 1$ and $k\sqrt{\frac{L_2}{L_1}} < 1$, the possible sectors are 1, 4, 7, 8, and 9. Each sector is generated by selecting suitable D_1, D_2. Δi_{L1}, Δi_{L2} versus D_t are shown for these sectors in Fig. 4.13. For $L_1 = 200.00\,\mu H$, $L_2 = 150.00\,\mu H$, $k = 0.8$, $\frac{1}{k\sqrt{\frac{L_1}{L_2}}} > 1$, and $k\sqrt{\frac{L_2}{L_1}} < 1$, the possible sectors are 1, 2, 4, 5, 6, 8, and 9. For this conditions only, Sector 5 and 6 are possible for CI-SIDO buck. Further, for generating these sectors, D_1, D_2 are selected accordingly. Δi_{L1}, Δi_{L2} versus D_t are shown for these sectors in Figs. 4.13(e)-4.13(f). For $L_1 = 100.00\,\mu H$, $L_2 = 200.00\,\mu H$, $k = 0.8$, $\frac{1}{k\sqrt{\frac{L_1}{L_2}}} > 1$ and $k\sqrt{\frac{L_2}{L_1}} > 1$, Sector 2 and 3 is generated using this coupled inductor. The waveforms of Δi_{L1}, Δi_{L2} versus D_t are shown in Figs. 4.13(b)-4.13(c). The results show that for all sectors, Δi_{L1}, Δi_{L2} decreases upto $D_t = \mathbf{D}_{min}$, then again increases if D_t is increased further. The simulation results are in agreement with the analysis and Table. 4.7.

4.4.2 Gate Pulse Shift for Minimum Inductor Current Ripples of CI-SIDO Buck-Boost

$\mathbf{D}_{min}$ for CI-SIDO buck-boost is verified by taking $L_1 = 200.00\,\mu H$, $L_2 = 150.00\,\mu H$, $k = 0.8$. First, the values of r_{NF1}, r_{FN1}, r_{NF2}, r_{FN2} are calculated and 9 sectors are identified as shown in Fig. 3.2. The values of D_1, D_2 are calculated to generate various sectors. The simulation results are shown in Fig. 4.14. The results show that the analysis is true for all the circuit conditions of CI-SIDO buck-boost.

4.4.3 Gate Pulse Shift for Minimum Inductor Current Ripples of Coupled Inductor Single Input Triple Output (CI-SITO) Boost Converter

The CI-SITO boost converter has one input V_{in} and three outputs V_{o1}, V_{o2}, V_{o3} as shown in Fig. 4.15. The switches include three diodes S_{d1}, S_{d2}, S_{d3} and three MOSFETs S_{t1}, S_{t2}, S_{t3} with gate pulses g_1, g_2, g_3 and corresponding duty ratios D_1, D_2, D_3. The topology has a coupled inductor with three windings L_1, L_2, L_3 and coupling coefficients k_{12} between windings L_1, L_2, k_{23} between L_2, L_3, and k_{13} between windings L_1, L_3. The voltage across the windings are given by (4.6). The voltage across windings are V_{in} when the MOSFETs are ON and $V_{in} - V_{ow}$ when MOSFETs are OFF where $w = 1$ for i_{L1}, $w = 2$ for i_{L2} and $w = 3$ for i_{L3}. The input-output voltage relationship in continuous



(a) $D_1 = 0.4$, $D_2 = 0.3$ (b) $D_1 = 0.5$, $D_2 = 0.3$ (c) $D_1 = 0.7$, $D_2 = 0.3$ (d) $D_1 = 0.4$, $D_2 = 0.5$

(e) $D_1 = 0.5$, $D_2 = 0.5$ (f) $D_1 = 0.7$, $D_2 = 0.5$ (g) $D_1 = 0.3$, $D_2 = 0.6$ (h) $D_1 = 0.5$, $D_2 = 0.6$

(i) $D_1 = 0.7$, $D_2 = 0.6$

Figure 4.14: Δi_{L1} (blue), Δi_{L2} (pink) vs. D_t for all 9 sectors of CI-SIDO buck-boost converter.

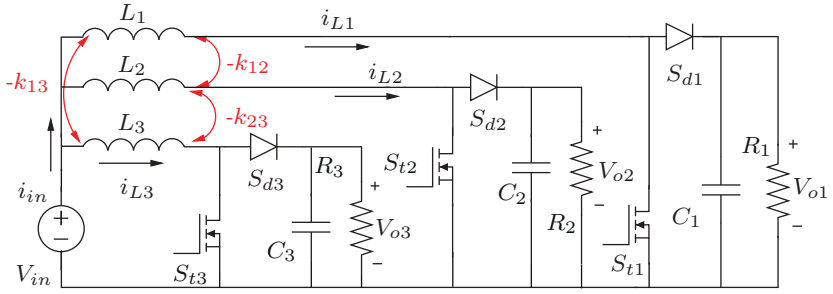


Figure 4.15: CI-SITO boost converter.

conduction mode (CCM) is independent of the coupling between the windings and is given by (4.7).

$$\begin{bmatrix} v_{L1} \\ v_{L2} \\ v_{L3} \end{bmatrix} = \left[\mathbf{L}\right] \frac{d}{dt} \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \end{bmatrix} \tag{4.6}$$

$$\text{where } \mathbf{L} = \begin{bmatrix} L_1 & -k_{12}\sqrt{L_1L_2} & -k_{13}\sqrt{L_1L_3} \\ -k_{12}\sqrt{L_1L_2} & L_2 & -k_{23}\sqrt{L_2L_3} \\ -k_{13}\sqrt{L_1L_3} & -k_{23}\sqrt{L_2L_3} & L_3 \end{bmatrix}$$

$$V_{o1} = \frac{V_{in}}{1-D_1}, \quad V_{o2} = \frac{V_{in}}{1-D_2}, \quad V_{o3} = \frac{V_{in}}{1-D_3} \tag{4.7}$$

Different Conditions of CI-SITO Boost Converter

The converter has three MOSFETs which give rise to eight possible states of the converter namely NNN, NNF, NFN, FNN, NFF, FNF, FFN, FFF where N represents the ON state and F represents the OFF state of the switches respectively. For each state, the slope of inductor current $\frac{di_{Lw}}{dt}$, is represented by G_{NNNw}, G_{NNFw}, G_{NFNw}, G_{NFFw}, G_{FNNw}, G_{FNFw}, G_{FFNw}, G_{FFFw} where $w = 1,\ 2,\ 3$ for i_{L1}, i_{L2}, i_{L3}. The slope of inductor current is formulated, in terms of winding voltages v_{L1}, v_{L2}, v_{L3} as presented in (4.8)-(4.9).

$$|\mathbf{L}| = L_1L_2L_3(1 - k_{12}^2 - k_{23}^2 - k_{13}^2 - 2k_{12}k_{23}k_{13}) \tag{4.8}$$

$$\frac{d}{dt}\begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \end{bmatrix} = \frac{1}{|\mathbf{L}|}\begin{bmatrix} L_2L_3(1-k_{23}^2) & L_3\sqrt{L_1L_2}(k_{12}+k_{13}k_{23}) & L_2\sqrt{L_1L_3}(k_{13}+k_{12}k_{23}) \\ L_3\sqrt{L_1L_2}(k_{12}+k_{13}k_{23}) & L_1L_3(1-k_{13}^2) & L_1\sqrt{L_2L_3}(k_{23}+k_{12}k_{13}) \\ L_2\sqrt{L_1L_3}(k_{13}+k_{12}k_{23}) & L_1\sqrt{L_2L_3}(k_{23}+k_{12}k_{13}) & L_1L_2(1-k_{12}^2) \end{bmatrix}\begin{bmatrix} v_{L1} \\ v_{L2} \\ v_{L3} \end{bmatrix} \tag{4.9}$$

Here, positive values of (4.8) is taken which is possible only for few combinations of k_{12}, k_{23}, k_{13}. This analysis is presented below-

Suppose $k_{12} = k_{23} = k >> k_{13}$

$$1 - 2k^2k_{13} - 2k^2 > 0 \implies \text{If } k_{13} = 0,\ k < 0.707 \tag{4.10}$$

In this case, the highest value which k_{12}, k_{23} takes is 0.707 and k_{13} is very less than 0.707.

Suppose $k_{12} > k_{23} > k_{13}$

$$1 - 2k_{12}^3 - 3k_{12}^2 > 0 \implies k_{12} < 0.5 \tag{4.11}$$

In this case, for feasible systems, k_{12} which is largest amongst k_{23}, k_{13} is smaller than 0.5. This means all coupling coefficient is smaller than 0.5.

Suppose $k_{12} = k, k_{23} = k_{13}$ **is very small, say** u

$$1 - 2ku^2 - k^2 > 0 \implies k < 1 \tag{4.12}$$

So, in this condition, any value of k_{12} is possible between 0 to 1. Here, case 1 is considered for the analysis.

Slope Calculation

To calculate the slopes of i_{L1}, i_{L2}, i_{L3} in, say state NNN, the values of $[v_{L1}\ v_{L2}\ v_{L3}]^T$ is $[V_{in}\ V_{in}\ V_{in}]^T$. These values of voltages are substituted in (4.9) to get the slopes G_{NNN1}, G_{NNN2} and G_{NNN3}. Similarly, to calculate the slopes of i_{L1}, i_{L2}, i_{L3} in state FFF, the values of $[v_{L1}\ v_{L2}\ v_{L3}]^T$ is $[V_{in} - V_{o1}\ V_{in} - V_{o2}\ V_{in} - V_{o3}]^T$. These values of voltages are substituted in (4.9) to get the slopes G_{FFF1}, G_{FFF2} and G_{FFF3}. The calculation shows that the slope conditions in states NNN and FFF are always positive and negative respectively. However, for the slope in the states like NNF, the values of $[v_{L1}\ v_{L2}\ v_{L3}]^T$ is $[V_{in}\ V_{in}\ V_{in} - V_{o3}]^T$. So, these slopes can take both negative and positive values.

The slopes of i_{L1} in all the eight states are shown in (4.13). Similarly, slopes can be formulated for i_{L2} and i_{L3} as well. From the slope expressions, it is found that–

- The slopes of inductor current in each states are different.
- In a particular state, the slopes of i_{L1}, i_{L2} and i_{L3} are different.
- $G_{NNNw} > 0$ and $G_{FFFw} < 0$ always.
- G_{NFFw}, G_{FNFw}, G_{FFNw}, G_{NNFw}, G_{NFNw}, G_{FNNw} can be positive or negative depending on the values of coupled inductor parameters and input, output voltages.

- For $G_{NFFw} > 0$, $G_{FNFw} > 0$, $G_{FFNw} > 0$, $G_{NNFw} > 0$, $G_{NFNw} > 0$, $G_{FNNw} > 0$, it is always true that $G_{NNNw} > G_{NFFw}$, $G_{NNNw} > G_{FNFw}$, $G_{NNNw} > G_{FFNw}$, $G_{NNNw} > G_{NNFw}$, $G_{NNNw} > G_{NFNw}$, $G_{NNNw} > G_{FNNw}$.

- Similarly, for $G_{NFFw} < 0$, $G_{FNFw} < 0$, $G_{FFNw} < 0$, $G_{NNFw} < 0$, $G_{NFNw} < 0$, $G_{FNNw} < 0$, it is always true that $|G_{FFFw}| > |G_{NFFw}|$, $|G_{FFFw}| > |G_{FNFw}|$, $|G_{FFFw}| > |G_{FFNw}|$, $|G_{FFFw}| > |G_{NNFw}|$, $|G_{FFFw}| > |G_{NFNw}|$, $|G_{FFFw}| > |G_{FNNw}|$.

$$G_{NNN1} = \frac{V_{in}}{\mathbf{L}}\Big[L_2L_3(1-k_{23}^2) + L_3\sqrt{L_1L_2}(k_{12}+k_{13}k_{23}) + L_2\sqrt{L_1L_3}(k_{13}+k_{12}k_{23})\Big] \tag{4.13a}$$

$$G_{NNF1} = \frac{1}{\mathbf{L}}\Big[[L_2L_3(1-k_{23}^2) + L_3\sqrt{L_1L_2}(k_{12}+k_{13}k_{23}) + L_2\sqrt{L_1L_3}(k_{13}+k_{12}k_{23})]V_{in} - L_2\sqrt{L_1L_3}(k_{13}+k_{12}k_{23})V_{o3}\Big] \tag{4.13b}$$

$$G_{NFN1} = \frac{1}{\mathbf{L}}\Big[[L_2L_3(1-k_{23}^2) + L_3\sqrt{L_1L_2}(k_{12}+k_{13}k_{23}) + L_2\sqrt{L_1L_3}(k_{13}+k_{12}k_{23})]V_{in} - L_3\sqrt{L_1L_2}(k_{12}+k_{13}k_{23})V_{o2}\Big] \tag{4.13c}$$

$$G_{FNN1} = \frac{1}{\mathbf{L}}\Big[[L_2L_3(1-k_{23}^2) + L_3\sqrt{L_1L_2}(k_{12}+k_{13}k_{23}) + L_2\sqrt{L_1L_3}(k_{13}+k_{12}k_{23})]V_{in} - L_2L_3(1-k_{23}^2)V_{o1}\Big] \tag{4.13d}$$

$$G_{FFN1} = \frac{1}{\mathbf{L}}\Big[[L_2L_3(1-k_{23}^2) + L_3\sqrt{L_1L_2}(k_{12}+k_{13}k_{23}) + L_2\sqrt{L_1L_3}(k_{13}+k_{12}k_{23})]V_{in} - L_2L_3(1-k_{23}^2)V_{o1} - L_3\sqrt{L_1L_2}(k_{12}+k_{13}k_{23})V_{o2}\Big] \tag{4.13e}$$

$$G_{FNF1} = \frac{1}{\mathbf{L}}\Big[[L_2L_3(1-k_{23}^2) + L_3\sqrt{L_1L_2}(k_{12}+k_{13}k_{23}) + L_2\sqrt{L_1L_3}(k_{13}+k_{12}k_{23})]V_{in} - L_2L_3(1-k_{23}^2)V_{o1} - L_2\sqrt{L_1L_3}(k_{13}+k_{12}k_{23})V_{o3}\Big] \tag{4.13f}$$

$$G_{NFF1} = \frac{1}{\mathbf{L}}\Big[[L_2L_3(1-k_{23}^2) + L_3\sqrt{L_1L_2}(k_{12}+k_{13}k_{23}) + L_2\sqrt{L_1L_3}(k_{13}+k_{12}k_{23})]V_{in} - L_3\sqrt{L_1L_2}(k_{12}+k_{13}k_{23})V_{o2} - L_2\sqrt{L_1L_3}(k_{13}+k_{12}k_{23})V_{o3}\Big] \tag{4.13g}$$

$$G_{FFF1} = \frac{1}{\mathbf{L}}\Big[[L_2L_3(1-k_{23}^2) + L_3\sqrt{L_1L_2}(k_{12}+k_{13}k_{23}) + L_2\sqrt{L_1L_3}(k_{13}+k_{12}k_{23})]V_{in} - L_2L_3(1-k_{23}^2)V_{o1} - L_3\sqrt{L_1L_2}(k_{12}+k_{13}k_{23})V_{o2} - L_2\sqrt{L_1L_3}(k_{13}+k_{12}k_{23})V_{o3}\Big] \tag{4.13h}$$

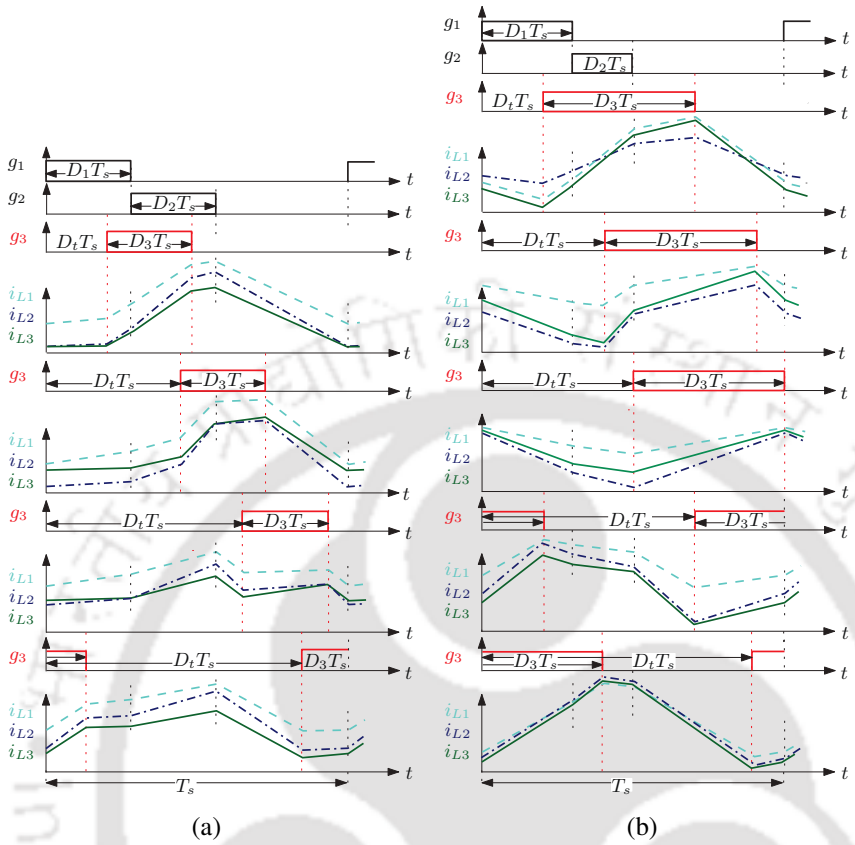


Figure 4.16: Effect of shifting gate pulse in CI-SITO boost converter for (a) $D_1 = D_2 = D_3$ and $D_1 + D_2 + D_3 < 1$, and (b) $D_3 > D_1 > D_2$ and $D_1 + D_2 + D_3 = 1$.

Effect of Gate Pulse Shifting

This section shows the effect of shifting the gate pulse on inductor current ripples. Two examples of gate pulses are taken for the analysis.

As the converter has three gate pulses, the shifting of g_2, g_3 is done with respect to the starting point of g_1. The gate pulse g_2 is shifted by a fixed value D_1T_s. The gate pulse g_3 is shifted such that it varies from 0 to 1 and is denoted by D_t. The ripple expression is denoted by Δi_{Lw} where $w = 1$ for i_{L1}, $w = 2$ for i_{L2} and $w = 3$ for i_{L3}. The expression of Δi_{Lw} is found by (2.13).

An example of gate pulses and inductor currents are shown in Fig. 4.16(a). The three inductor currents are shown for $D_1 = D_2 = D_3$ and $D_1 + D_2 + D_3 < 1$ as the shift, D_t varies from 0 to 1. The slope condition that is taken for the analysis is $G_{NNNw} > 0$, $G_{NFFw} > 0$, $G_{FNFw} > 0$, $G_{FFNw} > 0$, $G_{NNFw} > 0$, $G_{NFNw} > 0$, $G_{FNNw} > 0$, $G_{FFFw} < 0$. As D_t changes, the states of the converter changes, thus changing the ripple expression. At $D_t = 0$, the states of the converter are $NFN \rightarrow FNF \rightarrow FFF$.

Table 4.10: Inductor Current Ripple Expressions for $D_1 = D_2 = D_3$, $D_1 + D_2 + D_3 < 1$, and Slope Condition $G_{NNNw} > 0$, $G_{NFFw} > 0$, $G_{FNFw} > 0$, $G_{FFNw} > 0$, $G_{NNFw} > 0$, $G_{NFNw} > 0$, $G_{FNNw} > 0$, $G_{FFFw} < 0$ (Fig. 4.16(a))

States	Shift	Ripples
NFN, FNF, FFF	$D_t = 0$	$\lvert G_{FFFw}\rvert(1 - D_1 - D_2)T_s$
NFF, NFN, FNN, FNF, FFF	$0 < D_t < D_1$	$\lvert G_{FFFw}\rvert(1 - D_1 - D_2)T_s$
NFF, FNN, FFF	$D_t = D_1$	$\lvert G_{FFFw}\rvert(1 - D_1 - D_2)T_s$
NFF, FNF, FNN, FFN, FFF	$D_1 < D_t < (D_1 + D_2)$	$\lvert G_{FFFw}\rvert(1 - D_1 - D_2 - D_3)T_s < \Delta i_{Lw} < \lvert G_{FFFw}\rvert(1 - D_1 - D_2)T_s$
NFF, FNF, FFN, FFF	$D_t = (D_1 + D_2)$	$\lvert G_{FFFw}\rvert(1 - D_1 - D_2 - D_3)T_s$
NFF, FNF, FFF, FFN, FFF	$(D_1 + D_2) < D_t < (D_1 + D_2 + \underline{D_{PPPw}})$	$\max\{G_{NFFw}D_1T_s + G_{FNFw}D_2T_s, G_{FFNw}D_3T_s\} < \Delta i_{Lw} < \lvert G_{FFFw}\rvert(1 - D_1 - D_2 - D_3)T_s$
NFF, FNF, FFF, FFN, FFF	$(D_1 + D_2 + \underline{D_{PPPw}}) \leq D_t \leq (D_1 + D_2 + \overline{D_{PPPw}})$	$\max\{G_{NFFw}D_1T_s + G_{FNFw}D_2T_s, G_{FFNw}D_3T_s\}$
NFF, FNF, FFF, FFN, FFF	$(D_1 + D_2 + \overline{D_{PPPw}}) < D_t < (1 - D_3)$	$\max\{G_{NFFw}D_1T_s + G_{FNFw}D_2T_s, G_{FFNw}D_3T_s\} < \Delta i_{Lw} < \lvert G_{FFFw}\rvert(1 - D_1 - D_2 - D_3)T_s$
NFF, FNF, FFF, FFN	$D_t = (1 - D_3)$	$\lvert G_{FFFw}\rvert(1 - D_1 - D_2 - D_3)T_s$
NFN, NFF, FNF, FFF, FFN	$(1 - D_3) < D_t < 1$	$\lvert G_{FFFw}\rvert(1 - D_1 - D_2 - D_3)T_s < \Delta i_{Lw} < \lvert G_{FFFw}\rvert(1 - D_1 - D_2)T_s$

The ripple expression is given by (4.14).

$$\Delta i_{Lw} = G_{NFNw}D_1T_s + G_{FNFw}D_2T_s = |G_{FFFw}|(1 - D_1 - D_2)T_s \tag{4.14}$$

At $0 < D_t < D_1$, the states of the converter are $NFF \rightarrow NFN \rightarrow FNN \rightarrow FNF \rightarrow FFF$. The ripple expression is given by (4.15).

$$\begin{aligned}\Delta i_{Lw} &= G_{NFFw}D_tT_s + G_{NFNw}(D_1 - D_t)T_s + G_{FNNw}(D_t + D_3 - D_1)T_s + G_{FNFw}(D_1 + D_2 - D_3 - D_t)T_s \\ &= |G_{FFFw}|(1 - D_1 - D_2)T_s\end{aligned} \tag{4.15}$$

At $D_t = (D_1 + D_2)T_s$, the states of the converter are $NFF \rightarrow FNF \rightarrow FFN \rightarrow FFF$. The ripple expression is given by (4.16).

$$\Delta i_{Lw} = G_{NFFw}D_1T_s + G_{FNFw}D_2T_s + G_{FFNw}D_3T_s = |G_{FFFw}|(1 - D_1 - D_2 - D_3)T_s \tag{4.16}$$

Table 4.11: Inductor Current Ripple Expressions for $D_3 > D_1 > D_2$, $D_1 + D_2 + D_3 = 1$, and Slope Condition $G_{NNNw} > 0$, $G_{NFFw} < 0$, $G_{FNFw} < 0$, $G_{FFNw} > 0$, $G_{NNFw} > 0$, $G_{NFNw} > 0$, $G_{FNNw} > 0$, $G_{FFFw} < 0$ (Fig. 4.16(b))

States	Shift	Ripples
NFN, FNN, FFF	$D_t = 0$	$G_{FNNw}D_2T_s + G_{NFNw}D_1T_s$
NFF, NFN, FNN, FFN, FFF	$0 < D_t < D_1$	$G_{FNNw}D_2T_s + G_{FFNw}D_1T_s < \Delta i_{Lw} < G_{FNNw}D_2T_s + G_{NFNw}D_1T_s$
NFF, FNN, FFN, FFF	$D_t = D_1$	$G_{FNNw}D_2T_s + G_{FFNw}D_1T_s$
NFF, FNF, FNN, FFN, FFF	$D_1 < D_t < (D_1 + D_2)$	$G_{FFNw}D_3T_s < \Delta i_{Lw} < G_{FNNw}D_2T_s + G_{FFNw}D_1T_s$
NFF, FNF, FFN	$D_t = (D_1 + D_2)$	$G_{FFNw}D_3T_s$
NFN, NFF, FNF, FFF, FFN	$(D_1 + D_2) < D_t < (1 - D_2)$	$G_{FFNw}D_3T_s < \Delta i_{Lw} < G_{NFNw}D_1T_s + G_{FFNw}D_2T_s$
NFN, FNF, FFF, FFN	$D_t = (1 - D_2)$	$G_{NFNw}D_1T_s + G_{FFNw}D_2T_s$
NFN, FNN, FNF, FFF, FFN	$(1 - D_2) < D_t < 1$	$G_{NFNw}D_1T_s + G_{FFNw}D_2T_s < \Delta i_{Lw} < G_{FNNw}D_2T_s + G_{NFNw}D_1T_s$

The comparison of the expressions shows that ripples are getting reduced as D_t is changed. The ripple expressions for different values of D_t are presented in Table 4.10. The rows of the table represent the possible gate pulse shifts and the columns represent the states, shifts and the ripples corresponding to each shift. This table is added to find the ripple expressions at each shift and to find the minimum ripples by comparisons. Comparing all the ripple expressions, it is found that the minimum value of ripple expression is given in (4.17). The corresponding range of D_t is presented in (4.18).

$$\max\{G_{NFFw}D_1T_s + G_{FNFw}D_2T_s, G_{FFNw}D_3T_s\} \tag{4.17}$$

$$(D_1 + D_2 + \underline{D_{PPPw}}) \leq D_t \leq (D_1 + D_2 + \overline{D_{PPPw}}) \tag{4.18}$$

where

$$\underline{D_{PPPw}} = \frac{\min\{G_{NFFw}D_1T_s + G_{FNFw}D_2T_s, G_{FFNw}D_3T_s\}}{|G_{FFFw}|}$$
$$\overline{D_{PPPw}} = \frac{\max\{G_{NFFw}D_1T_s + G_{FNFw}D_2T_s, G_{FFNw}D_3T_s\}}{|G_{FFFw}|}$$

So, if the converter is operated with shift according to (4.18), the ripple in inductor current is reduced for the slope condition $G_{NNNw} > 0$, $G_{NFFw} > 0$, $G_{FNFw} > 0$, $G_{FFNw} > 0$, $G_{NNFw} > 0$, $G_{NFNw} > 0$, $G_{FNNw} > 0$, $G_{FFFw} < 0$.

Table 4.12: Simulation Parameters

V_{in}	6 V	$L_1 = L_2 = L_3$	100 μH
$k_{12} = k_{23}$	0.6	k_{13}	0.2
$R_1,\ R_2,\ R_3$	3, 5, 5 Ω	$D_1 = D_2 = D_3$	0.3

Table 4.13: Simulation Parameters

V_{in}	6 V	$L_1,\ L_2,\ L_3$	200, 150 , 100 μH
$k_{12} = k_{23}$	0.6	k_{13}	0.2
$R_1,\ R_2,\ R_3$	3, 5, 7 Ω	$D_1,\ D_2,\ D_3$	0.3, 0.2, 0.5

Similar analysis is done for different slope conditions of CI-SITO boost converter as shown in Fig. 4.16(b). The duty ratios are $D_3 > D_1 > D_2$, $D_3 = D_1 + D_2$, and $D_1 + D_2 + D_3 = 1$. The slope condition is given by $G_{NNNw} > 0$, $G_{NFFw} < 0$, $G_{FNFw} < 0$, $G_{FFNw} > 0$, $G_{NNFw} > 0$, $G_{NFNw} > 0$, $G_{FNNw} > 0$, $G_{FFFw} < 0$. As D_t changes from 0 to 1, the ripple expression are presented in Table 4.11. The rows of the table represent the possible gate pulse shifts and the columns represent the states, shifts and the ripples corresponding to each shift. This table is also added to find the ripple expressions at each shift and to find the minimum ripples by comparisons. Comparing all the expressions, it is found that the minimum ripple is given by (4.19). The corresponding D_t is at $D_1 + D_2$.

$$\Delta i_{Lw} = G_{FFNw} D_3 T_s \tag{4.19}$$

Simulation Results

This section verifies the analysis done for the CI-SITO boost converter. The simulations are done in MATLAB/Simulink for two sets of parameters as presented in Table 4.12 and Table 4.13. Keeping the parameters same, the values of inductor current ripples are obtained at different D_t varying from 0 to 1. The ripples at all D_t are compared to find the minimum inductor current ripples. The waveforms of i_{L1}, i_{L2}, i_{L3} at $D_t = 0$ and D_t where ripples are minimum are plotted for the two sets of parameters. The plots of ripples vs. D_t are also presented. The simulations for the parameters presented in Table 4.12 is presented in Fig. 4.17. The figure shows the waveforms of i_{L1}, i_{L2} and i_{L3} at $D_t = 0$ and $D_t = 0.64$. The waveforms show that the ripples in the inductor current reduces as gate pulses are shifted. The value of $\Delta i_{L1} = 2.1\ A$ at $D_t = 0$ and reduces to $\Delta i_{L1} = 0.7\ A$ as D_t is changed to 0.64. Similarly, Δi_{L2} reduces from 2.6 A to 0.8 A and Δi_{L3} reduces from 2.1 A to 0.5 A. The ripple values

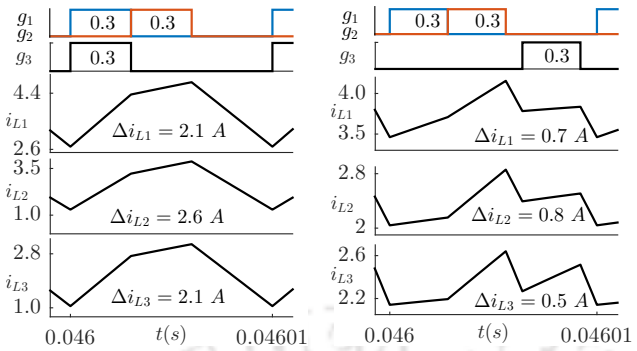


Figure 4.17: i_{L1}, i_{L2} and i_{L3} waveforms for $D_1 = 0.3$, $D_2 = 0.3$, $D_3 = 0.3$ for (a) $D_t = 0$, (b) $D_t = 0.64$.

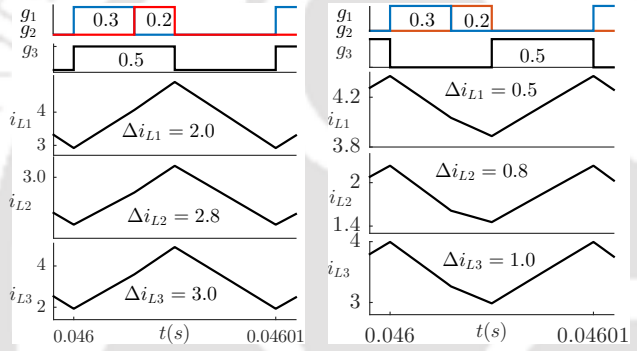
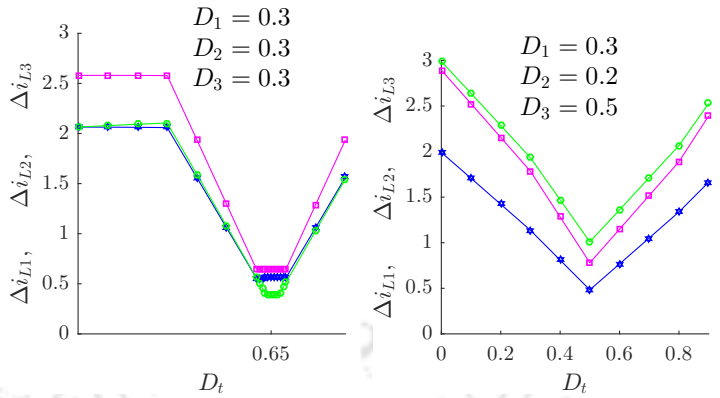


Figure 4.18: i_{L1}, i_{L2} and i_{L3} waveforms for $D_1 = 0.3$, $D_2 = 0.2$, $D_3 = 0.5$ for (a) $D_t = 0$, (b) $D_t = 0.5$.

show that the reduction in Δi_{L1}, Δi_{L2} and Δi_{L3} are 66.7%, 69.2% and 76.2%, respectively.

The simulations for the parameters presented in Table 4.13 is presented in Fig. 4.18. The figure shows the waveforms of i_{L1}, i_{L2} and i_{L3} at $D_t = 0$ and $D_t = 0.5$. The waveforms show that the ripples in the inductor current reduces as gate pulses are shifted. The value of $\Delta i_{L1} = 2.0\ A$ at $D_t = 0$ and reduces to $\Delta i_{L1} = 0.5\ A$ as D_t is changed to 0.5. Similarly, Δi_{L2} reduces from 2.8 A to 0.8 A and Δi_{L3} reduces from 3.0 A to 1.0 A. The ripple values show that the reduction in Δi_{L1}, Δi_{L2} and Δi_{L3} are 75.0%, 71.4% and 66.7%, respectively.

The inductor current ripples Δi_{L1}, Δi_{L2} and Δi_{L3} vs. D_t is plotted for two parameters, as D_t varies from 0 to 1. The plots are shown in Fig. 4.19. The plots show that the ripples are reduced as D_t is increased, up to some D_t where ripples are minimum. After that, the ripples again increase, as D_t is increased. This trend is similar to the CI-SIDO boost converter. This analysis is valid for all possible duty ratios, input-output voltages, load currents, and pulse patterns.



(a) (b)

Figure 4.19: Δi_{L1} (blue), Δi_{L2} (pink), Δi_{L3} (green) vs D_t for CI-SITO boost converter.

The reduction percentages of i_{L1}, i_{L2}, and i_{L3} show that the shifting of gate pulse has a significant effect on the inductor current ripples of CI-SITO boost converter. It is observed that the reduction up to 76.2% is obtained without the addition of any extra circuit elements like an inductor, capacitor. The analysis is also very simple to implement.

4.5 Advantages of Sector Formation

As discussed in the previous chapter, we proposed 9 sectors of duty ratios for CI-SIDO converters such that the slope conditions, the minimum inductor current ripple expressions, the shift in gate pulse for the minimum inductor current ripples, and the design of coupled inductors get unified for CI-SIDO buck, boost, and buck-boost. The unified gate pulse shift for minimum inductor current ripples are given by Table 4.7. Further, we propose a unified design of coupled inductor in Sector 5 for the CI-SIDO converters. For a given coupling coefficient k, the unified design of coupled inductors is given by (4.20).

$$k^2 \max\{1, \frac{D_1^2}{(1-D_1)^2}, \frac{(1-D_2)^2}{D_2^2}, \frac{(1-D_1)^2}{D_2^2}, \frac{D_1^2}{(1-D_2)^2}\} < \frac{L_1}{L_2} < \frac{1}{k^2} \min\{1, \frac{D_1^2}{(1-D_1)^2}, \frac{(1-D_2)^2}{D_2^2}, \frac{(1-D_1)^2}{D_2^2}, \frac{D_1^2}{(1-D_2)^2}\} \tag{4.20}$$

The advantages and the proofs of the proposed sectors of duty ratios and the unified coupled inductor design are presented in the subsequent sections.

4.5.1 Unified Gate Pulse Shift for Minimum Inductor Current Ripples

The minimum inductor current ripple expressions of waveforms shown in Fig. 3.3 is presented in (3.5). Corresponding to these ripple expressions of i_{L1} and i_{L2}, the shift in gate pulse is found for i_{L1} and i_{L2}. From Fig. 3.3(a), we observe that ripple expressions of i_{L1} is true when the gate pulse shift is (4.21) which is named as $\mathbf{D}_G$ in Table 4.7.

$$(1 - D_2) \leq D_t \leq D_1. \tag{4.21}$$

Similarly, the ripple expressions of i_{L2} is true when the gate pulse shift is (4.22) which is named as $\mathbf{D}_{NNw}$ in Table 4.7.

$$(D_1 - \overline{D_{NN_w}}) \leq D_t \leq (D_1 - \underline{D_{NN_w}}) \tag{4.22}$$

where

$$\underline{D_{NN_w}} = \frac{Min\{|G_{NF_w}|(1 - D_2), |G_{FN_w}|(1 - D_1)\}}{G_{NN_w}}$$
$$\overline{D_{NN_w}} = \frac{Max\{|G_{NF_w}|(1 - D_2), |G_{FN_w}|(1 - D_1)\}}{G_{NN_w}}$$

The gate pulse shift when both the inductor current ripples are minimum is $\mathbf{D}_G \cap \mathbf{D}_{NNw}$. Similarly, the unified gate pulse shift for minimum inductor current ripples for all the sectors of CI-SIDO converters are presented in Table 4.7.

4.5.2 Unified Design of Coupled Inductors

As discussed earlier, the CI-SIDO boost and buck-boost converter is in sector 5 for $r_{FN2} < D_1 < r_{FN1}$ and $r_{NF2} < D_2 < r_{NF1}$ as shown in Fig. 3.2. Therefore, the range of $\frac{L_1}{L_2}$ for given values of k, D_1, D_2 such that the converter operates in sector 5 of CI-SIDO boost is given by (4.23).

$$k^2 \max\{\frac{(1 - D_2)^2}{D_2^2}, \frac{D_1^2}{(1 - D_1)^2}\} < \frac{L_1}{L_2} < \frac{1}{k^2} \min\{\frac{(1 - D_2)^2}{D_2^2}, \frac{D_1^2}{(1 - D_1)^2}\}. \tag{4.23}$$

The CI-SIDO buck converter forms sector 5 when $k\sqrt{\frac{L_1}{L_2}} < 1$ and $k\sqrt{\frac{L_2}{L_1}} < 1$ as shown in Fig. 3.1. The range of $\frac{L_1}{L_2}$ for given values of k, D_1, D_2 such that the converter operates in sector 5 of CI-SIDO

buck is given by (4.24).

$$k^2 \max\{1, \frac{(1-D_1)^2}{D_2^2}, \frac{D_1^2}{(1-D_2)^2}\} < \frac{L_1}{L_2} < \frac{1}{k^2} \min\{1, \frac{(1-D_1)^2}{D_2^2}, \frac{D_1^2}{(1-D_2)^2}\} \tag{4.24}$$

Therefore, the range of $\frac{L_1}{L_2}$ for given values of k, D_1, D_2 such that the converter operates in sector 5 for all the three CI-SIDO converters is given by (4.20).

The presence of inversely coupled inductors in the CI-SIDO converters reduces the core size of the converter. The two inductor windings of the core are such that the flux due to one winding cancels the flux due to the other winding. So, the coupled inductor windings are designed in the sector where the inductor current ripple is minimum, reducing the flux in the core. Also, the sector where G_{NF1}, G_{NF2} and G_{FN1}, G_{FN2} cancel each other favours the flux cancellation in the core. The sector diagrams and slope conditions of Table 3.2 show that the slopes of i_{L1}, i_{L2} in states NF and FN are opposite only in sector 5. Hence, to reduce the flux in the core, the coupled inductors are designed in Sector 5.

4.5.3 Verification of Unified Design of Coupled Inductors

The unified design of coupled inductor is verified for $D_1 = 0.4$ and $D_2 = 0.6$ with $k = 0.8$. Using (4.20), the range of $\frac{L_1}{L_2}$ obtained is between 0.64 to 0.69. Therefore, we choose $\frac{L_1}{L_2} = 0.65$. The values of coupled inductors used for the experiments are $L_1 = 100\mu H$, $L_2 = 154\mu H$, $k = 0.8$. The coupled inductor is designed using the available E-shaped ferrite core numbered B66387G0000X127 (E65/32/27) and copper wire of 16 SWG. The inductor is designed with an air gap of 0.1 *mm* with the peak inductor current of 10 A. The windings are such that the flux due to one winding cancels the effect of the other in the magnetic core.

The results are presented in Fig. 4.20 for CI-SIDO buck, boost, and buck-boost converters. The details of the experiments are presented in the caption of the figures. All the results of Fig. 4.20 show that the converters are operating in Sector 5. Therefore, a unified waveform of inductor currents, unified minimum inductor current ripple expressions, and unified shift in gate pulse for minimum inductor current ripples are obtained for all the three CI-SIDO converters. The experimental parameters of each experiment are presented in Table. 3.4.

We have proposed a unified design of coupled inductor in Sector 5 for the CI-SIDO converters.

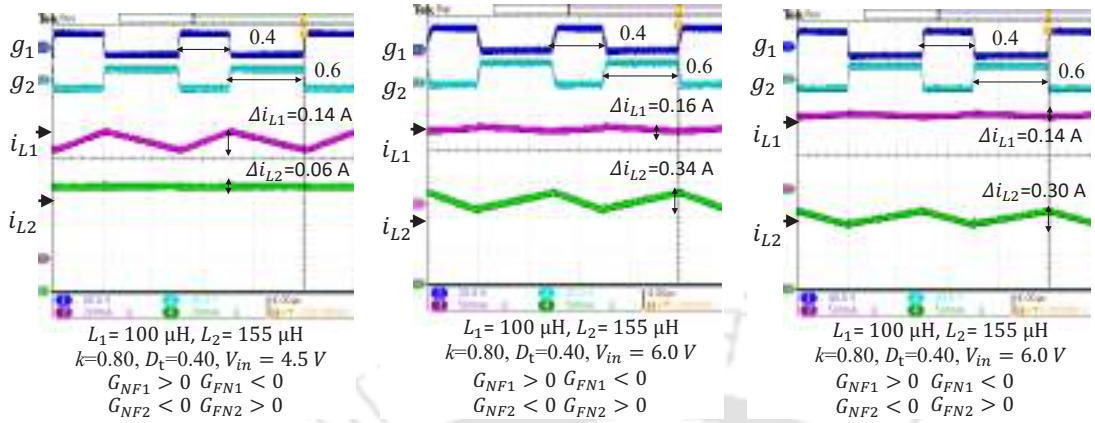


Figure 4.20: Experimental results of CI-SIDO (a) buck, (b) boost, and (c) buck-boost converters in sector 5 with same coupled inductors.

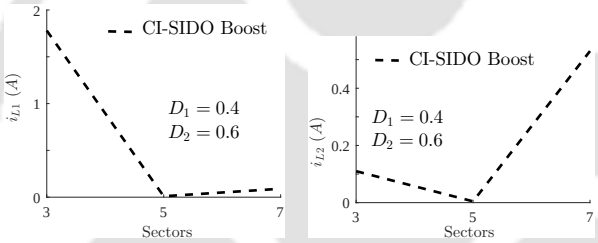


Figure 4.21: Inductor current ripple versus sector plot for CI-SIDO boost converter with $D_1 = 0.4$ and $D_2 = 0.6$.

For any duty ratios, we can obtain minimum inductor current ripples if we ensure that the CI-SIDO converter operates in Sector 5. To prove that, the inductor current ripples versus sectors graphs are plotted for CI-SIDO boost converter in Fig. 4.21. It is to be noted that D_1 and D_2 cannot be placed in all the sectors, as it depends on $D_1 + D_2$ as presented in Table 4.7. For Fig. 4.20 with $D_1 = 0.4$ and $D_2 = 0.6$, where $D_1 + D_2 = 1$, only sector 3, 5, 7 are possible. To place $D_1 = 0.4$ and $D_2 = 0.6$ in Sector 3, the coupled inductor parameters with $k = 0.8$ and $\frac{L_1}{L_2} = 0.25$ is selected. Similarly, other sectors are generated by changing coupled inductor parameters.

From Fig. 4.21, we can observe that lowest Δi_{L1} and Δi_{L2} are obtained in Sector 5. For $D_1 = 0.4$ and $D_2 = 0.6$, the lowest Δi_{L1} is obtained for $L_1 = 100\ \mu H$, $L_2 = 155\ \mu H$, $k = 0.80$ and the lowest Δi_{L2} is obtained for $L_1 = 100\ \mu H$, $L_2 = 440\ \mu H$, $k = 0.70$. Similarly, it can be shown for CI-SIDO buck and CI-SIDO buck-boost.

4.6 Summary of the Chapter

The findings of the chapter is as follows–

(i) The gate pulse shift for minimum inductor ripples is found for all the feasible cases of CI-SIDO boost converter. The obtained gate pulse shifts are verified experimentally and in Matlab Simulations.

(ii) The gate pulse shift for minimum inductor ripples of CI-SIDO boost converter is extended to CI-SIDO buck, CI-SIDO buck-boost converters. It is found that $\mathbf{D}_{min}$ is equally applicable to all the three converters.

(iii) The effect of gate pulse is also extended to CI-SITO boost converters. It is found that the shift in gate pulse also reduces the inductor current ripples of CI-SITO boost.

(iv) The advantages of sector formations are also extended here. The unified gate pulse shift is found where both the inductor current ripples are minimized for all three CI-SIDO converters.

(v) It is also found that the inductor current ripples are minimized in Sector 5 for all three CI-SIDO converters. A unified design of coupled inductors are proposed to operate in Sector 5 such that the inductor current ripples are reduced.

5

Input Current Ripple Minimization in CI-SIDO Boost Converter by Design of Coupled Inductor

Contents

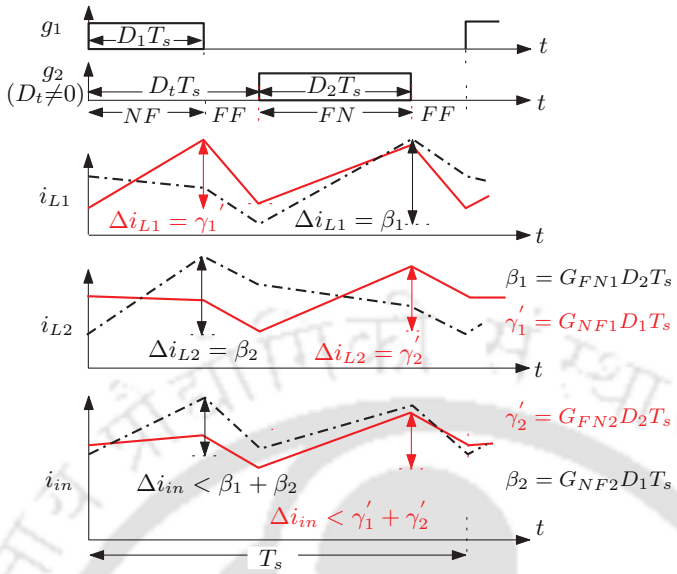


Figure 5.1: Effect of change in $\frac{L_1}{L_2}$ on Δi_{L1}, Δi_{L2} and Δi_{in}. N and F denotes ON and OFF of switches S_{t1} and S_{t2}, respectively.

5.1 Introduction

[1] The input current in the CI-SIDO boost converter is the sum of inductor currents. The reduced inductor current ripples do not ensure reduced input current ripples. A separate analysis is required to reduce the input current ripples. The maximum ripple cancellations are introduced to reduce the ripples in input current by shifting gate pulses. In addition to the shifting of gate pulses, the maximum ripple cancellation in the CI-SIDO boost converter depends on the design of coupled inductors. This chapter analyses the input current ripples of CI-SIDO boost converters in detail. The effect of gate pulse shift on the input current ripples is found, and the design of coupled inductors is proposed. In Fig. 5.1, i_{L1}, i_{L2} and i_{in} of CI-SIDO boost converters are shown which shows the effect of changing coupled inductor parameters on input current ripple, Δi_{in}. The waveforms are drawn for $D_t = \mathbf{D}_{min}$ as obtained from Table 5.2 where ripples in i_{L1}, i_{L2} and i_{in} are minimum.

In converters such as interleaved boost converters, the maximum ripple cancellations are introduced to reduce the ripples in input current by shifting gate pulses. However, from Fig. 5.1, it is

[1]Major part of this chapter is reproduced from my publications: (i) Nupur and S. Nath, "Maximizing Ripple Cancellation in Input Current for SIDO Boost Converter by Design of Coupled Inductors" *IEEE J. Emerg. Sel. Topics in Ind. Electron.*, vol. 2, no. 4, pp. 409–419, Oct. 2021. (ii) Nupur and S. Nath, "Input Current Ripple Minimization in Coupled SIDO Boost Converter by Shift of Gate Pulses," in *Proc. 12th Energy Convers. Congr. Expo. Asia*, May 2021, pp. 1660-1665. (iii) Nupur and S. Nath, "Achieving Approximately Zero Ripples in Input Current of Coupled SIDO Boost Converter," in *IEEE Trans. Ind. Appl.*, vol. 58, no. 3, pp. 3819-3829, May-Jun. 2022.

found that the problem of maximizing ripple cancellation in CI-SIDO boost is more challenging than interleaved boost. Some of the challenges are presented as follows-

- In CI-SIDO boost $D_1 \neq D_2$, $L_1 \neq L_2$ resulting in different slopes of i_{L1}, i_{L2}. So, numerous patterns of waveforms for i_{L1}, i_{L2} and i_{in} are possible. The shift at which Δi_{in} is minimum (called $\mathbf{D}_{min}$) depends on values of D_1, D_2, L_1/L_2, k. Whereas in interleaved boost $D_1 = D_2 = D$, $L_1 = L_2 = L$ resulting in equal slopes of i_{L1}, i_{L2}. So, limited number of waveforms patterns are possible. Here, $\mathbf{D}_{min}$ is a fixed value i.e. $\mathbf{D}_{min} = 1/n$.

- In CI-SIDO boost, slope cancellations do not always occur at all possible values of D_1, D_2, L_1/L_2, k. The slope cancellations do not always lead to ripple cancellation. Whereas in interleaved boost, slope cancellations always occur at $D_t = \mathbf{D}_{min}$. Also, the slope cancellations always lead to ripple cancellation.

- In CI-SIDO boost, $\Delta i_{in} =$ or $< \Delta i_{L1} + \Delta i_{L2}$. So, to minimize Δi_{in}, Δi_{L1}, Δi_{L2} need to be analyzed and minimized first. Also, Δi_{in} depends on choice of D_1, D_2, L_1/L_2, k, $\mathbf{D}_{min}$. The condition of maximum ripple cancellation is not present in the existing literature. However, in interleaved boost, $\Delta i_{in} < \Delta i_{L1} + \Delta i_{L2}$ always. The maximum ripple cancellation occurs at $\mathbf{D}_{min}$.

The input current i_{in} is the sum of inductor currents i_{L1}, i_{L2}, as seen in Fig. 1.4(b). The slopes of input current in each state is the sum of slopes of inductor currents in the corresponding states. In Fig. 5.1, i_{L1}, i_{L2} and i_{in} are shown for $\mathbf{D}_{min}T_s$ shifting between g_1 and g_2 (red solid lines), for $D_1 + D_2 < 1$ and $D_1 < D_2$. For $D_t \neq 0$ (D_t chosen as $D_1 < D_t < 1$), the converter goes through $NF \rightarrow FF \rightarrow FN \rightarrow FF$. Also, for same D_1, D_2 and D_t with same sequence of states, the pattern of i_{L1}, i_{L2} and i_{in} changes as $\frac{L_1}{L_2}$ changes (shown in black dashed-dotted lines of Fig. 5.1). We note the following from Fig. 5.1 that for same D_1, D_2, D_t and same sequence of states, as $\frac{L_1}{L_2}$ is changed the pattern of Δi_{in} changes along with the patterns of Δi_{L1} and Δi_{L2}. Therefore, the problem of maximizing ripple cancellation in i_{in} is solved by analyzing the patterns of i_{in}, and finding the patterns of i_{L1}, i_{L2} and ranges of L_1, L_2, k where maximum ripple cancellation between i_{L1} and i_{L2} takes place.

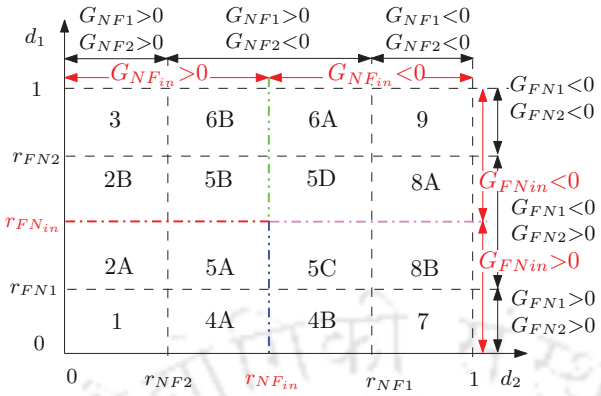


Figure 5.2: Sectors and sub-sectors of CI-SIDO boost converter.

5.2 Gate Pulse Shift for Minimum Input Current Ripples

The objective of this section is to find the ranges of D_t and so, the pattern of input current waveforms i_{in} where Δi_{in} are minimum, for all possible values of L_1, L_2, k. The range of D_t where Δi_{in} are minimum ($\underline{\Delta i_{in}}$) is denoted by $\mathbf{D}_{min}$.

5.2.1 Sectors and Sub-sectors

The expressions for slopes of i_{L1} and i_{L2} in all four states are shown in Table 2.2. The slopes of the input current in each of the four states are the sum of slopes of inductor currents in the corresponding states. The formulated slopes of input currents are presented in (5.1). It is found that the slopes of i_{in}, i_{L1} and i_{L2} are different in all four states. It is also found that for all duty ratios $G_{NNw} > 0$ and $G_{FFw} < 0$. Also, G_{NFw}, G_{FNw} can be >, < or = 0, depending on the values of k, L_1, L_2, V_{o1}, V_{o2}, V_{in}.

$$G_{NN_{in}} = \frac{1}{(1-k^2)L_1L_2}\left[V_{in}\left(L_1+L_2+2k\sqrt{L_1L_2}\right)\right] \tag{5.1a}$$

$$G_{FF_{in}} = \frac{1}{(1-k^2)L_1L_2}\left[\ V_{in}\left(L_1+L_2+2k\sqrt{L_1L_2}\right) - V_{o1}\left(L_2+k\sqrt{L_1L_2}\right) - V_{o2}\left(L_1+k\sqrt{L_1L_2}\right)\ \right] \tag{5.1b}$$

$$G_{NF_{in}} = \frac{1}{(1-k^2)L_1L_2}\left[\ V_{in}\left(L_1+L_2+2k\sqrt{L_1L_2}\right) - V_{o2}\left(L_1+k\sqrt{L_1L_2}\right)\ \right] \tag{5.1c}$$

$$G_{FN_{in}} = \frac{1}{(1-k^2)L_1L_2}\left[\ V_{in}\left(L_1+L_2+2k\sqrt{L_1L_2}\right) - V_{o1}\left(L_2+k\sqrt{L_1L_2}\right)\ \right] \tag{5.1d}$$

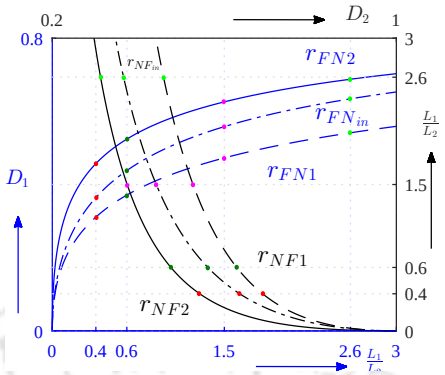


Figure 5.3: The plot of r_{NF1}, $r_{NF_{in}}$, r_{NF2}, r_{FN1}, $r_{FN_{in}}$ and r_{FN2} with respect to $\frac{L_1}{L_2}$.

For $G_{NF_{in}}$, G_{NF1}, G_{NF2} and $G_{FN_{in}}$, G_{FN1}, G_{FN2} to be greater than zero, D_2 should be smaller than $r_{NF_{in}}$, r_{NF1}, r_{NF2}, and D_1 should be smaller than $r_{FN_{in}}$, r_{FN1}, r_{FN2}, respectively, where

$$r_{NF2} = \frac{k\sqrt{\frac{L_2}{L_1}}}{\left(1 + k\sqrt{\frac{L_2}{L_1}}\right)}, \tag{5.2a}$$

$$r_{FN_{in}} = \frac{\left(\frac{L_1}{L_2} + k\sqrt{\frac{L_1}{L_2}}\right)}{\left(\frac{L_1}{L_2} + 2k\sqrt{\frac{L_1}{L_2}} + 1\right)}, \tag{5.2b}$$

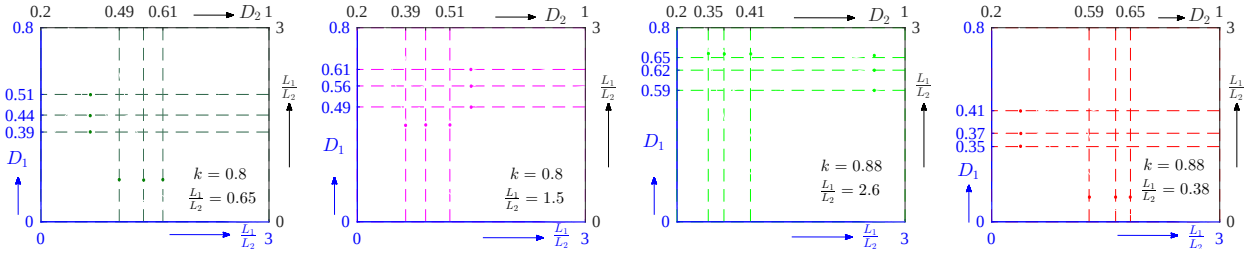
$$r_{FN1} = \frac{k\sqrt{\frac{L_1}{L_2}}}{\left(1 + k\sqrt{\frac{L_1}{L_2}}\right)}, \tag{5.2c}$$

$$r_{FN2} = \frac{1}{\left(1 + k\sqrt{\frac{L_2}{L_1}}\right)}, \tag{5.2d}$$

$$r_{NF_{in}} = \frac{\left(\frac{L_2}{L_1} + k\sqrt{\frac{L_2}{L_1}}\right)}{\left(\frac{L_2}{L_1} + 2k\sqrt{\frac{L_2}{L_1}} + 1\right)}, \tag{5.2e}$$

$$r_{NF1} = \frac{1}{\left(1 + k\sqrt{\frac{L_1}{L_2}}\right)}. \tag{5.2f}$$

It can be shown that $r_{NF2} < r_{NF_{in}} < r_{NF1}$ and $r_{FN1} < r_{FN_{in}} < r_{FN2}$. So, based on the conditions obtained, $[d_1, d_2]$ is divided into 16 distinct sectors as shown in Fig. 5.2. $[d_1, d_2]$ denote the range of all values from 0 to 1 that duty ratios D_1, D_2 can take. It is found that the sectors 2, 4, 5, 6, and 8 get divided into two sub-sectors due to the input current slopes, whereas sector 5 gets divided into four sub-sectors. In each sector, the slopes $G_{NF_{in}}$, G_{NF1}, G_{NF2}, $G_{FN_{in}}$, G_{FN1}, and G_{FN2} are different. So, the



(a) (b) (c) (d)

Figure 5.4: Sector formation for different values of $\frac{L_1}{L_2}$ and k: (a) $k = 0.8$ and $\frac{L_1}{L_2} = 0.65$, (b) $k = 0.8$ and $\frac{L_1}{L_2} = 1.5$, (c) $k = 0.88$ and $\frac{L_1}{L_2} = 2.6$, (d) $k = 0.88$ and $\frac{L_1}{L_2} = 0.38$.

patterns of currents are different for different sectors. Also, in any given sector, the patterns become different based on value of shift D_t and whether $D_1 + D_2 < 1$ or > 1 or $= 1$. The ripples obtained by varying D_t from 0 to 1 for all conditions of $D_1 + D_2$ in each sector, are compared and $\mathbf{D}_{min}$ are formulated. The detailed analysis is presented in Appendix B.

The expressions of r_{NF1}, $r_{NF_{in}}$, r_{NF2}, r_{FN1}, $r_{FN_{in}}$ and r_{FN2} are presented in (5.2). For given value of k, each expression is plotted with respect to $\frac{L_1}{L_2}$, as shown in Fig. 5.3. The plots show the effect of changing $\frac{L_1}{L_2}$ on the expressions. The figure shows D_1 vs $\frac{L_1}{L_2}$ (in blue) for r_{FN1}, $r_{FN_{in}}$ and r_{FN2}, and D_2 vs $\frac{L_1}{L_2}$ (in black) for r_{NF1}, $r_{NF_{in}}$ and r_{NF2}. The effect of changing $\frac{L_1}{L_2}$ on the sector dimensions can be observed from the plot. For example, for $k = 0.8$ and $\frac{L_1}{L_2} = 0.65$, a dot (dark green) is plotted at the intersection of $\frac{L_1}{L_2} = 0.65$ and plots of r_{NF1}, $r_{NF_{in}}$, r_{NF2}, r_{FN1}, $r_{FN_{in}}$ and r_{FN2}. Through each dot (dark green), lines are drawn to form the sector diagram, as shown in Fig. 5.4(a). Similarly, the sector formations are shown for $k = 0.8$ and $\frac{L_1}{L_2} = 1.5$ (pink), $k = 0.88$ and $\frac{L_1}{L_2} = 2.6$ (light green), and $k = 0.88$ and $\frac{L_1}{L_2} = 0.38$ (red) in Figs. 5.4(b), 5.4(c) and 5.4(d), respectively. It is observed that as the ratios of L_1, L_2 and k change, the dimension of sectors change.

5.2.2 Calculating Gate Pulse Shift for Minimum Input Current Ripples

As the patterns of i_{in}, i_{L1}, i_{L2} are different for each sector, the effect of gate pulse shift is different for each sector. For all possible slopes conditions, the gate pulse g_2 is shifted by D_t from the starting point of g_1 where D_t varies from 0 to 1. As D_t varies, the states of the converter changes which results in changed waveforms of i_{in}, i_{L1}, i_{L2}. Consequently, the ripples expressions at each D_t is different. The minimum Δi_{in} is obtained by comparing Δi_{in} at each D_t. This is explained here by taking an example

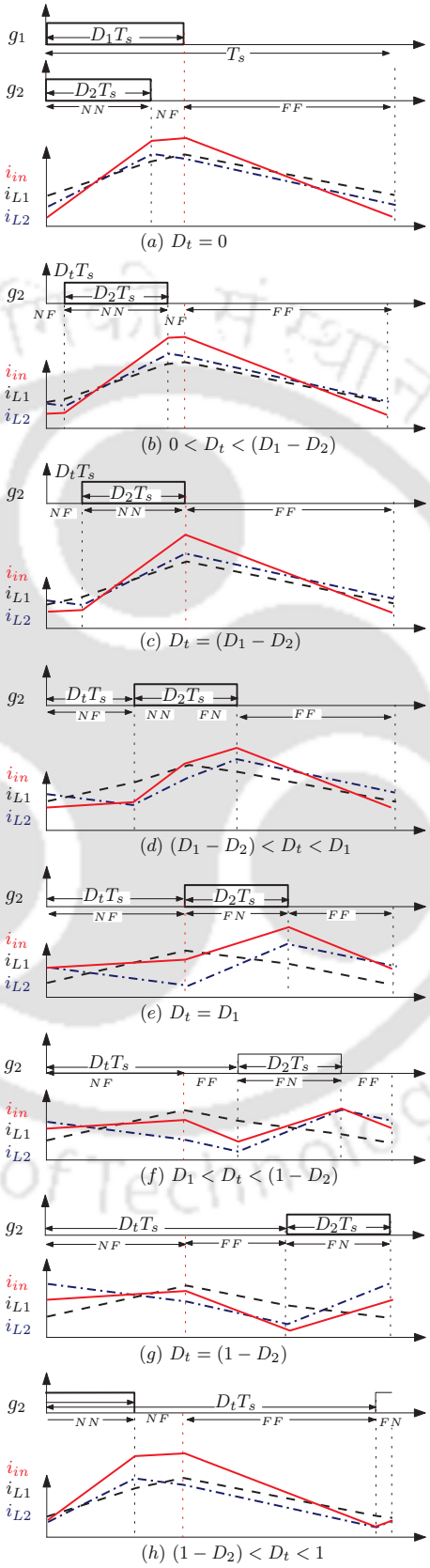


Figure 5.5: The patterns of i_{L1} (black dashed), i_{L2} (blue dash-dot) and i_{in} (red solid) in sector 5A as D_t varies from 0 to 1.

Table 5.1: Sector 5A for $D_1 + D_2 < 1$ and $D_1 > D_2$

Fig. No.	Δi_{L1} ($G_{NF1} > 0, G_{FN1} < 0$)	Δi_{L2} ($G_{NF2} < 0, G_{FN2} > 0$)	Δi_{in} ($G_{NFin} > 0, G_{FNin} > 0$)	D_t
2(a)	α_{11}	ϵ_{12}	α_{1in}	0
2(b)	α_{11}	ϵ_{12}	α_{1in}	$0 < D_t < (D_1 - D_2)$
2(c)	α_{11}	ϵ_{12}	α_{1in}	$(D_1 - D_2)$
2(d)	$\alpha_{11} > \Delta i_{L1} > \rho_{11}$	$\epsilon_{12} > \Delta i_{L2} > \tau_{12}$	$\alpha_{1in} > \Delta i_{in} > \beta_{1in}$	$(D_1 - D_2) < D_t < D_1$
2(e)	ρ_{11}	τ_{12}	β_{1in}	D_1
2(f)	ρ_{11}	τ_{12}	$\beta_{1in} > \Delta i_{in} > \gamma_{1in}$	$D_1 < D_t < (D_1 + \underline{D_{PPin}})$
	ρ_{11}	τ_{12}	γ_{1in}	$(D_1 + \underline{D_{PPin}}) \leq D_t \leq (D_1 + \overline{D_{PPin}})$
	ρ_{11}	τ_{12}	$\gamma_{1in} < \Delta i_{in} < \beta_{1in}$	$(D_1 + \overline{D_{PPin}}) < D_t < (1 - D_2)$
2(g)	ρ_{11}	τ_{12}	β_{1in}	$(1 - D_2)$
2(h)	$\rho_{11} < \Delta i_{L1} < \alpha_{11}$	$\tau_{12} < \Delta i_{L2} < \alpha_{12}$	$\beta_{1in} < \Delta i_{in} < \alpha_{1in}$	$(1 - D_2) < D_t < 1$

$\alpha_{11} \equiv G_{NN1}D_2T_s + G_{NF1}(D_1 - D_2)T_s$, $\epsilon_{12} \equiv G_{NN2}D_2T_s$, $\alpha_{1in} \equiv G_{NNin}D_2T_s + G_{NFin}(D_1 - D_2)T_s$
$\rho_{11} \equiv G_{NF1}D_1T_s$, $\tau_{12} \equiv G_{FN2}D_2T_s$, $\beta_{1in} \equiv G_{NFin}D_1T_s + G_{FNin}D_2T_s$
$\gamma_{1in} \equiv Max\{G_{NFin}D_1T_s, G_{FNin}D_2T_s\}$

for $D_1 > D_2$, $D_1 + D_2 < 1$ such that the converter operates in Sector 5A.

The waveforms of i_{L1}, i_{L2} and i_{in} as D_t is varied from 0 to 1, for sector 5A is shown in Fig. 5.5 for $D_1 > D_2$, $D_1 + D_2 < 1$. As presented in Fig. 5.2, the slope conditions in Sector 5A are $G_{NNin} > 0$, $G_{FFin} < 0$, $G_{NFin} > 0$, $G_{FNin} > 0$, $G_{NN1} > 0$, $G_{FF1} < 0$, $G_{NF1} > 0$, $G_{FN1} < 0$, $G_{NN2} > 0$, $G_{FF2} < 0$, $G_{NF2} < 0$, $G_{FN2} > 0$. Now, for $D_t = 0$, the states of the converter are $NN \rightarrow NF \rightarrow FF$ with their respective durations as $D_2T_s \rightarrow (D_1 - D_2)T_s \rightarrow (1 - D_1)T_s$. The ripple expressions are given by–

$$\Delta i_{in} = G_{NNin}D_2T_s + G_{NFin}(D_1 - D_2)T_s, \tag{5.3a}$$

$$\Delta i_{L1} = G_{NN1}D_2T_s + G_{NF1}(D_1 - D_2)T_s, \tag{5.3b}$$

$$\Delta i_{L2} = G_{NN2}D_2T_s \tag{5.3c}$$

For $0 < D_t < (D_1 - D_2)$, the states of the converter are $NF \rightarrow NN \rightarrow NF \rightarrow FF$ with their durations as $D_tT_s \rightarrow D_2T_s \rightarrow (D_1 - D_t - D_2)T_s \rightarrow (1 - D_1)T_s$ and the ripple expressions as (5.3). Again, if $D_t = (D_1 - D_2)$ the ripples expression is given by (5.3) with the changed states as $NF \rightarrow NN \rightarrow FF$ and changed durations as $D_tT_s \rightarrow (D_1 - D_t)T_s \rightarrow (1 - D_1)T_s$. Similarly, D_t is varied upto 1 as shown in Fig. 5.5 and Δi_{L1}, Δi_{L2}, Δi_{in} is found. Each ripple expressions are presented in Table 5.1 and compared to find the minimum Δi_{L1}, Δi_{L2}, Δi_{in}. The rows of Table 5.1 represent the figure number as gate pulse is shifted from 0 to 1 and the columns represent the current ripples. This table is added to find the current ripple expressions at each shift and to find the minimum ripples by comparisons

Table 5.2: $\mathbf{D}_{min}$ for minimum input current

Sector No.	$(D_1 + D_2)$	$\mathbf{D}_{min}$
1	< 1	$\mathbf{D}_{PP_{in}}$
2A 2B	< 1	$\mathbf{D}_{PP_{in}}$ $\mathbf{D}_L$
3	< 1 > 1 $= 1$	$\mathbf{D}_L$ $\mathbf{D}_G$ D_1
4A 4B	< 1	$\mathbf{D}_{PP_{in}}$ $\mathbf{D}_L$
5A	< 1	$\mathbf{D}_{PP_{in}}$
5B, 5C	< 1 > 1 $= 1$	$\mathbf{D}_L$ $\mathbf{D}_G$ D_1
5D	> 1	$\mathbf{D}_{NN_{in}}$
6A 6B	> 1	$\mathbf{D}_{NN_{in}}$ $\mathbf{D}_G$
7	< 1 > 1 $= 1$	$\mathbf{D}_L$ $\mathbf{D}_G$ D_1
8A 8B	> 1	$\mathbf{D}_{NN_{in}}$ $\mathbf{D}_G$
9	> 1	$\mathbf{D}_{NN_{in}}$

where, $\mathbf{D}_L = \{D_t \mid D_1 \le D_t \le (1 - D_2)\}$

$\mathbf{D}_G = \{D_t \mid (1 - D_2) \le D_t \le D_1\}$

$\mathbf{D}_{NNw} = \{D_t \mid (D_1 - \overline{D_{NN_w}}) \le D_t \le (D_1 - \underline{D_{NN_w}})\}$

$\overline{D_{NN_w}} = \max\{|G_{NF_w}|(1 - D_2), |G_{FN_w}|(1 - D_1)\}/G_{NN_w}$

$\underline{D_{NN_w}} = \min\{|G_{NF_w}|(1 - D_2), |G_{FN_w}|(1 - D_1)\}/G_{NN_w}$

$\mathbf{D}_{PPw} = \{D_t \mid (D_1 + \underline{D_{PP_w}}) \le D_t \le (D_1 + \overline{D_{PP_w}})$

$\overline{D_{PP_w}} = \max\{G_{NF_w}D_1, G_{FN_w}D_2\}/|G_{FF_w}|$

$\underline{D_{PP_w}} = \min\{G_{NF_w}D_1, G_{FN_w}D_2\}/|G_{FF_w}|$

for sector 5A. The comparisons show that Δi_{in} is minimum for $(D_1 + \underline{D_{PPin}}) \le D_t \le (D_1 + \overline{D_{PPin}})$ where $\underline{D_{PPin}}$ and $\overline{D_{PPin}}$ are shown in Table 5.1 (also marked in red color). The results in Table 5.1 show that Δi_{L1}, Δi_{L2} are minimum for $D_1 < D_t < (1 - D_2)$, however, the range of D_t where Δi_{in} is minimum has reduced to $(D_1 + \underline{D_{PPin}}) \le D_t \le (D_1 + \overline{D_{PPin}})$. Therefore, $\mathbf{D}_{min}$ for $\underline{\Delta i_{in}}$ for Sector 5A is $(D_1 + \underline{D_{PPin}}) \le D_t \le (D_1 + \overline{D_{PPin}})$ as presented in Table 5.2. The rows of Table 5.2 represent all 16 sectors and columns represent the values of $\mathbf{D}_{min}$ for $\underline{\Delta i_{in}}$ for all possible values of $D_1 + D_2$.

Similarly, this analysis is done for all 16 sectors of CI-SIDO boost converters by drawing figures and tables similar to Fig. 5.5 and Table 5.1, respectively, in Appendix B. The obtained $\mathbf{D}_{min}$ for all the 16 sectors are given in Table 5.2.

Table 5.3: Simulation Parameters

V_{in}	8 V	L_1, L_2	131.24, 94.61 μH	k =	0.73	R_1, R_2	8, 12 Ω

Table 5.4: Comparison of Analytical, Simulation and Experimental $\mathbf{D}_{min}$ and % Reduction in Δi_{in}

Fig. No.	$\mathbf{D}_{min}$			Reduction (%)
	Analytical	Simulation	Experiment	Δi_{in}
5.6(a)	0.46-0.54	0.46-0.54	0.46-0.54	64.19
5.6(b)	0.59-0.71	0.59-0.71	0.59-0.71	46.39
5.6(c)	0.62-0.68	0.62-0.68	0.62-0.68	64.15
5.6(d)	0.7-0.8	0.7-0.8	0.7-0.8	38.20
5.6(e)	0.43-0.47	0.43-0.47	0.43-0.47	57.88
5.6(f)	0.33-0.47	0.33-0.47	0.33-0.47	52.37
5.6(g)	0.54-0.55	0.54-0.55	0.54-0.55	89.22
5.6(h)	0.6	0.6	0.6	87.34
5.6(i)	0.5	0.5	0.5	90.57
5.6(j)	0.54-0.55	0.54-0.55	0.54-0.55	89.43
5.6(k)	0.58-0.62	0.58-0.62	0.58-0.62	69.43
5.6(l)	0.62-0.68	0.62-0.68	0.62-0.68	64.15
5.6(m)	0.3	0.3	0.3	43.99
5.6(n)	0.46-0.54	0.46-0.54	0.46-0.54	75.48
5.6(o)	0.34-0.46	0.34-0.46	0.34-0.46	52.37
5.6(p)	0.54-0.55	0.54-0.55	0.54-0.55	72.29

5.2.3 Gate Pulse Shift for Minimum Inductors and Input Currents Together

$\mathbf{D}_{PP1}$, $\mathbf{D}_{PP2}$ and $\mathbf{D}_{PP_{in}}$ are the sub-ranges of sequence C-II (shown in Fig. 5.5). In C-II the duration of state FF has fixed duration, $(1 - D_1 - D_2)T_s$. So, $\underline{D_{PP_w}} + \overline{D_{PP_w}} = (1 - D_1 - D_2)$. Therefore, it can be concluded that

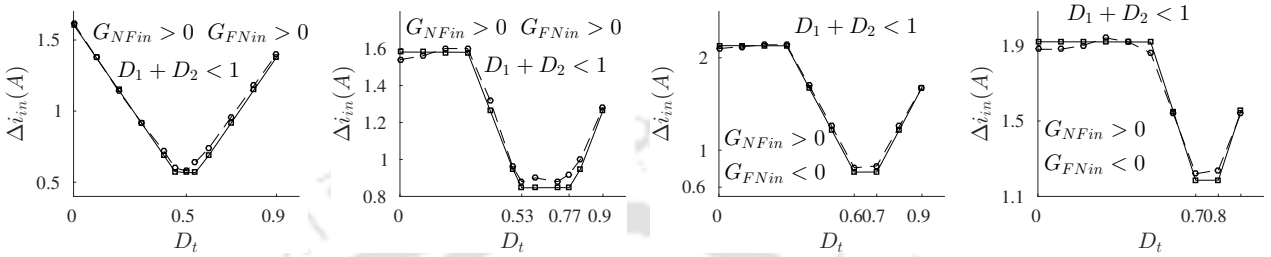
$$\text{If } \underline{D_{PP1}} < \underline{D_{PP2}} < \underline{D_{PP_{in}}} \text{ then } \overline{D_{PP1}} > \overline{D_{PP2}} > \overline{D_{PP_{in}}} \implies \mathbf{D}_{PP_{in}} \subset \mathbf{D}_{PP2} \subset \mathbf{D}_{PP1} \tag{5.4a}$$

$$\text{If } \underline{D_{PP1}} > \underline{D_{PP2}} > \underline{D_{PP_{in}}} \text{ then } \overline{D_{PP1}} < \overline{D_{PP2}} < \overline{D_{PP_{in}}} \implies \mathbf{D}_{PP1} \subset \mathbf{D}_{PP2} \subset \mathbf{D}_{PP_{in}} \tag{5.4b}$$

Similarly, various other combination of $\mathbf{D}_{PP1}$, $\mathbf{D}_{PP2}$ and $\mathbf{D}_{PP_{in}}$ are also valid. So, the intersections are always valid. Similar proof also shows that intersection of $\mathbf{D}_{NN1}$, $\mathbf{D}_{NN2}$ and $\mathbf{D}_{NN_{in}}$ are always possible.

5.2.4 Simulation and Experimental Results

The experimental prototype of 100 W CI-SIDO boost converter is developed using the parameters as shown in Table 5.3. To experimentally verify $\mathbf{D}_{min}$ obtained in Table 5.2, a coupled inductor is

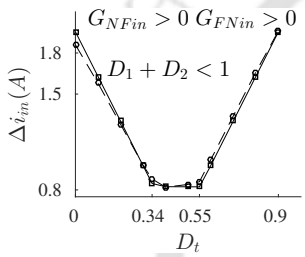


(a) D_1=0.3, D_2=0.3

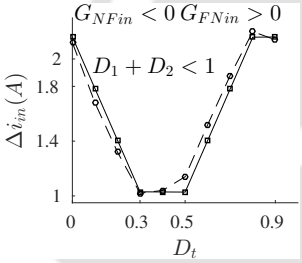
(b) D_1=0.5, D_2=0.2

(c) D_1=0.6, D_2=0.3

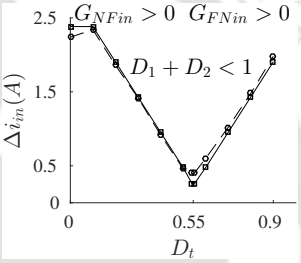
(d) D_1=0.7, D_2=0.2



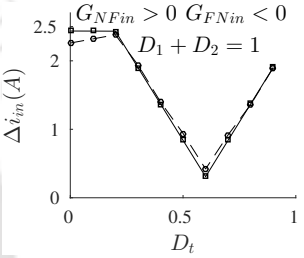
(e) D_1=0.3, D_2=0.4



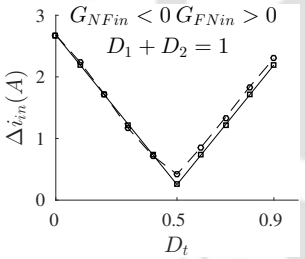
(f) D_1=0.3, D_2=0.5



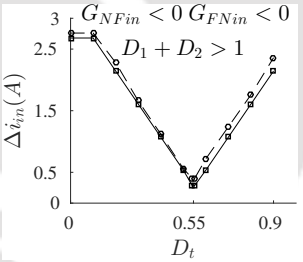
(g) D_1=0.5, D_2=0.4



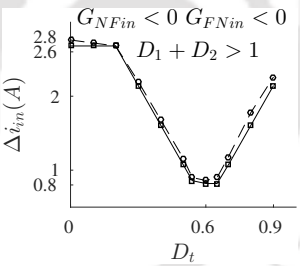
(h) D_1=0.6, D_2=0.4



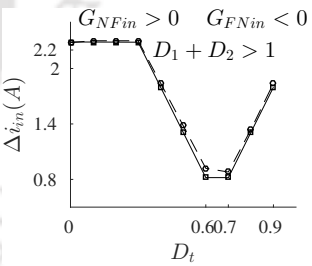
(i) D_1=0.5, D_2=0.5



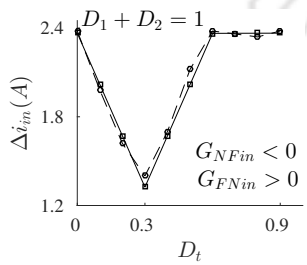
(j) D_1=0.6, D_2=0.5



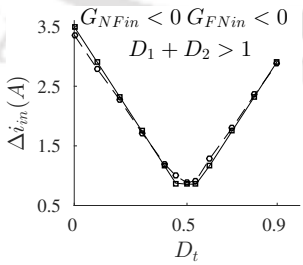
(k) D_1=0.7, D_2=0.5



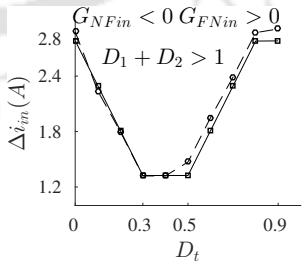
(l) D_1=0.7, D_2=0.4



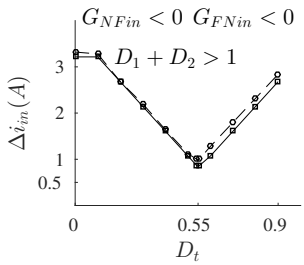
(m) D_1=0.3, D_2=0.7



(n) D_1=0.6, D_2=0.6



(o) D_1=0.5, D_2=0.7



(p) D_1=0.7, D_2=0.6

Figure 5.6: Plots of measured Δi_{in} vs D_t using simulation (square) and experimental (circle) data for sector no. : (a) 1 (b) 2A (c) 2B (d) 3 (e) 4A (f) 4B (g) 5A (h) 5B (i) 5C (j) 5D (k) 6A (l) 6B (m) 7 (n) 8A (o) 8B (p) 9.

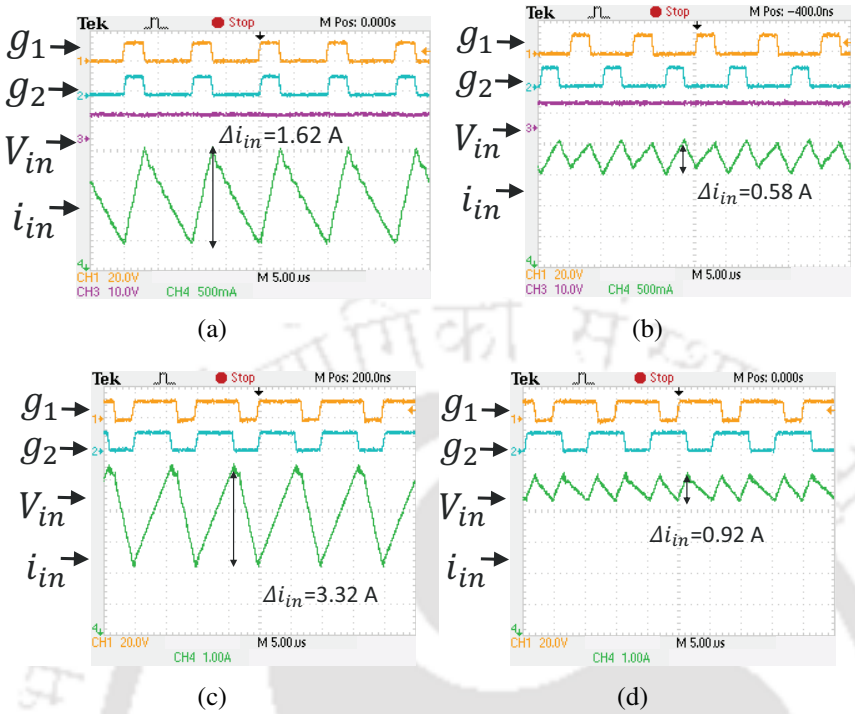
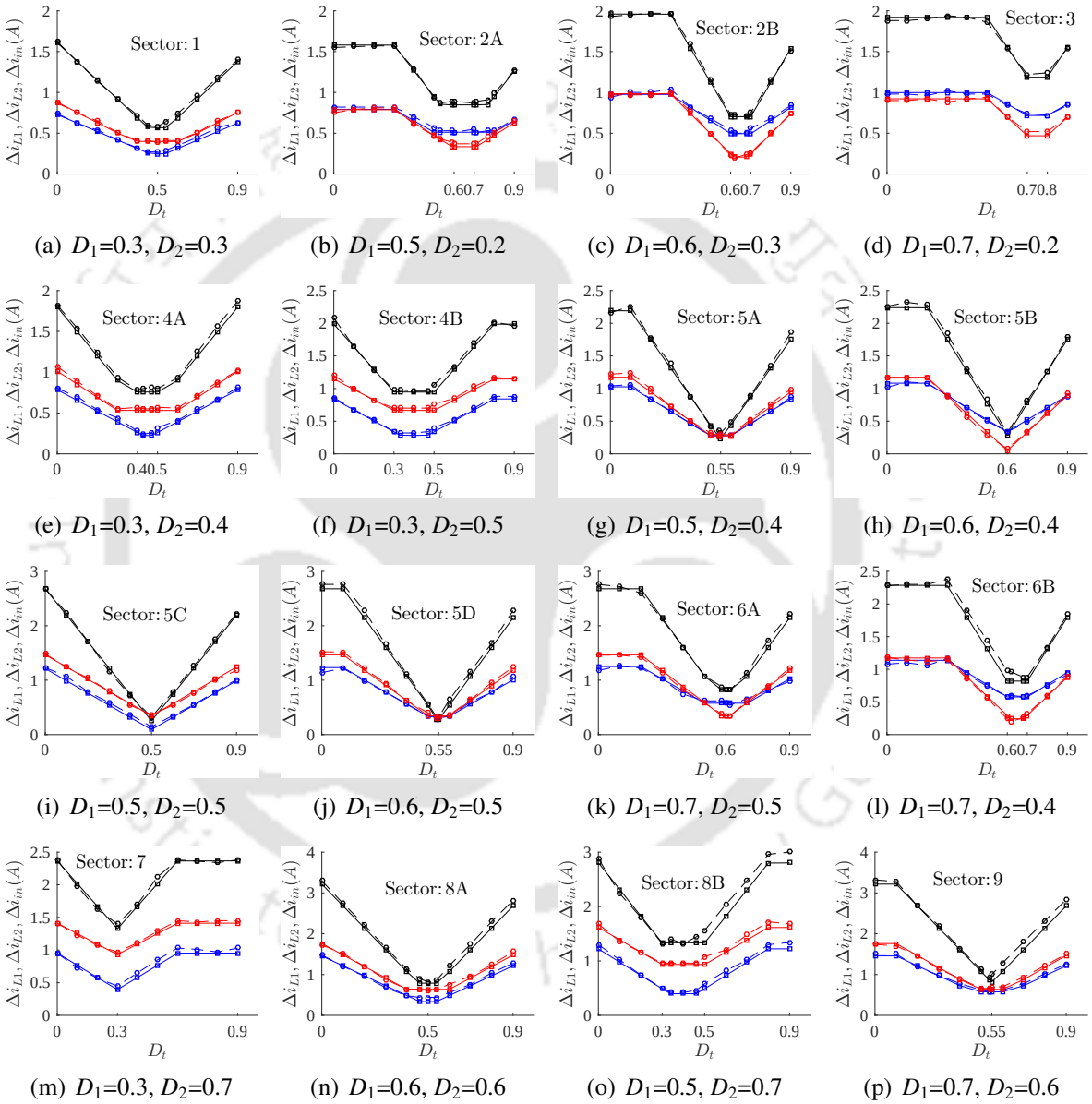


Figure 5.7: Experimental waveforms of i_{in} for $D_1 = D_2 = 0.3$ in Sector 1 at (a) $D_t = 0$, (b) $D_t = 0.5$, and for $D_1 = 0.7$, $D_2 = 0.6$ in Sector 9 at (c) $D_t = 0$, (d) $D_t = 0.55$.

selected i.e. $L_1 = 131.24\mu H$, $L_2 = 94.61\mu H$, $k = 0.73$. The values of r_{NF2}, r_{NFin}, r_{NF1}, r_{FN1}, r_{FNin}, r_{FN2} are calculated as 0.3826, 0.4529, 0.5377, 0.4623, 0.5471 and 0.6174 respectively. Then different sectors are generated by changing the duty ratios. The value of $\mathbf{D}_{min}$ is verified by calculating Δi_{in} at each D_t varying from 0 to 1, and then comparing the ripple for each D_t. The values of $\mathbf{D}_{min}$ is also verified by simulation, with the same parameters, in MATLAB/Simulink. The plots of Δi_{in} vs D_t is shown in Fig. 5.6 for all the 16 sectors of CI-SIDO boost converter. The slight mismatch of simulation and experimental values are due to the load inductances and fluctuations in input DC voltage.

The comparison of $\mathbf{D}_{min}$ obtained by analytical expression of Table 5.2, by simulation in MATLAB/ Simulink, by experimental prototype are compared in Table 5.4. The percentage reduction in Δi_{in} is obtained with respect to Δi_{in} at $D_t = 0$. The results show that Δi_{in} reduces significantly by implementing gate pulse shift. The highest ripple reduction is 90.57% in Sector 5C, and the lowest ripple reduction is 38.20% in Sector 3.

The experimental waveforms of i_{in} for sector 1 is shown in Fig. 5.7(a) for $D_t = 0$ and Fig. 5.7(b) for $D_t = 0.5$. Similarly, the experimental waveforms of i_{in} for sector 9 is shown in Fig. 5.7(c) for



(a) D_1=0.3, D_2=0.3 (b) D_1=0.5, D_2=0.2 (c) D_1=0.6, D_2=0.3 (d) D_1=0.7, D_2=0.2

(e) D_1=0.3, D_2=0.4 (f) D_1=0.3, D_2=0.5 (g) D_1=0.5, D_2=0.4 (h) D_1=0.6, D_2=0.4

(i) D_1=0.5, D_2=0.5 (j) D_1=0.6, D_2=0.5 (k) D_1=0.7, D_2=0.5 (l) D_1=0.7, D_2=0.4

(m) D_1=0.3, D_2=0.7 (n) D_1=0.6, D_2=0.6 (o) D_1=0.5, D_2=0.7 (p) D_1=0.7, D_2=0.6

Figure 5.8: Plots of measured Δi_{L1}, Δi_{L2} and Δi_{in} vs D_t using simulation (square) and experimental (circle) data for sector no. : (a) 1 (b) 2A (c) 2B (d) 3 (e) 4A (f) 4B (g) 5A (h) 5B (i) 5C (j) 5D (k) 6A (l) 6B (m) 7 (n) 8A (o) 8B (p) 9

$D_t = 0$ and Fig. 5.7(d) for $D_t = 0.55$. The results show that Δi_{in} is reducing significantly.

The plots of Δi_{L1}, Δi_{L2} and Δi_{in} vs D_t is shown in Fig. 5.8 for all the 16 sectors of CI-SIDO boost converter to show the gate pulse shift for minimum inductors and input currents together. The parameters for the experiments are presented in Table 5.3. It is observed that the $\mathbf{D}_{min}$ for $\underline{\Delta i_{L1}}$, $\underline{\Delta i_{L2}}$, and $\underline{\Delta i_{in}}$ intersects.

5.3 Maximizing Ripple Cancellations in Input Current

5.3.1 Analysis of Ripple Cancellation in Input Current

This section discusses the input current slope possibilities of the converter based on the values of L_1, L_2, k, V_{o1}, V_{o2}, V_{in}. A detailed analysis of the CI-SIDO boost converter to achieve maximum ripple cancellation in input current is also presented.

We define and distinguish two terms here:

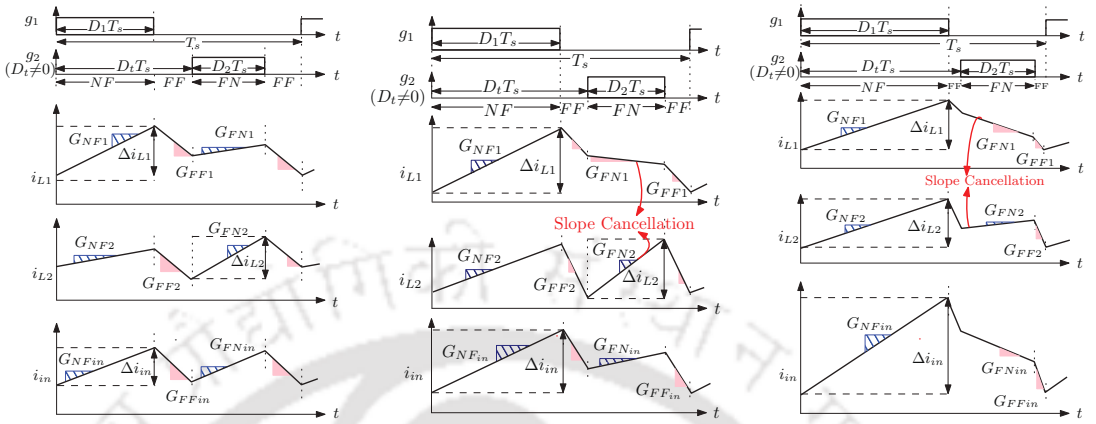
- Slope cancellation - When the slopes of i_{L1} and i_{L2} are opposite to each other in any state, it is termed as slope cancellation.
- Ripple cancellation - When $\Delta i_{in} < \Delta i_{L1} + \Delta i_{L2}$ it is termed as ripple cancellation.

In CI-SIDO boost converter, slope cancellation may or may not lead to ripple cancellation. This is unlike interleaved boost converters, where slope cancellation always leads to ripple cancellation.

The further analysis presented in the thesis is done for the gate pulse shift $\mathbf{D}_{min}$. The $\mathbf{D}_{min}$ for all the sectors and sub-sectors are taken from Table 5.2. The details of the slope cancellations and ripple cancellations for each sector is presented in Table 5.5. The rows of the table represent all 16 sectors and the columns represent the sign of slopes, sequence of states at $\mathbf{D}_{min}$, details of slope and ripple cancellations for all possible values of duty ratios. The table helps to find the sectors where slope cancellation and ripple cancellation is possible.

5.3.1.1 Slope Cancellation

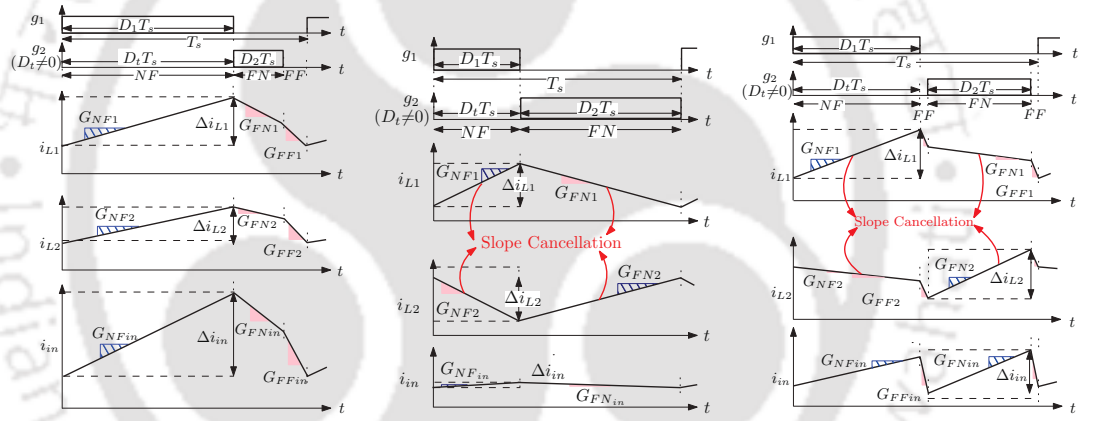
No slope cancellation is possible in states NN and FF of CI-SIDO boost, as G_{NNw} and G_{FFw} are always positive and negative, respectively. Only in states NF and FN slope cancellation may happen.



(a) Conditional ripple cancellation with no slope cancellation

(b) Conditional ripple cancellation with slope cancellation in FN

(c) No ripple cancellation with slope cancellation in FN

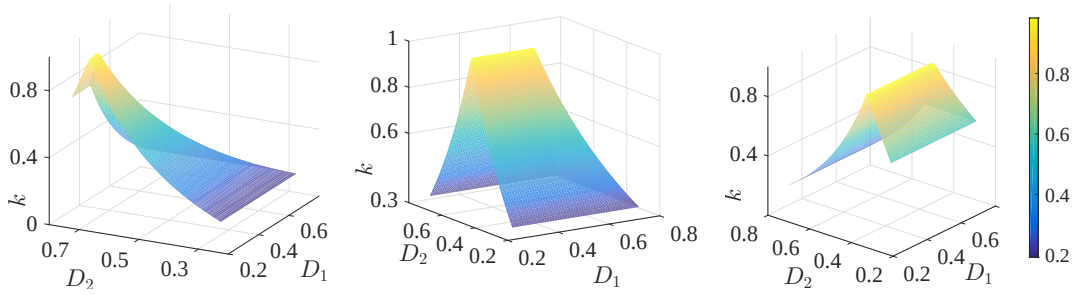


(d) No ripple cancellation with no slope cancellation

(e) Ripple cancellation due to slope cancellations in both states NF and FN for $D_1 + D_2 = 1$

(f) Ripple cancellation due to slope cancellations in both states NF and FN for $D_1 + D_2 < 1$

Figure 5.9: The waveforms of i_{L1}, i_{L2} and i_{in} with slope cancellation and ripple cancellation.



(a) (b) (c)

Figure 5.10: Plots of D_1, D_2, k for (a) $l_{12} = 0.45$, (b) $l_{12} = 1$, and (c) $l_{12} = 1.73$.

Table 5.5: Analysis of slope cancellation and ripple cancellation in all the sectors

Sect no.	(D_1+D_2)	Sign of slopes G_{NF1}	G_{NF2}	G_{FN1}	G_{FN2}	G_{NFin}	G_{FNin}	Sequence of states at $D_t = \mathbf{D}_{min}$	Slope cancellation	Δi_{in}	Ripple cancellation
1	< 1	+	+	+	+	+	+	$NF \rightarrow FF \rightarrow FN \rightarrow FF$	No	$\leq \Delta i_{L1} + \Delta i_{L2}$	Conditional
2A	< 1	+	+	-	+	+	+	$NF \rightarrow FF \rightarrow FN \rightarrow FF$	Yes in FN	$\leq \Delta i_{L1} + \Delta i_{L2}$	Conditional
2B						+	-			$= \Delta i_{L1} + \Delta i_{L2}$	No
3	< 1	+	+	-	-	+	-	$NF \rightarrow FN \rightarrow FF$	No	$= \Delta i_{L1} + \Delta i_{L2}$	No
	> 1							$NN \rightarrow NF \rightarrow NN \rightarrow FN$			
	$= 1$							$NF \rightarrow FN$			
4A	< 1	+	-	+	+	+	+	$NF \rightarrow FF \rightarrow FN \rightarrow FF$	Yes in NF	$\leq \Delta i_{L1} + \Delta i_{L2}$	Conditional
4B						-	+			$= \Delta i_{L1} + \Delta i_{L2}$	No
5A	< 1	+	-	-	+	+	+	$NF \rightarrow FF \rightarrow FN \rightarrow FF$	Yes in NF, FN	$< \Delta i_{L1} + \Delta i_{L2}$	Yes
5B	< 1					+	-	$NF \rightarrow FF \rightarrow FN \rightarrow FF$			
	> 1							$NN \rightarrow NF \rightarrow NN \rightarrow FN$			
	$= 1$							$NF \rightarrow FN$			
5C	< 1					-	+	$NF \rightarrow FF \rightarrow FN \rightarrow FF$			
	> 1							$NN \rightarrow NF \rightarrow NN \rightarrow FN$			
	$= 1$							$NF \rightarrow FN$			
5D	> 1					-	-	$NN \rightarrow NF \rightarrow NN \rightarrow FN$			
6A	> 1	+	-	-	-	-	-	$NN \rightarrow NF \rightarrow NN \rightarrow FN$	Yes in NF	$\leq \Delta i_{L1} + \Delta i_{L2}$	Conditional
6B						+	-			$= \Delta i_{L1} + \Delta i_{L2}$	No
7	< 1	-	-	+	+	-	+	$NF \rightarrow FN \rightarrow FF$	No	$= \Delta i_{L1} + \Delta i_{L2}$	No
	> 1							$NN \rightarrow NF \rightarrow NN \rightarrow FN$			
	$= 1$							$NF \rightarrow FN$			
8A	> 1	-	-	-	+	-	-	$NN \rightarrow NF \rightarrow NN \rightarrow FN$	Yes in FN	$\leq \Delta i_{L1} + \Delta i_{L2}$	Conditional
8B						-	+			$= \Delta i_{L1} + \Delta i_{L2}$	No
9	> 1	-	-	-	-	-	-	$NN \rightarrow NF \rightarrow NN \rightarrow FN$	No	$\leq \Delta i_{L1} + \Delta i_{L2}$	Conditional

For example, if G_{NF1} and G_{NF2} are positive and negative, respectively (or vice versa), then slope cancellation takes place in state NF (similarly for state FN). Table 5.5 (column 10) shows all the sectors, in which slope cancellation occur. We observe that only in sector 5 slope cancellations occur in both states NF and FN. Whereas in the rest of the sectors, either no slope cancellation or slope cancellation occurs only in state NF or FN.

5.3.1.2 Ripple Cancellation

The status of ripple cancellation is presented in Table 5.5 after analyzing– expressions of $\underline{\Delta i_{in}}$, corresponding sequence of states and states in which slope cancellation occurs; for each sector and conditions of $D_1 + D_2$. We observe the following for ripple cancellation:

(i) *No ripple cancellation*: In sectors 2B, 4B, 6B, 8B, 3 and 7 either there is no slope cancellation, or the state in which slope cancellation can occur is not present in expression of $\underline{\Delta i_{in}}$ i.e. that state does not affect the ripple of input current. So, based on the conditions of slope cancellation, two conditions are as follows–

- No slope cancellation: An example of no ripple cancellation with no slope

cancellation is shown in Fig. 5.9(d) for sector 3. There is no slope cancellation here, as G_{NF1}, G_{NF2} are both positive, and G_{FN1}, G_{FN2} are both negative. Here, $\Delta i_{in} = G_{NFin} D_1 T_s$ which is the sum of $G_{NF1} D_1 T_s$ and $G_{NF2} D_1 T_s$.

- Slope cancellation: An example of no ripple cancellation with slope cancellation in state FN is shown in Fig. 5.9(c) for sector 2B. There is slope cancellation in state FN, as $G_{FN1} < 0$, $G_{FN2} > 0$. Here, $\Delta i_{in} = G_{NFin} D_1 T_s$ which is the sum of $G_{NF1} D_1 T_s$ and $G_{NF2} D_1 T_s$. The state FN, in which slope cancellation occurs does not affect the ripple of input current.

(ii) *Conditional ripple cancellation*: In sectors 2A, 4A, 6A, 8A, 1, and 9, Δi_{in}= or $<\Delta i_{L1}+\Delta i_{L2}$ and is dependent on the relative magnitudes of $G_{NF_{in}}$, $G_{FN_{in}}$, and D_1, D_2. It is not affected by slope cancellation. Based on the conditions of slope cancellation, two conditions are as follows–

- No slope cancellation: An example of conditional ripple cancellation with no slope cancellation is shown in Fig. 5.9(a) for sector 1. There is no slope cancellation as G_{NF1}, G_{NF2}, G_{FN1}, and G_{FN2} are all positive. In Fig. 5.9(a), $\Delta i_{in} = G_{NFin} D_1 T_s$ which is less than or equal to the sum of $G_{NF1} D_1 T_s$ and $G_{FN2} D_2 T_s$.
- Slope cancellation: An example of conditional ripple cancellation with slope cancellation in state FN is shown in Fig. 5.9(b) for sector 2A. There is slope cancellation in state FN, as $G_{FN1} < 0$, $G_{FN2} > 0$. Here, $\Delta i_{in} = G_{NFin} D_1 T_s$ which is less than or equal to the sum of $G_{NF1} D_1 T_s$ and $G_{FN2} D_2 T_s$. Δi_{in} is dependent on the relative magnitudes of G_{NF1}, G_{FN2}, and D_1, D_2.

(iii) *Ripple cancellation*: In sectors 5A, 5B, 5C and 5D, slope cancellation in both states NF and FN makes $\Delta i_{in} < \Delta i_{L1}+\Delta i_{L2}$ for all possible conditions of $D_1 + D_2$. The condition $D_1 + D_2 = 1$ occurs in sectors 5B and 5C. We observe from Table 5.5, the sequence of states followed for $D_1 + D_2 = 1$ is $NF \rightarrow FN$ and Fig. 5.9(e) shows the same for sector 5C. The condition $D_1 + D_2 < 1$ occurs in sectors 5A, 5B, 5C and

$D_1 + D_2 > 1$ occurs in sectors 5B, 5C, 5D. We observe from Table 5.5, the sequence of states followed for $D_1 + D_2 <$ or $>$ 1 contain states NN or FF in addition to states NF and FN and Fig. 5.9(f) shows the scenario for sector 5A when $D_1 + D_2 < 1$.

5.3.1.3 Maximum Ripple Cancellation

From the above analysis, we find that maximum ripple cancellations take place in sectors 5A, 5B, 5C, and 5D for any given condition of $D_1 + D_2$.

For $D_1 + D_2 < 1$, we observe that CI-SIDO boost converter can be designed to operate in sectors 5A, 5B and 5C. The expressions of ripples in these three sectors are derived as:

$$\text{5A:} \quad \Delta i_{in} = Max\{G_{NF_{in5A}} D_1 T_s, G_{FN_{in5A}} D_2 T_s\} \tag{5.5}$$

$$\text{5B:} \quad \Delta i_{in} = G_{NF_{in5B}} D_1 T_s \tag{5.6}$$

$$\text{5C:} \quad \Delta i_{in} = G_{FN_{in5C}} D_2 T_s \tag{5.7}$$

It can be shown that

$$G_{NF_{in5A}} D_1 = G_{FF_{in5A}}(1 - D_1 - D_2) - G_{FN_{in5A}} D_2 \tag{5.8}$$

$$G_{NF_{in5B}} D_1 = G_{FF_{in5B}}(1 - D_1 - D_2) + G_{FN_{in5B}} D_2 \tag{5.9}$$

$$G_{FN_{in5C}} D_2 = G_{FF_{in5C}}(1 - D_1 - D_2) + G_{NF_{in5C}} D_1 \tag{5.10}$$

Thus, we observe that Δi_{in} of sector 5A is smaller than sectors 5B and 5C. Similarly, for $D_1 + D_2 > 1$ it can be shown that Δi_{in} of sector 5D is smaller than sectors 5B and 5C.

For $D_1 + D_2 = 1$, we observe that CI-SIDO boost converter can be designed to operate in sectors 5B and 5C. The expressions of ripples in these two sectors are derived as:

$$\text{5B:} \quad \Delta i_{in} = G_{NF_{in5B}} D_1 T_s = |G_{FN_{in5B}}| D_2 T_s \tag{5.11}$$

$$\text{5C:} \quad \Delta i_{in} = |G_{NF_{in5C}}| D_1 T_s = G_{FN_{in5C}} D_2 T_s \tag{5.12}$$

Thus, we observe that Δi_{in} of sectors 5B and 5C are equal.

5.3.2 Proposed Design of Inductors to Achieve Maximum Ripple Cancellation

Based on the findings, the thesis proposes the design method for any given value of D_1, D_2. The converter needs to be designed and operated in sector 5. The gate pulse g_2 is shifted w.r.t. g_1 by $\mathbf{D}_{min}$ taken from Table 5.2.

(i) If $D_1 + D_2 > 1$ design the converter to operate in sub-sectors 5D.

(ii) If $D_1 + D_2 < 1$ design the converter to operate in sub-sectors 5A.

(iii) If $D_1 + D_2 = 1$ design the converter to operate in sub-sectors 5B or 5C depending on the values of $\frac{L_1}{L_2}$. Though, design is easier if L_1, L_2 are close to each other i.e. $\max\{\frac{L_1}{L_2}, \frac{L_2}{L_1}\}$ should be as low as possible.

The following equations are derived to design the converter to operate in sub-sectors 5A, 5B, 5C, and 5D.

$$\left.\begin{aligned} \frac{(kl_{12})}{(kl_{12}+1)} < D_1 < \frac{\left({l_{12}}^2 + kl_{12}\right)}{\left({l_{12}}^2 + 2kl_{12} + 1\right)} \\ \frac{(k)}{(l_{12}+k)} < D_2 < \frac{(1+kl_{12})}{\left({l_{12}}^2 + 2kl_{12} + 1\right)} \end{aligned}\right\} : \text{Sector 5A} \tag{5.13}$$

$$\left.\begin{aligned} \frac{\left({l_{12}}^2 + kl_{12}\right)}{\left({l_{12}}^2 + 2kl_{12} + 1\right)} < D_1 < \frac{(l_{12})}{(l_{12}+k)} \\ \frac{(k)}{(l_{12}+k)} < D_2 < \frac{(1+kl_{12})}{\left({l_{12}}^2 + 2kl_{12} + 1\right)} \end{aligned}\right\} : \text{Sector 5B} \tag{5.14}$$

$$\left.\begin{aligned} \frac{(kl_{12})}{(kl_{12}+1)} < D_1 < \frac{\left({l_{12}}^2 + kl_{12}\right)}{\left({l_{12}}^2 + 2kl_{12} + 1\right)} \\ \frac{(1+kl_{12})}{\left({l_{12}}^2 + 2kl_{12} + 1\right)} < D_2 < \frac{(1)}{(kl_{12}+1)} \end{aligned}\right\} : \text{Sector 5C} \tag{5.15}$$

$$\left.\begin{aligned} \frac{\left({l_{12}}^2 + kl_{12}\right)}{\left({l_{12}}^2 + 2kl_{12} + 1\right)} < D_1 < \frac{(l_{12})}{(l_{12}+k)} \\ \frac{(1+kl_{12})}{\left({l_{12}}^2 + 2kl_{12} + 1\right)} < D_2 < \frac{(1)}{(kl_{12}+1)} \end{aligned}\right\} : \text{Sector 5D} \tag{5.16}$$

where, $l_{12} = \sqrt{\frac{L_1}{L_2}}$. For given values of D_1, D_2, solving inequalities (5.13), (5.14), (5.15), and (5.16), k and $\frac{L_1}{L_2}$ can be obtained to operate the converter in sectors 5A, 5B, 5C, and 5D, respectively.

The expressions derived for Δi_{in} for sectors 5A, 5B, 5C, and 5D are also given below.

$$\boxed{\Delta i_{in} = \max\{G_{NF_{in5A}} D_1 T_s, G_{FN_{in5A}} D_2 T_s\}\Big\}: \text{Sector 5A}} \tag{5.17}$$

$$\boxed{\Delta i_{in} = |G_{NF_{in}}| D_1 T_s = |G_{FN_{in}}| D_2 T_s: \text{Sectors 5B, 5C}} \tag{5.18}$$

$$\boxed{\Delta i_{in} = \max\{|G_{NF_{in5D}}|(1-D_2)T_s, |G_{FN_{in5D}}|(1-D_1)T_s\}\Big\}: \text{Sector 5D}} \tag{5.19}$$

It is to be noted that to ensure that the converter operates in sector 5, only a ratio of L_1 and L_2, i.e., $\frac{L_1}{L_2}$ is required. There is no dependence on the absolute values of L_1 and L_2. That is why our proposed design method is giving l_{12} for a selected value of k.

The actual values of L_1 and L_2 are calculated depending of the specified $\widehat{\Delta i_{in}}$, $\widehat{\Delta i_{L1}}$, $\widehat{\Delta i_{L2}}$ which is the maximum limit specified on the input current ripple and inductor current ripples respectively. In this way, the converter operates in sector 5 while maintaining the allowed maximum limit specified on the input current ripple.

To operate the converter in sector 5 for all possible duty ratios, the values of k is obtained using (5.20) for a particular l_{12}. The plots of D_1, D_2, k presented in Fig. 5.10 show the range of k for three different values of l_{12}.

$$k < \min\{\frac{l_{12}D_2}{(1-D_2)}, \frac{(1-D_2)}{l_{12}D_2}, \frac{D_1}{l_{12}(1-D_1)}, \frac{l_{12}(1-D_1)}{D_1}\} \tag{5.20}$$

It can be seen from Fig. 5.10 that reasonable l_{12} and k are obtained for any values of D_1, D_2.

5.3.3 Experimental Verification

This section provides the details of the test bench and results obtained for verifying the proposed design procedure.

5.3.3.1 Experimental Test Bench

A 100 W laboratory prototype of CI-SIDO boost converter, shown in Fig. 3.4(b), is developed for the experiment. The input voltage of 6 V is obtained from a regulated DC power supply of 64 V, 20 A. Two MOSFETs of 200 V, 90 A, and hyperfast diodes of 1200V, 30 A, are used. The current and voltage waveforms are observed in a four-channel digital storage oscilloscope (DSO) with current

Table 5.6: Converter Parameters

V_{in}	6 V	T_s 10 μs	C_1, C_2 100 μF
R_1, R_2	12 Ω, 8 Ω	MOSFET	IRFP90N20DPBF
		Diode	RHRP30120

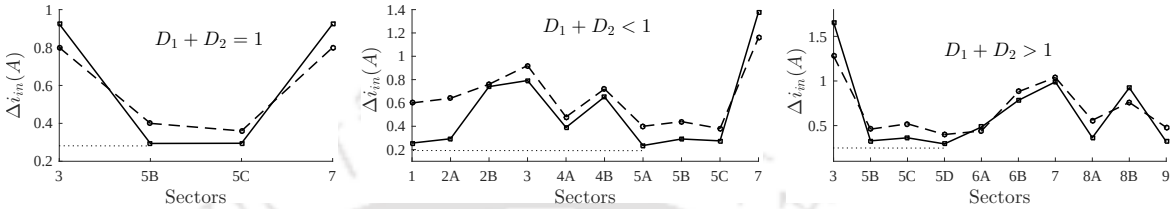


Figure 5.11: Plots of sectors vs Δi_{in} to verify maximum ripple cancellations, using simulations (□) and experimental (○) data for $D_1 + D_2$ (a) = 1, (b) < 1, (c) > 1.

probes and differential probes. The list of components used is presented in Table 5.6. The gate pulses g_1, g_2 are generated using FPGA kit– NI sbRIO 9637. The operation of CI-SIDO boost in different sectors with the same duty ratio requires different coupled inductors. The coupled inductors are made using ferrite cores with different coefficient of coupling varying from 0.7 to 0.92. It is to be noted that the analysis presented in the thesis is true for any value of the coefficient of coupling. The coefficient of coupling is varied by changing the air gap between the cores and the winding locations on the limbs of the core. Finally, the number of turns in coupled inductor windings of the desired inductance values depends on the core used and the size of the wire.

5.3.3.2 Verification of the Maximum Ripple Cancellation in Sub-sectors of Sector 5

To prove that sub-sectors of sector 5 have the minimum ripple amongst all sectors (and the basis on which the design method is proposed) and maximum ripple cancellation takes place in sub-sectors of sector 5, we have chosen different values of V_{o1}, V_{o2} and V_{in} such that $D_1 + D_2 = 1, < 1$ and > 1. Then obtained D_1, D_2 are placed in different sectors and sub-sectors by choosing various values of L_1, L_2 and k. A shift of D_t is given to gate pulse g_2 with respect to g_1, where $D_t \epsilon \mathbf{D}_{min}$ given in Table 5.2, and Δi_{in} is measured experimentally and by simulations. Values of load resistances used are given in Table 5.6.

It should be noted that D_1, D_2 cannot be placed in all the sectors and sub-sectors for any given values of V_{o1}, V_{o2} and V_{in}, as it depends on the condition of $D_1 + D_2$ mentioned in column 2 of

Table 5.5. For example, if the required output voltages are $V_{o1} = V_{o2} = 12\ V$ and $V_{in} = 6\ V$, the corresponding duty ratios are $D_1 = D_2 = 0.5$. As presented in column 2 of Table 5.5, for $D_1 + D_2 = 1$, sectors 3, 5B, 5C and 7 are possible. To place D_1, D_2 in sector 3, the values of L_1, L_2, k chosen are 90 μH, 235 μH, 0.88, respectively. Similarly, to place D_1, D_2 in sectors 5B, 5C, 7, the values of L_1, L_2, k chosen are 100 μH, 155 μH, 0.8, 155 μH, 100 μH, 0.8, and 235 μH, 90 μH, 0.88, respectively. The Δi_{in} obtained experimentally and by simulations are plotted against the sectors, and is shown in Fig. 5.11(a). The plot shows that ripple is minimum in sub-sectors of sector 5. Similarly, experiments are performed for $D_1 = 0.4$, $D_2 = 0.5$ (in Fig. 5.11(b)) and $D_1 = 0.6$, $D_2 = 0.5$ (in Fig. 5.11(c)). In all the cases, ripples are minimum in sub-sectors of sector 5 among all sectors.

5.3.3.3 Verification of Proposed Design Method to Achieve Maximum Ripple Cancellation

To verify the design procedure proposed in Section 5.3.2 to achieve maximum ripple cancellation, the CI-SIDO boost converter is designed and experimentally tested for few different values of V_{in}, V_{o1}, V_{o2}. Two examples of designing the converter are presented below.

Example 1: A CI-SIDO boost converter needs to be designed with $V_{in} = 3.3\ V$, $V_{o1} = 5.1\ V$, $V_{o2} = 11\ V$ and switching frequency 100 kHz. The maximum limit specified on input current ripple, $\widehat{\Delta i_{in}}$ as well as inductor current ripple, $\widehat{\Delta i_{Lw}}$ is within 0.05 A. Design CI-SIDO boost converter by choosing proper values of parameters L_1, L_2, k and shift D_t.

Solution: $D_1 = 0.35$, $D_2 = 0.7$. As $D_1 + D_2 > 1$, from the analysis in Section 5.3.2, CI-SIDO boost converter can be designed in Sector 5D. If $k = 0.8$, using (5.16) the range of l_{12} obtained are $0.43 < l_{12} < 0.57$ and $0.46 < l_{12} < 0.54$ from the equations presented here-

$$\frac{\left({l_{12}}^2 + 0.8 l_{12}\right)}{\left({l_{12}}^2 + 1.6 l_{12} + 1\right)} < 0.35 < \frac{(l_{12})}{(l_{12} + 0.8)}$$

$$\frac{(1 + 0.8 l_{12})}{\left({l_{12}}^2 + 1.6 l_{12} + 1\right)} < 0.70 < \frac{(1)}{(0.8 l_{12} + 1)}$$

So, the final range obtained are $0.46 < l_{12} < 0.54$. We choose $l_{12} = 0.5$. Now, for $k = 0.8$, $l_{12} = 0.5$, $V_{in} = 3.3$, $V_{o1} = 5.1$ and $V_{o2} = 11.0$, the expression of Δi_{in} from (5.19) reduces to-

$$\Delta i_{in} = \max\{\frac{1.28}{L_2} T_s, \frac{2.71}{L_2} T_s\} \tag{5.21}$$

As given, $\widehat{\Delta i_{in}} = 0.05 = \frac{2.71}{L_2} T_s$. Thus, $L_2 = 542.0\mu H$ and $L_1 = 135.5\mu H$. From Table 5.2, $\mathbf{D}_{min} = 0.32 - 0.33$. The expression of Δi_{L1} and Δi_{L2} in sector 5 for $D_1 + D_2 > 1$ and $D_1 < D_2$ is given by (5.22).

$$\underline{\Delta i_{L1}} = G_{NN1}(D_1 + D_2 - 1)T_s + G_{NF1}(1 - D_2)T_s, \tag{5.22a}$$

$$\underline{\Delta i_{L2}} = G_{NN2}(D_1 + D_2 - 1)T_s + G_{FN2}(1 - D_1)T_s \tag{5.22b}$$

From the above calculated L_1, L_2 , it is found that $\Delta i_{L1} = 0.061\ A$ and $\Delta i_{L2} = 0.037\ A$ which is above 0.05 A. So, based on $\widehat{\Delta i_{in}}$ and $\widehat{\Delta i_{Lw}}$ three solutions of L_1 and L_2 are possible which is as follows–.

(i) If $\underline{\Delta i_{in}} = 0.046\ A$ then $L_1 = 135.5\mu H \Rightarrow L_2 = L_1/0.25 \Rightarrow L_2 = 542.0\mu H \Rightarrow \underline{\Delta i_{L1}} = 0.061\ A \Rightarrow \underline{\Delta i_{L2}} = 0.037\ A$

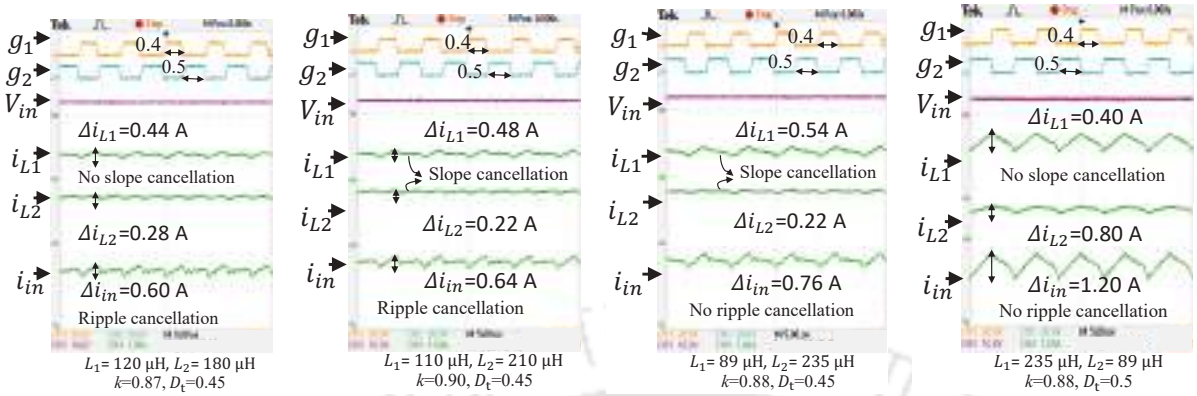
(ii) If $\underline{\Delta i_{L1}} = 0.05\ A$ then $L_1 = 165.0\mu H \Rightarrow L_2 = L_1/0.25 \Rightarrow L_2 = 660.0\mu H \Rightarrow \underline{\Delta i_{in}} = 0.037\ A \Rightarrow \underline{\Delta i_{L2}} = 0.031\ A$

(iii) If $\underline{\Delta i_{L2}} = 0.05\ A$ then $L_2 = 403.33\ \mu H \Rightarrow L_1 = 0.5L_2 \Rightarrow L_1 = 100.83\mu H \Rightarrow \underline{\Delta i_{in}} = 0.06\ A \Rightarrow \underline{\Delta i_{L1}} = 0.082\ A$

The second case keeps all the three current ripples Δi_{in}, Δi_{L1}, Δi_{L2} are within 0.05 A. So, we select $L_1 = 165.0\mu H$ and $L_2 = 660.0\mu H$.

Example 2: A coupled inductor is available with $\frac{L_1}{L_2} = 0.5$ and $k = 0.9$. The output voltages to be maintained are 6 V and 8.6 V. Find the range of input voltage such that CI-SIDO boost converter is operated in sector 5A with $\widehat{\Delta i_{in}}$ and $\widehat{\Delta i_{Lw}}$ within 0.04 A.

Solution: For $\frac{L_1}{L_2} = 0.5$ and $k = 0.9$, to operate the converter in sector 5A, $r_{FN1} = 0.3889$, $r_{FNin} = 0.4098$, $r_{NF2} = 0.56$ and $r_{NFin} = 0.5902$. If V_{in} is the input voltage, $D_1 = 1 - \frac{V_{in}}{6}$ and $D_2 = 1 - \frac{V_{in}}{8.6}$. For sector 5A, $0.3889 < 1 - \frac{V_{in}}{6} < 0.4098$ and $0.56 < 1 - \frac{V_{in}}{8.6} < 0.5902$. So, the range obtained is $3.54 < V_{in} < 3.67$. We choose, $V_{in} = 3.6$, so $D_1 = 0.4$ and $D_2 = 0.58$. From (5.17), the



(a) Sector 1 (b) Sector 2A (c) Sector 2B (d) Sector 7

Figure 5.12: The experimental waveforms of i_{L1}, i_{L2} and i_{in} with slope cancellation and ripple cancellation.

input current ripple expression is given by-

$$\Delta i_{in} = \max\{\frac{0.44}{L_1}T_s, \frac{0.5}{L_1}T_s\}$$

As given, $\widehat{\Delta i_{in}} = 0.04 = \frac{0.5}{L_1}T_s$. Thus, $L_1 = 125.0\mu H$ and $L_2 = 250.0\mu H$. From Table 5.2, $\mathbf{D}_{min} = 0.41$. The expression of Δi_{L1} and Δi_{L2} in sector 5 for $D_1 + D_2 < 1$ and $D_1 < D_2$ is given by (5.23).

$$\underline{\Delta i_{L1}} = G_{NF1}D_1T_s, \ \underline{\Delta i_{L2}} = G_{NF2}D_2T_s \tag{5.23}$$

From the above calculated L_1, L_2 , it is found that $\Delta i_{L1} = 0.067\ A$ and $\Delta i_{L2} = 0.5\ A$ which is above $0.04\ A$. So, based on $\widehat{\Delta i_{in}}$ and $\widehat{\Delta i_{Lw}}$ three solutions of L_1 and L_2 are possible which is as follows–.

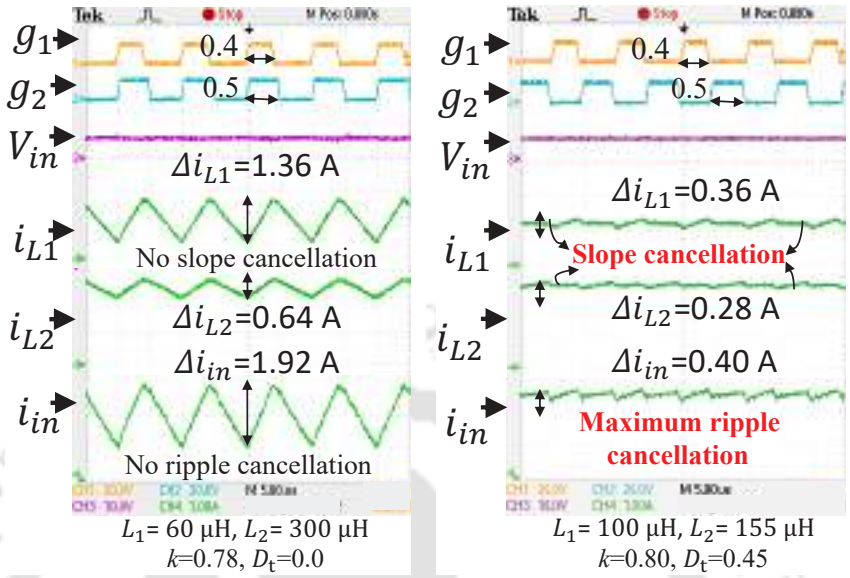
(i) If $\underline{\Delta i_{in}} = 0.04\ A$ then $L_1 = 125.0\mu H \Rightarrow L_2 = L_1/0.5 \Rightarrow L_2 = 250\mu H \Rightarrow \underline{\Delta i_{L1}} = 0.067\ A \Rightarrow \underline{\Delta i_{L2}} = 0.5\ A$

(ii) If $\underline{\Delta i_{L1}} = 0.04\ A$ then $L_1 = 230.0\mu H \Rightarrow L_2 = L_1/0.5 \Rightarrow L_2 = 460.0\mu H \Rightarrow \underline{\Delta i_{in}} = 0.022\ A \Rightarrow \underline{\Delta i_{L2}} = 0.036\ A$

(iii) If $\underline{\Delta i_{L2}} = 0.04\ A$ then $L_2 = 416.15\mu H \Rightarrow L_1 = 0.5L_2 \Rightarrow L_1 = 208.07\mu H \Rightarrow \underline{\Delta i_{in}} = 0.024\ A \Rightarrow \underline{\Delta i_{L1}} = 0.044\ A$

The second case keeps all the three current ripples Δi_{in}, Δi_{L1}, Δi_{L2} within $0.04\ A$. So, we select $L_1 = 230.0\mu H$ and $L_2 = 460.0\mu H$.

Similar to the examples, the CI-SIDO boost converter is designed for $V_{in} = 6.0\ V$, $V_{o1} = 10.0\ V$,



L_1= 60 µH, L_2= 300 µH
k=0.78, D_t=0.0

(a) Sector 3

L_1= 100 µH, L_2= 155 µH
k=0.80, D_t=0.45

(b) Sector 5A

Figure 5.13: Experimental results of i_{L1}, i_{L2}, i_{in} when (a) proposed method is not applied, (b) proposed method is used.

V_{o2} = 12.0 V and then experimentally tested to achieve $\widehat{\Delta i_{in}}$ = 0.5 A. So, D_1 and D_2 obtained are 0.4 and 0.5 such that $D_1 + D_2 < 1$. Following the design procedure, the converter is designed in Sector 5A. The obtained coupled inductor parameters are $L_1 = 100.0\mu H$, $L_2 = 155.0\mu H$, k = 0.8 and $\mathbf{D}_{min}$ = 0.45. The experimental result is shown in Fig. 5.13(b). The experimental results of D_1 = 0.4 and D_2 = 0.5 for four more sectors are presented in Fig. 5.12. Keeping the duty ratios same, different sectors are generated by varying the coupled inductor parameters L_1, L_2, k. The comparison of results show that for $D_1 + D_2$ = 0.9, the ripple is minimum in sub-sector 5A.

Table 5.7: % Reduction in input current ripple Δi_{in}

Sl. No.	Voltages			% reduction in Δi_{in}	Details of proposed method			
	V_{in} (V)	V_{o1} (V)	V_{o2} (V)		L_1 (μH)	L_2 (μH)	k	$\mathbf{D}_{min}$
1	6	12	12	87.33	155	100	0.8	0.5
2	6	10	12	85.29	100	155	0.8	0.45
3	6	15	12	87.80	155	100	0.8	0.55

In Table 5.7, the percentage reduction in Δi_{in} is presented when the converter is designed using proposed design method for three different conditions of duty ratios. The percentage is calculated w.r.t. the maximum Δi_{in} at D_t = 0. For example in third row, D_1 = 0.6, D_2 = 0.5 such that $D_1 + D_2$ = 1.1, the coupled inductor designed is L_1 = 155 μH, L_2 = 100 μH, k = 0.8 which lies in sector 5D.

Table 5.8: Comparisons of various ripple reduction methods in CI-SIDO converters

References	[72]	[56]	this analysis
Gate pulse shift	0	0.5	0.32
Input current Ripples	0.25 A	0.22 A	0.04 A
Inductor current Ripples	0.18, 0.06 A	0.16, 0.08 A	0.05, 0.03 A
Coupled inductor	232.05 μH, 1565.29 μH, $k = 0.8$	165.00 μH, 660.00 μH, $k = 0.8$	165.00 μH, 660.00 μH, $k = 0.8$
Remarks	only Δi_{L2} reduced	phase shift $360/n$ does not give reduced i_{in}	Least ripples with lowest coupled inductors

Therefore, the proposed designed method significantly reduces the input current ripples.

The experimental results of i_{L1}, i_{L2}, i_{in} when proposed method is not applied is shown in Fig. 5.13(a) for the duty ratios $D_1 = 0.4$, $D_1 = 0.5$. Compared to sector 5A in Fig. 5.13(b), Δi_{L1}, Δi_{L2}, Δi_{in} is higher by 73.5%, 56.25%, 79.17% respectively.

If the CI-SIDO boost converter has to maintain the output voltages such that one output voltage is too high compared to the other, the current ripple in one branch becomes too high for the switch. For example, if $V_{o1} = 3.09\ V$, $V_{o2} = 100\ V$ with the available input voltage of 3 V, then we obtain $D_1 = 0.03$, $D_2 = 0.97$ where $D_1 + D_2 = 1$. From the analysis, CI-SIDO converter is designed in Sector 5B. If $k = 0.8$, using (5.14) the range of l_{12} obtained is $0.0247 < l_{12} < 0.038$. We choose $l_{12} = 0.026$. Now, if we choose $L_1 = 1\ \mu H$ and $L_2 = 1400\ \mu H$, the values of ripples are $\Delta i_{L1} = 0.79\ A$, $\Delta i_{L2} = 0.004\ A$ such that Δi_{L1} is 197.5 times greater than Δi_{L2}. However, keeping l_{12} same we can limit the current ripples to design L_1 and L_2. For instance, if the allowed current ripples are 0.05 A, i.e., $\widehat{\Delta i_{in}} = \widehat{\Delta i_{L1}} = \widehat{\Delta i_{L2}} = 0.05\ A$, the inductance values obtained are $L_1 = 15.78\ \mu H$ and $L_2 = 22500\ \mu H$.

The ripple reduction methods of various other DC-DC converters are implemented in CI-SIDO boost converter to compare the input and inductor current ripples in Table 5.8. The parameters of the converter are taken from example 1, i.e., $V_{in} = 3.3\ V$, $V_{o1} = 5.1\ V$, $V_{o2} = 11\ V$ such that $D_1 = 0.35$, $D_2 = 0.7$. The coupled inductor design using [72] reduces only Δi_{L2}. Also, for same coupled inductors as this chapter, if the shifting is $360/n$ as discussed in [56], the values of Δi_{in}, Δi_{L1}, Δi_{L2} are higher by 82%, 69%, 62.5%, respectively, as compared to our proposed method.

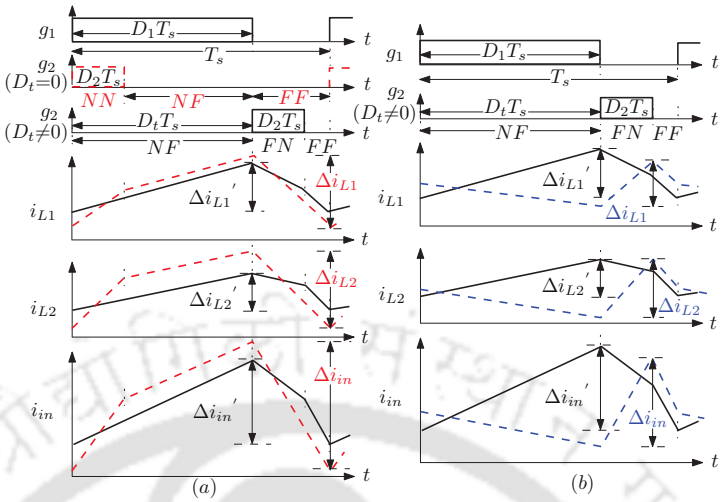


Figure 5.14: The current ripples Δi_{L1}, Δi_{L2}, Δi_{in} when (a) $D_t = 0$ (red dash) and $D_t = D_1$ (black solid), (b) $D_t = D_1$ (black solid) but L_1, L_2, k changed (blue dash).

5.4 Achieving Approximately Zero Ripples in Input Current

5.4.1 Challenges in Achieving Zero Ripple Input Current

In this section, the challenges are presented to achieve a zero ripple input current in the CI-SIDO boost converter. We note the following from Fig. 5.14.

- The input current ripples Δi_{in} depends the values of shifting between g_1 and g_2. From Fig. 5.14(a), it is shown that as gate pulse is shifted from $D_t = 0$ to $D_t = \mathbf{D}_{min}$ the ripples Δi_{L1}, Δi_{L2}, Δi_{in} decreases.

- Even if D_1, D_2, D_t are kept same, the change in coupled inductor parameters L_1, L_2, k change the ripples Δi_{L1}, Δi_{L2}, Δi_{in}, as shown in Fig. 5.14(b).

From the above analysis it is found that Δi_{in} depends on the values of shift D_t as well as on the values of L_1, L_2, k, D_1, D_2. Therefore, for given V_{o1}, V_{o2}, V_{in}, a design method is needed which takes into account both, the gate pulse shift D_t and the values of coupled inductor parameters L_1, L_2, k.

5.4.2 Achieving Zero Ripple Input Current: Proposed Design Method and its Proof

This section first proposes a design method for zero ripple input current in the CI-SIDO boost converter. In case the values of input and output voltages are such that absolute zero ripples in input

current are not possible, the design method proposes to achieve input current ripple less than maximum specified limit $\widehat{\Delta i_{in}}$. The analytical proofs of the proposed design method are also presented.

5.4.2.1 Proposed Design Method

The voltages V_{o1}, V_{o2}, V_{in} i.e. D_1, D_2, and maximum limit $\widehat{\Delta i_{in}}$ are specified for CI-SIDO boost converter. In this proposed design method, we have adopted a twofold approach to achieve input current ripple as either zero or less than maximum specified limit $\widehat{\Delta i_{in}}$. First is the shifting of gate pulse g_2 with respect to g_1 by $\mathbf{D}_{min}$, and second is choosing the proper values for coupled inductor parameters L_1, L_2, k. The shifting of gate pulse to achieve minimum input current ripples is already presented in Table 5.2. However, the systematic approach to choose the proper values of L_1, L_2, k is presented in this section.

We define a ratio of r as:

$$r = \begin{cases} \frac{D_2}{1-D_2} & : D_1 \geq D_2 \\ \\ \frac{1-D_1}{D_1} & : D_1 < D_2. \end{cases} \tag{5.24}$$

The proposed design method is divided in two parts-

- $D_1 + D_2 = 1$: For this condition of D_1 and D_2, absolute zero ripple input current is possible. First gate pulse g_2 is shifted w.r.t. g_1 by

$$\mathbf{D}_{min} = D_1. \tag{5.25}$$

  Second, L_1 and L_2 are chosen such that the ratio of $\frac{L_1}{L_2}$ is obtained as

$$\boxed{\frac{L_1}{L_2} = \left[\frac{-(r-1)k \pm \sqrt{[(r-1)k]^2 + 4r}}{2r}\right]^2}. \tag{5.26}$$

  The zero ripple input current does not depend on choice of L_1 or L_2, but only on $\frac{L_1}{L_2}$.

- $D_1 + D_2 <$ or > 1: In these cases, absolute zero ripple in input current is not possible. However, we can limit the input current ripple to the maximum specified ripple current limit $\widehat{\Delta i_{in}}$. To achieve that, first the value of shift in gate pulse $D_t = \mathbf{D}_{min}$ is given by

$$\mathbf{D}_{min} = \begin{cases} D_1 \leq D_t \leq 1 - D_2 & : D_1 + D_2 < 1 \\ 1 - D_2 \leq D_t \leq D_1 & : D_1 + D_2 > 1. \end{cases} \tag{5.27}$$

Second, $\frac{L_1}{L_2}$ is obtained using (5.26) and L_1 is obtained using

$$L_1 = \begin{cases} \frac{V_{o1}|l_{FN}|(1-D_1)T_s}{(1-k^2)\widehat{\Delta i_{in}}} & : D_1 \geq D_2,\ D_1 + D_2 > 1 \\ \frac{V_{o1}l_{FN}D_2T_s}{(1-k^2)\widehat{\Delta i_{in}}} & : D_1 \geq D_2,\ D_1 + D_2 < 1 \\ \frac{V_{o2}|l_{NF}|(1-D_2)T_s}{(1-k^2)\widehat{\Delta i_{in}}} & : D_1 < D_2,\ D_1 + D_2 > 1 \\ \frac{V_{o2}l_{NF}D_1T_s}{(1-k^2)\widehat{\Delta i_{in}}} & : D_1 < D_2,\ D_1 + D_2 < 1 \end{cases} \tag{5.28}$$

where, $l_{FN} = {l_r}^2 + kl_r - D_1({l_r}^2 + 2kl_r + 1)$

$l_{NF} = 1 + kl_r - D_2({l_r}^2 + 2kl_r + 1)$ and $l_r = \sqrt{\frac{L_1}{L_2}}$.

5.4.2.2 Proof of the Proposed Method

Proof of Absolute Zero-Ripple being Possible for $D_1 + D_2 = 1$; and Not Possible for $D_1 + D_2 <$ or > 1

The expression of Δi_{in} is given as

$$\Delta i_{in} = G_{NFin}D_1T_s = G_{FNin}D_2T_s. \tag{5.29}$$

For Δi_{in} to be zero, $G_{NFin}D_1T_s = 0$ and $G_{FNin}D_2T_s = 0$. As the duty ratios D_1 and D_2 can not be zero, the slopes G_{NFin} and G_{FNin} are zero.

For $G_{NFin} = 0$, substituting the expression of G_{NFin} from (5.1) we obtain

$$\begin{aligned} \left[L_2 + k\sqrt{L_1L_2} - D_2\left(L_1 + L_2 + 2k\sqrt{L_1L_2}\right)\right] = 0 \\ \Rightarrow D_2 = \frac{L_2 + k\sqrt{L_1L_2}}{L_1 + L_2 + 2k\sqrt{L_1L_2}}. \end{aligned} \tag{5.30}$$

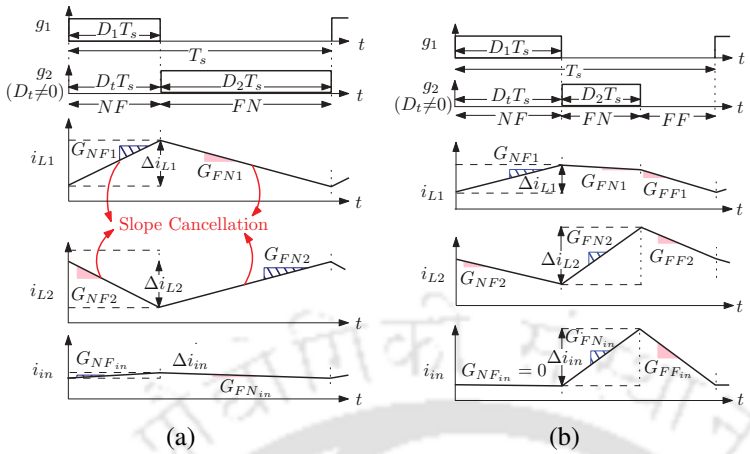


Figure 5.15: (a) Zero ripple input current for $D_1 + D_2 = 1$ when $G_{NFin} = 0$, $G_{FNin} = 0$, and (b) Ripple in input current for $D_1 + D_2 < 1$ when $G_{NFin} = 0$.

Similarly for $G_{FNin} = 0$, substituting the expression of G_{FNin} from (5.1) we obtain

$$\begin{aligned} \left[L_1 + k\sqrt{L_1L_2} - D_1\left(L_1 + L_2 + 2k\sqrt{L_1L_2}\right)\right] &= 0 \\ \Rightarrow D_1 &= \frac{L_1 + k\sqrt{L_1L_2}}{L_1 + L_2 + 2k\sqrt{L_1L_2}}. \end{aligned} \tag{5.31}$$

Adding the expression of D_1 and D_2, we have

$$\begin{aligned} D_1 + D_2 &= \frac{L_1 + k\sqrt{L_1L_2}}{L_1 + L_2 + 2k\sqrt{L_1L_2}} + \frac{L_2 + k\sqrt{L_1L_2}}{L_1 + L_2 + 2k\sqrt{L_1L_2}} \\ &= 1. \end{aligned} \tag{5.32}$$

Therefore, for absolute zero ripple input current, the sum of duty ratios is equal to 1.

For the cases when the sum of duty ratios are not equal to 1 i.e. $D_1 + D_2 <$ or > 1, the absolute zero ripple input current is not possible.

Proof of Proposed Design Method for $D_1 + D_2 = 1$

According to the proposed design method for absolute zero-ripple input current in Section 5.4.2.1, the value of gate pulse shift as presented in (5.25) is

$$\mathbf{D}_{min} = D_1. \tag{5.33}$$

The ratio of coupled inductor winding as given by (5.26) is

$$\frac{L_1}{L_2} = \left[\frac{-(r-1)k \pm \sqrt{[(r-1)k]^2 + 4r}}{2r}\right]^2. \tag{5.34}$$

The waveforms of i_{in}, i_{L1}, i_{L2} for $D_1 + D_2 = 1$ and $D_1 < D_2$ are shown in Fig. 5.15(a) for $\mathbf{D}_{min} = D_1$. From (5.26), it is the solution of a quadratic equation which is presented as

$$r\frac{L_1}{L_2} + (r-1)k\sqrt{\frac{L_1}{L_2}} - 1 = 0 \tag{5.35}$$

$$\Rightarrow \qquad r = \frac{1+k\sqrt{\frac{L_1}{L_2}}}{\frac{L_1}{L_2}+k\sqrt{\frac{L_1}{L_2}}}.$$

From Fig. 5.15(a), $D_1 < D_2$. Using (5.24),

$$\Rightarrow \quad r = \frac{1-D_1}{D_1} = \frac{1+k\sqrt{\frac{L_1}{L_2}}}{\frac{L_1}{L_2}+k\sqrt{\frac{L_1}{L_2}}} \tag{5.36}$$

$$\Rightarrow \quad D_1 = \frac{L_1+k\sqrt{L_1L_2}}{L_1+L_2+2k\sqrt{L_1L_2}}.$$

Substituting the above expression for D_1 in the expression of $G_{FN_{in}}$ given in (5.1), we obtain $G_{FN_{in}} = 0$.

Now we have $D_1 + D_2 = 1$. If $D_1 + D_2 = 1$, then $D_2 = 1 - D_1$. The expression of D_2 obtained is

$$D_2 = \frac{L_2 + k\sqrt{L_1L_2}}{L_1 + L_2 + 2k\sqrt{L_1L_2}}. \tag{5.37}$$

Substituting the above expression for D_2 in the expression of $G_{NF_{in}}$ given in (5.1), we obtain $G_{NF_{in}} = 0$. Thus, we obtain–

$$\boxed{\begin{aligned} &G_{NF_{in}} = 0 \text{ and } G_{FN_{in}} = 0 \quad : D_1 + D_2 = 1 \\ &\Delta i_{in} = G_{NFin}D_1T_s = G_{FNin}D_2T_s = 0. \end{aligned}} \tag{5.38}$$

Therefore, it is proved that for $D_1 + D_2 = 1$, the slopes of input current are zero using the proposed design method, resulting in zero ripple input current.

Proof of Proposed Design Method for $D_1 + D_2 <$ or > 1

In the cases where absolute zero ripple in input current is not possible, the value of shift in gate pulse $D_t = \mathbf{D}_{min}$ as presented in (5.27) is given by

$$\mathbf{D}_{min} = \begin{cases} D_1 \le D_t \le 1 - D_2 & : D_1 + D_2 < 1 \\ 1 - D_2 \le D_t \le D_1 & : D_1 + D_2 > 1. \end{cases} \tag{5.39}$$

The ratio of coupled inductor winding as given by (5.26) is

$$\frac{L_1}{L_2} = \left[\frac{-(r-1)k \pm \sqrt{[(r-1)k]^2 + 4r}}{2r}\right]^2. \tag{5.40}$$

The values of L_1 is obtained using (5.28) which is presented as

$$L_1 = \begin{cases} \frac{V_{o1}|I_{FN}|(1-D_1)T_s}{(1-k^2)\widehat{\Delta i_{in}}} & : D_1 \geq D_2,\ D_1 + D_2 > 1 \\ \frac{V_{o1}I_{FN}D_2T_s}{(1-k^2)\widehat{\Delta i_{in}}} & : D_1 \geq D_2,\ D_1 + D_2 < 1 \\ \frac{V_{o2}|I_{NF}|(1-D_2)T_s}{(1-k^2)\widehat{\Delta i_{in}}} & : D_1 < D_2,\ D_1 + D_2 > 1 \\ \frac{V_{o2}I_{NF}D_1T_s}{(1-k^2)\widehat{\Delta i_{in}}} & : D_1 < D_2,\ D_1 + D_2 < 1. \end{cases} \tag{5.41}$$

The waveforms of i_{in}, i_{L1}, i_{L2} for $D_1 + D_2 < 1$ and $D_1 > D_2$ is shown in Fig. 5.15(b) for $\mathbf{D}_{min} = D_1$. Using (5.35), the value of r obtained is

$$r = \frac{1 + k\sqrt{\frac{L_1}{L_2}}}{\frac{L_1}{L_2} + k\sqrt{\frac{L_1}{L_2}}}. \tag{5.42}$$

From Fig. 5.15(b), $D_1 > D_2$. Using (5.24),

$$\begin{aligned} \Rightarrow \quad r &= \frac{D_2}{1-D_2} = \frac{1+k\sqrt{\frac{L_1}{L_2}}}{\frac{L_1}{L_2}+k\sqrt{\frac{L_1}{L_2}}} \\ \Rightarrow \quad D_2 &= \frac{L_2+k\sqrt{L_1L_2}}{L_1+L_2+2k\sqrt{L_1L_2}}. \end{aligned} \tag{5.43}$$

Substituting the above expression for D_2 in the expression of $G_{NF_{in}}$ given in (5.1), we obtain $G_{NF_{in}} = 0$. Now from the example taken in Fig. 5.15(b), we have $D_1 + D_2 < 1$.

$$\begin{aligned} \text{If} \ \ D_1 + D_2 < 1 \Rightarrow D_1 < 1 - D_2. \\ \text{let} \ \ D_1 = 1 - D_2 - \delta. \end{aligned} \tag{5.44}$$

where, $\delta = 1 - D_1 - D_2$. Substituting (5.43) in above,

$$D_1 = \frac{L_1 + k\sqrt{L_1L_2}}{L_1 + L_2 + 2k\sqrt{L_1L_2}} - \delta. \tag{5.45}$$

Substituting the above expression for D_1 in the expression of $G_{FN_{in}}$ given in (5.1), we obtain

$$G_{FN_{in}} = \frac{\delta V_{o1}\left(L_1 + L_2 + 2k\sqrt{L_1L_2}\right)}{(1-k^2)L_1L_2} \Rightarrow G_{FN_{in}} > 0. \tag{5.46}$$

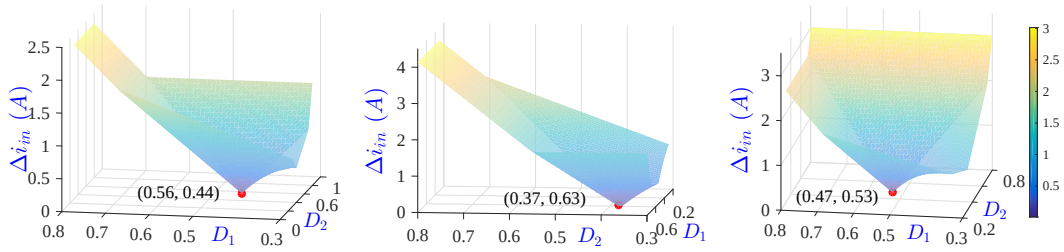


Figure 5.16: Input current ripples versus duty ratios plot for (a) $L_1 = 100\ \mu H$, $L_2 = 155\ \mu H$, $k = 0.8$ (b) $L_1 = 235\ \mu H$, $L_2 = 90\ \mu H$, $k = 0.88$ and (c) $L_1 = 130\ \mu H$, $L_2 = 105\ \mu H$, $k = 0.85$.

Table 5.9: Ripples in input current Δi_{in} at proposed design method

$D_1 + D_2$	D_1, D_2	Δi_{in}
< 1	$D_1 \geq D_2$	$G_{FN_{in}} D_2 T_s = \lvert G_{FF_{in}} \rvert (1 - D_1 - D_2) T_s$
> 1		$\lvert G_{FN_{in}} \rvert (1 - D_1) T_s = G_{NN_{in}} (D_1 + D_2 - 1) T_s$
< 1	$D_1 < D_2$	$G_{NF_{in}} D_1 T_s = \lvert G_{FF_{in}} \rvert (1 - D_1 - D_2) T_s$
> 1		$\lvert G_{NF_{in}} \rvert (1 - D_2) T_s = G_{NN_{in}} (D_1 + D_2 - 1) T_s$

Therefore for $D_1 + D_2 < 1$, $D_1 > D_2$, $G_{NFin} = 0$ and $G_{FNin} > 0$. From Fig. 5.15(b), the expression of Δi_{in} is given by

$$\begin{aligned} \Delta i_{in} &= G_{FNin} D_2 T_s \\ &= \frac{V_{o1} D_2 T_s (l_r{}^2 + k l_r - D_1 (l_r{}^2 + 2 k l_r + 1))}{(1 - k^2) L_1}. \end{aligned} \tag{5.47}$$

Substituting the given value of L_1 from (5.28), we obtain

$$\boxed{\Delta i_{in} = \widehat{\Delta i_{in}}.} \tag{5.48}$$

Similar proofs can be given for other conditions of D_1, D_2. Thus, we achieve (5.49) using the proposed design method. At the proposed design method Δi_{in} is presented in Table 5.9.

$$\boxed{\begin{cases} G_{NF_{in}} = 0 & : D_1 \geq D_2 \\ G_{FN_{in}} \begin{cases} < 0 & : D_1 + D_2 > 1,\ D_1 \geq D_2 \\ > 0 & : D_1 + D_2 < 1,\ D_1 \geq D_2 \end{cases} \\ G_{FN_{in}} = 0 & : D_1 < D_2 \\ G_{NF_{in}} \begin{cases} < 0 & : D_1 + D_2 > 1,\ D_1 < D_2 \\ > 0 & : D_1 + D_2 < 1,\ D_1 < D_2 \end{cases} \end{cases}} \tag{5.49}$$

The presented analysis shows that the zero ripple input current is possible once for a given coupled inductor at $D_1 + D_2 = 1$. As the operating point deviates from $D_1 + D_2 = 1$, the ripple in input current increases. To verify this, the curves of input current ripples versus the duty ratios are shown in Fig. 5.16 for three different values of the coupled inductor.

5.4.2.3 Inductor Current Ripples at Proposed Design Method

According to the proposed design method, zero input current ripples depend on $\frac{L_1}{L_2}$. It does not depend on the absolute values of L_1, L_2. Therefore, by designing the proper values of L_1, L_2 at the proposed zero ripple input current point, we can obtain an optimal design method for achieving zero input current ripples and minimized inductor current ripples simultaneously. The absolute values of the inductor can be formulated depending on the allowed maximum specified ripples in inductor currents for a given k. If both Δi_{L1} and Δi_{L2} are specified, L_1 and L_2 is designed based on the minimum Δi_{L1} or Δi_{L2}. If the values of Δi_{L1} is minimum, L_1 at zero ripple point is given by–

$$L_1 = \frac{V_{in} T_s}{(1-k^2)\Delta i_{L1}} \left[\frac{-k^2 r l_r^2 + (1-r)klr + 1}{r l_r^2 + 2krl_r + r} \right]. \tag{5.50}$$

Similarly, if specified Δi_{L2} is minimum, L_2 can be designed using–

$$L_2 = \frac{V_{in} T_s}{(1-k^2)\Delta i_{L2}} \left[\frac{r l_r^2 + (r-1)klr - k^2}{l_r^2 + 2kl_r + 1} \right]. \tag{5.51}$$

A similar analysis is true when approximately zero ripples are obtained.

5.4.3 Practical Design Considerations in the Proposed Design Method

This section shows the effect of parameter variations on the proposed design method of the CI-SIDO boost converter.

5.4.3.1 Effect of Variations in Input Voltage

Once the converter is designed at zero ripple input current for the given voltages V_{o1}, V_{o2}, V_{in}, and $\widehat{\Delta i_{in}}$, the coupled inductor parameters get fixed. After the design, if there are variation in the input

voltages i.e. $V_{in} \pm \Delta V_{in}$, the duty ratios of the converter changes as

$$\implies D_1^{'} = D_1 \mp \frac{\Delta V_{in}}{V_{o1}}, \quad D_2^{'} = D_2 \mp \frac{\Delta V_{in}}{V_{o2}}. \tag{5.52}$$

With the change in input voltage, the converter no longer has the zero ripple input current. However, the converter still operates with an input ripple less than the maximum specified limit. The allowed variation in input voltage such that the input current ripple is within the specified limit is given as –

$$-\frac{\widehat{\Delta i_{in}}}{X \max\{D_1, D_2\}}\} \leq \Delta V_{in} \leq \frac{\widehat{\Delta i_{in}}}{X \max\{(1-D_1),(1-D_2)\}}$$
$$\text{where } X = \frac{(L_1 + L_2 + 2k\sqrt{L_1 L_2})T_s}{(1-k^2)L_1 L_2}. \tag{5.53}$$

5.4.3.2 Effect of Variation in Coupled Inductor Parameters

Once the converter is designed for zero ripple input current, the coupled inductor parameters L_1, L_2, k are fixed. During the operation of the converter even if the coupled inductor parameters change due to any disturbances, the converter may get shifted from zero-ripple point i.e. $D_1 + D_2$ may become $>$ or <1, however, the converter still operates within $\widehat{\Delta i_{in}}$. For example, suppose $D_1 + D_2 = 1$ changes to $D_1 + D_2 < 1$ as shown in Fig. 5.15(b) for $D_1 > D_2$. The allowed deviation from zero-ripple condition such that the input current ripple is within specified limit is given as –

$$\delta \leq \frac{\widehat{\Delta i_{in}}(1-k^2)L_1 L_2}{V_{o1}\left(L_2 + k\sqrt{L_1 L_2}\right)T_s}. \tag{5.54}$$

The allowed deviations for other cases similarly follows.

5.4.3.3 Effect of Closed-Loop Control

The closed-loop control of the converter is required to regulate the output voltages against line and load variations. To design controllers, power electronic converters are linearized using state space averaging methods [73,74]. The generalized state space averaged equations for CI-SIDO boost are given by (5.55) where A_{av}, B_{av}, C_{av}, D_{av} are the analytical averaged matrix for different states of the converter depending on the ON-OFF states of MOSFETs and diodes, $\tilde{x} = [\tilde{i}_{L1}\ \tilde{v}_{o1}\ \tilde{i}_{L2}\ \tilde{v}_{o2}]^T$,

$\tilde{u} = [\tilde{v}_{in}\ \tilde{i}_{o1}\ \tilde{i}_{o2}\ \tilde{d}_1\ \tilde{d}_2]^T$, $\tilde{y} = [\tilde{v}_{o1}\ \tilde{v}_{o2}\ \tilde{i}_{in}]^T$ such that i_{L1}, i_{L2}, v_{o1}, v_{o2}, i_{o1}, i_{o2}, v_{in}, d_1, d_2 are the averaged values of i_{L1}, i_{L2}, V_{o1}, V_{o2}, i_{o1}, i_{o2}, V_{in}, D_1, D_2 over T_s, respectively. The corresponding tilde values are the perturbations over the averaged values.

$$\frac{d\tilde{x}}{dt} = A_{av}\tilde{x} + B_{av}\tilde{u}, \tag{5.55a}$$

$$\tilde{y} = C_{av}\tilde{x} + D_{av}\tilde{u} \tag{5.55b}$$

As per [74], the state transition matrices are invariant to the shift of gate pulse. The same state-space averaging can be used to obtain closed-loop control in our proposed design of the CI-SIDO boost converter. Therefore, the approximately zero ripple conditions are unaffected by closed-loop control.

5.4.4 Experimental Verifications

This section provides the practical design method of the coupled inductor. The section also presents the results for verifying the proposed design method. Besides, the usability of the proposed design method is illustrated by showing several solved examples.

Table 5.10: Converter Parameters

V_{in}	15 V	T_s 10 μs	C_1, C_2 100 μF
R_1, R_2	20.5 Ω, 14.5 Ω	MOSFET	IRF740
		Diode	MUR1560

5.4.4.1 Practical Design of Coupled Inductor

The experiments in this chapter is done for three coupled inductors with values $L_1 = 100\ \mu H$, $L_2 = 155\ \mu H$, $k = 0.8$, and $L_1 = 235\ \mu H$, $L_2 = 90\ \mu H$, $k = 0.88$, and $L_1 = 125\ \mu H$, $L_2 = 100\ \mu H$, $k = 0.60$. The inductor design is done with the assumption of 10 A peak inductor current with the ripple $\Delta i_{Lw} = 3\ A$ and $T_s = 10\ \mu s$. The available ferrite core for the inductor is B66387G0000X127 (E 65/32/27) and the copper wire used is 16 SWG. The approximate number of turns obtained is 5, 8, and 12, 5, and 10, 7, respectively. The coupling coefficient is varied by changing the air gap between the E cores and by a relative shifting of windings locations on the limbs of the core. The approximate air gap between the cores is 0.1 mm, 0.06 mm, 0.08 mm, respectively. Furthermore, to avoid tight coupling, the two winding are placed on two different limbs. The windings are done such that the flux

due to two windings oppose each other.

5.4.4.2 Verification of the Proposed Method

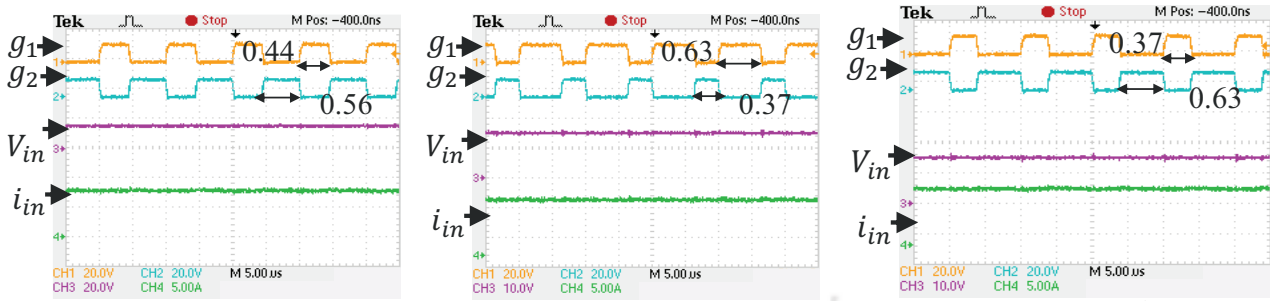
To verify the design method proposed in Section 5.4.2.1 to achieve Δi_{in} as either zero or < desired $\widehat{\Delta i_{in}}$, the CI-SIDO boost converter shown in Fig. 3.4(b) is designed and experimentally tested for different values of V_{in}, V_{o1}, V_{o2}. Example 1 is presented for designing the converter with zero-ripple Δi_{in} at $D_1 + D_2 = 1$. Example 2 presents the converter design for approximately zero-ripple Δi_{in} when absolute zero ripple i_{in} is not possible for $D_1 + D_2 > 1$.

Example 1: CI-SIDO boost converter has to maintain output voltages of $V_{o1} = 26.78\ V$ and $V_{o2} = 34.0\ V$. Design the converter such that zero input current ripple is achieved by appropriately choosing V_{in}.

Solution: For $V_{o1} = 26.78\ V$ and $V_{o2} = 34.0\ V$, the duty ratios obtained is $D_1 = 1 - \frac{V_{in}}{26.78}$, $D_2 = 1 - \frac{V_{in}}{34.0}$. For zero-ripple input current, $D_1 + D_2 = 1$, so, V_{in} obtained is 15.0 V. The duty ratios are $D_1 = 0.44$ and $D_2 = 0.56$. From (5.27) for $D_1 + D_2 = 1$, shift $D_t = D_1 = 0.44$. For zero ripple input current, $r = 1.27$ using (5.24). For $k = 0.8$, the values of $\frac{L_1}{L_2}$ are 0.65 and 0.98. Therefore, for $V_{in} = 15.0\ V$ and $\frac{L_1}{L_2} = 0.65$, or 0.98, the zero ripple input current is obtained. This result is shown in Fig. 5.17(a).

Similar to Example 1, the CI-SIDO boost converter is designed for 2 more different set of values for V_{in}, V_{o1}, V_{o2} and then experimentally verified. The first two set of values taken are $V_{o1} = 40.5\ V$, $V_{o2} = 23.81\ V$ and $V_{in} = 15.0\ V$; $V_{o1} = 23.81\ V$, $V_{o2} = 40.5\ V$ and $V_{in} = 15.0\ V$. In all these two sets, $D_1 + D_2 = 1$, so zero-ripple input current is possible. The converter is tested experimentally with the values of L_1, L_2, k and D_t, obtained by following the proposed design method in Section 5.4.2.1 and its use as presented in Example 1. The experimentally obtained g_1, g_2 and i_{in} are shown in Fig. 5.17. The design values are mentioned in the caption of sub-figures 5.17 (b), (c) and load resistances used are given in Table 5.10. We can observe in Fig. 5.17 that almost zero-ripple i_{in} is achieved.

Example 2: CI-SIDO boost converter needs to be designed with $V_{in} = 15.0\ V$, $V_{o1} = 23.8\ V$, $V_{o2} = 37.5\ V$ and switching frequency 100 kHz. The maximum limit specified on input current ripple, $\widehat{\Delta i_{in}}$ is 0.40 A. Design the converter by choosing proper values of L_1, L_2, k and shift D_t.



L_1= 100 µH, L_2= 155 µH
k=0.80, D_t=0.44

(a)

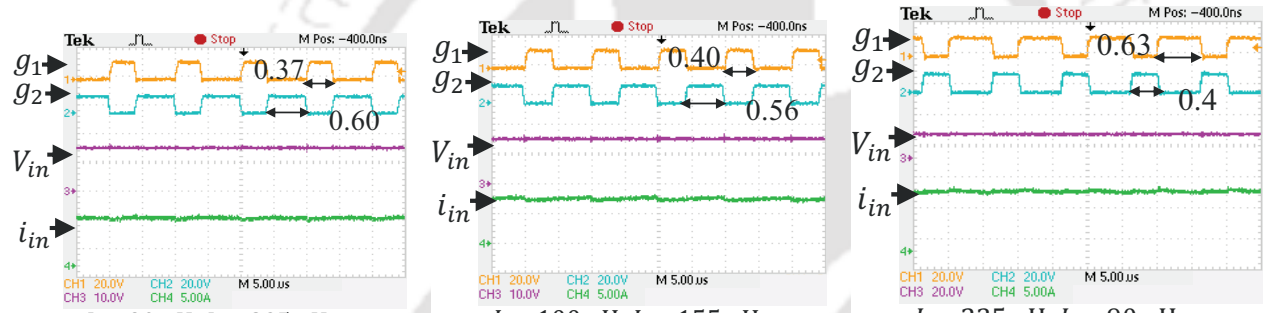
L_1= 235 µH, L_2= 90 µH
k=0.88, D_t=0.63

(b)

L_1= 90 µH, L_2= 235 µH
k=0.88, D_t=0.37

(c)

Figure 5.17: Zero ripple i_{in} for different D_1, D_2 such that $D_1 + D_2 = 1$. The analytical calculations show that for these coupled inductor parameters, duty ratios, and shifts, $\Delta i_{in} = 0$ is expected.



L_1= 90 µH, L_2= 235 µH
k=0.88, D_t=0.37

(a)

L_1= 100 µH, L_2= 155 µH
k=0.80, D_t=0.40

(b)

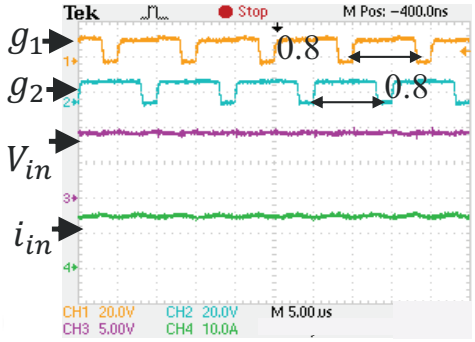
L_1= 235 µH, L_2= 90 µH
k=0.88, D_t=0.63

(c)

Figure 5.18: Approximately zero ripple i_{in} for different D_1, D_2 such that $D_1 + D_2 \gtrless 1$. As $D_1 + D_2 \neq 1$, absolute zero ripple input current is not possible. Approximatley zero ripple input current is expected.

Solution: Here, $D_1 = 0.37$, $D_2 = 0.60$. So, $D_1 < D_2$ and $D_1 + D_2 < 1$. Using (5.24), $r = 1.7$. If $k = 0.88$, $\frac{L_1}{L_2} = 0.38$ and $\frac{L_1}{L_2} = 0.94$ using (5.26). Using (5.28), the values of L_1 are 90.0 μH and 478.62 μH. The respective values of L_2 are 235.0 μH and 509.17 μH. Using (5.27), the value of shift $\mathbf{D}_{min}$ is $0.37 \leq D_t \leq 0.40$. The experimental result for $k = 0.88$, $\frac{L_1}{L_2} = 0.375$ is shown in Fig. 5.18(a).

Another two set of values taken are $V_{o1} = 25.0\ V$, $V_{o2} = 34.10\ V$ and $V_{in} = 15.0\ V$; $V_{o1} = 40.54\ V$, $V_{o2} = 25.0\ V$ and $V_{in} = 15.0\ V$. Note that here $D_1 + D_2 <$ or > 1. So, approximately zero ripple i_{in} where $\widehat{\Delta i_{in}} \leq 0.40\ A$ can be achieved. Again following the proposed design method in Section 5.4.2.1 and Example 2, the values of L_1, L_2, k and D_t are obtained. The experimental results of i_{in} reported in Fig. 5.18 (b), (c) show that approximately zero ripple i_{in} is achieved for all three cases. The experimental details of all 6 sets of values for V_{in}, V_{o1}, V_{o2} are tabulated in Table 5.11. A slight



L_1= 125 µH, L_2= 100 µH
k=0.60, D_t=0.50

Figure 5.19: Experimental result for $D_1 + D_2 > 1.5$.

Table 5.11: Input current ripple Δi_{in} for Experimental Values

Sl. No.	Voltages			Δi_{in}	Details of proposed method			
	V_{in} (V)	V_{o1} (V)	V_{o2} (V)	(A) $\widehat{\Delta i_{in}}$=0.4 A	L_1 (μH)	L_2 (μH)	k	$\mathbf{D}_{min}$
1	15	25.5	32.5	≈ 0	100	155	0.8	0.44
2	15	38.5	22.2	≈ 0	235	90	0.88	0.63
3	15	22.8	38.3	≈ 0	90	235	0.88	0.37
4	15	23.5	31.8	< $\widehat{\Delta i_{in}}$	100	155	0.8	0.4
5	15	37.8	22.5	< $\widehat{\Delta i_{in}}$	235	90	0.88	0.63
6	15	22.8	37.5	< $\widehat{\Delta i_{in}}$	90	235	0.88	0.37

mismatch in experiments is due to the non-idealities present in the circuit.

The experimental result when $D_1+D_2 > 1.5$ is shown in Fig. 5.19. The result is for $D_1 = D_2 = 0.8$, with $V_{in} = 9\ V$, $I_{in} = 14.5\ A$, $R_1 = 24.5\ \Omega$, $R_2 = 23\ \Omega$. We observe that approximately zero ripple input current is obtained.

From the above we observe that zero ripple i_{in} is obtained for a specific set of parameters L_1, L_2, k and D_t, determined using the proposed design method, for a given V_{in}, V_{o1}, V_{o2} and $\widehat{\Delta i_{in}}$. If value of any one of these parameters is changed, zero ripple i_{in} cannot be achieved. For example, in Fig. 5.20(a), zero ripple is achieved for $L_1 = 100\ \mu H$, $L_2 = 155\ \mu H$, $k = 0.8$, $D_t = D_1$ for given $D_1 = 0.44$, $D_2 = 0.56$. If only D_t is changed to 0 keeping rest of the values unchanged, Δi_{in} increases to 5.36 A, as seen in experimental results shown in Fig. 5.20(b). If the windings of coupled inductor are interchanged i.e. $L_1 = 155\ \mu H$, $L_2 = 100\ \mu H$ keeping rest of the values unchanged i.e. $k = 0.8$, $D_t = D_1$, Δi_{in} increases to 1.68 A, shown in experimental results of Fig. 5.20(c).

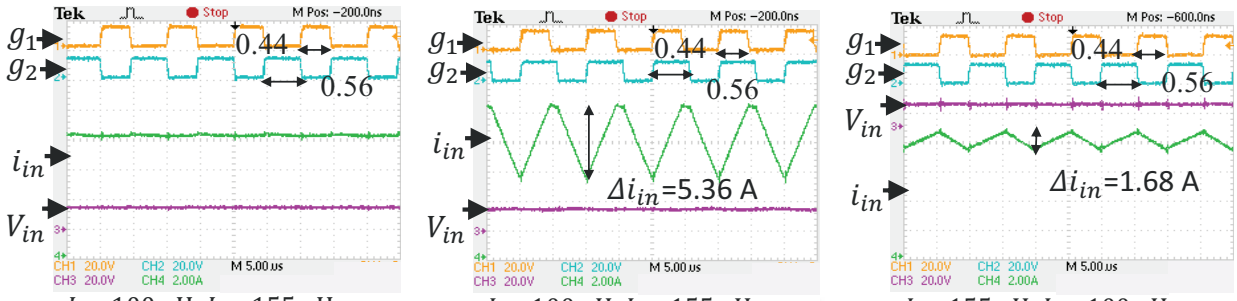
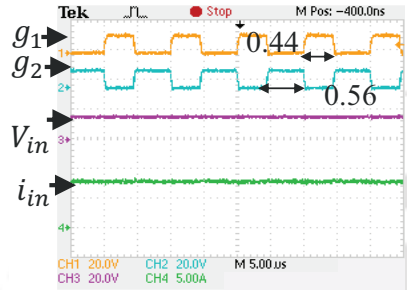


Figure 5.20: Comparison: (a) zero ripple, (b) $\Delta i_{in} = 5.36\ A$ when D_t is changed, and (c) $\Delta i_{in} = 1.68\ A$ when L_1, L_2 changed.

The proposed design method does not depend on the type of MOSFETs and diodes selected. To show this, LTspice simulations are done with SiC MOSFETs and SiC diodes. The spice model of SiC MOSFETs and diodes used are C2M0025120D and C6D04065A. To compare the simulation and experimental results, the simulations are done with the same parameters as the experiment. The simulations with SiC switches show that the absolute and approximate zero ripples are obtained for SiC devices also. The simulation results with SiC switches for zero ripple i_{in} for different D_1, D_2 such that $D_1 + D_2 = 1$ is presented in Fig. 5.21. The simulations corresponding to each experimental result are performed using the same system to verify the effectiveness of the proposed method. The LTspice simulation results for zero ripple input current are presented in Fig. 5.21. We can observe that the simulation and experimental results match.

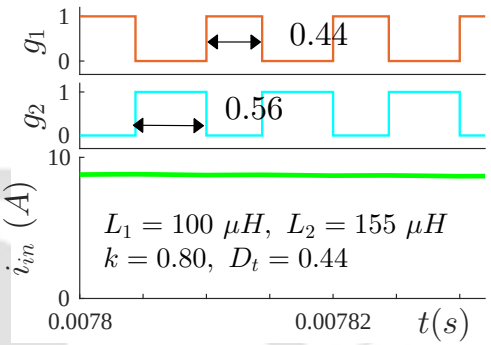
We observe that to obtain zero ripple i_{in} for $D_1 + D_2 = 1$, the ratio $\frac{L_1}{L_2}$ is only important and there is no restriction on the choice of L_1, L_2. However, for $D_1 + D_2 <$ or > 1 when maximum specified current limit is calculated, the choice of L_1, L_2 is also required in addition to the ratio $\frac{L_1}{L_2}$.

The existing ripple reduction methods of the DC-DC converters are implemented in the CI-SIDO converters, and the input current ripples are compared in Table 5.12. The converter parameters are taken from Example 1, i.e., $V_{in} = 15\ V$, $V_{o1} = 23.81\ V$, $V_{o2} = 40.5\ V$, $D_1 = 0.44$, $D_2 = 0.56$. The comparisons show that our proposed method achieves zero ripple input current in the CI-SIDO boost converter without any additional circuit elements.

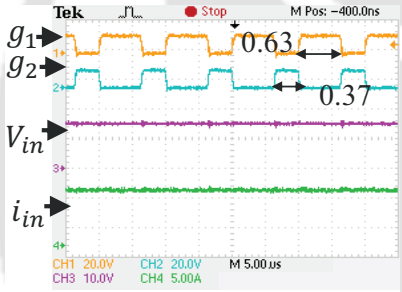


L_1= 100 µH, L_2= 155 µH
k=0.80, D_t=0.44

(a) Experimental

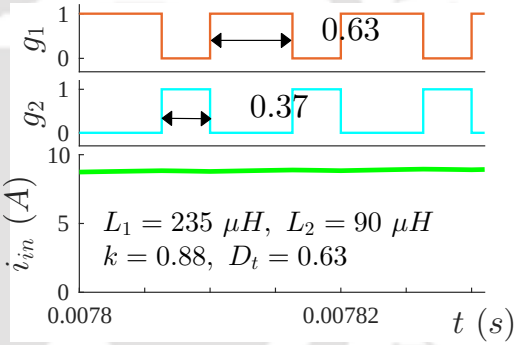


(b) Simulation

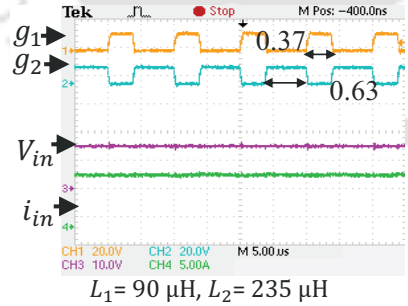


L_1= 235 µH, L_2= 90 µH
k=0.88, D_t=0.63

(c) Experimental

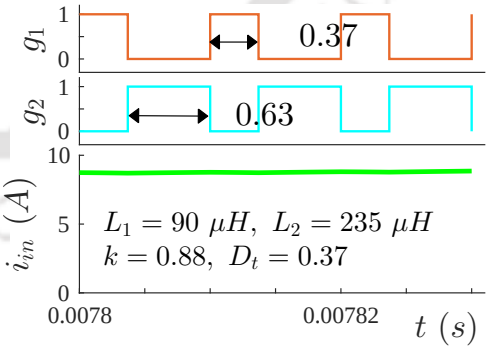


(d) Simulation



L_1= 90 µH, L_2= 235 µH
k=0.88, D_t=0.37

(e) Experimental



(f) Simulation

Figure 5.21: Comparisons of experimental and simulation results for zero ripple i_{in} for different D_1, D_2 such that $D_1 + D_2 = 1$.

Table 5.12: Comparisons of the proposed method with the already existing methods

References	[25]	[23]	[24]	this analysis
Condition for zero ripple	$D_2 = pD_1$, $L_2 = pL_1$, $k = 0$	Auxiliary inductance equal to mutual inductance of main inductors	Sum of two auxiliary inductances equal to mutual inductance of main inductors	$D_1 + D_2 = 1$
Inductor used	$L_1 = 100\ \mu H$, $L_2 = 127.3\ \mu H$	$L_1 = L_2 = 100\ \mu H$, $k = 0.74$, $L_{auxi} = 74\ \mu H$	$L_1 = L_2 = 100\ \mu H$, $k = 0.9$, $L_{auxi1} = 10\ \mu H$, $L_{auxi2} = 10.46\ \mu H$	$\frac{L_1}{L_2} = 0.65$ or 0.98, $k = 0.8$
Input current ripples	$0.66\ A$	$1.16\ A$	$0.24\ A$	$0.05\ A \approx 0$
Limitations of the method	Not suitable for dual output converters	Additional L, C in auxiliary circuit. Auxiliary circuit repeats for each output	Additional coupled inductor, L, C in auxiliary circuit. Auxiliary circuit repeats for each output	-

5.5 Summary of the Chapter

The findings of this chapter are as follows–

(i) All the feasible input current slope conditions are identified and presented in the form of 16 sectors and sub-sectors.

(ii) The range of gate pulse shift is obtained where input current ripples are minimum for all possible input, output voltage, and coupled inductor parameters.

(iii) A detailed analysis of CI-SIDO boost converter to achieve maximum ripple cancellation in input current is performed under continuous conduction mode (CCM).

(iv) Among all sub-sectors, those sub-sectors are identified where maximum ripple cancellation takes place.

(v) Based on these analyses, the thesis proposes a method to design the inductors of CI-SIDO boost such that the ripple in input current is less than the specified value.

(vi) The conditions of CI-SIDO boost converter are found where zero ripple input current is possible and where absolute zero ripples in input current are not possible.

(vii) A method is proposed to design the CI-SIDO boost converter with the zero ripple input current.

In case of operating conditions where absolute zero ripples in input current are not possible, a

design method is proposed such that the input current ripple remains within a desired specified limit.

(viii) Analytical proofs of the proposed design method are presented.

(ix) The effect of variations in input voltage, coupled inductor parameters on the proposed design method is introduced. A brief discussion on closed-loop control of the converter is also presented.

(x) The proposed design methods are verified by experiments using a laboratory prototype.

(xi) The proposed design methods are explained using practical design examples.

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6

Effect of Gate Pulse Shift on other Circuit Variables of CI-SIDO Boost

Contents

6.1 Introduction

[1] The CI-SIDO converters have two MOSFETs with two gate pulses. The shifting of gate pulses in CI-SIDO converters are required for inductors and input current ripple minimization. The ripple minimization reduces the capacitance value of input filter. Also, the device ratings of MOSFETs and diodes are reduced. The shift of gate pulses changes the pattern of inductor currents, which can change the average value of inductor currents. The change in average values of inductor currents can change average values of input currents. The effect of shifting gate pulses on the average values of inductor current and input current are not investigated till now. This chapter finds the effect of shifting gate pulses on the average currents of CI-SIDO boost converter.

It is required to observe if the reduction of ripples in inductor current has any effect on output voltage ripples or not. The value of output voltage ripples is required to select the suitable value of the capacitor. If the output voltage ripples are reduced, the value of the capacitor reduces, thus increasing the power density of the converter.

6.2 Effect of Gate Pulse Shift on Average of Inductor Current

For the ideal CI-SIDO boost converter, the input and output powers are equal, as presented in (6.1).

$$V_{o1}I_{o1} + V_{o2}I_{o2} = V_{in}I_{in} \tag{6.1}$$

For CI-SIDO boost, the relation between output and input current is -

$$I_{o1} = (1 - D_1)I_{L1}, \tag{6.2a}$$

$$I_{o2} = (1 - D_2)I_{L2} \tag{6.2b}$$

So, using (2.59), (6.1) and (6.2),

$$I_{in} = I_{L1} + I_{L2} \tag{6.3}$$

[1]Major part of this chapter is reproduced from my publications: (i) Nupur and S. Nath, "Effect of Shifting Gate Pulse on Output Voltage Ripple in Coupled SIDO Boost Converter," in *Proc. Calcutta Conf.*, Feb. 2020, pp. 391-395. (ii) Nupur and S. Nath, "Effect of Shifting Gate Pulse on Average Currents in Coupled SIDO Boost Converter," in *Proc. 9th Power India Int. Conf.*, Feb. 2020, pp. 1-6.

From (6.3), we can conclude that if I_{L1} is reduced, I_{L2} increases to keep I_{in} same. The inductor, MOSFET, diode currents of CI-SIDO boost converter, is related as–

$$I_{L1} = I_{t1} + I_{d1}, \tag{6.4a}$$

$$I_{L2} = I_{t2} + I_{d2} \tag{6.4b}$$

It is also observed that the average value of diode currents is related to load currents as–

$$I_{d1} = I_{o1}, \tag{6.5a}$$

$$I_{d2} = I_{o2} \tag{6.5b}$$

6.2.1 Analysis of Effect of Gate Pulse Shift on Average Inductor Currents

As the shifting is done, the loads are not changed. So, (6.5) is valid for all values of D_t. The pattern of inductor currents depend on the values of output voltages, input voltage and coupled inductor parameters. The analysis is done such that the shifting is at starting and ending of range $\mathbf{D}_{min}$. In Fig. 6.1, the current pattern is shown for $G_{NN1} > 0$, $G_{NF1} > 0$, $G_{FN1} > 0$, $G_{FF1} < 0$, $G_{NN2} > 0$, $G_{NF2} > 0$, $G_{FN2} > 0$, $G_{FF2} < 0$. The value of $\mathbf{D}_{min}$ for this case is presented in Table 4.7. Firstly, g_2 is shifted by $(D_1 + \underline{D_{PP1}})$ as shown in Fig. 6.1(a). The waveforms of i_{L1} and i_{L2} are shown with corresponding MOSFETs and diodes currents. Then g_2 is shifted by $(D_1 + \overline{D_{PP1}})$ as shown in Fig. 6.1(b). The waveforms are denoted by corresponding dashed value. Using (6.5), $I_{d1} = I_{d1}^{'}$ and $I_{d2} = I_{d2}^{'}$. The areas which are equal are represented by coloured shaded areas as shown in Fig. 6.1. From Fig. 6.1 and the slope conditions taken, we obtain $i_{L1}(0) < i_{L1}(t_2)$. Also, from (6.5), we obtain (6.6).

$$i_{L1}(t_2)(\underline{D_{PP1}} + D_2)T_s + i_{L1}(0)(1 - D_1 - D_2 - \underline{D_{PP1}})T_s = i_{L1}^{'}(0)(1 - D_1)T_s \tag{6.6a}$$

$$\implies i_{L1}(0) < i_{L1}^{'}(0) < i_{L1}(t_2) \tag{6.6b}$$

From (6.6), we obtain –

$$i_{L1}(0) < i_{L1}^{'}(0) \implies I_{t1} < I_{t1}^{'} \tag{6.7}$$

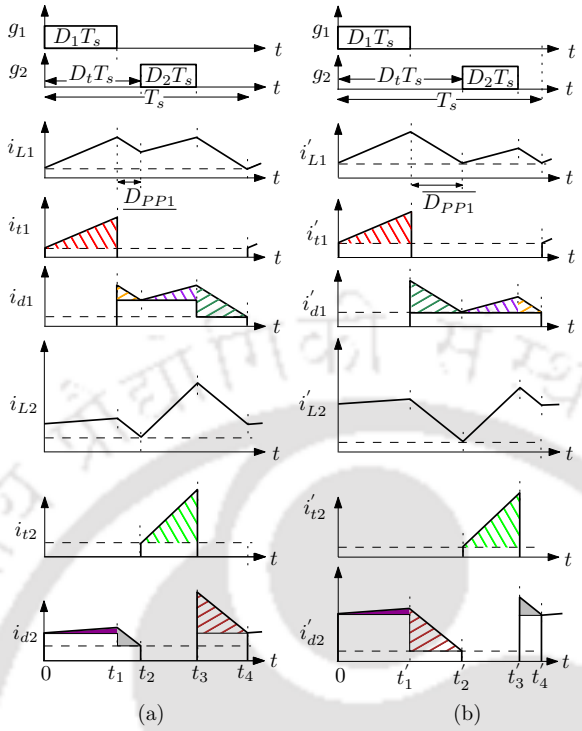


Figure 6.1: Change in average value of inductor current as gate pulse is shifted for $D_1 + D_2 < 1$. Slope condition is $G_{NN1} > 0$, $G_{NF1} > 0$, $G_{FN1} > 0$, $G_{FF1} < 0$, $G_{NN2} > 0$, $G_{NF2} > 0$, $G_{FN2} > 0$, $G_{FF2} < 0$. Dashed value is at $D_t = D_1 + \overline{D_{PP1}}$.

From (6.4) and (6.7), we obtain $I_{L1} < I'_{L1}$. Similarly, for i_{L2}, the equations obtained are presented in (6.8).

$$i_{L2}(t_2)(1 - D_2)T_s + [i_{L2}(0) - i_{L2}(t_2)](1 - D_2 - \underline{D_{PP1}})T_s \tag{6.8a}$$

$$= i'_{L2}(t'_2)(1 - D_2)T_s + [i'_{L2}(0) - i'_{L2}(t'_2)](D_1 + \underline{D_{PP1}})T_s \tag{6.8b}$$

Rearranging (6.8), we obtain (6.9).

$$[i_{L2}(t_2) - i'_{L2}(t'_2)](1 - D_2)T_s = [i'_{L2}(0) - i'_{L2}(t'_2)](D_1 + \underline{D_{PP1}})T_s - [i_{L2}(0) - i_{L2}(t_2)](D_1 + \overline{D_{PP1}})T_s \tag{6.9}$$

Solving the right side of (6.9), we obtain (6.10) which is positive.

$$D_1 T_s(\overline{D_{PP1}} - \underline{D_{PP1}})T_s(G_{NF2} + |G_{FF2}|) \tag{6.10}$$

From (6.9), (6.10) and Fig. 6.1, we obtain (6.11).

$$i_{L2}(t_2) > i'_{L2}(t'_2) \implies I_{t2} > I'_{t2} \implies I_{L2} > I'_{L2} \tag{6.11}$$

From (6.7) and (6.11), it is observed that as shifting is done, I_{L1} increases and I_{L2} decreases such that I_{in} remains same, as shown in (6.3). Similar analysis is done for different slope conditions and duty ratios, as shown in Fig. 6.2. The relations obtained from Fig. 6.2(a) are presented in (6.12)-(6.13).

$$i_{L1}(t_1) > i_{L1}(t_2) > i_{L1}(0) \tag{6.12a}$$

$$i'_{L1}(t'_1) > i'_{L1}(t'_2) > i'_{L1}(0) \tag{6.12b}$$

$$\begin{aligned} &i_{L1}(0)(1-D_1)T_s + [i_{L1}(t_2) - i_{L1}(0)]D_2T_s \\ &= i'_{L1}(0)(1-D_1)T_s + [i'_{L1}(t'_2) - i'_{L1}(0)](1-D_1-D_2)T_s \end{aligned} \tag{6.13}$$

Rearranging (6.13), the result obtained is (6.14).

$$(i_{L1}(0) - i'_{L1}(0))(1-D_1) = [i'_{L1}(t'_2) - i'_{L1}(0)](1-D_1-D_2) - [i_{L1}(t_2) - i_{L1}(0)]D_2 \tag{6.14a}$$

$$= (|G_{FN1}| - |G_{FF1}|)D_2(1-D_1-D_2) \tag{6.14b}$$

As $|G_{FFw}| > |G_{FNw}|$ in this case, $i'_{L1}(0) > i_{L1}(0)$ and $I'_{t1} > I_{t1}$. Hence, $I_{L1} < I'_{L1}$.

Similarly, equating the areas of i_{d2} and i'_{d2}, the equations obtained are presented in (6.15).

$$i_{L2}(t_1) > i_{L2}(t_2) > i_{L2}(0) \tag{6.15a}$$

$$i'_{L2}(t'_1) > i'_{L2}(t'_2) > i'_{L2}(0) \tag{6.15b}$$

$$i_{L2}(0)(1-D_2)T_s = i'_{L2}(0)D_1T_s + i'_{L2}(t'_2)(1-D_1-D_2)T_s \tag{6.15c}$$

From (6.15), the relation obtained is presented in (6.16).

$$i'_{L2}(t'_2) > i_{L2}(0) > i'_{L2}(0) \tag{6.16a}$$

$$i_{L2}(0) < i_{L2}(t_2) \tag{6.16b}$$

From (6.16), it is concluded that $i'_{L2}(0) < i_{L2}(t_2)$. Hence, $I_{L2} > I'_{L2}$. Similarly, the waveforms for $D_1 + D_2 > 1$ are shown in Fig. 6.2(b). Equating the area under curves of i_{d1} and i'_{d1}, the equations

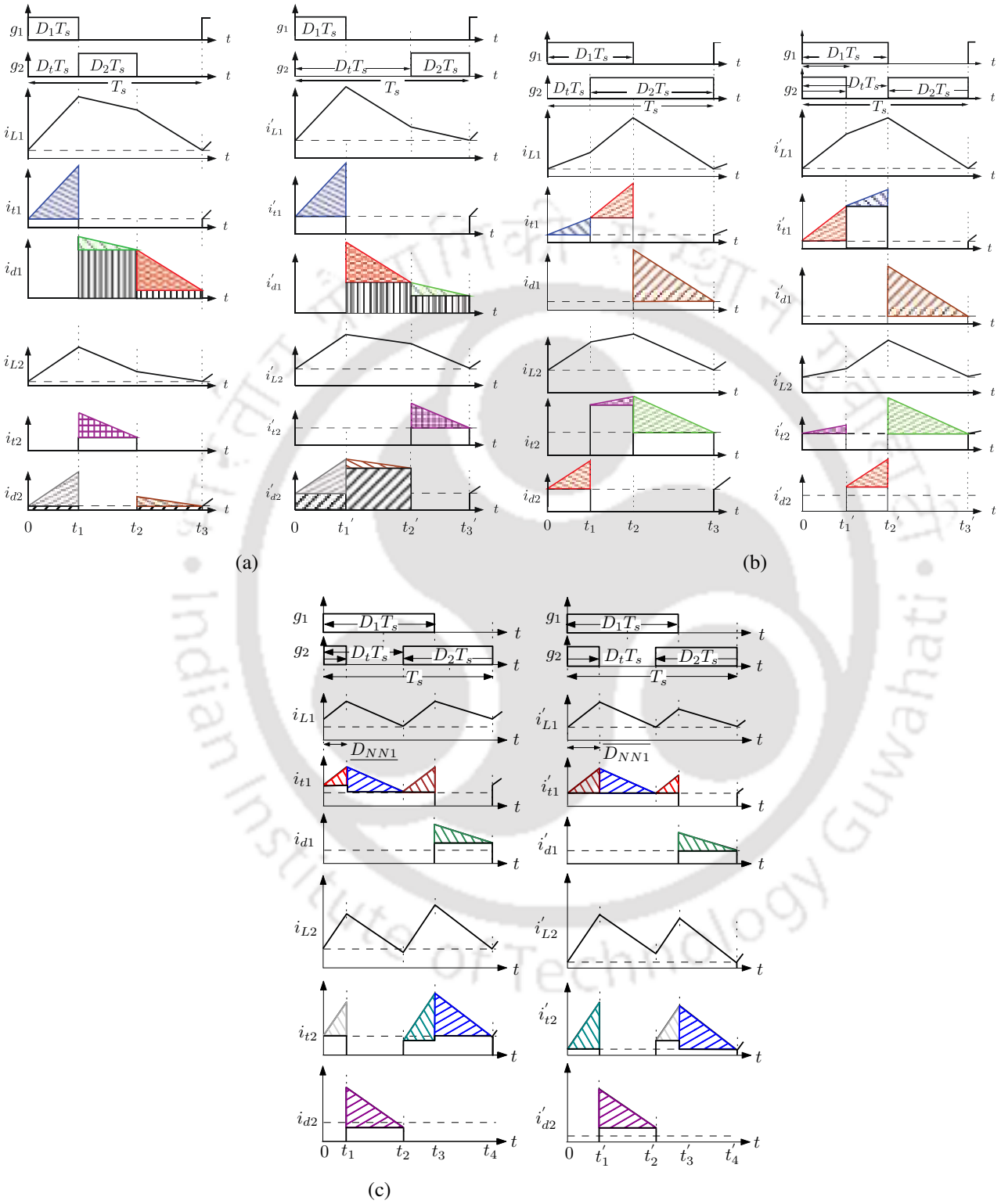


Figure 6.2: Change in average value of inductor current as gate pulse is shifted for (a) $D_1 + D_2 < 1$, (b) $D_1 + D_2 > 1$ where the slope condition is $G_{NN1} > 0$, $G_{NF1} > 0$, $G_{FN1} < 0$, $G_{FF1} < 0$, $G_{NN2} > 0$, $G_{NF2} > 0$, $G_{FN2} < 0$, $G_{FF2} < 0$, and (c) $D_1 + D_2 > 1$ where the slope condition is $G_{NN1} > 0$, $G_{NF1} < 0$, $G_{FN1} < 0$, $G_{FF1} < 0$, $G_{NN2} > 0$, $G_{NF2} < 0$, $G_{FN2} < 0$, $G_{FF2} < 0$.

obtained are presented in (6.17).

$$i_{L1}(t_2) > i_{L1}(t_1) > i_{L1}(0) \tag{6.17a}$$

$$i'_{L1}(t'_2) > i'_{L1}(t'_1) > i'_{L1}(0) \tag{6.17b}$$

$$i_{L1}(0)(1 - D_1)T_s = i'_{L1}(0)(1 - D_1)T_s \tag{6.17c}$$

The average values of switch currents are represented by (6.18) where γ_1 represents the common shaded areas.

$$I_{t1} = i_{L1}(0)D_1 + G_{NF1}(1 - D_2)(D_1 + D_2 - 1)T_s + \gamma_1 \tag{6.18a}$$

$$I'_{t1} = i'_{L1}(0)D_1 + G_{NN1}(1 - D_2)(D_1 + D_2 - 1)T_s + \gamma_1 \tag{6.18b}$$

$$\tag{6.18c}$$

As $G_{NN1} > G_{NF1}$, therefore, $I'_{t1} > I_{t1}$ and $I'_{L1} > I_{L1}$.

Similarly, equating the areas of i_{d2} and i'_{d2}, the equations obtained are presented in (6.19).

$$i_{L2}(t_2) > i_{L2}(t_1) > i_{L2}(0) \tag{6.19a}$$

$$i'_{L2}(t'_2) > i'_{L2}(t'_1) > i'_{L2}(0) \tag{6.19b}$$

$$i_{L2}(0)(1 - D_2)T_s = i'_{L2}(t'_1)(1 - D_2)T_s \tag{6.19c}$$

The average values of switch currents are represented by (6.20) where γ_2 represents the common shaded areas.

$$I_{t2} = i_{L2}(0)D_2 + G_{NF2}(1 - D_2)(D_1 + D_2 - 1)T_s + \gamma_2 \tag{6.20a}$$

$$I'_{t2} = i'_{L2}(0)D_2 + \gamma_2 \tag{6.20b}$$

As $G_{NF2} > 0$, therefore, $I_{t2}^{'} < I_{t2}$ and $I_{L2}^{'} < I_{L2}$. For the waveforms shown in Fig. 6.2(c), the equations obtained are presented in (6.21) where γ_3 represents the common shaded areas.

$$i_{L1}(0)(1-D_1)T_s = i_{L1}^{'}(0)(1-D_1)T_s \tag{6.21a}$$

$$I_{t1} = i_{L1}(0)D_1 - i_{L1}(t_2)(1-D_2+\overline{D_{NN1}}) + \gamma_3 \tag{6.21b}$$

$$I_{t1}^{'} = i_{L1}(0)D_1 + \gamma_3 \tag{6.21c}$$

Therefore, $I_{t1} < I_{t1}^{'}$ and $I_{L1} < I_{L1}^{'}$.

Similarly, (6.22) is obtained for i_{L2}, which concludes that $I_{t2}^{'} < I_{t2}$ and $I_{L2}^{'} < I_{L2}$.

$$i_{L2}(t_2)(1-D_2)T_s = i_{L2}^{'}(t_2^{'})(1-D_2)T_s \tag{6.22a}$$

$$I_{t2} = i_{L2}(t_2)D_2 + [i_{L2}(0) - i_{L2}(t_2)](D_2 - \overline{D_{NN1}}) + \gamma_4 \tag{6.22b}$$

$$I_{t2}^{'} = i_{L2}^{'}(t_2^{'})D_2 - [i_{L2}^{'}(t_2^{'}) - i_{L2}^{'}(0)](D_2 - \underline{D_{NN1}}) + \gamma_4 \tag{6.22c}$$

So, the analysis for different values of slope conditions and duty ratios show that $I_{L1} < I_{L1}^{'}$ and $I_{L2}^{'} < I_{L2}$; however the values of D_t for dashed values are different for different values of slope conditions and duty ratios. For slope conditions, $G_{NN1} > 0$, $G_{NF1} > 0$, $G_{FN1} < 0$, $G_{FF1} < 0$, $G_{NN2} > 0$, $G_{NF2} > 0$, $G_{FN2} < 0$, $G_{FF2} < 0$, for $D_1 + D_2 < 1$, dashed value is for $D_t = 1 - D_2$, where as for $D_1 + D_2 > 1$, dashed value is for $D_t = D_1$. For slope conditions $G_{NN1} > 0$, $G_{NF1} > 0$, $G_{FN1} > 0$, $G_{FF1} < 0$, $G_{NN2} > 0$, $G_{NF2} > 0$, $G_{FN2} > 0$, $G_{FF2} < 0$, and duty ratios $D_1 + D_2 < 1$, dashed value is at $D_t = D_1 + \overline{D_{PP1}}$. Similarly, for slope conditions $G_{NN1} > 0$, $G_{NF1} < 0$, $G_{FN1} < 0$, $G_{FF1} < 0$, $G_{NN2} > 0$, $G_{NF2} < 0$, $G_{FN2} < 0$, $G_{FF2} < 0$, and duty ratios $D_1 + D_2 > 1$, dashed value is at $D_t = D_1 - \underline{D_{NN1}}$.

The explanations for effect of shifting gate pulses on average values of currents are done for cases where the slope patterns of both inductor currents i_{L1} and i_{L2} are taken the same. However, the pattern of i_{L1} and i_{L2} can take different shapes, keeping $I_{L1} < I_{L1}^{'}$ and $I_{L2}^{'} < I_{L2}$.

It is also observed that the average value of input current, I_{in}, remains the same even though the average values of inductor currents, I_{L1} and I_{L2} changes as the shift is changed.

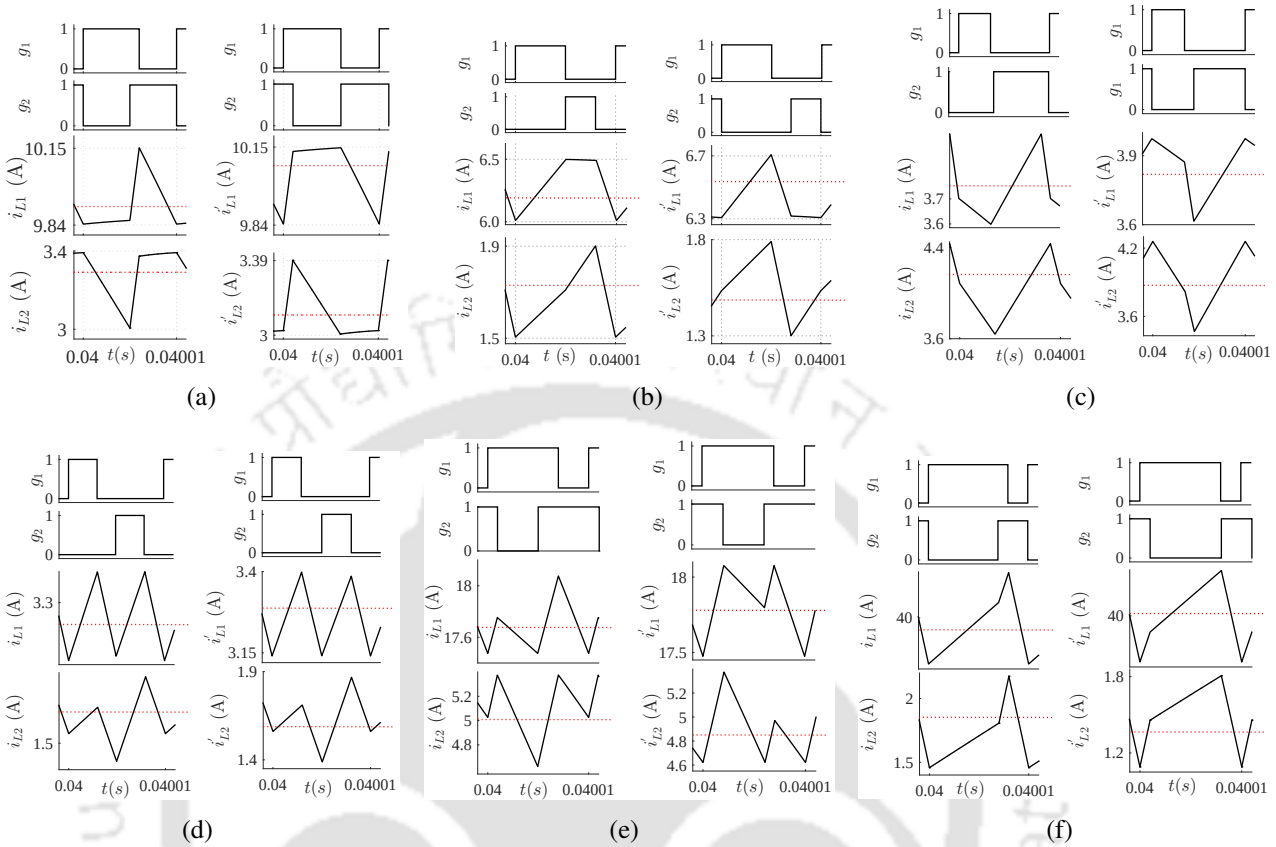


Figure 6.3: MATLAB simulation results for change in average value of inductor current for (a) $D_1 = 0.6$ and $D_2 = 0.5$: $I_{L1} = 9.92$, $I'_{L1} = 10.08$, $I_{L2} = 3.29$ and $I'_{L2} = 3.12$, (b) $D_1 = 0.5$ and $D_2 = 0.3$ $I_{L1} = 6.34$, $I'_{L1} = 6.46$, $I_{L2} = 1.70$ and $I'_{L2} = 1.57$, (c) $D_1 = 0.35$ and $D_2 = 0.55$: $I_{L1} = 3.74$, $I'_{L1} = 3.84$, $I_{L2} = 4.01$ and $I'_{L2} = 3.90$, (d) $D_1 = 0.3$ and $D_2 = 0.3$: $I_{L1} = 3.26$, $I'_{L1} = 3.27$, $I_{L2} = 1.63$ and $I'_{L2} = 1.62$, (e) $D_1 = 0.7$ and $D_2 = 0.6$: $I_{L1} = 17.69$, $I'_{L1} = 17.85$, $I_{L2} = 5.08$ and $I'_{L2} = 4.92$, and (f) $D_1 = 0.8$ and $D_2 = 0.3$: $I_{L1} = 39.93$, $I'_{L1} = 40.10$, $I_{L2} = 1.71$ and $I'_{L2} = 1.56$.

6.2.2 Simulation Results

Table 6.1: Converter Parameters

Parameters	Values
V_{in}	8 V
k	0.8
$C_1 = C_2 = C$	100 μF
f_s	100 kHz
L_1	150 μH
L_2	100 μH
R_1	5 Ω
R_2	10 Ω

The analysis done is verified by simulations of CI-SIDO boost converter in MATLAB/Simulink environment. The parameters used for simulations are presented in Table 6.1, however, the analysis

presented in this chapter is valid for all possible parameters. The simulation results are presented in Fig. 6.3. In Fig. 6.3(a), the average values of inductor currents are compared for slope conditions $G_{NN1} > 0$, $G_{NF1} > 0$, $G_{FN1} < 0$, $G_{FF1} < 0$, $G_{NN2} > 0$, $G_{NF2} < 0$, $G_{FN2} > 0$, $G_{FF2} < 0$. The duty ratios are $D_1 = 0.6$, $D_2 = 0.5$. The average values of i_{L1} are $I_{L1} = 9.92\ A$ at $D_t = 0.5$ and $I'_{L1} = 10.08\ A$ at $D_t = 0.6$. Similarly, the average values of i_{L2} are $I_{L2} = 3.29\ A$ at $D_t = 0.5$, and $I'_{L2} = 3.12\ A$ at $D_t = 0.6$. The comparisons shows that $I_{L1} < I'_{L1}$ and $I'_{L2} < I_{L2}$, however, I_{in} remains same at 13.2 A.

Similarly, Fig. 6.3(d) shows the simulation results for $D_1 = 0.3$, $D_2 = 0.3$ at $D_t = 0.495$ and $D_t = 0.505$. The average values of i_{L1} are $I_{L1} = 3.26\ A$ at $D_t = 0.495$ and $I'_{L1} = 3.27\ A$ at $D_t = 0.505$. The average values of i_{L2} are $I_{L2} = 1.63\ A$ at $D_t = 0.495$, and $I'_{L2} = 1.62\ A$ at $D_t = 0.505$. The results are in accordance with the analysis obtained from Fig. 6.1. The results show that $I_{L1} < I'_{L1}$ and $I'_{L2} < I_{L2}$, however, I_{in} remains same at 4.89 A. Similar results are shown in Figs. 6.3(b), 6.3(c), 6.3(e) and 6.3(f).

More simulation results are presented in Table 6.2 which covers all possible slope conditions. For all the cases, $I_{L1} < I'_{L1}$ and $I'_{L2} < I_{L2}$ keeping I_{in} almost same. However, the value of dashed terms is different for different slope conditions and duty ratios.

Table 6.2: Effect of Shifting Gate Pulse on Average Currents

Sl. No.	D_1	D_2	Slope conditions				Average currents				
			G_{NF1}	G_{FN1}	G_{NF2}	G_{FN2}	$I_{in}(A)$	$I_{L1}(A)$	$I'_{L1}(A)$	$I_{L2}(A)$	$I'_{L2}(A)$
1	0.5	0.4	+	-	-	+	8.62	6.35	6.45	2.27	2.17
2	0.6	0.5	+	-	-	+	13.20	9.92	10.08	3.29	3.12
3	0.4	0.5	+	+	-	+	7.65	4.40	4.49	3.25	3.16
4	0.5	0.6	-	-	-	+	11.40	6.34	6.46	5.07	4.93
5	0.7	0.6	-	-	-	-	22.78	17.69	17.86	5.08	4.92
6	0.3	0.3	+	+	+	+	4.89	3.26	3.27	1.63	1.62
7	0.8	0.3	+	-	+	-	41.64	39.93	40.06	1.71	1.56
8	0.55	0.3	+	-	+	+	9.54	7.84	7.96	1.69	1.58
9	0.7	0.4	+	-	-	-	19.99	17.70	17.85	2.29	2.15
10	0.3	0.6	-	+	-	+	8.26	3.22	3.31	5.05	4.95

6.3 Effect of Shifting Gate Pulse on Output Voltage Ripple

For the given load current, the shifting of the gate pulse changes the pattern of inductor currents. The change in inductor current changes the capacitor currents (Fig. 6.4). The capacitor currents

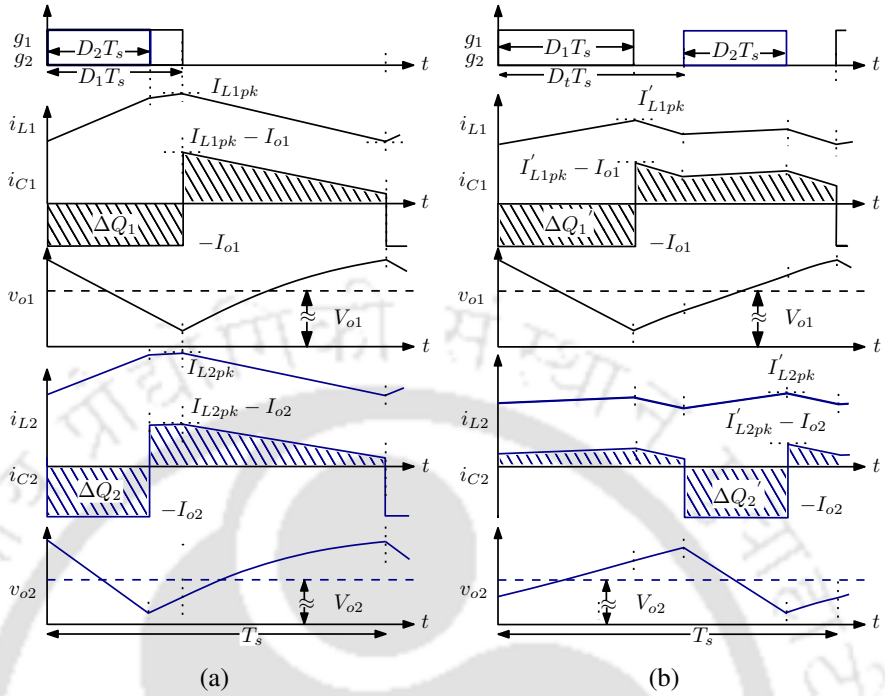


Figure 6.4: The patterns of indictor currents (i_{L1}, i_{L2}), capacitor currents (i_{C1}, i_{C2}) and output voltages (v_{o1}, v_{o2}) for given value of load at (a) $D_t = 0$, and $D_t = \mathbf{D}_{min}$.

decide the voltage ripples in the output capacitor. This chapter finds how much is the effect of shifting gate pulse on output voltage ripples. The chapter finds the conditions of output voltage ripples for different cases of duty ratios, load currents, and coupled inductor parameters.

6.3.1 Analysing the Effect of Gate Pulse Shift on Output Voltage Ripples

This section analyses the capacitor current when the gate pulse is shifted from $D_t = 0$ to $D_t = \mathbf{D}_{min}$. The capacitor current determines the ripple in output voltage. Based on capacitor current patterns, two types are observed: (i) The capacitor currents are always positive when the MOSFETs are OFF, and (ii) The capacitor currents become negative when the MOSFETs are OFF.

6.3.1.1 Capacitor Currents Always Positive when MOSFETs are OFF

The Fig. 6.4 shows the effect of shifting gate pulse on output voltage ripples. The figure shows the conditions for $D_t = 0$ and $D_t = \mathbf{D}_{min}$ in Fig. 6.4(a) and 6.4(b) respectively. The slope conditions considered are $G_{NN1} > 0$, $G_{NF1} > 0$, $G_{FN1} > 0$, $G_{FF1} < 0$ and $G_{NN2} > 0$, $G_{NF2} > 0$, $G_{FN2} > 0$, $G_{FF2} < 0$. The duty ratios are such that $D_1 > D_2$ and $D_1 + D_2 < 1$. In Fig. 6.4(a), i_{L1} is drawn with peak value I_{L1pk}. The capacitor current, i_{C1} is I_{o1} when MOSFET is ON and $i_{L1} - I_{o1}$ when MOSFET

is OFF with peak value $I_{L1pk} - I_{o1}$. v_{o1} is increasing when i_{C1} is positive and decreasing when i_{C1} is negative. The duration of i_{C1} when it is position or negative decides the voltage ripples. Similarly, i_{L2}, i_{C2} and v_{o2} are shown. If constant output currents are considered, (6.23) is obtained.

$$\Delta v_{o1} = \frac{\Delta Q_1}{C_1} = \frac{I_{o1} D_1 T_s}{C_1}, \tag{6.23a}$$

$$\Delta v_{o2} = \frac{\Delta Q_2}{C_2} = \frac{I_{o2} D_2 T_s}{C_2} \tag{6.23b}$$

In Fig. 6.4(b), as g_2 is shifted to $\mathbf{D}_{min}$, the pattern of i_{L1}, i_{C1} and v_{o1} are changed. The new peak value of i_{L1} is I'_{L1pk}. As the load is not changing as shifting is done, I_{o1} is same. The duration for which MOSFETs are ON and OFF are also not changing. So, the output voltage ripples are given by (6.24).

$$\Delta v_{o1}{}' = \frac{\Delta Q_1{}'}{C_1} = \frac{I_{o1} D_1 T_s}{C_1}, \tag{6.24a}$$

$$\Delta v_{o2}{}' = \frac{\Delta Q_2{}'}{C_2} = \frac{I_{o2} D_2 T_s}{C_2} \tag{6.24b}$$

Comparing (6.23) and (6.24), it is observed that, as the shifting is done, the voltage ripples are same for this case.

The analysis shown in Fig. 6.4, is also valid for other slope conditions. The value of capacitor currents is always equal to the load currents when the MOSFET is ON, irrespective of the inductor current patterns. So, the findings of this section are valid for all slope conditions of inductor currents.

6.3.1.2 Capacitor Currents Negative when MOSFETs are OFF

For different values of I_{o1} and I_{o2}, the output voltage ripples are observed. It is found that for reduced load currents, the capacitor current becomes negative for some portion of duration when MOSFETs are OFF.

In Fig. 6.5, i_{L1}, i_{C1} and v_{o1} are shown for three values of load currents. The waveforms for $D_t = 0$ is shown in Fig. 6.5(a)) and their corresponding conditions for $D_t = \mathbf{D}_{min}$ is shown in Fig. 6.5(b). It is observed from the figure that, as the load current decreases, a point is reached where an extra portion

of i_{C1} becomes negative. So in this case, the charge of capacitor is $\Delta Q_1 + B_1$ for $D_t = 0$ and $\Delta Q_1{}' + B_1'$ for $D_t = \mathbf{D}_{min}$.

Due to the extra negative portions, there is slight change in output voltage ripple. However, it is observed that $\Delta Q_1 >> B_1$ and $\Delta Q_1{}' >> B_1'$. So, for the loads where this conditions are possible, the change in voltage ripple has insignificant effect on the output voltage ripples. Similar analysis is also valid for i_{L2}, i_{C2} and v_{o2}.

Also, as expected from (6.23), the magnitude of output voltage ripples depends on the value of load currents. For a given C_1, C_2 values as the load currents are increased, the output voltage ripple magnitude is increased.

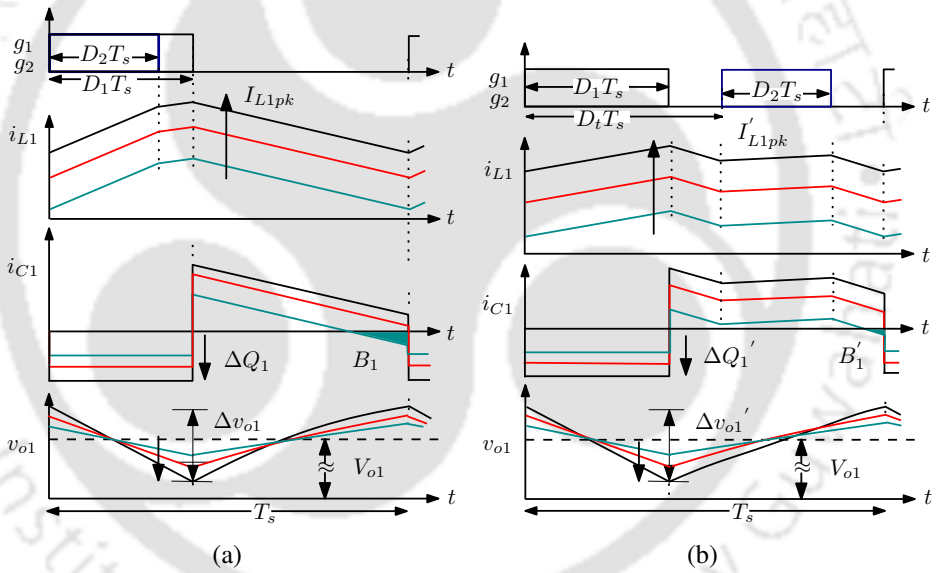


Figure 6.5: The patterns of inductor currents i_{L1}, capacitor currents i_{C1} and output voltages v_{o1} for different values of loads at (a) $D_t = 0$, and $D_t = \mathbf{D}_{min}$.

6.3.2 Simulation Results

The CI-SIDO boost converter is simulated in MATLAB/Simulink using the parameters presented in Table 6.3. The analysis presented in this chapter is true for continuous conduction mode (CCM) of the converter. So, the parameters are selected such that CI-SIDO boost operates in CCM. In this section, the simulation results are shown for different values of duty ratios and slope conditions. The comparisons of output voltage ripples are done for $D_t = 0$, and $D_t = \mathbf{D}_{min}$.

In Fig. 6.6, the values of inductor currents, capacitor currents and output voltages are shown for

Table 6.3: Simulation Parameters.

V_{in}	8 V	T_s	10 μs	k	0.73	C_1, C_2	100 μF
L_1	131.24 μH	L_2	94.61 μH	R_1	8 Ω	R_2	12 Ω

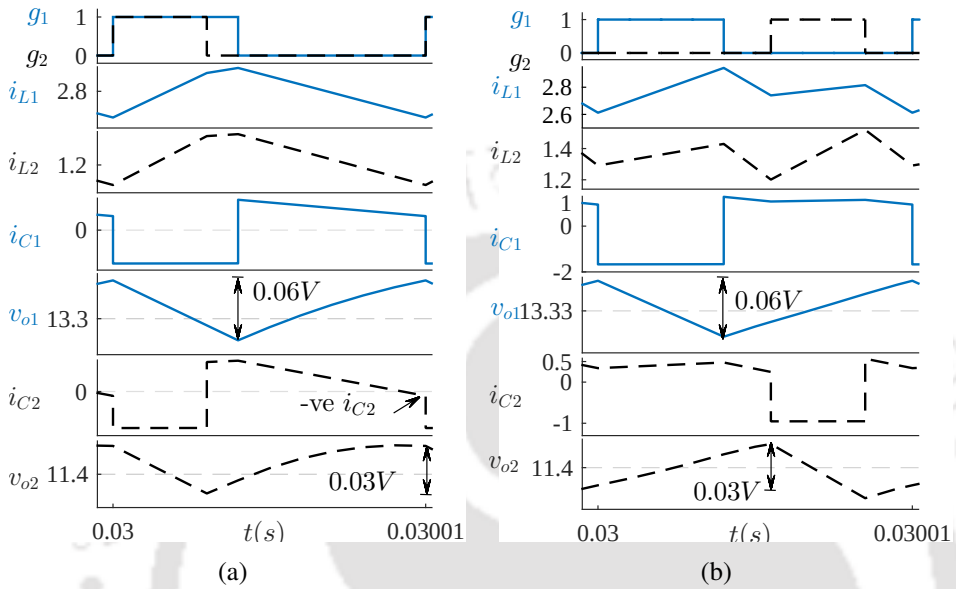


Figure 6.6: Inductor currents (in A), capacitor currents (in A), output voltages (in V) for $D_1 = 0.4$ and $D_2 = 0.3$ where $D_1 + D_2 < 1$ at (a) $D_t = 0$, and (b) $D_t = 0.55$. The slope conditions are $G_{NN1} > 0$, $G_{NF1} > 0$, $G_{FN1} > 0$, $G_{FF1} < 0$ and $G_{NN2} > 0$, $G_{NF2} > 0$, $G_{FN2} > 0$, $G_{FF2} < 0$.

$D_1 = 0.4$ and $D_2 = 0.3$ where $D_1 + D_2 < 1$ at $D_t = 0$ (Fig. 6.6(a)) and $D_t = 0.55$ (Fig. 6.6(b)).

The slope conditions are $G_{NN1} > 0$, $G_{NF1} > 0$, $G_{FN1} > 0$, $G_{FF1} < 0$ and $G_{NN2} > 0$, $G_{NF2} > 0$, $G_{FN2} > 0$, $G_{FF2} < 0$. It is observed that $\Delta v_{o1} = 0.06\ V$ for $D_t = 0$ and remains same as D_t is changed to 0.55. It is also observed from the figure that i_{C2} is becoming negative. Even though i_{C2} is negative for some time, $\Delta v_{o2} = 0.03\ V$ for $D_t = 0$ and remains same as D_t is changed to 0.55. The shifting is not changing the output voltage ripples even when capacitor current becomes negative for some time. In Fig. 6.7, i_{C1} is becoming negative for some time, however output voltage ripples 0.05 V and 0.15 V remains same for $D_t = 0$ and $D_t = \mathbf{D}_{min}$. Similar results in Fig. 6.8 and Fig. 6.9 shows that the ripples remain same for $D_t = 0$ and $D_t = \mathbf{D}_{min}$ for different values of duty ratios and slope conditions. The duty ratios and slope conditions of each simulation results are mentioned in the captions of respective figures.

The comparisons of output voltage ripples for different values of duty ratios are presented in Table 6.4. As the parameters are not changed, the magnitude of voltage ripples increase with increase in

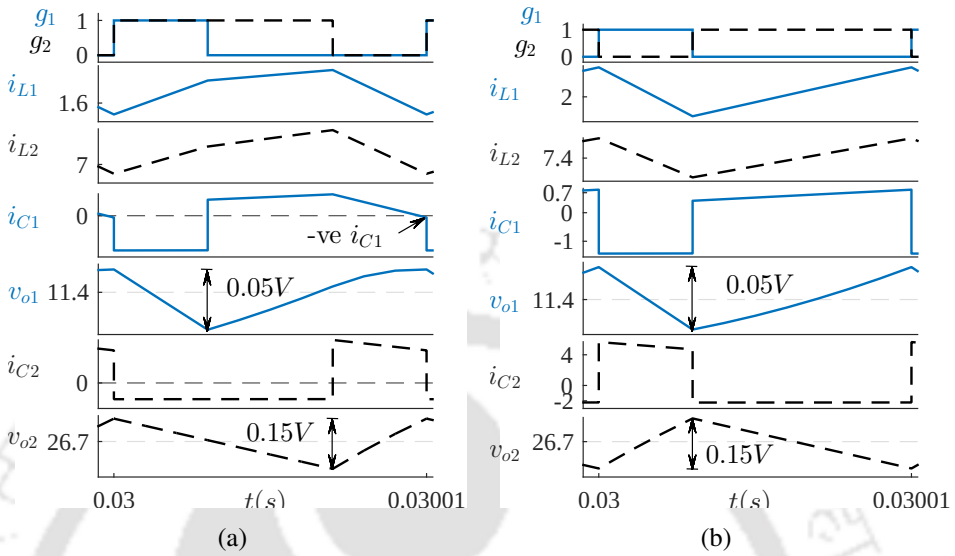


Figure 6.7: Inductor currents (in A), capacitor currents (in A), output voltages (in V) for $D_1 = 0.3$ and $D_2 = 0.7$ where $D_1 + D_2 = 1$ at (a) $D_t = 0$, and (b) $D_t = 0.3$. The slope conditions are $G_{NN1} > 0$, $G_{NF1} < 0$, $G_{FN1} > 0$, $G_{FF1} < 0$ and $G_{NN2} > 0$, $G_{NF2} < 0$, $G_{FN2} > 0$, $G_{FF2} < 0$.

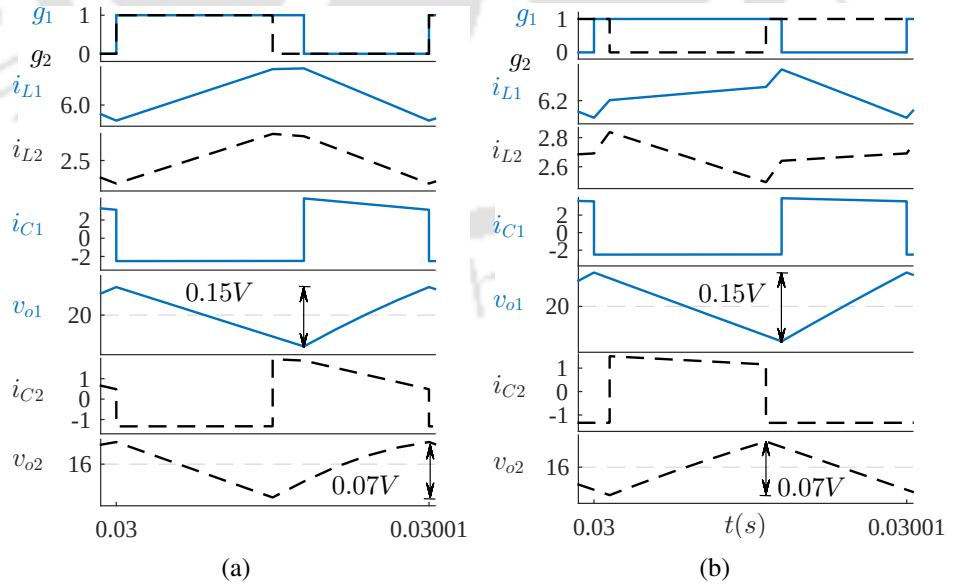


Figure 6.8: Inductor currents (in A), capacitor currents (in A), output voltages (in V) for $D_1 = 0.6$ and $D_2 = 0.5$ where $D_1 + D_2 > 1$ at (a) $D_t = 0$, and (b) $D_t = 0.55$. The slope conditions are $G_{NN1} > 0$, $G_{NF1} > 0$, $G_{FN1} < 0$, $G_{FF1} < 0$ and $G_{NN2} > 0$, $G_{NF2} < 0$, $G_{FN2} > 0$, $G_{FF2} < 0$.

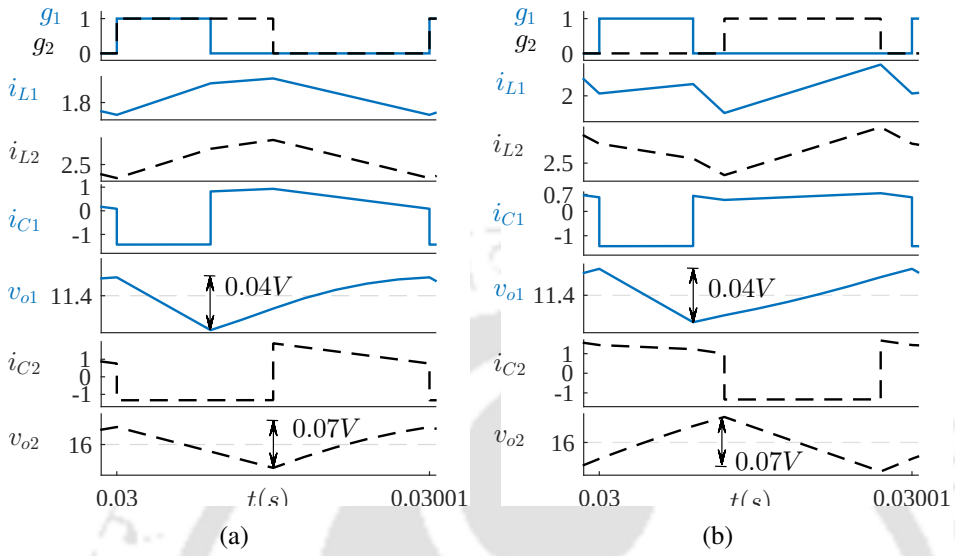


Figure 6.9: Inductor currents (in A), capacitor currents (in A), output voltages (in V) for $D_1 = 0.3$ and $D_2 = 0.5$ where $D_1 + D_2 < 1$ at (a) $D_t = 0$, and (b) $D_t = 0.4$. The slope conditions are $G_{NN1} > 0$, $G_{NF1} > 0$, $G_{FN1} > 0$, $G_{FF1} < 0$ and $G_{NN2} > 0$, $G_{NF2} < 0$, $G_{FN2} > 0$, $G_{FF2} < 0$.

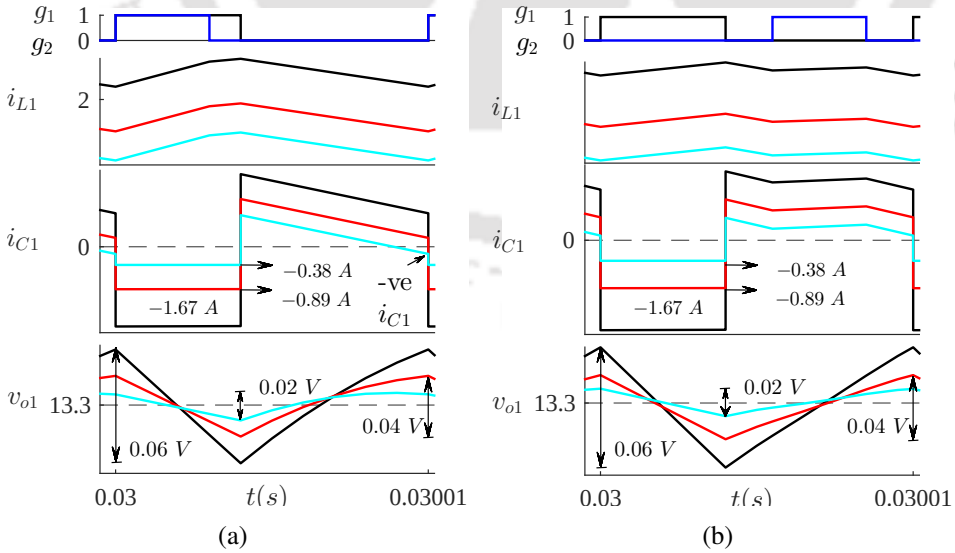


Figure 6.10: Inductor currents (in A), capacitor currents (in A), output voltages (in V) for $D_1 = 0.4$ and $D_2 = 0.3$ for different values of loads at (a) $D_t = 0$, and (b) $D_t = 0.55$. The slope conditions are $G_{NN1} > 0$, $G_{NF1} > 0$, $G_{FN1} > 0$, $G_{FF1} < 0$ and $G_{NN2} > 0$, $G_{NF2} > 0$, $G_{FN2} > 0$, $G_{FF2} < 0$. The loads are $R_1 = 8\ \Omega$, $R_2 = 12\ \Omega$ (black), $R_1 = 15\ \Omega$, $R_2 = 16\ \Omega$ (red) and $R_1 = 35\ \Omega$, $R_2 = 20\ \Omega$ (cyan).

Table 6.4: Comparison of Voltage Ripples for $D_t = 0$ and $D_t = \mathbf{D}_{min}$.

Sl. No	D_1	D_2	$\Delta v_{o1}(V)$	$\Delta v_{o1}{}'(V)$	$\Delta v_{o2}(V)$	$\Delta v_{o2}{}'(V)$
1	0.3	0.3	0.05	0.04	0.03	0.03
2	0.6	0.3	0.15	0.15	0.03	0.02
3	0.7	0.2	0.23	0.23	0.021	0.016
4	0.3	0.4	0.05	0.04	0.04	0.04
5	0.5	0.5	0.1	0.1	0.07	0.06
6	0.7	0.5	0.23	0.23	0.07	0.06
7	0.3	0.7	0.05	0.04	0.15	0.15
8	0.6	0.6	0.15	0.15	0.1	0.1
9	0.7	0.6	0.23	0.23	0.1	0.1

output voltage. The comparisons are done for $D_t = 0$ and $D_t = \mathbf{D}_{min}$. These comparisons show that the shift in gate pulse have insignificant effect on the output voltage ripples.

The simulation results of i_{L1}, i_{C1}, v_{o1} are also shown for duty ratios $D_1 = 0.4$, $D_2 = 0.3$ with changing loads. Figs. 6.10(a) and 6.10(b) are shown for $D_t = 0$ and $D_t = 0.55$, respectively. It is observed that for $I_{o1} = 0.38\ A$, $\Delta v_{o1} = 0.02\ V$ which remains same for $D_t = 0$ and $D_t = 0.55$, even though i_{C1} is negative for some time. For $I_{o1} = 0.89\ A$, Δv_{o1} increases to $0.04\ V$ and remains same for $D_t = 0$ and $D_t = 0.55$, i_{C1} is always positive when S_{t1} is OFF. Similarly, for $I_{o1} = 1.67\ A$, Δv_{o1} increases to $0.06\ V$ for $D_t = 0$ and $D_t = 0.55$.

The analysis shows that the output voltage ripples remain unaffected for shifting; however, it gets affected when load currents are changed. These results are valid for all values of duty ratios and coupled inductor parameters.

6.4 Summary of the Chapter

The following are the findings of the chapter–

(i) The chapter analyses the effect of gate pulse shift on the average values of inductor currents and the output voltage ripples in coupled inductor single input dual output (CI-SIDO) boost converter.

(ii) With shifting, the average values of first inductor current increases and second inductor current decreases, such that the average values of input currents do not change.

(iii) For all the cases, it is found that the shifting of gate pulse has an insignificant effect on output voltage ripples.

(iv) The analyses are proved analytically for different values of duty ratios and slope conditions.

(v) The analyses are validated by MATLAB simulations.

7

Dependence of CCM/DCM Boundary on Gate Pulse Shift in Coupled SIDO Boost Converter

Contents

7.1 Introduction

[1] The unidirectional DC-DC converters operate in two modes– continuous conduction mode (CCM) and discontinuous conduction mode (DCM). In CCM, the inductor currents remain non-zero for the entire switching period, T_s, whereas in DCM, the inductor currents become zero before the completion of T_s. The transition from CCM to DCM occurs at CCM/DCM boundary. At the boundary, the inductor current becomes zero at T_s. The converters operate in CCM when the load currents are higher than the CCM/DCM boundary currents. If the load currents reduce below the CCM/DCM boundary, the converter enters DCM.

The control of the converter is easier in CCM. Also, the output voltage does not depend on load currents. In DCM, the output voltage depends on the load currents, and the control of the converter also becomes load-dependent. Therefore, the DC-DC converters are preferred to be operated in CCM. However, to ensure the CCM operation of the converter, knowledge of the CCM/DCM boundary is necessary. If the boundary current is higher, the current range of CCM reduce. On the other hand, if the boundary current is reduced, the load current range of the CCM operations increase. For example, if the load range of converter is $0-5\ A$ and boundary value is $2\ A$, the range of CCM operation is $2-5\ A$. However, if we reduce the boundary current to $0.5\ A$, the range of CCM operation increases to $0.5-5\ A$.

The above discussions on DC-DC converters are true even if there is coupling between the inductors of the converters. The discussions are equally applicable for any DC-DC converters as well as the CI-SIDO converters. However, due to the presence of the coupled inductor, the CCM/DCM boundary operation of CI-SIDO converters are much more complex than conventional boost converters.

One of the methods to reduce the CCM/DCM boundary current is to increase the inductance values of the converter. However, the increase in inductance increases the core size of the inductor and the overall physical size of the converter. Therefore, the motivation of this work is to increase

[1]Note: Major part of this chapter is reproduced from my publications: (i) Nupur and S. Nath, "Effect of Shifting Gate Pulse on CCM/DCM Boundary in Coupled SIDO Boost Converter," in *Proc. Nat. Power Electron. Conf.*, Dec. 2019, pp. 1-6. (ii) Nupur and S. Nath, "Effect of Mutual Coupling on CCM/DCM Boundary in Single Input Dual Output Boost Converter," in *Proc. 8th Power India Int. Conf.*, Dec. 2018, pp. 1-6. (iii) Nupur and S. Nath, "Dependence of CCM/DCM Boundary on Gate Pulse Shift in Coupled SIDO Boost Converter," accepted in *IEEE Trans. Transp. Electrification.*

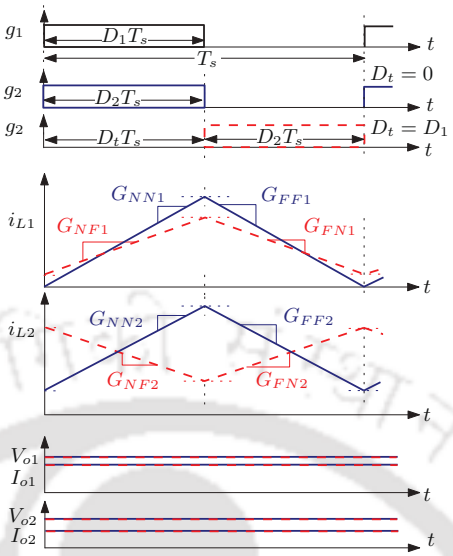


Figure 7.1: Change of inductor current from CCM/DCM boundary condition to CCM as g_2 is changed from $D_t = 0$ (blue) to $D_t = D_1$ (red).

the CCM operating range of CI-SIDO boost by reducing the CCM/DCM boundary current without changing any circuit parameters like inductance value. One of the methods that is proposed in this chapter is the shift of gate pulse. It is found that the CCM/DCM boundary depends on the gate pulse shift. As the gate pulse is shifted, the average values of inductor current at boundary reduces. This helps to increase the CCM operating range of CI-SIDO boost.

The effect of gate pulse shifting is shown in Fig. 7.1 for $D_t = 0$ (blue) and $D_t = D_1$ (red). As g_2 is shifted from 0 to D_1T_s, the inductor current patterns are changed. The following can be observed from the figure–

- i_{L1} is at boundary when $D_t = 0$ as it touches 0 at T_s.
- i_{L1} changes to CCM at $D_t = D_1$.
- i_{L2} is operated in CCM for $D_t = 0$ as well as $D_t = D_1$.
- The load currents and output voltages remain same for $D_t = 0$ and $D_t = D_1$.

The average value of i_{Lw} at boundary, is denoted by I_{LwB} at $D_t = 0$, and by I'_{LwB} at $D_t \neq 0$, where $w = 1$ for i_{L1}, and $w = 2$ for i_{L2}. The effect of gate pulse shift is also presented in Fig. 7.2.

The waveforms of i_{L1} at CCM/DCM boundary for $D_t = 0$ and $D_t \neq 0$ is shown in Fig. 7.2. From

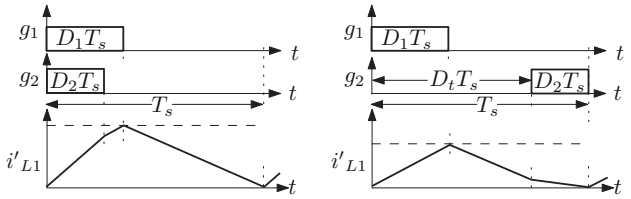


Figure 7.2: The inductor currents at (a) $D_t = 0$, and (b) $D_t = (1 - D_2)$.

the figure, it is found that the average values of i_{L1} at $D_t = 0$ is given by–

$$I_{L1B} = \frac{T_s V_{in}}{2(1-k^2)L_1}[D_1 + k\sqrt{\frac{L_1}{L_2}}D_2]. \tag{7.1}$$

The average values of i_{L1} at $D_t \neq 0$, i.e., $D_t = (1 - D_2)$ is given by–

$$I'_{L1B} = \frac{T_s V_{in}}{2(1-k^2)L_1}[D_1 - k\sqrt{\frac{L_1}{L_2}}D_2]. \tag{7.2}$$

By comparing the average values of i_{L1} for $D_t = 0$ and $D_t = (1 - D_2)$, we found that it is reduced by–

$$\frac{(I_{L1B} - I'_{L1B})}{I_{L1B}} \times 100\% = \frac{2k\sqrt{\frac{L_1}{L_2}}D_2}{[D_1 + k\sqrt{\frac{L_1}{L_2}}D_2]} \times 100\%. \tag{7.3}$$

For $k = 0.8$, $\frac{L_1}{L_2} = 0.65$, $D_1 = 0.4$, and $D_2 = 0.5$, the percentage reduction in average values of i_{L1} is 89%. This means for $V_{in} = 10\ V$, $L_1 = 100\ \mu H$, and $L_2 = 155\ \mu H$, the average value of i_{L1} at $D_t = 0$ is 1 A and $D_t = 0.5$ is 0.1 A. Therefore, at $D_t = 0$, i_{L1} is in CCM when i_{o1} is above 0.6 A while for $D_t = 0.5$, i_{L1} is in CCM when i_{o1} is above 0.05 A. Hence, we observe the advantages of shifting as–

- keeping all the parameters same, by introducing shift of gate pulse, the range of CCM operation is increased significantly.
- the value of shift where the average of inductor currents are minimum depends on the waveform patterns.
- with change in duty ratios, i.e., the voltages and coupled inductor patterns, the minimum average of inductor currents and the corresponding shift change.

Therefore, to increase the range of CCM without any additional circuit elements, the calculation of gate pulse shift is required where the average value of inductor current is minimum. This thesis finds

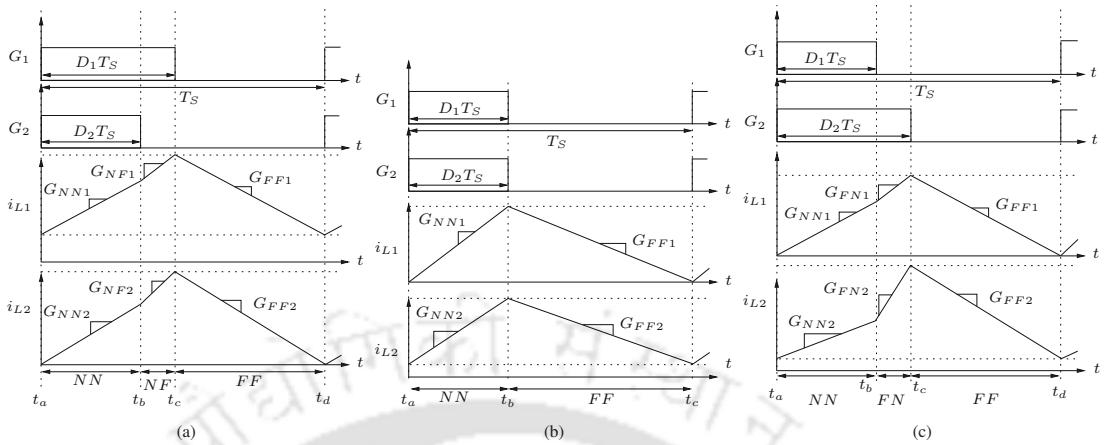


Figure 7.3: Theoretical waveforms of i_{L1} and i_{L2} (a) for $D_1 > D_2$; i_{L2} at the boundary condition, (b) for $D_1 = D_2$; i_{L1} at the boundary condition, and (c) for $D_1 < D_2$; i_{L1} at the boundary condition.

the gate pulse shift where the average value of inductor current is minimum for all possible waveforms of CI-SIDO boost converter.

7.2 Average Value of i_{Lw} at CCM/DCM Boundary, I_{LwB} for $D_t = 0$

The average of i_{L1} at the boundary, denoted by I_{L1B}, is given by (7.4).

$$I_{L1B} = \frac{1}{T_S}\int_0^{T_S} i_{L1}dt \tag{7.4}$$

At the edge of CCM, the pattern of i_{L1} is shown in Fig. 7.3. Using the figure, the average value (7.4) modifies to (7.5).

$$I_{L1B} = \frac{T_S}{2}\left[G_{NN1}D_1D_2 + G_{FF1}\left(1 - D_1 - D_2 + D_1D_2\right)\right] \tag{7.5}$$

Substituting the value of G_{NN1} and G_{FF1} in (7.5), the average value of i_{L1} at the edge of CCM is given by (7.6).

$$I_{L1B} = \frac{T_s V_{in}}{2(1-k^2)L_1}\left[D_1 + k\sqrt{\frac{L_1}{L_2}}D_2\right] \tag{7.6}$$

Similarly, the average of i_{L2} at boundary condition which is denoted by I_{L2B}, is given by (7.7).

$$I_{L2B} = \frac{T_s V_{in}}{2(1-k^2)L_2}\left[D_2 + k\sqrt{\frac{L_2}{L_1}}D_1\right] \tag{7.7}$$

The values of I_{L1B} and I_{L2B} are same for all the three conditions of D_1 and D_2. For example, when $D_1 = D_2$, (7.6) reduces to (7.8).

$$I_{L1B} = \frac{D_1 T_S}{2(1-k^2)L_1}\left(1 + k\sqrt{\frac{L_1}{L_2}}\right)V_{in} \tag{7.8}$$

The expressions (7.6) and (7.7) show that it depends on k, L_1, L_2, V_{in}, V_{o1} and V_{o2}. Even if the value of L_1 is quite large, i_{L1} goes to boundary. Due to mutual coupling, I_{L1B} not only depends on its own circuit parameters, but also on the parameters of second boost- V_{o2} and L_2 (and vice-versa). It is found that I_{L1B} and I_{L2B} depend on the values of D_1 and D_2, however do not depend on the relative values of D_1 and D_2 i.e. whether $D_1 > D_2$, $D_1 < D_2$ or $D_1 = D_2$.

7.2.1 Effect of changing $\frac{L_1}{L_2}$

The value of I_{L1B} depends on $\frac{L_1}{L_2}$ and I_{L2B} depends on $\frac{L_2}{L_1}$. In Fig. 7.4, it is shown that with increase in the ratio of $\frac{L_1}{L_2}$, the boundary value of i_{L1} increases while the boundary value of i_{L2} decreases. In Fig. 7.5, keeping the value of L_1 fixed, with the increase in the value of $\frac{L_1}{L_2}$, I_{L1B} is increased due to decrease in L_2. For example, with $\frac{V_{o1}}{V_{o2}} = 0.8$, the value of I_{L1B}, at $\frac{L_1}{L_2} = 0.5$, is 1.10 A, while at $\frac{L_1}{L_2} = 2$, is 1.54 A. Keeping L_2 fixed in Fig. 7.6, with increase in $\frac{L_1}{L_2}$, I_{L2B} decreases due to increase in L_1.

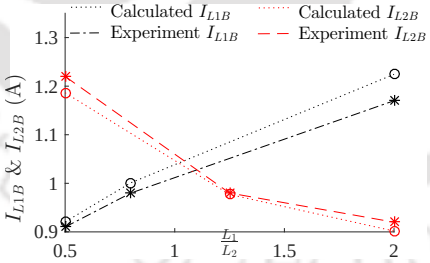


Figure 7.4: Variations of boundary currents with the change in inductance ratios for voltage ratios of 1.2.

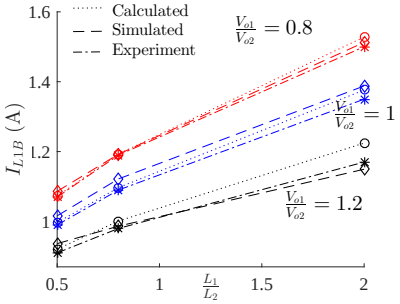


Figure 7.5: Effect of change in inductance ratios on the boundary condition of first inductor current for different values of voltage ratios.

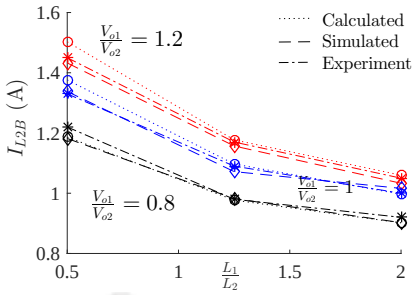
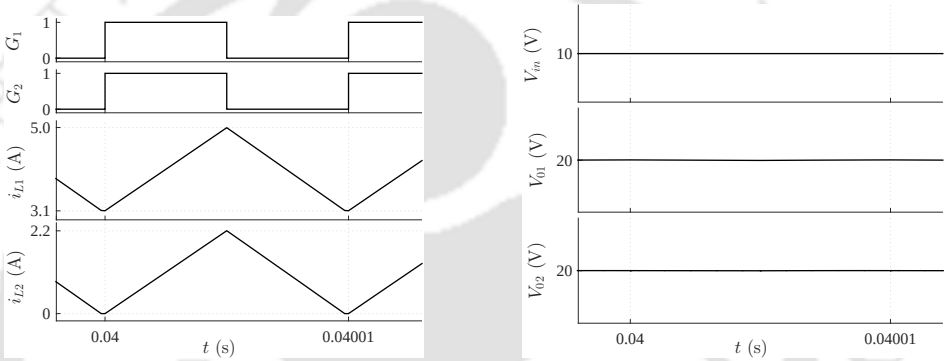


Figure 7.6: Effect of change in inductance ratios on the boundary condition of second inductor current for different values of voltage ratios.



(a) (b)

Figure 7.7: Simulation result for $D_1 = D_2 = 0.5$, $\frac{V_{o1}}{V_{o2}} = 1$, $\frac{L_1}{L_2} = 2$ and i_{L2} at boundary condition: (a) Pulse patterns and inductor currents, (b) Input and output voltages.

7.2.2 Effect of changing $\frac{V_{o1}}{V_{o2}}$

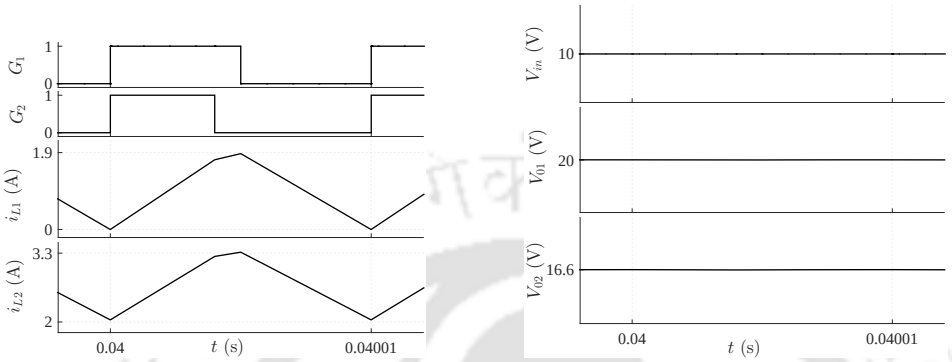
The boundary conditions of i_{L1} and i_{L2} depend on V_{o1} and V_{o2} both. The analysis is done to study the effect of change in V_{o2} on the values of I_{L1B} (and vice-versa).

In Fig. 7.5, I_{L1B} is plotted for various values of $\frac{V_{o1}}{V_{o2}}$ keeping V_{o1} fixed. For given V_{o1}, with increase in $\frac{V_{o1}}{V_{o2}}$ the value of V_{o2} decreases, thus, decreasing I_{L1B}. Similarly, in Fig. 7.6, I_{L2B} is plotted for various values of $\frac{V_{o1}}{V_{o2}}$ keeping V_{o2} fixed. Increase in $\frac{V_{o1}}{V_{o2}}$ increases the boundary condition because of the increase in V_{o1}.

7.2.3 Simulation Results

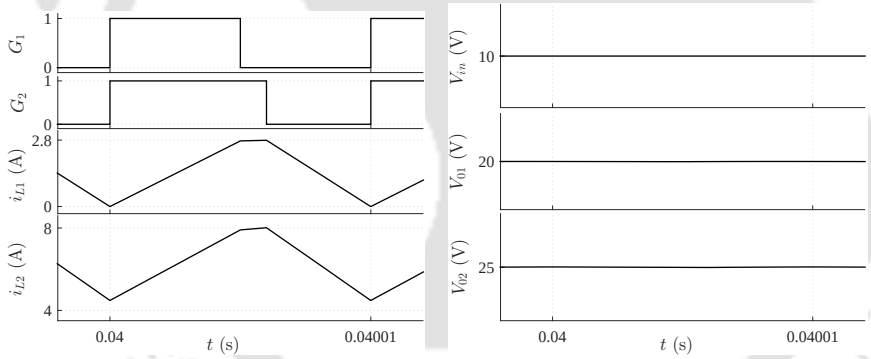
The analytical expressions are validated with the simulation results. The SIDO boost converter with the coupled inductor is simulated in MATLAB/Simulink and the results are presented. The simulation is done for $k = 0.9$. The input voltage, V_{in} is taken as 10 V. The capacitors, C_1 and C_2 are

taken equal with value $100\mu F$. The values of L_1, L_2, V_{o1} and V_{o2} are changed to obtain various values of $\frac{V_{o1}}{V_{o2}}$ and $\frac{L_1}{L_2}$. In Fig. 7.7, the simulation is done for $D_1 = D_2 = 0.5$. The output voltages are equal



(a) (b)

Figure 7.8: Simulation result for $D_1 = 0.5$, $D_2 = 0.4$, $\frac{V_{o1}}{V_{o2}} = 1.2$, $\frac{L_1}{L_2} = 0.5$ and i_{L1} at boundary condition: (a) Pulse patterns and inductor currents, (b) Input and output voltages.



(a) (b)

Figure 7.9: Simulation result for $D_1 = 0.5$, $D_2 = 0.6$, $\frac{V_{o1}}{V_{o2}} = 0.8$, $\frac{L_1}{L_2} = 1.5$ and i_{L1} at boundary condition: (a) Pulse patterns and inductor currents, (b) Input and output voltages.

with value 20 V, $\frac{V_{o1}}{V_{o2}} = 1$ and $\frac{L_1}{L_2} = 2$. The current i_{L2} reaches the boundary condition first while i_{L1} is in CCM. The value of I_{L2B} is 1.08 A approximately. In Fig. 7.8, the simulation is done for $D_1 = 0.5$, $D_2 = 0.4$, $\frac{V_{o1}}{V_{o2}} = 1.2$ and $\frac{L_1}{L_2} = 0.5$. The current i_{L1} reaches the boundary condition while i_{L2} is in CCM. The value of I_{L1B} is 0.97 A approximately. In Fig. 7.9, the simulation is done for $D_1 = 0.5$, $D_2 = 0.6$, $\frac{V_{o1}}{V_{o2}} = 0.8$ and $\frac{L_1}{L_2} = 1.5$. The current i_{L1} reaches the boundary condition while i_{L2} is in CCM. The value of I_{L1B} is 1.42 A approximately. More details of the simulation results are presented in Table 7.1 where P_{o1}, P_{o2} are load powers, P_{in} is input power, I_{o1}, I_{o2} are load currents and I_{in} is input current.

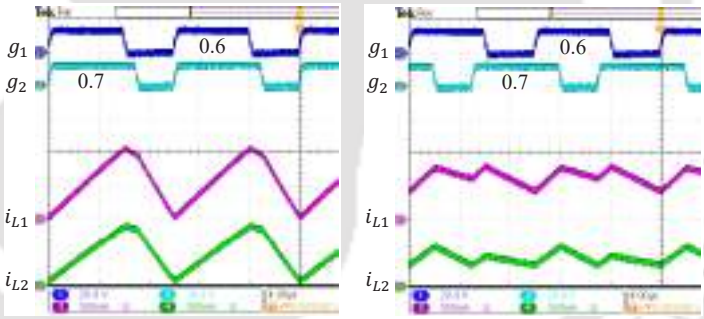
Table 7.1: Simulation results.

Fig. No.	I_{in} (A)	P_{in} (W)	I_{01} (A)	I_{02} (A)	P_{01} (W)	P_{02} (W)	L_1 (μH)	L_2 (μH)	Boundary current
7.7	5.08	50.76	2.00	0.54	40.10	10.50	400	200	i_{L2}
7.8	3.71	37.15	0.47	1.67	9.20	27.70	200	400	i_{L1}
7.9	7.92	79.20	0.84	2.51	16.50	62.50	200	133.33	i_{L1}

Table 7.2: Comparison of calculated and simulated values for various $\frac{L_1}{L_2}$ ratios at $\frac{V_{o1}}{V_{o2}} = 0.8$.

$\frac{L_1}{L_2}$	0.5	0.8	1	1.5	2
Calculated I_{L1B} (A)	1.16	1.29	1.37	1.53	1.66
Simulated I_{L1B} (A)	1.10	1.22	1.29	1.42	1.54
Calculated I_{L2B} (A)	1.28	1.15	1.10	1.02	0.97
Simulated I_{L2B} (A)	1.30	1.16	1.10	1.01	0.96

The effect of the change in $\frac{V_{o1}}{V_{o2}}$ and $\frac{L_1}{L_2}$, on I_{L1B} and I_{L2B} is verified with simulation. The calculated and simulated values are presented in Table. 7.2, for $\frac{V_{o1}}{V_{o2}} = 0.8$.



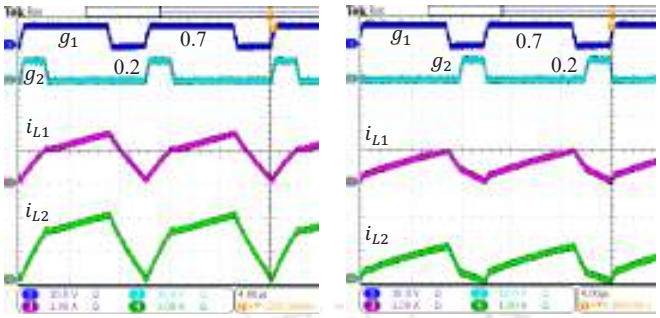
(a) $D_t = 0$ (b) $D_t = 0.5$

Figure 7.10: Change of inductor current from CCM/DCM boundary condition to CCM as g_2 is changed from (a) $D_t = 0$ to (b) $D_t = 0.5$.

7.2.4 Experimental Results

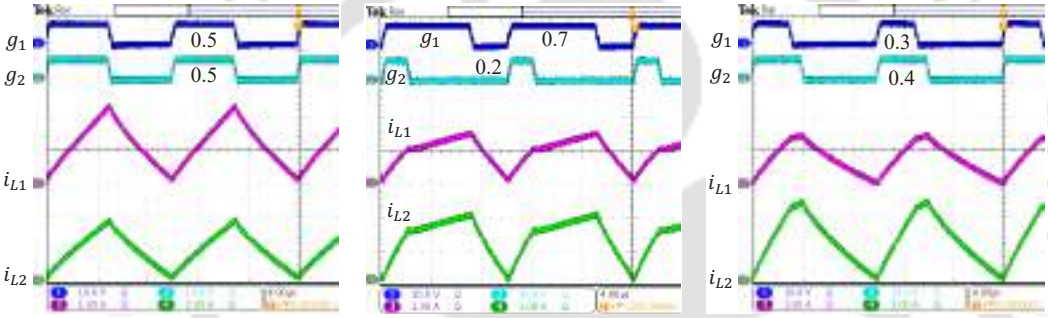
This section verifies the analytical and simulation results of CI-SIDO boost converter. The waveforms in Fig. 7.10 show the effect of gate pulse shift on the inductor current waveforms. The experiments are done for $k = 0.9$, $L_1 = 100\ \mu H$, $L_2 = 155\ \mu H$, $V_{in} = 4\ V$, $R_1 = 46\ \Omega$, $R_2 = 100\ \Omega$ and C_1 and C_2 are taken equal with value $100\mu F$. As expected, the waveforms change from CCM/DCM boundary to CCM as gate pulse shifts keeping other parameters same.

The inductor current waveforms at $D_t = 0$, and $D_t = (1 - D_2)$ is shown in Fig. 7.11. The experiments are done for $k = 0.65$, $L_1 = 120\ \mu H$, $L_2 = 48\ \mu H$, $V_{in} = 4\ V$, $R_1 = 156\ \Omega$, $R_2 = 12\ \Omega$ and



(a) (b)

Figure 7.11: The inductor currents at (a) $D_t = 0$, and (b) $D_t = (1 - D_2)$.



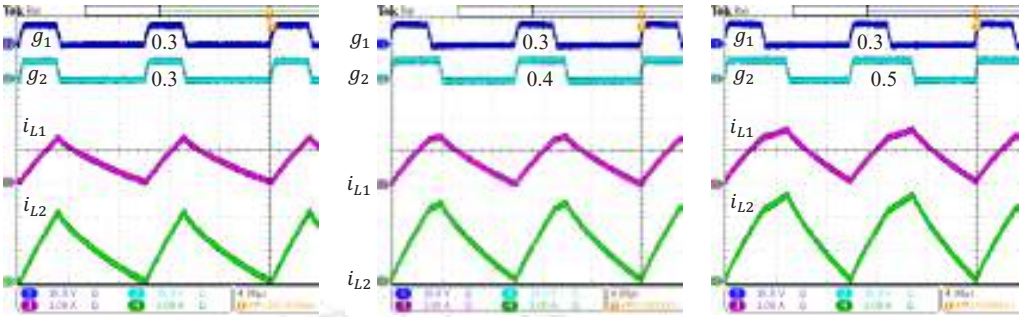
(a) (b) (c)

Figure 7.12: Experimental results with $\frac{L_1}{L_2} = 2.5$ for (a) $D_1 = D_2 = 0.5$, $\frac{V_{o1}}{V_{o2}} = 1$, (b) $D_1 = 0.7$, $D_2 = 0.2$, $\frac{V_{o1}}{V_{o2}} = 2.67$, (c) $D_1 = 0.3$, $D_2 = 0.4$, $\frac{V_{o1}}{V_{o2}} = 0.85$.

C_1 and C_2 are taken equal with value 100 μF. The reduction in the average values of i_{L1} for $D_t = 0$ and $D_t = 0.8$ is 40%, which is approximately matching with the theoretical expectations from (7.3).

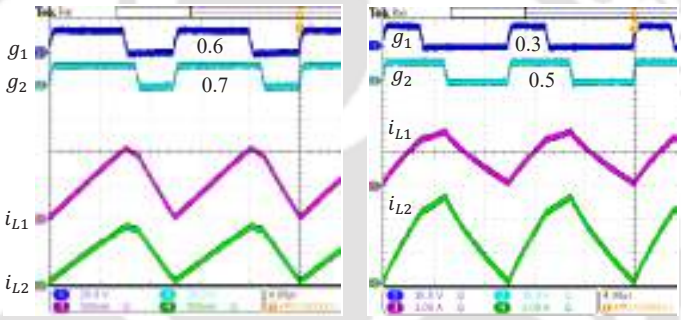
The simulation waveforms presented in Fig. 7.7 for $D_1 = D_2 = 0.5$ is verified experimentally in Fig. 7.12(a). The experiments are done for $k = 0.8$, $L_1 = 120\ \mu H$, $L_2 = 48\ \mu H$, $V_{in} = 5\ V$, $R_1 = 85\ \Omega$, $R_2 = 36\ \Omega$ and C_1 and C_2 are taken equal with value $100\mu F$. The simulation waveforms presented in Fig. 7.8 for $D_1 > D_2$ is verified experimentally in Fig. 7.12(b). The experiments are done for $k = 0.8$, $L_1 = 120\ \mu H$, $L_2 = 48\ \mu H$, $V_{in} = 5\ V$, $R_1 = 18\ \Omega$, $R_2 = 40\ \Omega$ and C_1 and C_2 are taken equal with value $100\mu F$. Similarly, the simulation waveforms presented in Fig. 7.9 for $D_1 < D_2$ is verified experimentally in Fig. 7.12(c). The experiments are done for $k = 0.8$, $L_1 = 120\ \mu H$, $L_2 = 48\ \mu H$, $V_{in} = 5\ V$, $R_1 = 160\ \Omega$, $R_2 = 12\ \Omega$ and $C_1 = C_2 = 100\mu F$.

The analysis is done to study the effect of change in V_{o2} on the values of I_{L1B}. In Fig. 7.13, i_{LwB} is plotted for various values of $\frac{V_{o1}}{V_{o2}}$ keeping V_{o1} fixed. For given V_{o1}, with decrease in $\frac{V_{o1}}{V_{o2}}$, the value of V_{o2}



(a) (b) (c)

Figure 7.13: Experimental results with $\frac{L_1}{L_2} = 2.5$ and $V_{in} = 5\ V$, $V_{o1} = 7.14\ V$ for (a) $\frac{V_{o1}}{V_{o2}} = 1$, (b) $\frac{V_{o1}}{V_{o2}} = 0.86$, (c) $\frac{V_{o1}}{V_{o2}} = 0.71$. The analysis is done to study the effect of change in V_{o2} on the values of I_{L1B}.



(a) (b)

Figure 7.14: Experimental results with $\frac{V_{o1}}{V_{o2}} = 0.72$ for (a) $\frac{L_1}{L_2} = 0.65$, (b) $\frac{L_1}{L_2} = 2.5$. The analysis is done to study the effect of change in $\frac{L_1}{L_2}$ on the values of I_{L1B}.

increases, thus increasing I_{L1B}. The value of I_{L1B} is 0.28 A at $\frac{V_{o1}}{V_{o2}} = 1$, 0.85 A at $\frac{V_{o1}}{V_{o2}} = 0.86$, and 1.18 A at $\frac{V_{o1}}{V_{o2}} = 0.71$. The values of I_{L1B} and I_{L2B} depend on $\frac{L_1}{L_2}$. In Fig. 7.14, it is shown that with increase in the ratio of $\frac{L_1}{L_2}$, the boundary value of i_{L1} increases. The value of I_{L1B} is 0.54 A at $\frac{L_1}{L_2} = 0.65$, 1.18 A at $\frac{L_1}{L_2} = 2.5$.

7.3 Effect of Gate Pulse Shift on Average Values at CCM/DCM Boundary for $D_t \neq 0$

The value of I'_{LwB} depends on the slope possibilities. The slope possibilities considered in the chapter is $G_{NF_w} > 0$ and $G_{FN_w} < 0$, or $G_{NF_w} < 0$ and $G_{FN_w} > 0$.

For example, consider the waveform with $D_1 > D_2$, $D_1 + D_2 < 1$ and $D_t = (1 - D_2)$ as shown in Fig. 7.15, for $G_{NF_w} < 0$ and $G_{FN_w} > 0$. The expression of I'_{LwB} is formulated by finding the area under

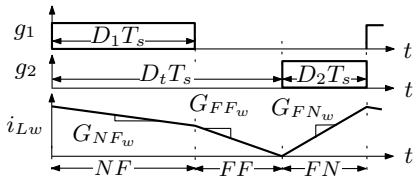


Figure 7.15: The pattern of inductor currents for $D_1 > D_2$, $D_1 + D_2 < 1$ and $D_t = (1 - D_2)$ when $G_{NF_w} < 0$ and $G_{FN_w} > 0$.

the curve, as presented in (7.9).

$$I'_{LwB} = \frac{1}{T_s}\int_0^{T_s} i_{Lw}dt \tag{7.9}$$

Solving the expression, (7.9) reduces to (7.10).

$$I'_{LwB} = \frac{T_s}{2}\left[\ G_{FN_w}(D_2^2 + D_1D_2) + |G_{FF_w}|(1 - D_2)(1 - D_1 - D_2)\ \right] \tag{7.10}$$

Substituting the values of slopes for $w = 1$ (i_{L1}) from Table 2.2, the expressions of I'_{L1B} are obtained as presented in (7.11).

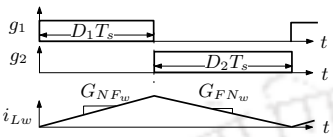
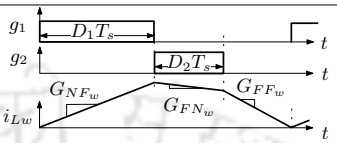
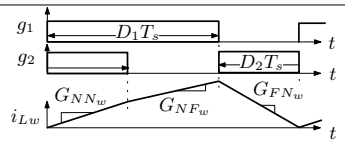
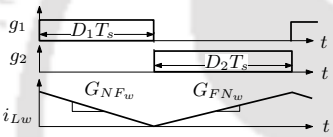
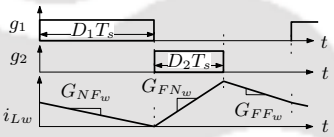
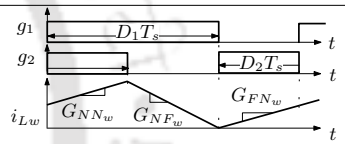
$$I'_{L1B} = \frac{T_sV_{in}}{2(1 - k^2)L_1}\left[D_1\left(\frac{(1 - D_1) - 2D_2}{(1 - D_1)}\right) + k\sqrt{\frac{L_1}{L_2}}D_2\right] \tag{7.11}$$

Comparing (7.6) and (7.11), it is found that (7.11) is lower because for same values of parameters, D_1 is multiplied by a fractional number which makes it smaller. In all other situations, when $(1-D_1) < 2D_2$, the negative term makes the equation smaller.

The possible values of D_t is from 0 to 1. The Fig. 7.15 considers $D_t = (1 - D_2)$. For all the other possible conditions, the expressions for I'_{L1B} and I'_{L2B} are presented in Table 7.3, for $D_t = D_1$. However, the analysis is true for all other value of D_t. In Table 7.3, the waveforms for two slope conditions are presented for different values of $D_1 + D_2$. The rows represent the average values of inductor current at CCM/DCM boundary. This table is presented to show that the CCM/DCM boundary decreases as the gate pulse shift is introduced.

Each expressions of I'_{L1B} and I'_{L2B} presented in Table 7.3, are compared with (7.6). In each case, it is found that $I'_{L1B} < I_{L1B}$ and $I'_{L2B} < I_{L2B}$. So, it is concluded that as D_t varies from 0 to 1, the CCM/DCM boundary is reduced. Whether both currents reach CCM/DCM boundary simultaneously

Table 7.3: Average values of inductor currents at CCM/DCM boundary for various duty ratios and slope conditions.

Slope condition: $G_{NF_w} > 0$ and $G_{FN_w} < 0$			
$D_1 + D_2$	$= 1$	< 1	> 1
Pattern			
I'_{L1B}	$\frac{T_s V_{in}}{2(1-k^2)L_1}[D_1 - k\sqrt{\frac{L_1}{L_2}}D_2]$	$\frac{T_s V_{in}}{2(1-k^2)L_1}\left[D_1 + k\sqrt{\frac{L_1}{L_2}}D_2\left(\frac{(1-D_2)-2D_1}{(1-D_2)}\right)\right]$	$\frac{T_s V_{in}}{2(1-k^2)L_1}\left[D_1 + k\sqrt{\frac{L_1}{L_2}}D_2\left(\frac{D_2-2(1-D_1)}{D_2}\right)\right]$
I'_{L2B}	$\frac{T_s V_{in}}{2(1-k^2)L_2}[-D_2 + k\sqrt{\frac{L_2}{L_1}}D_1]$	$\frac{T_s V_{in}}{2(1-k^2)L_2}\left[D_2\left(\frac{(1-D_2)-2D_1}{(1-D_2)}\right) + k\sqrt{\frac{L_2}{L_1}}D_1\right]$	$\frac{T_s V_{in}}{2(1-k^2)L_2}\left[D_2\left(\frac{D_2-2(1-D_1)}{D_2}\right) + k\sqrt{\frac{L_2}{L_1}}D_1\right]$
Slope condition: $G_{NF_w} < 0$ and $G_{FN_w} > 0$			
$D_1 + D_2$	$= 1$	< 1	> 1
Pattern			
I'_{L1B}	$\frac{T_s V_{in}}{2(1-k^2)L_1}[-D_1 + k\sqrt{\frac{L_1}{L_2}}D_2]$	$\frac{T_s V_{in}}{2(1-k^2)L_1}[-D_1 + k\sqrt{\frac{L_1}{L_2}}D_2]$	$\frac{T_s V_{in}}{2(1-k^2)L_1}[-D_1 + k\sqrt{\frac{L_1}{L_2}}D_2]$
I'_{L2B}	$\frac{T_s V_{in}}{2(1-k^2)L_2}[D_2 - k\sqrt{\frac{L_2}{L_1}}D_1]$	$\frac{T_s V_{in}}{2(1-k^2)L_2}[D_2 - k\sqrt{\frac{L_2}{L_1}}D_1]$	$\frac{T_s V_{in}}{2(1-k^2)L_2}[D_2 - k\sqrt{\frac{L_2}{L_1}}D_1]$

or only one at a time, the analysis is same. The average value calculation procedure is same.

7.3.1 Simulation Results

The analysis is validated by simulating CI-SIDO boost converter in MATLAB/Simulink. The values of I_{L1B}, I_{L2B}, I'_{L1B} and I'_{L2B} are compared for different values of duty ratios and slope conditions. The simulations are done for different values of D_t. The parameters of the converter used for simulations are presented in Table 7.4.

Table 7.4: Simulation parameters

V_{in}	10 V	L_1	154.56 μH	L_2	100.00 μH	k	0.8	C_1, C_2	100 μF

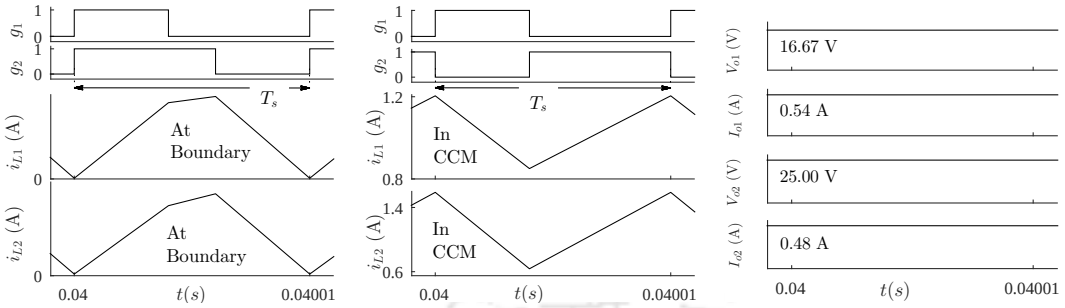


Figure 7.16: MATLAB results for $D_1 < D_2$, $D_1 + D_2 = 1$ when $G_{NF1} < 0$, $G_{FN1} > 0$, $G_{NF2} < 0$ and $G_{FN2} > 0$ ($D_1 = 0.4$ and $D_2 = 0.6$) for (a) $D_t = 0$ where i_{L1} and i_{L2} at boundary, (b) $D_t = 0.4$ where i_{L1} and i_{L2} in CCM, (c) Load currents and voltages remain same as D_t is changed.

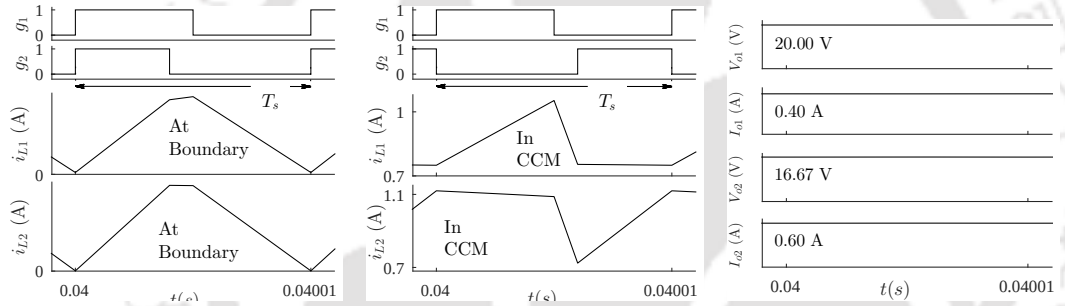


Figure 7.17: MATLAB results for $D_1 > D_2$, $D_1 + D_2 < 1$ when $G_{NF1} > 0$, $G_{FN1} < 0$, $G_{NF2} < 0$ and $G_{FN2} > 0$ ($D_1 = 0.5$ and $D_2 = 0.4$) for (a) $D_t = 0$ where i_{L1} and i_{L2} at boundary, (b) $D_t = 0.6$ where i_{L1} and i_{L2} in CCM, (c) Load currents and voltages remain same as D_t is changed.

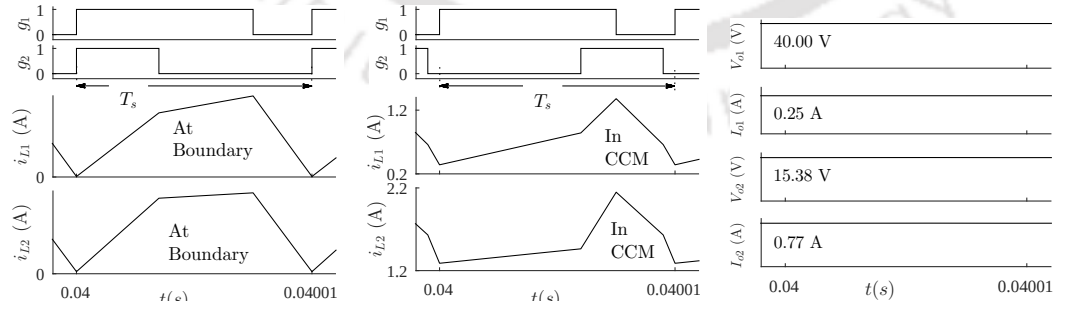
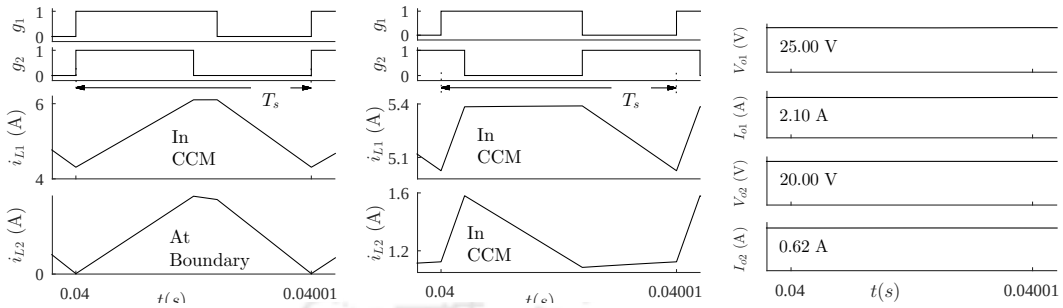


Figure 7.18: MATLAB results for $D_1 > D_2$, $D_1 + D_2 > 1$ when $G_{NF1} > 0$, $G_{FN1} < 0$, $G_{NF2} > 0$ and $G_{FN2} < 0$ ($D_1 = 0.75$ and $D_2 = 0.35$) for (a) $D_t = 0$ where i_{L1} and i_{L2} at boundary, (b) $D_t = 0.6$ where i_{L1} and i_{L2} in CCM, (c) Load currents and voltages remain same as D_t is changed.



(a) (b) (c)

Figure 7.19: MATLAB results for $D_1 > D_2$, $D_1 + D_2 > 1$ when $G_{NF1} > 0$, $G_{FN1} < 0$, $G_{NF2} < 0$ and $G_{FN2} > 0$ ($D_1 = 0.6$ and $D_2 = 0.5$) for (a) $D_t = 0$ where only i_{L2} at boundary while i_{L1} in CCM, (b) $D_t = 0.6$ where i_{L1} and i_{L2} in CCM, (c) Load currents and voltages remain same as D_t is changed.

The simulation results are shown for different duty ratios and slope conditions. The results for $D_1 = 0.4$ and $D_2 = 0.6$ are shown in Fig. 7.16 where $D_1 < D_2$, $D_1 + D_2 = 1$ and slope conditions are - $G_{NF_1} < 0$, $G_{FN_1} > 0$, $G_{NF_2} < 0$, $G_{FN_2} > 0$. The results show that for same $I_{o1} = 0.54A$, $V_{o1} = 16.67V$, $I_{o2} = 0.48A$ and $V_{o2} = 25V$ (Fig. 7.16(c)), i_{L1} and i_{L2} are at boundary for $D_t = 0$ (Fig. 7.16(a)), and, in CCM for $D_t = 0.4$ (Fig. 7.16(b)). Thus, as D_t varies from 0 to 0.4, the currents are changing from boundary to CCM for same load currents. Similar results are shown in Fig. 7.17 for $D_1 > D_2$, $D_1 + D_2 < 1$ and slope conditions are - $G_{NF_1} > 0$, $G_{FN_1} < 0$, $G_{NF_2} < 0$, $G_{FN_2} > 0$. The results for $D_1 > D_2$, $D_1 + D_2 > 1$ and slope conditions - $G_{NF_1} > 0$, $G_{FN_1} < 0$, $G_{NF_2} > 0$, $G_{FN_2} < 0$ are shown in Fig. 7.18 where D_t is changed to 0.6. The analysis is also true when only one current is at boundary and the other in CCM, as shown in Fig. 7.19. In all the cases, the boundary value is reducing as D_t is varied.

The values for I_{L1B}, I_{L2B}, I'_{L1B} and I'_{L2B} are calculated for different values of D_1 and D_2 and the results are compared, as presented in Table 7.5. The results are shown for $D_t = D_1$. The comparisons show that there is significant reduction in average values of inductor currents at CCM/DCM boundary as D_t is changed from 0 to D_1.

In previous sections, the effect of shifting is studied on the boundary value of the CI-SIDO boost converter. The study shows that with shifting, the average value of inductor current at boundary decreases up to a minimum value of shift, then it increases as shifting is increased further. The analysis shows the plot of the average value of inductor currents at the boundary with respect to the

Table 7.5: Comparison of average values of i_{L1} and i_{L2} at CCM/DCM boundary for $D_t = 0$ and $D_t = D_1$.

Sl. No	D_1	D_2	$I_{L1B}\ (A)$	$I'_{L1B}\ (A)$	$I_{L2B}\ (A)$	$I'_{L2B}\ (A)$
1	0.4	0.6	0.8957	0.1768	1.1908	0.4758
2	0.55	0.45	0.8964	0.0921	1.1166	0.1334
3	0.7	0.3	0.8971	0.3609	1.0423	0.2089
4	0.7	0.2	0.8078	0.4950	0.9034	0.4173
5	0.3	0.6	0.8058	0.2667	1.1015	0.5652
6	0.5	0.4	0.8068	0.2121	1.0024	0.1087
7	0.8	0.3	0.9870	0.6295	1.1317	0.5761
8	0.3	0.9	1.0739	0.5348	1.5181	0.9819
9	0.55	0.5	0.9411	0.1367	1.1860	0.2029

Table 7.6: Experimental parameters

L_1	$230.0\ \mu H$	L_2	$90.00\ \mu H$	k	0.88	C_1, C_2	$100\ \mu F$

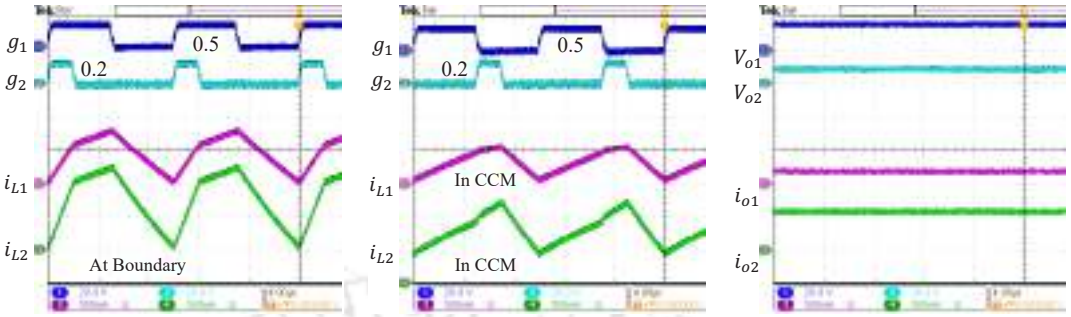
shift. However, the value of shift where the boundary is minimum is not found.

7.3.2 Experimental Results

The analysis is validated by experiments of CI-SIDO boost converter. The parameters of the converter used for experiments are presented in Table 7.6. The experimental results are shown for different duty ratios and slope conditions. The results for $D_1 = 0.5$ and $D_2 = 0.2$, $V_{in} = 8\ V$ are shown in Fig. 7.20 where $D_1 > D_2$, $D_1 + D_2 < 1$ and slope conditions are- $G_{NF1} > 0$, $G_{FN1} > 0$, $G_{NF2} > 0$, $G_{FN2} > 0$. The results show that for same $I_{o1} = 0.20\ A$, $V_{o1} = 16.00\ V$, $I_{o2} = 0.67\ A$ and $V_{o2} = 10\ V$ (Fig. 7.20), i_{L1} and i_{L2} are at boundary for $D_t = 0$ (Fig. 7.20(a)), and in CCM for $D_t = 0.5$ (Fig. 7.20(b)). Thus, as D_t varies from 0 to 0.5, the currents are changing from boundary to CCM for same load currents. Similar results are shown in Fig. 7.21 for $D_1 < D_2$, $D_1 + D_2 > 1$ and slope conditions are- $G_{NF1} < 0$, $G_{FN1} > 0$, $G_{NF2} < 0$, $G_{FN2} > 0$. The results for $D_1 < D_2$, $D_1 + D_2 < 1$ and slope conditions- $G_{NF1} > 0$, $G_{FN1} > 0$, $G_{NF2} < 0$, $G_{FN2} > 0$ are shown in Fig. 7.22 where D_t is changed to 0.5. In all the cases, the boundary value is reducing as D_t is varied.

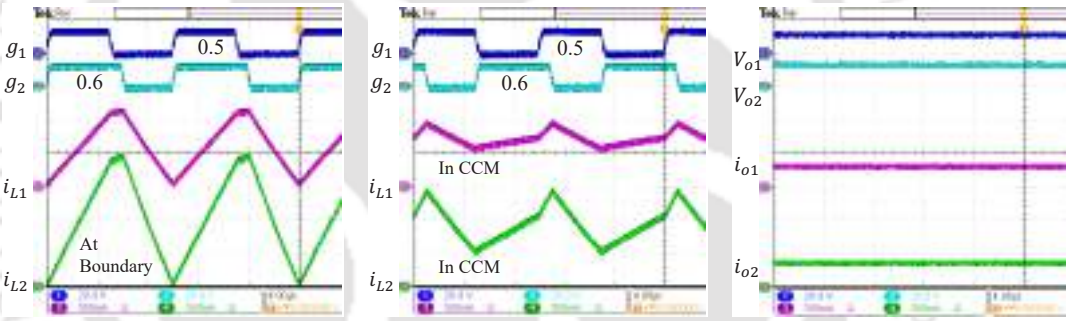
7.4 Minimizing CCM/DCM Boundary by Shifting of Gate Pulse

The gate pulse shift is found where the average value of inductor current at CCM/DCM boundary is minimum for all 36 conditions of CI-SIDO boost converter. For each case, the average values of inductor current at the CCM/DCM boundary are found as the gate pulse varies from 0 to 1. The average values of inductor current are compared amongst themselves to find the minimum value



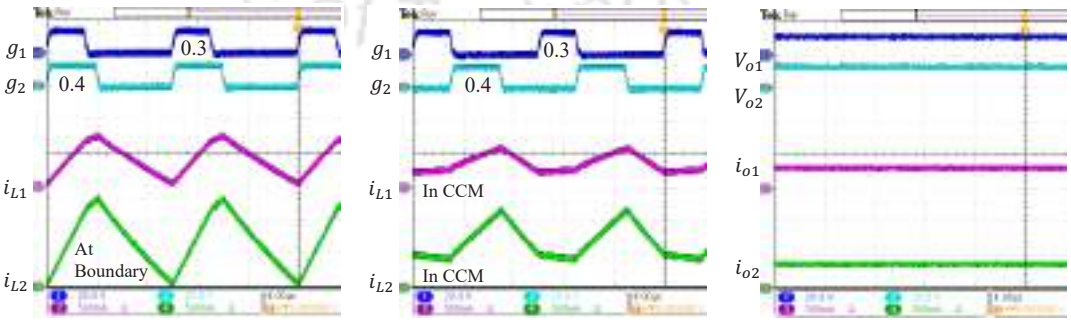
(a) (b) (c)

Figure 7.20: Experimental results for $D_1 > D_2$, $D_1 + D_2 < 1$ when $G_{NF1} > 0$, $G_{FN1} > 0$, $G_{NF2} > 0$ and $G_{FN2} > 0$ for (a) $D_t = 0$ where i_{L1} and i_{L2} at boundary, (b) $D_t = 0.5$ where i_{L1} and i_{L2} in CCM, (c) Load currents and voltages remain same as D_t is changed.



(a) (b) (c)

Figure 7.21: Experimental results for $D_1 < D_2$, $D_1 + D_2 > 1$ when $G_{NF1} < 0$, $G_{FN1} > 0$, $G_{NF2} < 0$ and $G_{FN2} > 0$ for (a) $D_t = 0$ where i_{L1} and i_{L2} at boundary, (b) $D_t = 0.5$ where i_{L1} and i_{L2} in CCM, (c) Load currents and voltages remain same as D_t is changed.



(a) (b) (c)

Figure 7.22: Experimental results for $D_1 < D_2$, $D_1 + D_2 < 1$ when $G_{NF1} > 0$, $G_{FN1} > 0$, $G_{NF2} < 0$ and $G_{FN2} > 0$ for (a) $D_t = 0$ where i_{L1} and i_{L2} at boundary, (b) $D_t = 0.5$ where i_{L1} and i_{L2} in CCM, (c) Load currents and voltages remain same as D_t is changed.

of average inductor current. The gate pulse shift corresponding to the minimum average inductor current is found for all 36 conditions. Based on the analysis, the critical inductances are found at CCM/DCM boundary. If the inductors are selected greater than these critical inductance values, the CCM operation of the converter is ensured.

This section finds the average values of inductor current at the boundary for different values of shifts. These values are then compared to find $I'_{LwB_{mn}}$. This analysis is done for all 36 possibilities of inductor currents.

As the gate pulse is shifted, the CCM/DCM boundary of the CI-SIDO boost is disturbed. This section aims to maintain the CI-SIDO boost at CCM/DCM boundary at all the values of gate pulse shift. Therefore, to keep the converter at CCM/DCM boundary for all the possible gate pulse shift, loads of the converter is changed as D_t is varied. It is to be noted that the change in loads does not change the slopes and patterns of the inductor currents as discussed in Chapter-4. The following sub-section finds the expressions of average inductor currents at CCM/DCM boundaries, I'_{LwB} at different gate pulse shift, D_t.

7.4.1 Finding Expressions of I'_{LwB} for Different D_t

Out of 36 conditions, one condition is selected at a time. For the given value of duty ratios, the value of gate pulse shift D_t is varied from 0 to 1. At each D_t, the inductor current is operated at CCM/DCM boundary. As D_t is changed, the loads are also changed such that both inductor currents are operated at CCM/DCM boundary. Then the area under curve is found at each D_t using (7.12).

$$I'_{LwB} = \frac{1}{T_s}\int_0^{T_s} i_{LwB}dt \tag{7.12}$$

Here, an example of $D_1 < D_2$ and $D_1 + D_2 < 1$ is taken with slope condition $G_{NNw} > 0$, $G_{FFw} < 0$, $G_{NFw} > 0$, $G_{FNw} > 0$, as shown in Fig. 7.23. The CCM/DCM boundary expressions at $D_t = 0$ is given by–

$$I_{LwB} = \frac{T_s}{2}\left[\, G_{NN_w} D_1 \left(D_2 - D_1 + 1\right) + G_{FN_w}\left(1 - D_1\right)\left(D_2 - D_1\right) \,\right]. \tag{7.13}$$

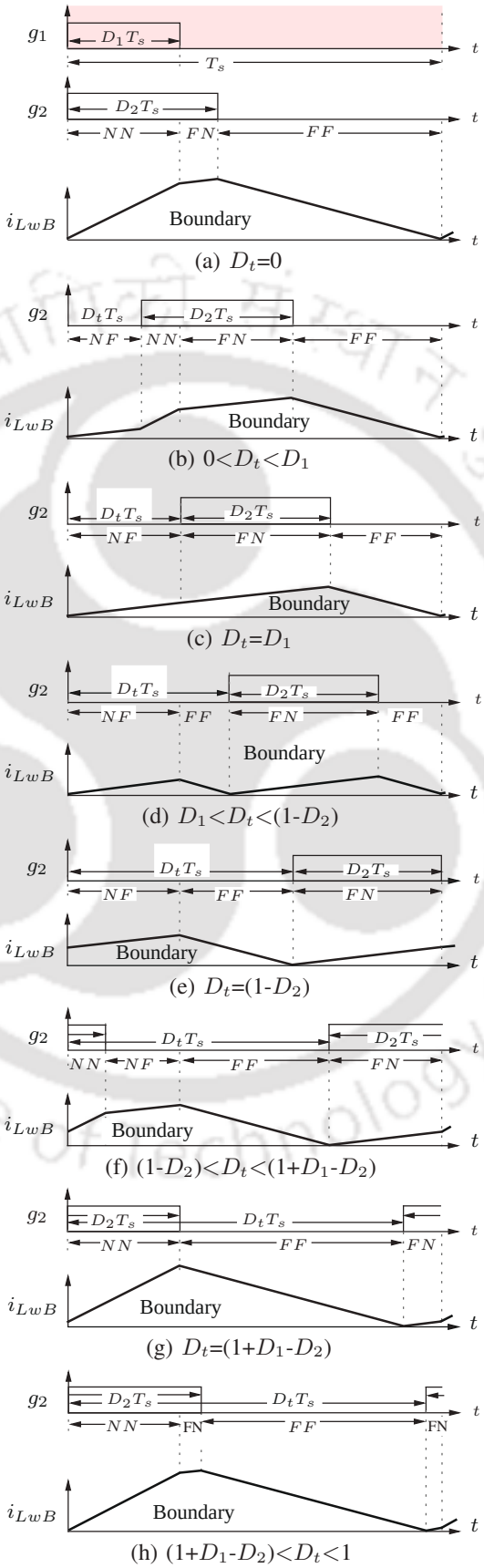


Figure 7.23: The inductor current waveforms at CCM/DCM boundary as D_t is varied from 0 to 1.

Table 7.7: Expressions of I'_{LwB} for $D_1 < D_2$ and $D_1 + D_2 < 1$ as D_t varies from 0 to 1.

Fig. No.	I'_{LwB}
7.23(a)	$\left\{ \begin{array}{l} G_{NN_w} D_1 (D_2 - D_1 + 1) \\ +G_{FN_w} (1 - D_1)(D_2 - D_1) \end{array} \right\} \frac{T_s}{2}$
7.23(b)	$\left\{ \begin{array}{l} G_{NN_w} (D_1 - D_t)(D_2 - D_1 + 1) \\ +G_{FN_w} (D_t + D_2 - D_1)(1 - D_1) \\ +G_{NF_w} D_t (D_2 + 1) \end{array} \right\} \frac{T_s}{2}$
7.23(c)	$\{G_{FN_w} D_2 (1 - D_1) + G_{NF_w} D_1 (D_2 + 1)\} \frac{T_s}{2}$
7.23(d)	$\left\{G_{FN_w} D_2 (D_2 + \overline{D_{PP_w}}) + G_{NF_w} D_1 (D_1 + \overline{D_{PP1}})\right\} \frac{T_s}{2}$
7.23(e)	$\{G_{FN_w} D_2 (1 + D_1) + G_{NF_w} D_1 (1 - D_2)\} \frac{T_s}{2}$
7.23(f)	$\left\{ \begin{array}{l} G_{NN_w} (D_t + D_2 - 1)(D_1 - D_2 + 1) \\ +G_{FN_w} (1 + D_1)(1 - D_t) \\ +G_{NF_w} (D_1 - D_t - D_2 + 1)(1 - D_2) \end{array} \right\} \frac{T_s}{2}$
7.23(g)	$\left\{ \begin{array}{l} G_{NN_w} D_1 (D_1 - D_2 + 1) \\ +G_{FN_w} (D_2 - D_1)(1 + D_1) \end{array} \right\} \frac{T_s}{2}$
7.23(h)	$\left\{ \begin{array}{l} G_{NN_w} D_1 (D_2 - D_1 + 2D_t - 1) \\ +G_{FN_w} \left(D_1 + D_2 + D_1^2 - D_1 D_2 - 2D_1 D_t\right) \end{array} \right\} \frac{T_s}{2}$

As the gate pulse shifts in the range $0 < D_t < D_1$, the converter changes to CCM. To operate the converter at CCM/DCM boundary, R_1 and R_2 are changed. The CCM/DCM boundary expression is given by–

$$I'_{LwB} = \frac{T_s}{2} \left[\; G_{NN_w} (D_1 - D_t)(D_2 - D_1 + 1) + G_{FN_w} (D_t + D_2 - D_1)(1 - D_1) + G_{NF_w} D_t (D_2 + 1) \; \right]. \tag{7.14}$$

Similarly, the expressions of I'_{LwB} are formulated as D_t is varied from 0 to 1 for $D_1 < D_2$ and $D_1 + D_2 < 1$. The obtained expressions are presented in Table 7.7. The rows represents the figure number corresponding to each shift. The column represents the average values of the inductor currents at CCM/DCM boundary. The table is presented to show the effect of gate pulse shift on the CCM/DCM boundary of the CI-SIDO boost converter and on the analytical expressions of the inductor current average values at CCM/DCM boundary. It is found that the area under curve depends on the following–

- the slope of inductor current in the states corresponding to the shift.
- duration of the states corresponding to the shift.

It is found that the magnitude of G_{NNw} is greater than magnitude of G_{NFw}, G_{FNw} if $G_{NFw} > 0, G_{FNw} > 0$ and magnitude of G_{FFw} is greater than magnitude of G_{NFw}, G_{FNw} if $G_{NFw} < 0, G_{FNw} < 0$. So, the area under curve is lower for lower values of slopes. If the value of slope is lower, the area under curve of inductor current waveforms are also lower.

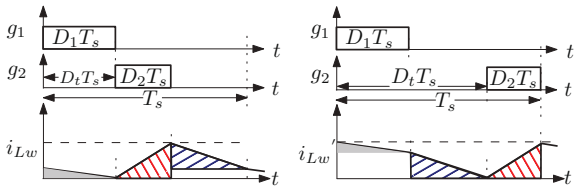


Figure 7.24: Graphical comparison of average values at CCM/DCM boundary within $\mathbf{D}_{min}$ for $G_{NF_w} < 0$ and $G_{FN_w} > 0$.

The ripples are minimum in $\mathbf{D}_{min}$ range where slopes of inductor currents are minimum. So, I'_{LwB} is minimum in the range, $\mathbf{D}_{min}$. Within the range, $\mathbf{D}_{min}$, the average of currents can be different as D_t is changed. The value of D_t at which average of inductor current is minimum is denoted by D_m, such that $D_m \in \mathbf{D}_{min}$.

7.4.2 Finding $I'_{LwB_{mn}}$ and corresponding D_m

This subsection finds the minimum average of inductor currents at CCM/DCM boundary, $I'_{LwB_{mn}}$. The average values are formulated at different D_t which varies from 0 to 1. The average values at different shifts are compared to find the minimum average value, $I'_{LwB_{mn}}$. The expressions of I'_{LwB} which is obtained for $D_1 < D_2$ and $D_1 + D_2 < 1$, as presented in Table 7.7, are compared. The comparisons show that $I'_{LwB_{mn}}$ is obtained for Fig. 7.23(d). The value of $I'_{L1B_{mn}}$ is–

$$I'_{L1B_{mn}} = \frac{T_s V_{in}}{2(1-k^2)L_1}\left[\frac{G_{NF1}}{|G_{FF1}|}\frac{D_1^2}{(1-D_1)} + k\sqrt{\frac{L_1}{L_2}}\frac{G_{FN1}}{|G_{FF1}|}\frac{D_2^2}{(1-D_2)}\right]. \tag{7.15}$$

The value of $I'_{L2B_{mn}}$ is–

$$I'_{L2B_{mn}} = \frac{T_s V_{in}}{2(1-k^2)L_2}\left[k\sqrt{\frac{L_2}{L_1}}\frac{G_{NF2}}{|G_{FF2}|}\frac{D_1^2}{(1-D_1)} + \frac{G_{FN2}}{|G_{FF2}|}\frac{D_2^2}{(1-D_2)}\right]. \tag{7.16}$$

The corresponding values of gate pulse shift are–

$$D_m = \begin{cases} D_1 + \overline{D_{PPw}} & \text{if } G_{NF_w}D_1T_s > G_{FN_w}D_2T_s \\ D_1 + \underline{D_{PPw}} & \text{if } G_{NF_w}D_1T_s < G_{FN_w}D_2T_s \end{cases} \tag{7.17}$$

where $\underline{D_{PP_w}}$, $\overline{D_{PP_w}}$ are presented in Table 4.7.

The analysis shows that $I'_{LwB_{mn}}$ lies in range $\mathbf{D}_{min}$. So, for different values of duty ratios and slope conditions, the graphical comparisons of I_{LwB} are done within $\mathbf{D}_{min}$. An example is shown in Fig. 7.24 with $G_{NF_w} < 0$ and $G_{FN_w} > 0$, $D_1 > D_2$. The comparison shown that extra areas with value

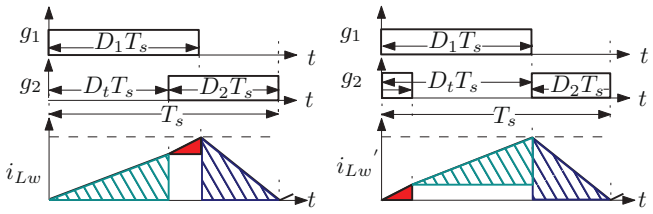


Figure 7.25: Graphical comparison of average values at CCM/DCM boundary within $\mathbf{D}_{min}$ for $G_{NF_w} > 0$ and $G_{FN_w} < 0$.

$(|G_{FF_w}|-|G_{NF_w}|)D_1T_s(1-D_1-D_2)T_s$ occurs at $D_t = 1-D_2$. Therefore, minimum CCM/DCM boundary occurs at D_1. Similarly, Fig. 7.25 shows that extra $(G_{NN_w} - G_{NF_w})(1 - D_2)T_s(D_1 + D_2 - 1)T_s$ occurs at $D_t = D_1$, so that minimum CCM/DCM boundary occurs at $1 - D_2$. The value of D_m for all 36 cases of CI-SIDO boost are presented in Table 7.8 where the average value of inductor currents at boundary is minimum. The values of $I'_{LwB_{mn}}$ for all 36 cases are presented in Table 7.9. The rows of Table 7.8 and Table 7.9 represent the possible slope conditions of CI-SIDO boost converter. The columns of Table 7.8 represent the gate pulse shift where average values of inductor current at CCM/DCM boundary is minimum whereas the minimum analytical expressions are presented in fourth column of Table 7.9.

Table 7.8: D_m in 36 conditions of CI-SIDO boost

Slope conditions		$(D_1 + D_2)$	D_m
G_{NF_w}	G_{FN_w}		
< 0	> 0	$>, <, = 1$	D_1
$= 0$	> 0	< 1	
< 0	$= 0$	> 1	
> 0	< 0	$>, <, = 1$	$1 - D_2$
> 0	$= 0$	< 1	
$= 0$	< 0	> 1	
> 0	> 0	< 1	$D_1 + \overline{D_{PP_w}}$ if $G_{NF_w}D_1 > G_{FN_w}D_2$ else $D_1 + \underline{D_{PP_w}}$
< 0	< 0	> 1	$D_1 - \underline{D_{NN_w}}$ if $\|G_{NF_w}\|(1 - D_2) > \|G_{FN_w}\|(1 - D_1)$ else $D_1 - \overline{D_{NN_w}}$

Table 7.9: $I'_{LwB_{mn}}$ in various conditions

Slope conditions		$(D_1 + D_2)$	$2\underline{I_{LwB}}/T_s$
G_{NF_w}	G_{FN_w}		
> 0	> 0	< 1	$G_{NFw}D_1^2\left[1 + \frac{G_{NFw}}{\|G_{FFw}\|}\right] + G_{FNw}D_2^2\left[1 + \frac{G_{FNw}}{\|G_{FFw}\|}\right]$
< 0	< 0	> 1	$G_{NFw}(1-D_2)^2\left[1 + \frac{\|G_{NFw}\|}{G_{NNw}}\right] + G_{FNw}(1-D_1)^2\left[1 + \frac{\|G_{FNw}\|}{G_{NNw}}\right]$
> 0	< 0	$>, <, = 1$	$G_{NFw}D_1(1-D_2) + \|G_{FNw}\|D_2(1-D_1)$
< 0	> 0	$>, <, = 1$	$\|G_{NFw}\|D_1(1-D_2) + G_{FNw}D_2(1-D_1)$
$= 0$	< 0	> 1	$G_{NNw}D_2(D_1 + D_2 - 1)$
$= 0$	> 0	< 1	$G_{FNw}D_2(1 - D_1)$
> 0	$= 0$	< 1	$G_{NFw}D_1(1 - D_2)$
< 0	$= 0$	> 1	$G_{NNw}(1 - D_2)(D_1 + D_2 - 1)$

7.4.3 Usability Analysis

The advantages of the gate pulse shift on the CCM/DCM boundary of the CI-SIDO boost converter is explained using the following examples.

Example 1: For the following specifications of the CI-SIDO boost converter, find the effect of gate pulse shift on the CCM/DCM boundary currents and powers. $V_{in} = 10\ V$, $L_1 = 100\ \mu H$, $L_2 = 155\ \mu H$, $k = 0.8$, $V_{o1} = 16.67\ V$, $V_{o2} = 20\ V$, $T_s = 10\ \mu s$.

Solution: With the given specifications, $D_1 = 0.4$ and $D_2 = 0.5$. Using (7.6) and (7.7), $I_{L1B} = 1\ A$ and $I_{L2B} = 1.25\ A$. The corresponding load currents are $I_{o1B} = 0.6\ A$ and $I_{o2B} = 0.625\ A$. Now, the gate pulse g_2 is shifted by 0.5. The value of $I'_{L1B} = 0.11\ A$ and $I'_{o1B} = 0.07\ A$. Therefore, we observe that the boundary i_{o1} decreases from 0.6 A to 0.07 A, i.e., boundary power 10 W to 1.17 W. Similarly, if we shift g_2 by 0.4, the value of $I'_{L2B} = 0.09\ A$ and $I'_{o2B} = 0.045\ A$. The boundary i_{o2} decreases from 0.625 A to 0.045 , i.e., boundary power 12.5 W to 0.9 W. Therefore, we observe that there are significant reduction in the boundary currents and powers as the gate pulse is shifted.

Example 2: Suppose the CI-SIDO boost converter is to be maintained in CCM above 50 W. The input voltage available is 12 V. The output voltages to be maintained are 30 V, 20 V. Find the lowest critical inductors, L_{cr1}, L_{cr2} such that CCM operations are ensured above 50 W.

Solution: For $V_{in} = 12\ V$, $V_{o1} = 30\ V$, $V_{o2} = 20\ V$, the duty ratios obtained are $D_1 = 0.6$ and $D_2 = 0.4$. Lets assume $k = 0.8$ and $\frac{L_1}{L_2} = 2.5$. As the CI-SIDO boost converter reaches boundary at 50 W, the boundary load currents obtained are– $i_{o1B} = 1.67\ A$ and $i_{o2B} = 2.5\ A$. The corresponding I'_{L1B} and I'_{L2B} are 4.167 and 4.167. Using the expressions of I'_{L1B}, L_{cr1} obtained is 3.76 μH. Since $\frac{L_1}{L_2} = 2.5$, the corresponding L_{cr2} obtained is 1.5 μH. In this case, the value of I'_{L2B} is 10.68 A.

Using the expressions of I'_{L2B}, L_{cr2} obtained is 3.86 μH. Since $\frac{L_1}{L_2} = 2.5$, the corresponding L_{cr1} obtained is 9.64 μH. In this case, the value of I'_{L1B} is 1.62 A. As the values of I'_{L1B} and I'_{L2B} are minimum for the second case, we choose $L_{cr1} = 3.86\ \mu H$ and $L_{cr2} = 9.64\ \mu H$. Therefore, to maintain the CI-SIDO boost converter in CCM, the inductance values should be above these critical values.

Keeping all the circuit conditions same, the critical inductance values at $D_t = 0$ are $L_{cr1} = 70.36\ \mu H$ and $L_{cr2} = 28.14\ \mu H$. Therefore, we observe that L_{cr1} has reduced from 70.36 μH to 3.86 μH. Similarly, L_{cr2} has reduced from 28.14 μH to 9.64 μH.

Table 7.10: Simulation parameters

V_{in}	5 V	k	0.8	L_1	120.00 μH	L_2	48.00 μH	C_1	100 μF	C_2	100 μF

The analysis presented above is still valid if the input/output voltage/current/power demand changes. It is again presented in Example-3.

Example 3: For $V_{in} = 4\ V$, $V_{o1} = 6.67\ V$, $V_{o2} = 8\ V$, the duty ratios obtained are $D_1 = 0.4$ and $D_2 = 0.5$. Lets assume $k = 0.7$ and $\frac{L_1}{L_2} = 0.5$. As the CI-SIDO boost converter reaches boundary at 100 W, the boundary load currents obtained are– $i_{o1B} = 15\ A$ and $i_{o2B} = 12.5\ A$. The corresponding I'_{L1B} and I'_{L2B} are 25 A. Using the expressions of I'_{L1B}, L_{cr1} obtained is 0.24 μH. Since $\frac{L_1}{L_2} = 0.5$, the corresponding L_{cr2} obtained is 0.48 μH. In this case, the value of I'_{L2B} is 8.53 A.

Using the expressions of I'_{L2B}, L_{cr2} obtained is 0.16 μH. Since $\frac{L_1}{L_2} = 0.5$, the corresponding L_{cr1} obtained is 0.08 μH. In this case, the value of I'_{L1B} is 73.31 A. As the values of I'_{L1B} and I'_{L2B} are minimum for the first case, we choose $L_{cr1} = 0.24\ \mu H$ and $L_{cr2} = 0.48\ \mu H$. Therefore, to maintain the CI-SIDO boost converter in CCM, the inductance values should be above these critical values.

Keeping all the circuit conditions same, the critical inductance values at $D_t = 0$ are $L_{cr1} = 1.06\ \mu H$ and $L_{cr2} = 1.4\ \mu H$. Therefore, we observe that L_{cr1} has reduced from 1.06 μH to 0.24 μH. Similarly, L_{cr2} has reduced from 1.4 μH to 0.48 μH.

Therefore, it can be observed that the analysis presented in the thesis is applicable to all possible values of duty ratios, input/output voltage/current/power demand changes. The analysis actually helps to design the CI-SIDO converters at the optimum design conditions.

7.4.4 Simulation and Experimental Results

A laboratory prototype of a CI-SIDO boost converter is designed in the laboratory, which is shown in Fig. 3.4(b). The converter is designed using MOSFETs with part number IRFP90N20DPBF and diodes with part number RHRP30120. The converter parameters are presented in Table 7.10. The gate pulse is generated using FPGA kit– NI sbRIO 9637. Using current and differential probes, the current and voltage waveforms are measured in a mixed domain oscilloscope (MDO). This section presents the trend of the average values of inductor currents at the boundary as D_t varies from 0 to 1. This section also compares the CCM/DCM boundary load currents for $D_t = 0$ and $D_t = D_m$

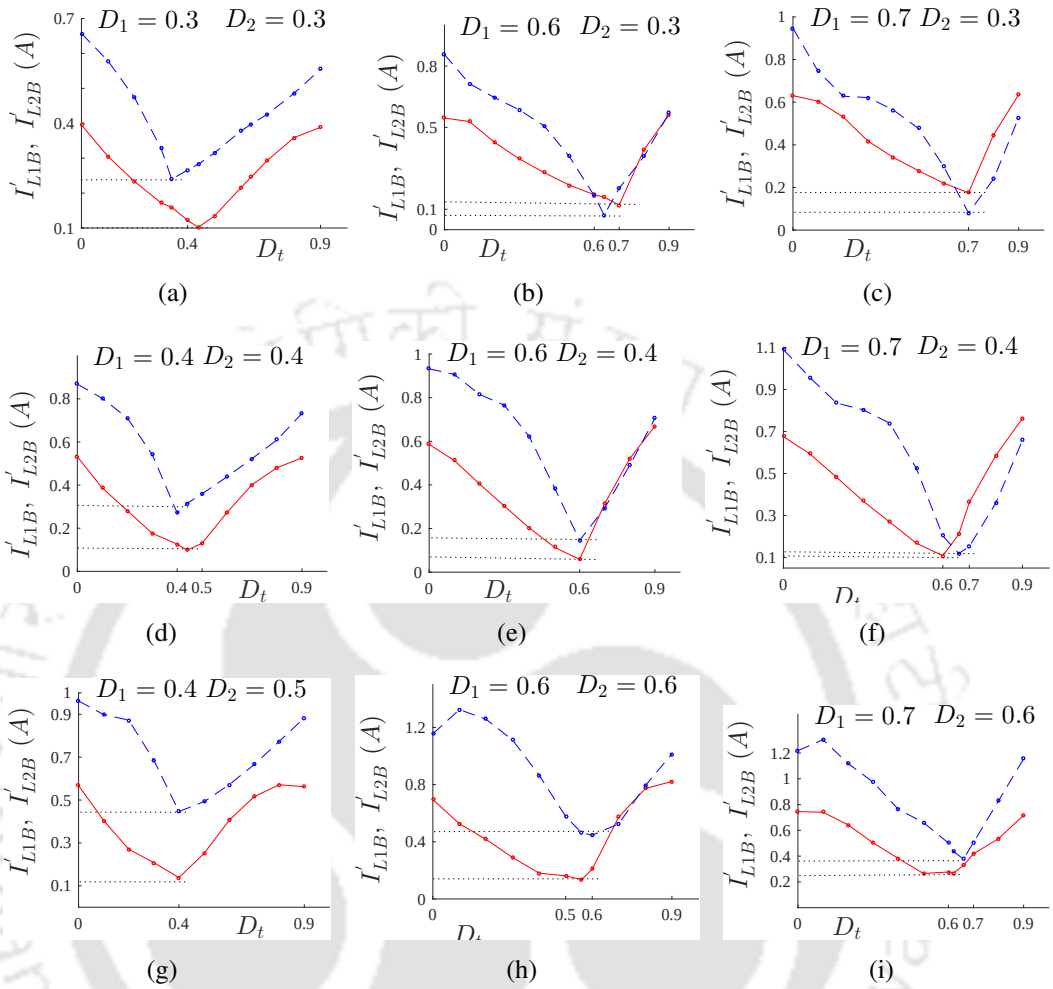
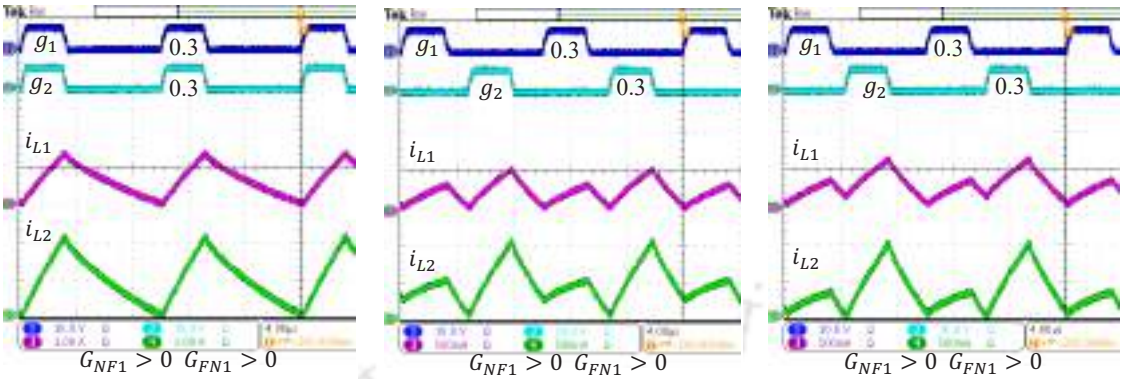


Figure 7.26: Reduction of I'_{LwB} as D_t varies from 0 to 1 for Sector (a) 1, (b) 2, (c) 3, (d) 4, (e) 5, (f) 6, (g) 7, (h) 8, (i) 9.

experimentally.

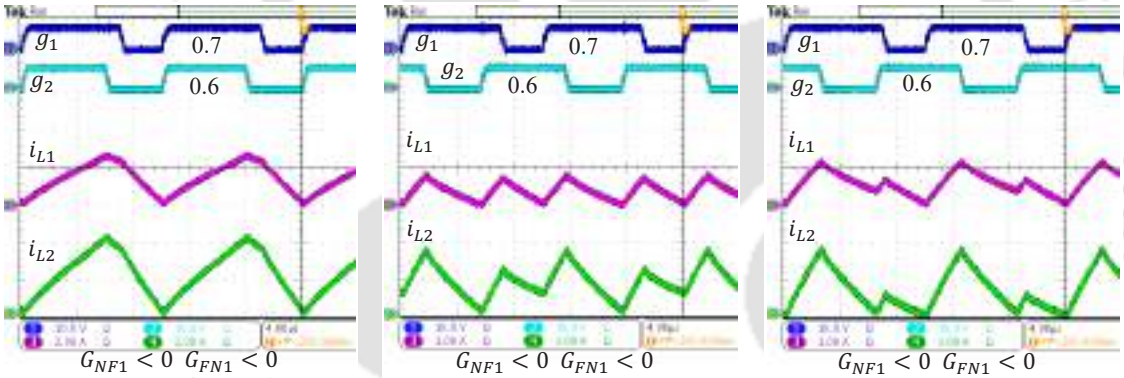
For the selected coupled inductor in Table 7.10, the sectors are formed as shown in Fig. 3.2. The values of r_{NF1}, r_{NF2}, r_{FN1}, r_{FN2} obtained are 0.44, 0.34, 0.56, and 0.66. By changing the duty ratios, the converter is operated in different sectors. For each sector, the average values of inductor currents at CCM/DCM boundary is found in Matlab simulations as D_t varies from 0 to 1. The plots of I'_{L1B} and I'_{L2B} versus D_t for all the sectors are shown in Fig. 7.26. The trends show that the average values are minimum for a particular value of D_t, called D_m. The shift, D_m is same as obtained in Table 7.8.

The experimental results are presented for four slope conditions of CI-SIDO boost converter. For $D_1 = 0.3$ and $D_2 = 0.3$ in Fig. 7.27(a), the CI-SIDO boost converter operates in Sector 1 with slope conditions – $G_{NF1} > 0$, $G_{FN1} > 0$, $G_{NF2} > 0$, $G_{FN2} > 0$. When $D_t = 0$, the CI-SIDO boost converter



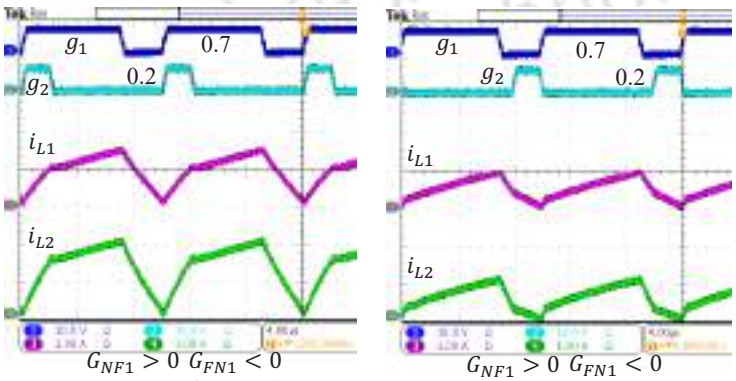
(a) $i_{o1B} = 0.40\ A$, $i_{o2B} = 0.60\ A$ (b) $i_{o1B} = 0.15\ A$, $i_{o2B} = 0.30\ A$ (c) $i_{o1B} = 0.20\ A$, $i_{o2B} = 0.20\ A$

Figure 7.27: The inductor current waveforms at CCM/DCM boundary for (a) $D_t = 0$, (b) $D_t = 0.47$, and (c) $D_t = 0.42$.



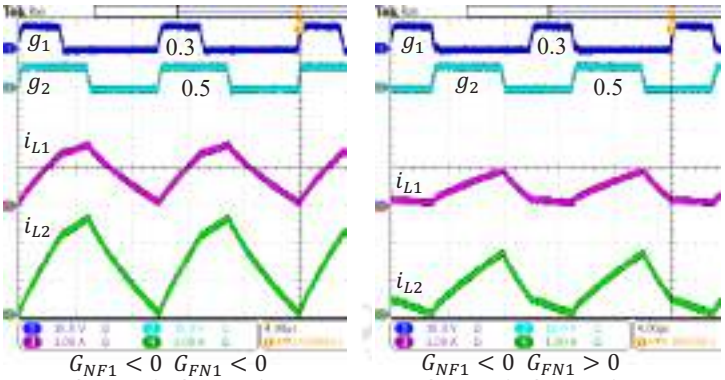
(a) $i_{o1B} = 0.30\ A$, $i_{o2B} = 0.80\ A$ (b) $i_{o1B} = 0.10\ A$, $i_{o2B} = 0.32\ A$ (c) $i_{o1B} = 0.10\ A$, $i_{o2B} = 0.30\ A$

Figure 7.28: The inductor current waveforms at CCM/DCM boundary for (a) $D_t = 0$, (b) $D_t = 0.56$, and (c) $D_t = 0.65$.



(a) $i_{o1B} = 0.20\ A$, $i_{o2B} = 1.0\ A$ (b) $i_{o1B} = 0.12\ A$, $i_{o2B} = 0.48\ A$

Figure 7.29: The inductor current waveforms at CCM/DCM boundary for (a) $D_t = 0$, (b) $D_t = 0.8$.



(a) $i_{o1B} = 0.60\ A$, $i_{o2B} = 0.60\ A$ (b) $i_{o1B} = 0.40\ A$, $i_{o2B} = 0.20\ A$

Figure 7.30: The inductor current waveforms at CCM/DCM boundary for (a) $D_t = 0$, (b) $D_t = 0.30$.

operates at CCM/DCM boundary with $i_{o1} = 0.40\ A$, $i_{o2} = 0.60\ A$. Keeping the load currents same, if D_t changes from 0 to 0.47 (D_m for i_{L1}), the CI-SIDO boost converter changes to CCM. To operate the CI-SIDO boost converter at CCM/DCM boundary for $D_t = 0.47$, the loads need to be reduced. For $i_{o1} = 0.15\ A$, $i_{o2} = 0.30\ A$, the converter changes from CCM to CCM/DCM boundary as shown in Fig. 7.27(b). Similarly, if D_t is changed to 0.42 which is D_m for i_{L2}, the converter goes to CCM/DCM boundary for $i_{o1} = 0.20\ A$, $i_{o2} = 0.20\ A$ as shown in Fig. 7.27(c). It is found that the average values of i_{o1B} has reduced by 62.5% at $D_t = 0.47$ and 50% at $D_t = 0.42$. The average values of i_{o2B} has reduced by 50% at $D_t = 0.47$ and 66.67% at $D_t = 0.42$.

Similarly, the waveforms are shown for Sector 9 in Fig. 7.28 with slope conditions – $G_{NF1} < 0$, $G_{FN1} < 0$, $G_{FN1} < 0$, $G_{FN2} < 0$. In this case, D_m for both the currents are different. D_m for i_{L1} occurs at 0.56 as shown in Fig. 7.28(b) and D_m for i_{L2} occurs at 0.65 as shown in Fig. 7.28(c). The average values of i_{o1B} has reduced by 66.67% at both shifts $D_t = 0.56$ and $D_t = 0.65$. The average values of i_{o2B} has reduced by 60% at $D_t = 0.56$ and 62.5% at $D_t = 0.65$.

The waveforms for Sector 3 is shown in Fig. 7.29 with $G_{NF1} > 0$, $G_{FN1} < 0$, $G_{FN1} > 0$, $G_{FN2} < 0$ for $D_1 = 0.7$ and $D_1 = 0.2$. The slopes of i_{L1} and i_{L2} are same and D_m values for both the currents are same, i.e., $D_m = (1 - D_2) = 0.8$. The values of i_{o1B} is reducing from 0.20 A to 0.12 A and i_{o2B} is reducing from 1.0 A to 0.48 A. In Fig. 7.30, the waveforms are shown for $D_1 = 0.3$ and $D_2 = 0.5$ with the slope conditions $G_{NF1} < 0$, $G_{FN1} > 0$, $G_{FN1} < 0$, $G_{FN2} > 0$. Again in this case, the slopes of i_{L1} and i_{L2} are same and D_m values for both the currents are same. The value of D_m in this case is

Table 7.11: Comparison of load currents at CCM/DCM boundary for $D_t = 0$ and $D_t = D_m$.

Fig.	D_1	D_2	I_{o1B} (A)	I'_{o1B} (A)	ΔI_{o1B}	I_{o2B} (A)	I'_{o2B} (A)	ΔI_{o2B}
7.26(a)	0.3	0.3	0.27	0.07	74.07%	0.46	0.17	63.04%
7.26(b)	0.6	0.3	0.22	0.05	77.27%	0.6	0.05	91.67%
7.26(c)	0.7	0.3	0.19	0.05	73.68%	0.66	0.06	90.91%
7.26(d)	0.4	0.4	0.32	0.05	84.37%	0.52	0.16	69.23%
7.26(e)	0.6	0.4	0.24	0.02	91.67%	0.56	0.09	83.93%
7.26(f)	0.7	0.4	0.20	0.03	85%	0.65	0.07	89.23%
7.26(g)	0.4	0.5	0.34	0.08	76.47%	0.48	0.23	52.08%
7.26(h)	0.6	0.6	0.27	0.08	70.37%	0.46	0.18	60.87%
7.26(i)	0.7	0.6	0.23	0.09	60.87%	0.49	0.18	63.26%

$D_1 = 0.3$. The values of i_{o1B} is reducing from 0.60 A to 0.40 A and i_{o2B} is reducing from 0.60 A to 0.20 A.

Therefore, it is found that for Sector 1 and 9, the values of D_m are different for i_{L1} and i_{L2}. However, for Sector 3 and 7, the CCM/DCM boundaries of both the currents are minimum at the same D_m. All the experimental verifications show that the CCM/DCM boundary reduces significantly with the shift in gate pulse for all the sectors.

The reduction in average values of i_{L1} and i_{L2} at CCM/DCM boundary for $D_t = 0$ and $D_t = D_m$ are compared in Table 7.11. The percentage reduction is calculated for both i_{L1} and i_{L2} with respect to the average values of i_{L1} and i_{L2} at CCM/DCM boundary for $D_t = 0$. By only the gate pulse shifting, there is significant reduction in the average values of i_{L1} and i_{L2} at CCM/DCM boundary. For these experimental results, the maximum reduction in I_{o1B} and I_{o2B} is 91.67%.

7.5 Summary of the Chapter

The following are the findings of the chapter–

(i) For non shifted cases, the CCM/DCM boundary condition depends on duty ratios of two boost converters, however, it does not depend on its relative value, i.e. whether duty ratios are greater, smaller or equal.

(ii) With the increase in inductance value of either boost, the CCM/DCM boundary condition of the other decreases, whereas it increases with an increase in output voltage.

(iii) By introducing the gate pulse shift, the CCM/DCM boundary of the CI-SIDO boost converters

are reduced without increasing the inductance values. The shift decreases the average inductor current at CCM/DCM boundary, thus, decreasing the critical inductances of the CI-SIDO boost converter.

(iv) If the CCM/DCM boundary is known as per the application, then using the shift found in this chapter, the values of the critical inductances are reduced.

(v) The gate pulse shift, D_m is found where the average inductor current at CCM/DCM boundary is minimum for all 36 cases of CI-SIDO boost converter. The obtained D_m is presented in Table 7.8. The shift in gate pulse reduces the boundary currents and powers. The range of CCM operations are increased as the CCM/DCM boundary is decreased.

(vi) The expressions of minimum average inductor current at CCM/DCM boundary for all 36 cases are presented in Table 7.9. These expressions help to calculate the critical inductances at CCM/DCM boundaries.

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8

Effect of Coupling on Discontinuous Conduction Mode of CI-SIDO Boost Converter

Contents

8.1 Introduction

[1] The general analysis of CI-SIDO boost converter in CCM is already presented in the previous chapters. The optimum design method of CI-SIDO boost converter is proposed in Chapter-5. Power electronic converter is usually designed for rated conditions. So, the values of different passive elements (like L_1, L_2, etc.) are chosen at the design stage according to the rating of the converter. However, the converter may not operate in rated conditions always. The load of the converter may reduce while operating, leading to the DCM of the converter. Therefore, this chapter evaluates the performance of the CI-SIDO boost converter in DCM.

The CI-SIDO boost converter has two different duty ratios, output voltages, loads, and inductance values. In interleaved boost converter, the duty ratios of two phases are equal, inductance values are also equal, and the load is common. So, the DCM approach adopted for interleaved boost converter does not apply to the CI-SIDO boost converter. The number of DCM operating modes of CI-SIDO boost converter is much more than the coupled inductor interleaved boost [71]. The DCM analysis of CI-SIDO boost is compared with the interleaved boost converter in Table 8.1.

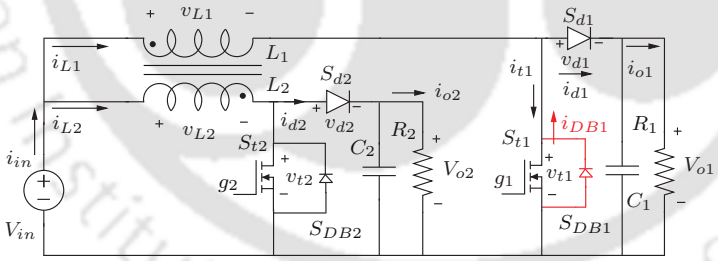


Figure 8.1: CI-SIDO boost converter when (a) S_{DB1} is ON and i_{L1} is negative (shown in red colour), (b) S_{DB1} is OFF (shown in black colour).

The chapter evaluates the effect of coupling on the DCM analysis of CI-SIDO boost (Fig. 8.1). The converter has so many different operating modes due to the coupled inductors, two different duty ratios, and two unequal loads. Furthermore, the turning ON of the body diode due to coupling further adds to the feasible operating modes. Also, the variation of input voltage affects both the boost

[1]Major part of this chapter is reproduced from my publications: (i) Nupur and S. Nath,"Effect of Coupling on Discontinuous Conduction Mode of Coupled Inductor SIDO Boost Converter" in *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 4991-5002, May 2022. (ii) Nupur and S. Nath, "Effect of Coupling on Input-Output Voltage relations in DCM of SIDO Boost Converters," in *Proc. 10th Nat. Power Electron. Conf.*, Dec. 2021. (iii) Nupur and S. Nath, "Numerous Patterns of Inductor Currents in DCM of Coupled SIDO Boost Converter" in *Proc. 47th Annu. Conf. IEEE Ind. Electron. Soc.*, Oct. 2021.

Table 8.1: Challenges in DCM analysis of CI-SIDO boost versus interleaved boost

Basis of comparison	[68, 69, 71]	this analysis
Topology	Interleaved Boost	CI-SIDO Boost
Relations between D_1, D_2, L_1, L_2	$D_1 = D_2 = D$, $L_1 = L_2 = L$	$D_1 \neq D_2$, $L_1 \neq L_2$
Output voltage	V_o is common, i.e., only one output	V_{o1}, V_{o2} are different and independent
Slopes of i_{L1}, i_{L2}	Same	Different
Number of DCM waveform patterns for i_{L1} and i_{L2}	10	21*
Forced turning ON of power diodes depend on	k	k, $\frac{L_1}{L_2}$
Turning ON of body diodes depend on	k	k, $\frac{L_1}{L_2}$
Boundaries of DCM operating modes depend on	$\frac{V_{in}}{V_o}$, k	$\frac{V_{in}}{V_{o1}}$, $\frac{V_{in}}{V_{o2}}$, $\frac{L_1}{L_2}$, k
Voltage and current stress	always less than or equal to CCM conditions	may increase or decrease depending on L_1, L_2, k
Duty ratio depends on	V_{in}, V_o, k, i_o	V_{in}, V_{o1}, V_{o2}, k, L_1, L_2, $\frac{L_1}{L_2}$, i_{o1}
Voltage gain depends on	V_{in}, V_o, k, D, i_o	V_{in}, V_{o1}, V_{o2}, k, L_1, L_2, $\frac{L_1}{L_2}$, i_{o1}, D_1, D_2

* number increases if both boost converters in DCM and gate pulse shift are considered.

converters of the CI-SIDO boost converter because of the common input. This chapter assumes that the first boost converter is in DCM while the second boost is still in CCM to show the effect of the DCM operation of the first boost on the CCM operation of the second boost. However, the approach presented in this chapter can be extended to CI-SIDO boost when both are in DCM.

The waveforms of inductor currents i_{L1}, i_{L2} and voltage across inductors v_{L1}, v_{L2} are shown in Fig. 8.2. From the figures, we found that–

- Both i_{L1} and i_{L2} are at boundary for a given load currents i_{o1} and i_{o2}, as shown in Fig. 8.2(a).
- As the load current i_{o1} decreases from the boundary condition, i_{L1} goes to DCM as shown in Fig. 8.2(b).
- As i_{L1} goes to DCM, i_{L2} shifts from boundary to CCM without any change in i_{o2} as shown in Fig. 8.2(b).
- In Fig. 8.2(b), we observe that i_{L1} is becoming negative.
- Even if i_{L2} of Fig. 8.2 is in CCM, its slope changes in state FF_{bD}.

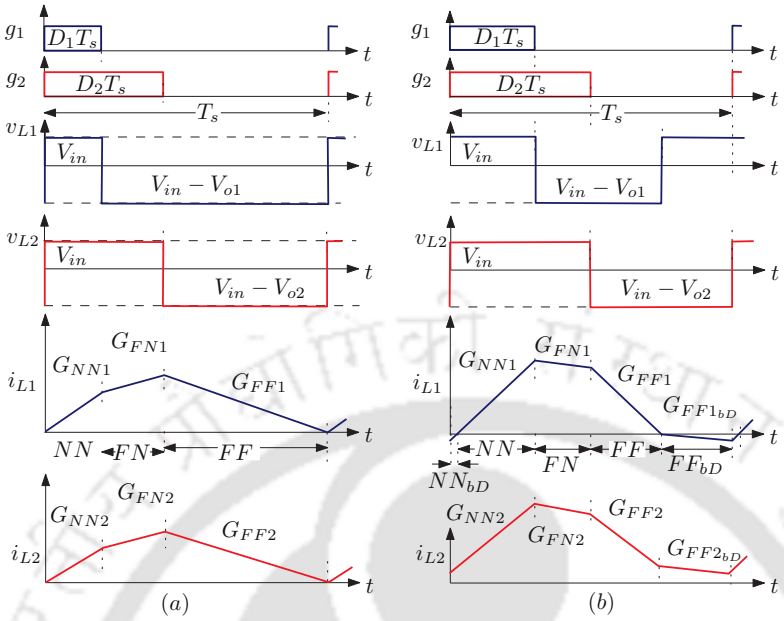


Figure 8.2: (a) Both inductor currents i_{L1} and i_{L2} are at boundary for a given load currents, (b) As the first load current decreases, i_{L1} goes to DCM. This shifts i_{L2} to CCM from boundary, without any change in the circuit.

As the load current i_{o1} decreases from the boundary condition to enter DCM, the waveforms of the inductor currents are changing. It is also observed that i_{L1} is becoming negative for some portion of the switching period. The change in the input voltage is expected to affect both the boost converters because of the common input voltage. This chapter aims to find the causes of the above behaviours of the CI-SIDO boost converter in detail. All these effects are related to the effect of coupling. Therefore, this chapter presents a detailed analysis of the CI-SIDO boost converter when the first boost is in DCM while the second boost is still in CCM. This assumption helps in better understanding the effect of coupling on DCM analysis of CI-SIDO boost converter.

It is to be noted that the CI-SIDO boost is analyzed with a non-shifted gate pulse, i.e., g_1, g_2 starts simultaneously. The advantage of the gate pulse shift is in the ripple reduction for CCM operation. In CI-SIDO boost, it is found that the value of shift where inductor current ripples are minimum is not fixed even in CCM unlike interleaved boost converters. As the CI-SIDO boost enters DCM, the inductor current waveform patterns become more complex. So, the process of finding the optimum shift for DCM is again becoming a function of several other parameters. The controller design for this type of shifting is more complex. For any controller, precisely generating this shift is going to be very difficult. Also, during DCM operation, the values of inductor currents become very small. So,

the amount of ripple is not a concern in DCM. So, to keep it simple, we have chosen to operate the converter for non-shifted gate pulse, i.e., g_1, g_2 starts simultaneously for DCM.

If the gate pulse of the CI-SIDO boost converter is given a shift, there are conditions when forced turn ON of the power diode takes place. When $v_{L2} = V_{in} - V_{o2}$, S_{d1} is not turned ON forcefully. For $v_{L2} = V_{in}$, the forced turn ON of S_{d1} takes place if (8.1) is satisfied.

$$\frac{V_{in}}{V_{o1}} > \frac{1}{(1 + k\sqrt{\frac{L_1}{L_2}})} \tag{8.1}$$

8.2 Circuit Description of CI-SIDO Boost Converter in DCM

This section presents the circuit description of the CI-SIDO boost converter, which includes the conditions of turning ON of body diodes and the formation of sectors.

8.2.1 Circuit Description of CI-SIDO Boost Converter

The topology of the CI-SIDO boost converter is shown in Fig. 8.1. The converter has two MOSFETs, S_{t1}, S_{t2}, and two diodes, S_{d1}, S_{d2}. The converter is the combination of two boost converters with a common input voltage V_{in} and two outputs V_{o1}, V_{o2}. A coupled inductor replaces the individual inductors with a coupling coefficient k, and windings L_1 and L_2. The first inductor current i_{L1} enters DCM, keeping i_{L2} in CCM. The first load current i_{o1} is varied to analyze the DCM operation of CI-SIDO boost, keeping i_{o2} unchanged. Due to the presence of coupled inductor, the body diode S_{DB1} turns ON when i_{L1} operates in DCM. When S_{DB1} turns ON, negative current flows through it, as shown in Fig. 8.1 (in red colour). When i_{L1} is positive, the current flows through S_{t1} as shown in Fig. 8.1 (in black colour).

8.2.1.1 Condition to turn ON Body Diode of MOSFET

The analysis of CI-SIDO boost converter in Fig. 8.1 is done to find the condition of turn ON of S_{DB1}. The voltage across the S_{t1} is given by $v_{t1} = V_{in} - v_{L1}$. When first boost is in DCM, $i_{L1} = 0$. So, $v_{L1} = -k\sqrt{\frac{L_1}{L_2}}v_{L2}$ where v_{L2} can take two values, i.e., V_{in} or $V_{in} - V_{o2}$ as second boost is in CCM.

Table 8.2: Slopes of inductor currents in four states when the first boost is in DCM while the second boost is in CCM

Inductor current	NN	FF	NF	FN
i_{L1}	$G_{NN1} = \frac{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)V_{in}}{(1-k^2)L_1}$	$G_{FF1} = \frac{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)V_{in}-\left(V_{o1}+k\sqrt{\frac{L_1}{L_2}}V_{o2}\right)}{(1-k^2)L_1}$	$G_{NF1} = \frac{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)V_{in}-k\sqrt{\frac{L_1}{L_2}}V_{o2}}{(1-k^2)L_1}$	$G_{FN1} = \frac{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)V_{in}-V_{o1}}{(1-k^2)L_1}$
i_{L2}	$G_{NN2} = \frac{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)V_{in}}{(1-k^2)L_2}$	$G_{FF2} = \frac{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)V_{in}-\left(V_{o2}+k\sqrt{\frac{L_2}{L_1}}V_{o1}\right)}{(1-k^2)L_2}$	$G_{NF2} = \frac{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)V_{in}-V_{o2}}{(1-k^2)L_2}$	$G_{FN2} = \frac{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)V_{in}-k\sqrt{\frac{L_2}{L_1}}V_{o1}}{(1-k^2)L_2}$
$i_{L1} = 0$, i_{L2} CCM, S_{DB1} OFF	$G_{NN2_0} = \frac{V_{in}}{L_2}$	$G_{FF2_0} = \frac{V_{in}-V_{o2}}{L_2}$	$G_{NF2_0} = \frac{V_{in}-V_{o2}}{L_2}$	$G_{FN2_0} = \frac{V_{in}}{L_2}$
i_{L1} negative, i_{L2} CCM, S_{DB1} ON	$G_{NN1_{bD}} = G_{NN1}$ $G_{NN2_{bD}} = G_{NN2}$	$G_{FF1_{bD}} = G_{NF1}$ $G_{FF2_{bD}} = G_{NF2}$	–	–

Accordingly, v_{t1} is given by –

$$v_{t1} = \begin{cases} (1 + k\sqrt{\frac{L_1}{L_2}})V_{in} & \text{if } v_{L2} = V_{in} \\ (1 + k\sqrt{\frac{L_1}{L_2}})V_{in} - k\sqrt{\frac{L_1}{L_2}}V_{o2} & \text{if } v_{L2} = V_{in} - V_{o2} \end{cases} \tag{8.2}$$

To turn ON S_{DB1}, $v_{t1} < 0$. As v_{t1} is always positive when $v_{L2} = V_{in}$, for $v_{t1} < 0$ we obtain the condition as –

$$\begin{aligned} &(1 + k\sqrt{\frac{L_1}{L_2}})V_{in} - k\sqrt{\frac{L_1}{L_2}}V_{o2} < 0, \\ \implies &\boxed{\frac{V_{in}}{V_{o2}} < \frac{k\sqrt{\frac{L_1}{L_2}}}{(1 + k\sqrt{\frac{L_1}{L_2}})}} \end{aligned} \tag{8.3}$$

Therefore, it is found that when $v_{L2} = V_{in}$, the body diode is never ON. For $v_{L2} = V_{in} - V_{o2}$, body diode is ON when (8.3) is satisfied.

8.2.1.2 Formation of Sectors in DCM

The values of slope in each state are presented in Table 8.2. The rows of the table represents the inductor currents conditions when first boost is in DCM and second boost in CCM. The columns of the table represent the slopes in four states of the converter. This table presents the inductor current ripple expressions for all four states and the assumed inductor current possibilities. The table shows

that–

- G_{NN1}, $G_{NN1_{bD}}$, G_{NN2}, G_{NN2_0}, $G_{NN2_{bD}}$ are always positive as L_1, L_2, k, V_{in}, V_{o1}, V_{o2} are positive.
- G_{FF1}, G_{FF2}, G_{FF2_0} are always negative as $V_{in} < V_{o1}$, $V_{in} < V_{o2}$.
- G_{FN1}, G_{FN2}, G_{NF1}, G_{NF2} can taken both positive as well as negative values depending on the voltages and coupled inductor parameters.

Using Table 8.2 for $G_{FN1} < 0$, we have–

$$\begin{aligned} &\frac{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)V_{in}-V_{o1}}{(1-k^2)L_1}<0 \\ \Rightarrow &\boxed{\frac{V_{in}}{V_{o1}}<\frac{1}{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)}(=rd_{FN1})} \end{aligned} \tag{8.4}$$

Thus, we find that-

$$G_{FN1}\begin{cases} <0 & \text{for } \frac{V_{in}}{V_{o1}} < rd_{FN1} \\ =0 & \text{at } \frac{V_{in}}{V_{o1}} = rd_{FN1} \\ >0 & \text{for } \frac{V_{in}}{V_{o1}} > rd_{FN1} \end{cases} \tag{8.5}$$

Similarly, for $G_{FN2} < 0$ we have–

$$\begin{aligned} &\frac{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)V_{in}-k\sqrt{\frac{L_2}{L_1}}V_{o1}}{(1-k^2)L_2}<0 \\ \Rightarrow &\boxed{\frac{V_{in}}{V_{o1}}<\frac{k\sqrt{\frac{L_2}{L_1}}}{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)}(=rd_{FN2})} \end{aligned} \tag{8.6}$$

Similarly, $\frac{V_{in}}{V_{o2}} < rd_{NF1}$ for $G_{NF1} < 0$ and $\frac{V_{in}}{V_{o2}} < rd_{NF2}$ for $G_{NF2} < 0$, where

$$rd_{NF1} = \frac{k\sqrt{\frac{L_1}{L_2}}}{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)}, \quad rd_{NF2} = \frac{1}{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)}.$$

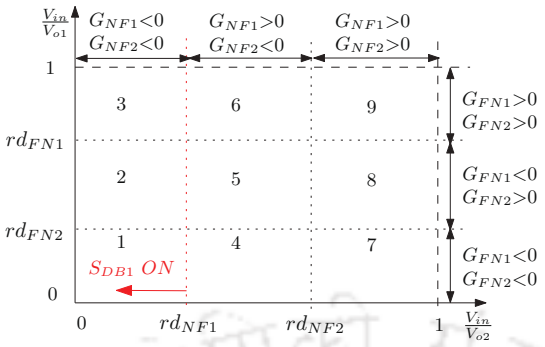


Figure 8.3: Sector diagram for DCM analysis of CI-SIDO boost converter.

It is also found that $rd_{NF1} < rd_{NF2}$, the proof of which is as follows–

$$\frac{k\sqrt{\frac{L_1}{L_2}}}{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)} < \frac{1}{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)} \Rightarrow 0 < k < 1 \tag{8.7}$$

Similarly, it can be proved that $rd_{FN2} < rd_{FN1}$. Plotting these values in $\frac{V_{in}}{V_{o1}}$ versus $\frac{V_{in}}{V_{o2}}$ plane, we obtain the sector diagram shown in Fig. 8.3. As shown, nine different sectors are possible for DCM analysis of CI-SIDO boost converter. Each sector has different waveform of inductor currents due to different $\frac{V_{in}}{V_{o1}}$ and $\frac{V_{in}}{V_{o2}}$ ratios. It is also found that the condition to turn ON body diode in (8.3) is the same as the conditions of Sectors 1, 2, and 3. Therefore, the body diode is turned ON in these sectors as marked in the sector diagram of Fig. 8.3.

8.3 Effect of Coupling on DCM Operation

8.3.1 Effect of Body Diode on DCM Operation of CI-SIDO Boost Converter

This section presents the effect of the body diode on the DCM operation of the converter.

8.3.2 DCM Operation When Body Diode is Turned ON

When body diode, S_{DB1} is turned ON, the currents i_{L1}, i_{d1}, i_{in} becomes negative for some values of i_{o1}. This section analyses the effect of negative currents on the slopes and average values of i_{L1}, i_{L2}, i_{d1}, i_{d2}, i_{in}, denoted by their corresponding capital letters.

8.3.2.1 Effect on Slopes of i_{L1}, i_{L2}, i_{d1}, i_{d2}, i_{in} When Body Diode is Turned ON

When the condition of turning ON of body diode in (8.3) is satisfied, the body diode turns ON. The effect of negative currents on the slopes of i_{L1}, i_{L2}, i_{d1}, i_{d2} are explained using the waveforms of Fig. 8.4(c). As discussed in Section 8.2.1.1, the body diode is turned ON when $v_{L2} = V_{in} - V_{o2}$. Therefore, for the duration of FN_o, $i_{L1} = 0$ and the slopes of i_{L2} changes. The voltages across the inductor windings in FN_o is given as-

$$v_{L1} = -k\sqrt{\frac{L_1}{L_2}}v_{L2}, \tag{8.8a}$$

$$v_{L2} = (1-k^2)L_2\frac{di_{L2}}{dt} - k\sqrt{\frac{L_2}{L_1}}v_{L1} \tag{8.8b}$$

Substituting the expression of v_{L1} in v_{L2}, the expression reduces to-

$$v_{L2} = L_2\frac{di_{L2}}{dt} \tag{8.9}$$

Therefore, for state FN_o where $v_{L2} = V_{in}$, the slope of i_{L2} called G_{FN2_0} is given by-

$$G_{FN2_o} = \frac{V_{in}}{L_2} \tag{8.10}$$

After the duration FN_o, S_{DB1} turns ON and i_{DB1} starts flowing in negative direction. This duration is called FF_{bD}. Even though S_{DB1} conducts in this state, $G_{FF1_{bD}} = G_{NF1}$ and $G_{FF2_{bD}} = G_{NF2}$, as presented in Table 8.2.

As the slopes of i_{L1}, i_{L2} changes, the waveforms of i_{d1}, i_{d2}, i_{in} changes as shown in Fig. 8.4(c). As the current i_{DB1} becomes negative upto T_s with negative slope $G_{FF1_{bD}}$, it remains in the negative direction at the starting of the next switching cycle with a positive slope of $G_{NN1_{bD}}$ for NN_{bD}. If the duration of NN_{bD} is smaller than D_1T_s, S_{t1} turns ON with positive i_{L1}. The currents i_{L1}, i_{L2} increases with their respective positive slopes G_{NN1}, G_{NN2} upto D_1T_s. After that i_{L1}, i_{L2} decreases with their respective negative slopes G_{FN1}, G_{FN2}. Thus, in this way the cycle repeats.

The slopes of input current in CI-SIDO boost converter is the sum of slopes of the inductor currents in the corresponding state. At boundary in Fig. 8.4(a), i_{in} starts from 0 as i_{L1} and i_{L2} starts from 0. When S_{DB1} is ON in Fig. 8.1, i_{in} starts from a negative value as the sum of i_{L1} and i_{L2} at $t = 0$ is

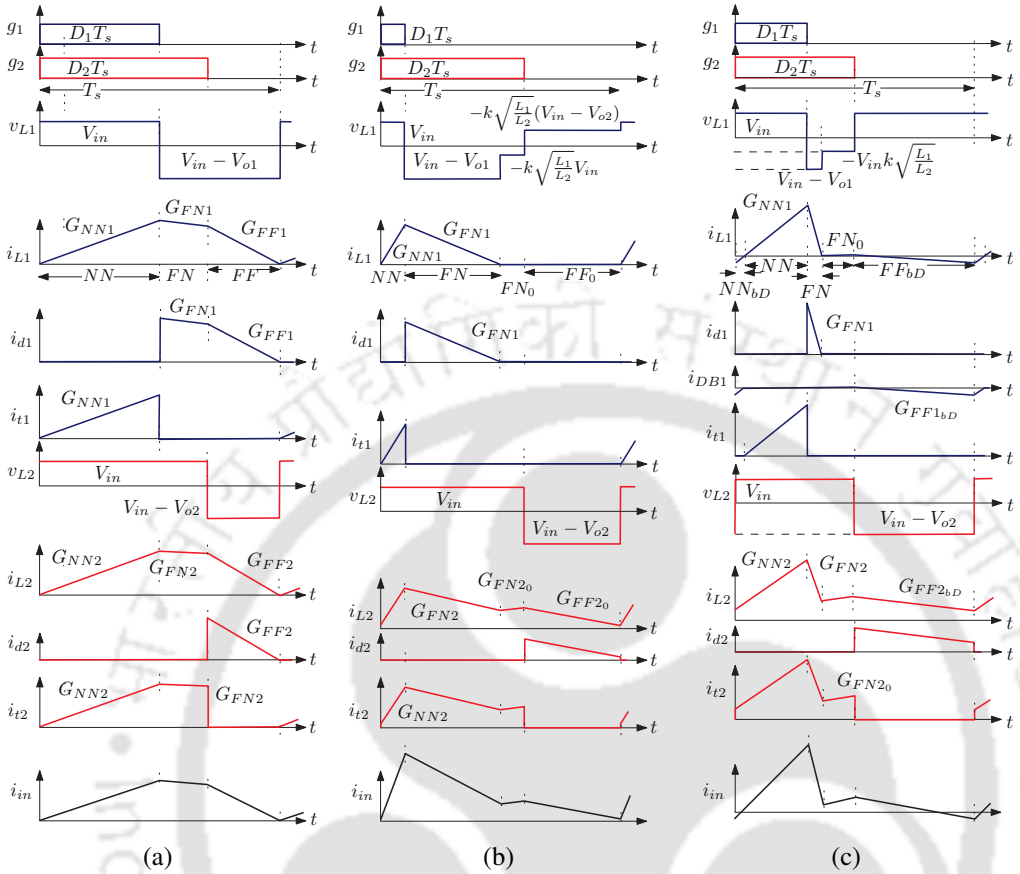


Figure 8.4: The theoretical waveforms of g_1, g_2, v_{L1}, i_{L1}, i_{d1}, i_{t1}, v_{L2}, i_{L2}, i_{d2}, i_{t2}, and i_{in} for a constant V_{o1}, V_{o2} at (a) CCM/DCM boundary, (b) when S_{DB1} is OFF, (c) when S_{DB1} is ON.

negative. As a result, i_{in} becomes negative for some portion of T_s when S_{DB1} is ON.

8.3.2.2 Effect on Average Values of i_{L1}, i_{L2}, i_{d1}, i_{d2}, i_{in} When Body Diode is Turned ON

To shown the effect of turning ON of body diode on the average values of i_{L1}, i_{L2}, i_{d1}, i_{d2}, one set of waveform is shown in Figs. 8.4(a), 8.4(c) where V_{o1} and V_{o2} is kept same and V_{in} is changed such that body diode S_{DB1} turns ON and negative current flows through it. The average values are compared with the condition when both i_{L1} and i_{L2} are at boundary as in Fig. 8.4(a). As the voltages V_{o1} and V_{o2} is to be maintained constant, the duty ratios D_1, D_2 changes in response to the change in input voltage V_{in}. For a given V_{in}, the first boost converter enters from CCM/DCM boundary to DCM by reducing the load current, i_{o1}. As the average value of i_{d1} is the load current i_{o1}, therefore, the average value of i_{d1} is decreasing as the converter enters from boundary to DCM. The average values of i_{L1}, i.e., I_{L1} decreases as the load current i_{o1} decreases from the boundary value. This is evident

from the waveforms of i_{L1} from Figs. 8.4(c) and 8.4(a).

As the second boost is not changed while the first enters from boundary to DCM, the load current of i_{o2} remains the same. Consequently, the average value of i_{d2} does not change. The average values of i_{L2}, i.e., I_{L2} remain approximately the same as the load current of the second boost, i.e., i_{o2} is not changed. The average value of i_{in} can become negative if the sum of average values of i_{L1} and i_{L2} are negative.

8.3.3 DCM Operation When Body Diode is Not Turned ON

When i_{L1} is in DCM, but body diode, S_{BD1} is not turned ON, the CI-SIDO boost converter operates in DCM without any negative current. This section analyzes the effect of $i_{L1} = 0$ on the slopes and average values of i_{L1}, i_{L2}, i_{d1}, i_{d2}, i_{in}.

8.3.3.1 Effect on Slopes of i_{L1}, i_{L2}, i_{d1}, i_{d2}, i_{in} When Body Diode is Not Turned ON

The waveforms are shown in Fig. 8.4(b). The inductor currents i_{L1}, i_{L2} starts from 0 with their respective slopes G_{NN1}, G_{NN2} in the state NN. After this state, S_{t1} turns OFF and i_{L1}, i_{L2} decreases with slopes G_{FN1}, G_{FN2} in the FN state. However, i_{L1} becomes 0 before turning OFF of S_{t2}. So, this state where S_{t1} is OFF, $i_{L1} = 0$, and S_{t2} is ON, is called FN_0 state. The slopes of i_{L2} in this state is given by G_{FN2_0} as presented in Table 8.2. The next state is FF_0 where both S_{t1}, S_{t2} are OFF and $i_{L1} = 0$. Using (8.9) in FN_0 and FF_0, the slopes of i_{L2} is given by–

$$G_{FN2_o} = \frac{V_{in}}{L_2}, \tag{8.11a}$$

$$G_{FF2_o} = \frac{V_{in} - V_{o2}}{L_2} \tag{8.11b}$$

When S_{DB1} is OFF in Fig. 8.4(b), i_{in} starts from a positive value as the sum of i_{L1} and i_{L2} at $t = 0$ is positive. Therefore, the sum of i_{L1} and i_{L2} are never negative, resulting in a positive i_{in}.

8.3.3.2 Effect on Average Values of i_{L1}, i_{L2}, i_{d1}, i_{d2}, i_{in} When Body Diode is Not Turned ON

Similar to Section 8.3.2.2, the average values of i_{L1}, i_{L2}, i_{d1}, i_{d2} when S_{DB1} is OFF (Fig. 8.4(b)) is compared to its boundary case (Fig. 8.4(a)). The comparisons show that the average values of i_{d1}, i_{L1} decreases as i_{o1} is decreased. This is clearly shown in Fig. 8.4(b) where the base as well as the

height of i_{d1} graph decreases compared to i_{d1} at boundary in Fig. 8.4(a). The average values of i_{d2} remains same as i_{o2} is not changing. As a result, the variation in average values of i_{L2} is insignificant compared to the average values of i_{L1}. In this case, the average values of i_{L1} is never negative. As the average value of i_{in} is the sum of average values of i_{L1} and i_{L2}, therefore it is never negative.

8.3.4 Effect of Change in Input Voltage, Load currents, and Duty Ratios: Different Modes of CI-SIDO Boost

In the CI-SIDO boost converters, the output voltages V_{o1}, V_{o2} is to be maintained based on the applications. If V_{in} changes, the values of $\frac{V_{in}}{V_{o1}}$, $\frac{V_{in}}{V_{o2}}$ change. This changes the sector of operation of CI-SIDO boost converter as shown in Fig. 8.3. The change in sector changes the waveforms of i_{L1}, i_{L2}, which is actually affecting the DCM operation of the CI-SIDO boost converter. Therefore, each sector is analyzed, and the range of V_{in}, i_{o1}, and D_1 are formulated for each sector. The formation of different modes is also discussed, followed by the grouping of sectors based on a similar i_{L1} pattern. The voltage and current stress on semiconductors are analysed, followed by the analysis of the output voltage gain.

8.3.4.1 Formation of Modes and Grouping of Sectors Based on Similar i_{L1} Patterns

As discussed earlier, the inductor current waveforms of all nine sectors are different from each other. For a given V_{o1}, V_{o2}, the range of V_{in} for each sector is formulated using Fig. 8.3. For example, the range of V_{in} for Sector 1 is–

$$\begin{aligned} &0 < V_{in} < V_{o2}.rd_{NF1}, \;\; 0 < V_{in} < V_{o1}.rd_{FN2}, \\ &\implies 0 < V_{in} < \min(V_{o1}.rd_{FN2}, V_{o2}.rd_{NF1}). \end{aligned} \tag{8.12}$$

Similarly, the range of V_{in} for all other sectors are formulated and presented in Table 8.3. The rows of the table represent all the 9 sectors and modes of the CI-SIDO boost and the columns represent the range of V_{in} for each sectors and the modes. This table brief the effect of change in the common input voltage of CI-SIDO boost.

Within a sector, the inductor current patterns further change depending on the load currents and duty ratios. Therefore, modes are formed within the sector. Sectors 1, 2, 4, 5, 7, 8 is divided into three

Table 8.3: Range of input voltage in different modes of DCM in CI-SIDO boost converter

Sector	Modes	Range of V_{in}
1	1a 1b 1c	$0 < V_{in} < \min(V_{o1}rd_{FN2}, V_{o2}rd_{NF1})$
2	2a 2b 2c	$\max(V_{o1}.rd_{FN2}, 0) < V_{in} < \min(V_{o1}.rd_{FN1}, V_{o2}.rd_{NF1})$
3	3	$\max(V_{o1}.rd_{FN1}, 0) < V_{in} < \min(V_{o1}, V_{o2}.rd_{NF1})$
4	4a 4b 4c	$\max(V_{o1}.rd_{FN2}, V_{o2}.rd_{NF1}) < V_{in} < \min(V_{o1}.rd_{FN2}, V_{o2}.rd_{NF2})$
5	5a 5b 5c	$\max(V_{o1}.rd_{FN2}, V_{o2}.rd_{NF1}) < V_{in} < \min(V_{o1}.rd_{FN1}, V_{o2}.rd_{NF2})$
6	6	$\max(V_{o1}rd_{FN1}, V_{o2}rd_{NF1}) < V_{in} < \min(V_{o1}, V_{o2}rd_{NF2})$
7	7a 7b 7c	$\max(0, V_{o2}.rd_{NF2}) < V_{in} <$ $\min(V_{o1}.rd_{FN2}, V_{o2})$
8	8a 8b 8c	$\max(V_{o1}.rd_{FN2}, V_{o2}.rd_{NF2}) < V_{in} < \min(V_{o1}.rd_{FN1}, V_{o2})$
9	9	$\max(V_{o1}rd_{FN1}, V_{o2}rd_{NF2}) < V_{in} < \min(V_{o1}, V_{o2})$

modes whereas Sectors 3, 6, 9 has only one modes. For example, the physical meaning of Sector '1' Mode '1a' is that its inductor current slope conditions are $G_{NN1} > 0$, $G_{NF1} < 0$, $G_{FN1} < 0$, $G_{FF1} < 0$, $G_{NN2} > 0$, $G_{NF2} < 0$, $G_{FN2} < 0$, $G_{FF2} < 0$, the load range is $i_{o11b} < i_{o1} < i_{o1bd}$, and the range of duty ratio is $D_{1_{1b}} < D_1 < t_{NN}$.

This chapter analyses CI-SIDO boost with i_{L1} is in DCM, keeping i_{L2} in CCM. Due to this considered assumption, the sectors of the CI-SIDO boost converter is divided into four groups based on the similar patterns of i_{L1}. The analysis of one waveform from each group is sufficient to show the behaviour of i_{L1} for each group.

The durations of states of each inductor current waveform pattern are discussed here. For a given value of coupled inductors, output, and input voltages, the slopes of the CI-SIDO boost converter are

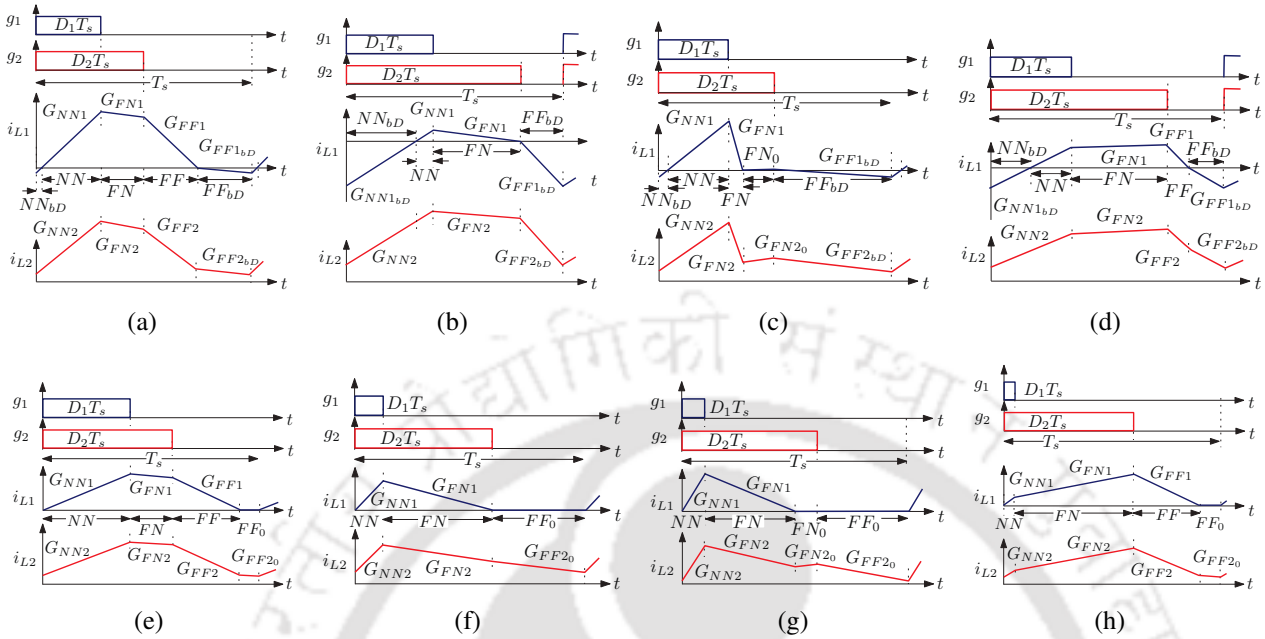


Figure 8.5: The theoretical waveforms of g_1, g_2, i_{L1}, i_{L2} when operating in modes (a) 1a, (b) 1b, (c) 1c, (d) 3, (e) 4a, (f) 4b, (g) 4c, and (h) 6.

known. For the required t_{FF}, the waveform of i_{L1} from Mode 1a of Fig. 8.5(a) gives–

$$t_{NN_{bD}} = \frac{|G_{NF1}|(1 - D_2 - t_{FF})}{G_{NN1}}, \tag{8.13a}$$

$$t_{FN} = \frac{(D_2 - t_{NN_{bD}} - t_{FF}\frac{|G_{FF1}|}{|G_{NN1}|})}{(1 + \frac{|G_{FN1}|}{|G_{NN1}|})}, \tag{8.13b}$$

$$t_{NN} = t_{FN}\frac{|G_{FN1}|}{|G_{NN1}|} + t_{FF}\frac{|G_{FF1}|}{|G_{NN1}|}, \tag{8.13c}$$

$$D_1 = t_{NN_{bD}} + t_{NN}, \tag{8.13d}$$

$$i_{o1} = \frac{T_s}{2}[t_{FF}(t_{FF} + t_{FN})|G_{FF1}| + t_{NN}t_{FN}G_{NN1}]. \tag{8.13e}$$

Now, at CCM/DCM boundary, we have $t_{NN_{bD}} = t_{FF_{bD}} = 0$, $t_{FF} = (1 - D_2)$, $D_2 = t_{NN} + t_{FN}$. The obtained values of $i_{o1} = i_{o1bd}$ and $D_1 = t_{NN}$ at the CCM/DCM boundary are–

$$\frac{T_s}{2}[t_{NN}(D_2 - t_{NN})G_{NN1} + (1 - D_2)(1 - t_{NN})|G_{FF1}|] \tag{8.14}$$
$$\text{where, } t_{NN} = \frac{D_2|G_{FN1}| + (1 - D_2)|G_{FF1}|}{G_{NN1} + G_{FN1}}.$$

Therefore, i_{L1} remains in DCM when $i_{o1} < i_{o1bd}$ and $D_1 < t_{NN}$ as presented in Table 8.4. Now, the

Table 8.4: Different sectors and modes in CI-SIDO boost converter when i_{L1} is in DCM while i_{L2} is in CCM

Sector	Modes	Slopes of i_{L1}	Range of i_{o1}	Range of D_1	sequence of states	Slopes of i_{L2}
1	1a	$\mathscr{S}$-III	$\mathscr{C}$-I	$\mathscr{D}$-I	$\mathscr{A}$-I	$\mathscr{S}$-III
2	2a					$\mathscr{S}$-II
1	1b		$\mathscr{C}$-II	$\mathscr{D}$-II	$\mathscr{A}$-II	$\mathscr{S}$-III
2	2b					$\mathscr{S}$-II
1	1c		$\mathscr{C}$-III	$\mathscr{D}$-III	$\mathscr{A}$-III	$\mathscr{S}$-III
2	2c					$\mathscr{S}$-II
3	3	$\mathscr{S}$-II	$\mathscr{C}$-III	$\mathscr{D}$-III	$\mathscr{A}$-I	$\mathscr{S}$-II
4	4a	$\mathscr{S}$-I	$\mathscr{C}$-IV	$\mathscr{D}$-IV	$\mathscr{A}$-IV	$\mathscr{S}$-III
5	5a					$\mathscr{S}$-II
7	7a					$\mathscr{S}$-I
8	8a					$\mathscr{S}$-IV
4	4b		$\mathscr{C}$-V	$\mathscr{D}$-V	$\mathscr{A}$-V	$\mathscr{S}$-III
5	5b					$\mathscr{S}$-II
7	7b					$\mathscr{S}$-I
8	8b					$\mathscr{S}$-IV
4	4c		$\mathscr{C}$-VI	$\mathscr{D}$-VI	$\mathscr{A}$-VI	$\mathscr{S}$-III
5	5c					$\mathscr{S}$-II
7	7c					$\mathscr{S}$-I
8	8c					$\mathscr{S}$-IV
6	6	$\mathscr{S}$-IV	$\mathscr{C}$-I	$\mathscr{D}$-I	$\mathscr{A}$-IV	$\mathscr{S}$-II
9	9					$\mathscr{S}$-IV

$\mathscr{S}$-I: $G_{NFw} > 0, G_{FNw} < 0$; $\mathscr{S}$-II: $G_{NFw} < 0, G_{FNw} > 0$

$\mathscr{S}$-III: $G_{NFw} < 0, G_{FNw} < 0$; $\mathscr{S}$-IV: $G_{NFw} > 0, G_{FNw} > 0$

$\mathscr{C}$-I: $i_{o11b} < i_{o1} < i_{o1bd}$; $\mathscr{D}$-I: $D_{1_{1b}} < D_1 < t_{NN}$

$\mathscr{C}$-III: $0 < i_{o1} < i_{o11b}$; $\mathscr{D}$-III: $0 < D_1 < D_{1_{1b}}$

$\mathscr{C}$-IV: $i_{o14b} < i_{o1} < i_{o1bd}$; $\mathscr{D}$-IV: $D_{1_{4b}} < D_1 < t_{NN}$

$\mathscr{C}$-II: $= i_{o1bd}$; $\mathscr{D}$-II: $= D_{1_{1b}}$, $\mathscr{C}$-V: $= i_{o14b}$; $\mathscr{D}$-V: $= D_{1_{4b}}$

$\mathscr{C}$-VI: $0 < i_{o1} < i_{o14b}$; $\mathscr{D}$-VI: $0 < D_1 < D_{1_{4b}}$

$\mathscr{A}$-I: $NN_{bD} \rightarrow NN \rightarrow FN \rightarrow FF \rightarrow FF_{bD}$

$\mathscr{A}$-II: $NN_{bD} \rightarrow NN \rightarrow FN \rightarrow FF_{bD}$

$\mathscr{A}$-III: $NN_{bD} \rightarrow NN \rightarrow FN \rightarrow FN_0 \rightarrow FF_{bD}$

$\mathscr{A}$-IV: $NN \rightarrow FN \rightarrow FF \rightarrow FF_0$

$\mathscr{A}$-V: $NN \rightarrow FN \rightarrow FF_0$, $\mathscr{A}$-VI: $NN \rightarrow FN \rightarrow FN_0 \rightarrow FF_0$

$$D_{1_{bd}} = \frac{(1-D_2)G_{FF1}-D_2G_{FN1}}{G_{NN1}-G_{FN1}},\quad D_{1_{4b}} = \frac{D_2G_{FN1}}{G_{NN1}+G_{FN1}}$$

$$D_{1_{1b}} = \frac{D_2G_{FN1}+(1-D_2)G_{NF1}}{G_{NN1}+G_{FN1}},\quad i_{o11b} = \frac{|G_{FN1}|(D_2T_sG_{NN1}-|G_{NF1}|(1-D_2)T_s)^2}{2T_s(|G_{FN1}|+G_{NN1})^2}$$

$$i_{o14b} = \frac{|G_{FN1}|G_{NN1}^2D_2^2T_s}{2(G_{NN1}+|G_{FN1}|)^2},\quad t_{NN} = \frac{D_2|G_{FN1}|+(1-D_2)|G_{FF1}|}{G_{NN1}+G_{FN1}}$$

$$i_{o1bd} = \frac{T_s}{2}\left[t_{NN}(D_2-t_{NN})G_{NN1} + (1-D_2)(1-t_{NN})|G_{FF1}|\right]$$

details of Mode 1b is obtained using Fig. 8.5(b) as follows–

$$t_{NN_{bD}} = \frac{G_{NF1}(1-D_2)}{G_{NN1}}, \tag{8.15a}$$

$$t_{NN} = \frac{(D_2 - t_{NN_{bD}})}{(1+\frac{G_{NN1}}{|G_{FN1}|})}, \tag{8.15b}$$

$$t_{FN} = \frac{G_{NN1}}{|G_{FN1}|}\frac{(D_2 - t_{NN_{bD}})}{(1+\frac{G_{NN1}}{|G_{FN1}|})}, \tag{8.15c}$$

$$D_1 = t_{NN_{bD}} + t_{NN}, \tag{8.15d}$$

$$i_{o1} = \frac{T_s}{2} t_{FN}^2 |G_{FN1}|. \tag{8.15e}$$

Finding the values of $i_{o1} = i_{o11b}$ and $D_1 = D_{1_{1b}}$ at Mode 1b, we obtain–

$$i_{o11b} = \frac{|G_{FN1}|(D_2 T_s G_{NN1} - |G_{NF1}|(1-D_2)T_s)^2}{2T_s(|G_{FN1}| + G_{NN1})^2}, \tag{8.16a}$$

$$D_{1_{1b}} = \frac{D_2 G_{FN1} + (1-D_2)G_{NF1}}{G_{NN1} + G_{FN1}}. \tag{8.16b}$$

Therefore, i_{L1} remains in Mode 1a when $i_{o11b} < i_{o1} < i_{o1bd}$ and $D_{1_{1b}} < D_1 < t_{NN}$. At $i_{o1} = i_{o11b}$ and $D_1 = D_{1_{1b}}$, the converter is at Mode 1b. After that if $i_{o1} < i_{o11b}$ and $D_1 < D_{1_{1b}}$, the converter operates in Mode 1c. As this analysis assumes that only i_{L1} is in DCM, the ranges of i_{o1} and D_1 is also valid for modes of Sector 2, i.e., Mode 2a, 2b, and 2c. Similarly, the range of V_{in}, i_{o1}, D_1 for all the sectors and modes are presented in Table 8.4. The rows of the table represents the sectors and modes of the CI-SIDO boost. The columns represent the slopes of i_{L1}, range of i_{o1}, D_1, sequence of states, slopes of i_{L2} in each sector and mode. The aim of this table is to give the range of load currents, duty ratios, sequence of states details of all the sectors and modes of CI-SIDO boost when first boost is in DCM and second boost is in CCM.

The analysis of other sectors show that Sector 3 has only one pattern as shown in Fig. 8.5(d). Also, from Fig. 8.3 and Table 8.4, we find that Sector 6 and 9 has same waveform of i_{L1} with only one waveform pattern as shown in Fig. 8.5(h). Similarly, out of Sectors 4, 5, 7, 8, the waveform of Sector 4 is shown in Figs. 8.5(e), 8.5(f), 8.5(g) which has three operating modes. The value of i_{o1}

corresponding to Modes 4b is given by-

$$i_{o14b} = \frac{|G_{FN1}|G_{NN1}^2 D_2^2 T_s}{2(G_{NN1} + |G_{FN1}|)^2}. \tag{8.17}$$

Therefore, this subsection shows that the CI-SIDO boost converter has nine sectors which are grouped into four groups based on similar i_{L1} patterns. Also, Sector 1, 2, 4, 5, 7, 8 is further divided into three modes. The waveforms from each mode and group are presented in Fig. 8.5. For each waveform, the duration of states are presented in Table 8.5. The rows represent the modes of the CI-SIDO converter. The columns represent the duration of each state, the input-output voltage relations, the voltages across the MOSFET and diode in each state. The aim of this table is to present the input-output voltage relations, the voltage and current stress details of CI-SIDO boost when first boost is in DCM and second boost is in CCM.

The summary of the sectors, modes, and the group of sectors are presented in Table 8.4. The sectors are a group of similar inductor current waveforms based on the inductor current slope conditions. Within the sectors, the inductor current patterns are further changing with load currents and duty ratios. For one inductor current slope condition, one particular type of waveforms pattern represents one mode. From Table 8.4, it is clear that four groups of sectors are possible based on the similar inductor current pattern.

8.3.4.2 Voltage and Current Stress on Semiconductors

As the load currents in DCM is very small compared to CCM, the peak values of MOSFETs and diodes are less compared to CCM. Therefore, the current stress on the MOSFETs and diodes are less compared to CCM. The peak values of MOSFET current for all the modes are–

$$i_{t1min} = 0, \tag{8.18a}$$

$$i_{t1max} = G_{NN1} t_{NN} T_s. \tag{8.18b}$$

Table 8.5: Duration of states, output voltage gain, and voltage stress on semiconductors of CI-SIDO boost converter in DCM

Modes	Duration of states	Input-output relations	v_{t1max} = max{}	v_{d1max} = min{}
1b, 2b	$t_{FF_{bD}} = (1 - D_2)$, $t_{NN_{bD}} = \frac{G_{NF1}(1-D_2)}{G_{NN1}}$, $t_{NN} = \frac{(D_2 - t_{NN_{bD}} - t_{FN_0})}{(1+\frac{G_{NN1}}{\lvert G_{FN1}\rvert})}$, $t_{FN} = \frac{G_{NN1}}{\lvert G_{FN1}\rvert}\frac{(D_2 - t_{NN_{bD}} - t_{FN_0})}{(1+\frac{G_{NN1}}{\lvert G_{FN1}\rvert})}$	$\frac{V_{o1}}{V_{in}} = \frac{1}{(D_2 - D_1)}$	V_{o1}	$-V_{o1}$
1c, 2c	$t_{FF_{bD}} = (1 - D_2)$, $t_{NN_{bD}} = \frac{G_{NF1}(1-D_2)}{G_{NN1}}$, $t_{NN} = \frac{(D_2 - t_{NN_{bD}} - t_{FN_0})}{(1+\frac{G_{NN1}}{\lvert G_{FN1}\rvert})}$, $t_{FN} = \frac{G_{NN1}}{\lvert G_{FN1}\rvert}\frac{(D_2 - t_{NN_{bD}} - t_{FN_0})}{(1+\frac{G_{NN1}}{\lvert G_{FN1}\rvert})}$	$\frac{V_{o1}}{V_{in}} = \frac{1 - t_{FN_0}(1+k\sqrt{\frac{L_1}{L_2}})}{t_{FN}}$	$\{V_{o1}, q_2 V_{in}\}$	$\{-V_{o1}, q_2 V_{in} - V_{o1}\}$
3	$t_{NN_{bD}} = \frac{\lvert G_{NF1}\rvert(1-D_2-t_{FF})}{G_{NN1}}$, $t_{FN} = \frac{(D_2 - t_{NN_{bD}} - t_{FF}\frac{\lvert G_{FF1}\rvert}{\lvert G_{NN1}\rvert})}{(1-\frac{\lvert G_{FN1}\rvert}{\lvert G_{NN1}\rvert})}$, $t_{NN} = t_{FF}\frac{\lvert G_{FF1}\rvert}{\lvert G_{NN1}\rvert} - t_{FN}\frac{\lvert G_{FN1}\rvert}{\lvert G_{NN1}\rvert}$	$\frac{V_{o1}}{V_{in}} = \frac{1}{(t_{FN}+t_{FF})}$	V_{o1}	$-V_{o1}$
4a, 5a, 7a, 8a	$t_{NN} = \frac{G_{FN1}D_2 + \lvert G_{FF1}\rvert t_{FF}}{(G_{NN1}+G_{FN1})}$, $t_{FN} = D_2 - t_{NN}$	$\frac{V_{o1}}{V_{in}} = \frac{1-t_{FF_0}(1+k\sqrt{\frac{L_1}{L_2}})}{(t_{FF}+t_{FN})} + \frac{k\sqrt{\frac{L_1}{L_2}}t_{FF_0}}{(t_{FF}+t_{FN})}\frac{V_{o2}}{V_{in}}$	$\left\{\begin{array}{l} V_{o1}, \\ q_2 V_{in} - q_1 V_{o2} \end{array}\right\}$	$\left\{\begin{array}{l} -V_{o1}, q_2 V_{in} \\ -V_{o1} - q_1 V_{o2} \end{array}\right\}$
4b, 5b, 7b, 8b	$t_{FF} = (1-D_2)$, $t_{FN}\{1+\frac{G_{FN1}}{G_{NN1}}\} = D_2$, $t_{NN} = \frac{G_{FN1}t_{FN}}{G_{NN1}}$	$\frac{V_{o1}}{V_{in}} = \frac{D_2(1+k\sqrt{\frac{L_1}{L_2}}) - k\sqrt{\frac{L_1}{L_2}}}{(D_2 - D_1)} + \frac{k\sqrt{\frac{L_1}{L_2}}(1-D_2)}{(D_2-D_1)}\frac{V_{o2}}{V_{in}}$	$\left\{\begin{array}{l} V_{o1}, \\ q_2 V_{in} - q_1 V_{o2} \end{array}\right\}$	$\left\{\begin{array}{l} -V_{o1}, q_2 V_{in} \\ -V_{o1} - q_1 V_{o2} \end{array}\right\}$
4c, 5c, 7c, 8c	$t_{FF_0} = (1-D_2)$, $t_{NN} = \frac{G_{FN1}t_{FN}}{G_{NN1}}$, $t_{FN}\{1+\frac{G_{FN1}}{G_{NN1}}\} = D_2 - t_{FN_0}$	$\frac{V_{o1}}{V_{in}} = \frac{D_1 + t_{FN} - k\sqrt{\frac{L_1}{L_2}}(t_{FN_0}+t_{FF_0})}{t_{FN}} + \frac{k\sqrt{\frac{L_1}{L_2}}t_{FF_0}}{t_{FN}}\frac{V_{o2}}{V_{in}}$	$\left\{\begin{array}{l} q_2 V_{in} - q_1 V_{o2}, \\ q_2 V_{in}, V_{o1} \end{array}\right\}$	$\left\{\begin{array}{l} q_2 V_{in} - V_{o1} - q_1 V_{o2}, \\ q_2 V_{in} - V_{o1}, -V_{o1} \end{array}\right\}$
6, 9	$t_{NN} = \frac{\lvert G_{FF1}\rvert t_{FF} - G_{FN1}D_2}{(G_{NN1} - G_{FN1})}$, $t_{FN} = D_2 - t_{NN}$	$\frac{V_{o1}}{V_{in}} = \frac{1-t_{FF_0}(1+k\sqrt{\frac{L_1}{L_2}})}{(t_{FF}+t_{FN})} + \frac{k\sqrt{\frac{L_1}{L_2}}t_{FF_0}}{(t_{FF}+t_{FN})}\frac{V_{o2}}{V_{in}}$	$\left\{\begin{array}{l} V_{o1}, \\ q_2 V_{in} - q_1 V_{o2} \end{array}\right\}$	$\left\{\begin{array}{l} -V_{o1}, q_2 V_{in} \\ -V_{o1} - q_1 V_{o2} \end{array}\right\}$
$q_1 = k\sqrt{\frac{L_1}{L_2}}$, $q_2 = (1 + k\sqrt{\frac{L_1}{L_2}})$				

The peak values of diode current are given by-

$$i_{d1max} = \begin{cases} G_{NN1}t_{NN}T_s + G_{FN1}t_{FN}T_s & \text{for Sector 3, 6, 9} \\ G_{NN1}t_{NN}T_s & \text{for other sectors} \end{cases} \tag{8.19}$$

The maximum current through the body diode is given by-

$$i_{DB1max} = G_{FF1_{bD}}t_{FF_{bD}}T_s \tag{8.20}$$

The maximum voltage across the MOSFET and diode depends on the coupled inductor parameters. Compared to their CCM values, the voltage stress may increase or decrease depending on the coupled inductor parameters. The maximum voltage stress on MOSFET, diode is presented in Table 8.5.

8.3.4.3 Output Voltage Gain Analysis

By applying the volt-second balance for v_{L1} in Mode 1a (Fig. 8.5(a)) where the body diode is ON, the input-output voltage relations are formulated as–

$$V_{in}(1 - t_{FN} - t_{FF}) + (V_{in} - V_{o1})(t_{FN} + t_{FF}) = 0, \tag{8.21a}$$

$$\implies \frac{V_{o1}}{V_{in}} = \frac{1}{(t_{FN} + t_{FF})}. \tag{8.21b}$$

Now, applying volt-second balance for v_{L1} in Mode 4b (Fig. 8.5(f)) where the body diode is not ON, the input-output voltage relations are formulated as–

$$V_{in}D_1 + (V_{in} - V_{o1})(D_2 - D_1) + k\sqrt{\frac{L_1}{L_2}}(V_{o2} - V_{in})(1 - D_2) = 0 \tag{8.22a}$$

$$\Rightarrow \frac{V_{o1}}{V_{in}} = \frac{D_2(1 + k\sqrt{\frac{L_1}{L_2}}) - k\sqrt{\frac{L_1}{L_2}}}{(D_2 - D_1)} + \frac{k\sqrt{\frac{L_1}{L_2}}(1 - D_2)}{(D_2 - D_1)}\frac{V_{o2}}{V_{in}} \tag{8.22b}$$

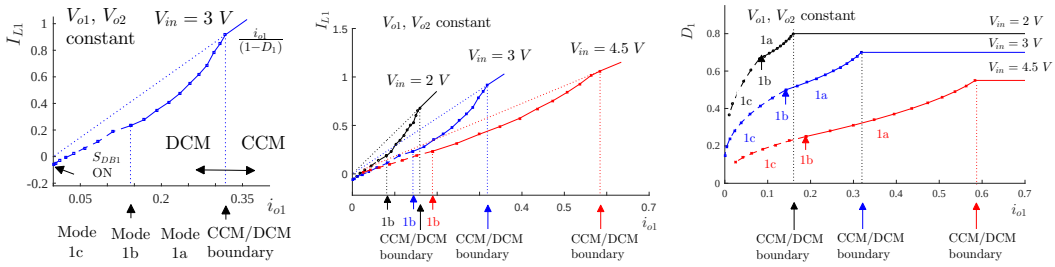
The input-output voltage relations of all the remaining waveforms are presented in Table 8.5. It is found that the input-output voltage relations in DCM depends on both the output voltages in addition to the coupled inductor values. As i_{L2} is in CCM, the input-output voltage relation is same as CCM–

$$\frac{V_{o2}}{V_{in}} = \frac{1}{(1 - D_2)}. \tag{8.23}$$

8.3.5 Simulation and Experimental Verifications

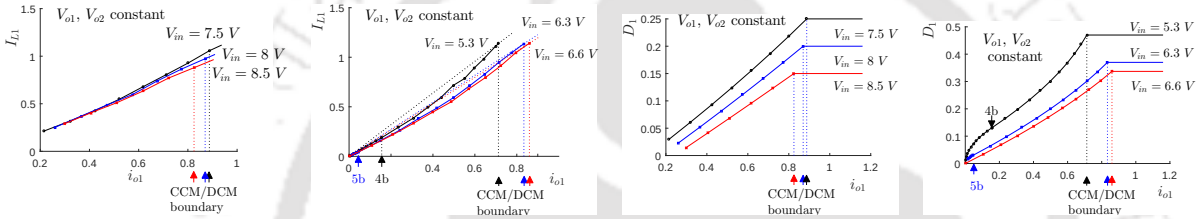
8.3.5.1 Simulation Verifications

The CI-SIDO boost converter is simulated in MATLAB/Simulink. The coupled inductor selected is $L_1 = 48.00\ \mu H$, $L_2 = 120.00\ \mu H$ and $k = 0.8$. The converter is operated with switching frequency of 100 kHz. Suppose, the output voltage to be maintained is $V_{o1} = 10\ V$ and $V_{o2} = 15\ V$. For the given values of L_1, L_2, k, V_{o1}, V_{o2}, the range of V_{in} is formulated for all the sectors using column 3 of Table 8.3. It is found that the feasible range of V_{in} is obtained for Sector 1, 4, 5, 8, and 9 only. The respective range obtained are $0 < V_{in} < 5.04$, $5.04 < V_{in} < 5.58$, $5.58 < V_{in} < 6.62$, $6.62 < V_{in} < 6.64$, $6.64 < V_{in} < 10$. Therefore, as V_{in} varies from 0 to 10 V the sectors of the converter changes.



(a) (b) (c)

Figure 8.6: (a) For a constant output-input voltages, the average value of i_{L1} decreases as i_{o1} is decreased. The negative average values of i_{L1} is due to S_{DB1} ON (Sector 1), (b) The average value of i_{L1} increases as input voltage is decreased, and (c) D_1 decreases as i_{o1} is decreased in DCM.



(a) (b) (c) (d)

Figure 8.7: For a constant output-input voltages, the average value of i_{L1} decreases as i_{o1} is decreased for (a) Sector 9, and (b) Sector 4, 5, 8. There is no negative I_{L1} as S_{DB1} is never ON. The average value of i_{L1} increases as input voltage is decreased in both the cases, and D_1 decreases as i_{o1} is decreased in DCM for (c) Sector 9, (d) Sector 4, 5, 8.

The waveform of I_{L1} vs i_{o1} is shown in Fig. 8.6(a). For i_{o1} higher than CCM/DCM boundary, I_{L1} is a straight line passing through the origin with slope $\frac{1}{(1-D_1)}$. As i_{o1} decreases and enters DCM, Mode 1a starts. The converter remains in Mode 1a until i_{o1} is greater than (8.16). As i_{o1} decreases further below (8.16), the converter enters Mode 1c. It is found that I_{L1} is negative for some values of i_{o1} due to the turning ON of S_{DB1}. The dotted lines represent the I_{L1} values in CCM. It is found that the value of I_{L1} in DCM has decreased from the boundary values. As the V_{in} is increased, the converter remains in Sector 1, however, I_{L1} is decreased and CCM/DCM boundary is increased. This is shown in Fig. 8.6(b).

It is to be noted that as V_{in} is changed, D_2 also changes because of the common input voltage V_{in}. However, as V_{o2} and R_2 are not changed. i_{o2} is not changed. Consequently, there is no significant change in I_{L2} as i_{o1} is changed.

The D_1 vs i_{o1} is shown in Fig. 8.6(c). The graphs show that as i_{o1} decreases from CCM/DCM boundary, the constant D_1 starts decreasing. As V_{in} is increased, D_1 decreases. As expected, in DCM

the duty ratios become load dependent.

Similar simulation graphs are shown for Sector 9 in Fig. 8.7(a) and Fig. 8.7(c). The graphs in Fig. 8.7(b) and Fig. 8.7(d) show that as V_{in} is changed, the sector of the converter is changed. For $V_{in} = 5.3\ V$ the converter operates in Sector 4, which changes to Sector 5 and 6 as V_{in} further changes to 6.3 V and 6.6 V.

The analysis in all the sectors show that the effect of turning ON of S_{DB1} does not change I_{L1} much. Though it depends on the L_1, L_2, k, D_1, D_2, V_{in}, the average value I_{L1} becomes negative only in Sector 1 for very small values of i_{o1}.

8.3.5.2 Experimental Verifications

To verify the sectors and modes presented in the chapter, a 100 W laboratory prototype of CI-SIDO boost converter is designed, as shown in Fig. 3.4(b). The converter is made using MOSFETs with part number IRFP90N20DPBF and diodes with part number RHRP30120. The input voltage V_{in} given is 4 V which is taken from a regulated DC supply of 64 V, 20 A. The capacitors of 100 μF are used. The rheostats are used as a load to the CI-SIDO boost converter that is changing for different modes. The currents and voltages are measured using current and differential probes in a four-channel mixed domain oscilloscope. Though the analysis presented in this chapter is valid for any parameters of a coupled inductor, this chapter presents the experiments for a ferrite core coupled inductor with $k = 0.8$, $L_1 = 48\ \mu H$, and $L_2 = 120\ \mu H$. The gate pulses g_1 and g_2 are generated using an FPGA kit numbered NI sbRIO 9637, which is programmed in the LabView platform.

The values of rd_{FN1}, rd_{FN2}, rd_{NF1}, rd_{NF2} are obtained as 0.66, 0.56, 0.34, 0.44 respectively. For given $V_{in} = 4\ V$, the ranges of V_{o1}, V_{o2} are obtained for each sector and mode. The values of V_{o1} is varied by changing R_1, D_1 as first boost is operated in DCM and V_{o2} is varied by changing D_2 as second boost is operated in CCM.

For sector 1, the ranges obtained are $0 < (V_{in}/V_{o1}) < 0.56$, and $0 < (V_{in}/V_{o2}) < 0.34$. The example of mode 1a is shown in Fig. 8.8(a) for $V_{in}/V_{o1} = 0.55$, $V_{in}/V_{o2} = 0.32$ such that D_1, D_2 obtained are 0.18, 0.7 and R_1, R_2 obtained are 24 Ω, 90 Ω. The mode 1b is shown in Fig. 8.8(b) for $V_{in}/V_{o1} = 0.55$, $V_{in}/V_{o2} = 0.32$ such that D_1, D_2 obtained are 0.18, 0.7 and R_1, R_2 obtained are 50.4 Ω, 90 Ω. The

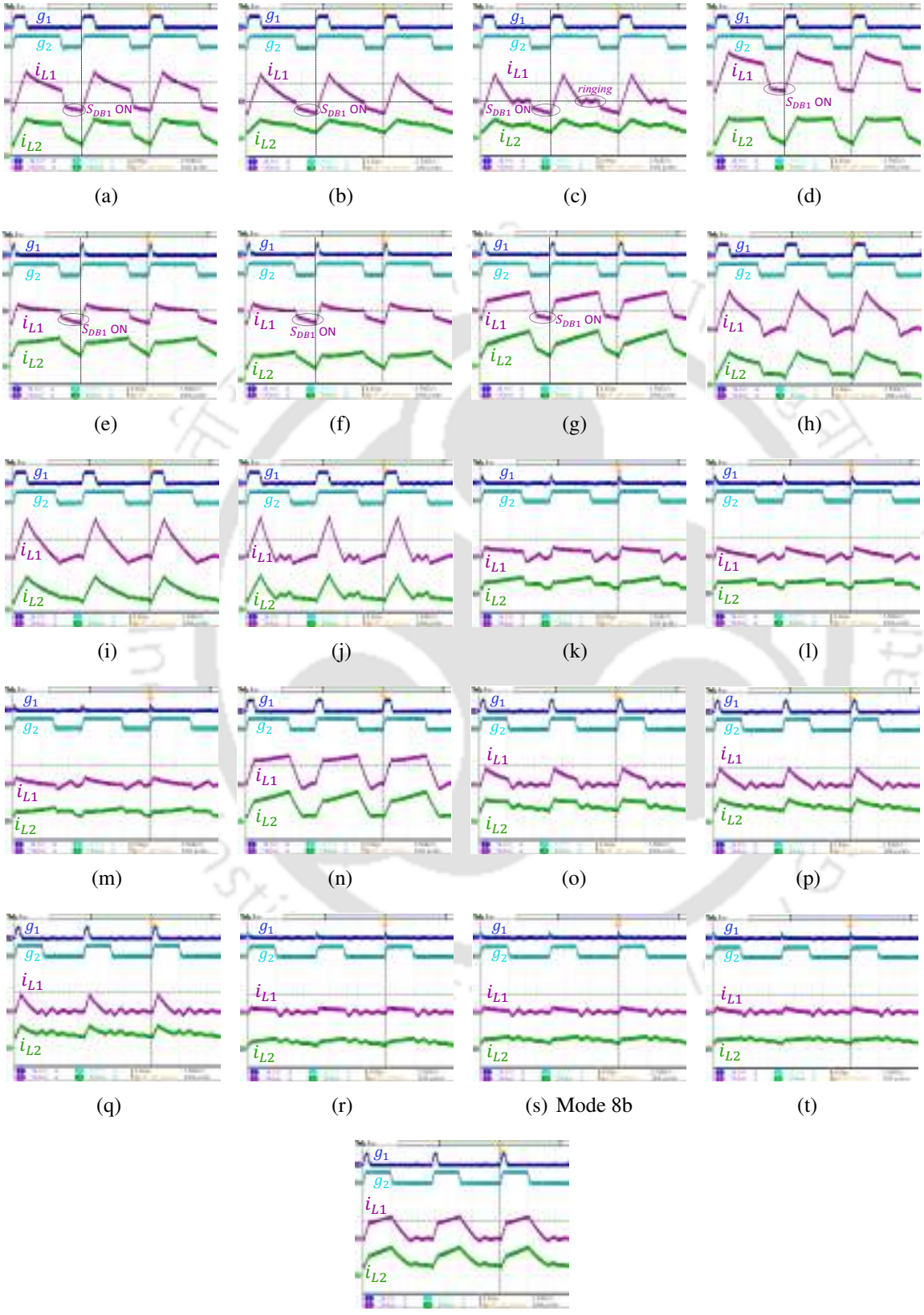


Figure 8.8: Experimental results of CI-SIDO boost converter in operating modes (a) 1a, (b) 1b, (c) 1c, (d) 2a, (e) 2b, (f) 2c, (g) 3, (h) 4a, (i) 4b, (j) 4c, (k) 5a, (l) 5b, (m) 5c, (n) 6, (o) 7a, (p) 7b, (q) 7c, (r) 8a, (s) 8b, (t) 8c, and (u) 9.

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mode 1c is shown in Fig. 8.8(c) for $V_{in}/V_{o1} = 0.47$, $V_{in}/V_{o2} = 0.32$ such that D_1, D_2 obtained are 0.18, 0.7 and R_1, R_2 obtained are 125.8 Ω, 90 Ω. Likewise, all the other modes are generated in the experiments. The experimental results for the remaining sectors are presented in Fig. 8.8. As discussed earlier, we observe that the body diode S_{DB1} is ON in Sectors 1, 2 and 3 only. In all the remaining sectors, there is no turning ON of the body diode S_{DB1}. The ringing in the experimental results is due to the parasitic inductances and capacitances present in the circuit.

8.3.6 Findings

The following are the findings of the analysis, simulation, and experiment of CI-SIDO boost converter–

- *Effect of DCM operation of the first boost on the second when second boost is at boundary or CCM:* As the first boost enters DCM, the slopes of i_{L1} and i_{L2} changes in each state. This changes the waveforms of i_{L1}, i_{L2}, i_{d1}, i_{d2}, i_{in}. The formulated slopes are presented in Table 8.2.

- *Conditions to turn ON body diode:* When the first boost is in DCM and the second boost in CCM, it is found that the body diode turns ON in Sectors 1, 2, and 3 only. The condition to turn ON S_{DB1} is given by (8.3).

- *Effect of body diode on the average values of inductor currents, diode currents, and input current:* The average value of i_{L1} may become negative when S_{DB1} is ON depending on the values of k, L_1, L_2, V_{o1}, V_{o2}, V_{in}. As the average values of i_{in} is the sum of the average values of i_{L1} and i_{L2}, its value can take negative values depending on the average value of i_{L1} and i_{L2}. When S_{DB1} is OFF, i_{L1} is never negative. Therefore, negative i_{in} is also not possible.

- *Effect of change in input voltage:* In practical applications where output voltages are maintained constant, the effect of variation in V_{in} is found. It is found that for a given k, L_1, L_2, V_{o1}, and V_{o2}, the range of V_{in} exists for each sector. As V_{in} increases, the converter may remain in the same sector or may change the sector. In both the case, as V_{in} increase, average values of i_{L1} decrease.

- *Effect of change in load current and duty ratio:* As the load current of the first boost decreases and enters DCM, the average values of the first inductor current also decrease. As the second load current is not changed, there is no significant change in the average values of the second inductor current. With the decrease in i_{o1}, D_1 decreases in DCM whereas D_2 changes with V_{in} as it is in CCM.

- *Voltage and current stress on semiconductors*: The current stress decreases compared to the CCM operations. However, the voltage stress depends on the voltages and coupled inductor parameters.

- *Output voltage gain*: The input-output voltage relations depend on the input voltage, both output voltages, and coupled inductor parameters.

The analysis presented in this chapter helps the designers with the choice of components. As the voltage gain of the converter increases many times in DCM, the voltage ratings of the output capacitors also get affected. The selection of MOSFETs and diodes also change depending on their voltage blocking capabilities and the currents carrying capabilities of the body diodes. Also, all the waveforms of the CI-SIDO boost converter that is presented in this chapter will help the system operator to design the controller for the CI-SIDO boost converter in DCM.

8.4 Numerous Patterns of Inductor Currents when both Boost in DCM

This section presents the DCM analysis of CI-SIDO boost when both the inductor current enters DCM. The DCM analysis of the CI-SIDO boost converter depends on the inductor current waveforms. As discussed in Chapter 2, the CI-SIDO boost converter has 36 different inductor current waveforms depending on the duty ratios, coupled inductor parameters. For each waveform, the DCM analysis is separate as DCM operation depends on the waveform patterns. The duty ratios also becomes load dependent in DCM.

There are many possibilities by which the two inductor currents reach zero. With a slight change in the point where inductor current reaches zero, the patterns of both inductor current change. Due to the presence of the coupled inductor, a small change in one inductor current tremendously affects

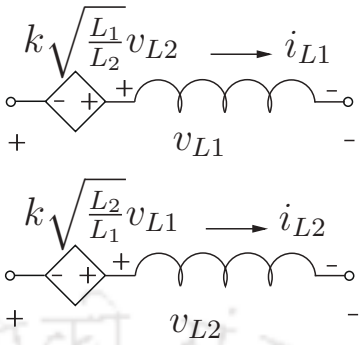


Figure 8.9: Coupled inductor equivalent circuit.

Table 8.6: Slopes of inductor currents in four states

Inductor current	*NN*	*FF*	*NF*	*FN*
i_{L1}	$G_{NN1}=\frac{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)V_{in}}{(1-k^2)L_1}$	$G_{FF1}=\frac{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)V_{in}-\left(V_{o1}+k\sqrt{\frac{L_1}{L_2}}V_{o2}\right)}{(1-k^2)L_1}$	$G_{NF1}=\frac{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)V_{in}-k\sqrt{\frac{L_1}{L_2}}V_{o2}}{(1-k^2)L_1}$	$G_{FN1}=\frac{\left(1+k\sqrt{\frac{L_1}{L_2}}\right)V_{in}-V_{o1}}{(1-k^2)L_1}$
i_{L2}	$G_{NN2}=\frac{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)V_{in}}{(1-k^2)L_2}$	$G_{FF2}=\frac{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)V_{in}-\left(V_{o2}+k\sqrt{\frac{L_2}{L_1}}V_{o1}\right)}{(1-k^2)L_2}$	$G_{NF2}=\frac{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)V_{in}-V_{o2}}{(1-k^2)L_2}$	$G_{FN2}=\frac{\left(1+k\sqrt{\frac{L_2}{L_1}}\right)V_{in}-k\sqrt{\frac{L_2}{L_1}}V_{o1}}{(1-k^2)L_2}$
$i_{L1}=0, i_{L2}>0$	$G_{NN2_0}=\frac{V_{in}}{L_2}$	$G_{FF2_0}=\frac{V_{in}-V_{o2}}{L_2}$	$G_{NF2_0}=\frac{V_{in}-V_{o2}}{L_2}$	$G_{FN2_0}=\frac{V_{in}}{L_2}$
$i_{L2}=0, i_{L1}>0$	$G_{NN1_0}=\frac{V_{in}}{L_1}$	$G_{FF1_0}=\frac{V_{in}-V_{o1}}{L_1}$	$G_{NF1_0}=\frac{V_{in}}{L_1}$	$G_{FN1_0}=\frac{V_{in}-V_{o1}}{L_1}$

the other inductor current. The DCM analysis of all 36 possibilities is very tedious. In Chapter 4, it is mentioned that the operation of CI-SIDO boost converter is preferred when the inductor current slopes are opposite to each other, i.e., called Sector 5. Therefore, the DCM analysis of the CI-SIDO boost converter is presented for Sector 5. However, the approach is valid for all the possibilities of CI-SIDO boost converter.

In this section, the DCM analysis of the CI-SIDO boost converter is analyzed for Sector 5. The analysis covers all possibilities of DCM for Sector 5. It is found that for Sector 5 only, eight different DCM possibilities are there. This chapter analyses all these eight inductor current patterns. The input-output voltage relations are also formulated for these waveforms.

The slopes of inductor currents, when either of them becomes zero, are formulated using the equivalent circuit diagram of the coupled inductor as shown in Fig. 8.9. Due to coupling, the voltages and currents are related as–

$$v_{L1}=(1-k^2)L_1\frac{di_{L1}}{dt}-k\sqrt{\frac{L_1}{L_2}}v_{L2}, \tag{8.24a}$$

$$v_{L2}=(1-k^2)L_2\frac{di_{L2}}{dt}-k\sqrt{\frac{L_2}{L_1}}v_{L1}. \tag{8.24b}$$

Therefore, as the inductor current becomes zero, the voltage across the inductors only depend on

other winding voltages. The slopes of inductor currents when either current becomes zero are added in Table 8.6. Two rows with $i_{L1} = 0$ and $i_{L2} = 0$ is added to Table 8.2 to make Table 8.6. The columns of the table represent the slopes of inductor currents in four states of CI-SIDO boost. The aim of the table is to present the inductor current slopes in all the four states of CI-SIDO boost when both the boost enters DCM. It is found that G_{NNw_0} and G_{FFw_0} are also positive and negative, respectively. While G_{NFw_0} and G_{FNw_0} can take positive as well as negative values depending on voltages and coupled inductor parameters. When both the inductors are non-zero, i.e., $i_{Lw} > 0$, v_{Lw} is given by–

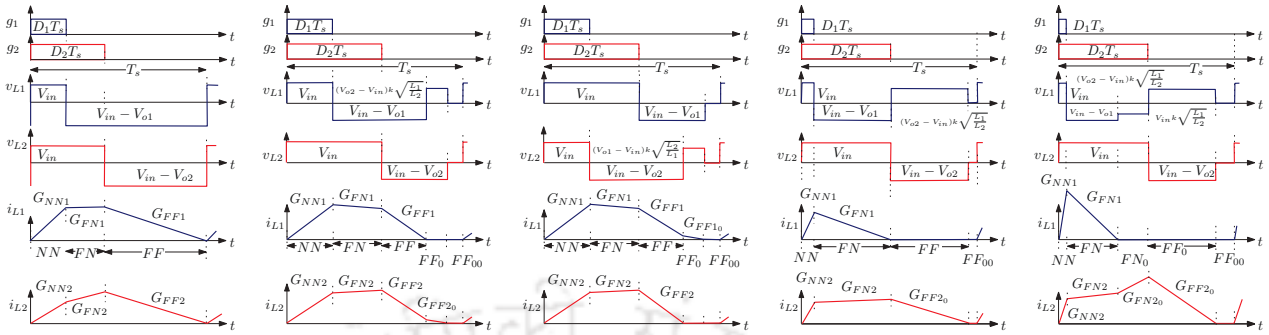
$$v_{Lw} = \begin{cases} V_{in} \text{ if } S_{tw} \text{ ON}, \\ V_{in} - V_{ow} \text{ if } S_{tw} \text{ OFF}. \end{cases} \tag{8.25}$$

It is found that the DCM operation of the CI-SIDO boost converter depends on the inductor current waveforms. The CI-SIDO boost converter has 36 different possibilities of inductor current waveforms depending on the voltages and coupled inductor parameters as discussed in Chapter 2. The behaviour of each waveform in DCM is different. The patterns again change with the change in the point when each inductor current reaches zero. With a small change in the point when the inductor current reaches zero, the pattern of both the inductor current change. Therefore, this section analyses the DCM analysis for slope conditions $G_{NN1} > 0$, $G_{FF1} < 0$, $G_{NF1} > 0$, $G_{FN1} < 0$, $G_{NN2} > 0$, $G_{FF2} < 0$, $G_{NF2} < 0$, $G_{FN2} > 0$. As discussed this slope condition is called Sector 5. This section covers all possible DCM waveforms of Sector 5.

8.4.1 Possible Inductor Current Waveforms of CI-SIDO Boost with both Boost in DCM

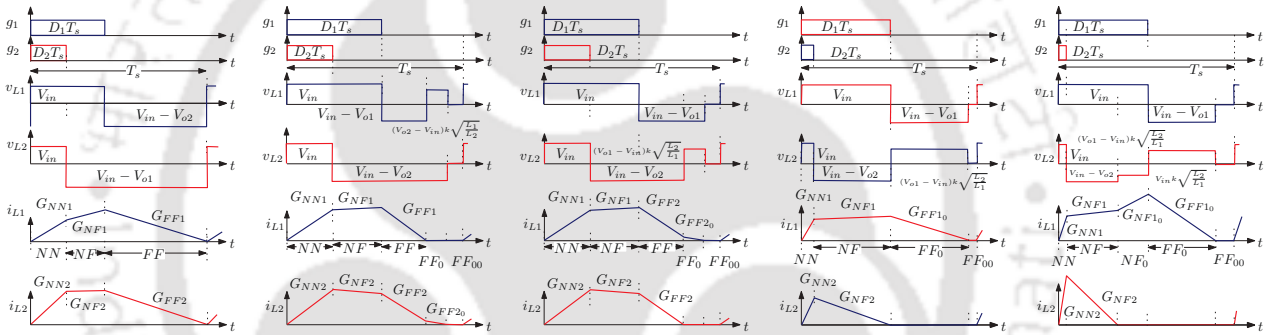
This section finds the possible inductor current waveforms in DCM for slope conditions $G_{NN1} > 0$, $G_{FF1} < 0$, $G_{NF1} > 0$, $G_{FN1} < 0$, $G_{NN2} > 0$, $G_{FF2} < 0$, $G_{NF2} < 0$, $G_{FN2} > 0$. The durations of each states are formulated and input-output voltage relations are found for each case.

The first set of waveforms for $D_1 < D_2$ are shown in Fig. 8.10. Based on the possible slope conditions of i_{L1} and i_{L2}, the feasible inductor current waveforms are drawn in DCM. As $G_{FN2} > 0$, i_{L2} can not become zero in FN state. The current i_{L2} can become zero in FF state only. However, i_{L1} can become zero in FN and FF states both. When both i_{L1} and i_{L2} are at CCM/DCM boundary, the waveforms look like Fig. 8.10(a). When i_{L1} is becoming zero in FF state, before i_{L2}, is shown in Fig.



(a) CCM/DCM boundary (b) Pattern 1 (c) Pattern 2 (d) Pattern 3 (e) Pattern 4

Figure 8.10: Possible DCM waveforms of CI-SIDO boost converter for $D_1 < D_2$ with slope conditions $G_{NN1} > 0$, $G_{FF1} < 0$, $G_{NF1} > 0$, $G_{FN1} < 0$, $G_{NN2} > 0$, $G_{FF2} < 0$, $G_{NF2} < 0$, $G_{FN2} > 0$.



(a) CCM/DCM boundary (b) Pattern 5 (c) Pattern 6 (d) Pattern 7 (e) Pattern 8

Figure 8.11: Possible DCM waveforms of CI-SIDO boost converter for $D_1 > D_2$ with slope conditions $G_{NN1} > 0$, $G_{FF1} < 0$, $G_{NF1} > 0$, $G_{FN1} < 0$, $G_{NN2} > 0$, $G_{FF2} < 0$, $G_{NF2} < 0$, $G_{FN2} > 0$.

8.10(b). When i_{L2} is becoming zero in FF state, before i_{L1}, is shown in Fig. 8.10(c). In Fig. 8.10(d), i_{L1} is becoming zero at D_2T_s, while i_{L2} becomes zero in FF state. The waveforms when i_{L1} becomes zero in FN state before D_2T_s, while i_{L2} becomes zero in FF state is shown in Fig. 8.10(e). As the inductor current waveforms are changing, the voltage across the inductor windings are also changing. This changes the input-output voltage relations of CI-SIDO boost converter.

Similarly, all the possible waveforms for $D_1 > D_2$ in DCM is presented in Fig. 8.11. In this case, $G_{NF1} > 0$, therefore, i_{L1} can reach zero in FF state only. Whereas i_{L2} can become zero in NF as well as FF states. When both the inductor currents are at CCM/DCM boundary, the waveforms are shown in Fig. 8.11(a). When i_{L1} becomes zero in FF state before i_{L2}, the waveforms look like Fig. 8.11(b). Whereas if i_{L2} becomes zero in FF state before i_{L1}, the waveforms look like Fig. 8.11(c). In Fig.

8.11(d), i_{L2} becomes zero at D_1T_s whereas i_{L1} becomes zero in FF state after i_{L2}. Similarly, in Fig. 8.11(e), i_{L2} becomes zero before D_1T_s whereas i_{L1} becomes zero in FF state after i_{L2}. Consequently, the voltage across the windings also change.

In Fig. 8.10(b), i_{L1}, i_{L2} both increases for $t_{NN}T_s$ with slopes G_{NN1}, G_{NN2}, respectively. After S_{t1} turns OFF, i_{L1} decreases with the slope G_{FN1} and i_{L2} increases with the slope G_{FN2} for $t_{FN}T_s$. When S_{t2} also turns OFF, i_{L1}, i_{L2} both decreases with their respective slopes G_{FF1}, G_{FF2}. This duration is called $t_{FF}T_s$. However, i_{L1} becomes zero before T_s while i_{L2} is still non-zero for $t_{FF_0}T_s$. In this duration, the slope of i_{L2} change, which is called G_{FF2_0}. Then i_{L2} also becomes zero before T_s. When both the inductor currents are non-zero, v_{L1} and v_{L2} are according to (2.50). Then for $t_{FF_{00}}T_s$, v_{L1} and v_{L2} are zero. In Fig. 8.10(b), t_{FF_0} and $t_{FF_{00}}$ are known based on the load currents i_{o1}, i_{o2}. The duration of other states are formulated as follows–

$$a_1t_{NN} + b_1t_{FN} = c_1, \tag{8.26a}$$

$$a_2t_{NN} + b_2t_{FN} = c_2, \text{ where,} \tag{8.26b}$$

$$a_1 = (G_{NN1} + |G_{FF1}|), \quad b_1 = (|G_{FF1}| - |G_{FN1}|), \tag{8.26c}$$

$$c_1 = |G_{FF1}|(1 - t_{FF_0} - t_{FF_{00}}), \quad a_2 = (G_{NN2} + |G_{FF2}|), \tag{8.26d}$$

$$b_2 = (|G_{FN2}| + |G_{FF2}|)t_{FN}, \quad c_2 = |G_{FF2}|(1 - t_{FF_0} - t_{FF_{00}}) + |G_{FF2_0}|t_{FF_0}. \tag{8.26e}$$

This is a linear equations in two variables, the solutions of which is given by–

$$t_{NN} = \frac{(b_2c_1 - b_1c_2)}{(a_1b_2 - a_2b_1)}, \tag{8.27a}$$

$$t_{FN} = \frac{(a_2c_1 - a_1c_2)}{(a_2b_1 - a_1b_2)}, \tag{8.27b}$$

$$t_{FF} = 1 - t_{NN} - t_{FN} - t_{FF_0} - t_{FF_{00}}. \tag{8.27c}$$

$$D_1 = t_{NN}, \tag{8.27d}$$

$$D_2 = t_{NN} + t_{FN}. \tag{8.27e}$$

The input-output voltage relations are formulated using the volt-seconds balance. Using the volt-

seconds balance for v_{L1}, we obtain–

$$V_{in}t_{NN} + (V_{o2} - V_{in})k\sqrt{\frac{L_1}{L_2}}t_{FF_0} = (V_{o1} - V_{in})(t_{FN} + t_{FF}), \tag{8.28a}$$

$$\implies V_{in}(t_{NN} + t_{FN} + t_{FF} - k\sqrt{\frac{L_1}{L_2}}t_{FF_0}) = V_{o1}(t_{FN} + t_{FF}) - V_{o2}k\sqrt{\frac{L_1}{L_2}}t_{FF_0} \tag{8.28b}$$

Similarly, using the volt-seconds balance for v_{L2}, we obtain–

$$V_{in}(t_{NN} + t_{FN}) = (V_{o2} - V_{in})(t_{FF} + t_{FF_0}), \tag{8.29a}$$

$$\implies V_{in}(t_{NN} + t_{FN} + t_{FF} + t_{FF_0}) = V_{o2}(t_{FF} + t_{FF_0}) \tag{8.29b}$$

The waveforms in Fig. 8.10(a) is a special case of Fig. 8.10(b) when $t_{FF_0} = 0$ and $t_{FF_{00}} = 0$. Therefore, (8.26) reduce to the following–

$$a_1 = (G_{NN1} + |G_{FF1}|), \tag{8.30a}$$

$$b_1 = (|G_{FF1}| - |G_{FN1}|) \tag{8.30b}$$

$$c_1 = |G_{FF1}|, \tag{8.30c}$$

$$a_2 = (G_{NN2} + |G_{FF2}|), \tag{8.30d}$$

$$b_2 = (|G_{FN2}| + |G_{FF2}|)t_{FN}, \tag{8.30e}$$

$$c_2 = |G_{FF2}|. \tag{8.30f}$$

$$\tag{8.30g}$$

The input-output voltage relations in (8.28), (8.29) reduce to–

$$V_{in} = V_{o1}(t_{FN} + t_{FF}), \tag{8.31a}$$

$$V_{in} = V_{o2}t_{FF}, \tag{8.31b}$$

$$\implies V_{in} = V_{o1}(1 - D_1), \tag{8.31c}$$

$$V_{in} = V_{o2}(1 - D_2). \tag{8.31d}$$

Similarly, a_1, a_2, b_1, b_2, c_1, c_2 for all the other waveforms are presented in Table 8.7. The rows represent the pattern number and the columns represent the values of the parameters and the input-

Table 8.7: Input-output voltage relations in DCM analysis of CI-SIDO boost converter

Pattern	Values of a_1, a_2, b_1, b_2, c_1, c_2	Input-output relations
2	$a_1 = (G_{NN1} + \|G_{FF1}\|)$, $b_1 = (\|G_{FF1}\| - \|G_{FN1}\|)$, $c_1 = \|G_{FF1}\|(1 - t_{FF_0} - t_{FF_{00}}) + \|G_{FF1_0}\|t_{FF_0}$, $a_2 = (G_{NN2} + \|G_{FF2}\|)$, $b_2 = (\|G_{FN2}\| + \|G_{FF2}\|)$, $c_2 = \|G_{FF2}\|(1 - t_{FF_0} - t_{FF_{00}})$	$V_{in}(t_{NN} + t_{FN} + t_{FF} + t_{FF_0}) = V_{o1}(t_{FN} + t_{FF} + t_{FF_0})$, $V_{in}(t_{NN} + t_{FN} + t_{FF} - k\sqrt{\frac{L_2}{L_1}}t_{FF_0}) = V_{o2}t_{FF} - V_{o1}k\sqrt{\frac{L_2}{L_1}}t_{FF_0}$
3	$a_1 = G_{NN1}$, $b_1 = -\|G_{FN1}\|$, $c_1 = 0$, $a_2 = (G_{NN2} + \|G_{FF2_0}\|)$, $b_2 = (\|G_{FN2}\| + \|G_{FF2_0}\|)$, $c_2 = \|G_{FF2_0}\|(1 - t_{FF_{00}})$	$V_{in}(t_{NN} + t_{FN} - k\sqrt{\frac{L_1}{L_2}}t_{FF_0}) = V_{o1}t_{FN} - V_{o2}k\sqrt{\frac{L_1}{L_2}}t_{FF_0}$, $V_{in}(t_{NN} + t_{FN} + t_{FF_0}) = V_{o2}t_{FF_0}$
4	$a_1 = G_{NN1}$, $b_1 = -\|G_{FN1}\|$, $c_1 = 0$, $a_2 = (G_{NN2} + \|G_{FF2_0}\|)$, $b_2 = (\|G_{FN2}\| + \|G_{FF2_0}\|)$, $c_2 = \|G_{FF2_0}\|(1 - t_{FF_{00}}) - (\|G_{FN2_0}\| + \|G_{FF2_0}\|)t_{FN_0}$	$V_{in}(t_{NN} + t_{FN} - k\sqrt{\frac{L_1}{L_2}}t_{FF_0} - k\sqrt{\frac{L_1}{L_2}}t_{FN_0}) = V_{o1}t_{FN} - V_{o2}k\sqrt{\frac{L_1}{L_2}}t_{FF_0}$, $V_{in}(t_{NN} + t_{FN} + t_{FN_0} + t_{FF_0}) = V_{o2}t_{FF_0}$
5	$a_1 = (G_{NN1} + \|G_{FF1}\|)$, $b_1 = (\|G_{NF1}\| + \|G_{FF1}\|)$, $c_1 = \|G_{FF1}\|(1 - t_{FF_0} - t_{FF_{00}}) + \|G_{FF1_0}\|t_{FF_0}$, $a_2 = (G_{NN2} + \|G_{FF2}\|)$, $b_2 = (\|G_{FF2}\| - \|G_{NF2}\|)$, $c_2 = \|G_{FF2}\|(1 - t_{FF_0} - t_{FF_{00}})$	$V_{in}(t_{NN} + t_{NF} + t_{FF} - k\sqrt{\frac{L_1}{L_2}}t_{FF_0}) = V_{o1}t_{FF} - V_{o2}k\sqrt{\frac{L_1}{L_2}}t_{FF_0})$, $V_{in}(t_{NN} + t_{NF} + t_{FF} + t_{FF_0}) = V_{o2}(t_{NF} + t_{FF} + t_{FF_0})$
6	$a_1 = (G_{NN1} + \|G_{FF1}\|)$, $b_1 = (\|G_{NF1}\| + \|G_{FF1}\|)$, $c_1 = \|G_{FF1}\|(1 - t_{FF_0} - t_{FF_{00}})$, $a_2 = (G_{NN2} + \|G_{FF2}\|)$, $b_2 = (\|G_{FF2}\| - \|G_{NF2}\|)$, $c_2 = \|G_{FF2}\|(1 - t_{FF_0} - t_{FF_{00}}) + G_{FF2_0}t_{FF_0}$	$V_{in}(t_{NN} + t_{NF} + t_{FF} + t_{FF_0}) = V_{o1}(t_{FF} + t_{FF_0})$, $V_{in}(t_{NN} + t_{NF} + t_{FF} - k\sqrt{\frac{L_2}{L_1}}t_{FF_0}) = V_{o2}(t_{NF} + t_{FF}) - V_{o1}k\sqrt{\frac{L_2}{L_1}}t_{FF_0})$
7	$a_1 = (G_{NN1} + \|G_{FF1_0}\|)$, $b_1 = (\|G_{NF1}\| + \|G_{FF1_0}\|)$, $c_1 = \|G_{FF1_0}\|(1 - t_{FF_{00}})$, $a_2 = G_{NN2}$, $b_2 = -\|G_{NF2}\|$, $c_2 = 0$	$V_{in}(t_{NN} + t_{NF} + t_{FF_0}) = V_{o1}t_{FF_0}$, $V_{in}(t_{NN} + t_{NF} - k\sqrt{\frac{L_2}{L_1}}t_{FF_0}) = V_{o2}t_{NF} - V_{o1}k\sqrt{\frac{L_2}{L_1}}t_{FF_0}$
8	$a_1 = (G_{NN1} + \|G_{FF1_0}\|)$, $b_1 = (\|G_{NF1}\| + \|G_{FF1_0}\|)$, $c_1 = \|G_{FF1_0}\|(1-t_{FF_{00}})-(\|G_{FF1_0}\|+\|G_{NF1_0}\|)t_{NF_0}$, $a_2 = G_{NN2}$, $b_2 = -\|G_{NF2}\|$, $c_2 = 0$	$V_{in}(t_{NN}+t_{NF}+t_{NF_0}+t_{FF_0}) = V_{o1}t_{FF_0}$, $V_{in}(t_{NN}+t_{NF}-k\sqrt{\frac{L_2}{L_1}}t_{FF_0} - k\sqrt{\frac{L_2}{L_1}}t_{NF_0}) = V_{o2}t_{NF} - V_{o1}k\sqrt{\frac{L_2}{L_1}}t_{FF_0}$

output relations of each pattern. This table presents the input-output voltage relations of CI-SIDO boost converter for all the possible waveforms of sector 5 when both the boost are in DCM. The input-output voltage relations are also presented for all the possibilities of Sector 5. The duty ratios of CI-SIDO boost converter when both currents are in DCM of Sector 5, for $D_1 > D_2$ is given by–

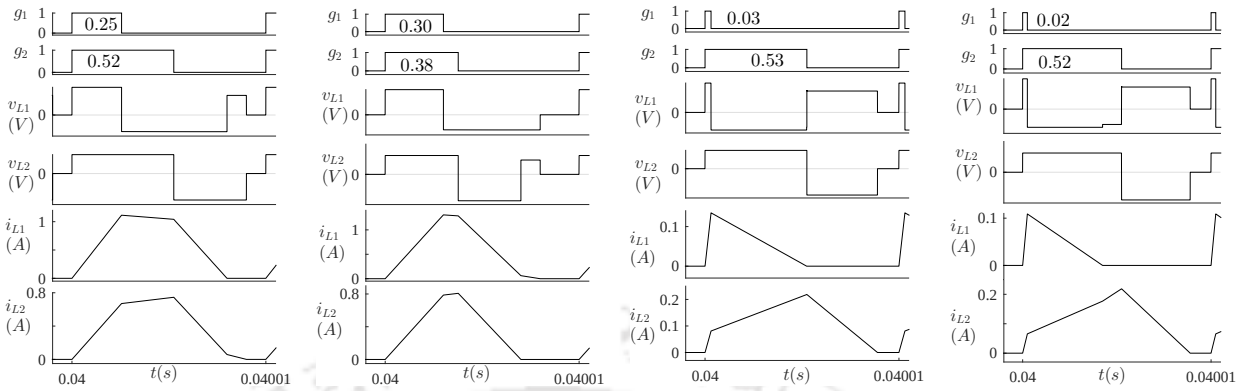
$$D_1 = t_{NN} + t_{NF}, \tag{8.32a}$$

$$D_2 = t_{NN}. \tag{8.32b}$$

8.4.2 Simulation Results

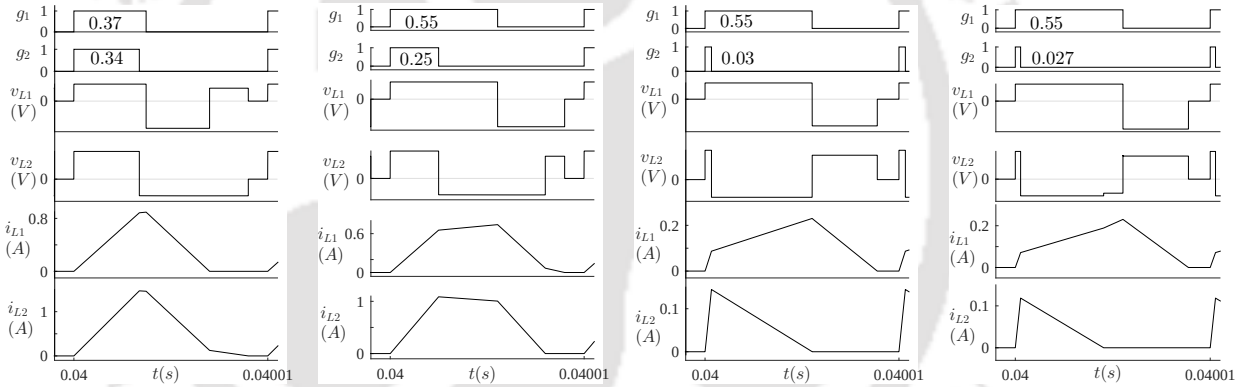
The DCM of the CI-SIDO boost converter is simulated in MATLAB Simulink. This section verifies all the DCM waveforms that are discussed in this section. The analytical expressions of input-output voltage relations are also demonstrated.

Depending on the output voltages to be maintained and the available input voltage, the duty ratios, and the load currents are found using the slope expressions and the durations of each state. In this



(a) Pattern 1 (b) Pattern 2 (c) Pattern 3 (d) Pattern 4

Figure 8.12: MATLAB simulation results of possible DCM waveforms of CI-SIDO boost converter for $D_1 < D_2$ with slope conditions $G_{NN1} > 0$, $G_{FF1} < 0$, $G_{NF1} > 0$, $G_{FN1} < 0$, $G_{NN2} > 0$, $G_{FF2} < 0$, $G_{NF2} < 0$, $G_{FN2} > 0$.



(a) Pattern 5 (b) Pattern 6 (c) Pattern 7 (d) Pattern 8

Figure 8.13: MATLAB simulation results of possible DCM waveforms of CI-SIDO boost converter for $D_1 > D_2$ with slope conditions $G_{NN1} > 0$, $G_{FF1} < 0$, $G_{NF1} > 0$, $G_{FN1} < 0$, $G_{NN2} > 0$, $G_{FF2} < 0$, $G_{NF2} < 0$, $G_{FN2} > 0$.

chapter, the simulations are done such that the output voltages are maintained at 8 V, 12 V, and 8 V, 13 V with the input voltage of 5 V. However, this analysis is valid for any values of input-output voltages as long as the DCM operation is ensured. The output capacitors of 100 μF are used.

For $D_1 < D_2$, the coupled inductors used are $L_1 = 48\ \mu H$, $L_2 = 120\ \mu H$, $k = 0.8$. In Fig. 8.12(a), to maintain the output voltages of 8 V and 12 V, with load currents $i_{o1} = 0.43\ A$, $i_{o2} = 0.11\ A$, the duty ratios obtained are $D_1 = 0.25$, $D_2 = 0.52$ for $t_{FF_{00}} = 0.1$, $t_{FF_0} = 0.1$. Similarly, for load currents $i_{o1} = 0.32\ A$, $i_{o2} = 0.13\ A$, the duty ratios obtained are $D_1 = 0.30$, $D_2 = 0.38$ for $t_{FF_{00}} = 0.1$, $t_{FF_0} = 0.2$, as shown in Fig. 8.12(b). For $D_1 > D_2$, the coupled inductors used are $L_1 = 120\ \mu H$, $L_2 = 48\ \mu H$, $k = 0.8$. In Fig. 8.13(a), to maintain the output voltages of 13 V and 8 V, with load

Table 8.8: Comparisons of Analytical and Simulation Results

Pattern No.	V_{o1} (V)	V_{o2} (V)	V_{in} (V)	Analytical						Simulation					
				D_1	D_2	R_1 (Ω)	R_2 (Ω)	i_{o1} (A)	i_{o2} (A)	D_1	D_2	R_1 (Ω)	R_2 (Ω)	i_{o1} (A)	i_{o2} (A)
1	8	12	5	0.25	0.52	18.46	105.78	0.43	0.11	0.25	0.52	18.50	105.80	0.42	0.12
2	8	12	5	0.30	0.38	24.95	91.89	0.32	0.13	0.30	0.38	24.95	91.90	0.32	0.13
3	8	12	5	0.03	0.53	240.8	292.57	0.03	0.04	0.03	0.53	240.80	292.60	0.03	0.04
4	8	12	5	0.025	0.52	367.48	292.57	0.02	0.04	0.025	0.52	367.50	292.57	0.03	0.05
5	13	8	5	0.37	0.34	88.72	24.73	0.14	0.32	0.37	0.34	88.70	24.75	0.14	0.30
6	13	8	5	0.55	0.25	126.88	18.11	0.10	0.44	0.55	0.25	126.90	18.12	0.12	0.44
7	13	8	5	0.55	0.03	322.36	212.95	0.04	0.03	0.55	0.03	322.40	212.98	0.04	0.03
8	13	8	5	0.55	0.03	322.92	317.13	0.04	0.025	0.55	0.03	322.90	317.15	0.05	0.026

currents $i_{o1} = 0.14\ A$, $i_{o2} = 0.32\ A$, the duty ratios obtained are $D_1 = 0.37$, $D_2 = 0.34$ for $t_{FF_{00}} = 0.1$, $t_{FF_0} = 0.2$. Similarly, for load currents $i_{o1} = 0.10\ A$, $i_{o2} = 0.44\ A$, the duty ratios obtained are $D_1 = 0.55$, $D_2 = 0.25$ for $t_{FF_{00}} = 0.1$, $t_{FF_0} = 0.1$, as shown in Fig. 8.13(b). The details of all the other simulation results are presented in Table 8.8.

The analytical expressions of input-output voltage relations derived using Table 8.7 are verified by comparing them with the simulation results. For the given values of output voltages, the durations of each state are formulated in terms of the input voltages. The relations between input-output voltages in Table 8.7, finally help to calculate input voltage. The obtained duty ratios and the loads are used for the MATLAB simulations. The duty ratios, and the load currents obtained analytically is compared with the simulation results in Table 8.8. The analytical and the simulation results are matching.

8.5 Summary of the Chapter

The following are the findings of the chapter–

(i) As the first boost enters DCM, the slopes of i_{L1} and i_{L2} changes in each state. This changes the waveforms of i_{L1}, i_{L2}, i_{d1}, i_{d2}, i_{in}. The formulated slopes are presented in Table 8.2.

(ii) When the first boost is in DCM and the second boost in CCM, it is found that the body diode turns ON in Sectors 1, 2, and 3 only. The condition to turn ON S_{DB1} is given by (8.3).

(iii) The average value of i_{L1} may become negative when S_{DB1} is ON depending on the values of k, L_1, L_2, V_{o1}, V_{o2}, V_{in}. As the average values of i_{in} is the sum of the average values of i_{L1} and i_{L2}, its value can take negative values depending on the average value of i_{L1} and i_{L2}. When S_{DB1} is OFF, i_{L1} is never negative. Therefore, negative i_{in} is also not possible.

(iv) In practical applications where output voltages are maintained constant, the effect of variation is V_{in} is found. It is found that for a given k, L_1, L_2, V_{o1}, and V_{o2}, the range of V_{in} exists for each sector. As V_{in} increases, the converter may remain in the same sector or may change the sector. In both the case, as V_{in} increase, average values of i_{L1} decrease.

(v) As the load current of the first boost decreases and enters DCM, the average values of the first inductor current also decrease. As the second load current is not changed, there is no significant change in the average values of the second inductor current. With the decrease in i_{o1}, D_1 decreases in DCM whereas D_2 changes with V_{in} as it is in CCM.

(vi) The current stress decreases compared to the CCM operations. However, the voltage stress depends on the voltages and coupled inductor parameters.

(vii) The input-output voltage relations depend on the input voltage, both output voltages, and coupled inductor parameters.

(viii) The two inductor currents can reach zero in many different possible ways. A small change in how inductor currents become zero affects the performance of the CI-SIDO boost converter.

(ix) The duty ratios in DCM depend on the duration of the states. The loads are calculated by finding the area under the curve of the diode current plots.

9

Conclusions and Future Scope of Work

Contents

9.1 Conclusion

The three coupled inductor single input dual output (CI-SIDO) converters- CI-SIDO buck, CI-SIDO boost, and CI-SIDO buck-boost are analysed in this thesis. This type of CI-SIDO converter can efficiently generate two different DC voltage levels from only one available DC input voltage with a reduced number of components, reduced losses and increased efficiency. The physical size of the CI-SIDO converters is also reduced due to the introduction of an inversely coupled inductor. The windings of the inversely coupled inductors are such that the flux due to one winding cancels the flux due to the other winding, thus, reducing the core size of the converter.

The analysis of the CI-SIDO converters shows that the converters operate in four switching states. The slopes of both the inductor currents in all four states are different from each other. The slopes and the current ripples depend on the input, and output voltages, duty ratios and coupled inductor parameters. The current ripples do not depend on the load currents, output power and load demands. It is found that the CI-SIDO converters have 36 inductor current slope possibilities. It is difficult to analyze each pattern of all CI-SIDO converters separately. An approach is presented to unify the analysis of CI-SIDO converters by forming sectors of duty ratios. It is found that 16 sectors of duty ratios are possible for CI-SIDO converters. The sector formation unifies the patterns of inductor currents, input current, and the expressions of current ripples for any values of output input voltage and coupled inductor parameter. It is also found that the sector formations of CI-SIDO boost and CI-SIDO buck-boost converters are the same. These converters always form nine sectors irrespective of the coupled inductor parameter values. In the CI-SIDO buck converter, all nine sectors are not formed simultaneously. Amongst nine sectors, which sector gets formed depends on the coupled inductor parameter values. If the coupled inductors are changed, the dimensions of nine sectors change in CI-SIDO boost and CI-SIDO buck-boost converter, while in CI-SIDO buck, the sector which gets formed also changes, in addition to the change in the dimension of the sectors.

The thesis finds that the current ripples are reduced by introducing the gate pulse shift. The values of gate pulse shift are found for all the sectors of duty ratios of CI-SIDO buck, boost and buck-boost converters. The current ripple reductions for CI-SIDO converters are also extended to

coupled inductor single input triple output (CI-SITO) boost converters. A detailed analysis of the CI-SIDO boost converter to achieve maximum ripple cancellation in input current is performed under continuous conduction mode (CCM). A method is proposed to design the CI-SIDO boost converter with the zero ripple input current. In the case of operating conditions where absolute zero ripples in input current are not possible, a design method is proposed such that the input current ripple remains within a desired specified limit. It is further found that there is no undesirable effect of gate pulse shifting on any of the variables of the CI-SIDO converter, such as the average value of inductor current, input current, and output voltage ripples.

By introducing the gate pulse shift, the CCM/DCM boundary of the CI-SIDO boost converters is reduced without increasing the inductance values. The shift decreases the average inductor current at CCM/DCM boundary, thus, decreasing the critical inductances of the CI-SIDO boost converter. The range of CCM operations is increased as the CCM/DCM boundary is decreased. The thesis finds the gate pulse shift where the average inductor current at the CCM/DCM boundary is minimum for all 36 cases of CI-SIDO boost converter. The expressions of minimum average inductor current at the CCM/DCM boundary are also found for all 36 cases. The CI-SIDO boost converter is also analysed for the discontinuous conduction mode (DCM) operation. As the converter enters DCM, the body diode of the MOSFETs turns ON, making the inductor currents negative. The sectors in which the body diode turns ON are identified. The current stress decreases compared to the CCM operations. However, the voltage stress depends on the voltages and coupled inductor parameters. The input-output voltage relations depend on the input voltage, output voltages, load currents and coupled inductor parameters. It is observed that the two inductor currents can reach zero in many different possible ways. A small change in how inductor currents become zero affects the performance of the CI-SIDO boost converter.

9.2 Future Scope

Some possible directions in which the present work can be extended are–

- The zero ripple input currents in CI-SIDO converters are an important factor to be considered while designing converters. This research work only presents the zero ripple input current

conditions for the CI-SIDO boost converter. A unified approach can be obtained where zero ripple input currents are obtained for all the CI-SIDO converters.

- The CCM/DCM boundary and DCM analysis presented for the CI-SIDO boost converter is equally applicable to all the CI-SIDO converters. The investigation is carried out without any assumptions; therefore, it can be extended to CI-SIDO buck and CI-SIDO buck-boost. However, this requires experimental verifications.

- The effect of gate pulse shift on DCM analysis of CI-SIDO needs further investigation. It is observed that the converter frequently goes into DCM due to reduced load currents. Thus, it is also desirable to know the effect of gate pulse shift on DCM analysis of CI-SIDO converters.

- The closed-loop control of the converter is required to regulate the output voltages against the line and load variations. The impact of closed-loop control on the proposed design method needs analysis.

- To design controllers, power electronic converters are linearized using state-space averaging methods. The generalized state-space averaged equations for CI-SIDO converters are available in the literature. The implementation and experimental verifications of gate pulse shift on the modelling and design of CI-SIDO converters are needed.

- The CI-SIDO converters are extensively used in microprocessors, electric vehicles, hybrid energy sources, battery charging and portable electronic devices. Implementation of CI-SIDO converters in these applications needs experimental verifications.

A

Numerous Patterns of Inductor Current Waveforms in CI-SIDO Boost Converter

A.1 All Possible Inductor Current Waveforms

A.1.1 When G_{NFw} and G_{FNw} are positive or negative

This section illustrates different sequences of states obtained, as D_t is varied from 0 to 1, for different conditions of D_1, D_2 (Figure A.1 - Figure A.8) when G_{NFw}, G_{FNw} are positive or negative.

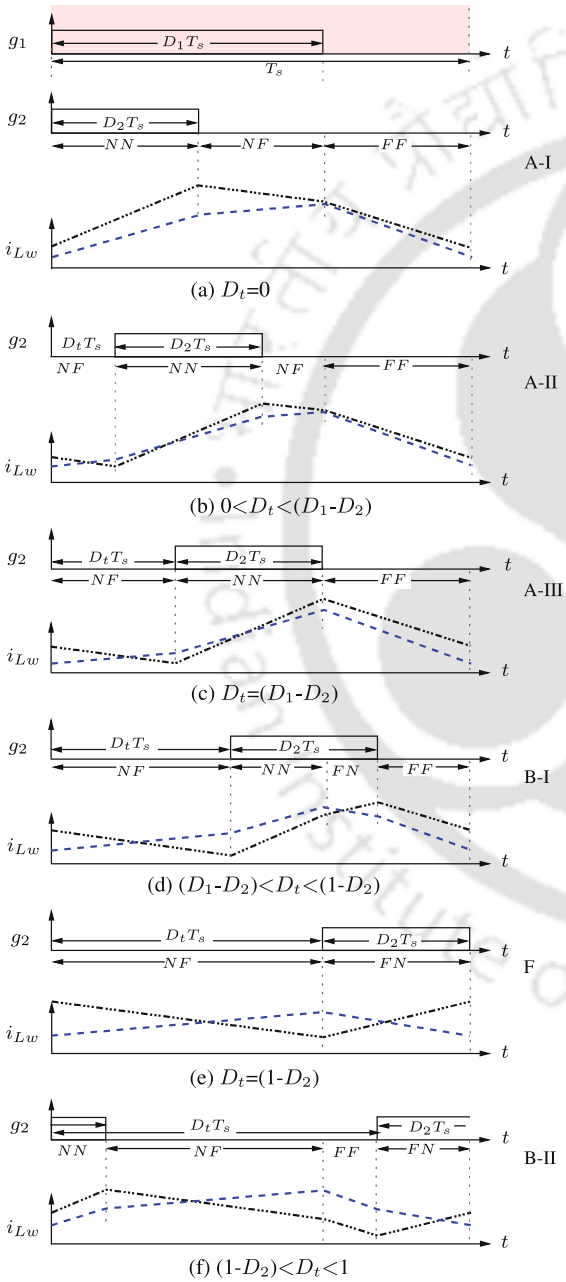


Figure A.1: Different sequences A-I, A-II,... and different patterns of i_{Lw} waveforms for (i) $G_{NF_w} > 0$, $G_{FN_w} < 0$ (blue dashed lines), (ii) $G_{NF_w} < 0$, $G_{FN_w} > 0$ (black dash-dotted lines) when $(D_1 + D_2) = 1$ and $D_1 > D_2$ (i.e. SR-7) as D_t varied from 0 to 1.

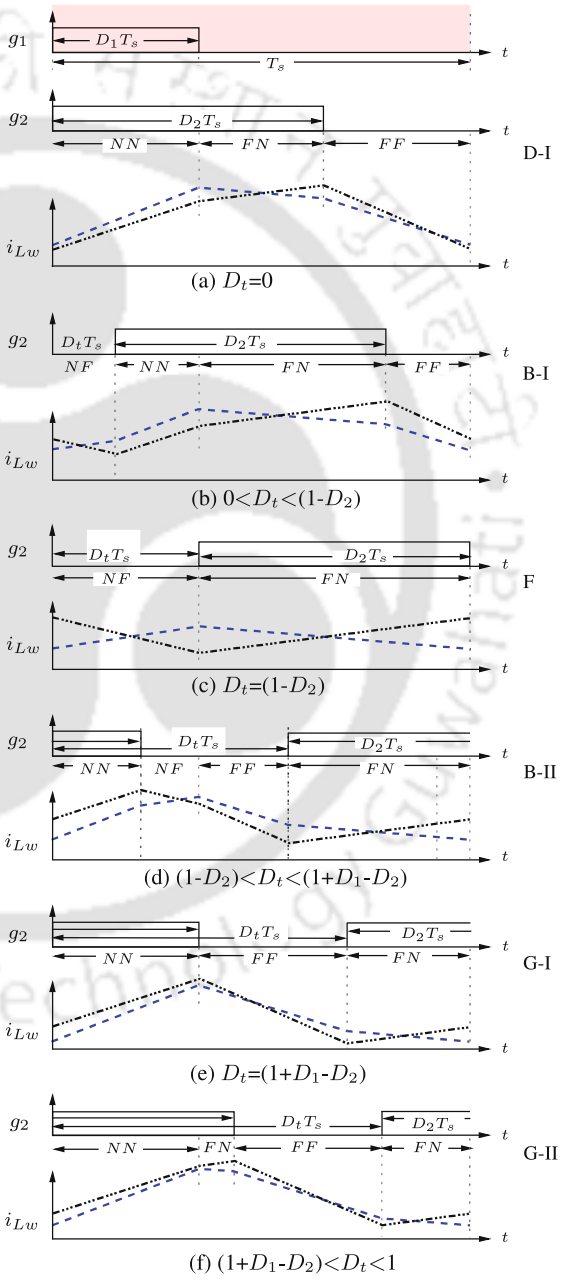


Figure A.2: Different sequences D-I, B-I,... and different patterns of i_{Lw} waveforms for (i) $G_{NF_w} > 0$, $G_{FN_w} < 0$ (blue dashed lines), (ii) $G_{NF_w} < 0$, $G_{FN_w} > 0$ (black dash-dotted lines) when $(D_1 + D_2) = 1$ and $D_1 < D_2$ (i.e. SR-8) as D_t varied from 0 to 1.

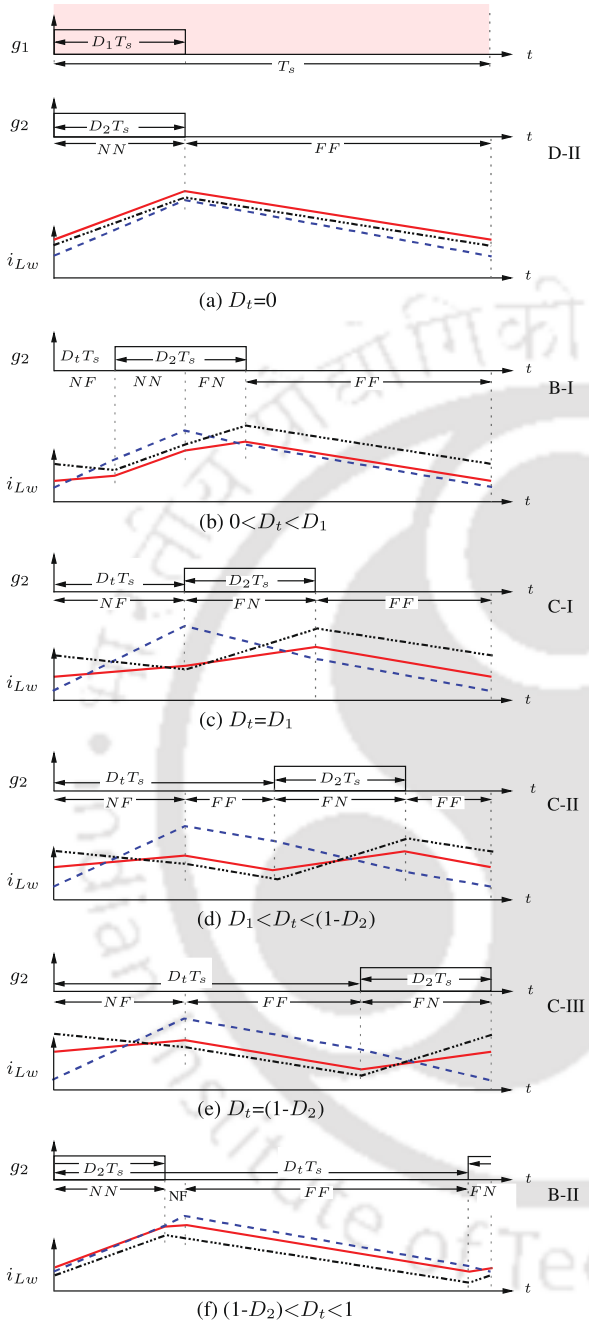


Figure A.3: Different sequences D-II, B-I,... and different patterns of i_{Lw} waveforms for (i) $G_{NF_w} > 0$, $G_{FN_w} > 0$ (red solid lines), (ii) $G_{NF_w} > 0$, $G_{FN_w} < 0$ (blue dashed lines), (iii) $G_{NF_w} < 0$, $G_{FN_w} > 0$ (black dash-dotted lines) when $(D_1 + D_2) < 1$ and $D_1 = D_2$ (i.e. SR-3) as D_t varied from 0 to 1.

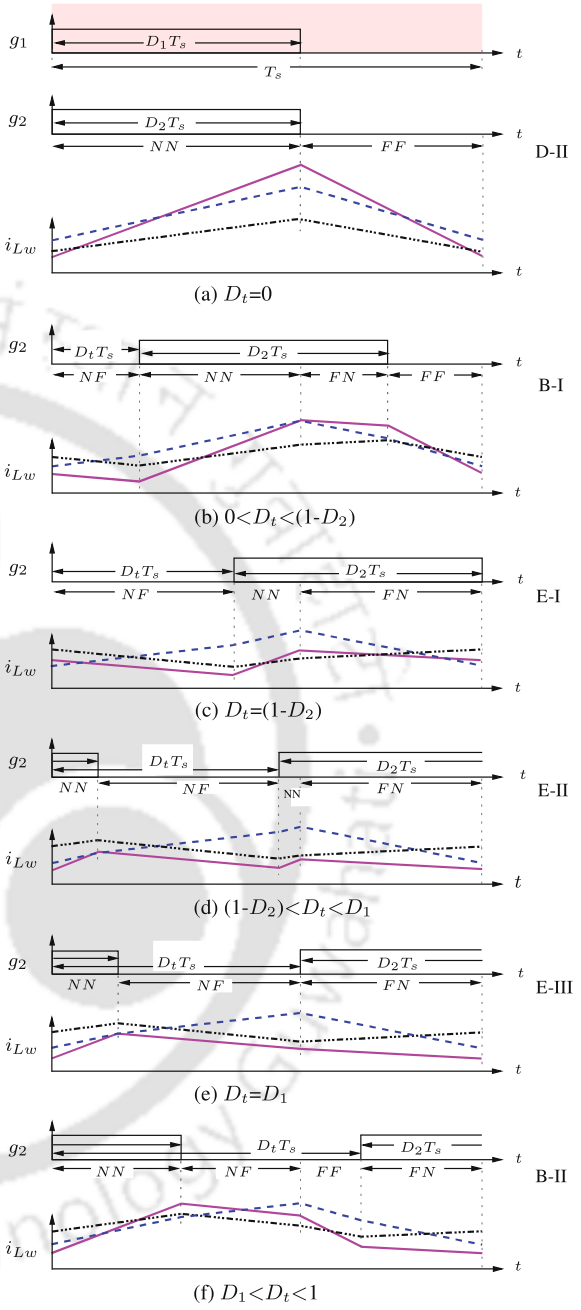


Figure A.4: Different sequences D-II, B-I,... and different patterns of i_{Lw} waveforms for (i) $G_{NF_w} < 0$, $G_{FN_w} < 0$ (magenta solid lines), (ii) $G_{NF_w} > 0$, $G_{FN_w} < 0$ (blue dashed lines), (iii) $G_{NF_w} < 0$, $G_{FN_w} > 0$ (black dash-dotted lines) when $(D_1 + D_2) > 1$ and $D_1 = D_2$ (i.e. SR-6) as D_t varied from 0 to 1.

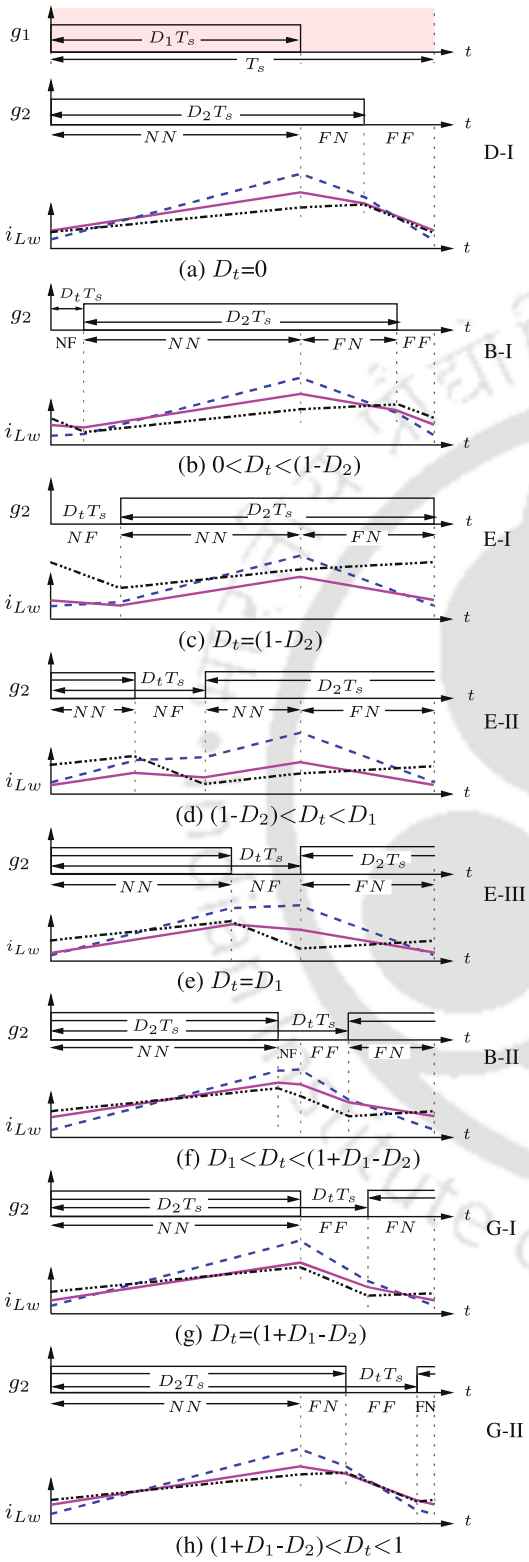


Figure A.5: Different sequences D-I, B-I,... and different patterns of i_{Lw} waveforms for (i) $G_{NF_w} < 0$, $G_{FN_w} < 0$ (magenta solid lines), (ii) $G_{NF_w} > 0$, $G_{FN_w} < 0$ (blue dashed lines), (iii) $G_{NF_w} < 0$, $G_{FN_w} > 0$ (black dash-dotted lines) when $(D_1 + D_2) > 1$ and $D_1 < D_2$ (i.e. SR-5) as D_t varied from 0 to 1.

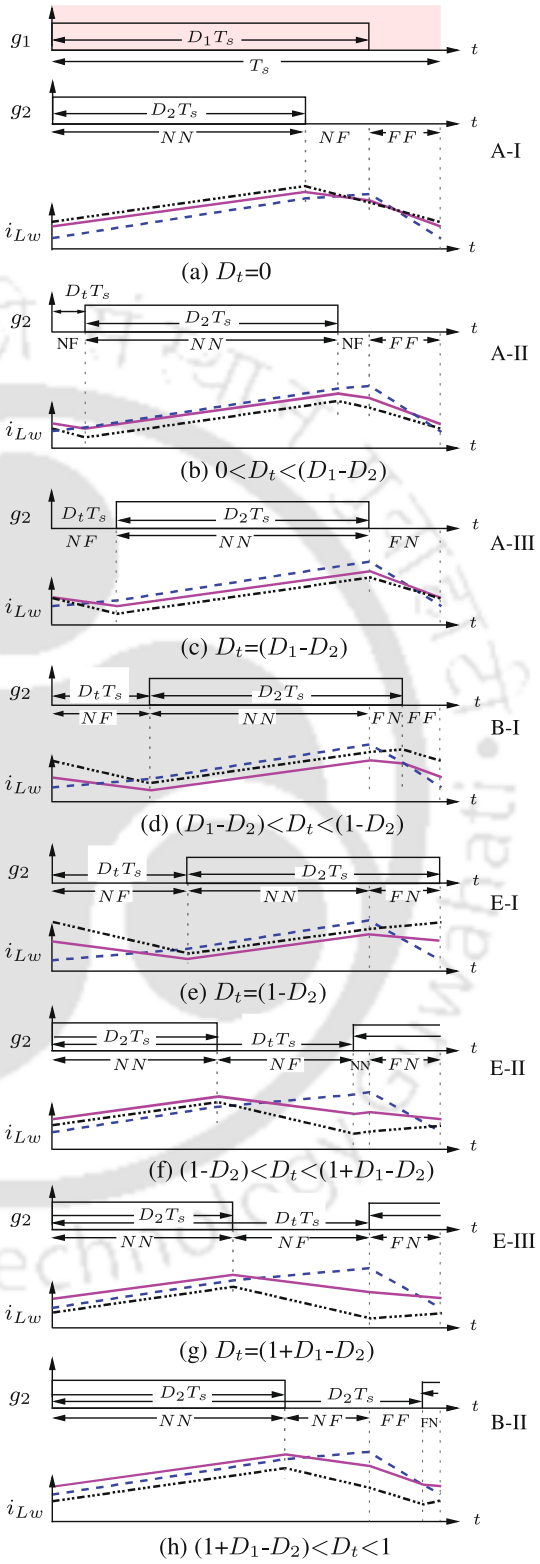


Figure A.6: Different sequences A-I, A-II,... and different patterns of i_{Lw} waveforms for (i) $G_{NF_w} < 0$, $G_{FN_w} < 0$ (magenta solid lines), (ii) $G_{NF_w} > 0$, $G_{FN_w} < 0$ (blue dashed lines), (iii) $G_{NF_w} < 0$, $G_{FN_w} > 0$ (black dash-dotted lines) when $(D_1 + D_2) > 1$ and $D_1 > D_2$ (i.e. SR-4) as D_t varied from 0 to 1.

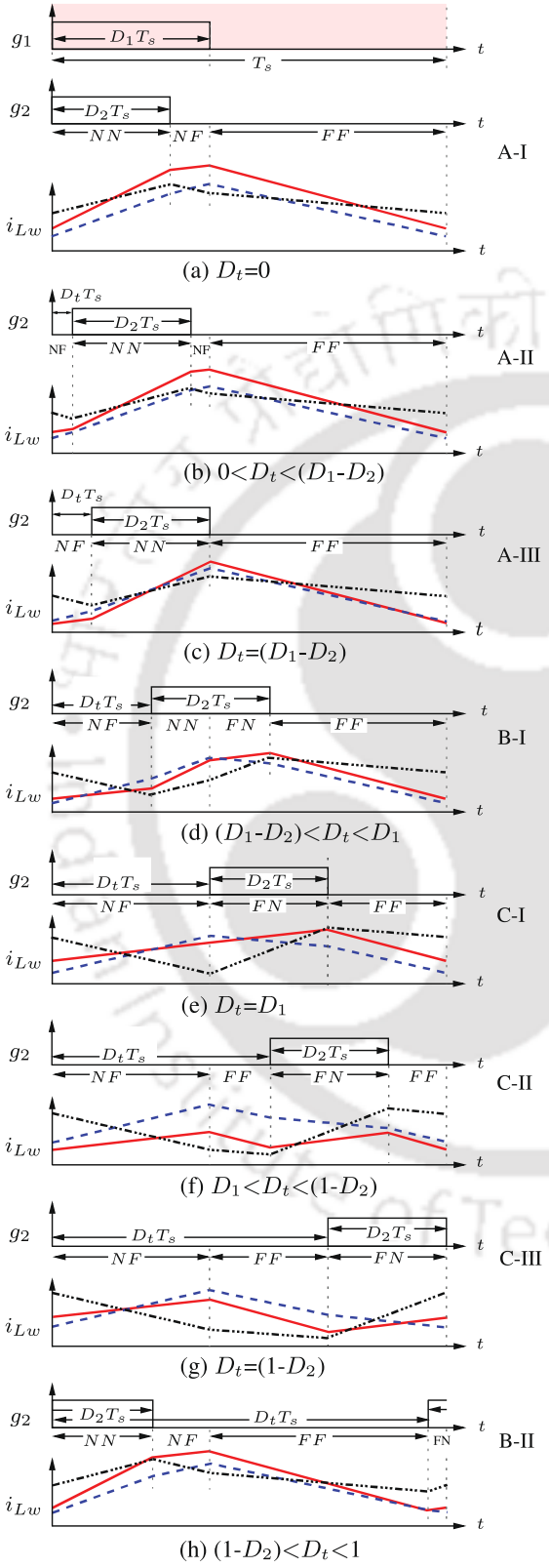


Figure A.7: Different sequences A-I, A-II,... and different patterns of i_{Lw} waveforms for (i) $G_{NF_w} > 0$, $G_{FN_w} > 0$ (red solid lines), (ii) $G_{NF_w} > 0$, $G_{FN_w} < 0$ (blue dashed lines), (iii) $G_{NF_w} < 0$, $G_{FN_w} > 0$ (black dash-dotted lines) when $(D_1 + D_2) < 1$ and $D_1 > D_2$ (i.e. SR-1) as D_t varied from 0 to 1.

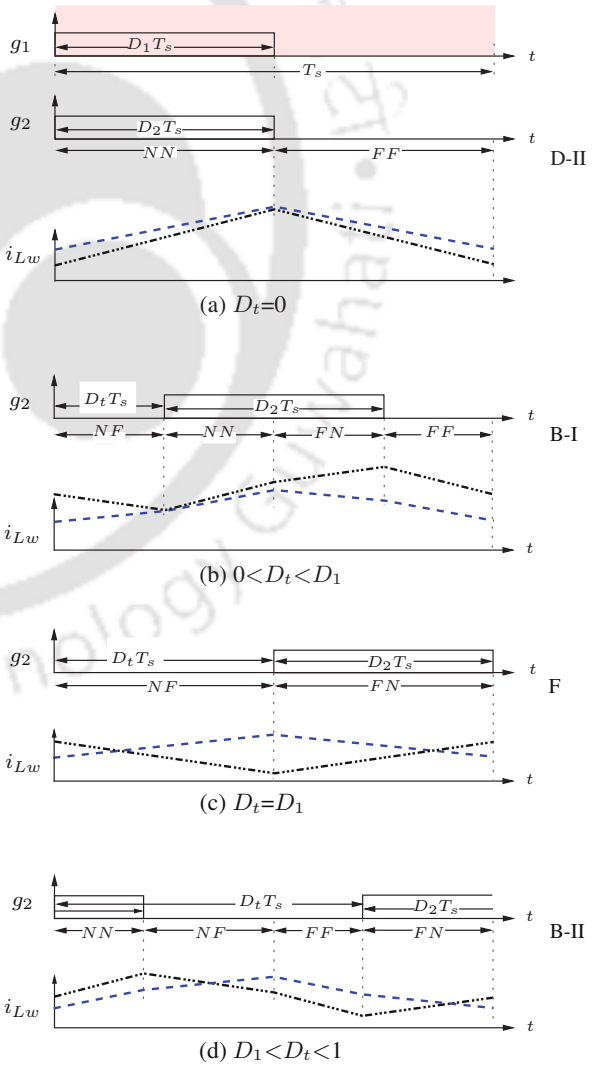


Figure A.8: Different sequences D-II, B-I,... and different patterns of i_{Lw} waveforms for (i) $G_{NF_w} > 0$, $G_{FN_w} < 0$ (blue dashed lines), (ii) $G_{NF_w} < 0$, $G_{FN_w} > 0$ (black dash-dotted lines) when $(D_1 + D_2) = 1$ and $D_1 = D_2$ (i.e. SR-9) as D_t varied from 0 to 1.

A. Numerous Patterns of Inductor Current Waveforms in CI-SIDO Boost Converter

Table A.1: Δi_{Lw} in different sequences for $(D_1 + D_2) < 1$ and $D_1 > D_2$ (i.e. SR-1)

Seq.	Δi_{Lw}			D_t
	$G_{NF_w} > 0, G_{FN_w} > 0$	$G_{NF_w} > 0, G_{FN_w} < 0$	$G_{NF_w} < 0, G_{FN_w} > 0$	
A-I	α_1	α_1	α_{11}	0
A-II	α_1	α_1	α_{11}	$0 < D_t < D_1$
A-III	α_1	α_1	α_{11}	$(D_1 - D_2)$
B-I	$\alpha_1 > \Delta i_{Lw} > \beta_1$	$\alpha_1 > \Delta i_{Lw} > \beta_{11}$	$\alpha_{11} > \Delta i_{Lw} > \beta_{12}$	$(D_1 - D_2) < D_t < D_1$
C-I	β_1	β_{11}	β_{12}	D_1
C-II	$\beta_1 > \Delta i_{Lw} > \gamma_1$	β_{11}	β_{12}	$D_1 < D_t < (D_1 + \underline{D_{PP_w}})$
	γ_1	β_{11}	β_{12}	$(D_1 + \underline{D_{PP_w}}) \le D_t \le (D_1 + \overline{D_{PP_w}})$
	$\gamma_1 < \Delta i_{Lw} < \beta_1$	β_{11}	β_{12}	$(D_1 + \overline{D_{PP_w}}) < D_t < (1 - D_2)$
C-III	β_1	β_{11}	β_{12}	$(1 - D_2)$
B-II	$\beta_1 < \Delta i_{Lw} < \alpha_1$	$\beta_{11} < \Delta i_{Lw} < \alpha_1$	$\beta_{12} < \Delta i_{Lw} < \alpha_{11}$	$(1 - D_2) < D_t < 1$

$\alpha_1 \equiv G_{NN_w} D_2 T_s + G_{NF_w}(D_1 - D_2)T_s, \quad \alpha_{11} \equiv G_{NN_w} D_2 T_s$
$\beta_1 \equiv G_{NF_w} D_1 T_s + G_{FN_w} D_2 T_s, \quad \beta_{11} \equiv G_{NF_w} D_1 T_s, \quad \beta_{12} \equiv G_{FN_w} D_2 T_s$
$\gamma_1 \equiv Max\{G_{NF_w} D_1 T_s, G_{FN_w} D_2 T_s\}$

Table A.2: Δi_{Lw} in different sequences for $(D_1 + D_2) < 1$ and $D_1 < D_2$ (i.e. SR-2)

Seq.	Δi_{Lw}			D_t
	$G_{NF_w} > 0, G_{FN_w} > 0$	$G_{NF_w} > 0, G_{FN_w} < 0$	$G_{NF_w} < 0, G_{FN_w} > 0$	
D-I	α_2	α_{21}	α_2	0
B-I	$\alpha_2 > \Delta i_{Lw} > \beta_2$	$\alpha_{21} > \Delta i_{Lw} > \beta_{21}$	$\alpha_2 > \Delta i_{Lw} > \beta_{22}$	$0 < D_t < D_1$
C-I	β_2	β_{21}	β_{22}	D_1
C-II	$\beta_2 > \Delta i_{Lw} > \gamma_2$	β_{21}	β_{22}	$D_1 < D_t < (D_1 + \underline{D_{PP_w}})$
	γ_2	β_{21}	β_{22}	$(D_1 + \underline{D_{PP_w}}) \le D_t \le (D_1 + \overline{D_{PP_w}})$
	$\gamma_2 < \Delta i_{Lw} < \beta_2$	β_{21}	β_{22}	$(D_1 + \overline{D_{PP_w}}) < D_t < (1 - D_2)$
C-III	β_2	β_{21}	β_{22}	$(1 - D_2)$
B-II	$\beta_2 < \Delta i_{Lw} < \alpha_2$	$\beta_{21} < \Delta i_{Lw} < \alpha_{21}$	$\beta_{22} < \Delta i_{Lw} < \alpha_2$	$(1 - D_2) < D_t < (1 + D_1 - D_2)$
G-I	α_2	α_{21}	α_2	$(1 + D_1 - D_2)$
G-II	α_2	α_{21}	α_2	$(1 + D_1 - D_2) < D_t < 1$

$\alpha_2 \equiv G_{NN_w} D_1 T_s + G_{FN_w}(D_2 - D_1)T_s, \quad \alpha_{21} \equiv G_{NN_w} D_1 T_s$
$\beta_2 \equiv G_{NF_w} D_1 T_s + G_{FN_w} D_2 T_s, \quad \beta_{21} \equiv G_{NF_w} D_1 T_s, \quad \beta_{22} \equiv G_{FN_w} D_2 T_s$
$\gamma_2 \equiv Max\{G_{NF_w} D_1 T_s, G_{FN_w} D_2 T_s\}$

Table A.3: Δi_{Lw} in different sequences for $(D_1 + D_2) = 1$ and $D_1 = D_2$ (i.e. SR-9)

Seq.	Δi_{Lw}		D_t
	$G_{NF_w} > 0, G_{FN_w} < 0$	$G_{NF_w} < 0, G_{FN_w} > 0$	
D-II	α_9	α_9	0
B-I	$\alpha_9 > \Delta i_{Lw} > \beta_9$	$\alpha_9 > \Delta i_{Lw} > \beta_9$	$0 < D_t < D_1$
F	β_9	β_9	D_1
B-II	$\beta_9 < \Delta i_{Lw} < \alpha_9$	$\beta_9 < \Delta i_{Lw} < \alpha_9$	$D_1 < D_t < 1$

$\alpha_9 \equiv G_{NN_w} D_1 T_s$
$\beta_9 \equiv G_{NF_w} D_1 T_s$

Table A.4: Δi_{Lw} in different sequences for $(D_1 + D_2) < 1$ and $D_1 = D_2$ (i.e. SR-3)

Seq.	Δi_{Lw}			D_t
	$G_{NF_w} > 0, G_{FN_w} > 0$	$G_{NF_w} > 0, G_{FN_w} < 0$	$G_{NF_w} < 0, G_{FN_w} > 0$	
D-II	α_3	α_3	α_3	0
B-I	$\alpha_3 > \Delta i_{Lw} > \beta_3$	$\alpha_3 > \Delta i_{Lw} > \beta_{31}$	$\alpha_3 > \Delta i_{Lw} > \beta_{32}$	$0 < D_t < D_1$
C-I	β_3	β_{31}	β_{32}	D_1
C-II	$\beta_3 > \Delta i_{Lw} > \gamma_3$	β_{31}	β_{32}	$D_1 < D_t < (D_1 + \underline{D_{PP_w}})$
	γ_3	β_{31}	β_{32}	$(D_1 + \underline{D_{PP_w}}) \le D_t \le (D_1 + \overline{D_{PP_w}})$
	$\gamma_3 < \Delta i_{Lw} < \beta_3$	β_{31}	β_{32}	$(D_1 + \overline{D_{PP_w}}) < D_t < (1 - D_2)$
C-III	β_3	β_{31}	β_{32}	$(1 - D_2)$
B-II	$\beta_3 < \Delta i_{Lw} < \alpha_3$	$\beta_{31} < \Delta i_{Lw} < \alpha_3$	$\beta_{32} < \Delta i_{Lw} < \alpha_3$	$(1 - D_2) < D_t < 1$

$\alpha_3 \equiv G_{NN_w} D_1 T_s$
$\beta_3 \equiv G_{NF_w} D_1 T_s + G_{FN_w} D_1 T_s, \quad \beta_{31} \equiv G_{NF_w} D_1 T_s, \quad \beta_{32} \equiv G_{FN_w} D_1 T_s$
$\gamma_3 \equiv Max\{G_{NF_w} D_1 T_s, G_{FN_w} D_2 T_s\}$

Table A.5: Δi_{Lw} in different sequences for $(D_1 + D_2) > 1$ and $D_1 > D_2$ (i.e. SR-4)

Seq.	Δi_{Lw}			D_t
	$G_{NF_w} < 0, G_{FN_w} < 0$	$G_{NF_w} > 0, G_{FN_w} < 0$	$G_{NF_w} < 0, G_{FN_w} > 0$	
A-I	α_{41}	α_4	α_{41}	0
A-II	α_{41}	α_4	α_{41}	$0 < D_t < (D_1 - D_2)$
A-III	α_{41}	α_4	α_{41}	$(D_1 - D_2)$
B-I	$\alpha_{41} > \Delta i_{Lw} > \beta_{41}$	$\alpha_4 > \Delta i_{Lw} > \zeta_4$	$\alpha_{41} > \Delta i_{Lw} > \beta_4$	$(D_1 - D_2) < D_t < (1 - D_2)$
E-I	β_{41}	ζ_4	β_4	$(1 - D_2)$
E-II	$\beta_{41} > \Delta i_{Lw} > \gamma_4$	ζ_4	β_4	$(1 - D_2) < D_t < (D_1 - \overline{D_{NN_w}})$
	γ_4	ζ_4	β_4	$(D_1 - \overline{D_{NN_w}}) \le D_t \le (D_1 - \underline{D_{NN_w}})$
	$\gamma_4 < \Delta i_{Lw} < \beta_{41}$	ζ_4	β_4	$(D_1 - \underline{D_{NN_w}}) < D_t < D_1$
E-III	β_{41}	ζ_4	β_4	D_1
B-II	β_{41}	$\zeta_4 < \Delta i_{Lw} < \alpha_4$	$\beta_4 < \Delta i_{Lw} < \alpha_{41}$	$D_1 < D_t < 1$

$\alpha_4 \equiv G_{NN_w} D_2 T_s + G_{NF_w}(D_1 - D_2) T_s, \quad \alpha_{41} \equiv G_{NN_w} D_2 T_s$
$\beta_4 \equiv G_{NN_w}(D_1 + D_2 - 1) T_s + G_{FN_w}(1 - D_1) T_s, \quad \beta_{41} \equiv G_{NN_w}(D_1 + D_2 - 1) T_s, \quad \beta_{42} \equiv |G_{FN_w}|(1 - D_1) T_s$
$\zeta_4 \equiv G_{NN_w}(D_1 + D_2 - 1) T_s + G_{NF_w}(1 - D_2) T_s, \quad \zeta_{42} \equiv |G_{NF_w}|(1 - D_2) T_s$
$\gamma_4 \equiv Max\{|G_{NF_w}|(1 - D_2) T_s, |G_{FN_w}|(1 - D_1) T_s\}$

Table A.6: Δi_{Lw} in different sequences for $(D_1 + D_2) = 1$ and $D_1 < D_2$ (i.e. SR-8)

Seq.	Δi_{Lw}		D_t
	$G_{NF_w} > 0, G_{FN_w} < 0$	$G_{NF_w} < 0, G_{FN_w} > 0$	
D-I	α_{81}	α_8	0
B-I	$\alpha_{81} > \Delta i_{Lw} > \beta_8$	$\alpha_8 > \Delta i_{Lw} > \gamma_8$	$0 < D_t < D_1$
F	β_8	γ_8	D_1
B-II	$\beta_8 < \Delta i_{Lw} < \alpha_{81}$	$\gamma_8 < \Delta i_{Lw} < \alpha_8$	$D_1 < D_t < (1 + D_1 - D_2)$
G-I	α_{81}	α_8	$(1 + D_1 - D_2)$
G-II	α_{81}	α_8	$(1 + D_1 - D_2) < D_t < 1$

$\alpha_8 \equiv G_{NN_w} D_1 T_s + G_{FN_w}(D_2 - D_1) T_s, \quad \alpha_{81} \equiv G_{NN_w} D_1 T_s$
$\beta_8 \equiv G_{NF_w} D_1 T_s$
$\gamma_8 \equiv G_{FN_w} D_2 T_s$

Table A.7: Δi_{Lw} in different sequences for $(D_1 + D_2) > 1$ and $D_1 < D_2$ (i.e. SR-5)

Seq.	Δi_{Lw}			D_t
	$G_{NF_w} < 0, G_{FN_w} < 0$	$G_{NF_w} > 0, G_{FN_w} < 0$	$G_{NF_w} < 0, G_{FN_w} > 0$	
D-I	α_{51}	α_{51}	α_5	0
B-I	$\alpha_{51} > \Delta i_{Lw} > \beta_{51}$	$\alpha_{51} > \Delta i_{Lw} > \zeta_5$	$\alpha_5 > \Delta i_{Lw} > \beta_5$	$0 < D_t < (1 - D_2)$
E-I	β_{51}	ζ_5	β_5	$(1 - D_2)$
E-II	$\beta_{51} > \Delta i_{Lw} > \gamma_5$	ζ_5	β_5	$(1 - D_2) < D_t < (D_1 - \overline{D_{NN_w}})$
	γ_5	ζ_5	β_5	$(D_1 - \overline{D_{NN_w}}) \le D_t \le (D_1 - \underline{D_{NN_w}})$
	$\gamma_5 < \Delta i_{Lw} < \beta_{51}$	ζ_5	β_5	$(D_1 - \underline{D_{NN_w}}) < D_t < D_1$
E-III	β_{51}	ζ_5	β_5	D_1
B-II	$\beta_{51} < \Delta i_{Lw} < \alpha_{51}$	$\zeta_5 < \Delta i_{Lw} < \alpha_{51}$	$\beta_5 < \Delta i_{Lw} < \alpha_5$	$D_1 < D_t < (1 + D_1 - D_2)$
G-I	α_{51}	α_{51}	α_5	$(1 + D_1 - D_2)$
G-II	α_{51}	α_{51}	α_5	$(1 + D_1 - D_2) < D_t < 1$

$\alpha_5 \equiv G_{NN_w} D_1 T_s + G_{FN_w}(D_2 - D_1)T_s, \quad \alpha_{51} \equiv G_{NN_w} D_1 T_s$
$\beta_5 \equiv G_{NN_w}(D_1 + D_2 - 1)T_s + G_{FN_w}(1 - D_1)T_s, \quad \beta_{51} \equiv G_{NN_w}(D_1 + D_2 - 1)T_s$
$\zeta_5 \equiv G_{NN_w}(D_1 + D_2 - 1)T_s + G_{NF_w}(1 - D_2)T_s$
$\gamma_5 \equiv Max\{|G_{NF_w}|(1 - D_2)T_s, |G_{FN_w}|(1 - D_1)T_s\}$

Table A.8: Δi_{Lw} in different sequences for $(D_1 + D_2) > 1$ and $D_1 = D_2$ (i.e. SR-6)

Seq.	Δi_{Lw}			D_t
	$G_{NF_w} < 0, G_{FN_w} < 0$	$G_{NF_w} > 0, G_{FN_w} < 0$	$G_{NF_w} < 0, G_{FN_w} > 0$	
D-II	α_{61}	α_{61}	α_{61}	0
B-I	$\alpha_{61} > \Delta i_{Lw} > \beta_{61}$	$\alpha_{61} > \Delta i_{Lw} > \zeta_6$	$\alpha_{61} > \Delta i_{Lw} > \beta_6$	$0 < D_t < (1 - D_2)$
E-I	β_{61}	ζ_6	β_6	$(1 - D_2)$
E-II	$\beta_{61} > \Delta i_{Lw} > \gamma_6$	ζ_6	β_6	$(1 - D_2) < D_t < (D_1 - \overline{D_{NN_w}})$
	γ_6	ζ_6	β_6	$(D_1 - \overline{D_{NN_w}}) \le D_t \le (D_1 - \underline{D_{NN_w}})$
	$\gamma_6 < \Delta i_{Lw} < \beta_{61}$	ζ_6	β_6	$(D_1 - \underline{D_{NN_w}}) < D_t < D_1$
E-III	β_{61}	ζ_6	β_6	D_1
B-II	$\beta_{61} < \Delta i_{Lw} < \alpha_{61}$	$\zeta_6 < \Delta i_{Lw} < \alpha_{61}$	$\beta_6 < \Delta i_{Lw} < \alpha_{61}$	$D_1 < D_t < 1$

$\alpha_{61} \equiv G_{NN_w} D_1 T_s$
$\beta_6 \equiv G_{NN_w}(D_1 + D_2 - 1)T_s + G_{FN_w}(1 - D_1)T_s, \quad \beta_{61} \equiv G_{NN_w}(D_1 + D_2 - 1)T_s$
$\zeta_6 \equiv G_{NN_w}(D_1 + D_2 - 1)T_s + G_{NF_w}(1 - D_2)T_s$
$\gamma_6 \equiv Max\{|G_{NF_w}|(1 - D_2)T_s, |G_{FN_w}|(1 - D_1)T_s\}$

Table A.9: Δi_{Lw} in different sequences for $(D_1 + D_2) = 1$ and $D_1 > D_2$ (i.e. SR-7)

Seq.	Δi_{Lw}		D_t
	$G_{NF_w} > 0, G_{FN_w} < 0$	$G_{NF_w} < 0, G_{FN_w} > 0$	
A-I	α_7	α_{71}	0
A-II	α_7	α_{71}	$0 < D_t < (D_1 - D_2)$
A-III	α_7	α_{71}	$(D_1 - D_2)$
B-I	$\alpha_7 > \Delta i_{Lw} > \beta_7$	$\alpha_{71} > \Delta i_{Lw} > \gamma_7$	$(D_1 - D_2) < D_t < D_1$
F	β_7	γ_7	D_1
B-II	$\beta_7 < \Delta i_{Lw} < \alpha_7$	$\gamma_7 < \Delta i_{Lw} < \alpha_{71}$	$D_1 < D_t < 1$

$\alpha_7 \equiv G_{NN_w} D_2 T_s + G_{NF_w}(D_1 - D_2)T_s, \quad \alpha_{71} \equiv G_{NN_w} D_2 T_s$
$\beta_7 \equiv G_{NF_w} D_1 T_s$
$\gamma_7 \equiv G_{FN_w} D_2 T_s$

A.1.2 When Either G_{NFw} or G_{FNw} are Zero

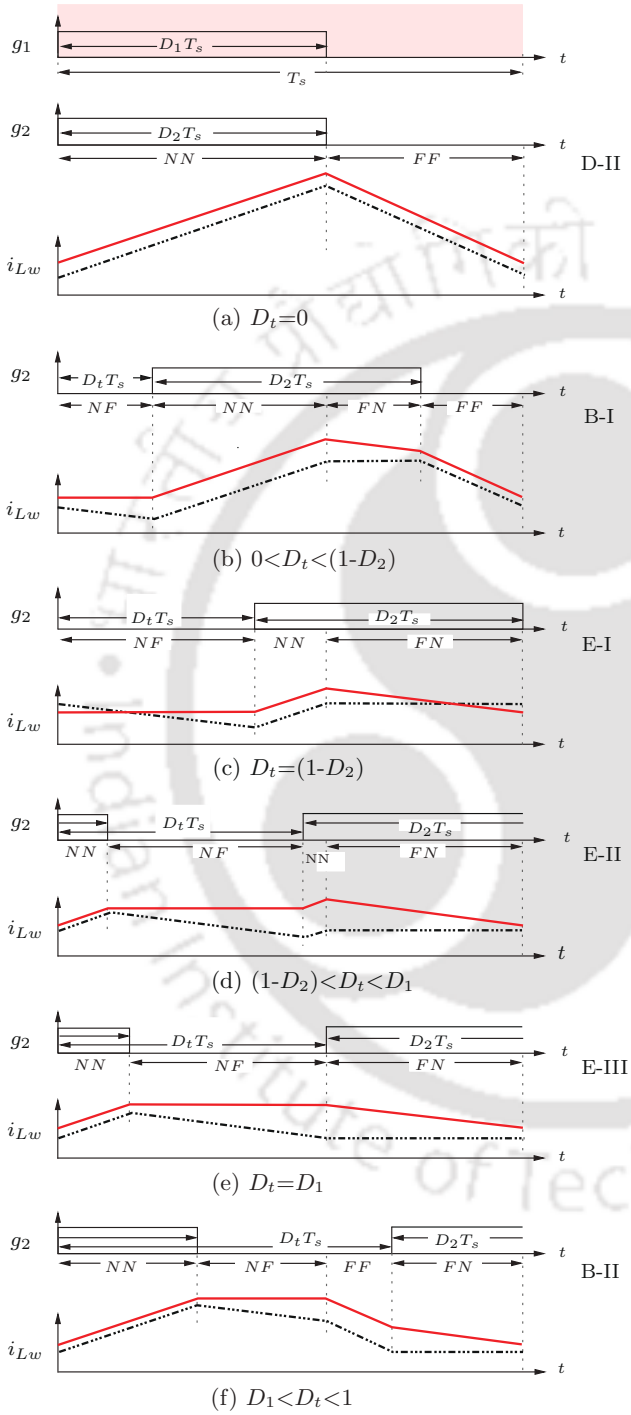


Figure A.9: Different sequences D-II, B-I,... and different patterns of i_{Lw} waveforms for (i) $G_{NF_w} = 0$, $G_{FN_w} < 0$ (red solid lines), (ii) $G_{NF_w} < 0$, $G_{FN_w} = 0$ (black dash-dotted lines) when $(D_1 + D_2) > 1$ and $D_1 = D_2$ (i.e. SR-3) as D_t varied from 0 to 1.

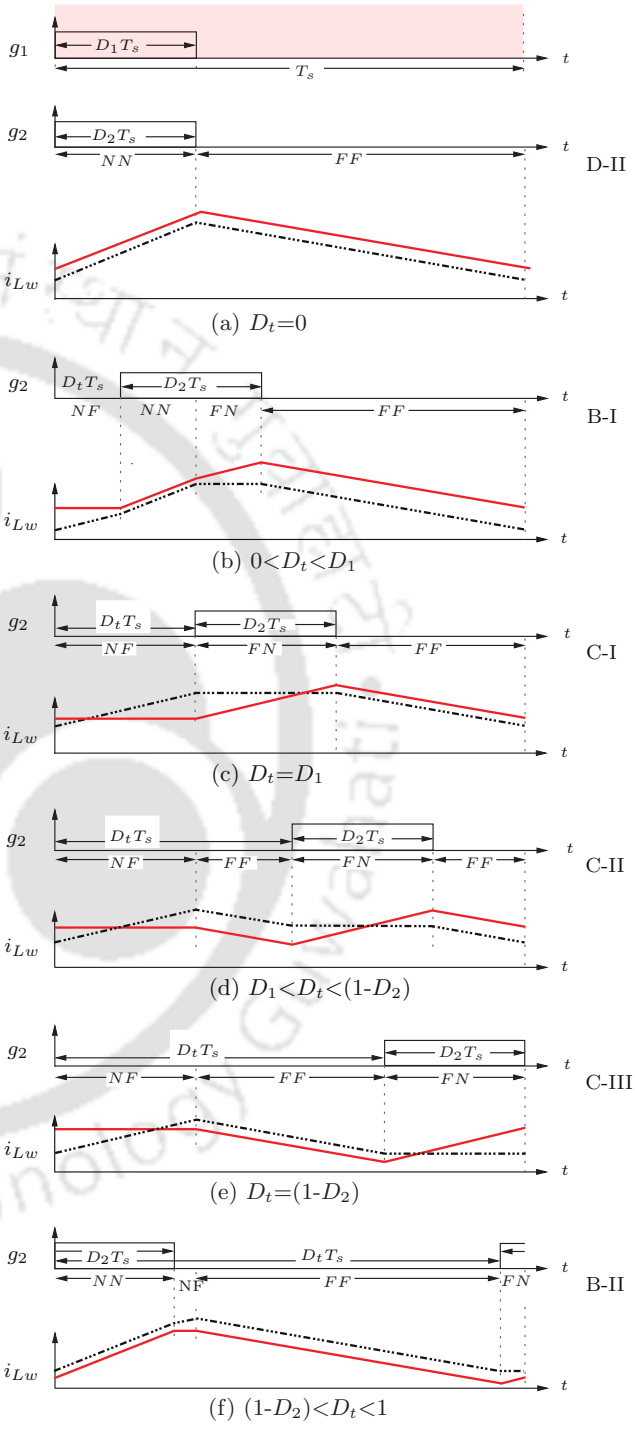


Figure A.10: Different sequences D-II, B-I,... and different patterns of i_{Lw} waveforms for (i) $G_{NF_w} = 0$, $G_{FN_w} > 0$ (red solid lines), (ii) $G_{NF_w} > 0$, $G_{FN_w} = 0$ (black dash-dotted lines) when $(D_1 + D_2) < 1$ and $D_1 = D_2$ (i.e. SR-6) as D_t varied from 0 to 1.

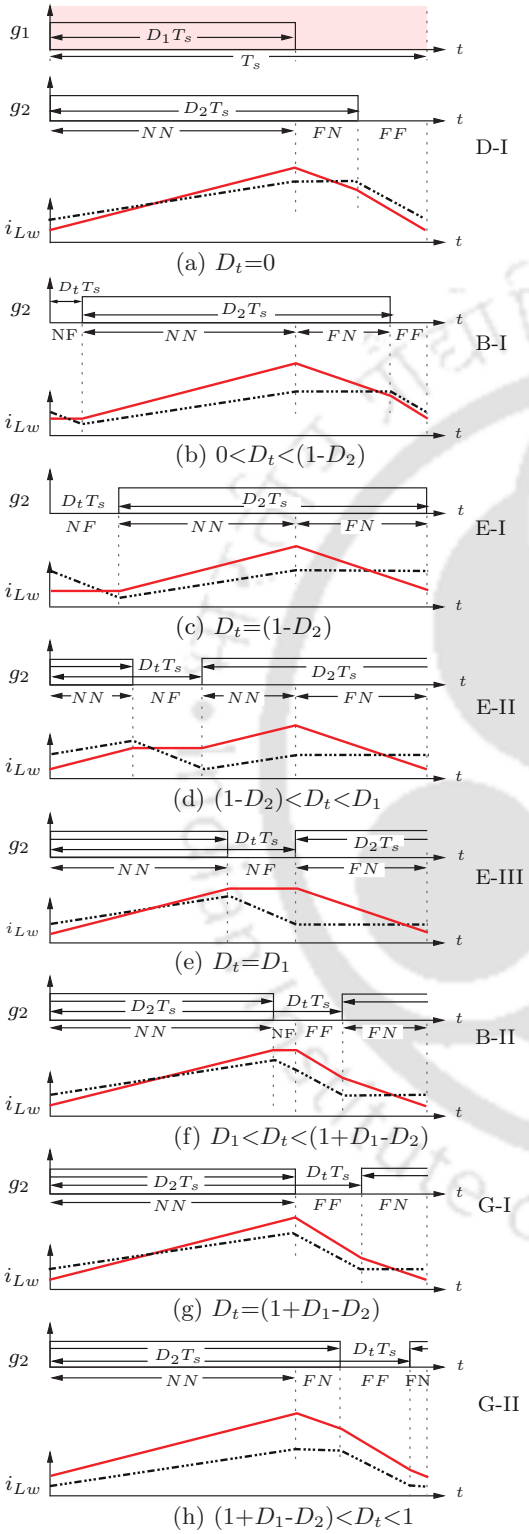


Figure A.11: Different sequences D-I, B-I,... and different patterns of i_{Lw} waveforms for (i) G_{NF_w} = 0, G_{FN_w} < 0 (red solid lines), (ii) G_{NF_w} < 0, G_{FN_w} = 0 (black dash-dotted lines) when (D_1 + D_2) > 1 and D_1 < D_2 (i.e. SR-5) as D_t varied from 0 to 1.

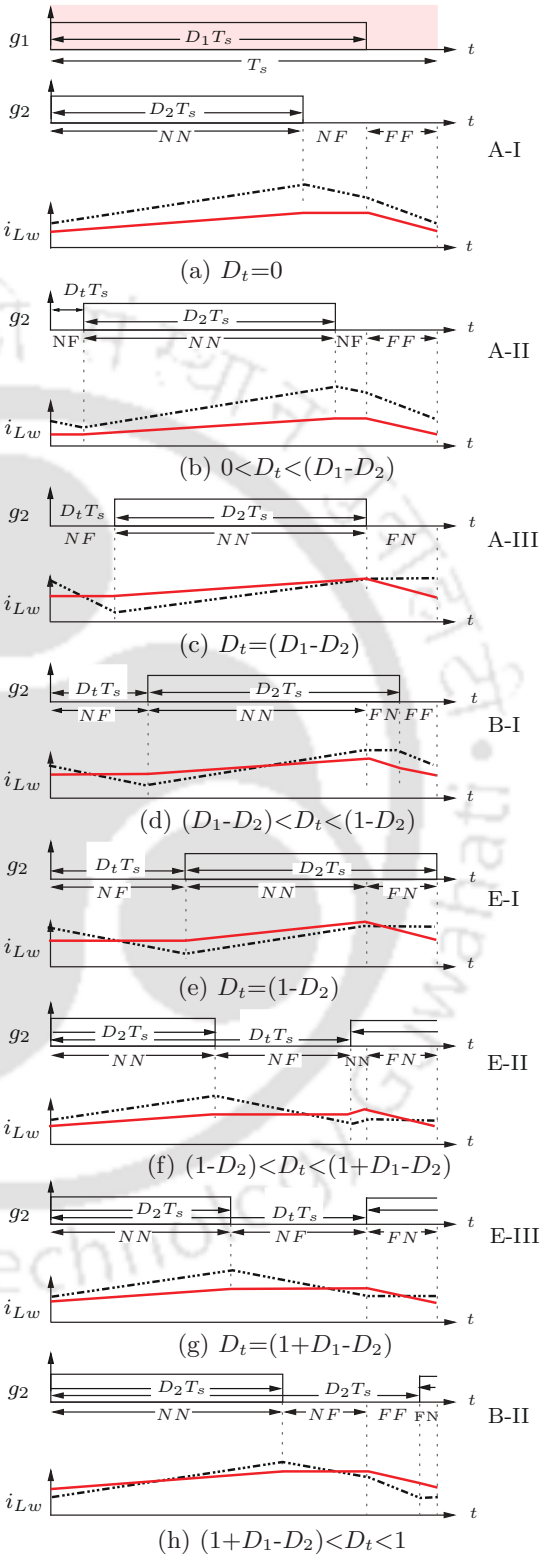


Figure A.12: Different sequences A-I, A-II,... and different patterns of i_{Lw} waveforms for (i) G_{NF_w} = 0, G_{FN_w} < 0 (red solid lines), (ii) G_{NF_w} < 0, G_{FN_w} = 0 (black dash-dotted lines) when (D_1 + D_2) > 1 and D_1 > D_2 (i.e. SR-4) as D_t varied from 0 to 1.

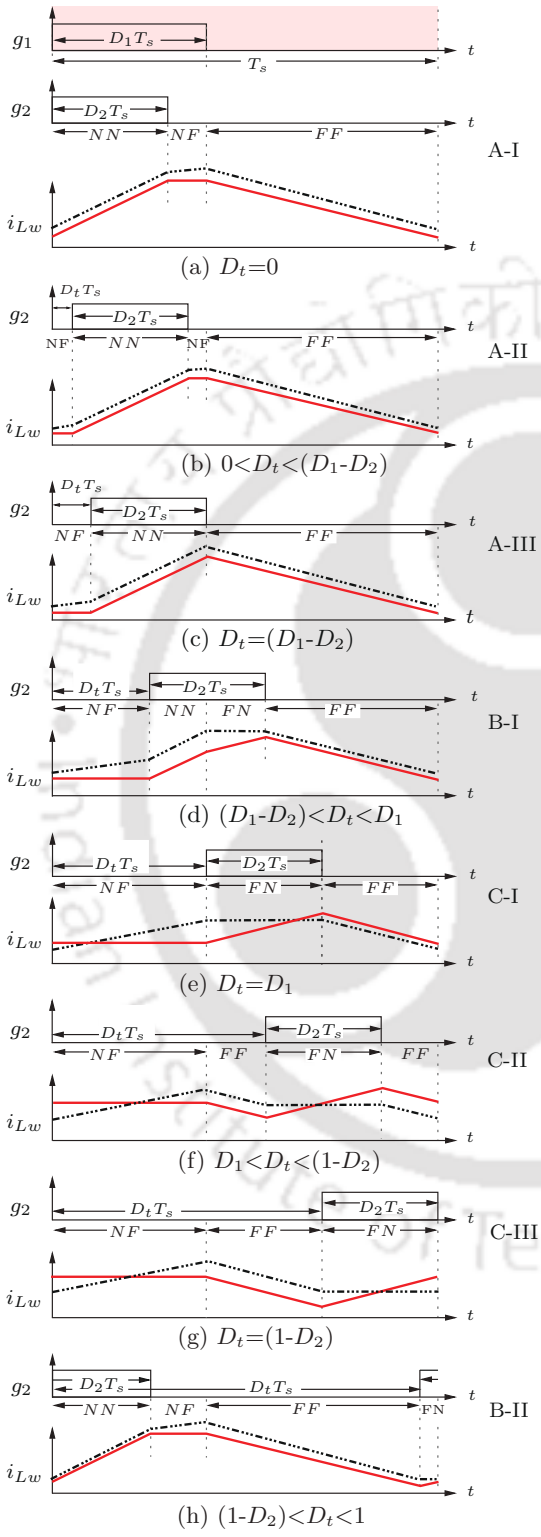


Figure A.13: Different sequences A-I, A-II,... and different patterns of i_{Lw} waveforms for (i) $G_{NF_w} > 0$, $G_{FN_w} = 0$ (red solid lines), (ii) $G_{NF_w} = 0$, $G_{FN_w} > 0$ (black dash-dotted lines) when $(D_1 + D_2) < 1$ and $D_1 > D_2$ (i.e. SR-1) as D_t varied from 0 to 1.

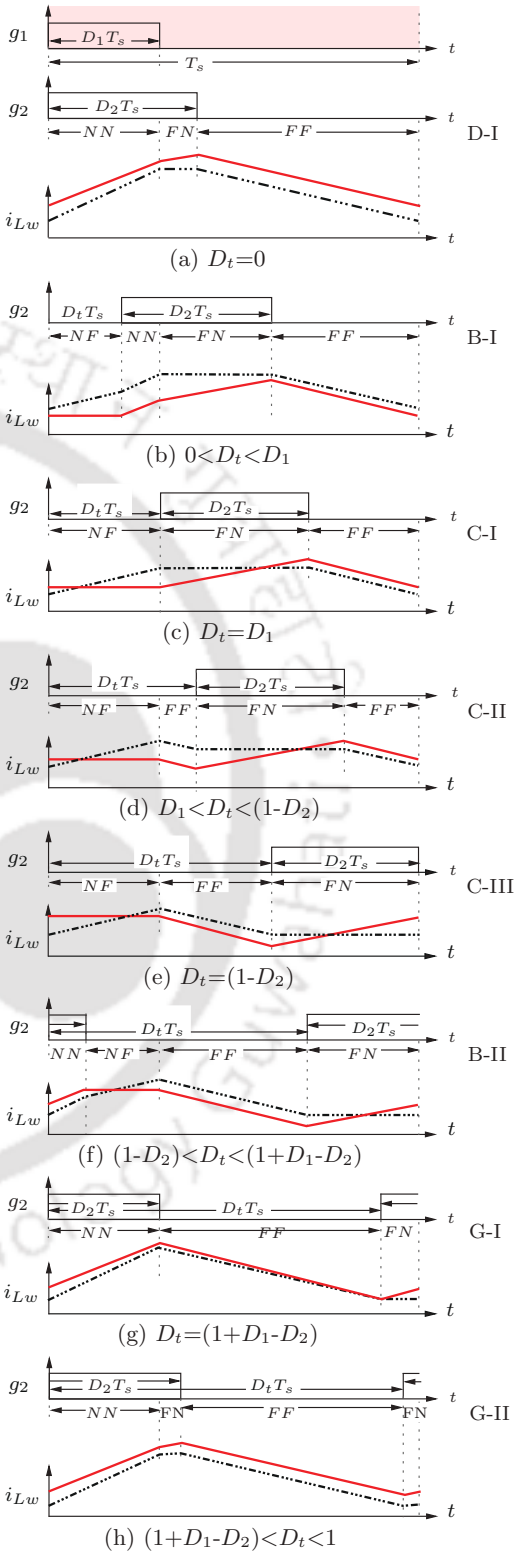


Figure A.14: Different sequences D-I, B-I,... and different patterns of i_{Lw} waveforms for (i) $G_{NF_w} = 0$, $G_{FN_w} > 0$ (red solid lines), (ii) $G_{NF_w} > 0$, $G_{FN_w} = 0$ (black dash-dotted lines) when $(D_1 + D_2) < 1$ and $D_1 < D_2$ (i.e. SR-5) as D_t varied from 0 to 1.

Table A.10: Δi_{Lw} in different sequences for $(D_1 + D_2) < 1$ and $D_1 > D_2$ (i.e. SR-1)

Seq.	Δi_{Lw}		D_t
	$G_{NF_w} = 0, G_{FN_w} > 0$	$G_{NF_w} > 0, G_{FN_w} = 0$	
A-I	α_{11}	α_1	0
A-II	α_{11}	α_1	$0 < D_t < (D_1 - D_2)$
A-III	α_{11}	α_1	$(D_1 - D_2)$
B-I	$\alpha_{11} > \Delta i_{Lw} > \beta_{12}$	$\alpha_1 > \Delta i_{Lw} > \beta_{11}$	$(D_1 - D_2) < D_t < D_1$
C-I	β_{12}	β_{11}	D_1
C-II	β_{12}	β_{11}	$D_1 < D_t < (1 - D_2)$
C-III	β_{12}	β_{11}	$(1 - D_2)$
B-II	$\beta_{12} < \Delta i_{Lw} < \alpha_{11}$	$\beta_{11} < \Delta i_{Lw} < \alpha_1$	$(1 - D_2) < D_t < 1$

$\alpha_1 \equiv G_{NN_w} D_2 T_s + G_{NF_w}(D_1 - D_2)T_s, \quad \alpha_{11} \equiv G_{NN_w} D_2 T_s$
$\beta_{11} \equiv G_{NF_w} D_1 T_s, \quad \beta_{12} \equiv G_{FN_w} D_2 T_s$

Table A.11: Δi_{Lw} in different sequences for $(D_1 + D_2) < 1$ and $D_1 < D_2$ (i.e. SR-2)

Seq.	Δi_{Lw}		D_t
	$G_{NF_w} = 0, G_{FN_w} > 0$	$G_{NF_w} > 0, G_{FN_w} = 0$	
D-I	α_2	α_{21}	0
B-I	$\alpha_2 > \Delta i_{Lw} > \beta_{22}$	$\alpha_{21} > \Delta i_{Lw} > \beta_{21}$	$0 < D_t < D_1$
C-I	β_{22}	β_{21}	D_1
C-II	β_{22}	β_{21}	D_1
C-III	β_{22}	β_{21}	$(1 - D_2)$
B-II	$\beta_{22} < \Delta i_{Lw} < \alpha_2$	$\beta_{21} < \Delta i_{Lw} < \alpha_{21}$	$(1 - D_2) < D_t < (1 + D_1 - D_2)$
G-I	α_2	α_{21}	$(1 + D_1 - D_2)$
G-II	α_2	α_{21}	$(1 + D_1 - D_2) < D_t < 1$

$\alpha_2 \equiv G_{NN_w} D_1 T_s + G_{FN_w}(D_2 - D_1)T_s, \quad \alpha_{21} \equiv G_{NN_w} D_1 T_s$
$\beta_2 \equiv G_{NF_w} D_1 T_s + G_{FN_w} D_2 T_s, \quad \beta_{21} \equiv G_{NF_w} D_1 T_s, \quad \beta_{22} \equiv G_{FN_w} D_2 T_s$

Table A.12: Δi_{Lw} in different sequences for $(D_1 + D_2) < 1$ and $D_1 = D_2$ (i.e. SR-3)

Seq.	Δi_{Lw}		D_t
	$G_{NF_w} = 0, G_{FN_w} > 0$	$G_{NF_w} > 0, G_{FN_w} = 0$	
D-II	α_3	α_3	0
B-I	$\alpha_3 > \Delta i_{Lw} > \beta_{32}$	$\alpha_3 > \Delta i_{Lw} > \beta_{31}$	$0 < D_t < D_1$
C-I	β_{32}	β_{31}	D_1
C-II	β_{32}	β_{31}	$(1 - D_2)$
C-III	β_{32}	β_{31}	$(1 - D_2)$
B-II	$\beta_{32} < \Delta i_{Lw} < \alpha_3$	$\beta_{31} < \Delta i_{Lw} < \alpha_3$	$(1 - D_2) < D_t < 1$

$\alpha_3 \equiv G_{NN_w} D_1 T_s$
$\beta_{31} \equiv G_{NF_w} D_1 T_s, \quad \beta_{32} \equiv G_{FN_w} D_2 T_s$
$\gamma_3 \equiv Max\{G_{NF_w} D_1 T_s, G_{FN_w} D_2 T_s\}$

Table A.13: Δi_{Lw} in different sequences for $(D_1 + D_2) > 1$ and $D_1 > D_2$ (i.e. SR-4)

Seq.	Δi_{Lw}		D_t
	$G_{NF_w} = 0, G_{FN_w} < 0$	$G_{NF_w} < 0, G_{FN_w} = 0$	
A-I	α_4	α_4	0
A-II	α_4	α_4	$0 < D_t < (D_1 - D_2)$
A-III	α_4	α_4	$(D_1 - D_2)$
B-I	$\alpha_4 > \Delta i_{Lw} > \beta_{41}$	$\alpha_4 > \Delta i_{Lw} > \zeta_4$	$(D_1 - D_2) < D_t < (1 - D_2)$
E-I	β_4	ζ_4	$(1 - D_2)$
E-II	β_{41}	ζ_4	D_1
E-III	β_{41}	ζ_4	D_1
B-II	β_{41}	$\zeta_4 < \Delta i_{Lw} < \alpha_4$	$D_1 < D_t < 1$

$\alpha_4 \equiv G_{NN_w} D_2 T_s$
$\beta_{41} \equiv G_{NN_w}(D_1 + D_2 - 1)T_s$
$\zeta_4 \equiv G_{NN_w}(D_1 + D_2 - 1)T_s$

Table A.14: Δi_{Lw} in different sequences for $(D_1 + D_2) > 1$ and $D_1 < D_2$ (i.e. SR-5)

Seq.	Δi_{Lw}		D_t
	$G_{NF_w} = 0, G_{FN_w} < 0$	$G_{NF_w} < 0, G_{FN_w} = 0$	
D-I	α_{51}	α_{51}	0
B-I	$\alpha_{51} > \Delta i_{Lw} > \beta_{51}$	$\alpha_{51} > \Delta i_{Lw} > \zeta_5$	$0 < D_t < (1 - D_2)$
E-I	β_{51}	β_{51}	$(1 - D_2)$
E-II	β_{51}	β_{51}	$(1 - D_2)$
E-III	β_{51}	β_{51}	D_1
B-II	$\beta_{51} < \Delta i_{Lw} < \alpha_{51}$	$\beta_{51} < \Delta i_{Lw} < \alpha_{51}$	$D_1 < D_t < (1 + D_1 - D_2)$
G-I	α_{51}	α_{51}	$(1 + D_1 - D_2)$
G-II	α_{51}	α_{51}	$(1 + D_1 - D_2) < D_t < 1$

$\alpha_{51} \equiv G_{NN_w} D_1 T_s$
$\beta_{51} \equiv G_{NN_w}(D_1 + D_2 - 1)T_s$

Table A.15: Δi_{Lw} in different sequences for $(D_1 + D_2) > 1$ and $D_1 = D_2$ (i.e. SR-6)

Seq.	Δi_{Lw}		D_t
	$G_{NF_w} = 0, G_{FN_w} < 0$	$G_{NF_w} < 0, G_{FN_w} = 0$	
D-II	α_{61}	α_{61}	0
B-I	$\alpha_{61} > \Delta i_{Lw} > \beta_{61}$	$\alpha_{61} > \Delta i_{Lw} > \zeta_6$	$0 < D_t < (1 - D_2)$
E-I	β_{61}	β_{61}	$(1 - D_2)$
E-II	β_{61}	β_{61}	D_1
E-III	β_{61}	β_{61}	D_1
B-II	$\beta_{61} < \Delta i_{Lw} < \alpha_{61}$	$\beta_{61} < \Delta i_{Lw} < \alpha_{61}$	$D_1 < D_t < 1$

$\alpha_{61} \equiv G_{NN_w} D_1 T_s$
$\beta_{61} \equiv G_{NN_w}(D_1 + D_2 - 1)T_s$

A.2 Variations of Δi_{Lw} Within Sequences C-II and E-II

The analysis of ripple Δi_{Lw} show that, in most of the sequences for different slope conditions, Δi_{Lw} either only increases or only decreases or remains constant. However, in sequences C-II and E-II, it is observed that Δi_{Lw} first decreases, then remains constant for some range and then increases. So, sub-ranges of sequences C-II and E-II are explored here.

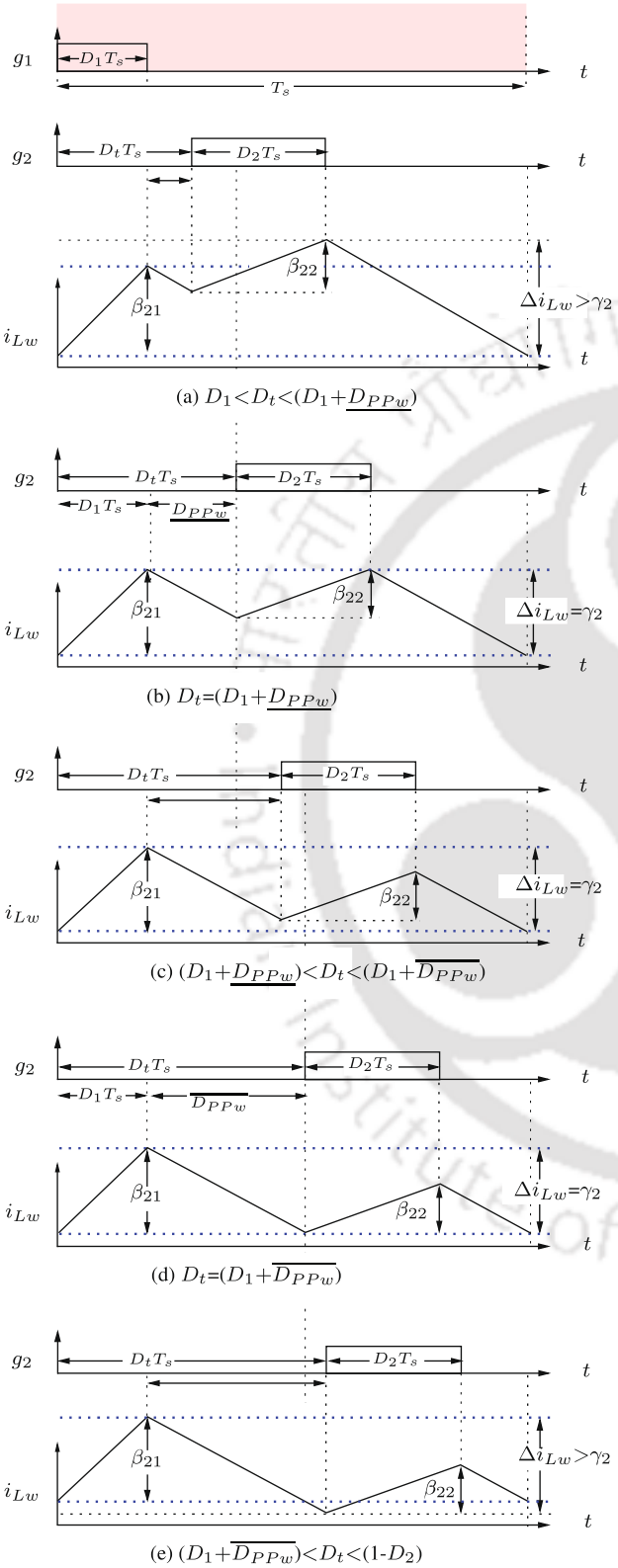


Figure A.15: Variation of Δi_{Lw} in sub-ranges of $D_1 < D_t < (1 - D_2)$ i.e. sequence C-II, for $G_{NF_w} > 0$, $G_{FN_w} > 0$ when $(D_1+D_2) < 1$ (Table A.2 of Appendix A).

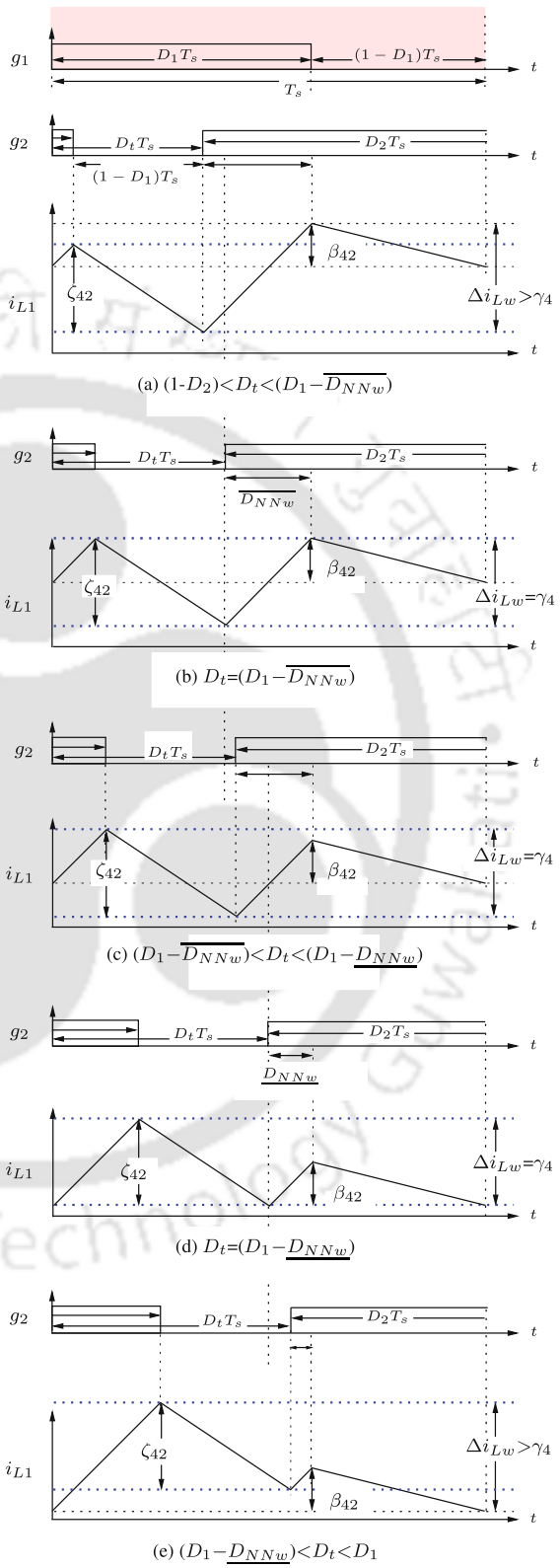


Figure A.16: Variation of Δi_{Lw} in sub-ranges of $(1 - D_2) < D_t < D_1$ i.e. sequence E-II, for $G_{NF_w} < 0$, $G_{FN_w} < 0$ when $(D_1+D_2) > 1$ (Table A.5 of Appendix A).

B

Input Current Ripple Minimization

B.1 Calculation of D_{min} for i_{in} as D_t varies from 0 to 1

This appendix presents different waveforms of i_{L1}, i_{L2} and i_{in} as D_t is varied from 0 to 1, for all the 16 sectors. The waveforms are shown for all possible D_1 and D_2 values. The section also shows the ripple expressions of i_{L1}, i_{L2} and i_{in} as D_t is varied from 0 to 1, in Table B.1 to Table B.16.

Table B.1: Sector 1 for $D_1 + D_2 < 1$ and $D_1 > D_2$.

Fig. No.	Δi_{L1} ($G_{NF1} > 0, G_{FN1} > 0$)	Δi_{L2} ($G_{NF2} > 0, G_{FN2} > 0$)	Δi_{in} ($G_{NFin} > 0, G_{FNin} > 0$)	D_t
(a)	α_{11}	α_{12}	α_{1in}	0
(b)	α_{11}	α_{12}	α_{1in}	$0 < D_t < (D_1 - D_2)$
(c)	α_{11}	α_{12}	α_{1in}	$(D_1 - D_2)$
(d)	$\alpha_{11} > \Delta i_{L1} > \beta_{11}$	$\alpha_{12} > \Delta i_{L2} > \beta_{12}$	$\alpha_{1in} > \Delta i_{in} > \beta_{1in}$	$(D_1 - D_2) < D_t < D_1$
(e)	β_{11}	β_{12}	β_{1in}	D_1
(f)	$\beta_{11} > \Delta i_{L1} > \gamma_{11}$ γ_{11} $\gamma_{11} < \Delta i_{L1} < \beta_{11}$	$\beta_{12} > \Delta i_{L2} > \gamma_{12}$ γ_{12} $\gamma_{12} < \Delta i_{L2} < \beta_{12}$	$\beta_{1in} > \Delta i_{in} > \gamma_{1in}$ γ_{1in} $\gamma_{1in} < \Delta i_{in} < \beta_{1in}$	$D_1 < D_t < (D_1 + \underline{D_{PPin}})$ $(D_1 + \underline{D_{PPin}}) \le D_t \le (D_1 + \overline{D_{PPin}})$ $(D_1 + \overline{D_{PPin}}) < D_t < (1 - D_2)$
(g)	β_{11}	β_{12}	β_{1in}	$(1 - D_2)$
(h)	$\beta_{11} < \Delta i_{L1} < \alpha_{11}$	$\beta_{12} < \Delta i_{L2} < \alpha_{12}$	$\beta_{1in} < \Delta i_{in} < \alpha_{1in}$	$(1 - D_2) < D_t < 1$

$\alpha_{11} \equiv G_{NN1}D_2T_s + G_{NF1}(D_1 - D_2)T_s$, $\alpha_{12} \equiv G_{NN2}D_2T_s + G_{NF2}(D_1 - D_2)T_s$, $\alpha_{1in} \equiv G_{NNin}D_2T_s + G_{NFin}(D_1 - D_2)T_s$
$\beta_{11} \equiv G_{NF1}D_1T_s + G_{FN1}D_2T_s$, $\beta_{12} \equiv G_{NF2}D_1T_s + G_{FN2}D_2T_s$, $\beta_{1in} \equiv G_{NFin}D_1T_s + G_{FNin}D_2T_s$
$\gamma_{11} \equiv Max\{G_{NF1}D_1T_s, G_{FN1}D_2T_s\}$, $\gamma_{12} \equiv Max\{G_{NF2}D_1T_s, G_{FN2}D_2T_s\}$, $\gamma_{1in} \equiv Max\{G_{NFin}D_1T_s, G_{FNin}D_2T_s\}$

Table B.2: Sector 2A for $D_1 + D_2 < 1$ and $D_1 > D_2$.

Fig. No.	Δi_{L1} ($G_{NF1} > 0, G_{FN1} < 0$)	Δi_{L2} ($G_{NF2} > 0, G_{FN2} > 0$)	Δi_{in} ($G_{NFin} > 0, G_{FNin} > 0$)	D_t
(a)	α_{11}	α_{12}	α_{1in}	0
(b)	α_{11}	α_{12}	α_{1in}	$0 < D_t < (D_1 - D_2)$
(c)	α_{11}	α_{12}	α_{1in}	$(D_1 - D_2)$
(d)	$\alpha_{11} > \Delta i_{L1} > \rho_{11}$	$\alpha_{12} > \Delta i_{L2} > \beta_{12}$	$\alpha_{1in} > \Delta i_{in} > \beta_{1in}$	$(D_1 - D_2) < D_t < D_1$
(e)	ρ_{11}	β_{12}	β_{1in}	D_1
(f)	ρ_{11} ρ_{11} ρ_{11}	$\beta_{12} > \Delta i_{L2} > \gamma_{12}$ γ_{12} $\gamma_{12} < \Delta i_{L2} < \beta_{12}$	$\beta_{1in} > \Delta i_{in} > \gamma_{1in}$ γ_{1in} $\gamma_{1in} < \Delta i_{in} < \beta_{1in}$	$D_1 < D_t < (D_1 + \underline{D_{PPin}})$ $(D_1 + \underline{D_{PPin}}) \le D_t \le (D_1 + \overline{D_{PPin}})$ $(D_1 + \overline{D_{PPin}}) < D_t < (1 - D_2)$
(g)	ρ_{11}	β_{12}	β_{1in}	$(1 - D_2)$
(h)	$\rho_{11} < \Delta i_{L1} < \alpha_{11}$	$\beta_{12} < \Delta i_{L2} < \alpha_{12}$	$\beta_{1in} < \Delta i_{in} < \alpha_{1in}$	$(1 - D_2) < D_t < 1$

$\alpha_{11} \equiv G_{NN1}D_2T_s + G_{NF1}(D_1 - D_2)T_s$, $\alpha_{12} \equiv G_{NN2}D_2T_s + G_{NF2}(D_1 - D_2)T_s$, $\alpha_{1in} \equiv G_{NNin}D_2T_s + G_{NFin}(D_1 - D_2)T_s$
$\rho_{11} \equiv G_{NF1}D_1T_s$, $\beta_{12} \equiv G_{NF2}D_1T_s + G_{FN2}D_2T_s$, $\beta_{1in} \equiv G_{NFin}D_1T_s + G_{FNin}D_2T_s$
$\gamma_{12} \equiv Max\{G_{NF2}D_1T_s, G_{FN2}D_2T_s\}$, $\gamma_{1in} \equiv Max\{G_{NFin}D_1T_s, G_{FNin}D_2T_s\}$

Table B.3: Sector 2B for $D_1 + D_2 < 1$ and $D_1 > D_2$.

Fig. No.	Δi_{L1} $G_{NF1}>0, G_{FN1}<0$	Δi_{L2} $G_{NF2}>0, G_{FN2}>0$	Δi_{in} $G_{NFin}>0, G_{FNin}<0$	D_t
(a)	α_{11}	α_{12}	α_{1in}	0
(b)	α_{11}	α_{12}	α_{1in}	$0 < D_t < (D_1 - D_2)$
(c)	α_{11}	α_{12}	α_{1in}	$(D_1 - D_2)$
(d)	$\alpha_{11} > \Delta i_{L1} > \rho_{11}$	$\alpha_{12} > \Delta i_{L2} > \beta_{12}$	$\alpha_{1in} > \Delta i_{in} > \rho_{1in}$	$(D_1 - D_2) < D_t < D_1$
(e)	ρ_{11}	β_{12}	ρ_{1in}	D_1
(f)	ρ_{11}	$\beta_{12} > \Delta i_{L2} > \gamma_{12}$	ρ_{1in}	$D_1 < D_t < (D_1 + \underline{D_{PP2}})$
	ρ_{11}	γ_{12}	ρ_{1in}	$(D_1 + \underline{D_{PP2}}) \le D_t \le (D_1 + \overline{D_{PP2}})$
	ρ_{11}	$\gamma_{12} < \Delta i_{L2} < \beta_{12}$	ρ_{1in}	$(D_1 + \overline{D_{PP2}}) < D_t < (1 - D_2)$
(g)	ρ_{11}	β_{12}	ρ_{1in}	$(1 - D_2)$
(h)	$\rho_{11} < \Delta i_{L1} < \alpha_{11}$	$\beta_{12} < \Delta i_{L2} < \alpha_{12}$	$\rho_{1in} < \Delta i_{in} < \alpha_{1in}$	$(1 - D_2) < D_t < 1$

$\alpha_{11} \equiv G_{NN1}D_2T_s + G_{NF1}(D_1 - D_2)T_s$, $\alpha_{12} \equiv G_{NN2}D_2T_s + G_{NF2}(D_1 - D_2)T_s$, $\alpha_{1in} \equiv G_{NNin}D_2T_s + G_{NFin}(D_1 - D_2)T_s$
$\rho_{11} \equiv G_{NF1}D_1T_s$, $\beta_{12} \equiv G_{NF2}D_1T_s + G_{FN2}D_2T_s$, $\rho_{1in} \equiv G_{NFin}D_1T_s$
$\gamma_{12} \equiv Max\{G_{NF2}D_1T_s, G_{FN2}D_2T_s\}$

Table B.4: Sector 3 for $D_1 + D_2 < 1$ and $D_1 > D_2$.

Fig. No.	Δi_{L1} $G_{NF1}>0, G_{FN1}<0$	Δi_{L2} $G_{NF2}>0, G_{FN2}<0$	Δi_{in} $G_{NFin}>0, G_{FNin}<0$	D_t
(a)	α_{11}	α_{12}	α_{1in}	0
(b)	α_{11}	α_{12}	α_{1in}	$0 < D_t < (D_1 - D_2)$
(c)	α_{11}	α_{12}	α_{1in}	$(D_1 - D_2)$
(d)	$\alpha_{11} > \Delta i_{L1} > \rho_{11}$	$\alpha_{12} > \Delta i_{L2} > \rho_{12}$	$\alpha_{1in} > \Delta i_{in} > \rho_{1in}$	$(D_1 - D_2) < D_t < D_1$
(e)	ρ_{11}	ρ_{12}	ρ_{1in}	D_1
(f)	ρ_{11}	ρ_{12}	ρ_{1in}	$D_1 < D_t < (1 - D_2)$
(g)	ρ_{11}	ρ_{12}	ρ_{1in}	$(1 - D_2)$
(h)	$\rho_{11} < \Delta i_{L1} < \alpha_{11}$	$\rho_{12} < \Delta i_{L2} < \alpha_{12}$	$\rho_{1in} < \Delta i_{in} < \alpha_{1in}$	$(1 - D_2) < D_t < 1$

$\alpha_{11} \equiv G_{NN1}D_2T_s + G_{NF1}(D_1 - D_2)T_s$, $\alpha_{12} \equiv G_{NN2}D_2T_s + G_{NF2}(D_1 - D_2)T_s$, $\alpha_{1in} \equiv G_{NNin}D_2T_s + G_{NFin}(D_1 - D_2)T_s$
$\rho_{11} \equiv G_{NF1}D_1T_s$, $\rho_{12} \equiv G_{NF2}D_1T_s$, $\rho_{1in} \equiv G_{NFin}D_1T_s$

Table B.5: Sector 4A for $D_1 + D_2 < 1$ and $D_1 > D_2$.

Fig. No.	Δi_{L1} $G_{NF1}>0, G_{FN1}>0$	Δi_{L2} $G_{NF2}<0, G_{FN2}>0$	Δi_{in} $G_{NFin}>0, G_{FNin}>0$	D_t
(a)	α_{11}	ϵ_{12}	α_{1in}	0
(b)	α_{11}	ϵ_{12}	α_{1in}	$0 < D_t < (D_1 - D_2)$
(c)	α_{11}	ϵ_{12}	α_{1in}	$(D_1 - D_2)$
(d)	$\alpha_{11} > \Delta i_{L1} > \rho_{11}$	$\epsilon_{12} > \Delta i_{L2} > \tau_{12}$	$\alpha_{1in} > \Delta i_{in} > \beta_{1in}$	$(D_1 - D_2) < D_t < D_1$
(e)	β_{11}	τ_{12}	β_{1in}	D_1
(f)	$\beta_{11} > \Delta i_{L1} > \gamma_{11}$	τ_{12}	$\beta_{1in} > \Delta i_{in} > \gamma_{1in}$	$D_1 < D_t < (D_1 + \underline{D_{PPin}})$
	γ_{11}	τ_{12}	γ_{1in}	$(D_1 + \underline{D_{PPin}}) \le D_t \le (D_1 + \overline{D_{PPin}})$
	$\gamma_{11} < \Delta i_{L1} < \beta_{11}$	τ_{12}	$\gamma_{1in} < \Delta i_{in} < \beta_{1in}$	$(D_1 + \overline{D_{PPin}}) < D_t < (1 - D_2)$
(g)	β_{11}	τ_{12}	β_{1in}	$(1 - D_2)$
(h)	$\beta_{11} < \Delta i_{L1} < \alpha_{11}$	$\tau_{12} < \Delta i_{L2} < \alpha_{12}$	$\beta_{1in} < \Delta i_{in} < \alpha_{1in}$	$(1 - D_2) < D_t < 1$

$\alpha_{11} \equiv G_{NN1}D_2T_s + G_{NF1}(D_1 - D_2)T_s$, $\epsilon_{12} \equiv G_{NN2}D_2T_s$, $\alpha_{1in} \equiv G_{NNin}D_2T_s + G_{NFin}(D_1 - D_2)T_s$
$\beta_{11} \equiv G_{NF1}D_1T_s + G_{FN1}D_2T_s$, $\tau_{12} \equiv G_{FN2}D_2T_s$, $\beta_{1in} \equiv G_{NFin}D_1T_s + G_{FNin}D_2T_s$
$\gamma_{11} \equiv Max\{G_{NF1}D_1T_s, G_{FN1}D_2T_s\}$, $\gamma_{1in} \equiv Max\{G_{NFin}D_1T_s, G_{FNin}D_2T_s\}$

Table B.6: Sector 4B for $D_1 + D_2 < 1$ and $D_1 > D_2$.

Fig. No.	Δi_{L1} ($G_{NF1} > 0, G_{FN1} > 0$)	Δi_{L2} ($G_{NF2} < 0, G_{FN2} > 0$)	Δi_{in} ($G_{NFin} < 0, G_{FNin} > 0$)	D_t
(a)	α_{11}	ϵ_{12}	ϵ_{1in}	0
(b)	α_{11}	ϵ_{12}	ϵ_{1in}	$0 < D_t < (D_1 - D_2)$
(c)	α_{11}	ϵ_{12}	ϵ_{1in}	$(D_1 - D_2)$
(d)	$\alpha_{11} > \Delta i_{L1} > \beta_{11}$	$\epsilon_{12} > \Delta i_{L2} > \tau_{12}$	$\epsilon_{1in} > \Delta i_{in} > \tau_{1in}$	$(D_1 - D_2) < D_t < D_1$
(e)	β_{11}	τ_{12}	τ_{1in}	D_1
(f)	$\beta_{11} > \Delta i_{L1} > \gamma_{11}$	τ_{12}	τ_{1in}	$D_1 < D_t < (D_1 + \underline{D_{PP1}})$
	γ_{11}	τ_{12}	τ_{1in}	$(D_1 + \underline{D_{PP1}}) \le D_t \le (D_1 + \overline{D_{PP1}})$
	$\gamma_{11} < \Delta i_{L1} < \beta_{11}$	τ_{12}	τ_{1in}	$(D_1 + \overline{D_{PP1}}) < D_t < (1 - D_2)$
(g)	β_{11}	τ_{12}	τ_{1in}	$(1 - D_2)$
(h)	$\beta_{11} < \Delta i_{L1} < \alpha_{11}$	$\tau_{12} < \Delta i_{L2} < \alpha_{12}$	$\tau_{1in} < \Delta i_{in} < \alpha_{1in}$	$(1 - D_2) < D_t < 1$

$\alpha_{11} \equiv G_{NN1}D_2T_s + G_{NF1}(D_1 - D_2)T_s$, $\epsilon_{12} \equiv G_{NN2}D_2T_s$, $\epsilon_{1in} \equiv G_{NNin}D_2T_s$
$\beta_{11} \equiv G_{NF1}D_1T_s + G_{FN1}D_2T_s$, $\tau_{12} \equiv G_{FN2}D_2T_s$, $\tau_{1in} \equiv G_{FNin}D_2T_s$
$\gamma_{11} \equiv Max\{G_{NF1}D_1T_s, G_{FN1}D_2T_s\}$

Table B.7: Sector 5A for $D_1 + D_2 < 1$ and $D_1 > D_2$.

Fig. No.	Δi_{L1} ($G_{NF1} > 0, G_{FN1} < 0$)	Δi_{L2} ($G_{NF2} < 0, G_{FN2} > 0$)	Δi_{in} ($G_{NFin} > 0, G_{FNin} > 0$)	D_t
(a)	α_{11}	ϵ_{12}	α_{1in}	0
(b)	α_{11}	ϵ_{12}	α_{1in}	$0 < D_t < (D_1 - D_2)$
(c)	α_{11}	ϵ_{12}	α_{1in}	$(D_1 - D_2)$
(d)	$\alpha_{11} > \Delta i_{L1} > \rho_{11}$	$\epsilon_{12} > \Delta i_{L2} > \tau_{12}$	$\alpha_{1in} > \Delta i_{in} > \beta_{1in}$	$(D_1 - D_2) < D_t < D_1$
(e)	ρ_{11}	τ_{12}	β_{1in}	D_1
(f)	ρ_{11}	τ_{12}	$\beta_{1in} > \Delta i_{in} > \gamma_{1in}$	$D_1 < D_t < (D_1 + \underline{D_{PPin}})$
	ρ_{11}	τ_{12}	γ_{1in}	$(D_1 + \underline{D_{PPin}}) \le D_t \le (D_1 + \overline{D_{PPin}})$
	ρ_{11}	τ_{12}	$\gamma_{1in} < \Delta i_{in} < \beta_{1in}$	$(D_1 + \overline{D_{PPin}}) < D_t < (1 - D_2)$
(g)	ρ_{11}	τ_{12}	β_{1in}	$(1 - D_2)$
(h)	$\rho_{11} < \Delta i_{L1} < \alpha_{11}$	$\tau_{12} < \Delta i_{L2} < \alpha_{12}$	$\beta_{1in} < \Delta i_{in} < \alpha_{1in}$	$(1 - D_2) < D_t < 1$

$\alpha_{11} \equiv G_{NN1}D_2T_s + G_{NF1}(D_1 - D_2)T_s$, $\epsilon_{12} \equiv G_{NN2}D_2T_s$, $\alpha_{1in} \equiv G_{NNin}D_2T_s + G_{NFin}(D_1 - D_2)T_s$
$\rho_{11} \equiv G_{NF1}D_1T_s$, $\tau_{12} \equiv G_{FN2}D_2T_s$, $\beta_{1in} \equiv G_{NFin}D_1T_s + G_{FNin}D_2T_s$
$\gamma_{1in} \equiv Max\{G_{NFin}D_1T_s, G_{FNin}D_2T_s\}$

Table B.8: Sector 5B for $D_1 + D_2 < 1$ and $D_1 > D_2$.

Fig. No.	Δi_{L1} ($G_{NF1} > 0, G_{FN1} < 0$)	Δi_{L2} ($G_{NF2} < 0, G_{FN2} > 0$)	Δi_{in} ($G_{NFin} > 0, G_{FNin} < 0$)	D_t
(a)	α_{11}	ϵ_{12}	α_{1in}	0
(b)	α_{11}	ϵ_{12}	α_{1in}	$0 < D_t < (D_1 - D_2)$
(c)	α_{11}	ϵ_{12}	α_{1in}	$(D_1 - D_2)$
(d)	$\alpha_{11} > \Delta i_{L1} > \rho_{11}$	$\epsilon_{12} > \Delta i_{L2} > \tau_{12}$	$\alpha_{1in} > \Delta i_{in} > \rho_{1in}$	$(D_1 - D_2) < D_t < D_1$
(e)	ρ_{11}	τ_{12}	ρ_{1in}	D_1
(f)	ρ_{11}	τ_{12}	ρ_{1in}	$D_1 < D_t < (1 - D_2)$
(g)	ρ_{11}	τ_{12}	ρ_{1in}	$(1 - D_2)$
(h)	$\rho_{11} < \Delta i_{L1} < \alpha_{11}$	$\tau_{12} < \Delta i_{L2} < \alpha_{12}$	$\rho_{1in} < \Delta i_{in} < \alpha_{1in}$	$(1 - D_2) < D_t < 1$

$\alpha_{11} \equiv G_{NN1}D_2T_s + G_{NF1}(D_1 - D_2)T_s$, $\epsilon_{12} \equiv G_{NN2}D_2T_s$, $\alpha_{1in} \equiv G_{NNin}D_2T_s + G_{NFin}(D_1 - D_2)T_s$
$\rho_{11} \equiv G_{NF1}D_1T_s$, $\tau_{12} \equiv G_{FN2}D_2T_s$, $\rho_{1in} \equiv G_{NFin}D_1T_s$

Table B.9: Sector 5C for $D_1 + D_2 < 1$ and $D_1 > D_2$.

Fig. No.	Δi_{L1} $G_{NF1}>0, G_{FN1}<0$	Δi_{L2} $G_{NF2}<0, G_{FN2}>0$	Δi_{in} $G_{NFin}<0, G_{FNin}>0$	D_t
(a)	α_{11}	ϵ_{12}	ϵ_{1in}	0
(b)	α_{11}	ϵ_{12}	ϵ_{1in}	$0 < D_t < (D_1 - D_2)$
(c)	α_{11}	ϵ_{12}	ϵ_{1in}	$(D_1 - D_2)$
(d)	$\alpha_{11} > \Delta i_{L1} > \rho_{11}$	$\epsilon_{12} > \Delta i_{L2} > \tau_{12}$	$\epsilon_{1in} > \Delta i_{in} > \tau_{1in}$	$(D_1 - D_2) < D_t < D_1$
(e)	ρ_{11}	τ_{12}	τ_{1in}	D_1
(f)	ρ_{11}	τ_{12}	τ_{1in}	$D_1 < D_t < (1 - D_2)$
(g)	ρ_{11}	τ_{12}	τ_{1in}	$(1 - D_2)$
(h)	$\rho_{11} < \Delta i_{L1} < \alpha_{11}$	$\tau_{12} < \Delta i_{L2} < \alpha_{12}$	$\tau_{1in} < \Delta i_{in} < \alpha_{1in}$	$(1 - D_2) < D_t < 1$

$\alpha_{11} \equiv G_{NN1}D_2T_s + G_{NF1}(D_1 - D_2)T_s$, $\epsilon_{12} \equiv G_{NN2}D_2T_s$, $\epsilon_{1in} \equiv G_{NNin}D_2T_s$
$\rho_{11} \equiv G_{NF1}D_1T_s$, $\tau_{12} \equiv G_{FN2}D_2T_s$, $\tau_{1in} \equiv G_{FNin}D_2T_s$

Table B.10: Sector 5D for $D_1 + D_2 > 1$ and $D_1 < D_2$.

Fig. No.	Δi_{L1} $G_{NF1}>0, G_{FN1}<0$	Δi_{L2} $G_{NF2}<0, G_{FN2}>0$	Δi_{in} $G_{NFin}<0, G_{FNin}<0$	D_t
(a)	ν_{11}	σ_{12}	ν_{1in}	0
(b)	$\nu_{11} > \Delta i_{L1} > \eta_{11}$	$\sigma_{12} > \Delta i_{L2} > \zeta_{12}$	$\nu_{1in} > \Delta i_{in} > \upsilon_{1in}$	$0 < D_t < (1 - D_2)$
(c)	η_{11}	ζ_{12}	υ_{1in}	$(1 - D_2)$
(d)	η_{11}	ζ_{12}	$\upsilon_{1in} > \Delta i_{in} > \chi_{1in}$	$(1 - D_2) < D_t < (D_1 - \overline{D_{NNin}})$
	η_{11}	ζ_{12}	χ_{1in}	$(D_1 - \overline{D_{NNin}}) \le D_t \le (D_1 - \underline{D_{NNin}})$
	η_{11}	ζ_{12}	$\chi_{1in} < \Delta i_{in} < \upsilon_{1in}$	$(D_1 - \underline{D_{NNin}}) < D_t < D_1$
(e)	η_{11}	ζ_{12}	υ_{1in}	D_1
(f)	$\eta_{11} < \Delta i_{L1} < \nu_{11}$	$\zeta_{12} < \Delta i_{L2} < \sigma_{12}$	$\upsilon_{1in} < \Delta i_{in} < \nu_{1in}$	$D_1 < D_t < (1 + D_1 - D_2)$
(g)	ν_{11}	σ_{12}	ν_{1in}	$(1 + D_1 - D_2)$
(h)	ν_{11}	σ_{12}	ν_{1in}	$(1 + D_1 - D_2) < D_t < 1$

$\nu_{11} \equiv G_{NN1}D_1T_s$, $\nu_{1in} \equiv G_{NNin}D_1T_s$
$\upsilon_{1in} \equiv G_{NNin}(D_1 + D_2 - 1)T_s$
$\chi_{1in} \equiv Max\{|G_{NFin}|(1 - D_2)T_s, |G_{FNin}|(1 - D_1)T_s\}$
$\zeta_{12} \equiv G_{NN2}(D_1 + D_2 - 1)T_s + G_{FN2}(1 - D_1)T_s$
$\eta_{11} \equiv G_{NN1}(D_1 + D_2 - 1)T_s + G_{NF1}(1 - D_2)T_s$
$\sigma_{12} \equiv G_{NN2}D_1T_s + G_{FN2}(D_2 - D_1)T_s$

Table B.11: Sector 6A for $D_1 + D_2 > 1$ and $D_1 < D_2$.

Fig. No.	Δi_{L1} $G_{NF1}>0, G_{FN1}<0$	Δi_{L2} $G_{NF2}<0, G_{FN2}<0$	Δi_{in} $G_{NFin}<0, G_{FNin}<0$	D_t
(a)	ν_{11}	ν_{12}	ν_{1in}	0
(b)	$\nu_{11} > \Delta i_{L1} > \eta_{11}$	$\nu_{12} > \Delta i_{L2} > \upsilon_{12}$	$\nu_{1in} > \Delta i_{in} > \upsilon_{1in}$	$0 < D_t < (1 - D_2)$
(c)	η_{11}	υ_{12}	υ_{1in}	$(1 - D_2)$
(d)	η_{11}	$\upsilon_{12} > \Delta i_{L2} > \chi_{12}$	$\upsilon_{1in} > \Delta i_{in} > \chi_{1in}$	$(1 - D_2) < D_t < (D_1 - \overline{D_{NNin}})$
	η_{11}	χ_{12}	χ_{1in}	$(D_1 - \overline{D_{NNin}}) \le D_t \le (D_1 - \underline{D_{NNin}})$
	η_{11}	$\chi_{12} < \Delta i_{L2} < \upsilon_{12}$	$\chi_{1in} < \Delta i_{in} < \upsilon_{1in}$	$(D_1 - \underline{D_{NNin}}) < D_t < D_1$
(e)	η_{11}	υ_{12}	υ_{1in}	D_1
(f)	$\eta_{11} < \Delta i_{L1} < \nu_{11}$	$\upsilon_{12} < \Delta i_{L2} < \nu_{12}$	$\upsilon_{1in} < \Delta i_{in} < \nu_{1in}$	$D_1 < D_t < (1 + D_1 - D_2)$
(g)	ν_{11}	ν_{12}	ν_{1in}	$(1 + D_1 - D_2)$
(h)	ν_{11}	ν_{12}	ν_{1in}	$(1 + D_1 - D_2) < D_t < 1$

$\nu_{11} \equiv G_{NN1}D_1T_s$, $\nu_{12} \equiv G_{NN2}D_1T_s$, $\nu_{1in} \equiv G_{NNin}D_1T_s$
$\upsilon_{12} \equiv G_{NN2}(D_1 + D_2 - 1)T_s$, $\upsilon_{1in} \equiv G_{NNin}(D_1 + D_2 - 1)T_s$
$\chi_{12} \equiv Max\{|G_{NF2}|(1 - D_2)T_s, |G_{FN2}|(1 - D_1)T_s\}$, $\chi_{1in} \equiv Max\{|G_{NFin}|(1 - D_2)T_s, |G_{FNin}|(1 - D_1)T_s\}$
$\eta_{11} \equiv G_{NN1}(D_1 + D_2 - 1)T_s + G_{NF1}(1 - D_2)T_s$

Table B.12: Sector 6B for $D_1 + D_2 > 1$ and $D_1 < D_2$.

Fig. No.	Δi_{L1} ($G_{NF1} > 0, G_{FN1} < 0$)	Δi_{L2} ($G_{NF2} < 0, G_{FN2} < 0$)	Δi_{in} ($G_{NFin} > 0, G_{FNin} < 0$)	D_t
(a)	ν_{11}	ν_{12}	ν_{1in}	0
(b)	$\nu_{11} > \Delta i_{L1} > \eta_{11}$	$\nu_{12} > \Delta i_{L2} > \upsilon_{12}$	$\nu_{1in} > \Delta i_{in} > \eta_{1in}$	$0 < D_t < (1 - D_2)$
(c)	η_{11}	υ_{12}	η_{1in}	$(1 - D_2)$
(d)	η_{11}	$\upsilon_{12} > \Delta i_{L2} > \chi_{12}$	η_{1in}	$(1 - D_2) < D_t < (D_1 - \overline{D_{NN2}})$
	η_{11}	χ_{12}	η_{1in}	$(D_1 - \overline{D_{NN2}}) \leq D_t \leq (D_1 - \underline{D_{NN2}})$
	η_{11}	$\chi_{12} < \Delta i_{L2} < \upsilon_{12}$	η_{1in}	$(D_1 - \underline{D_{NN2}}) < D_t < D_1$
(e)	η_{11}	υ_{12}	η_{1in}	D_1
(f)	$\eta_{11} < \Delta i_{L1} < \nu_{11}$	$\upsilon_{12} < \Delta i_{L2} < \nu_{12}$	$\eta_{1in} < \Delta i_{in} < \nu_{1in}$	$D_1 < D_t < (1 + D_1 - D_2)$
(g)	ν_{11}	ν_{12}	ν_{1in}	$(1 + D_1 - D_2)$
(h)	ν_{11}	ν_{12}	ν_{1in}	$(1 + D_1 - D_2) < D_t < 1$

$\nu_{11} \equiv G_{NN1} D_1 T_s, \quad \nu_{12} \equiv G_{NN2} D_1 T_s, \quad \nu_{1in} \equiv G_{NNin} D_1 T_s$
$\upsilon_{12} \equiv G_{NN2}(D_1 + D_2 - 1) T_s$
$\chi_{12} \equiv Max\{|G_{NF2}|(1 - D_2)T_s, |G_{FN2}|(1 - D_1)T_s\}$
$\eta_{11} \equiv G_{NN1}(D_1 + D_2 - 1)T_s + G_{NF1}(1 - D_2)T_s$, $\eta_{1in} \equiv G_{NNin}(D_1 + D_2 - 1)T_s + G_{NFin}(1 - D_2)T_s$

Table B.13: Sector 7 for $D_1 + D_2 < 1$ and $D_1 > D_2$.

Fig. No.	Δi_{L1} ($G_{NF1} < 0, G_{FN1} > 0$)	Δi_{L2} ($G_{NF2} < 0, G_{FN2} > 0$)	Δi_{in} ($G_{NFin} < 0, G_{FNin} > 0$)	D_t
(a)	ϵ_{11}	ϵ_{12}	ϵ_{1in}	0
(b)	ϵ_{11}	ϵ_{12}	ϵ_{1in}	$0 < D_t < (D_1 - D_2)$
(c)	ϵ_{11}	ϵ_{12}	ϵ_{1in}	$(D_1 - D_2)$
(d)	$\epsilon_{11} > \Delta i_{L1} > \tau_{11}$	$\epsilon_{12} > \Delta i_{L2} > \tau_{12}$	$\epsilon_{1in} > \Delta i_{in} > \tau_{1in}$	$(D_1 - D_2) < D_t < D_1$
(e)	τ_{11}	τ_{12}	τ_{1in}	D_1
(f)	τ_{11}	τ_{12}	τ_{1in}	$D_1 < D_t < (1 - D_2)$
(g)	τ_{11}	τ_{12}	τ_{1in}	$(1 - D_2)$
(h)	$\tau_{11} < \Delta i_{L1} < \epsilon_{11}$	$\tau_{12} < \Delta i_{L2} < \epsilon_{12}$	$\tau_{1in} < \Delta i_{in} < \epsilon_{1in}$	$(1 - D_2) < D_t < 1$

$\epsilon_{11} \equiv G_{NN1} D_2 T_s, \quad \epsilon_{12} \equiv G_{NN2} D_2 T_s$, $\epsilon_{1in} \equiv G_{NNin} D_2 T_s$
$\tau_{11} \equiv G_{FN1} D_2 T_s, \quad \tau_{12} \equiv G_{FN2} D_2 T_s, \quad \tau_{1in} \equiv G_{FNin} D_2 T_s$

Table B.14: Sector 8A for $D_1 + D_2 > 1$ and $D_1 < D_2$.

Fig. No.	Δi_{L1} ($G_{NF1} < 0, G_{FN1} < 0$)	Δi_{L2} ($G_{NF2} < 0, G_{FN2} > 0$)	Δi_{in} ($G_{NFin} < 0, G_{FNin} < 0$)	D_t
(a)	ν_{11}	σ_{12}	ν_{1in}	0
(b)	$\nu_{11} > \Delta i_{L1} > \upsilon_{11}$	$\sigma_{12} > \Delta i_{L2} > \zeta_{12}$	$\nu_{1in} > \Delta i_{in} > \upsilon_{1in}$	$0 < D_t < (1 - D_2)$
(c)	υ_{11}	ζ_{12}	υ_{1in}	$(1 - D_2)$
(d)	$\upsilon_{11} > \Delta i_{L1} > \chi_{11}$	ζ_{12}	$\upsilon_{1in} > \Delta i_{in} > \chi_{1in}$	$(1 - D_2) < D_t < (D_1 - \overline{D_{NNin}})$
	χ_{11}	ζ_{12}	χ_{1in}	$(D_1 - \overline{D_{NNin}}) \leq D_t \leq (D_1 - \underline{D_{NNin}})$
	$\chi_{11} < \Delta i_{L1} < \upsilon_{11}$	ζ_{12}	$\chi_{1in} < \Delta i_{in} < \upsilon_{1in}$	$(D_1 - \underline{D_{NNin}}) < D_t < D_1$
(e)	υ_{11}	ζ_{12}	υ_{1in}	D_1
(f)	$\upsilon_{11} < \Delta i_{L1} < \nu_{11}$	$\zeta_{12} < \Delta i_{L2} < \sigma_{12}$	$\upsilon_{1in} < \Delta i_{in} < \nu_{1in}$	$D_1 < D_t < (1 + D_1 - D_2)$
(g)	ν_{11}	σ_{12}	ν_{1in}	$(1 + D_1 - D_2)$
(h)	ν_{11}	σ_{12}	ν_{1in}	$(1 + D_1 - D_2) < D_t < 1$

$\nu_{11} \equiv G_{NN1} D_1 T_s, \quad \nu_{1in} \equiv G_{NNin} D_1 T_s$
$\upsilon_{11} \equiv G_{NN1}(D_1 + D_2 - 1) T_s$
$\chi_{11} \equiv Max\{|G_{NF1}|(1 - D_2)T_s, |G_{FN1}|(1 - D_1)T_s\}$, $\chi_{1in} \equiv Max\{|G_{NFin}|(1 - D_2)T_s, |G_{FNin}|(1 - D_1)T_s\}$
$\zeta_{12} \equiv G_{NN2}(D_1 + D_2 - 1)T_s + G_{FN2}(1 - D_1)T_s$
$\sigma_{12} \equiv G_{NN2} D_1 T_s + G_{FN2}(D_2 - D_1)T_s$

Table B.15: Sector 8B for $D_1 + D_2 > 1$ and $D_1 < D_2$.

Fig. No.	Δi_{L1} $G_{NF1}<0, G_{FN1}<0$	Δi_{L2} $G_{NF2}<0, G_{FN2}>0$	Δi_{in} $G_{NFin}<0, G_{FNin}>0$	D_t
(a)	ν_{11}	σ_{12}	σ_{1in}	0
(b)	$\nu_{11} > \Delta i_{L1} > \upsilon_{11}$	$\sigma_{12} > \Delta i_{L2} > \zeta_{12}$	$\sigma_{1in} > \Delta i_{in} > \zeta_{1in}$	$0 < D_t < (1 - D_2)$
(c)	υ_{11}	ζ_{12}	ζ_{1in}	$(1 - D_2)$
(d)	$\upsilon_{11} > \Delta i_{L1} > \chi_{11}$ χ_{11} $\chi_{11} < \Delta i_{L1} < \upsilon_{11}$	ζ_{12} ζ_{12} ζ_{12}	ζ_{1in} ζ_{1in} ζ_{1in}	$(1 - D_2) < D_t < (D_1 - \overline{D_{NNin}})$ $(D_1 - \overline{D_{NNin}}) \le D_t \le (D_1 - \underline{D_{NNin}})$ $(D_1 - \underline{D_{NNin}}) < D_t < D_1$
(e)	υ_{11}	ζ_{12}	ζ_{1in}	D_1
(f)	$\upsilon_{11} < \Delta i_{L1} < \nu_{11}$	$\zeta_{12} < \Delta i_{L2} < \sigma_{12}$	$\zeta_{1in} < \Delta i_{in} < \sigma_{1in}$	$D_1 < D_t < (1 + D_1 - D_2)$
(g)	ν_{11}	σ_{12}	σ_{1in}	$(1 + D_1 - D_2)$
(h)	ν_{11}	σ_{12}	σ_{1in}	$(1 + D_1 - D_2) < D_t < 1$

$\nu_{11} \equiv G_{NN1} D_1 T_s$
$\upsilon_{11} \equiv G_{NN1}(D_1 + D_2 - 1)T_s$
$\chi_{11} \equiv Max\{|G_{NF1}|(1 - D_2)T_s, |G_{FN1}|(1 - D_1)T_s\}$
$\zeta_{12} \equiv G_{NN2}(D_1 + D_2 - 1)T_s + G_{FN2}(1 - D_1)T_s$, $\zeta_{1in} \equiv G_{NNin}(D_1 + D_2 - 1)T_s + G_{FNin}(1 - D_1)T_s$
$\sigma_{12} \equiv G_{NN2} D_1 T_s + G_{FN2}(D_2 - D_1)T_s$, $\sigma_{1in} \equiv G_{NNin} D_1 T_s + G_{FNin}(D_2 - D_1)T_s$

Table B.16: Sector 9 for $D_1 + D_2 > 1$ and $D_1 < D_2$.

Fig. No.	Δi_{L1} $G_{NF1}<0, G_{FN1}<0$	Δi_{L2} $G_{NF2}<0, G_{FN2}<0$	Δi_{in} $G_{NFin}<0, G_{FNin}<0$	D_t
(a)	ν_{11}	ν_{12}	ν_{1in}	0
(b)	$\nu_{11} > \Delta i_{L1} > \upsilon_{11}$	$\nu_{12} > \Delta i_{L2} > \upsilon_{12}$	$\nu_{1in} > \Delta i_{in} > \upsilon_{1in}$	$0 < D_t < (1 - D_2)$
(c)	υ_{11}	υ_{12}	υ_{1in}	$(1 - D_2)$
(d)	$\upsilon_{11} > \Delta i_{L1} > \chi_{11}$ χ_{11} $\chi_{11} < \Delta i_{L1} < \upsilon_{11}$	$\upsilon_{12} > \Delta i_{L2} > \chi_{12}$ χ_{12} $\chi_{12} < \Delta i_{L2} < \upsilon_{12}$	$\upsilon_{1in} > \Delta i_{in} > \chi_{1in}$ χ_{1in} $\chi_{1in} < \Delta i_{in} < \upsilon_{1in}$	$(1 - D_2) < D_t < (D_1 - \overline{D_{NNin}})$ $(D_1 - \overline{D_{NNin}}) \le D_t \le (D_1 - \underline{D_{NNin}})$ $(D_1 - \underline{D_{NNin}}) < D_t < D_1$
(e)	υ_{11}	υ_{12}	υ_{1in}	D_1
(f)	$\upsilon_{11} < \Delta i_{L1} < \nu_{11}$	$\upsilon_{12} < \Delta i_{L2} < \nu_{12}$	$\upsilon_{1in} < \Delta i_{in} < \nu_{1in}$	$D_1 < D_t < (1 + D_1 - D_2)$
(g)	ν_{11}	ν_{12}	ν_{1in}	$(1 + D_1 - D_2)$
(h)	ν_{11}	ν_{12}	ν_{1in}	$(1 + D_1 - D_2) < D_t < 1$

$\nu_{11} \equiv G_{NN1} D_1 T_s$, $\nu_{12} \equiv G_{NN2} D_1 T_s$, $\nu_{1in} \equiv G_{NNin} D_1 T_s$
$\upsilon_{11} \equiv G_{NN1}(D_1 + D_2 - 1)T_s$, $\upsilon_{12} \equiv G_{NN2}(D_1 + D_2 - 1)T_s$, $\upsilon_{1in} \equiv G_{NNin}(D_1 + D_2 - 1)T_s$
$\chi_{11} \equiv Max\{|G_{NF1}|(1 - D_2)T_s, |G_{FN1}|(1 - D_1)T_s\}$
$\chi_{12} \equiv Max\{|G_{NF2}|(1 - D_2)T_s, |G_{FN2}|(1 - D_1)T_s\}$, $\chi_{1in} \equiv Max\{|G_{NFin}|(1 - D_2)T_s, |G_{FNin}|(1 - D_1)T_s\}$

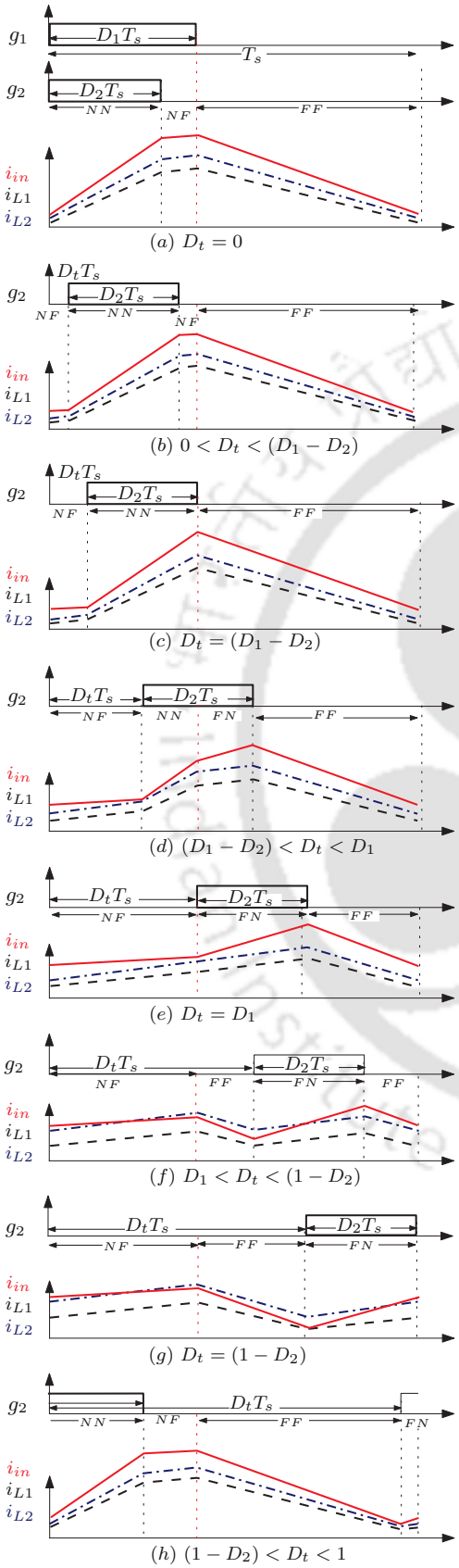


Figure B.1: The patterns of i_{L1} (black dashed), i_{L2} (blue dash-dot) and i_{in} (red solid) in sector 1 as D_t varies from 0 to 1.

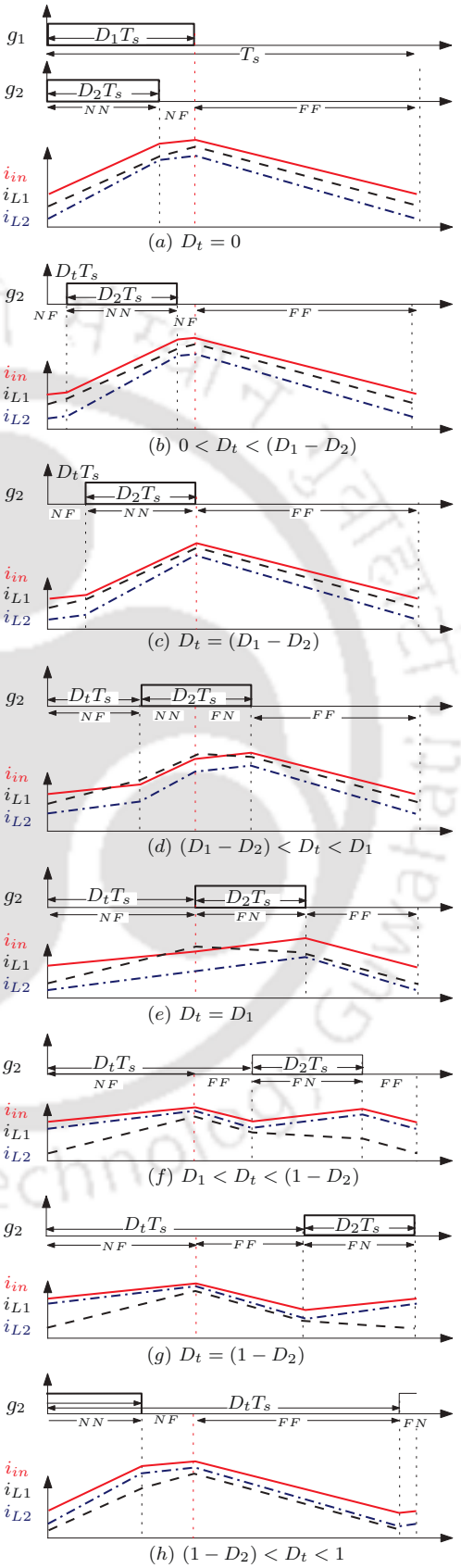


Figure B.2: The patterns of i_{L1} (black dashed), i_{L2} (blue dash-dot) and i_{in} (red solid) in sector 2A as D_t varies from 0 to 1.

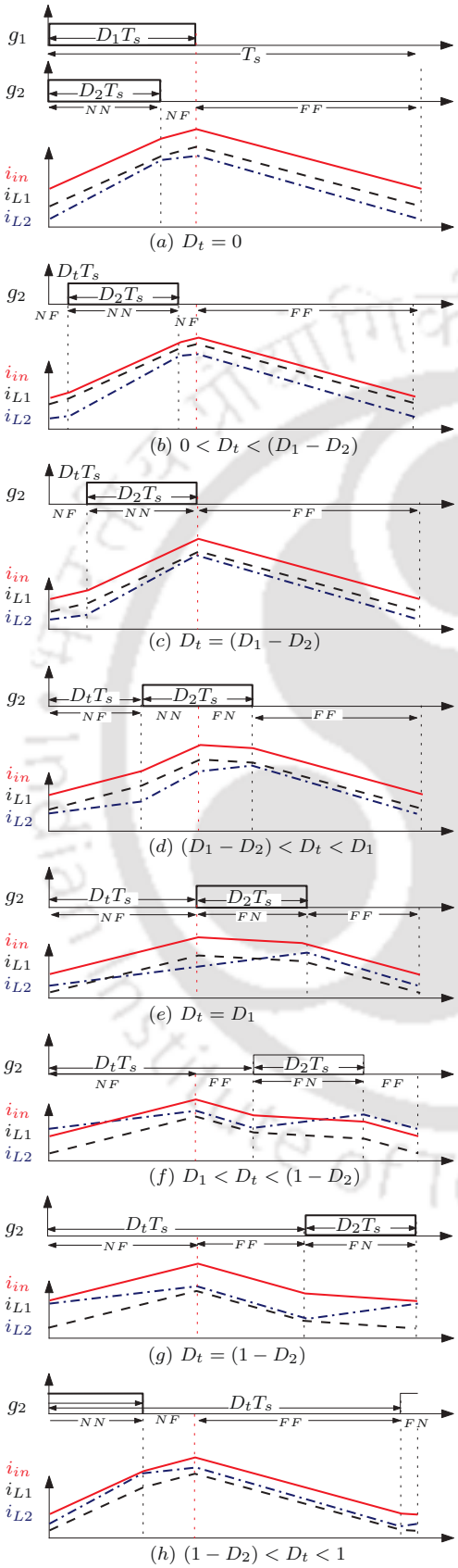


Figure B.3: The patterns of i_{L1} (black dashed), i_{L2} (blue dash-dot) and i_{in} (red solid) in sector 2B as D_t varies from 0 to 1.

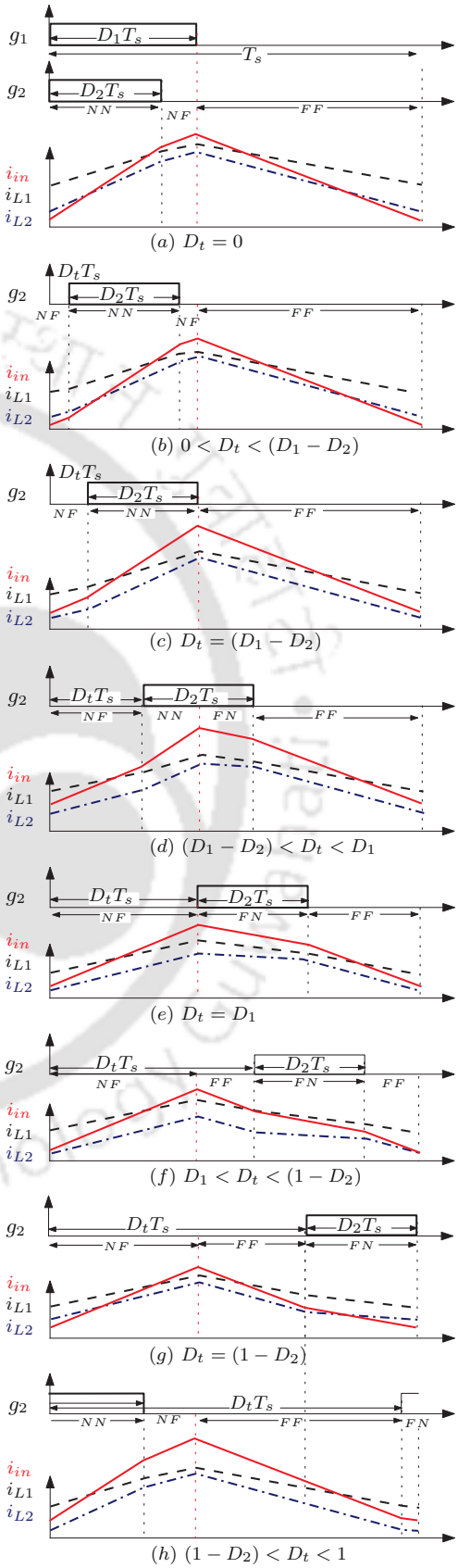


Figure B.4: The patterns of i_{L1} (black dashed), i_{L2} (blue dash-dot) and i_{in} (red solid) in sector 3 as D_t varies from 0 to 1.

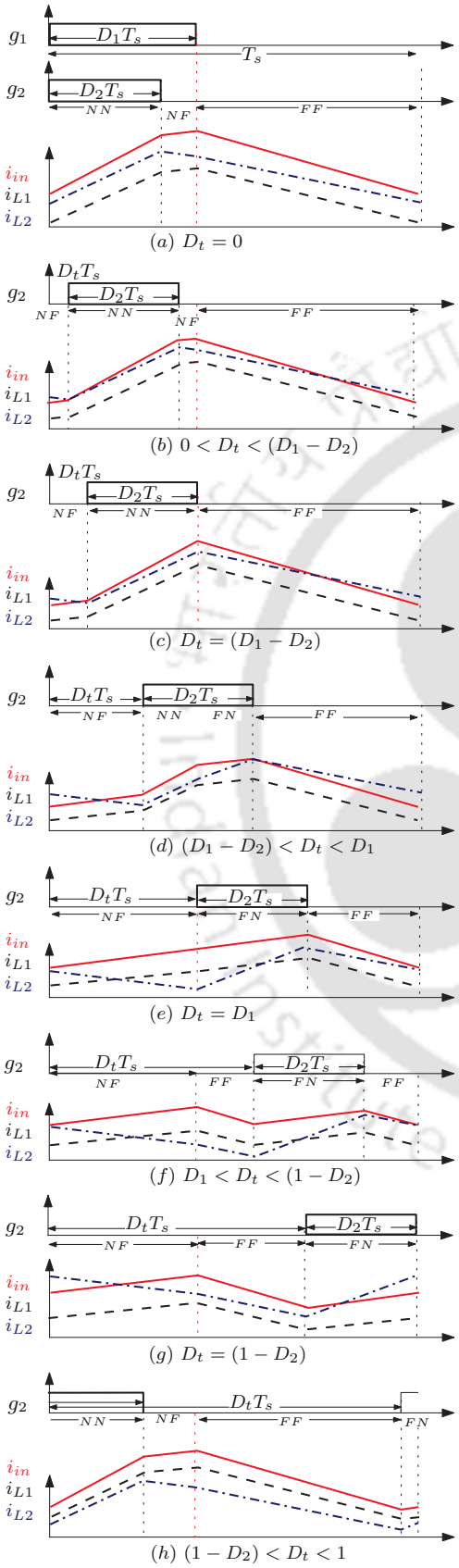


Figure B.5: The patterns of i_{L1} (black dashed), i_{L2} (blue dash-dot) and i_{in} (red solid) in sector 4A as D_t varies from 0 to 1.

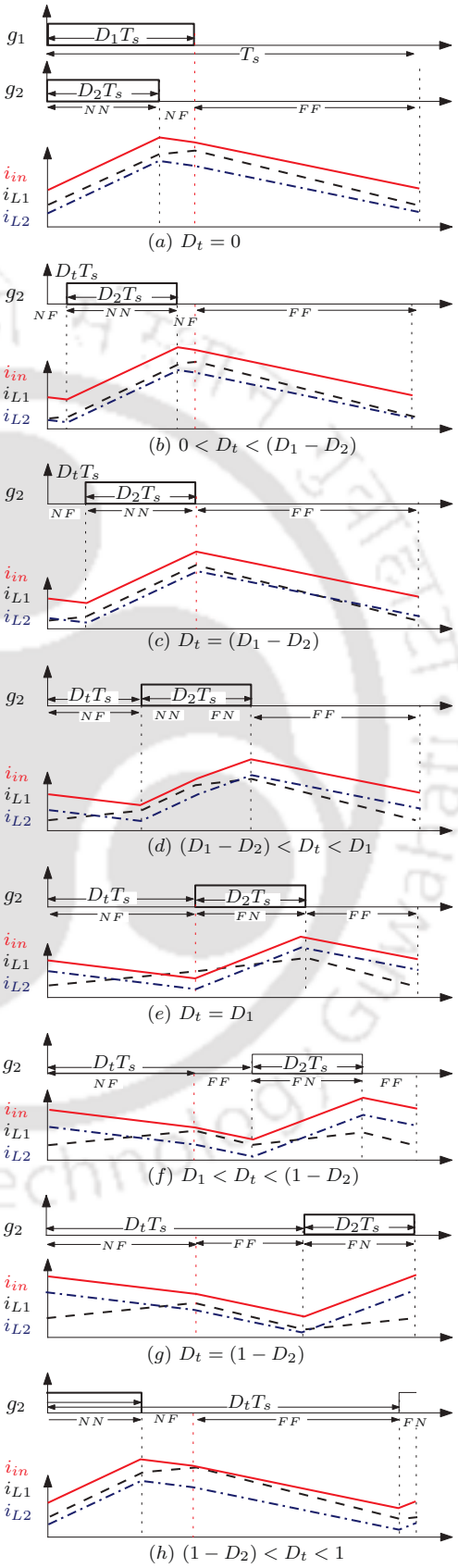


Figure B.6: The patterns of i_{L1} (black dashed), i_{L2} (blue dash-dot) and i_{in} (red solid) in sector 4B as D_t varies from 0 to 1.

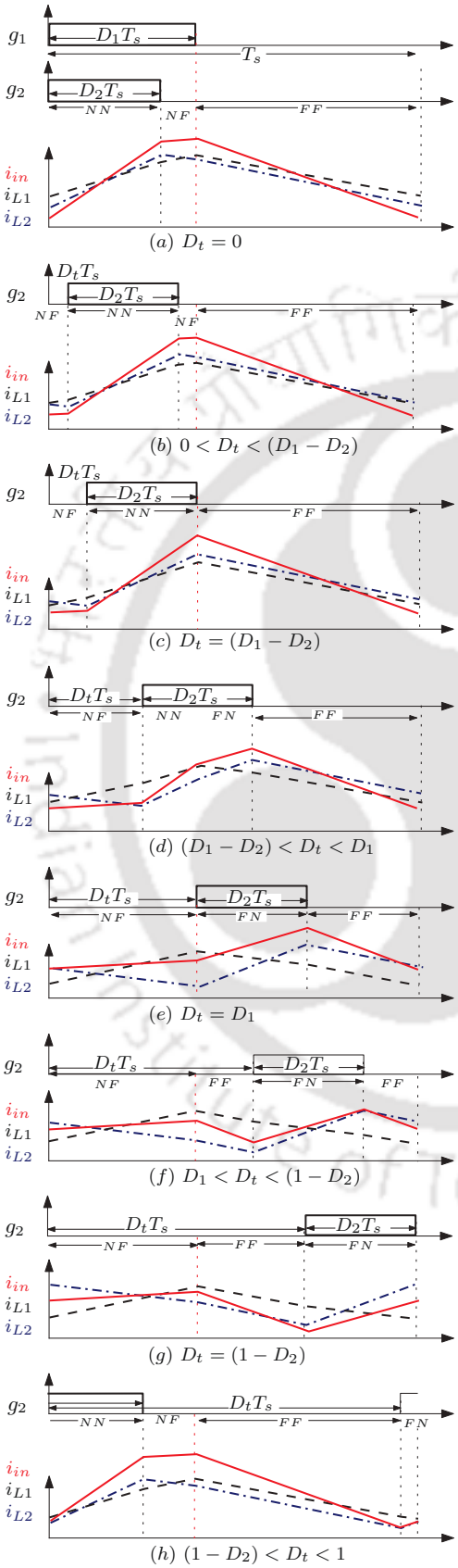


Figure B.7: The patterns of i_{L1} (black dashed), i_{L2} (blue dash-dot) and i_{in} (red solid) in sector 5A as D_t varies from 0 to 1.

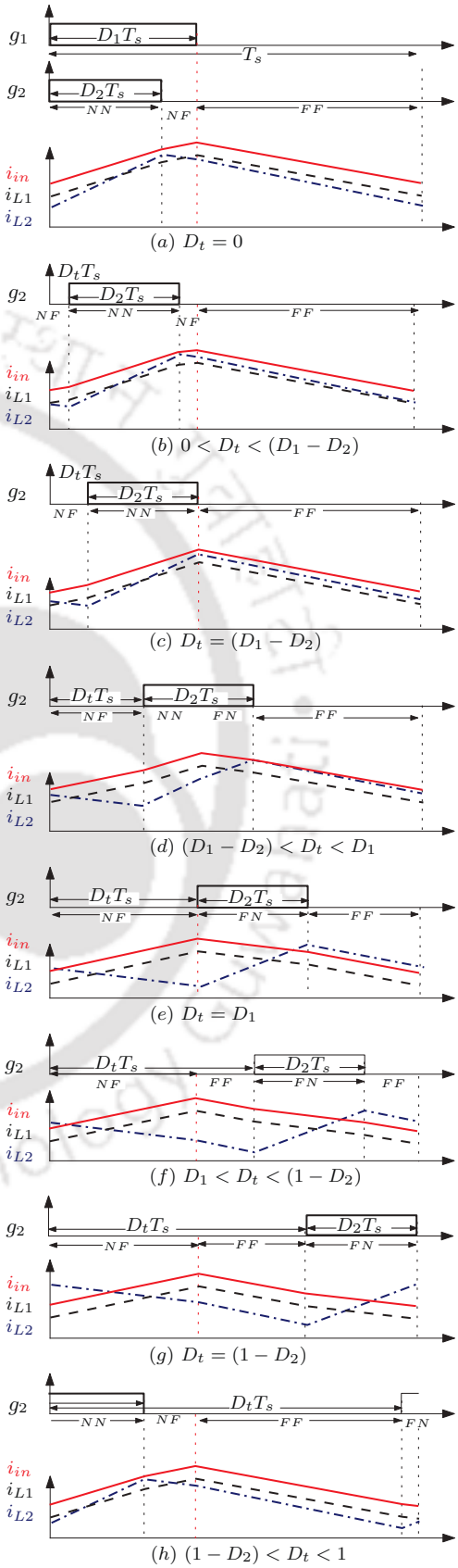


Figure B.8: The patterns of i_{L1} (black dashed), i_{L2} (blue dash-dot) and i_{in} (red solid) in sector 5B as D_t varies from 0 to 1.

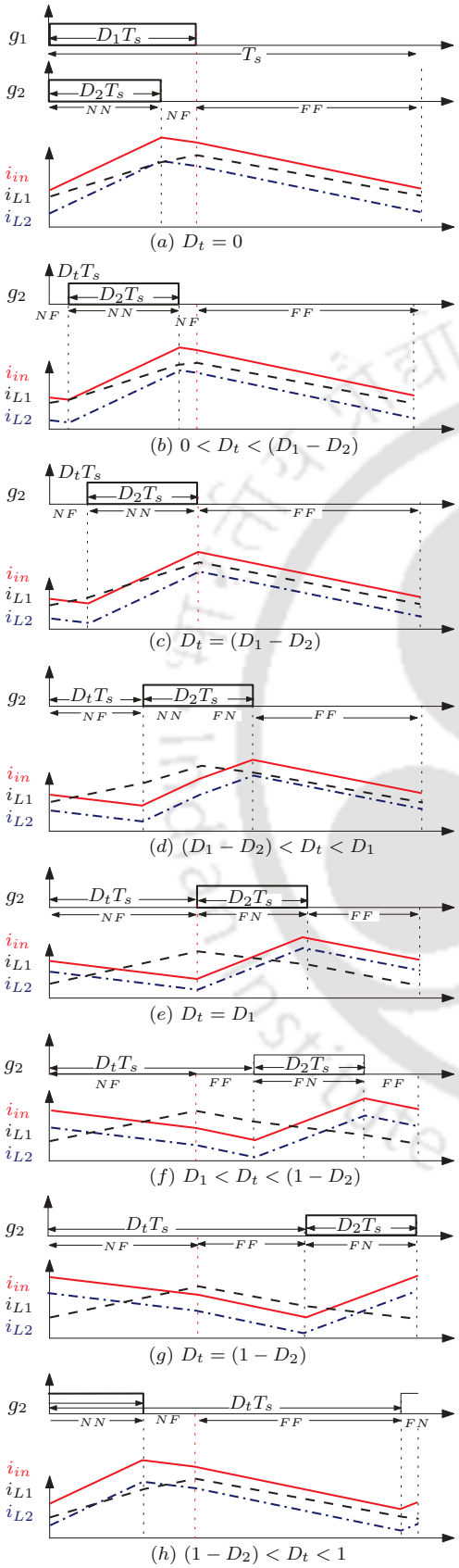


Figure B.9: The patterns of i_{L1} (black dashed), i_{L2} (blue dash-dot) and i_{in} (red solid) in sector 5C as D_t varies from 0 to 1.

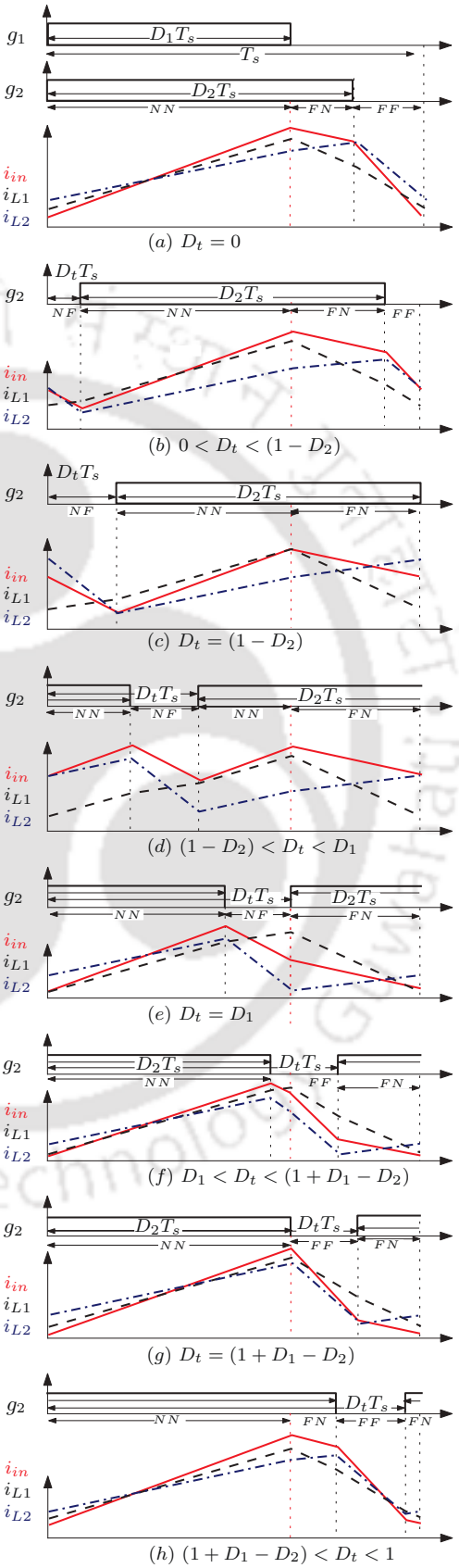


Figure B.10: The patterns of i_{L1} (black dashed), i_{L2} (blue dash-dot) and i_{in} (red solid) in sector 5D as D_t varies from 0 to 1.

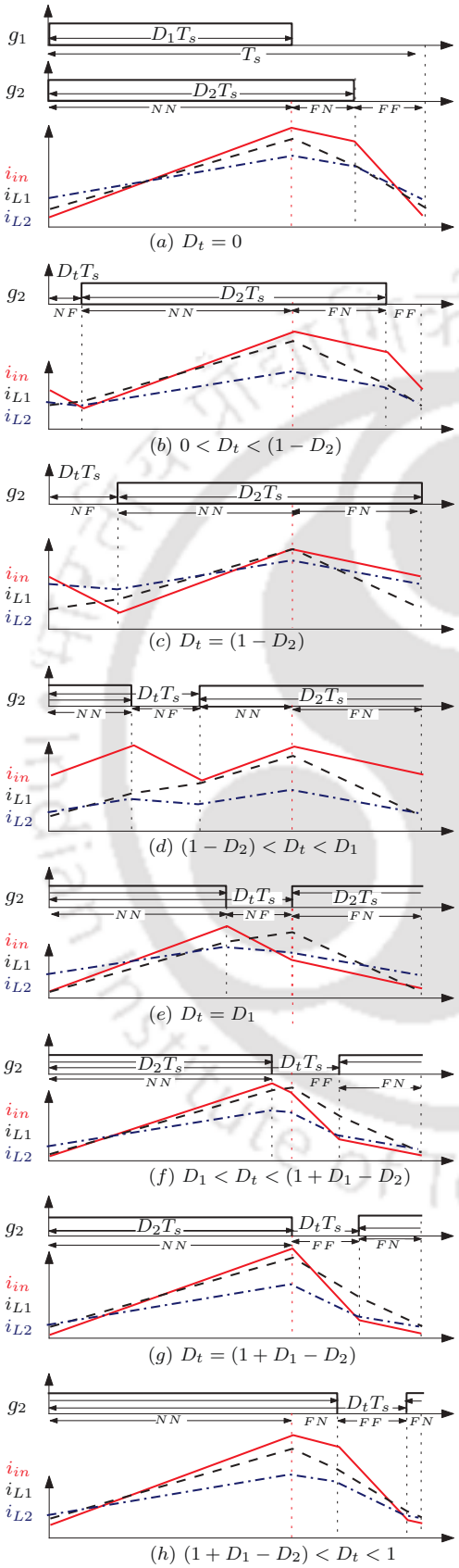


Figure B.11: The patterns of i_{L1} (black dashed), i_{L2} (blue dash-dot) and i_{in} (red solid) in sector 6A as D_t varies from 0 to 1.

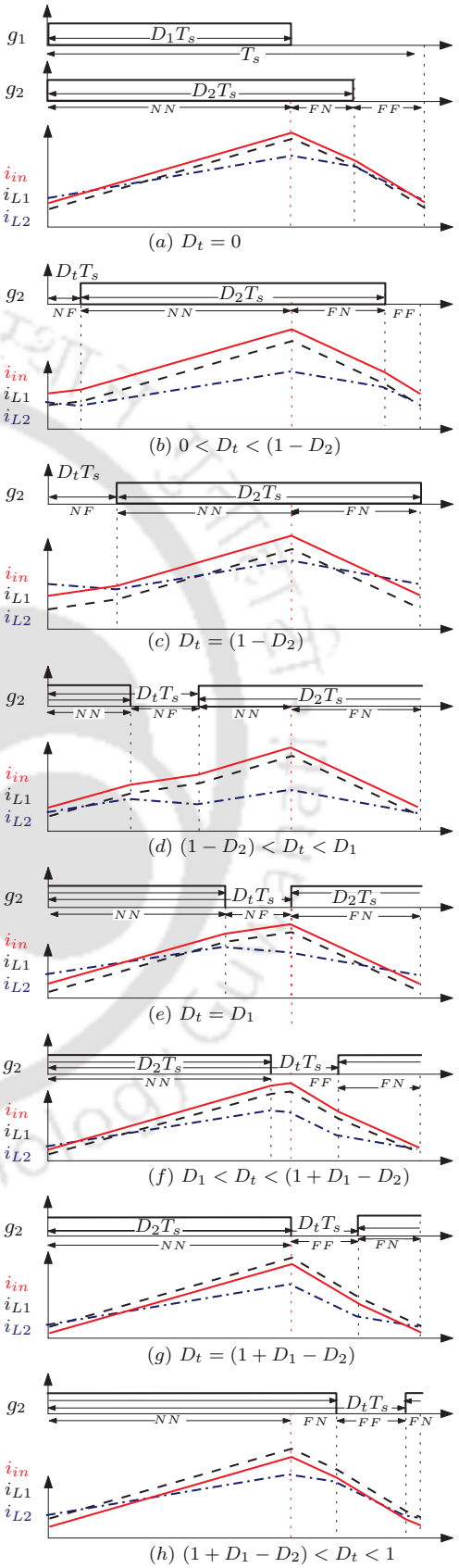


Figure B.12: The patterns of i_{L1} (black dashed), i_{L2} (blue dash-dot) and i_{in} (red solid) in sector 6B as D_t varies from 0 to 1.

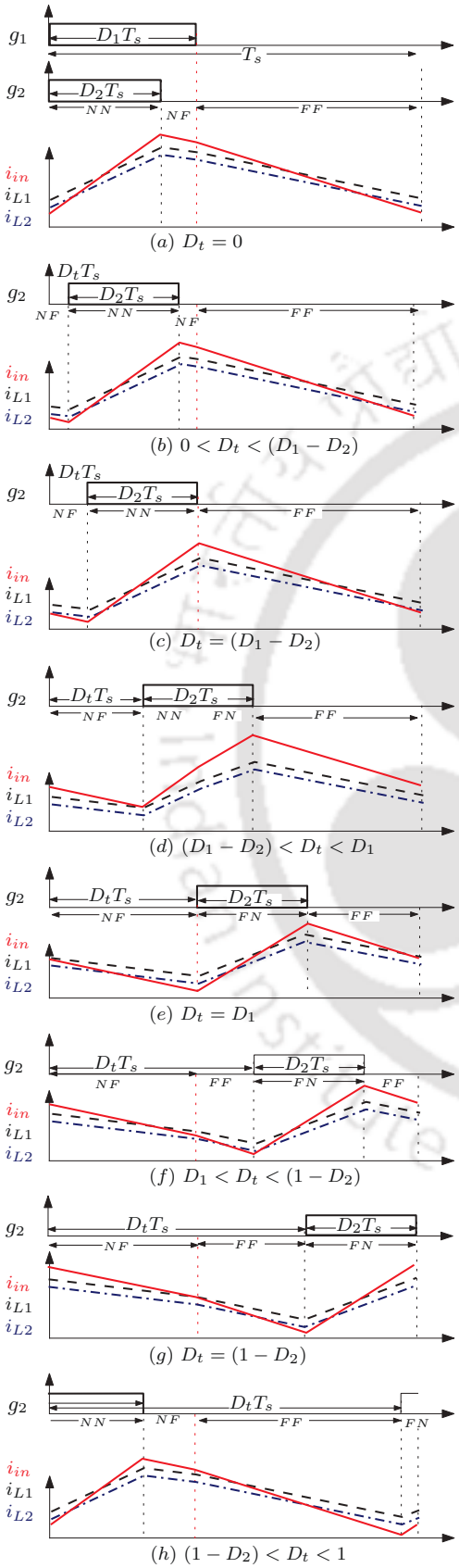


Figure B.13: The patterns of i_{L1} (black dashed), i_{L2} (blue dash-dot) and i_{in} (red solid) in sector 7 as D_t varies from 0 to 1.

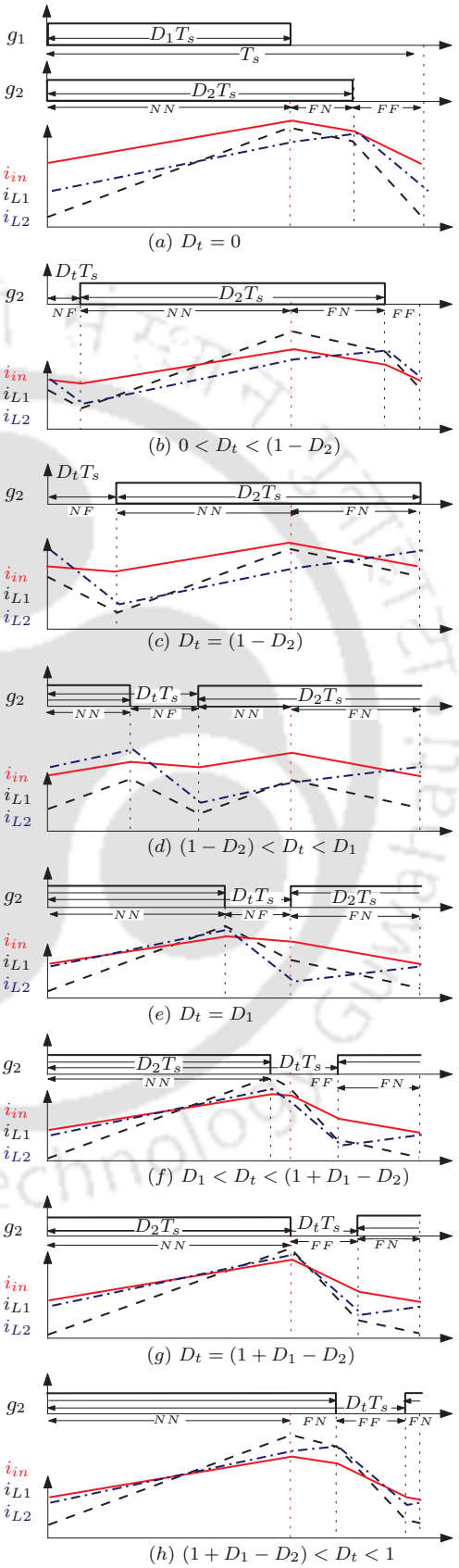


Figure B.14: The patterns of i_{L1} (black dashed), i_{L2} (blue dash-dot) and i_{in} (red solid) in sector 8A as D_t varies from 0 to 1.

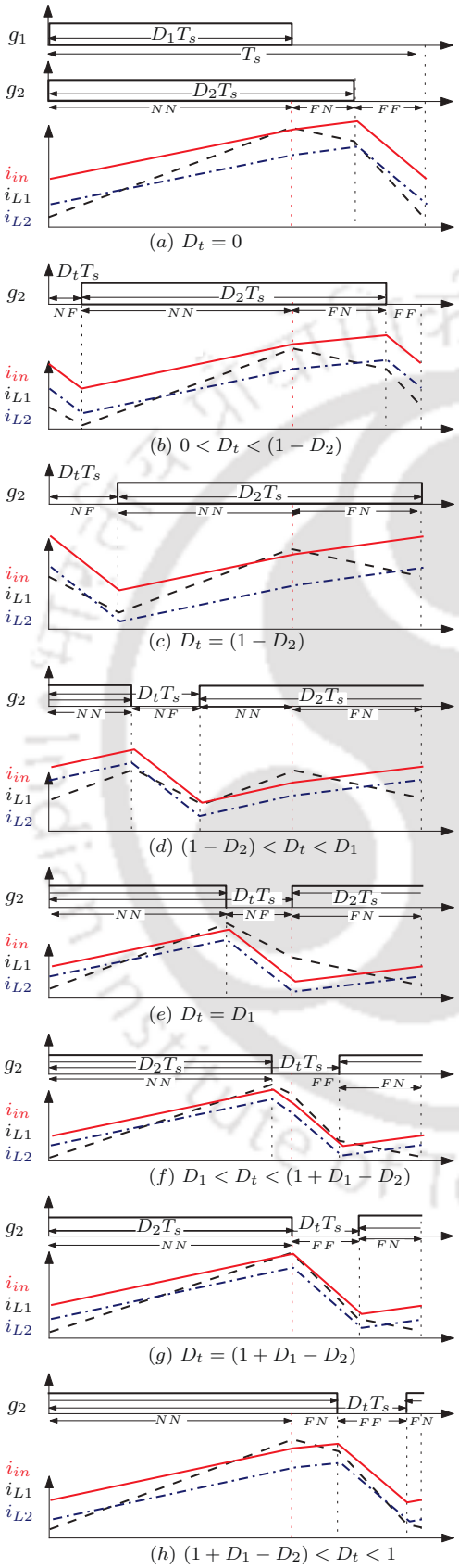


Figure B.15: The patterns of i_{L1} (black dashed), i_{L2} (blue dash-dot) and i_{in} (red solid) in sector 8B as D_t varies from 0 to 1.

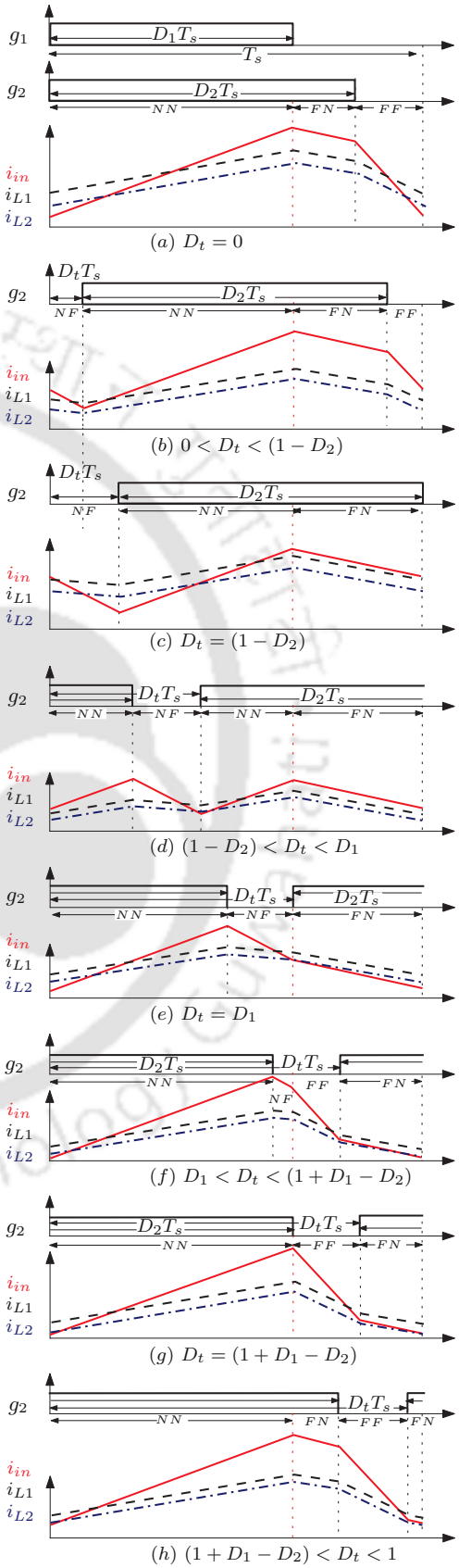


Figure B.16: The patterns of i_{L1} (black dashed), i_{L2} (blue dash-dot) and i_{in} (red solid) in sector 9 as D_t varies from 0 to 1.

B.2 Sector wise slope cancellation and ripple cancellation in i_{in}

This appendix shows the patterns of i_{L1}, i_{L2} and i_{in} at $D_t = \mathbf{D}_{min}$. The states are shown where slope cancellation and ripple cancellation occurs. Examples from all 16 possible sectors are shown in Figures B.17 to B.32.

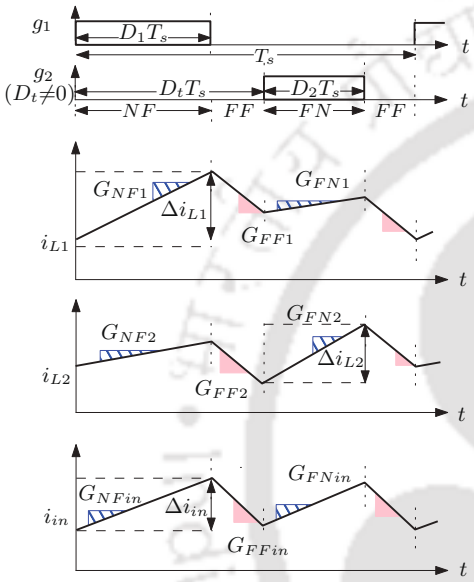


Figure B.17: No slope cancellation and conditional ripple cancellation in sector 1 for $D_t = \mathbf{D}_{min}$.

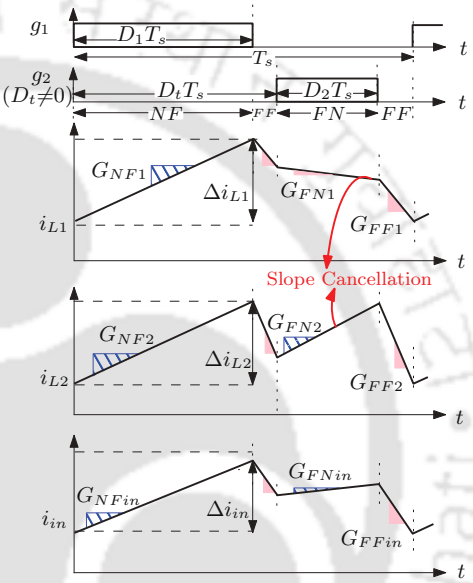


Figure B.18: The slope cancellation in FN and conditional ripple cancellation in sector 2A for $D_t = \mathbf{D}_{min}$.

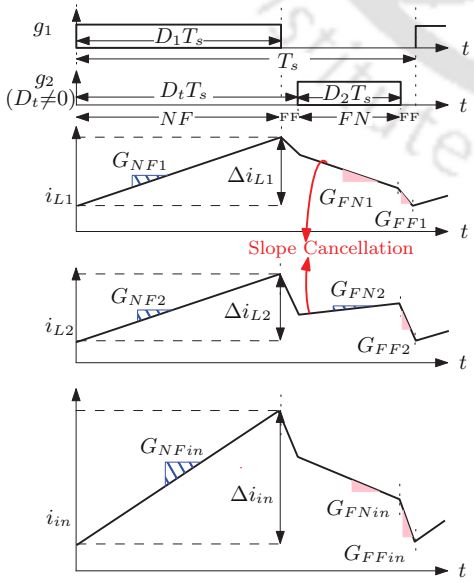


Figure B.19: The slope cancellation in FN with no ripple cancellation in sector 2B for $D_t = \mathbf{D}_{min}$.

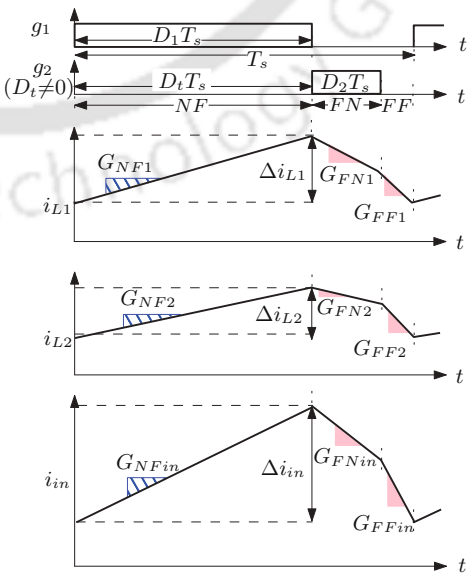


Figure B.20: No slope cancellation with no ripple cancellation in sector 3 for $D_t = \mathbf{D}_{min}$.

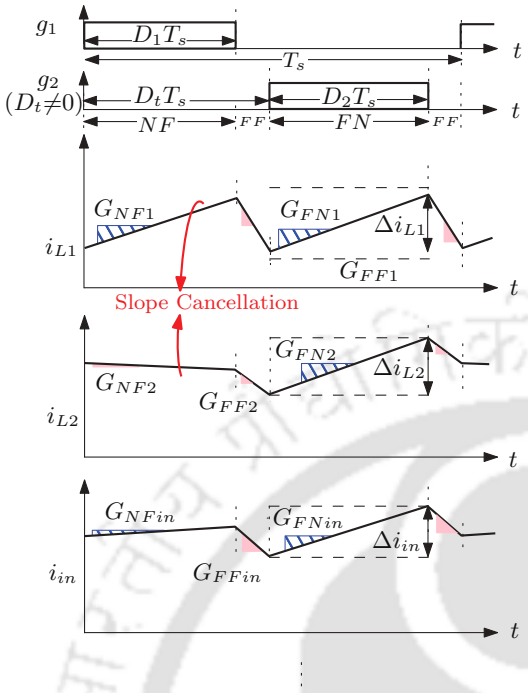


Figure B.21: The slope cancellation in NF and conditional ripple cancellation in sector 4A for D_t = $\mathbf{D}_{min}$.

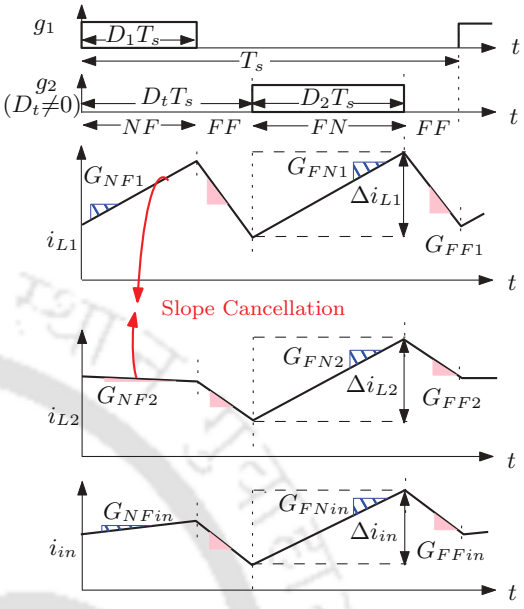


Figure B.22: The slope cancellation in NF with no ripple cancellation in sector 4B for $D_t\mathbf{D}_{min}$.

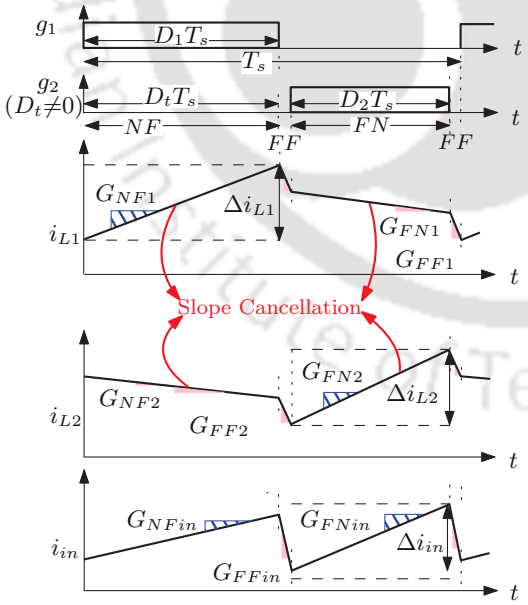


Figure B.23: The slope cancellation in both NF and FN with ripple cancellation in sector 5A for D_t = $\mathbf{D}_{min}$.

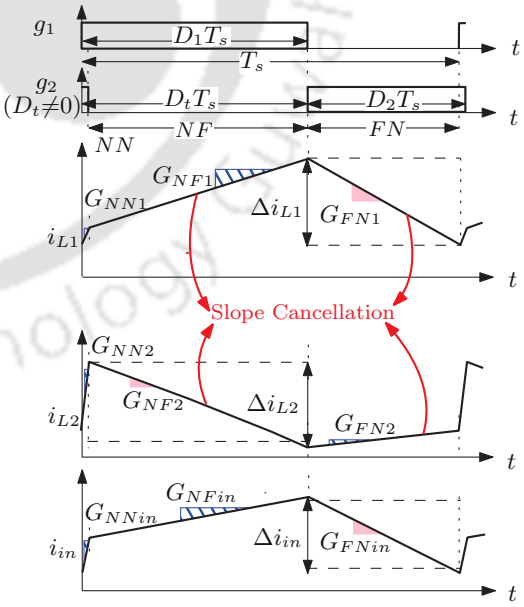


Figure B.24: The slope cancellation in both NF and FN with ripple cancellation in sector 5B for D_t = $\mathbf{D}_{min}$.

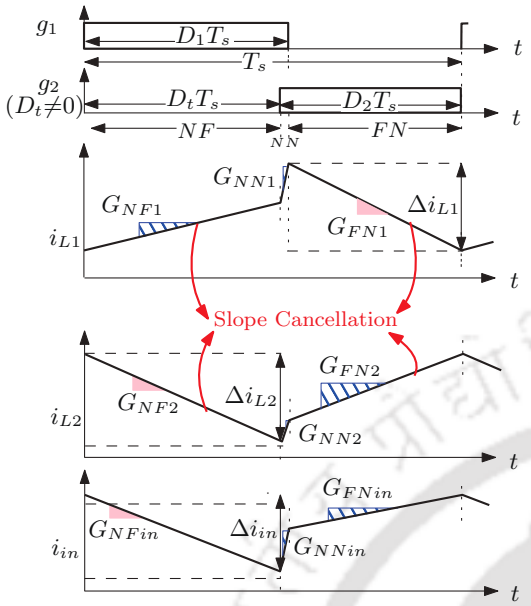


Figure B.25: The slope cancellation in both *NF* and *FN* with ripple cancellation in sector 5C for $D_t = \mathbf{D}_{min}$.

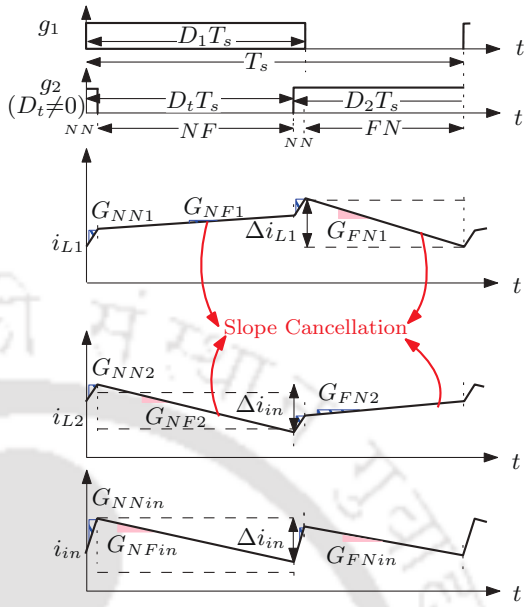


Figure B.26: The slope cancellation in both *NF* and *FN* with ripple cancellation in sector 5D for $D_t = \mathbf{D}_{min}$.

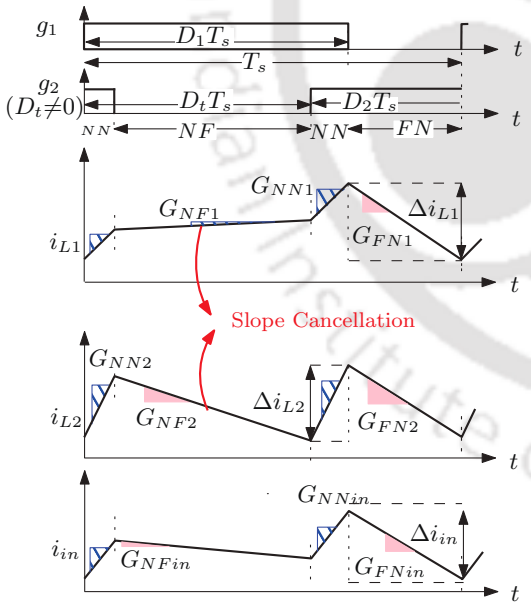


Figure B.27: The slope cancellation in *NF* and conditional ripple cancellation in sector 6A for $D_t = \mathbf{D}_{min}$.

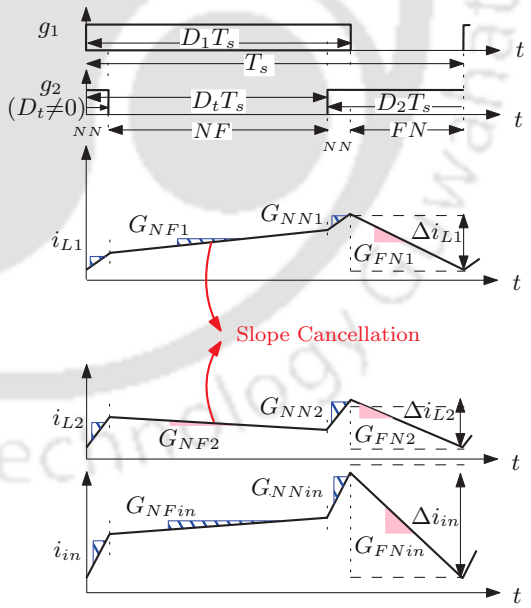


Figure B.28: The slope cancellation in *NF* with no ripple cancellation in sector 6B for $D_t = \mathbf{D}_{min}$.

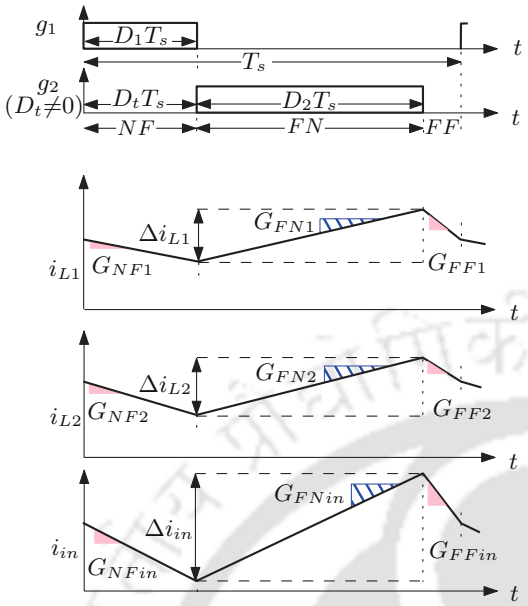


Figure B.29: No slope cancellation with no ripple cancellation in sector 7 for $D_t = \mathbf{D}_{min}$.

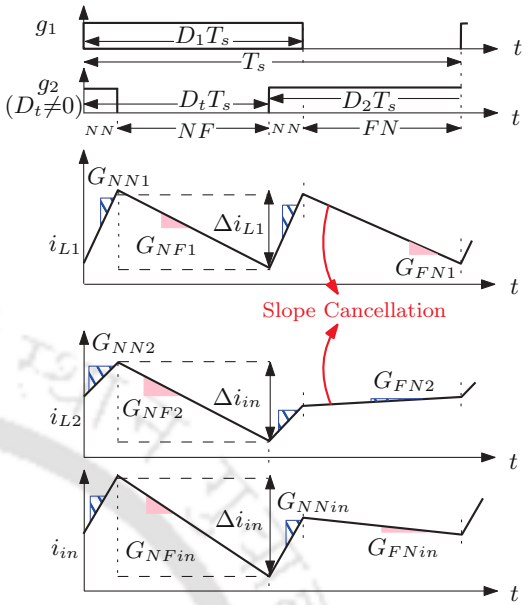


Figure B.30: The slope cancellation in FN and conditional ripple cancellation in sector 8A for $D_t = \mathbf{D}_{min}$.

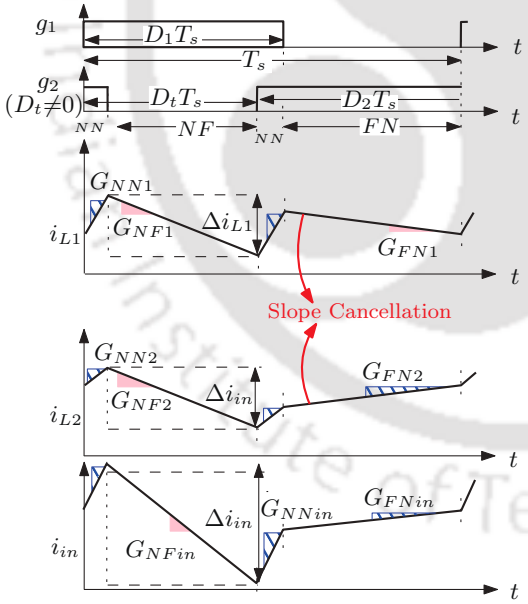


Figure B.31: The slope cancellation in FN with no ripple cancellation in sector 8B for $D_t = \mathbf{D}_{min}$.

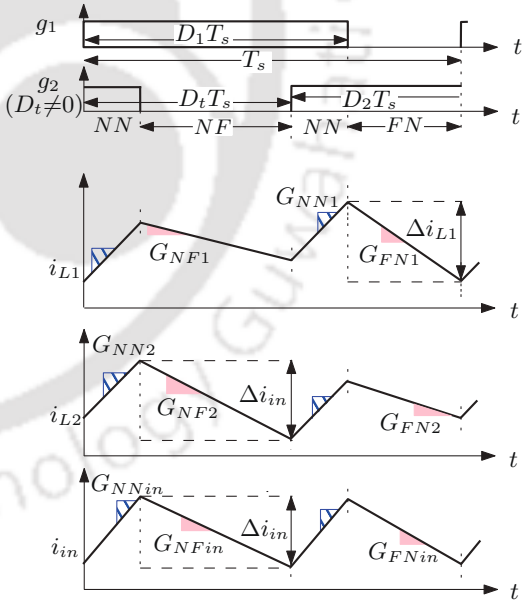


Figure B.32: No slope cancellation and conditional ripple cancellation in sector 9 for $D_t = \mathbf{D}_{min}$.

C

All the sectors and modes of CI-SIDO boost converter when i_{L1} is in DCM and i_{L2} is in CCM

C.1 Durations of All the States of CI-SIDO Boost converter in DCM

This appendix shows the waveforms of all the sectors and modes of CI-SIDO boost converter. The durations of all the states are also derived for each sectors and modes.

C.1.1 Sector 1 and 2

C.1.1.1 Modes 1a and 2a

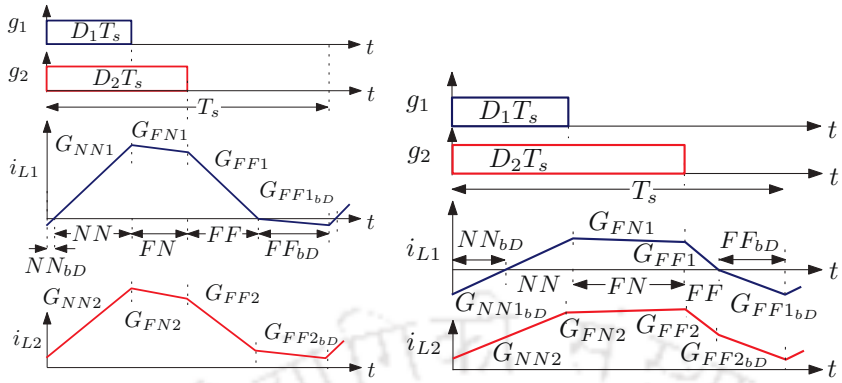
The waveforms of Mode 1a is shown in Fig. C.1(a) and Mode 2a is shown in Fig. C.1(b). Using the figure, the analysis is presented below-

$$\begin{aligned}
D_2 &= t_{NN_{bD}} + t_{NN} + t_{FN}, \\
G_{NN1} t_{NN_{bD}} &= G_{NF1}(1 - D_2 - t_{FF}), \\
\implies t_{NN_{bD}} &= \frac{|G_{NF1}|(1 - D_2 - t_{FF})}{G_{NN1}}, \\
|G_{NN1}| t_{NN} &= |G_{FN1}| t_{FN} + |G_{FF1}| t_{FF}, \\
\implies t_{FN} &= \frac{(D_2 - t_{NN_{bD}} - t_{FF}\frac{|G_{FF1}|}{|G_{NN1}|})}{(1 + \frac{|G_{FN1}|}{|G_{NN1}|})}, \\
D_1 &= t_{NN_{bD}} + t_{NN}, \\
i_{o1} &= \frac{T_s}{2}[(t_{FF} \times |G_{FF1}| \times t_{FF}) + (t_{FN} \times (t_{NN} G_{NN1} + t_{FF}|G_{FF1}|)].
\end{aligned} \tag{C.1}$$

At CCM/DCM boundary, we have $t_{NN_{bD}} = t_{FF_{bD}} = 0$, $t_{FF} = (1 - D_2)$, $D_2 = t_{NN} + t_{FN}$. The obtained values of $i_{o1} = i_{o1bd}$ and $D_1 = t_{NN}$ at the CCM/DCM boundary are–

$$\begin{aligned}
i_{o1bd} &= \frac{T_s}{2}\,[t_{NN}(D_2 - t_{NN})G_{NN1} + (1 - D_2)(1 - t_{NN})|G_{FF1}|] \\
&\text{where, } t_{NN} = \frac{D_2|G_{FN1}| + (1 - D_2)|G_{FF1}|}{G_{NN1} + G_{FN1}}.
\end{aligned} \tag{C.2}$$

Therefore, i_{L1} remains in Mode 1a when $i_{o11b} < i_{o1} < i_{o1bd}$ and $D_{1_{1b}} < D_1 < t_{NN}$.



(a) Mode 1a (b) Mode 2a

Figure C.1: The theoretical waveforms of g_1, g_2, i_{L1}, i_{L2}, when operating in Mode 1a and 2a of CI-SIDO boost converter.

C.1.1.2 Modes 1b and 2b

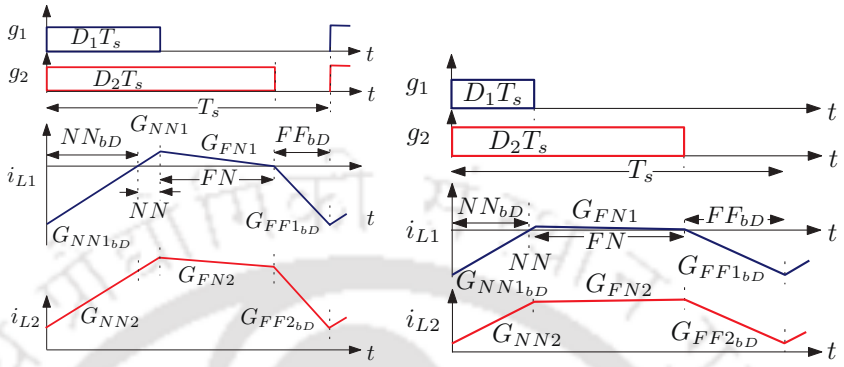
The waveforms of Mode 1b is shown in Fig. C.2(a) and Mode 2b is shown in Fig. C.2(b).

$$
\begin{aligned}
t_{FF_{bD}} &= (1 - D_2), \\
G_{NN1} t_{NN_{bD}} &= G_{NF1}(1 - D_2), \\
\implies t_{NN_{bD}} &= \frac{G_{NF1}(1 - D_2)}{G_{NN1}}, \\
t_{NN} + t_{FN} &= D_2 - t_{NN_{bD}} - t_{FF_{bD}}, \\
t_{FN} &= \frac{G_{NN1} t_{NN}}{|G_{FN1}|}, \\
t_{NN} &= \frac{(D_2 - t_{NN_{bD}} - t_{FF_{bD}})}{(1 + \frac{G_{NN1}}{|G_{FN1}|})}, \\
t_{FN} &= \frac{G_{NN1}}{|G_{FN1}|} \frac{(D_2 - t_{NN_{bD}} - t_{FF_{bD}})}{(1 + \frac{G_{NN1}}{|G_{FN1}|})}, \\
D_1 &= t_{NN_{bD}} + t_{NN}, \\
i_{o1} &= \frac{T_s}{2}[t_{FN} \times |G_{FN1}| \times t_{FN}].
\end{aligned}
\tag{C.3}
$$

Finding the values of $i_{o1} = i_{o11b}$ and $D_1 = D_{1_b}$ at Mode 1b, we obtain–

$$
\begin{aligned}
i_{o11b} &= \frac{|G_{FN1}|(D_2 T_s G_{NN1} - |G_{NF1}|(1 - D_2)T_s)^2}{2T_s(|G_{FN1}| + G_{NN1})^2}, \\
D_{1_b} &= \frac{D_2 G_{FN1} + (1 - D_2)G_{NF1}}{G_{NN1} + G_{FN1}}.
\end{aligned}
\tag{C.4}
$$

At $i_{o1} = i_{o11b}$ and $D_1 = D_{1_b}$, the converter is at Mode 1b. After that if $i_{o1} < i_{o11b}$ and $D_1 < D_{1_b}$, the converter operates in Mode 1c.

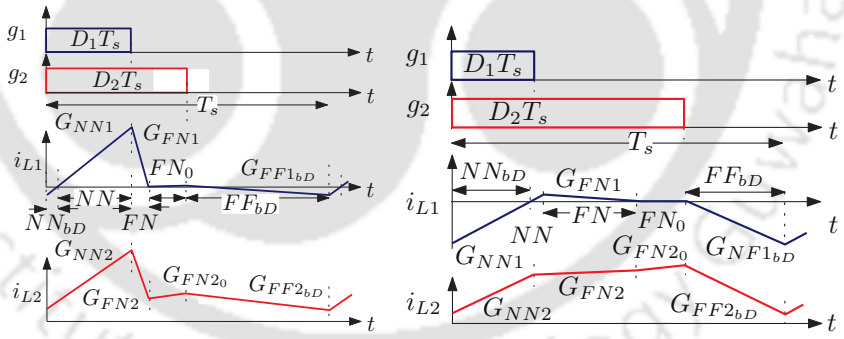


(a) Mode 1b (b) Mode 2b

Figure C.2: The theoretical waveforms of g_1, g_2, i_{L1}, i_{L2}, when operating in Mode 1b and 2b of CI-SIDO boost converter.

C.1.1.3 Modes 1c and 2c

The waveforms of Mode 1c is shown in Fig. C.3(a) and Mode 2c is shown in Fig. C.3(b).



(a) Mode 1c (b) Mode 2c

Figure C.3: The theoretical waveforms of g_1, g_2, i_{L1}, i_{L2}, when operating in Mode 1c and 2c of CI-SIDO boost converter.

$$
\begin{aligned}
t_{FF_{bD}} &= (1 - D_2), \\
G_{NN1} t_{NN_{bD}} &= G_{NF1}(1 - D_2), \\
\implies t_{NN_{bD}} &= \frac{G_{NF1}(1 - D_2)}{G_{NN1}}, \\
t_{NN} + t_{FN} &= D_2 - t_{NN_{bD}} - t_{FN_0}, \\
t_{FN} &= \frac{G_{NN1} t_{NN}}{|G_{FN1}|}, \\
t_{NN} &= \frac{(D_2 - t_{NN_{bD}} - t_{FN_0})}{(1 + \frac{G_{NN1}}{|G_{FN1}|})}, \\
t_{FN} &= \frac{G_{NN1}}{|G_{FN1}|} \frac{(D_2 - t_{NN_{bD}} - t_{FN_0})}{(1 + \frac{G_{NN1}}{|G_{FN1}|})}, \\
D_1 &= t_{NN_{bD}} + t_{NN}, \\
I_{o1} &= \frac{T_s}{2}[t_{FN} \times |G_{FN1}| \times t_{FN}].
\end{aligned}
\tag{C.5}
$$

C.1.2 Sector 3

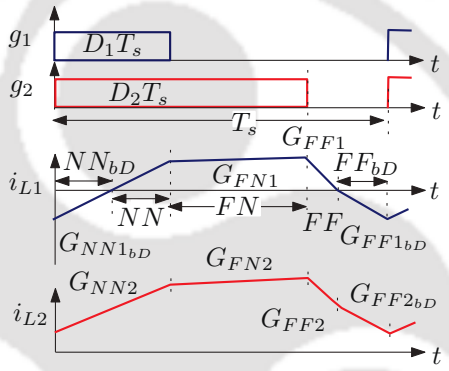
The waveforms of CI-SIDO boost converter in Sector 3 is shown in Fig. C.4(a). The durations are derived as presented below-

$$
\begin{aligned}
D_2 &= t_{NN_{bD}} + t_{NN} + t_{FN}, \\
G_{NN1} t_{NN_{bD}} = G_{NF1}(1 - D_2 - t_{FF}) &\implies t_{NN_{bD}} = \frac{|G_{NF1}|(1 - D_2 - t_{FF})}{G_{NN1}}, \\
|G_{NN1}| t_{NN} + |G_{FN1}| t_{FN} &= |G_{FF1}| t_{FF}, \\
t_{FN} &= \frac{(D_2 - t_{NN_{bD}} - t_{FF}\frac{|G_{FF1}|}{|G_{NN1}|})}{(1 - \frac{|G_{FN1}|}{|G_{NN1}|})}, \\
t_{NN} &= t_{FF}\frac{|G_{FF1}|}{|G_{NN1}|} - t_{FN}\frac{|G_{FN1}|}{|G_{NN1}|}, \\
i_{o1} &= \frac{T_s}{2}[(t_{FF} \times |G_{FF1}| \times t_{FF}) + t_{FN} \times (t_{NN} G_{NN1} + t_{FF}|G_{FF1}|)].
\end{aligned}
\tag{C.6}
$$

At CCM/DCM boundary, $t_{NN_{bD}} = t_{FF_{bD}} = 0$, $t_{FF} = (1 - D_2)$, and $t_{NN} + t_{FN} = D_2$. The boundary values of load currents and duty ratios are–

$$\begin{aligned} i_{o1bd} &= \frac{T_s}{2}\left[t_{NN}(D_2 - t_{NN})G_{NN1} + (1 - D_2)(1 - t_{NN})|G_{FF1}|\right] \\ \text{where, } t_{NN} &= \frac{|G_{FF1}|(1 - D_2) - G_{FN1}D_2}{(G_{NN1} - G_{FN1})}. \\ D_{1_{bd}} &= t_{NN}. \end{aligned} \tag{C.7}$$

Therefore, to operate the converter in Sector 3, $i_{o1} < i_{o1bd}$ and $D_1 < D_{1_{bd}}$.



(a) Mode 3

Figure C.4: The theoretical waveforms of g_1, g_2, i_{L1}, i_{L2}, when operating in Sector 3 of CI-SIDO boost converter.

C.1.3 Sector 4, 5, 7, 8

C.1.3.1 Modes 4a, 5a, 7a and 8a

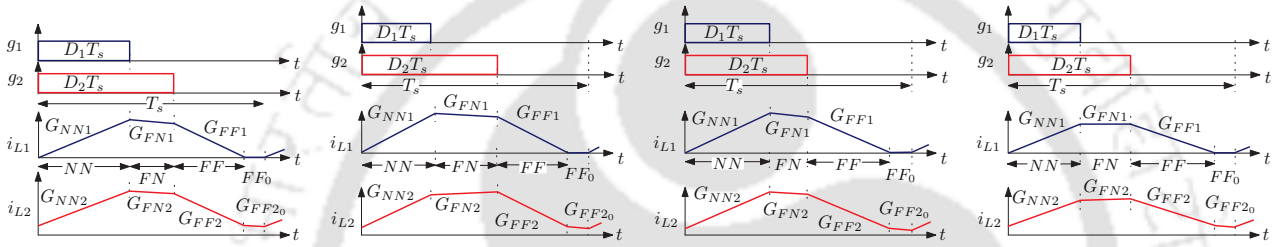
The waveforms of Modes 4a, 5a, 7a and 8a are shown in Figs. C.5(a), C.5(b), C.5(c) and C.5(d) respectively.

$$\begin{aligned} t_{NN} + t_{FN} &= D_2 \\ t_{FN} &= D_2 - t_{NN} \\ G_{NN1}t_{NN} &= G_{FN1}t_{FN} + |G_{FF1}|t_{FF} \\ (G_{NN1} + G_{FN1})t_{NN} &= G_{FN1}D_2 + |G_{FF1}|t_{FF} \\ t_{NN} &= \frac{G_{FN1}D_2 + |G_{FF1}|t_{FF}}{(G_{NN1} + G_{FN1})} \\ i_{o1} &= \frac{T_s}{2}[t_{FF}.|G_{FF1}|.t_{FF} + t_{FN}.(G_{NN1}.t_{NN} + |G_{FF1}|.t_{FF})]. \end{aligned} \tag{C.8}$$

At CCM/DCM boundary, $t_{FF} = (1-D_2)$, the boundary values of load current and duty ratios are given by–

$$i_{o1bd} = \frac{T_s}{2}\left[t_{NN}(D_2 - t_{NN})G_{NN1} + (1-D_2)(1-t_{NN})|G_{FF1}|\right]$$
$$\text{where, } t_{NN} = \frac{D_2|G_{FN1}| + (1-D_2)|G_{FF1}|}{G_{NN1} + G_{FN1}}. \tag{C.9}$$
$$D_1 = t_{NN}$$

Therefore, i_{L1} remains in Mode 4a when $i_{o14b} < i_{o1} < i_{o1bd}$ and $D_{1_{4b}} < D_1 < t_{NN}$.



(a) Mode 4a (b) Mode 5a (c) Mode 7a (d) Mode 8a

Figure C.5: The theoretical waveforms of g_1, g_2, i_{L1}, i_{L2}, when operating in Mode 4a, 5a, 7a and 8a of CI-SIDO boost converter.

C.1.3.2 Modes 4b, 5b, 7b and 8b

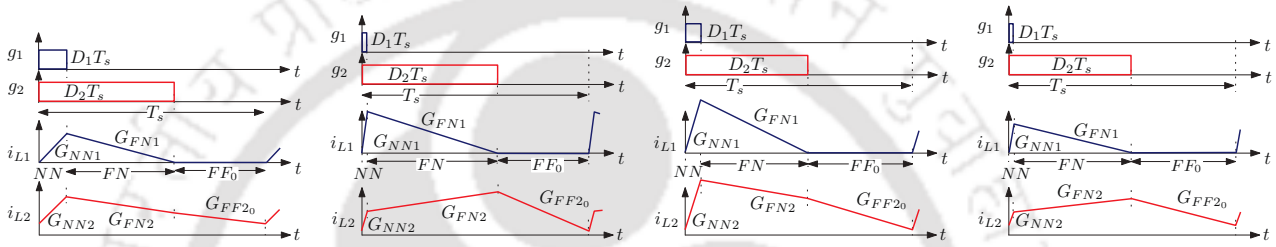
The waveforms of Modes 4b, 5b, 7b and 8b are shown in Figs. C.6(a), C.6(b), C.6(c) and C.6(d) respectively.

$$t_{NN} + t_{FN} = D_2$$
$$t_{FF} = (1-D_2)$$
$$G_{NN1}t_{NN} = G_{FN1}t_{FN}$$
$$t_{NN} = \frac{G_{FN1}t_{FN}}{G_{NN1}} \tag{C.10}$$
$$t_{FN}\{1 + \frac{G_{FN1}}{G_{NN1}}\} = D_2$$
$$i_{o1} = \frac{T_s}{2}[t_{FN}.G_{NN1}.t_{NN}].$$

Finding the values of $i_{o1} = i_{o14b}$ and $D_1 = D_{1_{4b}}$ for Mode 4b, we obtain–

$$\begin{aligned} i_{o14b} &= \frac{|G_{FN1}|G_{NN1}^2 D_2^2 T_s}{2(G_{NN1} + |G_{FN1}|)^2}, \\ D_{1_{4b}} &= \frac{D_2 G_{FN1}}{G_{NN1} + G_{FN1}}. \end{aligned} \tag{C.11}$$

At $i_{o1} = i_{o14b}$ and $D_1 = D_{1_{4b}}$, the converter is at Mode 4b. After that if $i_{o1} < i_{o14b}$ and $D_1 < D_{1_{4b}}$, the converter operates in Mode 4c.



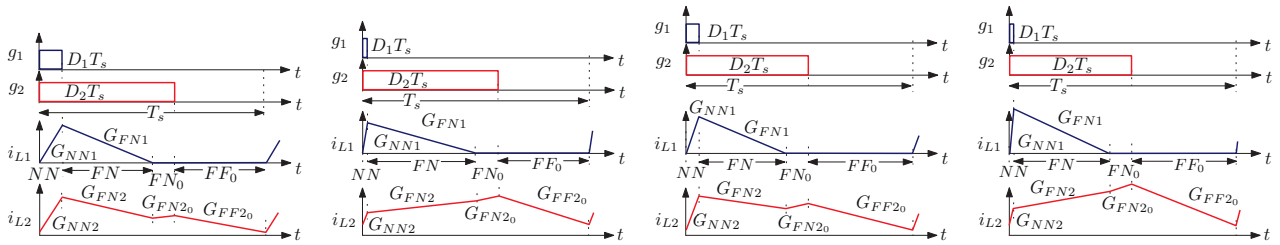
(a) Mode 4b (b) Mode 5b (c) Mode 7b (d) Mode 8b

Figure C.6: The theoretical waveforms of g_1, g_2, i_{L1}, i_{L2}, when operating in Mode 4b, 5b, 7b and 8b of CI-SIDO boost converter.

C.1.3.3 Modes 4c, 5c, 7c and 8c

The waveforms of Modes 4c, 5c, 7c and 8c are shown in Figs. C.7(a), C.7(b), C.7(c) and C.7(d) respectively.

$$\begin{aligned} t_{NN} + t_{FN} &= D_2 - t_{FN_0} \\ t_{FF_0} &= (1 - D_2) \\ G_{NN1} t_{NN} &= G_{FN1} t_{FN} \\ t_{NN} &= \frac{G_{FN1} t_{FN}}{G_{NN1}} \\ t_{FN}\{1 + \frac{G_{FN1}}{G_{NN1}}\} &= D_2 - t_{FN_0} \\ i_{o1} &= \frac{T_s}{2}[t_{FN}.G_{NN1}.t_{NN}]. \end{aligned} \tag{C.12}$$



(a) Mode 4c (b) Mode 5c (c) Mode 7c (d) Mode 8c

Figure C.7: The theoretical waveforms of g_1, g_2, i_{L1}, i_{L2}, when operating in Mode 4c, 5c, 7c and 8c of CI-SIDO boost converter.

C.1.4 Sector 6 and 9

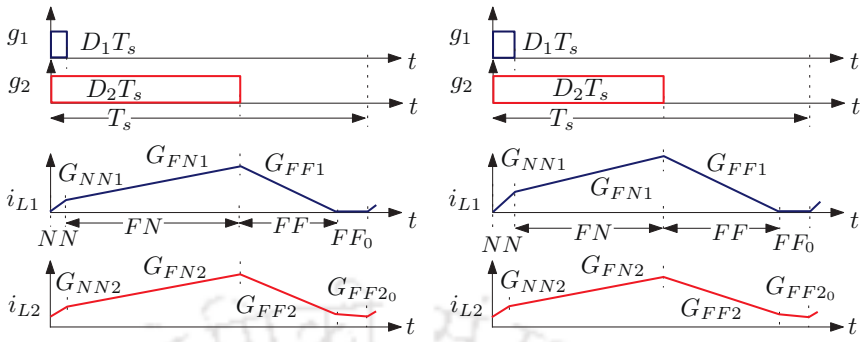
The waveforms of Modes 6 and 9 are shown in Figs. C.8(a), and C.8(b) respectively.

$$\begin{aligned} t_{NN} + t_{FN} &= D_2 \\ t_{FN} &= D_2 - t_{NN} \\ G_{NN1}t_{NN} + G_{FN1}t_{FN} &= |G_{FF1}|t_{FF} \\ (G_{NN1} - G_{FN1})t_{NN} &= |G_{FF1}|t_{FF} - G_{FN1}D_2 \\ t_{NN} &= \frac{|G_{FF1}|t_{FF} - G_{FN1}D_2}{(G_{NN1} - G_{FN1})} \\ i_{o1} &= \frac{T_s}{2}[t_{FF}.|G_{FF1}|.t_{FF} + t_{FN}.(G_{NN1}.t_{NN} + |G_{FF1}|.t_{FF})]. \end{aligned} \tag{C.13}$$

At CCM/DCM boundary, $t_{FF} = (1 - D_2)$. Therefore, the boundary load current and duty ratio reduces to–

$$\begin{aligned} i_{o1bd} &= \frac{T_s}{2}\,[t_{NN}(D_2 - t_{NN})G_{NN1} + (1 - D_2)(1 - t_{NN})|G_{FF1}|] \\ \text{where, } t_{NN} &= \frac{|G_{FF1}|(1 - D_2) - G_{FN1}D_2}{(G_{NN1} - G_{FN1})}. \\ D_{1_{bd}} &= t_{NN}. \end{aligned} \tag{C.14}$$

Therefore, to operate the converter in Sector 6 and 9, $i_{o1} < i_{o1bd}$ and $D_1 < D_{1_{bd}}$.



(a) Mode 6 (b) Mode 9

Figure C.8: The theoretical waveforms of g_1, g_2, i_{L1}, i_{L2}, when operating in Sector 6 and 9 of CI-SIDO boost converter.

D

PCB Design of CI-SIDO Converters and Pulse Generation in LabView FPGA

D.1 PCB Design of CI-SIDO Converters

The PCB design of CI-SIDO boost converter is presented in Fig. D.1. The MOSFETs used are IRFP90N20DPBF and diodes used are RHRP30120. The gate driver used are HCPL-3120.

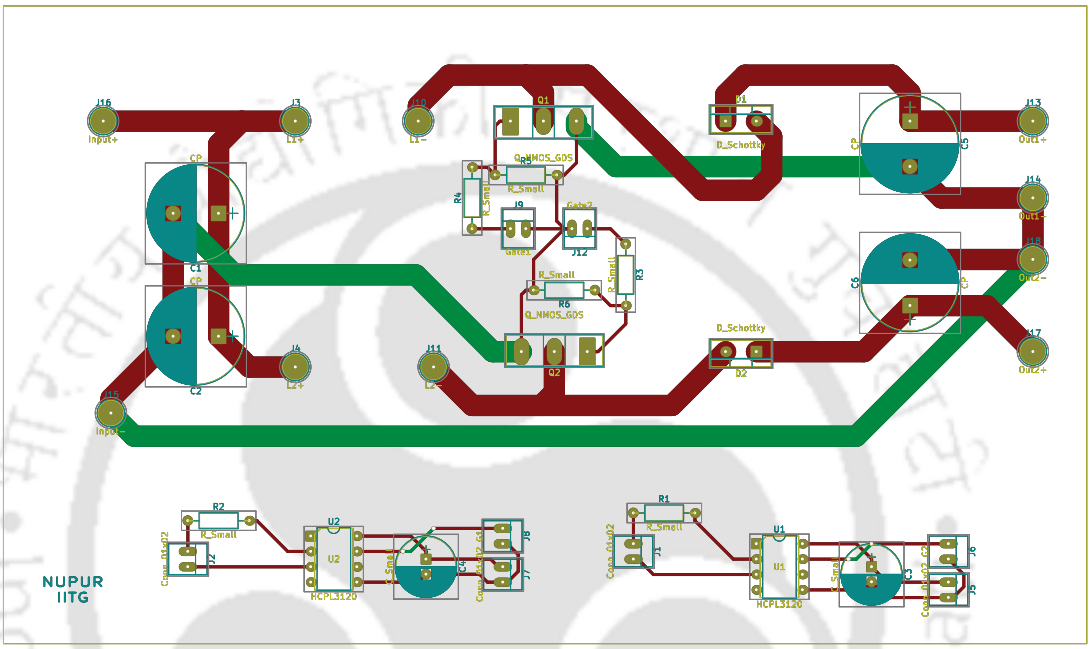


Figure D.1: PCB board of CI-SIDO boost converter.

D.2 Pulse Generation in LabView FPGA

The pulse is generated by NI single board RIO 9636, programmed in LabView. The second pulse is started at a delay from the starting point of the first pulse. This delay is the D_t which is changed from 0 to 1. The screen shot of the code is shown in Figs. D.2 and D.3.

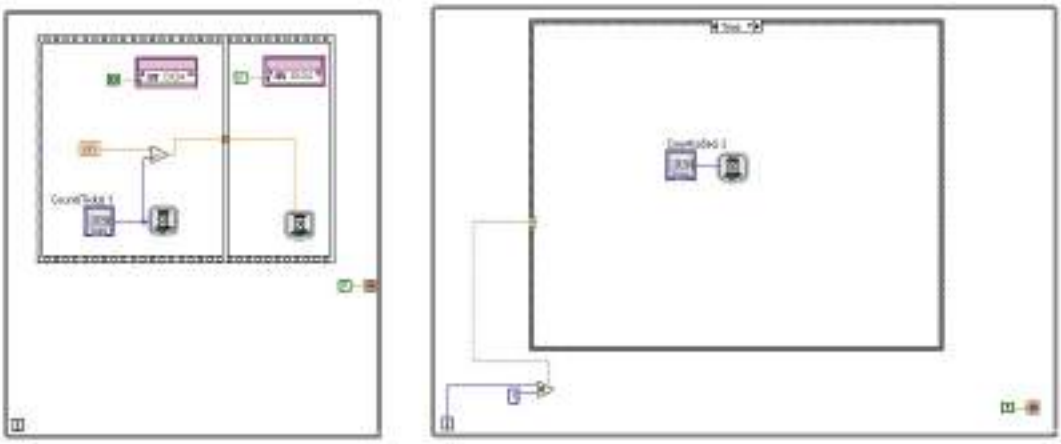


Figure D.2: Screenshot for pulse generation when the delay is given to g_2.

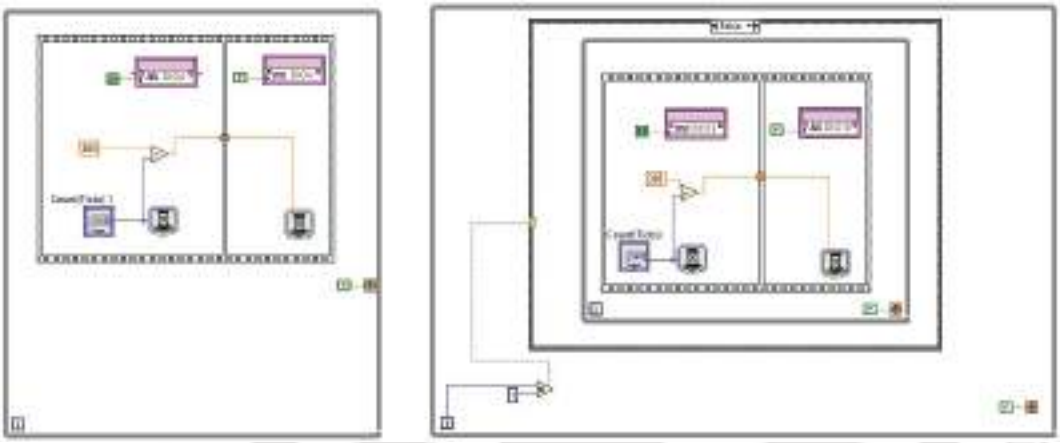


Figure D.3: Screenshot for pulse generation after the delay is given.

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List of Publications

Journals

1. **Nupur** and S. Nath, "Dependence of CCM/DCM Boundary on Gate Pulse Shift in Coupled SIDO Boost Converter," accepted in *IEEE Trans. Transport. Electrific.*

2. **Nupur** and S. Nath,"Effect of Coupling on Discontinuous Conduction Mode of Coupled Inductor SIDO Boost Converter" in *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 4991-5002, May 2022.

3. **Nupur** and S. Nath, "Minimizing Ripples of Inductor Currents in Coupled SIDO Boost Converter by Shift of Gate Pulses," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1217-1226, Feb. 2020.

4. **Nupur** and S. Nath, "Unifying Inductor Current Ripples and Inductor Design in Coupled SIDO Converters by Forming Sectors of Duty Ratios," in *IEEE Trans. Ind. Appl.*, vol. 58, no. 3, pp. 3830-3839, May-Jun. 2022.

5. **Nupur** and S. Nath, "Achieving Approximately Zero Ripples in Input Current of Coupled SIDO Boost Converter," in *IEEE Trans. Ind. Appl.*, vol. 58, no. 3, pp. 3819-3829, May-Jun. 2022.

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