INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI
SHORT ABSTRACT OF THESIS

Name of the Student	:	PRAMIT NANDI
Roll Number	:	166102001
Programme of Study	:	Ph.D.

Thesis Title: Low-frequency ripple analysis and mitigation of Single-Phase Switched Boost Inverter and Reduced-Switch Current-Fed Switched Inverter

Name of Thesis Supervisor(s)	:	DR. RAVINDRANATH ADDA
Thesis Submitted to the Department/ Center	:	EEE
Date of completion of Thesis Viva-Voce Exam	:	20/03/2024
Key words for description of Thesis Work	:	Low-frequency ripple mitigation, single-phase inverter, switched boost inverter, reduced-switch current-fed switched inverter.

SHORT ABSTRACT

Active-Front-End Impedance Source Inverters (AFE-ISIs), viz., switched boost inverter (SBI), current-fed switched inverter (CFSI), etc., are explored in literature as alternatives to the conventional voltage source inverter (VSI) in low power applications. They are more reliable against EMI noise and better protected against unintentional shorting of legs. Also, they can operate in both buck and boost modes, providing a wide range of operations. This thesis proposes a new AFE-ISI topology, named reduced-switch current-fed switched inverter (RSCFSI), which can provide improved voltage gain, continuous input current, and better efficiency than SBI. The derivation and steady-state analysis of RSCFSI are explained in detail. This thesis also proposes two PWM strategies for RSCFSI.

Furthermore, this thesis explores the low-frequency ripple problem that plagues single-phase AFE-ISIs. This problem affects the dc-side passive elements and distorts the inverter's output voltage. The conventional solution is the employment of bulky inductors and less reliable electrolytic capacitors, but this solution affects overall system power density, cost, efficiency, and reliability. As a solution to the low-frequency problem of SBI and RSCFSI, this thesis proposes the integration of the active power decoupling topologies with SBI and RSCFSI. The mitigation of low-frequency ripple helps reduce the size of the passive elements and facilitates the use of more reliable film capacitors, which also improves the overall lifetime of the inverters. The proposed topologies are validated using detailed experimental results.