

Abstract

In future communication systems, the requirement is not only for improving the quality of service but also towards finding an integrated solution for all the existing standards. Consequently, the coming generation RF system-on-chips (SOCs) must have the ability to cover a wide range of spectrum for different applications without much relaxation in their energy consumption. The transceiver SOCs may require multiple LNAs (low-noise amplifier), a key component of the receiver, where the LNA count increases almost proportionally with the number of supporting bands. Further, added diversity features incorporated in applications like LTE (Long Term Evolution) may use techniques such as massive MIMO (Multiple Input Multiple Output) that increase the hardware (the number of LNAs) requirement compared to earlier single input and single output (SISO) systems. Moreover, LNAs are one of the major power consuming blocks in a receiver. One must therefore design an LNA to operate at as low a power as possible while maintaining the minimum noise performance and acceptable linearity requirement. The scope of this research is motivated by the implementation challenges of low power, low noise amplifiers, particularly in sub-nanometer technology.

The LNA exhibits three key issues when it is designed for low power conditions in sub-nanometer technological nodes. Firstly, reliability becomes a major concern in sub nanometer technology nodes. The performance parameters undergo large deviations when circuits are subjected to unavoidable PVT (process-voltage-temperature) variations. These demand development of compensation circuits to improve the reliability of the amplifier. Secondly, the performance parameters such as gain and noise undergo degradation. Therefore, topological modifications to the conventional techniques are necessary to enhance the performances when they are operating under low power conditions. Thirdly, circuit integration along with passive elements becomes unrealizable through conventional implementations in advanced technology nodes (like 65nm or below), particularly for low noise amplifiers.

To begin with, the initial approach to address these issues involved a thorough investigation of an MOS device performance in Strong, Moderate, and Weak inversion (SI, MI, WI) regions. It is explored in this thesis whether LNA devices operating in MI offer a better noise-power trade-off as compared to the conventional SI regions implementations. In addition, it is explored whether full system integration is always the viable option for low power circuit implementation. Further, the suitability of implementing sub-mW powered LNA is also investigated for applications like LTE by deducing the system level requirement from the specifications of the LTE standard.

Coming to the reliability issue, effective compensation circuits based on simple current comparison techniques are introduced to nullify the PVT variations and to improve the reliability of the amplifier. In addition to the realization of compensation mechanisms, a novel low voltage constant current reference (CCR) based on beta multiplier is introduced in this thesis. Finally, a gain enhancement technique based on the current-reuse topology is introduced to balance the degradation due to the low power operating conditions. Overall, this thesis has introduced circuit techniques along with an investigative study for improving the performance of low-power low-noise amplifiers.