Voltage and Current Mode Controls of Coupled Inductor Single Input Dual Output DC-DC Converters

A

Thesis Submitted

in Partial Fulfilment of the Requirements

for the Degree of

DOCTOR OF PHILOSOPHY

By

Gayatri Nayak

Department of Electronics and Electrical Engineering

Indian Institute of Technology Guwahati

Guwahati - 781 039, India

March 2021

Certificate

This is to certify that the thesis entitled "**Voltage and Current Mode Controls of Coupled Inductor Single Input Dual Output DC-DC Converters**", submitted by **Gayatri Nayak**, a research scholar in the *Department of Electronics and Electrical Engineering, Indian Institute of Technology Guwahati*, for the award of the degree of **Doctor of Philosophy**, is a record of an original research work carried out by him under my supervision and guidance. The thesis has fulfilled all requirements as per the regulations of the institute and has reached the standard needed for submission. The results embodied in this thesis have not been submitted to any other University or Institute for the award of any degree or diploma.

Dated:

Guwahati.

Dr. Shabari Nath
Assistant Professor
Dept. of Electronics and Electrical Engg.
Indian Institute of Technology Guwahati
Guwahati - 781 039, Assam, India.

To my family...

Acknowledgement

First, I would like to extend heartfelt gratitude to my thesis supervisor Dr. Shabari Nath. Her constant motivation, support and excellent guidance gave me much needed strength during this fruitful journey. I am extremely grateful to her for her time and guidance. Without these, my thesis would not have reached the current form.

I also thank my doctoral committee members Prof. Ratnajit Bhattacharjee, Dr. Praveen Tripathy, Dr. Ravindranath Adda for their constructive and constant monitoring of my thesis work and suggestions which were immensely helpful for enhancing the quality of my thesis and assuring timely completion of targets. I would also like to thank the previous and current Head of the Department, other faculty members, technical staff and lab assistants for their immeasurable support during this journey. I would specially like to acknowledge Mr. Rakesh Singha and Mr. Paban Bujor Barua whose help in procuring necessary materials and ensuring smooth operation of the Power Electronics Laboratory went a long way to ensure successful completion of experiments essential for my thesis.

My journey would not be complete without the support of my parents, parents-in-law, sister Santoshi Nayak and brothers Srikant Nayak, Prashant Nayak who have been the guiding light of my life. My strongest pillar of support during this journey has been my husband Abhishek Mahapatra to whom any amount of thanks wouldn't be enough.

No course is complete without the quintessential friends and colleagues who are the part and parcel of the day to day research life. I am grateful to them for endless beautiful memories and support. Vivek Joshi, Rajdib Dey, Nishant Anurag, Archit Joshi, Pramit Nandi, Gautam Sethia, Tarique Sayeed Khan, Abhishek Paikray, Sourav kumar Ghosh, Amit Kumar Baghel, Kamakshi Manjari, Tako Nama, Sumi Phukan, Protima Nama Sudro are the people I would like to thank the most. Apart from this anyone not mentioned by name here but has been a part of my research journey deserves my heartfelt thanks and gratitude.

Finally, I am grateful to the God Almighty without whom my life would be unimaginable let alone the research journey.

Gayatri Nayak

Abstract

Applications like electric vehicle, LED drivers, and portable devices are moving towards miniaturization. The power management unit of these applications operating from single voltage source demand better efficiency, compactness, longer battery life and regulated voltages. To achieve these requirements many single-input multiple-output (SIMO) DC-DC converters have been proposed in the literature. This research work focuses on coupled inductor single-input dual-output (CI-SIDO) converters. The CI-SIDO converter utilizes coupled inductors on one magnetic core and hence reduces the number of magnetic components. The use of an inversely coupled inductor offers benefits of reduced current ripple and improved efficiency. However, due to the coupling of inductor currents, the outputs are coupled and CI-SIDO converters suffer from cross-coupling and cross-regulation problems. These issues affect the converter performance and stability. Thus, designing an appropriate control technique is a fundamental challenge for achieving desired performance and stability. Hence converter dynamics need to be analyzed and predicted accurately.

The dynamics of CI-SIDO converters are analyzed by developing the small-signal model using the state-space averaging method. It is inferred that the steady-state behaviour of CI-SIDO converters is the same as that of single-input single-output (SISO) dc-dc converters. However, the CI-SIDO converter's dynamic characteristic is affected by choice of the coefficient of coupling k. The derived small-signal transfer functions reveal that complex poles and zeros of the converter, cross-coupling and cross-regulation are affected by choice of k. As a result, with tight coupling (high value of k), the converter leads to instability with sever cross-coupling and

cross-regulation effects. Therefore, the moderate coupling is preferred for CI-SIDO converters.

For CI-SIDO converters, achieving independent regulation of output voltages and maintaining good dynamic performance are difficult due to cross-regulation and cross-coupling problems. Therefore, this thesis proposes a decoupled voltage mode control (VMC) and decoupled average current mode (ACC) control for CI-SIDO buck converter to address the issues of cross-coupling. The proposed decoupled method ensures good dynamic performance and is validated using experimental and simulation results.

To further suppress the cross-regulation, peak current mode (PCM) control is introduced for CI-SIDO converter in this thesis. Compared to the conventional PCM control of SISO converter, the PCM control of CI-SIDO converter has more complex structure and stability issues. Therefore, a unified small-signal model is developed for PCM controlled CI-SIDO converter to predict the instability and dynamic characteristics. Moreover, using the unified small-signal model, the design procedure for slope-compensation and controller is proposed for PCM controlled CI-SIDO buck converter. The proposed PCM control suppresses the cross-regulation, cross-coupling of the CI-SIDO buck converter with good dynamic performance and is verified through simulation and experimental results.

Contents

List of Figures

List of Tables

List of Common Abbreviations

ACC	Average Current Control
CCM	Continuous Conduction Mode
CI-SIDO	Coupled Inductor Single Input Dual Output
CI-SIMO	Coupled Inductor Single Input Multiple Output
DCM	Discontinuous Conduction Mode
ESR	Effective Series Resistances
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
PCCM	Pseudo-Continuous Conduction Mode
PCM	Peak Current Mode Control
PMU	Power Management Unit
PWM	Pulse Width Modulation
SIDO	Single Input Dual Output
SIMO	Single Input Multiple Output
SISO	Single Input Single Output
SI-SIDO	Single Inductor Single Input Dual Output
SI-SIMO	Single Inductor Single Input Multiple Output
VMC	Volateg Mode Control

List of Symbols

L_1, L_2	Self inductances
M	Mutual inductance
k	Coefficient of coupling
C_1, C_2	Output capacitors
R_1, R_2	Load resistances
S_{T1}, S_{T2}	Power electronic switches
S_{D1}, S_{D2}	Diodes
r_{c1}, r_{c2}	Effective series resistance (ESR) of capacitors
$v_{in}(t)$	Instantaneous input voltage
v_{in}	Input voltage averaged over switching time period
V_{in}	DC value of input voltage
$\hat{v}_{in}$	Perturbation/ disturbance in input voltage
$v_{01}(t), v_{02}(t)$	Instantaneous output voltages
v_{01}, v_{02}	Output voltages averaged over switching time period
V_{01}, V_{02}	DC value of output voltages
$\hat{v}_{01}, \hat{v}_{02}$	Perturbation in output voltages
$v_{C1}(t), v_{C2}(t)$	Instantaneous capacitor voltages
v_{C1}, v_{C2}	Capacitor voltages averaged over switching time period
V_{C1}, V_{C2}	DC value of capacitor voltages
$\hat{v}_{C1}, \hat{v}_{C2}$	Perturbation in capacitor voltages
$i_{L1}(t), i_{L2}(t)$	Instantaneous inductor currents
i_{L1}, i_{L2}	Inductor currents averaged over switching time period

I_{L1}, I_{L2}	DC value of inductor currents
$\hat{i}_{L1}, \hat{i}_{L2}$	Perturbation in inductor currents
$i_{01}(t), i_{02}(t)$	Instantaneous load currents
i_{01}, i_{02}	Load currents averaged over switching time period
I_{01}, I_{02}	DC value of load currents
$\hat{i}_{01}, \hat{i}_{02}$	Perturbation in load currents
$i_{C1}(t), i_{C2}(t)$	Instantaneous capacitor currents
i_{C1}, i_{C2}	Capacitor currents averaged over switching time period
$\hat{i}_{C1}, \hat{i}_{C2}$	Perturbation in capacitor currents
g_{T1}, g_{T2}	gate pulse signal to switch S_{T1}, S_{T2}
d_1, d_2	duty cycles
D_1, D_2	DC value of Duty cycles
$\hat{d}_1, \hat{d}_2$	Perturbation in duty cycles
f_s	Switching frequency
T_s	Switching period
v_{ramp}	Ramp signal
V_m	Peak voltage of external ramp signal
v_{f1}, v_{f2}	Feedback voltage signals
$\hat{v}_{f1}, \hat{v}_{f2}$	Perturbation in feedback voltage signals
v_{e1}, v_{e2}	Error signals
$\hat{v}_{e1}, \hat{v}_{e2}$	Perturbation in error signals
v_{cn1}, v_{cn2}	Reference control signal generated by voltage controller
$\hat{v}_{cn1}, \hat{v}_{cn2}$	Perturbation in reference control signal
v_{d1}, v_{d2}	Control signal generated by inner current controller
$\hat{v}_{d1}, \hat{v}_{d2}$	Perturbation in v_{d1}, v_{d2}
V_{ref1}, V_{ref2}	DC Reference voltages
$\hat{v}_{ref1}, \hat{v}_{ref2}$	Perturbation in reference voltages
$\mathbf{A}$	Dynamic transmission matrix

$\mathbf{B}$	Input transmission matrix
$\mathbf{C}$	Output transmission matrix
$\mathbf{D}$	Direct transmission matrix
$\mathbf{x}(t)$	Instantaneous state space variable vector $[i_{L1}(t)\ v_{C1}(t)\ i_{L2}(t)\ v_{C2}(t)]^T$
$\mathbf{x}$	State-space variable vector averaged over switching time period $[i_{L1}\ v_{C1}\ i_{L2}\ v_{C2}]^T$
$\mathbf{X}$	DC value of state variable vector $[I_{L1}\ V_{C1}\ I_{L2}\ V_{C2}]^T$
$\hat{\mathbf{x}}$	perturbation in state variable vector $[\hat{i}_{L1}\ \hat{v}_{C1}\ \hat{i}_{L2}\ \hat{v}_{C2}]^T$
$\mathbf{y}(t)$	Instantaneous output variable vector $[v_{01}(t)\ v_{02}(t)]^T$
$\mathbf{y}$	Output variable vector averaged over switching time period $[v_{01}\ v_{02}]^T$
$\mathbf{Y}$	DC value of output variable vector $[V_{01}\ V_{02}]^T$
$\hat{\mathbf{y}}$	perturbation in output variable vector $[\hat{v}_{01}\ \hat{v}_{02}]^T$
$\mathbf{u}(t)$	Instantaneous input variable vector $[v_{in}(t)\ i_{01}(t)\ i_{02}(t)]^T$
$\mathbf{u}$	Input variable vector averaged over switching time period $[v_{in}\ i_{01}\ i_{02}]^T$
$\mathbf{U}$	DC value of input variable vector $[V_{in}\ I_{01}\ I_{02}]^T$
$\hat{\mathbf{u}}$	perturbation in input variable vector $[\hat{v}_{in}\ \hat{i}_{01}\ \hat{i}_{02}]^T$
$G_{id11},\ G_{id22}$	Duty cycle to inductor current transfer functions
$G_{id12},\ G_{id21}$	Cross-coupling transfer functions between duty cycle and inductor current
$G_{vd11},\ G_{vd22}$	Duty cycle to output voltage transfer functions
$G_{vd12},\ G_{vd21}$	Cross-coupling transfer functions between duty cycle and output voltage
$Z_{vi11},\ Z_{vi22}$	Self-regulation transfer functions
$Z_{vi12},\ Z_{vi21}$	Cross-regulation transfer functions
$H_{ii11},\ H_{ii22}$	Load current to inductor current transfer functions
$H_{ii12},\ H_{ii21}$	Cross-coupling transfer functions between load current to inductor current
$G_{vg1},\ G_{vg2}$	Audio susceptibility transfer functions
$G_{ig1},\ G_{ig2}$	Input voltage to inductor current transfer functions
$G_{id1},\ G_{id2}$	Approximated duty cycle to inductor current transfer functions
$G_{vd1},\ G_{vd2}$	Approximated duty cycle to output voltage transfer functions
$G_{c1},\ G_{c2}$	Current Controller transfer functions

$G_{v1},\ G_{v2}$	Voltage Controller transfer functions
$\beta_1,\ \beta_2$	Feedback gains
$G_{m1},\ G_{m2}$	Pulse width modulator (PWM) transfer functions
$r_{s1},\ r_{s2}$	Current sensing resistances
$T'_{i1},\ T'_{i2}$	Actual inner current loop gain transfer functions
$T_{i1},\ T_{i2}$	Approximated inner current loop gain transfer functions
$T'_1,\ T'_2$	Actual outer loop gain trnasfer functions
$T_1,\ T_2$	Approximated outer loop gain transfer functions
$T_{v1},\ T_{v2}$	Approximated voltage loop gain transfer functions
PM	Phase margin
$\omega_{p1},\ \omega_{p2}$	Frequency of complex poles
$\omega_{z1},\ \omega_{z2}$	Frequency of complex zeros
$\omega_{esr1},\ \omega_{esr2}$	Frequency of ESR zero
$\omega_{rhz1},\ \omega_{rhz2}$	Frequency of right half plane zero
$Q_{p1},\ Q_{p2}$	Quality factor of complex poles $w_{p1},\ w_{p2}$
$Q_{z1},\ Q_{z2}$	Quality factor of complex zeros $w_{z1},\ w_{z2}$
k_{c1}, k_{c2}	Controllers gain
$\omega_{c1-z}, \omega_{c2-z}$	Controllers zero frequency
$\omega_{c1-p},\ \omega_{c2-p}$	Controllers pole frequency
$\omega_{c1},\ \omega_{c2}$	Crossover frequency of outer loop gains
$\omega_{ci1},\ \omega_{ci2}$	Crossover frequency of inner current loop gains
$m_{c1},\ m_{c2}$	Slope compensations
Z'_{vi11cl}, Z'_{vi22cl}	Closed loop actual self-regulation transfer functions
Z'_{vi12cl}, Z'_{vi21cl}	Closed loop actual cross-regulation transfer functions
G'_{vg1cl}, G'_{vg2cl}	Closed loop actual audio susceptibility transfer functions
Z_{vi11cl}, Z_{vi22cl}	Closed loop approximated self-regulation transfer functions
Z_{vi12cl}, Z_{vi21cl}	Closed loop approximated cross-regulation transfer functions
G_{vg1cl}, G_{vg2cl}	Closed loop approximated audio susceptibility transfer functions

1

Introduction

Contents

1.1 Introduction

The rapid growth of electric vehicles and portable devices like mobile phones, Laptops, MP3 players, wireless sensor, etc., is promoting extensive research in their design [3, 4]. The implementation of numerous features in electric vehicles and portable devices necessitates the use of multiple voltage supplies with varying voltage levels, which in turn are supplied by a single rechargeable battery like a Lithium-ion battery or silver-zinc battery. Figure 1.1(a) and Figure 1.1(b) show the block diagram of today's EVs and portable devices, respectively. As illustrated in Figure 1.1(a), each sub-module of EVs, like USB, CD player, rain wiper, air conditioner, lighting system, provides various functionalities and may generally require multiple supplies to operate. Similarly, as illustrated in Figure 1.1(b), each sub-module of the portable device, like a modem, a GPS module, a Bluetooth module, an application processor, a memory subsystem, etc., requires multiple supplies to function. The power management unit (PMU) of EVs and portable devices provide the different regulated voltages to the numerous sub-modules from single source. The power management unit (PMU) uses buck converters to step-down, boost converters to step-up, buck-boost converter to generate negative voltage and linear regulators to meet the different load requirements.

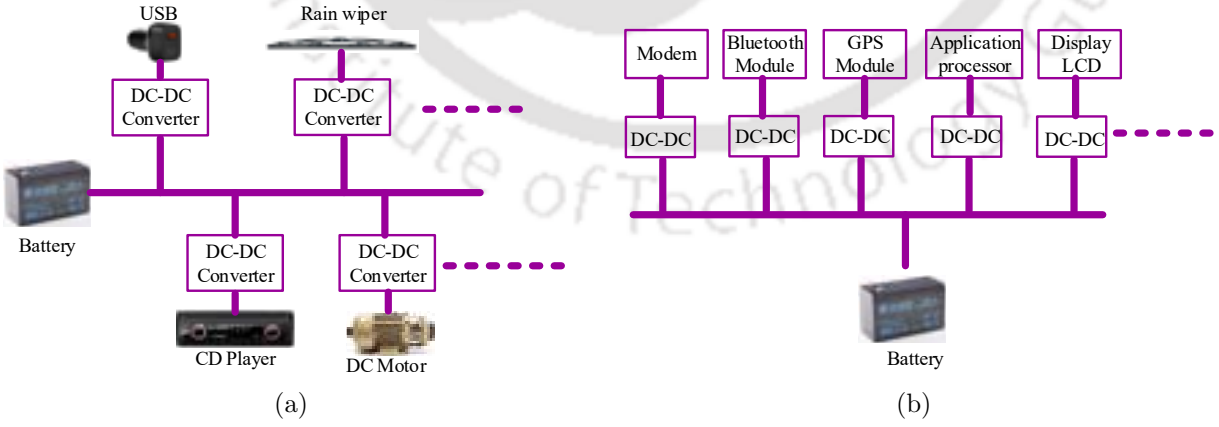


Figure 1.1: Block diagram of power management unit of today's EV and portable devices (a) Electric vehicle (EV) (b) Portable devices

The conventional implementation of PMU in EVs and portable devices as shown in Figure 1.1 consists of multiple parallel DC-DC converters for the generation of non-isolated voltage

supplies. The applications where isolation is required employ a flyback or forward converter with multiple secondary windings to generate multiple outputs [5], [6]. The first approach requires many power devices, inductors and controllers, which leads to increased size, cost and reduced efficiency. The second approach has a significant limitation on output voltage scaling and does not ensure independent control of output voltages [7], [8], [9].

In the present scenario, the main requirement of PMU in these systems is to achieve better voltage regulation, higher efficiency, longer battery life and at the same time, compact size and low cost. Therefore, to meet miniaturization, compactness, lower cost, and better efficiency, many single-input multiple-output (SIMO) converter topologies have been extensively proposed and studied in recent research. The SIMO converter topologies eliminate many issues of multiple parallel dc-dc converters. The SIMO topologies allow reduced use of bulky components such as inductors, power devices which significantly save the overall weight, volume and cost.

1.2 Review of Single Input Multiple Output (SIMO) Converters

As discussed in the previous section, SIMO converters serve as a good replacement to multiple DC-DC converters due to the many advantages like reduced cost, size and higher efficiency. However, SIMO converter topologies present some disadvantages [10]. The main problem of SIMO converter topologies is cross-coupling and cross-regulation. The variation in load current of one output affecting the other output voltages is defined as cross-regulation as shown in Figure 1.2(a). The variation in reference voltage of one output affecting the other output voltages is defined as cross-coupling as shown in Figure 1.2(b). These issues affect the system performance and stability in both the steady-state and dynamic state. Moreover, due to cross-coupling and cross-regulation, the SIMO converter operation, design and control are quite complex compared to the conventional single output DC-DC converter.

Extensive research has been carried out in the recent literature on the synthesis of SIMO converter topologies and the implementation of improved control techniques to overcome the problems of SIMO converter. For the SIMO converter, both isolated and non-isolated topologies

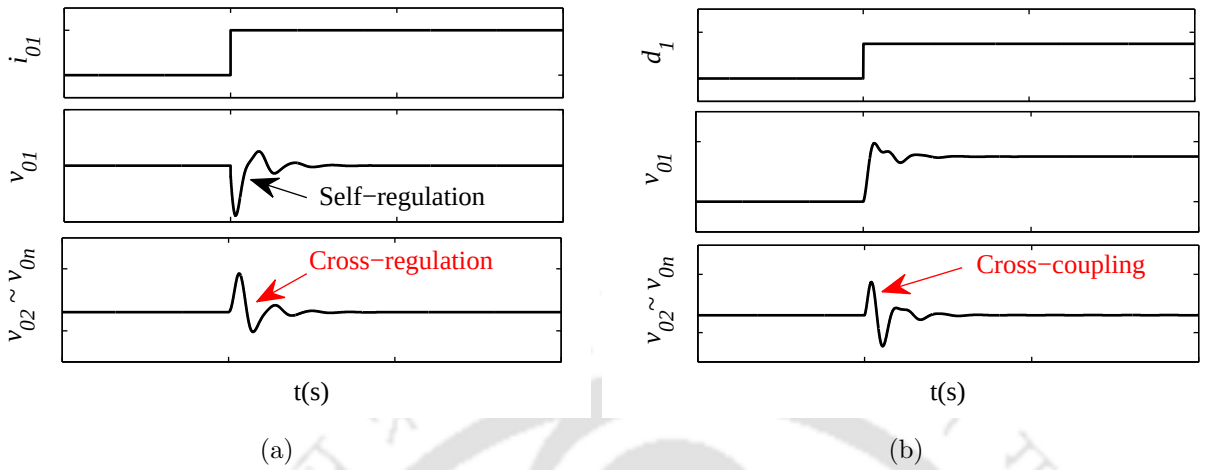


Figure 1.2: Cross-regulation and cross-coupling effect in SIMO converter (a) Cross-regulation (b) Cross-coupling

are available in the literature. The non-isolated topologies can be further classified based on the type of inductor configuration: (i) Single inductor SIMO (SI-SIMO) converter, which is capable of generating multiple outputs by sharing only one single inductor. (ii) Integrated SIMO converter, which is capable of generating multiple outputs with the reduced number of switches and integrated inductor. (iii) Coupled inductor SIMO converter, which is capable of generating multiple outputs by sharing one coupled inductor.

1.2.1 Single Inductor SIMO Converters

Many single inductor SIMO (SI-SIMO) converter topologies have been proposed in literature based on buck derived topologies [1, 11–13], boost derived topologies [14–17] and buck-boost derived topologies [18–20]. Moreover, there are many SIMO converter topologies which are capable of generating buck and/or boost outputs simultaneously [21], inverted output along with buck, boost output [22]. Figure 1.3 shows the circuit configuration of SI-SIMO buck converter. The main attraction of an SI-SIMO converter lies in the fact that the converter can provide multiple regulated output voltages with relatively small size and low cost.

In spite of its advantages, a SIMO converter suffers cross-coupling and cross-regulation problems among the output voltages when operated in continuous conduction mode (CCM) [10].

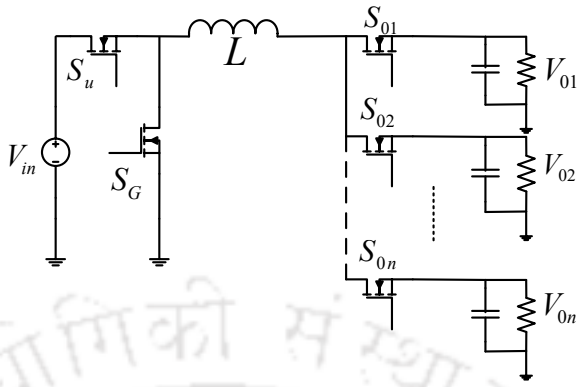


Figure 1.3: Single inductor single input multiple output (SI-SIMO) buck converter [1]

Several improved control methods have been proposed for SI-SIMO converters to alleviate the cross-coupling and cross-regulation problems. The proposed methods are mainly based on the operating condition of SI-SIMO converters, i.e., discontinuous conduction mode (DCM), pseudo-continuous conduction mode (PCCM), and continuous conduction mode (CCM).

Time-multiplexing switching scheme is proposed to operate the SI-SIMO converter in DCM [23–25]. Here, each switching interval is divided into n sub-intervals (for n outputs) and operated individually. This suppresses the cross-regulation but results in a large current ripple at heavy load conditions and cannot be performed at heavy load. A freewheel switching scheme is proposed to operate the SI-SIMO converter in PCCM [26–29]. In this method, an additional switch is installed across the inductor to freewheel the inductor current, which results in increased cost and conduction losses. The SI-SIMO converter operated in DCM or PCCM faces the issues of large current ripple, low current capability and low efficiency. Therefore, an SI-SIMO converter operated in CCM is preferred if cross-regulation among the output voltages can be suppressed.

In literature, several voltage-mode and current-mode control methods, including both digital and analog implementation, have been proposed for SI-SIMO converter operating in CCM to suppress the cross-regulation problem. A comparator based control method is proposed in [30–32] for SI-SIMO converter to regulate the output voltages with fast transient response and low cross-regulation. However, in light load condition, the converter faces issues like regu-

lation instability and low efficiency. A voltage mode control based on decoupling procedure is proposed in [33] to regulate the output voltages of SI-SIDO buck converter. A cross-derivative state feedback control method is proposed [34] to reduce the cross-regulation problem in single inductor single input dual output (SI-SIDO) buck converter. In this method, a cross-loop compensation network is designed to reduce the cross-regulation. But, other performance parameters like audio-susceptibility, cross-coupling have not been considered. A multi-variable control technique is proposed in [35] to suppress the cross-regulation in SI-SIDO buck converter. In this method H_∞ theory is used to design controllers. However, to meet the design requirements, it requires multiple operating points with circuit variations. In [36–40], several digital control techniques have been conducted in SI-SIDO buck converter to suppress the cross-regulation problem. In [36], digital control with phase sequence interchange scheme is proposed. In [37], a digital control based on differential-mode and common-mode output voltages is proposed to suppress cross-regulation. In [38], [39], predictive voltage control and model predictive current control are proposed respectively which generate duty cycles as per low cross-regulation. In [40], deadbeat control technique is proposed for independent regulation of output voltage. However, a huge computational burden is present in digital control. To effectively suppress the cross-regulation several ripple base current control techniques have been implemented for SI-SIMO converters in [41–46]. A hysteresis current control is proposed for SI-SIMO buck converter in [41] to obtain fast response and low cross-regulation. In [42], peak current common mode and ripple compare differential mode is proposed for SI-SIDO buck converter to improve transient response and reduce cross-regulation. In [43], adaptive current mode control is proposed. In [44] and [45], peak current control method is proposed for SI-SIDO buck converter and SI-SIDO boost converter respectively to suppress the cross-regulation. In [46], capacitor ripple current control is proposed for SI-SIDO buck converter to suppress cross-regulation and improve dynamic performance.

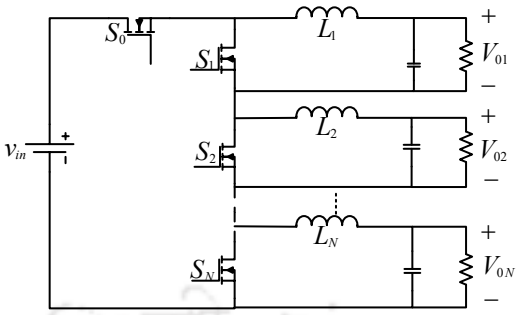


Figure 1.4: Integrated multiple output buck converter [2]

1.2.2 Integrated SIMO Converters

Many integrated SIMO converters based on isolated and non-isolated topologies have been proposed in the literature to generate multiple outputs with a reduced cross-regulation problem. These integrated SIMO converter topologies are proposed based on buck derived topologies, boost derived topologies and simultaneous buck/boost derived topologies with reduced switches. In [2, 47, 48] integrated non-isolated SIMO converters are proposed which generate only buck outputs. Figure 1.4 shows the circuit configuration of integrated multiple output buck converter. In [49], [50] integrated non-isolated dual output converters have been proposed which generate only boost outputs. In [51–54] a integrated non-isolated SIDO converter is proposed which can generate simultaneously buck and boost outputs. In [55], integrated isolated SIMO converter topology is proposed based on flyback converter. In [56], synthesis of integrated SIMO converter topologies is presented using a reduced number of switches aiming to provide many SIMO topologies so that based on a specific application, an engineer can select the preferred one. In [57], integrated SIMO converter is proposed based on SEPIC converter using integrated inductor. In [58], integrated SIMO converter is proposed which can provide high step down output voltages. In [59] integrated buck-boost flyback SIMO converter using reduced switches is proposed. In [60], high compact integrated sepic boost flyback SIMO converter is proposed.

However, this class of converters use multiple inductors or integrated inductors with low coefficient of coupling ($k < 0.3$), which does not lead to an effective reduction in the size of the magnetic core.

1.2.3 Coupled Inductor SIMO Converters

The SIMO converter using coupled inductor is an effective way to generate multiple outputs from a single input source with reduced cross-regulation. Since inductor is the largest and heaviest component in a power electronics converter, use of coupled inductor instead of multiple independent inductors is an effective way to reduce the size and volume of the converter. Moreover, the use of coupled inductor reduces ripple, increases efficiency, and increases transient response. Thus, SIMO converter using coupled inductor reduces the size, weight, volume, footprint and increases efficiency [61], [62]. Many SIMO converter using coupled inductor have been proposed in the literature based on isolated and non-isolated topologies. The isolated topologies are proposed by coupling the filter inductors of multiple output forward converter [63–65]. In this type of topologies, output voltages are not independently controlled. In [66], [67] high efficiency SIMO boost converter using coupled inductor is proposed with the utilization of zero current switching. In [68], single input three output converter using coupled inductor is proposed based on soft switching technique. However, to incorporate soft-switching technique additional clamped circuit are used which increases the size of converter. In [69], [70] SIMO converter using coupled inductor is proposed with power factor correction (PFC) function for LED drivers. In [71] SIMO converter based on buck outputs is proposed by replacing the single inductor in SI-SIMO buck converter with a coupled inductor. However, the converter posses high inductor current ripple which lead to reduce efficiency.

The other effective way of generating SIMO non-isolated converter using coupled inductor is by coupling the inductors of multiple SISO DC-DC converters. Taking dual output as an example Figure 1.5(a) shows the configuration of single-input dual-output (SIDO) buck converter using coupled inductor and is named as CI-SIDO buck converter. Similarly, Figure 1.5(b) shows the CI-SIDO boost converter which is obtained by coupling the inductors of two boost converters. Figure 1.5(c) show the CI-SIDO boost and buck converter which is obtained by coupling the inductors of boost and buck converters. In [61], [62] the current ripple reduction in CI-SIDO buck converter by phase shifting the duty cycles is analyzed. With the use of inverse coupled inductor and applying phase shift between the duty cycles, the

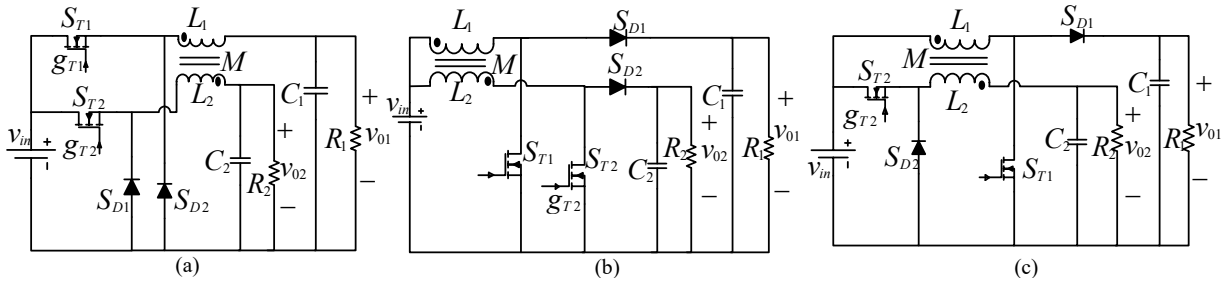


Figure 1.5: Coupled inductor single input dual output (CI-SIDO) converters (a) CI-SIDO buck converter (b) CI-SIDO boost converter (c) CI-SIDO boost and buck converter

inductor current ripple is minimized which results in high efficiency and fast transient response. However, the modelling and design of closed-loop control of CI-SIDO buck converter has not been analyzed. In CI-SIDO converter, it is observed that due to the coupling of the inductor currents, the outputs are coupled. As a result the converter suffer from cross-coupling and cross-regulation problems. These issues affect the converter performance and stability. Thus, designing an appropriate control technique is a fundamental challenge for achieving desired performance and stability. Moreover, till date research has been focused on developing control technique for SI-SIDO converter to reduce cross-regulation and there exists limited research on reducing the cross-coupling and cross-regulation effects in CI-SIDO converters. Therefore, to fill the gap in the literature, this thesis analyzes the CI-SIDO converters in detail and proposes control technique in order to suppress the cross-coupling and cross-regulation problems with good dynamic performance and stability.

1.3 Motivation for the Thesis

Having discussed the problems of the CI-SIDO converter which have not been solved in the current literature in the previous section, the motivation to carry out the research work is as follows:

- Coupled inductor single-input dual-output converter is a preferred candidate compared to parallel converters due to small volume and reduced current ripple. However, due to mutual coupling the converter suffers from cross-regulation and cross-coupling problem

which affects the characteristics of the converter. Therefore, it is essential to study the effect of mutual coupling on the characteristics of CI-SIDO converter and find out the range of coefficient of coupling used in the design of coupled inductor for better performance and stability of the converter.

- It is desirable to achieve independent control of output voltages for more efficient operation of CI-SIDO converters. However, it is difficult to execute independent regulation due to the issues of cross-regulation and cross-coupling. Therefore, work on developing a method of decoupling the cross-coupling problem in CI-SIDO converter under voltage mode control and average current control is needed.

- Peak current mode (PCM) control is a control scheme widely adapted for dc-dc converters owing to its merits over voltage-mode control like current limiting, fast transient response, noise rejection, etc. Thus, the design of PCM control when applied to CI-SIDO converter needs to be explored.

1.4 Contribution of the Thesis

Based on the motivations, following are the contribution of the thesis:

(i) The small-signal model of CI-SIDO converters is developed to analyze the effect of mutual coupling on the steady-state and transient characteristics of the converter.

(ii) A decoupled voltage mode control method is proposed for CI-SIDO buck converters using simple and cost-effective analog controllers, i.e., Type-II/Type-III compensator.

(iii) A decoupled average current control method is proposed for CI-SIDO buck converter using analog Type-II compensator.

(iv) A unified small-signal model of peak current mode controlled CI-SIDO converters is developed to analyze the inner current loop dynamics.

(v) The design procedure for slope compensations and Type-II compensator is proposed for peak current mode (PCM) controlled CI-SIDO buck converter.

1.5 Organization of the Thesis

The organization of the thesis is as follows:

- Chapter 2 presents the small-signal modelling of CI-SIDO converter using the state-space averaging technique. The modelling has been done for three topologies of CI-SIDO converter, i.e., CI-SIDO buck converter, CI-SIDO boost converter, CI-SIDO boost and buck converter. The developed model is used to study the dynamic of the converter.

- Chapter 3 analyses the effect of mutual coupling on the small-signal characteristic of CI-SIDO converter and provides the range of coefficient of coupling k that needs to be chosen for proper operation and control of CI-SIDO converters.

- Chapter 4 proposes a decoupled voltage-mode control (VMC) for CI-SIDO buck converter operating in continuous conduction mode using a simple and cost-effective analog Type-II compensator. The decoupled VMC improves the closed-loop performance of the converter by reducing the effect of cross-coupling and is validated through simulation and experiment.

- Chapter 5 proposes a decoupled average current control (ACC) for CI-SIDO buck converter operating in CCM using Type-II compensator to reduce the cross-regulation and cross-coupling. The proposed decoupled ACC reduces the cross-coupling and cross-regulation significantly and is validated through simulation and experiment.

- Chapter 6 presents the unified small-signal model for peak current mode controlled CI-SIDO converters. The model has been derived for CI-SIDO buck converter, CI-SIDO boost converter, CI-SIDO boost and buck converter. The unified model developed is validated through simulation and experiment. Moreover, using the developed small-signal model, the instability of peak current mode controlled CI-SIDO converter without slope compensation is predicted and verified through simulation and experiment.

- Chapter 7 proposes a peak current mode control for the CI-SIDO buck converter. The analysis of PCM controlled CI-SIDO buck converter is carried out using the small-signal

model developed in Chapter 6, and based on the study, a design procedure for slope compensation and controller are proposed to reduce cross-regulation and prevent sub-harmonic oscillation. The proposed PCM control for CI-SIDO buck converter is validated through simulation and experiment.

- Chapter 8 presents the conclusion of the research work and provides the scope for the future research.

2

Analysis and Modelling of Coupled Inductor Single Input Dual Output DC-DC Converters

Contents

2.1 Introduction

Coupled inductor single-input dual-output (CI-SIDO) converters are derived by coupling the inductor of two single-input single-output (SISO) dc-dc converters. The inductors are inversely coupled. Figure 2.1(a) shows the CI-SIDO buck converter, which is derived by coupling the inductors of two buck converters. Figure 2.1(b) shows the CI-SIDO boost converter, which is derived from two boost converters. Figure 2.1(c) shows the CI-SIDO boost and buck converter, which is derived by coupling the inductors of the boost converter and buck converter.

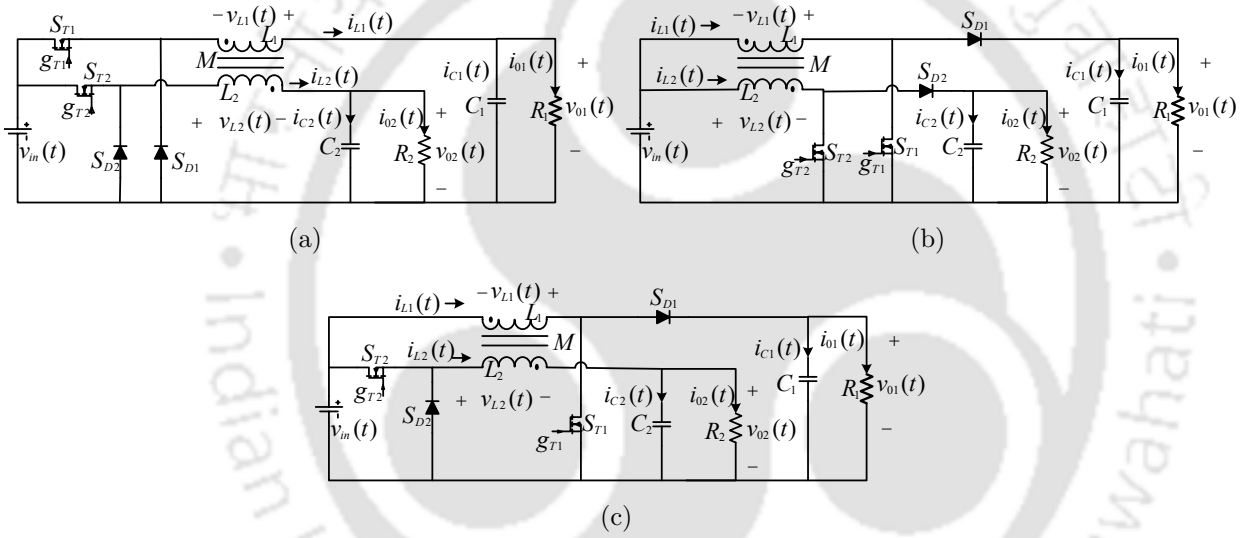


Figure 2.1: Coupled inductor single input dual output (CI-SIDO) converters (a) CI-SIDO buck converter (b) CI-SIDO boost converter (c) CI-SIDO boost buck converter

2.2 Circuit Operation

The circuit of CI-SIDO converters are shown in Figure 2.1. The circuit consists of one input voltage source v_{in}, two power MOSFET's (S_{T1}, S_{T2}), two diodes (S_{D1}, S_{D2}), one coupled inductor with coefficient of coupling $k = \frac{M}{\sqrt{L_1 L_2}}$, two output capacitors C_1, C_2, two load resistances R_1, R_2 and two output voltages v_{01}, v_{02}. The switches S_{T1}, S_{T2} and diodes S_{D1}, S_{D2} are used to control the power flow from input to the outputs. The switches S_{T1}, S_{T2} are controlled by the gate signals g_{T1}, g_{T2} generated by pulse width modulation (PWM) and are turned on and off at the switching frequency $f_s = 1/T_s$ with the duty cycles D_1 and D_2. The output voltages

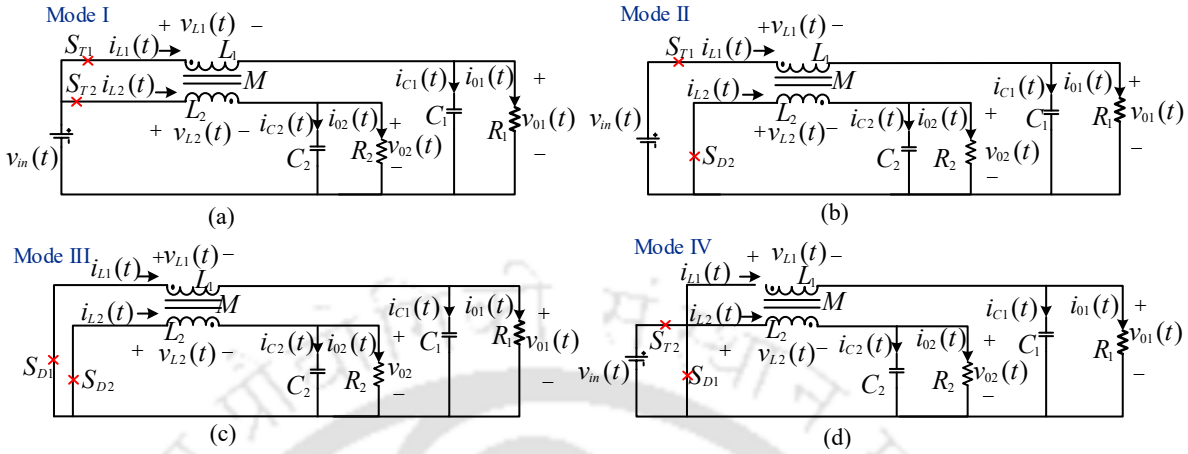


Figure 2.2: Circuit configuration of CI-SIDO buck converter in different modes of operation (a) Mode I (b) Mode II (c) Mode III (d) Mode IV

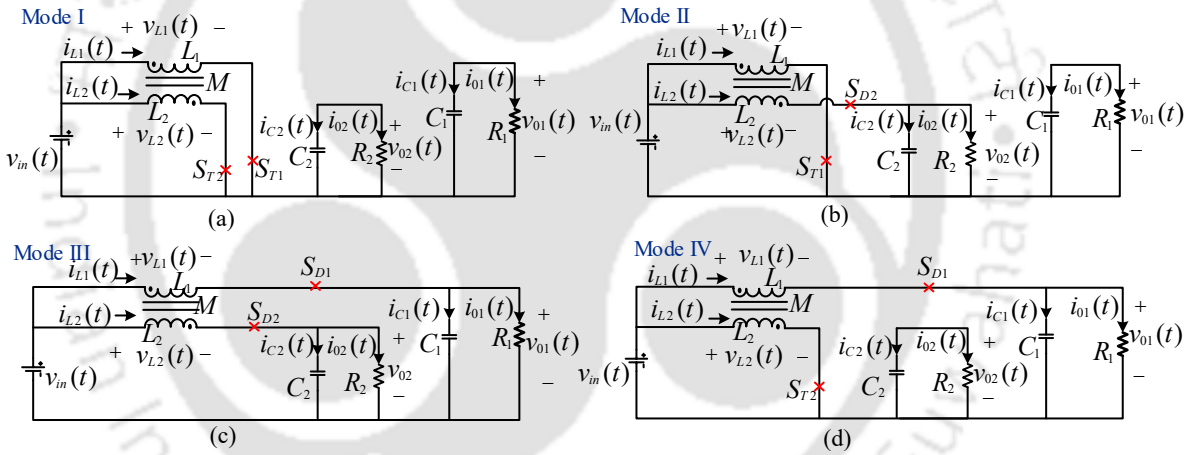


Figure 2.3: Circuit configuration of CI-SIDO boost converter in different modes of operation (a) Mode I (b) Mode II (c) Mode III (d) Mode IV

v_{01}, v_{02} are regulated with the duty cycles d_1, d_2, respectively.

Due to the presence of two switches in CI-SIDO converter, four modes of operation are possible depending on the state of switches as follows

- Mode I: Both switches S_{T1}, S_{T2} are ON and both diodes S_{D1}, S_{T2} are OFF.
- Mode II: Switch S_{T1} is ON, S_{T2} is OFF and diode S_{D1} is OFF, S_{D2} is ON.
- Mode III: Both switches S_{T1}, S_{T2} are OFF and both diodes S_{D1}, S_{T2} are ON.
- Mode IV: Switch S_{T2} is ON, S_{T1} is OFF and diode S_{D2} is OFF, S_{D1} is ON.

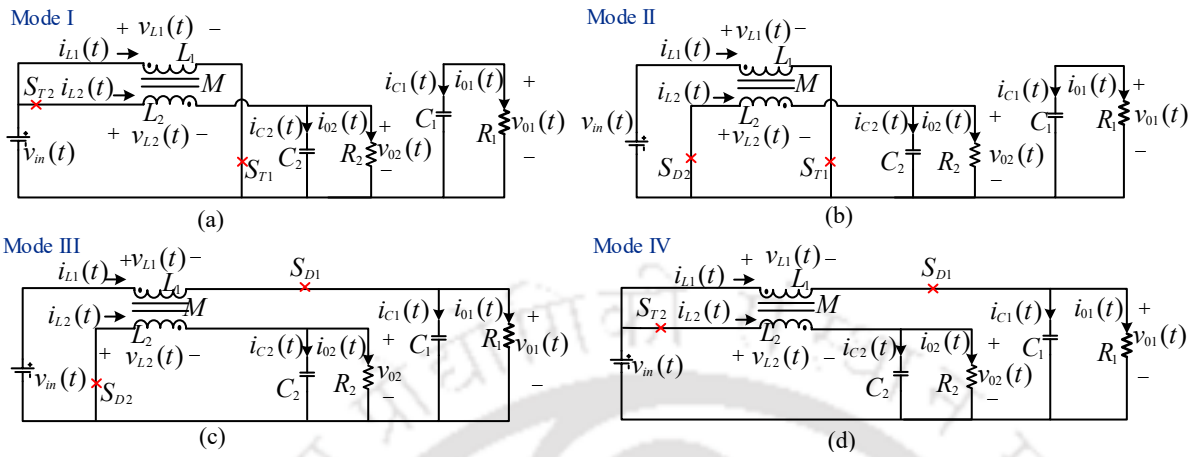


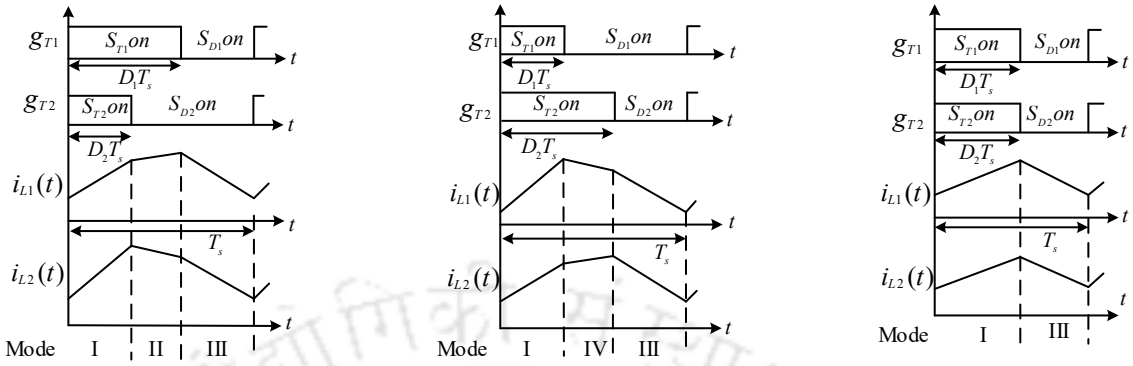
Figure 2.4: Circuit configuration of CI-SIDO boost and buck converter in different modes of operation (a) Mode I (b) Mode II (c) Mode III (d) Mode IV

Figure 2.2 shows the circuit configuration of CI-SIDO buck converter in four modes of operation. Figure 2.3 shows the circuit configuration of CI-SIDO boost converter in four modes of operation. Figure 2.4 shows the circuit configuration of CI-SIDO boost and buck converter in four modes of operation.

Depending to the magnitude of the duty cycles, the CI-SIDO converter operate in three cases, i.e Case A: $D_1 > D_2$, Case B: $D_1 < D_2$, and Case C: $D_1 = D_2$. The waveforms of the inductor currents and MOSFET gate signals are shown in Figure 2.5 for continuous conduction mode (CCM) operation.

Case A: $D_1 > D_2$

In this case, the total switching time T_S is divided into three switching interval. For the first switching interval D_2T_s, both switches S_{T1}, S_{T2} are ON, both diodes S_{D1}, S_{D2} are OFF, the converter operate in Mode I and the power is provided to both outputs v_{01}, v_{02} from v_{in}. For the second switching interval $(D_1 - D_2)T_s$, only one switch is ON i.e., switch S_{T1} is ON and S_{T2} is turned OFF, the converter operate in Mode II and the inductor current i_{L1} provides power to v_{01} from v_{in}, inductor current i_{L2} freewheels through diode S_{D2}, and provides power to v_{02}. For the last switching interval $(1 - D_1)T_s$, both the switches are OFF, both diodes are ON, the converter operate in Mode III and the inductor currents freewheels through diodes S_{D1}, S_{D2} and provides power to v_{01}, v_{02}.



(a) $D_1 > D_2$ (b) $D_1 < D_2$ (c) $D_1 = D_2$

Figure 2.5: Operating waveforms of CI-SIDO converter for CCM operation

Thus, in this case the converter operates in Mode I-Mode II-Mode III.

Case B: $D_1 < D_2$

In this case, the total switching period T_S is divided into three switching intervals. For the first switching interval D_1T_s, both switches S_{T1}, S_{T2} are ON, both diodes S_{D1}, S_{D2} are OFF, converter operate in Mode I and the power is provided to both outputs v_{01}, v_{02}. For the second switching interval $(D_2-D_1)T_s$, switch S_{T2} is ON and S_{T1} is turned OFF, the converter operate in Mode IV and the inductor current i_{L1} freewheels through diode S_{D1}, provides power to v_{01} and inductor current i_{L2} provides power to v_{02} from v_{in}. For the last switching interval $(1-D_1)T_s$, both the switches are OFF, converter operate in Mode III and the inductor currents freewheels through diodes S_{D1}, S_{D2} and provides power to v_{01}, v_{02}.

Thus, in this case the converter operates in Mode I-Mode IV-Mode III.

Case C: $D_1 = D_2$

The gate signal of both switches are equal in this case. Thus, the total switching period T_S is divided into two switching intervals. For the first interval D_2T_s, both switches S_{T1}, S_{T2} are ON, both diodes S_{D1}, S_{D2} are OFF, the converter operate in Mode I and the power is provided to both outputs v_{01}, v_{02}. For the second interval $(1-D_1)T_s$, both the switches are OFF, converter operate in Mode III and the inductor currents freewheels through diodes S_{D1}, S_{D2} and provides power to v_{01}, v_{02}. Thus, in this case the converter operates in Mode I-Mode III.

2.3 Mathematical Model of Coupled Inductor

Mathematical model of coupled inductor is required to derive the state-space equation and slopes of inductor currents of CI-SIDO converter. The voltage-current relation of inverse coupled inductor is described as

$$\begin{aligned} v_{L1}(t) &= L_1 \frac{di_{L1}(t)}{dt} - M \frac{di_{L2}(t)}{dt} \\ v_{L2}(t) &= L_2 \frac{di_{L2}(t)}{dt} - M \frac{di_{L1}(t)}{dt} \end{aligned} \tag{2.1}$$

where, L_1, L_2 are the self-inductance of each winding and M is the mutual inductance. The mutual inductance is $M = k\sqrt{L_1 L_2}$, where k is the coefficient of coupling.

The expression in (2.1) can be rearranged as

$$\begin{aligned} L_1^{'} \frac{di_{L1}(t)}{dt} &= v_{L1}(t) + \frac{M}{L_2} v_{L2}(t) \\ L_2^{'} \frac{di_{L2}(t)}{dt} &= v_{L2}(t) + \frac{M}{L_1} v_{L1}(t) \end{aligned} \tag{2.2}$$

where, $L_1^{'} = L_1(1-k^2)$, $L_2^{'} = L_2(1-k^2)$.

Equation (2.2) are used in deriving the instantaneous inductor current equation of CI-SIDO converters in Section 2.5.1.1, 2.4.2, 2.4.3.

2.4 Steady-state Analysis of CI-SIDO Converters

The steady-state equation of CI-SIDO converters are derived for the Case A ($D_1 > D_2$) and the steady-state equation remains same for all cases.

2.4.1 Steady-state Analysis of CI-SIDO Buck Converter

For Case A $D_1 > D_2$, the converter operates in three mode of operation, i.e., Mode I for $D_2 T_s$ interval, Mode II for $(D_1 - D_2)T_s$ interval, Mode III for $(1 - D_1)T_s$ interval. The inductor voltages and capacitor currents for all three switching interval can be obtained by applying kirchhoffs voltage law (KVL) and kirchhoffs current law (KCL) in the circuit configuration shown in Figure 2.2 and are written as:

For intervals:

$$\begin{array}{ccc} \overbrace{}^{D_2T_s} & \overbrace{}^{(D_1-D_2)T_s} & \overbrace{}^{(1-D_1)T_s} \\ v_{L1}(t) = v_{in}(t) - v_{01}(t) & v_{L1}(t) = v_{in}(t) - v_{01}(t) & v_{L1}(t) = -v_{01}(t) \\ v_{L2}(t) = v_{in}(t) - v_{02}(t) & v_{L2}(t) = -v_{02}(t) & v_{L2}(t) = -v_{02}(t) \\ i_{C1}(t) = i_{L1}(t) - i_{01}(t) & i_{C1}(t) = i_{L1}(t) - i_{01}(t) & i_{C1}(t) = i_{L1}(t) - i_{01}(t) \\ i_{C2}(t) = i_{L2}(t) - i_{02}(t) & i_{C2}(t) = i_{L2}(t) - i_{02}(t) & i_{C2}(t) = i_{L2}(t) - i_{02}(t) \end{array} \tag{2.3}$$

By assuming large C_1 and C_2, $v_{01}(t) \approx V_{01}$, $v_{02}(t) \approx V_{02}$, $i_{01}(t) \approx i_{01}$ and $i_{02}(t) \approx I_{02}$ where, V_{01}, V_{02}, I_{01}, I_{02} are the corresponding DC values. By applying inductor volt-sec balance equation which is given by

$$\frac{1}{T_s}\int_0^{T_s} v_{L1}(t)dt = 0 \quad , \quad \frac{1}{T_s}\int_0^{T_s} v_{L2}(t)dt = 0 \tag{2.4}$$

Solving the above equation, the output voltages are given by

$$V_{01} = D_1 V_{in} \qquad V_{02} = D_2 V_{in} \tag{2.5}$$

By applying charge balance equation which is given by

$$\frac{1}{T_s}\int_0^{T_s} i_{C1}(t)dt = 0 \quad , \quad \frac{1}{T_s}\int_0^{T_s} i_{C2}(t)dt = 0 \tag{2.6}$$

Solving we get,

$$I_{L1} = I_{01} \qquad I_{L2} = I_{02} \tag{2.7}$$

Equation (2.5), (2.7) shows that in steady-state, CI-SIDO buck behaves like a simple buck while the cross-coupling and cross-regulation effects are absent.

2.4.2 Steady-state Analysis of CI-SIDO Boost Converter

The inductor voltages and capacitor currents for all three switching intervals can be obtained by applying KVL and KCL in the circuit configuration shown in Figure 2.3 and are written as:

For intervals:

$$\begin{array}{ccc} \overbrace{\phantom{v_{L1}(t)=v_{in}(t)}}^{D_2T_s} & \overbrace{\phantom{v_{L1}(t)=v_{in}(t)}}^{(D_1-D_2)T_s} & \overbrace{\phantom{v_{L1}(t)=v_{in}(t)-v_{01}(t)}}^{(1-D_1)T_s} \\ v_{L1}(t)=v_{in}(t) & v_{L1}(t)=v_{in}(t) & v_{L1}(t)=v_{in}(t)-v_{01}(t) \\ v_{L2}(t)=v_{in}(t) & v_{L2}(t)=v_{in}(t)-v_{02}(t) & v_{L2}(t)=v_{in}(t)-v_{02}(t) \\ i_{C1}(t)=-i_{01}(t) & i_{C1}(t)=-i_{01}(t) & i_{C1}(t)=i_{L1}(t)-i_{01}(t) \\ i_{C2}(t)=-i_{02}(t) & i_{C2}(t)=i_{L2}(t)-i_{02}(t) & i_{C2}(t)=i_{L2}(t)-i_{02}(t) \end{array} \tag{2.8}$$

By assuming, $v_{01}(t) \approx V_{01}$, $v_{02}(t) \approx V_{02}$, $i_{01}(t) \approx i_{01}$ and $i_{02}(t) \approx I_{02}$ where, V_{01}, V_{02}, I_{01}, I_{02} are the corresponding DC values. By applying inductor volt-sec balance and capacitor charge balance equation, the steady-state output voltages and inductor currents are given by

$$V_{01} = \frac{V_{in}}{1-D_1}\ , \quad V_{02} = \frac{V_{in}}{1-D_2}\ , \quad I_{L1} = \frac{I_{01}}{1-D_1}\ , \quad I_{L2} = \frac{I_{02}}{1-D_2} \tag{2.9}$$

Equation (2.9) shows that in steady-state, CI-SIDO boost behaves like a simple boost while the cross-coupling and cross-regulation effects are absent.

2.4.3 Steady-state Analysis of CI-SIDO Boost and Buck Converter

The inductor voltages and capacitor currents for different switching intervals can be obtained by applying KVL and KCL in the circuit configuration shown in Figure 2.4 and are written as: For intervals:

$$\begin{array}{ccc} \overbrace{\phantom{v_{L1}(t)=v_{in}(t)}}^{D_2T_s} & \overbrace{\phantom{v_{L1}(t)=v_{in}(t)}}^{(D_1-D_2)T_s} & \overbrace{\phantom{v_{L1}(t)=v_{in}(t)-v_{01}(t)}}^{(1-D_1)T_s} \\ v_{L1}(t)=v_{in}(t) & v_{L1}(t)=v_{in}(t) & v_{L1}(t)=v_{in}(t)-v_{01}(t) \\ v_{L2}(t)=v_{in}(t)-v_{02}(t) & v_{L2}(t)=-v_{02}(t) & v_{L2}(t)=-v_{02}(t) \\ i_{C1}(t)=-i_{01}(t) & i_{C1}(t)=-i_{01}(t) & i_{C1}(t)=i_{L1}(t)-i_{01}(t) \\ i_{C2}(t)=i_{L1}(t)-i_{02}(t) & i_{C2}(t)=i_{L2}(t)-i_{02}(t) & i_{C2}(t)=i_{L2}(t)-i_{02}(t) \end{array} \tag{2.10}$$

By assuming, $v_{01}(t) \approx V_{01}$, $v_{02}(t) \approx V_{02}$, $i_{01}(t) \approx i_{01}$ and $i_{02}(t) \approx I_{02}$ where, V_{01}, V_{02}, I_{01}, I_{02} are the corresponding DC values. By applying inductor volt-sec balance and capacitor charge balance equation, the steady-state output voltages and inductor currents are given by

$$V_{01} = \frac{V_{in}}{1-D_1}\ , \quad V_{02} = D_2 V_{in}\ , \quad I_{L1} = \frac{I_{01}}{1-D_1}\ , \quad I_{L2} = I_{02} \tag{2.11}$$

Equation (2.11) shows that in steady-state, CI-SIDO boost and buck converter behaves like a simple boost and simple buck, while the cross-coupling and cross-regulation effects are absent.

2.5 Small-signal Modelling of CI-SIDO Converters

The application of the CI-SIDO converter demands the output voltages to remain constant irrespective of the variation in input voltage and load currents. This is accomplished by designing a feedback system such that the output voltages are regulated and becomes insensitive to the disturbance in input voltage and load currents. To design the feedback system and understand the dynamics of the CI-SIDO converter, i.e., how output voltages are affected by the variation in input voltage, load currents and duty cycles, we need a small-signal model of the CI-SIDO converter. The small-signal model of the CI-SIDO converter is derived using the state-space averaging technique [72], [73–76]. Based on the averaging method, firstly, a set of linear equations is derived called an average state-space equation that describes the complete dynamics of the converter. Secondly, a small-signal averaged model is derived by applying perturbation and linearization to the averaged state-space equation to obtain the converter's small-signal transfer functions.

Average State-Space Equations

The derivation of average state-space equations for CI-SIDO converter is shown considering Case A $D_1 > D_2$. The average state-space equations remain the same for Case B and Case C as well.

From Figure 2.5, it is observed that CI-SIDO converter in continuous conduction mode (CCM) operate in three modes of operation in an entire switching period T_s. That means converter operates in Mode I (both switches ON) during d_2T_s interval, Mode II (one switch OFF) during $(d_1 - d_2)T_s$ interval and Mode III (both switch OFF) during $(1 - d)T_s$ interval. The circuit configuration in three operating modes are different. In each mode, the converter circuit is linear time-invariant as shown in Figure 2.2, 2.3, 2.4. Thus, the CI-SIDO converter

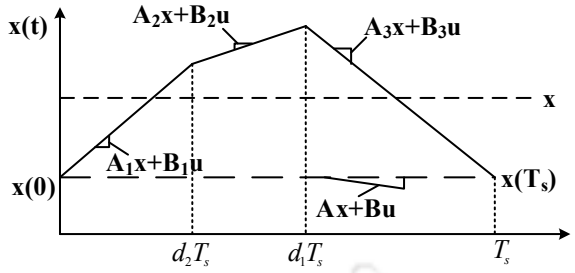


Figure 2.6: Relation between an element of state vector with its average in one switching period

can be described by a set of state-space equations in each mode and is given below:

$$\text{Mode I } (0 < t < d_2T_s): \begin{cases} \dot{\mathbf{x}}(t) = \mathbf{A}_1\mathbf{x}(t) + \mathbf{B}_1\mathbf{u}(t) \\ \mathbf{y}(t) = \mathbf{C}_1\mathbf{x}(t) + \mathbf{D}_1\mathbf{u}(t) \end{cases}$$

$$\text{Mode II } (d_2T_s < t < d_1T_s): \begin{cases} \dot{\mathbf{x}}(t) = \mathbf{A}_2\mathbf{x}(t) + \mathbf{B}_2\mathbf{u}(t) \\ \mathbf{y}(t) = \mathbf{C}_2\mathbf{x}(t) + \mathbf{D}_2\mathbf{u}(t) \end{cases}$$

$$\text{Mode III } (d_1T_s < t < T_s): \begin{cases} \dot{\mathbf{x}}(t) = \mathbf{A}_3\mathbf{x}(t) + \mathbf{B}_3\mathbf{u}(t) \\ \mathbf{y}(t) = \mathbf{C}_3\mathbf{x}(t) + \mathbf{D}_3\mathbf{u}(t) \end{cases}$$

where,

$\mathbf{A}_i$, $\mathbf{B}_i$, $\mathbf{C}_i$, $\mathbf{D}_i$ denote the state-space matrices for i^{th} state of the converter, $\mathbf{x}(t)$ denotes state variable vector, $\mathbf{u}(t)$ denotes input variable vector, $\mathbf{y}(t)$ denotes output variable vector, and $i = \{1, 2, 3\}$. The vector representation of the state variable, input variable, and output vector are $\mathbf{x}(t) = [i_{L1}(t)\ v_{C1}(t)\ i_{L2}(t)\ v_{C2}(t)]^T$, $\mathbf{u}(t) = [v_{in}(t)\ i_{01}(t)\ i_{02}(t)]^T$, $\mathbf{y}(t) = [v_{01}(t)\ v_{02}(t)]^T$.

The averaged state-space equation for the entire switching period T_s is obtained by averaging the state-space equations of all three switching intervals and is given by:

$$\begin{aligned} \dot{\mathbf{x}} &= \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \\ \mathbf{y} &= \mathbf{C}\mathbf{x} + \mathbf{D}\mathbf{u} \end{aligned} \tag{2.12}$$

where,

$\mathbf{A} = \mathbf{A}_1 d_2 + \mathbf{A}_2(d_1 - d_2) + \mathbf{A}_3(1 - d_1)$

$\mathbf{B} = \mathbf{B}_1 d_2 + \mathbf{B}_2(d_1 - d_2) + \mathbf{B}_3(1 - d_1)$

$\mathbf{C} = \mathbf{C}_1 d_2 + \mathbf{C}_2(d_1 - d_2) + \mathbf{C}_3(1 - d_1)$

$\mathbf{D} = \mathbf{D}_1 d_2 + \mathbf{D}_2(d_1 - d_2) + \mathbf{D}_3(1 - d_1)$

Equation (2.12) is the averaged state-space model which describes the dynamics of the converter. The variation of a element of $\mathbf{x}$(t) and its average are shown in Figure 2.6.

Small Signal Perturbation and Linearization

Considering the feedback circuit disable, the perturbation in the input variables and duty cycles causes perturbation in the steady-state value of inductor currents, capacitor voltages and output voltages. Perturbation is the low-frequency sinusoidal waveform superimposed on the DC nominal value. The averaged state variable vector, input variable vector, output variable vector and control variables can be written as:

$$\mathbf{x} = \mathbf{X} + \hat{\mathbf{x}} \qquad \mathbf{y} = \mathbf{Y} + \hat{\mathbf{y}} \qquad \mathbf{u} = \mathbf{U} + \hat{\mathbf{u}} \qquad d_1 = D_1 + \hat{d}_1 \qquad d_2 = D_2 + \hat{d}_2$$

where $\mathbf{X}$, $\mathbf{Y}$, $\mathbf{U}$, D_1, D_2 are the nominal DC values of $\mathbf{x}$, $\mathbf{y}$, $\mathbf{u}$, d_1, d_2 and $\hat{\mathbf{x}}$, $\hat{\mathbf{y}}$, $\hat{\mathbf{u}}$, $\hat{d}_1$, $\hat{d}_2$ are the perturbation in $\mathbf{X}$, $\mathbf{Y}$, $\mathbf{U}$, D_1, D_2.

Due to the perturbation in the duty cycles, the average state-space matrices $\mathbf{A}$, $\mathbf{B}$, $\mathbf{C}$, $\mathbf{D}$ get affected and can be written as:

$$\begin{aligned}
\mathbf{A} &= \mathbf{A}_1 d_2 + \mathbf{A}_2(d_1 - d_2) + \mathbf{A}_3(1 - d_1) \\
&= \mathbf{A}_1 D_2 + \mathbf{A}_2(D_1 - D_2) + \mathbf{A}_3(1 - D_1) + (\mathbf{A}_1 - \mathbf{A}_2)\hat{d}_2 + (\mathbf{A}_2 - \mathbf{A}_3)\hat{d}_1 \\
&= \mathbf{A}_{av} + (\mathbf{A}_1 - \mathbf{A}_2)\hat{d}_2 + (\mathbf{A}_2 - \mathbf{A}_3)\hat{d}_1 \\
\mathbf{B} &= \mathbf{B}_1 d_2 + \mathbf{B}_2(d_1 - d_2) + \mathbf{B}_3(1 - d_1) \\
&= \mathbf{B}_1 D_2 + \mathbf{B}_2(D_1 - D_2) + \mathbf{B}_3(1 - D_1) + (\mathbf{B}_1 - \mathbf{B}_2)\hat{d}_2 + (\mathbf{B}_2 - \mathbf{B}_3)\hat{d}_1 \\
&= \mathbf{B}_{av} + (\mathbf{B}_1 - \mathbf{B}_2)\hat{d}_2 + (\mathbf{B}_2 - \mathbf{B}_3)\hat{d}_1 \\
\mathbf{C} &= \mathbf{C}_1 d_2 + \mathbf{C}_2(d_1 - d_2) + \mathbf{C}_3(1 - d_1) \\
&= \mathbf{C}_1 D_2 + \mathbf{C}_2(D_1 - D_2) + \mathbf{C}_3(1 - D_1) + (\mathbf{C}_1 - \mathbf{C}_2)\hat{d}_2 + (\mathbf{C}_2 - \mathbf{C}_3)\hat{d}_1 \\
&= \mathbf{C}_{av} + (\mathbf{C}_1 - \mathbf{C}_2)\hat{d}_2 + (\mathbf{C}_2 - \mathbf{C}_3)\hat{d}_1
\end{aligned}$$

$$\begin{aligned}\mathbf{D} &= \mathbf{D}_1 d_2 + \mathbf{D}_2(d_1 - d_2) + \mathbf{D}_3(1 - d_1) \\ &= \mathbf{D}_1 D_2 + \mathbf{D}_2(D_1 - D_2) + \mathbf{D}_3(1 - D_1) + (\mathbf{D}_1 - \mathbf{D}_2)\hat{d}_2 + (\mathbf{D}_2 - \mathbf{D}_3)\hat{d}_1 \\ &= \mathbf{D}_{av} + (\mathbf{D}_1 - \mathbf{D}_2)\hat{d}_2 + (\mathbf{D}_2 - \mathbf{D}_3)\hat{d}_1\end{aligned}$$

Inserting all the perturbations variables in the averaged state-space equations (2.12), gives:

$$\begin{cases} \frac{d[\mathbf{X}+\hat{\mathbf{x}}]}{dt} &= [\mathbf{A}_{av} + (\mathbf{A}_1 - \mathbf{A}_2)\hat{d}_2 + (\mathbf{A}_2 - \mathbf{A}_3)\hat{d}_1][\mathbf{X} + \hat{\mathbf{x}}] \\ & \quad +[\mathbf{B}_{av} + (\mathbf{B}_1 - \mathbf{B}_2)\hat{d}_2 + (\mathbf{B}_2 - \mathbf{B}_3)\hat{d}_1][\mathbf{U} + \hat{\mathbf{u}}] \\ \mathbf{Y} + \hat{\mathbf{y}} &= [\mathbf{C}_{av} + (\mathbf{C}_1 - \mathbf{C}_2)\hat{d}_2 + (\mathbf{C}_2 - \mathbf{C}_3)\hat{d}_1][\mathbf{X} + \hat{\mathbf{x}}] \\ & \quad +[\mathbf{D}_{av} + (\mathbf{D}_1 - \mathbf{D}_2)\hat{d}_2 + (\mathbf{D}_2 - \mathbf{D}_3)\hat{d}_1][\mathbf{U} + \hat{\mathbf{u}}] \end{cases} \tag{2.13}$$

The derivation of constant is zero, the above expression can be written as:

$$\begin{cases} \frac{d\hat{\mathbf{x}}}{dt} &= \mathbf{A}_{av}\mathbf{X} + \mathbf{B}_{av}\mathbf{U} + \mathbf{A}_{av}\hat{\mathbf{x}} + \mathbf{B}_{av}\hat{\mathbf{u}} + [(\mathbf{A}_1 - \mathbf{A}_2)\hat{d}_2 + (\mathbf{A}_2 - \mathbf{A}_3)\hat{d}_1]\mathbf{X} \\ & \quad +[(\mathbf{B}_1 - \mathbf{B}_2)\hat{d}_2 + (\mathbf{B}_2 - \mathbf{B}_3)\hat{d}_1]\mathbf{U} + [(\mathbf{A}_1 - \mathbf{A}_2)\hat{d}_2 + (\mathbf{A}_2 - \mathbf{A}_3)\hat{d}_1]\hat{\mathbf{x}} \\ & \quad +[(\mathbf{B}_1 - \mathbf{B}_2)\hat{d}_2(t) + (\mathbf{B}_2 - \mathbf{B}_3)\hat{d}_1]\hat{\mathbf{u}} \\ \mathbf{Y} + \hat{\mathbf{y}} &= \mathbf{C}_{av}\mathbf{X} + \mathbf{D}_{av}\mathbf{U} + \mathbf{C}_{av}\hat{\mathbf{x}} + \mathbf{D}_{av}\hat{\mathbf{u}} + [(\mathbf{C}_1 - \mathbf{C}_2)\hat{d}_2 + (\mathbf{C}_2 - \mathbf{C}_3)\hat{d}_1]\mathbf{X} \\ & \quad +[(\mathbf{D}_1 - \mathbf{D}_2)\hat{d}_2 + (\mathbf{D}_2 - \mathbf{D}_3)\hat{d}_1]\mathbf{U} + [(\mathbf{C}_1 - \mathbf{C}_2)\hat{d}_2 + (\mathbf{C}_2 - \mathbf{C}_3)\hat{d}_1]\hat{\mathbf{x}} \\ & \quad +[(\mathbf{D}_1 - \mathbf{D}_2)\hat{d}_2 + (\mathbf{D}_2 - \mathbf{D}_3)\hat{d}_1]\hat{\mathbf{u}} \end{cases} \tag{2.14}$$

Separating the DC part, AC part and neglecting the non-linear terms, the above expression can be written as:

$$dc \begin{cases} 0 = \mathbf{A}_{av}\mathbf{X} + \mathbf{B}_{av}\mathbf{U} \\ \mathbf{Y} = \mathbf{C}_{av}\mathbf{X} + \mathbf{D}_{av}\mathbf{U} \end{cases} \quad ac \begin{cases} \frac{d}{dt}\hat{\mathbf{x}} &= \mathbf{A}_{av}\hat{\mathbf{x}} + \mathbf{B}_{av}\hat{\mathbf{u}} + [(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)\mathbf{U}]\hat{d}_2 \\ & \quad +[(\mathbf{A}_2 - \mathbf{A}_3)\mathbf{X} + (\mathbf{B}_2 - \mathbf{B}_3)\mathbf{U}]\hat{d}_1 \\ \hat{\mathbf{y}} &= \mathbf{C}_{av}\hat{\mathbf{x}} + \mathbf{D}_{av}\hat{\mathbf{u}} + [(\mathbf{C}_1 - \mathbf{C}_2)\mathbf{X} + (\mathbf{D}_1 - \mathbf{D}_2)\mathbf{U}]\hat{d}_2 \\ & \quad +[(\mathbf{C}_2 - \mathbf{C}_3)\mathbf{X} + (\mathbf{D}_2 - \mathbf{D}_3)\mathbf{U}]\hat{d}_1 \end{cases} \tag{2.15}$$

The solution of DC part is given as:

$$\mathbf{X} = -\mathbf{A}_{av}^{-1}\mathbf{B}_{av}\mathbf{U} \qquad \mathbf{Y} = (-\mathbf{C}_{av}\mathbf{A}_{av}^{-1}\mathbf{B}_{av} + \mathbf{D}_{av})\mathbf{U} \tag{2.16}$$

Equation (2.16) is based on the average state-space matrices, which is derived by assuming

small ripple approximation. Using (2.16) steady-state value of inductor currents, capacitor voltages and output voltages can be calculated.

By applying Laplace transform to the ac part, gives:

$$\begin{cases} s\hat{\mathbf{x}}(s) = \mathbf{A}_{av}\hat{\mathbf{x}}(s) + \mathbf{B}_{av}\hat{\mathbf{u}}(s) + [(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)\mathbf{U}]\hat{d}_2(s) \\ \qquad\qquad +[(\mathbf{A}_2 - \mathbf{A}_3)\mathbf{X} + (\mathbf{B}_2 - \mathbf{B}_3)\mathbf{U}]\hat{d}_1(s) \\ \hat{\mathbf{y}}(s) = \mathbf{C}_{av}\hat{\mathbf{x}}(s) + \mathbf{D}_{av}\hat{\mathbf{u}}(s) + [(\mathbf{C}_1 - \mathbf{C}_2)\mathbf{X} + (\mathbf{D}_1 - \mathbf{D}_2)\mathbf{U}]\hat{d}_2(s) \\ \qquad\qquad +[(\mathbf{C}_2 - \mathbf{C}_3)\mathbf{X} + (\mathbf{D}_2 - \mathbf{D}_3)\mathbf{U}]\hat{d}_1(s) \end{cases} \tag{2.17}$$

resulting in

$$\hat{\mathbf{x}}(s) = (s\mathbf{I} - \mathbf{A}_{av})^{-1}\mathbf{B}_{av}\hat{\mathbf{u}}(s) + (s\mathbf{I} - \mathbf{A}_{av})^{-1}[(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)\mathbf{U}]\hat{d}_2(s) + (s\mathbf{I} - \mathbf{A}_{av})^{-1}[(\mathbf{A}_2 - \mathbf{A}_3)\mathbf{X} + (\mathbf{B}_2 - \mathbf{B}_3)\mathbf{U}]\hat{d}_1(s) \tag{2.18}$$

$$\hat{\mathbf{y}}(s) = [\mathbf{C}_{av}(s\mathbf{I} - \mathbf{A}_{av})^{-1}\mathbf{B}_{av} + \mathbf{D}_{av}]\hat{\mathbf{u}}(s) + \mathbf{C}_{av}(s\mathbf{I} - \mathbf{A}_{av})^{-1}[(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)\mathbf{U}]\hat{d}_2(s) + \mathbf{C}_{av}(s\mathbf{I} - \mathbf{A}_{av})^{-1}[(\mathbf{A}_2 - \mathbf{A}_3)\mathbf{X} + (\mathbf{B}_2 - \mathbf{B}_3)\mathbf{U}]\hat{d}_1(s) + [(\mathbf{C}_1 - \mathbf{C}_2)\mathbf{X} + (\mathbf{D}_1 - \mathbf{D}_2)\mathbf{U}]\hat{d}_2(s) + [(\mathbf{C}_2 - \mathbf{C}_3)\mathbf{X} + (\mathbf{D}_2 - \mathbf{D}_3)\mathbf{U}]\hat{d}_1(s) \tag{2.19}$$

The transfer functions between the state variables and input variables are obtained using (2.18) by considering $\hat{d}_1 = \hat{d}_2 = 0$ and is given by

$$\hat{\mathbf{x}}(s) = (s\mathbf{I} - \mathbf{A}_{av})^{-1}\mathbf{B}_{av}\hat{\mathbf{u}}(s) \tag{2.20}$$

The transfer functions between the state variables and duty ratios are obtained using (2.18) by considering $\hat{\mathbf{u}} = 0$ and is given by

$$\begin{aligned} \hat{\mathbf{x}}(s) &= (s\mathbf{I} - \mathbf{A}_{av})^{-1}[(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)\mathbf{U}]\hat{d}_2(s) \\ &\quad +(s\mathbf{I} - \mathbf{A}_{av})^{-1}[(\mathbf{A}_2 - \mathbf{A}_3)\mathbf{X} + (\mathbf{B}_2 - \mathbf{B}_3)\mathbf{U}]\hat{d}_1(s) \end{aligned} \tag{2.21}$$

The transfer functions between the output variables and input variables are obtained using (2.19) by considering $\hat{d}_1 = \hat{d}_2 = 0$ and is given by

$$\hat{\mathbf{y}}(s) = [\mathbf{C}_{av}(s\mathbf{I} - \mathbf{A}_{av})^{-1}\mathbf{B}_{av} + \mathbf{D}_{av}]\hat{\mathbf{u}}(s) \tag{2.22}$$

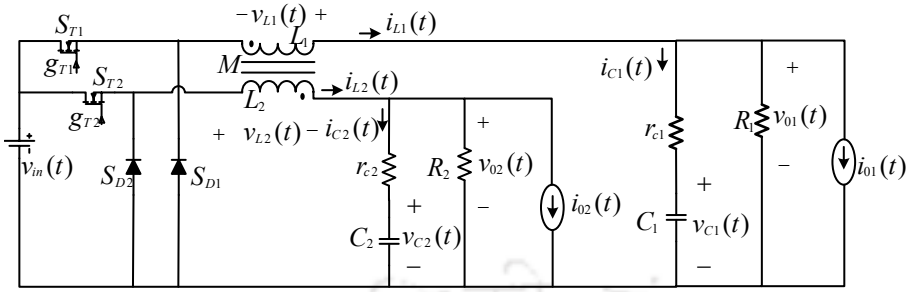


Figure 2.7: Circuit diagram of CI-SIDO buck converter considering ESR of capacitor

The transfer functions between the output variables and duty ratios are obtained using (2.19) by considering $\hat{\mathbf{u}} = 0$ and is given by

$$\hat{\mathbf{y}}(s) = \{\mathbf{C}_{av}(s\mathbf{I} - \mathbf{A}_{av})^{-1}[(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)\mathbf{U}] + (\mathbf{C}_1 - \mathbf{C}_2)\mathbf{X} + (\mathbf{D}_1 - \mathbf{D}_2)\mathbf{U}\}\hat{d}_2(s)$$
$$+ \{\mathbf{C}_{av}(s\mathbf{I} - \mathbf{A}_{av})^{-1}[(\mathbf{A}_2 - \mathbf{A}_3)\mathbf{X} + (\mathbf{B}_2 - \mathbf{B}_3)\mathbf{U}] + (\mathbf{C}_2 - \mathbf{C}_3)\mathbf{X} + (\mathbf{D}_2 - \mathbf{D}_3)\mathbf{U}\}\hat{d}_1(s) \quad (2.23)$$

2.5.1 Small-signal Modelling of CI-SIDO Buck Converter

The small-signal modelling of CI-SIDO buck converter is performed assuming: (i) ideal switches and diodes (ii) considering effective series resistance (ESR) of capacitors and neglecting ESR of coupled inductor.

Figure 2.7 shows the circuit diagram of CI-SIDO buck converter considering ESR of capacitors r_{c1}, r_{c2}.

2.5.1.1 State-space Equations

Considering Case A ($D_1 > D_2$), the CI-SIDO buck converter has three modes of operation. The state-space equation for all three modes of operation are given as follows:

Mode I: (d_2T_s interval)

In this switching interval, both the switches are turned ON. The equivalent circuit for this interval is shown in Figure 2.8. Applying KVL to the inductor and capacitor loops in the

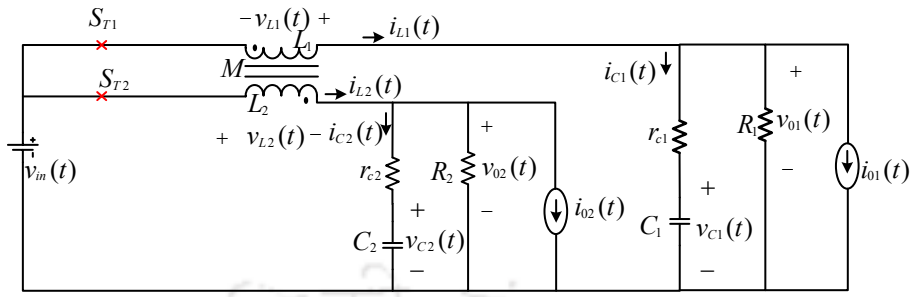


Figure 2.8: Mode I circuit configuration of CI-SIDO buck converter

equivalent circuit of d_2T_s interval gives:

$$
\begin{aligned}
L_1^{'}\frac{di_{L1}(t)}{dt} &= v_{in}(t) - r_1^{'}i_{L1}(t) - r_1^{''}v_{C1}(t) + r_{c1}r_1^{''}i_{01}(t) + \frac{M}{L_2}(v_{in}(t) - r_2^{'}i_{L2}(t) - r_2^{''}v_{C2}(t) + r_{c2}r_2^{''}i_{02}(t)) \\
C_1\frac{dv_{C1}(t)}{dt} &= r_1^{''}i_{L1}(t) - \frac{r_1^{''}v_{C1}(t)}{R_1} - r_1^{''}i_{01}(t) \\
L_2^{'}\frac{di_{L2}(t)}{dt} &= v_{in} - r_2^{'}i_{L2}(t) - r_2^{''}v_{C2(t)} + r_{c2}r_2^{''}i_{02}(t) + \frac{M}{L_1}(v_{in} - r_1^{'}i_{L1}(t) - r_1^{''}v_{C1}(t) + r_{c1}r_1^{''}i_{01}(t)) \\
C_2\frac{dv_{C2}(t)}{dt} &= r_2^{''}i_{L2}(t) - \frac{r_2^{''}v_{C2}(t)}{R_2} - r_2^{''}i_{02}(t)
\end{aligned}
\tag{2.24}
$$

$$
\begin{aligned}
v_{01}(t) &= r_{c1}r_1^{''}i_{L1}(t) - r_{c1}v_{C1}(t) - r_{c1}r_1^{''}i_{01}(t) \\
v_{02}(t) &= r_{c1}r_2^{''}i_{L2}(t) - r_{c2}v_{C2}(t) - r_{c2}r_2^{''}i_{02}(t)
\end{aligned}
\tag{2.25}
$$

where, $r_1^{'} = \frac{R_1 r_{c1}}{R_1+r_{c1}}$, $r_2^{'} = \frac{R_2 r_{c2}}{R_2+r_{c2}}$, $r_1^{''} = \frac{R_1}{R_1+r_{c1}}$, $r_2^{''} = \frac{R_2}{R_2+r_{c2}}$.

leading to state-space equation of the d_2T_s interval:

$$
\frac{d\mathbf{x}(t)}{dt} = \mathbf{A}_1\mathbf{x}(t) + \mathbf{B}_1\mathbf{u}(t)
$$

$$
\mathbf{y}(t) = \mathbf{C}_1\mathbf{x}(t) + \mathbf{D}_1\mathbf{u}(t)
$$

$$
\mathbf{A}_1 = \begin{bmatrix}
\frac{-r_1^{'}}{L_1^{'}} & \frac{-r_1^{''}}{L_1^{'}} & \frac{-Mr_2^{'}}{L_2L_1^{'}} & \frac{-Mr_2^{''}}{L_2L_1^{'}} \\
\frac{r_1^{''}}{C_1} & \frac{-r_1^{''}}{C_1R_1} & 0 & 0 \\
\frac{-Mr_1^{'}}{L_1L_2^{'}} & \frac{-Mr_1^{''}}{L_1L_2^{'}} & \frac{-r_2^{'}}{L_2^{'}} & \frac{-r_2^{''}}{L_2^{'}} \\
0 & 0 & \frac{r_2^{''}}{C_2} & \frac{-r_2^{''}}{C_2R_2}
\end{bmatrix}
\quad
\mathbf{B}_1 = \begin{bmatrix}
\frac{(1+\frac{M}{L_2})}{L_1^{'}} & \frac{r_{c1}r_1^{''}}{L_1^{'}} & \frac{Mr_{c2}r_2^{''}}{L_2L_1^{'}} \\
0 & -\frac{r_1^{''}}{C_1} & 0 \\
\frac{(1+\frac{M}{L_1})}{L_2^{'}} & \frac{Mr_{c1}r_1^{''}}{L_1L_2^{'}} & \frac{r_{c2}r_2^{''}}{L_2^{'}} \\
0 & 0 & -\frac{r_2^{''}}{C_2}
\end{bmatrix}
$$

$$
\mathbf{C}_1 = \begin{bmatrix}
r_{c1}r_1^{''} & r_1^{''} & 0 & 0 \\
0 & 0 & r_{c2}r_2^{''} & r_2^{''}
\end{bmatrix}
\quad
\mathbf{D}_1 = \begin{bmatrix}
0 & -r_{c1}r_1^{''} & 0 \\
0 & 0 & -r_{c2}r_2^{''}
\end{bmatrix}
$$

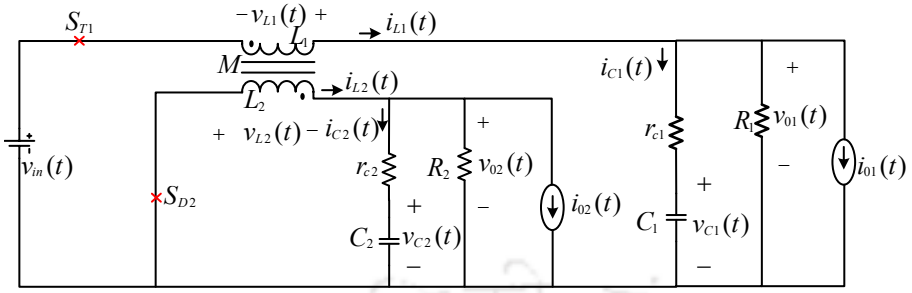


Figure 2.9: Mode II circuit configuration of CI-SIDO buck converter

Mode II: $(d_1 - d_2)T_s$ **interval**

In this switching interval, only one switch S_{T1} is turned ON and the other switch S_{T2} is turned OFF. The equivalent circuit for this interval is shown in Figure 2.9. Applying KVL to the inductor and capacitor loops in the equivalent circuit of $(d_1 - d_2)T_s$ interval gives:

$$\begin{aligned}
L_1^{'}\frac{di_{L1}(t)}{dt} &= v_{in}(t) - r_1^{'}i_{L1}(t) - r_1^{''}v_{C1}(t) + r_{c1}r_1^{''}i_{01}(t) + \frac{M}{L_2}(-r_2^{'}i_{L2}(t) - r_2^{''}v_{C2}(t) + r_{c2}r_2^{''}i_{02}(t)) \\
C_1\frac{dv_{C1}(t)}{dt} &= r_1^{''}i_{L1}(t) - \frac{r_1^{''}v_{C1}(t)}{R_1} - r_1^{''}i_{01}(t) \\
L_2^{'}\frac{di_{L2}(t)}{dt} &= -r_2^{'}i_{L2}(t) - r_2^{''}v_{C2}(t) + r_{c2}r_2^{''}i_{02}(t) + \frac{M}{L_1}(v_{in}(t) - r_1^{'}i_{L1}(t) - r_1^{''}v_{C1}(t) + r_{c1}r_1^{''}i_{01}(t)) \\
C_2\frac{dv_{C2}(t)}{dt} &= r_2^{''}i_{L2}(t) - \frac{r_2^{''}v_{C2}(t)}{R_2} - r_2^{''}i_{02}(t)
\end{aligned} \tag{2.26}$$

$$\begin{aligned}
v_{01}(t) &= r_{c1}r_1^{''}i_{L1}(t) - r_{c1}v_{C1}(t) - r_{c1}r_1^{''}i_{01}(t) \\
v_{02}(t) &= r_{c1}r_2^{''}i_{L2}(t) - r_{c2}v_{C2}(t) - r_{c2}r_2^{''}i_{02}(t)
\end{aligned} \tag{2.27}$$

leading to state-space equation of the $(d_1 - d_2)T_s$ interval:

$$\frac{d\mathbf{x}(t)}{dt} = \mathbf{A}_2\mathbf{x}(t) + \mathbf{B}_2\mathbf{u}(t) \quad \mathbf{y}(t) = \mathbf{C}_2\mathbf{x}(t) + \mathbf{D}_2\mathbf{u}(t)$$

$$\mathbf{A}_2 = \begin{bmatrix} \frac{-r_1^{'}}{L_1^{'}} & \frac{-r_1^{''}}{L_1^{'}} & \frac{-Mr_2^{'}}{L_2L_1^{'}} & \frac{-Mr_2^{''}}{L_2L_1^{'}} \\ \frac{r_1^{''}}{C_1} & \frac{-r_1^{''}}{C_1R_1} & 0 & 0 \\ \frac{-Mr_1^{'}}{L_1L_2^{'}} & \frac{-Mr_1^{''}}{L_1L_2^{'}} & \frac{-r_2^{'}}{L_2^{'}} & \frac{-r_2^{''}}{L_2^{'}} \\ 0 & 0 & \frac{r_2^{''}}{C_2} & \frac{-r_2^{''}}{C_2R_2} \end{bmatrix} \quad \mathbf{B}_2 = \begin{bmatrix} \frac{1}{L_1^{'}} & \frac{r_{c1}r_1^{''}}{L_1^{'}} & \frac{Mr_{c2}r_2^{''}}{L_2L_1^{'}} \\ 0 & -\frac{r_1^{''}}{C_1} & 0 \\ \frac{M}{L_1L_2^{'}} & \frac{Mr_{c1}r_1^{''}}{L_1L_2^{'}} & \frac{r_{c2}r_2^{''}}{L_2^{'}} \\ 0 & 0 & -\frac{r_2^{''}}{C_2} \end{bmatrix}$$

$$\mathbf{C}_2 = \begin{bmatrix} r_{c1}r_1^{''} & r_1^{''} & 0 & 0 \\ 0 & 0 & r_{c2}r_2^{''} & r_2^{''} \end{bmatrix} \quad \mathbf{D}_2 = \begin{bmatrix} 0 & -r_{c1}r_1^{''} & 0 \\ 0 & 0 & -r_{c2}r_2^{''} \end{bmatrix}$$

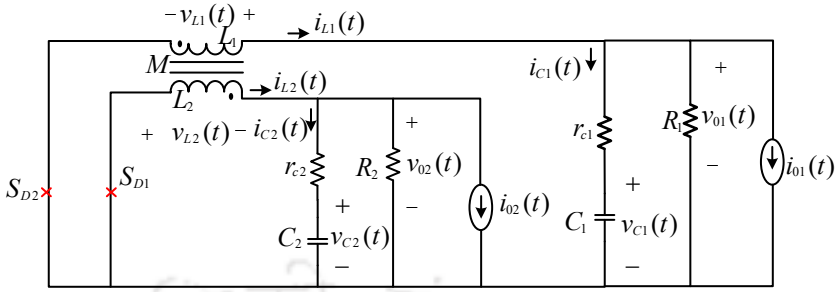


Figure 2.10: Mode III circuit configuration of CI-SIDO buck converter

Mode III: $(1-d_1)T_s$ **interval**

In this switching interval, both switches are turned OFF. The equivalent circuit for this interval is shown in Figure 2.10. Applying KVL to the inductor and capacitor loops in the equivalent circuit of $(1-d_1)T_s$ interval gives:

$$\begin{aligned}
L_1^{'}\tfrac{di_{L1}(t)}{dt} &= -r_1^{'}i_{L1}(t) - r_1^{''}v_{C1}(t) + r_{c1}r_1^{''}i_{01}(t) + \tfrac{M}{L_2}(-r_2^{'}i_{L2}(t) - r_2^{''}v_{C2}(t) + r_{c2}r_2^{''}i_{02}(t)) \\
C_1\tfrac{dv_{C1}(t)}{dt} &= r_1^{''}i_{L1} - \tfrac{r_1^{''}v_{C1}}{R_1} - r_1^{''}i_{01} \\
L_2^{'}\tfrac{di_{L2}(t)}{dt} &= -r_2^{'}i_{L2}(t) - r_2^{''}v_{C2}(t) + r_{c2}r_2^{''}i_{02}(t) + \tfrac{M}{L_1}(-r_1^{'}i_{L1}(t) - r_1^{''}v_{C1}(t) + r_{c1}r_1^{''}i_{01}(t)) \\
C_2\tfrac{dv_{C2}(t)}{dt} &= r_2^{''}i_{L2}(t) - \tfrac{r_2^{''}v_{C2}(t)}{R_2} - r_2^{''}i_{02}(t)
\end{aligned} \tag{2.28}$$

$$\begin{aligned}
v_{01}(t) &= r_{c1}r_1^{''}i_{L1}(t) - r_{c1}v_{C1}(t) - r_{c1}r_1^{''}i_{01}(t) \\
v_{02}(t) &= r_{c1}r_2^{''}i_{L2}(t) - r_{c2}v_{C2}(t) - r_{c2}r_2^{''}i_{02}(t)
\end{aligned} \tag{2.29}$$

leading to state-space equation of the $(1-d_1)T_s$ interval:

$$\frac{d\mathbf{x}(t)}{dt} = \mathbf{A}_3\mathbf{x}(t) + \mathbf{B}_3\mathbf{u}(t) \quad \mathbf{y}(t) = \mathbf{C}_3\mathbf{x}(t) + \mathbf{D}_3\mathbf{u}(t)$$

$$\mathbf{A}_3 = \begin{bmatrix} \frac{-r_1^{'}}{L_1^{'}} & \frac{-r_1^{''}}{L_1^{'}} & \frac{-Mr_2^{'}}{L_2L_1^{'}} & \frac{-Mr_2^{''}}{L_2L_1^{'}} \\ \frac{r_1^{''}}{C_1} & \frac{-r_1^{''}}{C_1R_1} & 0 & 0 \\ \frac{-Mr_1^{'}}{L_1L_2^{'}} & \frac{-Mr_1^{''}}{L_1L_2^{'}} & \frac{-r_2^{'}}{L_2^{'}} & \frac{-r_2^{''}}{L_2^{'}} \\ 0 & 0 & \frac{r_2^{''}}{C_2} & \frac{-r_2^{''}}{C_2R_2} \end{bmatrix} \quad \mathbf{B}_3 = \begin{bmatrix} 0 & \frac{r_{c1}r_1^{''}}{L_1^{'}} & \frac{Mr_{c2}r_2^{''}}{L_2L_1^{'}} \\ 0 & -\frac{r_1^{''}}{C_1} & 0 \\ 0 & \frac{Mr_{c1}r_1^{''}}{L_1L_2^{'}} & \frac{r_{c2}r_2^{''}}{L_2^{'}} \\ 0 & 0 & -\frac{r_2^{''}}{C_2} \end{bmatrix}$$

$$\mathbf{C}_3 = \begin{bmatrix} r_{c1}r_1^{''} & r_1^{''} & 0 & 0 \\ 0 & 0 & r_{c2}r_2^{''} & r_2^{''} \end{bmatrix} \quad \mathbf{D}_3 = \begin{bmatrix} 0 & -r_{c1}r_1^{''} & 0 \\ 0 & 0 & -r_{c2}r_2^{''} \end{bmatrix}$$

2.5.1.2 Average State-space Equation

Now the averaged state-space equation is written as

$$\frac{d\mathbf{x}}{dt} = \mathbf{Ax} + \mathbf{Bu} \quad \mathbf{y} = \mathbf{Cx} + \mathbf{Du}$$

where, the average state-space matrices is calculated using (2.12) and are given by

$$\mathbf{A} = \begin{bmatrix} \frac{-r_1^{'}}{L_1^{'}} & \frac{-r_1^{''}}{L_1^{'}} & \frac{-Mr_2^{'}}{L_2L_1^{'}} & \frac{-Mr_2^{''}}{L_2L_1^{'}} \\ \frac{r_1^{''}}{C_1} & \frac{-r_1^{''}}{C_1R_1} & 0 & 0 \\ \frac{-Mr_1^{'}}{L_1L_2^{'}} & \frac{-Mr_1^{''}}{L_1L_2^{'}} & \frac{-r_2^{'}}{L_2^{'}} & \frac{-r_2^{''}}{L_2^{'}} \\ 0 & 0 & \frac{r_2^{''}}{C_2} & \frac{-r_2^{''}}{C_2R_2} \end{bmatrix} \mathbf{B} = \begin{bmatrix} \frac{d_1+\frac{M}{L_2}d_2}{L_1^{'}} & \frac{r_{c1}r_1^{''}}{L_1^{'}} & \frac{Mr_{c2}r_2^{''}}{L_2L_1^{'}} \\ 0 & -\frac{r_1^{''}}{C_1} & 0 \\ \frac{d_2+\frac{M}{L_1}d_1}{L_2^{'}} & \frac{Mr_{c1}r_1^{''}}{L_1L_2^{'}} & \frac{r_{c2}r_2^{''}}{L_2^{'}} \\ 0 & 0 & -\frac{r_2^{''}}{C_2} \end{bmatrix}$$

$$\mathbf{C} = \begin{bmatrix} r_{c1}r_1^{''} & r_1^{''} & 0 & 0 \\ 0 & 0 & r_{c2}r_2^{''} & r_2^{''} \end{bmatrix} \mathbf{D} = \begin{bmatrix} 0 & -r_{c1}r_1^{''} & 0 \\ 0 & 0 & -r_{c2}r_2^{''} \end{bmatrix}$$

2.5.1.3 Small-signal Open-loop Transfer Functions of CI-SIDO Buck Converter

The open loop transfer functions of CI-SIDO buck converter are derived as follows:

Small-signal transfer functions between the state variable and input variables:

The small-signal open-loop transfer functions between the state variable and input variables are derived using (2.20) and is written as

$$\hat{\mathbf{x}}(s) = (s\mathbf{I} - \mathbf{A}_{av})^{-1}\mathbf{B}_{av}\hat{\mathbf{u}}(s)$$

which is expressed as

$$\begin{bmatrix} \hat{i}_{L1}(s) \\ \hat{v}_{C1}(s) \\ \hat{i}_{L2}(s) \\ \hat{v}_{C2}(s) \end{bmatrix} = \begin{bmatrix} s+\frac{r_1^{'}}{L_1^{'}} & \frac{r_1^{''}}{L_1^{'}} & \frac{Mr_2^{'}}{L_2L_1^{'}} & \frac{Mr_2^{''}}{L_2L_1^{'}} \\ \frac{-r_1^{''}}{C_1} & s+\frac{r_1^{''}}{C_1R_1} & 0 & 0 \\ \frac{Mr_1^{'}}{L_1L_2^{'}} & \frac{Mr_1^{''}}{L_1L_2^{'}} & s+\frac{r_2^{'}}{L_2^{'}} & \frac{r_2^{''}}{L_2^{'}} \\ 0 & 0 & \frac{-r_2^{''}}{C_2} & s+\frac{r_2^{''}}{C_2R_2} \end{bmatrix}^{-1} \begin{bmatrix} \frac{D_1+\frac{M}{L_2}D_2}{L_1^{'}} & \frac{r_{c1}r_1^{''}}{L_1^{'}} & \frac{Mr_{c2}r_2^{''}}{L_2L_1^{'}} \\ 0 & -\frac{r_1^{''}}{C_1} & 0 \\ \frac{D_2+\frac{M}{L_1}D_1}{L_2^{'}} & \frac{Mr_{c1}r_1^{''}}{L_1L_2^{'}} & \frac{r_{c2}r_2^{''}}{L_2^{'}} \\ 0 & 0 & -\frac{r_2^{''}}{C_2} \end{bmatrix} \begin{bmatrix} \hat{v}_{in}(s) \\ \hat{i}_{01}(s) \\ \hat{i}_{02}(s) \end{bmatrix} \tag{2.30}$$

Input voltage to inductor currents transfer functions: By solving the first and third line of (2.30), and making $\hat{i}_{01} = \hat{i}_{02} = 0$ we obtain the input voltage to inductor currents transfer functions as

$$\begin{aligned} G_{ig1} &= \frac{\hat{i}_{L1}}{\hat{v}_{in}} = \frac{(s + \frac{r_1^{''}}{C_1})}{L_1^{'} L_2} \frac{(s^2(L_2 D_1 + D_2 M) + s(r_2^{'} D_1 + \frac{L_2 D_1 + D_2 M}{C_2(R_2 + r_{c2})}) + \frac{D_1 R_2 r_2^{''}}{C_2})}{Dn_{bu}(s)} \\ G_{ig2} &= \frac{\hat{i}_{L2}}{\hat{v}_{in}} = \frac{(s + \frac{r_2^{''}}{C_2})}{L_1 L_2^{'}} \frac{(s^2(L_1 D_2 + D_1 M) + s(r_1^{'} D_2 + \frac{L_1 D_2 + D_1 M}{C_1(R_1 + r_{c1})}) + \frac{D_2 R_1 r_1^{''}}{C_1})}{Dn_{bu}(s)} \end{aligned} \tag{2.31}$$

where,

$$\begin{aligned} Dn_{bu}(s) = s^4 + s^3(\frac{r_1^{'}}{L_1^{'}} + \frac{r_2^{'}}{L_2^{'}} + \frac{r_1^{''}}{C_1} + \frac{r_2^{''}}{C_2}) + s^2(\frac{r_1^{'} r_2^{'}}{L_1 L_2^{'}} + \frac{R_2 r_2^{''}}{C_2 L_2^{'}} + \frac{R_1 r_1^{''}}{C_1 L_1^{'}} + \frac{r_2^{'} r_1^{''} L_1^{'}}{C_1} + \frac{r_1^{'} r_2^{''} L_2^{'}}{C_2} + \frac{r_2^{''} r_1^{''}}{C_1 C_2}) \\ + s(\frac{r_1^{'} r_2^{''} R_2}{L_1 L_2^{'} C_2} + \frac{r_2^{'} r_1^{''} R_1}{L_2 L_1^{'} C_1} + \frac{(L_1 R_2 + L_2 R_1) r_1^{''} r_2^{''}}{L_1 L_2^{'} C_1 C_2}) + \frac{R_1 R_2 r_1^{''} r_2^{''}}{L_1 L_2^{'} C_1 C_2} \end{aligned}$$

Load currents to inductor currents transfer functions: By solving first and third line of (2.30) and making the $\hat{v}_{in} = 0$ we obtain the load currents to inductor currents transfer functions as

$$\begin{aligned} H_{ii11} &= \frac{\hat{i}_{L1}}{\hat{i}_{01}} = \frac{r_1^{'}(s + \frac{1}{r_{c1} C_1})}{L_1^{'}} \frac{(s^2 + s(\frac{r_2^{'}}{L_2} + \frac{r_2^{''}}{C_2}) + \frac{R_2 r_2^{''}}{L_2 C_2})}{Dn_{bu}(s)} \\ H_{ii22} &= \frac{\hat{i}_{L2}}{\hat{i}_{02}} = \frac{r_2^{'}(s + \frac{1}{r_{c2} C_2})}{L_2^{'}} \frac{(s^2 + s(\frac{r_1^{'}}{L_1} + \frac{r_1^{''}}{C_1}) + \frac{R_1 r_1^{''}}{L_1 C_1})}{Dn_{bu}(s)} \end{aligned} \tag{2.32}$$

$$\begin{aligned} H_{ii12} &= \frac{\hat{i}_{L1}}{\hat{i}_{02}} = \frac{M r_2^{'}}{L_1^{'} L_2} \frac{s(s + \frac{1}{R_1 C_1})(s + \frac{1}{r_{c2} C_2})}{Dn_{bu}(s)} \\ H_{ii21} &= \frac{\hat{i}_{L2}}{\hat{i}_{01}} = \frac{M r_1^{'}}{L_1 L_2^{'}} \frac{s(s + \frac{1}{R_2 C_2})(s + \frac{1}{r_{c1} C_1})}{Dn_{bu}(s)} \end{aligned} \tag{2.33}$$

Small-signal transfer functions between the state variables and duty cycles:

The small-signal open-loop transfer functions between the state variables and duty cycles are derived using (2.21). In CI-SIDO buck $\mathbf{A}_1 = \mathbf{A}_2 = \mathbf{A}_3$, (2.21) becomes as

$$\hat{\mathbf{x}}(s) = (s\mathbf{I} - \mathbf{A}_{av})^{-1} \left([(\mathbf{B}_1 - \mathbf{B}_2)\mathbf{U}] \hat{d}_2(s) + [(\mathbf{B}_2 - \mathbf{B}_3)\mathbf{U}] \hat{d}_1(s) \right)$$

$$\implies \hat{\mathbf{x}}(s) = (s\mathbf{I} - \mathbf{A}_{av})^{-1} \begin{bmatrix} (\mathbf{B}_1 - \mathbf{B}_2)\mathbf{U} & (\mathbf{B}_2 - \mathbf{B}_3)\mathbf{U} \end{bmatrix} \begin{bmatrix} \hat{d}_2(s) \\ \hat{d}_1(s) \end{bmatrix}$$

and is expressed as

$$\begin{bmatrix} \hat{i}_{L1}(s) \\ \hat{v}_{C1}(s) \\ \hat{i}_{L2}(s) \\ \hat{v}_{C2}(s) \end{bmatrix} = \begin{bmatrix} s+\frac{r_1^{'}}{L_1^{'}} & \frac{r_1^{''}}{L_1^{'}} & \frac{Mr_2^{'}}{L_2L_1^{'}} & \frac{Mr_2^{''}}{L_2L_1^{'}} \\ \frac{-r_1^{''}}{C_1} & s+\frac{r_1^{''}}{C_1R_1} & 0 & 0 \\ \frac{Mr_1^{'}}{L_1L_2^{'}} & \frac{Mr_1^{''}}{L_1L_2^{'}} & s+\frac{r_2^{'}}{L_2^{'}} & \frac{r_2^{''}}{L_2^{'}} \\ 0 & 0 & \frac{-r_2^{''}}{C_2} & s+\frac{r_2^{''}}{C_2R_2} \end{bmatrix}^{-1} \begin{bmatrix} \frac{MV_{in}}{L_1L_2^{'}} & \frac{V_{in}}{L_1^{'}} \\ 0 & 0 \\ \frac{V_{in}}{L_2^{'}} & \frac{MV_{in}}{L_1L_2^{'}} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{d}_2(s) \\ \hat{d}_1(s) \end{bmatrix} \tag{2.34}$$

Duty cycles to inductor currents transfer functions: Solving first and third line of (2.34), we obtain the duty cycles to inductor currents transfer functions as

$$\begin{aligned} G_{id11} &= \frac{\hat{i}_{L1}}{\hat{d}_1} = \frac{V_{in}}{L_1^{'}}(s+\frac{r_1^{''}}{C_1})\frac{(s^2+s(\frac{r_2^{'}}{L_2}+\frac{r_2^{''}}{C_2})+\frac{R_2r_2^{''}}{L_2C_2})}{Dn_{bu}(s)} \\ G_{id22} &= \frac{\hat{i}_{L2}}{\hat{d}_2} = \frac{V_{in}}{L_2^{'}}(s+\frac{r_2^{''}}{C_2})\frac{(s^2+s(\frac{r_1^{'}}{L_1}+\frac{r_1^{''}}{C_1})+\frac{R_1r_1^{''}}{L_1C_1})}{Dn_{bu}(s)} \end{aligned} \tag{2.35}$$

Cross-coupling transfer functions between inductor current and duty cycles are

$$G_{id21} = \frac{\hat{i}_{L2}}{\hat{d}_1} = \frac{MV_{in}}{L_1^{'}L_2}\frac{s(s+\frac{r_1^{''}}{C_1})(s+\frac{r_2^{''}}{C_2})}{Dn_{bu}(s)}, \quad G_{id12} = \frac{\hat{i}_{L1}}{\hat{d}_2} = \frac{MV_{in}}{L_1L_2^{'}}\frac{s(s+\frac{r_2^{''}}{C_2})(s+\frac{r_1^{''}}{C_1})}{Dn_{bu}(s)} \tag{2.36}$$

Small-signal transfer functions between the output variable and input variables: The small-signal open-loop transfer functions between the output variables and input variables are derived using (2.22) and written as

$$\hat{\mathbf{y}}(s) = \left(\mathbf{C}_{av}(s\mathbf{I}-\mathbf{A}_{av})^{-1}\mathbf{B}_{av}+\mathbf{D}_{av}\right)\hat{\mathbf{u}}(s)$$

which is expressed as

$$\begin{bmatrix}\hat{v}_{01}(s)\\ \hat{v}_{02}(s)\end{bmatrix}=\begin{bmatrix}r_{c1}r_1^{''} & r_1^{''} & 0 & 0\\ 0 & 0 & r_{c2}r_2^{''} & r_2^{''}\end{bmatrix}\begin{bmatrix}s+\frac{r_1^{'}}{L_1^{'}} & \frac{r_1^{''}}{L_1^{'}} & \frac{Mr_2^{'}}{L_2L_1^{'}} & \frac{Mr_2^{''}}{L_2L_1^{'}}\\ \frac{-r_1^{''}}{C_1} & s+\frac{r_1^{''}}{C_1R_1} & 0 & 0\\ \frac{Mr_1^{'}}{L_1L_2^{'}} & \frac{Mr_1^{''}}{L_1L_2^{'}} & s+\frac{r_2^{'}}{L_2^{'}} & \frac{r_2^{''}}{L_2^{'}}\\ 0 & 0 & \frac{-r_2^{''}}{C_2} & s+\frac{r_2^{''}}{C_2R_2}\end{bmatrix}^{-1}$$
$$\begin{bmatrix}\frac{D_1+\frac{M}{L_2}D_2}{L_1^{'}} & \frac{r_{c1}r_1^{''}}{L_1^{'}} & \frac{Mr_{c2}r_2^{''}}{L_2L_1^{'}}\\ 0 & -\frac{r_1^{''}}{C_1} & 0\\ \frac{D_2+\frac{M}{L_1}D_1}{L_2^{'}} & \frac{Mr_{c1}r_1^{''}}{L_1L_2^{'}} & \frac{r_{c2}r_2^{''}}{L_2^{'}}\\ 0 & 0 & -\frac{r_2^{''}}{C_2}\end{bmatrix}+\begin{bmatrix}0 & -r_{c1}r_1^{''} & 0\\ 0 & 0 & -r_{c2}r_2^{''}\end{bmatrix}\begin{bmatrix}\hat{v}_{in}(s)\\ \hat{i}_{01}(s)\\ \hat{i}_{02}(s)\end{bmatrix} \tag{2.37}$$

Input voltage to output voltage transfer functions: The input voltage to output voltage transfer functions is also called as audio-susceptibility and is found by solving (2.37), making the $\hat{i}_{01}=\hat{i}_{02}=0$ and is given by:

$$\begin{aligned}G_{vg1}=\frac{\hat{v}_{01}}{\hat{v}_{in}}&=\frac{r_1^{'}(s+\frac{1}{r_{c1}C_1})}{L_1^{'}L_2}\frac{(s^2(L_2D_1+D_2M)+s(r_2^{'}D_1+\frac{L_2D_1+D_2M}{C_2(R_2+r_{c2})})+\frac{D_1R_2r_2^{''}}{C_2})}{Dn_{bu}(s)}\\ G_{vg2}=\frac{\hat{v}_{02}}{\hat{v}_{in}}&=\frac{r_2^{'}(s+\frac{1}{r_{c2}C_2})}{L_1L_2^{'}}\frac{(s^2(L_1D_2+D_1M)+s(r_1^{'}D_2+\frac{L_1D_2+D_1M}{C_1(R_1+r_{c1})})+\frac{D_2R_1r_1^{''}}{C_1})}{Dn_{bu}(s)}\end{aligned} \tag{2.38}$$

Load currents to output voltage transfer functions: The load current to output voltage transfer function is also called as load regulation transfer function. In CI-SIDO converter load regulation is divided into self-regulation and cross-regulation. The load regulation transfer function are found by solving (2.37), making the $\hat{v}_{in}=0$ and are given as follows

Self-regulation transfer functions:

$$\begin{aligned}Z_{vi11}=\frac{\hat{v}_{01}}{\hat{i}_{01}}&=-r_1^{'}s(s+\frac{1}{r_{c1}C_1})\frac{(s^2+s(\frac{r_2^{'}}{L_2^{'}}+\frac{r_2^{''}}{C_2})+\frac{R_2r_2^{''}}{L_2^{'}C_2})}{Dn_{bu}(s)}\\ Z_{vi22}=\frac{\hat{v}_{01}}{\hat{i}_{02}}&=-r_2^{'}s(s+\frac{1}{r_{c2}C_2})\frac{(s^2+s(\frac{r_1^{'}}{L_1^{'}}+\frac{r_1^{''}}{C_1})+\frac{R_1r_1^{''}}{L_1^{'}C_1})}{Dn_{bu}(s)}\end{aligned} \tag{2.39}$$

Cross-regulation transfer functions:

$$\begin{aligned} Z_{vi12} &= \frac{\hat{v}_{01}}{\hat{i}_{02}} = \frac{Mr_2^{'}r_1^{'}}{L_1^{'}L_2}\frac{s(s+\frac{1}{r_{c1}C_1})(s+\frac{1}{r_{c2}C_2})}{Dn_{bu}(s)} \\ Z_{vi21} &= \frac{\hat{v}_{02}}{\hat{i}_{01}} = \frac{Mr_1^{'}r_2^{'}}{L_1L_2^{'}}\frac{s(s+\frac{1}{r_{c2}C_2})(s+\frac{1}{r_{c1}C_1})}{Dn_{bu}(s)} \end{aligned} \tag{2.40}$$

Small-signal transfer functions between the output variables and duty cycles:

The small-signal open-loop transfer functions between the output variables and duty cycles can be obtained from (2.23). In CI-SIDO buck converter $\mathbf{A}_1 = \mathbf{A}_2 = \mathbf{A}_3$, $\mathbf{C}_1 = \mathbf{C}_2 = \mathbf{C}_3$, $\mathbf{D}_1 = \mathbf{D}_2 = \mathbf{D}_3$, and thus (2.23) becomes

$$\hat{\mathbf{y}}(s) = (\mathbf{C}_{av}(s\mathbf{I} - \mathbf{A}_{av})^{-1}[(\mathbf{B}_1 - \mathbf{B}_2)\mathbf{U}])\hat{d}_2(s) + (\mathbf{C}_{av}(s\mathbf{I} - \mathbf{A}_{av})^{-1}[(\mathbf{B}_2 - \mathbf{B}_3)\mathbf{U}])\hat{d}_1(s)$$

$$\implies \hat{\mathbf{Y}}(s) = \mathbf{C}_{av}(s\mathbf{I} - \mathbf{A}_{av})^{-1}\begin{bmatrix}(\mathbf{B}_1 - \mathbf{B}_2)\mathbf{U} & (\mathbf{B}_2 - \mathbf{B}_3)\mathbf{U}\end{bmatrix}\begin{bmatrix}\hat{d}_2(s) \\ \hat{d}_1(s)\end{bmatrix}$$

and is expressed as

$$\begin{bmatrix}\hat{v}_{01}(s) \\ \hat{v}_{02}(s)\end{bmatrix} = \begin{bmatrix} r_{c1}r_1^{''} & r_1^{''} & 0 & 0 \\ 0 & 0 & r_{c2}r_2^{''} & r_2^{''}\end{bmatrix}\begin{bmatrix} s+\frac{r_1^{'}}{L_1^{'}} & \frac{r_1^{''}}{L_1^{'}} & \frac{Mr_2^{'}}{L_2L_1^{'}} & \frac{Mr_2^{''}}{L_2L_1^{'}} \\ \frac{-r_1^{''}}{C_1} & s+\frac{r_1^{''}}{C_1R_1} & 0 & 0 \\ \frac{Mr_1^{'}}{L_1L_2^{'}} & \frac{Mr_1^{''}}{L_1L_2^{'}} & s+\frac{r_2^{'}}{L_2^{'}} & \frac{r_2^{''}}{L_2^{'}} \\ 0 & 0 & \frac{-r_2^{''}}{C_2} & s+\frac{r_2^{''}}{C_2R_2}\end{bmatrix}^{-1} \times \begin{bmatrix}\frac{MV_{in}}{L_1L_2(1-k^2)} & \frac{V_{in}}{L_1(1-k^2)} \\ 0 & 0 \\ \frac{V_{in}}{L_2(1-k^2)} & \frac{MV_{in}}{L_1L_2(1-k^2)} \\ 0 & 0\end{bmatrix}\begin{bmatrix}\hat{d}_2(s) \\ \hat{d}_1(s)\end{bmatrix} \tag{2.41}$$

solving we obtain duty-cycle to output voltage transfer functions as

$$\begin{aligned} G_{vd11} &= \frac{\hat{v}_{01}}{\hat{d}_1} = \frac{V_{in}r_1^{'}}{L_1^{'}}(s+\frac{1}{r_{c1}C_1})\frac{(s^2+s(\frac{r_2^{'}}{L_2}+\frac{r_2^{''}}{C_2})+\frac{R_2r_2^{''}}{L_2C_2})}{Dn_{bu}(s)} \\ G_{vd22} &= \frac{\hat{v}_{02}}{\hat{d}_2} = \frac{V_{in}r_2^{'}}{L_2^{'}}(s+\frac{1}{r_{c2}C_2})\frac{(s^2+s(\frac{r_1^{'}}{L_1}+\frac{r_1^{''}}{C_1})+\frac{R_1r_1^{''}}{L_1C_1})}{Dn_{bu}(s)} \end{aligned} \tag{2.42}$$

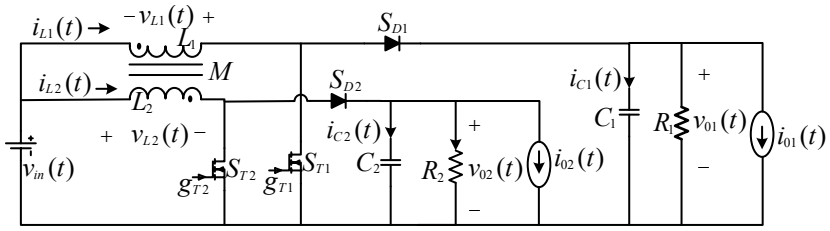


Figure 2.11: Circuit diagram of CI-SIDO boost converter

Cross-coupling transfer functions:

$$G_{vd21} = \frac{\hat{v}_{02}}{\hat{d}_1} = \frac{MV_{in}r_2'}{L_1L_2'}\frac{s(s+\frac{1}{r_{c2}C_2})(s+\frac{r_1''}{C_1})}{Dn_{bu}(s)} \tag{2.43}$$

$$G_{vd12} = \frac{\hat{v}_{01}}{\hat{d}_2} = \frac{MV_{in}r_1'}{L_2L_1'}\frac{s(s+\frac{1}{r_{c1}C_1})(s+\frac{r_2''}{C_2})}{Dn_{bu}(s)} \tag{2.44}$$

2.5.2 Small-signal Modelling of CI-SIDO Boost Converter

The small-signal modelling of CI-SIDO boost converter is obtained considering ideal condition. Figure 2.11 shows the circuit diagram of CI-SIDO boost converter.

2.5.2.1 State-space Equation

Considering Case A ($D_1 > D_2$), the CI-SIDO boost converter has three modes of operation. The state-space equation for all the operating modes are given as follows:

Mode I: d_2T_s **interval**

The equivalent circuit for this interval is shown in Figure 2.12. Applying KVL and KCL in the equivalent circuit of d_2T_s interval gives:

$$\begin{aligned} L_1'\tfrac{di_{L1}(t)}{dt} &= v_{in}(t) + \tfrac{M}{L_2}v_{in}(t) \\ C_1\tfrac{dv_{01}(t)}{dt} &= \tfrac{-v_{01}(t)}{R_1} - i_{01}(t) \\ L_2'\tfrac{di_{L2}(t)}{dt} &= v_{in}(t) + \tfrac{M}{L_1}v_{in}(t) \\ C_2\tfrac{dv_{02}(t)}{dt} &= \tfrac{-v_{02}(t)}{R_2} - i_{02}(t) \end{aligned} \tag{2.45}$$

leading to state-space equation of the d_2T_s interval:

$$\frac{d\mathbf{x}(t)}{dt} = \mathbf{A}_1\mathbf{x}(t) + \mathbf{B}_1\mathbf{u}(t) \quad , \quad \mathbf{y}(t) = \mathbf{C}_1\mathbf{x}(t) + \mathbf{D}_1\mathbf{u}(t)$$

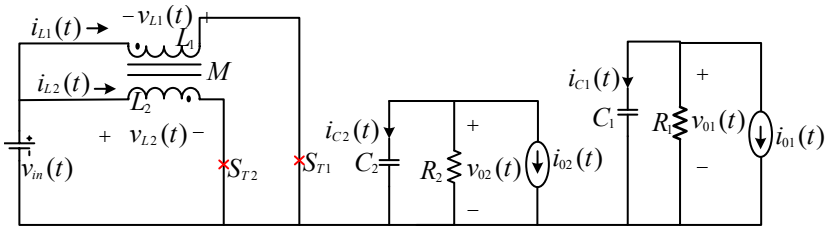


Figure 2.12: Mode I circuit configuration of CI-SIDO boost converter

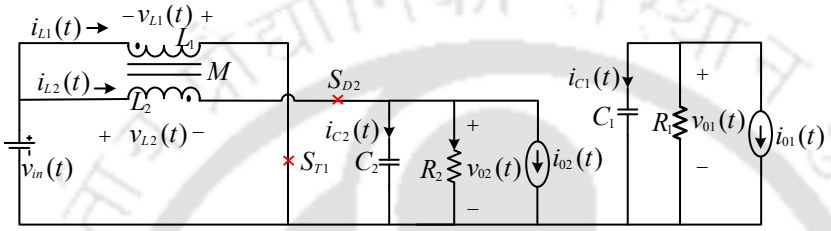


Figure 2.13: Mode II circuit configuration of CI-SIDO boost converter

$$\mathbf{A}_1 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & \frac{-1}{C_1 R_1} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{C_2 R_2} \end{bmatrix} \quad \mathbf{B}_1 = \begin{bmatrix} \frac{1}{L_1'}(1+\frac{M}{L_2}) & 0 & 0 \\ 0 & -\frac{1}{C_1} & 0 \\ \frac{1}{L_2'}(1+\frac{M}{L_1}) & 0 & 0 \\ 0 & 0 & -\frac{1}{C_2} \end{bmatrix} \quad \mathbf{C}_1 = \begin{bmatrix} 0\ 1\ 0\ 0 \\ 0\ 0\ 0\ 1 \end{bmatrix} \quad \mathbf{D}_1 = \begin{bmatrix} 0\ 0\ 0 \\ 0\ 0\ 0 \end{bmatrix}$$

Mode II: $(d_1 - d_2)T_s$ **interval**

The equivalent circuit for this interval is shown in Figure 2.13. Applying KVL and KCL in the equivalent circuit of $(d_1 - d_2)T_s$ interval gives:

$$\begin{aligned} L_1' \frac{di_{L1}(t)}{dt} &= v_{in}(t) + \frac{M}{L_2}(v_{in}(t) - v_{02}(t)) \\ C_1 \frac{dv_{01}(t)}{dt} &= -\frac{v_{01}(t)}{R_1} - i_{01}(t) \\ L_2' \frac{di_{L2}(t)}{dt} &= v_{in}(t) - v_{02}(t) + \frac{M}{L_1} v_{in}(t) \\ C_2 \frac{dv_{02}(t)}{dt} &= i_{L2}(t) - \frac{v_{02}(t)}{R_2} - i_{02}(t) \end{aligned} \tag{2.46}$$

leading to state-space equation of the $(d_1 - d_2)T_s$ interval:

$$\frac{d\mathbf{x}(t)}{dt} = \mathbf{A}_2\mathbf{x}(t) + \mathbf{B}_2\mathbf{u}(t) \quad \mathbf{y}(t) = \mathbf{C}_2\mathbf{x}(t) + \mathbf{D}_2\mathbf{u}(t)$$

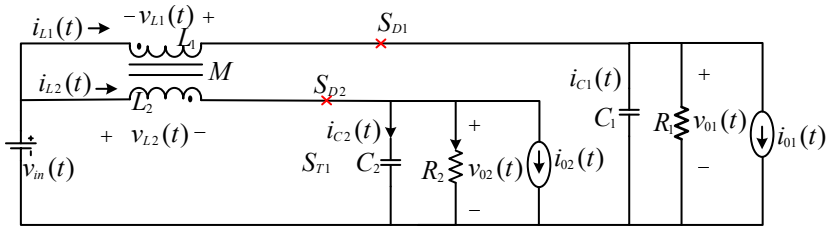


Figure 2.14: Mode III circuit configuration of CI-SIDO boost converter

$$\mathbf{A}_2 = \begin{bmatrix} 0 & 0 & 0 & \frac{-M}{L_2L_1'} \\ 0 & \frac{-1}{C_1R_1} & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{L_2'} \\ 0 & 0 & \frac{1}{C_2} & \frac{-1}{C_2R_2} \end{bmatrix} \quad \mathbf{B}_2 = \begin{bmatrix} \frac{1}{L_1'}(1+\frac{M}{L_2}) & 0 & 0 \\ 0 & -\frac{1}{C_1} & 0 \\ \frac{1}{L_2'}(1+\frac{M}{L_1}) & 0 & 0 \\ 0 & 0 & -\frac{1}{C_2} \end{bmatrix} \quad \mathbf{C}_2 = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \quad \mathbf{D}_2 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

Mode III: $(1-d_1)T_s$ **interval**

The equivalent circuit for this interval is shown in Figure 2.14. Applying KVL and KCL in the equivalent circuit of $(1-d_1)T_s$ interval gives:

$$\begin{aligned} L_1'\tfrac{di_{L1}(t)}{dt} &= v_{in}(t) - v_{01}(t) + \tfrac{M}{L_2}(v_{in}(t) - v_{02}(t)) \\ C_1\tfrac{dv_{01}(t)}{dt} &= i_{L1}(t) - \tfrac{v_{01}(t)}{R_1} - i_{01}(t) \\ L_2'\tfrac{di_{L2}(t)}{dt} &= v_{in}(t) - v_{02}(t) + \tfrac{M}{L_1}(v_{in}(t) - v_{01}(t)) \\ C_2\tfrac{dv_{02}(t)}{dt} &= i_{L2}(t) - \tfrac{v_{02}(t)}{R_2} - i_{02}(t) \end{aligned} \tag{2.47}$$

leading to state-space equation of the $(1-d_1)T_s$ interval:

$$\frac{d\mathbf{x}(t)}{dt} = \mathbf{A}_3\mathbf{x}(t) + \mathbf{B}_3\mathbf{u}(t) \quad \mathbf{y}(t) = \mathbf{C}_3\mathbf{x}(t) + \mathbf{D}_3\mathbf{u}(t)$$

$$\mathbf{A}_3 = \begin{bmatrix} 0 & \frac{-1}{L_1'} & 0 & \frac{-M}{L_2L_1'} \\ \frac{1}{C_1} & \frac{-1}{C_1R_1} & 0 & 0 \\ 0 & \frac{-M}{L_1L_2'} & 0 & \frac{-1}{L_2'} \\ 0 & 0 & \frac{1}{C_2} & \frac{-1}{C_2R_2} \end{bmatrix} \quad \mathbf{B}_3 = \begin{bmatrix} \frac{1}{L_1'}(1+\frac{M}{L_2}) & 0 & 0 \\ 0 & -\frac{1}{C_1} & 0 \\ \frac{1}{L_2'}(1+\frac{M}{L_1}) & 0 & 0 \\ 0 & 0 & -\frac{1}{C_2} \end{bmatrix} \quad \mathbf{C}_3 = \mathbf{C}_1 \quad \mathbf{D}_3 = \mathbf{D}_1$$

2.5.2.2 Average State-space Equation

Now the averaged state-space equation is written as

$$\frac{d\mathbf{x}}{dt} = \mathbf{Ax} + \mathbf{Bu} \quad \mathbf{y} = \mathbf{Cx} + \mathbf{Du}$$

where, the average state-space matrices is calculated using (2.12) and are given by

$$\mathbf{A} = \begin{bmatrix} 0 & -\frac{(1-d_1)}{L_1'} & 0 & -\frac{M(1-d_2)}{L_2L_1'} \\ \frac{1-d_1}{C_1} & -\frac{1}{C_1R_1} & 0 & 0 \\ 0 & -\frac{M(1-d_1)}{L_1L_2'} & 0 & -\frac{(1-d_2)}{L_2'} \\ 0 & 0 & \frac{1-d_2}{C_2} & -\frac{1}{C_2R_2} \end{bmatrix} \mathbf{B} = \begin{bmatrix} \frac{1}{L_1'}(1+\frac{M}{L_2}) & 0 & 0 \\ 0 & -\frac{1}{C_1} & 0 \\ \frac{1}{L_2'}(1+\frac{M}{L_1}) & 0 & 0 \\ 0 & 0 & -\frac{1}{C_2} \end{bmatrix}$$

$$\mathbf{C} = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \quad \mathbf{D} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

2.5.2.3 Small-signal Open-loop Transfer Functions of CI-SIDO Boost Converter

The open loop transfer functions of CI-SIDO boost converter are derived as follows:

Small-signal transfer functions between the state variable and input variables:

The small-signal open-loop transfer functions between the state variable and input variables are derived using (2.20) and is written as

$$\hat{\mathbf{x}}(s) = (s\mathbf{I} - \mathbf{A}_{av})^{-1}\mathbf{B}_{av}\hat{\mathbf{u}}(s)$$

which is expressed as

$$\begin{bmatrix} \hat{i}_{L1}(s) \\ \hat{v}_{C1}(s) \\ \hat{i}_{L2}(s) \\ \hat{v}_{C2}(s) \end{bmatrix} = \begin{bmatrix} s & \frac{(1-D_1)}{L_1'} & 0 & \frac{M(1-D_2)}{L_2L_1'} \\ -\frac{1-D_1}{C_1} & s+\frac{1}{C_1R_1} & 0 & 0 \\ 0 & \frac{M(1-D_1)}{L_1L_2'} & s & \frac{(1-D_2)}{L_2'} \\ 0 & 0 & -\frac{1-D_2}{C_2} & s+\frac{1}{C_2R_2} \end{bmatrix}^{-1} \begin{bmatrix} \frac{1}{L_1'}(1+\frac{M}{L_2}) & 0 & 0 \\ 0 & -\frac{1}{C_1} & 0 \\ \frac{1}{L_2'}(1+\frac{M}{L_1}) & 0 & 0 \\ 0 & 0 & -\frac{1}{C_2} \end{bmatrix} \begin{bmatrix} \hat{v}_{in}(s) \\ \hat{i}_{01}(s) \\ \hat{i}_{02}(s) \end{bmatrix} \tag{2.48}$$

Input voltage to inductor currents transfer functions: By solving the first and third line of (2.48) and making the $\hat{i}_{01} = \hat{i}_{02} = 0$, we obtain the input voltage to inductor currents transfer functions as

$$\begin{aligned} G_{ig1} &= \frac{\hat{i}_{L1}}{\hat{v}_{in}} = \frac{1}{L_1'} \frac{(s + \frac{1}{R_1C_1})(s^2 + \frac{s}{R_2C_2} + \frac{(1-D_2)^2}{L_2C_2} + \frac{M}{L_2}(s^2 + \frac{s}{R_2C_2}))}{Dn_{bo}(s)} \\ G_{ig2} &= \frac{\hat{i}_{L2}}{\hat{v}_{in}} = \frac{1}{L_2'} \frac{(s + \frac{1}{R_2C_2})(s^2 + \frac{s}{R_1C_1} + \frac{(1-D_1)^2}{L_1C_1} + \frac{M}{L_1}(s^2 + \frac{s}{R_1C_1}))}{Dn_{bo}(s)} \end{aligned} \tag{2.49}$$

where,

$$\begin{aligned} Dn_{bo}(s) = s^4 + (\frac{1}{R_1C_1} + \frac{1}{R_2C_2})s^3 + (\frac{(1-D_1)^2}{L_1'C_1} + \frac{(1-D_2)^2}{L_2'C_2} + \frac{1}{R_1R_2C_1C_2})s^2 \\ + (\frac{(1-D_1)^2}{L_1'C_1R_2C_2} + \frac{(1-D_2)^2}{L_2'C_2R_1C_1})s + \frac{(1-D_1)^2(1-D_2)^2}{L_1'L_2C_1C_2} \end{aligned}$$

Load currents to Inductor currents transfer functions: By solving the first and third line of (2.48) and making the $\hat{v}_{in} = 0$, we obtain the load currents to inductor currents transfer functions and are given by

$$\begin{aligned} H_{ii11} &= \frac{\hat{i}_{L1}}{\hat{i}_{01}} = \frac{1-D_1}{L_1'C_1} \frac{(s^2 + \frac{s}{R_2C_2} + \frac{(1-D_2)^2}{L_2C_2})}{Dn_{bo}(s)} \\ H_{ii22} &= \frac{\hat{i}_{L2}}{\hat{i}_{02}} = \frac{1-D_2}{L_2'C_2} \frac{(s^2 + \frac{s}{R_1C_1} + \frac{(1-D_1)^2}{L_1C_1})}{Dn_{bo}(s)} \\ H_{ii12} &= \frac{\hat{i}_{L1}}{\hat{i}_{02}} = \frac{M(1-D_2)}{L_2L_1'C_2} \frac{s(s + \frac{1}{R_1C_1})}{Dn_{bo}(s)} \\ H_{ii21} &= \frac{\hat{i}_{L2}}{\hat{i}_{01}} = \frac{M(1-D_1)}{L_1L_2'C_1} \frac{s(s + \frac{1}{R_2C_2})}{Dn_{bo}(s)} \end{aligned} \tag{2.50}$$

Small-signal transfer functions between the state variables and duty cycles:

The small-signal open-loop transfer functions between the state variables and duty cycles are derived using (2.21). In CI-SIDO boost $\mathbf{B}_1 = \mathbf{B}_2 = \mathbf{B}_3$, (2.21) becomes as

$$\hat{\mathbf{x}}(s) = (s\mathbf{I} - \mathbf{A}_{av})^{-1} \Big([(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X}]\hat{d}_2(s) + [(\mathbf{A}_2 - \mathbf{A}_3)\mathbf{X}]\hat{d}_1(s) \Big)$$

$$\implies \hat{\mathbf{x}}(s) = (s\mathbf{I} - \mathbf{A}_{av})^{-1} \begin{bmatrix} (\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} & (\mathbf{A}_2 - \mathbf{A}_3)\mathbf{X} \end{bmatrix} \begin{bmatrix} \hat{d}_2(s) \\ \hat{d}_1(s) \end{bmatrix}$$

and is expressed as

$$\begin{bmatrix} \hat{i}_{L1}(s) \\ \hat{v}_{C1}(s) \\ \hat{i}_{L2}(s) \\ \hat{v}_{C2}(s) \end{bmatrix} = \begin{bmatrix} s & \frac{(1-D_1)}{L_1'} & 0 & \frac{M(1-D_2)}{L_2L_1'} \\ -\frac{1-D_1}{C_1} & s+\frac{1}{C_1R_1} & 0 & 0 \\ 0 & \frac{M(1-D_1)}{L_1L_2'} & s & \frac{(1-D_2)}{L_2'} \\ 0 & 0 & -\frac{1-D_2}{C_2} & s+\frac{1}{C_2R_2} \end{bmatrix}^{-1} \begin{bmatrix} \frac{MV_{in}}{L_2L_1'(1-D_2)} & \frac{V_{in}}{L_1'(1-D_2)} \\ 0 & \frac{-V_{in}}{R_1C_1(1-D_1)^2} \\ \frac{V_{in}}{L_2'(1-D_2)} & \frac{MV_{in}}{L_1L_2'(1-D_1)} \\ \frac{-V_{in}}{R_2C_2(1-D_2)^2} & 0 \end{bmatrix} \begin{bmatrix} \hat{d}_2(s) \\ \hat{d}_1(s) \end{bmatrix} \tag{2.51}$$

Duty cycles to Inductor currents transfer functions: Solving first and third line of (2.51), we obtain the duty cycles to inductor currents transfer functions as

$$G_{id11} = \frac{\hat{i}_{L1}}{\hat{d}_1} = \frac{V_{in}}{L_1'(1-D_1)} \frac{(s+\frac{2}{R_1C_1})(s^2+\frac{1}{R_2C_2}+\frac{(1-D_2)^2}{L_2C_2})}{Dn_{bo}(s)} \tag{2.52}$$

$$G_{id22} = \frac{\hat{i}_{L2}}{\hat{d}_2} = \frac{V_{in}}{L_2'(1-D_2)} \frac{(s+\frac{2}{R_2C_2})(s^2+\frac{1}{R_1C_1}+\frac{(1-D_1)^2}{L_1C_1})}{Dn_{bo}(s)} \tag{2.53}$$

$$G_{id12} = \frac{\hat{i}_{L1}}{\hat{d}_2} = \frac{MV_{in}}{L_2L_1'(1-D_2)} \frac{s(s+\frac{1}{R_1C_1})(s+\frac{2}{R_2C_2})}{Dn_{bo}(s)} \tag{2.54}$$

$$G_{id21} = \frac{\hat{i}_{L2}}{\hat{d}_1} = \frac{MV_{in}}{L_1L_2'(1-D_1)} \frac{s(s+\frac{1}{R_2C_2})(s+\frac{2}{R_1C_1})}{Dn_{bo}(s)} \tag{2.55}$$

Small-signal transfer functions between the output variables and input variables: The small-signal open-loop transfer functions between the output variables and input variables are derived using (2.22) and is written as

$$\hat{\mathbf{y}}(s) = \left(\mathbf{C}_{av}(s\mathbf{I}-\mathbf{A}_{av})^{-1}\mathbf{B}_{av}+\mathbf{D}_{av}\right)\hat{\mathbf{u}}(s)$$

which is expressed as

$$\begin{bmatrix} \hat{v}_{01}(s) \\ \hat{v}_{02}(s) \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} s & \frac{(1-D_1)}{L_1'} & 0 & \frac{M(1-D_2)}{L_2L_1'} \\ \frac{-1-D_1}{C_1} & s+\frac{1}{C_1R_1} & 0 & 0 \\ 0 & \frac{M(1-D_1)}{L_1L_2'} & s & \frac{(1-D_2)}{L_2'} \\ 0 & 0 & -\frac{1-D_2}{C_2} & s+\frac{1}{C_2R_2} \end{bmatrix}^{-1} \begin{bmatrix} \frac{(1+\frac{M}{L_2})}{L_1'} & 0 & 0 \\ 0 & \frac{-1}{C_1} & 0 \\ \frac{(1+\frac{M}{L_1})}{L_2'} & 0 & 0 \\ 0 & 0 & \frac{-1}{C_2} \end{bmatrix} \begin{bmatrix} \hat{v}_{in}(s) \\ \hat{i}_{01}(s) \\ \hat{i}_{02}(s) \end{bmatrix} \tag{2.56}$$

Input voltage to output voltage (Audio-susceptibility) transfer functions: The input voltage to output voltage transfer functions are found by solving (2.56), making the $\hat{i}_{01} = \hat{i}_{02} = 0$ and is given by:

$$\begin{aligned} G_{vg1} &= \frac{\hat{v}_{01}}{\hat{v}_{in}} = \frac{1-D_1}{L_1'C_1}\frac{(s^2 + \frac{s}{R_2C_2} + \frac{(1-D_2)^2}{L_2C_2} + \frac{M}{L_2}(s^2 + \frac{s}{R_2C_2}))}{Dn_{bo}(s)} \\ G_{vg2} &= \frac{\hat{v}_{02}}{\hat{v}_{in}} = \frac{1-D_2}{L_2'C_2}\frac{(s^2 + \frac{s}{R_1C_1} + \frac{(1-D_1)^2}{L_1C_1} + \frac{M}{L_1}(s^2 + \frac{s}{R_1C_1}))}{Dn_{bo}(s)} \end{aligned} \tag{2.57}$$

Load current to output voltage (Load Regulation) transfer functions: The load currents to output transfer functions are found by solving (2.56), making the $\hat{v}_{in} = 0$ and is given by:
Self-regulation transfer functions:

$$\begin{aligned} Z_{vi11} &= \frac{\hat{v}_{01}}{\hat{i}_{01}} = \frac{-s}{C_1}\frac{(s^2 + \frac{s}{R_2C_2} + \frac{(1-D_2)^2}{L_2'C_2})}{Dn_{bo}(s)} \\ Z_{vi22} &= \frac{\hat{v}_{02}}{\hat{i}_{02}} = \frac{-s}{C_2}\frac{(s^2 + \frac{s}{R_1C_1} + \frac{(1-D_1)^2}{L_1C_1})}{Dn_{bo}(s)} \end{aligned} \tag{2.58}$$

Cross-regulation transfer function:

$$\begin{aligned} Z_{vi12} &= \frac{\hat{v}_{01}}{\hat{i}_{02}} = \frac{M(1-D_1)(1-D_2)}{L_2L_1'C_1C_2}\frac{s}{Dn_{bo}(s)} \\ Z_{vi21} &= \frac{\hat{v}_{02}}{\hat{i}_{01}} = \frac{M(1-D_1)(1-D_2)}{L_1L_2'C_1C_2}\frac{s}{Dn_{bo}(s)} \end{aligned} \tag{2.59}$$

Small-signal transfer functions between the output variable and duty cycles:
The small-signal open-loop transfer functions between the output variables and duty cycles can be obtained from (2.23). In CI-SIDO boost $\mathbf{B}_1 = \mathbf{B}_2 = \mathbf{B}_3$, $\mathbf{C}_1 = \mathbf{C}_2 = \mathbf{C}_3$, $\mathbf{D}_1 = \mathbf{D}_2 = \mathbf{D}_3$, (2.23) becomes

$$\hat{\mathbf{y}}(s) = (\mathbf{C}_{av}(s\mathbf{I} - \mathbf{A}_{av})^{-1}[(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X}])\hat{d}_2(s) + (\mathbf{C}_{av}(s\mathbf{I} - \mathbf{A}_{av})^{-1}[(\mathbf{A}_2 - \mathbf{A}_3)\mathbf{X}])\hat{d}_1(s)$$

$$\implies \hat{\mathbf{y}}(s) = \mathbf{C}_{av}(s\mathbf{I} - \mathbf{A}_{av})^{-1}\begin{bmatrix}(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} & (\mathbf{A}_2 - \mathbf{A}_3)\mathbf{X}\end{bmatrix}\begin{bmatrix}\hat{d}_2(s) \\ \hat{d}_1(s)\end{bmatrix}$$

and is expressed as

$$\begin{bmatrix}\hat{v}_{01}(s)\\ \hat{v}_{02}(s)\end{bmatrix} = \begin{bmatrix}0 & 1 & 0 & 0\\ 0 & 0 & 0 & 1\end{bmatrix} \begin{bmatrix} s & \frac{(1-D_1)}{L_1'} & 0 & \frac{M(1-D_2)}{L_2L_1'}\\ -\frac{1-D_1}{C_1} & s+\frac{1}{C_1R_1} & 0 & 0\\ 0 & \frac{M(1-D_1)}{L_1L_2'} & s & \frac{(1-D_2)}{L_2'}\\ 0 & 0 & -\frac{1-D_2}{C_2} & s+\frac{1}{C_2R_2}\end{bmatrix}^{-1} \times \begin{bmatrix}\frac{MV_{in}}{L_2L_1'(1-D_2)} & \frac{V_{in}}{L_1'(1-D_2)}\\ 0 & \frac{-V_{in}}{R_1C_1(1-D_1)^2}\\ \frac{V_{in}}{L_2'(1-D_2)} & \frac{MV_{in}}{L_1L_2'(1-D_1)}\\ \frac{-V_{in}}{R_2C_2(1-D_2)^2} & 0\end{bmatrix} \begin{bmatrix}\hat{d}_2(s)\\ \hat{d}_1(s)\end{bmatrix} \tag{2.60}$$

Duty cycles to output voltages transfer functions: Solving (2.60), we obtain the duty cycles to output voltages transfer functions as

$$\begin{aligned} G_{vd11} &= \frac{\hat{v}_{01}}{\hat{d}_1} = \frac{V_{in}}{L_1'C_1}\frac{(s^2+\frac{s}{R_2C_2}+\frac{(1-D_2)^2}{L_2'C_2})(\frac{-L_1's}{R_1(1-D_1)^2}+1)-\frac{M^2(1-D_2)^2}{L_1L_2L_2'C_2}}{Dn_{bo}(s)}\\ G_{vd22} &= \frac{\hat{v}_{02}}{\hat{d}_2} = \frac{V_{in}}{L_2'C_2}\frac{(s^2+\frac{s}{R_1C_1}+\frac{(1-D_1)^2}{L_1'C_1})(\frac{-L_2's}{R_2(1-D_2)^2}+1)-\frac{M^2(1-D_1)^2}{L_1L_2L_1'C_1}}{Dn_{bo}(s)} \end{aligned} \tag{2.61}$$

Cross-coupling transfer functions:

$$\begin{aligned} G_{vd12} &= \frac{\hat{v}_{01}}{\hat{d}_2} = \frac{MV_{in}(1-D_1)}{L_2L_1'C_1(1-D_2)}\frac{s(s+\frac{2}{R_2C_2})}{Dn_{bo}(s)}\\ G_{vd21} &= \frac{\hat{v}_{02}}{\hat{d}_1} = \frac{MV_{in}(1-D_2)}{L_1L_2'C_2(1-D_1)}\frac{s(s+\frac{2}{R_1C_1})}{Dn_{bo}(s)} \end{aligned} \tag{2.62}$$

2.5.3 Small-signal Modelling of CI-SIDO Boost and Buck Converter

The small-signal modelling of CI-SIDO boost and buck converter is obtained considering ideal condition. Figure 2.15 shows the circuit diagram of CI-SIDO boost and buck converter.

2.5.3.1 State-space Equation

Considering Case A ($D_1 > D_2$), the CI-SIDO boost and buck converter has three modes of operation. The state space equation for all the operational modes are given as follows:

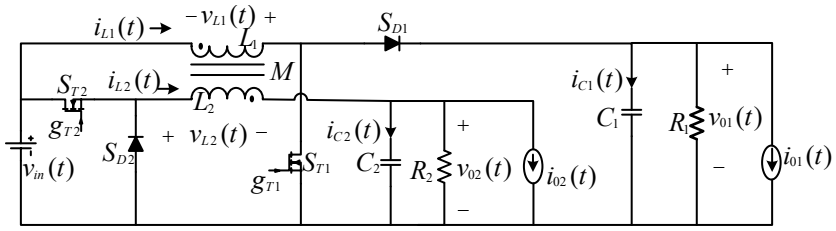


Figure 2.15: Circuit diagram CI-SIDO boost and buck converter

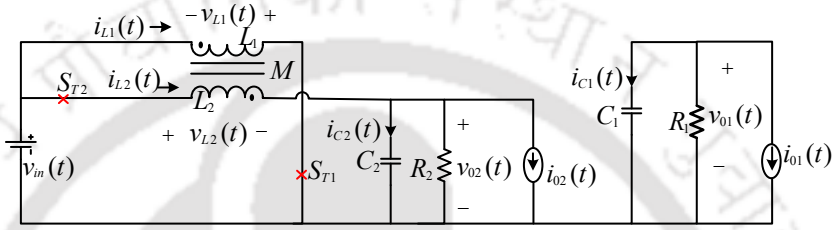


Figure 2.16: Mode I circuit configuration of CI-SIDO boost and buck converter

Mode I: d_2T_s interval

The equivalent circuit for this interval is shown in Figure 2.16. Applying KVL and KCl in the equivalent circuit of d_2T_s interval gives:

$$\begin{aligned} L_1' \frac{di_{L1}(t)}{dt} &= v_{in}(t) + \frac{M}{L_2}(v_{in}(t) - v_{02}(t)) \\ C_1 \frac{dv_{01}(t)}{dt} &= \frac{-v_{01}(t)}{R_1} - i_{01}(t) \\ L_2' \frac{di_{L2}(t)}{dt} &= (v_{in}(t) - v_{02}(t)) + \frac{M}{L_1} v_{in}(t) \\ C_2 \frac{dv_{02}(t)}{dt} &= i_{L2}(t) - \frac{v_{02}(t)}{R_2} - i_{02}(t) \end{aligned} \tag{2.63}$$

leading to state-space equation of the d_2T_s interval:

$$\frac{d\mathbf{x}(t)}{dt} = \mathbf{A}_1\mathbf{x}(t) + \mathbf{B}_1\mathbf{u}(t) \quad , \quad \mathbf{y}(t) = \mathbf{C}_1\mathbf{x}(t) + \mathbf{D}_1\mathbf{u}(t)$$

$$\mathbf{A}_1 = \begin{bmatrix} 0 & 0 & 0 & \frac{-M}{L_2L_1'} \\ 0 & \frac{-1}{C_1R_1} & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{L_2'} \\ 0 & 0 & \frac{1}{C_2} & \frac{-1}{C_2R_2} \end{bmatrix} \quad \mathbf{B}_1 = \begin{bmatrix} \frac{1}{L_1'}(1+\frac{M}{L_2}) & 0 & 0 \\ 0 & \frac{-1}{C_1} & 0 \\ \frac{1}{L_2'}(1+\frac{M}{L_1}) & 0 & 0 \\ 0 & 0 & \frac{-1}{C_2} \end{bmatrix} \quad \mathbf{C}_1 = \begin{bmatrix} 0\ 1\ 0\ 0 \\ 0\ 0\ 0\ 1 \end{bmatrix} \quad \mathbf{D}_1 = \begin{bmatrix} 0\ 0\ 0 \\ 0\ 0\ 0 \end{bmatrix}$$

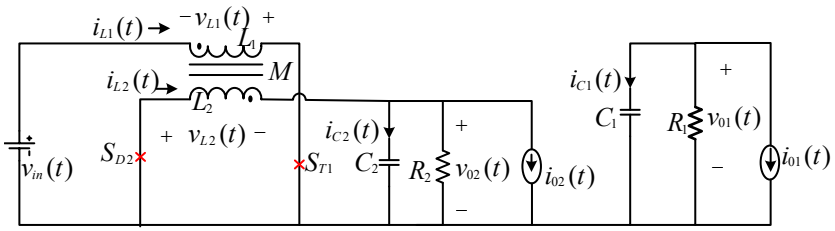


Figure 2.17: Mode II circuit configuration of CI-SIDO boost and buck converter

Mode II: $(d_1 - d_2)T_s$ **interval**

The equivalent circuit for this interval is shown in Figure 2.17. Applying KVL and KCL in the equivalent circuit of $(d_1 - d_2)T_s$ interval gives:

$$\begin{aligned} L_1' \tfrac{di_{L1}(t)}{dt} &= v_{in}(t) + \tfrac{M}{L_2}(-v_{02}(t)) \\ i_{c1}(t) = C_1 \tfrac{dv_{01}(t)}{dt} &= -v_{01}(t)/R_1 - i_{01}(t) \\ L_2' \tfrac{di_{L2}(t)}{dt} &= -v_{02}(t) + \tfrac{M}{L_1} v_{in}(t) \\ i_{c2}(t) = C_2 \tfrac{dv_{02}(t)}{dt} &= i_{L2}(t) - v_{02}(t)/R_2 - i_{02}(t) \end{aligned} \tag{2.64}$$

leading to state-space equation of the $(d_1 - d_2)T_s$ interval:

$$\frac{d\mathbf{x}(t)}{dt} = \mathbf{A}_2\mathbf{x}(t) + \mathbf{B}_2\mathbf{u}(t) \quad \mathbf{y}(t) = \mathbf{C}_2\mathbf{x}(t) + \mathbf{D}_2\mathbf{u}(t)$$

$$\mathbf{A}_2 = \begin{bmatrix} 0 & 0 & 0 & \frac{-M}{L_2 L_1'} \\ 0 & \frac{-1}{C_1 R_1} & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{L_2'} \\ 0 & 0 & \frac{1}{C_2} & \frac{-1}{C_2 R_2} \end{bmatrix} \quad \mathbf{B}_2 = \begin{bmatrix} \frac{1}{L_1'} & 0 & 0 \\ 0 & -\frac{1}{C_1} & 0 \\ \frac{M}{L_1 L_2'} & 0 & 0 \\ 0 & 0 & -\frac{1}{C_2} \end{bmatrix} \quad \mathbf{C}_2 = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \quad \mathbf{D}_2 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

Mode III: $(1 - d_1)T_s$ **interval**

The equivalent circuit for this interval is shown in Figure 2.18. Applying KVL and KCL in the equivalent circuit of $(1 - d_1)T_s$ interval gives:

$$\begin{aligned} L_1' \tfrac{di_{L1}(t)}{dt} &= v_{in}(t) - v_{01}(t) + \tfrac{M}{L_2}(-v_{02}(t)) \\ i_{c1}(t) = C_1 \tfrac{dv_{01}(t)}{dt} &= i_{L1}(t) - v_{01}(t)/R_1 - i_{01}(t) \\ L_2' \tfrac{di_{L2}(t)}{dt} &= -v_{02}(t) + \tfrac{M}{L_1}(v_{in}(t) - v_{01}(t)) \\ i_{c2}(t) = C_2 \tfrac{dv_{02}(t)}{dt} &= i_{L2}(t) - v_{02}(t)/R_2 - i_{02}(t) \end{aligned} \tag{2.65}$$

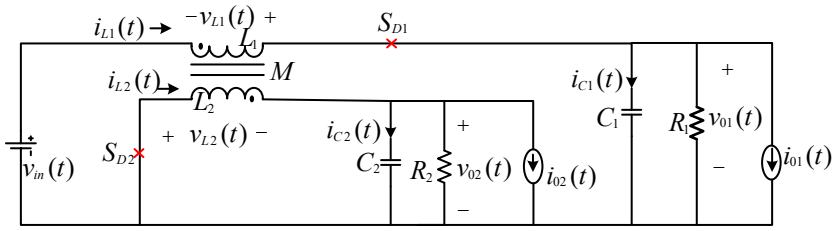


Figure 2.18: Mode III circuit configuration of CI-SIDO boost and buck converter

leading to state-space equation of the $(1-d_1)T_s$ interval:

$$\frac{d\mathbf{x}(t)}{dt} = \mathbf{A}_3\mathbf{x}(t) + \mathbf{B}_3\mathbf{u}(t) \quad \mathbf{y}(t) = \mathbf{C}_3\mathbf{x}(t) + \mathbf{D}_3\mathbf{u}(t)$$

$$\mathbf{A}_3 = \begin{bmatrix} 0 & \frac{-1}{L_1'} & 0 & \frac{-M}{L_2L_1'} \\ \frac{1}{C_1} & \frac{-1}{C_1R_1} & 0 & 0 \\ 0 & \frac{-M}{L_1L_2'} & 0 & \frac{-1}{L_2'} \\ 0 & 0 & \frac{1}{C_2} & \frac{-1}{C_2R_2} \end{bmatrix} \quad \mathbf{B}_3 = \begin{bmatrix} \frac{1}{L_1'} & 0 & 0 \\ 0 & \frac{-1}{C_1} & 0 \\ \frac{M}{L_1L_2'} & 0 & 0 \\ 0 & 0 & \frac{-1}{C_2} \end{bmatrix} \quad \mathbf{C}_3 = \mathbf{C}_1 \quad \mathbf{D}_3 = \mathbf{D}_1$$

2.5.3.2 Average State-space Equation

Now the averaged state-space equation is written as

$$\frac{d\mathbf{x}}{dt} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \quad \mathbf{y} = \mathbf{C}\mathbf{x} + \mathbf{D}\mathbf{u}$$

where, the average state-space matrices is calculated using (2.12) and are given by

$$\mathbf{A} = \begin{bmatrix} 0 & -\frac{(1-d_1)}{L_1'} & 0 & -\frac{M}{L_2L_1'} \\ \frac{1-d_1}{C_1} & -\frac{1}{C_1R_1} & 0 & 0 \\ 0 & -\frac{M(1-d_1)}{L_1L_2'} & 0 & -\frac{1}{L_2'} \\ 0 & 0 & \frac{1}{C_2} & -\frac{1}{C_2R_2} \end{bmatrix} \quad \mathbf{B} = \begin{bmatrix} \frac{1}{L_1'}(1+\frac{Md_2}{L_2}) & 0 & 0 \\ 0 & -\frac{1}{C_1} & 0 \\ \frac{1}{L_2'}(d_2+\frac{M}{L_1}) & 0 & 0 \\ 0 & 0 & -\frac{1}{C_2} \end{bmatrix}$$

$$\mathbf{C} = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \quad \mathbf{D} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

2.5.3.3 Small-signal Open-loop Transfer Functions of CI-SIDO Boost and Buck Converter

The open loop transfer functions of CI-SIDO boost and buck converter are derived as follows:

Small-signal transfer functions between the state variables and input variables:

The small-signal open-loop transfer functions between the state variables and input variables are derived using (2.20) and is written as

$$\hat{\mathbf{x}}(s) = (s\mathbf{I} - \mathbf{A}_{av})^{-1}\mathbf{B}_{av}\hat{\mathbf{u}}(s)$$

which is expressed as

$$\begin{bmatrix} \hat{i}_{L1}(s) \\ \hat{v}_{C1}(s) \\ \hat{i}_{L2}(s) \\ \hat{v}_{C2}(s) \end{bmatrix} = \begin{bmatrix} s & \frac{(1-D_1)}{L_1'} & 0 & \frac{M}{L_2L_1'} \\ \frac{-(1-D_1)}{C_1} & s+\frac{1}{C_1R_1} & 0 & 0 \\ 0 & \frac{M(1-D_1)}{L_1L_2'} & s & \frac{1}{L_2'} \\ 0 & 0 & \frac{-1}{C_2} & s+\frac{1}{C_2R_2} \end{bmatrix}^{-1} \begin{bmatrix} \frac{1}{L_1'}(1+\frac{MD_2}{L_2}) & 0 & 0 \\ 0 & -\frac{1}{C_1} & 0 \\ \frac{1}{L_2'}(D_2+\frac{M}{L_1}) & 0 & 0 \\ 0 & 0 & -\frac{1}{C_2} \end{bmatrix} \begin{bmatrix} \hat{v}_{in}(s) \\ \hat{i}_{01}(s) \\ \hat{i}_{02}(s) \end{bmatrix} \tag{2.66}$$

Input voltage to inductor currents transfer functions: By solving the first and third line of (2.66) and making the $\hat{i}_{01} = \hat{i}_{02} = 0$, we obtain the input voltage to inductor currents transfer functions as

$$\begin{aligned} G_{ig1} = \frac{\hat{i}_{L1}}{\hat{v}_{in}} &= \frac{1}{L_1'}\frac{(s+\frac{1}{R_1C_1})(s^2+\frac{s}{R_2C_2}+\frac{1}{L_2C_2}+\frac{MD_2}{L_2}(s^2+\frac{s}{R_2C_2}))}{Dn_{bobu}(s)} \\ G_{ig2} = \frac{\hat{i}_{L2}}{\hat{v}_{in}} &= \frac{1}{L_2'}\frac{(s+\frac{1}{R_2C_2})(D_2(s^2+\frac{s}{R_1C_1}+\frac{(1-D_1)^2}{L_1C_1})+\frac{M}{L_1}(s^2+\frac{s}{R_1C_1}))}{Dn_{bobu}(s)} \end{aligned} \tag{2.67}$$

where,

$$\begin{aligned} Dn_{bobu}(s) = s^4 + (\frac{1}{R_1C_1}+\frac{1}{R_2C_2})s^3 + (\frac{(1-D_1)^2}{L_1'C_1}+\frac{1}{L_2'C_2}+\frac{1}{R_1R_2C_1C_2})s^2 \\ + (\frac{(1-D_1)^2}{L_1'C_1R_2C_2}+\frac{1}{L_2'C_2R_1C_1})s + \frac{(1-D_1)^2}{L_1'L_2C_1C_2} \end{aligned}$$

Load currents to Inductor currents transfer functions: By solving the first and third line of (2.66) and making the $\hat{v}_{in} = 0$, we obtain the load currents to inductor currents transfer

functions and are given by

$$H_{ii11} = \frac{\hat{i}_{L1}}{\hat{i}_{01}} = \frac{1-D_1}{L_1'C_1}\frac{(s^2+\frac{s}{R_2C_2}+\frac{1}{L_2C_2})}{Dn_{bobu}(s)} \quad H_{ii22} = \frac{\hat{i}_{L2}}{\hat{i}_{02}} = \frac{1}{L_2'C_2}\frac{(s^2+\frac{s}{R_1C_1}+\frac{(1-D_1)^2}{L_1C_1})}{Dn_{bobu}(s)}$$
$$H_{ii12} = \frac{\hat{i}_{L1}}{\hat{i}_{02}} = \frac{M}{L_2L_1'C_2}\frac{s(s+\frac{1}{R_1C_1})}{Dn_{bobu}(s)} \quad H_{ii21} = \frac{\hat{i}_{L2}}{\hat{i}_{01}} = \frac{M(1-D_1)}{L_1L_2'C_1}\frac{s(s+\frac{1}{R_2C_2})}{Dn_{bobu}(s)} \tag{2.68}$$

Small-signal transfer functions between the state variable and duty cycles:

The small-signal open-loop transfer functions between the state variable and duty cycles are derived using (2.21). In CI-SIDO boost and buck converter, $\mathbf{A}_1 = \mathbf{A}_2$, $\mathbf{B}_2 = \mathbf{B}_3$, (2.21) becomes

$$\hat{\mathbf{x}}(s) = (s\mathbf{I} - \mathbf{A}_{av})^{-1}\{[(\mathbf{B}_1 - \mathbf{B}_2)\mathbf{U}]\hat{d}_2(s) + [(\mathbf{A}_2 - \mathbf{A}_3)\mathbf{X}]\hat{d}_1(s)\}$$

and is expressed as

$$\begin{bmatrix}\hat{i}_{L1}(s)\\ \hat{v}_{01}(s)\\ \hat{i}_{L2}(s)\\ \hat{v}_{02}(s)\end{bmatrix} = \begin{bmatrix} s & \frac{(1-D_1)}{L_1'} & 0 & \frac{M}{L_2L_1'}\\ \frac{-(1-D_1)}{C_1} & s+\frac{1}{C_1R_1} & 0 & 0\\ 0 & \frac{M(1-D_1)}{L_1L_2'} & s & \frac{1}{L_2'}\\ 0 & 0 & \frac{-1}{C_2} & s+\frac{1}{C_2R_2}\end{bmatrix}^{-1}\begin{bmatrix}\frac{MV_{in}}{L_2L_1'} & \frac{V_{in}}{L_1'(1-D_2)}\\ 0 & \frac{-V_{in}}{R_1C_1(1-D_1)^2}\\ \frac{V_{in}}{L_2'} & \frac{MV_{in}}{L_1L_2'(1-D_1)}\\ 0 & 0\end{bmatrix}\begin{bmatrix}\hat{d}_2(s)\\ \hat{d}_1(s)\end{bmatrix} \tag{2.69}$$

Inductor current to duty cycle transfer functions: Solving first and third line of (2.69), we obtain the duty cycles to inductor currents transfer functions as

$$G_{id11} = \frac{\hat{i}_{L1}}{\hat{d}_1} = \frac{V_{in}}{L_1'(1-D_1)}\frac{(s+\frac{2}{R_1C_1})(s^2+\frac{s}{R_2C_2}+\frac{1}{L_2C_2})}{Dn_{bobu}(s)}$$
$$G_{id22} = \frac{\hat{i}_{L2}}{\hat{d}_2} = \frac{V_{in}}{L_2'}\frac{(s+\frac{1}{R_2C_2})(s^2+\frac{s}{R_1C_1}+\frac{(1-D_1)^2}{L_1C_1})}{Dn_{bobu}(s)} \tag{2.70}$$

$$G_{id12} = \frac{\hat{i}_{L1}}{\hat{d}_2} = \frac{MV_{in}}{L_2L_1'}\frac{s(s+\frac{1}{R_1C_1})(s+\frac{1}{R_2C_2})}{Dn_{bobu}(s)} \quad G_{id21} = \frac{\hat{i}_{L2}}{\hat{d}_1} = \frac{MV_{in}}{L_1L_2'(1-D_1)}\frac{s(s+\frac{1}{R_2C_2})(s+\frac{2}{R_1C_1})}{Dn_{bobu}(s)} \tag{2.71}$$

Small-signal transfer functions between the output variables and input variables:

The small-signal open-loop transfer functions between the output variables and input variables are derived using (2.22) and is written as

$$\hat{\mathbf{y}}(s) = \left(\mathbf{C}_{av}(s\mathbf{I} - \mathbf{A}_{av})^{-1}\mathbf{B}_{av} + \mathbf{D}_{av}\right)\hat{\mathbf{u}}(s)$$

which is expressed as

$$\begin{bmatrix}\hat{v}_{01}(s)\\ \hat{v}_{02}(s)\end{bmatrix}=\begin{bmatrix}0&1&0&0\\0&0&0&1\end{bmatrix}\begin{bmatrix}s&\frac{(1-D_1)}{L_1'}&0&\frac{M}{L_2L_1'}\\ \frac{-(1-D_1)}{C_1}&s+\frac{1}{C_1R_1}&0&0\\0&\frac{M(1-D_1)}{L_1L_2'}&s&\frac{1}{L_2'}\\0&0&\frac{-1}{C_2}&s+\frac{1}{C_2R_2}\end{bmatrix}^{-1}\begin{bmatrix}\frac{1}{L_1'}(1+\frac{MD_2}{L_2})&0&0\\0&-\frac{1}{C_1}&0\\ \frac{1}{L_2'}(D_2+\frac{M}{L_1})&0&0\\0&0&-\frac{1}{C_2}\end{bmatrix}\begin{bmatrix}\hat{v}_{in}(s)\\ \hat{i}_{01}(s)\\ \hat{i}_{02}(s)\end{bmatrix} \tag{2.72}$$

Input voltage to output voltage (Audio-susceptibility) transfer functions: The input voltage to output transfer functions are found by solving (2.72), making the $\hat{i}_{01}=\hat{i}_{02}=0$ and is given by:

$$\begin{aligned}G_{vg1}&=\frac{\hat{v}_{01}}{\hat{v}_{in}}=\frac{1-D_1}{L_1'C_1}\frac{(s^2+\frac{s}{R_2C_2}+\frac{1}{L_2C_2}+\frac{MD_2}{L_2}(s^2+\frac{s}{R_2C_2}))}{Dn_{bobu}(s)}\\ G_{vg2}&=\frac{\hat{v}_{02}}{\hat{v}_{in}}=\frac{1}{L_2'C_2}\frac{(D_2(s^2+\frac{s}{R_1C_1}+\frac{(1-D_1)^2}{L_1C_1})+\frac{M}{L_1}(s^2+\frac{s}{R_1C_1}))}{Dn_{bobu}(s)}\end{aligned} \tag{2.73}$$

Load current to output voltage (Load Regulation) transfer functions: The load currents to output transfer functions are found by solving (2.72), making the $\hat{v}_{in}=0$ and is given by:

Self-regulation transfer functions:

$$Z_{vi11}=\frac{\hat{v}_{01}}{\hat{i}_{01}}=\frac{-s}{C_1}\frac{(s^2+\frac{s}{R_2C_2}+\frac{1}{L_2'C_2})}{Dn_{bobu}(s)}\quad Z_{vi22}=\frac{\hat{v}_{02}}{\hat{i}_{02}}=\frac{-s}{C_2}\frac{(s^2+\frac{s}{R_1C_1}+\frac{(1-D_1)^2}{L_1C_1})}{Dn_{bobu}(s)} \tag{2.74}$$

cross-regulation transfer functions:

$$Z_{vi12}=\frac{\hat{v}_{01}}{\hat{i}_{02}}=\frac{M(1-D_1)}{L_2L_1'C_1C_2}\frac{s}{Dn_{bobu}(s)}\quad Z_{vi21}=\frac{\hat{v}_{02}}{\hat{i}_{01}}=\frac{M(1-D_1)}{L_1L_2'C_1C_2}\frac{s}{Dn_{bobu}(s)} \tag{2.75}$$

Small-signal transfer functions between the output variable and duty cycles:

The small-signal open-loop transfer functions between the output variables and duty cycles can be obtained from (2.23). In CI-SIDO boost and buck converter $\mathbf{A}_1=\mathbf{A}_2$, $\mathbf{B}_2=\mathbf{B}_3$ $\mathbf{C}_1=\mathbf{C}_2=\mathbf{C}_3$, $\mathbf{D}_1=\mathbf{D}_2=\mathbf{D}_3$, (2.23) becomes as

$$\hat{\mathbf{y}}(s)=\{(\mathbf{C}_{av}(s\mathbf{I}-\mathbf{A}_{av})^{-1}[(\mathbf{B}_1-\mathbf{B}_2)\mathbf{U}])\}\hat{d}_2(s)+\{(\mathbf{C}_{av}(s\mathbf{I}-\mathbf{A}_{av})^{-1}[(\mathbf{A}_2-\mathbf{A}_3)\mathbf{X}])\}\hat{d}_1(s)$$

$$\implies \hat{\mathbf{y}}(s)=\mathbf{C}_{av}(s\mathbf{I}-\mathbf{A}_{av})^{-1}\begin{bmatrix}(\mathbf{B}_1-\mathbf{B}_2)\mathbf{U} & (\mathbf{A}_2-\mathbf{A}_3)\mathbf{X}\end{bmatrix}\begin{bmatrix}\hat{d}_2(s)\\ \hat{d}_1(s)\end{bmatrix}$$

and is expressed as

$$\begin{bmatrix}\hat{v}_{01}(s)\\ \hat{v}_{02}(s)\end{bmatrix} = \begin{bmatrix}0 & 1 & 0 & 0\\ 0 & 0 & 0 & 1\end{bmatrix} \begin{bmatrix} s & \frac{(1-D_1)}{L_1'} & 0 & \frac{M}{L_2L_1'}\\ \frac{-(1-D_1)}{C_1} & s+\frac{1}{C_1R_1} & 0 & 0\\ 0 & \frac{M(1-D_1)}{L_1L_2'} & s & \frac{1}{L_2'}\\ 0 & 0 & \frac{-1}{C_2} & s+\frac{1}{C_2R_2}\end{bmatrix}^{-1} \begin{bmatrix}\frac{MV_{in}}{L_2L_1'} & \frac{V_{in}}{L_1'(1-D_2)}\\ 0 & \frac{-V_{in}}{R_1C_1(1-D_1)^2}\\ \frac{V_{in}}{L_2'} & \frac{MV_{in}}{L_1L_2'(1-D_1)}\\ 0 & 0\end{bmatrix} \begin{bmatrix}\hat{d}_2(s)\\ \hat{d}_1(s)\end{bmatrix} \tag{2.76}$$

Duty cycle to output voltage transfer functions: Solving (2.76), we obtain the duty cycles to output voltages transfer functions as

$$\begin{aligned} G_{vd11} = \frac{\hat{v}_{01}}{\hat{d}_1} &= \frac{V_{in}}{L_1'C_1}\frac{(s^2+\frac{s}{R_2C_2}+\frac{1}{L_2'C_2})(\frac{-L_1's}{R_1(1-D_1)^2}+1)-\frac{M^2}{L_1L_2L_2'C_2}}{Dn_{bobu}(s)}\\ G_{vd22} = \frac{\hat{v}_{02}}{\hat{d}_2} &= \frac{V_{in}}{L_2'C_2}\frac{(s^2+\frac{s}{R_1C_1}+\frac{(1-D_1)^2}{L_1C_1})}{Dn_{bobu}(s)} \end{aligned} \tag{2.77}$$

Cross-coupling transfer functions:

$$\begin{aligned} G_{vd12} = \frac{\hat{v}_{01}}{\hat{d}_2} &= \frac{MV_{in}(1-D_1)}{L_2L_1'C_1}\frac{s(s+\frac{1}{R_2C_2})}{Dn_{bobu}(s)}\\ G_{vd21} = \frac{\hat{v}_{02}}{\hat{d}_1} &= \frac{MV_{in}}{L_1L_2'C_2(1-D_1)}\frac{s(s+\frac{2}{R_1C_1})}{Dn_{bobu}(s)} \end{aligned} \tag{2.78}$$

2.6 Small-signal Model of CI-SIDO Converter

Using all the transfer functions, the small-signal model of CI-SIDO converters can be represented in matrix form as

$$\begin{bmatrix}\hat{i}_{L1}\\ \hat{i}_{L2}\end{bmatrix} = \begin{bmatrix}G_{id11} & G_{id12}\\ G_{id21} & G_{id22}\end{bmatrix}\begin{bmatrix}\hat{d}_1\\ \hat{d}_2\end{bmatrix} + \begin{bmatrix}G_{ig1}\\ G_{ig2}\end{bmatrix}\begin{bmatrix}\hat{v}_{in}\end{bmatrix} + \begin{bmatrix}H_{ii11} & H_{ii12}\\ H_{ii21} & H_{ii22}\end{bmatrix}\begin{bmatrix}\hat{i}_{01}\\ \hat{i}_{02}\end{bmatrix} \tag{2.79}$$

$$\begin{bmatrix}\hat{v}_{01}\\ \hat{v}_{02}\end{bmatrix} = \begin{bmatrix}G_{vd11} & G_{vd12}\\ G_{vd21} & G_{vd22}\end{bmatrix}\begin{bmatrix}\hat{d}_1\\ \hat{d}_2\end{bmatrix} + \begin{bmatrix}G_{vg1}\\ G_{vg2}\end{bmatrix}\begin{bmatrix}\hat{v}_{in}\end{bmatrix} + \begin{bmatrix}Z_{vi11} & Z_{vi12}\\ Z_{vi21} & Z_{vi22}\end{bmatrix}\begin{bmatrix}\hat{i}_{01}\\ \hat{i}_{02}\end{bmatrix} \tag{2.80}$$

Equation (2.79) represent how the variation in input voltage, load currents affect the inductor currents. Equation (2.80) show how the variation in input voltage, load currents affect the output voltages.

2.7 Conclusion

This chapter presents the steady-state analysis and small-signal modelling of three topologies of CI-SIDO converter, i.e., CI-SIDO buck, CI-SIDO boost, CI-SIDO boost and buck converter. From the steady-state analysis it is observed that mutual coupling does not affect the steady-state behaviour, i.e., steady-state of CI-SIDO converter behave the same as SISO converter. However, the dynamic behaviour of CI-SIDO converter is different from SISO converter as the order of CI-SIDO converter has increase to fourth order. Due to the coupling, there are additional cross-regulation and cross-coupling transfer functions. These are absent in SISO buck converter and SISO boost converter.

Note: Major part of this chapter is reproduced from my publications:

1. G. Nayak and S. Nath, "Small Signal Model for Current Mode Control of Coupled Inductor SIDO Buck Converter," 2019 IEEE Transportation Electrification Conference (ITEC-India), Bengaluru, India, 2019, pp. 1-6.
doi: 10.1109/ITEC-India48457.2019.ITECINDIA2019-252.

2. G. Nayak and S. Nath, "Unaffected Dynamic Performance of Coupled SIDO Converters Due to Phase Shift," 2019 National Power Electronics Conference (NPEC), Tiruchirappalli, India, 2019, pp. 1-6.
doi: 10.1109/NPEC47332.2019.9034867.

3

Choosing Coefficient of Coupling for Coupled SIDO Converters

Contents

3.1 Introduction

The coefficient of coupling k between the two magnetically coupled inductors play an important role in the dynamic behaviour of CI-SIDO converters. The transfer function derived in Chapter 2 shows that complex poles and zeros of the converter, cross-coupling and cross-regulation are affected by the choice of k. Hence, this chapter investigates the effect of coefficient of coupling k on characteristics of CI-SIDO buck converter and CI-SIDO boost converter and finds the suitable choices for k.

3.2 Effect of Coefficient of Coupling on Boundary Value of Inductance

To ensure continuous conduction mode (CCM) of operation, the inductance L_1, L_2 of coupled inductor should be chosen larger than the boundary value. The boundary inductance value of two type of CI-SIDO converter topologies, i.e., CI-SIDO buck converter and CI-SIDO boost converter are calculated and effect of k on the boundary value of inductance are analysed in the following subsections.

3.2.1 CI-SIDO Buck Converter

The inductance at the boundary of CCM and DCM for CI-SIDO buck converter is calculated and are given by

$$L_1 = \frac{R_1(D_1D_1' + \frac{M}{L_2}D_2D_2')}{2D_1f_s(1-k^2)} \; ; \; L_2 = \frac{R_2(D_2D_2' + \frac{M}{L_1}D_1D_1')}{2D_2f_s(1-k^2)} \tag{3.1}$$

It is noted that with increase in k, the boundary inductance value increases. Figure 3.1 shows the plot of inductor values with increase in k for CI-SIDO buck converter. From the figure it is observed that the boundary inductance value is high with tight coupling, i.e., $k > 0.8$.

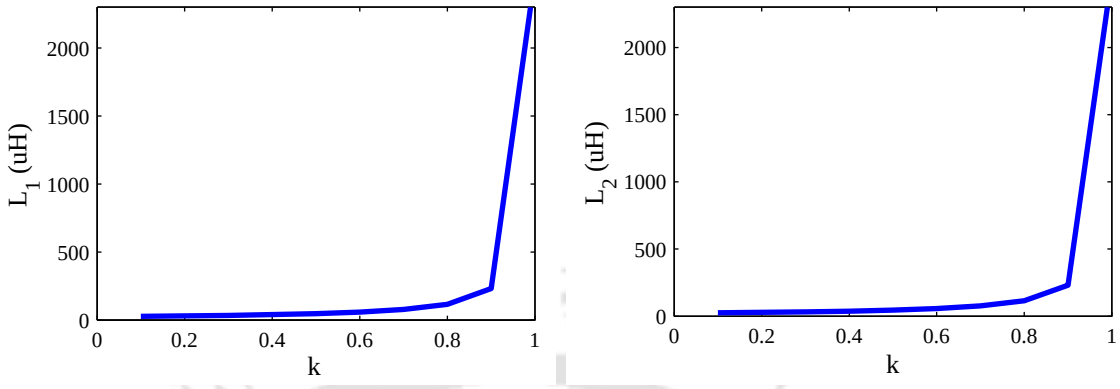


Figure 3.1: Boundary inductance value of CI-SIDO buck converter with variation in k considering $V_{in} = 10$, $d_1 = 0.6$, $d_2 = 0.33$, $R_1 = 12\Omega$, $R_2 = 6.6\Omega$ (a) L_1 (b) L_2

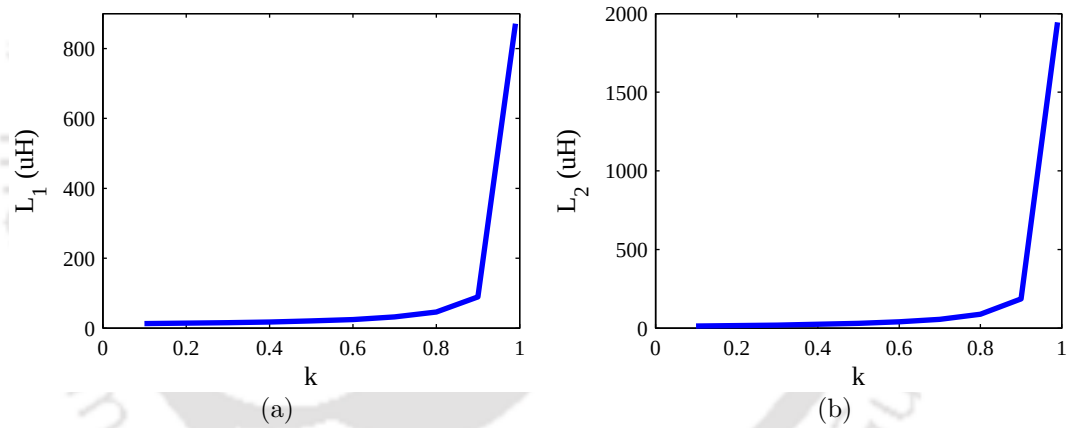


Figure 3.2: Boundary inductance value of CI-SIDO boost converter with variation in k considering $V_{in} = 5$, $d_1 = 0.583$, $d_2 = 0.375$, $R_1 = 24\Omega$, $R_2 = 16\Omega$ (a) L_1 (b) L_2

3.2.2 CI-SIDO Boost Converter

The inductance at the boundary of CCM and DCM for CI-SIDO boost converter is calculated and are given by

$$L_1 = \frac{R_1 D_1^{'2}(D_1 + \frac{M}{L_2}D_2)}{2f_s(1-k^2)} \;;\; L_2 = \frac{R_2 D_2^{'2}(D_2 + \frac{M}{L_1}D_1)}{2f_s(1-k^2)} \tag{3.2}$$

Figure 3.2 shows the plot of inductor values with increase in k for CI-SIDO boost converter. From the figure it is observed that with tight coupling, i.e., $k > 0.8$, the boundary inductance value is very large.

3.3 Effect of Coefficient of Coupling on Duty Cycle to Output Voltage Transfer Functions

Duty cycle to output voltage transfer functions are used to design controller and analyse the stability of the converter. Thus, following subsection analyses the effect of k on the duty cycle to output voltage transfer functions of two topologies of CI-SIDO converter, i.e., CI-SIDO buck converter and CI-SIDO boost converter using root locus plot, bode plot and step response plot. The parameter used in the analysis are shown in Table 3.1.

3.3.1 CI-SIDO Buck Converter

The duty cycle to output voltage transfer functions G_{vd11}, G_{vd22} for CI-SIDO buck converter are derived in Chapter 2 and considering ideal condition the transfer functions are given by

$$\begin{aligned} G_{vd11} &= \frac{V_{in}}{L_1' C_1} \frac{(s^2 + \frac{s}{R_2 C_2} + \frac{1}{L_2 C_2})}{(s^2 + \frac{s}{R_2 C_2} + \frac{1}{L_2' C_2})(s^2 + \frac{s}{R_1 C_1} + \frac{1}{L_1' C_1}) - \frac{k^2}{L_1' L_2' C_1 C_2}} \\ G_{vd22} &= \frac{V_{in}}{L_2' C_2} \frac{(s^2 + \frac{s}{R_1 C_1} + \frac{1}{L_1 C_1})}{(s^2 + \frac{s}{R_2 C_2} + \frac{1}{L_2' C_2})(s^2 + \frac{s}{R_1 C_1} + \frac{1}{L_1' C_1}) - \frac{k^2}{L_1' L_2' C_1 C_2}} \end{aligned} \tag{3.3}$$

The duty cycle to output voltage transfer functions as given in (3.3) can be written in pole-zero form as

$$\begin{aligned} G_{vd11} &= \frac{G_{01}(s^2 + \frac{w_{z1}}{Q_{z1}} s + w_{z1}^2)}{(s^2 + \frac{w_{p1}}{Q_{p1}} s + w_{p1}^2)(s^2 + \frac{w_{p2}}{Q_{p2}} s + w_{p2}^2)} \\ G_{vd22} &= \frac{G_{02}(s^2 + \frac{w_{z2}}{Q_{z2}} s + w_{z2}^2)}{(s^2 + \frac{w_{p1}}{Q_{p1}} s + w_{p1}^2)(s^2 + \frac{w_{p2}}{Q_{p2}} s + w_{p2}^2)} \end{aligned} \tag{3.4}$$

where, $G_{01} = \frac{V_{in}}{L_1' C_1}$, $G_{02} = \frac{V_{in}}{L_2' C_2}$

$$\begin{aligned} w_{p1} &\approx \frac{w_{p1-BC}}{\sqrt{1+k}},\ w_{p2} \approx \frac{w_{p2-BC}}{\sqrt{1-k}},\ w_{z1} = w_{p2-BC},\ w_{z2} = w_{p1-BC} \\ Q_{p1} &\approx \frac{Q_{p1-BC}}{\sqrt{1+k}},\ Q_{p2} \approx \frac{Q_{p2-BC}}{\sqrt{1-k}},\ Q_{z1} = Q_{p2-BC},\ Q_{z2} = Q_{p1-BC} \end{aligned} \tag{3.5}$$

where, w_{p1-BC}, w_{p2-BC}, Q_{p1-BC}, Q_{p2-BC} are the resonant frequency of complex poles, its quality factors of SISO buck converters and are given as $w_{p1-BC} = \sqrt{\frac{1}{L_1 C_1}}$, $Q_{p1-BC} = R_1 \sqrt{\frac{C_1}{L_1}}$, $w_{p2-BC} = \sqrt{\frac{1}{L_2 C_2}}$, $Q_{p2-BC} = R_2 \sqrt{\frac{C_2}{L_2}}$.

Table 3.1: Parameters of CI-SIDO converter

CI-SIDO Buck converter							
Parameter	V_{in}	V_{01}	V_{02}	R_1, R_2	$L_1 = L_2$	$C_1 = C_2$	f_s
values	10 V	6 V	3.3 V	12 Ω, 6.6 Ω	115 μH	320 μF	100 kHz
CI-SIDO Boost converter							
values	5 V	10 V	7 V	24 Ω, 14 Ω	115 μH	220 μF	100 kHz

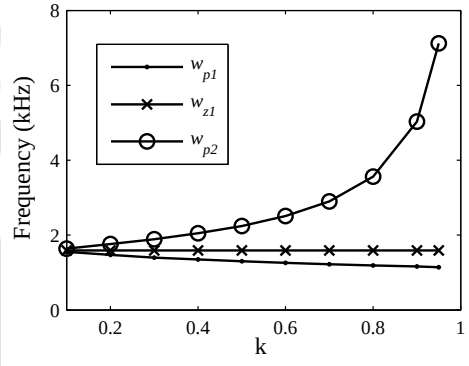


Figure 3.3: Variation of resonant frequencies w_{p1}, w_{p2}, w_{z1} with k

According to (3.4), the transfer function G_{vd11} has two complex poles and one complex zero. From (3.5), resonant frequency of complex poles w_{p1}, w_{p2} depends on k and resonant frequency of complex zeros w_{z1} doesn't depend on k. Thus, with variation in k, w_{z1} is fixed while w_{p1}, w_{p2} varies. Figure 3.3 shows the plot of w_{p1}, w_{p2}, w_{z1} with k variation. From (3.5) and Figure 3.3, it can be observed, the G_{vd11} has interlaced pole-zero distribution as

$$w_{p1} << w_{z1} << w_{p2} \tag{3.6}$$

Same is true for G_{vd22} as well. The interlaced pole and zero distribution makes the CI-SIDO buck converter to behave as 2^{nd} order (buck converter) both in low and high frequency region. However, in mid-frequency region, frequency response exhibits multiple resonant peaks as shown in Figure 3.4. The resonant peak is due to the quality factor of poles and zero. From (3.5), quality factor of complex poles depend on k and quality factor of complex zero doesn't depend on k. Figure 3.5 shows the variation of Q_{p1}, Q_{p2} with k. From (3.5) and Figure 3.5, it is seen that with increase in k, Q_{p2} increases and Q_{p1} decreases. Increase in quality factor result in more oscillation in transient response which eventually increases the settling time.

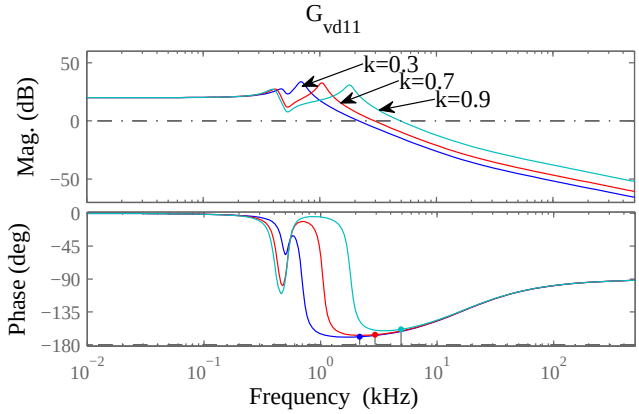


Figure 3.4: Bode plot for G_{vd11} of CI-SIDO buck with different k

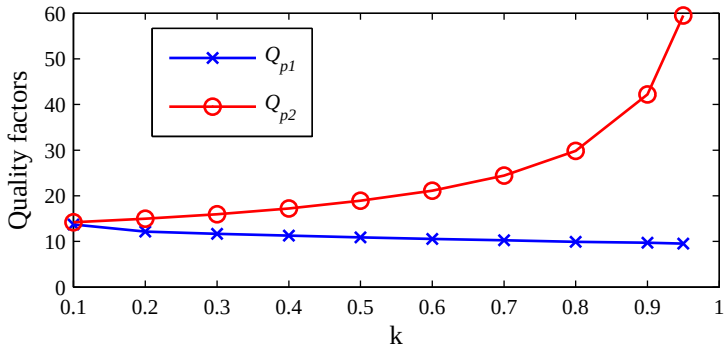
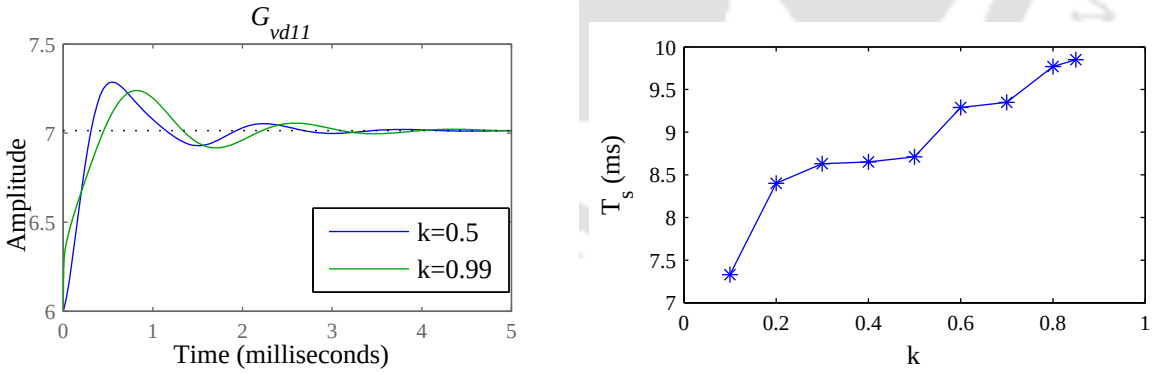


Figure 3.5: Variation of quality factors Q_{p1}, Q_{p2} with k



(a) (b)

Figure 3.6: (a) Step response of G_{vd11} of CI-SIDO buck considering circuit parasitics with medium and tight coupling (b) Settling time of G_{vd11} for CI-SIDO buck as function of k

Figure 3.6(a) shows the step response of G_{vd11} with medium and tight coupling and Figure 3.6(b) shows the change in settling time T_s with k. It is observed that with increase in k, settling time increases.

3.3.2 CI-SIDO Boost Converter

The duty cycle to output voltage transfer functions $G_{vd11} = \frac{\hat{v}_{01}}{\hat{d}_1}$, $G_{vd22} = \frac{\hat{v}_{02}}{\hat{d}_2}$ of CI-SIDO boost converter are given by

$$\begin{aligned} G_{vd11} &= \frac{\frac{V_{in}}{L_1'C_1}(s^2 + \frac{s}{R_2C_2} + \frac{(1-D_2)^2}{L_2'C_2})(\frac{-L_1's}{R_1(1-D_1)^2} + 1) - \frac{k^2(1-D_2)^2}{L_2'C_2}}{(s^2 + \frac{s}{R_2C_2} + \frac{(1-D_2)^2}{L_2'C_2})(s^2 + \frac{s}{R_1C_1} + \frac{(1-D_1)^2}{L_1'C_1}) - \frac{k^2(1-D_1)^2(1-D_2)^2}{L_1'L_2'C_1C_2}} \\ G_{vd22} &= \frac{\frac{V_{in}}{L_2'C_2}(s^2 + \frac{s}{R_1C_1} + \frac{(1-D_1)^2}{L_1'C_1})(\frac{-L_2's}{R_2(1-D_2)^2} + 1) - \frac{k^2(1-D_1)^2}{L_1'C_1}}{(s^2 + \frac{s}{R_2C_2} + \frac{(1-D_2)^2}{L_2'C_2})(s^2 + \frac{s}{R_1C_1} + \frac{(1-D_1)^2}{L_1'C_1}) - \frac{k^2(1-D_1)^2(1-D_2)^2}{L_1'L_2'C_1C_2}} \end{aligned} \tag{3.7}$$

and can be written in pole-zero form as

$$\begin{aligned} G_{vd11} &= \frac{G_{01}(1 - \frac{s}{w_{rhz1}})(s^2 + \frac{w_{z1}}{Q_{z1}}s + w_{z1}^2)}{(s^2 + \frac{w_{p1}}{Q_{p1}}s + w_{p1}^2)(s^2 + \frac{w_{p2}}{Q_{p2}}s + w_{p2}^2)} \\ G_{vd22} &= \frac{G_{02}(1 - \frac{s}{w_{rhz2}})(s^2 + \frac{w_{z2}}{Q_{z2}}s + w_{z2}^2)}{(s^2 + \frac{w_{p1}}{Q_{p1}}s + w_{p1}^2)(s^2 + \frac{w_{p2}}{Q_{p2}}s + w_{p2}^2)} \end{aligned} \tag{3.8}$$

where, $G_{01} = \frac{V_{in}}{L_1'C_1}$, $G_{02} = \frac{V_{in}}{L_2'C_2}$

$$\begin{gathered} w_{p1} \approx \frac{w_{p1-BO}}{\sqrt{1+k}},\ w_{p2} \approx \frac{w_{p2-BO}}{\sqrt{1-k}},\ w_{z1} \approx w_{p2-BC},\ w_{z2} \approx w_{p1-BO} \\ Q_{p1} \approx \frac{Q_{p1-BO}}{\sqrt{1+k}},\ Q_{p2} \approx \frac{Q_{p2-BO}}{\sqrt{1-k}},\ Q_{z1} \approx \frac{Q_{p2-BO}}{1-k^2},\ Q_{z2} \approx \frac{Q_{p1-BO}}{1-k^2} \\ w_{rhz1} \approx \frac{w_{rhz1-BO}}{1-k^2},\ w_{rhz2} \approx \frac{w_{rhz2-BO}}{1-k^2} \end{gathered} \tag{3.9}$$

where, w_{p1-BO}, w_{p2-BO}, Q_{p1-BO}, Q_{p2-BO} are the resonant frequencies of complex poles, its quality factors of SISO boost converters, respectively and are given by $w_{p1-BO} = \frac{(1-D_1)}{\sqrt{L_1C_1}}$, $Q_{p1-BO} = (1-D_1)R_1\sqrt{\frac{C_1}{L_1}}$, $w_{p2-BO} = \frac{(1-D_2)}{\sqrt{L_2C_2}}$, $Q_{p2-BO} = (1-D_2)R_2\sqrt{\frac{C_2}{L_2}}$, $w_{rhz1-BO} = \frac{R_1(1-D_1)^2}{L_1}$, $w_{rhz2} = \frac{R_2(1-D_2)^2}{L_2}$.

According to (3.8), the transfer function G_{vd11} has two complex poles, one complex zero and one right half plane (RHP) zero. From (3.9), w_{p1}, w_{p2} depend on k and w_{z1}, w_{z2} does not depend on k. Thus, with variation in k, w_{z1}, w_{z2}, are fixed while w_{p1}, w_{p2} varies. From (3.9), it is observed that, the G_{vd11} of CI-SIDO boost has interlaced pole-zero distribution as given in (3.6). The interlaced pole and zero distribution exhibit multiple resonant peaks around mid-frequency range. The resonant peak is due to the quality factor of poles and zero. From (3.9),

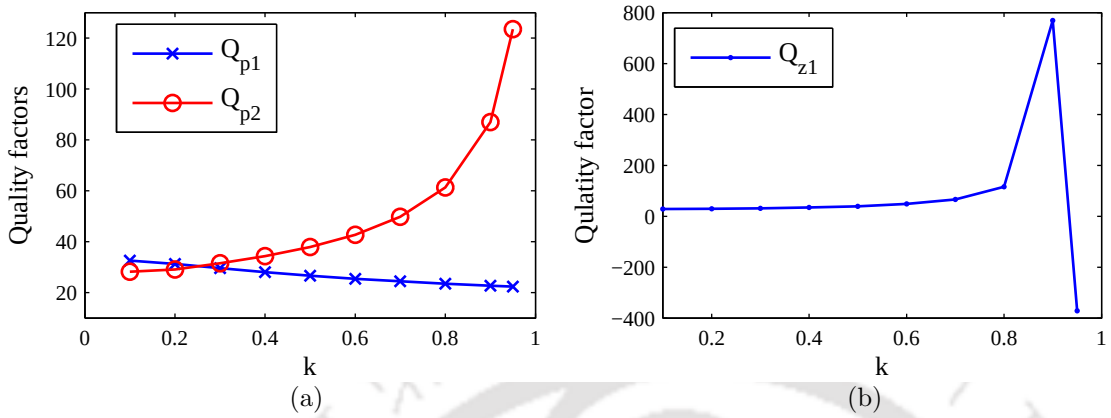


Figure 3.7: Effect of k on quality factors of G_{vd11} of CI-SIDO boost (a) Q_{p1}, Q_{p2} (b) Q_{z1}

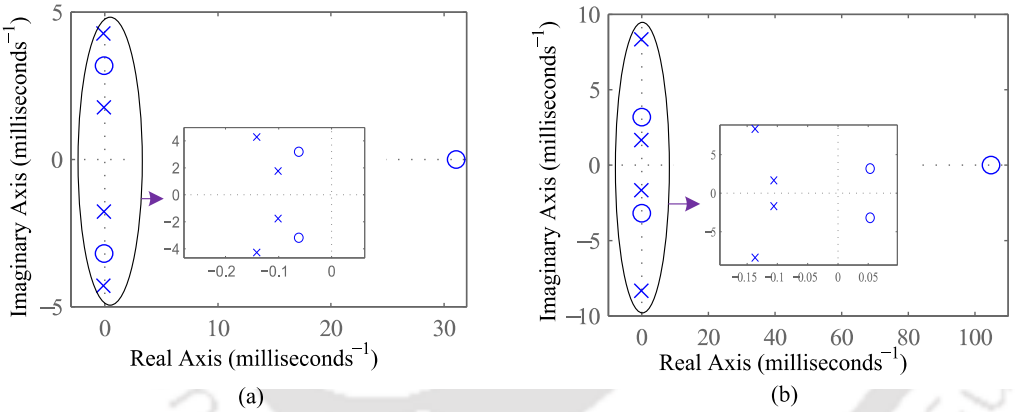


Figure 3.8: Pole zero map for G_{vd11} of CI-SIDO boost converter (a) medium coupling (k=0.5) (b) tight coupling (k=0.9)

it is found that quality factor of complex poles and zero depend on k. Figure 3.7 shows the plot of quality factors as a function of k and is observed that with increase in k, Q_{p1} decrease, Q_{z1}, Q_{p2} increases. Moreover, it is observed, with tight coupling the Q_{z1} becomes negative that means the complex zero moves to right half plane (RHP). Figure 3.8 shows the pole-zero map for G_{vd11} with medium and tight coupling and is observed that with tight coupling the complex zero moves to right half plane. The RHP complex zero with high quality factor, changes the phase abruptly and lead to instability as shown in Figure 3.10.

Figure 3.9 shows the asymptotic magnitude plots of G_{vd11} with variation in Q factors and is

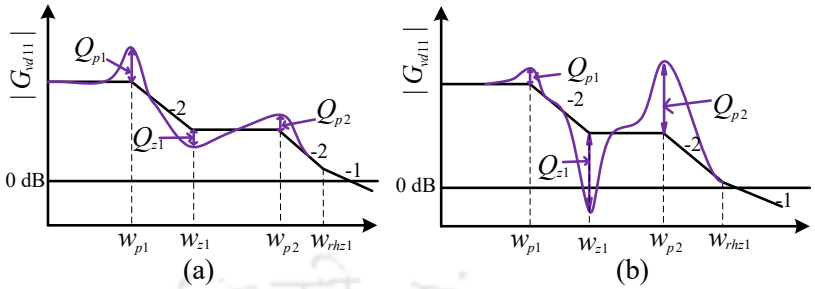


Figure 3.9: Asymptotic bode of G_{vd11} of CI-SIDO boost (a) Low Q-factor (k=0.4) (b) High Q-factor (k=0.9)

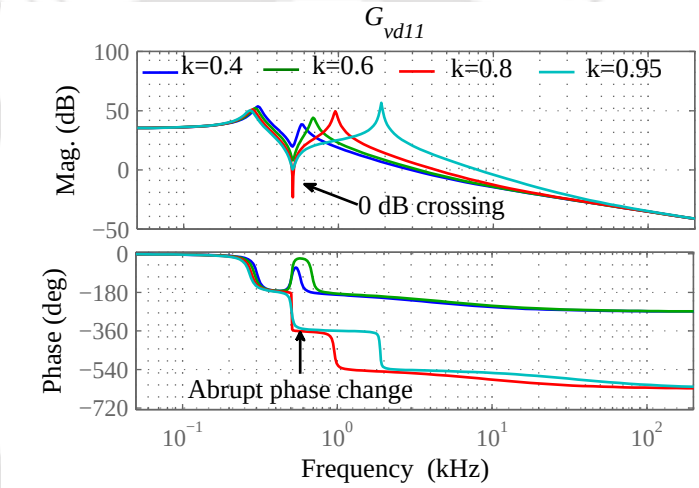


Figure 3.10: Frequency response plot for G_{vd11} of CI-SIDO boost with k as running parameter

observed that with high Q_{z1} the system undergoes multiple 0 dB crossing, i.e., system lead to conditional stability. Figure 3.10 shows the bode plot of G_{vd11} with increase in k. From Figure 3.10 it is observed that with tight coupling, the magnitude plot of G_{vd11} shows multiple 0 dB crossing and phase plot of G_{vd11} shows abrupt phase change. This is due to right half complex zero and it makes difficult to design controller.

3.4 Effect of Coefficient of Coupling on Cross-coupling

Cross-coupling is defined as the effect on the output voltage of one sub-converter due to variation in duty cycle of other sub-converter. The cross-coupling in CI-SIDO converter occur due to coefficient of coupling k and affects the converter performance. Following subsection analyses the effect of k on the cross-coupling transfer function of CI-SIDO buck converter and

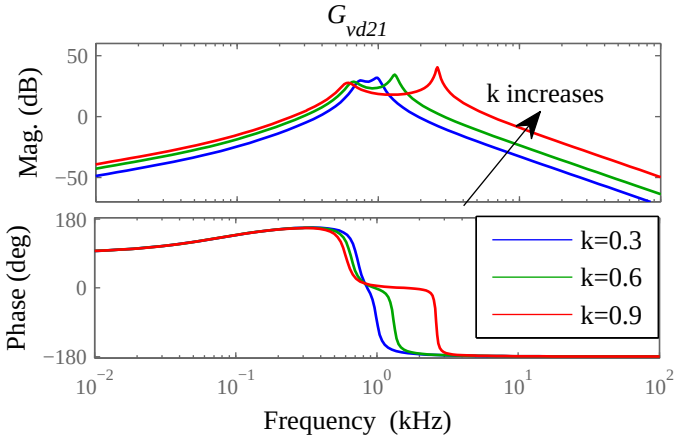


Figure 3.11: Bode plot for cross-coupling transfer function G_{vd21} of CI-SIDO buck with different k

CI-SIDO boost converter using bode plot, step response plot. The parameter used are shown in Table 3.1

3.4.1 CI-SIDO Buck Converter

The cross-coupling transfer functions of CI-SIDO buck converters are given by

$$G_{vd12} = \frac{k\sqrt{\frac{L_1}{L_2}}\frac{V_{in}}{L_1'C_1}s(s+\frac{1}{R_2C_2})}{(s^2+\frac{s}{R_2C_2}+\frac{1}{L_2'C_2})(s^2+\frac{s}{R_1C_1}+\frac{1}{L_1'C_1})-\frac{k^2}{L_1'L_2'C_1C_2}}$$
$$G_{vd21} = \frac{k\sqrt{\frac{L_2}{L_1}}\frac{V_{in}}{L_2'C_2}s(s+\frac{1}{R_1C_1})}{(s^2+\frac{s}{R_2C_2}+\frac{1}{L_2'C_2})(s^2+\frac{s}{R_1C_1}+\frac{1}{L_1'C_1})-\frac{k^2}{L_1'L_2'C_1C_2}} \quad (3.10)$$

From (3.10) it is observed that cross-coupling transfer function have a zero at origin which means cross-coupling only affects the transient performance. Moreover, it is found that gain of cross-coupling transfer function depends on k. Thus with increase in k, the gain increases. Figure 3.11 shows the bode plot of cross-coupling transfer function G_{vd21} with different k value for CI-SIDO buck converter. It is observed from Figure 3.11 that with increase in k, the resonant peak increases. Figure 3.12 shows the step response of G_{vd21} with increase in k and is observed that with increase in k the overshoot and settling time of step response of output voltage increases. Figure 3.12(b) shows the plot of overshoot in v_{02} with increase in k and is found that with increase in k, cross-coupling effect (overshoot in output voltage) increases.

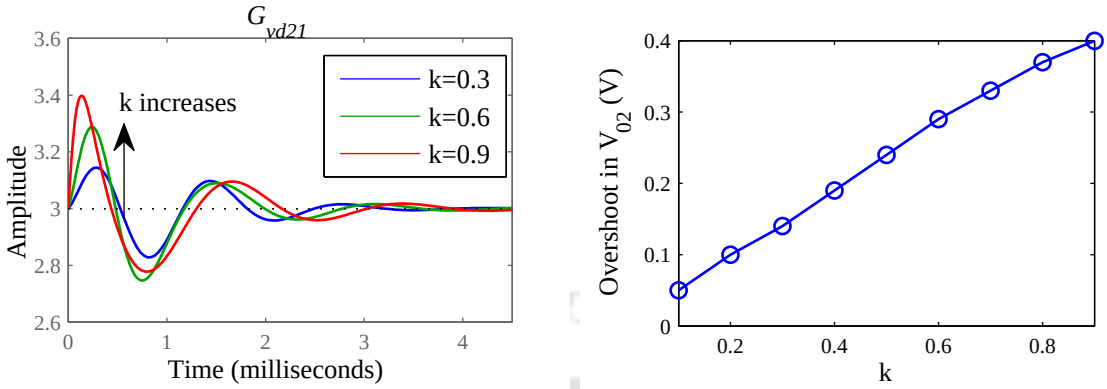


Figure 3.12: Effect of k on cross-coupling transfer function G_{vd21} of CI-SIDO buck converter (a) step response (b) overshoot in v_{02} vs k

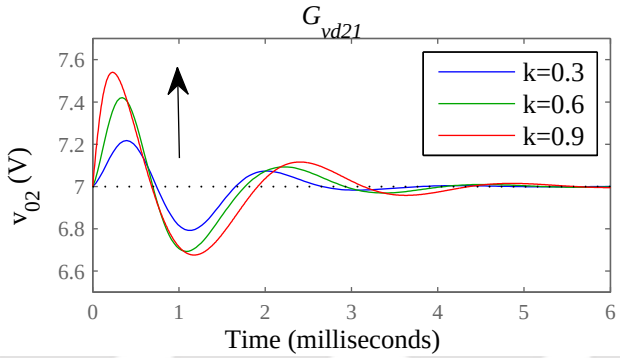


Figure 3.13: Effect of k on cross-coupling transfer function G_{vd21} of CI-SIDO boost

3.4.2 CI-SIDO Boost Converter

The cross-coupling transfer functions of CI-SIDO boost converters are given by

$$G_{vd12} = k\sqrt{\frac{L_1}{L_2}}\frac{V_{in}D_1'}{L_1'C_1D_2'}\frac{s(s+\frac{2}{R_2C_2})}{(s^2+\frac{s}{R_2C_2}+\frac{(1-D_2)^2}{L_2'C_2})(s^2+\frac{s}{R_1C_1}+\frac{(1-D_1)^2}{L_1'C_1})-\frac{k^2(1-D_1)^2(1-D_2)^2}{L_1'L_2'C_1C_2}}$$
$$G_{vd21} = k\sqrt{\frac{L_2}{L_1}}\frac{V_{in}D_2'}{L_2'C_2D_1'}\frac{s(s+\frac{2}{R_1C_1})}{(s^2+\frac{s}{R_2C_2}+\frac{(1-D_2)^2}{L_2'C_2})(s^2+\frac{s}{R_1C_1}+\frac{(1-D_1)^2}{L_1'C_1})-\frac{k^2(1-D_1)^2(1-D_2)^2}{L_1'L_2'C_1C_2}} \quad (3.11)$$

From (3.11) it is observed that cross-coupling transfer function depend on k and only affects the transient performance. Figure 3.13 shows the step response of cross-coupling transfer function G_{vd21} with different k value for CI-SIDO boost converter. Same observation is found that with increase in k, the maximum overshoot increases.

3.5 Effect of Coefficient of Coupling on Load Regulation

In CI-SIDO converters, load regulation is divided into two part, i.e., self-regulation and cross-regulation. Self-regulation is defined as the effect on the output voltage of one sub-converter due to variation in load current of same sub-converter. Cross-regualtion is defined as the effect on the output voltage of one sub-converter due to variation in load current of other sub-converter. The cross-regulation in CI-SIDO converter occur due to k and affects the converter performance. Following subsection analyzes the effect of k on the self-regulation and cross-cross-regulation transfer function of two type of CI-SIDO converters, i.e., CI-SIDO buck converter and CI-SIDO boost converter using bode plot and step response plot. The parameter used are shown in Table 3.1.

3.5.1 CI-SIDO Buck Converter

The self-regulation transfer functions of CI-SIDO buck converter are given by:

$$\begin{aligned} Z_{vi11} &= \frac{\frac{-s}{C_1}(s^2+\frac{s}{C_2R_2}+\frac{1}{C_2L_2'})}{(s^2+\frac{s}{R_2C_2}+\frac{1}{L_2'C_2})(s^2+\frac{s}{R_1C_1}+\frac{1}{L_1'C_1})-\frac{k^2}{L_1'L_2'C_1C_2}} \\ Z_{vi22} &= \frac{\frac{-s}{C_2}(s^2+\frac{s}{C_1R_1}+\frac{1}{C_1L_1'})}{(s^2+\frac{s}{R_2C_2}+\frac{1}{L_2'C_2})(s^2+\frac{s}{R_1C_1}+\frac{1}{L_1'C_1})-\frac{k^2}{L_1'L_2'C_1C_2}} \end{aligned} \tag{3.12}$$

The cross-regulation transfer functions of CI-SIDO buck converter are given by:

$$\begin{aligned} Z_{vi12} &= \frac{k\sqrt{\frac{L_1}{L_2}}\frac{s}{C_1C_2L_1'}}{(s^2+\frac{s}{R_2C_2}+\frac{1}{L_2'C_2})(s^2+\frac{s}{R_1C_1}+\frac{1}{L_1'C_1})-\frac{k^2}{L_1'L_2'C_1C_2}} \\ Z_{vi21} &= \frac{k\sqrt{\frac{L_2}{L_1}}\frac{s}{C_1C_2L_2'}}{(s^2+\frac{s}{R_2C_2}+\frac{1}{L_2'C_2})(s^2+\frac{s}{R_1C_1}+\frac{1}{L_1'C_1})-\frac{k^2}{L_1'L_2'C_1C_2}} \end{aligned} \tag{3.13}$$

From (3.12), (3.13) it is observed that self-regulation and cross-regulation transfer functions have a zero at origin. Due to the presence of zero at origin, self-regulation and cross-regulation transfer functions affect only the transient performance. Moreover, it is observed that, k directly affects the cross-regulation transfer functions.

Figure 3.14 shows the step response of Z_{vi11}, Z_{vi21} with different k value. From Figure

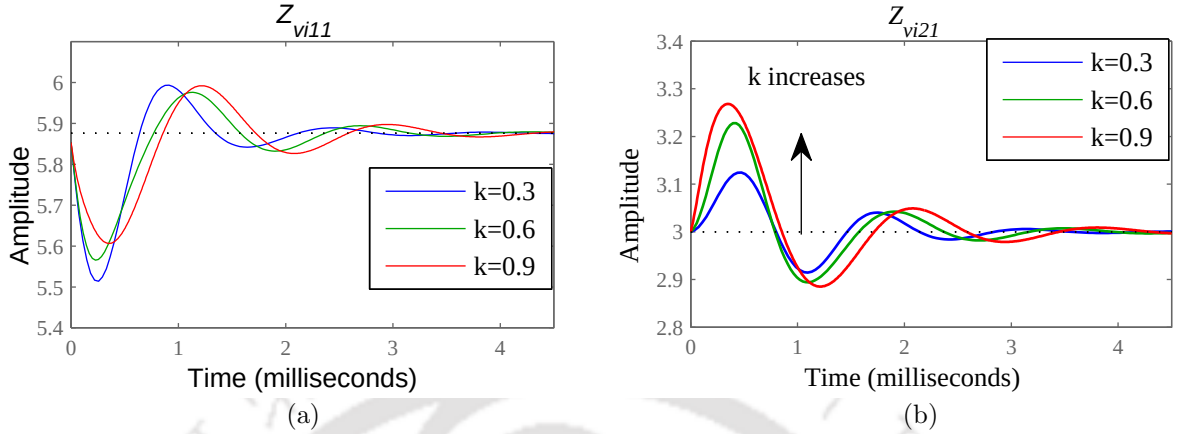


Figure 3.14: Effect of k on self-regulation and cross-regulation transfer function of CI-SIDO buck (a) Z_{vi11} (b) Z_{vi21}

3.14 it is observed that with increase in k, the self-regulation effect (undershoot) decreases and cross-regulation effect (overshoot) increases.

3.5.2 CI-SIDO Boost Converter

The self-regulation transfer functions of CI-SIDO boost converter are given by:

$$Z_{vi11} = \frac{\frac{-s}{C_1}(s^2 + \frac{s}{R_2C_2} + \frac{D_2'^2}{L_2'C_2})}{(s^2 + \frac{s}{R_2C_2} + \frac{(1-D_2)^2}{L_2'C_2})(s^2 + \frac{s}{R_1C_1} + \frac{(1-D_1)^2}{L_1'C_1}) - \frac{k^2(1-D_1)^2(1-D_2)^2}{L_1'L_2'C_1C_2}}$$
$$Z_{vi22} = \frac{\frac{-s}{C_2}(s^2 + \frac{s}{R_1C_1} + \frac{D_1'^2}{L_1'C_1})}{(s^2 + \frac{s}{R_2C_2} + \frac{(1-D_2)^2}{L_2'C_2})(s^2 + \frac{s}{R_1C_1} + \frac{(1-D_1)^2}{L_1'C_1}) - \frac{k^2(1-D_1)^2(1-D_2)^2}{L_1'L_2'C_1C_2}} \quad (3.14)$$

The cross-regulation transfer function of CI-SIDO boost converter are given by:

$$Z_{vi12} = k\sqrt{\frac{L_1}{L_2}}\frac{D_1'D_2'}{L_1'C_1C_2}\frac{s}{(s^2 + \frac{s}{R_2C_2} + \frac{(1-D_2)^2}{L_2'C_2})(s^2 + \frac{s}{R_1C_1} + \frac{(1-D_1)^2}{L_1'C_1}) - \frac{k^2(1-D_1)^2(1-D_2)^2}{L_1'L_2'C_1C_2}}$$
$$Z_{vi21} = k\sqrt{\frac{L_2}{L_1}}\frac{MD_1'D_2'}{L_2'C_1C_2}\frac{s}{(s^2 + \frac{s}{R_2C_2} + \frac{(1-D_2)^2}{L_2'C_2})(s^2 + \frac{s}{R_1C_1} + \frac{(1-D_1)^2}{L_1'C_1}) - \frac{k^2(1-D_1)^2(1-D_2)^2}{L_1'L_2'C_1C_2}} \quad (3.15)$$

From (3.14), (3.15) it is observed that self-regulation and cross-regulation transfer functions only affect the transient performance due to the presence of zero at origin. Moreover, it is observed that, k directly affects the low frequency gain of cross-regulation transfer functions.

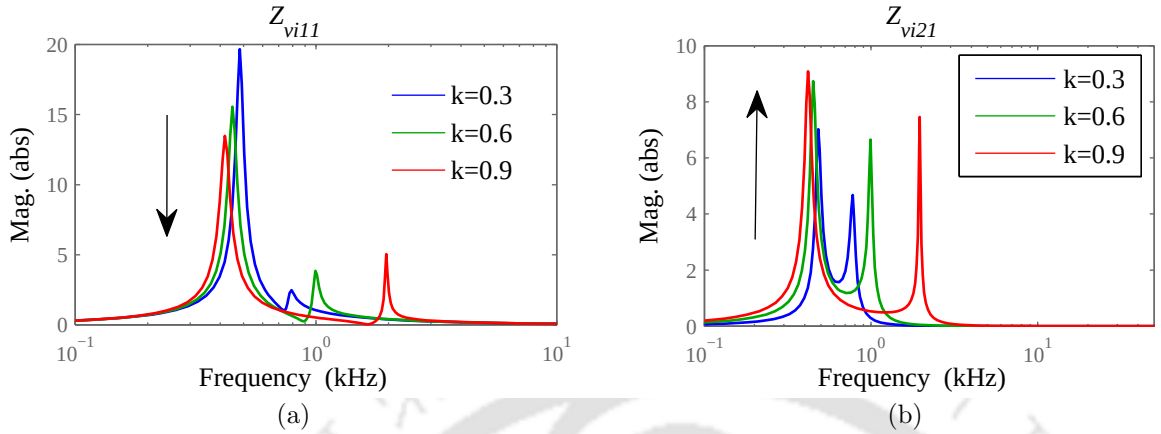


Figure 3.15: Effect of k on self-regulation and cross-regulation transfer function of CI-SIDO boost (a) Z_{vi11} (b) Z_{vi21}

Figure 3.15 shows the magnitude plot of self-regulation Z_{vi11} and cross-regulation Z_{vi21} transfer function for different k value. It is observed that, with increase in k, resonant peak of Z_{vi11} decreases and resonant peak of Z_{vi21} increases. Thus, it is concluded that with increase in k, self-regulation (undershoot) decreases and cross-regulation effect (overshoot) increases.

3.6 Main Findings and Choice of k

Based on the analysis following are the effects of mutual coupling on CI-SIDO converter:

(i) With increase in coupling, the boundary inductance value increase. Thus for tight coupling higher value of L_1, L_2 are needed to operate the converter in CCM and hence effects the power density of converter.

(ii) In CI-SIDO converters the quality factors of resonant pole and zero frequencies depend on k. Thus, as k increases the quality factors increases. In frequency response, increase in quality factors lead to increase in magnitude of resonant peaks which may lead to conditional stability. In time domain, increase in quality factors lead to increase in settling time which degrade transient characteristics of the converter.

(iii) In CI-SIDO boost converter, the complex zero of control-to-output transfer functions

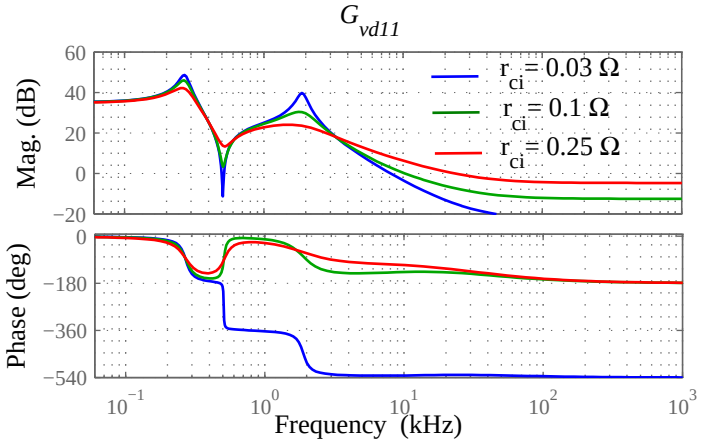


Figure 3.16: Bode plot of G_{vd11} of CI-SIDO boost at $k = 0.95$ with different ESR of capacitors r_{ci} where $i = \{1, 2\}$

(G_{vd11}, G_{vd22}) depend on k. Thus, with tight coupling, the complex zero moves to right half plane and degrade the system stability.

(iv) It is also observed that the cross-coupling and cross-regulation transfer functions of CI-SIDO converter depends on k. Thus, with tight coupling, cross-coupling and cross-regulation effect increases which degrade the dynamic performance of the converter.

The conditional stability and RHP complex zero can be avoided by increasing the effective series resistance (ESR) of capacitors and inductors as observed in Figure 3.16. The reason is that quality factors depends on ESR and it reduces with increase in ESR. However, high values of ESR reduces the efficiency of converter.

Therefore, to prevent conditional stability and obtain better dynamic characteristic of CI-SIDO converter medium coupling ($0.4 < k < 0.7$) of coupled inductor is preferred.

3.7 Experimental Verification

To verify the theoretical analysis, experiments are performed for CI-SIDO buck and CI-SIDO boost converter. The experimental prototype of CI-SIDO converter is shown in Figure 3.17.

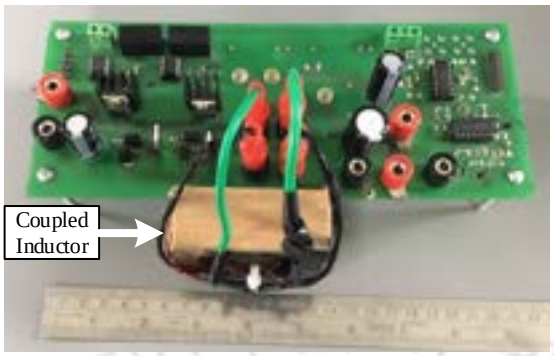


Figure 3.17: Experimental prototype of CI-SIDO converter

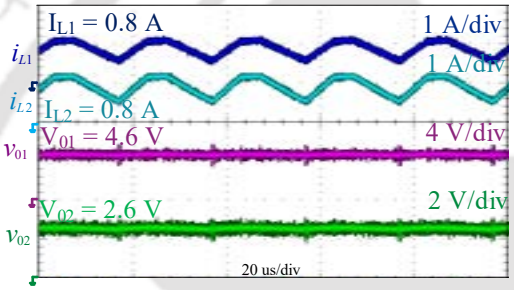


Figure 3.18: Steady state experimental results of CI-SIDO buck converter

3.7.1 Experimental Results of CI-SIDO Buck Converter

The circuit parameters of CI-SIDO buck converter are:

$V_{in} = 10$ V, $D_1 = 0.5$, $D_2 = 0.3$, $C_1 = C_2 = 320$ μF, $R_1 = 6$ Ω, $R_2 = 3$ Ω, $f_s = 50$ kHz. The experiment of CI-SIDO buck converter is done for two cases, i.e., Case I: medium coupling $k = 0.45$ and Case II: tight coupling $k = 0.8$. The coupled inductor values for two cases are:

Case I: $L_1 = 118$ μH, $L_2 = 112$ μH, $M = 52$ μH.

Case II: $L_1 = 118$ μH, $L_2 = 112$ μH, $M = 92$ μH.

3.7.1.1 Steady-state Results

Corresponding to duty cycle $D_1 = 0.5$, $D_2 = 0.3$, the steady-state output voltages are $V_{01} = 5$ V, $V_{02} = 3$ V for ideal case. Figure 3.18 shows the steady-state results of CI-SIDO buck converters. The obtained steady-state values are $V_{01} = 4.6$ V, $V_{02} = 2.6$ V. This is due to the practical nature of semiconductor switches, such as diode forward drop, MOSFET on-state resistance, etc.

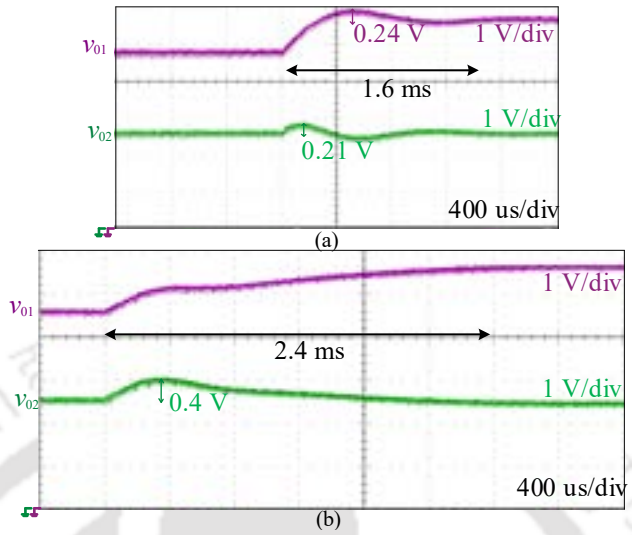


Figure 3.19: Experimental results of CI-SIDO buck converter for step change in d_1 (a) Medium coupling $k = 0.45$ (b) Tight coupling $k = 0.8$

3.7.1.2 Transient Waveform

Figure 3.19 shows the transient response of CI-SIDO buck with medium and tight coupling for step change is duty cycle D_1. In medium coupling case as shown in Figure 3.19(a), when D_1 changes from 0.5 to 0.6, V_{01} changes from 4.6 V to 5.6 V in time 1.24 ms with overshoot 0.24 V and V_{02} experience cross-coupling effect (overshoot) of 0.21 V. In tight coupling case as shown in Figure 3.19(b), the settling time increases to 2.4 ms, and cross-coupling in V_{02} increases to 0.4 V. Thus, from Figure 3.19, it is conclude that with tight coupling cross-coupling and settling time increases. This validated the theoretical analysis.

3.7.2 Experimental Results of CI-SIDO Boost Converters

The circuit parameters of CI-SIDO boost converter are:
$V_{in} = 5$ V, $D_1 = 0.5$, $D_2 = 0.3$, $C_1 = C_2 = 220$ μF, $R_1 = 24$ Ω, $R_2 = 14$ Ω, $f_s = 50$ kHz. The experiment of CI-SIDO boost converter is done for two cases as like CI-SIDO buck.

3.7.2.1 Steady-state Results

Corresponding to duty cycle $D_1 = 0.5$, $D_2 = 0.3$, the steady-state output voltages are $V_{01} = 10$ V, $V_{02} = 7.14$ V for ideal case. Figure 3.20 shows the steady-state results of CI-SIDO

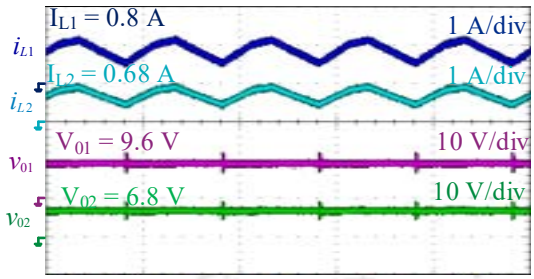


Figure 3.20: Steady state experimental results CI-SIDO boost converter

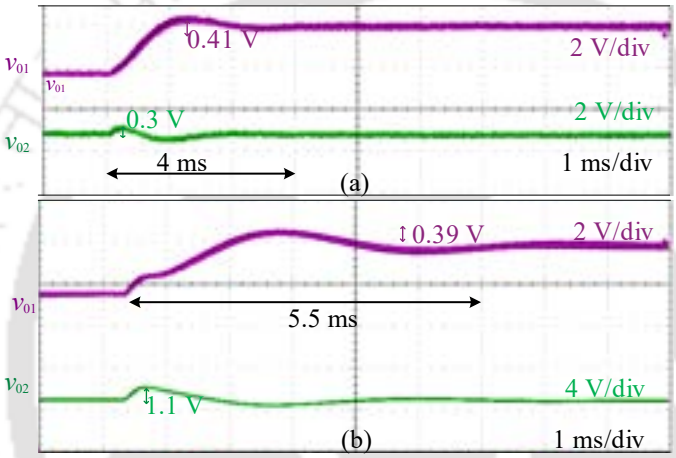


Figure 3.21: Experimental results of CI-SIDO boost converter for step change in d_1 (a) medium coupling (b) tight coupling

boost converters. The obtained steady-state values are $V_{01} = 9.6$ V, $V_{02} = 6.8$ V. This is due to the practical nature of semiconductor switches.

3.7.2.2 Transient Results

Figure 3.21 shows the transient response of CI-SIDO boost converter with medium and tight coupling for step change in D_1. In medium coupling case (Figure 3.21(a)), when D_1 changes from 0.5 to 0.6, V_{01} changes from 9.6 V to 12 V in time 4 ms with overshoot 0.41 V and V_{02} experience cross-coupling effect (overshoot) of 0.3 V. In tight coupling case (Figure 3.21(b)), the settling time increases to 5.5 ms, overshoot in V_{01} is 0.39 V and cross-coupling in V_{02} increases to 1.1 V. Thus, from Figure 3.21, it is conclude that with tight coupling cross-coupling and settling time increases. This validated the theoretical analysis.

3.8 Conclusion

This chapter describes how the coefficient of coupling k affects the frequency domain and time domain characteristics of CI-SIDO converters, i.e., CI-SIDO buck converter and CI-SIDO boost converter. The analyses is carried out using various transfer functions derived in Chapter 2. It is observed that with increase in coefficient of coupling k, the pole and zeros varies and the converter control-to-output transfer functions has interlaced pole-zero distribution. With interlaced pole-zero distribution converter the controller design is easy. However, it is observed that with increase in k, the complex zero moves to right half plane which cause instability and also experience multiple resonant peak and may lead to conditional stability. Moreover, it is found that with increase in k, the cross-coupling and cross-regulation effect increases. Therefore, to prevent RHP complex zero, conditional stability and reduce cross-coupling and cross-regulation effect, moderate coupling is preferred for CI-SIDO converters.

4

Decoupled Voltage Mode Control of CI-SIDO Buck Converter

Contents

4.1 Introduction

Chapter 2 has presented the modelling of CI-SIDO buck converter. The modelling shows that two output voltages are coupled, leading to cross-coupling and cross-regulation problems, due to coupling in the inductor currents. Each output voltage suffers from cross-regulation effect when there is a step-change in load of other output. This affects system performance. The duty cycle of one output is coupled to the other output through the cross-coupling transfer function. This makes it challenging to find the loop gains for outputs to design the controller. Thus, with a dual output converter, the converter control, and design becomes complex as compared to the SISO buck converter.

The objective of this chapter is to present the small-signal analysis of CI-SIDO buck converter with voltage-mode control. The analysis is focused on developing a decoupling condition that can decouple the two outputs and make the controller design independent. The effect of decoupling on the closed-loop transfer functions of the system are analyzed. Also, the stability of the closed-loop system is studied. Based on the condition of decoupling and stability, the procedure for the compensator design is derived. Finally, the proposed decoupling methods are validated both using simulations and experiments.

4.2 Circuit Operation of CI-SIDO Buck Converter with Voltage Mode Control

The CI-SIDO buck converter with voltage mode control is shown in Figure 4.1(a). For two output in CI-SIDO buck converter, two feedback loops are realized. The feedback loops are formed using two controllers G_{v1}, G_{v2}, two pulse width modulator (PWM) gains G_{m1}, G_{m2} and two feedback gains β_1, β_2. In voltage mode control, the duty cycles d_1, d_2 are controlled by the control voltages v_{cn1}, v_{cn2} which are derived from the reference voltage v_{ref1}, v_{ref2} and feedback voltage v_{f1}, v_{f2}. Using the small-signal model of CI-SIDO buck converter developed in Chapter 2, the small-signal block diagram model of closed-loop voltage mode controlled CI-SIDO buck converter is shown in Figure 4.1(b).

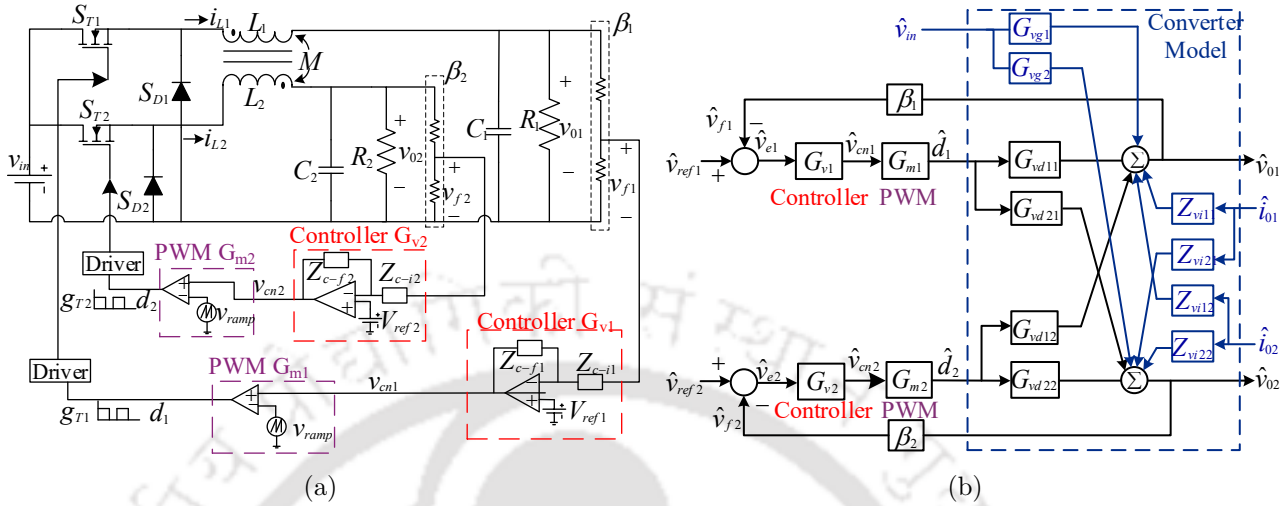


Figure 4.1: Voltage mode control of CI-SIDO buck converter

4.3 Proposed Decoupled Voltage Mode Control of CI-SIDO buck Converter

The output voltages as shown in Figure 4.1(b) can be written as

$$\begin{bmatrix} \hat{v}_{01} \\ \hat{v}_{02} \end{bmatrix} = \begin{bmatrix} G_{vd11} & G_{vd12} \\ G_{vd21} & G_{vd22} \end{bmatrix} \begin{bmatrix} \hat{d}_1 \\ \hat{d}_2 \end{bmatrix} + \begin{bmatrix} G_{vg1} \\ G_{vg2} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \end{bmatrix} + \begin{bmatrix} Z_{vi11} & Z_{vi12} \\ Z_{vi21} & Z_{vi22} \end{bmatrix} \begin{bmatrix} \hat{i}_{01} \\ \hat{i}_{02} \end{bmatrix} \tag{4.1}$$

The duty cycles are generated by the controllers as shown in Figure 4.1(b) and is given as

$$\begin{bmatrix} \hat{d}_1 \\ \hat{d}_2 \end{bmatrix} = \begin{bmatrix} G_{v1}G_{m1} & 0 \\ 0 & G_{v2}G_{m2} \end{bmatrix} \begin{bmatrix} \hat{v}_{ref1} - \beta_1\hat{v}_{01} \\ \hat{v}_{ref2} - \beta_2\hat{v}_{02} \end{bmatrix} \tag{4.2}$$

Using (4.2) in (4.1) becomes as

$$\begin{bmatrix} \hat{v}_{01} \\ \hat{v}_{02} \end{bmatrix} = \begin{bmatrix} G_{vd11} & G_{vd12} \\ G_{vd21} & G_{vd22} \end{bmatrix} \begin{bmatrix} G_{v1}G_{m1} & 0 \\ 0 & G_{v2}G_{m2} \end{bmatrix} \begin{bmatrix} \hat{v}_{ref1} - \beta_1\hat{v}_{01} \\ \hat{v}_{ref2} - \beta_2\hat{v}_{02} \end{bmatrix} + \begin{bmatrix} G_{vg1} \\ G_{vg2} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \end{bmatrix} + \begin{bmatrix} Z_{vi11} & Z_{vi12} \\ Z_{vi21} & Z_{vi22} \end{bmatrix} \begin{bmatrix} \hat{i}_{01} \\ \hat{i}_{02} \end{bmatrix} \tag{4.3}$$

Rearranging (4.3), we get:

$$\begin{bmatrix} 1+\beta_1 G_{v1}G_{m1}G_{vd11} & \beta_2 G_{v2}G_{m2}G_{vd12} \\ \beta_1 G_{v1}G_{m1}G_{vd21} & 1+\beta_2 G_{v2}G_{m2}G_{vd22} \end{bmatrix} \begin{bmatrix} \hat{v}_{01} \\ \hat{v}_{02} \end{bmatrix} = \begin{bmatrix} G_{v1}G_{m1}G_{vd11} & G_{v2}G_{m2}G_{vd12} \\ G_{v1}G_{m1}G_{vd21} & G_{v2}G_{m2}G_{vd22} \end{bmatrix} \begin{bmatrix} \hat{v}_{ref1} \\ \hat{v}_{ref2} \end{bmatrix} + \begin{bmatrix} G_{vg1} \\ G_{vg2} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \end{bmatrix} + \begin{bmatrix} Z_{vi11} & Z_{vi12} \\ Z_{vi21} & Z_{vi22} \end{bmatrix} \begin{bmatrix} \hat{i}_{01} \\ \hat{i}_{02} \end{bmatrix} \quad (4.4)$$

By nullifying the disturbances, i.e., $\hat{v}_{in} = \hat{i}_{01} = \hat{i}_{02} = 0$ in (4.4) and solving the equation, we get, the closed-loop reference-to-output as

$$\begin{bmatrix} \hat{v}_{01} \\ \hat{v}_{02} \end{bmatrix} = \begin{bmatrix} \frac{A'_{11}}{1+T'_1} & \frac{A'_{12}}{1+T'_1} \\ \frac{A'_{21}}{1+T'_2} & \frac{A'_{22}}{1+T'_2} \end{bmatrix} \begin{bmatrix} \hat{v}_{ref1} \\ \hat{v}_{ref2} \end{bmatrix} \quad (4.5)$$

where,

$$\begin{aligned} A'_{12} &= G_{v2}G_{m2}\left(G_{vd12} - \frac{G_{vd12}G_{vd22}\beta_2 G_{v2}G_{m2}}{1+G_{vd22}G_{v2}G_{m2}\beta_2}\right) \\ A'_{21} &= G_{v1}G_{m1}\left(G_{vd21} - \frac{G_{vd21}G_{vd11}\beta_1 G_{v1}G_{m1}}{1+G_{vd11}G_{v1}G_{m1}\beta_1}\right) \end{aligned} \quad (4.6)$$

$$\begin{aligned} A'_{11} &= G_{v1}G_{m1}\left(G_{vd11} - \frac{G_{vd21}G_{vd12}\beta_2 G_{v2}G_{m2}}{1+G_{vd22}G_{v2}G_{m2}\beta_2}\right) \\ A'_{22} &= G_{v2}G_{m2}\left(G_{vd22} - \frac{G_{vd21}G_{vd12}\beta_1 G_{v1}G_{m1}}{1+G_{vd11}G_{v1}G_{m1}\beta_1}\right) \end{aligned} \quad (4.7)$$

$$\begin{aligned} T'_1 &= \beta_1 G_{v1}G_{m1}\left(G_{vd11} - \frac{G_{vd21}G_{vd12}\beta_2 G_{v2}G_{m2}}{1+G_{vd22}G_{v2}G_{m2}\beta_2}\right) \\ T'_2 &= \beta_2 G_{v2}G_{m2}\left(G_{vd22} - \frac{G_{vd12}G_{vd21}\beta_1 G_{v1}G_{m1}}{1+G_{vd11}G_{v1}G_{m1}\beta_1}\right) \end{aligned} \quad (4.8)$$

T'_1 and T'_2 are the outer loop gain transfer functions.

It is observed from (4.5) that there exist cross-coupling between the two voltage mode controls. Moreover, it is found from (4.8) that the outer loop gain transfer functions T'_1, T'_2 depends on both controller G_{v1}, G_{v2}. Thus, the design of controller is not independent.

4.3.1 Approximate Decoupling

It is observed from (4.5) that, if $A'_{12} \approx 0$ and $A'_{21} \approx 0$ then the voltage mode control becomes decoupled. From (4.6), we observe that if the compensator's G_{v1} and G_{v2} are designed such

that,

$$|G_{vd11}G_{v1}G_{m1}\beta_1| >> 1 \text{ and } |G_{vd22}G_{v2}G_{m2}\beta_2| >> 1 \tag{4.9}$$

then the closed-loop reference-to-output relationship of (4.5) becomes

$$\begin{bmatrix} \hat{v}_{01} \\ \hat{v}_{02} \end{bmatrix} = \begin{bmatrix} \frac{A_{11}}{1+T_1} & \epsilon \\ \epsilon & \frac{A_{22}}{1+T_2} \end{bmatrix} \begin{bmatrix} \hat{v}_{ref1} \\ \hat{v}_{ref2} \end{bmatrix} \tag{4.10}$$

where $\epsilon \to 0$ and

$$A_{11} = G_{v1}G_{m1}G_{vd1} \approx A_{11}^{'}, \quad A_{22} = G_{v2}G_{m2}G_{vd2} \approx A_{22}^{'} \tag{4.11}$$

$$T_1 = \beta_1 G_{v1}G_{m1}G_{vd1} \approx T_1^{'}, \quad T_2 = \beta_2 G_{v2}G_{m2}G_{vd2} \approx T_2^{'} \tag{4.12}$$

where, T_1 and T_2 are the approximated outer loop gain transfer functions, G_{vd1}, G_{vd2} are the approximated control-to-output voltage transfer functions. The expression of G_{vd1}, G_{vd2} are given by

$$\begin{aligned} G_{vd1} &= G_{vd11} - \frac{G_{vd21}G_{vd12}}{G_{vd22}} = \frac{V_{in}r_1^{'}}{L_1} \frac{(s + \frac{1}{r_{c1}C_1})}{s^2 + s(\frac{r_1^{'}}{L_1} + \frac{r_1^{''}}{C_1}) + \frac{R_1 r_1^{''}}{L_1 C_1}} \\ G_{vd2} &= G_{vd22} - \frac{G_{vd21}G_{vd12}}{G_{vd11}} = \frac{V_{in}r_2^{'}}{L_2} \frac{(s + \frac{1}{r_{c2}C_2})}{s^2 + s(\frac{r_2^{'}}{L_2} + \frac{r_2^{''}}{C_2}) + \frac{R_2 r_2^{''}}{L_2 C_2}} \end{aligned} \tag{4.13}$$

From (4.13), it is observed that approximated control-to-output voltage transfer functions G_{vd1}, G_{vd2} is same as that of control-to-output transfer functions of simple buck converter.

Therefore, we observe that if G_{v1} and G_{v2} are designed satisfying (4.9), then the two outputs v_{01}, v_{02} get decoupled, and the closed-loop reference-to-output transfer function of CI-SIDO buck converter becomes same as simple buck converter.

4.3.2 Effect of Decoupling on Closed-loop Performance

The effect of decoupling on closed-loop performance of CI-SIDO buck converter is evaluated by analysing closed-loop audio susceptibility and load regulations.

4.3.2.1 Closed-loop Audio-susceptibility

Closed-loop audio susceptibility refers to the regulation ability to attenuate the disturbance propagating from input voltage to output voltages. The closed-loop audio susceptibility transfer functions can be calculated using (4.4) by making $\hat{v}_{ref1} = \hat{v}_{ref2} = \hat{i}_{01} = \hat{i}_{02} = 0$ and solving the equation we get,

$$\begin{bmatrix} \hat{v}_{01} \\ \hat{v}_{02} \end{bmatrix} = \begin{bmatrix} 1+\beta_1 G_{v1} G_{m1} G_{vd11} & \beta_2 G_{v2} G_{m2} G_{vd12} \\ \beta_1 G_{v1} G_{m1} G_{vd21} & 1+\beta_2 G_{v2} G_{m2} G_{vd22} \end{bmatrix}^{-1} \begin{bmatrix} G_{vg1} \\ G_{vg2} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \end{bmatrix} \tag{4.14}$$

solving we get,

$$\begin{aligned} G'_{vg1-cl} &= \left.\frac{\hat{v}_{01}}{\hat{v}_{in}}\right|_{CL} = \frac{G_{vg1} - \frac{G_{vg2}G_{vd12}\beta_2 G_{v2}G_{m2}}{1+G_{vd22}G_{v2}G_{m2}\beta_2}}{1+T'_1} \\ G'_{vg2-cl} &= \left.\frac{\hat{v}_{02}}{\hat{v}_{in}}\right|_{CL} = \frac{G_{vg2} - \frac{G_{vg1}G_{vd21}\beta_1 G_{v1}G_{m1}}{1+G_{vd11}G_{v1}G_{m1}\beta_1}}{1+T'_2} \end{aligned} \tag{4.15}$$

Applying approximation of (4.9) in (4.15), we get

$$\begin{aligned} G'_{vg1-cl} &\approx \frac{G_{vg1} - \frac{G_{vd12}G_{vg2}}{G_{vd22}}}{1+T_1} = \frac{G_{v1}}{1+T_1} \equiv G_{vg1-cl} \\ G'_{vg2-cl} &\approx \frac{G_{vg2} - \frac{G_{vd21}G_{vg1}}{G_{vd11}}}{1+T_2} = \frac{G_{v2}}{1+T_2} \equiv G_{vg2-cl} \end{aligned} \tag{4.16}$$

Where, G_{v1}, G_{v2} are the approximated audio-susceptibility transfer functions and are given by

$$G_{v1} = \frac{D_1 r_1^{'}}{L_1} \frac{(s+\frac{1}{r_{c1}C_1})}{s^2 + s(\frac{r'_1}{L_1} + \frac{r''_1}{C_1}) + \frac{R_1 r''_1}{L_1 C_1}}, \quad G_{v2} = \frac{D_2 r_2^{'}}{L_2} \frac{(s+\frac{1}{r_{c2}C_2})}{s^2 + s(\frac{r'_2}{L_2} + \frac{r''_2}{C_2}) + \frac{R_2 r''_2}{L_2 C_2}} \tag{4.17}$$

From (4.16), it is observed that if (4.9) is satisfied than the closed-loop audio susceptibility of CI-SIDO buck converter get simplified and becomes same as that of simple buck converter. Further, it can be observed that the loop gain contributes to the closed-loop audio susceptibility. Larger the loop gains T_1, T_2 better is the audio susceptibility.

4.3.2.2 Closed-loop Load Regulation

Closed-loop load regulation is of two types - self-regulation and cross-regulation. Closed-loop self-regulation refers to the ability to attenuate disturbances propagating from the one

load current to the corresponding self output voltage. Closed-loop cross-regulation refers to the regulation ability to attenuate disturbances propagating from the one load current to the cross output voltage.

The closed-loop load regulation transfer functions can be calculated using (4.4) by making $\hat{v}_{ref1} = \hat{v}_{ref2} = \hat{v}_{in} = 0$ and solving the equation we get,

$$\begin{bmatrix} \hat{v}_{01} \\ \hat{v}_{02} \end{bmatrix} = \begin{bmatrix} 1+\beta_1 G_{v1} G_{m1} G_{vd11} & \beta_2 G_{v2} G_{m2} G_{vd12} \\ \beta_1 G_{v1} G_{m1} G_{vd21} & 1+\beta_2 G_{v2} G_{m2} G_{vd22} \end{bmatrix}^{-1} \begin{bmatrix} Z_{vi11} & Z_{vi12} \\ Z_{vi21} & Z_{vi22} \end{bmatrix} \begin{bmatrix} \hat{i}_{01} \\ \hat{i}_{02} \end{bmatrix} \tag{4.18}$$

solving we get,

Closed-loop self-regulation transfer functions:

$$\begin{aligned} Z'_{vi11-cl} &= \left.\frac{\hat{v}_{01}}{\hat{i}_{01}}\right|_{CL} = \frac{Z_{vi11} - \frac{Z_{vi21} G_{vd12} \beta_2 G_{v2} G_{m2}}{1+G_{vd22} G_{v2} G_{m2} \beta_2}}{1+T'_1} \\ Z'_{vi22-cl} &= \left.\frac{\hat{v}_{02}}{\hat{i}_{02}}\right|_{CL} = \frac{Z_{vi22} - \frac{Z_{vi12} G_{vd21} \beta_1 G_{v1} G_{m1}}{1+G_{vd11} G_{v1} G_{m1} \beta_1}}{1+T'_2} \end{aligned} \tag{4.19}$$

Closed-loop cross-regulation transfer functions:

$$\begin{aligned} Z'_{vi12-cl} &= \left.\frac{\hat{v}_{01}}{\hat{i}_{02}}\right|_{CL} = \frac{Z_{vi12} - \frac{Z_{vi22} G_{vd12} \beta_2 G_{v2} G_{m2}}{1+G_{vd22} G_{v2} G_{m2} \beta_2}}{1+T'_1} \\ Z'_{vi21-cl} &= \left.\frac{\hat{v}_{02}}{\hat{i}_{01}}\right|_{CL} = \frac{Z_{vi21} - \frac{Z_{vi11} G_{vd21} \beta_1 G_{v1} G_{m1}}{1+G_{vd11} G_{v1} G_{m1} \beta_1}}{1+T'_2} \end{aligned} \tag{4.20}$$

Applying approximation of (4.9) in (4.19), we get the approximated closed loop self-regulation transfer functions as

$$\begin{aligned} Z'_{vi11-cl} &\approx \frac{Z_{vi11} - \frac{Z_{vi21} G_{vd12}}{G_{vd22}}}{1+T_1} = \frac{Z_{vi1}}{1+T_1} \equiv Z_{vi11-cl} \\ Z'_{vi22-cl} &\approx \frac{Z_{vi22} - \frac{Z_{vi12} G_{vd21}}{G_{vd11}}}{1+T_2} = \frac{Z_{vi2}}{1+T_2} \equiv Z_{vi22-cl} \end{aligned} \tag{4.21}$$

where, Z_{vi1}, Z_{vi2} are the approximated self-regulation trnasfer functions and are given by

$$Z_{vi1} = -\frac{r'_1 s(s+\frac{1}{r_{c1}C_1})}{s^2 + s(\frac{r'_1}{L_1} + \frac{r''_1}{C_1}) + \frac{R_1 r''_1}{L_1 C_1}}, \quad Z_{vi2} = -\frac{r'_2 s(s+\frac{1}{r_{c2}C_2})}{s^2 + s(\frac{r'_2}{L_2} + \frac{r''_2}{C_2}) + \frac{R_2 r''_2}{L_2 C_2}} \tag{4.22}$$

Applying approximation of (4.9) in (4.20), we get the approximated closed loop cross-regulation

transfer functions as

$$\begin{aligned} Z'_{vi12-cl} &\approx \frac{Z_{vi12} - \frac{Z_{vi22}G_{vd12}}{G_{vd22}}}{1+T_1} = \frac{\frac{M}{L_2}Z_{vi2}}{1+T_1} \equiv Z_{vi12-cl} \\ Z'_{vi21-cl} &\approx \frac{Z_{vi21} - \frac{Z_{vi11}G_{vd21}}{G_{vd11}}}{1+T_2} = \frac{\frac{M}{L_1}Z_{vi1}}{1+T_2} \equiv Z_{vi21-cl} \end{aligned} \tag{4.23}$$

Following observations are drawn from equations (4.21)-(4.23):

- The self-regulations and cross-regulations can be improved by making the loop gains T_1, T_2 large.
- The closed-loop self-regulations are simplified and become same as simple buck converter.
- It is observed that cross-regulation is due to mutual inductance. Larger the mutual inductance larger is the cross-regulation. However, it can be reduced by designing the compensators such that T_1, T_2 are large.

4.4 Stability of Closed-loop System

The stability of the closed-loop system can be evaluated based on the approximated outer loop gains T_j, $j = \{1, 2\}$. From (4.12), T_j can be expressed as

$$T_j(s) = G_{vj}(s)G_{mj}\beta_j G_{vdj}(s) \quad \text{where}, j = \{1, 2\} \tag{4.24}$$

Type-II compensator is considered for controller G_{v1}, G_{v2} and the circuit diagram is shown in Figure 4.2(a). The transfer function of controller and PWM are given as

$$G_{vj}(s) = \frac{k_{cj}(1 + \frac{s}{\omega_{cj-z}})}{s(1 + \frac{s}{\omega_{cj-p}})}, \quad G_{mj} = \frac{1}{V_m} \tag{4.25}$$

where, $k_{cj} = \frac{1}{r_1(c_1+c_2)}$ is the compensator gain, $\omega_{cj-z} = \frac{1}{c_1 r_2}$ is the compensator zero, $\omega_{cj-p} = \frac{c_1+c_2}{c_1 c_2 r_2}$ is the compensator pole. V_m is the peak voltage of external ramp signal.

Using (4.13), (4.25) in (4.24), we get

$$T_j = \frac{V_{in}\beta_j k_{cj}}{V_m} \frac{(1 + \frac{s}{\omega_{esrj}})(1 + \frac{s}{\omega_{cj-z}})}{s(\frac{s^2}{\omega_{o,j}^2} + \frac{2\zeta_j s}{\omega_{o,j}} + 1)(1 + \frac{s}{\omega_{cj-p}})} \tag{4.26}$$

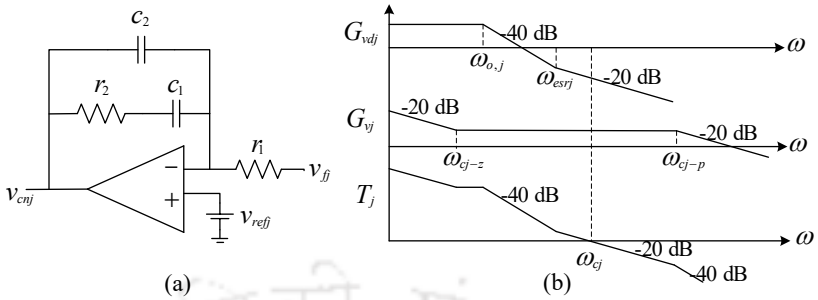


Figure 4.2: (a) Type II compensator (b) Bode plot of G_{vdj}, G_{vj}, desire T_j

where, $\omega_{esrj} = \frac{1}{r_{cj}C_j}$, $\omega_{o,j} = \sqrt{\frac{R_j r_j''}{L_j C_j}}$, $\zeta_j = \frac{C_j r_j' + L_j r_j''}{2\sqrt{L_j C_j R_j r_j''}}$

It is observed from (4.13), that the poles and zero of G_{vdj} lies in left-half of s-plane, i.e., open loop system is stable. Thus, the closed-loop stability depends on the design of G_{vj}. The design of G_{vj} involves calculating compensator gain and finding the location of compensator pole, zero. The compensator gain is related to crossover frequency. Higher the compensator gain, higher will be the crossover frequency.

The goal for compensator design is to make the overall loop transfer function satisfy stability criteria. The Nyquist stability criteria for the closed loop system is $T_j(j\omega) = -1$ and results into

$$|G_{vj}(j\omega)G_{mj}\beta_j G_{vdj}(j\omega)| = 1 \tag{4.27}$$

$$\angle G_{vj}(j\omega)G_{mj}\beta_j G_{vdj}(j\omega) = -\pi \tag{4.28}$$

Considering a phase margin ϕ_m at crossover frequency ω_{cj}, (4.28) becomes as

$$\angle G_{vj}(j\omega_{cj}) + \angle G_{vdj}(j\omega_{cj}) \geq -\pi + \phi_m \tag{4.29}$$

Since a Type-II compensator has a phase lag between 0 to $\pi/2$, we find the crossover frequency ω_{cj} limit to be

$$\begin{aligned} -\pi + \phi_m &\leq \angle G_{vdj}(j\omega_{cj}) \leq -\pi/2 + \phi_m \\ -\pi + \phi_m \leq tan^{-1}\left(\frac{\omega_{cj}}{\omega_{esrj}}\right) &- tan^{-1}\left(\frac{\frac{2\zeta_j\omega_{cj}}{\omega_{o,j}}}{1-(\frac{\omega_{cj}}{\omega_{o,j}})^2}\right) \leq -\pi + \phi_m \end{aligned} \tag{4.30}$$

Table 4.1: Design specification of the converter and compensator

V_{in}	V_{01}, V_{02}	R_1, R_2	C_1, C_2	L_1,L_2	M	f_s	V_m	β_1, β_2
10 V	6 V, 3.3 V	6 Ω, 3.3 Ω	100 μF, 100 μF	190 μH ,180 μH	130 μH	100 kHz	5 V	1/3, 1/3

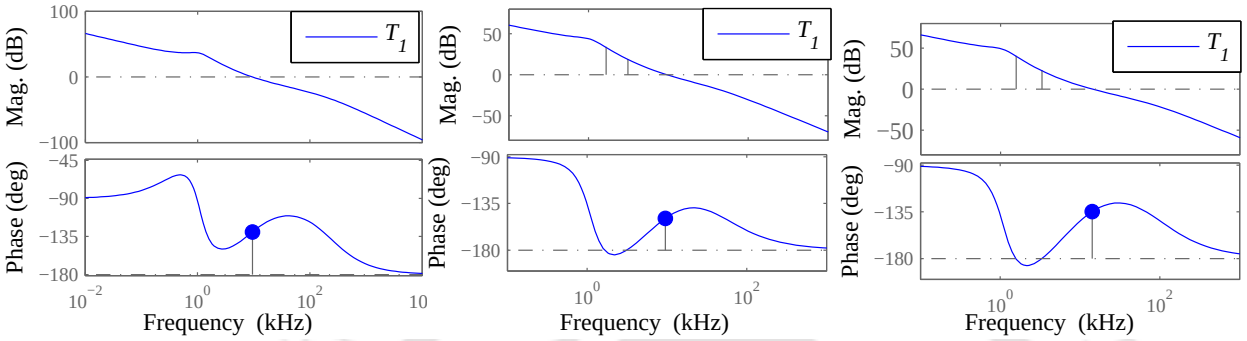


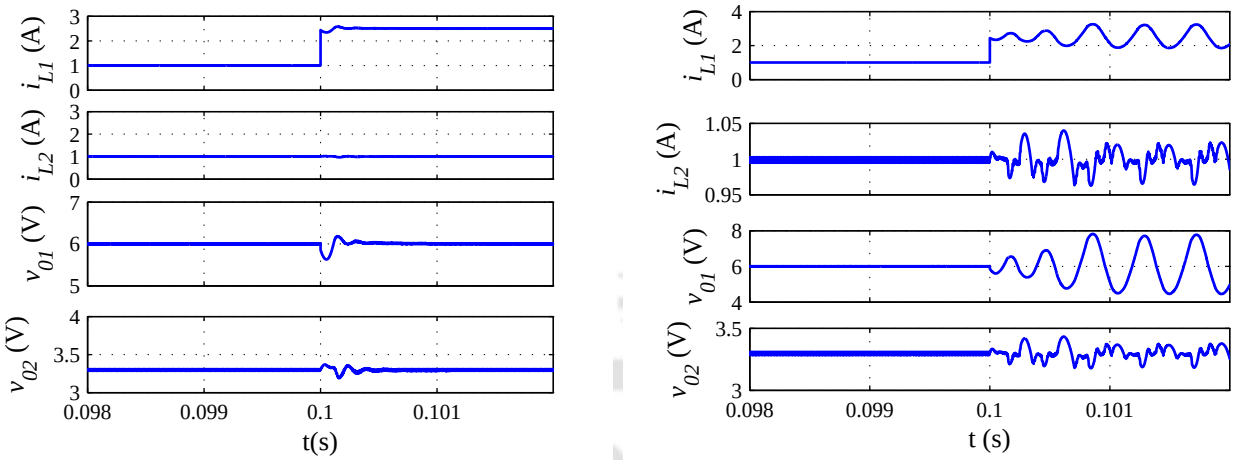
Figure 4.3: Bode plot of loop gain T_1 for three cases (a) Case A: $f_{cj} = 10$ kHz, $\omega_{cj-z} < \omega_{o,j}$ (stable) (b) Case B: $f_{cj} = 10$ kHz, $\omega_{cj-z} > \omega_{o,j}$ (unstable) (c) Case C: $f_{cj} = 15$ kHz (unstable)

Thus, to ensure stability of the closed loop system the maximum limit of choosing the crossover frequency is determined by (4.30). Considering $\phi_m = 55°$ and using the value of circuit parameter given in Table 4.1 in above equation, we obtain

$$f_{cj} \leq 10.37 \text{ kHz} \tag{4.31}$$

Once the crossover frequency is determined next target is to determine the location of compensator zero and pole to ensure the stable closed loop system. Figure 4.2(b) shows the asymptotic bode plot of G_{vdj}, G_{vj}, desired loop T_j. From (4.26) and Figure 4.2(b), T_j therefore, contains a pole at dc frequency, a compensator zero at ω_{cj-z}, complex pole at $\omega_{o,j}$, ESR zero at ω_{esrj}, compensator pole at ω_{cj-p}. The compensator zero ω_{cj-z} should be placed $< \omega_{o,j}$ to compensate the phase-delay effect of complex pole. Otherwise, the phase margin of T_j either becomes low or negative, based on the Q factor of the complex pole. The compensator pole ω_{cj-p} should be placed higher than ω_{cj} so that its lagging phase does not decrease the T_j phase margin. Therefore, it is concluded that $f_{cj} < 10.37$ kHz, ω_{cj-z} must be lower than $\omega_{o,j}$ and ω_{cj-p} must be higher than ω_{cj} to be stable.

Bode plot of T_1 can be used to predict the stability phase margin of T_1. The bode plot of



(a) (b)

Figure 4.4: Simulation results for step change in load current i_{01} from 1 A to 2.4 A (a) Case A: stable (b) Case B: unstable

T_1 as shown in Figure 4.3 is obtained using circuit parameter shown in Table 4.1 and designing controller for three cases. Case A is for $f_{c1} = 10$ kHz and $\omega_{cj-z} < \omega_{o,j}$, Case B is for $f_{c1} = 10$ kHz and $\omega_{cj-z} > \omega_{o,j}$, Case C is for $f_{c1} = 15$ kHz. Case B, Case C are, as predicted, unstable, which can be seen in Figure 4.3(b), Figure 4.3(c) that the phase plot is crossing $-180°$ and Case A is stable with good phase margin. Figure 4.4 shows the simulation results for both Case A and Case B. It is observed that when load current i_{01} is step changed from 1 A to 2.4 A the system remains stable for case A as shown in Figure 4.4(a) and becomes unstable for Case B as shown in Figure 4.4(b).

4.5 Proposed Compensator Design Procedure

The procedure to design compensator for voltage mode control of CI-SIDO buck converter is as follows

4.5.1 Design Considerations

Based on the analysis, the following needs to be considered while designing the controller G_{vj}:

4.5.1.1 Decoupling of Output Voltages

To decouple the output voltages, G_{vj} needs to be designed satisfying (4.9). In other words, the cross-coupling $A_{21}^{'} \approx 0$, if from (4.6)

$$\frac{|G_{vd21}|}{|G_{vd11}G_{m1}\beta_1| * |G_{v1}|} \approx 0 \tag{4.32}$$

Equation (4.32) is satisfied only if $|G_{v1}| \to \infty$. Practically $|G_{v1}|$ can not be made ∞. Therefore, considering $\frac{|G_{vd21}|}{|G_{vd11}G_{v1}G_{m1}\beta_1|} = \gamma$, where $\gamma \approx 0$, $|G_{v1}|$ is given by

$$|G_{v1}| = \frac{|G_{vd21}|}{|G_{vd11}G_{m1}\beta_1| * \gamma} \tag{4.33}$$

The loop gains T_1 at gain crossover frequency ω_{c1} is

$$|G_{vd1}G_{v1}G_{m1}\beta_1| = 1 \tag{4.34}$$

Using (4.33) in (4.34) and substituting circuit parameters, ω_{c1} for G_{v1} is found as

$$\omega_{c1} = \frac{V_{in}Mr_2^{'}}{\gamma L_1 L_2} \Rightarrow f_{c1} = \frac{1}{2\pi}\frac{V_{in}Mr_2^{'}}{\gamma L_1 L_2} \tag{4.35}$$

Similarly, f_{c1} for G_{v2} is found as $f_{c1} = \frac{1}{2\pi}\frac{V_{in}Mr_1^{'}}{\gamma L_1 L_2}$.

As γ and f_{cj} are inversely proportional, higher the f_{cj}, lower the cross-coupling and faster the transient response.

4.5.1.2 Achieving Good Bandwidth and Stability Margin

The choice of gain crossover frequency and the placement of poles and zeros of the compensator decides the bandwidth and stability margin. According to the analysis presented in Section 4.4, $f_{cj} = 10$ kHz, $\omega_{cj-z} < \omega_{o,j}$ and $\omega_{cj-p} > \omega_{cj}$.

4.5.2 Type-II Compensator Design Procedure

The objective of designing compensator is to obtain higher f_{cj}, consistent with stability boundary. Also, the desire loop gain at f_{cj} should be -20 dB with phase margin (PM) greater than 45°. Figure 4.2 shows the Type-II compensator and the bode plot. The design procedure

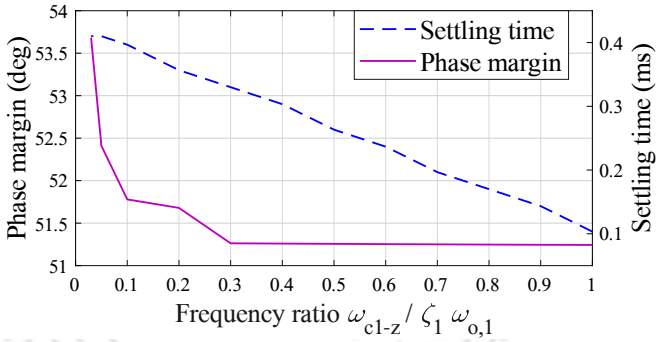


Figure 4.5: Variation of phase margin and settling time with $\frac{\omega_{c1-z}}{\zeta_1 \omega_{o,1}}$

is as follows:

- Step 1: Choose the gain crossover frequency ω_{cj}: To reduce cross-coupling, f_{cj} should be high being consistent with stability boundary. Thus, f_{cj} is chosen as given by (4.31).

- Step 2: Calculate the compensator gain: From (4.27), compensator gain is calculated as

$$|G_{vj}|_{f_{gc}} = \frac{1}{|G_{vdj}|_{f_{cj}} * |G_{mj}| * \beta_j} \tag{4.36}$$

- Step 3: Set the compensator zero w_{cj-z}: The placement of ω_{cj-z} affects the stability of the system. To ensure good stability margin, $\omega_{cj-z} < \omega_{o,j}$. Figure 4.5 shows the plot of phase margin and settling time as placement of ω_{c1-z} is varied for the compensator. It can be seen that if ω_{c1-z} is placed close to the $\omega_{o,j}$ phase margin and settling time decreases. The phase margin is found to be $> 50°$ in range of $0.1\omega_{o,1}$ to $0.3\omega_{o,1}$. Similar concept applies for ω_{c2-z}. Thus, ω_{cj-z} is chosen as

$$\omega_{cj-z} = 0.2 * \zeta_j \omega_{o,j} \tag{4.37}$$

- Step 4: Set the compensator pole ω_{cj-p}: For Type-II compensator $\omega_{cj} = \sqrt{\omega_{cj-z}\omega_{cj-p}}$, and

$$\omega_{cj-p} = \frac{\omega_{cj}^2}{\omega_{cj-z}} \tag{4.38}$$

- Step 5: Calculate the circuit parameters of G_{vj}: Using (4.36)-(4.38), the parameters of compensator (r_1, r_2, c_1, c_2) can be calculated.

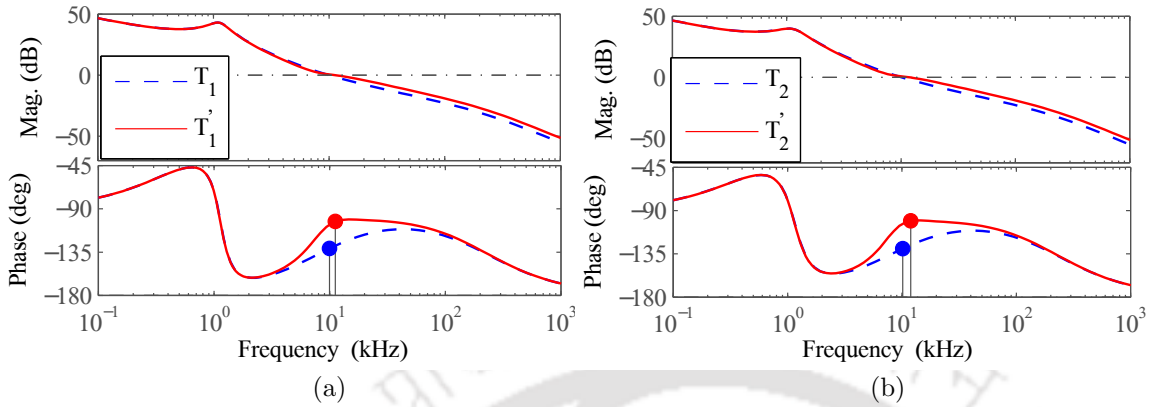


Figure 4.6: Bode plot of loop gain transfer function (a) $T_1^{'}$ (b) $T_2^{'}$

4.5.3 Example of Compensator Design

Based on the proposed design procedure, Type-II compensators G_{v1}, G_{v2} are designed. The design parameters of the converter are listed in Table 4.1. From (4.31), f_{cj} is chosen as 10 kHz. Using converter circuit parameters, $|G_{vd1}|_{f_{c1}} = 0.211$, $|G_{vd2}|_{f_{c2}} = 0.215$, $\omega_{o,1} = 7136$ rad/sec, $\omega_{o,2} = 7237$ rad/sec, $|G_{m1}| = |G_{m2}| = 0.2$, $\beta_1 = \beta_2 = 0.33$. Using (4.36)-(4.38), $\omega_{c1-z} = 1427$ rad/sec, $\omega_{c1-p} = 2.76 * 10^6$ rad/sec and $k_{c1} = 102 * 10^3$. The transfer function of G_{v1} is given by

$$G_{v1}(s) = 101 * 10^3 \frac{(1 + 7 * 10^{-4}s)}{s(1 + 0.36 * 10^{-6}s)} \tag{4.39}$$

Similarly, using (4.36)-(4.38), $\omega_{c2-z} = 1447$ rad/sec, $\omega_{c2-p} = 2.72 * 10^6$ rad/sec and $k_{c2} = 102 * 10^3$. The transfer function of G_{v2} is given by

$$G_{v2}(s) = 102 * 10^3 \frac{(1 + 6.9 * 10^{-4}s)}{s(1 + 0.367 * 10^{-6}s)} \tag{4.40}$$

Figure 4.6 shows the bode plots of the actual loop transfer functions $T_1^{'}$, $T_2^{'}$ and approximated loop transfer functions T_1, T_2. It shows that both magnitude plots are nearly equal, but deviations occur in phase plots around f_{c1}, f_{c2} in $T_1^{'}$, $T_2^{'}$ due to the influence of both controllers. The phase margin of $T_1^{'}$, $T_2^{'}$ are 76°, 79° at 11 kHz, 12 kHz respectively, which are good enough for regulating the output voltages.

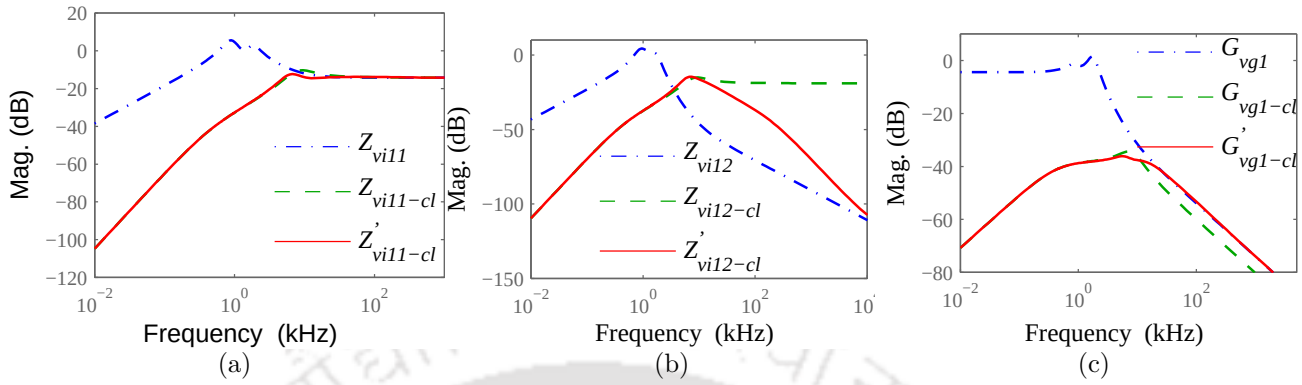


Figure 4.7: Bode plots of open, closed-loop self-regulation, cross-regulation and audio susceptibility (a) Z_{vi11}, $Z_{vi11-cl}$, $Z'_{vi11-cl}$ (b) Z_{vi12}, $Z_{vi12-cl}$, $Z'_{vi12-cl}$ (c) G_{vg1}, G_{vg1-cl}, G'_{vg1-cl}

4.6 Simulation Results and Analysis

To validate the effectiveness of the proposed control method, CI-SIDO buck converter is simulated in MATLAB SIMULINK environment.

4.6.1 Frequency Domain Results

To verify the effectiveness of the proposed controller, the closed-loop performance is studied in the frequency domain and is compared with the open loop performance. Figure 4.7 show the bode plots of self-regulation, cross-regulation, and audio susceptibility, respectively, for open loop (Z_{vi11}, Z_{vi12}, G_{vg1}), closed-loop actual ($Z'_{vi11-cl}$, $Z'_{vi12-cl}$, G'_{vg1-cl}), and approximated ($Z_{vi11-cl}$, $Z_{vi12-cl}$, G_{vg1-cl}) transfer functions. These figures show that the actual and approximated closed-loop transfer functions are same in frequency range up to f_{cj}, i.e., 10 kHz. In the high-frequency range, the actual closed-loop transfer functions deviate from approximated transfer functions and become same as that of the open loop. From Figure 4.7, it is observed that due to the proposed controller, the magnitudes of closed-loop self-regulation $Z'_{vi11-cl}$, cross-regulation $Z'_{vi12-cl}$, and audio-susceptibility G'_{vg1-cl} are reduced significantly by 18 dB, 19 dB, and 38 dB respectively as compared to open loop. Thus, with the proposed controller, the closed-loop performance is improved.

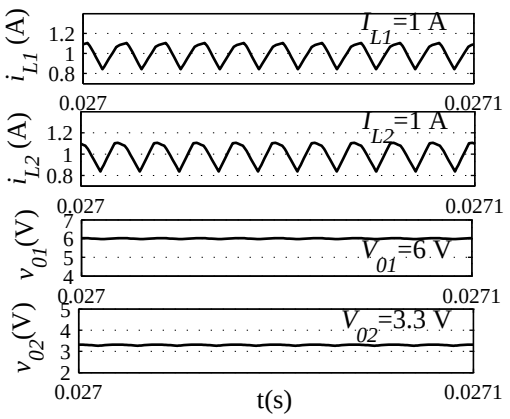


Figure 4.8: Simulation results of steady state i_{L1}, i_{L2}, v_{01}, v_{02}

4.6.2 Time Domain Results

4.6.2.1 Steady-state

Figure 4.8 shows the simulated waveform of inductor currents and output voltages at steady state condition. It is observed that the output voltages V_{01}/V_{02} are able to regulate to their respective reference voltages, i.e., $V_{01} = 6$ V, $V_{02} = 3.3$ V with voltage ripple $\Delta v_{01} = 50mV$, $\Delta v_{02} = 55mV$ which is less than 3%.

4.6.2.2 Dynamic Performance

Load Regulation: Figure 4.9 shows the simulation results of output voltages for step change is load current. Figure 4.9(a) shows the simulation results for step change in i_{01} from 0.4 A to 2.5 A keeping i_{02} constant at 1 A. It is observed that due the step change in i_{01}, the output voltages v_{01} and v_{02} experience negligible transient response which settles very quickly. As in Figure 4.9(a), the output voltage v_{01} under goes undershoot (self-regulation) of 0.7 V and v_{02} under goes overshoot (cross-regulation) of 0.08 V with settling time of 0.2 ms. Similarly, Figure 4.9(b) shows the simulation results for step change in i_{02} from 0.4 A to 2.5 A keeping i_{01} constant at 1 A. It is observed that the v_{01} under goes overshoot (cross-regulation) of 0.15 V and v_{02} under goes undershoot (self-regulation) of 0.33 V with settling time of 0.2 ms.

Cross-coupling: Figure 4.10 shows the simulation results of output voltages for step change is reference voltage. It shows that the designed compensator regulates v_{01} and v_{02} with reduced

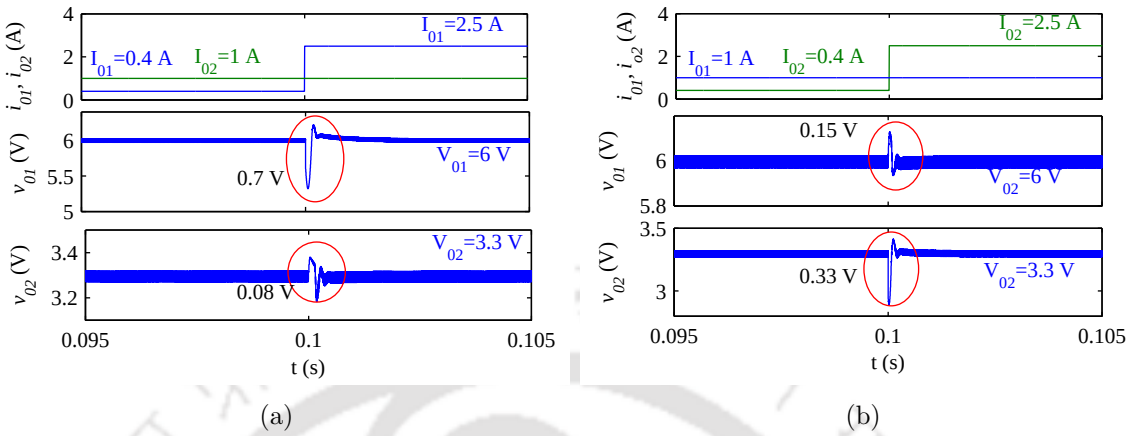


Figure 4.9: Simulated results for load regulation (a) Step change in i_{01} (b) Step change in i_{02}

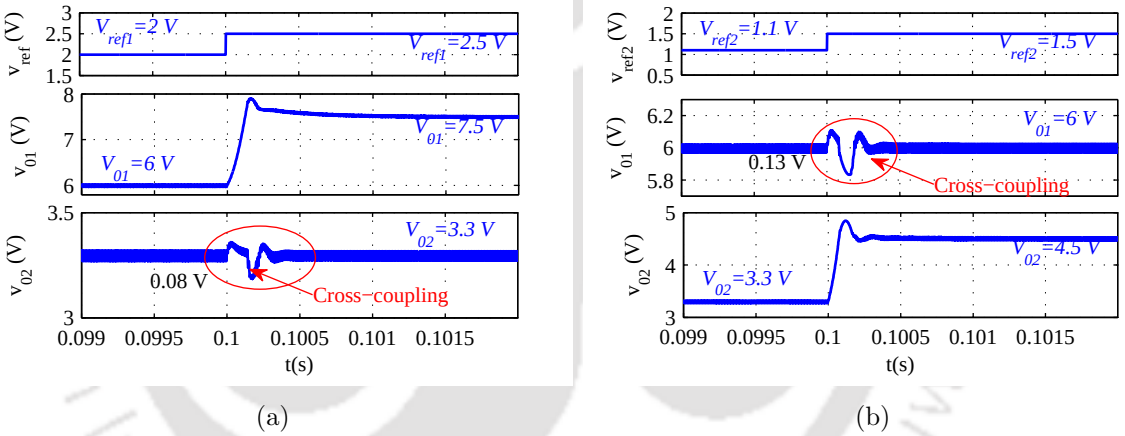


Figure 4.10: Simulated results for cross-coupling (a) Step change in v_{ref1} (b) Step change in v_{ref2}

cross-coupling. For step change in v_{ref1}=2 V to 2.5 V, v_{01} change from 6 V to 7.5 V and v_{02} experience negligible cross-coupling of 0.08 V as shown in Figure 4.10(a). Similarly, for step change in v_{ref2} from 1.1 V to 1.5 V, v_{02} change from 3.3 V to 4.5 V and v_{01} experience negligible cross-coupling of 0.13 V as shown in Figure 4.10(b).

Audio-susceptibility: Figure 4.11 shows the simulation results of output voltage for step change is input voltage v_{in}. Initially, the converter is in steady state. At t= 0.07 s, the input voltage v_{in} is step change from 10 V to 14 V. It is observed that the output voltages v_{01} and v_{02} experience negligible audio-susceptibility effect and settles to steady state very quickly. The overshoot in v_{01}, v_{02} are found to be equal to 60 mV, 50 mV, respectively.

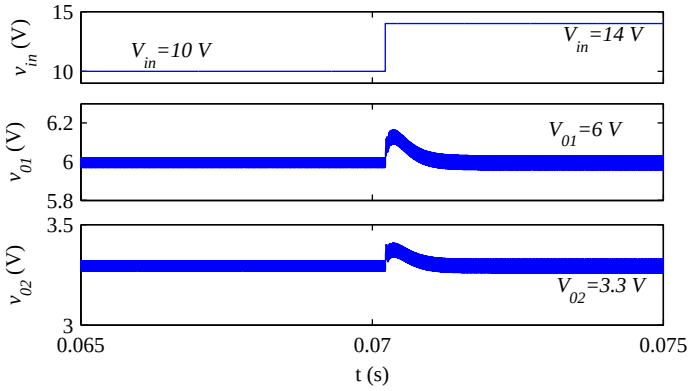


Figure 4.11: Simulation results for audio-susceptibility (Step change in v_{in})

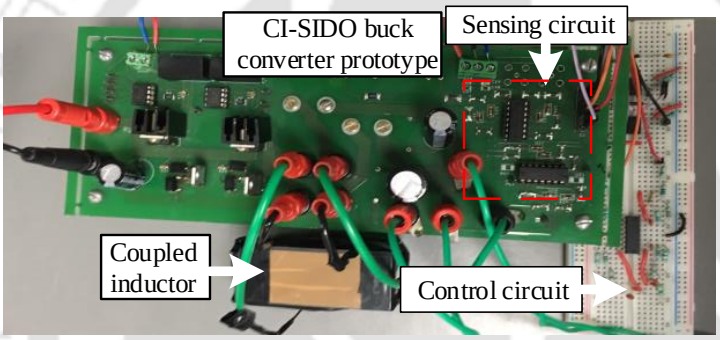
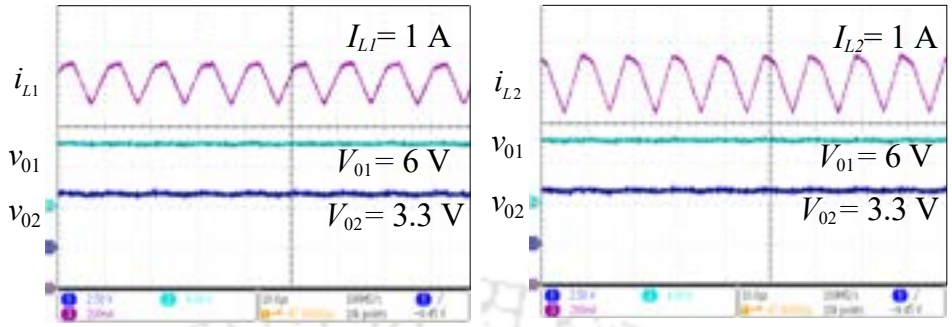


Figure 4.12: Experimental set-up of proposed decoupled voltage mode control of CI-SIDO buck converter

4.7 Experimental Results

The proposed decoupled voltage-mode control method is verified by developing a 24 W experimental prototype of CI-SIDO buck converter. The parameter of the converter for experimental test is same as listed in Table 4.1. Figure 4.12 shows the experimental setup of the closed loop CI-SIDO buck converter. The experimental prototype is divided into two part i.e power circuit and control circuit. The power circuit consist of two power MOSFETs (IRF540), two Schottky diodes (STPS20SM60), one coupled inductor, two electrolytic capacitors and two load resistances. For driving the two power MOSFETs, two gate drivers (HCPL-3120) are used. The gate pulses to the drivers are provided by the control circuit. The control circuit consists of the two voltage sensors, two Type-II compensators, and two voltage comparators (LM311). Two Type-II compensators are implemented using op-amp LF347N and passive components.



(a) (b)

Figure 4.13: Experimental results of steady-state waveform (a) i_{L1}, v_{01}, v_{02} (b) i_{L2}, v_{01}, v_{02}

Based on the laboratory setup, experimental results are presented to verify the proposed method.

4.7.1 Steady-state Performance

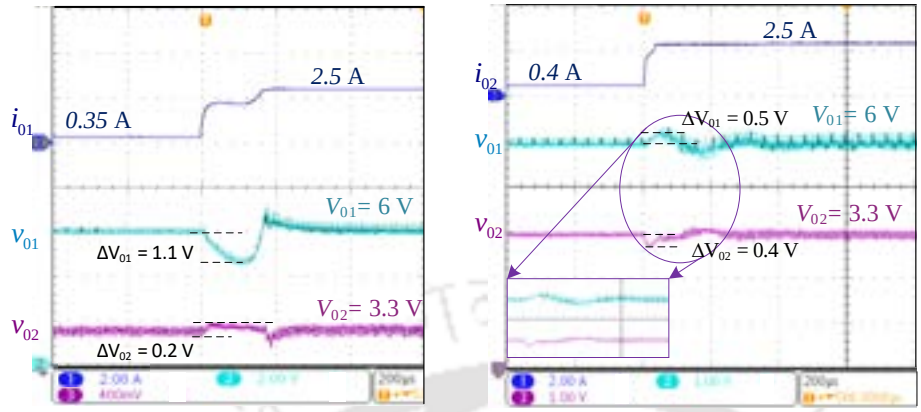
Figure 4.13 shows the experimental waveforms of the inductor currents and output voltages at steady state. It is observed that v_{01}, v_{02} are able to track their respective reference voltages, i.e., $V_{01} = 6$ V, $V_{02} = 3.3$ V with voltage ripples $\Delta v_{01} = 50mV$ and $\Delta v_{02} = 55mV$, which are less than 2%.

4.7.2 Dynamic Performance

4.7.2.1 Self and Cross-regulations

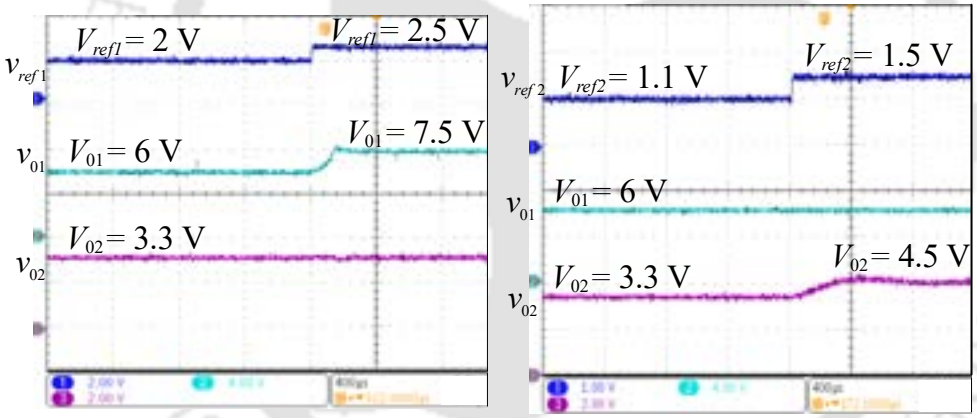
The transient response of output voltages due to load regulation is shown in Figure 4.14. In Figure 4.14(a), when i_{01} is step changed from 0.35 A to 2.5 A and $i_{02} = 1$ A, v_{01} and v_{02} experience transients which settle very quickly. The self regulation of v_{01} is about 1.1 V, cross regulation of v_{02} is 200 mV and the transient response time is 220 μs. Similarly, when i_{02} is step changed from 0.4 A to 2.5 A and $i_{01} = 1$ A, the self regulation of v_{02} is about 400 mV, cross regulation of output v_{02} is 500 mV and the transient response time is 220 μs, as shown in Figure 4.14(b).

Figure 4.14 indicate that the proposed control method is able to suppress the load regulation i.e., self-regulation and cross-regulation.



(a) (b)

Figure 4.14: Experimental results for self and cross-regulations. Step change in load current (a) i_{01} (b) i_{02}



(a) (b)

Figure 4.15: Experimental results for cross-couplings. Step change in reference voltage (a) v_{ref1} (b) v_{ref2}

4.7.2.2 Cross-Couplings

To verify the effectiveness of the designed compensator in decoupling the output voltage, a test with step change in reference voltage is done and the experimental results are shown in Figure 4.15. In Figure 4.15(a), v_{ref1} is changed from 2 V to 2.5 V, accordingly v_{01} changes from 6 V to 7.5 V and v_{02} experiences negligible cross-coupling effect. Similarly, in Figure 4.15(b), v_{ref2} is changed from 1.1 V to 1.5 V, accordingly v_{02} changes from 3.3 V to 4.5 V and v_{01} experiences negligible cross-coupling effect.

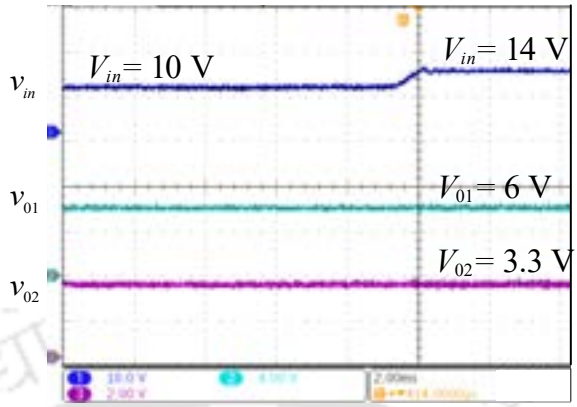


Figure 4.16: Experimental results for audio-susceptibility. Step change in v_{in}

From Figure 4.15, it is observed that the designed compensator is able to regulate v_{01} and v_{02} with negligible cross-coupling. Therefore, the proposed control method is successful in suppressing the cross-coupling effect and approximately decoupling the two output voltages.

4.7.2.3 Audio-susceptibility

Figure 4.16 shows the experimental results for step change in input voltage. The figure shows that for a step change in v_{in} from 10 V to 14 V, the output voltages stay regulated at their reference voltages with negligible audio susceptibility and settle to steady state very quickly. Therefore, audio-susceptibility is satisfactory.

4.7.3 Performance Comparison

The performance of CI-SIDO converter is compared using the several performance indices which includes self-regulation index (SRI), cross-regulation index (CRI), cross-coupling index (CCI) and audio-susceptibility index (ASI). The several indices are defined as follows:

$$\begin{aligned}
\mathrm{SRI}_1 &= \frac{\Delta V_{01}/V_{01}}{\Delta I_{01}/I_{01}}\ ,\ \mathrm{SRI}_2 = \frac{\Delta V_{02}/V_{02}}{\Delta I_{02}/I_{02}} \\
\mathrm{CRI}_1 &= \frac{\Delta V_{01}/V_{01}}{\Delta I_{02}/I_{02}}\ ,\ \mathrm{CRI}_2 = \frac{\Delta V_{02}/V_{02}}{\Delta I_{01}/I_{01}} \\
\mathrm{ASI}_1 &= \frac{\Delta V_{01}/V_{01}}{\Delta V_{in}/V_{in}}\ ,\ \mathrm{ASI}_2 = \frac{\Delta V_{02}/V_{02}}{\Delta V_{in}/V_{in}} \\
\mathrm{CCI}_1 &= \frac{\Delta V_{01}/V_{01}}{\Delta V_{ref2}/V_{ref2}}\ ,\ \mathrm{CCI}_2 = \frac{\Delta V_{02}/V_{02}}{\Delta V_{ref1}/V_{ref1}}
\end{aligned} \tag{4.41}$$

Table 4.2: Comparison with existing SIDO converter implementation

References	[34]	[35]	This Chapter
Topology	SI-SIDO buck	SI-SIDO buck	CI-SIDO buck
Control method	Cross-derivative state feedback control	Multi-variable control	Decoupled voltage mode control
Process	Discrete component	FPGA	Discrete component
Input voltage	4.8 V	5 V	10 V
Output voltage	3.3 V, 1.2 V	1 V, 1.5 V	6 V, 3.3 V
Load current	0.1 A, 0.1 A	0.5 A, 0.5 A	2.5 A, 2.5 A
Output power	0.45 W	1.25 W	24 W
f_s	100 kHz	500 kHz	100 kHz
Transient response	*	*	220 μs
SRI_1 SRI_2	0.033 0.03	0.025 0.033	0.03 0.023
CRI_1 CRI_2	0.015 0.013	0.02 0.01	0.016 0.01
CCI_1 CCI_2	* *	* *	0.059 0.096
ASI_1 ASI_2	* *	* *	0.025 0.037

* value not reported in the literature

where, ΔV_{01}, ΔV_{02} are the variation in v_{01}, v_{02}, ΔI_{01}, ΔI_{02} are the variation in i_{01}, i_{02}, ΔV_{ref1}, ΔV_{ref2} are the variation in v_{ref1}, v_{ref2}, ΔV_{in} is the variation in v_{in}. V_{01}, V_{02}, V_{ref1}, V_{ref2}, V_{in}, I_{01}, I_{02} are the rated output voltages, reference voltages, input voltage and load currents.

As per the Figure 4.14-4.16, the performance indices of decoupled voltage mode controlled CI-SIDO buck converter are calculated as

$$\begin{aligned}
\mathrm{SRI}_1 &= \frac{1.1/6}{2.15/0.35} = 0.03, \quad \mathrm{SRI}_2 = \frac{0.4/3.3}{2.1/0.4} = 0.023 \quad \text{(Experimental)} \\
\mathrm{CRI}_1 &= \frac{0.5/6}{2.1/0.4} = 0.016, \quad \mathrm{CRI}_2 = \frac{0.2/3.3}{2.15/0.35} = 0.01 \quad \text{(Experimental)} \\
\mathrm{CCI}_1 &= \frac{0.13/6}{0.4/1.1} = 0.059, \quad \mathrm{CCI}_2 = \frac{0.08/3.3}{0.5/2} = 0.096 \quad \text{(Simulation)} \\
\mathrm{ASI}_1 &= \frac{0.06/6}{4/10} = 0.025, \quad \mathrm{CCI}_2 = \frac{0.05/3.3}{4/10} = 0.037 \quad \text{(Simulation)}
\end{aligned} \tag{4.42}$$

Table 4.2 shows the performance comparison of CI-SIDO buck converter with the existing works [34], [35] available in the literature for SI-SIDO buck converter. It is observed from Table 4.2 that SRI achieved by the proposed method is almost same as that in [34], [35]. CRI is improved as compared to that in [35]. Moreover, the ASI and CCI of the proposed decoupled control for CI-SIDO buck converter are 0.037 and 0.096 respectively. In this work we have used simple and inexpensive analog controller (Type-II compensator) for CI-SIDO buck converter. Still it shows similar dynamic performance as [35] which uses expensive FPGA based digital controller. Therefore, the proposed decoupled control is able to regulate the output voltages independently with good dynamic performance.

4.8 Conclusion

In this chapter, a decoupling method for CI-SIDO buck converter under voltage mode control is proposed. Cross-coupling and cross-regulation are the problems found in CI-SIDO converters due to the presence of the coupled inductor. The detailed analysis performed shows that the two outputs can be decoupled by designing the compensator with high gain or high crossover frequency.

The effect of decoupling is investigated on the transfer functions of load-regulations and audio-susceptibility. It shows that the 4^{th} order transfer functions of audio-susceptibility and self-regulation of CI-SIDO buck get reduced to that of the 2^{nd} order transfer functions of a simple buck converter. The cross-regulation transfer function also gets simplified. All the three self and cross-regulations, and audio-susceptibility can be reduced by designing the compensator with high gain. However, with high gain or crossover frequency the system stability is affected. Thus, stability boundary of crossover frequency is derived. Good stability margin for the closed-loop system requires the compensator zero and pole to be placed less than complex pole frequency and greater than crossover frequency, respectively.

Based on these conditions, the design procedure for the decoupled voltage mode control is developed using simple analog Type-II compensator. Steady-state operation and dynamic performance of the CI-SIDO buck converter are studied. The simulation and experimental

results using hardware prototype show that the proposed method satisfactorily regulates and approximately decouples the output voltages, and reduces self and cross-regulations, and audio-susceptibility.

Note: Major part of this chapter is reproduced from my publications:

1. G. Nayak, S. Nath, Decoupled Voltage Mode Control of Coupled Inductor Single input dual Output Buck Converter, in IEEE Transactions on Industry Applications, vol. 56, no. 4, pp. 4040-4050, July-Aug. 2020, doi: 10.1109/TIA.2020.2991650.

2. G. Nayak and S. Nath, "Voltage Mode Control of Magnetically Coupled SIDO Buck Converter," 2018 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Chennai, India, 2018, pp. 1-6, doi: 10.1109/PEDES.2018.8707607.

5

Decoupled Average Current Control of CI-SIDO Buck Converter

Contents

5.1 Introduction

Chapter 4 has introduced a decoupled voltage-mode control for CI-SIDO buck converter to regulate the output voltages, reduce cross-regulation, and cross-coupling with good dynamic performance. However, voltage mode control exhibits slow response and limited bandwidth which results in poor dynamic performance. The slow response is because the change in load current or input voltage is first sensed as output change and then corrected by a feedback loop. The limited bandwidth is due to the presence of double pole in the duty cycle-to-output transfer functions. Therefore, a practical solution to reduce the cross-coupling and cross-regulation problem in CI-SIDO converters is to improve the converter's transient response. The transient response is improved with the use of current control technique.

Current control is a control scheme that uses both the output voltage and inductor current for closed-loop control. The most popular current controls are average current control (ACC) and peak current mode (PCM) control. In current control, the output is indirectly controlled by directly controlling the inductor current and thus improves the transient response. The other advantages of current control are over-load protection, noise immunity, and current limiting. However, the analysis and design of current control for CI-SIDO converter is challenging due to cross-coupling problem.

This chapter aims to provide a detailed design insight into average current control when applied to CI-SIDO buck converter. This chapter proposes a controller design procedure based on decoupling and stability criteria found during analysis for CI-SIDO buck converter.

5.2 Circuit Operation of CI-SIDO Buck Converter with Average Current Control

Figure 5.1(a) illustrates the architecture of a CI-SIDO buck converter with average current control (ACC). There are two control loops for each output voltage: inner current loop and outer voltage loop. The inner current loops is formed using two sensing resistances (r_{s1}, r_{s2}), two current controllers G_{c1}, G_{c2}, and two PWM gains G_{m1}, G_{m2}. The outer voltage loops are

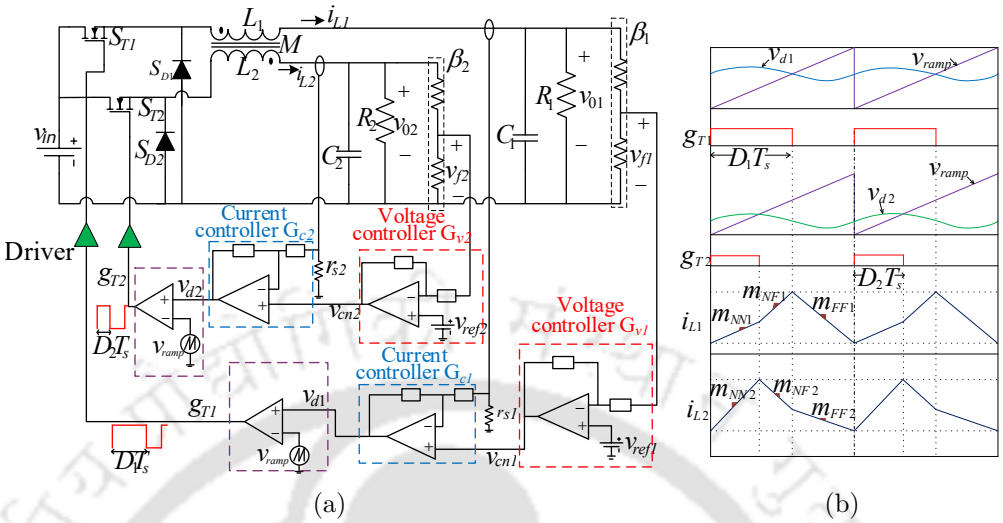


Figure 5.1: Circuit diagram and desired waveform of CI-SIDO buck with ACC

formed using two feedback gains β_1, β_2 and two voltage controllers G_{v1}, G_{v2}.

The outer voltage loops regulate the output voltages v_{01}, v_{02} by generating the reference inductor currents for inner current loops. The inner current loops tune the inductor currents to its reference currents by adjusting the duty ratios of the switches.

The control waveform is shown in Figure 5.1(b). Here, it is considered $V_{01} > V_{02}$, so $D_1 > D_2$. The duty ratios of the switches are generated by comparing the output signal of current controller v_{d1}, v_{d2} with the ramp signal v_{ramp}.

5.3 Proposed Decoupled Average Current Control of CI-SIDO Buck Converter

The small-signal model of CI-SIDO buck converter is developed in Chapter 2. Using the small-signal model of CI-SIDO buck, the block diagram model of closed-loop average current controlled CI-SIDO buck converter is shown in Figure 5.2.

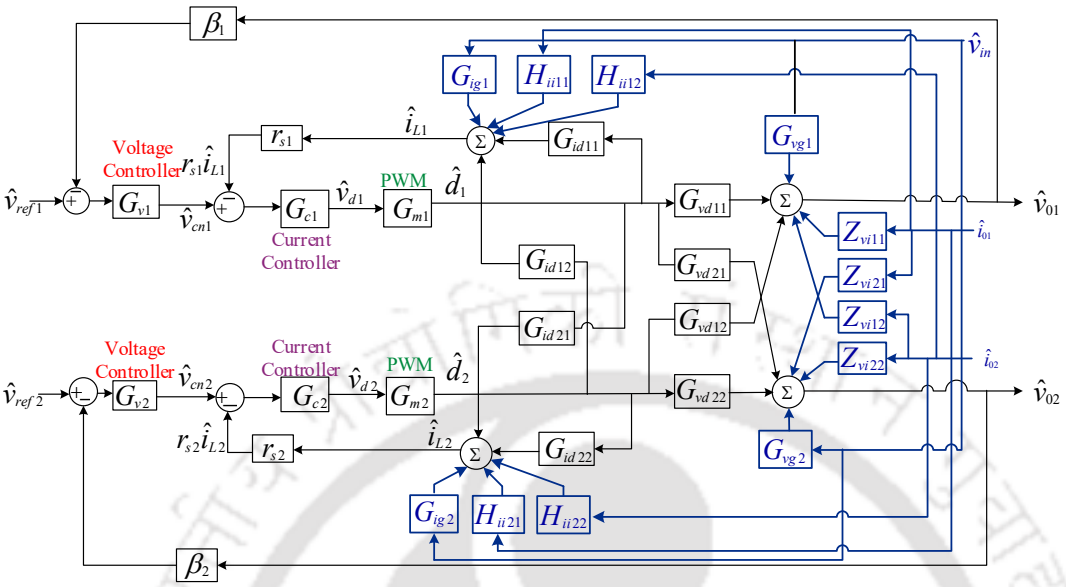


Figure 5.2: Block diagram representation for ACC of CI-SIDO buck converter

5.3.1 Analysis of Inner Current Loops

From Figure 5.2, the inductor currents can be written in matrix form as

$$\begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \end{bmatrix} = \begin{bmatrix} G_{id11} & G_{id12} \\ G_{id21} & G_{id22} \end{bmatrix} \begin{bmatrix} \hat{d}_1 \\ \hat{d}_2 \end{bmatrix} + \begin{bmatrix} G_{ig1} \\ G_{ig2} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \end{bmatrix} + \begin{bmatrix} H_{ii11} & H_{ii12} \\ H_{ii21} & H_{ii22} \end{bmatrix} \begin{bmatrix} \hat{i}_{01} \\ \hat{i}_{02} \end{bmatrix} \tag{5.1}$$

From Figure 5.2, the duty cycles generated from inner current control can be written as:

$$\begin{bmatrix} \hat{d}_1 \\ \hat{d}_2 \end{bmatrix} = \begin{bmatrix} G_{c1}G_{m1} & 0 \\ 0 & G_{c2}G_{m2} \end{bmatrix} \begin{bmatrix} \hat{v}_{cn1} \\ \hat{v}_{cn2} \end{bmatrix} - \begin{bmatrix} r_{s1}G_{c1}G_{m1} & 0 \\ 0 & r_{s2}G_{c2}G_{m2} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \end{bmatrix} \tag{5.2}$$

The inner closed-loop reference control voltage to inductor currents can be obtained using (5.2) in (5.1), making disturbance input zero, i.e., $\hat{v}_{in} = \hat{i}_{01} = \hat{i}_{02} = 0$ and is written as

$$\begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \end{bmatrix} = \begin{bmatrix} \frac{A'_{11}}{1+T'_{i1}} & \frac{A'_{12}}{1+T'_{i1}} \\ \frac{A'_{21}}{1+T'_{i2}} & \frac{A'_{22}}{1+T'_{i2}} \end{bmatrix} \begin{bmatrix} \hat{v}_{c1} \\ \hat{v}_{c2} \end{bmatrix} \tag{5.3}$$

where,

$$\begin{aligned} A'_{11} &= G_{c1}G_{m1}(G_{id11} - \frac{G_{id21}G_{id12}r_{s2}G_{c2}G_{m2}}{1 + G_{id22}G_{c2}G_{m2}r_{s2}}) \\ A'_{22} &= G_{c2}G_{m2}(G_{id22} - \frac{G_{id21}G_{id12}r_{s1}G_{c1}G_{m1}}{1 + G_{id11}G_{c1}G_{m1}r_{s1}}) \end{aligned} \tag{5.4}$$

$$A_{12}^{'} = G_{c2}G_{m2}(G_{id12} - \frac{G_{id12}G_{id22}r_{s2}G_{c2}G_{m2}}{1 + G_{id22}G_{c2}G_{m2}r_{s2}})$$
$$A_{21}^{'} = G_{c1}G_{m1}(G_{id21} - \frac{G_{id21}G_{id11}r_{s1}G_{c1}G_{m1}}{1 + G_{id11}G_{c1}G_{m1}r_{s1}}) \quad (5.5)$$

$$T_{i1}^{'} = r_{s1}G_{c1}G_{m1}(G_{id11} - \frac{G_{id21}G_{id12}r_{s2}G_{c2}G_{m2}}{1 + G_{id22}G_{c2}G_{m2}r_{s2}})$$
$$T_{i2}^{'} = r_{s2}G_{c2}G_{m2}(G_{id22} - \frac{G_{id12}G_{id21}r_{s1}G_{c1}G_{m1}}{1 + G_{id11}G_{c1}G_{m1}r_{s1}}) \quad (5.6)$$

$T_{i1}^{'}$ and $T_{i2}^{'}$ are the inner current loop gains.

It is observed from (5.3) that there exist cross-coupling between the two inner current loops. Moreover, it is found from (5.6) that the inner current loop gain transfer functions $T_{i1}^{'}$, $T_{i2}^{'}$ depends on both current controllers G_{c1}, G_{c2}. Thus, the design of G_{c1}, G_{c2} is not independent.

5.3.1.1 Approximate Decoupling of Inner Current Loops

From (5.3), it is found that, if $A_{12}^{'} \approx 0$, $A_{21}^{'} \approx 0$ then the inner current loops are decoupled. From (5.5), it is found that if G_{c1} and G_{c2} are designed such that,

$$|G_{id11}G_{c1}G_{m1}r_{s1}| >> 1 \text{ and } |G_{id22}G_{c2}G_{m2}r_{s2}| >> 1 \quad (5.7)$$

then the inner closed-loop reference control voltage to inductor currents relationship of (5.3) becomes as

$$\begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \end{bmatrix} = \begin{bmatrix} \frac{A_{11}}{1+T_{i1}} & \epsilon \\ \epsilon & \frac{A_{22}}{1+T_{i2}} \end{bmatrix} \begin{bmatrix} \hat{v}_{c1} \\ \hat{v}_{c2} \end{bmatrix} \quad (5.8)$$

where $\epsilon \to 0$ and

$$A_{11} = G_{c1}G_{m1}G_{id1} \approx A_{11}^{'} \; ; \quad A_{22} = G_{c2}G_{m2}G_{id2} \approx A_{22}^{'} \quad (5.9)$$

$$T_{i1} = rs1G_{c1}G_{m1}G_{id1} \approx T_{i1}^{'} \; ; \quad T_{i2} = r_{s2}G_{c2}G_{m2}G_{id2} \approx T_{i2}^{'} \quad (5.10)$$

where, T_{i1}, T_{i2} are the approximated current loop gain transfer functions, G_{id1}, G_{id2} are the approximated duty cycle-to-inductor current transfer functions. The expression of G_{id1}, G_{id2}

are given by

$$G_{id1} = G_{id11} - \frac{G_{id21}G_{id12}}{G_{id22}} = \frac{\frac{V_{in}}{L_1}(s + \frac{r_1''}{C_1})}{s^2 + s(\frac{r_1'}{L_1} + \frac{r_1''}{C_1}) + \frac{R_1 r_1''}{L_1 C_1}}$$
$$G_{id2} = G_{id22} - \frac{G_{id21}G_{id12}}{G_{id11}} = \frac{\frac{V_{in}}{L_2}(s + \frac{r_2''}{C_2})}{s^2 + s(\frac{r_2'}{L_2} + \frac{r_2''}{C_2}) + \frac{R_2 r_2''}{L_2 C_2}} \tag{5.11}$$

From (5.11), it is observed that approximated duty cycle-to-inductor current transfer functions G_{id1}, G_{id2} is same as that of duty cycle-to-inductor current transfer functions of simple buck.

Therefore, if G_{c1} and G_{c2} are designed satisfying (5.7), then the inner closed-loop reference control input to inductor current transfer functions of CI-SIDO buck becomes same as that of simple buck converter, in addition to the two inductor current i_{L1}, i_{L2} getting decoupled.

5.3.1.2 Inner Closed-loop Transfer Functions

The inner closed-loop relation between duty cycles with control input and disturbance input can be obtained using (5.1) in (5.2) and is given by

$$\begin{bmatrix}\hat{d}_1\\ \hat{d}_2\end{bmatrix} = \begin{bmatrix}G_{c1}G_{m1} & 0\\ 0 & G_{c2}G_{m2}\end{bmatrix}\begin{bmatrix}\hat{v}_{cn1}\\ \hat{v}_{cn2}\end{bmatrix} - \begin{bmatrix}G_{c1}G_{m1}r_{s1} & 0\\ 0 & G_{c2}G_{m2}r_{s2}\end{bmatrix}\left(\begin{bmatrix}G_{id11} & G_{id12}\\ G_{id21} & G_{id22}\end{bmatrix}\begin{bmatrix}\hat{d}_1\\ \hat{d}_2\end{bmatrix} + \begin{bmatrix}G_{ig1}\\ G_{ig2}\end{bmatrix}\begin{bmatrix}\hat{v}_{in}\end{bmatrix} + \begin{bmatrix}H_{ii11} & H_{ii12}\\ H_{ii21} & H_{ii22}\end{bmatrix}\begin{bmatrix}\hat{i}_{01}\\ \hat{i}_{02}\end{bmatrix}\right) \tag{5.12}$$

Rearranging (5.12), we get

$$\begin{bmatrix}\hat{d}_1\\ \hat{d}_2\end{bmatrix} = \begin{bmatrix}1 + r_{s1}G_{c1}G_{m1}G_{id11} & r_{s1}G_{c1}G_{m1}G_{id12}\\ r_{s2}G_{c2}G_{m2}G_{id21} & 1 + r_{s2}G_{c2}G_{m2}G_{id22}\end{bmatrix}^{-1}\left(\begin{bmatrix}G_{c1}G_{m1} & 0\\ 0 & G_{c2}G_{m2}\end{bmatrix}\begin{bmatrix}\hat{v}_{cn1}\\ \hat{v}_{cn2}\end{bmatrix} - \begin{bmatrix}r_{s1}G_{c1}G_{m1}G_{ig1}\\ r_{s2}G_{c2}G_{m2}G_{ig2}\end{bmatrix}\begin{bmatrix}\hat{v}_{in}\end{bmatrix} - \begin{bmatrix}r_{s1}G_{c1}G_{m1}H_{ii11} & r_{s1}G_{c1}G_{m1}H_{ii12}\\ r_{s2}G_{c2}G_{m2}H_{ii21} & r_{s2}G_{c2}G_{m2}H_{ii22}\end{bmatrix}\begin{bmatrix}\hat{i}_{01}\\ \hat{i}_{02}\end{bmatrix}\right) \tag{5.13}$$

5.3.2 Effect of Decoupling on Outer Voltage Loops

The reference control voltages v_{cn1}, v_{cn2} to inner loops are given by outer voltage loops and is written as

$$\begin{bmatrix}\hat{v}_{cn1}\\ \hat{v}_{cn2}\end{bmatrix}=\begin{bmatrix}G_{v1} & 0\\ 0 & G_{v2}\end{bmatrix}\begin{bmatrix}v_{ref1}-\beta_1 v_{01}\\ v_{ref2}-\beta_2 v_{02}\end{bmatrix}=\begin{bmatrix}G_{v1} & 0\\ 0 & G_{v2}\end{bmatrix}\begin{bmatrix}v_{ref1}\\ v_{ref2}\end{bmatrix}-\begin{bmatrix}\beta_1 G_{v1} & 0\\ 0 & \beta_2 G_{v2}\end{bmatrix}\begin{bmatrix}v_{01}\\ v_{02}\end{bmatrix} \tag{5.14}$$

Using (5.14) in 5.13, we get

$$\begin{aligned}\begin{bmatrix}\hat{d}_1\\ \hat{d}_2\end{bmatrix}=&\begin{bmatrix}1+r_{s1}G_{c1}G_{m1}G_{id11} & r_{s1}G_{c1}G_{m1}G_{id12}\\ r_{s2}G_{c2}G_{m2}G_{id21} & 1+r_{s2}G_{c2}G_{m2}G_{id22}\end{bmatrix}^{-1}\left(\begin{bmatrix}G_{c1}G_{m1}G_{v1} & 0\\ 0 & G_{c2}G_{m2}G_{v2}\end{bmatrix}\begin{bmatrix}\hat{v}_{ref1}\\ \hat{v}_{ref2}\end{bmatrix}\right.\\ &-\begin{bmatrix}\beta_1 G_{v1}G_{c1}G_{m1} & 0\\ 0 & \beta_2 G_{v2}G_{c2}G_{m2}\end{bmatrix}\begin{bmatrix}v_{01}\\ v_{02}\end{bmatrix}-\begin{bmatrix}r_{s1}G_{c1}G_{m1}G_{ig1}\\ r_{s2}G_{c2}G_{m2}G_{ig2}\end{bmatrix}\begin{bmatrix}\hat{v}_{in}\end{bmatrix}\\ &\left.-\begin{bmatrix}r_{s1}G_{c1}G_{m1}H_{ii11} & r_{s1}G_{c1}G_{m1}H_{ii12}\\ r_{s2}G_{c2}G_{m2}H_{ii21} & r_{s2}G_{c2}G_{m2}H_{ii22}\end{bmatrix}\begin{bmatrix}\hat{i}_{01}\\ \hat{i}_{02}\end{bmatrix}\right)\end{aligned} \tag{5.15}$$

The output voltage is expressed as

$$\begin{bmatrix}\hat{v}_{01}\\ \hat{v}_{02}\end{bmatrix}=\begin{bmatrix}G_{vd11} & G_{vd12}\\ G_{vd21} & G_{vd22}\end{bmatrix}\begin{bmatrix}\hat{d}_1\\ \hat{d}_2\end{bmatrix}+\begin{bmatrix}G_{vg1}\\ G_{vg2}\end{bmatrix}\begin{bmatrix}\hat{v}_{in}\end{bmatrix}+\begin{bmatrix}Z_{vi11} & Z_{vi12}\\ Z_{vi21} & Z_{vi22}\end{bmatrix}\begin{bmatrix}\hat{i}_{01}\\ \hat{i}_{02}\end{bmatrix} \tag{5.16}$$

Using (5.15) in (5.16), and solving we obtain

$$\begin{aligned}\begin{bmatrix}1+\beta_1 G_{v1}G_{c1}G_{m1}X_{11} & \beta_2 G_{v2}G_{c2}G_{m2}X_{12}\\ \beta_1 G_{v1}G_{c1}G_{m1}X_{21} & 1+\beta_2 G_{v2}G_{c2}G_{m2}X_{22}\end{bmatrix}\begin{bmatrix}\hat{v}_{01}\\ \hat{v}_{02}\end{bmatrix}=&\begin{bmatrix}G_{c1}G_{m1}G_{v1}X_{11} & G_{c2}G_{m2}G_{v2}X_{12}\\ G_{c1}G_{m1}G_{v1}X_{21} & G_{c2}G_{m2}G_{v2}X_{22}\end{bmatrix}\begin{bmatrix}\hat{v}_{ref1}\\ \hat{v}_{ref2}\end{bmatrix}\\ &+\begin{bmatrix}G_{vg1}\\ G_{vg2}\end{bmatrix}\begin{bmatrix}\hat{v}_{in}\end{bmatrix}+\begin{bmatrix}Z_{vi11} & Z_{vi12}\\ Z_{vi21} & Z_{vi22}\end{bmatrix}\begin{bmatrix}\hat{i}_{01}\\ \hat{i}_{02}\end{bmatrix}-\begin{bmatrix}X_{11} & X_{12}\\ X_{21} & X_{22}\end{bmatrix}\left(\begin{bmatrix}G_{ig1}r_{s1}G_{c1}G_{m1}\\ G_{ig2}r_{s2}G_{c2}G_{m2}\end{bmatrix}\begin{bmatrix}\hat{v}_{in}\end{bmatrix}\right.\\ &\left.+\begin{bmatrix}H_{ii11}r_{s1}G_{c1}G_{m1} & H_{ii12}r_{s1}G_{c1}G_{m1}\\ H_{ii21}r_{s2}G_{c2}G_{m2} & H_{ii22}r_{s2}G_{c2}G_{m2}\end{bmatrix}\begin{bmatrix}\hat{i}_{01}\\ \hat{i}_{02}\end{bmatrix}\right)\end{aligned} \tag{5.17}$$

$$
\begin{aligned}
X_{11} &= \frac{1}{1+T_{i1}'}(G_{vd11} - \frac{G_{vd12}G_{id21}G_{c2}G_{m2}r_{s2}}{1+G_{id22}G_{c2}G_{m2}r_{s2}}) \\
X_{22} &= \frac{1}{1+T_{i2}'}(G_{vd22} - \frac{G_{vd21}G_{id12}G_{c1}G_{m1}r_{s1}}{1+G_{id11}G_{c1}G_{m1}r_{s1}}) \\
X_{12} &= \frac{1}{1+T_{i2}'}(G_{vd12} - \frac{G_{vd11}G_{id12}G_{c1}G_{m1}r_{s1}}{1+G_{id11}G_{c1}G_{m1}r_{s1}}) \\
X_{21} &= \frac{1}{1+T_{i1}'}(G_{vd21} - \frac{G_{vd22}G_{id21}G_{c2}G_{m2}r_{s2}}{1+G_{id22}G_{c2}G_{m2}r_{s2}})
\end{aligned}
\tag{5.18}
$$

Using the expression of all transfer function in (5.18) and applying (5.7) , we get

$$
X_{11} \approx \frac{G_{vd1}}{1+T_{i1}},\ X_{22} \approx \frac{G_{vd2}}{1+T_{i2}},\ X_{12} \approx 0,\ X_{21} \approx 0 \tag{5.19}
$$

where, G_{vd1}, G_{vd2} are the duty-cycles to output voltage transfer functions of simple buck converter and are given by

$$
G_{vdj} = \frac{\frac{V_{in}r_j'}{L_j}(s+\frac{1}{r_{cj}C_j})}{s^2 + s(\frac{r_j'}{L_j} + \frac{r_j''}{C_j}) + \frac{R_j r_j''}{L_j C_j}} \text{ where, } j = \{1,2\} \tag{5.20}
$$

5.3.2.1 Closed-loop Reference Voltage to Output Voltage Transfer Functions

The closed-loop reference voltage to output voltage transfer functions can be obtained from (5.17) by making $\hat{v}_{in} = \hat{i}_{01} = \hat{i}_{02} = 0$, applying (5.19) and is given by

$$
\begin{bmatrix} 1+\frac{\beta_1 G_{v1}G_{c1}G_{m1}G_{vd1}}{1+T_{i1}} & 0 \\ 0 & 1+\frac{\beta_2 G_{v2}G_{c2}G_{m2}G_{vd2}}{1+T_{i2}} \end{bmatrix} \begin{bmatrix} \hat{v}_{01} \\ \hat{v}_{02} \end{bmatrix} \approx \begin{bmatrix} \frac{G_{v1}G_{c1}G_{m1}G_{vd1}}{1+T_{i1}} & 0 \\ 0 & \frac{G_{v2}G_{c2}G_{m2}G_{vd2}}{1+T_{i2}} \end{bmatrix} \begin{bmatrix} \hat{v}_{ref1} \\ \hat{v}_{ref2} \end{bmatrix} \tag{5.21}
$$

Solving (5.21), we obtain the approximated closed-loop reference voltage to output voltage transfer functions as

$$
\begin{bmatrix} \hat{v}_{o1} \\ \hat{v}_{o2} \end{bmatrix} \approx \begin{bmatrix} \frac{B_{11}}{1+T_1} & 0 \\ 0 & \frac{B_{22}}{1+T_2} \end{bmatrix} \begin{bmatrix} \hat{v}_{ref1} \\ \hat{v}_{ref2} \end{bmatrix} \tag{5.22}
$$

where,

$$
B_{11} = \frac{G_{v1}G_{c1}G_{m1}G_{vd1}}{1+T_{i1}}\ ;\ B_{22} = \frac{G_{v2}G_{c2}G_{m2}G_{vd2}}{1+T_{i2}} \tag{5.23}
$$

$$
T_1 = \beta_1 B_{11}\ ;\ T_2 = \beta_2 B_{22} \tag{5.24}
$$

T_1 and T_2 are the approximated outer loop gains.

Thus, it is observed from (5.22) that once the inner loops are decoupled the output loops get simplified and becomes the same as that of buck converter.

5.3.3 Effect of Decoupling on Closed-loop Transfer Functions

The closed-loop performance of CI-SIDO buck can be evaluated by analyzing the closed-loop audio-susceptibility and load regulations.

5.3.3.1 Closed-loop Audio-susceptibility

The closed-loop audio-susceptibility transfer functions can be obtained from (5.17) by making $\hat{v}_{ref1} = \hat{v}_{ref2} = \hat{i}_{01} = \hat{i}_{02} = 0$, applying (5.19) and is given by

$$\begin{bmatrix} 1+T_1 & 0 \\ 0 & 1+T_2 \end{bmatrix} \begin{bmatrix} \hat{v}_{01} \\ \hat{v}_{02} \end{bmatrix} \approx \left(\begin{bmatrix} G_{vg1} \\ G_{vg2} \end{bmatrix} - \begin{bmatrix} \frac{G_{vd1}}{1+T_{i1}} & 0 \\ 0 & \frac{G_{vd2}}{1+T_{i2}} \end{bmatrix} \begin{bmatrix} G_{ig1} r_{s1} G_{c1} G_{m1} \\ G_{ig2} r_{s2} G_{c2} G_{m2} \end{bmatrix} \right) \begin{bmatrix} \hat{v}_{in} \end{bmatrix} \tag{5.25}$$

Solving (5.25), we get the approximated closed-loop audio susceptibility G_{vg1-cl}, G_{vg2-cl} as

$$\begin{aligned} G_{vg1-cl} &= \left.\frac{\hat{v}_{01}}{\hat{v}_{in}}\right|_{CL} \approx \frac{1}{1+T_1}\left(G_{vg1} - \frac{r_{s1} G_{m1} G_{c1} G_{ig1} G_{vd1}}{1+T_{i1}}\right) \\ G_{vg2-cl} &= \left.\frac{\hat{v}_{02}}{\hat{v}_{in}}\right|_{CL} \approx \frac{1}{1+T_2}\left(G_{vg2} - \frac{r_{s2} G_{m2} G_{c2} G_{ig2} G_{vd2}}{1+T_{i2}}\right) \end{aligned} \tag{5.26}$$

It is to be noted that when current loop is absent ($T_{i1} = T_{i2} = 0$), the expression of G_{vg1-cl}, G_{vg2-cl} become same as in voltage mode control (VMC). It is observed from (5.26) that inner current loop provides addition attenuation to G_{vg1}, G_{vg2}. Thus, audio susceptibility is improved with ACC.

5.3.3.2 Closed-loop Load Regulation

The closed-loop load regulation transfer functions can be obtained from (5.17) by making $\hat{v}_{ref1} = \hat{v}_{ref2} = \hat{v}_{in} = 0$, applying (5.19) and is given by

$$\begin{bmatrix} 1+T_1 & 0 \\ 0 & 1+T_2 \end{bmatrix} \begin{bmatrix} \hat{v}_{01} \\ \hat{v}_{02} \end{bmatrix} \approx \left(\begin{bmatrix} Z_{vi11} & Z_{vi12} \\ Z_{vi21} & Z_{vi22} \end{bmatrix} - \begin{bmatrix} \frac{G_{vd1}}{1+T_{i1}} & 0 \\ 0 & \frac{G_{vd2}}{1+T_{i2}} \end{bmatrix} \begin{bmatrix} H_{ii11} r_{s1} G_{c1} G_{m1} & H_{ii12} r_{s1} G_{c1} G_{m1} \\ H_{ii21} r_{s2} G_{c2} G_{m2} & H_{ii22} r_{s2} G_{c2} G_{m2} \end{bmatrix} \right) \begin{bmatrix} \hat{i}_{01} \\ \hat{i}_{02} \end{bmatrix} \tag{5.27}$$

Solving (5.27), we get

The approximated closed-loop self-regulation as

$$\begin{aligned} Z_{vi11-cl} &= \left.\frac{\hat{v}_{01}}{-\hat{i}_{01}}\right|_{CL} \approx \frac{1}{1+T_1}(Z_{vi11} + \frac{r_{s1}G_{m1}G_{c1}G_{vd1}H_{ii11}}{1+T_{i1}}) \\ Z_{vi22-cl} &= \left.\frac{\hat{v}_{02}}{-\hat{i}_{02}}\right|_{CL} \approx \frac{1}{1+T_2}(Z_{vi22} + \frac{r_{s2}G_{m2}G_{c2}G_{vd2}H_{ii22}}{1+T_{i2}}) \end{aligned} \tag{5.28}$$

The approximated closed-loop cross-regulation as

$$\begin{aligned} Z_{vi12-cl} &= \left.\frac{\hat{v}_{01}}{\hat{i}_{02}}\right|_{CL} \approx \frac{1}{1+T_1}(Z_{vi12} - \frac{r_{s1}G_{m1}G_{c1}G_{vd1}H_{ii12}}{1+T_{i1}}) \\ Z_{vi21-cl} &= \left.\frac{\hat{v}_{02}}{\hat{i}_{01}}\right|_{CL} \approx \frac{1}{1+T_2}(Z_{vi21} - \frac{r_{s2}G_{m2}G_{c2}G_{vd2}H_{ii21}}{1+T_{i2}}) \end{aligned} \tag{5.29}$$

When current loop is absent ($T_{i1} = T_{i2} = 0$), the expression of closed-loop self and cross regulation reduces and becomes same as in VMC. It is seen from (5.29) that, inner loop provides additional attenuation to Z_{vi12}, Z_{vi21}. Thus, cross-regulation is improved with ACC. From (5.28), it is worth noting that inner loop provides addition gain to $Z_{vi11-cl}$, $Z_{vi22-cl}$. Thus, self-regulation is inferior with ACC as compared to VMC.

5.4 Stability of Inner Current Loops

The stability of the inner current loop can be evaluated based on the approximated inner current loop gains T_{i1}, T_{i2}. Substituting (5.11), transfer function of controller and PWM in (5.10), we obtain

$$T_{ij} = \frac{V_{in}r_{sj}k_{cj}}{V_m R_j} \frac{(1+C_j(R_j+r_{cj})s)(1+\frac{s}{\omega_{cj-z}})}{s(\frac{L_jC_j(R_j+r_{cj})}{R_j}s^2 + s(\frac{L_j}{R_j}+C_jr_{cj})+1)(1+\frac{s}{\omega_{cj-p}})}$$

At high frequency, T_{ij} is approximated as

$$T_{ij} \approx \frac{V_{in}r_{sj}k_{cj}}{V_m L_j \omega_{cj-z}} \frac{1}{s(1+\frac{s}{\omega_{cj-p}})}, \text{ where, } j = \{1,2\} \tag{5.30}$$

The phase of T_{ij} with (5.30) never gets beyond -180^0. Thus, a continuous-time control circuit is expected to be stable. However, a switching control circuit may be unstable, i.e., exhibit sub-harmonic oscillation when the loop gain $|T_{ij}|$ is high.

The sub-harmonic oscillation can be avoided by optimally designing $|G_{cj}|$ based on slope-criteria [77]. The slope-criteria is that up-slope of G_{cj} output (i.e., same as the off-time slope of inductor currents) applied at one input of PWM is equal to ramp slope applied at other input of PWM.

The off-time slope of i_{L1} when S_{T1} is off is m_{FF1} and off-time slope of i_{L2} when S_{T2} is off is m_{NF2} as shown in Figure 5.1(b). The magnitude of inductor current slopes are provided in Table 6.1 and the slopes m_{FF1}, m_{NF2} are given as

$$m_{FF1} = \frac{V_{01} + \frac{M}{L_2}V_{02}}{L_1^{'}} \quad m_{NF2} = \frac{V_{02} + \frac{M}{L_1}(V_{in} - V_{01})}{L_2^{'}}$$

The stability criteria becomes

$$\begin{aligned} |G_{c1}|r_{s1}m_{FF1} = V_m f_s \implies \frac{|G_{c1}|r_{s1}}{L_1^{'}}(V_{01} + \frac{M}{L_2}V_{02}) = V_m f_s \\ |G_{c2}|r_{s2}m_{NF2} = V_m f_s \implies \frac{|G_{c2}|r_{s2}}{L_2^{'}}(V_{02} + \frac{M}{L_1}(V_{in} - V_{01})) = V_m f_s \end{aligned} \tag{5.31}$$

solving (5.31) we get,

$$\begin{aligned} |G_{c1}| = \frac{\hat{v}_{d1}}{\hat{v}_{rs1}} = \frac{V_m f_s L_1^{'}}{r_{s1}(V_{01} + \frac{M}{L_2}V_{02})} \\ |G_{c2}| = \frac{\hat{v}_{d2}}{\hat{v}_{rs2}} = \frac{V_m f_s L_2^{'}}{r_{s2}(V_{02} + \frac{M}{L_1}(V_{in} - V_{01}))} \end{aligned} \tag{5.32}$$

The small-signal control to output gain ($\frac{\hat{v}_{rs1}}{\hat{v}_{d1}}$, $\frac{\hat{v}_{rs2}}{\hat{v}_{d2}}$) of CI-SIDO buck at high frequency are given by

$$\frac{\hat{v}_{rs1}}{\hat{v}_{d1}} = \frac{r_{s1}V_{in}}{sV_m L_1^{'}} \ , \ \frac{\hat{v}_{rs2}}{\hat{v}_{d2}} = \frac{r_{s2}V_{in}}{sV_m L_2^{'}} \tag{5.33}$$

By multiplying (5.32) with (5.33) and setting equal to 1, the gain crossover frequency of G_{c1} (f_{ci1}) and G_{c2} (f_{ci2}) are

$$f_{ci1} = \frac{f_s}{2\pi(D_1 + \frac{M}{L_2}D_2)} \ , \ f_{ci2} = \frac{f_s}{2\pi(D_2 + \frac{M}{L_1}(1 - D_1))} \tag{5.34}$$

To avoid the instability, the gain crossover frequency of G_{c1}, G_{c2} have upper limits as defined in (5.34). Substituting the circuit parameters in (5.34), we get, $f_{ci1} = 19.8$ kHz, $f_{ci2} = 28.34$ kHz. The correctness of stability requirement in (5.34) is validated by simulating following four

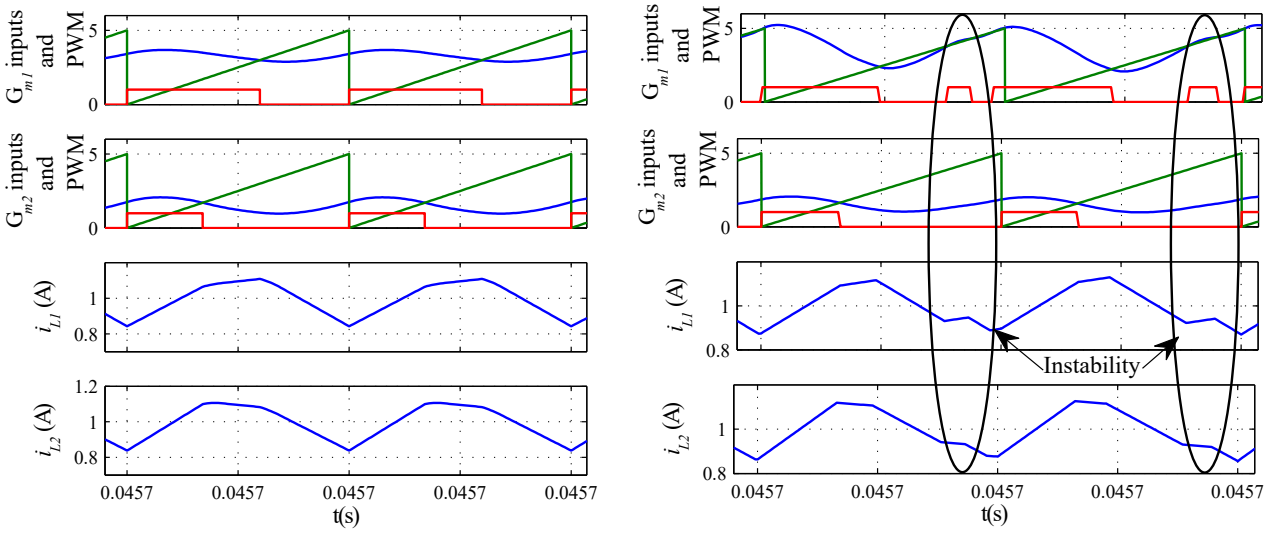
cases with different f_{ci1} and f_{ci2} and the results are shown in Figure 5.3.

Case A: $f_{ci1} = 13\ kHz\ <\ 19.8\ kHz$, $f_{ci2} = 27\ kHz\ <\ 28.34\ kHz$

Case B: $f_{ci1} = 28\ kHz\ >\ 19.8\ kHz$, $f_{ci2} = 27\ kHz\ <\ 28.34\ kHz$

Case C: $f_{ci1} = 13\ kHz\ <\ 19.8\ kHz$, $f_{ci2} = 38\ kHz\ >\ 28.34\ kHz$

Case D: $f_{ci1} = 28\ kHz\ >\ 19.8\ kHz$, $f_{ci2} = 38\ kHz\ >\ 28.34\ kHz$



(a) Case A (b) Case B

(c) Case C (d) Case D

Figure 5.3: Steady-state inductor current waveforms along with comparator inputs and PWM signals

Figure 5.3 shows the inductor current waveforms along with comparator inputs and PWM signals. It is seen that stable inductor current waveforms are obtained only in case A, as

required by stability criteria of (5.34). And as predicted instability occurs in Case B, C, D.

5.5 Proposed Compensator Design Procedure

This section provides the procedure to design current and voltage compensators for ACC of CI-SIDO buck converter.

5.5.1 Design Procedure for Inner Current Compensator

The target of designing inner current compensator G_{cj} is to suppress the cross-coupling effect and avoid instability.

5.5.1.1 Design Consideration

Following design considerations are used for designing G_{cj}:

(i) Decoupling of inductor currents: To decouple the inductor currents, G_{cj} needs to be designed satisfying (5.7). In other words, the cross-coupling $A_{21}^{'} \approx 0$, if from (5.5)

$$\frac{|G_{id21}|}{|G_{id11}G_{m1}r_{s1}G_{c1}|} \approx 0, \quad \frac{|G_{id12}|}{|G_{id22}G_{m2}r_{s2}G_{c2}|} \approx 0$$

The above ratio is satisfied, if $|G_{cj}| \to \infty$. Practically, it is not possible. Therefore, considering $\frac{|G_{id21}|}{|G_{id11}G_{m1}r_{s1}G_{c1}|} = \gamma$, $\frac{|G_{id12}|}{|G_{id22}G_{m2}r_{s2}G_{c2}|} = \gamma$ where $\gamma \approx 0$, $|G_{c1}|$, $|G_{c2}|$ are given by

$$|G_{c1}| = \frac{|G_{id21}|}{|G_{id11}G_{m1}r_{s1}| * \gamma}, \quad |G_{c2}| = \frac{|G_{id12}|}{|G_{id22}G_{m2}r_{s2}| * \gamma} \tag{5.35}$$

The decoupled inner current loop gain T_{i1}, T_{i2} at gain crossover frequency f_{ci1}, f_{ci2} are given by

$$|G_{id1}G_{c1}G_{m1}r_{s1}| = 1 \text{ and } |G_{id2}G_{c2}G_{m2}r_{s2}| = 1 \tag{5.36}$$

Using (5.35) in (5.36), f_{ci1}, f_{ci2} are found to be

$$f_{ci1} = f_{ci2} = \frac{1}{2\pi}\frac{V_{in}M}{\gamma L_1 L_2} \tag{5.37}$$

As γ and f_{ci1} are inversely proportional, larger the f_{ci1}, lower will be cross-coupling and faster will be transient response. However, larger f_{ci1} leads to instability problem.

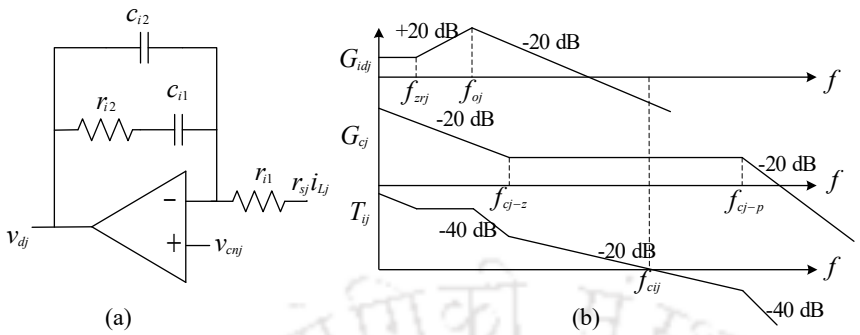


Figure 5.4: Bode plots of G_{idj}, loop gain T_{ij}, compensator G_{cj}

(ii) Stability criteria: As discussed in Section 5.4, the sub-harmonic oscillations is avoided by choosing the inner loop gain crossover frequency less than (5.34).

5.5.1.2 Current Compensator Design Procedure

The goal of designing G_{cj} is to obtain highest crossover frequency f_{cij}, consistent with stability criteria. f_{cij} is related to speed of the system response and cross-coupling. Higher the f_{cij} lesser the cross-coupling and faster the transient response. However, f_{cij} has upper limit based on stability criteria. Also, the desired loop gain at f_{cij} should have -20 dB slope with phase margin (PM) greater than 45^o. Figure 5.4 shows the circuit diagram of Type-II compensator G_{cj} and bode plots of G_{idj}, T_{ij}, G_{cj}. In Figure 5.4, f_{zrj}, f_{oj} are the zero frequency, resonant pole frequency of G_{idj} given by (5.11) and f_{cj-z}, f_{cj-p} are the zero, pole frequency of G_{cj}. The design procedure is as follows:

- Step 1: Calculate the compensator gain: The compensator gain $|G_{cj}|$ is calculated using (5.32).
- Step 2: Calculate the gain crossover frequency f_{cij}: To reduce the cross-coupling, f_{cij} should be high being consistent with stability criteria. Thus, the f_{cij} is chosen as given in (5.34).
- Step 3: Place the compensator zero f_{cj-z}: To achieve good PM, the compensator should have flat gain characteristic at f_{cij} as shown in Figure 5.4. Thus, the compensator zero

Table 5.1: Design specification of the converter

Symbol	V_{in}	V_{01}, V_{02}	C_1, C_2	R_1, R_2	$r_{c1} = r_{c2}$	$\beta_1 = \beta_2$
Value	10 V	6 V, 3.3 V	320 μF, 320 μF	6 Ω, 3.3 Ω	0.2 Ω	1/3
Symbol	V_m	$r_{s1} = r_{s2}$	L_1, L_2	M	f_s	
Value	5 V	0.5	190 μH ,180 μH	130 μH	100 kHz	

is placed at

$$f_{cj-z} = \frac{1}{2\pi c_{i1} r_{i2}} = \frac{f_{cij}}{3} \tag{5.38}$$

- Step 4: Place the compensator pole f_{cj-p}: The purpose of the compensator pole is to eliminate the switching noise spikes. Thus, the compensator pole is placed at

$$f_{cj-p} = \frac{1}{2\pi}\left(\frac{c_{i1} + c_{i2}}{c_{i1} c_{i2} r_{i2}}\right) = \frac{f_s}{2} \tag{5.39}$$

5.5.2 Design Procedure for Outer Voltage Compensator

With a well designed inner current compensator, outer voltage compensator is simple. The output loop gains (T_1, T_2) are given in (5.24) and can be approximated as

$$T_j \approx \frac{\beta_j G_{vj} G_{vdj}}{r_{sj} G_{idj}} \quad \text{where, } j = \{1, 2\}. \tag{5.40}$$

In ACC, the inner current loop has a fast dynamic, and outer voltage loop has a slow dynamic. The reason is that the inductor current responds quickly to change in input and load. Therefore, the crossover frequency of outer voltage loop (f_{cj}) is taken $1/10^{th}$ of f_{cij} [77], [78]. For good transient response, i.e. less overshoot and less ringing, a phase margin (PM) greater than 45^o is required. Thus, to achieve PM of 55^o at f_{cj}, the parameters of the compensator are calculated using

$$\left|\frac{G_{vj} G_{vdj} \beta_j}{r_{sj} G_{idj}}\right| = 1 \; ; \; 180^o + \angle\left(\frac{G_{vj} G_{vdj} \beta_j}{r_{sj} G_{idj}}\right) = PM \tag{5.41}$$

5.5.3 Example of Compensator Design

This subsection provides the design example following the design procedure as discussed in Section 5.5. The converter parameter is shown in Table 5.1.

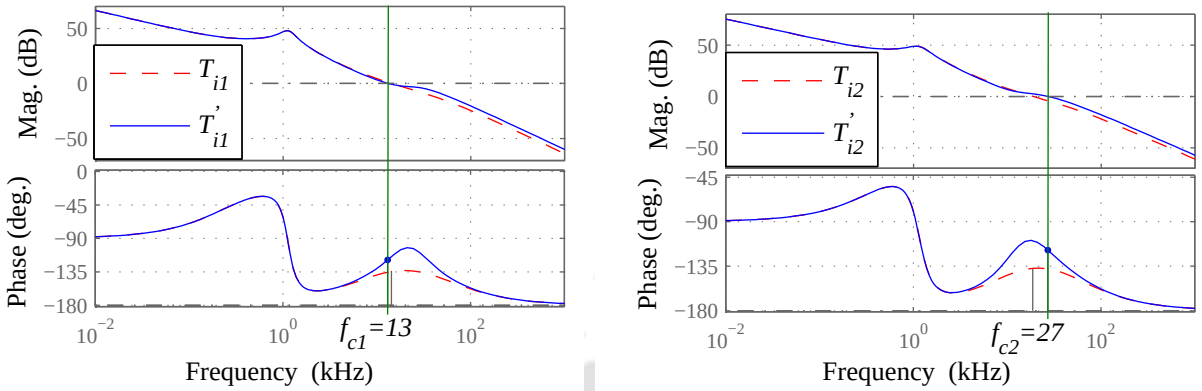


Figure 5.5: Bode plot of current loop gain transfer function (a) $T_{i1}^{'}$ (b) $T_{i2}^{'}$

5.5.3.1 Design Example of Current Loops

The current compensator G_{c1}, G_{c2} is designed as follows:

Step 1: Using circuit parameter in (5.32),

$$|G_{c1}|_{f_{ci1}} = \frac{k_{c1}}{\omega_{c1-z}} = 15.16 \; ; \; |G_{c2}|_{f_{ci2}} = \frac{k_{c1}}{\omega_{c1-z}} = 20.51 \tag{5.42}$$

Step 2: Using circuit parameter in (5.34), f_{ci1}, f_{ci2} are found to be 19.8 kHz and 28.34 kHz.

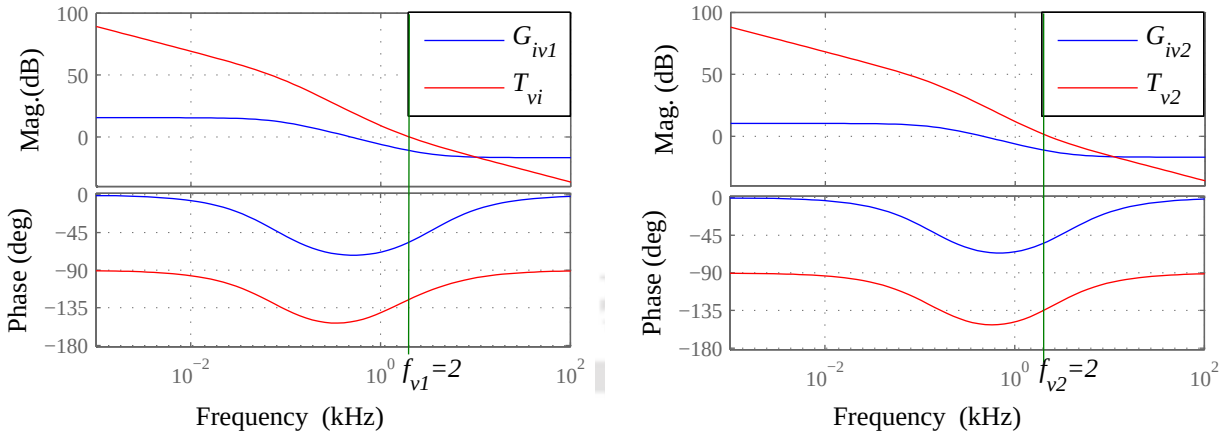
Step 3: Using (5.38), zero of compensator G_{c1}, G_{c2} is placed at $\omega_{c1-z} = 41460$ rad/s, $\omega_{c2-z} = 59355$ rad/s respectively. From (5.42), we get $k_{c1} = 628 * 10^3$, $k_{c2} = 1217.48 * 10^3$.

Step 4: Using (5.39), pole of the compensator G_{c1}, G_{c2} is placed at $\omega_{c1-p} = \omega_{c2-p} = 314159$ rad/s.

Thus, G_{c1}, G_{c2} is given by

$$G_{c1} = \frac{628 * 10^3(1 + 24 * 10^{-6}s)}{s(1 + 3.18 * 10^{-6}s)}; \; G_{c2} = \frac{1217 * 10^3(1 + 16.8 * 10^{-6}s)}{s(1 + 3.18 * 10^{-6}s)} \tag{5.43}$$

The bode plot of both actual ($T_{i1}^{'}$, $T_{i2}^{'}$) and approximated (T_{i1}, T_{i2}) current loop gains with designed compensator G_{c1}, G_{c2} are plotted in Figure 5.5. As it can be seen in the figure, the magnitude plots of both actual and approximated current loop gains are nearly equal, and deviation in phase plot at crossover frequency occurs in actual loop gains. This is due to the influence of both controllers G_{c1}, G_{c2} in $T_{i1}^{'}$, $T_{i2}^{'}$. The PM = 61° of $T_{i1}^{'}$ is achieved at 13 kHz.



(a) (b)

Figure 5.6: Bode plot of uncompensated and compensated voltage loop gain transfer functions (a) $G_{vi1} = \frac{G_{vd1}}{G_{id1}}$ and T_{v1} (a) $G_{vi2} = \frac{G_{vd2}}{G_{id2}}$ and T_{v2}

The PM $= 61°$ of T'_{i2} is achieved at 27 kHz. The low frequency gain is improved.

5.5.3.2 Design Example of Voltage Loops

The crossover frequency f_{c1}, f_{c2} of voltage loop are selected as 2 kHz. From Figure 5.6, the magnitude and phase of $G_{vi1} = \frac{G_{vd1}}{G_{id1}}$, $G_{vi2} = \frac{G_{vd2}}{G_{id2}}$ is found as $|G_{vi1}|_{f_{c1}} = -11$ dB, $|G_{vi2}|_{f_{c2}} = -11.2$ dB and $\angle G_{iv1}|_{f_{c1}} = 56.6^o$, $\angle G_{iv2}|_{f_{c2}} = 54.7^o$. Using the above value in (5.41) and solving we get,

$$G_{v1} = \frac{45.4 * 10^3(1 + 117 * 10^{-6}s)}{s(1 + 54 * 10^{-6}s)} \quad ; \quad G_{v2} = \frac{47.8 * 10^3(1 + 113 * 10^{-6}s)}{s(1 + 56 * 10^{-6}s)} \tag{5.44}$$

The required PM $= 55^o$ is achieved with the designed G_{v1}, G_{v2} and is observed from the bode plots shown in Figure 5.6.

5.6 Simulation Results and Analysis

To validate the effectiveness of the proposed control method, CI-SIDO buck converter with average current control is simulated in MATLAB SIMULINK environment. The converter parameter used in simulation are given in Table 5.1.

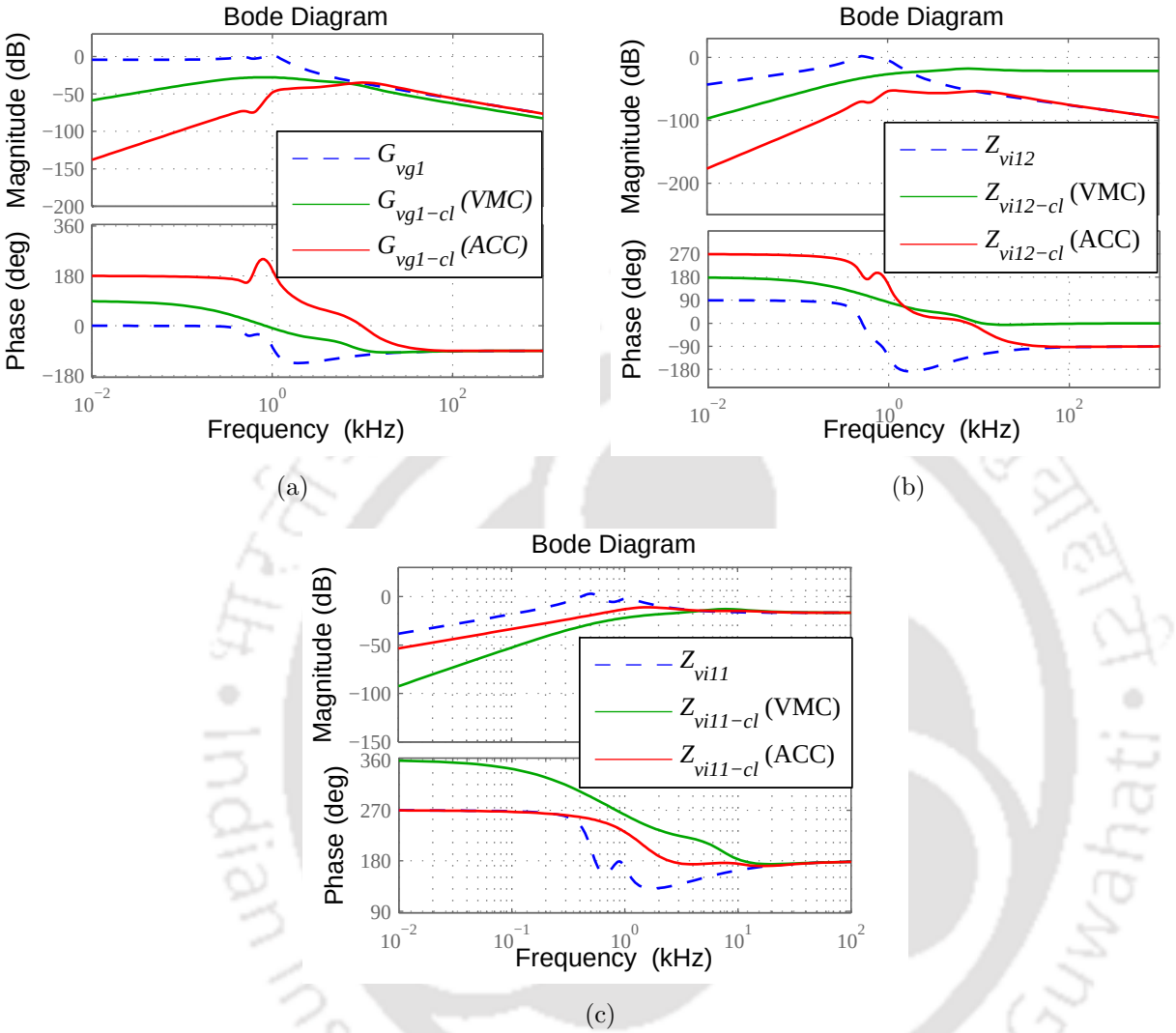


Figure 5.7: Comparison of audio-susceptibility, cross-regulation and self-regulation with ACC and VMC (a) G_{vg1} (b) Z_{vi12} (c) Z_{vi11}

5.6.1 Frequency Domain Analysis

The closed-loop performance of the proposed decoupled average current control is studied using the bode plots of cross-regulation $Z_{vi12-cl}$, audio-susceptibility G_{vg1-cl}, self-regulation $Z_{vi11-cl}$. Figure 5.7 shows the bode plots of closed-loop audio susceptibility, cross-regulation and self-regulation for both average current control (ACC) and voltage mode control (VMC) together with open loop transfer functions. It can be observed that audio-susceptibility and cross-regulation is improved with ACC which shows low magnitude in low frequency region. Moreover, the self-regulation with ACC is worse compared to VMC. The reason is that the

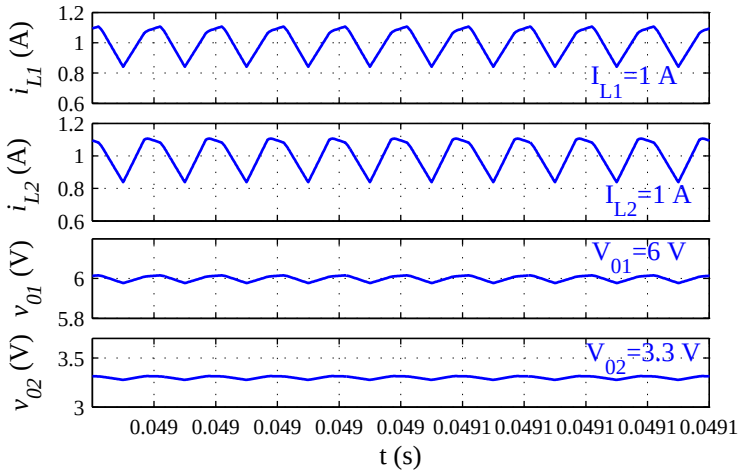


Figure 5.8: Simulation results of steady-state i_{L1}, i_{L2}, v_{01}, v_{02}

inner current loop provides additional gain in the closed-loop self-regulation transfer function as illustrated in (5.28).

5.6.2 Time Domain Analysis

5.6.2.1 Steady-state Performance

Figure 5.8 shows the simulation results for steady-state inductor currents and output voltages. It is observed that the proposed decoupled ACC method is able to regulate v_{01} and v_{02} at 6 V and 3.3 V with voltage ripple $\Delta v_{01} = 40$ mV, $\Delta v_{02} = 39$ mV which is less than 3%.

5.6.2.2 Dynamic Performance

Load regulation: Figure 5.9 shows the simulation results for step change in load current. Figure 5.9(a) shows the simulation results for step change in i_{01} from 1 A to 2 A keeping i_{02} constant at 1 A. It is observed that due the step change in i_{01}, the output voltage v_{01} under goes undershoot (self-regulation) of 0.2 V with settling time 0.4 ms and v_{02} under goes overshoot (cross-regulation) of 0.005 V with settling time of 0.08 ms. Similarly, Figure 5.9(b) shows the simulation results for step change in i_{02} from 1 A to 2 A keeping i_{01} constant at 1 A. It is observed that the v_{01} under goes overshoot (cross-regulation) of 0.03 V with settling time 0.08 ms and v_{02} under goes undershoot (self-regulation) of 0.18 V with settling time of 0.4 ms.

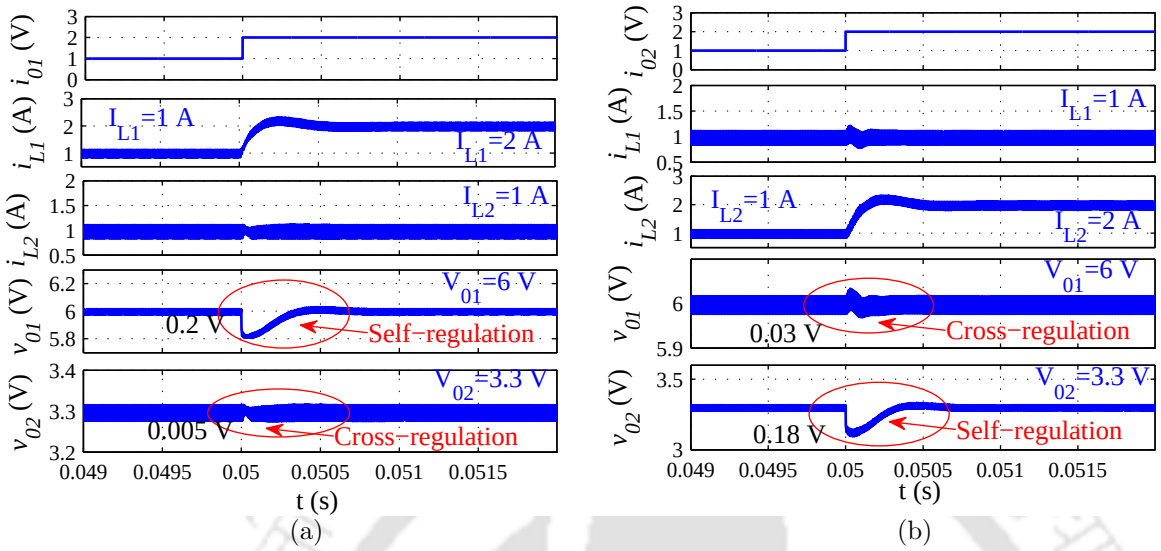


Figure 5.9: Simulation results for load regulation (a) Step change in i_{01} (b) Step change in i_{02}

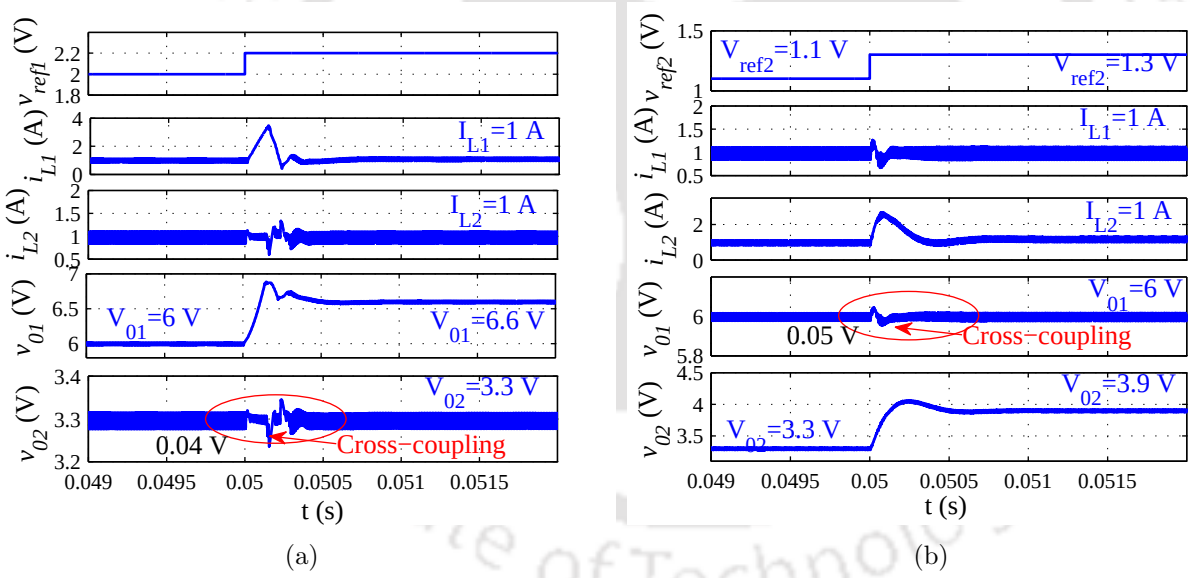


Figure 5.10: Simulated results for cross-coupling (a) Step change in v_{ref1} (b) Step change in v_{ref2}

Cross-coupling: Figure 5.10 shows the simulation results for step change is reference voltage. Figure 5.10(a) shows the simulation results for step change in v_{ref1} from 2 V to 2.2 V. It is observed that when v_{ref1} changes from 2 V to 2.2 V correspondingly v_{01} changes from 6 V to 6.6 V with negligible cross-coupling effect in v_{02} of about 0.04 V with transient time 0.35 ms. Similarly, for step change in v_{ref2} from 1.1 V to 1.3 V, v_{02} change from 3.3 V to 3.9 V and v_{01} experience negligible cross-coupling of 0.05 V with transient time 0.15 ms.

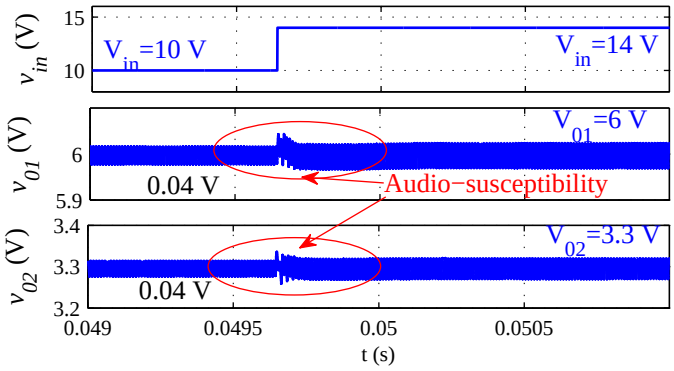


Figure 5.11: Simulation results for audio-susceptibility (Step change in v_{in})

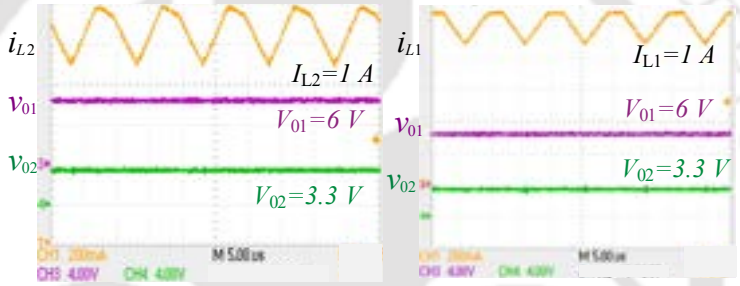


Figure 5.12: Experimental results of steady-state waveform of i_{L1}, i_{L2}, v_{01}, v_{02}

Audio-susceptibility: Figure 5.11 shows the simulation results of output voltage for step change is input voltage v_{in}. It is observed that for step change in the input voltage v_{in} from 10 V to 14 V, the output voltages v_{01} and v_{02} experience negligible audio-susceptibility of about 0.04 V with settling time 0.2 ms.

5.7 Experimental Results

The proposed decoupled average current control method is verified by developing a experimental prototype of CI-SIDO buck converter. The parameter of the converter used for experimental test is same as listed in Table 5.1.

5.7.1 Steady-state Performance

Figure 5.12 gives the experimental steady-state waveform of output voltages (v_{01}, v_{02}) and inductor currents (i_{L1}, i_{L2}). The v_{01}, v_{02} are regulated at 6 V and 3.3 V respectively.

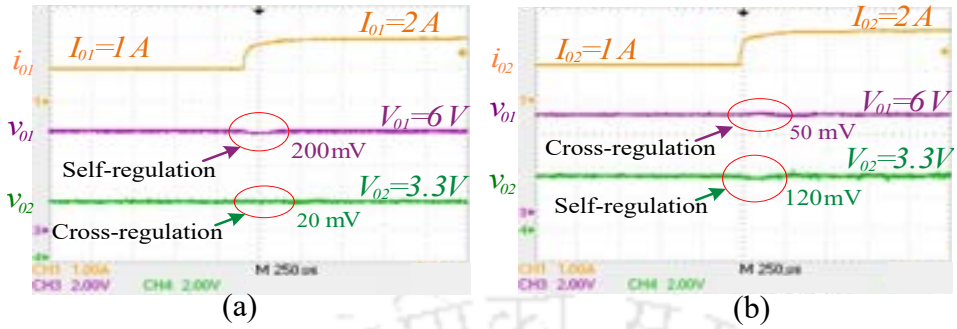


Figure 5.13: Experimental results for step change in load current (a) i_{01} (b) i_{02}

5.7.2 Dynamic Performance

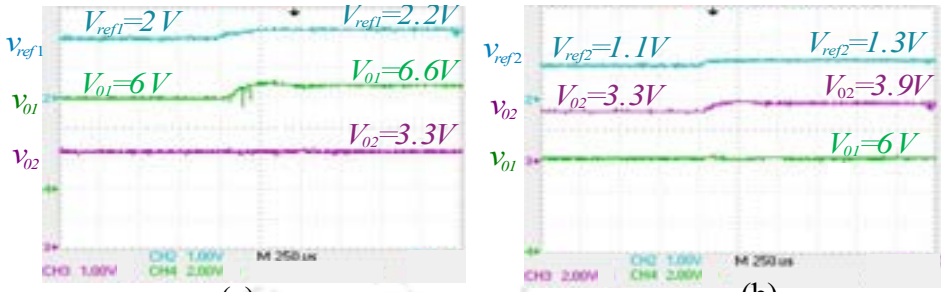
5.7.2.1 Load Regulation

The experimental waveforms for the step load response are presented in Figure 5.13. The results are presented for 100 % load increment. The transient response time of v_{01} is 0.2 ms, when i_{01} is changed from 1 A to 2 A with i_{02} = 1 A; v_{01} undergoes an undershoot (self-regulation) of about 0.2 V, and v_{02} experience overshoot (cross-regulation) of about 0.02 V (shown in Figure 5.13(a)).

Similarly, the transient response time of v_{02} is 0.2 ms, when i_{02} is changed from 1 A to 2 A with i_{01} = 1 A; v_{02} undergoes self-regulation of about 0.12 V, and v_{01} experiences cross-regulation of about 0.05 V (shown in Figure 5.13(b)).

5.7.2.2 Cross-coupling

The experimental results for step change in reference voltage are shown in Figure 5.14. It can be seen in Figure 5.14(a) that when v_{ref1} is changed from 2 V to 2.2 V, v_{01} changes accordingly from 6 V to 6.6 V, and v_{02} experiences negligible cross-coupling. Similarly, it can be observed in Figure 5.14(b) that, when v_{ref2} is changed from 1.1 V to 1.3 V, v_{02} changes accordingly from 3.3 V to 3.9 V, and v_{01} experiences negligible cross-coupling. This shows that the proposed controller is able to reduce the cross-coupling effect.



(a) (b)

Figure 5.14: Experimental results for step change in (a) v_{ref1} (b) v_{ref2}

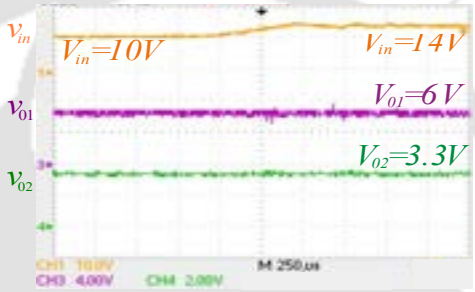


Figure 5.15: Experimental results for step change in v_{in}

5.7.2.3 Audio-susceptibility

The experimental result for step change in input voltage is shown in Figure 5.15. It is observed that v_{01}, v_{02} experience negligible audio-susceptibility effect, when v_{in} is changed from 10 V to 14 V. Thus, the proposed controller improves audio-susceptibility.

5.7.3 Performance Comparison

The closed-loop performance of the proposed decoupled ACC for CI-SIDO buck converter is evaluated based on the performance indices discussed in chapter 4. Based on the simulation and experimental results, the performance indices of decoupled average current controlled CI-SIDO

Table 5.2: Comparison with existing methods of SIDO converter

References	[34]	[38]	[46]	Chapter 4	This Chapter
Topology	SI-SIDO buck	SI-SIDO buck	SI-SIDO buck	CI-SIDO buck	CI-SIDO buck
Control method	Cross-derivative state feedback	Model Predictive control	Current ripple control	Decoupled Voltage mode control	Decoupled average current control
Input	4.8 V	20 V	10 V	10 V	10 V
Output	3.3 V, 1.2 V	12 V, 8 V	5 V, 3.3 V	6 V, 3.3 V	6 V, 3.3 V
Load current	0.1 A, 0.1 A	1.2 A - 2.4 A 0.8 A - 2.0 A	2.5 A, 1.1 A	0.5 A - 3 A 0.5 A - 3 A	1 A - 2.5 A, 1 A - 2.5 A
Output power	0.45 W	39 W	16 W	28 W	24 W
f_s	100 kHz	100 kHz	50 kHz	100 kHz	100 kHz
SRI_1 SRI_2	0.033 0.03	0.014 0.019	* *	0.03 0.024	0.033 0.036
CRI_1 CRI_2	0.015 0.013	0.025 0.01	0.04 0.006	0.016 0.015	0.008 0.006
CCI_1 CCI_2	* *	0.27 *	* *	0.059 0.096	0.046 0.12
ASI_1 ASI_2	* *	* *	* *	0.025 0.037	0.016 0.022

buck converter are calculated as follows

$$\begin{aligned}
\mathrm{SRI}_1 &= \frac{\Delta V_{01}/V_{01}}{\Delta I_{01}/I_{01}} = \frac{0.2/6}{1/1} = 0.033\ ,\ \mathrm{SRI}_2 = \frac{\Delta V_{02}/V_{02}}{\Delta I_{02}/I_{02}} = \frac{0.12/3.3}{1/1} = 0.036 \quad \text{(Experimental)} \\
\mathrm{CRI}_1 &= \frac{\Delta V_{01}/V_{01}}{\Delta I_{02}/I_{02}} = \frac{0.05/6}{1/1} = 0.008\ ,\ \mathrm{CRI}_2 = \frac{\Delta V_{02}/V_{02}}{\Delta I_{01}/I_{01}} = \frac{0.02/3.3}{1/1} = 0.006 \quad \text{(Experimental)} \\
\mathrm{ASI}_1 &= \frac{\Delta V_{01}/V_{01}}{\Delta V_{in}/V_{in}} = \frac{0.04/6}{4/10} = 0.016\ ,\ \mathrm{ASI}_2 = \frac{\Delta V_{02}/V_{02}}{\Delta V_{in}/V_{in}} = \frac{0.03/3.3}{4/10} = 0.0227 \quad \text{(Simulation)} \\
\mathrm{CCI}_1 &= \frac{\Delta V_{01}/V_{01}}{\Delta V_{ref2}/V_{ref2}} = \frac{0.05/6}{0.2/1.1} = 0.045, \mathrm{CCI}_2 = \frac{\Delta V_{02}/V_{02}}{\Delta V_{ref1}/V_{ref1}} = \frac{0.04/3.3}{0.2/2} = 0.12 \text{(Simulation)}
\end{aligned} \tag{5.45}$$

The performance comparison of the proposed control method for CI-SIDO buck with other related work existing in literature, i.e., [34], [38], [46] for SIDO buck converter is shown in Table 5.2. From Table 5.2, it is observed that the CRI value of this chapter is less than all existing work. SRI value is almost same as that in [34], and higher than decoupled VMC. However, CCI and ASI is less than decoupled VMC of CI-SIDO buck converter. Therefore, the proposed decoupled average current control for CI-SIDO buck has better cross-regulation suppression, medium self-regulation suppression and reduced cross-coupling and audio-susceptibility with good dynamic response.

5.8 Conclusion

This chapter presents a method of decoupling the cross-coupling problem in CI-SIDO buck converter under average current control. The decoupling process allows the inner current controller to be designed with high gain or high gain crossover frequency. The effect of decoupling is investigated on closed-loop transfer functions. It shows that the outer voltage loop becomes the same as that of the buck converter, and the closed-loop transfer functions, i.e., audio-susceptibility, self-regulation and cross-regulation become simplified. However, with high controller gain, there exists instability in the inner current loop. So, the optimal current compensator gain condition to avoid instability is derived. A design procedure for the current controller is proposed by considering both the decoupling and the stability condition.

The closed-loop performance of average current control is compared with voltage-mode control, which reveals that the proposed control has better dynamic performance. The presented decoupling and compensator design method is validated using both simulation and experimental results. The decoupling is demonstrated experimentally with tracking of the output voltage of one sub-converter unaffected by the change in reference voltage of the other sub-converter, and vice versa.

Note: Major part of this chapter is reproduced from my publications:

1. G. Nayak and S. Nath, "Decoupled Average Current Control of Coupled Inductor Single-Input Dual-Output Buck Converter," in IEEE Journal of Emerging and Selected Topics in Industrial Electronics, vol. 1, no. 2, pp. 152-161, Oct. 2020, doi: 10.1109/JESTIE.2020.3014833.

2. G. Nayak and S. Nath, "Dynamic Performance of Coupled SIDO Buck Converter Operating in Current Mode and Voltage Mode Control", 2020 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Jaipur, India, 2020. (Accepted)

6

Unified Model of Peak Current Mode Controlled CI-SIDO Converters

Contents

6.1 Introduction

Chapter 5 has introduced the average current control (ACC) for CI-SIDO buck converter to improve the dynamic performance and suppress the cross-regulation and cross-coupling. However, the ACC suffers from switching instability when the inner current controller gain is high. Thus, to avoid instability, the inner current loop bandwidth is limited, which results in slow transient response and poor cross-regulation. Moreover, four controllers are needed to implement average current control for CI-SIDO converter.

The effective way to improve the dynamic performance and reduce cross-regulation is by introducing peak current mode control for the CI-SIDO converter. Peak current mode (PCM) control is a promising control scheme for DC-DC converters due to its advantages such as fast transient response, inherent current limiting, over current protection and easier controller design [79]. While PCM control has many benefits, there is one drawback, i.e., PCM exhibits switching instability known as a sub-harmonic oscillation (SHO), which occurs when the duty cycle is greater than 0.5. SHO lead to reduced efficiency, increased noise, and should be avoided. SHO is prevented by using external slope compensation. Thus, to design controller and slope compensation for PCM controlled converter, it is essential to derive a large-signal and small-signal model of the converter under PCM control to predict the system stability and dynamic characteristic. Many modelling techniques have been developed in the literature to predict the SISO dc-dc converters stability and dynamic behaviour under PCM control [79–86]. However, no work is available in the literature that develops the large-signal and small-signal model for PCM controlled CI-SIDO converters and predicts stability and dynamic characteristics.

This chapter aims to provide a unified large-signal and small-signal model of PCM controlled CI-SIDO converters. The model is derived for the three CI-SIDO converter topologies, i.e., CI-SIDO buck converter, CI-SIDO boost converter, CI-SIDO boost and buck converter. The unified model of PCM controlled CI-SIDO converter is developed by combining the current modulator's unified model with the CI-SIDO converter model. The developed unified model is validated both using simulations and experiments. Moreover, using the developed unified

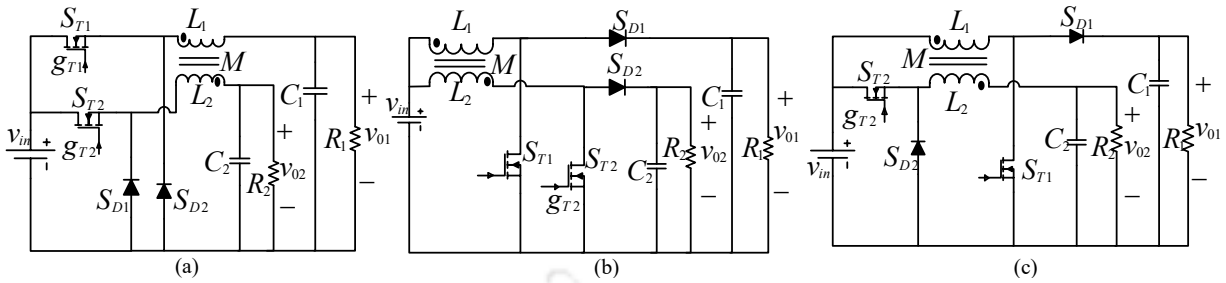


Figure 6.1: Circuit diagram of CI-SIDO converters (a) CI-SIDO buck converter (b) CI-SIDO boost converter (c) CI-SIDO boost and buck converter

model, the instability of the PCM controlled CI-SIDO converter is predicted and verified by simulation and experiment.

6.2 Operational Principle of Peak Current Mode Controlled CI-SIDO Converters

6.2.1 Different Inductor Current Slope Patterns in CI-SIDO Converter

The circuit diagram of three topologies of CI-SIDO converter is shown in Figure 6.1. The output voltages v_{01}, v_{02} are regulated by controlling the duty cycles d_1, d_2 of switches S_{T1}, S_{T2} respectively. The two switches S_{T1}, S_{T2} can operate in four different state and thus converter has four modes of operation, i.e., Mode I (S_{T1}, S_{T2} ON), Mode II (S_{T1} ON, S_{T2} OFF), Mode III (S_{T1}, S_{T2} OFF), Mode IV (S_{T1} OFF, S_{T2} ON). In CI-SIDO converters, at the given operating points D_1, D_2 the converter can operate in three modes of operation. Based on the relation of duty cycles D_1, D_2, the CI-SIDO converter can operate in three cases, i.e., Case A: $D_1 > D_2$, Case B: $D_1 < D_2$, Case C: $D_1 = D_2$. In Case A, the converter operate in Mode I, Mode II, Mode III. In Case B, the converter operate in Mode I, Mode IV, Mode III. In Case C, the converter operate in Mode I, Mode III. The slope of inductor current i_{Lj} in Mode I, II, III, IV are denoted as m_{NNj}, m_{NFj}, m_{FFj}, m_{FNj} respectively and are given in Table 6.1. Here $j = 1$ denote i_{L1}, $j = 2$ denote i_{L2}. From Table 6.1, it is observed that the slope m_{NNj} is always positive, slope m_{FFj} is always negative and slopes m_{NFj}, m_{FNj} may become positive or negative depending on the value of output voltages and coupled inductor parameters. Figure 6.2 shows

Table 6.1: Inductor current slopes of CI-SIDO converters

CI-SIDO Buck converter				
Inductor currents	NN	FF	NF	FN
i_{L1}	$m_{NN1}=\frac{(V_{in}-V_{01})+\frac{M}{L_2}(V_{in}-V_{02})}{L_1(1-k^2)}$	$m_{FF1}=\frac{(-V_{01})+\frac{M}{L_2}(-V_{02})}{L_1(1-k^2)}$	$m_{NF1}=\frac{(V_{in}-V_{01})+\frac{M}{L_2}(-V_{02})}{L_1(1-k^2)}$	$m_{FN1}=\frac{(-V_{01})+\frac{M}{L_2}(V_{in}-V_{02})}{L_1(1-k^2)}$
i_{L2}	$m_{NN2}=\frac{(V_{in}-V_{02})+\frac{M}{L_1}(V_{in}-V_{01})}{L_2(1-k^2)}$	$m_{FF2}=\frac{(-V_{02})+\frac{M}{L_1}(-V_{01})}{L_2(1-k^2)}$	$m_{NF2}=\frac{(-V_{02})+\frac{M}{L_1}(V_{in}-V_{01})}{L_2(1-k^2)}$	$m_{FN2}=\frac{(V_{in}-V_{02})+\frac{M}{L_1}(-V_{01})}{L_2(1-k^2)}$
CI-SIDO Boost converter				
i_{L1}	$m_{NN1}=\frac{V_{in}+\frac{M}{L_2}V_{in}}{L_1(1-k^2)}$	$m_{FF1}=\frac{(V_{in}-V_{01})+\frac{M}{L_2}(V_{in}-V_{02})}{L_1(1-k^2)}$	$m_{NF1}=\frac{V_{in}+\frac{M}{L_2}(V_{in}-V_{02})}{L_1(1-k^2)}$	$m_{FN1}=\frac{(V_{in}-V_{01})+\frac{M}{L_2}V_{in}}{L_1(1-k^2)}$
i_{L2}	$m_{NN2}=\frac{V_{in}+\frac{M}{L_1}V_{in}}{L_2(1-k^2)}$	$m_{FF2}=\frac{(V_{in}-V_{02})+\frac{M}{L_1}(V_{in}-V_{01})}{L_2(1-k^2)}$	$m_{NF2}=\frac{(V_{in}-V_{02})+\frac{M}{L_1}V_{in}}{L_2(1-k^2)}$	$m_{FN2}=\frac{V_{in}+\frac{M}{L_1}(V_{in}-V_{01})}{L_2(1-k^2)}$
CI-SIDO Boost and buck converter				
i_{L1}	$m_{NN1}=\frac{V_{in}+\frac{M}{L_2}(V_{in}-V_{02})}{L_1(1-k^2)}$	$m_{FF1}=\frac{(V_{in}-V_{01})+\frac{M}{L_2}(-V_{02})}{L_1(1-k^2)}$	$m_{NF1}=\frac{V_{in}+\frac{M}{L_2}(-V_{02})}{L_1(1-k^2)}$	$m_{FN1}=\frac{(V_{in}-V_{01})+\frac{M}{L_2}(V_{in}-V_{02})}{L_1(1-k^2)}$
i_{L2}	$m_{NN2}=\frac{(V_{in}-V_{02})+\frac{M}{L_1}V_{in}}{L_2(1-k^2)}$	$m_{FF2}=\frac{(-V_{02})+\frac{M}{L_1}(V_{in}-V_{01})}{L_2(1-k^2)}$	$m_{NF2}=\frac{(-V_{02})+\frac{M}{L_1}V_{in}}{L_2(1-k^2)}$	$m_{FN2}=\frac{(V_{in}-V_{02})+\frac{M}{L_1}(V_{in}-V_{01})}{L_2(1-k^2)}$

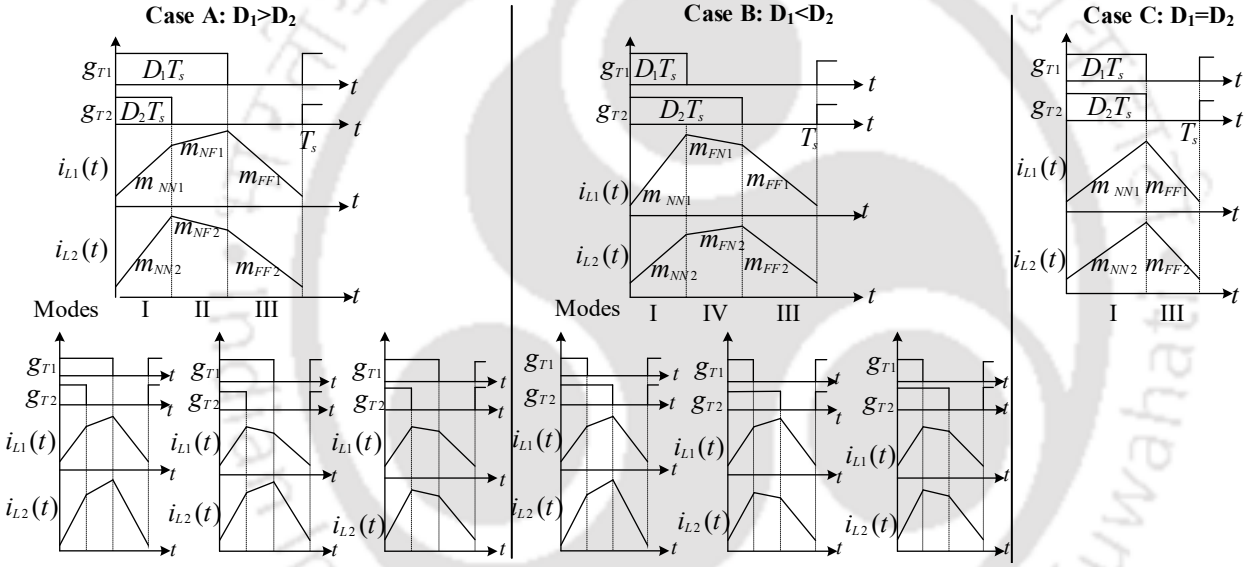


Figure 6.2: Waveform of inductor currents of CI-SIDO converters for Case A: $D_1 > D_2$, Case B: $D_2 < D_2$, Case C: $D_1 = D_2$

the waveforms of duty cycles and inductor currents for three cases with different possibility of inductor current slope pattens. It is observed from Figure 6.2 that there are four possible inductor current patterns in Case A and Case B. In Case C, there is only one possible inductor current pattens. Therefore, in CI-SIDO converter total 9 inductor current slope patterns are possible.

6.2.2 Peak Current Mode Control for CI-SIDO Converters

To regulate the two outputs of CI-SIDO converters, two peak current mode (PCM) control are implemented and is shown in Figure 6.3. The PCM control circuit as shown in Figure 6.3

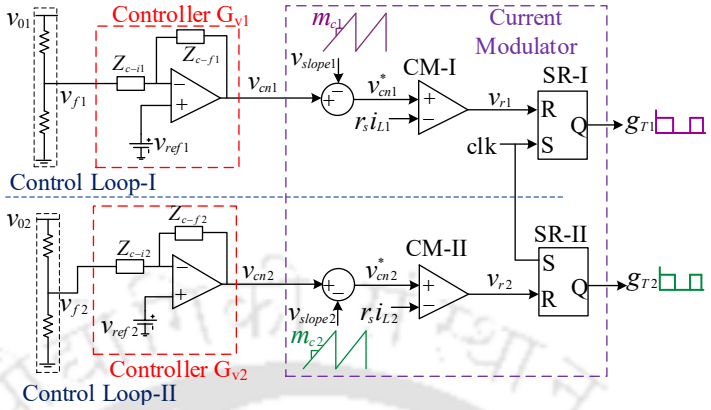


Figure 6.3: Control circuit of peak current mode controlled CI-SIDO converters

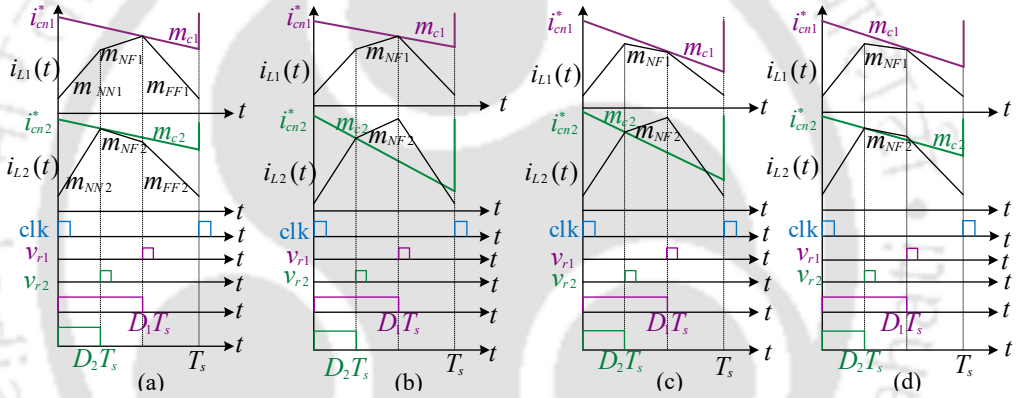


Figure 6.4: Operating waveform of PCM controlled CI-SIDO converter for Case A with different inductor current slopes (a) $m_{NF1} > 0$, $m_{NF2} < 0$ (b) $m_{NF1} > 0$, $m_{NF2} > 0$ (c) $m_{NF1} < 0$, $m_{NF2} > 0$ (d) $m_{NF1} < 0$, $m_{NF2} < 0$

includes two control loop, i.e., control loop-I, control loop-II for controlling two switches S_{T1}, S_{T2}. Each control loop consist of inner current loop and outer voltage loop. Outer voltage loops are formed by feedback gains β_1/β_2 and controllers G_{c1}, G_{c2} which are responsible to generate the reference control signals to inner loops. Inner current loops are formed by two equal current sensing resistances r_s, clock input clk, slope compensation m_{c1}, m_{c2}, comparators CM-I/CM-II and SR flip-flops SR-I/SR-II.

Figure 6.4 show the operating waveforms of PCM controlled CI-SIDO converter for Case A with different patterns of inductor current slopes. The operation of PCM control for Case A is described as follows: At each switching period T_s, clock clk set the SR flip-flop to output high level. Thus, switches S_{T1}, S_{T2} are turned on which causes inductor current i_{L1}, i_{L2} to rise with

slope m_{NN1}, m_{NN2}, respectively. When i_{L2} increases to reference control signal $i^*_{cn2} \equiv v^*_{cn2}/r_s$, the output of comparator resets the SR-II to output low level. Thus, switch S_{T2} is turned off, diode S_{D2} turns on and slope of i_{L2} changes to m_{NF2}. Due to coupling of inductor currents, the slope of i_{L1} also changes to m_{NF1}. Similarly, when i_{L1} increases to reference control signal $i^*_{cn1} \equiv v^*_{cn2}/r_s$, the output of comparator resets the SR-I to output low level. Thus S_{T1} is turned off and S_{D1} is turned on which causes the slope of i_{L1} decrease to m_{FF1}. Due to coupling, the slope of i_{L2} also changes to m_{FF2}.

6.3 Unified Model of Current Modulator

In the PCM controlled converter, the current modulator generates the duty cycle. The current modulator is composed of voltage comparator and SR flip-flop. The duty cycle is generated when the inductor current reaches the reference control signal, as shown in Figure 6.4. Therefore, in PCM control, reference control signal is the control variable and duty cycle is indirectly controlled. Thus, the equation that relates the reference control signal, inductor current and slope compensation at the instant the duty cycle is generated are called the current modulator equation.

6.3.1 Challenge in Deriving Unified Current Modulator Model

In CI-SIDO converter, the inductor current slopes depend on coupled inductor parameters (L_1, L_2, k), input voltage and output voltages as shown in Table 6.1. As a result, various trends of inductor current slopes are observed, as shown in Figure 6.2. It is not practical to derive the current modulator expression for each case, each pattern of inductor current slopes, and design the controller.

6.3.1.1 Solution: Operation of CI-SIDO Converter in Sector 5

To overcome the challenges in deriving the current modulator expression, the coupled inductor parameters are designed such that the reference control signal becomes the same as the peak value of inductor current as shown in Figure 6.5. In this case, deriving the unified current

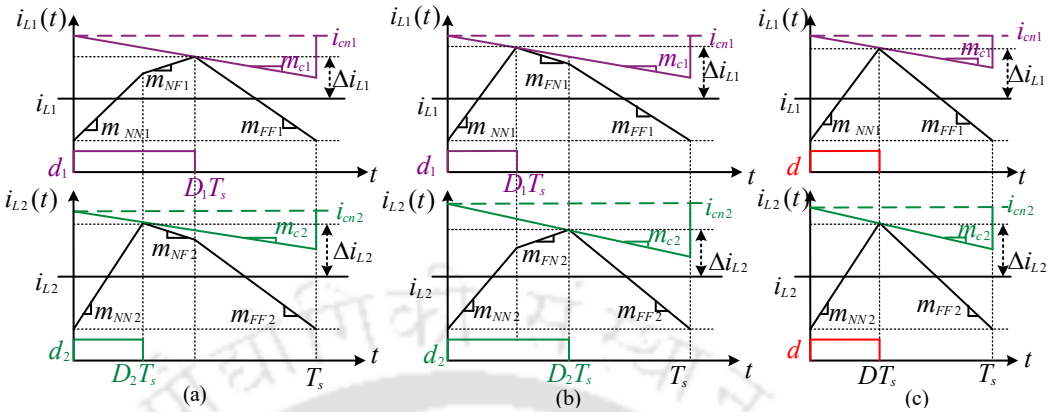


Figure 6.5: Waveform of inductor currents, slope compensation and reference control signal (a) Case A: $D_1 > D_2$ (b) Case B: $D_1 < D_2$ (c) Case C: $D_1 = D_2 = D$

modulator expression for three CI-SIDO converter topologies is easy. Therefore, to obtain the waveform of inductor currents as shown in Figure 6.5 in the range of operating point (D_1, D_2), the coupled inductor parameters (L_1, L_2, k) are designed such that inductor current slopes $m_{NF1} > 0$, $m_{NF2} < 0$, $m_{FN1} < 0$, $m_{FN2} > 0$. In [87], based on the different slopes possibilities of inductor currents, 9 sectors are formed for operation of CI-SIDO converter. As per our requirement of inductor current slopes i.e., $m_{NF1} > 0$, $m_{NF2} < 0$, $m_{FN1} < 0$, $m_{FN2} > 0$, the CI-SIDO converter need to be operated in sector 5 [87]. Thus, the coupled inductor is designed such that the converter operates in sector 5.

6.3.2 Derivation of Unified Current Modulator Model

In order to develop a unified model of current modulator, the duty cycles are expressed in terms of control signals i_{cn1}, i_{cn2}, inductor currents i_{L1}, i_{L2} and effective voltages v_{off1}, v_{off2} which determines the slopes of inductor currents. The effective voltage is the sum of the voltage across switch and diode. Since CI-SIDO converter in steady-state behaves same as a basic single output DC-DC converter, the definition of effective voltage v_{off} proposed in [84] for dc-dc converters can hold good for CI-SIDO converters. Thus, the v_{off1}, v_{off2} is related directly with input voltage v_{in} and output voltages v_{01}, v_{02} as

$$v_{off1} = \alpha_1 v_{in} + \rho_1 v_{01} \quad , \quad v_{off2} = \alpha_2 v_{in} + \rho_2 v_{02} \tag{6.1}$$

where, $\alpha_1, \alpha_2, \rho_1, \rho_2 \in \{0, 1\}$ and for

CI-SIDO buck: $\alpha_1 = \alpha_2 = 1$, $\rho_1 = \rho_2 = 0$

CI-SIDO boost: $\alpha_1 = \alpha_2 = 0$, $\rho_1 = \rho_2 = 1$

CI-SIDO boost and buck: $\alpha_1 = 0$, $\rho_1 = 1$, $\alpha_2 = 1$, $\rho_2 = 0$

Figure 6.5 shows the waveforms of inductor currents i_{L1}, i_{L2} and is considered to derive the current modulator expression in this thesis. The geometry of the waveforms shown in Figure 6.5 provides the fundamental information to obtain the current modulator model. From Figure 6.5 the relation between the reference control current and inductor currents are given by

$$\begin{aligned} i_{cn1} - m_{c1} d_1 T_s &= i_{L1} + \Delta i_{L1} \\ i_{cn2} - m_{c2} d_2 T_s &= i_{L2} + \Delta i_{L2} \end{aligned} \tag{6.2}$$

where, i_{L1}, i_{L2} are the inductor current averaged over switching period, Δi_{L1} is the difference between average, peak value of i_{L1} and similarly Δi_{L2} is the difference between average, peak value of i_{L2}.

Since, the inductor currents averaged over switching period i_{L1}, i_{L2} lies exactly at the middle of the ripple band [88], the Δi_{L1}, Δi_{L2} can be obtained by averaging the area covered by the ripple band.

The expression of Δi_{L1}, Δi_{L2} for Case A is given by

$$\begin{aligned} \Delta i_{L1} &= \frac{T_s}{2} m_{NN1} d_2^2 + \frac{T_s}{2} m_{NF1} (d_1 - d_2)^2 + m_{NN1} d_2 (d_1 - d_2) T_s + \frac{T_s}{2} m_{FF1} (1 - d_1)^2 \\ \Delta i_{L2} &= \frac{T_s}{2} m_{NN2} d_2^2 + \frac{T_s}{2} m_{NF2} (d_1 - d_2)^2 + m_{FF2} (1 - d_1)(d_1 - d_2) T_s + \frac{T_s}{2} m_{FF2} (1 - d_1)^2 \end{aligned} \tag{6.3}$$

Using the expression of slopes given in Table 6.1 in (6.3) and simplifying, the expression of Δi_{L1}, Δi_{L2} for three CI-SIDO converter topologies are calculated and are given as follows:

CI-SIDO buck converter

$$\begin{aligned} \Delta i_{L1} &= \frac{T_s}{2L_1'} (d_1 (1 - d_1) v_{in} + \frac{M}{L_2} d_2 (1 - d_2) v_{in}) \\ \Delta i_{L2} &= \frac{T_s}{2L_2'} (d_2 (1 - d_2) v_{in} + \frac{M}{L_1} d_1 (1 - d_1) v_{in}) \end{aligned} \tag{6.4}$$

CI-SIDO boost converter

$$\begin{aligned}\Delta i_{L1} &= \frac{T_s}{2L_1^{'}}(d_1(1-d_1)v_{01} + \frac{M}{L_2}d_2(1-d_2)v_{02}) \\ \Delta i_{L2} &= \frac{T_s}{2L_2^{'}}(d_2(1-d_2)v_{02} + \frac{M}{L_1}d_1(1-d_1)v_{01})\end{aligned} \tag{6.5}$$

CI-SIDO boost and buck converter

$$\begin{aligned}\Delta i_{L1} &= \frac{T_s}{2L_1^{'}}(d_1(1-d_1)v_{01} + \frac{M}{L_2}d_2(1-d_2)v_{in}) \\ \Delta i_{L2} &= \frac{T_s}{2L_2^{'}}(d_2(1-d_2)v_{in} + \frac{M}{L_1}d_1(1-d_1)v_{01})\end{aligned} \tag{6.6}$$

The expression of Δi_{L1}, Δi_{L2} given in (6.4), (6.5), (6.6) remains same for Case B and Case C as shown in Figure 6.5.

The Δi_{L1}, Δi_{L2} for three converters can be expressed in terms of effective voltage v_{off1}, v_{off2} as given in (6.1) to obtain a unified ripple expression as

$$\begin{aligned}\Delta i_{L1} &= \frac{T_s}{2L_1^{'}}(d_1(1-d_1)v_{off1} + \frac{M}{L_2}d_2(1-d_2)v_{off2}) \\ \Delta i_{L2} &= \frac{T_s}{2L_2^{'}}(d_2(1-d_2)v_{off2} + \frac{M}{L_1}d_1(1-d_1)v_{off1})\end{aligned} \tag{6.7}$$

Using (6.7) in (6.2), the unified current modulator equation of CI-SIDO converter under PCM control can be written as

$$\begin{aligned}i_{cn1} - m_{c1}d_1T_s &= i_{L1} + \frac{T_s}{2L_1^{'}}(d_1d_1^{'}v_{off1} + \frac{M}{L_2}d_2d_2^{'}v_{off2}) \\ i_{cn2} - m_{c2}d_2T_s &= i_{L2} + \frac{T_s}{2L_2^{'}}(d_2d_2^{'}v_{off2} + \frac{M}{L_1}d_1d_1^{'}v_{off1})\end{aligned} \tag{6.8}$$

where, $d_1^{'} = 1 - d_1$, $d_2^{'} = 1 - d_2$

Equation (6.8) is a unified large signal expressions of current modulator which describes how d_1, d_2 are generated. The unified small-signal expressions of current modulator is obtained by applying perturbations and linearisation. Let

$$\begin{aligned}i_{cn1} = I_{cn1} + \hat{i}_{cn1}\ ,\ i_{cn2} = I_{cn2} + \hat{i}_{cn2}\ ,\ i_{L1} = I_{L1} + \hat{i}_{L1}\ ,\ i_{L2} = I_{L2} + \hat{i}_{L2} \\ d_1 = D_1 + \hat{d}_1\ ,\ d_2 = D_2 + \hat{d}_2\ ,\ v_{in} = V_{in} + \hat{v}_{in}\end{aligned} \tag{6.9}$$

Substitution of (6.9) in (6.8) and separating the DC part, first order ac terms and neglecting

the non-linear terms, we obtain the unified steady-state and small-signal current modulator expression. The steady-state expression of current modulator is given by

$$\begin{aligned} I_{cn1} - I_{L1} &= m_{c1} D_1 T_s + \frac{T_s}{2L_1^{'}}(D_1 D_1^{'} V_{off1} + \frac{M}{L_2} D_2 D_2^{'} V_{off2}) \\ I_{cn2} - I_{L2} &= m_{c2} D_2 T_s + \frac{T_s}{2L_2^{'}}(D_2 D_2^{'} V_{off2} + \frac{M}{L_1} D_1 D_1^{'} V_{off1}) \end{aligned} \tag{6.10}$$

The small-signal expression of current modulator is given by

$$\begin{aligned} \hat{i}_{cn1} - \hat{i}_{L1} &= (m_{c1} T_s + \frac{V_{off1}(1-2D_1)}{2L_1^{'}/T_s})\hat{d}_1 + \frac{D_1 D_1^{'}}{2L_1^{'}/T_s}\hat{v}_{off1} + \frac{M V_{off2}(1-2D_2)}{2L_2 L_1^{'}/T_s}\hat{d}_2 + \frac{M D_2 D_2^{'}}{2L_2 L_1^{'}/T_s}\hat{v}_{off2} \\ \hat{i}_{cn2} - \hat{i}_{L2} &= (m_{c2} T_s + \frac{V_{off2}(1-2D_2)}{2L_2^{'}/T_s})\hat{d}_2 + \frac{D_2 D_2^{'}}{2L_2^{'}/T_s}\hat{v}_{off2} \frac{M V_{off1}(1-2D_1)}{2L_1 L_2^{'}/T_s}\hat{d}_1 + \frac{M D_1 D_1^{'}}{2L_1 L_2^{'}/T_s}\hat{v}_{off1} \end{aligned} \tag{6.11}$$

Equation (6.11) can be re-written in matrix form as

$$\begin{bmatrix} \hat{d}_1 \\ \hat{d}_2 \end{bmatrix} = \begin{bmatrix} 2L_1^{'} m_{c1} + V_{off1}(1-2D_1) & \frac{M V_{off2}}{L_2}(1-2D_2) \\ \frac{M V_{off1}}{L_1}(1-2D_1) & 2L_2^{'} m_{c2} + V_{off2}(1-2D_2) \end{bmatrix}^{-1} \times \left(\begin{bmatrix} \frac{2L_1^{'}}{T_s} & 0 \\ 0 & \frac{2L_2^{'}}{T_s} \end{bmatrix} \begin{bmatrix} \hat{i}_{cn1} - \hat{i}_{L1} \\ \hat{i}_{cn2} - \hat{i}_{L2} \end{bmatrix} - \begin{bmatrix} D_1 D_1^{'} & \frac{M D_2 D_2^{'}}{L_2} \\ \frac{M D_1 D_1^{'}}{L_1} & D_2 D_2^{'} \end{bmatrix} \begin{bmatrix} \hat{v}_{off1} \\ \hat{v}_{off2} \end{bmatrix} \right) \tag{6.12}$$

Solving (6.12) we obtain the unified small-signal model of current modulator as

$$\begin{bmatrix} \hat{d}_1 \\ \hat{d}_2 \end{bmatrix} = \begin{bmatrix} f_{m11} & -f_{m12} \\ -f_{m21} & f_{m22} \end{bmatrix} \begin{bmatrix} \hat{i}_{cn1} - \hat{i}_{L1} \\ \hat{i}_{cn2} - \hat{i}_{L2} \end{bmatrix} - \begin{bmatrix} k_{v11} & k_{v12} \\ k_{v21} & k_{v21} \end{bmatrix} \begin{bmatrix} \hat{v}_{off1} \\ \hat{v}_{off2} \end{bmatrix} \tag{6.13}$$

Using (6.1) in (6.13), we can rewrite the unified small-signal model as

$$\begin{bmatrix} \hat{d}_1 \\ \hat{d}_2 \end{bmatrix} = \begin{bmatrix} f_{m11} & -f_{m12} \\ -f_{m21} & f_{m22} \end{bmatrix} \begin{bmatrix} \hat{i}_{cn1} - \hat{i}_{L1} \\ \hat{i}_{cn2} - \hat{i}_{L2} \end{bmatrix} - \begin{bmatrix} k_{v11} & k_{v12} \\ k_{v21} & k_{v21} \end{bmatrix} \begin{bmatrix} \alpha_1 v_{in} + \rho_1 v_{01} \\ \alpha_2 v_{in} + \rho_2 v_{02} \end{bmatrix} \tag{6.14}$$

Where, f_{m11}, f_{m22}, f_{m12}, f_{m21} are the modulator gains and k_{v11}, k_{v12}, k_{v21}, k_{v22} are the feed-forward gains. The expression of modulator and feedforward gains without and with slope compensations are shown in Table 6.2.

Table 6.2: Modulator and feedforward gains

Without Slope compensation

$$f_{m11} = \frac{2L_1/T_s}{V_{off1}(1-2D_1)},\ f_{m12} = \frac{Mf_{m11}}{L_1},\ f_{m22} = \frac{2L_2/T_s}{V_{off2}(1-2D_2)}, f_{m21} = \frac{Mf_{m22}}{L_2},$$

$$k_{v22} = \frac{D_2(1-D_2)}{V_{off2}(1-2D_2)}, k_{v11} = \frac{D_1(1-D_1)}{V_{off1}(1-2D_1)}, k_{v12} = k_{v21} = 0$$

With Slope Compensation

$$f_{m11} = \frac{1/T_s}{m_{c1} + \frac{V_{off1}(1-2D_1)}{2L_1'} - \frac{k^2V_{off2}^2(1-2D_1)(1-2D_2)}{4L_{k1}L_2'(m_{c2} + \frac{V_{off2}(1-2D_2)}{2L_2'})}}, \quad f_{m12} = \frac{\frac{MV_{off2}(1-2D_2)}{2L_2L_1'}f_{m11}}{m_{c2} + \frac{V_{off2}(1-2D_2)}{2L_2'}}$$

$$f_{m22} = \frac{1/T_s}{m_{c2} + \frac{V_{off2}(1-2D_2)}{2L_2'} - \frac{k^2V_{off1}^2(1-2D_1)(1-2D_2)}{4L_{k1}L_2'(m_{c1} + \frac{V_{off1}(1-2D_1)}{2L_1'})}}, \quad f_{m21} = \frac{\frac{MV_{off1}(1-2D_1)}{2L_1L_{k2}}f_{m22}}{m_{c1} + \frac{V_{off1}(1-2D_1)}{2L_1'}}$$

$$k_{v11} = \frac{T_sD_1D_1'}{2L_1'}f_{m11}\left(1 - \frac{k^2V_{off2}(1-2D_2)}{2L_2'm_{c2} + V_{off2}(1-2D_2)}\right), k_{v22} = \frac{T_sD_2D_2'}{2L_2'}f_{m22}\left(1 - \frac{k^2V_{off1}(1-2D_1)}{2L_1'm_{c1} + V_{off1}(1-2D_1)}\right)$$

$$k_{v12} = \frac{T_sMD_2D_2'}{2L_2L_1'}f_{m11}\left(1 - \frac{V_{off2}(1-2D_2)}{2L_2'm_{c2} + V_{off2}(1-2D_2)}\right), k_{v21} = \frac{T_sMD_1D_1'}{2L_2L_1'}f_{m22}\left(1 - \frac{V_{off1}(1-2D_1)}{2L_1'm_{c1} + V_{off1}(1-2D_1)}\right)$$

where,
For CI-SIDO buck converter: $V_{off1} = V_{off2} = V_{in}$
For CI-SIDO boost converter: $V_{off1} = V_{01}$, $V_{off2} = V_{02}$
For CI-SIDO boost and buck converter: $V_{off1} = V_{01}$, $V_{off2} = V_{in}$

6.4 Unified Model of Peak Current Mode Controlled CI-SIDO Converter

The small-signal model of peak current mode (PCM) controlled CI-SIDO converter is essential for designing the controller and slope compensation. Moreover, using the small-signal model the converter performance parameter like audio-susceptibility, output impedance can be calculated. The small-signal model of PCM controlled CI-SIDO converter is formed by interfacing the unified small-signal model of current modulator with small-signal model of CI-SIDO converter derived in Chapter 2. Figure 6.6 shows the unified small-signal block diagram model for PCM controlled CI-SIDO converter with only inner loop closed.

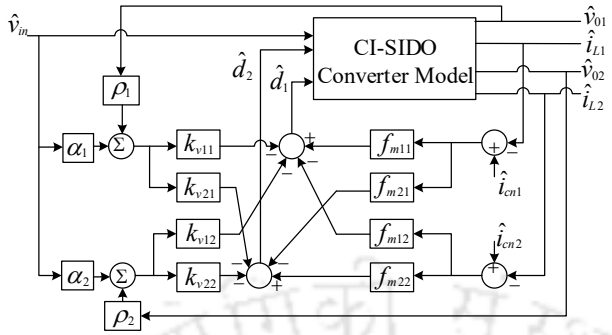


Figure 6.6: Unified model of peak current mode controlled CI-SIDO converters

Table 6.3: Parameters of CI-SIDO converter

CI-SIDO Buck converter					
Parameter	V_{in}	R_1, R_2	L_1, L_2, M	C_1, C_2	f_s
values	10 V	5 Ω 5 Ω	112 μH, 70 μH, 40 μH	320 μF, 320 μF	100 kHz
CI-SIDO Boost converter					
values	5 V	15 Ω 15 Ω	112 μH, 70 μH, 40 μH	220 μF, 320 μF	100 kHz
CI-SIDO Boost and buck converter					
values	5 V	15 Ω 3 Ω	112 μH, 70 μH, 40 μH	320 μF, 320 μF	100 kHz

6.4.1 Small-signal Model of PCM Controlled CI-SIDO Buck Converter

The circuit diagram of PCM controlled CI-SIDO buck converter with only inner loop is shown in Figure 6.7(a) and its small-small model is shown in Figure 6.7(b). The state-space model of CI-SIDO buck converter shown in Figure 6.7(b) is already derived in chapter 2 and considering ideal condition is given by

$$\frac{d}{dt}\begin{bmatrix}\hat{i}_{L1}\\ \hat{i}_{L2}\\ \hat{v}_{01}\\ \hat{v}_{02}\end{bmatrix} = \begin{bmatrix}0 & 0 & -\frac{1}{L_{k1}} & -\frac{M}{L_2L_{k1}}\\ 0 & 0 & -\frac{M}{L_1L_{k2}} & -\frac{1}{L_{k2}}\\ \frac{1}{C_1} & 0 & -\frac{1}{C_1R_1} & 0\\ 0 & \frac{1}{C_2} & 0 & -\frac{1}{C_2R_2}\end{bmatrix}\begin{bmatrix}\hat{i}_{L1}\\ \hat{i}_{L2}\\ \hat{v}_{01}\\ \hat{v}_{02}\end{bmatrix} + \begin{bmatrix}\frac{(D_1+\frac{M}{L_2}D_2)}{L_{k1}}\\ \frac{(D_2+\frac{M}{L_1}D_1)}{L_{k2}}\\ 0\\ 0\end{bmatrix}\begin{bmatrix}\hat{v}_{in}\end{bmatrix} + \begin{bmatrix}\frac{V_{in}}{L_{k1}} & \frac{MV_{in}}{L_2L_{k1}}\\ \frac{MV_{in}}{L_1L_{k2}} & \frac{V_{in}}{L_{k2}}\\ 0 & 0\\ 0 & 0\end{bmatrix}\begin{bmatrix}\hat{d}_1\\ \hat{d}_2\end{bmatrix} \tag{6.15}$$

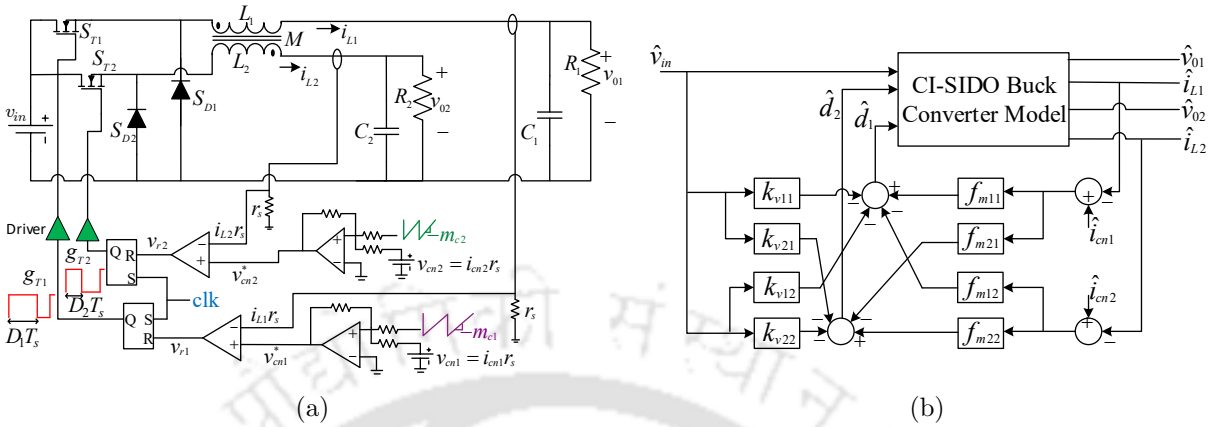


Figure 6.7: Peak current mode controlled CI-SIDO buck converters with only inner loops closed (a) Circuit diagram (b) Small-signal model

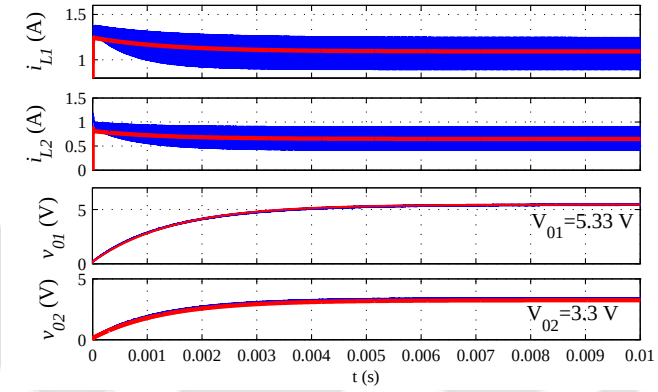


Figure 6.8: Simulation response of inductor currents, output voltages at $I_{cn1} = 1.4$ A, $I_{cn2} = 1$ A (circuit simulation (in blue), small-signal model simulation (in red))- PCM controlled CI-SIDO buck converter

6.4.1.1 Simulation Verification

The developed small-signal model of PCM controlled CI-SIDO buck converter with inner loops closed as shown in Figure 6.7 is validated using simulation results. The simulation is performed in MATLAB SIMULINK environment. The converter parameter used in simulation are shown in Table 6.3 and slope compensation considered are $m_{c1} = m_{c2} = 27000$ V/s.

Figure 6.8 shows the simulation response of linear small-signal model and non-linear circuit model for reference control inputs $i_{cn1} = 1.4$ A, $i_{cn2} = 1$ A. It can be seen from Figure 6.8 that the response of small-signal model matches with the switching circuit model almost perfectly.

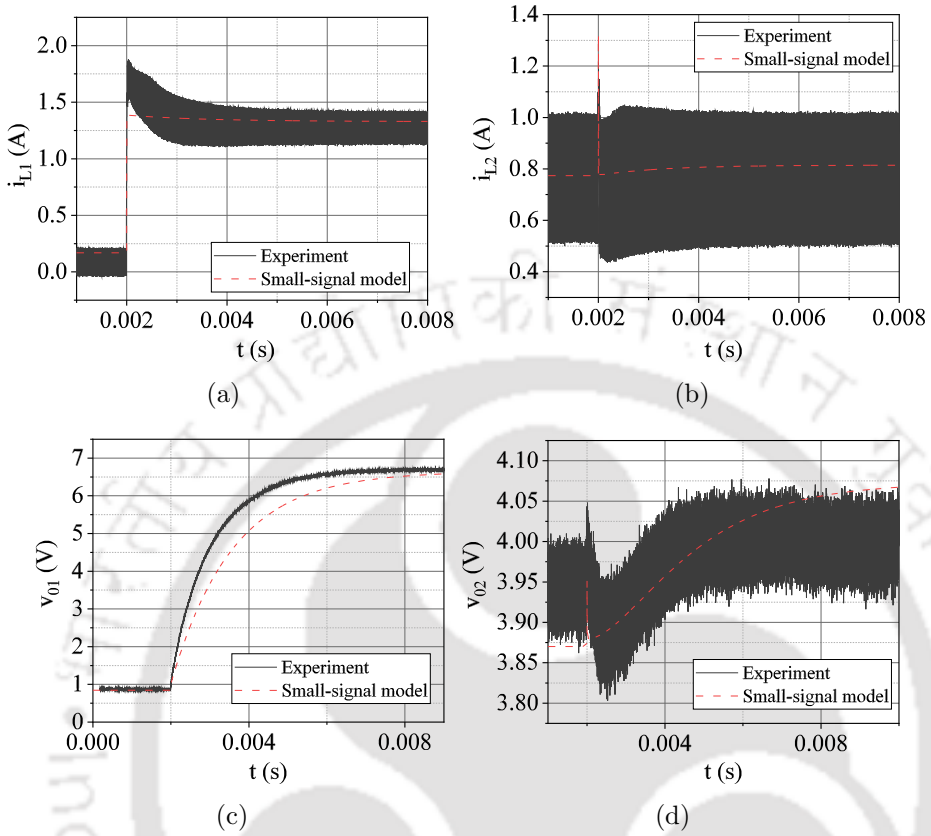


Figure 6.9: Experimental and small-signal response of inductor currents and output voltages for step change in I_{cn1} from 0.38 A to 1.6 A keeping $I_{cn2} = 1.2$ A - PCM controlled CI-SIDO buck converter

The maximum error in the output voltage response of the small-signal model is approximately equal to the voltage ripple.

6.4.1.2 Experimental Verification

The small-signal model is experimentally verified on a custom-build prototype of CI-SIDO buck converter under PCM control with only inner loops closed. The converter parameter used in experiment is same as that used in simulation. Figure 6.9 shows the experimental and small-signal response of inductor currents and output voltages for step change in reference control signal I_{cn1} from 0.38 A to 1.6 A keeping $I_{cn2} = 1.2$ A. It is observed that small-signal model satisfactorily predicts the steady-state and transient state behaviour of the experimental prototype. The maximum error between small-signal average model and experiment is less than 5%.

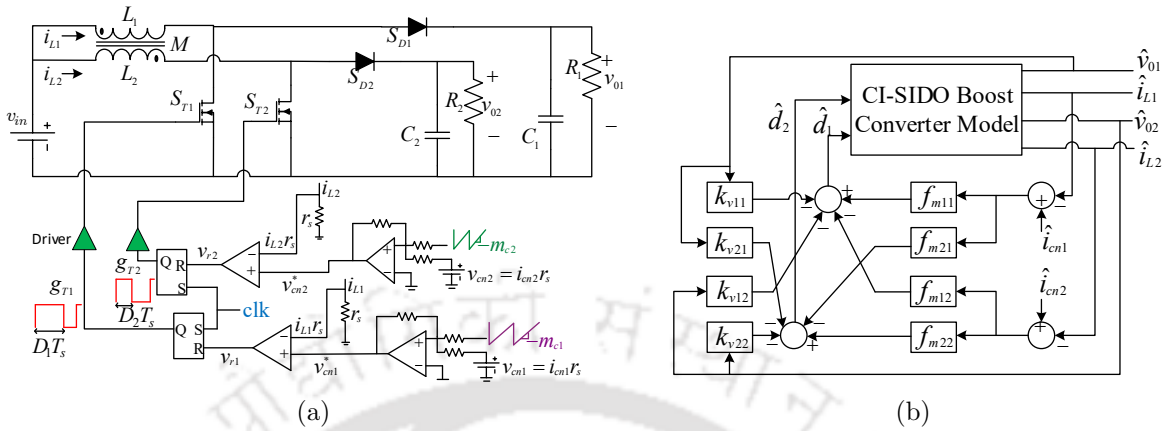


Figure 6.10: Peak current mode controlled CI-SIDO boost converters with only inner loops closed (a) Circuit diagram (b) Small-signal model

6.4.2 Small-signal Model of PCM Controlled CI-SIDO Boost Converter

The circuit diagram of PCM controlled CI-SIDO boost converter with only inner loop is shown in Figure 6.10(a) and its small-small model is shown in Figure 6.10(b). The state-space model of CI-SIDO boost converter shown in Figure 6.10(b) is derived in chapter 2 and is given by

$$\frac{d}{dt}\begin{bmatrix}\hat{i}_{L1}\\ \hat{i}_{L2}\\ \hat{v}_{01}\\ \hat{v}_{02}\end{bmatrix}=\begin{bmatrix}0 & 0 & \frac{-(1-D_1)}{L_1'} & \frac{-M(1-D_2)}{L_2L_1'}\\ 0 & 0 & \frac{-M(1-D_1)}{L_1L_2'} & \frac{-(1-D_2)}{L_2'}\\ \frac{1-D_1}{C_1} & 0 & \frac{-1}{C_1R_1} & 0\\ 0 & \frac{1-D_2}{C_2} & 0 & \frac{-1}{C_2R_2}\end{bmatrix}\begin{bmatrix}\hat{i}_{L1}\\ \hat{i}_{L2}\\ \hat{v}_{01}\\ \hat{v}_{02}\end{bmatrix}+\begin{bmatrix}\frac{(1+\frac{M}{L_2})}{L_1'}\\ \frac{(1+\frac{M}{L_1})}{L_2'}\\ 0\\ 0\end{bmatrix}\begin{bmatrix}\hat{v}_{in}\end{bmatrix}+\begin{bmatrix}\frac{V_{01}}{L_1'} & \frac{MV_{02}}{L_2L_1'}\\ \frac{MV_{01}}{L_1L_2'} & \frac{V_{02}}{L_2'}\\ \frac{-I_{L1}}{C_1} & 0\\ 0 & \frac{-I_{L2}}{C_2}\end{bmatrix}\begin{bmatrix}\hat{d}_1\\ \hat{d}_2\end{bmatrix} \tag{6.16}$$

6.4.2.1 Simulation Verification

The small-signal model of PCM controlled CI-SIDO boost converter with inner loops closed as shown in Figure 6.10 is validated using simulation results. The converter parameters used in simulation is shown in Table 6.3 and slope compensations considered are $m_{c1} = m_{c2} = 35000$ V/s. Figure 6.11 shows the simulation response for step change in i_{cn1} from 1 A to 1.7 A keeping

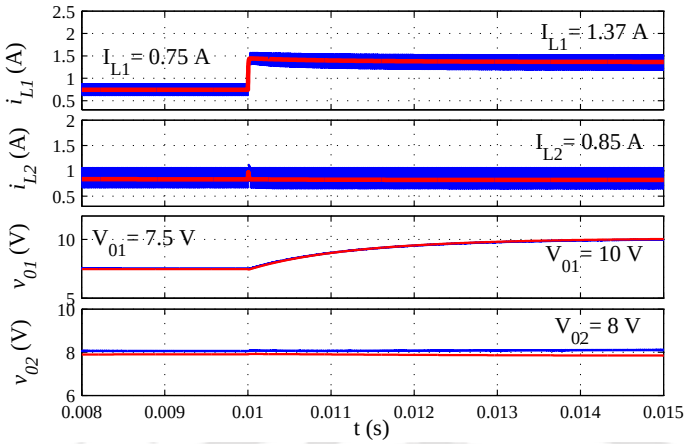


Figure 6.11: Simulation response of inductor currents, output voltages for step change in I_{cn1} from 1 A to 1.7 A and $I_{cn2} = 1.2$ A (circuit simulation (in blue), small-signal model simulation (in red)) - PCM controlled CI-SIDO boost converter

$i_{cn2} = 1.2$ A. When i_{cn1} is changed from 1 A to 1.7 A keeping $i_{cn2} = 1.2$ A, I_{L1} changes from 0.75 A to 1.35 A with $I_{L2} = 0.85$ A, V_{01} change from 7.5 V to 10 V with $V_{02} = 8$ V. It is observed that the response of small-signal model matches with the switching circuit model almost perfectly. The maximum error in the steady-state output voltage response of the small-signal model is less than 5%.

6.4.2.2 Experimental Verification

The small-signal model is experimentally verified on a custom-build prototype of CI-SIDO boost converter under PCM control with only inner loops closed. The converter parameter used in experiment is same as that used in simulation. Figure 6.12 shows the experimental and small-signal response of inductor currents and output voltages for step change in reference control signal I_{cn1} from 0.5 A to 2.2 A keeping $I_{cn2} = 1.3$ A. It is observed that small-signal model satisfactorily predicts the steady-state and transient state behaviour of the experimental prototype. The maximum error between steady-state small-signal average model and experiment is less than 5%.

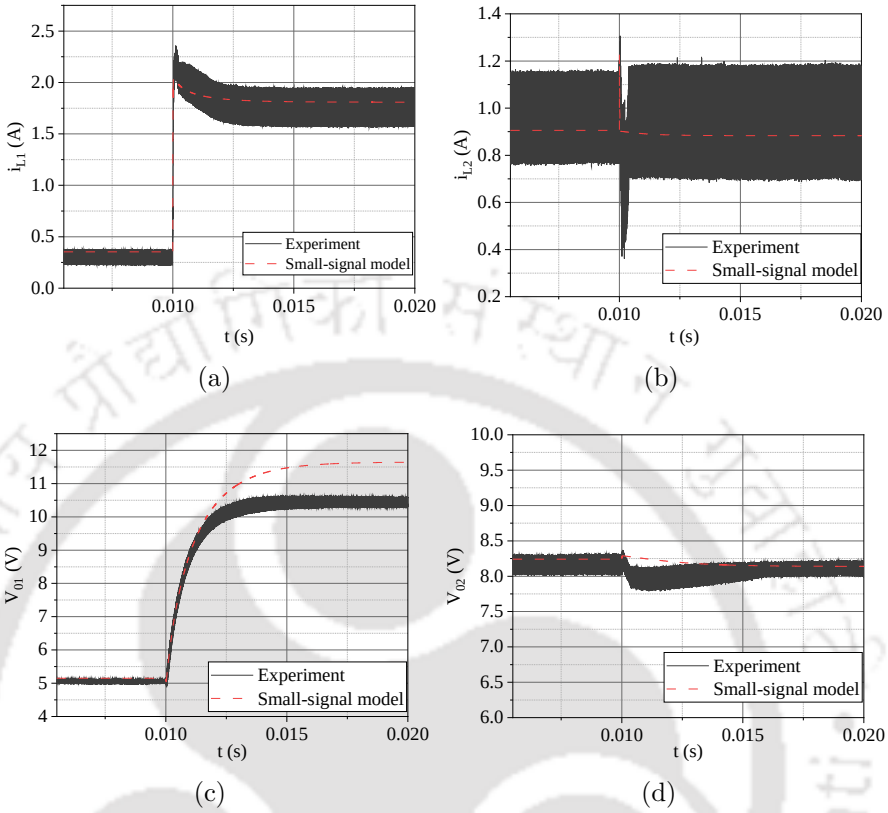


Figure 6.12: Experimental and small-signal response of inductor currents and output voltages for step change in I_{cn1} from 0.5 A to 2.2 A keeping I_{cn2} = 1.3 A - PCM controlled CI-SIDO boost converter

6.4.3 Small-signal Model of PCM Controlled CI-SIDO Boost and Buck Converter

The circuit diagram of PCM controlled CI-SIDO boost and buck converter with only inner loop is shown in Figure 6.13(a) and its small-small model is shown in Figure 6.13(b). The state-space model of CI-SIDO boost and buck converter shown in Figure 6.13(b) is derived in chapter 2 and is given by

$$\frac{d}{dt}\begin{bmatrix}\hat{i}_{L1}\\ \hat{i}_{L2}\\ \hat{v}_{01}\\ \hat{v}_{02}\end{bmatrix} = \begin{bmatrix}0 & 0 & -\frac{(1-D_1)}{L_1'} & -\frac{M}{L_2L_1'}\\ 0 & 0 & -\frac{M(1-D_1)}{L_1L_2'} & -\frac{1}{L_2'}\\ \frac{1-D_1}{C_1} & 0 & -\frac{1}{C_1R_1} & 0\\ 0 & \frac{1}{C_2} & 0 & -\frac{1}{C_2R_2}\end{bmatrix}\begin{bmatrix}\hat{i}_{L1}\\ \hat{i}_{L2}\\ \hat{v}_{01}\\ \hat{v}_{02}\end{bmatrix} + \begin{bmatrix}\frac{(1+\frac{MD_2}{L_2})}{L_1'}\\ \frac{(D_2+\frac{M}{L_1})}{L_2'}\\ 0\\ 0\end{bmatrix}\begin{bmatrix}\hat{v}_{in}\end{bmatrix} + \begin{bmatrix}\frac{V_{01}}{L_1'} & \frac{MV_{in}}{L_2L_1'}\\ \frac{MV_{01}}{L_1L_2'} & \frac{V_{in}}{L_2'}\\ \frac{-I_{L1}}{C_1} & 0\\ 0 & 0\end{bmatrix}\begin{bmatrix}\hat{d}_1\\ \hat{d}_2\end{bmatrix} \tag{6.17}$$

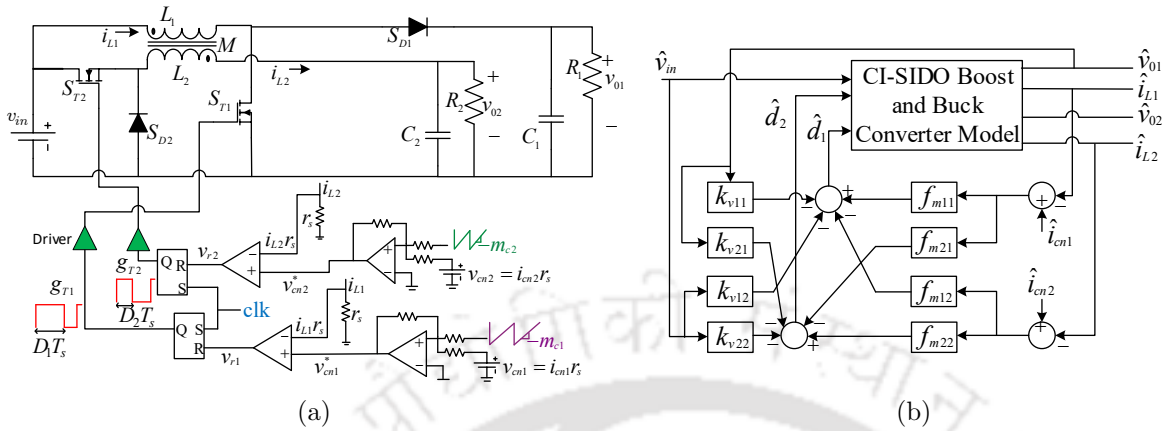


Figure 6.13: Peak current mode controlled CI-SIDO boost and buck converters with only inner loops closed (a) Circuit diagram (b) Small-signal model

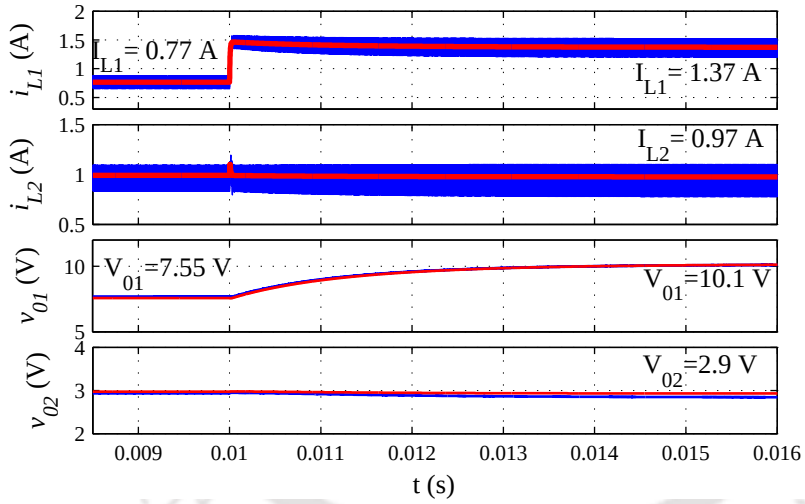


Figure 6.14: Simulation response of inductor currents, output voltages for step change in I_{cn1} from 1 A to 1.7 A and $I_{cn2} = 1.3$ A (circuit simulation (in blue), small-signal model simulation (in red))-PCM controlled CI-SIDO boost and buck converter

6.4.3.1 Simulation Verification

The small-signal model of PCM controlled CI-SIDO boost and buck converter with inner loops closed as shown in Figure 6.13 is validated using simulation results. The converter parameters used in simulation are shown in Table 6.3 and slope compensations considered are $m_{c1} = m_{c2} = 35000$ V/s. Figure 6.14 shows the simulation response for step change in i_{cn1} from 1 A to 1.7 A keeping $i_{cn2} = 1.3$ A. When i_{cn1} is changed from 1 A to 1.7 A keeping $i_{cn2} = 1.3$ A, I_{L1} changes from 0.77 A to 1.37 A with $I_{L2} = 0.97$ A, V_{01} change from 7.55 V to 10.1 V with

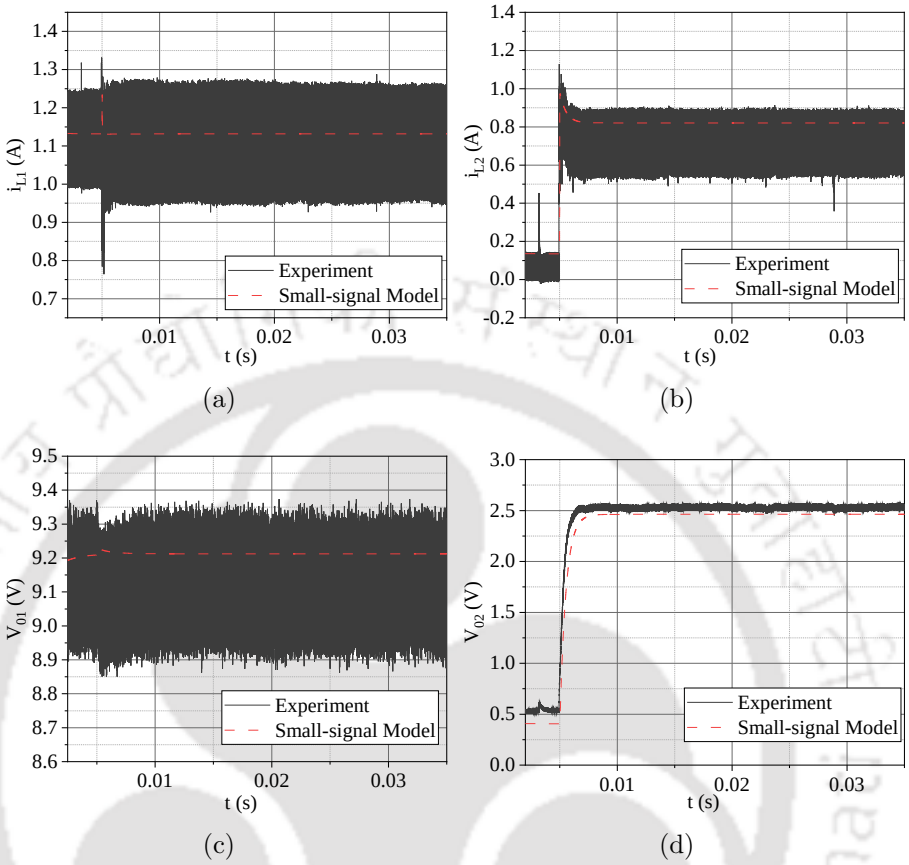


Figure 6.15: Experimental and small-signal response of inductor currents and output voltages for step change in I_{cn2} from 0.35 A to 1.2 A keeping $I_{cn1} = 1.5$ A - PCM controlled CI-SIDO boost and buck converter

$V_{02} = 2.9$ V. It is observed that the response of small-signal model matches with the switching circuit model almost perfectly. The maximum error in the steady-state output voltage response of the small-signal model is less than 3%.

6.4.3.2 Experimental Verification

The small-signal model of CI-SIDO boost and buck converter under PCM control with only inner loops closed is experimentally verified as shown in Figure 6.15. The converter parameter used in experiment is same as that used in simulation. Figure 6.15 shows the experimental and small-signal response of inductor currents and output voltages for step change in reference control signal I_{cn2} from 0.35 A to 1.2 A keeping $I_{cn1} = 1.5$ A. It is observed that small-signal model satisfactorily predicts the steady-state and transient state behaviour of the

experimental prototype. The maximum error between steady-state small-signal average model and experiment is less than 5%.

6.5 Inner Loop Instability of PCM Controlled CI-SIDO Converter

The inner loop of PCM controlled converter without slope compensation becomes unstable or exhibit sub-harmonic oscillation when duty cycle is greater that 0.5. The inner loop instability can be predicted using the developed unified small signal model of PCM controlled CI-SIDO converter and is discussed in the following subsections for three CI-SIDO converter topologies.

6.5.1 Inner Loop Instability for PCM Control of CI-SIDO Buck Converter

The small-signal model of current modulator without slope-compensation for CI-SIDO buck converter is obtained from (6.11) using $m_{c1} = m_{c2} = 0$, $V_{off1} = V_{off2} = V_{in}$, $\hat{v}_{off1} = \hat{v}_{off2} = \hat{v}_{in}$ and is given by

$$\begin{bmatrix} \hat{d}_1 \\ \hat{d}_2 \end{bmatrix} = \begin{bmatrix} \frac{-2L_1}{T_s V_{in}(1-2D_1)} & \frac{2M}{T_s V_{in}(1-2D_1)} \\ \frac{2M}{T_s V_{in}(1-2D_2)} & \frac{-2L_2}{T_s V_{in}(1-2D_2)} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \end{bmatrix} + \begin{bmatrix} \frac{2L_1}{T_s V_{in}(1-2D_1)} & \frac{-2M}{T_s V_{in}(1-2D_1)} \\ \frac{-2M}{T_s V_{in}(1-2D_2)} & \frac{2L_2}{T_s V_{in}(1-2D_2)} \end{bmatrix} \begin{bmatrix} \hat{i}_{cn1} \\ \hat{i}_{cn2} \end{bmatrix} - \begin{bmatrix} \frac{D_1(1-D_1)}{V_{in}(1-2D_1)} \\ \frac{D_2(1-D_2)}{V_{in}(1-2D_2)} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \end{bmatrix} \quad (6.18)$$

Using (6.18) in (6.15), we obtain the complete state-space model of PCM controlled CI-SIDO buck converter with inner loops closed and is written as

$$\frac{d}{dt} \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{v}_{01} \\ \hat{v}_{02} \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} & a_{13} & a_{14} \\ a_{21} & a_{22} & a_{23} & a_{24} \\ a_{31} & 0 & a_{33} & 0 \\ 0 & a_{42} & 0 & a_{44} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{v}_{01} \\ \hat{v}_{02} \end{bmatrix} + \begin{bmatrix} b_{11} & b_{12} & b_{13} \\ b_{21} & b_{22} & b_{23} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_{cn1} \\ \hat{i}_{cn2} \end{bmatrix} \quad (6.19)$$

where,

$$a_{11} = \frac{-2}{T_s(1-k^2)}\left(\frac{1}{1-2D_1} - \frac{k^2}{1-2D_2}\right),\ a_{12} = \frac{2M}{T_s L_1'}\left(\frac{1}{1-2D_1} - \frac{1}{1-2D_2}\right),\ a_{13} = \frac{-1}{L_1'},\ a_{14} = \frac{-M}{L_2 L_1'}$$

$$a_{21} = \frac{2M}{T_s L_2'}\left(\frac{1}{1-2D_2} - \frac{1}{1-2D_1}\right),\ a_{22} = \frac{-2}{T_s(1-k^2)}\left(\frac{1}{1-2D_2} - \frac{k^2}{1-2D_1}\right),\ a_{23} = \frac{-M}{L_1 L_2'},\ a_{24} = \frac{-1}{L_2'}$$

$$a_{31} = \frac{1}{C_1},\ a_{33} = \frac{-1}{C_1 R_1},\ a_{42} = \frac{1}{C_2},\ a_{44} = \frac{-1}{C_2 R_2} \tag{6.20}$$

$$b_{11} = \frac{1}{L_1'}\left(\frac{D_1(1-D_1)}{1-2D_1} + \frac{MD_2(1-D_2)}{L_2(1-2D_2)}\right),\ b_{21} = \frac{1}{L_2'}\left(\frac{D_2(1-D_2)}{1-2D_2} + \frac{MD_1(1-D_1)}{L_1(1-2D_1)}\right)$$

$$b_{12} = -a_{11},\ b_{13} = -a_{12},\ b_{22} = -a_{21},\ b_{23} = -a_{22}$$

Stability of the system depends on the eigenvalues of **A**, i.e., the roots of the characteristic polynomial det(sI - **A**).

$$det(sI - \mathbf{A}) = s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0 \tag{6.21}$$

where,

$$a_3 = \frac{1}{C_2 R_2} + \frac{1}{C_1 R_1} + \frac{2}{T_s}\left(\frac{1}{1-2D_1} + \frac{1}{1-2D_2}\right)$$

$$a_2 = \frac{1}{C_1 L_1'} + \frac{1}{C_2 L_2'} + \frac{1}{C_1 C_2 R_1 R_2} + \left(\frac{1}{C_2 R_2} + \frac{1}{C_1 R_1}\right)\left(\frac{2}{T_s}\left(\frac{1}{1-2D_1} + \frac{1}{1-2D_2}\right)\right) + \frac{4}{T_s^2}\left(\frac{1}{(1-2D_1)(1-2D_2)}\right)$$

$$a_1 = \frac{1}{L_1' C_1 C_2 R_2} + \frac{1}{L_2' C_1 C_2 R_1} + \frac{2}{T_s L_2' C_2}\left(\frac{1}{1-2D_1}\right) + \frac{2}{T_s L_1' C_1}\left(\frac{1}{1-2D_2}\right) + \frac{2}{T_s R_1 R_2 C_1 C_2}\left(\frac{1}{1-2D_1} + \frac{1}{1-2D_2}\right)$$

$$a_0 = \frac{1}{L_1 L_2' C_1 C_2} + \frac{2}{T_s L_2' C_1 C_2 R_1}\left(\frac{1}{1-2D_1}\right) + \frac{2}{T_s L_1' C_1 C_2 R_2}\left(\frac{1}{1-2D_2}\right) + \frac{4}{T_s^2 L_1' C_1 C_2 R_2 R_1}\left(\frac{1}{(1-2D_1)(1-2D_2)}\right)$$

Necessary and sufficient condition of stability is that all coefficients of the characteristic equation must have positive sign. Note that the coefficients of the characteristic equation become negative for $D_1 > 0.5$ or $D_2 > 0.5$ or $D_1 > 0.5$ and $D_2 > 0.5$. For Example, considering the circuit parameters shown in Table 6.3 the coefficients of the characteristic equation are found for three cases as:

Case 1: $D_1 = 0.52$, $D_2 = 0.3$, the coefficients of the characteristic equation are found as: $a_3 = -4.49 * 10^6$, $a_2 = -2.5 * 10^{12}$, $a_1 = -3.389 * 10^{15}$, $a_0 = -1.139 * 10^{18}$

Case 2: $D_1 = 0.4$, $D_2 = 0.6$, the coefficients of the characteristic equation are found as: $a_3 = 1250$, $a_2 = -9.999 * 10^{12}$, $a_1 = -1.228 * 10^{15}$, $a_0 = -3.759 * 10^{17}$

Case 3: $D_1 = 0.55$, $D_2 = 0.6$, the coefficients of the characteristic equation are found as: $a_3 = -2.998 * 10^6$, $a_2 = 1.996 * 10^{12}$, $a_1 = 2.351 * 10^{15}$, $a_0 = 6.907 * 10^{17}$

This confirms that instability in PCM controlled CI-SIDO buck converter occurs when both duty ratios (D_1, D_2) or any one duty ratio is greater than 0.5.

6.5.1.1 Simulation Verification

The instability of inner loop is validated using simulation results. The CI-SIDO buck converter parameter used in simulation are shown in Table 6.3. Figure 6.16 shows the simulated waveform of reference current i_{cn1}, i_{cn2}, sensed inductor currents i_{L1}, i_{L2}, gate pulses and output voltages v_{01}, v_{02} which is obtained for different duty cycles.

Figure 6.16(a) shows the simulation results which is obtained at duty ratios $D_1 = 0.48$, $D_2 = 0.33$. It is observed that as $D_1 < 0.5$, $D_2 < 0.5$ the waveform of inductor currents are stable.

Figure 6.16(b) shows the simulation results obtained for duty cycles $D_1 = 0.66$, $D_2 = 0.33$. It is observed that as $D_1 > 0.5$, i_{L1} become unstable and due to the coupling i_{L2} also became unstable. Similarly, Figure 6.16(c) shows the results obtained for $D_1 = 0.3$, $D_2 = 0.66$ and is observed that as $D_2 > 0.5$, i_{L2} exhibits sub-harmonic oscillation and due to coupling sub-harmonic oscillation is also observed in i_{L1}. Thus, as predicted the inductor current waveforms show sub-harmonic oscillation for any one duty cycle greater than 0.5.

Figure 6.16(d) shows the simulation results obtained for $D_1 = 0.66$, $D_2 = 0.54$. It is seen that the inductor current waveforms are unstable, i.e., show sub-harmonic oscillations. Thus, as predicted the inductor current waveforms show sub-harmonic oscillation for $D_1 > 0.5$ and $D_2 > 0.5$.

6.5.1.2 Experimental Verification

The instability of inner current loop is validated experimentally as shown in Figure 6.17. The CI-SIDO buck converter parameter used in experiment is same as used in simulation. Figure 6.17(a) shows the stable waveform of inductor currents for $D_1 = 0.4$, $D_2 = 0.2$. Figure 6.17(b) shows the marginal stable waveform of inductor currents for $D_1 = 0.24$, $D_2 = 0.5$. Figure 6.17(c) shows the unstable waveform of inductor currents for $D_1 = 0.6$, $D_2 = 0.3$.

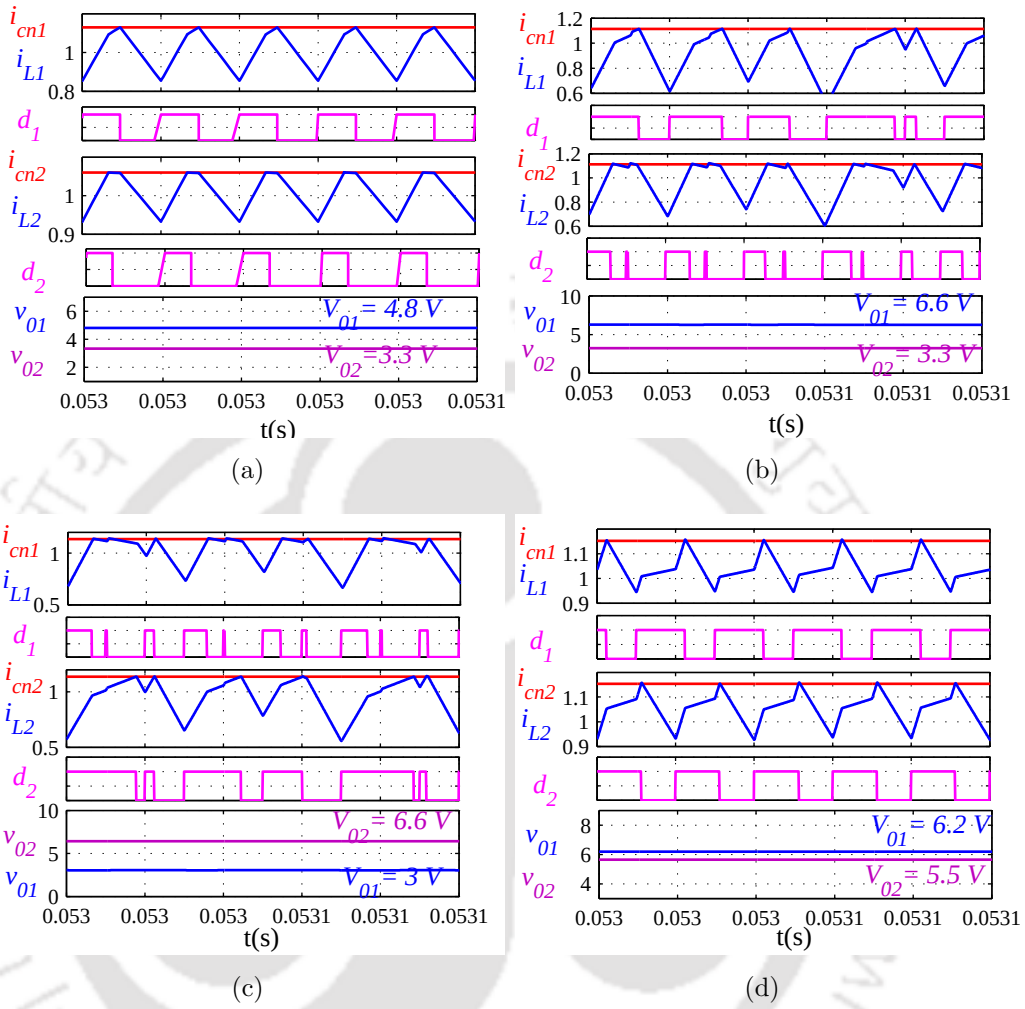


Figure 6.16: Simulation results of PCM controlled CI-SIDO buck converter with inner loops closed (a) $D_1 = 0.48$, $D_2 = 0.33$ (b) $D_1 = 0.66$, $D_2 = 0.33$ (c) $D_1 = 0.3$, $D_2 = 0.66$ (d) $D_1 = 0.66$, $D_2 = 0.54$

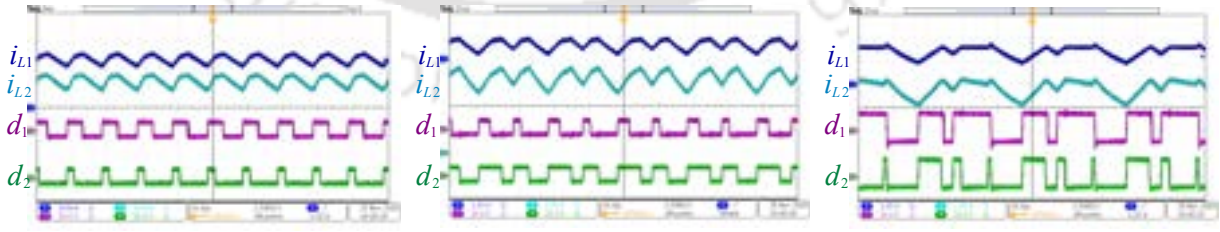


Figure 6.17: Waveform of inductor currents and duty cycles of PCM control CI-SIDO buck with inner loop close (a) Case 1: $D_1 < 0.5$, $D_2 < 0.5$ stable (b) Case 2: $D_1 < 0.5$, $D_2 = 0.5$ marginal stable (c) Case 3: $D_1 > 0.5$, $D_2 < 0.5$ unstable

6.5.2 Inner Loop Instability for PCM Control of CI-SIDO Boost Converter

The small-signal model of current modulator without slope-compensation for CI-SIDO boost converter is obtained from (6.11) using $m_{c1} = m_{c2} = 0$, $V_{off1} = V_{01}$, $V_{off2} = V_{02}$, $\hat{v}_{off1} = \hat{v}_{01}$, $\hat{v}_{off2} = \hat{v}_{02}$ and is given by

$$\begin{bmatrix}\hat{d}_1\\ \hat{d}_2\end{bmatrix} = \begin{bmatrix}\frac{-2L_1}{T_sV_{01}(1-2D_1)} & \frac{2M}{T_sV_{01}(1-2D_1)}\\ \frac{2M}{T_sV_{02}(1-2D_2)} & \frac{-2L_2}{T_sV_{02}(1-2D_2)}\end{bmatrix}\begin{bmatrix}\hat{i}_{L1}\\ \hat{i}_{L2}\end{bmatrix} + \begin{bmatrix}\frac{2L_1}{T_sV_{01}(1-2D_1)} & \frac{-2M}{T_sV_{01}(1-2D_1)}\\ \frac{-2M}{T_sV_{02}(1-2D_2)} & \frac{2L_2}{T_sV_{02}(1-2D_2)}\end{bmatrix}\begin{bmatrix}\hat{i}_{cn1}\\ \hat{i}_{cn2}\end{bmatrix} - \begin{bmatrix}\frac{D_1(1-D_1)}{V_{01}(1-2D_1)} & 0\\ 0 & \frac{D_2(1-D_2)}{V_{02}(1-2D_2)}\end{bmatrix}\begin{bmatrix}\hat{v}_{01}\\ \hat{v}_{02}\end{bmatrix} \tag{6.22}$$

Using (6.22) in (6.16), we can obtain the complete state-space model of PCM controlled CI-SIDO boost converter with inner loops closed. The **A** matrix of the complete state-space model is given by

$$A = \begin{bmatrix}a_{11} & a_{12} & a_{13} & a_{14}\\ a_{21} & a_{22} & a_{23} & a_{24}\\ a_{31} & a_{32} & a_{33} & 0\\ a_{41} & a_{42} & 0 & a_{44}\end{bmatrix} \tag{6.23}$$

where,

$$\begin{aligned} a_{11} &= \tfrac{-2}{T_s(1-k^2)}\left(\tfrac{1}{1-2D_1} - \tfrac{k^2}{1-2D_2}\right),\ a_{12} = \tfrac{2M}{T_sL_1'}\left(\tfrac{1}{1-2D_1} - \tfrac{1}{1-2D_2}\right)\\ a_{13} &= \tfrac{-(1-D_1)}{L_1'} - \tfrac{D_1(1-D_1)}{L_1'(1-2D_1)},\ a_{14} = \tfrac{-M(1-D_2)}{L_2L_1'} - \tfrac{MD_2(1-D_2)}{L_2L_1'(1-2D_2)}\\ a_{21} &= \tfrac{2M}{T_sL_2'}\left(\tfrac{1}{1-2D_2} - \tfrac{1}{1-2D_1}\right),\ a_{22} = \tfrac{-2}{T_s(1-k^2)}\left(\tfrac{1}{1-2D_2} - \tfrac{k^2}{1-2D_1}\right)\\ a_{23} &= \tfrac{-M(1-D_1)}{L_1L_2'} - \tfrac{MD_1(1-D_1)}{L_1L_2'(1-2D_1)},\ a_{24} = \tfrac{-(1-D_2)}{L_2'} - \tfrac{D_2(1-D_2)}{L_2'(1-2D_2)}\\ a_{31} &= \tfrac{(1-D_1)}{C_1} + \tfrac{2I_{L1}L_1}{T_sC_1V_{01}(1-2D_1)},\ a_{32} = \tfrac{-2I_{L1}M}{T_sC_1V_{01}(1-2D_1)},\ a_{33} = \tfrac{I_{L1}D_1(1-D_1)}{C_1V_{01}(1-2D_1)} - \tfrac{1}{C_1R_1}\\ a_{41} &= \tfrac{-2I_{L2}M}{T_sC_2V_{02}(1-2D_2)},\ a_{42} = \tfrac{(1-D_2)}{C_2} + \tfrac{2I_{L2}L_2}{T_sC_2V_{02}(1-2D_2)},\ a_{44} = \tfrac{I_{L2}D_2(1-D_2)}{C_2V_{02}(1-2D_2)} - \tfrac{1}{C_2R_2} \end{aligned} \tag{6.24}$$

The eigenvalues of **A**, i.e., the roots of the characteristic polynomial is given by

$$det(sI - \mathbf{A}) = s^4 + a_3s^3 + a_2s^2 + a_1s + a_0 \tag{6.25}$$

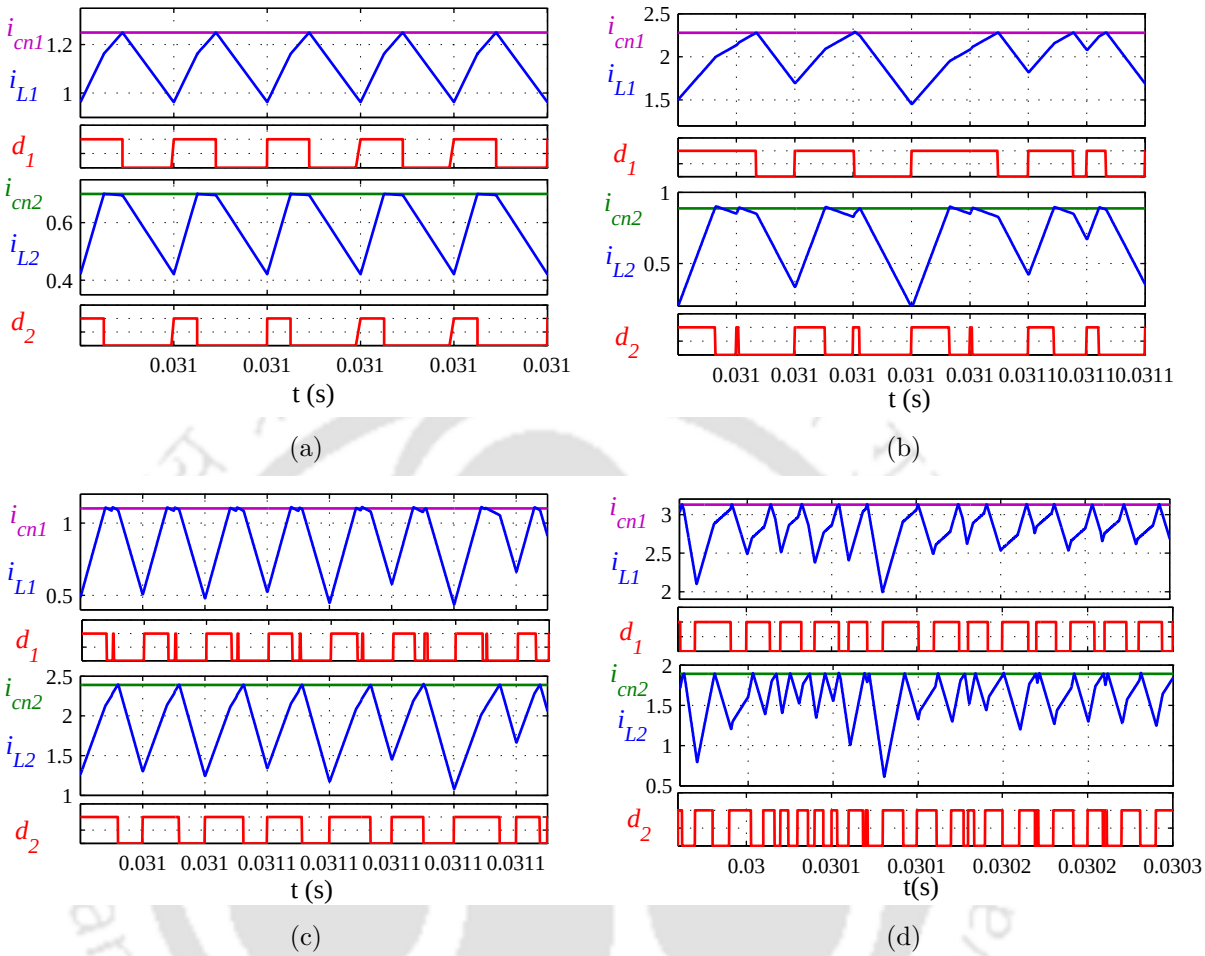


Figure 6.18: Simulation results of PCM controlled CI-SIDO boost converter with inner loops closed (a) $D_1 = 0.45$, $D_2 = 0.22$ (b) $D_1 = 0.6$, $D_2 = 0.3$ (c) $D_1 = 0.4$, $D_2 = 0.6$ (d) $D_1 = 0.66$, $D_2 = 0.54$

Note that the coefficients of the characteristic equation given in (6.25) are function of D_1, D_2 and is found that when $D_1 > 0.5$ or $D_2 > 0.5$ or $D_1 > 0.5$ and $D_2 > 0.5$, the coefficients becomes negative making the system unstable. This confirms that instability in PCM controlled CI-SIDO boost converter occurs when both duty ratios (D_1, D_2) or any one duty ratio is greater than 0.5.

6.5.2.1 Simulation Verification

The instability of PCM controlled CI-SIDO boost converter without slope compensation is validated using simulation results. The CI-SIDO boost converter parameter used in simulation are shown in Table 6.3. Figure 6.18 shows the simulated waveform of reference current i_{cn1},

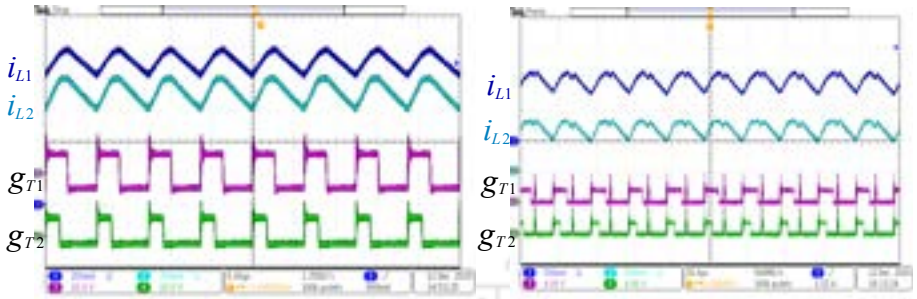


Figure 6.19: Waveform of inductor currents and duty cycles of PCM control CI-SIDO buck with inner loop close (a) $D_1 = 0.48$, $D_2 = 0.35$ stable (b) $D_1 = 0.55$, $D_2 = 0.4$ unstable stable

i_{cn2}, inductor currents i_{L1}, i_{L2}, gate pulses which is obtained for different duty cycles. It is observed that the waveform of inductor currents are stable for $D_1 < 0.5$, $D_2 < 0.5$ as shown in Figure 6.18(a) and unstable for any one or both duty cycle greater than 0.5 as shown in Figure 6.18(b), 6.18(c), 6.18(d).

6.5.2.2 Experimental Verification

The instability of PCM controlled CI-SIDO boost converter without slope compensation is validated experimentally as shown in Figure 6.19. The CI-SIDO boost converter parameter used in experiment is same as used in simulation. Figure 6.19(a) shows the stable waveform of inductor currents for $D_1 = 0.48$, $D_2 = 0.35$ and Figure 6.19(a) shows the unstable waveform of inductor currents for $D_1 = 0.55$, $D_2 = 0.4$.

6.5.3 Inner Loop Instability for PCM Control of CI-SIDO Boost and Buck Converter

The small-signal model of current modulator without slope-compensation for CI-SIDO boost and buck converter is obtained from (6.11) using $m_{c1} = m_{c2} = 0$, $V_{off1} = V_{01}$, $V_{off2} = V_{in}$, $\hat{v}_{off1} = \hat{v}_{01}$, $\hat{v}_{off2} = \hat{v}_{in}$ and is given by

$$\begin{bmatrix}\hat{d}_1\\ \hat{d}_2\end{bmatrix} = \begin{bmatrix}\frac{-2L_1}{T_sV_{01}(1-2D_1)} & \frac{2M}{T_sV_{01}(1-2D_1)}\\ \frac{2M}{T_sV_{in}(1-2D_2)} & \frac{-2L_2}{T_sV_{in}(1-2D_2)}\end{bmatrix}\begin{bmatrix}\hat{i}_{L1}\\ \hat{i}_{L2}\end{bmatrix} + \begin{bmatrix}\frac{2L_1}{T_sV_{01}(1-2D_1)} & \frac{-2M}{T_sV_{01}(1-2D_1)}\\ \frac{-2M}{T_sV_{in}(1-2D_2)} & \frac{2L_2}{T_sV_{in}(1-2D_2)}\end{bmatrix}\begin{bmatrix}\hat{i}_{cn1}\\ \hat{i}_{cn2}\end{bmatrix} - \begin{bmatrix}\frac{D_1(1-D_1)}{V_{01}(1-2D_1)} & 0\\ 0 & \frac{D_2(1-D_2)}{V_{in}(1-2D_2)}\end{bmatrix}\begin{bmatrix}\hat{v}_{01}\\ \hat{v}_{in}\end{bmatrix} \quad (6.26)$$

Using (6.26) in (6.17), we can obtain the complete state-space model of PCM controlled CI-SIDO boost and buck converter with inner loops closed and its **A** matrix is given by

$$A = \begin{bmatrix}a_{11} & a_{12} & a_{13} & a_{14}\\ a_{21} & a_{22} & a_{23} & a_{24}\\ a_{31} & a_{32} & a_{33} & 0\\ 0 & a_{42} & 0 & a_{44}\end{bmatrix} \quad (6.27)$$

where,

$$\begin{aligned} a_{11} &= \tfrac{-2}{T_s(1-k^2)}\left(\tfrac{1}{1-2D_1} - \tfrac{k^2}{1-2D_2}\right),\ a_{12} = \tfrac{2M}{T_sL_1'}\left(\tfrac{1}{1-2D_1} - \tfrac{1}{1-2D_2}\right)\\ a_{13} &= \tfrac{-(1-D_1)}{L_1'} - \tfrac{D_1(1-D_1)}{L_1'(1-2D_1)},\ a_{14} = \tfrac{-M}{L_2L_1'}\\ a_{21} &= \tfrac{2M}{T_sL_2'}\left(\tfrac{1}{1-2D_2} - \tfrac{1}{1-2D_1}\right),\ a_{22} = \tfrac{-2}{T_s(1-k^2)}\left(\tfrac{1}{1-2D_2} - \tfrac{k^2}{1-2D_1}\right)\\ a_{23} &= \tfrac{-M(1-D_1)}{L_1L_2'} - \tfrac{MD_1(1-D_1)}{L_1L_2'(1-2D_1)},\ a_{24} = \tfrac{-1}{L_2'}\\ a_{31} &= \tfrac{(1-D_1)}{C_1} + \tfrac{2I_{L1}L_1}{T_sC_1V_{01}(1-2D_1)},\ a_{32} = \tfrac{-2I_{L1}M}{T_sC_1V_{01}(1-2D_1)},\ a_{33} = \tfrac{I_{L1}D_1(1-D_1)}{C_1V_{01}(1-2D_1)} - \tfrac{1}{C_1R_1}\\ a_{42} &= \tfrac{1}{C_2},\ a_{44} = -\tfrac{1}{C_2R_2} \end{aligned} \quad (6.28)$$

The eigenvalues of **A**, i.e., the roots of the characteristic polynomial is given by

$$det(sI - \mathbf{A}) = s^4 + a_3s^3 + a_2s^2 + a_1s + a_0 \quad (6.29)$$

Note that the coefficients of the characteristic equation given in (6.29) are function of D_1, D_2 and is found that when $D_1 > 0.5$ or $D_2 > 0.5$ or $D_1 > 0.5$ and $D_2 > 0.5$, the coefficients becomes negative making the system unstable. This confirms that instability in PCM controlled CI-SIDO boost and buck converter occurs when both duty ratios (D_1, D_2) or any one duty

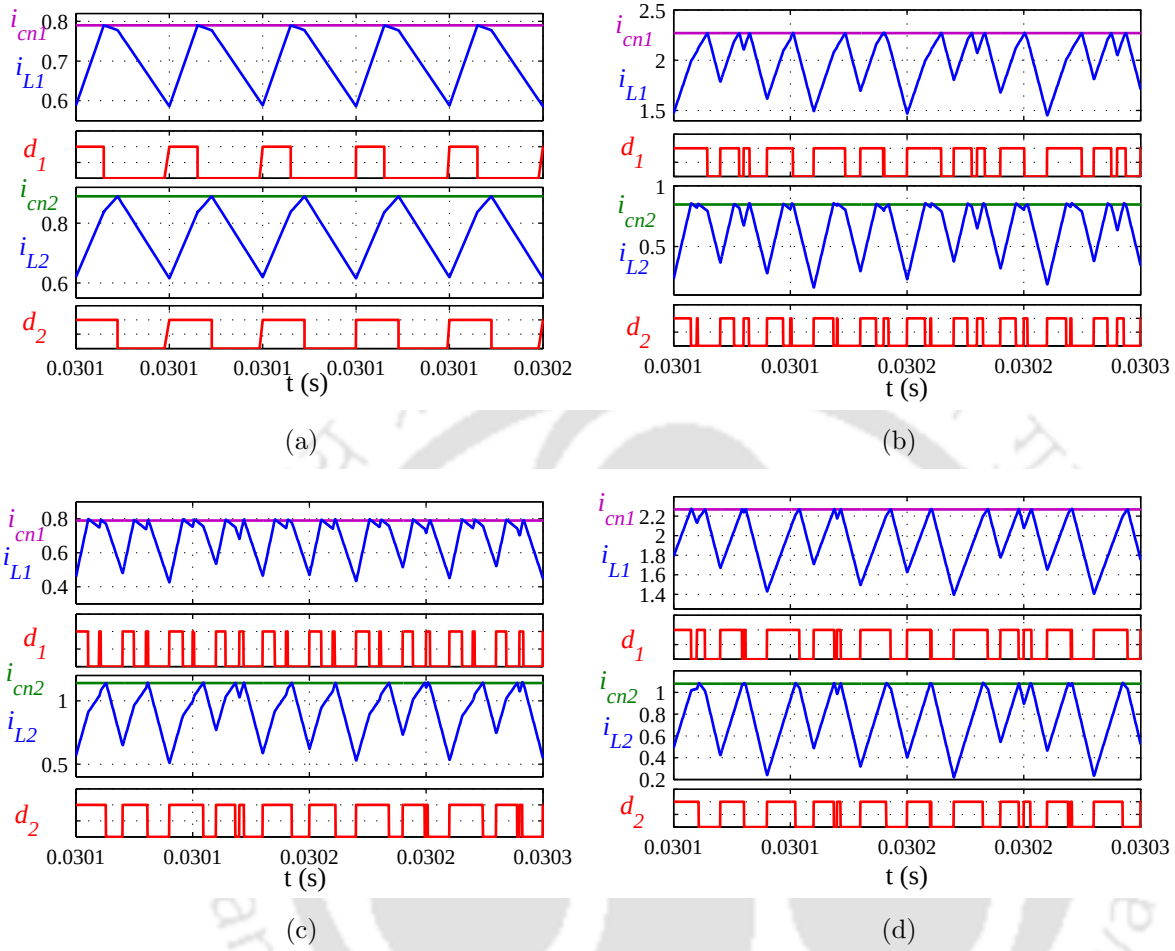


Figure 6.20: Simulation results of PCM controlled CI-SIDO boost and buck converter with inner loops closed (a) $D_1 = 0.3$, $D_2 = 0.45$ (b) $D_1 = 0.6$, $D_2 = 0.4$ (c) $D_1 = 0.3$, $D_2 = 0.6$ (d) $D_1 = 0.6$, $D_2 = 0.54$

ratio is greater than 0.5.

6.5.3.1 Simulation Verification

The instability of PCM controlled CI-SIDO boost and buck converter without slope compensation is validated using simulation results. The CI-SIDO boost and buck converter parameter used in simulation are shown in Table 6.3. Figure 6.20 shows the simulated waveform of reference current i_{cn1}, i_{cn2}, inductor currents i_{L1}, i_{L2}, gate pulses which is obtained for different duty cycles. It is observed that the waveform of inductor currents are stable for $D_1 < 0.5$, $D_2 < 0.5$ as shown in Figure 6.20(a) and unstable for any one or both duty cycle greater than 0.5 as shown in Figure 6.20(b), 6.20(c), 6.20(d).

6.6 Conclusion

This chapter develops a unified large signal and small-signal model for peak current mode (PCM) controlled coupled inductor single-input dual-output (CI-SIDO) converters operating in continuous conduction mode. The unified model of PCM controlled CI-SIDO converter is developed by interfacing unified model of current modulator with the small-signal model of CISIDO converter. The unified analytical model is validated in both simulation and experiment. Moreover, using the unified model the instability of PCM controlled CI-SIDO converter without slope compensation is predicted. It is observed that instability in PCM controlled CI-SIDO converter occur if both duty ratios or any one duty ratio is greater than 0.5. Finally the instability of PCM controlled CI-SIDO converter is verified using simulation and experimental results.

Note: Major part of this chapter is reproduced from my publications:

1. G. Nayak and S. Nath, "Instability in Peak Current Mode Controlled Coupled SIDO Buck Converter", 2020 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Jaipur, India, 2020. (Accepted)

2. G. Nayak, S. Nath, "Small Signal Model for Peak Current Controlled Coupled SIDO Buck Converter", 2021 IEEE Energy Conversion Congress and Exposition Asia (ECCE ASIA-2021). (Accepted)

7

Design of Peak Current Mode Control for CI-SIDO Buck Converter

Contents

7.1 Introduction

This chapter aims to design peak current mode (PCM) control for CI-SIDO buck converter to reduce cross-regulation, improve dynamic performance and prevent sub-harmonic oscillations. Using the small-signal model of PCM controlled CI-SIDO buck converter developed in Chapter 6, the slope compensation and Type-II compensator design procedure are proposed. The effectiveness of designed slope compensation and controller for PCM controlled CI-SIDO buck converter is validated experimentally on an experimental prototype.

7.2 Analysis of Peak Current Mode Controlled CI-SIDO Buck Converter

Figure 7.1 and 7.2 show the circuit diagram and small-signal block diagram model of PCM controlled CI-SIDO buck converter, respectively. Figure 7.2 shows two feedback loops, i.e., inner current and outer voltage feedback for each output. The inner current feedbacks are formed using two equal sensing resistances r_s, two slope compensations m_{c1}, m_{c2} and gains of current modulators f_{m11}, f_{m22}, f_{m12}, f_{m21}. The modulator gains are functions of slope compensations. The outer voltage feedbacks are formed using two sensing gains β_1, β_2 and two voltage controllers G_{v1}, G_{v2}.

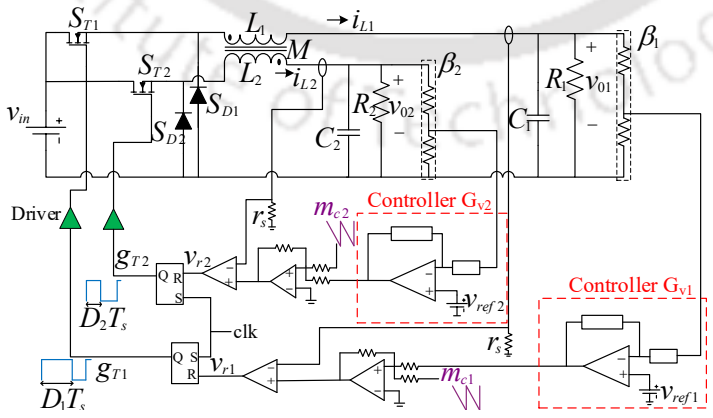


Figure 7.1: Circuit diagram of Peak current mode control CI-SIDO buck converter

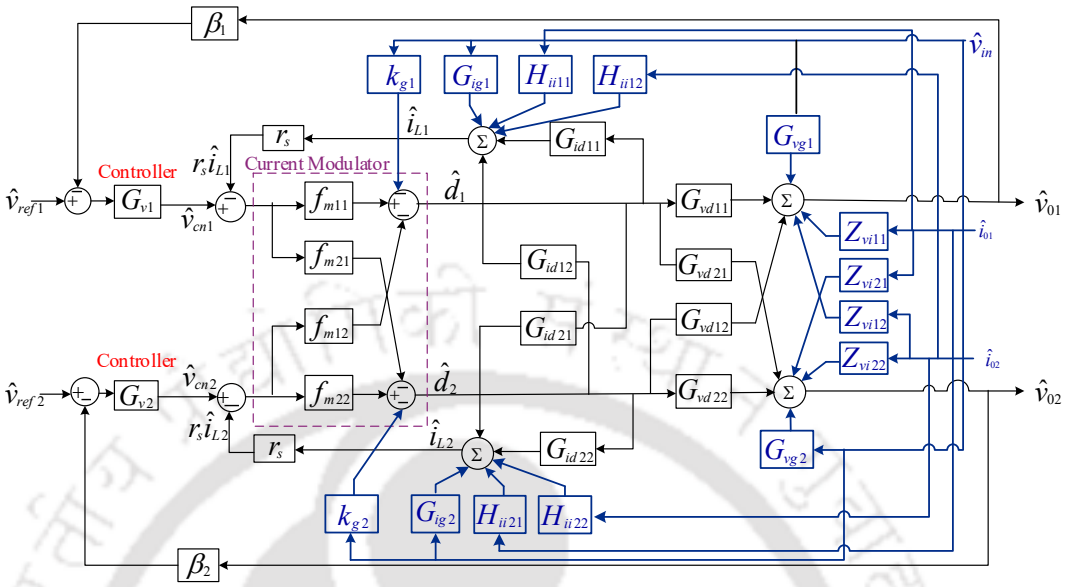


Figure 7.2: Small signal model of peak current mode controlled CI-SIDO buck converter

7.2.1 Analysis of Inner Current Loops

From Figure (7.2), the inductor currents can be written in matrix form as

$$\begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \end{bmatrix} = \begin{bmatrix} G_{id11} & G_{id12} \\ G_{id21} & G_{id22} \end{bmatrix} \begin{bmatrix} \hat{d}_1 \\ \hat{d}_2 \end{bmatrix} + \begin{bmatrix} G_{ig1} \\ G_{ig2} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \end{bmatrix} + \begin{bmatrix} H_{ii11} & H_{ii12} \\ H_{ii21} & H_{ii22} \end{bmatrix} \begin{bmatrix} \hat{i}_{01} \\ \hat{i}_{02} \end{bmatrix} \tag{7.1}$$

The expression of all transfer functions in (7.1) are given in Chapter 2.

From Figure (7.2), the duty cycles are expressed as

$$\begin{aligned} \begin{bmatrix} \hat{d}_1 \\ \hat{d}_2 \end{bmatrix} &= \begin{bmatrix} f_{m11} & -f_{m12} \\ -f_{m21} & f_{m22} \end{bmatrix} \begin{bmatrix} \hat{v}_{cn1} - r_s\hat{i}_{L1} \\ \hat{v}_{cn2} - r_s\hat{i}_{L2} \end{bmatrix} - \begin{bmatrix} k_{g1} \\ k_{g2} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \end{bmatrix} \\ &= \begin{bmatrix} f_{m11} & -f_{m12} \\ -f_{m21} & f_{m22} \end{bmatrix} \begin{bmatrix} \hat{v}_{cn1} \\ \hat{v}_{cn2} \end{bmatrix} - \begin{bmatrix} f_{m11}r_s & -f_{m12}r_s \\ -f_{m21}r_s & f_{m22}r_s \end{bmatrix} \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \end{bmatrix} - \begin{bmatrix} k_{g1} \\ k_{g2} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \end{bmatrix} \end{aligned} \tag{7.2}$$

where, $k_{g1} = k_{v11} + k_{v12}$, $k_{g2} = k_{v22} + k_{v21}$. The expression of modulator gains f_{m11}, f_{m22}, f_{m12}, f_{m21} and feed-forward gains k_{v11}, k_{v12}, k_{v21}, k_{v22} are given in Chapter 6.

Using (7.1) in (7.2), we get

$$\begin{bmatrix}\hat{d}_1\\ \hat{d}_2\end{bmatrix} = \begin{bmatrix} f_{m11} & -f_{m12}\\ -f_{m21} & f_{m22}\end{bmatrix}\begin{bmatrix}\hat{v}_{cn1}\\ \hat{v}_{cn2}\end{bmatrix} - \begin{bmatrix} f_{m11}r_s & -f_{m12}r_s\\ -f_{m21}r_s & f_{m22}r_s\end{bmatrix}\left(\begin{bmatrix} G_{id11} & G_{id12}\\ G_{id21} & G_{id22}\end{bmatrix}\begin{bmatrix}\hat{d}_1\\ \hat{d}_2\end{bmatrix} + \begin{bmatrix}G_{ig1}\\ G_{ig2}\end{bmatrix}\begin{bmatrix}\hat{v}_{in}\end{bmatrix} + \begin{bmatrix} H_{ii11} & H_{ii12}\\ H_{ii21} & H_{ii22}\end{bmatrix}\begin{bmatrix}\hat{i}_{01}\\ \hat{i}_{02}\end{bmatrix}\right) - \begin{bmatrix}k_{g1}\\ k_{g2}\end{bmatrix}\begin{bmatrix}\hat{v}_{in}\end{bmatrix} \tag{7.3}$$

Rearranging (7.3), we get

$$\begin{bmatrix} 1+X_{11} & X_{12}\\ X_{21} & 1+X_{22}\end{bmatrix}\begin{bmatrix}\hat{d}_1\\ \hat{d}_2\end{bmatrix} = \begin{bmatrix} f_{m11} & -f_{m12}\\ -f_{m21} & f_{m22}\end{bmatrix}\begin{bmatrix}\hat{v}_{cn1}\\ \hat{v}_{cn2}\end{bmatrix} - \begin{bmatrix}X_{ig1}\\ X_{ig2}\end{bmatrix}\begin{bmatrix}\hat{v}_{in}\end{bmatrix} - \begin{bmatrix} Y_{ii11} & Y_{ii12}\\ Y_{ii21} & Y_{ii22}\end{bmatrix}\begin{bmatrix}\hat{i}_{01}\\ \hat{i}_{02}\end{bmatrix} \tag{7.4}$$

where,

$$\begin{aligned} X_{11} &= r_s(f_{m11}G_{id11} - f_{m12}G_{id21}),\ X_{22} = r_s(f_{m22}G_{id22} - f_{m21}G_{id12})\\ X_{12} &= r_s(f_{m11}G_{id12} - f_{m12}G_{id22}),\ X_{21} = r_s(f_{m22}G_{id21} - f_{m21}G_{id11})\\ X_{ig1} &= k_{g1} + r_s(f_{m11}G_{ig1} - f_{m12}G_{ig2}),\ X_{ig2} = k_{g2} + r_s(f_{m22}G_{ig2} - f_{m21}G_{ig1})\\ Y_{ii11} &= r_s(f_{m11}H_{ii11} - f_{m12}H_{i121}),\ Y_{ii22} = r_s(f_{m22}H_{ii22} - f_{m21}H_{i112})\\ Y_{ii12} &= r_s(f_{m11}H_{ii12} - f_{m12}H_{i122}),\ Y_{ii21} = r_s(f_{m22}H_{ii21} - f_{m21}H_{i112}) \end{aligned} \tag{7.5}$$

The expressions of (7.5) in terms of circuit variables are obtained using the expressions of all transfer functions, modulator gains assuming ideal condition (no parasitic resistances) and are given as follows

$$
\begin{aligned}
X_{11} &= x_{01}(1-\frac{k^2a_2}{m_{c1}+a_2})\frac{(s+\frac{1}{R_1C_1})(s^2+\frac{s}{R_2C_2}+\frac{1}{L_{eq2}C_2})}{Deno(s)} \\
X_{22} &= x_{02}(1-\frac{k^2a_1}{m_{c1}+a_1})\frac{(s+\frac{1}{R_2C_2})(s^2+\frac{s}{R_1C_1}+\frac{1}{L_{eq1}C_1})}{Deno(s)} \\
X_{12} &= \frac{Mx_{01}(s+\frac{1}{R_2C_2})}{L_2}\frac{(s^2(1-\frac{a_2}{m_{c2}+a_2})+\frac{s}{R_1C_1}(1-\frac{a_2}{m_{c2}+a_2})+\frac{-a_2}{L_1C_1(m_{c2}+a_2)})}{Deno(s)} \\
X_{21} &= \frac{Mx_{02}(s+\frac{1}{R_1C_1})}{L_1}\frac{(s^2(1-\frac{a_1}{m_{c1}+a_1})+\frac{s}{R_2C_2}(1-\frac{a_1}{m_{c1}+a_1})+\frac{-a_1}{L_2C_2(m_{c1}+a_1)})}{Deno(s)} \\
X_{ig1} &= k_{g1}+\frac{r_sf_{m1}D_1}{L_1}\frac{(s+\frac{1}{R_1C_1})(s^2+\frac{s}{R_2C_2}+\frac{1}{L_2'C_2})-\frac{MD_2}{L_2L_1'C_1D_1}(s+\frac{1}{R_2C_2})}{Deno(s)} \\
X_{ig2} &= k_{g2}+\frac{r_sf_{m2}D_2}{L_2}\frac{(s+\frac{1}{R_2C_2})(s^2+\frac{s}{R_1C_1}+\frac{1}{L_1'C_1})-\frac{MD_1}{L_1L_2'C_2D_2}(s+\frac{1}{R_1C_1})}{Deno(s)} \\
Y_{ii11} &= \frac{r_sf_{m1}}{L_1C_1}\frac{(s^2+\frac{s}{R_2C_2}+\frac{1}{L_2'C_2})}{deno(s)},\ Y_{ii22}=\frac{r_sf_{m2}}{L_2C_2}\frac{(s^2+\frac{s}{R_1C_1}+\frac{1}{L_1'C_1})}{deno(s)} \\
Y_{ii21} &= \frac{-r_sf_{m2}M}{L_2L_1'C_1}\frac{\frac{1}{L_2C_2})}{deno(s)},\ Y_{ii12}=\frac{-r_sf_{m1}M}{L_1L_2'C_2}\frac{\frac{1}{L_1C_1})}{deno(s)}
\end{aligned}
\tag{7.6}
$$

where, $Deno(s)=(s^2+\frac{s}{R_1C_1}+\frac{1}{L_{k1}C_1})(s^2+\frac{s}{R_2C_2}+\frac{1}{L_{k2}C_2})-\frac{k^2}{L_{k1}L_{k2}C_1C_2}$

$x_{01}=\frac{r_sV_{in}f_{m11}}{L_1'}$, $x_{01}=\frac{r_sV_{in}f_{m22}}{L_2'}$, $a_1=\frac{V_{in}(1-2D_1)}{2L_1'}$, $a_2=\frac{V_{in}(1-2D_2)}{2L_2'}$, $L_{eqj}=L_j(1-\frac{k^2a_j}{m_{cj}+a_j})$, $j=\{1,2\}$

Solving (7.4), we get

$$
\begin{aligned}
\begin{bmatrix}\hat{d}_1\\ \hat{d}_2\end{bmatrix} &= \begin{bmatrix}\frac{f_{m11}+\frac{f_{m21}X_{12}}{1+X_{22}}}{1+T_{i1}'} & -\frac{f_{m12}+\frac{f_{m22}X_{12}}{1+X_{22}}}{1+T_{i1}'} \\ -\frac{f_{m21}+\frac{f_{m11}X_{21}}{1+X_{11}}}{1+T_{i2}'} & \frac{f_{m22}+\frac{f_{m12}X_{21}}{1+X_{11}}}{1+T_{i2}'}\end{bmatrix}\begin{bmatrix}\hat{v}_{cn1}\\ \hat{v}_{cn2}\end{bmatrix}-\begin{bmatrix}\frac{X_{ig1}-\frac{X_{ig2}X_{12}}{1+X_{22}}}{1+T_{i1}'}\\ \frac{X_{ig2}-\frac{X_{ig1}X_{21}}{1+X_{11}}}{1+T_{i2}'}\end{bmatrix}\begin{bmatrix}\hat{v}_{in}\end{bmatrix} \\
&\quad -\begin{bmatrix}\frac{Y_{ii11}-\frac{Y_{ii21}X_{12}}{1+X_{22}}}{1+T_{i1}'} & \frac{Y_{ii12}-\frac{Y_{ii22}X_{12}}{1+X_{22}}}{1+T_{i1}'}\\ \frac{Y_{ii21}-\frac{Y_{ii11}X_{21}}{1+X_{11}}}{1+T_{i2}'} & \frac{Y_{ii22}-\frac{Y_{ii12}X_{21}}{1+X_{11}}}{1+T_{i2}'}\end{bmatrix}\begin{bmatrix}\hat{i}_{01}\\ \hat{i}_{02}\end{bmatrix}
\end{aligned}
\tag{7.7}
$$

where,

$$
T_{i1}'=X_{11}-\frac{X_{12}X_{21}}{1+X_{22}}\ ,\ T_{i2}'=X_{22}-\frac{X_{12}X_{21}}{1+X_{11}} \tag{7.8}
$$

T_{i1}', T_{i2}' are the current loop gains.

7.2.1.1 Current Loop Gains

The current loop gain transfer functions are denoted as $T_{i1}^{'}$, $T_{i2}^{'}$ and are given by (7.8). The DC gains of X_{11}, X_{22}, X_{11}, X_{22} are

$$\begin{aligned} |X_{11}| &= \frac{r_s V_{in}/R_1 T_s}{m_{c1} + a_1 - \frac{k^2 a_1 a_2}{m_{c2}+a_2}}, \ |X_{12}| = \frac{-Ma_2|X_{11}|}{L_1(m_{c2}+a_2)} \\ |X_{22}| &= \frac{r_s V_{in}/R_2 T_s}{m_{c2} + a_2 - \frac{k^2 a_1 a_2}{m_{c1}+a_1}}, \ |X_{21}| = \frac{-Ma_1|X_{22}|}{L_2(m_{c1}+a_1)} \end{aligned} \tag{7.9}$$

From (7.8), (7.9), it is observed that $T_{ij}^{'}$ becomes negative when $m_{cj} = 0$, $D_j > 0.5$, which lead to instability of inner current loop. Therefore, to prevent instability of inner loops for $D_j > 0.5$, the slope compensations m_{cj} are designed to make

$$|X_{11}| >> 0 \quad , \quad |X_{22}| >> 0 \tag{7.10}$$

Applying, (7.10) in (7.8), the current loop gains can be approximated as

$$\begin{aligned} T_{i1}^{'} &\approx X_{11} - \frac{X_{12}X_{21}}{X_{22}} = r_s f_{m1} G_{id1} \equiv T_{i1} \\ T_{i2}^{'} &\approx X_{22} - \frac{X_{12}X_{21}}{X_{11}} = r_s f_{m2} G_{id2} \equiv T_{i2} \end{aligned} \tag{7.11}$$

where, G_{idj}, f_{mj} are the approximated duty cycle to inductor current transfer function, current modulator gain and are given by

$$\begin{aligned} G_{idj}|_{ideal} &= \frac{\frac{V_{in}}{L_{eqj}}(s+\frac{1}{R_j C_j})}{s^2+\frac{s}{R_2 C_j}+\frac{1}{L_{eqj}C_j}}, \quad G_{idj}|_{non-ideal} = \frac{\frac{V_{in}}{L_{eqj}}(s+\frac{r_j^{''}}{C_j})}{s^2+s(\frac{r_j^{'}}{L_{eqj}}+\frac{r_j^{''}}{C_j})+\frac{R_j r_j^{''}}{L_{eqj}C_j}} \\ f_{mj} &= \frac{1/T_s}{(m_{cj}+\frac{V_{in}(1-2D_j)}{2L_j})} \end{aligned} \tag{7.12}$$

From (7.11), (7.12) it is found that the instability can be prevented if slope compensation satisfies

$$m_{cj} > \frac{V_{in}(1-2D_j)}{2L_j}, \text{ for } D_j > 0.5 \tag{7.13}$$

It is noted from (7.11), (7.12) that m_{cj} are inversely related with the DC gains and resonant frequency of T_{ij}. Thus, with large m_{cj}, DC gains and resonant frequency of T_{ij} decreases and the control scheme reduce to voltage mode control. So, m_{cj} are designed to ensure faster current

loops and satisfy (7.13).

7.2.2 Analysis of Outer Voltage Loops

The output voltages of the converter is written in matrix form as

$$\begin{bmatrix}\hat{v}_{01}\\ \hat{v}_{02}\end{bmatrix}=\begin{bmatrix}G_{vd11} & G_{vd12}\\ G_{vd21} & G_{vd22}\end{bmatrix}\begin{bmatrix}\hat{d}_1\\ \hat{d}_2\end{bmatrix}+\begin{bmatrix}G_{vg1}\\ G_{vg2}\end{bmatrix}\begin{bmatrix}\hat{v}_{in}\end{bmatrix}+\begin{bmatrix}Z_{vi11} & Z_{vi12}\\ Z_{vi21} & Z_{vi22}\end{bmatrix}\begin{bmatrix}\hat{i}_{01}\\ \hat{i}_{02}\end{bmatrix} \tag{7.14}$$

The expressions of all transfer functions in (7.14) are given in Chapter 2.

Using (7.7) in (7.14), we get

$$\begin{bmatrix}\hat{v}_{01}\\ \hat{v}_{02}\end{bmatrix}=\begin{bmatrix}G_{vd11} & G_{vd12}\\ G_{vd21} & G_{vd22}\end{bmatrix}\left(\begin{bmatrix}\frac{f_{m11}+\frac{f_{m21}X_{12}}{1+X_{22}}}{1+T'_{i1}} & -\frac{f_{m12}+\frac{f_{m22}X_{12}}{1+X_{22}}}{1+T'_{i1}}\\ -\frac{f_{m21}+\frac{f_{m11}X_{21}}{1+X_{11}}}{1+T'_{i2}} & \frac{f_{m22}+\frac{f_{m12}X_{21}}{1+X_{11}}}{1+T'_{i2}}\end{bmatrix}\begin{bmatrix}\hat{v}_{cn1}\\ \hat{v}_{cn2}\end{bmatrix}-\begin{bmatrix}\frac{X_{ig1}-\frac{X_{ig2}X_{12}}{1+X_{22}}}{1+T'_{i1}}\\ \frac{X_{ig2}-\frac{X_{ig1}X_{21}}{1+X_{11}}}{1+T'_{i2}}\end{bmatrix}\begin{bmatrix}\hat{v}_{in}\end{bmatrix}\right.$$
$$\left.-\begin{bmatrix}\frac{Y_{ii11}-\frac{Y_{ii21}X_{12}}{1+X_{22}}}{1+T'_{i1}} & \frac{Y_{ii12}-\frac{Y_{ii22}X_{12}}{1+X_{22}}}{1+T'_{i1}}\\ \frac{Y_{ii21}-\frac{Y_{ii11}X_{21}}{1+X_{11}}}{1+T'_{i2}} & \frac{Y_{ii22}-\frac{Y_{ii12}X_{21}}{1+X_{11}}}{1+T'_{i2}}\end{bmatrix}\begin{bmatrix}\hat{i}_{01}\\ \hat{i}_{02}\end{bmatrix}\right)+\begin{bmatrix}G_{vg1}\\ G_{vg2}\end{bmatrix}\begin{bmatrix}\hat{v}_{in}\end{bmatrix}+\begin{bmatrix}Z_{vi11} & Z_{vi12}\\ Z_{vi21} & Z_{vi22}\end{bmatrix}\begin{bmatrix}\hat{i}_{01}\\ \hat{i}_{02}\end{bmatrix} \tag{7.15}$$

The reference control voltages v_{cn1}, v_{cn2} for inner current loops are generated by the outer voltage loops as shown in Figure 7.2(b) and is written as

$$\begin{bmatrix}\hat{v}_{cn1}\\ \hat{v}_{cn2}\end{bmatrix}=\begin{bmatrix}G_{v1} & 0\\ 0 & G_{v2}\end{bmatrix}\begin{bmatrix}v_{ref1}-\beta_1 v_{01}\\ v_{ref2}-\beta_2 v_{02}\end{bmatrix} \tag{7.16}$$

Using (7.16) in (7.15), and rearranging we get

$$\begin{bmatrix}1+\beta_1 G_{v1}H_{vc11} & \beta_2 G_{v2}H_{vc12}\\ \beta_1 G_{v1}H_{vc21} & 1+\beta_2 G_{v2}H_{vc22}\end{bmatrix}\begin{bmatrix}\hat{v}_{01}\\ \hat{v}_{02}\end{bmatrix}=\begin{bmatrix}G_{v1}H_{vc11} & G_{v2}H_{vc12}\\ G_{v1}H_{vc21} & G_{v2}H_{vc22}\end{bmatrix}\begin{bmatrix}\hat{v}_{ref1}\\ \hat{v}_{ref2}\end{bmatrix}$$
$$+\left(\begin{bmatrix}G_{vg1}\\ G_{vg2}\end{bmatrix}-\begin{bmatrix}G_{vd11} & G_{vd12}\\ G_{vd21} & G_{vd22}\end{bmatrix}\begin{bmatrix}\frac{X_{ig1}-\frac{X_{ig2}X_{12}}{1+X_{22}}}{1+T'_{i1}}\\ \frac{X_{ig2}-\frac{X_{ig1}X_{21}}{1+X_{11}}}{1+T'_{i2}}\end{bmatrix}\right)\begin{bmatrix}\hat{v}_{in}\end{bmatrix} \tag{7.17}$$
$$+\left(\begin{bmatrix}Z_{vi11} & Z_{vi12}\\ Z_{vi21} & Z_{vi22}\end{bmatrix}-\begin{bmatrix}G_{vd11} & G_{vd12}\\ G_{vd21} & G_{vd22}\end{bmatrix}\begin{bmatrix}\frac{Y_{ii11}-\frac{Y_{ii21}X_{12}}{1+X_{22}}}{1+T'_{i1}} & \frac{Y_{ii12}-\frac{Y_{ii22}X_{12}}{1+X_{22}}}{1+T'_{i1}}\\ \frac{Y_{ii21}-\frac{Y_{ii11}X_{21}}{1+X_{11}}}{1+T'_{i2}} & \frac{Y_{ii22}-\frac{Y_{ii12}X_{21}}{1+X_{11}}}{1+T'_{i2}}\end{bmatrix}\right)\begin{bmatrix}\hat{i}_{01}\\ \hat{i}_{02}\end{bmatrix}$$

where,

$$\begin{aligned}
H_{vc11} &= \frac{1}{1+T'_{i1}}\left(G_{vd11}\left(f_{m11}+\frac{f_{m21}X_{12}}{1+X_{22}}\right)-G_{vd12}\left(f_{m21}\frac{1+X_{11}}{1+X_{22}}+\frac{f_{m11}X_{21}}{1+X_{22}}\right)\right)\\
H_{vc22} &= \frac{1}{1+T'_{i2}}\left(G_{vd22}\left(f_{m22}+\frac{f_{m12}X_{21}}{1+X_{11}}\right)-G_{vd21}\left(f_{m12}\frac{1+X_{22}}{1+X_{11}}+\frac{f_{m22}X_{12}}{1+X_{11}}\right)\right)\\
H_{vc12} &= \frac{1}{1+T'_{i1}}\left(G_{vd12}\left(f_{m22}\frac{1+X_{11}}{1+X_{22}}+\frac{f_{m12}X_{21}}{1+X_{22}}\right)-G_{vd11}\left(f_{m12}+\frac{f_{m22}X_{12}}{1+X_{22}}\right)\right)\\
H_{vc21} &= \frac{1}{1+T'_{i2}}\left(G_{vd21}\left(f_{m11}\frac{1+X_{22}}{1+X_{11}}+\frac{f_{m21}X_{12}}{1+X_{11}}\right)-G_{vd22}\left(f_{m21}+\frac{f_{m11}X_{21}}{1+X_{11}}\right)\right)
\end{aligned} \tag{7.18}$$

Solving (7.17), we get the closed-loop expression as

$$\begin{aligned}
\begin{bmatrix}\hat{v}_{01}\\ \hat{v}_{02}\end{bmatrix} = &\begin{bmatrix}\frac{1}{1+T'_1} & \frac{-\beta_2 G_{v2}H_{vc12}}{(1+\beta_2 G_{v2}H_{vc22})(1+T'_1)}\\ \frac{-\beta_1 G_{v1}H_{vc21}}{(1+\beta_1 G_{v1}H_{vc11})(1+T'_2)} & \frac{1}{1+T'_2}\end{bmatrix}\left(\begin{bmatrix}G_{v1}H_{vc11} & G_{v2}H_{vc12}\\ G_{v1}H_{vc21} & G_{v2}H_{vc22}\end{bmatrix}\begin{bmatrix}\hat{v}_{ref1}\\ \hat{v}_{ref2}\end{bmatrix}\right.\\
&+\left(\begin{bmatrix}G_{vg1}\\ G_{vg2}\end{bmatrix}-\begin{bmatrix}G_{vd11} & G_{vd12}\\ G_{vd21} & G_{vd22}\end{bmatrix}\begin{bmatrix}\frac{X_{ig1}-\frac{X_{ig2}X_{12}}{1+X_{22}}}{1+T'_{i1}}\\ \frac{X_{ig2}-\frac{X_{ig1}X_{21}}{1+X_{11}}}{1+T'_{i2}}\end{bmatrix}\right)\begin{bmatrix}\hat{v}_{in}\end{bmatrix}\\
&\left.+\left(\begin{bmatrix}Z_{vi11} & Z_{vi12}\\ Z_{vi21} & Z_{vi22}\end{bmatrix}-\begin{bmatrix}G_{vd11} & G_{vd12}\\ G_{vd21} & G_{vd22}\end{bmatrix}\begin{bmatrix}\frac{Y_{ii11}-\frac{Y_{ii21}X_{12}}{1+X_{22}}}{1+T'_{i1}} & \frac{Y_{ii12}-\frac{Y_{ii22}X_{12}}{1+X_{22}}}{1+T'_{i1}}\\ \frac{Y_{ii21}-\frac{Y_{ii11}X_{21}}{1+X_{11}}}{1+T'_{i2}} & \frac{Y_{ii22}-\frac{Y_{ii12}X_{21}}{1+X_{11}}}{1+T'_{i2}}\end{bmatrix}\right)\begin{bmatrix}\hat{i}_{01}\\ \hat{i}_{02}\end{bmatrix}\right)
\end{aligned} \tag{7.19}$$

where, T'_1, T'_2 are the outer loop gains and are given as

$$\begin{aligned}
T'_1 &= \beta_1 G_{v1}(H_{vc11}-\frac{\beta_2 G_{v2}H_{vc12}H_{vc21}}{1+\beta_2 G_{v2}H_{vc22}})\\
T'_2 &= \beta_2 G_{v2}(H_{vc22}-\frac{\beta_1 G_{v1}H_{vc12}H_{vc21}}{1+\beta_1 G_{v1}H_{vc11}})
\end{aligned} \tag{7.20}$$

It is observed from (7.20) that the outer loop gain transfer functions T'_1, T'_2 depend on both controller G_{v1}, G_{v2}. Thus, the design of controller is not independent.

7.2.2.1 Approximated Outer Loop Gains

The outer loop gains is given by (7.20). Controller increases the low frequency gains, and thus we can assume

$$|\beta_1 G_{v1}H_{vc11}| >> 1 \quad , \quad |\beta_2 G_{v2}H_{vc22}| >> 1 \tag{7.21}$$

Applying (7.21) in (7.20), the outer loop gains is approximated as

$$\begin{aligned} T_1' &\approx \beta_1 G_{v1}(H_{vc11} - \frac{H_{vc12}H_{vc21}}{H_{vc22}}) \\ T_2' &\approx \beta_2 G_{v2}(H_{vc22} - \frac{H_{vc12}H_{vc21}}{H_{vc11}}) \end{aligned} \tag{7.22}$$

Using (7.18) in (7.22) and applying (7.10), the approximated outer loop gains can be written as

$$\begin{aligned} T_1' &\approx \frac{\beta_1 G_{v1} f_{m1} G_{vd1}}{1+T_{i1}} = \frac{T_{v1}}{1+T_{i1}} \equiv T_1 \\ T_2' &\approx \frac{\beta_2 G_{v2} f_{m2} G_{vd2}}{1+T_{i2}} = \frac{T_{v2}}{1+T_{i2}} \equiv T_2 \end{aligned} \tag{7.23}$$

where, T_j are the approximated outer loop gains, T_{vj} are the approximated voltage loop gains and G_{vdj} are the approximated duty cycle to output voltage transfer function. G_{vdj} is given by

$$G_{vdj}|_{ideal} = \frac{\frac{V_{in}}{L_{eqj}C_j}}{s^2 + \frac{s}{R_jC_j} + \frac{1}{L_{eqj}C_j}}, \quad G_{vdj}|_{non-ideal} = \frac{\frac{V_{in}r_j'}{L_{eqj}}(s + \frac{1}{r_{cj}C_j})}{s^2 + s(\frac{r_j'}{L_{eqj}} + \frac{r_j''}{C_j}) + \frac{R_j r_j''}{L_{eqj}C_j}} \tag{7.24}$$

Equation (7.23) shows that G_{v1} is related to T_1 and G_{v2} is related to T_2. Thus, the controller design is independent. It is also observed from (7.23), that the controller G_{cj} directly affects T_{vj} and indirectly effects T_j.

7.2.3 Closed-loop Transfer Functions

The stability and closed-loop performance of PCM controlled CI-SIDO buck converter is studied by analysing closed-loop audio susceptibility and load regulations.

7.2.3.1 Closed-loop Audio-susceptibility

The closed-loop audio susceptibility transfer functions can be calculated using (7.19) by making $\hat{v}_{ref1} = \hat{v}_{ref2} = \hat{i}_{01} = \hat{i}_{02} = 0$ and is given by

$$\begin{bmatrix} \hat{v}_{01} \\ \hat{v}_{02} \end{bmatrix} = \begin{bmatrix} \frac{1}{1+T_1'} & \frac{-\beta_2 G_{v2} H_{vc12}}{(1+\beta_2 G_{v2} H_{vc22})(1+T_1')} \\ \frac{-\beta_1 G_{v1} H_{vc21}}{(1+\beta_1 G_{v1} H_{vc11})(1+T_2')} & \frac{1}{1+T_2'} \end{bmatrix} \left(\begin{bmatrix} G_{vg1} \\ G_{vg2} \end{bmatrix} - \begin{bmatrix} G_{vd11} & G_{vd12} \\ G_{vd21} & G_{vd22} \end{bmatrix} \begin{bmatrix} \frac{X_{ig1} - \frac{X_{ig2}X_{12}}{1+X_{22}}}{1+T_{i1}'} \\ \frac{X_{ig2} - \frac{X_{ig1}X_{21}}{1+X_{11}}}{1+T_{i2}'} \end{bmatrix} \right) \begin{bmatrix} \hat{v}_{in} \end{bmatrix} \tag{7.25}$$

Applying (7.10), (7.21) in (7.25), we obtain

$$\begin{bmatrix}\hat{v}_{01}\\ \hat{v}_{02}\end{bmatrix} \approx \begin{bmatrix}\frac{1}{1+T_1} & 0\\ 0 & \frac{1}{1+T_2}\end{bmatrix}\left(\begin{bmatrix}G_{vg1}\\ G_{vg2}\end{bmatrix} - \begin{bmatrix}G_{vd11} & G_{vd12}\\ G_{vd21} & G_{vd22}\end{bmatrix}\begin{bmatrix}\frac{X_{ig1}-\frac{X_{ig2}X_{12}}{X_{22}}}{1+T_{i1}}\\ \frac{X_{ig2}-\frac{X_{ig1}X_{21}}{X_{11}}}{1+T_{i2}}\end{bmatrix}\right)\begin{bmatrix}\hat{v}_{in}\end{bmatrix} \tag{7.26}$$

Using (7.6), expression of G_{vd11}, G_{vd12}, G_{vd21}, G_{vd22} in (7.26) and solving we obtain the closed-loop audio-susceptibility as

$$G_{vg1-cl} = \frac{\hat{v}_{01}}{\hat{v}_{in}}\bigg|_{CL} \approx \frac{(G_{vg1} - \frac{Y_{ig1}}{1+T_{i1}})}{1+T_1}, \quad G_{vg2-cl} = \frac{\hat{v}_{02}}{\hat{v}_{in}}\bigg|_{CL} \approx \frac{(G_{vg2} - \frac{Y_{ig2}}{1+T_{i2}})}{1+T_2} \tag{7.27}$$

where, $Y_{ig1} = G_{vd1}(\frac{k_{g1}}{1-k^2} + \frac{Mf_{m1}k_{g2}}{L_1(1-k^2)f_{m2}} + G_{ig1}r_sf_{m1})$, $Y_{ig2} = G_{vd2}(\frac{k_{g2}}{1-k^2} + \frac{Mf_{m2}k_{g1}}{L_2(1-k^2)f_{m1}} + G_{ig2}r_sf_{m2})$

Without feed-forward gains, i.e., $k_{g1} = k_{g2} = 0$, the closed-loop transfer functions are simplified to

$$G_{vg1-cl}|_{k_{g1}=k_{g2}=0} \approx \frac{(G_{vg1} - \frac{G_{vd1}G_{ig1}r_sf_{m1}}{1+T_{i1}})}{1+T_1}, \quad G_{vg2-cl}|_{k_{g1}=k_{g2}=0} \approx \frac{(G_{vg2} - \frac{G_{vd2}G_{ig2}r_sf_{m2}}{1+T_{i2}})}{1+T_2} \tag{7.28}$$

It is observed from (7.28), that inner loop attenuates the gain of open loop audio-susceptibility G_{vg1}/G_{vg2}, as a result it improves the closed-loop audio-susceptibility G_{vg1-cl}/G_{vg2-cl}. Moreover, it is found from (7.27) that feed-forward gains in PCM control further improves the closed-loop audio-susceptibility.

7.2.3.2 Closed-loop Load Regulation

The closed-loop load regulation transfer functions can be calculated using (7.19) by making $\hat{v}_{ref1} = \hat{v}_{ref2} = \hat{v}_{in} = 0$, applying (7.10), (7.21) and we get

$$\begin{bmatrix}\hat{v}_{01}\\ \hat{v}_{02}\end{bmatrix} \approx \begin{bmatrix}\frac{1}{1+T_1} & 0\\ 0 & \frac{1}{1+T_2}\end{bmatrix}\left(\begin{bmatrix}Z_{vi11} & Z_{vi12}\\ Z_{vi21} & Z_{vi22}\end{bmatrix} - \begin{bmatrix}G_{vd11} & G_{vd12}\\ G_{vd21} & G_{vd22}\end{bmatrix}\begin{bmatrix}\frac{Y_{ii11}-\frac{Y_{ii21}X_{12}}{X_{22}}}{1+T_{i1}} & \frac{Y_{ii12}-\frac{Y_{ii22}X_{12}}{X_{22}}}{1+T_{i1}}\\ \frac{Y_{ii21}-\frac{Y_{ii11}X_{21}}{X_{11}}}{1+T_{i2}} & \frac{Y_{ii22}-\frac{Y_{ii12}X_{21}}{X_{11}}}{1+T_{i2}}\end{bmatrix}\right)\begin{bmatrix}\hat{i}_{01}\\ \hat{i}_{02}\end{bmatrix} \tag{7.29}$$

Using (7.6), expression of G_{vd11}, G_{vd12}, G_{vd21}, G_{vd22} in (7.29) and solving we obtain the approximated closed-loop load-regulation as follows:

Approximated closed-loop self-regulation

$$\begin{aligned} Z_{vi11-cl} &= \left.\frac{\hat{v}_{01}}{-\hat{i}_{01}}\right|_{CL} \approx \frac{1}{1+T_1}(Z_{vi11} + \frac{r_s f_{m1} G_{vd1} H_{ii11}}{1+T_{i1}}) \\ Z_{vi22-cl} &= \left.\frac{\hat{v}_{02}}{-\hat{i}_{02}}\right|_{CL} \approx \frac{1}{1+T_2}(Z_{vi22} + \frac{r_s f_{m2} G_{vd2} H_{ii22}}{1+T_{i2}}) \end{aligned} \tag{7.30}$$

Approximated closed-loop cross-regulation

$$\begin{aligned} Z_{vi12-cl} &= \left.\frac{\hat{v}_{01}}{\hat{i}_{02}}\right|_{CL} \approx \frac{1}{1+T_1}(Z_{vi12} - \frac{r_s f_{m1} G_{vd1} H_{ii12}}{1+T_{i1}}) \\ Z_{vi21-cl} &= \left.\frac{\hat{v}_{02}}{\hat{i}_{01}}\right|_{CL} \approx \frac{1}{1+T_2}(Z_{vi21} - \frac{r_s f_{m2} G_{vd2} H_{ii21}}{1+T_{i2}}) \end{aligned} \tag{7.31}$$

It is observed from (7.30) that, inner loop provides additional gain to the open loop self-regulation transfer function (Z_{vi11}/Z_{vi22}) and thus closed-loop self-regulation is inferior with PCM control compared to VMC. Moreover, from (7.31) it is observed that inner loop provides additional attenuation of open loop cross-regulation and thus closed-loop cross-regulation is improved with PCM control.

7.3 Stability Analysis of Closed-loop System

The stability of the closed-loop system can be analysed using the outer loop gain transfer functions as given in (7.23). The outer loop gain T_j is related with voltage loop T_{vj} and current loop T_{ij} as

$$T_j = \frac{T_{vj}}{1+T_{ij}} = \begin{cases} \frac{T_{vj}}{T_{ij}}, \text{ at low freq. } |T_{i1}| >> 1 \\ T_{vj}, \text{at high freq. } |T_{i1}| << 1 \end{cases} \tag{7.32}$$

From (7.32), it is observed that stability of T_j depends on stability of T_{ij}, T_{vj}. Thus, if T_{vj} or T_{ij} becomes unstable then T_j also become unstable. The stability of T_{ij} depend on slope compensation and stability of T_{vj} depends on controller design. Moreover, to achieve tight regulation, good closed-loop stability and performance, the gain of T_j should be high at low frequency and low at high frequency with sufficient phase margin. For this, the G_{cj} are designed such that T_{vj} should dominate over T_{ij} at low frequency region and T_{ij} should dominate over T_{vj} at high frequency.

Inner Current Loop Stability

As discussed in Section 7.2.1.1, the inner current loop gains become unstable when $D_j > 0.5$. The instability of T_{ij} is prevented by the use of slope compensations. The inner current loop gain transfer function is written in non-dimensional form as

$$T_{ij} = T_{i0}\frac{(1+\frac{s}{\omega_{idj}})}{1+\frac{2\zeta_j s}{\omega_{oj}}+\frac{s^2}{\omega_{oj}^2}} \quad \text{where, } j=\{1,2\} \tag{7.33}$$

where, $T_{i0} = f_{mj}r_s V_{in}/R_j$, $\omega_{oj} = R_j r_j^{''}/C_j L_{eqj}$, $\omega_{idj} = r_j^{''}/C_j$, $\zeta_j = \frac{C_j r_j^{'} + L_{eqj} r_j^{''}}{2\sqrt{L_{eqj}C_j R_j r_j^{''}}}$.

Figure 7.3 show the asymptotic bode plot of T_{ij}. The inner current loop is inherently stable with -20 dB slope at crossover frequency ω_{ci1} with 90° final phase. Moreover, it is found that slope compensation effect the DC gain, resonant frequency. Higher the slope compensation lower is the DC gain and crossover frequency. Therefore, the objective for designing slope compensation is to ensure faster inner current loop. To achieve the objective, the inner loop crossover frequency ω_{ci1} needs to be placed at a higher frequency. The ω_{ci1} of T_{i1} is increases up to the frequency where the small-signal analysis is valid, i.e., half of the switching frequency.

Outer and Voltage Loop Stability

The stability of T_j, T_{vj} depends on the design of controller G_{cj}. To improve the low frequency gain Type-II compensator is used. The transfer function of T_{vj} is given in (7.23) and is written in non-dimensional form as

$$T_{vj} = \beta_j f_{mj} G_{cj} G_{vdj} = T_{v0}\frac{(1+\frac{s}{\omega_{esrj}})(1+\frac{s}{\omega_{cj-z}})}{s(1+\frac{2\zeta_j s}{\omega_{oj}}+\frac{s^2}{\omega_{oj}^2})(1+\frac{s}{\omega_{cj-p}})} \tag{7.34}$$

where, $T_{v0} = \beta_j f_{mj} k_{cj} V_{in}$, $\omega_{esrj} = \frac{1}{r_{cj}C_j}$, $\omega_{oj} = \sqrt{\frac{R_j r_j^{''}}{L_{eqj}C_j}}$, $\zeta_j = \frac{C_j r_j^{'} + L_{eqj} r_j^{''}}{2\sqrt{L_{eqj}C_j R_j r_j^{''}}}$

Figure 7.3 shows the asymptote bode plot plots of T_{ij}, T_{vj}, T_j. The compensator pole ω_{cj-p} is placed after ESR zero to ensure dominance of T_{ij} at high frequency. The compensator zero ω_{cj-z} is placed before complex pole frequency ω_{oj} to avoid conditional stability of T_{vj}.

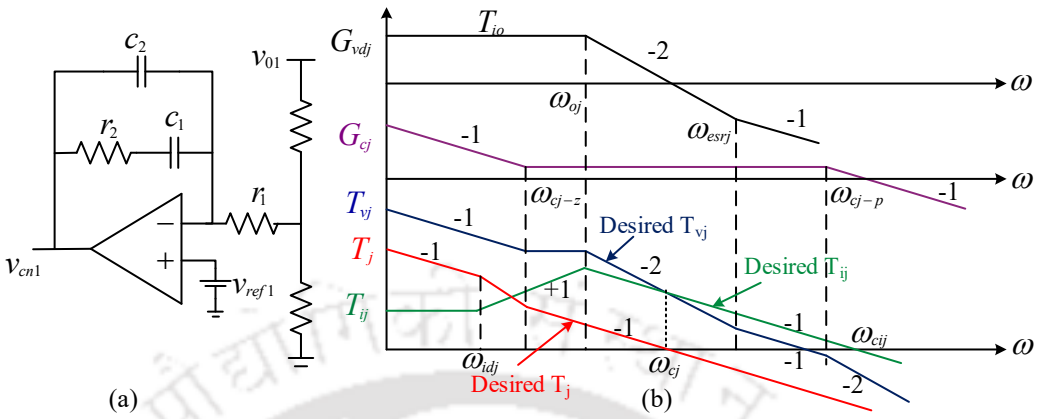


Figure 7.3: Proposed controller design (a) Circuit diagram of Type-II compensator (b) Desire characteristics of loop gains T_{ij}, T_{vj}, T_j

7.4 Proposed Controller Design Procedure

Based on the analysis discussed in Section 7.2, Section 7.3, design procedure for PCM controlled CI-SIDO buck converter is established. Firstly, slope compensations are designed to prevent current loop instability and ensure fast response than voltage loop. Second, the controllers are designed to improve closed-loop stability and performance.

7.4.1 Slope Compensation Design

The design procedure is as follows:

(i) Choose the crossover frequency of T_{ij}: Select w_{cij} between $0.2\omega_s$ to $0.5\omega_s$

(ii) Determine the DC gain of T_{ij}, i.e., T_{i0}: From Fig. 7.3(b) the DC gain T_{i0} is

$$20log(T_{i0}) + 20log(\frac{\omega_{ioj}}{\omega_{idj}}) - 20log(\frac{\omega_{cij}}{\omega_{ioj}}) = 0\ dB$$
$$\implies T_{i0}(\frac{\omega_{ioj}}{\omega_{idj}})\frac{\omega_{ioj}}{\omega_{cij}} = 1 \implies T_{i0} = \frac{\omega_{cij}\omega_{idj}}{\omega_{ioj}^2} \tag{7.35}$$

(iii) Determine the required slope compensation m_{cj}:

Using (7.35), (7.12) in $T_{i0} = f_{mj}r_sV_{in}/R_j$, the m_{cj} is

$$m_{cj} = \frac{r_sV_{in}}{T_s\omega_{cij}L_j} - \frac{V_{in}(1-2D_j)}{2L_j} \tag{7.36}$$

Equation (7.36) clarifies that the condition (7.13) is satisfied for $D_j > 0.5$.

7.4.2 Compensator Design

Based on desired characteristic as shown in Figure 7.3(b) the design procedure is as follows:

(i) Place Controller zero ω_{cj-z}: Place ω_{cj-z} before ω_{oj} to provide 90° phase boost for preventing conditional stability of T_{vj}. As a thumb rule, place ω_{cj-z} at

$$\omega_{cj-z} = 0.8\omega_{oj} \tag{7.37}$$

(ii) Place Controller pole ω_{cj-p}: Place ω_{cj-p} at $\omega_{cj-p} = 2\omega_{esrj}$ to ensure dominance of T_{ij} at high frequency.

(iii) Choose crossover frequency ω_{cj} of outer loop T_j: Select ω_{cj} of T_j less that ω_{esr} to ensure faster inner current loop and good load regulation. Thus, ω_{cj} is

$$\omega_{cj} = 0.4\omega_{esrj} \tag{7.38}$$

(iv) Calculate controller gain k_{cj}: Based on Figure 7.3(b), the controller gain is

$$k_{cj} = \frac{r_s\omega_{cj}\omega_{cj-z}}{\omega_{idj}\beta_j R_j} \tag{7.39}$$

(v) Calculate circuit parameter of G_{cj}: Use (7.37)-(7.39) to calculate the controller parameter (r_1, r_2, c_1, c_2)

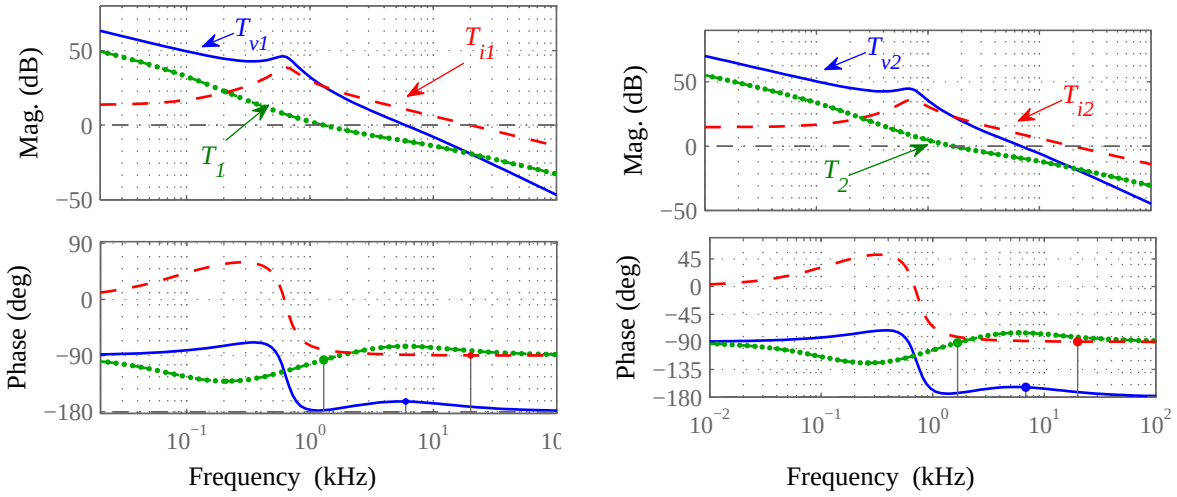
7.4.3 Design Example

The slope compensation and controller are designed using the circuit parameter shown in Table 7.1.

Slope Compensation Design: The inner loops crossover frequency are chosen as $f_{ci1} = f_{ci2} = 20$ kHz. Using the circuit parameter values as given in Table 7.1 in (7.36), the slope compensations are found as $m_{c1} = 20941$ V/s, $m_{c2} = 12827$ V/s. Figure 7.4 shows the bode plots of current loop gains T_{i1}, T_{i2} and is observed that with designed slope compensation, required crossover frequency is achieved.

Table 7.1: Design parameter of CI-SIDO buck converter

Parameter	V_{in}	V_{01}, V_{02}	C_1, C_2	R_1, R_2	$r_{c1} = r_{c2}$
Value	10 V	5 V, 3.3 V	320 μF, 320 μF	5 Ω, 3.3 Ω	0.15 Ω
Parameter	r_s	L_1, L_2	M	f_s	$\beta_1 = \beta_2$
Value	0.5	190 μH ,180 μH	130 μH	100 kHz	1/3



(a) (b)

Figure 7.4: Bode plots of loop gains (a) T_{i1}, T_{v1}, T_1 (b) T_{i2}, T_{v2}, T_2

Controller Design: Using the parameter shown in Table 7.1, $\omega_{esr1} = \omega_{esr2} = 1/r_{c1}C_1 = 20833$ rad/sec, $\omega_{o1} = 4000$ rad/sec, $\omega_{o2} = 4520$ rad/sec, $\omega_{id1} = 607$ rad/sec, $\omega_{id2} = 906$ rad/sec. From (7.38), the crossover frequency of outer loop is found as $f_{c1} = f_{c2} = 1.32$ kHz. Using (7.37)-(7.39), the parameter of G_{v1}, G_{v2} are calculated as $\omega_{c1-z} = 3200$ rad/sec, $k_{c1} = 13179$, $\omega_{c2-z} = 3616$ rad/sec, $k_{c2} = 15116$, $\omega_{c1-p} = \omega_{c2-p} = 41666$ rad/sec. The designed G_{v1}, G_{v2} transfer functions are

$$G_{v1} = \frac{13179(1 + 3.125 * 10^{-4}s)}{s(1 + 2.4 * 10^{-5}s)}, \quad G_{v2} = \frac{15116(1 + 2.76 * 10^{-4}s)}{s(1 + 2.4 * 10^{-5}s)} \tag{7.40}$$

Figure 7.4 shows the bode plot of loop gains. From Figure 7.4(a), it is observed that with designed controller, T_1 follows T_{v1} at low frequency region and follow T_{i1} at high frequency with phase margin $PM = 86°$. Same observation is seen for T_2 in Figure 7.4(b) with phase margin 88°.

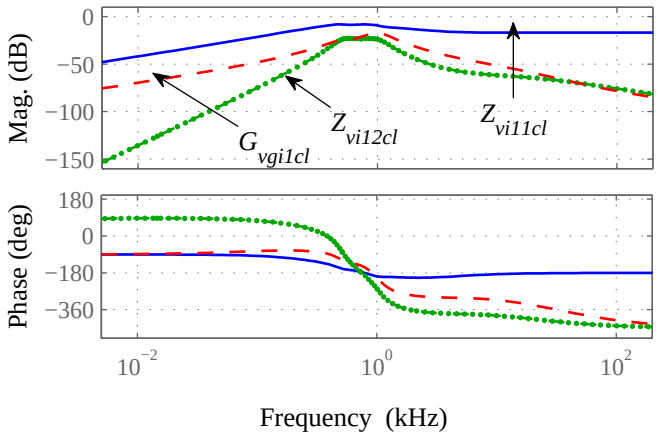


Figure 7.5: Bode plots of closed-loop transfer functions G_{vg1cl}, Z_{vi12cl}, Z_{vi11cl}

7.5 Simulation Results and Analysis

To evaluate the performance of the PCM controlled CI-SIDO buck converter, simulation studied are conducted in MATLAB SIMULINK environment. The parameter of the converter are shown in Table 7.1.

7.5.1 Frequency Domain Analysis

The closed-loop performance of the proposed PCM control is analysed using bode plots of cross-regulation Z_{vi12cl}, audio-susceptibility G_{vg1cl}, self-regulation Z_{vi11cl} as shown in Figure 7.5. It is observed that the low frequency gains of Z_{vi12cl}, G_{vg1cl} are lower than Z_{vi11cl} which means cross-regulation, audio-susceptibility are better than self-regulation. The reason behind inferior self-regulation is that inner current loop provides additional gain to self-regulation transfer function as shown in (7.30) as a result of which the gain of Z_{vi11cl} increases.

7.5.2 Time Domain Analysis

7.5.2.1 Steady-state Performance

The simulated waveform of proposed PCM control with slope compensation is shown in Figure 7.6. Figure 7.6(a) shows the waveform of control inputs and gate pulses. As shown in Figure 7.6(a), gate pulses d_1, d_2 are generated when sensed inductor currents $r_{s1}i_{L1}$, $r_{s2}i_{L2}$ reaches the control input $v_{cn1} - v_{slope1}$, $v_{cn2} - v_{slope2}$, respectively. Figure 7.6(b) shows the

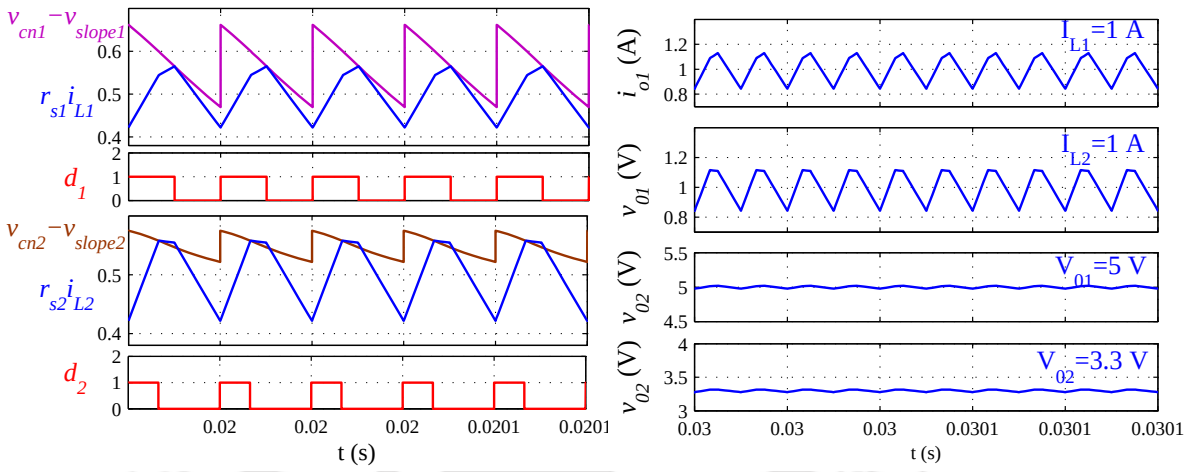


Figure 7.6: Steady-state simulation results (a) Gate signals (b) Inductor currents and output voltages

steady-state inductor currents and output voltage waveforms. It is observed that the proposed controller and slope compensation is able to regulate v_{01} and v_{02} at 5 V and 3.3 V and achieve stability.

7.5.2.2 Dynamic Performance

The dynamic performance of the PCM controlled CI-SIDO buck converter is studied using transient response of output voltages for step change in load currents, reference voltages and input voltage.

Load Regulation: Figure 7.7 shows the simulation results for step change is load current. Figure 7.7(a) shows the results for step change in i_{01} from 1 A to 2 A keeping i_{02} constant at 1 A. It is observed that when i_{01} is step changed, v_{01} experience self-regulation (undershoot) of 0.2 V with settling time 0.8 ms and v_{02} experience cross-regulation (overshoot) of 0.02 V with settling time 0.1 ms. Similarly, Figure 7.7(b) shows the simulation results for step change in i_{02} from 1 A to 2 A keeping i_{01} constant at 1 A. It is observed that the v_{01} under goes overshoot (cross-regulation) of 0.03 V with settling time 0.1 ms and v_{02} under goes undershoot (self-regulation) of 0.2 V with settling time 0.8 ms.

Cross-coupling Figure 7.8 shows the simulation results for step change in reference voltage. In Figure 7.8(a), when v_{ref1} is change from 1.6 V to 1.83 V, v_{01} changes from 4.8 V to 5.5 V and

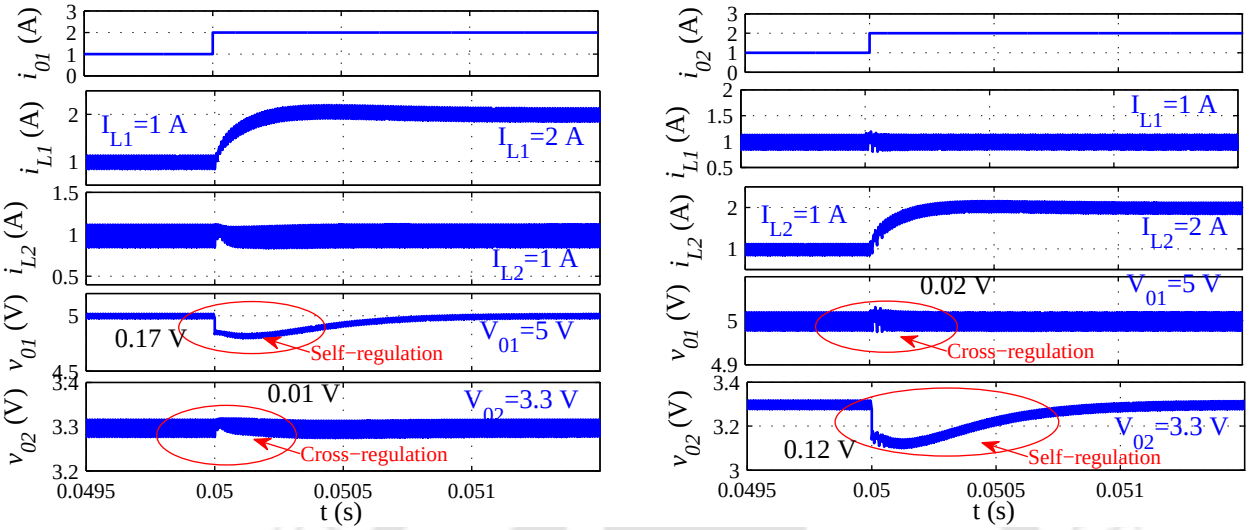


Figure 7.7: Simulation results for load regulation (a) Step change in i_{01} (b) Step change in i_{02}

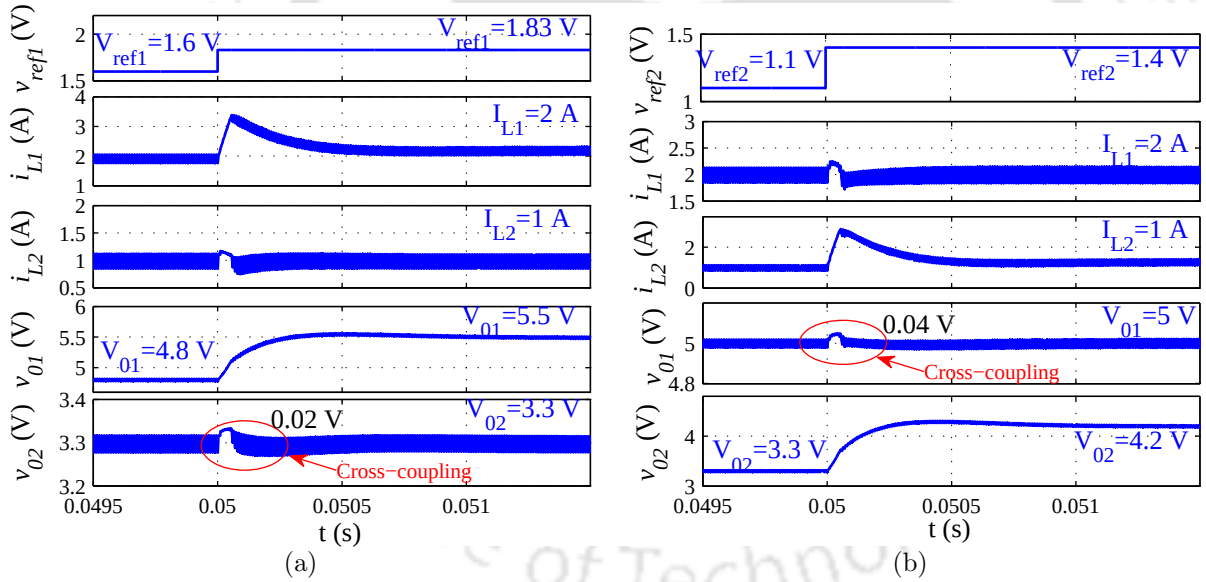


Figure 7.8: Simulation results for cross-coupling (a) Step change in v_{ref1} (b) Step change in v_{ref2}

v_{02} experience negligible cross-coupling effect of 30 mV with settling time 0.1 ms. Similarly, in Figure 7.8(b), when v_{ref2} changes from 1.1 V to 1.4 V then v_{02} changes from 3.3 V to 4.2 V and v_{01} experience cross-coupling of 50 mV with settling time 0.1 ms.

Audio-susceptibility Figure 7.9 shows the simulation results for step change in input voltage. It is observed that when input voltage v_{in} is step changed from 10 V to 12 V, v_{01}, v_{02} experience negligible audio-susceptibility effect.

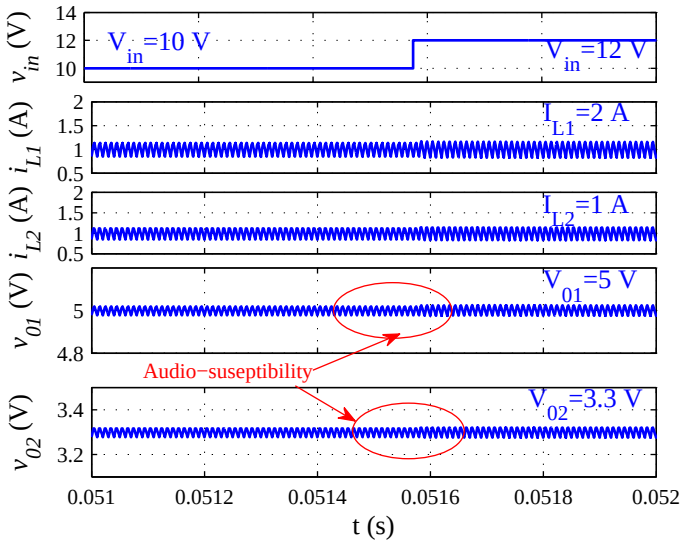
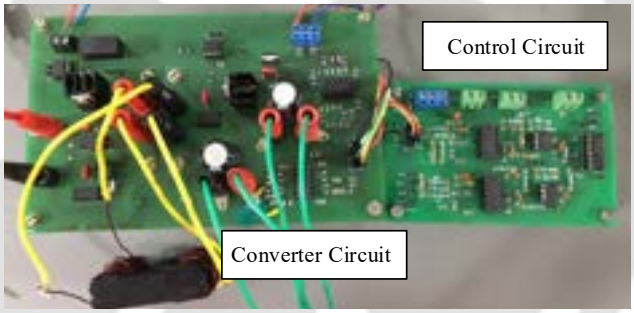


Figure 7.9: Simulation results for audio-susceptibility (step change in v_{in})



(a)

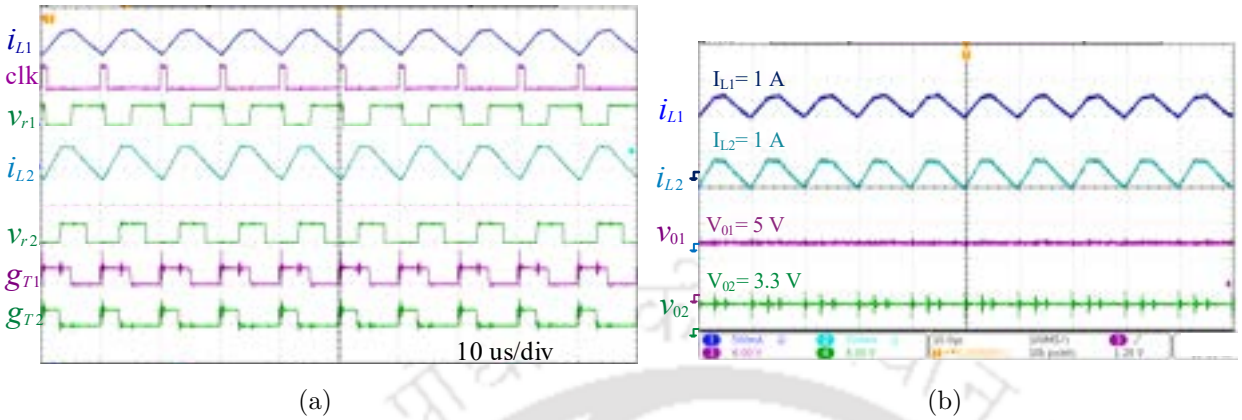
Figure 7.10: Experimental set-up of peak current mode controlled CI-SIDO buck converter

7.6 Experimental Results

The peak current-mode (PCM) CI-SIDO buck converter is validated experimentally by developing an experimental prototype as shown in Figure 7.10. The PCM control is realized using OpAmp LF347N, SR latch CD4043, comparator LM311. The clock signal and slope compensation are generated using a signal generator. The parameter values are used in experiment is same as used in simulation (Table 7.1).

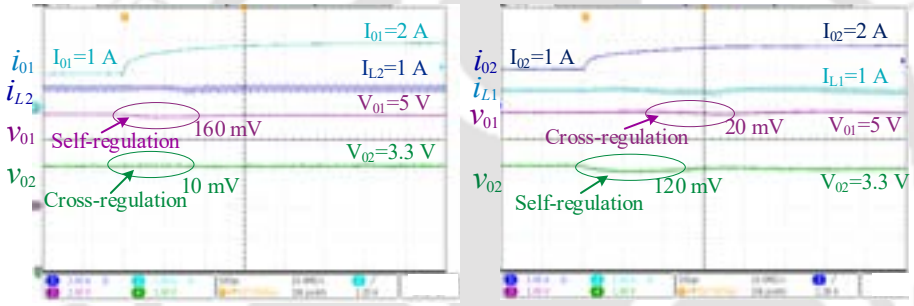
7.6.1 Steady-state Performance

The experimental waveform of proposed PCM control with slope compensation is shown in Figure 7.11. Figure 7.11(a) shows the waveform of control inputs, i,e., set, reset to SR flip-flops,



(a) (b)

Figure 7.11: Experimental steady state results



(a) (b)

Figure 7.12: Experimental results for load regulation (a) step change in i_{01} (b) step change in i_{02}

gate pulses and i_{L1}, i_{L2} in order to explain the operation of PCM control. As shown in Figure 7.11(a), clk sets the SR flip-flops, turns on the S_{T1}, S_{T2}. When resets v_{r2} is on, S_{T2} is turned off. When reset v_{r1} is on, S_{T1} is turned off. It is observed from Figure 7.11(b) that the proposed controller and slope compensation is able to regulate v_{01} and v_{02} at 5 V and 3.3 V and achieve stability.

7.6.2 Dynamic Performance

7.6.2.1 Load Regulation

The experimental results for load regulation are shown in Figure 7.12. For 100% step change in load current i_{01} as shown in Figure 7.12(a), the output voltages v_{01} experience self-regulation (undershoot) of 0.16 V, v_{02} experience a negligible cross-regulation of 0.01 V with settling time 200 μs. Similarly, for 100 % step load change in i_{02} as shown in Figure 7.12(b), v_{02} experience

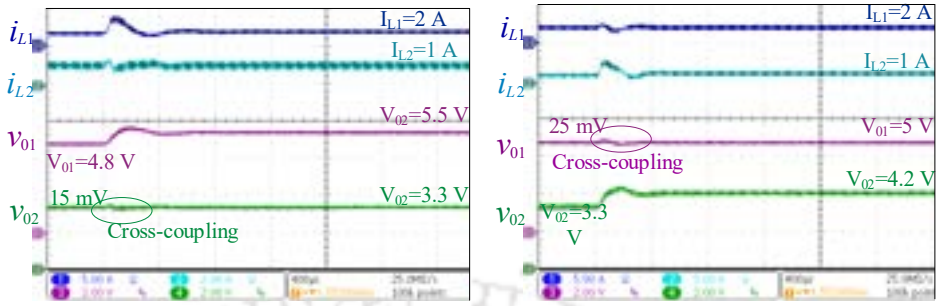


Figure 7.13: Experimental results for cross-coupling (a) step change in v_{ref1} (b) step change in v_{ref2}

self-regulation of 0.12 V, v_{01} experience negligible cross-regulation of 0.02 V with settling time 200 μs.

7.6.2.2 Cross-coupling

The response of output voltages v_{01}, v_{02} for step change in reference voltage v_{ref1}, v_{ref2} are depicted in Figure 7.13. In Figure 7.13(a), when v_{ref1} is change from 1.6 V to 1.83 V, v_{01} changes from 4.8 V to 5.5 V and v_{02} experience negligible cross-coupling effect of 20 mV. Similarly, in Figure 7.13(b), when v_{ref2} changes from 1.1 V to 1.4 V then v_{02} changes from 3.3 V to 4.2 V and v_{01} experience cross-coupling of 40 mV. From Figure 7.13, it can be conclude that with PCM control, the cross-coupling effect is negligible.

7.6.2.3 Audio-susceptibility

The experimental result for audio-susceptibility is shown in Figure 7.14. For step change in input voltage from 10 V to 12 V, the output voltages v_{01}, v_{02} experience negligible audio-susceptibility effect. Thus, audio-susceptibility is improved with PCM control.

7.6.3 Performance Comparison

The closed-loop performance of the proposed PCM control for CI-SIDO buck converter is evaluated based on the performance indices discussed in chapter 4. Based on the simulation and experimental results, the performance indices of PCM controlled CI-SIDO buck converter

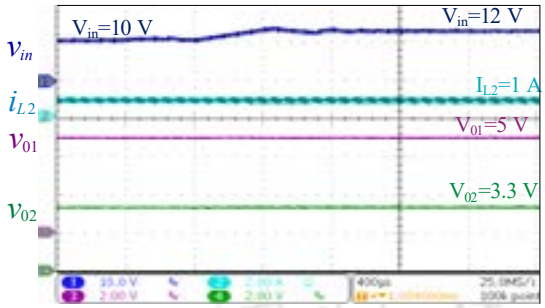


Figure 7.14: Experimental results for audio-susceptibility (step change in v_{in})

Table 7.2: Comparison with existing methods of SIDO Buck converter

References	[34]	[38]	[46]	Chapter 4	Chapter 5	This Chapter
Topology	SI-SIDO	SI-SIDO	SI-SIDO	CI-SIDO	CI-SIDO	CI-SIDO
Control method	State feedback	Model predictive	Current ripple control	Decoupled voltage	Decoupled average current	PCM control
Input	4.8 V	20 V	10 V	10 V	10 V	10 V
Output	3.3 V, 1.2 V	12 V, 8 V	5 V, 3.3 V	6 V, 3.3 V	6 V, 3.3 V	5 V, 3.3 V
Load current	0.1 A, 0.1 A	1.2 A-2.4 A 0.8 A-2.0 A	2.5 A, 1.1 A	0.5 A - 3 A 0.5 A - 3 A	1 A - 2.5 A, 1 A - 2.5 A	1 A-2.5 A , 1 A- 2.5 A
Output power	0.45 W	39 W	16 W	28 W	24 W	21 W
f_s	100 kHz	100 kHz	50 kHz	100 kHz	100 kHz	100 kHz
Transient time	*	444 μs	150 μs	220 μs	200 μs	200 μs
SRI_1	0.033	0.014	*	0.03	0.033	0.033
SRI_2	0.03	0.019	*	0.024	0.036	0.036
CRI_1	0.015	0.025	0.04	0.016	0.008	**0.004**
CRI_2	0.013	0.01	0.006	0.015	0.006	**0.003**
CCI_1	*	0.27	*	0.059	0.046	**0.029**
CCI_2	*	*	*	0.096	0.12	**0.042**
ASI_1	*	*	*	0.025	0.016	**0**
ASI_2	*	*	*	0.037	0.022	**0**

* value not reported

are calculated as follows

$$\begin{aligned} \text{SRI}_1 = \frac{\Delta V_{01}/V_{01}}{\Delta I_{01}/I_{01}} = \frac{0.16/5}{1/1} = 0.032\ ,\ \text{SRI}_2 = \frac{\Delta V_{02}/V_{02}}{\Delta I_{02}/I_{02}} = \frac{0.12/3.3}{1/1} = 0.036 \\ \text{CRI}_1 = \frac{\Delta V_{01}/V_{01}}{\Delta I_{02}/I_{02}} = \frac{0.02/5}{1/1} = 0.004\ ,\ \text{CRI}_2 = \frac{\Delta V_{02}/V_{02}}{\Delta I_{01}/I_{01}} = \frac{0.01/3.3}{1/1} = 0.003 \\ \text{ASI}_1 = \frac{\Delta V_{01}/V_{01}}{\Delta V_{in}/V_{in}} \approx 0\ ,\ \text{ASI}_2 = \frac{\Delta V_{02}/V_{02}}{\Delta V_{in}/V_{in}} \approx 0 \\ \text{CCI}_1 = \frac{\Delta V_{01}/V_{01}}{\Delta V_{ref2}/V_{ref2}} = \frac{0.04/5}{0.3/1.1} = 0.029\ ,\ \text{CCI}_2 = \frac{\Delta V_{02}/V_{02}}{\Delta V_{ref1}/V_{ref1}} = \frac{0.02/3.3}{0.23/1.6} = 0.042 \end{aligned} \tag{7.41}$$

The closed-loop performance of PCM control CI-SIDO buck converter is compared with the decoupled VMC discussed in Chapter 4, decoupled ACC discussed in Chapter 5 and existing methods for SI-SIDO converter and is tabulated in Table 7.2. From the Table 7.2, it is observed that proposed PCM control for CI-SIDO buck has cross-regulation index CRI as 0.004 which is

less compared to other methods. Moreover, the cross-coupling and audio-susceptibility index of PCM controlled CI-SIDO buck converter is less compare to decoupled VMC and decoupled ACC. Thus, it is concluded that PCM control is a promising control method for CI-SIDO buck converter to suppress cross-regulation with improve dynamic performance.

7.7 Conclusion

In this chapter, a peak current mode (PCM) control is proposed for CI-SIDO buck converter to minimize cross-regulation with improved dynamic performance. PCM controlled CI-SIDO buck suffers from sub-harmonic oscillation problem when any one or both duty cycles are greater than 0.5. Thus, to design slope-compensation and controller, the small-signal model of PCM controlled CI-SIDO buck converter is analysed and simplified to obtain loop gain transfer functions. By studying the stability of loop gain transfer functions, the design criteria of slope compensation and controller is derived to prevent sub-harmonic oscillation and improve closed-loop performance. Based on the design criteria, a design procedure for slope compensation and controller is proposed and verified experimentally. The experimental results confirms that PCM control suppresses the cross-regulation of CI-SIDO buck converter with improved dynamic performance.

8

Conclusion and Future Scope

Contents

8.1 Conclusion

Applications like electric vehicle, LED drivers, portable devices, etc., are moving towards miniaturization. Its power management unit demands compactness, better efficiency, longer battery life and regulated voltages. Coupled-inductor single input dual outputs (CI-SIDO) DC-DC converter can be a better alternative to multiple DC-DC converters to meet these requirements. Using coupled inductor instead of multiple inductors can reduce the size and volume of the converter while reducing ripple, increasing efficiency, and increasing transient response. However, with its advantages, the CI-SIDO converter is affected by instability, cross-regulation and cross-coupling problems. CI-SIDO converter can be classified into three categories based on the output voltage level, i.e., CI-SIDO buck converter, CI-SDO boost converter, CI-SIDO boost and buck converter. The CI-SIDO buck converter only provides buck outputs; the CI-SIDO boost converter only provides boost outputs; the CI-SIDO boost and buck converter provides both boost and buck outputs.

Unlike conventional basic DC-DC converters, the circuit operation and control of the CI-SIDO converter are quite complex. A proper understanding of the converter steady-state and dynamic behaviour needs an accurate small-signal model. A control technique also needs to be adopted to independently regulate the output voltages with reduced cross-coupling and cross-regulation effect.

This thesis presents the small-signal modelling of three topologies of CI-SIDO converter, i.e., CI-SIDO buck converter, CI-SIDO boost converter, CI-SIDO boost and buck converter using the state-space averaging technique. The developed small-signal model can predict the steady-state and dynamic performance of the converter accurately. From the model, it is observed that mutual coupling doesn't affect the CI-SIDO converter's steady-state behaviour, i.e., the CI-SIDO converters behave the same as that of SISO converters in steady-state. However, the mutual coupling affects the CI-SIDO converter's dynamic behaviour, i.e., due to coupling, the CI-SIDO converter's order becomes 4th order with extra complex zeros and additional cross-coupling and cross-regulation transfer functions.

The effect of coefficient of coupling k on the converter's transfer functions is analyzed in detail. The analysis shows that with the increase in the coefficient of coupling k, the pole and zeros vary, and the converter has interlaced pole-zero distribution. With an interlaced pole-zero distribution converter, the controller design is easy. However, it is observed that with the increase in k, the complex zero moves to the right half-plane, which causes instability and also experience multiple resonant peaks and may lead to conditional stability. Moreover, it is found that with the increase in k, the cross-coupling and cross-regulation effect increases. Therefore, to prevent RHP complex zero, conditional stability, and reduce cross-coupling, cross-regulation effect, moderate coupling is preferred for CI-SIDO converter.

As mentioned CI-SIDO converter has the issue of cross-coupling, due to which independent control of output voltages is challenging. Therefore, to independently control the output voltages, a method of decoupling the cross-coupling problem in CI-SIDO buck converter under voltage-mode control (VMC) and average current control (ACC) is proposed in this thesis. The decoupling process allows the controller to be designed with high gain or high gain crossover frequency. However, with high controller gain, the stability of the closed-loop system is affected. Therefore, a design procedure for the controller is proposed considering decoupling and stability criteria under both VMC and ACC. The presented decoupling method under VMC and ACC is validated in both simulation and experiment. The results show that the proposed decoupled method under VMC and ACC satisfactorily regulates and approximately decouples the output voltages and reduces self and cross-regulations and audio-susceptibility.

To further reduce the cross-regulation effect, a peak current mode (PCM) control is introduced for CI-SIDO converters. To design controller and slope compensation for PCM controlled CI-SIDO converter, an accurate small-signal model of the system is needed. Therefore, a unified small-signal model for PCM controlled CI-SIDO converter is developed, which can predict the instability and dynamic performance of CI-SIDO converter under PCM control. The developed unified model is validated in both simulation and experiment. Moreover, using the unified small-signal model of PCM controlled CI-SIDO buck converter, the design procedure for slope-compensation and controller is proposed and verified through simulation and experimental

results. The experimental results reveal that PCM control suppresses the cross-regulation, cross-coupling of the CISIDO buck converter with good dynamic performance.

8.2 Future Scope

The future possible direction of this research work which are worth to explore are given as follows:

- This thesis has proposed the decoupled method under voltage-mode control and average current mode control for CI-SIDO converters. The decoupled method is implemented for the CI-SIDO buck converter, and it is observed that the decoupled plant transfer function becomes the same as that of the simple buck converter. Thus, the outputs of the CI-SIDO buck converter is regulated by proper designing Type-II compensators. However, the decoupled method, when implemented for CI-SIDO boost converter, CI-SIDO boost and buck converter, it is observed that the decoupled plant transfer function becomes unstable non-minimum phase system. As a result, it is challenging to regulate the converter using Type-II/III compensator. Therefore, further research on controller design for unstable non-minimum phase system is required.

- This thesis has proposed the unified small-signal model of peak current mode controlled CI-SIDO converters. The model is derived by assuming the peak inductor current equal to the reference inductor current. This assumption is only valid when coupled inductor parameters are chosen such that the inductor currents slopes $m_{NF1} > 0$, $m_{NF2} < 0$, $m_{FN1} < 0$, $m_{FN2} > 0$. The developed unified model with the assumption shows a maximum of 5% error between the experimental and ideal analytical model results. Therefore, further research on developing an accurate model for PCM controlled CI-SIDO converter considering all possible inductor currents slopes patterns need to be developed to accurately predict the system's dynamic performance.

- This thesis has proposed the controller design procedure for PCM controlled CI-SIDO

buck converter. Further research can be carried out on design of PCM control for CI-SIDO boost converter, CI-SIDO boost and buck converter.

- In this thesis, analysis and small-signal model is developed for CI-SIDO buck converter, CI-SIDO boost converter, CI-SIDO boost and buck converter. Further research can be carried out on modelling, design and control of CI-SIDO buck-boost converter.
- In this thesis, control techniques are proposed for CI-SIDO converters. Further research can be carried out on developing control techniques for coupled inductor single input three output (CI-SITO) converters.

A

Appendix A

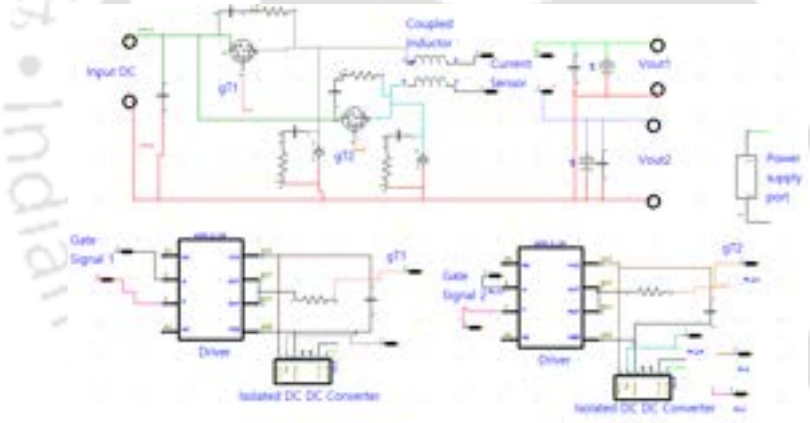
Contents

A.1 PCB Design Layout of Converter Circuit

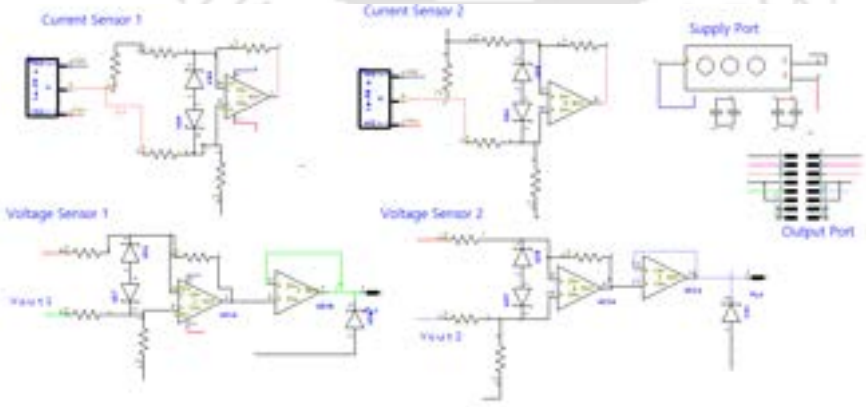
The hardware prototype of three topologies of CI-SIDO converter and its sensor circuit and control circuit is developed to conduct the experimental required for the research work.

A.1.1 CI-SIDO Buck Converter

The schematic design and PCB design layout of CI-SIDO buck converter and its sensor circuit is carried out in DESIGN SPARK PCB software. Figure A.1 shows the schematic design of CI-SIDO buck converter circuit and its sensor circuit. Figure A.2 shows the PCB design layout of CI-SIDO buck converter along with its sensor circuit. Figure A.3 shows the prototype of CI-SIDO buck converter.



(a)



(b)

Figure A.1: Schematic design layout (a) CI-SIDO buck converter circuit (b) Sensor circuit

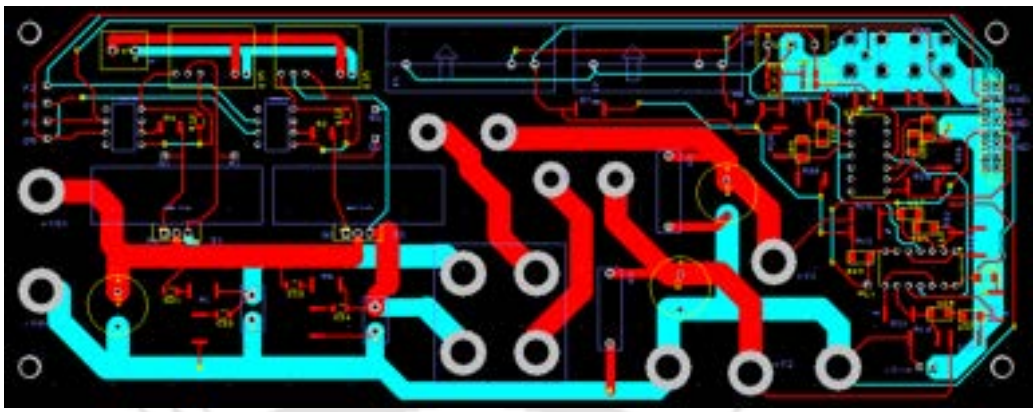


Figure A.2: PCB design layout of CI-SIDO buck converter along with sensor circuit

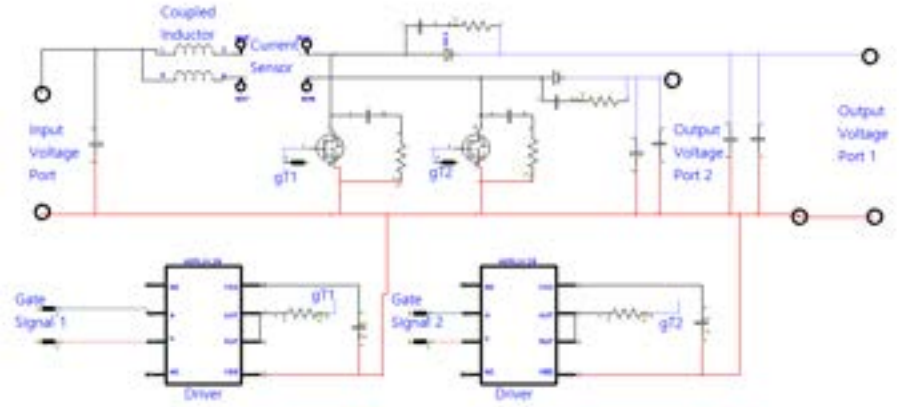
Figure A.3: Prototype of CI-SIDO buck converter

A.1.2 CI-SIDO Boost Converter

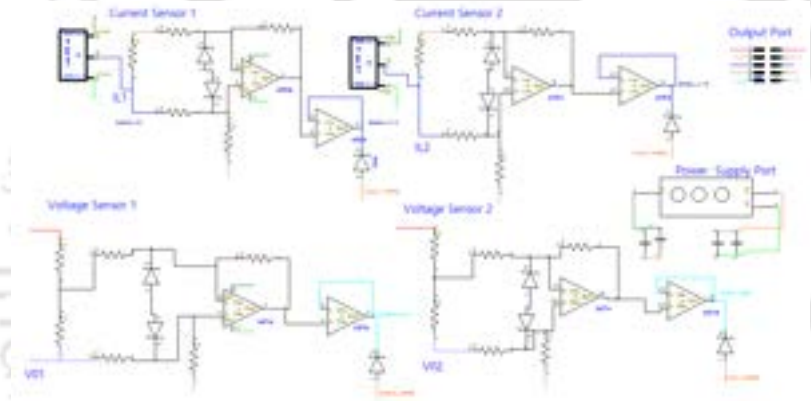
Figure A.4 shows the schematic design of CI-SIDO boost converter circuit and its sensor circuit. Figure A.5 shows the PCB design layout of CI-SIDO boost converter along with sensor circuit. Figure A.6 shows the prototype of CI-SIDO boost converter.

A.1.3 CI-SIDO Boost and Buck Converter

Figure A.7 shows the schematic design of CI-SIDO boost and buck converter circuit and its sensor circuit. Figure A.8 shows the PCB design layout of CI-SIDO boost and buck converter along with sensor circuit. Figure A.9 shows the prototype of CI-SIDO boost and buck converter.



(a)



(b)

Figure A.4: Schematic design layout (a) CI-SIDO boost converter circuit (b) Sensor circuit

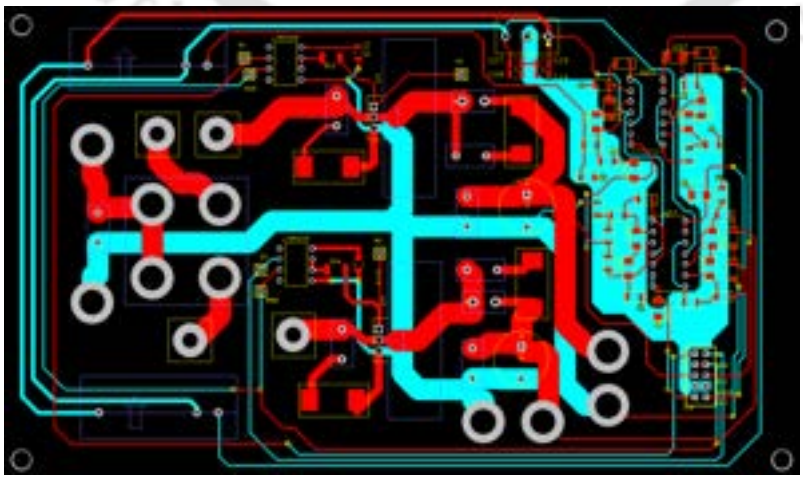


Figure A.5: PCB design layout of CI-SIDO boost converter along with sensor circuit

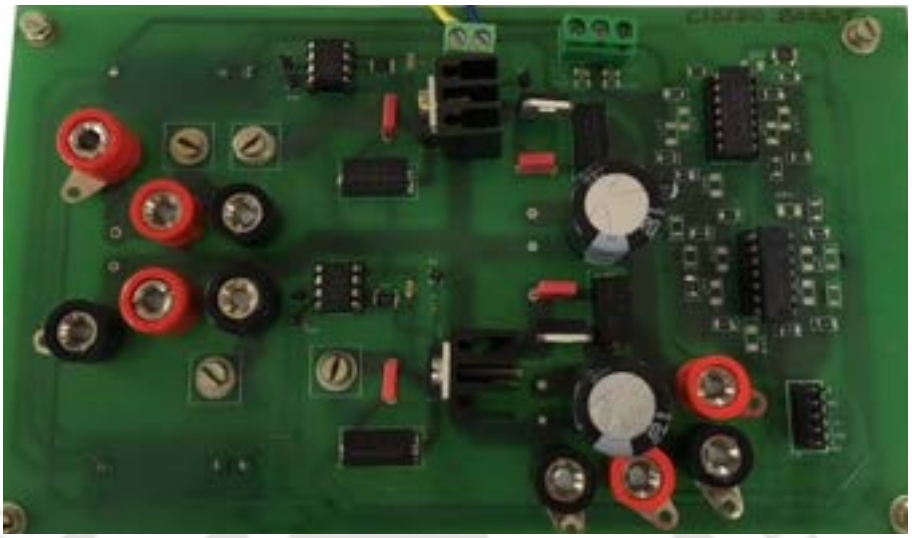
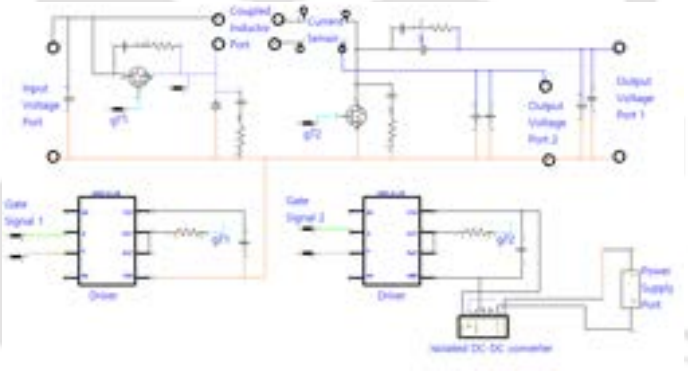
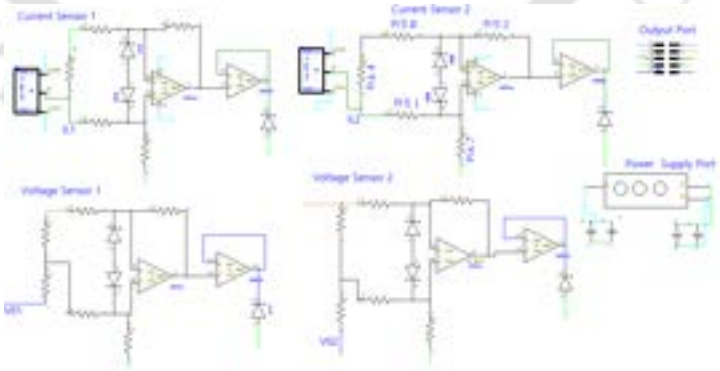


Figure A.6: Prototype of CI-SIDO boost converter



(a)



(b)

Figure A.7: Schematic design layout (a) CI-SIDO boost and buck converter circuit (b) Sensor circuit

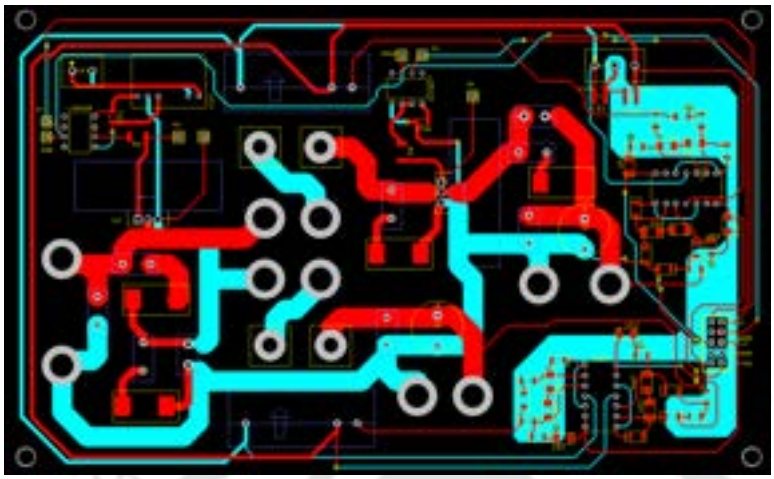


Figure A.8: PCB design layout of CI-SIDO boost and buck converter along with sensor circuit

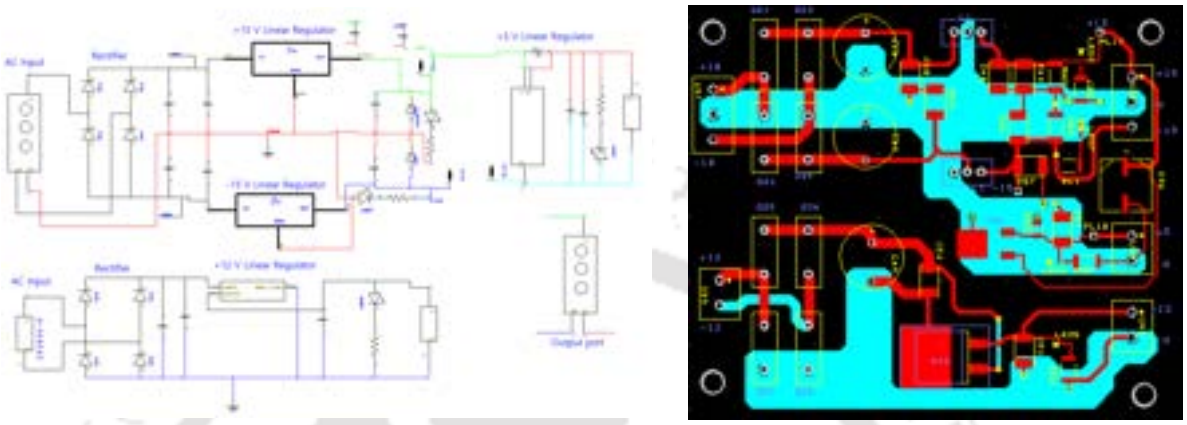
Figure A.9: Prototype of CI-SIDO boost and buck converter

A.2 PCB Design Layout of Power Supply Circuit

Figure A.10 shows the schematic and PCB design layout of power supply circuit. Figure A.11 shows the prototype of power supply circuit.

A.3 PCB Design Layout of Control Circuit

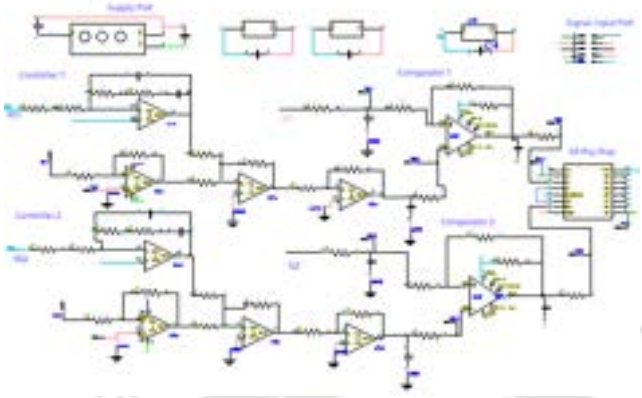
Figure A.12 shows the schematic and PCB design layout of peak current mode control circuit. Figure A.13 shows the prototype of peak current mode control circuit.



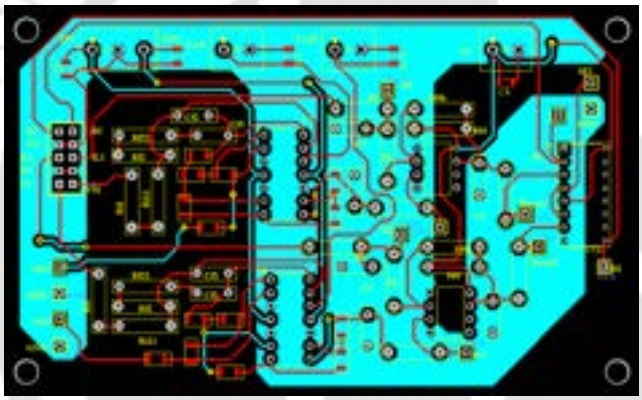
(a) (b)

Figure A.10: Schematic and PCB design layout of power supply circuit (a) Schematic design (b) PCB design

Figure A.11: Prototype of power supply circuit prototype



(a)



(b)

Figure A.12: Schematic and PCB design layout of peak current mode control circuit (a) Schematic design (b) PCB design

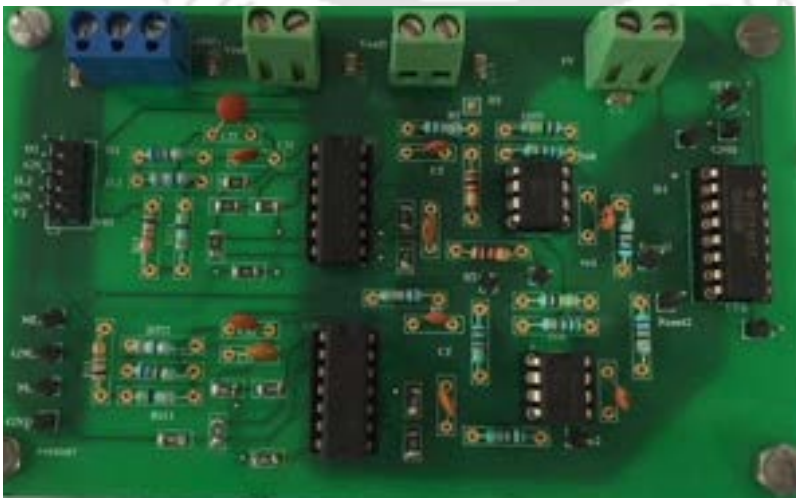


Figure A.13: Prototype of peak current mode control

References

[1] H. Kim, C. S. Yoon, D. Jeong, and J. Kim, "A single-inductor, multiple-channel current-balancing led driver for display backlight applications," *IEEE Transactions on Industry Applications*, vol. 50, no. 6, pp. 4077–4081, Nov. 2014.

[2] G. Chen, Y. Deng, J. Dong, Y. Hu, L. Jiang, and X. He, "Integrated multiple-output synchronous buck converter for electric vehicle power supply," *IEEE Transactions on Vehicular Technology*, vol. 66, no. 7, pp. 5752–5761, Jul. 2017.

[3] C. Li, W. Huang, R. Cao, F. Bu, and C. Fan, "An integrated topology of charger and drive for electric buses," *IEEE Transactions on Vehicular Technology*, vol. 65, no. 6, pp. 4471–4479, Jun. 2016.

[4] J. Choi and H. Cha, "A processor power management scheme for handheld systems considering off-chip contributions," *IEEE Transactions on Industrial Informatics*, vol. 6, no. 3, pp. 255–264, Aug. 2010.

[5] L. Zhang, X. Ma, and Y. Ye, "Research on cross-regulation characteristic of flyback power converter with multiple-output port and its controlling technique," in *proceedings of IEEE Conference on Industrial Electronics and Applications (ICIEA)*, Jun. 2016, pp. 2241–2246.

[6] Min-Chin Lee, Jan-Bin Lio, Dan Y. Chen, Yie-Tone Chen, and Yan-Pei Wu, "Small-signal modeling of multiple-output flyback converters in continuous conduction mode with weighted feedback," *IEEE Transactions on Industrial Electronics*, vol. 45, no. 2, pp. 236–248, Apr. 1998.

[7] D. Maksimovic and R. Erickson, "Modeling of cross-regulation in multiple-output flyback converters," in *proceedings of IEEE Applied Power Electronics Conference and Exposition (APEC)*, vol. 2, Mar. 1999, pp. 1066–1072.

[8] Q. Chen, F. C. Lee, and M. Jovanovic, "Analysis and design of weighted voltage-mode control for a multiple-output forward converter," in *proceedings of IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 1993, pp. 449–455.

[9] Chuanwen Ji, M. Smith, K. M. Smedley, and K. King, "Cross regulation in flyback converters: analytic model and solution," *IEEE Transactions on Power Electronics*, vol. 16, no. 2, pp. 231–239, Mar. 2001.

[10] M. Jung, S. Shin, and G. Cho, "Issues of single-inductor multiple-output dc-dc converters," in *proceedings of International SoC Design Conference (ISOCC)*, Nov. 2015, pp. 115–116.

[11] M.-H. Huang, K.-H. Chen, and W.-H. Wei, "Single-inductor dual-output dc-dc converters with high light-load efficiency and minimized cross-regulation for portable devices," in *proceedings of IEEE Symposium on VLSI Circuits*, Jun. 2008, pp. 132–133.

[12] M.-Y. Jung, S.-H. Park, J.-S. Bang, and G.-H. Cho, "An error-based controlled single-inductor 10-output dc-dc buck converter with high efficiency under light load using adaptive pulse modulation," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 2825–2838, Dec. 2015.

[13] M. Belloni, E. Bonizzoni, and F. Maloberti, "On the design of single-inductor multiple-output dc-dc buck converters," in *proceedings of IEEE International Symposium on Circuits and Systems*, May 2008, pp. 3049–3052.

[14] C. Chen, T. Liao, K. Hsu, and C. Hung, "A single-inductor multiple-output boost converter with freewheel charge-pump control," in *proceedings of ESSCIRC*, Sep. 2012, pp. 157–160.

[15] J. Kim and C. Kim, "A single-inductor 8-channel output dc-dc boost converter with time-limited power distribution control and single shared hysteresis comparator," in *proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2014, pp. 33–34.

[16] D. Dah-Chuan Lu, M. Wu, and T. Cheng, "Using cross regulation in single-switch single-inductor dual-output ccm boost converter to simplify controller design," in *proceedings of International Conference on Industrial Technology (ICIT)*, Mar. 2016, pp. 390–395.

[17] X. Liu, J. Xu, Z. Chen, and N. Wang, "Single-inductor dual-output buckboost power factor correction converter," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 2, pp. 943–952, Feb. 2015.

[18] Y. Zheng, J. Guo, and K. N. Leung, "A single-inductor multiple-output buck/boost DC-DC converter with duty-cycle and control-current predictor," *IEEE Transactions on Power Electronics*, vol. 35, no. 11, pp. 12 022–12 039, Nov. 2020.

[19] Y. Zheng, M. Ho, J. Guo, and K. N. Leung, "A single-inductor multiple-output auto-buck-boost DC-DC converter with tail-current control," *IEEE Transactions on Power Electronics*, vol. 31, no. 11, pp. 7857–7875, Nov. 2016.

[20] W. Xu, Y. Li, Z. Hong, and D. Killat, "A 90 % peak efficiency single-inductor dual-output buck-boost converter with extended-pwm control," in *proceedings of International Solid-State Circuits Conference*, Feb. 2011, pp. 394–396.

[21] C.-S. Huang, D. Chen, C.-J. Chen, and K. H. Liu, "Mix-voltage conversion for single-inductor dual-output buck converters," *IEEE Transactions on Power Electronics*, vol. 25, no. 8, pp. 2106–2114, Aug. 2009.

[22] P. Patra, A. Patra, and N. Misra, "A single-inductor multiple-output switcher with simultaneous buck, boost, and inverted outputs," *IEEE Transactions on Power Electronics*, vol. 27, no. 4, pp. 1936–1951, Apr. 2012.

[23] D. Ma, W.-H. Ki, C.-Y. Tsui, and P. K. T. Mok, "Single-inductor multiple-output switching converters with time-multiplexing control in discontinuous conduction mode," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 1, pp. 89–100, Jan. 2003.

[24] H. Chen, Y. Zhang, and D. Ma, "A SIMO parallel-string driver IC for dimmable led backlighting with local bus voltage optimization and single time-shared regulation loop," *IEEE Transactions on Power Electronics*, vol. 27, no. 1, pp. 452–462, Jan. 2012.

[25] W. Huang, J. A. A. Qahouq, and Z. Dang, "CCM-DCM power-multiplexed control scheme for single-inductor multiple-output DC-DC power converter with no cross regulation," *IEEE Transactions on Industrial Applications*, vol. 53, no. 2, pp. 1219–1231, Mar. 2017.

[26] K. Kwan and W. Ki, "Freewheel duration adjustment circuits for charge-control single-inductor dual-output switching converters," in *proceedings of IEEE International Symposium on Circuits and Systems*, May 2010, pp. 2722–2725.

[27] Suet-Chui Koon, Yat-Hei Lam, and Wing-Hung Ki, "Integrated charge-control single-inductor dual-output step-up/step-down converter," in *proceedings of IEEE International Symposium on Circuits and Systems*, May 2005, pp. 3071–3074.

[28] D. Ma, W.-H. Ki, and C.-Y. Tsui, "A pseudo-ccm/dcm simo switching converter with freewheel switching," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 6, pp. 1007–1014, Jun. 2003.

[29] Y. Moon, Y. Roh, J. Gong, and C. Yoo, "Load-independent current control technique of a single-inductor multiple-output switching DC-DC converter," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 59, no. 1, pp. 50–54, Jan. 2012.

[30] M.-Y. Jung, S.-H. Park, J.-S. Bang, and G.-H. Cho, "An error-based controlled single-inductor 10-output DC-DC buck converter with high efficiency under light load using adaptive pulse modulation," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 2825–2838, Dec. 2015.

[31] T. Y. Goh and W. T. Ng, "Single discharge control for single-inductor multiple-output DC-DC buck converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2307–2316, Mar. 2018.

[32] J. Kim, D. S. Kim, and C. Kim, "A single-inductor eight-channel output DC-DC converter with time-limited power distribution control and single shared hysteresis comparator," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 12, pp. 3354–3367, Dec. 2013.

[33] K.-Y. Lin, C.-S. Huang, D. Chen, and K. H. Liu, "Modeling and design of feedback loops for a voltage-mode single-inductor dual-output buck converter," in *proceedings of IEEE Power Electronics Specialists Conference*, Jun. 2008, pp. 3389–3395.

[34] P. Patra, J. Ghosh, and A. Patra, "Control scheme for reduced cross-regulation in single-inductor multiple-output dc-dc converters," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 11, pp. 5095–5104, Nov. 2013.

[35] J. D. Dasika, B. Bahrani, M. Saeedifard, A. Karimi, and A. Rufer, "Multivariable control of single-inductor dual-output buck converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 4, pp. 2061–2070, Apr. 2014.

[36] B.-W. Chen and L.-R. Chang-Chien, "Digitally controlled low cross-regulation single-inductor dual-output (sido) buck converter," in *proceedings of IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2015, pp. 2497–2500.

[37] D. Trevisan, P. Mattavelli, and P. Tenti, "Digital control of single-inductor multiple-output step-down DC-DC converters in CCM," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 9, pp. 3476–3483, Sep. 2008.

[38] B. Wang, V. R. K. Kanamarlapudi, L. Xian, X. Peng, K. T. Tan, and P. L. So, "Model predictive voltage control for single-inductor multiple-output DC-DC converter with reduced cross regulation," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 7, pp. 4187–4197, Jul. 2016.

[39] Z. Shen, X. Chang, W. Wang, X. Tan, N. Yan, and H. Min, "Predictive digital current control of single-inductor multiple-output converters in ccm with low cross regulation," *IEEE Transactions on Power Electronics*, vol. 27, no. 4, pp. 1917–1925, Apr. 2012.

[40] X. Zhang, B. Wang, X. Tan, H. B. Gooi, H. H. C. Iu, and T. Fernando, "Deadbeat control for single-inductor multiple-output dcdc converter with effectively reduced cross regulation," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 4, pp. 3372–3381, Dec. 2020.

[41] C. J. Solis and G. A. Rincn-Mora, "Nested hysteretic current-mode single-inductor multiple-output (simo) boosting buck converter," in *proceedings of New Circuits and Systems Conference (NEWCAS)*, Jun. 2013, pp. 1–4.

[42] W. Sun, C. Han, M. Yang, S. Xu, and S. Lu, "A ripple control dual-mode single-inductor dual-output buck converter with fast transient response," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 23, no. 1, pp. 107–117, Jan. 2015.

[43] W. Xu, Y. Li, X. Gong, Z. Hong, and D. Killat, "A dual-mode single-inductor dual-output switching converter with small ripple," *IEEE Transactions on Power Electronics*, vol. 25, no. 3, pp. 614–623, Mar. 2010.

[44] Y. Wang, J. Xu, S. Zhou, T. Zhao, and K. Liao, "Current-mode controlled single-inductor dual-output buck converter with ramp compensation," in *proceedings of IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct. 2017, pp. 4996–5000.

[45] S. Zhou, G. Zhou, G. Liu, and G. Mao, "Small-signal modeling and cross-regulation suppressing for current-mode controlled single-inductor dual-output dc-dc converters," *IEEE Transactions on Industrial Electronics*, pp. 1–1, May 2020.

[46] Y. Wang, J. Xu, and G. Yin, "Cross-regulation suppression and stability analysis of capacitor current ripple controlled SIDO CCM buck converter," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 3, pp. 1770–1780, Mar. 2019.

[47] E. C. dos Santos, "Dual-output DC-DC buck converters with bidirectional and unidirectional characteristics," *IET Power Electronics*, vol. 6, no. 5, pp. 999–1009, May 2013.

[48] P. Kumar and M. Rojas-Gonzalez, "Novel 3-switch dual output buck voltage regulator," in *proceedings of IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2006, pp. 467–473.

[49] S. K. Mishra, K. K. Nayak, M. S. Rana, and V. Dharmarajan, "Switched-boost action based multiport converter," *IEEE Transactions on Industrial Applications*, vol. 55, no. 1, pp. 964–975, Jan. 2019.

[50] S. K. Mishra and K. K. Nayak, "Boost topology based multi-output converters," in *proceedings of IEEE Industry Applications Society Annual Meeting*, Oct. 2017, pp. 1–5.

[51] O. Ray, J. A. Prasad, and S. Mishra, "A multi-port dc-dc converter topology with simultaneous buck and boost outputs," in *proceedings of International Symposium on Industrial Electronics*, Feb. 2013, pp. 1–6.

[52] O. Ray, A. P. Josyula, S. Mishra, and A. Joshi, "Integrated dual-output converter," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 1, pp. 371–382, Jan. 2015.

[53] D. Venugopalan and C. R. Raj, "Integrated dual output buck boost converter for industrial application," in *proceedings of International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT)*, Mar. 2016, pp. 342–345.

[54] S. Palanidoss and T. V. S. Vishnu, "Experimental analysis of conventional buck and boost converter with integrated dual output converter," in *proceedings of International Conference on Electrical, Electronics, Communication, Computer, and Optimization Techniques (ICEECCOT)*, Dec. 2017, pp. 323–329.

[55] G. Chen, Y. Deng, K. Wang, Y. Hu, L. Jiang, H. Wen, and X. He, "Topology derivation and analysis of integrated multiple output isolated dcdc converters with stacked configuration for low-cost applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 8, pp. 2207–2218, Aug. 2017.

[56] G. Chen, Y. Liu, X. Qing, and F. Wang, "Synthesis of integrated multiport dcdc converters with reduced switches," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 6, pp. 4536–4546, Jun. 2020.

[57] J. B. V. Reddy, G. Bhuvaneswari, and B. Singh, "A single dc-dc converter based multiple output smps with fully regulated and isolated outputs," in *proceedings of Annual IEEE India Conference - Indicon*, Dec. 2005, pp. 585–589.

[58] X. L. Li, Z. Dong, and C. K. Tse, "Analysis of basic structures of interconnected converters for single-input multiple-output applications," in *proceedings of IEEE Power Electronics and Application Conference and Exposition (PEAC)*, Nov. 2018, pp. 1–6.

[59] K. M. Divya and R. Parackal, "High power factor integrated buck-boost flyback converter driving multiple outputs," in *proceedings of International Conference on Green Engineering and Technologies (IC-GET)*, Nov. 2015, pp. 1–5.

[60] T. Lodh and T. Majumder, "Highly efficient and compact sepic-boost-flyback integrated converter with multiple outputs," in *proceedings of International Conference on Signal Processing, Communication, Power and Embedded System (SCOPES)*, Oct. 2016, pp. 6–11.

[61] A. Ikriannikov and T. Schmid, "Magnetically coupled buck converters," in *proceedings of IEEE Energy Conversion Congress and Exposition*, Sep. 2013, pp. 4948–4954.

[62] M. S. A. Jafarian and H. R. Karshenas, "Current ripple reduction in single-input, multiple-output converters using phase-shift and coupled inductors," in *proceedings of Iranian Conference on Electrical Engineering (ICEE)*, May 2016, pp. 816–821.

[63] Y. . Chen, D. Y. Chen, and Y. . Wu, "Control-loop modeling of multiple-output feedback of forward converters," *IEEE Transactions on Power Electronics*, vol. 8, no. 3, pp. 320–328, Jul. 1993.

[64] Yie-Tone Chen, "Small-signal analysis of a synchronous-switch post regulator with coupled inductors," *IEEE Transactions on Industrial Electronics*, vol. 47, no. 1, pp. 55–66, Feb. 2000.

[65] G. Zhu, B. McDonald, and K. Wang, "Modeling and analysis of coupled inductors in power converters," in *proceedings of Applied Power Electronics Conference and Exposition (APEC)*, Feb. 2009, pp. 83–89.

[66] N. Deshpande, R. D. Chavhan, and N. Deshpande, "Coupled inductor based single-input multiple-outputs boost converter," in *proceedings of International Conference on Advances in Electrical, Electronics, Information, Communication and Bio-Informatics (AEEICB)*, Feb. 2017, pp. 126–130.

[67] R. Wai and K. Jheng, "High-efficiency single-input multiple-output dcdc converter," *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 886–898, Feb. 2013.

[68] R.-J. Wai and Z.-F. Zhang, "High-efficiency single-input triple-outputs dc-dc converter with zero-current switching," *IEEE Access*, vol. 7, pp. 84 952–84 966, Jun. 2019.

[69] H. Wu, S. Wong, C. K. Tse, and Q. Chen, "A pfc single-coupled-inductor multiple-output led driver without electrolytic capacitor," *IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1709–1725, Feb. 2019.

[70] H. Wu, S. Wong, and C. K. Tse, "A more efficient pfc single-coupled-inductor multiple-output electrolytic capacitor-less led driver with energy-flow-path optimization," *IEEE Transactions on Power Electronics*, vol. 34, no. 9, pp. 9052–9066, Sep. 2019.

[71] Y. C. Hsu, J. Y. Lin, C. H. Wang, and S. W. Chou, "An simo step-down converter with coupled inductor," in *proceedings of IEEE International Symposium on VLSI Design, Automation and Test (VLSI-DAT)*, Aug. 2020, pp. 1–4.

[72] R. D. Middlebrook and S. Cuk, "A general unified approach to modelling switching-converter power stages," in *proceedings of IEEE Power Electronic Specialists Conference*, Jun. 1976, pp. 18–34.

[73] R. W. Erickson and D. Maksimovic, *Fundamentals of power electronics*. Springer Science & Business Media, 2007.

[74] M. K. Kazimierczuk, *Pulse-width modulated DC-DC power converters*. John Wiley & Sons, 2015.

[75] A. Ioinovici, *Power Electronics and Energy Conversion Systems: Fundamentals and Hard-switching Converters. Volume 1*. Wiley, 2013.

[76] N. Mohan, *Power electronics: a first course*. Wiley, 2011.

[77] L. Dixon, "Average current mode control of switching power supplies," in *Unitrode Power Supply Design Seminar*. Unitrode Corp., 1990, pp. 5.1–5.14.

[78] B. R. Raymond, H. BO, and C. FRED, "Analysis and interpretaion of loop gains of multiloop-controlled switching regulators," *IEEE Transactions on Power Electronics*, vol. 3, no. 4, p. 489, Oct. 1988.

[79] R. D. Middlebrook, "Topics in multiple-loop regulators and current-mode programming," *IEEE Transactions on Power Electronics*, vol. PE-2, no. 2, pp. 109–124, Apr. 1987.

[80] G. C. Verghese, M. E. Elbuluk, and J. G. Kassakian, "A general approach to sampled-data modeling for power electronic circuits," *IEEE Transactions on Power Electronics*, vol. PE-1, no. 2, pp. 76–89, Apr. 1986.

[81] R. Tymerski and D. Li, "State-space models for current programmed pulsewidth-modulated converters," *IEEE Transactions on Power Electronics*, vol. 8, no. 3, pp. 271–278, Jul. 1993.

[82] D. Maksimovic and R. Zane, "Small-signal discrete-time modeling of digitally controlled pwm converters," *IEEE Transactions on Power Electronics*, vol. 22, no. 6, pp. 2552–2556, Nov. 2007.

[83] R. B. Ridley, "A new, continuous-time model for current-mode control (power convertors)," *IEEE Transactions on Power Electronics*, vol. 6, no. 2, pp. 271–280, Apr. 1991.

[84] F. D. Tan and R. D. Middlebrook, "A unified model for current-programmed converters," *IEEE Transactions on Power Electronics*, vol. 10, no. 4, pp. 397–408, Jul. 1995.

[85] B. Bryant and M. K. Kazimierczuk, "Modeling the closed-current loop of pwm boost dc-dc converters operating in ccm with peak current-mode control," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 11, pp. 2404–2412, Nov. 2005.

[86] M. K. Kazimierczuk, "Transfer function of current modulator in pwm converters with current-mode control," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 47, no. 9, pp. 1407–1412, Sep. 2000.

[87] N. Nupur and S. Nath, "Minimizing ripples of inductor currents in coupled sido boost converter by shift of gate pulses," *IEEE Transactions on Power Electronics*, vol. 35, no. 2, pp. 1217–1226, Jul. 2020.

[88] T. Suntio, M. Hankaniemi, and T. Roinila, "Dynamical modelling of peak-current-mode-controlled converter in continuous conduction mode," *Simulation Modelling Practice and Theory*, vol. 15, no. 10, pp. 1320–1337, Nov. 2007.

LIST OF PUBLICATIONS

Journal Publications:

Published

1. G. Nayak, S. Nath, Decoupled Voltage Mode Control of Coupled Inductor Single input dual Output Buck Converter, in IEEE Transactions on Industry Applications, vol. 56, no. 4, pp. 4040-4050, July-Aug. 2020.
   doi: 10.1109/TIA.2020.2991650.

2. G. Nayak and S. Nath, "Decoupled Average Current Control of Coupled Inductor Single-Input Dual-Output Buck Converter," in IEEE Journal of Emerging and Selected Topics in Industrial Electronics, vol. 1, no. 2, pp. 152-161, Oct. 2020.
   doi: 10.1109/JESTIE.2020.3014833.

To be Submitted

1. G. Nayak, S. Nath, "Design of Peak Current Mode Control for Coupled SIDO Buck Converter", IEEE Transaction on Industrial Electronics.

2. G. Nayak, S. Nath, " Unified Model of Peak Current Mode Control Coupled SIDO Converters", IEEE Transaction on Power Electronics.

3. G. Nayak, S. Nath, "Choosing Coefficient of Coupling for Coupled SIDO converters", IEEE Transactions on Circuits and Systems I: Regular Papers.

Conference Publications:

Published

1. G. Nayak and S. Nath, "Comparing Performances of SIDO Buck Converters," 2018 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Chennai, India, 2018, pp. 1-6.
   doi: 10.1109/PEDES.2018.8707459.

2. G. Nayak and S. Nath, "Voltage Mode Control of Magnetically Coupled SIDO Buck Converter," 2018 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Chennai, India, 2018, pp. 1-6.
   doi: 10.1109/PEDES.2018.8707607.

3. G. Nayak and S. Nath, "Small Signal Modeling and Analysis of Single Input Three Output Buck Converter Using Coupled Inductor," 2019 National Power Electronics Conference (NPEC), Tiruchirappalli, India, 2019, pp. 1-6.
   doi: 10.1109/NPEC47332.2019.9034743.

4. G. Nayak and S. Nath, "Unaffected Dynamic Performance of Coupled SIDO Converters Due to Phase Shift," 2019 National Power Electronics Conference (NPEC), Tiruchirappalli, India, 2019, pp. 1-6.
   doi: 10.1109/NPEC47332.2019.9034867.

5. G. Nayak and S. Nath, "Small Signal Model for Current Mode Control of Coupled Inductor SIDO Buck Converter," 2019 IEEE Transportation Electrification Conference (ITEC-India), Bengaluru, India, 2019, pp. 1-6.
   doi: 10.1109/ITEC-India48457.2019.ITECINDIA2019-252.

Accepted

1. G. Nayak and S. Nath, "Instability in Peak Current Mode Controlled Coupled SIDO Buck Converter", 2020 IEEE International Conference on Power Electronics, Drives and

Energy Systems (PEDES), Jaipur, India, 2020. (Accepted)

2. G. Nayak and S. Nath, "Input Voltage Feedforward and Feedback Control of Coupled Inductor SIDO Buck Converter", 2020 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Jaipur, India, 2020. (Accepted)

3. G. Nayak and S. Nath, "Dynamic Performance of Coupled SIDO Buck Converter Operating in Current Mode and Voltage Mode Control", 2020 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Jaipur, India, 2020. (Accepted)

4. G. Nayak, S. Nath, "Small Signal Model for Peak Current Controlled Coupled SIDO Buck Converter", 2021 IEEE Energy Conversion Congress and Exposition Asia (ECCE ASIA-2021). (Accepted)