



INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI  
SHORT ABSTRACT OF THESIS

Name of the Student : SIVAKUMAR S.

Roll Number : 176101010

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Performance and Lifetime Enhancement of Non-Volatile Memory Caches

Name of Thesis Supervisor(s) : Dr. JOHN JOSE

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Processing data-intensive applications demands more on-chip memory. Realizing large volumes of on-chip memory is challenging as conventional memories such as DRAM and SRAM occupy more on-chip area and consume leakage power. Emerging non-volatile memories (NVMs) such as Spin Transfer Torque RAM (STT-RAM) can overcome this bottleneck to realize large volumes of on-chip memories. Even though NVMs possess larger packaging density and zero leakage power, their limited endurance, higher write energy, and latency are serious concerns. The thesis discusses three contributions that improve the lifetime of single-level cell (SLC) and multi-level cell (MLC) NVMs when used in last-level caches. The first contribution discusses the NVM-friendly cache replacement policy and a wear-leveling strategy that uniformly distributes the writes in SLC NVM LLCs to improve their lifetime. As the second contribution, the thesis proposes logically splitting unified LLC into instruction and data cache and periodically interchange the mapping for better write distribution. As data blocks are heavily written compared to instructions, the periodic reorganization ensures the distribution of heavily written blocks across the SLC NVM LLC, resulting in a better lifetime. The thesis's third contribution proposes using the embedded trace buffer, left unused after post-silicon validation, to act as a write buffer for the MLC NVM caches and improve its lifetime and performance. Experimental results show significant improvement in the lifetime and performance of SLC and MLC NVM caches.