**INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI**
**SHORT ABSTRACT OF THESIS**

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Thesis Title : **Design of Machine Learning Based Framework for Semiconductor Device Analysis**

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## SHORT ABSTRACT

The quest for making sub-nano regime devices is posing several challenges to the electronics industry, such as high leakage current, high DIBL, hot electron effect and other short channel effects. Technology Computer Aided Design (TCAD) simulations can help overcome all these issues in the best possible manner, provided it gives reliable and accurate results. The solution accuracy of the TCAD simulations depends mainly on two main factors; 1) Transport model employed for the analysis, and 2) Numerical solution of the transport model which basically depends on the type of discretization scheme used for the approximation. In this thesis, the two main challenges of the TCAD; Accuracy and Computation time, have been addressed by incorporating different discretization methodologies, such as Finite Element Method (FEM), Discontinuous Galerkin Finite Element Method (DG-FEM), Streamline Upwind Petrov Galerkin (SUPG) based Finite Element Method (SUPG-FEM) and Element Free Galerkin (EFG) to improve the solution accuracy, and Random Walk and Machine Learning based methodologies to reduce the computation time of the analysis. This thesis presents the design and development of a parallel and scalable framework, VEDA (Very Efficient Device Analyzer), for the analysis of semiconductor devices. The proposed methodologies are employed to discretize fundamental device equations, a set of Partial Differential Equations (PDEs), governing the flow of carriers inside the device, and later solved numerically using a suitable methodology to compute the solution.

DG-FEM and SUPG-FEM are two variants of FEM based on two different approaches to improve the solution accuracy. In DG-FEM, the basis functions employed for the discretization are discontinuous piecewise polynomials which aid to conserve the flux efficiently and are capable of handling complex geometries. In VEDA, SUPG method is employed to calculate flux and flow of charge in the device. It is observed that the SUPG stabilization technique is better than the classical Scharfetter-Gummel method to solve a convection-diffusion equation. On the other hand, EFG is an element free or meshfree method to discretize the problem domain. In EFG a set of nodes are scattered throughout the domain to formulate linear algebraic equations which represent carrier transport in semiconductor devices without employing mesh for domain discretization. The solution provided by our proposed method is

compared with other discretization techniques including the methodology adopted by commercial TCAD simulator, Sentaurus. The accuracy of the solution obtained by the proposed method is approximately 10 better as compared to the solution provided by Sentauras.

Since the solution provided by EFG is accurate but not efficient in terms of computational time, we employ random walk method to speed up the solution of device equations. As we know that the numerical solution of differential equations depends on the initial guess, therefore, we propose to improve it by using random walk method. In this method, equivalent electrical circuits of fundamental device equations are formulated and are analyzed self-consistently in a coupled manner to perform device analysis. The random walk method is based on the probability distribution calculated from the weights at each node. The parallelizable aspect of random walk method has also been explored to improve the computation time of the analysis. The proposed method exhibits up to 20% faster solution with the maximum error of 4% in the initial guess as compared to the final solution. Although the improvement in the computational time obtained using random walk method is not significant, it motivates us to explore other methods such as machine learning algorithms and its application to the semiconductor device analysis. Therefore, different machine learning algorithms along with Artificial Neural Network (ANN) have been employed for the analysis of semiconductor devices for a given set of parameters. It is observed that the use of ANN has helped not only in improvising computation time but also providing nearly accurate solution. We have observed a minimum speedup of 1:86x (13 iterations to 7 iterations) and maximum speedup of 3:5x (21 iterations to 6 iterations) for a different set of parameters by using the proposed methodology. The implementation of ANN has enabled us to explore a new paradigm in the domain of TCAD. The ANNs mimicking the electrical characteristics of semiconductor devices are also employed to perform circuit analysis. We have designed different circuits using these ANN based semiconductor devices, and their performances are found to be within the acceptable accuracy limits. The methodology employed for the analysis of circuits having ANN based semiconductor devices can easily be parallelized enabling quick turnout of the solution. This approach helps us to overcome issues related to the semiconductor device modeling without developing a semiconductor device model in the early stage of the device design. It eliminates the need for semiconductor device modeling and the efforts taken in the development of compact device models of semiconductor devices including novel devices (forthcoming devices whose device models are not yet known). The machine learning based semiconductor device and circuit analysis is found to be efficient in terms of accuracy and computation time as compared to the lookup table based methods employed for TCAD and circuit analysis. This begins a new era in the area of VLSI for semiconductor device design, modeling and circuit analysis.