Engineering Solution Processable Organic Field Effect Transistor for Opto-electronic Applications

A dissertation submitted in partial fulfilment of requirements for the degree of

Doctor of Philosophy

by

Anwesha Choudhury

Roll No. 176153007

Centre for Nanotechnology

Indian Institute of Technology Guwahati

Guwahati-781039, Assam, India

August 2022

Statement

I do hereby declare that the work incorporated in this thesis entitled, "**Engineering Solution Processable Organic Field Effect Transistor for Opto-electronic Applications**" is the result of investigations carried out by me under the guidance of Prof. Parameswar Krishnan Iyer, at the Centre for Nanotechnology, Indian Institute of Technology Guwahati, Guwahati, Assam, India.

In keeping with the general practice of reporting scientific observations, due acknowledgements have been made wherever the work described is based on the findings of other investigators. I further declare that this work has not been submitted in part or full to any other university or institute for award of any degree or diploma.

IIT Guwahati Anwesha Choudhury

August 2022

Dr. Parameswar K. Iyer
Department of Chemistry and Center for Nanotechnology
Indian Institute of Technology Guwahati
Guwahati-781039, Assam, India
http://www.iitg.ac.in/chemistry/fac/pki/

Phone : +91-361-2582314
Fax : +91-361-2690762
: +91-361-2582349
E-mail : pki@iitg.ac.in

Certificate

This is to certify that the work included in this thesis entitled "**Engineering Solution Processable Organic Field Effect Transistor for Opto-electronic Applications**" by Anwesha Choudhury, Centre for Nanotechnology, Indian Institute of Technology Guwahati has been carried out under my supervision. I further certify that this work has not been submitted to any other University or Institution in part or full for the award of any degree or diploma.

IIT Guwahati

August 2022

Parameswar Krishnan Iyer

Thesis supervisor
Centre for Nanotechnology &
Department of Chemistry
Indian Institute of Technology Guwahati
Guwahati – 781039, Assam, India

Dedicated to my parents

Table of Contents

Acknowledgement

I am delighted to put across my heartfelt appreciation and gratefulness to everyone who in one way or the other have contributed in the completion of this thesis. Many individuals have supported me in this truly unforgettable and amazing journey. I have tried to list everyone who have sincerely helped and guided me in the completion of this thesis. I thank each person from the bottom of my heart.

First of all, I am extremely beholden to my supervisor and mentor Prof. Parameswar Krishnan Iyer for providing me a precious opportunity to work in his group. His continuous support, valuable suggestions, scientific guidance, deep insights, and motivation have encouraged me to take up the tasks and introduced me to a field that I knew little about. I earnestly thank him for having trust in me and giving me total freedom in choosing the direction of my research. I feel fortunate to have him as my guide who has always motivated me with his hard work, dedication and optimism. He has been ever patient with me and was always available to provide his very useful opinion regarding my thesis work.

Besides my supervisor, I am highly indebted to my doctoral committee members, Dr. Partho Sarathi Gooh Pattader, Prof. D. Pamu, and Prof. Harshal B. Nemade for assessing my research work regularly. Their invaluable suggestions and crucial comments during all my seminars helped me broaden my research from various perspectives and improve my thesis.

My sincere thanks also goes to Dr. Arun Tej M., Department of EEE, IIT Guwahati. I found him available whenever I was having a query related to the charge transport kinetics of any electronic devices. Attending lectures on organic electronic device has really helped me in my Ph.D thesis work.

I am also thankful to all the research scholars and staff of the Centre for Nanotechnology, IIT Guwahati for their kind cooperation and support. Further, I am grateful to Department of Chemistry and Central Instrument Facility, IIT Guwahati for allowing me to access their facility for the various experimentations as and when required. I am indebted to the staff of Student Affairs, Academic Affairs and Finance sections of IIT Guwahati for being kind enough to advise and help in their respective roles.

I have learnt a lot from Anamika di, Ashish Bhaiya, Adil bhaiya, Ramesh bhaiya and Rahul bhaiya who taught me the fabrication during my early days in Organic Electronics Laboratory, IIT Guwahati. Further, the research experience gathered along Ritesh, Rabindra had helped me complete my thesis.

I would also like to acknowledge all my other lab mates including Arvin Bhaiya, Raman Bhaiya, Nehal, Paromita, Retwik, Biki, Nasima, Raj, Priyam, Debika, Sushant, Gopal and Geetmani Da for their timely assistance and support. I also had a great learning experience with Priyanka and Swapna while they completed their summer internship project with me. I would also like to thank each one of them for creating a pleasant laboratory atmosphere and making my days memorable.

I was privileged to be part of the organizing team of ICANN2017, ICANN2019 and ICANN2021 conferences. I had the opportunity to interact with the topmost scientists across the world and discuss my research work with them.

I was also fortunate to be working in the Organic Electronics Laboratory of IIT Guwahati which houses all the sophisticated instruments. I have learnt a lot to keep these instruments in working conditions through proper maintenance. During all the maintenance activities, I have received ample support from various engineers. I would like to thank Mr. R. K. Tripathi, RVL Scientific & Engineering Pvt. Ltd., Mr. T. P. Kundu, IKA India Pvt. Ltd., Mr. Subrata Sardar, Silsil International Pvt. Ltd. and Mr. M. Nandan, Bat-Sol Equipments & Technology. They have extended all possible help as and when required.

I also want to take this opportunity to thank my close friends Nasima, Paromita, Tanusree, Megha, Himakshi, Atanu who have helped me in academic and even non academic endeviours in IIT Guwahati campus and made my stay in campus pleasant.

I extend my sincere thanks to my cycling group comprising of Rahul Bhaiya, Nilanjan Da and Ritesh. All our weekend cycling trips will be one of the most memorable times that I will be taking back from IIT Guwahati.

Finally I would like to show my gratitude to my parents (Mr. Abhijit Choudhury & Mrs. Alpana Choudhury) who actually taught the value of education. I would also like to

express my appreciation to my husband Dr. Prasenjit Deb whose encouragement made me start this Ph.D. journey and was there throughout the journey motivating me.

I express gratitude towards each individual for extending their support, encouragement and remembering me in their prayers.

Anwesha Choudhury

[This page was intentionally left blank]

Thesis Abstract

Electronic devices have made people's life easier, and in today's modern lifestyle electronic devices have become one of the basic requirements of human beings. Inorganic material are used extensively in electronic devices but the requirement of energy efficient, low-cost and flexible devices can be easily fulfilled by the organic solution processable materials. Organic field effect transistors (OFET) will enable easy implementation of large scale and flexible applications. Organic materials also have the advantage of easy tunability of the optoelectronic properties. OFETs have numerous applications like various sensors, smart card, e-skin etc. Some of the organic electronic devices like OLED, solar cell is already available in market, but low mobility and stability is a road block for organic transistors to be commercialized in high end applications.

Considering todays need for solution processed, flexible and energy efficient organic electronic devices, methods to understand the dielectric/semiconductor interfacial defects introduced due to solution processing and techniques to improve the device properties is covered in this thesis. This thesis is divided into three parts, the first part (Chapter 2) is about the understanding the interfacial defects arising due to complete solution processing of the dielectric and semiconductor. Second part (Chapter 3 and 4) consists of solvent engineering technique to improve the device mobility and stability. A ~5-fold increment in device mobility and also improvement in device stability in dark and under illumination is attained by solvent engineering. Third part (chapter 5) is the application of the improved device in various opto-electronic applications thereby, NOT and NOR logic are demonstrated by applying light and voltage input simultaneously.

The efforts made in this thesis highlights the usefulness of various device engineering to develop OFET to regulate the morphology and crystallization of the photo-active semiconductor layer to achieve highly efficient, stable and repeatable OFETs and its application as phototransistor, and logic gates. The thesis provides the basis for facilitating the commercialization of OFET in the near future.

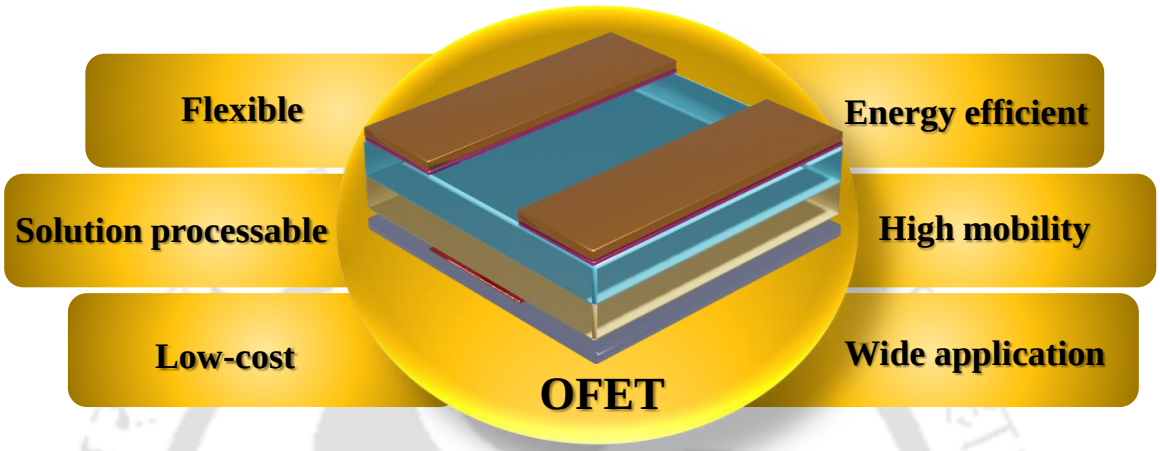
[This page was intentionally left blank]

List of Figures

List of Tables

Chapter 1

Introduction



[This page was intentionally left blank]

Abstract

The electronic industry has grown massively and today electronic devices are counted in the basic necessity for human beings. Even though most of the electronic devices presently use inorganic materials there is a growing demand of environment friendly, low cost, flexible, energy efficient devices. Hence, the need for organic field effect transistors (OFETs) based electronic circuits is ever increasing. In this introduction chapter, the importance of OFET followed by a brief history of transistors, four basic architectures and working principle of OFET are discussed. Thereafter, various parameters required for understanding the performance of any OFET is explained. Then the various interfaces present in OFET, choice of dielectric, solution processing of organic materials for the flexible OFETs, charge transport properties and factors affecting charge transport in OFET followed by a brief discussion on the applications in phototransistor, and in digital electronic circuits as opto-inverter are discussed. Lastly, a thesis overview is presented, at the end of the chapters.

1.1 Overview

Transistors are the basic building blocks of electronics, the development of which has revolutionized the field of electronic circuits. The invention of organic materials for transistors has added a new dimension to transistors and other electronic devices by paving the way for low cost, solution-processable, and flexible electronics. Polymers have been present in our daily life for ages and also in electronic devices as insulating materials. However, it was only in the late nineties that the outstanding discovery of oxidation enhanced conductivity of polyacetylene opened up a new avenue of organic electronics. Since then, intense research and tremendous progress have been achieved by developing various organic materials, synthesis techniques, and device engineering approaches. Transistors based on polymer materials have now reported mobility >10 cm^2 V^{-1} s^{-1},[1, 2] which is higher than amorphous silicon. The optoelectronic properties of the organic materials can also be utilized to fabricate organic phototransistors, opto logic gates, image sensors. Many organic electronic devices are already available in the market and become ubiquitous in our society. Tremendous research is carried out on increasing the mobility and stability of OFETs. However, the basic circuits in smart tags, driving matrix of flexible displays, radio frequency identification tags (RFID), etc., demand the use of low cost, large area, printed OFET based circuits.[3-5] Research is already in progress for OFET-based integrated circuits paving the way for the energy-efficient fabrication of electronic circuits.

For futuristic electronics and the commercialization of OFETs-based electronic circuits, the two main hurdles are the stability and mobility of the OFETs. The transport properties and mechanism need to be better understood to achieve high mobility and better stability. Improvement in charge transport in OFET can be achieved by improving the dielectric/semiconductor (d/s) interface and semiconductor morphology. Most semiconductors are insoluble, including organic oligomers, until they are carefully functionalized to be soluble. However, this functionalization may hamper their carrier mobility. Organic polymers are typically more soluble and have better film-forming capability by solution processing techniques than small molecules. Still, they can be modulated and improved by various methods. The fabrication or coating technique is crucial in forming a defect-free morphology and interfaces for solution-processed polymer thin films. These defects will lead to the device's instability and hamper the charge transport properties. Therefore, considering the current demand for flexible and energy-

efficient electronic devices, improving mobility and stability has become one of the most important research topic as these are indispensable properties for implemention of OFETs in different flexible circuit designs.

1.2 Organic Field Effect Transistor (OFET)

Organic Field Effect Transistor (OFET) is like a conventional transistor, a three-terminal device in which the current flow between the two terminals, i.e., source and drain, can be modulated by the voltage applied in the third terminal. i.e., the gate. The semiconductor or the dielectric needs to be organic for a transistor to be classified as an OFET.

1.2.1 History of transistor

The field-effect transistor was proposed in 1925 by Lilienfeld Julius Edgar and patented the idea in 1930.[6] However, the first working transistor was demonstrated at Bell laboratory by William Shockley, John Bardeen, and Walter Brattain in 1947, and they were honoured in 1956 with the Nobel prize in physics. This invention revolutionized the electronic industry and replaced vacuum tube-based devices with solid-state electronics. Inorganic semiconductor materials like Si and Ge dominated the electronics industry. Nevertheless, a new electronic revolution started with the development of OSCs. Though OSCs are not new, even in the early 20th century, there were studies on the dark and photoconductivity of anthracene crystals.[7] However, in 1976, with the discovery on conducting polymers by Alan J. Heeger, Alan G. MacDiarmid, and Hideki Shirakawa, the research and development of organic electronic devices started.[8] They were jointly awarded the Nobel Prize in Chemistry in 2000 for this breakthrough discovery.[9] The first OFET was reported by Tsumura *et al.* in 1986 and used polythiophene film as the active layer.[10] Owing to the extensive efforts of academic and industrial research over the last two decades, OFET has achieved mobility higher than amorphous silicon (a-Si). Already organic light-emitting diode (OLED) based displays have achieved commercialization. In the near future, OFET based applications like logic circuits, image sensors, displays, etc. will also follow.

1.2.2 Working principle

The conduction mechanism in organic materials is quite different than the inorganic counterparts. The organic molecules do not have any intrinsic conductivity; excess carriers need to be injected to start the conduction. Hence OFETs mostly work in the accumulation

mode rather than in depletion or inversion mode because of the low density of carriers in the OSC. The gate electrode is electrically isolated from the rest of the device by the dielectric. The charge transport takes place only in a thin layer of the semiconductor, close to the d/s interface, i.e., the bulk semiconductor is not affected by the gate field. On application of negative bias to the gate and drain of a p-type OFET, a linear current regime is observed for $V_{DS}<V_{GS}$. As V_{DS} becomes increasingly negative, the density of accumulated charges decreases from the source to the drain, and the current I_{DS} increases linearly. When the potential of the drain becomes more negative than that of the gate, a zone of depletion appears close to the drain (pinching of the channel), and the current tends to saturate. The output characteristic of a FET is the series of I_{DS} versus V_{DS} curves with a fixed V_{GS}. The transfer characteristic is the series of I_{DS} versus V_{GS} curves with a fixed V_{DS} These measurements can give the same information, as long as a sufficient number of gate voltages (drain voltages) are scanned as output (transfer) characteristics. Transfer characteristics are typically taken at two fixed V_{DS}: one is set as small as possible; much smaller than the maximum scanning gate voltage and the second V_{DS} is set larger than the maximum scanning V_{GS}. These two regimes are known as the linear and saturation regime, respectively. From the transfer characteristics of the OFET, we can extract various parameters such as the field-effect mobility (μ_{FET}) of the linear field and saturation field, the threshold voltage, and the on/off ratio.

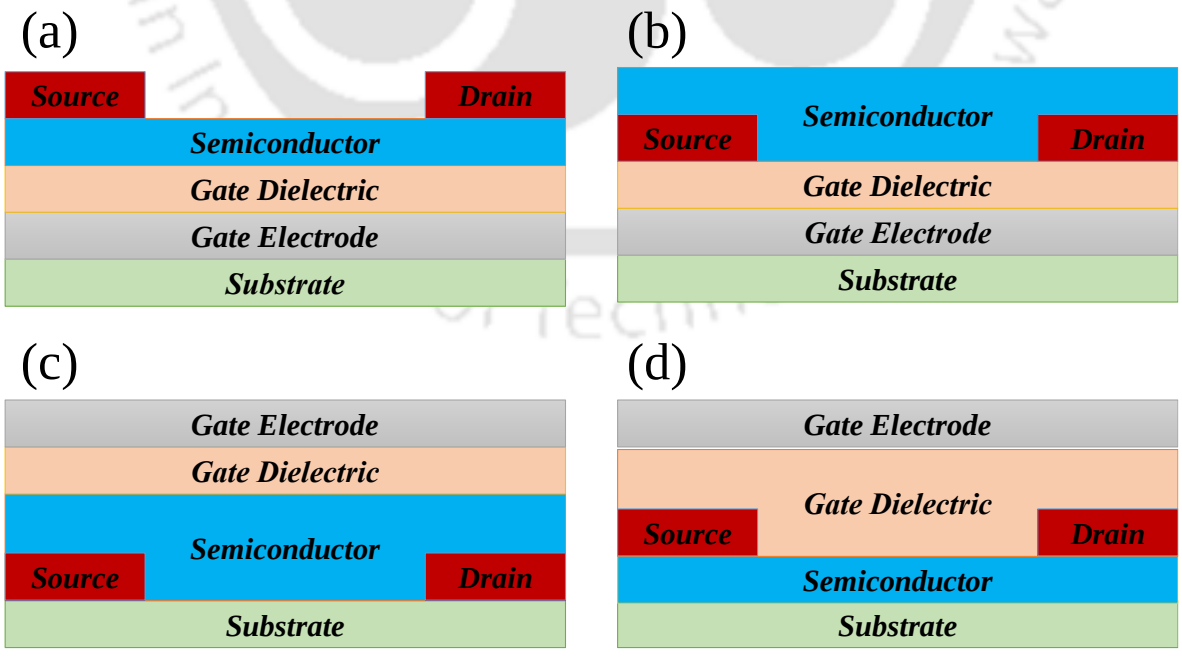


Figure 1.1: Cross sections views of OFETs geometries: a) bottom gate top contact b) bottom gate bottom **contact c**) top gate bottom contact d) top gate top contact configurations.

1.2.3 Structures of OFET

An OFET typically has three electrodes, gate, source, and drain. Depending on whether the position of the gate, source-drain is above or below the dielectric, semiconductor respectively, the OFET structure can be classified into four types (**Figure 1.1**): a) top gate bottom contact (TGBC) b) bottom-gate top contact (BGTC), OFET characterization parameters are extracted b) top gate top contact (TGTC) b) bottom gate bottom contact (BGBC).

1.3 Parameters to define OFET performance

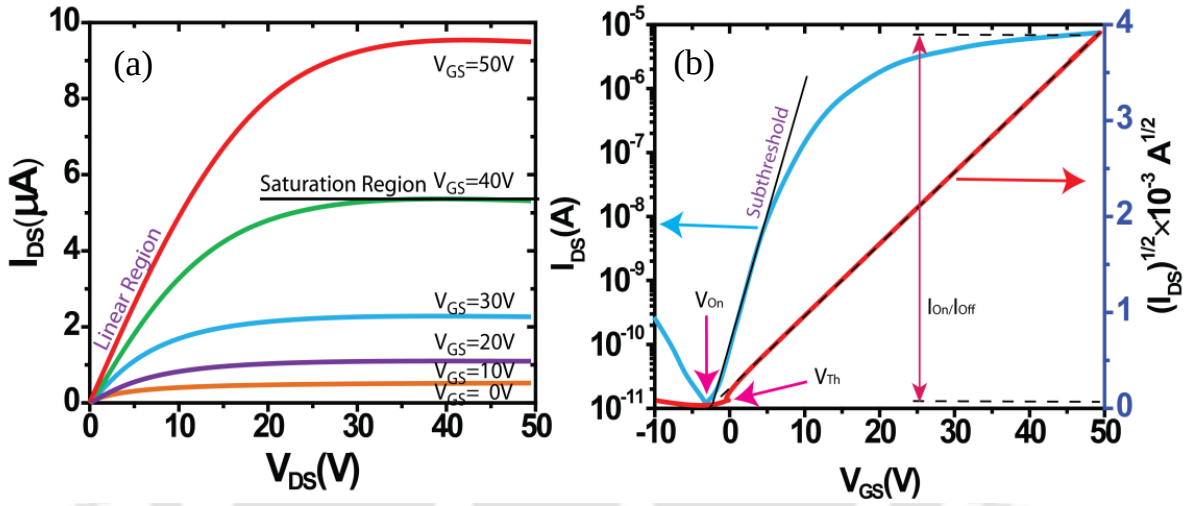


Figure 1.2: a) Output characteristic and b) transfer characteristic of OFET.

There are several analytical models[11-14] for current-voltage characterization of OFETs. The parameters for OFET characterization are extracted however from expression of drain current derived from traditional inorganic MOSFET model. The regions of operation are determined by the values of applied voltages, V_{DS} and V_{GS} as shown in **Figure 1.2**. The device is operated in the linear regime for $|V_{DS}| \leq |V_{GS} - V_t|$. In linear regime the current I_{DS} varies linearly with V_{DS} and is given by:

$$I_{DS} = \frac{W}{L} C_{ox} \mu (V_{GS-} V_t) V_{DS} \qquad (1.1)$$

and in saturation regime for $|V_{DS}| \geq |V_{GS} - V_t|$, I_{DS} becomes independent of V_{DS} and varies as square of V_{GS}. In saturation regime I_{DS} is given by:

$$I_{DS} = \frac{W}{L} C_{ox} \mu (V_{GS-} V_t)^2 \qquad (1.2)$$

Here, C_{ox} is the capacitance of the insulator, μ is field-effect carrier mobility and V_{GS}, V_{DS} and V_t are the gate-source, drain-source and threshold voltages respectively. W (width) and L (length) are the dimensions of the semiconductor channel defined by the source and drain electrodes.

Field-Effect Mobility

The carrier field-effect mobility in the linear regime can be extracted from the transconductance, g_m which is the change of I_{DS} with V_{GS} for a small drain voltage, V_{DS}. From Equation (1.1), g_m is given by

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}=small\ constant} = \frac{W\mu C_{ox}}{L} V_{DS} \qquad (1.3)$$

Therefore, the linear mobility solved from Equation (1.1) is given as:

$$\mu = g_m \left.\frac{L}{WC_{ox}V_{DS}}\right|_{V_{DS}=small\ constant} \qquad (1.4)$$

The field-effect mobility in the saturation regime is also extracted from the transfer characteristics (I_{DS} vs. V_{GS}). Equation (1.2) shows that the square root of the saturation current is linearly dependent on the gate voltage. The field-effect mobility can be extracted from the slope of the curve which plots the square root of the saturation current as a function of gate voltage V_{GS}, as shown in **Figure 1.2**. The mobility can be calculated from Equation (1.2) and is given as:

$$\mu = 2\frac{L}{WC_{ox}V_{DS}}\left(\frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}}\right)^2 \qquad (1.5)$$

Threshold Voltage

The threshold voltage can be defined as the gate voltage at which the conduction channel starts to form. V_t can be extracted by plotting. I_{DS} vs V_{GS} and extrapolating to I_{DS}=0. For many applications, low V_t are required to keep the drive voltage low.

Current On/Off ratio

Ion/Ioff is the ratio of the maximum I_{DS} ("on" current) value to the minimum I_{DS} ("off" current) value, obtained from transfer characteristics plotted on a logarithmic scale. The ratio characterizes the ability of the device to switch a signal from "on" to "off".

Subthreshold Swing

Subthreshold slope 'S' is defined as the rate at which I_{DS} varies (in decades) with V_{GS}

for device operation in the subthreshold region. It describes the turn-on characteristics of the device and is given as:

$$S = \frac{dV_{GS}}{d\log I_{DS}} \quad (1.6)$$

'S' can be extracted by fitting a line to the steepest part in the subthreshold region and calculating its inverse.

The trap density, N_{trap} can be calculated from SS.

$$N_{trap} = \left(\frac{SS \times q \times \log e}{KT} - 1\right)\frac{C_o}{q} \quad (1.7)$$

Contact Resistance:

The contact resistance (R_C) in organic transistors, as well as channel resistance (R_{ch}), has a significant effect on device performance. The total resistance of the device (R_{on}) is:

$$R_{on} = R_{ch} + R_c \quad (1.8)$$

While $$R_c = R_{source} + R_{drain} \quad (1.9)$$

where R_{source} and R_{drain} are the source and drain contact resistances respectively

The contact resistance depends on the structure of the transistor and the nature of the electrodes, e.g., its work function. It also decreases with increasing gate voltage. This can be explained by the increased density of charge carriers in the channel and close to the contacts that would have a similar effect as doping the contacts.[15, 16] Contact resistance are often higher in the bottom-contact structure and depend on the drain voltage. The differences existing in bottom-contact and top-contact devices can have various origins. One reason can be the larger injection surface in a top-contact structure or non-uniform and disturbed growth of organic material by triple interfaces in bottom-contact structures. [16, 17]

1.4 Interfaces in OFET

The most important parameter to define an OFET performance is the field-effect mobility (μ_{FET}). Higher mobility ensures wider applications of the OFET. The mobility

depends on charge transport which is profoundly regulated by the interfaces in the OFET. The four basic interfaces in a bottom gate top contact OFET are, the metal/dielectric, OSC/atmosphere, dielectric/OSC and metal/OSC interface. A schematic representation of all the four interfaces affecting the OFET performance is shown in **Figure 1.3**. The interface roughness of the gate electrode and dielectric is important for the devices with ultra-thin dielectrics in which with the increase in roughness, there is an increase in the leakage current.[18] The OSC/atmosphere interface affects the device performance as the atmospheric oxygen and moisture may induce undesirable charge carrier trapping in the OSC. This interface becomes more important for sensor applications as the output depends on the adsorption of the analyte. By strategic material design, we can make the OSC environmentally robust. For an OFET the two interfaces are critical: the interface between the semiconductor and metal electrodes, where the charge injection takes place and the other is the interface between the dielectric and OSC, where the charge transport takes place.

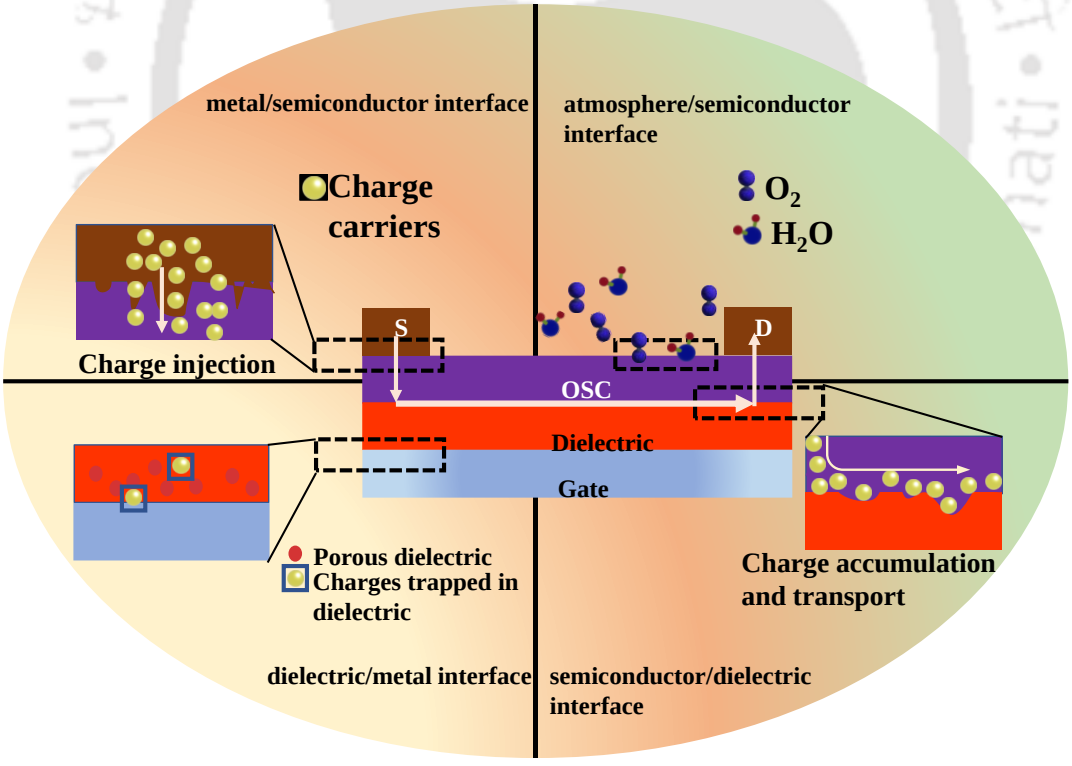


Figure 1.3: Schematic illustration of the four crucial interfaces in a bottom gate top contact OFET.

1.4.1 OSC/dielectric

The OSC/dielectric interface is the most crucial as the charge transport takes place at the dielectric surface and within a few nanometers of the interface. Since in BGTC the

semiconductor is deposited directly on the dielectric surface, the interfacial properties determine the morphology and the molecular structure of the OSC thin film. The trap states at the dielectric surface and the bulk of semiconductor will lead to non-idealities in the device. For polymer dielectric containing functional groups like -OH, -NH_2, -COOH the surface energy is high and are the main origin of traps. [19] There are many dielectric modification techniques reported to reduce the interfacial traps like the use of self-assembled monolayer (SAM), using bilayer dielectric system, crosslinking of dielectrics.[20-25]

1.4.2 OSC/metal

The OSC/metal interface is important because the charge injection from source/drain electrodes to the semiconductor bulk takes place here. The contact resistance is decided by the quality of this interface. For an ideal OFET characteristics, the source/drain contacts should be ohmic, i.e., the contact resistance should be negligible compared to the channel resistance. Though high potential barrier exists in most metal/OSC interfaces, however ohmic contact is possible. As charge injection is mostly field emission or defect assisted instead of thermionic. The device architecture also influences the OSC/metal interface depending on the difference of fabrication step and contact area of top-contact and bottom-contact configurations. In top-contact the semiconductor is grown on the dielectric and defects may arise at the metal/OSC contact by deposition of hot metal on the semiconductor, the area of contact is less compared to bottom contact. In case of bottom-contact, the semiconductor film is deposited on the metal and many researchers have reported that the morphology of the semiconductor in the vicinity of the metal is non-ideal mostly due to heterogeneous nucleation process. Hence pretreatment processes are also reported for contact modification in both top-contact and bottom-contact configurations.[18, 26] For better injection properties, chemical modifications by thiols, disulfides are commonly used to tune the work function, also deposition of wide band gap compounds like MoO_X before metal deposition is another widely adopted interfacial engineering technique.

1.5 Choice of dielectric

The choice of gate insulator or the dielectric plays a crucial role in determining the performance of Organic Field Effect Transistor (OFET). The performance defining parameters of OFET like threshold voltage, mobility, sub-threshold swing, and I_{ON}/I_{OFF}

ratio, hysteresis can be controlled with proper selection of the dielectric layer. The interaction of the semiconductor with the dielectric not only affects semiconductor layer morphology but also changes the Density of States (DoS) due to the effect of local polarization at the interface.[27-29] The dielectric constant has been another point of debate as issues like gate leakage current and power consumption can be reduced by using high-K dielectrics, which in turn will increase the energy disorder caused by randomly oriented dipoles, attributing to poor semiconductor-dielectric interface resulting in poor performance of high-k dielectric. However there are reports that low-k polymer dielectric CYTOP, PMMA offers better interface for charge transport which results in higher mobility and on/off ratio when compared with high-k dielectric P(VDF-TrFE-CTFE).[30] High K dielectrics have high surface energy which negatively impacts mobility. Nevertheless, there are reports on surface energy match of the dielectric with the semiconductor resulting in obtaining maximum mobility.[31, 32] The good dielectric material will possess a smooth dielectric surface, large energy band gap, high dielectric constant, and less surface energy. To achieve these, techniques like, crosslinking of High-K polymer dielectric, surface treatments by using Self Assembled Monolayers (SAMs) and bilayer dielectric system has been reported as a solution to Interfacial trap states.[33-35] Incomplete crosslinking may generate interfacial states at the d/s interface as a result of leftover reagents or unsatisfied bonds. The polar groups of the interfacial dielectric or the SAM layer influence the transistor parameters.[36] For example, the presence of electron-withdrawing groups like -F will attract electrons from the semiconductor film and will result in a positive shift in p-type OFET, on the contrary for electron-donating groups like -NH_2 will result in a negative V_{TH} shift.[37-39] Presence of moisture is another factor affecting the OFET performance by inducing hysteresis and then degrading the device. Hydroxyl groups in polymer dielectric can attract moisture, there are reports on the reduction of hydroxyl group concentration.[40] Not drying the dielectric properly before deposition of the semiconductor layer can also induce high hysteresis.[19]

1.6 Solution processing for flexible OFET

Solution processability offers perks like ease of processing, low-cost, low-temperature processing attributed to the nature of weak Vander Waals intermolecular interactions. With just π-π conjugation the organic compounds are insoluble, and side chains are incorporated to increase the solubility. There are several methods for solution processing like the spin coating, drop casting, inkjet printing, screen printing, doctor

blading. Spin coating results in fast evaporation of solvent, allowing lesser time for molecular ordering but forms more homogeneous film. The study of the growth mechanism is crucial to understand and control the charge transport properties. The factors affecting the polymer growth during solution processing are the volatility of the solvent, solubility of the polymer, nature of the substrate, surface growth, solvent evaporation rate, molecular weight, π conjugation of backbone, side chain.

1.7 Charge transport in OFET

Understanding the charge transport mechanism is important for designing a high mobility OFET. Especially the charge transport in Donor-Acceptor (D-A) π-conjugated polymers is critical and still not clear. Mobility greater than a-Si has been reported till date for D-A polymer based FET.[20]

1.7.1 Transport Models

Various models have been suggested to understand the charge transport, like the multiple trap release (MTR) model and mobility edge model, which applies to crystalline ordered semiconductors, for example, single crystals and polycrystalline thermally deposited small molecule thin films. For amorphous and disordered materials, variable range hopping (VRH) model,[41] and percolation models are mostly applied. However, in solution-processed conjugated polymer thin film the small polaron model is applied typically as in solution-processed thin films, delocalization degrees are lower and energetic disorders are higher compared to the vacuum-deposited film.

1.7.2 Traps in organic semiconductor

There are several sources of trap sites in organic solution processed semiconductors:

- The presence of chemical impurities having energy levels in between the HOMO/LUMO of the semiconductor material will act as trap
- Structural defects in the polymer structure will act as trap. As the HOMO/LUMO is also affected by the electronic polarization of the surrounding of the material. The HOMO/LUMO of the material is determined by the effective conjugation length. These traps arising from structural imperfections can be shallow traps or even deep traps like that arising from huge grain boundaries.

- Self-trapping can be induced by formation of polarons as excess carrier lead to molecular deformation. Especially in some polymers like polythiophene, these excess charge carriers forms a self-trap.

1.7.3 Polymer thin film morphology

The polymer thin film morphology plays a huge rule in determining the charge transport and hence the OFET performance. Charge transport is affected by the local structural disorder of the polymer chain in nano level, crystallinity, size of the grains and grain boundaries in macro level. The grains are the regions where the arrangement of the molecule is ordered hence forms crystalline domains and charge transport easily occurs, where the grain boundaries molecule is disordered and there is a high potential drop bet ween the grains resulting in hampered charge transport. Solution processed films shows various types of morphologies ranging from amorphous texture to nanofibrils depending on 1) coating surface 2) solvent used 3) processing technique 4) molecular weight. Characterization techniques like the Atomic Force Microscopy (AFM), Field emission scanning electron microscopy (FESEM), X-ray diffraction (XRD), Ultraviolet–visible (UV-vis) spectroscopy are utilized to study the morphology and crystallinity of the thin film. Solution state UV-Vis is also employed to understand the solvent and additive-induced changes in the polymer chain. Different processing techniques are reported to control the thin film morphology which includes applying strain, rubbing, using additives and templates for obtaining the required edge-on or face-on orientation polymer chain orientation.[42, 43] Though edge-on orientation is favorable for in-plane charge transport, however face-on orientation is also reported in some cases to improve the charge transport properties.

1.7.3 Role of solvent additives

Inclusion of solvent additive is a strategy to modulate the solution processed thin film. Various mechanisms for explaining the effect of solvent additive on thin morphology is reported. Another reported mechanism to explain the role of additives is the varying solubility of molecules helps in obtaining the required molecular ordering of morphology, other is the varying volatility of the binary solvents. Solvent additives are also reported to help fill in the grain boundaries and reduce traps. This method is well established to improve the morphology in the bulk-heterojunction solar cell by promoting phase separation of the donor and acceptor depending on the difference in solubility. However,

this technique is not much explored for transistors and the transport mechanism in OFETs is completely different from solar cell. Because of this change in charge transport mechanism, the solvent additives are much more effective for OFET than solar-cell.

1.8 Applications in Optoelectronic Integrated circuit

The use of OFET in integrated circuit was limited because of the low mobility. However, with slight improvement in mobility, the OFET based circuits can be easily implemented in low-end applications like as basic circuits component in RFID, sensors, memory, driving circuit in displays and e-paper, where low cost, easy processing and, flexibility are more important than high speed operation. Depending on the properties of the active material, the OFET can have applications in different types of sensors. For example, photoactive materials can help to implement photo-transistors, which can be implemented in different dual input logic gates.

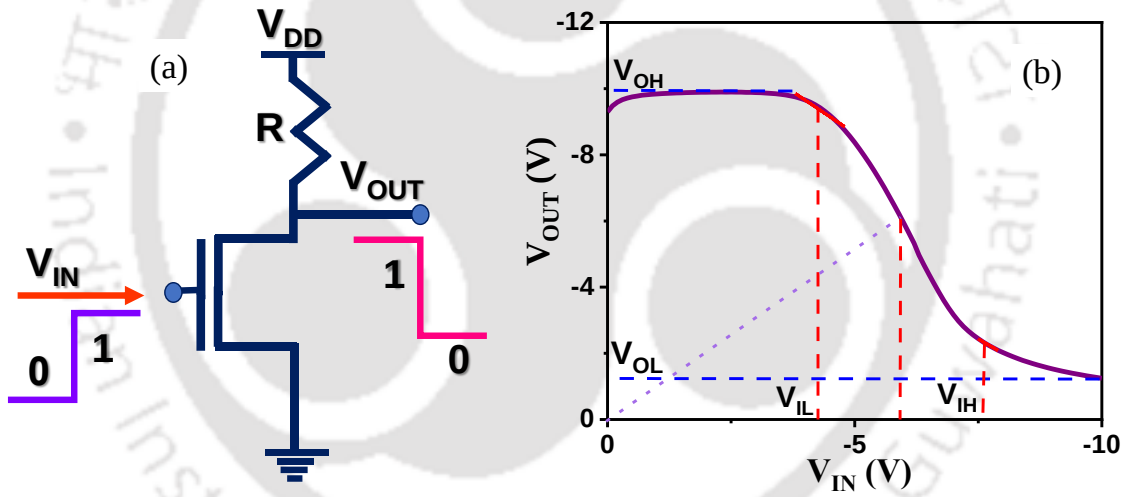


Figure 1.4: (a) Circuit diagram (b) voltage transfer characteristic (VTC) of a basic resistive load inverter.

1.8.1 Phototransistor

A phototransistor (PT) converts the light signal to detectable electrical signal and also amplifies it. Hence, compared to other photodetectors, it provides better functionality.[44] The first organic phototransistor (OPT) was reported in 2001 which used polymer poly-3-octylthiophene-2,5-diyl (P3OT) as the active material,[45] This was followed by a lot of other reports on OPT and a tremendous improvement in properties was observed.[46-49] The increased photocurrent to dark current ratio obtained was higher than that in amorphous silicon based PT.[50] The active material can be chosen according to the required working wavelength. Organic materials offer advantage of easily tunable band gap

and hence can have a wide range of absorptions. When the light wavelength matches the semiconductor's band gap, it is absorbed which produces excitons that further contributes to the charge transport. All the regions of the spectrum have various applications like the phototransistor working in UV region can be employed in communication, security and the one working in IR and NIR can have application in biomedical devices. Hence owing to their high-cost production and structural rigidity, inorganic semiconductors are not suitable for applications requiring structural flexibility, lightweight, low cost and large-scale production. The parameters that determine the phototransistor performance are photocurrent (I_{ph}), responsivity (R) and detectivity (D*).

$$R = \frac{(I_{ph} - I_D)}{P_{in}\, x\, S} \qquad (1.10)$$

$$D^* = R\, x\, S^{1/2}(2eI_D)^{-1/2} \qquad (1.11)$$

where I_{ph} represents the source-to-drain current under illumination; I_D is the source–drain current under dark; and P_{in} represents the power of the incident light per unit area, respectively. e is the charge of an electron. *S* is the effective sensing area of the device.

1.8.2 OFET for Logic gates

A logic gate is the fundamental decision-making component of any digital circuit. It performs Boolean functions based on a one or more inputs, to generate a single output. Logic gates are implemented with transistors. There are different ways of constructing a logic gate. It can be implemented with combination of only transistors (TTL) or combination of diode transistor (DTL) or resistor transistor (RTL) etc. The most fundamental logic gate is the NOT gate or inverter which inverts the single input variable. A simple resistive load inverter circuit is shown in **Figure 1.4a**. The inverter circuit is the basis of logic circuit as utilizing the same design and analysis principles, other complex logic gates like the NOR, OR, NAND gates can be implemented. The performance determining parameters for inverter that can be extracted from the voltage transfer characteristic (VTC) (**Figure 1.4b**) are: gain, noise margin, static power dissipation.

The steady-state behavior of the inverter is determined by the five critical voltage levels labeled in the VTC (**Figure1.4b)**:

1) V_{OH} is the output high voltage, which is the maximum output voltage when the output level is logic '1' that can be obtained from inverter. When the input voltage (V_{IN}) is low, the output voltage, $V_{OUT} = V_{DD}$.

2) V_{OL} is the minimum output voltage when the output is logic '0'. When V_{IN} is high i.e., $V_{IN}=V_{DD}$, the transistor is operating in the linear region and the output will be at low state having value between 0 and V_{DD}.

3) V_{IL} is the low input value at which the VTC slope becomes equal to -1 ($dV_{OUT}/dV_{IN}=-1$). At V_{IL} the output voltage, V_{OUT} is slightly lower than V_{OH}.

4) V_{IH} is the high input voltage and a transition point at which $dV_{OUT}/dV_{IN}=-1$ but V_{IH} is the larger between the two input transition points. It can be observed from **Figure 1.4b** that at V_{IH} the V_{OUT} is slightly higher than V_{OL}

5) V_{th} is threshold voltage of the inverter at which the transition occurs and in VTC, V_{IN} becomes equal to V_{OUT}.

The two noise margins (NM) are the noise margin for low level (NM_L) and the noise margin for high level (NM_H).

$$NM_L = V_{IL}-V_{OL} \quad (1.12)$$

$$NM_H = V_{OH}-V_{IH} \quad (1.13)$$

The gain of the inverter is defined as dV_{OUT}/dV_{IN}, and the Static power dissipation is given by: $P_D = V_{DD} \times I_D$ (1.14)

1.8.2 Opto-logic gates

Opto logic gate is a circuit which deploys a phototransistor in a logic gate circuit. It is a more advanced optoelectronic application beyond a basic unit phototransistor. This can be implemented in any circuit requiring a photodetector and a logic gate to reduce the number of components and complexity. An opto logic gate can operate with both light and electrical input and hence different logics can be implemented with this bifunctional circuit.

1.9 Thesis Overview

Considering the need for high performance, lowcost and flexible OFET for advancement of organic electronics, the inspiration of this thesis was the development of solution processing techniques for OFETs and their application in integrated circuit. The working chapters of this thesis can be divided into three parts. The first part is concentrated on understanding charge transport and the role of traps. The second part is an effort to improve the charge transport and the third part is the implementation of the improved devices in Logic gates. The results obtained during the course of this thesis work are divided into four chapters and in conclusion, thesis summary and future prospects are discussed. A brief overview of the chapters is given below:

Chapter 2 focuses on understanding the d/s interface. Specially in solution processed, the d/s interfacial defects and traps plays a crucial role in determining the charge transport and hence the device performance. Three devices with different interfacial dielectric are fabricated and characterized. Impedance spectroscopy is utilized to investigate the interface and find the reason for variation in device performance with the change in the interfacial dielectric. Thereafter a flexible solution processed OFET was fabricated with the optimized parameters. The device showed mechanical stability and was able withstand a strain of ~2.5%.

Chapter 3 deals with improvement of the semiconductor thin film morphology for efficient utilization of the device in phototransistor. Two solvent additives 1,8-diiodooctane (DIO) and 1,8-dibromooctane (DBrO) are employed to study the effect of solvent additive in controlling the semiconductor morphology. The OFET showed a ~3 folds improvement in mobility from 0.08 to 0.22 $cm^2\ V^{-1}\ s^{-1}$ with the inclusion of DBrO as solvent additive. The device showed improvement in bias stress stability in dark and under illumination.

Chapter 4 studies the effect of a series of aromatic (naphthalene) based solvent additives in determining the performance of the solution processed OFET. Three additives namely, 1-Chloronaphthalene (CN), 1-Bromonaphthalene (BN), 1-Iodonaphthalene (IN), are studied, and a significant improvement in OFET performances have been demonstrated. Morphological, photophysical and electrical characterization was conducted to support these findings. Visible change in the semiconductor morphology with the incorporation of solvent additives leading to thin-film packing crystallinity improvement was observed. An optimum condition has been achieved as the film formation time can be modulated with the use of additives. The stability of the device also improved as the traps related to the

disordered film are reduced improving the charge transport. As a result, a significant improvement in the mobility of the PTB7-Th based OFET has been observed from a mobility of 0.9 $cm^2 V^{-1} s^{-1}$ obtained for the control device to a mobility of 0.5 $cm^2 V^{-1} s^{-1}$ for the BN modified device.

Chapter 5 demonstrates the application of the photo-active semiconductor PTB7-Th based solution processed phototransistor. Thereafter the phototransistor is integrated with a solution processed resistor to implement NOT gate. Employing the photoactive property of the OFET, opto inverter is demonstrated. On simultaneous application of both the light and electrical input signal a complete solution processed dual input logic gate circuit is demonstrated on ultra-flexible PI substrate. The circuit consisted of a PT with high mobility of 0.5 $cm^2 V^{-1} s^{-1}$ and responsivity of 688 A/W. The PT is integrated with a simple drop casted resistive load. This simple circuit design showed comparable performance with the complementary OFET based circuits. The opto-electrical inverter showed a Noise margin for logic low (NM_L) of 60% and Noise margin for logic high (NM_H) of 98%. The delay for the voltage pulse input was 0.12 s and for light input was 0.16 s. Thereafter, both electrical and optical inputs were applied simultaneously and dual input NOR logic was demonstrated.

Chapter 6 illustrates the summary and the future prospects of this thesis. A concise discussion on the main research results is presented along with the future prospects of the solution processed OFET and their application in integrated circuits.

References

1. P. Ghamari, M. R. Niazi and D. F. Perepichka, *Chem. Mater.*, 2021, **33**, 2937-2947.
2. C. Lee, W. Lee, H. Kim and Y. Kim, *Macromol. Rapid Commun.*, 2022, **43**, 2100922.
3. K. Ishida, T.-C. Huang, K. Honda, T. Sekitani, H. Nakajima, H. Maeda, M. Takamiya, T. Someya and T. Sakurai, *IEEE J. Solid-State Circuits*, 2011, **47**, 301-309.
4. H.-Y. Tseng and V. Subramanian, *Org. Electron.*, 2011, **12**, 249-256.
5. Y. Yan, Y. Zhao and Y. Liu, *J. Polym. Sci.*, 2022, **60**, 311-327.
6. 1,745,175, 1926.
7. H. Kallmann and M. Pope, *Nature*, 1960, **186**, 31-33.
8. C. K. Chiang, C. R. Fincher, Y. W. Park, A. J. Heeger, H. Shirakawa, E. J. Louis, S. C. Gau and A. G. MacDiarmid, *Phys. Rev. Lett.*, 1977, **39**, 1098-1101.
9. The Nobel Prize in Chemistry 2000, <https://www.nobelprize.org/prizes/chemistry/2000/summary/>).
10. A. Tsumura, H. Koezuka and T. Ando, *Appl. Phys. Lett.*, 1986, **49**, 1210-1212.
11. M. Pei, J. Guo, B. Zhang, S. Jiang, Z. Hao, X. Xu and Y. Li, *Advances in Physics: X*, 2020, **5**, 1747945.
12. G. Horowitz, in *Semiconducting Polymers*, 1999, DOI: https://doi.org/10.1002/3527602186.ch14, pp. 463-514.
13. C. D. Dimitrakopoulos and P. R. L. Malenfant, *Adv. Mater.*, 2002, **14**, 99-117.
14. P. G. Le Comber and W. E. Spear, *Physical Review Letters*, 1970, **25**, 509-511.
15. G. Kim, C. Fuentes-Hernandez, S. Choi, X. Jia and B. Kippelen, *Appl. Phys. Lett.*, 2021, **119**, 263301.
16. R. A. Street and A. Salleo, *Appl. Phys. Lett.*, 2002, **81**, 2887-2889.
17. D. J. Gundlach, L. Zhou, J. A. Nichols, T. N. Jackson, P. V. Necliudov and M. S. Shur, *J. Appl. Phys.*, 2006, **100**, 024509.
18. J. Y. Son, W. J. Maeng, W.-H. Kim, Y. H. Shin and H. Kim, *Thin Solid Films*, 2009, **517**, 3892-3895.
19. Y. H. Noh, S. Young Park, S.-M. Seo and H. H. Lee, *Org. Electron.*, 2006, **7**, 271-275.
20. H. J. Cheon, T. K. An and Y. H. Kim, *Macromol. Res.*, 2022, **30**, 71-84.

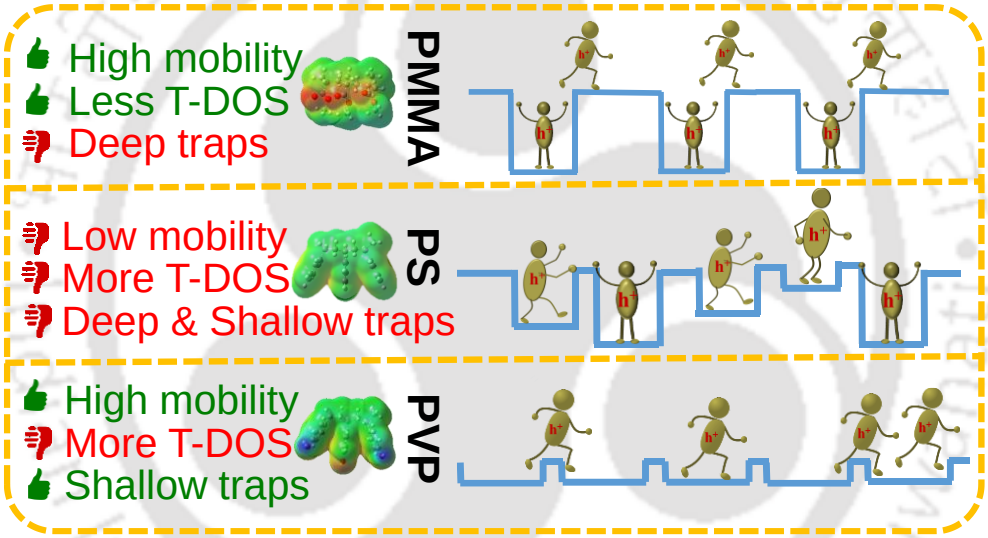
21. H.-j. Kwon, H. Ye, K. Shim, H. G. Girma, X. Tang, B. Lim, Y. Kim, J. Lee, C. E. Park, S.-H. Jung, J. M. Park, Y. J. Jung, D.-H. Hwang, H. Kong and S. H. Kim, *Adv. Funct. Mater.*, 2021, **31**, 2007304.
22. H. Ren, Y. Tong, M. Ouyang, J. Wang, L. Zhang, Y. Fu and Q. Tang, *IEEE Trans. on Electron Devices*, 2022, DOI: 10.1109/TED.2022.3191283, 1-6.
23. Z.-G. Gu, S.-C. Chen, W.-Q. Fu, Q. Zheng and J. Zhang, *ACS Appl. Mater. Interfaces*, 2017, **9**, 7259-7264.
24. Y. Lei, B. Wu, W.-K. E. Chan, F. Zhu and B. S. Ong, *J. Mater. Chem. C*, 2015, **3**, 12267-12272.
25. Y. Yang, Y. Hong and X. Wang, *ACS Appl. Mater. Interfaces*, 2021, **13**, 8682-8691.
26. D. Liu and Q. Miao, *Mater. Chem. Front.*, 2018, **2**, 11-21.
27. I. N. Hulea, S. Fratini, H. Xie, C. L. Mulder, N. N. Iossad, G. Rastelli, S. Ciuchi and A. F. Morpurgo, *Nat. Mater.*, 2006, **5**, 982-986.
28. X. Wu, R. Jia, J. Pan, X. Zhang and J. Jie, *Nanoscale Horiz.*, 2020, **5**, 454-472.
29. M. I. Nugraha, R. Häusermann, S. Watanabe, H. Matsui, M. Sytnyk, W. Heiss, J. Takeya and M. A. Loi, *ACS Appl. Mater. Interfaces*, 2017, **9**, 4719-4724.
30. Y. Wang, X. Huang, T. Li, L. Li, X. Guo and P. Jiang, *Chem. Mater.*, 2019, **31**, 2212-2240.
31. S.-H. Lee, Y. Xu, D. Khim, W.-T. Park, D.-Y. Kim and Y.-Y. Noh, *ACS Appl. Mater. Interfaces*, 2016, **8**, 32421-32431.
32. X. Sun, C.-a. Di and Y. Liu, *J. Mater. Chem.*, 2010, **20**, 2599-2611.
33. J. F. Martínez Hardigree, T. J. Dawidczyk, R. M. Ireland, G. L. Johns, B.-J. Jung, M. Nyman, R. Österbacka, N. Marković and H. E. Katz, *ACS Appl. Mater. Interfaces*, 2013, **5**, 7025-7032.
34. A. R. V. Benvenho, W. S. Machado, I. Cruz-Cruz and I. A. Hümmelgen, *J. Appl. Phys.*, 2013, **113**, 214509.
35. X. Cheng, M. Caironi, Y.-Y. Noh, J. Wang, C. Newman, H. Yan, A. Facchetti and H. Sirringhaus, *Chem. Mater.*, 2010, **22**, 1559-1566.
36. U. Zschieschang, F. Ante, M. Schlörholz, M. Schmidt, K. Kern and H. Klauk, *Adv. Mater.*, 2010, **22**, 4489-4493.
37. E.-S. Shin, W.-T. Park, Y.-W. Kwon, Y. Xu and Y.-Y. Noh, *ACS Appl. Mater. Interfaces*, 2019, **11**, 12709-12716.
38. S. Riera-Galindo, L. Chen, M. S. Maglione, Q. Zhang, S. T. Bromley, C. Rovira and M. Mas-Torrent, *Applied Physics A*, 2022, **128**, 322.

39. A. Ulman, *Chem. Rev.*, 1996, **96**, 1533-1554.
40. M. N. Tousignant, N. A. Rice, J. Niskanen, C. M. Richard, D. Ritaine, A. Adronov and B. H. Lessard, *Adv. Electron. Mater.*, 2021, **7**, 2100700.
41. R. M. Hill, *physica status solidi (a)*, 1976, **34**, 601-613.
42. M. J. Han, M. McBride, B. Risteen, G. Zhang, B. V. Khau, E. Reichmanis and D. K. Yoon, *Chem. Mater.*, 2020, **32**, 688-696.
43. D. Gargi, R. J. Kline, D. M. DeLongchamp, D. A. Fischer, M. F. Toney and B. T. O'Connor, *J. Phys. Chem. C*, 2013, **117**, 17421-17428.
44. B. Mukherjee, M. Mukherjee, Y. Choi and S. Pyo, *ACS Appl. Mater. Interfaces*, 2010, **2**, 1614-1620.
45. K. S. Narayan and N. Kumar, *Appl. Phys. Lett.*, 2001, **79**, 1891-1893.
46. S. Dutta and K. S. Narayan, *Adv. Mater.*, 2004, **16**, 2151-2155.
47. X. Tong and S. R. Forrest, *Org. Electron.*, 2011, **12**, 1822-1825.
48. K. Swathi and K. S. Narayan, *Appl. Phys. Lett.*, 2016, **109**, 193302.
49. S. Dutta and K. S. Narayan, *Phys. Rev. B*, 2003, **68**, 125208.
50. Y.-Y. Noh, D.-Y. Kim, Y. Yoshida, K. Yase, B.-J. Jung, E. Lim and H.-K. Shim, *Appl. Phys. Lett.*, 2005, **86**, 043501.

Chapter 2

Tailoring Trap Density of States through Impedance Analysis for Flexible Organic Field-Effect Transistor

---



Manuscript: Anwesha Choudhury, Ritesh Kant Gupta, Rabindranath Garai, Parameswar Krishnan Iyer, "Tailoring Trap Density of States through Impedance Analysis for Flexible Organic Field-Effect Transistors." *Adv. Mater. Interfaces* **2021,** *8* (15), 2100574, DOI: 10.1002/admi.202100574

[This page was intentionally left blank]

Abstract

The selection of dielectric material impacts the dielectric/semiconductor (D/S) interface which plays a significant role in defining the device performance. Hence, investigation of the D/S interfacial defects and trap states is essential for improving the device performance and designing new semiconductor and dielectric materials for OFET. Here, the trap density of states (T-DOS) at the interface is investigated by impedance spectroscopy (IS). OFETs were fabricated with three different dielectric combinations and the highest mobility was found to be 0.12 cm^2/V-s. Detailed analysis of the semiconductor thin film and the D/S interface was performed by AFM, PL, TRPL and was found consistent with the DOS analysis. This work validates that IS can be utilized as a prospective DOS analysis method for OFET applications. Finally, for evaluating the potential application of the device architecture towards developing flexible electronic circuit components, the device was fabricated on a flexible substrate and the mechanical stability was examined by subjecting the device to a strain of 2.5 %. The device showed no significant degradation in the operation confirming its practical utility.

2.1 Overview

Organic Field Effect Transistors (OFETs) are the basic building blocks of any flexible and low-cost electronic system like wearable sensors, e-skin, active matrix for displays.[1-5] Since the first report of OFET in the 1980s,[6] this field has attracted tremendous research interest. New organic semiconductor materials are being designed and advanced fabrication techniques are being developed for OFET.[7-9] Mobility values of OFETs are now challenging the mobility of amorphous silicon.[10-13] For further development of reliable OFET device, other parameters related to the dielectric layer and the D/S interface need to be extensively studied.

Various inorganic and organic gate dielectric materials and their modifications are studied to date, including self-assembled monolayers, multi-layer dielectric, dielectric cross-linking, etc.[14-16] Among diverse dielectric materials, polymer dielectrics are best suited for flexible OFET because of their intrinsic flexibility and compatibility with both organic semiconductor active layer and flexible substrates.[17, 18] However, the polar side groups of polymer dielectric induce shallow traps at the interface and the effect of dielectric polarity on device characteristics was systematically studied by adopting different combinations of semiconductors and multi-layer dielectric systems.[19] The polarization of dielectric and the effect of polymer dielectrics with polar groups in enhancing the sensitivity of various OFET-based sensors like temperature, humidity and photo transistors are reported.[20, 21] Other than the choice of semiconductor and dielectric, D/S interface also plays a very crucial role in defining the performance of OFET. Although the semiconductor is the active layer, accumulation of charges and charge transport occurs within a few nanometers of the D/S interface. The D/S interface not only affects the morphology of the active layer but also defines the charge carrier transport in it.[22-24] Over the last decade, the charge carrier mechanism and its transport in a semiconductor is being studied thoroughly. In contrast, understanding the effect of dielectric in defining charge transport is still in its infancy stage.[25, 26] The charge transport can be well understood by determining the density of states (DOS).[27] Analysis and understanding the DOS can help achieve better charge transport, stability and reproducibility of the device. The main factor that determines T-DOS in OFET with similar semiconductor morphology is the nature of dielectric.[28] Various experimental and analytical methods have been reported to estimate the DOS, which includes optical, electrical and thermal measurement tools.[29-31] The scanning probe techniques

are used to study the T-DOS as the presence of trapped charges modifies the contact potential. Hence, this is reported as an efficient tool for determining the origin and spatial distribution of traps.[32-35] Some other experimental methods like space charge limited current (SCLC), thermal admittance spectroscopy (TAS), driven level capacitance profiling (DLCP) method are also reported for single semiconductor layer trap study in solar cell study.[36-38] These studies are done for the vertical charge transport whereas in transistor system which requires both vertical and horizontal transport, this is not yet extensively studied. Analytical methods based on temperature dependence conductivity of OFET were used to determine the DOS spectrum.[39, 40] The estimation of subthreshold swing (SS) from transfer characteristics of transistor gives an overall idea of the trap states. However, the investigation of the energy distribution of interfacial traps is complex and requires assumptions and equivalent circuit modeling. Impedance Spectroscopy (IS) is an effective method for determining the energetic distribution of T-DOS and not yet explored in the study of OFET. IS has been used as a tool for determining carrier recombination in solar cell and hence can be a possible method for analyzing charge trapping and release in OFETs.[41, 42] It is well known that the -OH group acts as the electron trap and the hysteresis in the electrical characteristics is because of the moisture related impurity, trapped by the hydrophilic polar dielectric material which degrades the dielectric properties and causes interfacial traps.[11] Slow polarization of hydroxyl groups is yet another reported reason for hysteresis in OFET devices.[43] The characterizations like SS and hysteresis study give an overall idea of charge carrier traps. Yet, the origin of these traps is not established correctly. Hence, a more reliable and simple technique is essential to understand the mechanism of trapping/de-trapping and their position whether these traps are interfacial traps or bulk traps. The organic-organic interface is complicated and complex interaction takes place at the interface, which affects the transistor properties, and all these changes in OFET properties are carefully examined here.

In this work, IS has been utilized as an effective method to obtain the DOS spectrum for the interfacial trap study. We have shown how the interface governs the performance of the device. We have fabricated transistors with different dielectrics and studied how the choice of dielectric and D/S Interface affects DOS and plays a crucial role in controlling the transistor characteristics. To further verify the findings of IS, characterization techniques like AFM, PL, and TRPL are performed. The presence of dipolar molecules at the D/S interface also affects the transistor parameters. Three dielectrics with different polarity and permittivity were chosen and

their respective interface DOS is studied for a better understanding of the effect of dielectric surface polarity, surface energy and dielectric constant (k) on transistor properties. Highest mobility of 0.120 cm^2/V-s, 0.095 cm^2/V-s, and 0.050 cm^2/V-s is obtained for the device having PVP, PMMA, and PS as the interfacial dielectric respectively. Enhanced device performance is observed for the device with lowest T-DOS. This work provides IS as an efficient tool for understanding the different characteristics of OFET.

2.2 Experimental Section

2.2.1 Materials

PTB7-Th was thermally synthesized according to the previous literature.[8] Poly(methyl methacrylate) (average Mw ~ 996 kDa), Polystyrene (average Mw ~ 350kDa), Poly(4-vinylphenol) (average Mw ~ 25 kDa), Molybdenum(VI) oxide, Aluminium wire (Al) and Copper (Cu) wire were purchased from Sigma Aldrich and PVA (average Mw ~ 115 kDa) from Loba Chemicals and used without further purification. FTO of 13 Ω/□ purchased from Sigma Aldrich.

2.2.2 Device Fabrication

IS study: For the Metal Insulator semiconductor (MIS) architecture used for IS, FTO was used as a substrate where the dielectric layer was first spin-coated. FTOs were cleaned by ultra-sonication subsequently in deionized water, acetone and isopropanol followed by UV ozone treatment for 15 min. 30 mg/mL solution of the dielectric PMMA, PS, PVP were made in solvents anisole, toluene, tetrahydrofuran, respectively and spin-coated on the cleaned FTO substrates at 2000 rpm for 30 s to get a ~150 nm thick layer and dried at 100 ^oC for 30 min and then properly cooled down. A 10 mg/mL solution of PTB7-Th in chlorobenzene was prepared by stirring for 1 hour at 50 °C and then 1% of DIO was added. The solution was then cooled down to room temperature and was spin coated to ensure it does not hamper the underlying dielectric coating. DIO is reported for improving the thin film morphology. The semiconductor solution was then spin-coated done over the previously dielectric coated FTO substrate and antisolvent treatment with methanol was done. These were then annealed for 10 min at 70 °C. Thereafter Cu electrodes were deposited by thermal deposition.

OFET: The OFET was fabricated following the bottom gate top contact architecture. The glass substrates were cleaned by dipping the substrates in piranha solution for 1 hour. 100 nm of

Al was thermally deposited on the cleaned glass substrates to form the gate electrode of width 1mm by shadow masking on a glass substrate. 100 mg/mL solution of PVA in DI water was prepared and coated over the gate deposited substrate and dried at 100 ^{o}C for 1 hour to form 1 µm thick layer. PVA acts as the first dielectric in all three OFETs, over which a 100 nm (3000 rpm 30 s) thick second dielectric layer and 60 nm thick PTB7-Th layer was coated following the same process as was done for the MIS structure. Finally, for the top contact 5 nm of MoO_x and 60 nm of Cu were thermally deposited using shadow masking to form a channel of length (L) 40 µm and width (W) 0.8 mm. All the fabrication processes were done in ambient condition. The devices with PMMA, PS, PVP as the second and interfacial dielectric layer are termed as PMMA, PS and PVP, respectively throughout. For flexible devices instead of glass, PET substrates were used and remaining all other processes was same as the rigid device.

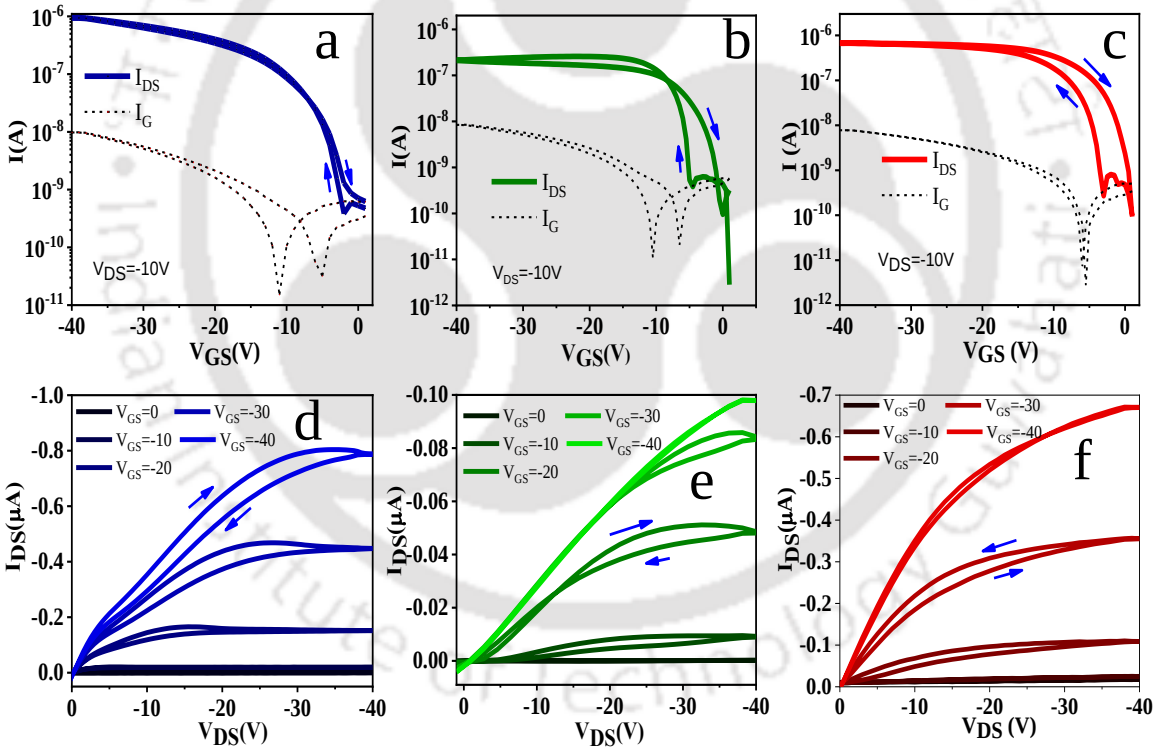


Figure 2.1: Transfer curves, output curves of PTB7-Th based OFET for dielectric combinations (a), (d) PVA/PMMA, (b), (e) PVA/PS, (c), (f) PVA/PVP.

2.2.3 Characterization

CH Instruments 760D was used for Electrochemical measurements. For PL measurements, a Horiba Fluoromax-4 spectrofluorometer was used and MicroTime 200 was

used for TRPL. DFT method using the Gaussian 03 package with the B3LYP hybrid functional and a 6-31G basis set was used for theoretical calculations. The thickness of the thin films was measured using Dektek 150 stylus profilometer. The AFM images were recorded on an Agilent 5500 AFM/SPM microscope in tapping mode to avoid tip surface interaction causing any film damage. All the transistor characterization was performed using a Keithley 4200 SCS parameter analyzer under vacuum conditions.

2.3 Results and Discussions

The output and transfer characteristic graphs of the OFETs with double dielectric PVA/PMMA (device PMMA), PVA/PS (device PS), PVA/PVP (device PVP) are shown in **Figure 2.1a-c** and **Figure 2.1d-f** respectively. Because of its high dielectric constant and good insulation properties, PVA is chosen as the first dielectric (dielectric I) layer so that a thicker layer (1 µm) can be implemented and the leakage current can be reduced. It can be observed that the leakage current is at least two order less than I_{DS}. Polymer dielectrics without any modification is known to have high leakage current.[43] However, the highly polar PVA with polar –OH side group is reported to interact with water molecules and degrade the device faster.[44]

Table 2.1: Summarized Transistor parameters extracted from transfer and output characteristics.

Dielectric	Saturation Mobility [cm^2/V-s] [a)]	Linear Mobility [cm^2/V-s] [a)]	V_{TH} [V] [a)]	SS [V/dec]	Volume Trap density (from SS) [cm^{-3} eV^{-1}] [a)]	I_{ON}/I_{OFF}
PMMA	0.095 (0.085±0.005)	0.076 (0.065±0.005)	3.7(±0.7)	0.4(±0.08)	$4.7x10^{16}$	10^4
PS	0.05 (0.045 ±0.005)	0.03 (0.025 ±0.005)	7.4(±1.5)	2.1 (±1.2)	$2.8x10^{17}$	10^4
PVP	0.12 (0.096 ±0.006)	0.08 (0.074±0.006)	2.3(±0.8)	1 (±0.1)	$1.3x10^{17}$	10^3

[a)]Highest and average data for 20 devices

All the three devices were tested and the parameters were extracted from the characteristic graphs and shown in **Table 2.1**. It can be observed that all the three devices show distinctly different characteristics, which demands a detailed analysis to understand these characteristics. The D/S interface is crucial in defining the operation of the OFET device as the

primary charge transport takes place within a few nanometers of this interface. Hysteresis in OFET is one such operational parameter that is defined by the D/S interfacial traps.[17] Hysteresis in the transfer characteristics is mainly dominated by properties of dielectric. The lower back-sweep (LBS) is attributed to trapping of mobile holes in the dielectric whereas higher back sweep (HBS) current is due to slow polarization of the dielectric.

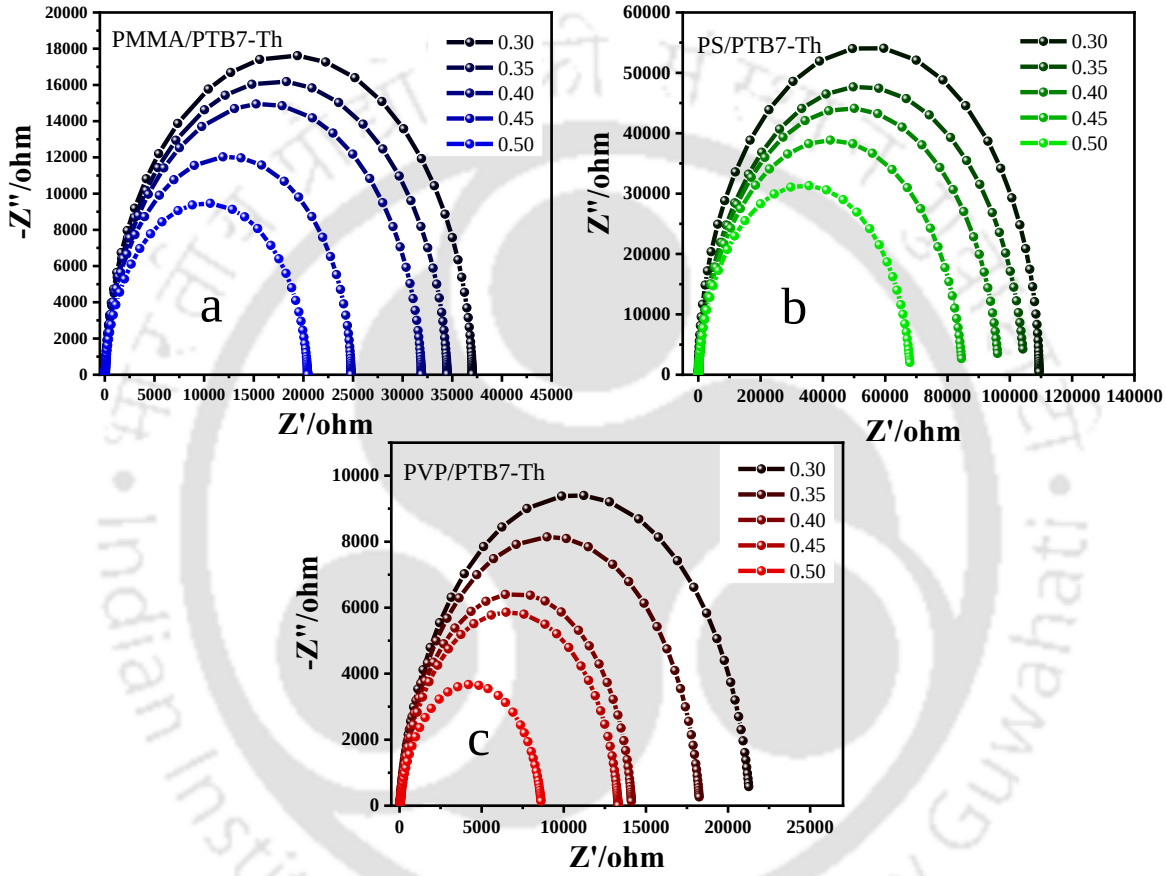


Figure 2.2: Nyquist plot obtained from IS (a) PMMA/PTB7-Th (b) PS/PTB7-Th (c) PVP/PTB7-Th.

Output characteristics hysteresis can be related to the traps hampering charge transport through the channel. In all the three devices at low gate voltage (V_{GS}) slow polarization due to bulk dielectric (PVA) is visible but device PS shows both LBS and HBS implying the trapping of holes in PS. The PS shows high hysteresis in transfer characteristics and a late saturation in the output characteristics. The output characteristic of PMMA does not saturate appropriately and a slight reduction in drain-source current (I_{DS}) with gate-source voltage (V_{GS}) after a point is observed in the forward sweep. In the case of PVP, the hysteresis in output characteristics is

negligible and well defined linear and saturation regions are obtained. The highest mobility is obtained for the PVP device despite the higher interface trap states calculated from the SS, suggesting traps are favoring charge transport. The dielectric constant is an essential parameter that decides the areal capacitance and is thus closely related to the threshold voltage. The low V_{TH} of device PVP was expected because of the high polarity of PVP.

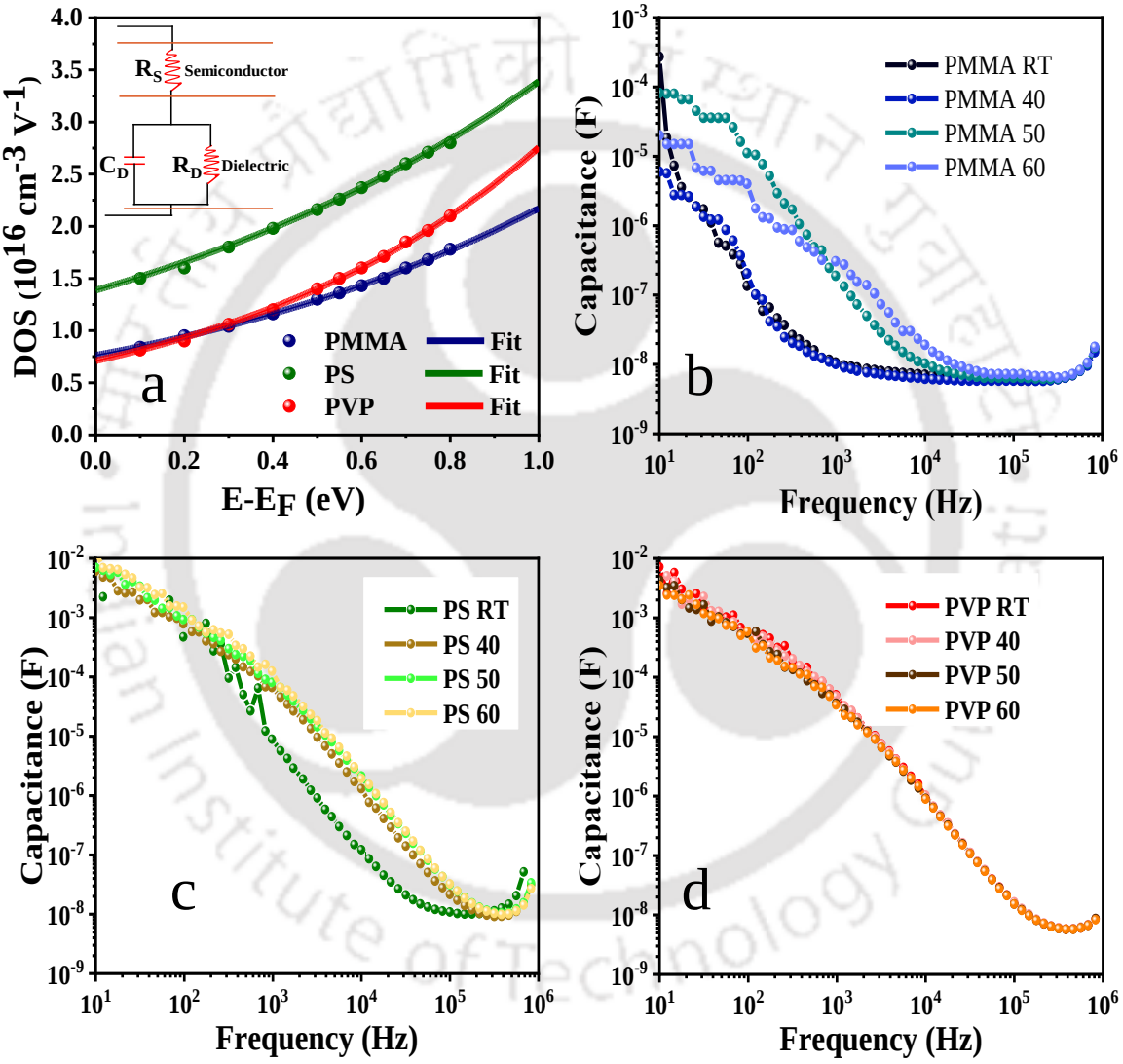


Figure 2.3: Plots deduced from IS (a) Density of trap states vs Energy level comparison for the three MIS devices, Capacitance vs Frequency response comparison at different temperatures and at an applied bias of 0.7 V for (b) PMMA (c) PS (d) PVP.

IS was carried for the MIS structure to investigate the D/S interface charge trapping and releasing processes. Capacitance (C_D) and resistances (R_D and Rs), extracted from the Nyquist

plot (**Figure 2.2**) by fitting the circuit diagram as shown in the inset image of **Figure 2.3a**, can also be utilized to investigate defects. A bias of 0.1-0.8 V was applied and the Nyquist plots were measured. From the Nyquist plot, the capacitance and resistances are extracted. The DOS is directly proportional to the capacitance, as the capacitance is a reflex of the stored charges at the traps and hence the DOS versus energy level plot was derived (**Figure 2.3a**) using **Equation 2.1**:

$$DOS = 6.24 \times 10^{18} \times C_D / (d*A) \qquad (2.1)$$

PS based MIS structure showed the maximum trap states whereas PVP showed the minimum DOS till a bias of 0.4 V. From 0.4 V to 0.9 V, there is an increase in DOS for PVP, whereas PMMA has the least DOS at all applied bias. The increase in DOS of PVP after 0.4 eV can be correlated to electron trap closer to the conduction band arising from –OH side group in PVP. where d is the combined thickness of dielectric and semiconductor, A is the area of one cell. The trap states are directly proportional to the C_D, as at a given bias, the C_D is defined by the accumulated charges at the trapping sites.[45-47] CF plots shown in **Figure 2.3b-d** are deduced from the IS. At a particular DC bias (0.7 V), as the AC frequency sweep of 10 Hz to 10^6 Hz is applied, the capacitance obtained is related to the depth of traps. When the AC signal time period is slower than the trapping and detrapping time of charges, then the capacitance associated with traps increases. Hence, the capacitance increases by few orders of magnitude at lower frequencies. The particular frequency where the capacitance starts to increase rapidly is the transition frequency (f_{ci}). This increase in capacitance at lower frequencies corresponds to the charge accumulation caused by localized traps or the deep traps, whereas the higher frequency response is due to an accumulation of delocalized charges or accumulation at shallow traps and these charges may instead favor the charge transport. In the case of PVP, the f_{Ci} is 10^5 Hz, and a trivial variation with temperature confirms the presence of delocalized charges and the absence of deep traps. For PS, the capacitance increase starts from 10^5 Hz and with increase in temperature a right shift in f_{Ci} is observed. For PMMA, f_{Ci} shifts towards the higher frequency with an increase in temperature and at room temperature f_{Ci} is 10^3 Hz suggesting more localized traps or deep traps at room temperature and with an increase in temperature, the traps are released and delocalized charges get accumulated. For PMMA, the capacitance in the lower frequency range (10-100 Hz) is almost two orders of magnitude lower than that of PS, suggesting comparatively lesser traps. PVP is having almost the same density of traps, but the traps are

shallow in nature and are assisting in transport, whereas PS has shallow and deep traps that are hampering the charge transport. This is consistent with the DOS study and even justifies the mobility order and interface traps calculated from SS for the OFETs (**Table 2.1**).

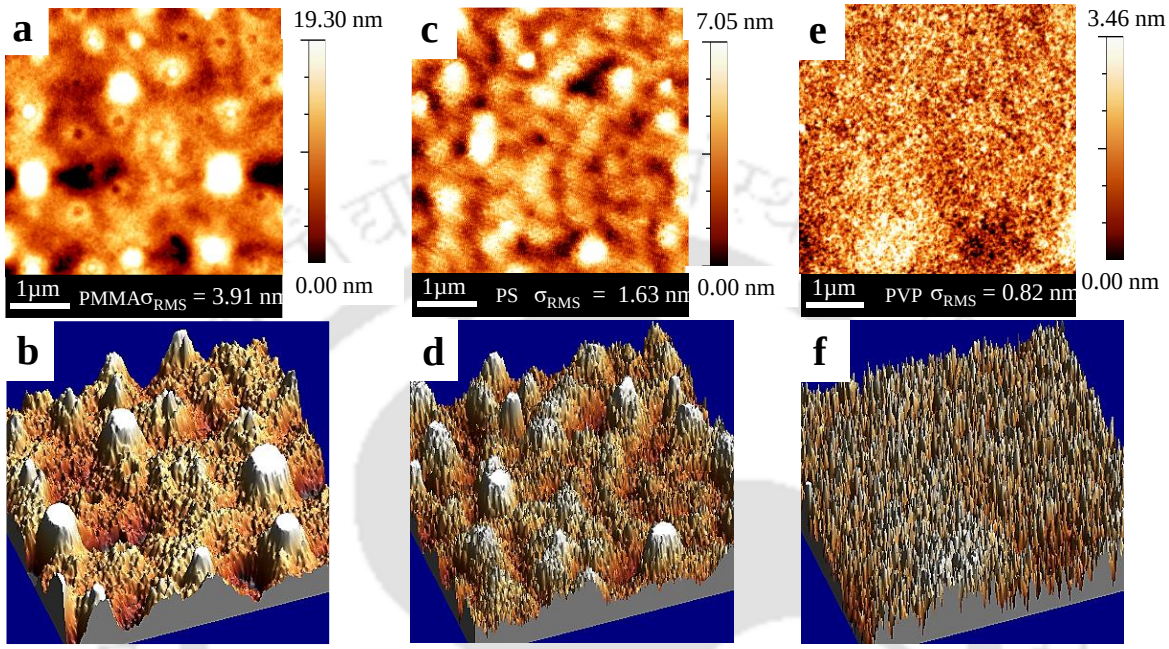


Figure 2.4: 5X5 µm^2 2D and3D AFM images of PTB7-Th coated on dual dielectric system (a) and (b) PVA/PMMA (c) and (d) PVA/PS (e) and (f) PVA/PVP.

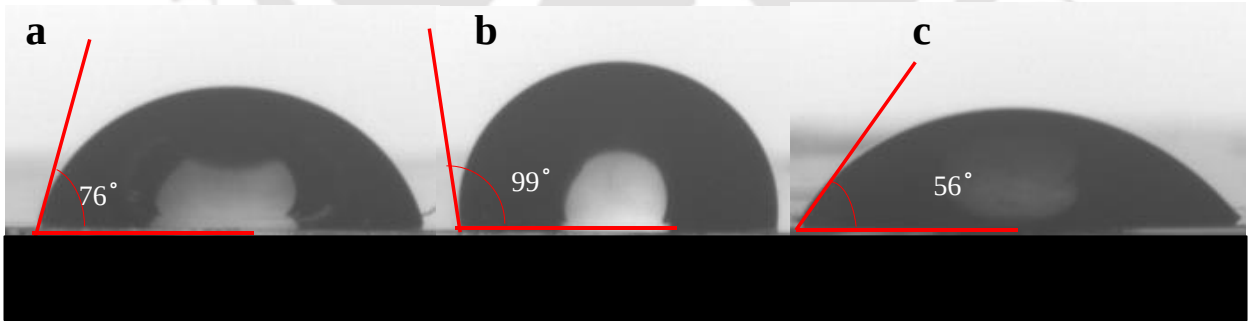


Figure 2.5: Contact angle measurement for (a) PMMA (b) PS and (c) PVP.

The morphology of PTB7-Th coated on dual dielectric thin film fabricated on a glass substrate is investigated by AFM as shown in **Figure 2.4**. The morphology of the semiconductor coated on dielectric is a critical factor that needs to be analyzed to understand the interfacial defects as these surface irregularities act as physical traps and affects the charge transport. The

rms roughness of PTB7-Th coated on PVA/PMMA (**Figure 2.4a, b**) is 3.91 nm which is highest among the three and that for PVA/PS is 1.63 nm (**Figure 2.4c, d**). PTB7-Th coated on dual dielectric PVA/PVP (**Figure 2.4e, f**), showed least rms roughness of 0.82 nm and a homogenous, smooth morphology with few defects is observed for PTB7-Th coated on hydrophilic –OH group-containing PVP. PTB7-Th coated on more hydrophobic PMMA and PS showed similar surface morphologies having non uniform hilly aggregates (**Figure 2.4b, d**) because of which the surface roughness increased where as in PVP the morphology is uniform. A defect-free interface is beneficial for the accumulation and transport of charge carriers. These physical defects act as deep traps that hinder the charge transport, which justifies the low f_{ci} obtained from CF analysis. The contact angle measurements with deionized water were recorded to confirm the surface hydrophobicity of PMMA, PS and PVP (**Figure 2.5**). PVP forms the most hydrophilic surface followed by PMMA and PS.

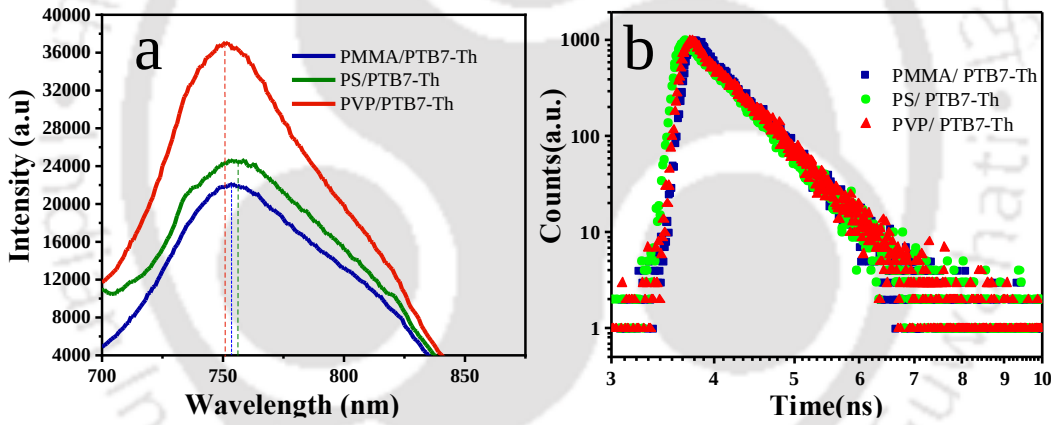


Figure 2.6: (a) Time Resolved Photoluminescence intensity decay spectra and (b) Photoluminescence Spectra of PTB7-Th coated on PMMA (Blue), PS (Green), PVP (Red).

To better understand the role of traps, the PL spectra and TRPL decay spectra comparison are shown in **Figure 2.6a, b**, respectively. Both the PL and TRPL spectra show minor changes in the three devices, which is quite obvious as the semiconductor is same in all three and the only change is in the interface. The highest PL intensity is obtained for PVP followed by PS and the least is for PMMA. But for PS, maximum red shift is observed which suggest that there is a contribution of traps in the recombination process. From TRPL decay spectra, the radiative decay lifetime (τ_1) and the trap assisted recombination lifetime (τ_2) are

extracted by biexponential fitting and the average carrier lifetime (τ_{av}) is calculated. The τ_{av} follows the same trend as the PL intensity for all the three cases. PVP having the slowest τ_{av} confirms that the traps are not affecting the carrier recombination for PVP, whereas in the case of PS, τ_{av} is lower than PMMA but surprisingly τ_2 is faster indicating faster trap assisted recombination in PS. This justifies the red shift observed in PS indicating trap assisted recombination, and also justifies low value of τ_2 in the TRPL data. The radiative decay lifetime (τ_1) is 0.45 ns for PMMA and 0.47 ns for PS, but the trap assisted recombination lifetime (τ_2) is slower in PMMA than in PS. This justifies the red shift in PS as observed in PL spectra. The PVP showed slowest radiative and trap assisted recombination and hence had the highest average carrier lifetime and highest PL intensity as well. This suggests that the carrier recombination at the trapping sites is less in PVP and hence the traps are not hampering the charge transport.

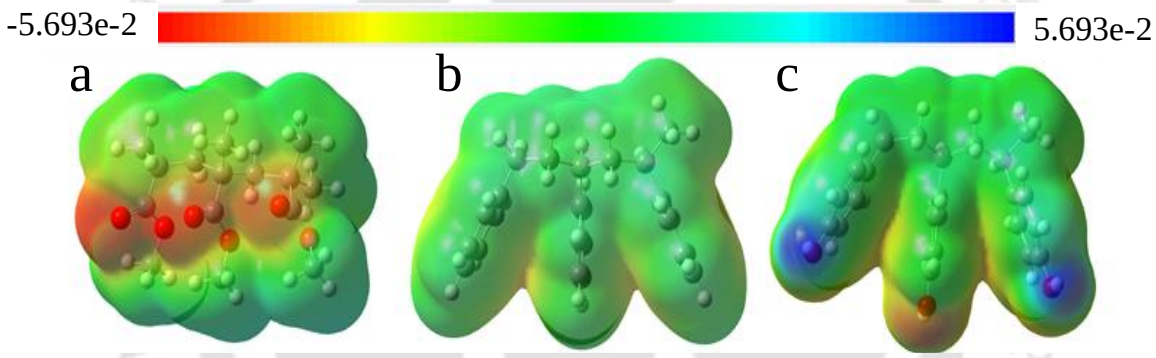


Figure 2.7: DFT of (a) PMMA (b) PS and (c) PVP.

The electron density distribution is obtained from DFT simulation (**Figure 2.7**). PMMA exhibits a strong negative charge density distribution in the electrostatic potential (ESP) profiles that may attract the positive charges from the bulk to the interface. As a result, these positive charges screen the gate voltage as can be seen from the output characteristics of PMMA (**Figure 2.1b**) and as the drain-source voltage (V_{DS}) increases further, the current starts reducing while in reverse sweep the charges follow a different path formed away from the interface. This explains the complex hysteresis in the output characteristics of PMMA. In PS, no such behavior is observed due to its neutral charge density distribution. PVP reveals a bipolar charge distribution in the ESP profile indicating more charge accumulation at the interface and negligible hysteresis in output characteristics.

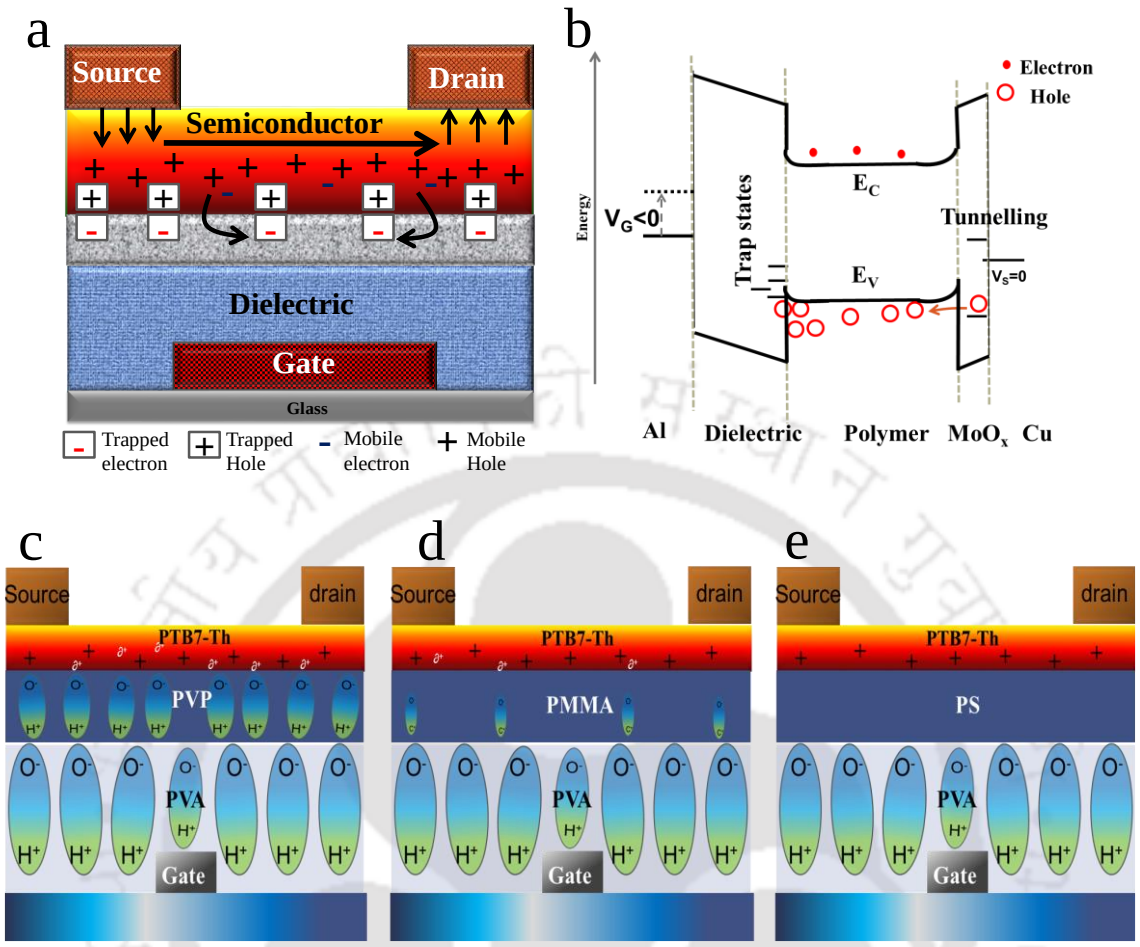


Figure 2.8: (a) Schematic representation of device, (b) energy band diagram to explain the mechanism of charge trapping and transport, schematic illustration of oriented side groups in the polar dielectric layer (c) fully oriented −OH groups due to applied gate voltage in highly polar dielectric PVA/PVP in device PVP (d) oriented −CH and -OH groups due to applied gate voltage in highly polar PVA and slightly polar PMMA in device PMMA, and (e) oriented -OH groups due to applied gate voltage in highly polar PVA only in device PS.

Finally, to merge all the results of the IS based DOS study, OFET characteristics and other film characterizations, a schematic model as shown in **Figure 2.8** has been proposed. The proposed schematic illustration explains the correlation of DOS with the different characteristics of the three devices. It explains the role of interfacial dielectric in generating distinctly different transfer and output characteristics of the three devices. **Figure 2.8a** shows the position and type of traps in the device architecture, whereas **Figure 2.8b** explains traps position and charge injection using energy band diagram. The surface states or the interface trap arising from the hydroxyl group of PVP are acceptor-like and it traps the mobile electrons in the P-type semiconductor, which in turn provide hoping sites for holes. From the DOS analysis (**Figure**

2.3a), it can be observed that there is DOS broadening for PVP which is consistent with reported results.[48]

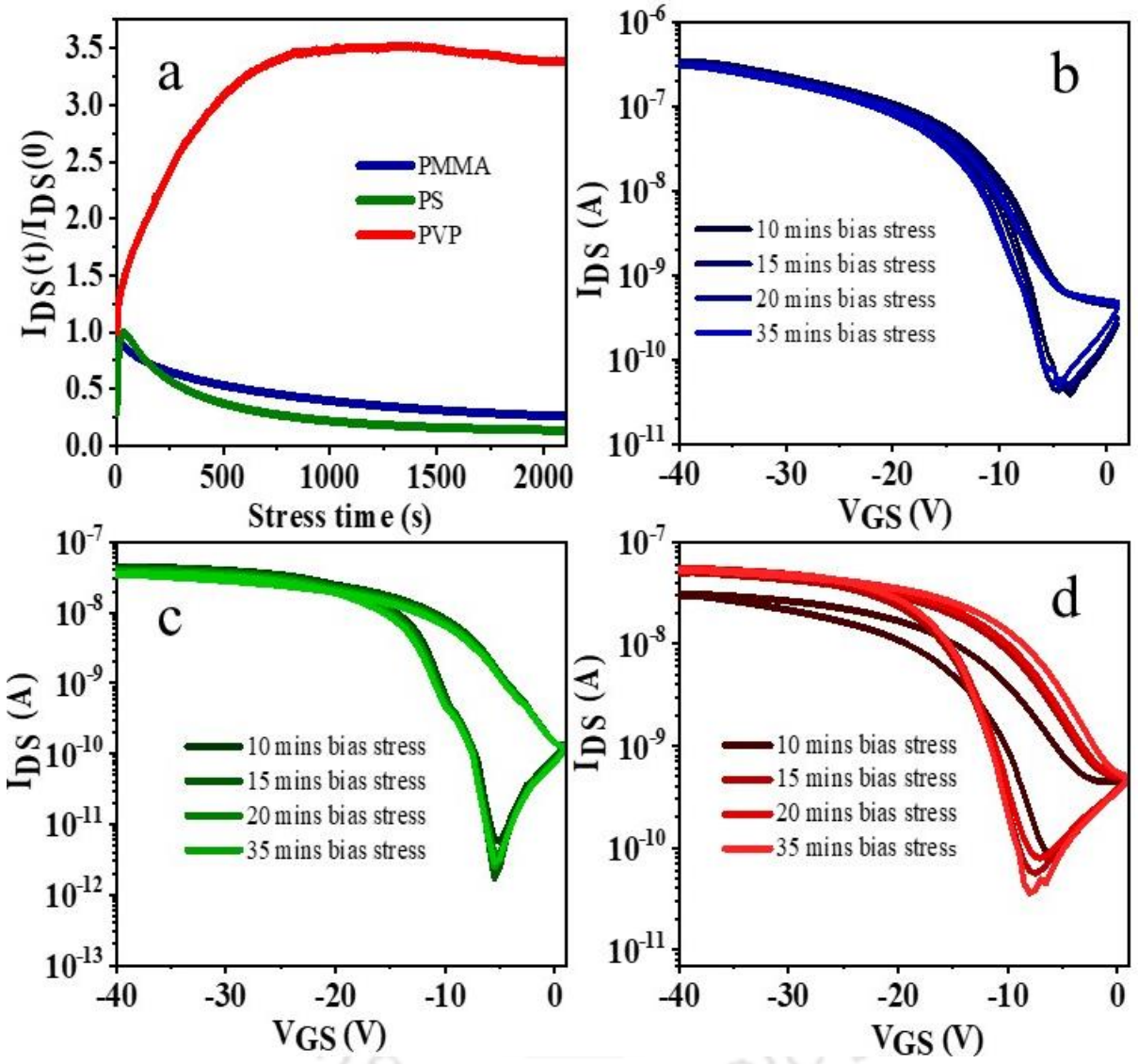


Figure 2.9: (a) The normalised I_{DS} under bias stress of V_{DS}=V_{GS}= -40 V, successive transfer characteristics runs taken after bias stress at different time intervals for device (b) PMMA, (c) PS, (d) PVP.

These hopping sites act as shallow traps and hence the off current is higher, causing reduction in I_{on}/I_{off}. The increased dipole moment at the PVP/PTB7-Th interface induces additional positive charges (**Figure 2.8c**). As a result, the side group of PVP assists the hole transport process, whereas in case of PMMA, there is very little polarity (**Figure 2.8d**) and in the case of PS (**Figure 2.8e**), there are no polar groups to trap the electrons. In device PMMA and

PS, the transport of holes gets hampered because of the non-uniformity of the film that can be seen from the AFM which causes the large hysteresis output characteristic of these devices. But in temperature-dependent CF, the maximum change in response with the temperature was observed for PMMA, which may be because of the physical traps arising from higher roughness of the film as confirmed from the AFM study. The maximum hole trap in the interface can be seen in T-DOS of PS which is in agreement with the low mobility of device PS.

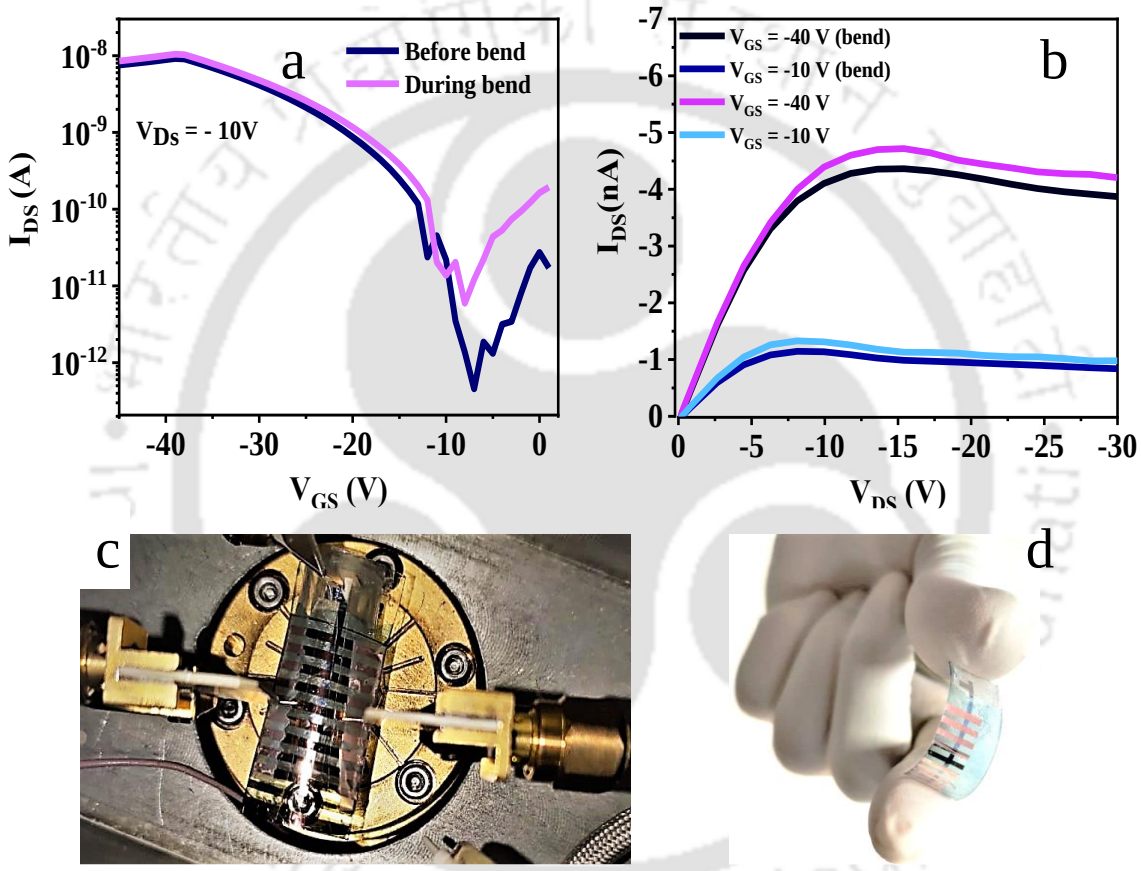


Figure 2.10: (a) Transfer characteristics and (b) output characteristic of the flexible device showing the comparison between flat device and the bend device under 2.5% strain. (c) photograph of the measurement setup of the bent array of OFETs (d) photograph of the Flexible OFET array.

To study the stability, all the three devices were subjected to bias stress (**Figure 2.9**). The PMMA device showed usual decay in current whereas in case of PS device, the current increased first and the decay started which may be because of charge trapping in the dielectric whereas in the case of PVP, slow polarization dominated.[49, 50] All the three devices showed stability on successive operation and no significant change in V_{TH} was observed. For PVP the current

increased on successive operation which also regained to original after the bias stress. The bias stress was applied after exposing the devices to ambient atmosphere and PMMA showed almost similar results as before, even after bias stress and few successive operations. Therefore, the PMMA device is fabricated on a PET flexible substrate to validate the applicability of the proposed device structure for flexible devices. This was done to manifest that the implemented device architecture and the obtained results are applicable irrespective of the substrate used. **Figure 2.10** shows the flexible device fabricated on PET substrate. Because of the higher roughness of the substrate highest mobility obtained for the flexible device was $2x10^{-2}$ cm^2/V-s. A bending test was performed to check the mechanical stability of the device. Even after subjecting the device to bending for 1hour, the device retained almost the same characteristics, except for a small OFF current increase. This reduction in I_{ON}/I_{OFF} may be the effect of device degradation by trapping of atmospheric oxygen and moisture during the bending process as the bending was performed in ambient conditions, and then the measurements were done under vacuum. The data for 100 bending cycles is shown in **Table 2.2**. This type of behavior after ambient air exposure is reported in even rigid substrates.[51] The device was repeatedly bent at a radius of curvature (r) of 4 mm and the thickness of the substrate (D) is 0.2 mm. 2.5% strain was calculated using the formula: strain (σ)= D/2r.

Table 2.2: Stability data for the Flexible PMMA based OFET.

No. of bending cycles	Mobility (cm^2/V-s)	Threshold Voltage (V)
1^{st}	$2.01x10^{-2}$	7
After 10	1.20×10^{-2}	7.5
After 100	8×10^{-3}	9

2.4 Conclusions

In this work, IS is demonstrated as a potential method for analyzing T-DOS in MIS architecture. The study has been exclusively used to understand and explain different characteristics of the fabricated OFET devices. All the transistor parameters such as threshold voltage, mobility, sub-threshold swing, hysteresis, trap-density from sub-threshold swing, I_{ON}/I_{OFF} are calculated and the effect of T-DOS is used as a tool to understand the variation in these parameters by changing the dielectric interface with respect to the semiconducting polymer. IS measurement at different temperatures is also done and capacitance-frequency plots

are extracted to understand the effect of temperature on the interfacial traps. Comparatively, higher mobility and lower hysteresis have been observed with the lowering of T-DOS. Further characterizations like AFM, TRPL, PL were also carried out and are found to be consistent with the DOS analysis. These results suggest that IS can be used as a convenient T-DOS analysis tool for understanding or predicting the OFET performance. OFETs developed till date lack sufficient stability and lack reproducibility of electrical parameters. Therefore, for a better understanding of the reason of these issues, the complex organic-organic D/S interface and mutual interaction between the dielectric and semiconductor material need detailed analysis. This understanding will also significantly help in developing new semiconductors and dielectric materials for OFET.

References

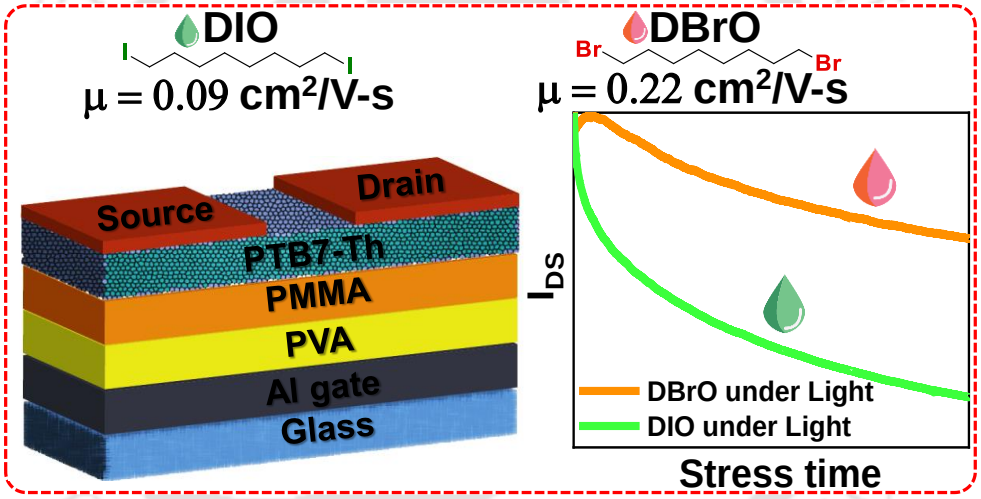
1. H. E. Katz, L. Torsi and A. Dodabalapur, *Chem. Mater.*, 1995, **7**, 2235-2237.
2. M. Lefenfeld, G. Blanchet and J. A. Rogers, *Adv. Mater.*, 2003, **15**, 1188-1191.
3. W. Shi, Y. Guo and Y. Liu, *Adv. Mater.*, 2020, **32**, 1901493.
4. V. Raghuwanshi, P. Saxena, S. Rahi, A. K. Mahato, I. Varun and S. P. Tiwari, *ACS Appl. Electron. Mater.*, 2020, **2**, 3373-3379.
5. X. Ren, K. Pei, B. Peng, Z. Zhang, Z. Wang, X. Wang and P. K. L. Chan, *Adv. Mater.*, 2016, **28**, 4832-4838.
6. A. Tsumura, H. Koezuka and T. Ando, *Appl. Phys. Lett.*, 1986, **49**, 1210-1212.
7. J. Mei, Y. Diao, A. L. Appleton, L. Fang and Z. Bao, *J. Am. Chem. Soc.*, 2013, **135**, 6724-6746.
8. R. Garai, M. Adil Afroz, R. K. Gupta, A. Choudhury and P. K. Iyer, *ACS Omega*, 2020, **5**, 2747-2754.
9. A. Kalita, N. V. V. Subbarao and P. K. Iyer, *J. Phys. Chem. C*, 2015, **119**, 12772-12779.
10. K. Kurlekar, A. Anjali, S. Sonalin, P. M. Imran and S. Nagarajan, *ACS Appl. Electron. Mater.*, 2020, **2**, 3402-3408.
11. S. Lee, B. Koo, J. Shin, E. Lee, H. Park and H. Kim, *Appl. Phys. Lett.*, 2006, **88**, 162109.
12. Q. Liu, S. Kumagai, S. Manzhos, Y. Chen, I. Angunawela, M. M. Nahid, K. Feron, S. E. Bottle, J. Bell, H. Ade, J. Takeya and P. Sonar, *Adv. Funct. Mater.*, 2020, **30**, 2000489.
13. Q. Liu, Y. Wang, A. Kohara, H. Matsumoto, S. Manzhos, K. Feron, S. E. Bottle, J. Bell, T. Michinobu and P. Sonar, *Adv. Funct. Mater.*, 2020, **30**, 1907452.
14. A. R. V. Benvenho, W. S. Machado, I. Cruz-Cruz and I. A. Hümmelgen, *J. Appl. Phys.*, 2013, **113**, 214509.
15. J. Kim, J. Jang, K. Kim, H. Kim, S. H. Kim and C. E. Park, *Adv. Mater.*, 2014, **26**, 7241-7246.
16. C. J. Bettinger and Z. Bao, *Adv. Mater.*, 2010, **22**, 651-655.
17. Y. Wang, X. Huang, T. Li, L. Li, X. Guo and P. Jiang, *Chem. Mater.*, 2019, **31**, 2212-2240.
18. S. Yuvaraja, A. Nawaz, Q. Liu, D. Dubal, S. G. Surya, K. N. Salama and P. Sonar, *Chem. Soc. Rev.*, 2020, **49**, 3423-3460.

19. A. Dey, A. Singh, D. Dutta, S. S. Ghosh and P. K. Iyer, *J. Mater. Chem. A*, 2019, **7**, 18330-18337.
20. N. V. V. Subbarao, M. Gedda, P. K. Iyer and D. K. Goswami, *ACS Appl. Mater. Interfaces*, 2015, **7**, 1915-1924.
21. A. Dey, A. Singh, D. Das and P. K. Iyer, *ACS Omega*, 2017, **2**, 1241-1248.
22. W. Lee, D. Kim, J. Rivnay, N. Matsuhisa, T. Lonjaret, T. Yokota, H. Yawo, M. Sekino, G. G. Malliaras and T. Someya, *Adv. Mater.*, 2016, **28**, 9722-9728.
23. H. Sirringhaus, M. Bird and N. Zhao, *Adv. Mater.*, 2010, **22**, 3893-3898.
24. G. Wang, N. Persson, P.-H. Chu, N. Kleinhenz, B. Fu, M. Chang, N. Deb, Y. Mao, H. Wang, M. A. Grover and E. Reichmanis, *ACS Nano*, 2015, **9**, 8220-8230.
25. A. Dey, A. Singh, D. Das and P. K. Iyer, *Phys. Chem. Chem. Phys.*, 2016, **18**, 32602-32609.
26. C. Wang, X. Zhang, H. Dong, X. Chen and W. Hu, *Adv. Energy Mater.*, 2020, **10**, 2000955.
27. A. Karki, G.-J. A. H. Wetzelaer, G. N. M. Reddy, V. Nádaždy, M. Seifrid, F. Schauer, G. C. Bazan, B. F. Chmelka, P. W. M. Blom and T.-Q. Nguyen, *Adv. Funct. Mater.*, 2019, **29**, 1901109.
28. S. Anand, K. P. Goetz, Z. A. Lamport, A. M. Zeidell and O. D. Jurchescu, *Appl. Phys. Lett.*, 2019, **115**, 073301.
29. W. L. Kalb, S. Haas, C. Krellner, T. Mathis and B. Batlogg, *Phys. Rev. B*, 2010, **81**, 155315.
30. H. F. Iqbal, E. K. Holland, J. E. Anthony and O. D. Jurchescu, *Mater. Horiz.*, 2020, **7**, 2390-2398.
31. S. Hunter, A. D. Mottram and T. D. Anthopoulos, *J. Appl. Phys.*, 2016, **120**, 025502.
32. E. M. Muller and J. A. Marohn, *Adv. Mater.*, 2005, **17**, 1410-1414.
33. E. Gomar-Nadal, B. R. Conrad, W. G. Cullen and E. D. Willams, *J. Phys. Chem. C*, 2008, **112**, 5646-5650.
34. M. Jaquith, E. M. Muller and J. A. Marohn, *J. Phys. Chem. B*, 2007, **111**, 7711-7714.
35. K. Puntambekar, J. Dong, G. Haugstad and C. D. Frisbie, *Adv. Funct. Mater.*, 2006, **16**, 879-884.
36. R. H. Bube, *J. Appl. Phys.*, 1962, **33**, 1733-1737.

37. Y. Shao, Z. Xiao, C. Bi, Y. Yuan and J. Huang, *Nat. Commun.*, 2014, **5**, 5784.
38. Z. Ni, C. Bao, Y. Liu, Q. Jiang, W.-Q. Wu, S. Chen, X. Dai, B. Chen, B. Hartweg, Z. Yu, Z. Holman and J. Huang, *Science*, 2020, **367**, 1352.
39. G. Horowitz, R. Hajlaoui and P. Delannoy, *J. phys., III*, 1995, **5**, 355-371.
40. W. L. Kalb and B. Batlogg, *Phys. Rev. B*, 2010, **81**, 035327.
41. R. Garai, M. A. Afroz, R. K. Gupta and P. K. Iyer, *Adv. Sustain. Syst.*, 2020, **4**, 2000078.
42. R. K. Gupta, R. Garai, M. A. Afroz and P. K. Iyer, *J. Mater. Chem. C*, 2020, **8**, 8191-8198.
43. Y.-Y. Noh and H. Sirringhaus, *Org. Electron.*, 2009, **10**, 174-180.
44. C. Ucurum, H. Goebel, F. A. Yildirim, W. Bauhofer and W. Krautschneider, *J. Appl. Phys.*, 2008, **104**, 084501.
45. D. K. Hwang, M. S. Oh, J. M. Hwang, J. H. Kim and S. Im, *Appl. Phys. Lett.*, 2008, **92**, 013304.
46. L. Guan, N. Jiao and Y. Guo, *J. Phys. Chem. C*, 2019, **123**, 14223-14228.
47. B. C. O'Regan, S. Scully, A. C. Mayer, E. Palomares and J. Durrant, *J. Phys. Chem. B*, 2005, **109**, 4616-4623.
48. T. Richards, M. Bird and H. Sirringhaus, *J. Chem. Phys.*, 2008, **128**, 234905.
49. J. Martins, P. Bahubalindruni, A. Rovisco, A. Kiazadeh, R. Martins, E. Fortunato and P. Barquinha, *Materials*, 2017, **10**, 680.
50. S. Singh and Y. N. Mohapatra, *Org. Electron.*, 2017, **51**, 128-136.
51. D. K. Hwang, C. Fuentes-Hernandez, J. Kim, W. J. Potscavage Jr., S.-J. Kim and B. Kippelen, *Adv. Mater.*, 2011, **23**, 1293-1298.

Chapter 3

Tuning Polymer Semiconductor Morphology through Additive Engineering for Stable Phototransistor



Manuscript: Anwesha Choudhury, Ritesh Kant Gupta, Rabindranath Garai, Parameswar Krishnan Iyer, "Tuning Polymer Semiconductor Morphology through Additive Engineering for a Stable Phototransistor". *ACS Appl. Electron. Mater.* **2021,** *3* (12), 5393-5401, DOI: 10.1021/acsaelm.1c00873.

[This page was intentionally left blank]

Abstract

The application of PTB7-Th polymer as an efficient semiconductor material in photo-transistor (PT) has been demonstrated, with a strategy to improve the hole transport and increase stability under dark as well as illumination conditions. The results have been established using two solvent additives, namely 1,8-diiodooctane (DIO) and 1,8-dibromooctane (DBrO) which have the ability to modulate the polymer morphology. These additives also improve the charge transport properties and helps in achieving higher mobility in organic field effect transistor (OFET). The DIO and DBrO-modified devices show an increase in mobility (0.09 and 0.22 cm^2/V-s, respectively) with respect to the pristine device (without any additive). Further, the device stability in dark as well as under illumination improves drastically for DBrO-modified device whereas photo-degradation of DIO-modified device is observed. The photo-physical studies, AFM, FESEM, XRD and electrical investigations were carried out to understand the effect of solvent additive in lowering the contact resistance, suppressing traps and improving morphology. With the optimized concentration of DBrO as solvent additive, a PTB7-Th based PT is implemented and a responsivity of 688 A/W is obtained.

3.1 Overview

A high performing, stable and robust organic field effect transistor (OFET) is an essential component for various commercial electronic applications. However, achieving high-performance OFETs faces major roadblocks like low mobility and stability which can be attributed to the interfacial and bulk traps. To overcome these hurdles, various approaches are being attempted including development of various organic semiconductor materials, source-drain contact modification, doping of the active layer, and adopting various device engineering.[1-7] The mobility in polymer-based FETs is mainly challenged by the 1) structural disorder, 2) interfacial traps, and 3) traps induced by environmental conditions like temperature, light, moisture, oxygen etc. However, polymer backbone alignment is a major deciding factor for achieving higher FET mobility.[8] The alignment of the polymer is preferred parallel to the substrate for better charge transport from source to drain in FET.[9] The alignment of the polymer backbone can be modified by various techniques like blade coating, nano grooving, annealing, additives engineering, etc.[8, 10] The incorporation of molecular additives is known to improve the thin film morphology and reduce traps.[11] Despite the utilization of solvent additives to modulate the device performance in photovoltaic and thermoelectric device is very common, its significance in polymer FETs is less explored. Solvent additives like 1,8-diiodooctane (DIO) and chloronaphthalene are previously used as morphology modifiers for achieving enhanced mobility.[12-17] By introducing solvent additives of varying volatility, the alignment of the polymer chains is modulated and the charge transport property is also regulated.[18-20] Less volatile solvent additives are reported to help in controlling thin film morphology in order to achieve better charge transport, nevertheless residuals of these solvents hamper the stability of the device. Even DIO is reported to form photo-acid in presence of light, hence, any of its residuals degrades the device performance further.[21] Therefore, the investigation for proper solvent additive is required to attain improved active layer morphology for enhanced device efficiency and stability. One largely adopted method for residual additive solvent removal is by treating the film with an anti-solvent.[22] This method can produce similar device results as attained by high vacuum drying or high-temperature annealing process.

Polymer based FET device can also be utilized as photo-transistor (PT), which is an indispensable part for digital camera, satellite, wearable and biomedical electronics. For this

application, the active layer materials should be highly stable under illumination.[23, 24] Generally, materials displaying high absorption coefficient are utilized as active materials for PT application. Various photo-active inorganic[25] and organic small molecules[26-28] have been explored rigorously for PTs, yet the use of polymers is minimal.[29] PTs based on polymer semiconductors possess advantages like low cost, low-temperature solution processing and easy implementation of flexible devices.[30] PTB7-Th is a good photoactive polymer material,[31-33] yet despite having considerable mobility and high absorption coefficient, it is not yet explored for active material of a PT.

Herein, the effect of solvent additive in improving the charge transport of holes in a PTB7-Th based FET device has been studied. Also, for the first time, PTB7-Th based photo-active material has been demonstrated in a PT device with increased stability under dark as well as illumination conditions. DIO and (1,8-dibromooctane) DBrO have been used as solvent additives in the semiconductor layer of the FET device and their comparison has also been done without any solvent additive in the semiconductor layer. Both DIO and DBrO modulate the charge transport in transistor, however the highest mobility (0.22 cm^2/V-s) and stability is attained by using DBrO as the additive. Therefore, DBrO is reported as a new and efficient solvent additive for p-type PT with the aim of improving the charge transport properties and hence enhancing the stability of PT as well. It has been observed that DBrO as a solvent additive not only improves the thin film morphology but also suppresses the charge carrier trapping and enhances the stability of the device in dark and under illumination. Electrical characterization of the device is carried out for different concentrations of solvent additives. Atomic force microscopy (AFM) and field emission scanning electron microscopy (FESEM) are employed to study the morphological variations achieved by the solvent additives. X-ray diffraction (XRD) is used to understand how the solvent additives change the orientation, crystallinity of the films and alignment of the chains. The absorption and emission are analyzed by studying the UV-Visible and photoluminescence (PL) spectra, while Urbach energy is calculated from UV-Vis spectra to understand the degree of disorder in the semiconductor thin films.

3.2 Experimental Section

3.2.1 Materials

PTB7-Th was thermally synthesized according to the previous literature.[31] Poly(methyl methacrylate) (average Mw ~996 kDa), Polystyrene (average Mw ~350kDa), Poly(4-vinylphenol) (average Mw ~25 kDa), Molybdenum(VI) oxide, Aluminium (Al) and Copper (Cu) wire were purchased from Sigma Aldrich and PVA (average Mw ~115 kDa) from Loba Chemicals and used without further purification.

3.2.2 Device Fabrication

The OFET was fabricated following the Bottom gate top contact architecture. The glass substrates were cleaned by dipping the substrates in piranha solution for 1 hour. 100 nm of Al was thermally deposited on the cleaned glass substrates to form the gate electrode of width 1mm by shadow masking on a glass substrate. 100 mg/mL solution of PVA in DI water was prepared and spin coated with 1000 rpm for 30 s on the gate deposited substrate and dried at 100 ºC for 1 hour to form 1 µm thick layer. PVA acts as the first dielectric in all three OFETs, over which a 100 nm (3000 rpm 30 s) thick second dielectric layer (PMMA) is coated and dried at 100 ºC for 1 hour and 60 nm thick polymer semiconductor layer was spin coated. Finally, for the top contact 5 nm of MoO_x and 60 nm of Cu were thermally deposited using shadow masking to form a channel of length (L) 40 µm and width (W) 0.8 mm. All the fabrication processes were done in ambient condition. The device architecture is depicted in **Figure 3.1 a**.

For the semiconductor, a solution of 10 mg/ml of PTB7-Th in chlorobenzene was prepared by continuously stirring for 1 hour at 50 ºC. After 1 hour of stirring the solvent additive (DIO and DBrO) was added and kept on stirring for 10 min more. The devices were optimized for different concentrations (0% or control device, 0.5% v/v, 1% v/v, 1.5% v/v, 2% v/v) of the solvent additives. Then the solution was coated by following a 2 step spin coating process. In first step, PTB7-Th was dynamically spin coated at 2500 rpm for 45 s, and in the second step, methanol was used for antisolvent washing at 4000 rpm for 40 s. Finally, the substrates were dried at 70 ºC for 10 min to form a film of ~ 60 nm thickness.

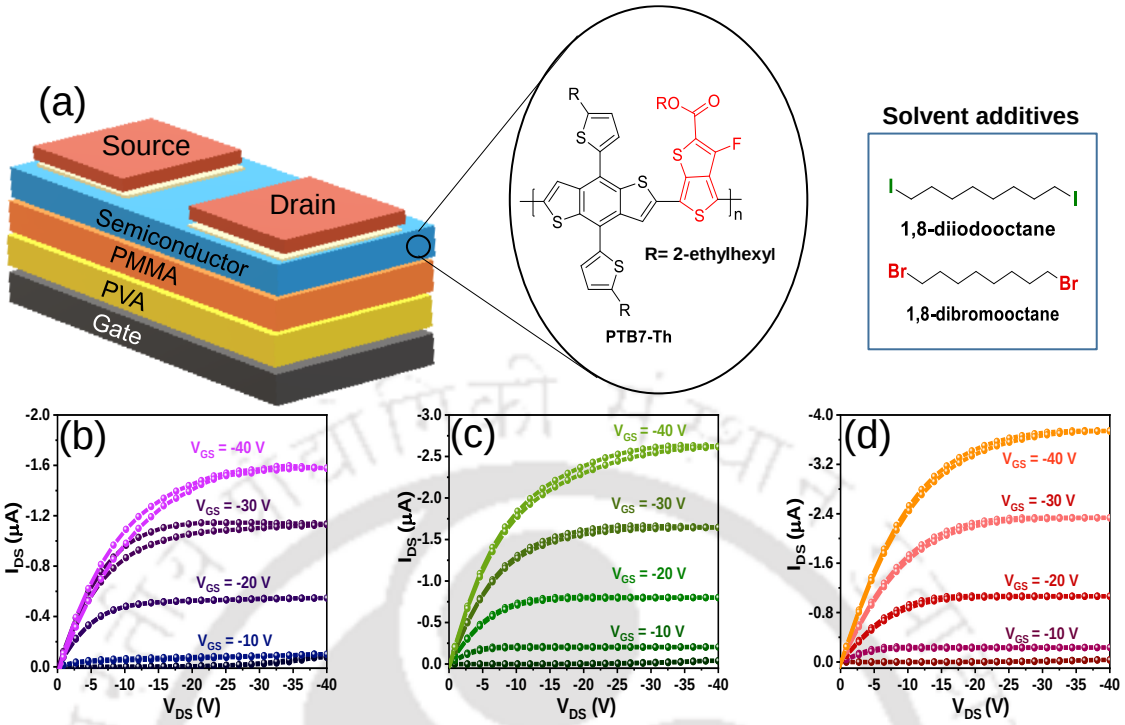


Figure 3.1: (a) Device architecture, molecular structure of PTB7-Th and solvent additives (DIO and DBrO), output curves of PTB7-Th based OFET with (b) no solvent additive, (c) DIO as solvent additive, and (d) DBRO as solvent additive.

3.2.3 Characterization

CH Instruments 760D was used for Electrochemical measurements. For PL measurements, a Horiba Fluoromax-4 spectrofluorometer was used and MicroTime 200 was used for TRPL. DFT method using the Gaussian 03 package with the B3LYP hybrid functional and a 6-31G basis set was used for theoretical calculations. The thickness of the thin films was measured using Dektek 150 stylus profiler. The AFM images were recorded on an Agilent 5500 AFM/SPM microscope in tapping mode to avoid tip surface interaction causing any film damage. All the transistor characterization was performed by using a Keithley 4200 SCS parameter analyser under vacuum conditions. For UV-VIS, a Shimadzu UV 2600 UV-VIS spectrophotometer and for XRD a Rigaku X-Ray diffractometer was used.

3.3 Results and Discussions

Bottom-gate-top-contact OFET devices were fabricated using PTB7-Th polymer as the semiconductor active layer. Three variants of devices were fabricated based on the solvent used: (i) the control device in which chlorobenzene (CB) is used as processing solvent without

any additive, (ii) DIO-modified device in which varying concentrations of DIO is used along with CB as processing solvent, and (iii) DBrO-modified device in which varying concentrations of DBrO is used along with CB as processing solvent. The device architecture of the OFET, materials used as semiconductor layer and solvent additives are presented in **Figure 3.1 a.**

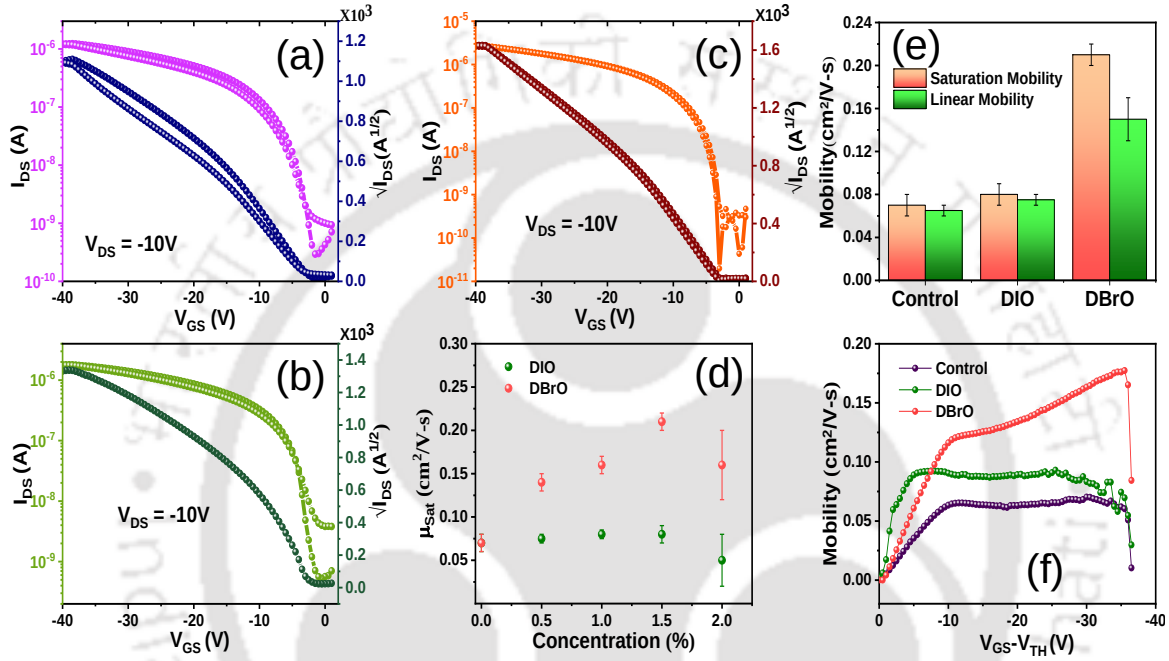


Figure 3.2. Transfer curves of PTB7-Th based OFET with (a) no solvent additive (control), (b) DIO as solvent additive, and (c) DBrO as solvent additive, (d) error bar diagram showing the comparison of saturation mobility of the OFETs for different concentration of DIO and DBrO devices, (e) comparison of linear and saturation mobility of control, DIO, DBrO modified devices, and (f) linear mobility as a function of V_{GS}-V_{TH}.

Table 3.1: Summarized OFET parameters.

Device	Saturation Mobility (μ_{sat}), cm^2/V-s	Linear Mobility (μ_{lin}), cm^2/V-s	V_{TH}, V	SS, V/dec	Trap density (from SS), cm^{-2} eV^{-1}	I_{ON}/I_{OFF}
Control	0.080 (0.075±0.005)	0.075 (0.070±0.005)	0.7±0.3	1.3	$4.4x10^{11}$	10^4
DIO (1.5 %)	0.090 (0.08 ±0.01)	0.080 (0.075 ±0.005)	1.5±1	1.2	$3.9x10^{11}$	10^4
DBRO (1.5 %)	0.22 (0.21 ±0.01)	0.17 (0.15 ±0.02)	2.0±1	0.9	$3x10^{11}$	10^5

#Highest and average value of 20 devices

A bilayer polymer dielectric system (PVA+PMMA) is adopted to achieve optimum accumulation of charges at the interface and reduced interfacial traps. The output characteristic

graphs obtained for the three devices with optimum processing conditions are shown in **Figure 3.1 b-d**. From the output curves it can be perceived that least hysteresis and highest I_{DS} is obtained for DBrO-modified device, suggesting lesser density of trap states and better charge transport compared to both DIO-modified and control devices. Transfer curves for the three devices are obtained simultaneously and shown in **Figure 3.2 a-c**. All the performance defining parameters such as linear mobility (μ_{lin}) and saturation mobility (μ_{sat}), threshold voltage (V_{TH}), subthreshold swing (SS), trap density (N_{Trap}) of the three devices are extracted and presented in **Table 3.1**. A low threshold voltage of < 1V is obtained for control device which increased slightly for the modified devices. This slight increase in V_{TH} in the modified devices is because of the residual solvent additive as these additives act as insulator, as a result higher voltage is required to switch on the device. Next to confirm the trap density, subthreshold swing (SS) is calculated and is found to be 1.3, 1.2 and 0.9 V/dec for control, DIO and DBrO-modified devices, respectively. Furthermore, the trap density is calculated from the SS values and is estimated to be 4.4 x 10^{11}, 3.9 x 10^{11} and 3.0 x 10^{11} cm^{-2} eV^{-1} for control, DIO and DBrO-modified devices, respectively. The reduced trap density for DBrO-modified device leads to mitigated hysteresis and higher I_{ON}/I_{OFF}. High back sweep current hysteresis in transfer characteristics can be observed at low V_{GS}, which can be attributed to the slow polarization effect induced by the first dielectric PVA.[34-36] However at higher V_{GS}, hysteresis is negligible in both DIO and DBrO modified devices, low back sweep hysteresis arising due to higher density of traps can be observed in the control device. All the observations suggest that the trap density reduces with inclusion of solvent additive and the least trap density is obtained for DBrO-modified device. Considering the significant improvement of the device performance with solvent additives, an analysis on the effect of solvent additive concentration on the mobility of OFETs is carried out. **Figure 3.2 d** shows the comparison of μ_{Sat} for different concentration of solvent additives. A rise in μ_{Sat} has been observed with increase in concentration of solvent additive from 0.5-1.5 % v/v. A ~3-fold enhancement in mobility (0.22 cm^2/V-s) was observed for 1.5 % v/v addition of DBrO compared to the control device (0.08 cm^2/V-s). The mobility of the DBrO device has improved significantly from the previous PTB7-Th based OFET reports.[31, 37-39]

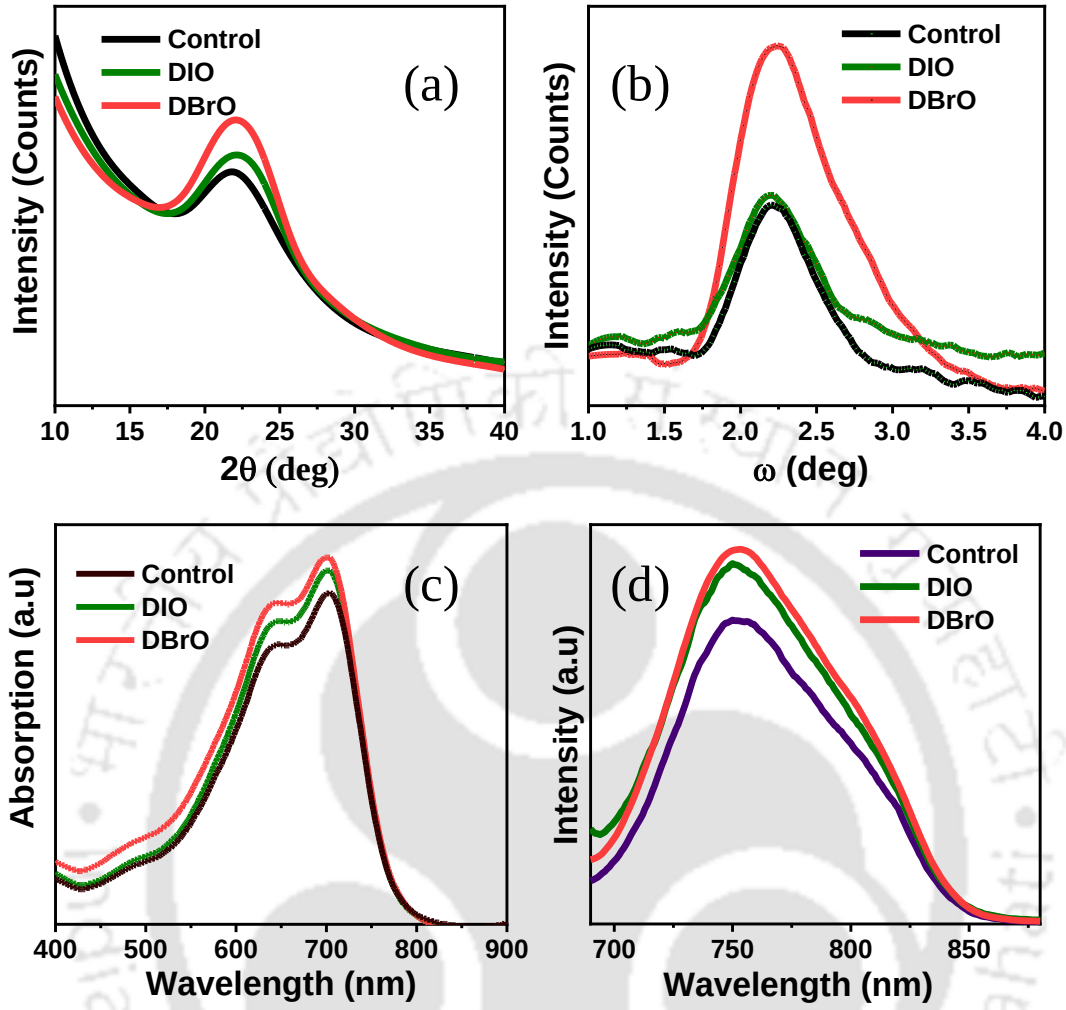


Figure 3.3**:** X-ray diffraction pattern (XRD) (a) 2theta scan, (b) omega scan (for 010 plane), (c) UV-Vis, and (d) photoluminescence spectra of PTB7-Th thin film.

However, at 2% of additive, the device repeatability and mobility reduced. This may be because of residual solvent additive at higher additive concentration resulting in increased traps states.[41] Increase in both μ_{lin} and μ_{sat} is realized for DBrO device compared to the control and DIO (**Figure 3.2 e**) due to least trap density. The μ_{sat} which is supposed to be injection limited is higher than μ_{lin} indicating that the mobility is not injection limited in the all three devices especially in DBrO-modified. The gate voltage dependent mobility plot demonstrates increased dependency of mobility on V_{GS} for DBrO (**Figure 3.2 f**). The increase in mobility with V_{GS} in the linear region is attributed to the rise in carrier concentration in the channel.[35] This confirms that the interfacial traps are less in DBrO as the mobility linearly increases with V_{GS} suggesting better accumulation even at higher V_{GS}. From the characteristic graphs it can

be analyzed that the charge transport is improved with the incorporation of solvent additives and the best results are obtained for the DBrO-modified device.

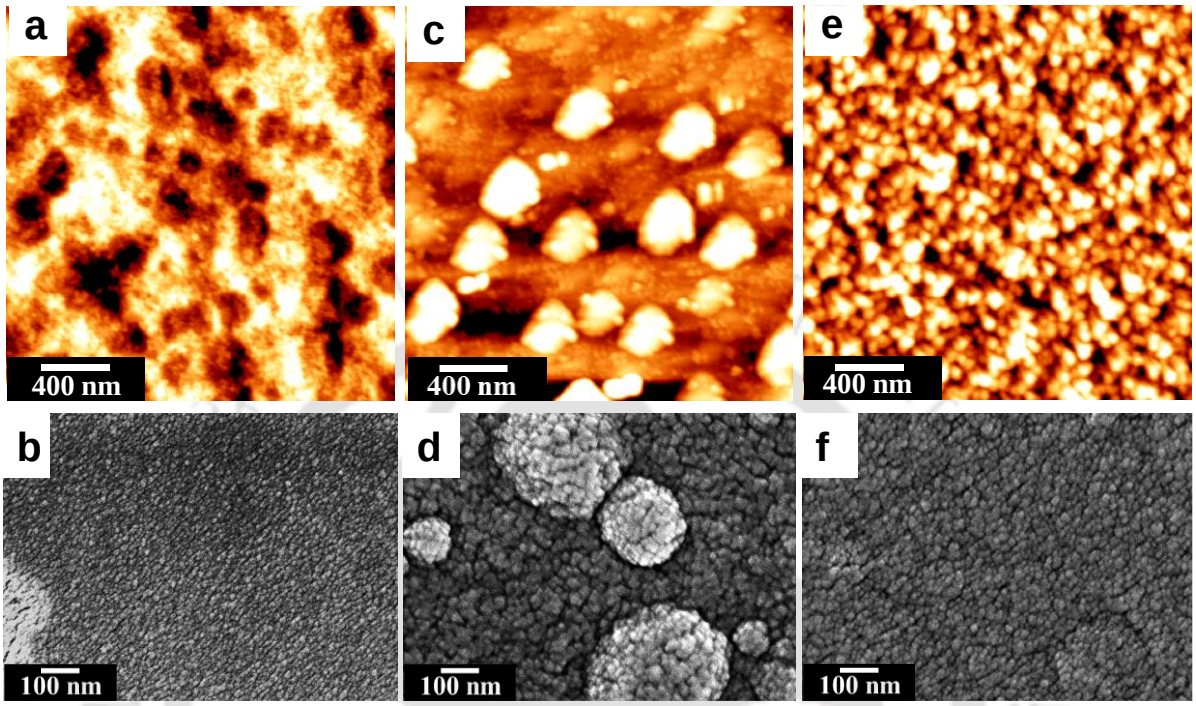


Figure 3.4: AFM, FESEM images of PTB7-Th coated on dielectric PMMA with (a), (b) no solvent additive, (c), (d) DIO as solvent additive, and (e), (f) DBrO as solvent additive.

The effect of solvent additive on the orientation, crystallinity and order of the polymer thin films were investigated by XRD and UV-Vis study. To understand the orientation of the polymer films in the direction parallel (∥) and perpendicular (⊥) to the substrate, 2θ (**Figure 3.3 a**) and grazing incidence angle scan (ω) (**Figure 3.3 b**) were recorded, respectively. ∥ is the direction of charge transport and ⊥ is the direction of charge injection for the OFET architecture adopted here.[35] Hence highly ordered film in both the directions is essential for realizing high performance of the device. In the 2θ XRD measurement, the peak for the 010 plane at 22.6˚ corresponds to the π-π stacking with d spacing of 3.9 Å. The peak intensity increased for the modified films compared to the control film and the highest intensity is obtained for DBrO-modified film. The ω scan gives the arrangement of the film in the ⊥ direction and the highest intensity is obtained for DBrO. The increased diffraction peak intensity of the DBrO-modified film in both 2θ and ω scans suggests increased crystallinity and higher ordered film of DBrO in both the ⊥ and ∥ vertical direction. This ensures better

injection of the charges in the semiconductor as well as its transport in the channel which is consistent with the mobility values extracted for the OFET devices. To better understand the degree of disorder present in the film, UV-Vis and PL spectroscopy are studied (**Figure 3.3 c, d**). As seen in the UV-Vis absorption spectra, the solvent additive modified films illustrate higher vibronic peak intensity 640 and 700 nm.[31] The shoulder peak at shorter wavelength of 500 nm also increased for DBrO modified film indicating easy high energy electronic state transition which is almost absent in the control and DIO films. The Urbach energy (E_u), another quantification of film disorder, is also extracted from the UV spectra using **Equation 3.1**:[40-42]

$$\alpha = \alpha_0 \exp\left(\frac{E}{E_u}\right), \qquad (3.1)$$

where α is the absorption coefficient, α_0 is a constant, and E is the photon energy. E_u can be extracted from inverse slope of the lnα vs E plot. The localized states near the band edge create shallow traps and Urbach energy can be directly correlated with these localized defect states or the tail states.[42, 43] The minimum value of 20 meV is found for DBrO-modified film. The DIO incorporated film has slight higher Urbach energy of 50 meV indicating disordered film which is also consistent with the XRD study whereas, control film showed the highest Urbach energy of 140 meV, hence the highest disorderness which is most likely due to utmost trap density. The photoluminescence (PL) also confirms better ordering in the DBrO film as the PL intensity follows the same order DBrO > DIO > control. All these observations are in agreement with the charge carrier mobility obtained for the OFETs. Further to investigate the impact of solvent additives in defining the morphology and crystallinity of the microstructures of the semiconductor thin film, AFM and FESEM characterizations were performed. The AFM images of the films coated on the interfacial dielectric are shown in **Figure 3.4 a-c** and the FESEM images are presented in **Figure 3.4 d-f**. In the control film, no specific structures or domains are observed (**Figure 3.4 a**), however, at higher resolution and magnification of FESEM, small domains could also be observed (**Figure 3.4 d**). In the DIO-modified film, huge aggregations separated by large distance are observed in AFM image (**Figure 3.4 b**). This sort of morphology of DIO modified PTB7-Th film has been previously obtained as well.[39] Similar aggregation is seen in FESEM image (**Figure 3.4 e**) as well, however in FESEM, the domains can be visualized and increase in domain sizes compared with the control film is observed. These large nano-aggregates likely hinder the charge transport which restricts the mobility

improvement and decreases the device repeatability. The DBrO-modified film showed distinct, homogeneous domains which are closely packed (**Figure 3.4 c**). The FESEM image (**Figure 3.4 f**) shows the compact and larger domains of the DBrO modified film. This further validates the higher crystallinity perceived from the 2θ XRD pattern (**Figure 3.3 a**) of DBrO-modified film which might be a reason for higher mobility of OFET.[43]

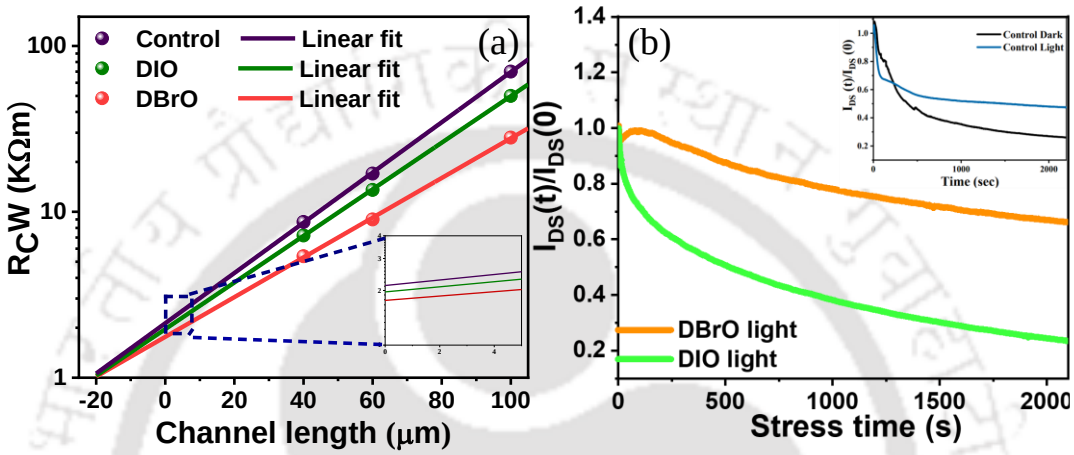


Figure 3.5: (a) Channel width normalised channel and contact resistance vs channel length plot to find the channel resistance following TLM method and the inset is showing the contact resistance of the three devices at channel length (L=0), and (b) bias stress measurement for 1hr (30 min in dark +30 min in light) of the PTB7-Th based transistor with DIO and DBrO as solvent additive and for the control device is shown in the inset.

Thereafter, to understand the influence of morphology in charge injection, the contact resistance is extracted (**Figure 3.5 a**) from the output curves at V_{GS}= -40 V. The transmission line method (TLM) used to calculate the contact resistance indicate that the DBrO-modified device had least contact resistance which explains the higher peak intensity of DBrO modified film in the ω scan (**Figure 3.3 b**) confirming better charge injection compared to DIO-based and control devices. The channel resistance (at L > 0 μm) also follows the same sequence indicating better charge transport in DBrO. Next, the stability of the device is tested to understand the effect of traps and defects in deteriorating device conditions. The bias stress measurement for the devices in dark and under illumination are measured for 1 hour (30 min in dark + 30 min in light) (**Figure 3.5 b**). The DBrO device showed sluggish decay and the device retained 60% of the initial current value in dark and 78% in illumination.

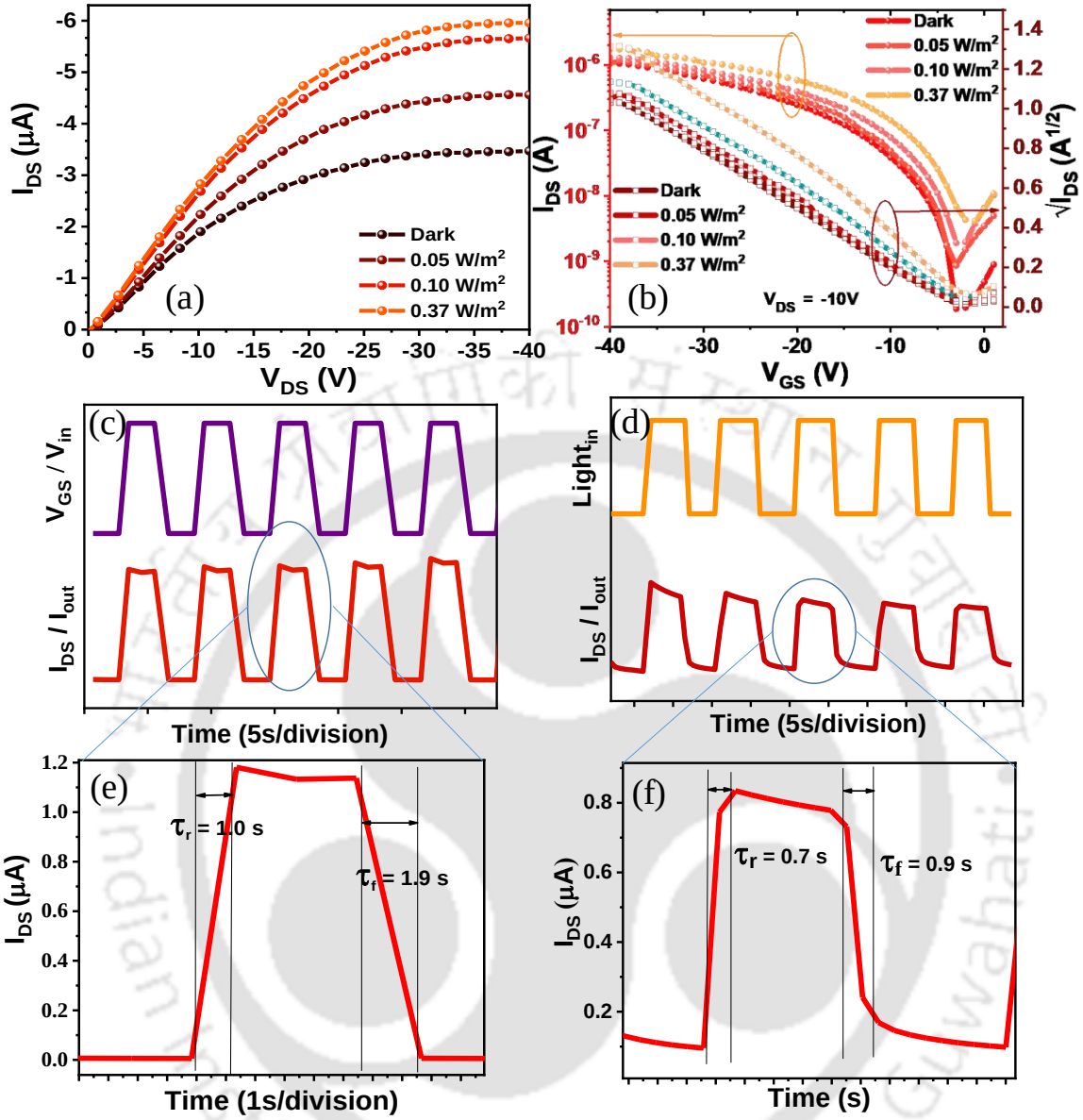


Figure 3.6: (a) Output characteristics and (b) transfer characteristics of PTB7-Th based PT at different light intensities, I_{DS} response as a function of (c) pulsed V_{GS} (0.2 Hz) and (d) pulsed light input (0.2 Hz), Rise time and fall time of I_{DS} vs. time for (e) V_{GS} input, (f) light input.

The DIO-modified device retained 58% in dark and reduced to 25% of initial I_{DS} under illumination. The control device degrades to 20 % of the initial I_{DS} in dark (**Figure 3.5 b** inset) and to ~50% under light. Though in dark both DIO and DBrO devices show comparable stability but under illumination DIO device degrades significantly. The reduced stability of DIO device compared to DBrO is because of residual DIO forming photo-acid in presence of light.[21] Iodine readily dissociates in presence of light to form HI which is a strong acid and its

presence in the semiconductor film degrades the device properties, whereas, DBrO does not readily dissociate, hence formation of photo-acid is hindered.[44] Owing to higher electronegativity of bromine compared to iodine, bromine is a better electron acceptor as well. As a result, it helps in improving the charge transport of holes.[44] Thus, by introducing DBrO as solvent additive, a significant enhancement of device stability is realized which suggests that infusing DBrO reduces the interfacial and bulk trap states significantly and contributes to improving the OFET-based device performance and increases its stability. On obtaining the best device performance and stability for DBrO-modified OFET device, its photo response behavior is studied using a light source having a band-pass wavelength of 500-800 nm. Output and transfer characteristic showing the photoresponse at different light intensities are obtained for the same device architecture and shown in **Figure 3.6 a, b** respectively and the values are listed in **Table 3.2**. Maximum photo responsivity of 688 A/W and Detectivity of 1.2 x 10^{11} is obtained at a light intensity of 0.05 W/m^2. The Responsivity (R) and Detectivity (D*) are calculated using **Equations 3.2** and **3.3** respectively:

$$R = (I_{Light} - I_{Dark})/(P_{in} \times S) \quad (3.2)$$

$$D^* = R \times S^{1/2}(2eI_{Dark})^{-1/2} \quad (3.3)$$

Table 3.2: Photo response characteristics of the DBrO PT

Power, W/m^2	Responsivity, A/W	Detectivity
0.37	209	3.6 x 10^{10}
0.10	460	9.2 x 10^{10}
0.05	688	1.2 x 10^{11}

where I_{Light} represents the source-to-drain current under illumination, I_{Dark} is the source–drain current under dark, and P_{in} represents the power of the incident light per unit area, e is the charge of an electron, S (=3.2 x 10^{-4} cm^2) is the effective sensing area of the device. Finally, the electro-optical response of the DBrO device is tested by employing a combination of light and electrical signal. The change in output current (I_{OUT}/I_{DS}) with the two inputs, optical ($Light_{in}$) and electrical (gate voltage, V_{GS}) are shown in **Figure 3.6 c, e**. This can be presented as an OR gate with light and gate voltage as the two inputs as a high output current i.e., a drain current (I_{DS}) will be obtained if either of the two inputs are high. **Figure 3.6 c, e** demonstrates the OR gate function of the OFET. The rise time (τ_r) and fall time (τ_f) are shown in **Figure 3.6 d, f** and a total response time ($\tau_r + \tau_f$) of 1.6 s is obtained for light switching at V_{GS} = -40 V.

3.4 Conclusions

In summary, enhanced device performance of p-type PTB7-Th based FET is demonstrated utilizing a solvent additive incorporation strategy. Two solvent additives, namely DIO and DBrO, are used and their effects on the device parameters are carefully investigated. The morphology of the semiconductor thin film can be regulated via fine tuning the functionalization of the solvent additives. The concentration of the additives is also optimized strategically and it is found that the device with optimal DBrO concentration reveals highest mobility of 0.22 cm^2/V-s which is almost 3 times higher than that of the control device. The stability of the DBrO modified device also significantly improves under dark and under illumination where it retains ~78% of the device properties after 1 hour of bias stress. This notable device performance is attributed to the improved film morphology and reduced traps. After confirming the best device performance and stability under illumination, PT was fabricated with the DBrO modified device. A responsivity of 688 A/W is obtained for an applied optical power of 0.05 W/m^2. This facile additive engineering approach provides deep insights into the morphology driven correlation with FET device parameters and their application in PTs.

References

1. B. Kumar, B. K. Kaushik and Y. S. Negi, *Polym Rev*, 2014, **54**, 33-111.
2. G.-S. Ryu and Y.-Y. Noh, *Mol. Cryst. Liq.*, 2017, **652**, 207-212.
3. X. Zhang, H. Bronstein, A. J. Kronemeijer, J. Smith, Y. Kim, R. J. Kline, L. J. Richter, T. D. Anthopoulos, H. Sirringhaus, K. Song, M. Heeney, W. Zhang, I. McCulloch and D. M. DeLongchamp, *Nat. Commun.*, 2013, **4**, 2238.
4. Z. Zhao, Z. Yin, H. Chen, L. Zheng, C. Zhu, L. Zhang, S. Tan, H. Wang, Y. Guo, Q. Tang and Y. Liu, *Adv. Mater.*, 2017, **29**, 1602410.
5. S. Vasimalla, S. P. Senanayak, M. Sharma, K. S. Narayan and P. K. Iyer, *Chem. Mater.*, 2014, **26**, 4030-4037.
6. R. K. Gupta, R. Garai, M. Hossain, M. A. Afroz, D. Kalita and P. K. Iyer, *J. Mater. Chem. C*, 2021, DOI: 10.1039/D1TC01860D.
7. E.-S. Shin, J.-Y. Go, G.-S. Ryu, A. Liu and Y.-Y. Noh, *ACS Appl. Mater. Interfaces*, 2021, **13**, 4278-4283.
8. H.-R. Tseng, H. Phan, C. Luo, M. Wang, L. A. Perez, S. N. Patel, L. Ying, E. J. Kramer, T.-Q. Nguyen, G. C. Bazan and A. J. Heeger, *Adv. Mater.*, 2014, **26**, 2993-2998.
9. H.-R. Tseng, L. Ying, B. B. Y. Hsu, L. A. Perez, C. J. Takacs, G. C. Bazan and A. J. Heeger, *Nano Lett.*, 2012, **12**, 6353-6357.
10. M. S. Chen, O. P. Lee, J. R. Niskala, A. T. Yiu, C. J. Tassone, K. Schmidt, P. M. Beaujuge, S. S. Onishi, M. F. Toney, A. Zettl and J. M. J. Fréchet, *J. Am. Chem. Soc.*, 2013, **135**, 19229-19236.
11. E. F. Manley, J. Strzalka, T. J. Fauvell, T. J. Marks and L. X. Chen, *Adv. Energy Mater.*, 2018, **8**, 1800611.
12. G. J. Chae, S.-H. Jeong, J. H. Baek, B. Walker, C. K. Song and J. H. Seo, *J. Mater. Chem. C*, 2013, **1**, 4216-4221.
13. T. K. An, I. Kang, H.-j. Yun, H. Cha, J. Hwang, S. Park, J. Kim, Y. J. Kim, D. S. Chung, S.-K. Kwon, Y.-H. Kim and C. E. Park, *Adv. Mater.*, 2013, **25**, 7003-7009.
14. J. K. Park, B. Walker and J. H. Seo, *ACS Appl. Mater. Interfaces*, 2013, **5**, 4575-4580.
15. Y. J. Park, J. H. Seo, W. Elsawy, B. Walker, S. Cho and J.-S. Lee, *J. Mater. Chem. C*, 2015, **3**, 5951-5957.
16. M. S. Park and F. S. Kim, *Polymers*, 2019, **11**, 112.

17. W. J. Park, S. H. Chae, J. Shin, D. H. Choi and S. J. Lee, *Synth. Met.*, 2015, **205**, 206-211.
18. J. W. Jeong, G. Jo, S. Choi, Y. A. Kim, H. Yoon, S.-W. Ryu, J. Jung and M. Chang, *ACS Appl. Mater. Interfaces*, 2018, **10**, 18131-18140.
19. C. P. L. Rubinger, H. F. Haneef, C. Hewitt, D. Carroll, J. E. Anthony and O. D. Jurchescu, *Org. Electron.*, 2019, **68**, 205-211.
20. G. Jo, S. H. Cho, H. Kim, H. Yoon, S. Han and M. Chang, *Org. Electron.*, 2020, **81**, 105688.
21. N. Y. Doumon, G. Wang, X. Qiu, A. J. Minnaard, R. C. Chiechi and L. J. A. Koster, *Sci. Rep.*, 2019, **9**, 4350.
22. C. McDowell, M. Abdelsamie, M. F. Toney and G. C. Bazan, *Adv. Mater.*, 2018, **30**, 1707114.
23. S. Ishida, Y. Anno, M. Takeuchi, M. Matsuoka, K. Takei, T. Arie and S. Akita, *Sci. Rep.*, 2015, **5**, 15491.
24. Y. Chu, X. Wu, J. Lu, D. Liu, J. Du, G. Zhang and J. Huang, *Adv. Sci.*, 2016, **3**, 1500435.
25. H.-S. Kang, C.-S. Choi, W.-Y. Choi, D.-H. Kim and K.-S. Seo, *Appl. Phys. Lett.*, 2004, **84**, 3780-3782.
26. F. Li, Y. Chen, C. Ma, U. Buttner, K. Leo and T. Wu, *Adv. Electron. Mater.*, 2017, **3**, 1600430.
27. Q. Tang, L. Li, Y. Song, Y. Liu, H. Li, W. Xu, Y. Liu, W. Hu and D. Zhu, *Adv. Mater.*, 2007, **19**, 2624-2628.
28. A. Dey, A. Singh, D. Das and P. K. Iyer, *Phys. Chem. Chem. Phys.*, 2016, **18**, 32602-32609.
29. P. Gu, Y. Yao, L. Feng, S. Niu and H. Dong, *Polym. Chem.*, 2015, **6**, 7933-7944.
30. Q. Li, Y. Ran, W. Shi, M. Qin, Y. Sun, J. Kuang, H. Wang, H. Chen, Y. Guo and Y. Liu, *Appl. Mater. Today*, 2021, **22**, 100899.
31. R. Garai, M. Adil Afroz, R. K. Gupta, A. Choudhury and P. K. Iyer, *ACS Omega*, 2020, **5**, 2747-2754.
32. R. Fan, Z. Huai, Y. Sun, X. Li, G. Fu, S. Huang, L. Wang and S. Yang, *J. Mater. Chem. C*, 2017, **5**, 10985-10990.

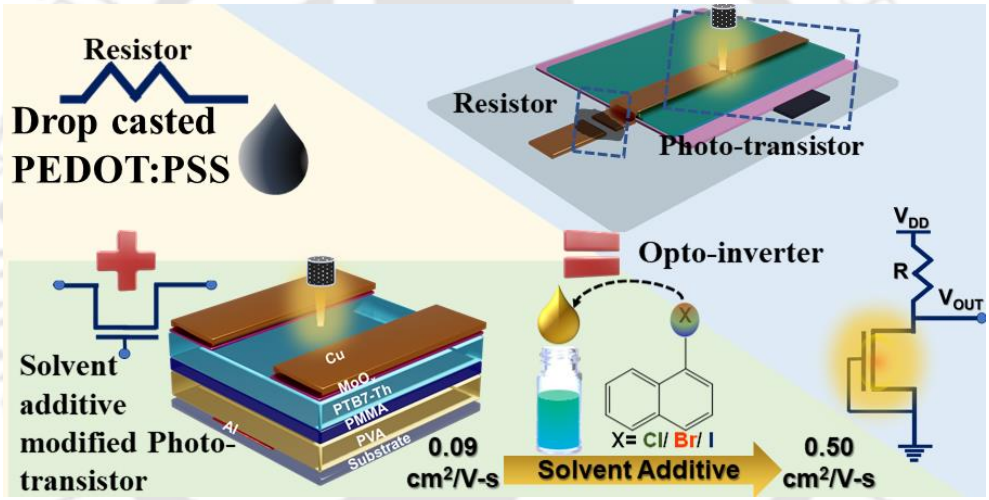
33. R. K. Gupta, R. Garai, M. A. Afroz and P. K. Iyer, *J. Mater. Chem. C*, 2020, **8**, 8191-8198.
34. S. D. Baranovskii, *Phys. Status Solidi B*, 2014, **251**, 487-525.
35. S. Jung, J. W. Jin, V. Mosser, Y. Bonnassieux and G. Horowitz, *IEEE Trans. Electron Devices*, 2019, **66**, 4894-4900.
36. S. Vasimalla, N. V. V. Subbarao and P. K. Iyer, *J. Mater. Chem. C*, 2016, **4**, 7102-7109.
37. K. Patrikar, N. Jain, D. Chakraborty, P. Johari, V. R. Rao and D. Kabra, *Adv. Funct. Mater.*, 2019, **29**, 1805878.
38. S. F. Hoefler, T. Rath, N. Pastukhova, E. Pavlica, D. Scheunemann, S. Wilken, B. Kunert, R. Resel, M. Hobisch, S. Xiao, G. Bratina and G. Trimmel, *J. Mater. Chem. A*, 2018, **6**, 9506-9516.
39. A. Choudhury, R. K. Gupta, R. Garai and P. K. Iyer, *Adv. Mater. Interfaces*, 2021, **8**, 2100574.
40. R. Garai, R. K. Gupta, A. S. Tanwar, M. Hossain and P. K. Iyer, *Chem. Mater.*, 2021, **33**, 5709–5717.
41. V. R. Akshay, B. Arun, G. Mandal and M. Vasundhara, *Phys. Chem. Chem. Phys.*, 2019, **21**, 12991-13004.
42. R. K. Gupta, R. Garai, M. Hossain, A. Choudhury and P. K. Iyer, *ACS Sustainable Chem. Eng.*, 2021, **9**, 7993-8001.
43. J. Cheng, R. Hu, X. Meng, Y. Li, X. Yan, X. Yang, X. Liao, L. Li, Q. Pei and K. B. Chong, *Sol. RRL*, 2018, **2**, 1800064.
44. J. Yuan, Y. Xu, G. Shi, X. Ling, L. Ying, F. Huang, T. H. Lee, H. Y. Woo, J. Y. Kim, Y. Cao and W. Ma, *J. Mater. Chem. A*, 2018, **6**, 10421-10432.

[This page was intentionally left blank]

Chapter 4

Engineering Semiconductor Layer using Halonaphthalene Additives for Organic Opto-Inverter Circuit

---



Manuscript: Anwesha Choudhury, Ritesh Kant Gupta, Rabindranath Garai, Parameswar Krishnan Iyer, "Engineering Semiconductor Layer Using Halonaphthalene Additives for Organic Opto-Inverter Circuits." *ACS Appl. Electron. Mater.* **2022**, DOI: 10.1021/acsaelm.2c01272.

[This page was intentionally left blank]

Abstract

Solution processable organic field-effect transistors (OFETs) are at the forefront of the future of electronic circuits. They have the potential for low-cost, large-scale fabrication on a variety of substrates. However, their application in electronic circuits is challenged by the unforeseen presence of defects leading to lower mobility. This contribution demonstrates the application of a photo-active polymer-based phototransistor (PT) in a digital electronic circuit. Initially, solvent additive engineering strategy is adopted to tune the thin film morphology and reduce morphology related defects, resulting in improved device performance. The incorporation of 1-bromonaphthalene improves the mobility from 0.09 to 0.50 $cm^2 V^{-1} s^{-1}$ with enhancement in both photo-absorption and photo-stability. The results are well supported with electrical characterization, photo-physical and morphological studies. Thereafter a novel and unique architecture of opto-inverter is presented using the PT. In this work, opto-electronic logic NOT gate is also fabricated by utilizing a simple resistive load circuit. This circuit demonstrated the combined functionality of a logic gate and a transducer. Further, this technique can be easily implemented for minimizing the circuit components and complexity by replacing a photodetector and a NOT gate with a single opto-inverter in application requiring both

4.1 Overview

Over the last few years, solution processable organic field effect transistors (OFETs) based integrated circuits (ICs) like basic logic gates have seen a surge in research interest.[1-4] This is because of the enormous advantages such as low cost and easy processing, band tunability, and the possibility to be fabricated on a variety of substrates like plastic, cloth, paper, etc.[5-7] But the morphological defects are more challenging in thin films formed by solution processing rather than vacuum deposition. Even though transistors are known to be the basic building block for any IC, the OFETs have found their applications primarily in switches and are being extended to biological, chemical, and gas sensors.[8-11] Utilizing OFETs for designing various other circuits needs more exploration to realize potentially efficient devices and applications. One of the fundamental hurdles for OFETs to be employed in IC is its low mobility, limiting its use primarily to sensors, where the requisite is only the amplification of the output signal and not high mobility of the OFET. The key factors contributing in restricting the mobility are morphological disorder, interfacial traps, and traps contributed from environmental conditions like moisture, temperature, and light. Several materials have been developed and simple device engineering strategies have been utilized till date to improve the mobility and performance of the device.[12-14] The strategy of incorporating solvent additive is one such technique to modulate the morphology of the polymer thin film and enhance the device performance.[15, 16] There are numerous reports confirming the usage of solvent additives as morphology modifier for solar cell applications and they have the ability to tune OFET device performance,[17, 18] however, this is relatively new for transistor applications. Thus, the choice of solvent additive can open up newer avenues for OFET application beyond sensors. The mobility obtained in this work is highest for all OFET based devices with PTB7-Th including our previous works.[7, 15, 19, 20] The molecular structure and bandgap of organic semiconductors induce photoelectric properties in OFETs which have allowed them to be utilized as phototransistors (PT), light-emitting transistors, optical memory devices, and photo synaptic transistors.[21-25] Recently, OFETs have also been investigated for fabrication of integrated circuits (ICs) and various logic gates.[1, 2] However, most of the reports have explored the ambipolar nature of the semiconducting organic layer for transistors with

only electrical input and output. Further, IC fabrication for inverter application utilizing n-type and p-type OFETs (complementary OFETs) on the same substrate has been also attempted.[26, 27] Nevertheless, these type of inverters involve complex fabrication steps as two separate transistors with different channel dimensions and electrodes are required on the same substrate.[1, 2, 26, 28] This requires separate optimization of channel dimensions and charge transport properties of the two different transistors. Whereas, resistive load inverters (RLIs) in which one of the transistors is replaced with a resistance reducing the overall fabrication complexity. However, this technology has been less explored in the scientific community due to the requirement of extra layout space and additional component. Utilizing PT in of RLIs will allow easy implementation of opto-inverters which will facilitate the use of both electrical and optical inputs and eliminate any extra fabrication cost.

It has been generally observed that an external component is integrated with a transistor for fabrication of a conventional RLIs. For the removal of that external component a resistive load opto-inverter has been fabricated by integrating a simple resistive component (drop-casted PEDOT:PSS) with PTB7-Th based PT in this work. In this simple IC, combined function of a transducer converting the light input to electrical output and a logic NOT gate to invert the input signal is availed. Unlike a simple photodetector, here the need for a separate driving circuit is eliminated, lowering the circuit complexity and improving the overall circuit compactness. For implementing the opto-inverter, the resistor was fabricated simultaneously along with the OFET on the same substrate. At first the solvent additive technique is utilized to improve the PTB7-Th based OFET. A series of naphthalene-based solvent additives, namely 1-Chloronaphthalene (CN), 1-Bromonaphthalene (BN), 1-Iodonaphthalene (IN), were studied, and their effect on OFET characteristic parameters are compared with the device without any solvent additive. All three additives have shown modulation of the device properties. However, the highest mobility of 0.50 $cm^2 V^{-1} s^{-1}$ is obtained for the BN modified device. Further, the photo response of the PTB7-Th based PT is examined by analyzing various parameters such as responsivity, detectivity, and their stability under light and in the dark. After examining the light response and stability of the variants of the device, the opto-inverter circuit is fabricated and characterized to invert the electrical output to validate the function as logic NOT gate.

4.2 Experimental Section

4.2.1 Materials

PTB7-Th was thermally synthesized according to the previous literature.[20] Poly(methyl methacrylate) (average Mw ~ 996 kDa), Molybdenum(VI) oxide, and Aluminium and Copper wire were purchased from Sigma Aldrich, Poly(3,4-ethylene dioxythiophene)-poly(styrene sulfonate) (PEDOT:PSS, PVP AI 4083) was bought from Clevios and PVA (average Mw ~ 115 kDa) from Loba Chemicals and used without further purification.

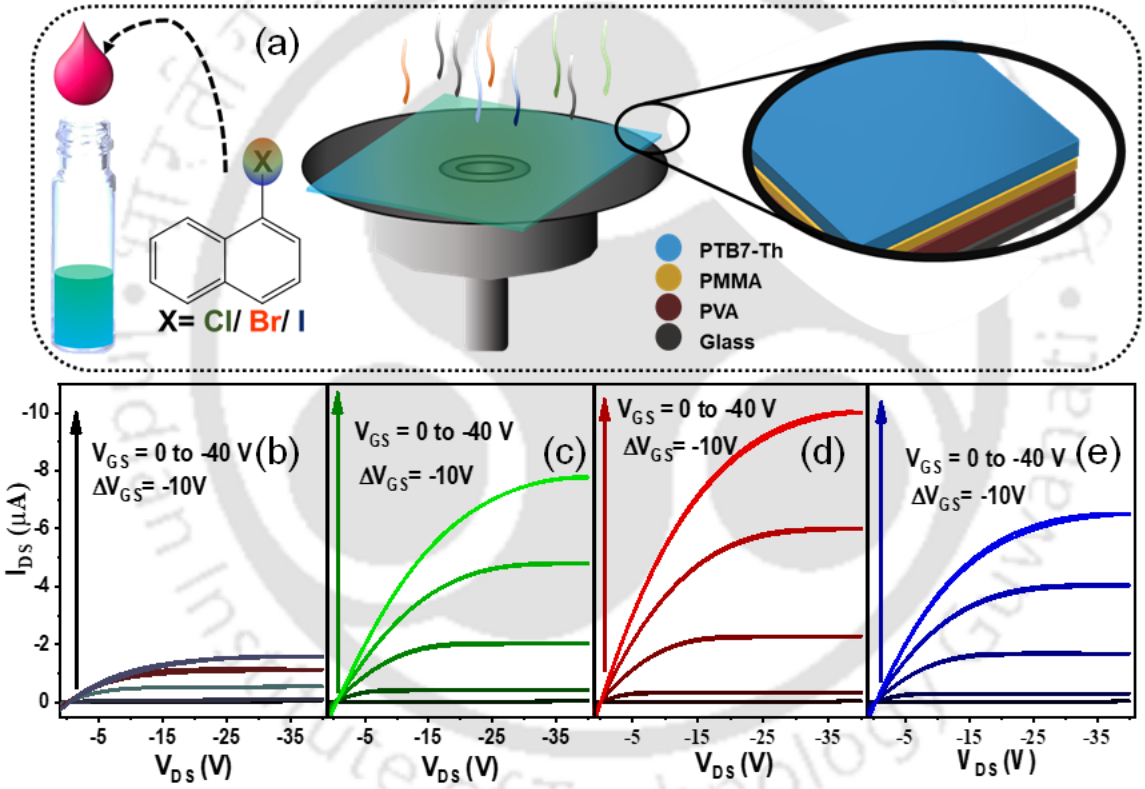


Figure 4.1: (a) Schematic of PTB7-Th thin-film coating; output characteristics of (b) Control, (c) CN (d) BN (e) IN modified OFETs.

4.2.2 Device Fabrication

OFET: The OFET fabrication technique and OFET parameter calculation formulae used are similar to our previous work.[15] For semiconductor layer spin coating, solvent additives

(CN, BN, IN) was added and kept on stirring for 10 min more. The devices were optimized for different concentrations (0% or control device, 0.5% v/v, 1% v/v, 1.5% v/v, 2% v/v) of the solvent additives.

Opto-Inverter Circuit: For the resistive load, the drain electrode was extended, and a channel of 100 µm was made by shadow masking simultaneously during the source-drain deposition. After deposition of the metal electrode, PEDOT:PSS was drop cast on the Channel and vacuum dried for 10 hours before starting measurement.

4.2.3 Characterization

The thickness of the thin films was measured using Dektek 150 stylus profiler. The AFM images were recorded in tapping mode on an Agilent 5500 AFM/SPM microscope to avoid tip surface interaction causing any film damage. All electrical characterizations were performed using a Keithley 4200 SCS parameter analyzer under vacuum conditions. For the phototransistor and opto-inverter measurements, an Oriel DC regulated illuminator of 0.37 W m^{-2} power and wavelength in the range of 550-800 nm was used. For UV-VIS, a Shimadzu UV 2600 UV-VIS spectrophotometer, for PL measurements, a Horiba Fluoromax-4 spectrofluorometer was used, and for XRD, a Rigaku X-ray diffractometer was used.

4.3 Results and Discussions

One of the many challenges of fabricating an OFET is obtaining optimum morphology of a solution-processed semiconductor layer. Four variants of OFET (one control and three additive modified) are fabricated with the bottom-gate-top contact architecture, where PTB7-Th is used as the photosensitive semiconductor layer, to investigate the role of solvent additive as morphology modifier in modulating transistor performance. Three types of morphology modifier (CN, BN and IN) is utilized to fabricate devices along with chlorobenzene (CB) as the primary processing solvent. For comparison, a control device is fabricated with only CB as the processing solvent The schematic representation of the PTB7-Th thin film formation for OFET is shown in **Figure 4.1 a**. **Figure 4.1 b-e** shows the output characteristic graphs of all the where it can be observed that the BN-modified device has demonstrated the highest current and no hysteresis.

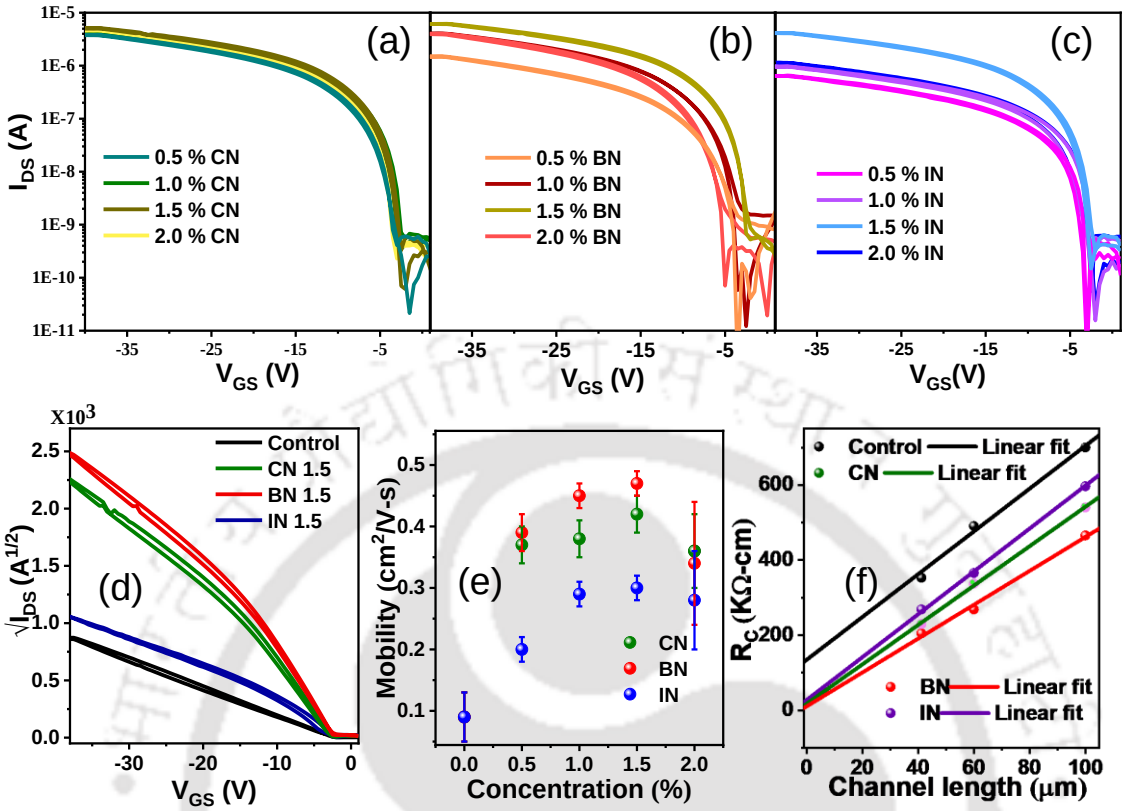


Figure 4.2: Comparison of transfer characteristics at different concentrations of solvent additives (a) CN (b) BN (c) IN modified OFETs, (d) comparison of the $\sqrt{I_{DS}}$ vs. V_{GS} for the four variants of OFET; (e) error bar diagram showing the change in mobility of the OFETs with different concentrations of solvent additives; (f) Channel width normalized channel resistance vs channel length plot to find the contact resistance following the TLM method.

The comparison of transfer characteristics (**Figure 4.2 a-c**) with various concentrations of the solvent additives is also recorded. **Figure 4.2 d** comprises of the transfer characteristic curves for the best concentration of device (1.5% v/v) for each solvent additive. The optimum device properties in terms of mobility are defined by 1.5% v/v of solvent additive as depicted in the error bar diagram (**Figure 4.2 e**). On increasing the additive concentration above 1.5% v/v, the device properties degrade, and a huge variation is observed in the mobility value which might be due to the residual additive as already obtained in one of our previous works.[15] Transmission line method has been utilized to evaluate the contact resistance for all the devices (**Figure 4.2 f**). The resistances are extracted from the output characteristic graph of the device fabricated with different channel lengths (40 μm, 60 μm, 100 μm). The obtained contact

resistances for the control device is ~129 KΩ-cm, as well as CN, BN and IN modified device are ~13 KΩ-cm, ~7 KΩ-cm, and ~21 KΩ-cm respectively. Hence it can be observed that the contact resistance reduces with the inclusion of solvent additive, and the lowest contact resistance is observed for the BN modified device. This suggests that the inclusion of the solvent additive not only improves the charge transport but also enhances the charge injection in the semiconductor layer.

Table 4.1. Summarized OFET parameters.

Device	Linear Mobility (μ), [cm^2 V^{-1} s^{-1}] [a)]	V_{TH}, [V][a)]	SS, V dec^{-1}	Trap density (from SS), cm^{-2} eV^{-1}	I_{ON}/I_{OFF} $_{OFF}$
Control	0.09 (0.08±0.01)	1.9±1	1.26	4.4x10	10^4
CN (1.5 %)	0.42 (0.39 ±0.03)	3.0±1	0.91	3.9x10	10^5
BN (1.5 %)	0.50 (0.47 ±0.03)	3.3±1	0.88	3.1x10	10^5
IN (1.5 %)	0.30 (0.29 ±0.01)	2±1	0.83	2.0x10	10^5

[a)] Standard deviation of 20 devices

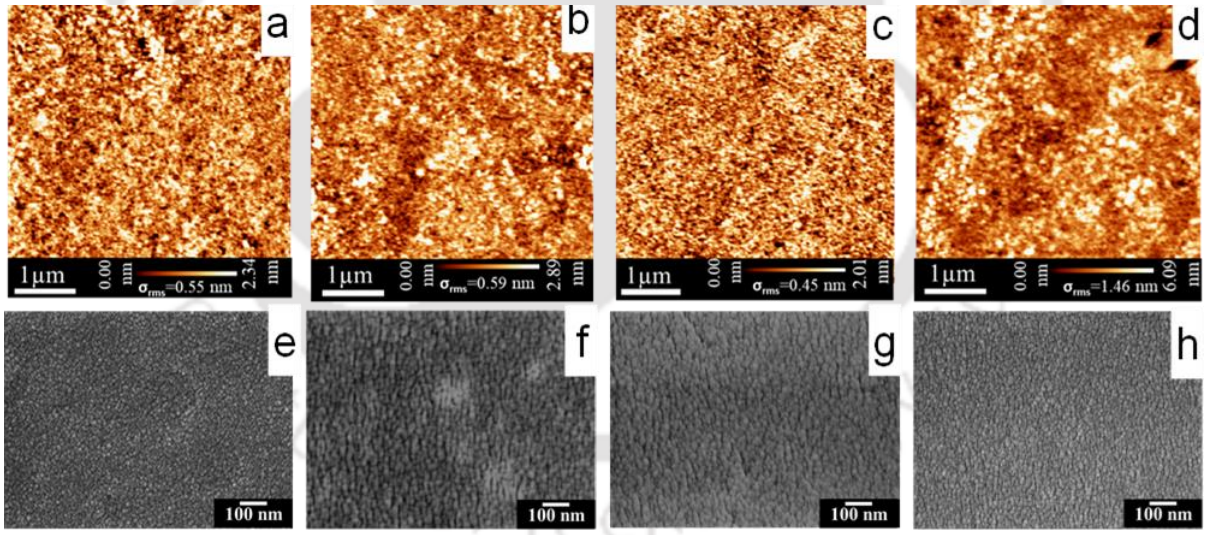


Figure 4.3: AFM, FESEM images of PTB7-Th coated on dielectric PMMA with (a), (e) no solvent additive, (b), (f) CN as solvent additive, (c), (g) BN as solvent additive and (d), (h) IN as solvent additive respectively.

To better understand the device properties, a comparison of all the device parameters was performed and listed in **Table 4.1**. The control device exhibits mobility of 0.09 cm^2 V^{-1} s^{-1} which improves to 0.30 cm^2 V^{-1} s^{-1} after adding an optimal amount (1.5% v/v) of IN as solvent additive, which further enhanced to 0.42 cm^2 V^{-1} s^{-1} with

CN as a solvent additive in the same concentration as the processing solvent CB. However, the highest mobility of 0.50 cm^2 V^{-1} s^{-1} is obtained from the BN modified device, which is the best value reported till date for PTB7-Th based OFETs. [7, 15, 19, 29, 30] A slight increase in threshold voltage is noticed in the modified devices (3.3 V) compared to the control device (1.9 V). This increase in threshold voltage may be due to the residues of the high boiling point solvent additives as they are insulators in nature, acting as traps. Hence higher voltage is required for sufficient accumulation of charges to turn on the device. The sub-threshold swing also improved for the modified devices, while almost similar I_{ON}/I_{OFF} is obtained for all the devices.

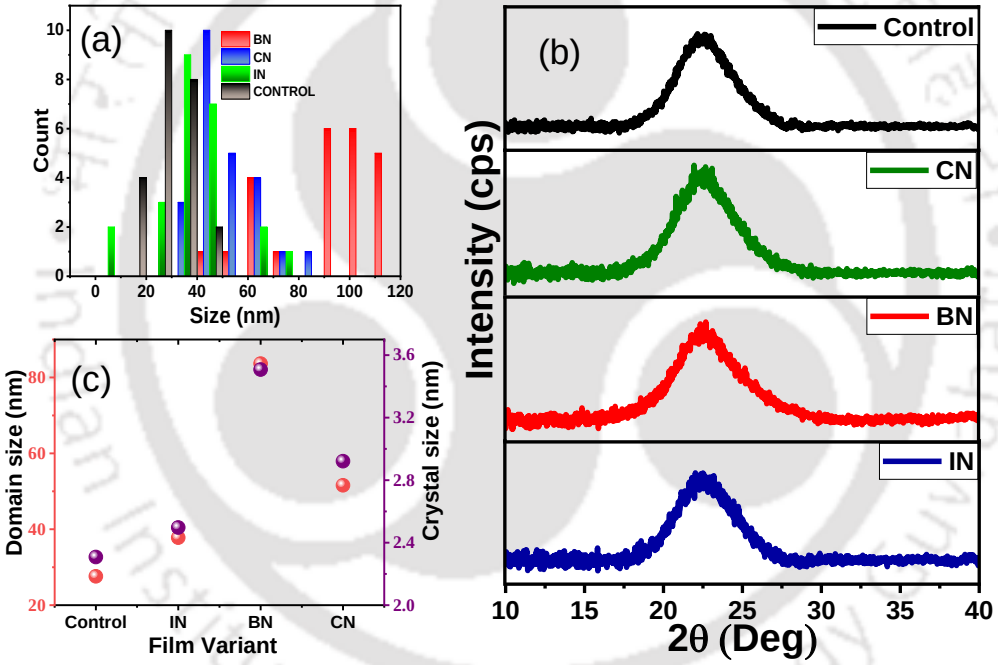


Figure 4.4: (a) Domain size distribution measured from FESEM;(b) XRD spectra; (c) comparison of the domain size obtained from FESEM and the crystal size calculated from XRD of the control, CN, BN, IN modified films.

Further, to understand the mechanism behind the improvement in the device properties, the semiconductor morphology is examined utilizing AFM and FESEM analyses. It can be observed from the AFM images (**Figure 4.3 a-d**) that the root mean square roughness (σ_{rms}) of all the modified films has reduced compared with the control film. The least roughness is obtained for the BN-modified film. This is in agreement

with the enhanced charge transport and hence high charge carrier mobility of the BN-modified device.[31] The change in morphology and variation in domain size of the semiconductor film with the inclusion of solvent additive is easily distinguishable from the FESEM images (**Figure 4.3 e-h**). It can be well observed that the shape of the domains also changes with the inclusion of various additives. The control film (**Figure 4.3 e**) shows the smallest and spherical shaped domains, whereas with the incorporation of solvent additives the domains become more fibrillar and the average size also increases. BN-modified film displayed largest grain size (**Figure 4.4 a**). The larger size of the domains can be linked with higher mobility values as the highly ordered and interconnected fibrillar structure are reported to improve the charge transport.[32, 33] To consider the bulk crystallinity, XRD spectra is recorded as shown in (**Figure 4.4 b**) from where full width half maxima (FWHM) and crystal size are also estimated (**Figure 4.4 c**). FWHM was the least for BN-modified film which also confirms its largest crystallite size. This follows a same trend as that of the domain size obtained from the FESEM results. A clear correlation between the bulk crystallinity and the surface morphology is drawn and is in good agreement with the mobility values obtained for the OFET devices.

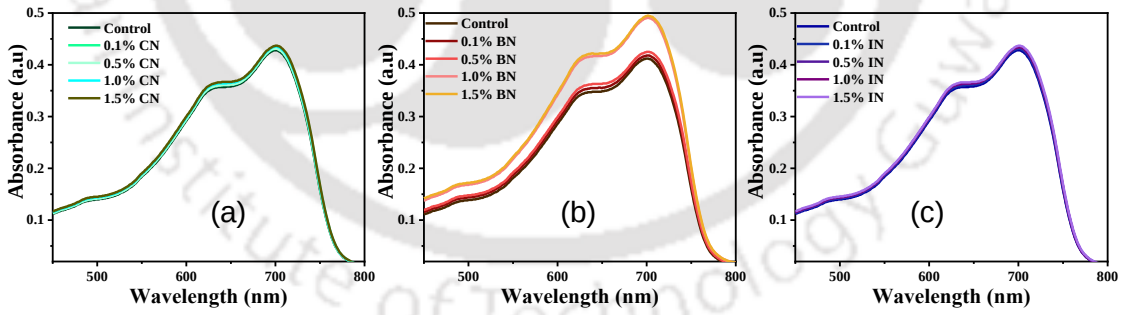


Figure 4.5: UV-Vis absorption of the PTB7-Th solution with different concentrations of the additives (a) CN, (b) BN, and (c) IN.

In order to get an insight of the effect of the solvent additives in modifying the light sensing property, UV-vis absorption spectra of the polymer solution with different solvent additive loading is collected. The crystallization process can be determined from the aggregation formed in the polymer solution prior to the spin-coating.

Predetermination of the growth and nucleation of the thin film from the UV-vis of the polymer solution has been previously reported[17, 34, 35] No significant change in absorption spectra is observed on gradually increasing the loading of CN and IN from 0.1% to 1.5% v/v. However, on increasing the loading of BN from 0.1% to 1.5% v/v, a significant enhancement in the absorbance occurs (**Figure 4.5**) indicating that BN helps in improving the absorption of PTB7-Th which was absent in the case of CN and IN loading.

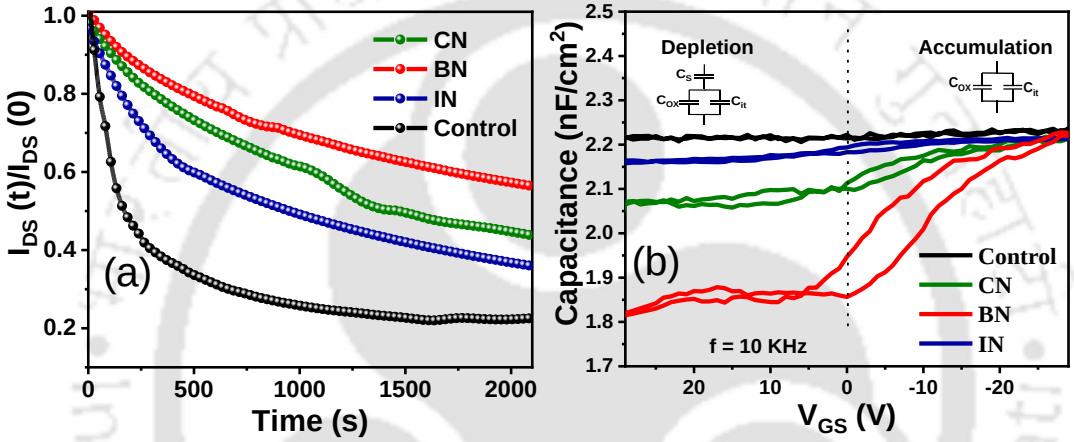


Figure 4.6: (a) Normalized drain current behaviour under bias stress of V_{GS} = V_{DS}= -40 V and (b) capacitance vs voltage characteristic curve comparison for the CN, BN, IN modified devices at 10 kHz frequency for the control, CN, BN, IN modified devices.

Next, to understand the effect of incorporating high boiling point solvent additive in charge trapping and transport properties of the devices, an important criterion that needs to be analyzed is the stability of the device. The device stability is tested through a bias stress measurement, in which a constant voltage of V_{DS} = V_{GS} = - 40 V for 30 min is applied. It was suspected that the residuals of solvent additive might hamper device stability in the long run. However, surprisingly, the device's stability has improved with the incorporation of solvent additives which is most likely due to the improved crystalline morphology. This resulted in lower traps than control, thereby improving the device stability.[36] **Figure 4.6 a** shows the normalized decay of drain current. The control device degrades to 25% of its initial current value after 30 min of bias stress. However, the IN modified device retained 37% of its initial properties, and the CN modified device retained 45%, and BN retained 60%. In addition to

this, the presence of traps can also be observed from the capacitance-voltage (CV) measurement (**Figure 4.6 b**) The total capacitance can be modelled as the semiconductor capacitance (C_S) in series with the combination of interfacial capacitance (C_{it}) and the dielectric capacitance (C_{ox}) in parallel. The dielectric capacitance, which is $C_{ox}=\varepsilon A/d$, (where ε is the equivalent dielectric constant, A is the area and d is the width of the dielectrics) remains constant throughout the voltage sweep (-30 V to 30 V). In the accumulation region (negative voltage sweep region) charges are accumulated at the dielectric-semiconductor interface and the equivalent capacitance reduces to a parallel combination of C_{ox} and C_{it} only (inset of **Figure 4.6 b**).

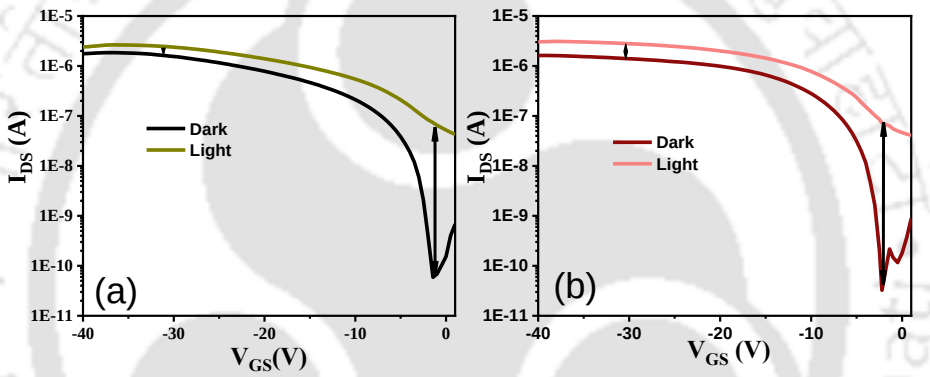


Figure 4.7: Transfer characteristic of the (a) Control and (b) BN modified PTB7-Th based PT in the dark and under illumination.

However, during the positive voltage sweep, the device enters the depletion region and the semiconductor is depleted of mobile charges, leading to C_S in series with the parallel combination C_{ox} and C_{it} (inset of **Figure 4.6 b**). Hence, in the presence of a high trap density, the depletion capacitance will be very high compared to C_{ox}. Thus, the equivalent capacitance will not reduce, even in the positive voltage sweep.[37] As can be observed from **Figure 4.6 b**, the change of capacitance for BN modified device is highest with voltage sweep compared to IN and CN based devices. Hence the CV analysis further proves that least trap density is present in BN-modified device.

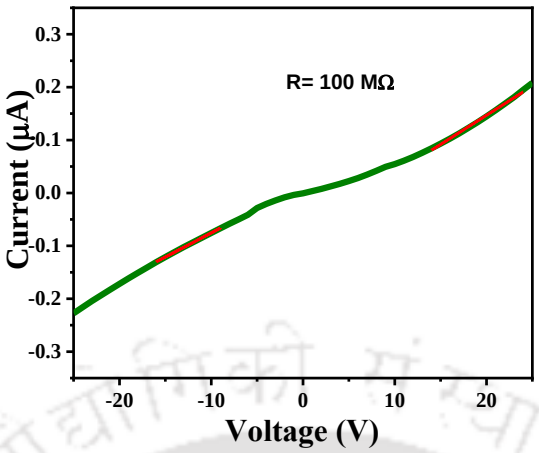


Figure 4.8: Current Vs. voltage curve of PEDOT:PSS.

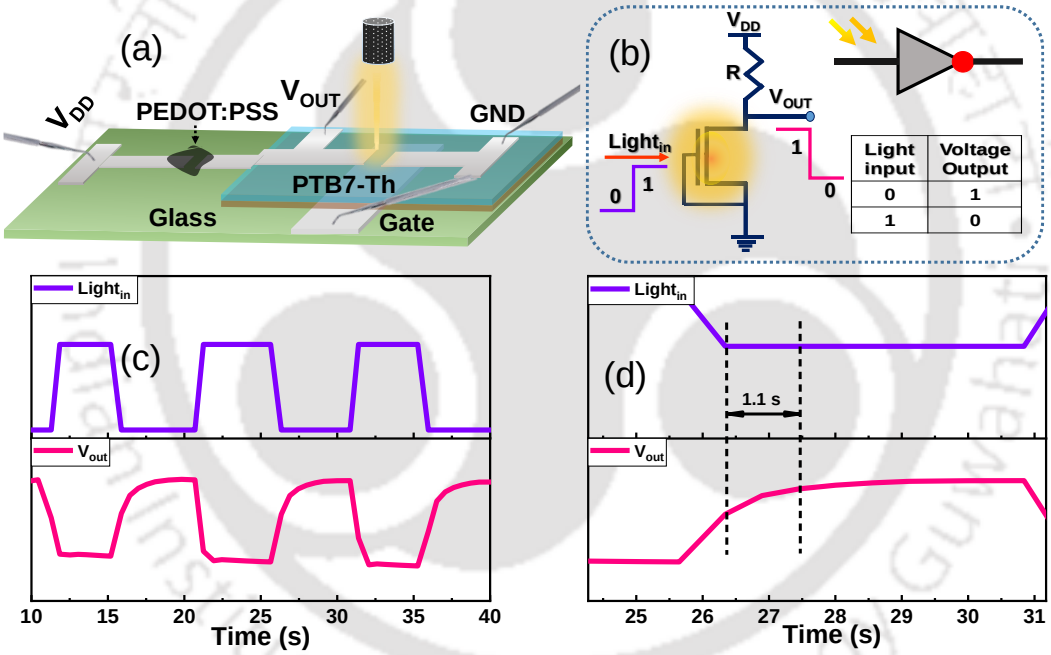


Figure 4.9: (a) Schematic showing the measurement of the opto-inverter circuit; (b) symbolic representation of the inverter circuit, NOT gate symbol and the truth table; (c) The change of the output voltage in response to the light pulse as a function of time; (d) rise time delay.

BN modified OFET is further utilized in studying the light sensitivity and its application as a PT (**Figure 4.7**) after confirming its optimum morphology, molecular ordering, stability, charge transport and trapping. The BN modified device was observed to show better light sensitivity of $3x10^3$ compared to $1x10^3$ control device which is also in agreement with the increased UV-Vis absorbance spectra. The improved absorbance can be related to the better

sensitivity to light or increased formation of light generated excitons and hence increased availability of charges resulting in increase in current.[38] Thereafter, to utilize the full potential and to check the viability of the PT as an electronic circuit component a simple resistive load opto-inverter is fabricated. To establish the inverter logic, the resistive load fabricated by drop casting PEDOT:PSS (current vs. voltage for calculating resistance of PEDOT:PSS is given in **Figure 4.8**) is connected with the PT as shown in **Figure 4.9 a**. The circuit design and the schematic representation of the working mechanism of the opto-electronic inverter are shown in **Figure 4.9 b**. The main drawback of a conventional resistive load logic gate circuit is the requirement of extra space and fabrication complexity of integrating an external resistor with the transistor.[39, 40] This complexity has been completely eliminated by this simple strategy of circuit design. The complete circuit, combination of OFET and PEDOT:PSS based resistive load, is solution processed and fabricated on the same substrate simultaneously. When a bias of V_{DD} = -10V is applied, the V_{OUT} can be shown as $V_{OUT} = V_{DD} - IR_1$, (where R_1 is the impedance across Resistive load and I is the circuit current). When the device is not illuminated i.e., the light input is LOW, the transistor is in OFF state and the resistance of the driving transistor (R_2) is high compared to the impedance of the load resistor (R_1). So, the voltage drop across the load resistor is ZERO, and the output voltage (V_{OUT}) is equivalent to V_{DD} (as $IR_1 \sim 0$). Next, when the device is illuminated, i.e., light input is HIGH, the charge accumulation starts and driver transistor will start conducting a non-zero current. This brings the transistor to ON state, and hence making the resistance of the transistor negligible compared to load resistor ($R_2 << R_1$). As a result, voltage drop across the load resistor increases pulling V_{OUT} to LOW state. Thus an inversion of the input in both cases is demonstrated, i.e., when light input is LOW, V_{OUT} is high, and when light input is HIGH, V_{OUT} is LOW. The truth table is shown in **Figure 4.9 b** and the results obtained are shown in **Figure 4.9 c**. The fall time is negligible as the V_{OUT} became LOW as soon as the light is turned on, however there is a delay observed during the rise of V_{OUT}. It took a delay of 1.1 s for the V_{OUT} to attain a HIGH state after the light is turned OFF as the light induced charges needs time to be swept out and completely turn off the transistor (**Figure 4.9 d**).

4.4 Conclusion

In summary, significant improvements in OFET performances have been demonstrated using the solvent additive technique leading to the application of a photo-active polymer-based phototransistor in a digital electronic circuit and as an opto-inverter. The comprehensive investigation of the effect of a series of aromatic (halonaphthalene) solvent reveals an improved active layer morphology with better crystallinity. The stability of the device also improves as the traps related to the disordered film were reduced. As a result, a significant improvement in the mobility of the PTB7-Th based OFET was observed. The present strategy of using solvent additives can also be extended to other solution-processed polymers as the working mechanism of additives is to improve the active layer morphology by optimizing the evaporation rate and controlling the arrangement of the polymer chain as well the crystallinity. Thereafter, BN-modified PT was used as an opto-inverter. These electronic circuit components can be further explored and implemented in light sensor arrays and in any electronic circuit which demands the use of a combination of logic gate and photo-transistor. This can reduce the number of components in a circuit thereby leading to compact designs. Hence this method of additive engineering and incorporation of RLIs will be very advantageous in terms of the implementation of the OFET based digital circuits.

References

1. C. Liu, F. Dai, B. Liu, H. Wei, P. Chen, Y. Hu, J. Wu and C. Liu, *Adv. Electron. Mater.*, 2021, **7**, 2001134.
2. X. Fang, J. Shi, X. Zhang, X. Ren, B. Lu, W. Deng, J. Jie and X. Zhang, *Adv. Funct. Mater.*, 2021, **31**, 2100237.
3. Z. Li, Y. J. Jeong, J. Hong, H.-j. Kwon, H. Ye, R. Wang, H. H. Choi, H. Kong, H. Hwang, S. H. Kim and X. Tang, *ACS Appl. Mater. Interfaces*, 2022, **14**, 7073-7081.
4. K. J. Baeg, D. Khim, J. Kim, D. Y. Kim, S. W. Sung, B. D. Yang and Y. Y. Noh, *IEEE Electron Device Lett.*, 2013, **34**, 126-128.
5. A. S. Sharova and M. Caironi, *Adv. Mater.*, 2021, **33**, 2103183.
6. C.-K. Chen, Y.-C. Lin, S. Miyane, S. Ando, M. Ueda and W.-C. Chen, *ACS Appl. Polym. Mater.*, 2020, **2**, 3422-3432.
7. A. Choudhury, R. K. Gupta, R. Garai and P. K. Iyer, *Adv. Mater. Interfaces*, 2021, **8**, 2100574.
8. A. Dey, A. Singh, D. Dutta, S. S. Ghosh and P. K. Iyer, *J. Mater. Chem. A*, 2019, **7**, 18330-18337.
9. Y. Zang, D. Huang, C.-a. Di and D. Zhu, *Adv. Mater.*, 2016, **28**, 4549-4555.
10. Q. Liu, S. E. Bottle and P. Sonar, *Adv. Mater.*, 2020, **32**, 1903882.
11. S. G. Surya, S. S. Nagarkar, S. K. Ghosh, P. Sonar and V. Ramgopal Rao, *Sens. Actuators B: Chem.*, 2016, **223**, 114-122.
12. F. Wu, Y. Liu, J. Zhang, S. Duan, D. Ji and H. Yang, *Small Methods*, 2021, **5**, 2100676.
13. C. Wang, X. Zhang, H. Dong, X. Chen and W. Hu, *Adv. Energy Mater.*, 2020, **10**, 2000955.
14. M. Hossain, M. A. Afroz, R. Garai and P. K. Iyer, *Sustain. Energy Fuels.*, 2021, **5**, 874-879.
15. A. Choudhury, R. K. Gupta, R. Garai and P. K. Iyer, *ACS Appl. Electron. Mater.*, 2021, **3**, 5393-5401.
16. R. K. Gupta, R. Garai, M. Hossain, M. A. Afroz, D. Kalita and P. K. Iyer, *J. Mater. Chem. C*, 2021, **9**, 8746-8775.

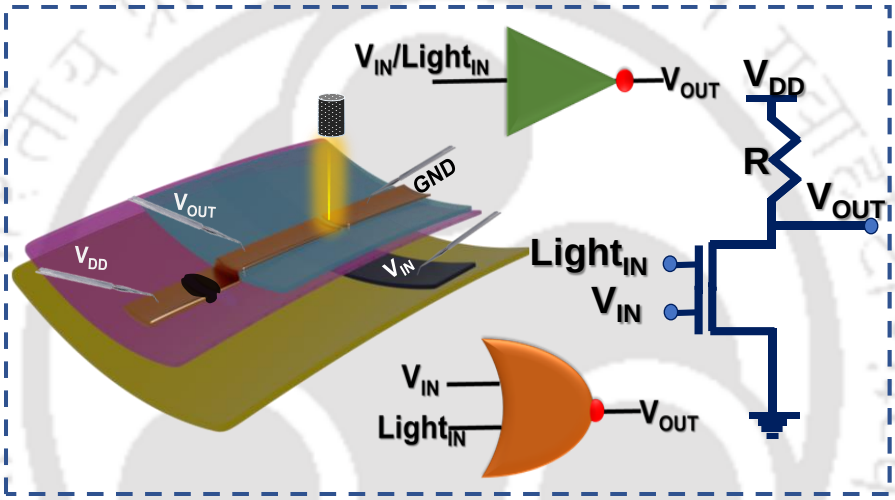
17. J. Yuan, Y. Xu, G. Shi, X. Ling, L. Ying, F. Huang, T. H. Lee, H. Y. Woo, J. Y. Kim, Y. Cao and W. Ma, *J. Mater. Chem. A*, 2018, **6**, 10421-10432.
18. R. K. Gupta, R. Garai, M. A. Afroz and P. K. Iyer, *J. Mater. Chem. C*, 2020, **8**, 8191-8198.
19. K. Patrikar, N. Jain, D. Chakraborty, P. Johari, V. R. Rao and D. Kabra, *Adv. Funct. Mater.*, 2019, **29**, 1805878.
20. R. Garai, M. Adil Afroz, R. K. Gupta, A. Choudhury and P. K. Iyer, *ACS Omega*, 2020, **5**, 2747-2754.
21. Y. Qian, W. Li, W. Li, X. Xu, Z. Lin, L. Xie, M. Yi and W. Huang, *Adv. Electron. Mater.*, 2015, **1**, 1500230.
22. K. Pei, X. Ren, Z. Zhou, Z. Zhang, X. Ji and P. K. L. Chan, *Adv. Mater.*, 2018, **30**, 1706647.
23. Q. Shi, D. Liu, S. Dai and J. Huang, *Adv. Opt. Mater.*, 2021, **9**, 2100654.
24. Y. T. Lee, J.-H. Kang, K. Kwak, J. Ahn, H. T. Choi, B.-K. Ju, S. H. Shokouh, S. Im, M.-C. Park and D. K. Hwang, *ACS Photonics*, 2018, **5**, 4745-4750.
25. J. Li, Y. H. Yang, W. H. Fu, Q. Chen, D. L. Jiang, W. Q. Zhu and J. H. Zhang, *Mater. Today Phys.*, 2020, **15**, 100264.
26. H. Park, S. Yoo, J. Ha, J. Kim, H. J. Mun, T. J. Shin, J. C. Won and Y. H. Kim, *ACS Appl. Mater. Interfaces*, 2021, **13**, 30921-30929.
27. T. D. Anthopoulos, *Appl. Phys. Lett.*, 2007, **91**, 113513.
28. B. Sun, T. Guo, G. Zhou, S. Ranjan, Y. Jiao, L. Wei, Y. N. Zhou and Y. A. Wu, *Mater. Today Phys.*, 2021, **18**, 100393.
29. S. F. Hoefler, T. Rath, N. Pastukhova, E. Pavlica, D. Scheunemann, S. Wilken, B. Kunert, R. Resel, M. Hobisch, S. Xiao, G. Bratina and G. Trimmel, *J. Mater. Chem. A*, 2018, **6**, 9506-9516.
30. J. Tang, J. Ji, R. Chen, Y. Yan, Y. Zhao and Z. Liang, *Adv. Sci.*, 2022, **9**, 2103646.
31. A. Kalita, A. Dey and P. K. Iyer, *Phys. Chem. Chem. Phys.*, 2016, **18**, 12163-12168.
32. M. J. Han, M. McBride, B. Risteen, G. Zhang, B. V. Khau, E. Reichmanis and D. K. Yoon, *Chem. Mater.*, 2020, **32**, 688-696.

33. P.-H. Chu, N. Kleinhenz, N. Persson, M. McBride, J. L. Hernandez, B. Fu, G. Zhang and E. Reichmanis, *Chem. Mater.*, 2016, **28**, 9099-9109.
34. R. Noriega, J. Rivnay, K. Vandewal, F. P. V. Koch, N. Stingelin, P. Smith, M. F. Toney and A. Salleo, *Nat. Mater.*, 2013, **12**, 1038-1044.
35. Y.-Q. Zheng, Z.-F. Yao, J.-H. Dou, Y. Wang, W. Ma, L. Zou, S. Nikzad, Q.-Y. Li, Z.-H. Sun, Z.-A. Yu, W.-B. Zhang, J.-Y. Wang and J. Pei, *Giant*, 2021, **7**, 100064.
36. A. Campos, S. Riera-Galindo, J. Puigdollers and M. Mas-Torrent, *ACS Appl. Mater. Interfaces*, 2018, **10**, 15952-15961.
37. A. Wang, I. Kymissis, V. Bulovic and A. I. Akinwande, *IEEE Trans Electron Devices*, 2006, **53**, 9-13.
38. H. Kim, Z. Wu, N. Eedugurala, J. D. Azoulay and T. N. Ng, *ACS Appl. Mater. Interfaces*, 2019, **11**, 36880-36885.
39. S. Rahi, V. Raghuwanshi, P. Saxena, G. Konwar and S. P. Tiwari, *IEEE Trans Electron Devices*, 2022, DOI: 10.1109/TED.2022.3148700, 1-7.
40. D. K. Hwang, C. Fuentes-Hernandez, J. B. Kim, W. J. Potscavage and B. Kippelen, *Org. Electron.*, 2011, **12**, 1108-1113.

[This page was intentionally left blank]

Chapter 5

Solution-Processed Flexible Circuit Design for Dual Input Logic Gates



Manuscript: Anwesha Choudhury, Ritesh Kant Gupta, Rabindranath Garai, Parameswar Krishnan Iyer, "Solution Processable Flexible Circuit Design for Dual Input Opto-Electrical Logic Gates."

[This page was intentionally left blank]

Abstract

Dual input inverter and the NOR logic are demonstrated utilizing a simple circuit design which consists of two components, a phototransistor and a resistor. Both the components are solution-processed and fabricated simultaneously on a flexible polyimide substrate. An optimized PTB7-Th p-type OFET with high mobility of 0.45 cm^2 V^{-1} s^{-1} and a very low threshold voltage of 2 V along with PEDOT:PSS as the drop-casted resistor helped to attain the efficient logic gates. A high noise immunity upto ~98% and a gain of 12.5 are obtained for the inverter. The resistive load inverter operation is established with both light and voltage as input signal and then a single transistor NOR gate is also demonstrated on simultaneous application of both inputs.

5.1 Overview

Polymers are a promising class of materials for electronic and optoelectronic devices as they offer invaluable advantages like low cost, low temperature, solution processing. Considering the current demand for flexible, wearable, and large-area electronic devices, the solution processable polymers has been one of the best choices.[1-4] However, the mobility of solution processed thin films is limiting its usage in commercial applications requiring high frequency operation.[5-9] But for the basic circuits in optical communication, smart tags, flexible display sensors, disposable memories, the flexible, solution processed logic gates are a perfect fit.[10,11] Though polymer OFET based logic gates have recently gained attention and several research groups have reported the use of flexible circuits, yet reports on opto logic gates, image sensors are very rare and no reports on simultaneous dual input (both electrical and optical) logic gates are known.[12-14] Also the focus was on developing complementary OFETs for logic circuits and the simple resistive load circuit design which was neglected as it possess many demerits like the requirement of extra space, integration complexity, requirement of external component and power loss.[15-17] As a result the resistive load design remains less explored overlooking the ease of fabrication that the circuit provides. For a complementary circuit two different transistors need to be optimized and fabricated which is quite difficult and complicated.[18,19] Also, for applications that require combined functionality of light dependent decision making or switching, a resistive load opto logic gate can simplify the circuit further by reducing the number of components. Thus, for advanced applications requiring more than a unit photodetector device, the opto logic gate provides a simple and low cost alternative.

In this work, a completely solution processed phototransistor (PT) is fabricated, and is utilized to demonstrate various flexible logic gates. PTB7-Th is used as the active layer because of its high photo response and the ability to form superior thin film morphology by solution processing. The OFET used is highly optimized and showed a mobility of 0.45 $cm^2 V^{-1} s^{-1}$ and a low threshold of ~2V. PEDOT:PSS was drop casted to obtain a resistance of 100 MΩ. By using the optimized PT and the resistor, high performance resistive load inverters were then fabricated without the use of any external circuit component. Further, the dual input i.e., electrical and light input functionality of the inverter was demonstrated. The opto-inverter showed a slight propagation delay of ~0.06 s. Finally, a single transistor NOR gate

was also successfully demonstrated by simultaneous use of both light and electrical input signals.

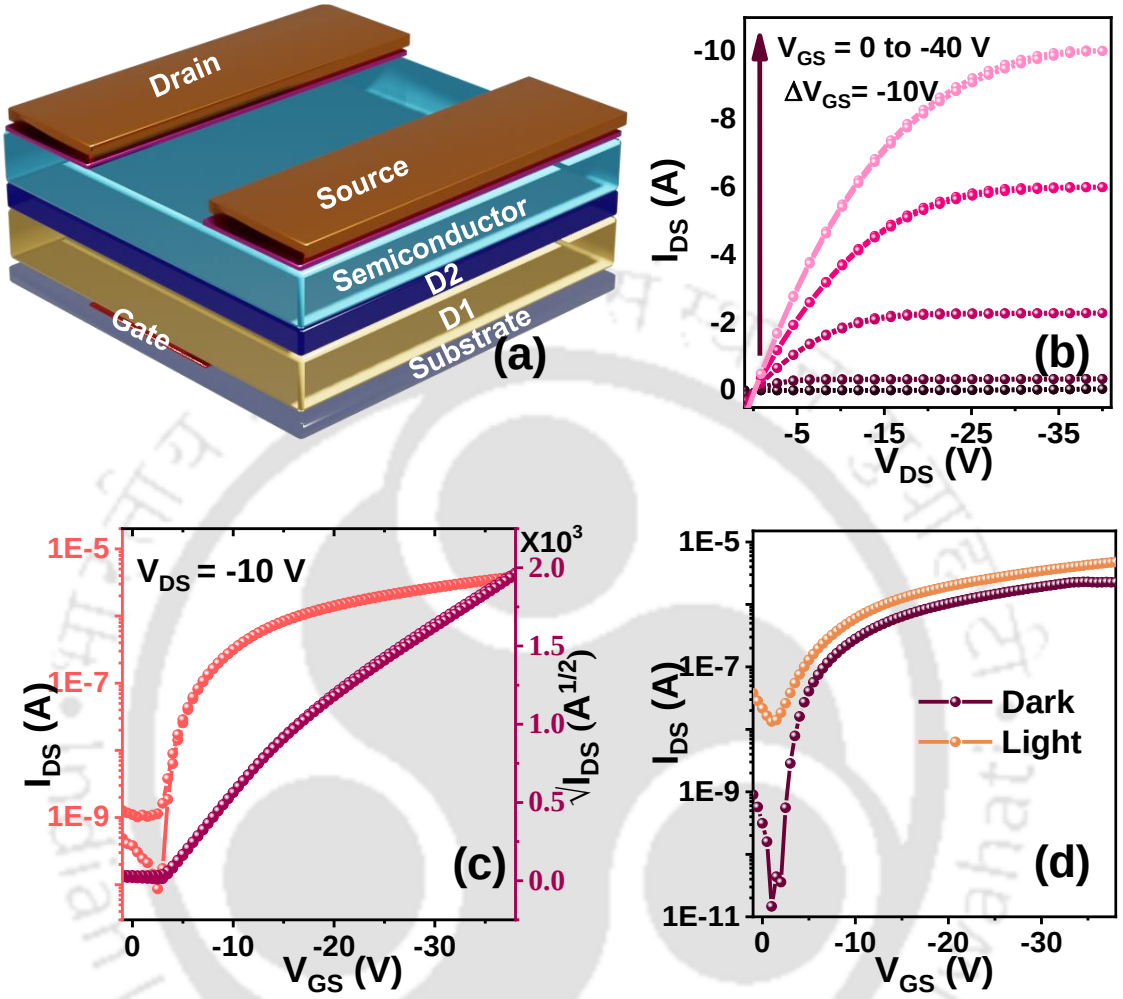


Figure 5.1: (a) Device architecture. (b) Output characteristics at V_{GS} = 0 to -40 V, (c) transfer characteristics at V_{DS} = -10 V and transfer characteristic showing (d) the light response.

5.2 Experimental Section

5.2.1 Materials

PTB7-Th was thermally synthesized according to the previous literature.[20] Poly(methyl methacrylate) (PMMA) (average Mw ~996 kDa), 1-bromonaphthalene (BN), Molybdenum(VI) oxide, and Aluminium (Al) and Copper (Cu) wire were purchased from Sigma Aldrich, Poly(3,4-ethylene dioxythiophene)-poly(styrene sulfonate) (PEDOT:PSS,

PVP AI 4083) was bought from Clevios and polyvinyl alcohol (PVA) (average Mw ~ 115 kDa) from Loba Chemicals and used without further purification.

5.2.2 Device Fabrication

Polyimide (PI) substrates were cleaned in ultrasonic bath in isopropanol, acetone, de-ionized water successively for 15 min each and dried before depositing the Al gate. 100 mg/mL solution of PVA in DI water was prepared and spin coated with 1000 rpm for 30 secs on the gate deposited substrate and dried at 100 ^{o}C for 1 hour to form 1 µm thick layer. PVA acts as the first dielectric in all three OFETs, over which a 100 nm (3000 rpm 30 sec) thick second dielectric layer (PMMA) is coated and dried at 100 ^{o}C for 1 hour and 60 nm thick polymer semiconductor layer was spin coated. Finally, for the top contact 5 nm of MoO_x and 60 nm of Copper were thermally deposited using shadow masking to form a channel of length (L) 40 µm and width (W) 0.8 mm. All the fabrication processes were done in ambient condition. For semiconductor layer spin coating, an optimized concentration of 1.5% v/v of the solvent additive, BN was added and kept on stirring for 10 min more. Similar device fabrication and optimization in details is given in our previous publication. [21, 22]

For the resistive load, the drain electrode was extended, and a channel of 100 µm was made by shadow masking simultaneously during the source-drain deposition. After deposition of the metal electrode, PEDOT:PSS was drop cast on the 100 µm channel and vacuum dried for 10 hours before starting measurement. A Tektronix arbitrary function generator AFG1062 was used to generate the pulses for voltage input.

5.2.3 Characterization

The thickness of the thin films was measured using Dektek 150 stylus profiler. The AFM images were recorded in tapping mode on an Agilent 5500 AFM/SPM microscope to avoid tip surface interaction causing any film damage. All electrical characterizations were performed using a Keithley 4200 SCS parameter analyzer under vacuum conditions. For the phototransistor and opto-inverter measurements, an Oriel DC regulated illuminator of 0.37 W m^{-2} power and wavelength in the range of 550-800 nm was used. For UV-Vis, a Shimadzu UV 2600 UV-Vis spectrophotometer, for PL measurements, a Horiba Fluoromax-4 spectrofluorometer was used, and for XRD, a Rigaku X-ray diffractometer was used.

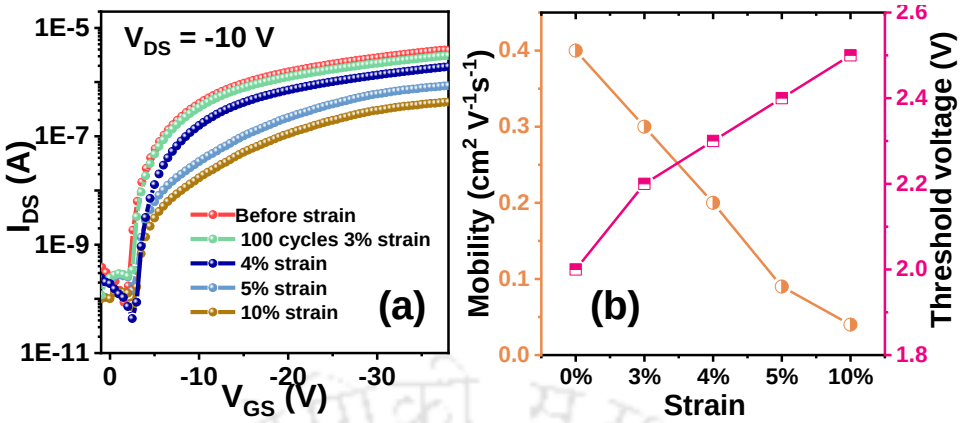


Figure 5.2: The effect of bending in (a) the transfer characteristic and (b) the calculated mobility and threshold voltage.

5.3 Results and Discussions

The device architecture is shown in the inset of **Figure 5.1 a**. A bilayer dielectric system is used where first dielectric (D1) is PVA and second dielectric (D2) is PMMA. The optimization for the presented architecture is done our previous work.[21,22] The output and transfer characteristics of the OFET (**Figure 5.1 b, c**) do not show any hysteresis indicating completely optimized devices.

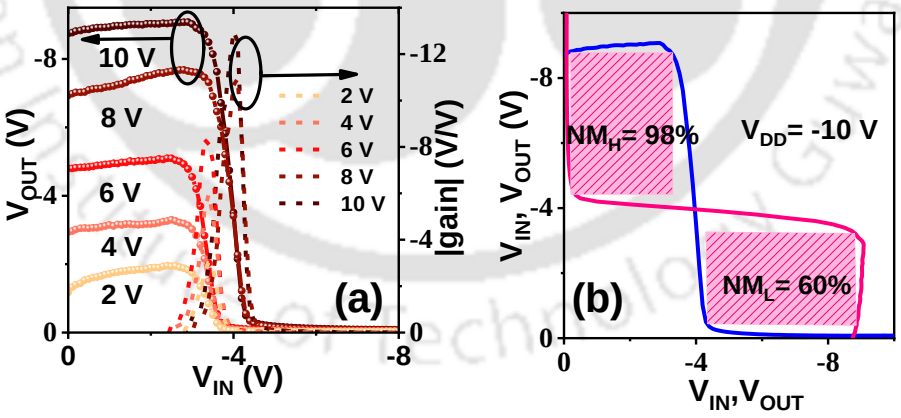


Figure 5.3: (a) Voltage transfer characteristics (VTC) at V_{DD} =-2 to, -10 V and the corresponding gains and (b) noise margin calculated from the VTC at V_{DD}= -10V for the device before subjecting to any strain.

A mobility of 0.45 cm^2 V^{-1} s^{-1}, V_{TH} of ~2 V and I_{ON}/I_{OFF} of 10^5 was obtained. The photo response was measured and the PTB7-Th based PT showed a high photo-response of 688 A/W (**Figure 5.2 a**). Thereafter the flexibility of the devices was tested by applying

mechanical strain. The change in the transistor properties with varying strain levels is recorded (**Figure 5.3 a**). A small change in threshold voltage from 2 V to 2.5 V and mobility reduction from 0.45 cm^2 V^{-1} s^{-1} to 0.30 cm^2 V^{-1} s^{-1} is observed. The voltage transfer characteristics (VTCs) of the flexible resistive load inverter at different V_{DD} and the corresponding gain are plotted in **Figure 5.3 a.** A very high gain of 12.5 is obtained at V_{DD}= -10 V. A noise margin of NM_H 98% and NM_L 60% is obtained at V_{DD} = -10 V (**Figure 5.3 b**).

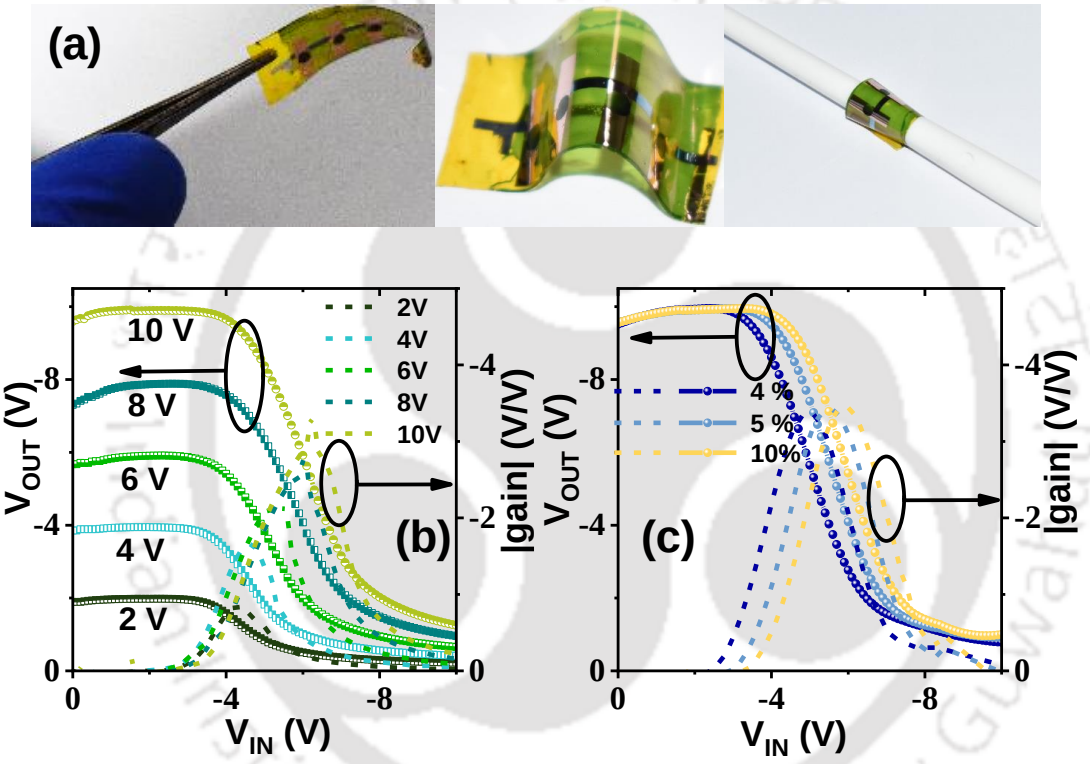


Figure 5.4: (a) Images of the flexible devices fabricated on PI substrate. (b) VTC at V_{DD} =-2 to, -10 V and the corresponding gains, (c) VTC at different recorded after applying different strains and the corresponding gains.

The photograph of the flexible device are shown in **Figure 5.4 a.** After 100 bending cycles at strain of 3%, a slight increase in the threshold voltage is observed, however with further increase in strain from 4% to 10% negligible change in threshold voltage and mobility is observed as obtained from **Figure 5.2 b**. The gain also reduced to ~3.5 after strain of 3% for 100 cycles (**Figure 5.4 b**). The inversion voltage (V_{inv}) changed slightly from 4.5 V to 5 V which is attributed to the increase in threshold with the application of strain. However, when the strain was further increased, there was negligible increase in V_{inv} and a similar gain

of ~3.5 is obtained even at a high stress of 10 % as shown in **Figure 5.4 c**

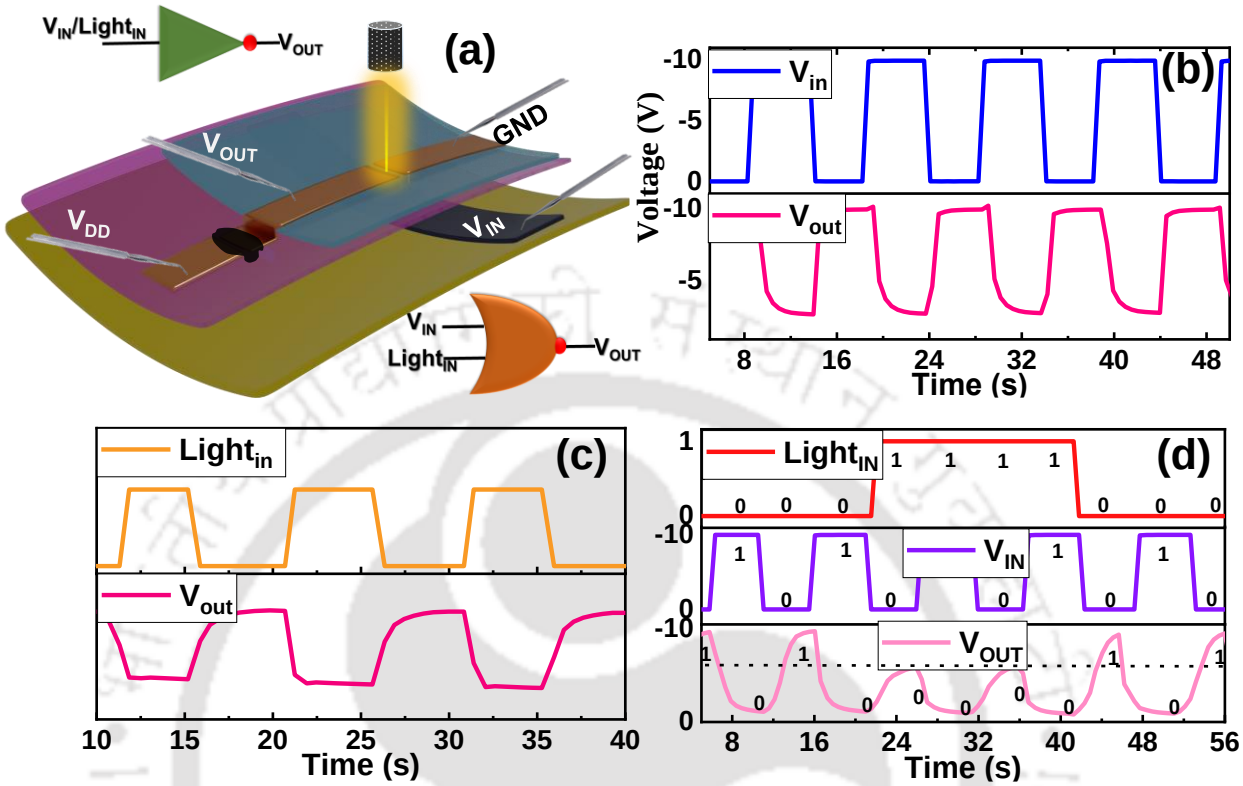


Figure 5.5: (a) The schematic of the working and circuit of flexible opto-electronic logic gates and the circuit symbol of the NOT and NOR logic gates. The voltage output in response to input (b) voltage pulse and (c) light pulse with respect to time. (d) The voltage output of NOR gate with simultaneous application of both light input and voltage input signals.

After confirming the high performance and mechanical stability of the resistive load flexible inverter, the working of the opto-inverter was established by applying a light pulse as the input signal. The schematic showing the operation of the opto-electronic inverter is shown in (**Figure 5.5 a**). The inverter was first characterized by applying input voltage pulse and a small delay of 0.06 s was observed (**Figure 5.5 b**). Then a light pulse at 1 Hz frequency was applied and for the opto inverter a minimal delay of 0.06 s in rise time and 0.1 s in fall time are obtained (**Figure 5.5 c**). The PT recovery time is a bit higher than its response time and hence the inverters rise time > fall time. For demonstrating a two input NOR logic, both the electrical and optical inputs are applied simultaneously. In case if any of the inputs is high, the PT starts conducting and the output voltage obtained is low. The output voltage is high only when both the inputs are low, resulting in the demonstration of the NOR logic

(**Figure 5.5 d**). For establishing the NOR logic -10 V is treated as the logic '1' and below -5 V is treated as the logic '0' for the output. Since the delay in the phototransistor recovery has a bit higher, logic '0' shifted from 0 V to -5 V for an operational frequency of 1 Hz. This can be further improved by reducing recovery time of the PT.

5.4 Conclusion

In summary, a complete solution processed dual input logic gate circuit is demonstrated on ultra-flexible PI substrate. The circuit consisted of a PT with high mobility of 0.45 $cm^2\ V^{-1}\ s^{-1}$ and responsivity of 688 A/W. The PT is integrated with a simple drop casted resistive load. This simple circuit design showed comparable performance with the complementary OFET based circuits. The opto-electrical inverter showed a NM_L of 60% and NM_H of 98%. The delay for the voltage pulse input was 0.12 s and for light input was 0.16 s. Thereafter, both electrical and optical inputs were applied simultaneously and dual input NOR logic was demonstrated.

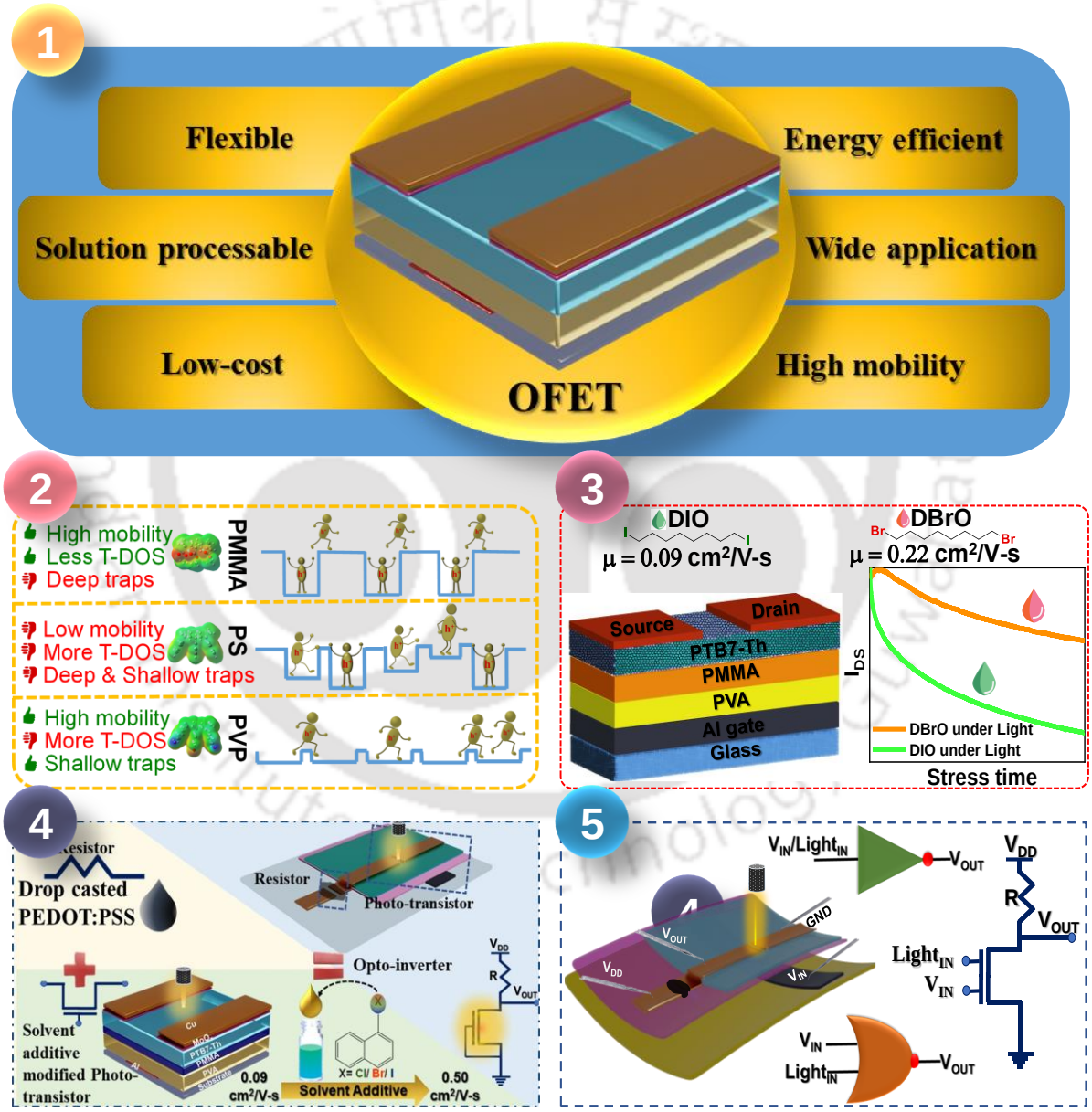
References

1. H. Sirringhaus, *Adv. Mater.*, 2005, **17**, 2411-2425.
2. R. C. G. Naber, C. Tanase, P. W. M. Blom, G. H. Gelinck, A. W. Marsman, F. J. Touwslager, S. Setayesh and D. M. de Leeuw, *Nat. Mater.*, 2005, **4**, 243-248.
3. A. A. Boampong, J. H. Cho, Y. Choi and M. H. Kim, *Adv. Electron. Mater.*, 2021, **7**, 2100430.
4. M. Higashinakaya, T. Nagase, H. Abe, R. Hattori, S. Tazuhara, T. Kobayashi and H. Naito, *Appl. Phys. Lett.*, 2021, **118**, 103301.
5. G. Gelinck, P. Heremans, K. Nomoto and T. D. Anthopoulos, *Adv. Mater.*, 2010, **22**, 3778-3798.
6. W. Tang, Y. Huang, L. Han, R. Liu, Y. Su, X. Guo and F. Yan, *J. Mater. Chem. C*, 2019, **7**, 790-808.
7. A. Perinot, B. Passarella, M. Giorgio and M. Caironi, *Adv. Funct. Mater.*, 2020, **30**, 1907641.
8. A. Yamamura, T. Sakon, K. Takahira, T. Wakimoto, M. Sasaki, T. Okamoto, S. Watanabe and J. Takeya, *Adv. Funct. Mater.*, 2020, **30**, 1909501.
9. H.-I. Un, J.-Y. Wang and J. Pei, *Adv. Sci.*, 2019, **6**, 1900375.
10. J. H. Cho, J. Lee, Y. Xia, B. Kim, Y. He, M. J. Renn, T. P. Lodge and C. Daniel Frisbie, *Nat. Mater.*, 2008, **7**, 900-906.
11. J. Smith, A. Bashir, G. Adamopoulos, J. E. Anthony, D. D. C. Bradley, M. Heeney, I. McCulloch and T. D. Anthopoulos, *Adv. Mater.*, 2010, **22**, 3598-3602.
12. Y. T. Lee, J.-H. Kang, K. Kwak, J. Ahn, H. T. Choi, B.-K. Ju, S. H. Shokouh, S. Im, M.-C. Park and D. K. Hwang, *ACS Photonics*, 2018, **5**, 4745-4750.
13. T. D. Anthopoulos, *Appl. Phys. Lett.*, 2007, **91**, 113513.
14. K. J. Baeg, D. Khim, J. Kim, D. Y. Kim, S. W. Sung, B. D. Yang and Y. Y. Noh, *IEEE Electron Device Lett.*, 2013, **34**, 126-128.
15. S. Rahi, V. Raghuwanshi, P. Saxena, G. Konwar and S. P. Tiwari, *IEEE Trans. Electron Devices*, 2022, DOI: 10.1109/TED.2022.3148700, 1-7.
16. D. K. Hwang, C. Fuentes-Hernandez, J. B. Kim, W. J. Potscavage and B. Kippelen, *Org. Electron.*, 2011, **12**, 1108-1113.

17. M. Jea, A. Kumar, H. Cho, D. Yang, H. Shim, A. K. Palai and S. Pyo, *J. Mater. Chem. C*, 2014, **2**, 3980-3987.
18. H. Park, S. Yoo, J. Ha, J. Kim, H. J. Mun, T. J. Shin, J. C. Won and Y. H. Kim, *ACS Appl. Mater. Interfaces*, 2021, **13**, 30921-30929.
19. Y. Yan, Y. Zhao and Y. Liu, *J. Polym. Sci.*, 2022, **60**, 311-327.
20. R. Garai, M. Adil Afroz, R. K. Gupta, A. Choudhury and P. K. Iyer, *ACS Omega*, 2020, **5**, 2747-2754.
21. A. Choudhury, R. K. Gupta, R. Garai and P. K. Iyer, *Adv. Mater. Interfaces*, 2021, **8**, 2100574.
22. A. Choudhury, R. K. Gupta, R. Garai and P. K. Iyer, *ACS Appl. Electron. Mater.*, 2021, **3**, 5393-5401.

Chapter 6

Summary and Prospects



[This page was intentionally left blank]

6.1 Summary

Due to the growing demand for flexible, low-cost electronic circuits, the motivation of the work was to develop a solution-processable organic field-effect transistor (OFET) for implementation in flexible circuits. The significant challenges in solution-processable OFET are the poor dielectric/semiconductor (d/s) interface and the quality of the semiconductor thin film. This thesis mainly focuses on improving the understanding of these challenges, which will aid enhancing the device performance. First, the d/s interface is studied which is followed by improving the semiconductor morphology. Once the desired semiconductor morphology was achieved, flexible and solution-processed integrated circuit was implemented.

The first chapter of this thesis introduced the basic concept of a transistor, the need for energy-efficient processing techniques of electronic circuits, the basic working and architectures of OFET, the performance defining parameters, different interfaces present in the device, their importance in determining the device performance, and the choice of dielectric materials. The various techniques employed in this thesis to improve the device performance and the applications of solution-processed OFET for flexible circuits are also discussed.

In the second chapter, the d/s interfacial defect states are probed by employing impedance spectroscopy (IS) as a tool to improve the understanding of charge transport. A detailed study of morphology, photophysical property, and crystallinity of the semiconductor thin film is conducted. Also, electrostatic potential and contact of the dielectrics are studied to verify the understanding obtained from IS. Thus, it has been proved that IS can be effective in understanding the d/s interfacial defects and hence the charge transport of OFET.

The third chapter introduced solvent additive as a morphology modifier of the semiconductor. An improvement in device properties has been confirmed with the high quality films, and the results were established after fabricating three types of devices and comparing their properties. The three devices comprised of the control device (without any solvent additive) and the other two with the inclusion of two different solvent additives namely, 1,8-diiodooctane (DIO) and 1,8-dibromooctane (DBrO). It has been also observed

that along with mobility, the device stability improved as well in the dark and under light in the DBrO modified device. Hence the phototransistor properties were also studied, and high responsivity of 688 A/W was demonstrated.

Chapter four described the utilization of a series of halonaphthalene-based solvent additives to improve the device properties further. A ~5-fold improvement in mobility was obtained for 1-bromonaphthalene modified device. After that, an optoelectronic inverter logic is demonstrated by integrating the phototransistor with a solution-processed resistor.

In chapter five, the understanding and improvement of OFET device properties as obtained from the previous chapters are utilized to demonstrate an optoelectronic NOT and NOR logic. Not just a unit device, but a complete circuit is fabricated by solution processing. A very efficient, ultra-flexible opto inverter and an opto NOR logic on polyimide substrate were demonstrated. First, the inverter circuit parameters were defined, and then dual-gate measurements were presented.

6.2 Prospects

Understanding trap density of states (T-DOS) can help in achieving better charge transport and improving the stability and reproducibility of the device. Various experimental and analytical methods comprising optical, electrical, and thermal measurement tools have been reported to estimate the DOS. The impedance spectroscopy techniques used in this thesis for understanding the d/s interface will help to analyze poor OFET properties arising from d/s interfacial defects and, hence, will significantly contribute to developing new semiconductor and dielectric materials compatible with each other and allowing defect-free charge transport in OFET.

Low mobility and stability are the two crucial factors hindering the progress of organic electronic circuits. In the last few years, molecular engineering has facilitated many organic materials to exhibit a tremendous improvement in performance. Especially, donor-acceptor (D-A) materials have shown high mobility and enhanced stability. Basic circuits like sensors, memory smart tags, and driving circuits for appearing displays can be easily implemented. However, when it comes to high-end applications of flexible microprocessors, they still lag behind. By combining material engineering and device engineering, the

performance of these devices can be further improved, which will make their implementation even in high-end applications possible. As demonstrated in this thesis, the morphology modification by introducing solvent additive can be combined with other device engineering and material engineering to further improve the performance.

The resistive load inverter circuit demonstrated in this thesis is entirely solution-processed. Hence, printing can be easily implemented for the same circuit design, allowing energy-efficient printable electronic circuits to be developed. Moreover, both electrical and light input can be applied in the demonstrated circuit design and so this design can reduce the number of components used and the complexity of any circuit which requires a combined functionality of a photodetector and a logic gate. Demonstration of the universal NOR gate allows implementation of other logic gates possible through simple solution-processed and printing techniques.

In summary, the research work presented in this thesis first develops an understanding on the solution-processed d/s interface and its impact on charge transport and device properties using IS as a tool. Then it improves the device properties by introducing the solvent additive technique and finally implements the improved device for a solution-processed flexible integrated circuit.

[This page was intentionally left blank]

Outcomes

Publications

(1) **Choudhury, A.;** Gupta, R. K.; Garai, R.; Iyer, P. K. Solution Processed Flexible Circuit Design for Dual Input Logic Gates (Under Review)

(2) **Choudhury, A.;** Gupta, R. K.; Garai, R.; Iyer, P. K. Engineering Semiconductor Layer Using Halonaphthalene Additives for Organic Opto-Inverter Circuits. *ACS Appl. Electron. Mater.* **2022**, DOI: 10.1021/acsaelm.2c01272.

(3) **Choudhury, A**.; Gupta, R. K.; Garai, R.; Iyer, P. K. Tuning Polymer Semiconductor Morphology through Additive Engineering for a Stable Phototransistor. *ACS Appl. Electron. Mater.* **2021,** *3* (12), 5393-5401, DOI: 10.1021/acsaelm.1c00873.

(4) **Choudhury, A.;** Gupta, R. K.; Garai, R.; Iyer, P. K. Tailoring Trap Density of States through Impedance Analysis for Flexible Organic Field-Effect Transistors. *Adv. Mater. Interfaces* **2021,** *8* (15), 2100574, DOI: https://doi.org/10.1002/admi.202100574.

(5) Garai, R.; Gupta, R. K.; **Choudhury, A**.; Iyer, P. K. Triple Passivation Approach to Laminate Perovskite Layers for Augmented UV and Ambient Stable Photovoltaics. *ACS Appl. Energy Mater.* **2022,** *5* (3), 3392-3400, DOI: 10.1021/acsaem.1c03997.

(6) Gupta, R. K.; Garai, R.; Hossain, M.; **Choudhury, A.;** Iyer, P. K. Halide Engineering for Mitigating Ion Migration and Defect States in Hot-Cast Perovskite Solar Cells. *ACS Sustainable Chem. Eng.* **2021,** *9* (23), 7993-8001, DOI: 10.1021/acssuschemeng.1c02537.

(7) Das, S.; **Choudhury, A**.; Mandal, A.; Kumar, C.; Ranjan Sahoo, S.; Bedi, A.; Shekhar Karmakar, H.; Gopal Ghosh, N.; Dey, S.; Krishnan Iyer, P.; Bhattacharyya, S.; Zade, S. S. An unconventional route to an ambipolar azaheterocycle and its in situ generated radical anion. *Org. Biomol. Chem* **2021,** *19* (23), 5114-5120, DOI: 10.1039/D1OB00826A.

(8) Mondal, S.; Zehra, N.; **Choudhury, A**.; Iyer, P. K. Wearable Sensing Devices for Point of Care Diagnostics. *ACS Appl. Bio Mater.* **2021,** *4* (1), 47-70, DOI: 10.1021/acsabm.0c00798.

(9) Bhanvadia, V. J.; **Choudhury, A**.; Iyer, P. K.; Zade, S. S.; Patel, A. L. Constructing fused bis-isatins from pyrroloindoles using direct oxidation approach and re-visiting indophenine reaction. *Polymer* **2020,** *210*, 123032, DOI: https://doi.org/10.1016/j.polymer.2020.123032.

(10) Mandal, A.; **Choudhury, A.**; Sau, S.; Iyer, P. K.; Mal, P. Exploring Ambipolar Semiconductor Nature of Binary and Ternary Charge-Transfer Cocrystals of Triphenylene, Pyrene, and TCNQ. *J. Phys. Chem. C* **2020,** *124* (12), 6544-6553, DOI: 10.1021/acs.jpcc.0c00426.

(11) Garai, R.; Adil Afroz, M.; Gupta, R. K.; **Choudhury, A**.; Iyer, P. K. High-Performance Ambient-Condition-Processed Polymer Solar Cells and Organic Thin-Film Transistors. *ACS Omega* **2020,** *5* (6), 2747-2754, DOI: 10.1021/acsomega.9b03347.

(12) Mandal, A.; **Choudhury, A**.; Iyer, P. K.; Mal, P. Charge Transfer Versus Arene–Perfluoroarene Interactions in Modulation of Optical and Conductivity Properties in Cocrystals of 2,7-Di-tert-butylpyrene. *J. Phys. Chem. C* **2019,** *123* (30), 18198-18206, DOI: 10.1021/acs.jpcc.9b03827.

(13) Mandal, A.; **Choudhury, A**.; Kumar, R.; Iyer, P. K.; Mal, P. Exploring the semiconductor properties of a charge transfer cocrystal of 1-aminopyrene and TCNQ. *CrystEngComm* **2020,** *22* (4), 720-727, DOI: 10.1039/C9CE01507H.

(14) **Choudhury, A**.; Dogra, P.; Teron, B.; Gupta, R. K.; Dey, A.; Singh, A.; Garai, R.; Iyer, P. K. In *Morphology Control of Mixed Halide Perovskite for its Application in Low-cost Thin Film Transistor*, 2018 2nd IEEE International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES), 22-24 Oct. 2018; 2018; pp 743-747.

Book Chapter

(1) Gupta, R. K.; Arunagirinathan, R. N.; Afroz, M. A.; Garai, R.; **Choudhury, A**.; Hossain, M.; Yathirajula, R. B.; Iyer, P. K. Chapter 4 - Functional materials for various organic electronic devices. In *Chemical Solution Synthesis for Materials Design and Thin Film Device Applications*; Das, S.; Dhara, S., Eds.; Elsevier: 2021; pp 119-165.

Conferences & Workshops

(1) North-East Research Conclave Assam Biotech Conclave 2022. (NERC &ABC 2022) Indian Institute of Technology Guwahati, India, Science, Technology and Climate Change Dept.& Dept. of Education, Govt. of Assam May 20 - 22, 2022 (Oral presentation)

(2) International Symposium on Organic Iontronics for Sustainable Future organized by Materials Research Society of Japan (MRSJ) during December 13-15, 2021 (Oral Presentation)

(3) Online workshop on Research level understanding and hands-on Training on SCAPS-1D for the TCAD designing of solar cells organized by Chitkara University, Punjab during September 22-25, 2020.

(4) Participated in 6th National Workshop on MEMS/NEMS and Theranostic Devices (NWNTD2020) organized by Centre for Nanotechnology, IIT Guwahati, Assam during December 1-3, 2020.

(5) The 26th CRSI National Symposium in Chemistry (CRSI NSC-26), held in VIT Vellore during Feb. 7-9, 2020 (Poster Presentation)

(6) International Conference on Advanced Nanomaterials and Nanotechnology (ICANN2019), held at Indian Institute of Technology Guwahati, Assam during December 18-21, 2019 (Poster Presentation)

(7) International Conference on Advanced Nanomaterials and Nanotechnology (ICANN2017), held at Indian Institute of Technology Guwahati, Assam during December 18-21, 2017

Synopsis Report
on

Engineering Solution Processable Organic Field Effect Transistor for Opto-electronic Applications

Submitted By

Anwesha Choudhury

Roll No.: 176153007

under the supervision of

Prof. Parameswar Krishnan Iyer

Centre for Nanotechnology
Indian Institute of Technology Guwahati
Guwahati-781039, Assam, India

May 2022

Transistors are the basic building block of electronics and its development has revolutionized the field of electronic circuits. Further, the invention of conducting organic materials has added a new dimension to transistors and other electronic devices by paving the way for low cost, solution-processable, and flexible electronics. Polymers have been present in our daily life for ages and also in electronic devices as insulating materials. However, it was only in the late nineties that the outstanding discovery of oxidation enhanced the conductivity of polyacetylene opened up a new avenue of organic electronics. Since then, intense research and tremendous progress have been achieved by developing various organic materials, synthesis techniques, and device engineering approaches. Transistors based on polymer materials have now reported mobility >10 $cm^2 V^{-1} s^{-1}$ which is higher than amorphous silicon.[1-2] The optoelectronic properties of the organic materials can also be utilized to fabricate organic phototransistors, opto logic gates, and image sensors. Many organic electronic devices are already available in the market and become ubiquitous in our society. Organic field effect transistors (OFETs) lack mobility and stability compared to their inorganic counterparts which has allowed immense research to be carried out for achieving better device properties. However, the basic circuits in smart tags, driving matrix of flexible displays, radio frequency identification tags (RFID), etc., demand the use of low cost, large area, printed OFET based circuits.[3-5] Research is already in progress for OFET-based integrated circuits facilitating energy-efficient fabrication of electronic circuits.

For advanced electronics and the commercialization of OFETs-based electronic circuits, the two major hurdles are stability and mobility. A thorough understanding of transport properties and mechanisms is crucial for achieving high mobility and better stability. Improvement in charge transport in OFET can be achieved by improving the dielectric/semiconductor interface and semiconductor morphology. Most semiconductors are insoluble, including organic oligomers, until they are carefully functionalized to be soluble. However, this functionalization may hamper their carrier mobility. It is well known that organic polymers are typically more soluble and have better film-forming capability by solution processing techniques than small molecules. However, they can be modulated and improved by various methods. The fabrication or coating technique is crucial in forming a defect-free morphology and interfaces for solution-processed polymer thin films. These defects will lead to the device's instability and hamper the charge transport properties. Various experimental and analytical methods have been reported to estimate the DOS which includes optical, electrical and thermal measurement tools.[6-8] The scanning probe techniques are used to study

the T-DOS as the presence of trapped charges modifies the contact potential. Hence, this is reported as an efficient tool for determining the origin and spatial distribution of traps.[9-12] Some other experimental methods like space charge limited current (SCLC), thermal admittance spectroscopy (TAS), and driven level capacitance profiling (DLCP) method are also reported for single semiconductor layer trap study in solar cell study.[13-15] Analytical methods based on temperature dependence conductivity of OFET were used to determine the DOS spectrum as well.[16-17] Considering the current demand for flexible and energy-efficient electronic devices, improving mobility and stability has become one of the most important research topics as that ensures the implementation of OFET in different flexible circuit designs. The summarized mobility reported till date for PTB7-Th OFET are given in Table 1.

Table 1. Summarized literature on PTB7-Th based OFET.

Mobility, cm^2 /V-s	**Theme of the work**	**References**
1×10^{-2}	PTB7-Th molecular weight	18
1.4×10^{-1}	Effect of pendent group	19
2×10^{-2}, 1.3×10^{-1}	Thermal and Microwave synthesis	20
1.2×10^{-1}	Role of dielectric	21
2.2×10^{-1}	Effect of DIO and DBrO solvent additive	22 **(Part of thesis)**
5.0×10^{-1}	Effect of halonaphthalene based solvent additive	**Part of thesis**
5.0×10^{-1}	Flexible opto logic gate	**Part of thesis**

This thesis contains methods of improving the semiconductor/dielectric interface and semiconductor morphology to obtain high performance OFETs both in rigid and flexible substrates. Further, the OFETs have been utilized to develop photo-transistors and digital opto-logic gates. Chapter wise synopsis of each work has been presented below.

Chapter 1: Introduction

The first chapter of this thesis focuses on the importance of solution-processed organic thin film transistors, the history of transistors, working principle structures, important performance defining parameters, the importance of understanding the interfaces present in OFET, and its influence on charge transport. Finally, this chapter also discusses the application of transistors in optoelectronic integrated circuits.

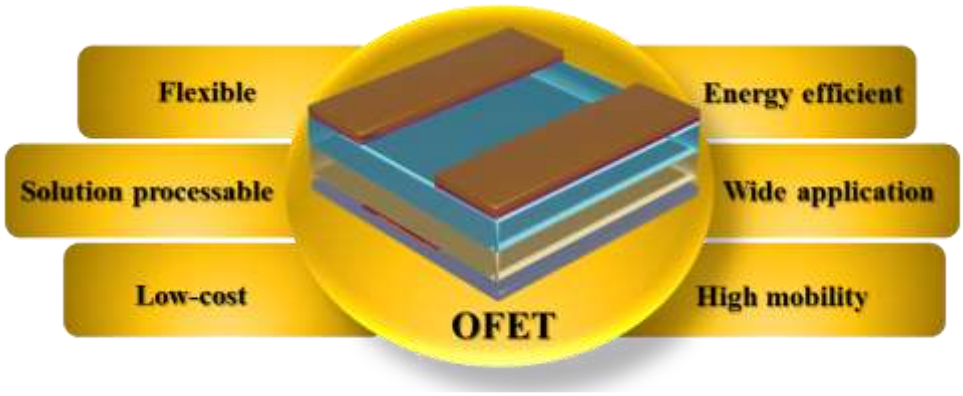


Figure 1: Schematic showing advantages of OFET

Chapter 2: Tailoring Trap Density of States through Impedance Analysis for Flexible Organic Field-Effect Transistor

In this work, impedance spectroscopy (IS) has been utilized as an effective method to obtain the density of States (DOS) spectrum for the interfacial trap study. We have shown how the interface governs the performance of the device. We have fabricated transistors with different dielectrics and studied how the choice of dielectric and dielectric/semiconductor (D/S) interface effect DOS and plays a crucial role in controlling the transistor characteristics. To further verify the findings of IS, characterization techniques like AFM, PL and TRPL are performed. The presence of dipolar molecules at the D/S interface also affects the transistor parameters. Three dielectrics with different polarity and permittivity were chosen and their respective interface DOS is studied for a better understanding of the effect of dielectric surface polarity, surface energy, and dielectric constant (k) on transistor properties. Highest mobility of 0.12 $cm^2 V^{-1} s^{-1}$, 0.095 $cm^2 V^{-1} s^{-1}$, and 0.05 $cm^2 V^{-1} s^{-1}$ is obtained for the device having PVP, PMMA, PS as the interfacial dielectric respectively. Enhanced device performance is observed for the device with lowest trap-DOS. This work provides IS as an efficient tool for understanding the different characteristics of OFET. Further, for evaluating the potential application of the device architecture towards developing flexible electronic circuit components, the device was fabricated on a flexible substrate and the mechanical stability was examined by subjecting the device to a strain of 2.5%. The device showed no significant degradation.

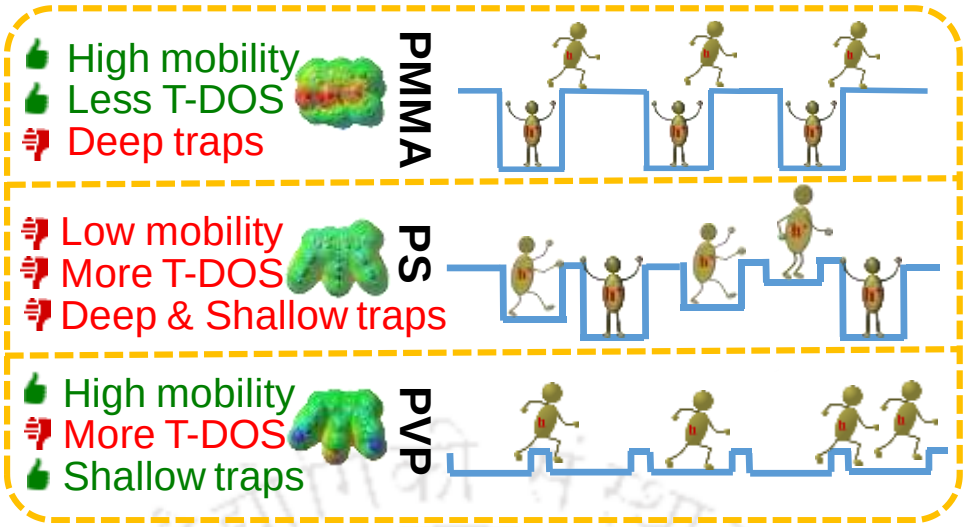


Figure 2: Schematic showing conclusion obtained from the work performed in chapter 2.

Chapter 3: Tuning Polymer Semiconductor Morphology through Additive Engineering for phototransistor.

After the DOS analysis is performed in chapter 2, the non-idealities are identified and modified in this chapter. In this work the proposed transistor architecture is employed for the application of light sensors. 1,8-Diiodooctane (DIO) which is a solvent additive reported for PTB7-Th based solar cells is observed to have a photodegradation effect. Hence here 1,8-Dibromooctane (DBrO) is introduced as a solvent additive for PTB7-Th based OFET and a comparison of transistor characteristics are done between DIO and DBrO OFET. It is observed that when DBrO is used as a solvent additive, the device properties including photostability of the device improved. The OFET mobility increased almost 3-fold compared to the control device and the device retained 70% of the properties even after 35 min of bias stress at a very high voltage of V_{GS}= V_{DS}= -40 V in dark and more 35 min in light while the DIO device degraded to 20% after the bias stress. Different concentration of DBrO is used and the optimum results are obtained at 1.5% of DBrO. Finally, with the optimized concentration of DBrO as a solvent additive, a PTB7-Th based phototransistor (PT) is implemented and responsivity of 688 A/W is obtained.

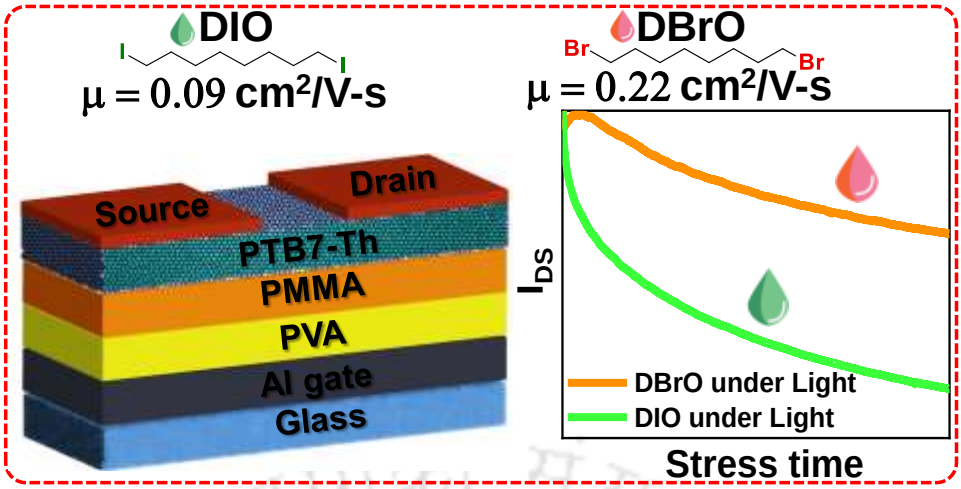


Figure 3: Schematic showing the work performed in chapter 3.

Chapter 4: Engineering Semiconductor Layer for Organic Opto-Inverter Circuit

After exploring the phototransistor (PT) properties of the solvent additive modified transistor in the last chapter, the application of a photo-active polymer-based phototransistor in a digital electronic circuit is demonstrated in this work. Three new Halonaphthalene based solvent additives are studied to tune the thin film morphology and reduce morphology related defects, resulting in improved device performance. The incorporation of 1-bromonaphthalene (BN) improved the mobility from 0.09 to 0.50 $cm^2 V^{-1} s^{-1}$ with enhancement in both photo-absorption and photo-stability. The results are well supported by electrical characterization, photo-physical and morphological studies. Thereafter a novel and unique architecture of opto-inverter is presented using the PT. In this work, opto-electronic logic NOT gate is also fabricated by utilizing a simple resistive load circuit. This circuit is also demonstrated to perform the combined functionality of a logic gate and a transducer. Further, this technique can be easily implemented for minimizing the circuit components and complexity by replacing a photodetector and a NOT gate with a single opto-inverter for example in an image sensor.

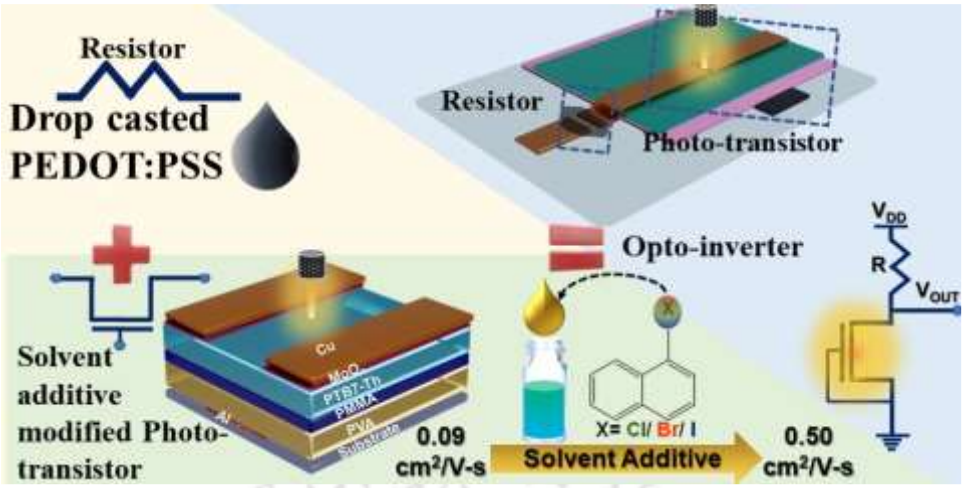


Figure 4: Schematic showing the work performed in chapter 4.

Chapter 5: Solution processed flexible circuit design for dual input logic gates.

The dual input inverter and the NOR logic are demonstrated utilizing a simple circuit design that consists of two components, a phototransistor, and a resistor. Both the components are solution-processed and fabricated simultaneously on a flexible Polyimide/Kapton substrate. An optimized PTB7-Th p-type OFET with high mobility of 0.50 cm^2 V^{-1} s^{-1} and a very low threshold voltage of 2 V along with PEDOT: PSS as the drop-casted resistor helped to attain the high performing logic gates. A high noise immunity up to ~98% and a gain of 12.5 are obtained for the inverter. The resistive load inverter is demonstrated to operate with both light and voltage as input signal along with the single transistor NOR gate.

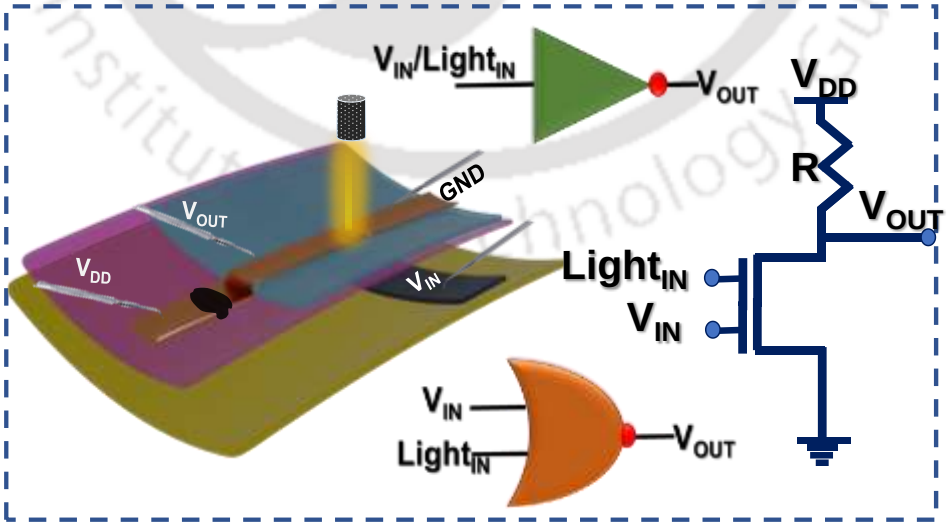


Figure 5: Schematic showing the work performed in chapter 5.

Chapter 6: Summary and future prospects.

This chapter focuses on the conclusion of all the research work done in this thesis and their future prospect. A concise discussion of the main research results is presented along with the future prospects of the solution-processed OFET and their application in integrated circuits.

Outcomes

Journal:

(1) **Choudhury, A.;** Gupta, R. K.; Garai, R.; Iyer, P. K. Solution Processable Flexible circuit design for opto-eletronic logic gates. (Manuscript submitted)

(2) **Choudhury, A.;** Gupta, R. K.; Garai, R.; Iyer, P. K. Engineering Semiconductor Layer for Organic Opto-Inverter Circuit. (Manuscript submitted)

(3) **Choudhury, A.;** Gupta, R. K.; Garai, R.; Iyer, P. K. Tuning Polymer Semiconductor Morphology through Additive Engineering for a Stable Phototransistor. *ACS Appl. Electron. Mater.* **2021,***3* (12), 5393-5401, DOI: 10.1021/acsaelm.1c00873.

(4) **Choudhury, A.;** Gupta, R. K.; Garai, R.; Iyer, P. K. Tailoring Trap Density of States through Impedance Analysis for Flexible Organic Field-Effect Transistors. *Adv. Mater. Interfaces* **2021,***8* (15), 2100574, DOI: https://doi.org/10.1002/admi.202100574.

(5) Garai, R.; Gupta, R. K.; **Choudhury, A.**; Iyer, P. K. Triple Passivation Approach to Laminate Perovskite Layers for Augmented UV and Ambient Stable Photovoltaics. *ACS Appl. Energy Mater.* **2022,***5* (3), 3392-3400, DOI: 10.1021/acsaem.1c03997.

(6) Gupta, R. K.; Garai, R.; Hossain, M.; **Choudhury, A.**; Iyer, P. K. Halide Engineering for Mitigating Ion Migration and Defect States in Hot-Cast Perovskite Solar Cells. *ACS Sustainable Chem. Eng.* **2021,***9* (23), 7993-8001, DOI: 10.1021/acssuschemeng.1c02537.

(7) Das, S.; **Choudhury, A.**; Mandal, A.; Kumar, C.; Ranjan Sahoo, S.; Bedi, A.; Shekhar Karmakar, H.; Gopal Ghosh, N.; Dey, S.; Krishnan Iyer, P.; Bhattacharyya, S.; Zade, S. S. An unconventional route to an ambipolar azaheterocycle and its in situ generated radical anion. *Organic & Biomolecular Chemistry* **2021,***19* (23), 5114-5120, DOI: 10.1039/D1OB00826A.

(8) Mondal, S.; Zehra, N.; **Choudhury, A.**; Iyer, P. K. Wearable Sensing Devices for Point of Care Diagnostics. *ACS Applied Bio Materials* **2021,***4* (1), 47-70, DOI: 10.1021/acsabm.0c00798.

(9) Bhanvadia, V. J.; **Choudhury, A.**; Iyer, P. K.; Zade, S. S.; Patel, A. L. Constructing fused bis-isatins from pyrroloindoles using direct oxidation approach and re-visiting indophenine reaction. *Polymer* **2020,***210*, 123032, DOI: https://doi.org/10.1016/j.polymer.2020.123032.

(10) Mandal, A.; **Choudhury, A.**; Sau, S.; Iyer, P. K.; Mal, P. Exploring Ambipolar Semiconductor Nature of Binary and Ternary Charge-Transfer Cocrystals of Triphenylene, Pyrene, and TCNQ. *J. Phys. Chem. C* **2020,***124* (12), 6544-6553, DOI: 10.1021/acs.jpcc.0c00426.

(11) Garai, R.; Adil Afroz, M.; Gupta, R. K.; **Choudhury, A.**; Iyer, P. K. High-Performance Ambient-Condition-Processed Polymer Solar Cells and Organic Thin-Film Transistors. *ACS Omega* **2020,***5* (6), 2747-2754, DOI: 10.1021/acsomega.9b03347.

(12) Mandal, A.; **Choudhury, A.**; Iyer, P. K.; Mal, P. Charge Transfer Versus Arene–Perfluoroarene Interactions in Modulation of Optical and Conductivity Properties in Cocrystals of 2,7-Di-tert-butylpyrene. *J. Phys. Chem. C* **2019,***123* (30), 18198-18206, DOI: 10.1021/acs.jpcc.9b03827.

(13) Mandal, A.; **Choudhury, A.**; Kumar, R.; Iyer, P. K.; Mal, P. Exploring the semiconductor properties of a charge transfer cocrystal of 1-aminopyrene and TCNQ. *CrystEngComm* **2020,***22* (4), 720-727, DOI: 10.1039/C9CE01507H.

Conference Publication:

Choudhury, A.; Dogra, P.; Teron, B.; Gupta, R. K.; Dey, A.; Singh, A.; Garai, R.; Iyer, P. K. In *Morphology Control of Mixed Halide Perovskite for its Application in Low-cost Thin Film Transistor*, 2018 2nd IEEE International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES), 22-24 Oct. **2018**; pp 743-747.

Book Chapter:

Gupta, R. K.; Arunagirinathan, R. N.; Afroz, M. A.; Garai, R.; **Choudhury, A.;** Hossain, M.; Yathirajula, R. B.; Iyer, P. K. Chapter 4 - Functional materials for various organic electronic devices. In *Chemical Solution Synthesis for Materials Design and Thin Film Device Applications*; Das, S.; Dhara, S., Eds.; Elsevier: 2021; pp 119-165.

Conferences and workshops attended:

(1) International Conference on Advanced Nanomaterials and Nanotechnology (ICANN2017), held at Indian Institute of Technology Guwahati, Assam during December 18-21, 2017

(2) International Conference on Advanced Nanomaterials and Nanotechnology (ICANN2019), held at Indian Institute of Technology Guwahati, Assam during December 18-21, 2019 (Poster Presentation)

(3) The 26th CRSI National Symposium in Chemistry (CRSI NSC-26), held in VIT Vellore during Feb. 7-9, 2020 (Poster Presentation)

(4) Participated in 6th National Workshop on MEMS/NEMS and Theranostic Devices (NWNTD2020) organized by Centre for Nanotechnology, IIT Guwahati, Assam during December 1-3, 2020.

(5) Online workshop on Research level understanding and hands-on Training on SCAPS-1D for the TCAD designing of solar cells organized by Chitkara University, Punjab during September 22-25, 2020.

(6) International Symposium on Organic Iontronics for Sustainable Future organized by Materials Research Society of Japan (MRSJ) during December 13-15, 2021 (Oral Presentation)

References

(1) Ghamari, P.; Niazi, M. R.; Perepichka, D. F. Controlling Structural and Energetic Disorder in High-Mobility Polymer Semiconductors via Doping with Nitroaromatics. *Chem. Mater.* **2021,** *33* (8), 2937-2947, DOI: 10.1021/acs.chemmater.1c00448.

(2) Lee, C.; Lee, W.; Kim, H.; Kim, Y. Water-Soluble Reactive Polymer Blends for Stable Memory Layers in Low-Voltage Nonvolatile Organic Memory Transistors with High Mobility and Data-Retention Characteristics. *Macromolecular Rapid Communications* **2022,** *43* (8), 2100922, DOI: https://doi.org/10.1002/marc.202100922.

(3) Ishida, K.; Huang, T.-C.; Honda, K.; Sekitani, T.; Nakajima, H.; Maeda, H.; Takamiya, M.; Someya, T.; Sakurai, T. A 100-V AC energy meter integrating 20-V organic CMOS digital and analog circuits with a floating gate for process variation compensation and a 100-V organic pMOS rectifier. *IEEE Journal of Solid-State Circuits* **2011,** *47* (1), 301-309.

(4) Tseng, H.-Y.; Subramanian, V. All inkjet-printed, fully self-aligned transistors for low-cost circuit applications. *Org. Electron.* **2011,** *12* (2), 249-256, DOI: https://doi.org/10.1016/j.orgel.2010.11.013.

(5) Yan, Y.; Zhao, Y.; Liu, Y. Recent progress in organic field-effect transistor-based integrated circuits. *Journal of Polymer Science* **2022,** *60* (3), 311-327, DOI: https://doi.org/10.1002/pol.20210457.

(6) Kalb, W. L.; Haas, S.; Krellner, C.; Mathis, T.; Batlogg, B. Trap density of states in small-molecule organic semiconductors: A quantitative comparison of thin-film transistors with single crystals. *Physical Review B* **2010,** *81* (15), 155315, DOI: 10.1103/PhysRevB.81.155315.

(7) Iqbal, H. F.; Holland, E. K.; Anthony, J. E.; Jurchescu, O. D. Real-time monitoring of trap dynamics reveals the electronic states that limit charge transport in crystalline organic semiconductors. *Materials Horizons* **2020,** *7* (9), 2390-2398, DOI: 10.1039/D0MH00706D.

(8) Hunter, S.; Mottram, A. D.; Anthopoulos, T. D. Temperature and composition-dependent density of states in organic small-molecule/polymer blend transistors. *Journal of Applied Physics* **2016,** *120* (2), 025502, DOI: 10.1063/1.4955282.

(9) Muller, E. M.; Marohn, J. A. Microscopic Evidence for Spatially Inhomogeneous Charge Trapping in Pentacene. *Adv. Mater.* **2005,** *17* (11), 1410-1414, DOI: https://doi.org/10.1002/adma.200401174.

(10) Gomar-Nadal, E.; Conrad, B. R.; Cullen, W. G.; Willams, E. D. Effect of Impurities on Pentacene Thin Film Growth for Field-Effect Transistors. *J. Phys. Chem. C* **2008,** *112* (14), 5646-5650, DOI: 10.1021/jp711622z.

(11) Jaquith, M.; Muller, E. M.; Marohn, J. A. Time-resolved electric force microscopy of charge trapping in polycrystalline pentacene. *The journal of physical chemistry. B* **2007,** *111* (27), 7711-7714, DOI: 10.1021/jp073626l.

(12) Puntambekar, K.; Dong, J.; Haugstad, G.; Frisbie, C. D. Structural and Electrostatic Complexity at a Pentacene/Insulator Interface. *Adv. Funct. Mater.* **2006,** *16* (7), 879-884, DOI: https://doi.org/10.1002/adfm.200500816.

(13) Bube, R. H. Trap Density Determination by Space-Charge-Limited Currents. *Journal of Applied Physics* **1962,** *33* (5), 1733-1737, DOI: 10.1063/1.1728818.

(14) Shao, Y.; Xiao, Z.; Bi, C.; Yuan, Y.; Huang, J. Origin and elimination of photocurrent hysteresis by fullerene passivation in CH3NH3PbI3 planar heterojunction solar cells. *Nat. Commun.* **2014,** *5* (1), 5784, DOI: 10.1038/ncomms6784.

(15) Ni, Z.; Bao, C.; Liu, Y.; Jiang, Q.; Wu, W.-Q.; Chen, S.; Dai, X.; Chen, B.; Hartweg, B.; Yu, Z.; Holman, Z.; Huang, J. Resolving spatial and energetic distributions of trap states in metal halide perovskite solar cells. *Science* **2020,** *367* (6484), 1352, DOI: 10.1126/science.aba0893.

(16) Horowitz, G.; Hajlaoui, R.; Delannoy, P. Temperature dependence of the field-effect mobility of sexithiophene. Determination of the density of traps. *Journal de Physique III* **1995,** *5* (4), 355-371.

(17) Kalb, W. L.; Batlogg, B. Calculating the trap density of states in organic field-effect transistors from experiment: A comparison of different methods. *Physical Review B* **2010,** *81* (3), 035327, DOI: 10.1103/PhysRevB.81.035327.

(18) Hoefler, S. F.; Rath, T.; Pastukhova, N.; Pavlica, E.; Scheunemann, D.; Wilken, S.; Kunert, B.; Resel, R.; Hobisch, M.; Xiao, S.; Bratina, G.; Trimmel, G. The effect of polymer molecular weight on the performance of PTB7-Th:O-IDTBR non-fullerene organic solar cells. *J. Mater. Chem. A* **2018,** *6* (20), 9506-9516, DOI: 10.1039/C8TA02467G.

(19) Patrikar, K.; Jain, N.; Chakraborty, D.; Johari, P.; Rao, V. R.; Kabra, D. Influence of Pendant Group on Mobility of Organic Thin Film Transistor in Correlation with Reorganization Energy of Molecules. *Adv. Funct. Mater.* **2019,** *29* (8), 1805878, DOI: https://doi.org/10.1002/adfm.201805878.

(20) Garai, R.; Adil Afroz, M.; Gupta, R. K.; Choudhury, A.; Iyer, P. K. High-Performance Ambient-Condition-Processed Polymer Solar Cells and Organic Thin-Film Transistors. *ACS Omega* **2020,** *5* (6), 2747-2754, DOI: 10.1021/acsomega.9b03347.

(21) Choudhury, A.; Gupta, R. K.; Garai, R.; Iyer, P. K. Tailoring Trap Density of States through Impedance Analysis for Flexible Organic Field-Effect Transistors. *Adv. Mater. Interfaces* **2021,** *8* (15), 2100574, DOI: https://doi.org/10.1002/admi.202100574.

(22) Choudhury, A.; Gupta, R. K.; Garai, R.; Iyer, P. K. Tuning Polymer Semiconductor Morphology through Additive Engineering for a Stable Phototransistor. *ACS Appl. Electron. Mater.* **2021,** *3* (12), 5393-5401, DOI: 10.1021/acsaelm.1c00873.

Thesis Abstract

Electronic devices have made people's life easier, and in today's modern lifestyle electronic devices have become one of the basic requirements of human beings. Inorganic material are used extensively in electronic devices but the requirement of energy efficient, low-cost and flexible devices can be easily fulfilled by the organic solution processable materials. Organic field effect transistors (OFET) will enable easy implementation of large scale and flexible applications. Organic materials also have the advantage of easy tunability of the optoelectronic properties. OFETs have numerous applications like various sensors, smart card, e-skin etc. Some of the organic electronic devices like OLED, solar cell is already available in market, but low mobility and stability is a road block for organic transistors to be commercialized in high end applications.

Considering todays need for solution processed, flexible and energy efficient organic electronic devices, methods to understand the dielectric/semiconductor interfacial defects introduced due to solution processing and techniques to improve the device properties is covered in this thesis. This thesis is divided into three parts, the first part (Chapter 2) is about the understanding the interfacial defects arising due to complete solution processing of the dielectric and semiconductor. Second part (Chapter 3 and 4) consists of solvent engineering technique to improve the device mobility and stability. A ~5-fold increment in device mobility and also improvement in device stability in dark and under illumination is attained by solvent engineering. Third part (chapter 5) is the application of the improved device in various opto-electronic applications thereby, NOT and NOR logic are demonstrated by applying light and voltage input simultaneously.

The efforts made in this thesis highlights the usefulness of various device engineering to develop OFET to regulate the morphology and crystallization of the photo-active semiconductor layer to achieve highly efficient, stable and repeatable OFETs and its application as phototransistor, and logic gates. The thesis provides the basis for facilitating the commercialization of OFET in the near future.