INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI
SHORT ABSTRACT OF THESIS

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Thesis Title: MODELLING AND SIMULATION OF SHORT CHANNEL JUNCTIONLESS TRANSISTOR FROM AN ANALOG DESIGN PERSPECTIVE

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SHORT ABSTRACT

Low power and high performance devices are in demand for today's microelectronics market. Conventional planar CMOS transistors on bulk silicon substrate have been a key component in ultra-large-scale integration technology for the past four decades, but are approaching the fundamental physical limits imposed by short-channel-effects (SCEs) and gate oxide tunnelling. Fully depleted multiple-gate-field-effect-transistors (Mug-FETs) was proposed as an alternative to planar devices because of their robust electrostatic control which too face technological challenges in super-steep doping profile requirement and high thermal budget for sub-20 nm channel length era along with excessive SCEs. Junctionless transitors (JLT), which do not have any pn junction in the source-channel-drain path can be scaled to lower channel lengths because of lower SCEs and easy fabrication steps and can be a prospective candidate for replacement to conventional Mug-FETs in sub-20 nm regime. The thesis discusses about the analog and digital performances; process and temperature effects of a double-gate junctionless transistor (DGJLT). The effects of the fringing fields on the device and circuit performances of a JLT are discussed. Different architectures to improve the analog performance of a JLT are examined with the help of extensive device simulations. An analytical channel potential model for shorter-channel dual-material gate DGJLT valid in subthreshold region is developed. Also, a semi-analytical electrostatic potential and a drain current model for single-material gate DGJLT are derived. Finally, the process simulation of DGJLT is carried out with the help of Genius device simulator.