Design and Analysis of Memelements for Low Power and Area Efficient High Frequency Applications

A

Thesis submitted

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By

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Certificate

This is to certify that the thesis entitled "**Design and Analysis of Memelements for Low Power and Area Efficient High Frequency Applications**", submitted by **ANANDA Y R** (186102001), a research scholar in the *Department of Electronics and Electrical Engineering, Indian Institute of Technology Guwahati*, for the award of the degree of **Doctor of Philosophy**, is a record of an original research work carried out by him under my supervision and guidance. The thesis has fulfilled all requirements as per the regulations of the institute and in my opinion has reached the standard needed for submission. The results embodied in this thesis have not been submitted to any other University or Institute for the award of any degree or diploma.

Dated:

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Dedicated to my parents and sisters for their unremitting support and strength.

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ANANDA Y R

Abstract

Memristor, memcapacitor, and meminductor are the three types of memory elements (memelements). The memristor is the fourth fundamental circuit element based on the missing relationship between two fundamental electrical quantities, the charge (q) and the flux (ϕ). The memristor is considered one of the most promising nano-devices among the devices currently being studied for possible use in future electronic systems. The best performance features include fast switching speed, high endurance and data retention, low power consumption, high integration density, and CMOS compatibility. Memristors are being explored as a potential technology to replace CMOS for logic-in-memory systems exploiting memristive nonvolatility. It is one of the prominent characteristic features of the memristor, which effectively solves the so-called memory wall problem in conventional von-Neumann architecture. A memristive device is highly nonlinear and nonvolatile, making it a better storage element with higher data density than the existing memory devices. In addition, the memristor exhibits switching capability, which is more relevant for implementing logic gates, a realization of Boolean functions, and system designing, such as arithmetic units like adders, subtractors, multipliers and dividers.

Meminductors and memcapacitors are the two special classes of memelements that exhibit inductive and capacitive behaviour. Memcapacitor is the constitutive relation between the time integral of the charge (TIC) and the flux, and the meminductor is the time integral of the flux (TIF) and the charge. These memelements exhibit a pinched hysteresis loop (PHL), indicating their nonvolatile behaviour capable of storing the data. Memcapacitors and meminductors are lossless devices and more power efficient than the memristor. The distinctive properties of memelements offer several advantages, such as high scalability and low power consumption, making them suitable for designing high-performance neuromorphic computing, programmable analog ICs, oscillators, filters, amplifiers, process analog information in artificial intelligence (AI) applications, adaptive learning circuits, spik-

ing neural networks, chaotic oscillators, and several bio-inspired applications. The realization of these memelements requires suitable materials and a novel fabrication process. However, these memelements are emulated by the scientific community using solid-state discrete electronic devices for designing practical applications. The emulators presented in the literature require active and passive elements, which increases the hardware complexity with limited operating frequency. It motivated us to propose area and power-efficient emulators capable of operating at high frequency for realizing memelements using the minimum number of off-the-shelf circuit elements.

Further, very efficient, computationally accurate, highly nonlinear and scalable window functions for the linear ion-dopant-drift memristor models are designed. These novel window functions are proposed by incorporating new parameters called *Error Parameter* (ϵ_0) and *Adaptive constant* (A_D), which aid in adjusting the nonlinearity for any variation in the applied voltage and frequency. Thus, the proposed window functions help generate expected PHL for a wide range of voltage and frequency operations without distortion and boundary effects compared to other standard window functions reported in the literature.

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Introduction

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1.1 Introduction

The novel fundamental circuit element memristor was conceptualized by Leon Chua [2] based on the missing relationship between charge (q) and flux (ϕ). Memristor is employed due to its characteristic as a memory and a resistor. It holds the previous resistance value without an applied electric field, showcasing its nonvolatile property. The first physical memristor fabricated by HP Labs in 2008 [3] consists of bilayered TiO_2 sandwiched between two platinum electrodes. Later, a general class of systems was defined [4], extending the behaviour of memory elements not only for resistive behaviour but also for capacitive and inductive properties. As a result, a special class of two new memelements is evolved in addition to a memristor, namely, memcapacitor and meminductor [4]. These memelements (memory circuit elements) [5] attracted the scientific and research communities to explore potential applications mainly in ultra-high density resistive switching memory (ReRAM) [6], chaotic oscillators [7], programmable analog circuits [8], neuromorphic computing [9], Adaptive Spiking Neural Networks [10], and bio-inspired system design [11, 12]. The key features of these memelements are higher scalability, high performance, low power dissipation, computation in-memory operation, and nonvolatility. The fundamentals of these memelements are discussed in the following section.

1.1.1 Memristor

As stated above, Leon Chua hypothesized a memristor [2] as the new fourth fundamental circuit element alongside the other three, viz. resistor, inductor, and capacitor. He found a missing symmetry in the relation among the four basic circuit parameters, as shown in Fig. 1.1 and proposed the link between flux (φ) and charge (q). Along with a nonlinear behaviour of a memristor, it also exhibits the NVM (nonvolatile memory) property, which implies that memory retention is independent of the power supply applied to the element. The fundamental equation that defines a memristor is given below.

$$V(t) = R_m(x, I, t)\ I(t) \tag{1.1}$$

R_m is the memristance of the memristor, and x is a state variable.

From Eq. 1.1, it is evident that memristance has the dimensions of resistance. It is also seen that its value is dependent on past behaviour and is not a constant; unlike a resistor, this particular dependence on the resistance makes the memristor capable of having a memory. Eq. 1.2 depicts the

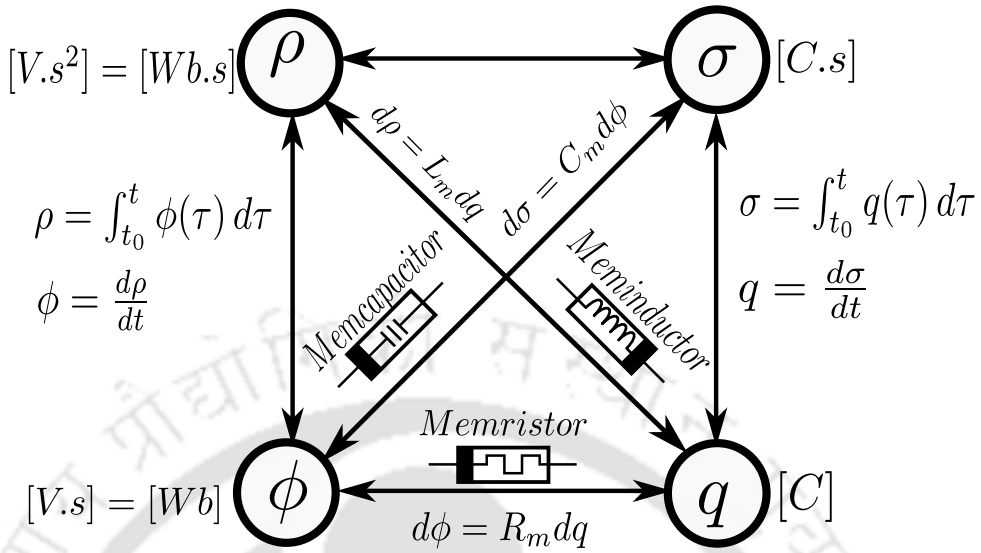

Figure 1.1: Fundamental circuit parameters and their relationships [1]

complete form of a charge-controlled memristor.

$$R_m(q) = \frac{V(t)}{I(t)} = \left[a_1 + a_2 \int I(t)\, dt\right] = [a_1 + a_2\ q(t)] \tag{1.2}$$

where a_1 and a_2 are the constants.

Since the memristor links two circuit parameters, we can also model it as a flux-controlled device defined by Eq. 1.3, and is elaborated in Eq. 1.4.

$$I(t) = R_m^{-1}(x, V, t)\ V(t) \tag{1.3}$$

$$R_m^{-1}(\varphi) = \frac{I(t)}{V(t)} = \left[a_1' + a_2' \int V(t)\, dt\right] = \left[a_1' + a_2'\ \varphi(t)\right] \tag{1.4}$$

where a_1' and a_2' are the constants, and x is a state variable.

Memristor results in a PHL (pinched hysteresis loop) as a Lissajous pattern when plotted as $V(t)$ vs. $I(t)$. The presence of PHL is one of the conditions that need to be fulfilled for a memelement, along with common zero crossings in transient voltage $V(t)$ and current $I(t)$ curves. Although the memristor does not consume any power when storing the data, it does consume power when data is read or written into it. Meminductor and memcapacitor are two new memelements that minimize power consumption. The following section explains the concept behind these two memelements in detail.

1.1.2 Evolution of new memelements

Meminductor and memcapacitor are the two new memelements introduced by Di et al. [4]. As seen from Fig. 1.1, the other missing links between the flux (φ), charge (q), time-integral of flux TIF ($\rho = \int \varphi \, dt$) and time-integral of charge TIC ($\sigma = \int q \, dt$) form the basis for these two new memelements.

1.1.2.1 Meminductor

Meminductor establishes the relation between TIF (ρ) and charge (q), and its fundamental mathematical model for the current-controlled element is given by Eq. 1.5.

$$\varphi(t) = L_m(x, I, t) \; I(t) \tag{1.5}$$

Eq. 1.5 is further elaborated below.

$$L_m(I) = \frac{\varphi(t)}{I(t)} = \left[b_1 + b_2 \int I(t) \, dt \right] \tag{1.6}$$

where b_1 and b_2 are the constants, L_m is the meminductance of the meminductor, and x is a state variable.

From Eq. 1.5, it is evident that meminductance changes with the applied input. It can be of two types, viz., current-controlled and flux-controlled. Eq. 1.5 and Eq. 1.7 represent mathematical models for the current-controlled and flux-controlled meminductors.

$$I(t) = L_m^{-1}(x, \varphi, t) \; \varphi(t) \tag{1.7}$$

Eq. 1.7 is elaborated further as depicted below.

$$L_m^{-1}(\varphi) = \frac{I(t)}{\varphi(t)} = \left[b_1' + b_2' \int \varphi(t) \, dt \right] \tag{1.8}$$

where b_1' and b_2' are the constants, and L_m^{-1} is the inverse meminductance.

From Eqs. 1.6 and 1.8, b_1 and b_1' are called initial inductance and inverse inductance of the meminductor, and the constants b_2 and b_2' are the scaling product terms. The integration terms in Eqs. 1.6 and 1.8 signify that the meminductance is not constant but depends on the flux accumulation or the current since its value strongly depends on its past behaviour. Both equations mentioned

above shall be used to model a meminductor controlled by either flux or current. According to the mathematical model, meminductor design can be realized with the help of active analog blocks.

1.1.2.2 Memcapacitor

Memcapacitor is the other new memelement postulated by Di et al. [4]. It establishes a relationship between flux (φ) and TIC (σ), as evident from Fig. 1.1. The fundamental equations defining the memcapacitor are as follows.

$$q(t) = C_m(x, V, t)V(t) \tag{1.9}$$

Eq. 1.9 can be stated further as shown in Eq. 1.10.

$$C_m = \frac{q(t)}{V(t)} = \left[c_1 + c_2 \int V(t)\, dt\right] \tag{1.10}$$

where c_1 and c_2 are constants, C_m is the memcapacitance of the memcapacitor, and x is a state variable. From Eq. 1.9, it is evident that memcapacitance depends on the applied input, and it can be of two types, viz. voltage and charge controlled. Eq. 1.9 represents a mathematical model of the voltage-controlled memcapacitor. Similarly, Eq. 1.11 is the mathematical model for the charge-controlled memcapacitor.

$$V(t) = C_m^{-1}(x, q, t)q(t) \tag{1.11}$$

Eq. 1.11 can be further formulated as stated in Eq. 1.12.

$$C_m^{-1} = \frac{V(t)}{q(t)} = \left[c_1' + c_2' \int q(t)\, dt\right] \tag{1.12}$$

where c_1' and c_2' are constants, and C_m^{-1} is the inverse memcapacitance.

From Eqs. 1.10 and 1.12, c_1 and c_1' are the initial memcapacitance and inverse memcapacitance of a memcapacitor. The constants c_2 and c_2' represent the scaling product terms. The integration terms in Eqs. 1.10 and 1.12 signify that the characteristic of a memcapacitor, i.e., memcapacitance, is not constant but depends on the past behaviour of voltage or charge. Both equations mentioned above are employed to model a memcapacitor controlled by voltage or charge. A detailed survey of the above-stated memelements is elucidated in the next section for completeness.

1.2 Literature Survey on Memelements

The memristor drew the attention of the research community after its first physical fabrication. Various experiments on memristors have been conducted to study their nonlinear and nonvolatile properties applicable to diverse applications. Further, the design and implementation of any of these applications require a physical memristor, but the fabrication complexities incurred in developing nanostructured memristive devices impact its commercialization [13] and wide usage.

The solid-state memristors are commercialized by KNOWM [14]. However, commercial memristors have strict operational conditions, especially DC and AC responses, which limit their general acceptance. Therefore, many memristor models [15–18] have been developed aiming to implement it in various real-life applications and are analyzed numerically. One of the most promising methods to circumvent this limitation is the physical realization of a memristor (or emulation) using discrete components, such as MOSFETs.

The memristor emulator designed by Pershin et al. [19] includes a microcontroller, an ADC, and a digital potentiometer. The operating frequency of this emulator is limited to 50 Hz, and circuit complexity restricts this emulator from being used with other circuit elements operating at a high frequency. The memristor emulator proposed by Hyongsuk Kim et al. [20] consists of several discrete elements, such as an operational amplifier, analog multiplier, transistors and resistors. However, this emulator is unsuitable for monolithic integration due to many discrete components and a large on-chip area. Similarly, there are many memristor emulators available in the literature, which employ second-generation current conveyors (CCII) and passive elements [21,22], differential difference current conveyor (DDCC) [23], current feedback operational amplifiers (CFOAs) and operational transconductance amplifier (OTA) [24], current backward transconductance amplifier (CBTA) [25], differential voltage current conveyor transconductance amplifier (DVCCTA) [26], etc. Note that memristor emulators with discrete circuit elements are available as analog ICs [24,27–31] for commercial use. However, Babacan et al. [32] presented a grounded memristor emulator using four MOSFETs with a maximum operating frequency of 100 MHz. Since this emulator is of the grounded type, one of its terminals is always connected to the ground. It also requires an external DC supply making its usage complex in practical applications [10].

A meminductor [4] is characterized by formulating a constitutive relationship between the charge q and the time integral of the flux (TIF). The fabrication of the nano-sized meminductor is delayed due

to the complexity and difficulty in selecting suitable materials [33] for its physical realization. Thus, several models [34–36] suggested by the researchers to exploit its vital properties. Another alternative to realizing a meminductor is to emulate its characteristic using off-the-shelf components suitable for real-time applications. A meminductor emulator [37] was proposed initially using a microcontroller, opamps, and other passive elements. In 2010, Biolek and Biolkova [38] proposed a set of mutators that could be used to transform a memristor into a meminductor or a memcapacitor. In some of these proposed designs, a meminductor was realized using memristor-less circuits [39] consisting of CCII (current conveyors), analog adders, and multipliers.

An emulator illustrated in [40] is also a memristor-less design. A mutator-based meminductor emulator was depicted in [41], in which various configurations of memristors were implemented to realize different meminductor circuits. A universal emulator was discussed in [42], yielding a memristor, meminductor, and memcapacitor by simply changing some of the passive elements without altering the overall topology of the emulator. A nano memristor was transformed into a meminductor employing a gyrator, as shown in [43]. Another universal mutator for realizing memcapacitor and meminductor was proposed in [44], which was based on CBTA (Current backward transconductance amplifier), a memristor, and a capacitor.

In [45], a meminductor emulator was presented, which was based on a modified Antoniou's gyrator circuit. It was realized practically and was verified using off-the-shelf components. A single operational amplifier, a memristor, and passive elements were used to design a meminductor emulator [46]. Based on the Riordan gyrator, a floating meminductor emulator was reported in [47]. M. Konal and F. Kacar [48] realized a meminductor that was electronically tunable using an OTA (Operational transconductance amplifier). S. Minaei et al. proposed a meminductor circuit [49] that was built using adder and subtractor circuits along with a memristor. A mutator was designed using VDCC (voltage differencing current conveyor), which transformed a memristor to a meminductor or a memcapacitor emulator, was presented in [50].

The mutator-based meminductor emulators [34,37,41,44,51–53] were designed using several analog building blocks, such as CCII, CBTA, analog multiplier (AM), and passive elements for transforming memristive behavior into meminductors. A dedicated meminductor emulator without mutator presented by M. P. Sah et al. [40] was realized using an analog multiplier, an inductor, a resistor, and other analog blocks, but using an analog multiplier reduces the lobe area of the PHL [54]. This

emulator also exhibits high hardware complexity and a limited operating frequency range. The other state-of-the-art emulators available in the literature are designed using many active and passive elements, and their hardware complexities and operating frequencies are depicted in Table 1.1. All the emulators reported in the literature require passive elements and other active blocks, making them comparatively challenging to fabricate on silicon.

Table 1.1: Summary of the available meminductor emulators

Authors	Year	Ref.	Components used	Hardware Complexity	Operating Frequency
Sah et al.	2014	[55]	1-buffer, 3-opamps, 1-AM, 2-CCII, 8-R, 2-C	high	low
Fouda et al.	2014	[39]	3-CCII, 1-analog adder, 1-AM, 3-R, 2-C		
Zhao et al.	2019	[42]	3-CCII, 1-AM, 2-R, 2-C		
Romero et al.	2020	[45]	2-opamps, 1-C, 3-R		
Raj et al.	2021	[56]	1-CCII, 1-OTA, 2-C, 2-R	high	moderate
Liu et al.	2020	[33]	4-CCII, 1-AM, 1-opamps, 6-R, 2-C		
Raj et al.	2021	[57]	2-OTA, 1-DVCC, 1-R, 1-C		
Raj et al.	2021	[58]	3-OTA, 2-C	moderate	moderate
Vista et al.	2019	[54]	2-VDTA, 2-C		

Here, R and C represents resistor and capacitor.

Similarly, the new process technology, specific materials, and different electroforming techniques are required for manufacturing the nano-dimensional memcapacitor, which delayed its production and commercialization. The constraints, which limit the commercialization of the memelements, especially memcapacitors, are primarily the sophisticated and very expensive fabrication mechanism and setup [59, 60]. Therefore, the scientific and research communities designed several emulators using off-the-shelf components for realizing memcapacitors. These emulators can be easily manufactured using the current technology nodes and aid the research on memelements for realizing practical applications.

One of the initial proposals of the memcapacitor includes a mutator model [61] realized using a memristor, active components, and an LDR (light dependent resistor). Yu et al. [62] proposed a memcapacitor utilizing active analog blocks and a memristor. A three-port mutator, which allows the transformation of a memristor into a meminductor and a memcapacitor with the help of two CCIIs (second generation current conveyors), was suggested by Yu et al. [63] in 2014. A memcapacitor designed using a VDTA (voltage differencing transconductance amplifier) and a memristor is proposed by

Hosbas et al. [64]. Many memristor-less designs are depicted in the literature, including a memcapacitor by Fouda et al. [65], which is a charge-controlled device assembled using off-the-shelf components. An electronically controllable memcapacitor is illustrated in [66] and is implemented using CCII, OTA, and AM (analog multiplier). In [67], a charge-controlled memelement emulator is proposed for realizing a memristor and a memcapacitor. Further, a grounded memcapacitor is presented in [68] employing a VDCC (voltage differencing current conveyor). A charge-controlled memcapacitor using off-the-shelf elements is presented by Sah et al. [69], whereas another memcapacitor is proposed in [70], which is implemented in chaotic circuit to verify its applicability.

In the literature, many circuits are proposed which can realize more than one memory element by introducing minor modifications. Such circuits are called universal emulators. One such universal emulator is presented in [71], which realizes all three memelements using CCII, AM and opamps (operational amplifiers). Using varactor diode and active analog blocks, a simple mutator is elaborated by Yu et al. [72], capable of realizing three memelements just by making changes in the position of passive elements in the mutator circuit. In 2014, a universal mutator is proposed [73], which is designed utilizing three off-the-shelf active components. Singh et al. [74] present a mutator based on VDCC (voltage difference current conveyors) that transforms a memristor into meminductor and memcapacitor simply by interchanging the position of the components.

Yu et al. [75] presented two flux-coupled memcapacitors used to implement a relaxation oscillator with controllable oscillation frequency and duty cycle. An SRAM (static random access memory) circuit has been implemented by Abbasi et al. [76] using transistors and memcapacitors, yielding better performance. In 2019 [77], a memcapacitor is employed to encrypt images. However, numerous emulators are available in the literature, utilizing many active blocks, passive elements, and memristors exhibiting limited operating frequency. Not only this increases the complexity of the emulators but also their power consumption. Further, these emulators used multiplier and mutator to realize a memcapacitor, exhibiting high design complexity. Also, due to the use of a multiplier, the lobe area of the PHL reduces, limiting their operating frequency [78]. Therefore, various limitations of memelements emulators reported in the scientific literature motivated us to realize optimized emulators with respect to area, power, and frequency, as discussed in the following section.

1.3 Motivation

As discussed above, available emulators in the scientific literature exhibit several limitations, such as high hardware complexity due to the utilization of a large number of components, increased power consumption, and limited operating frequency, which deterred them from employing in designing practical applications. These factors motivated us to design area, power, and performance-efficient emulators for various applications. Note that memelements can be used for several high-performance applications, such as next-generation neuromorphic computing systems [79], parallel analog processors [5], and several bio-inspired computing architectures [80]. Therefore, memelements operating at high frequency are essential for designing these applications.

Additionally, several window functions are available in the literature to incorporate nonlinear behaviour into the memristor model. However, these window functions exhibit limited nonlinearity when the operating frequency exceeds the acceptable range. Hence, this led us to propose new window functions for modelling memristor to enhance the nonlinearity, scalability, and other prominent features compared to earlier window functions.

This thesis proposes four memelements emulators and two window functions as the novel contributions in this thesis, which are discussed below.

1.4 Research contributions

Nonlinearity is one of the prominent properties of a memristor, which can be integrated with the linear ion drift model of a memristor by employing a window function. This work presents two window functions, exhibiting better nonlinearity and scalability over a wide range of applied frequencies. The vital features of these window functions are mentioned below.

(i) As we know, a memristor is a dynamic electronic device whose conductivity changes with respect to the change in the applied electric field. This phenomenon of a memristor is achieved by introducing a new parameter, ϵ_0, in the proposed *Dynamic window function*. This window function exhibits higher nonlinearity than the other window functions available in the literature [81–84]. Also, unlike other window functions, this function does not require a high value of j at a higher frequency due to the incorporation of ϵ_0.

(ii) *Adaptive window function* is the second window function proposed in this work. As the name

suggests, the nonlinearity adapts itself with respect to the variation in applied voltages and frequencies. There is no need to change any static parameters for a change in the operating voltage or frequency due to using an adaptive constant (A_D) in the proposed window functions, which helps boost the nonlinearity compared to those reported in the literature.

After studying and understanding the nonlinear behaviour of the memristor and its $I-V$ characteristic based on the change in the applied voltages and frequencies, an area-efficient memristor emulator is proposed to realize the memristor using off-the-shelf components. As stated below, the proposed memristors offer several advantages over its contemporary memristor emulator.

(i) As per our knowledge, the proposed emulator is better area efficient than any other memristor emulators presented in the literature.

(ii) Its simple design is due to the absence of an external DC supply.

(iii) It has the highest operating frequency range than any other floating memristor emulators proposed in the literature.

(iv) It can be utilized to design various applications due to its floating nature and easier integration with other circuit elements.

Subsequently, we studied the inverse frequency behaviour of a memristor (inverse memristor). A few inverse memristor emulators are presented in the literature consisting of several active and passive elements, which increase the hardware complexity and limited operating frequencies. These limitations of earlier inverse memristor emulators are addressed in the proposed inverse memristor emulator. The following are the pivotal merits of the proposed emulator.

(i) It is the simplest inverse memristor emulator designed using only four MOSFETs. Hence, it utilizes less area and consumes lower power.

(ii) It is suitable for designing several potential applications.

(iii) It offers the maximum operating frequency in MHz range compared to other inverse memristors.

Further, we propose a meminductor emulator using MOSFETs only for the first time without utilizing passive elements. The proposed meminductor emulator is fully optimized with respect to area, power, and frequency. The main features of the proposed emulator are mentioned as follows.

(i) It exhibits efficient area utilization and less power consumption due to using the minimum number of active elements.

(ii) The maximum operating frequency is in the range of several MHz.

(iii) Its simplicity makes it suitable for monolithic IC fabrication and easier integration with other components while designing practical applications.

Our proposed memcapacitor emulator alleviates the limitations exhibited by contemporary memcapacitors. The major contributions of the proposed memcapacitor emulator are described below.

(i) It requires the minimum number of MOSFETs and only one resistor exhibiting better area utilization and lower power consumption compared to contemporary memcapacitors.

(ii) It exhibits the highest operating frequency than other memcapacitor emulators.

(iii) It is a potential candidate for designing various applications due to its simple circuit topology.

1.5 Organization of the Thesis

The thesis consists of seven chapters, and their outlines are summarized below.

- **Chapter 2** presents window functions for modelling a memristor, the limitations of linear ion drift of a memristor, and introduces a window function and its essential features. The detailed analysis of state-of-the-art window functions and their drawbacks, along with mathematical models and the numerical analyses of the proposed window functions are also depicted in this chapter. It also states the advantages of the proposed window functions over standard window functions.

- **Chapter 3** discusses the memristor emulator, and its design and implementation along with its mathematical model. Numerical and experimental validation of the proposed emulator are detailed in this chapter.

- **Chapter 4** describes the study and analysis of a memristor with inverse frequency characteristics (inverse memristor). This chapter states its design and implementation, along with its numerical and experimental validation.

- **Chapter 5** elucidates the implementation of a meminductor emulator using off-the-shelf circuit elements. The realization of the proposed meminductor emulator and its analytical study, numerical and experimental verification are presented in this chapter.
- **Chapter 6** elaborates on the memcapacitor emulator. The realization and analysis of proposed memcapacitor emulators, their parametric analyses and experimental validation are depicted in this chapter.
- **Chapter 7** concludes this thesis's research contributions, giving future directions for the proposed research work.

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2

Window Functions for Modelling Memristor

Contents

Objective:

Design and analysis of window functions to improve and increase the nonlinearity and scalability of the linear ion drift model of the memristor.

2.1 Introduction

HP Labs [3] fabricated a memristor in 2008 and derived its mathematical model. Strukov et al. [3] proposed a memristor model based on the linear electric field. Hence, this model is called as linear ion drift model.

Practically, a memristor is a nonlinear device with a width below the sub-nanometer regime, leading to nonlinear electric field variations, in which a small change in the voltage causes a large change in the electric field. Therefore, a window function [3] has been introduced to achieve a certain degree of nonlinearity satisfying boundary conditions related to the physical dimension of a memristor. Joglekar et al. [81] formulated a window function to achieve nonlinearity in the linear ion drift model of a memristor. However, this window function has several limitations, including boundary lock problems and scalability issues. Biolek et al. [82] proposed a new window function, which has limited scalability and distortion in the pinched hysteresis loop (PHL) at certain voltages and frequencies. Prodromakis et al. [83] devised a window function that has better scalability but leads to a boundary lock problem. Jinxiang et al. [84] introduced a novel window function, which retains the advantages of Prodromakis without a boundary lock problem, but has limited nonlinearity. Hence, it leads to distorted PHL at various frequencies and voltages. The limitations of the window functions stated above motivated us to propose two window functions, which are as follows.

(i) Dynamic window function

(ii) Adaptive window function

As we know, the memristor is a dynamic electronic device in which memristance changes with respect to the change in the applied voltage. Considering the dynamic behaviour of a memristor, new parameters are introduced in the proposed window functions employed to imitate the behaviour of a memristor. Furthermore, the proposed window functions are designed to ensure nonlinearity at the boundary of the active layer of a memristor. These window functions are validated at various performance parameters exhibiting full scalability and nonlinearity. Further, the boundary lock problem for

different valid combinations of control parameters, voltages, and frequencies is resolved by employing proposed window functions. The memristor model using proposed window functions generates expected PHL with higher nonlinearity and scalability without violating boundary conditions in the wide range frequency operations.

The various features of the proposed window functions are summarized below for completeness.

(i) Generation of PHL at all operational frequencies and voltages

(ii) Lower values of parameters at high frequencies

(iii) Increased nonlinearity compared to existing window functions

(iv) Dynamic behaviour due to the presence of dynamic parameter

This chapter is structured as follows. Section 2.2 presents the linear ion drift model of a memristor. Section 2.3 discusses the prior artwork of window functions. Section 2.4 depicts the proposed dynamic window function. Section 2.5 elucidates the parametric analysis of the proposed window function. Section 2.6 describes the proposed adaptive window function. Section 2.7 enunciates the numerical analysis of the proposed adaptive window function. Section 2.8 concludes this chapter.

2.2 Linear ion drift model of memristor

The physical structure of a memristor comprises an insulator or a semiconductor material based active layer of dimension D sandwiched between two platinum electrodes. The active layer of the memristor has two regions: an oxygen deficit region (doped region) of width w and an oxygen-rich (undoped region), as shown in Fig. 2.1.

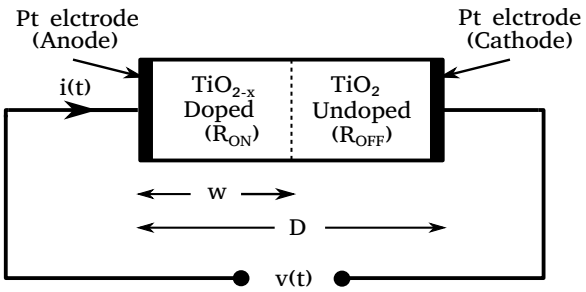


Figure 2.1: $Pt/TiO_2/Pt$ memristive device structure

The equivalent circuit of the memristor, which represents two resistive states, R_{ON} (low resistance)

and R_{OFF} (high resistance), with respect to change in the width w of the doped region and the direction of current flow, is illustrated in Fig. 2.2.

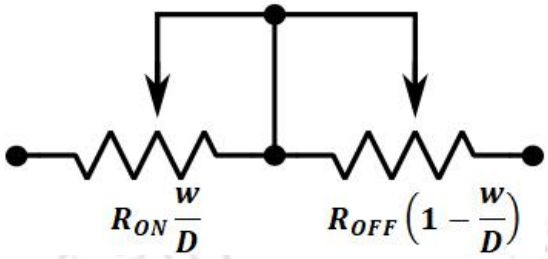


Figure 2.2: Equivalent circuit of a memristor

The boundary between doped and undoped regions changes due to the application of external voltage because of the movement of charged dopants in the active layer of the device. Stanley William et al. [3] formulated the mathematical model of a memristor by considering linear ionic drift mechanism in a uniform electric field and average ion mobility μ_d as expressed in the equation below.

$$v(t) = \left(R_{ON}\frac{w(t)}{D} + R_{OFF}\left(1 - \frac{w(t)}{D}\right)\right) i(t) \tag{2.1}$$

$$\frac{dw(t)}{dt} = \mu_d \frac{R_{ON}}{D} i(t) \tag{2.2}$$

where $v(t)$ and $i(t)$ are the time varying analog input voltage and current through memristor, respectively.

By solving Eq. 2.1 and 2.2, the following relationship for $w(t)$ can be derived.

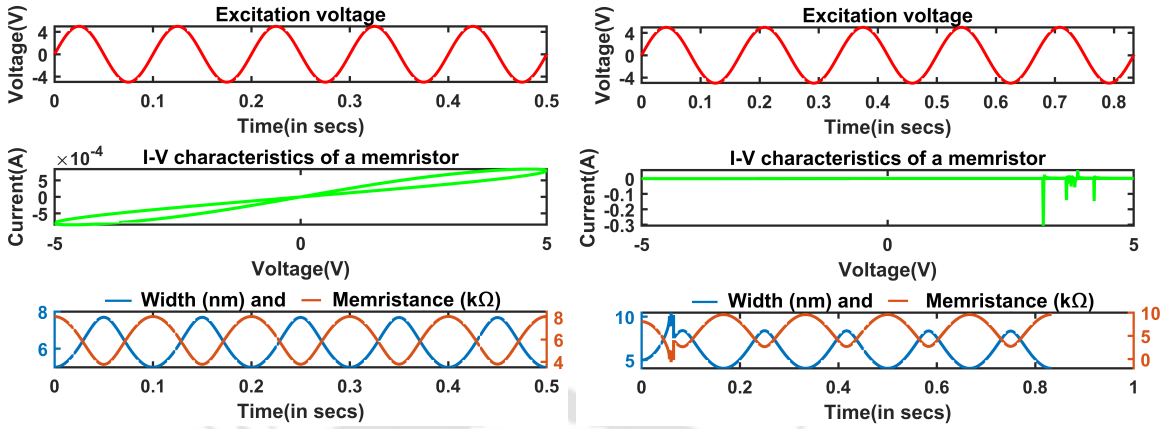
$$w(t) = \mu_d \frac{R_{ON}}{D} q(t) \tag{2.3}$$

By employing Eq. 2.1 and 2.3, the memristance of the memristor can be estimated. Considering $R_{ON} \ll R_{OFF}$, the above equations can be simplified to the following mathematical expression.

$$R_{mem} = M(q) = R_{OFF}\left(1 - \frac{\mu_d R_{ON}}{D^2} q(t)\right) \tag{2.4}$$

Eq. 2.2 represents drift velocity is inversely proportional to the thickness of bilayer structure D. Further, in eq. 2.4, memristance is the function of charge $q(t)$ and mobility of dopant μ_d.

Fig. 2.3(a) exhibits an analytical study of the linear ion drift model of a memristor when it is excited with a sinusoidal signal having 5 V amplitude and 10 Hz frequency. The parameters of the



(a) (b)

Figure 2.3: Numerical analysis of a memristor using linear ion drift model (a) PHL for sinusoidal signal having 5 V amplitude and 10 Hz frequency and (b) limitation

linear ion drift model of TiO_2 memristor [3] are selected as $D = 10\ nm$, $R_{ON} = 100\ \Omega$, $R_{OFF} = 16\ k\Omega$ and $\mu_d = 10^{-14}\ m^2 s^{-1} V^{-1}$, as mentioned in [3]. These values are obtained experimentally by Stanley William et al. [3] and are employed for validating the setup of the critical analysis of the standard window functions.

Note that this model is neither accurate nor suitable for studying the nonlinear behaviour of the memristor because a uniform electric field is assumed for an applied voltage. In the nanoscale device, slight variations in the voltage lead to a very high nonlinear electric field. Therefore, the linear ion drift model fails to generate PHL due to a nonlinear electric field and exceeds boundary conditions beyond the actual width of the device $(0, D)$, as shown in Fig. 2.3(b).

2.3 Prior art work of window functions

Strukov et al. [3] proposed a linear ion drift model that works on linear ion transport. Therefore, the window function is incorporated in the linear ion drift model to achieve nonlinearity and to keep the transportation of ions within the physical dimension of the device. Hence, boundary conditions are satisfied for the correct functional behaviour of the model to realize the physical memristor accurately.

The mathematical equation for the linear ion drift model with a window function is mentioned below.

$$\frac{dx(t)}{dt} = \mu_d \frac{R_{ON}}{D^2} i(t).f(x) \tag{2.5}$$

The necessity of applying the window function in the linear ion drift model is described below.

- For retaining the dimension of the device within the boundary between two electrodes of the memristor for any mode of conduction.
- For providing nonlinear variations in the dopant drift kinetics of the active layer of the memristor.
- Utilizing control parameters to adjust scalability and nonlinearity for generating PHL without distortion depending on the applied voltage and frequency.
- The window function $f(x)$ must be within the range $0 \leq f(x) \leq 1$ for proper functioning of memristor.

The well-known standard window functions used by the scientific community in modelling a memristor are explained below. Note that the numerical study of a memristor using these standard window functions is performed using MATLAB.

2.3.1 Joglekar window function

This window function [81] introduces nonlinearity in the linear drift model by accommodating boundary effects. Here, the rate of change of normalized width, $x = \frac{w}{D}$, i.e. the dopant velocity, is assumed to be a function of x. The mathematical formulation of this window function is presented in Eq. 2.6.

$$f(x) = 1 - (2x - 1)^{2p} \tag{2.6}$$

where p is a positive integer and can be used as a control parameter to adjust the nonlinearity and scalability of the memristor.

The numerical analysis of a memristor employing the Joglekar window function is performed using a sinusoidal signal having a peak value of 0.1 V and 0.05 Hz frequency as input. The outcome of this analysis is exhibited in Fig. 2.4(b), which validates the correctness of the Joglekar window function. It can be observed that PHL is successfully generated using a memristor employing the Joglekar window function. Also, the change in width and memristance can be realized with sinusoidal excitation.

The absence of scalability in the Joglekar window function can be seen in Fig. 2.4(a). Even if p increases, the maximum value of the window function remains constant at 1, which is illustrated in this figure. Further, the memristor model with the Joglekar window function becomes linear as p attains higher values.

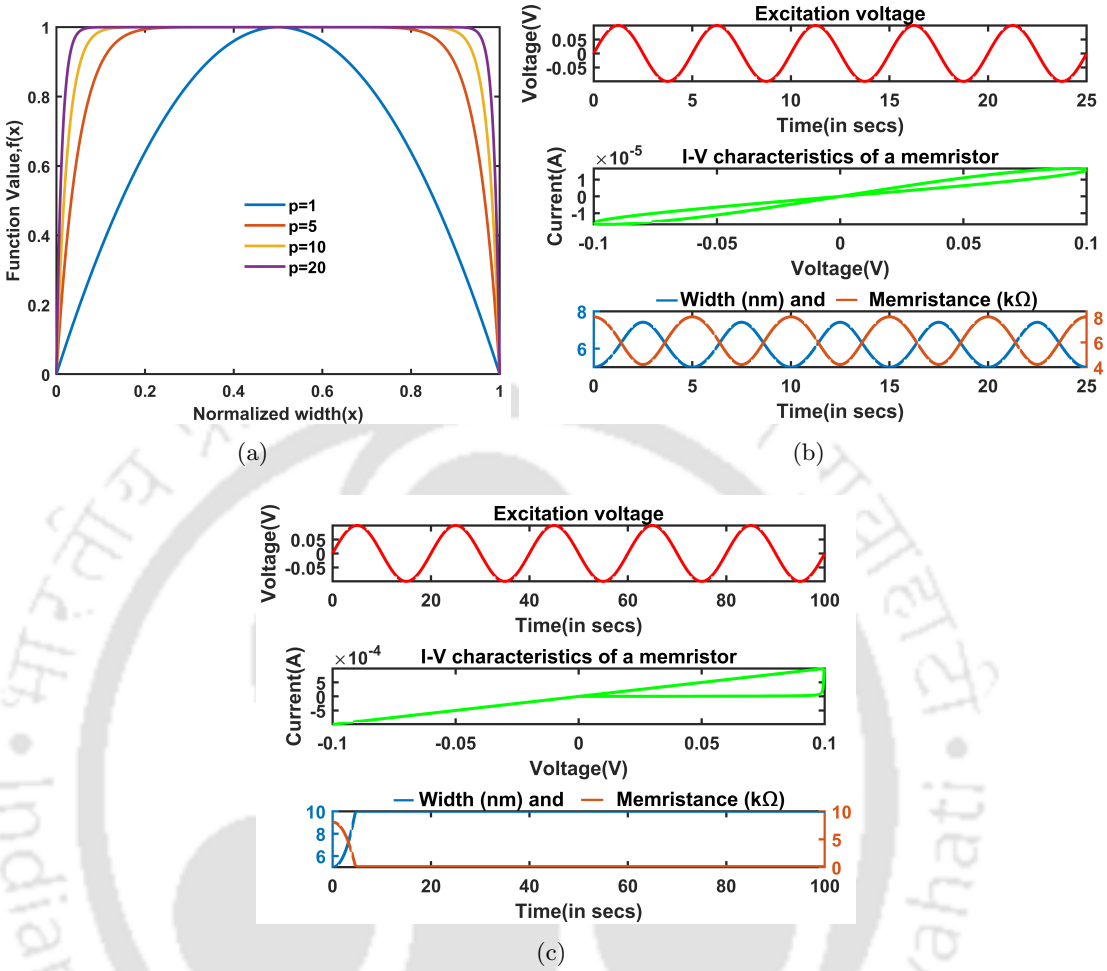


Figure 2.4: Analytical results of linear ion drift memristor model using Joglekar window function (a) at different values of p parameter (b) PHL generation and (c) limitation

It can be observed in Fig. 2.4(c) that the Joglekar window function suffers from boundary lock issues. This arises when w, the width of the memristor, reaches either minimum or maximum during the OFF or ON state of the memristor, respectively. This further saturates memristance M, even if the applied voltage at a given frequency varies. It also distorts PHL because the memristor becomes resistive after reaching maximum memristance. When the polarity of an input signal is reversed due to a boundary lock issue, the memristor behaves like a pure resistor. Therefore, other window functions are investigated to address this issue, which is depicted in the following sections.

2.3.2 Biolek window function

The mathematical model of the Biolek window function [82] is expressed in Eq. (2.7).

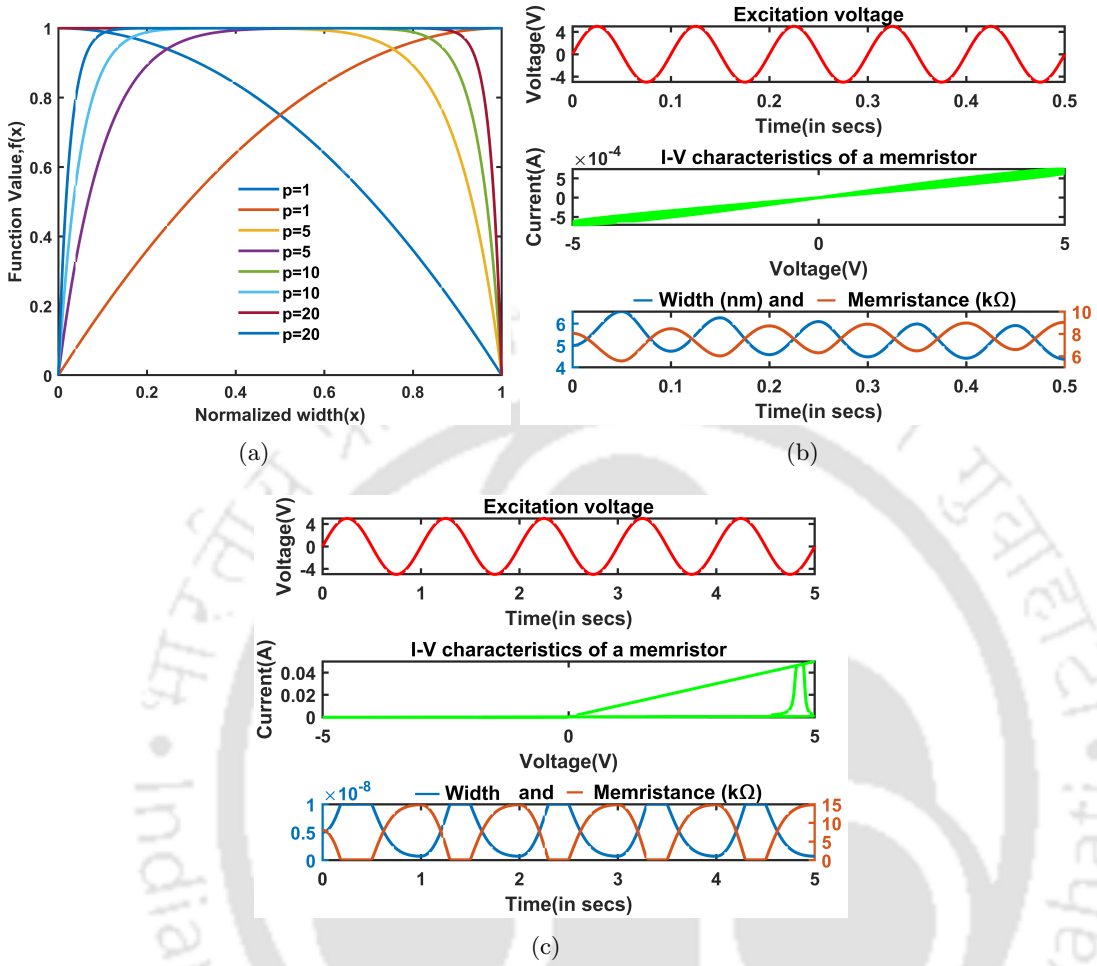


Figure 2.5: Analytical results of linear ion drift memristor model using Biolek window function (a) at different values of p parameter (b) PHL generation and (c) limitation

$$f(x) = 1 - (x - stp(-i))^{2p} \tag{2.7}$$

This window function includes the current i flowing through the memristor. The i increases with an increase in the width of the doped layer for $x \to 1$. However, the current is zero at each side of the device boundary, represented as follows.

$$stp(i) = \begin{cases} 1 & i \geq 0 \\ 0 & i < 0 \end{cases} \tag{2.8}$$

This window function incorporates the direction of current flow through the memristor for overcoming the boundary lock issue. Different functional values are obtained for the same value of p, as

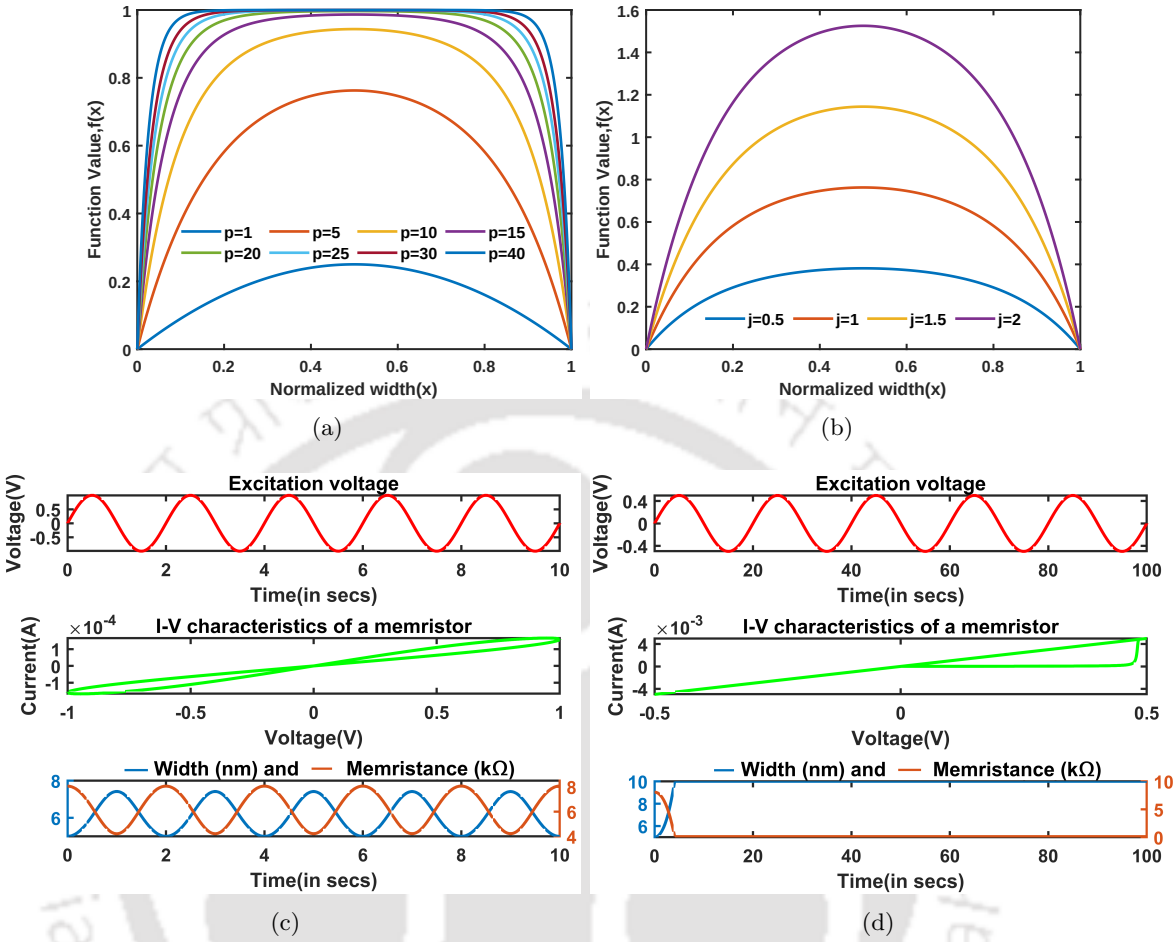


Figure 2.6: Analytical results of linear ion drift model using Prodromakis window function (a) at different values of p parameter (b) at different values of j parameter (c) PHL generation and (d) limitation of the Prodromakis window function

depicted in Fig. 2.5(a). The boundary lock problem is resolved by ensuring the width can be returned to the restricted range of $[0, 1]$. It helps in getting the boundary conditions satisfied.

Fig. 2.5(b) illustrates that this window function with the linear ion drift model generates PHL for a limited range of voltages and frequencies. The PHL for this window function exhibits strong distortion instead of a boundary lock problem due to voltage and frequency exceeding the allowable range, as shown in Fig. 2.5(c). Although the Biolek window function resolves the boundary lock issue, the scalability and nonlinearity remain poor. It is further validated by Fig. 2.5(a), highlighting the max value of $f(x)$ to be constant at 1. The window functions described in the following sections address the issue of scalability and nonlinearity to a larger extent.

2.3.3 Prodromakis window function

The mathematical model of the Prodromakis window function [83] can be formulated as

$$f(x) = j(1 - ((x - 0.5)^2 + 0.75)^p) \tag{2.9}$$

Here, control parameters p and j are employed to achieve scalability and nonlinearity. The numerical analysis is performed for the linear ion drift model using the Prodromakis window function by applying a sinusoidal input signal, as illustrated in Fig. 2.6(c). The control parameter p increases scalability as well as nonlinearity, which is shown in Fig. 2.6(a), whereas j increases the value of $f(x) \geq 1$, which is shown in Fig. 2.6(b). Thus, control parameters offer scalability and nonlinearity to a considerable extent as compared to previously reported window functions.

The memristor with the Prodromakis window function is numerically analyzed by applying a sinusoidal signal. The PHL generated by this analysis is presented in Fig. 2.6(c).

Although this window function provides better scalability and nonlinearity than Joglekar and Biolek window functions, PHL generated in this analysis is distorted due to the limited range of voltages and frequencies and is shown in Fig. 2.6(d). The boundary lock issue of the Prodromakis window function also contributes to this distortion, which can be observed in Fig. 2.6(d). The limitations imposed by this window function are addressed by the Jinxiang window function, which is explained in the next section.

2.3.4 Jinxiang Window Function

Considering the current i flowing through the memristor, a new window function is derived by Jinxiang et al. [84]. Its mathematical formulation is shown below.

$$f(x) = j(1 - (0.25(x - stp(-i))^2 + 0.75)^p) \tag{2.10}$$

where step function of current $stp(i)$ is given as follows.

$$stp(i) = \begin{cases} 1 & i \geq 0 \\ 0 & i < 0 \end{cases} \tag{2.11}$$

where, p and j are control parameters, and i is the current flowing through the memristor. Note that this window function resolves the issue of boundary lock due to introducing the ***stp*** function and

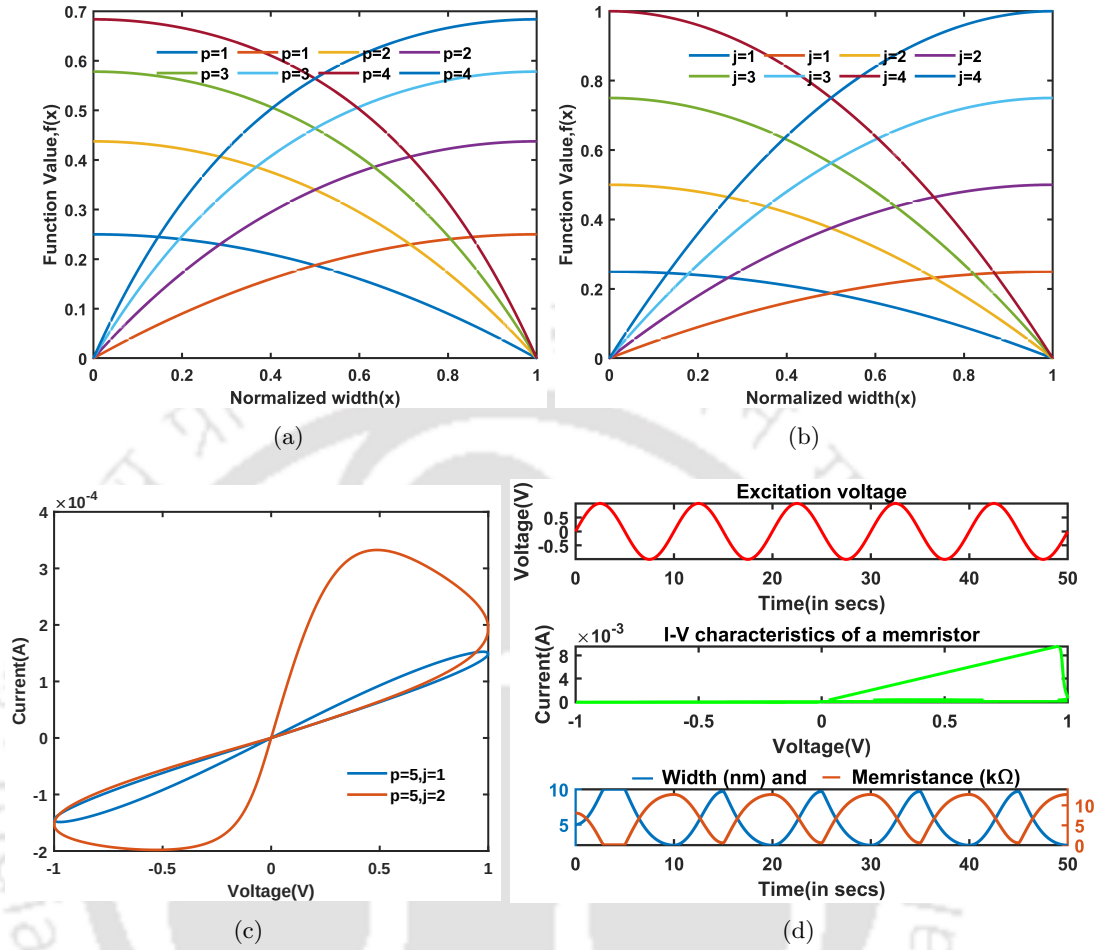


Figure 2.7: Analytical results of linear ion drift model using Jinxiang window function (a) at different values of p parameter (b) at different values of j parameter (c) PHL generation at various j and fixed p and limitation of Jinxiang window function

retains all the advantages of the Prodromakis window function.

The PHL generated with the Jinxiang window function is shown in Fig. 2.7(c) for two different values of j and a fixed p. Figs. 2.7(a) and 2.7(b) illustrate scalability and nonlinear properties of Jinxiang window function for different values of p and j, respectively. Although this window function offers scalability, nonlinearity and no boundary lock issue, the presence of strong distortion, as shown in Fig. 2.7(d), indicates their limited scope. It leads to the Jinxiang window function with the linear model generating PHL for a limited voltage and frequency range. Hence, it limits the usage of the Jinxiang window function in various applications.

2.4 Proposed dynamic window function

The previous window functions have several advantages but fail at critical voltages and frequencies. The main problem these window functions encounter is the narrow range of voltages at a particular frequency. It is due to the coefficient of x^{2p} becoming constant for any p irrespective of x. Experimentally, nonlinearity becomes stronger near boundaries in real memristors. It motivates us to depict a new approach in this work, which introduces desired nonlinearities in the proposed window function. One of the approaches is to choose the coefficient of x^{2p} as a function of x for any p. This coefficient is termed as ϵ_0, which is dynamic in nature and changes with x. This parameter is also called *Error Parameter*, and as a new dynamic parameter, it boosts the range of the previous window functions to a large extent. Note that any function of x can be utilized for the said purpose, but a monomial function of x is chosen for simplicity.

Moreover, this function is to be discontinuous to ensure that the maximum value of the window function remains only at the centre, where the boundary effects are absent. Further, a new term *order* is also introduced in our proposed window function as an exponent of j, essential for generating PHL at high frequencies. Note that the standard window functions require very high values of j to generate PHL at high frequencies. For example, at $f = 1\ MHz$, the Jinxiang window function requires j to be $5 * 10^5$. The introduction of *order* as an exponent of j eliminates these issues.

In this work, we propose a novel window function for addressing various issues in the standard window functions, and its detailed description is given below.

2.4.1 Mathematical model of the proposed window function

The mathematical formulation of the proposed window function incorporating a dynamic parameter is derived below.

Let the window function for $p = 1$ and $j = 1$ be $g(x)$, and the slope of the proposed window function is $\frac{dg(x)}{dx}$.

Assuming,

$$\frac{dg(x)}{dx} = A - \epsilon x \tag{2.12}$$

Integration of Eq. 2.12 results into the following mathematical expression.

$$g(x) = Ax - \epsilon\frac{x^2}{2} + B \tag{2.13}$$

Rearranging Eq. 2.13 yields,

$$g(x) = \frac{A^2}{2\epsilon} + B - \frac{\epsilon}{2}\left(x - \frac{A}{\epsilon}\right)^2 \tag{2.14}$$

In Eq. 2.14, A, B, and ϵ are the constants, which can be determined using the following steps. We know that,

$$g(1) = g(0) = 0$$

B and A can be estimated using this condition as $B = 0$ and $A = \frac{\epsilon}{2}$, respectively. Then Eq. 2.14 transforms into the following expression.

$$g(x) = \frac{\epsilon}{8} - \frac{\epsilon}{2}\left(x - \frac{1}{2}\right)^2 \tag{2.15}$$

Eq. 2.15 can further be simplified as mentioned below.

$$g(x) = 1 - \left[\frac{\epsilon}{2}\left(x - \frac{1}{2}\right)^2 + 1 - \frac{\epsilon}{8}\right]^1 \tag{2.16}$$

$$g(x, p, j, order) = j^{order}\left(1 - \left[\frac{\epsilon}{2}\left(x - \frac{1}{2}\right)^2 + 1 - \frac{\epsilon}{8}\right]^p\right) \tag{2.17}$$

Replacing $\epsilon_0 = \frac{\epsilon}{2}$ in Eq. 2.17 and declaring it as *Error Parameter*, Eq. 2.17 can be formulated as stated below.

$$g(x, p, j, order, \epsilon_0) = j^{order}\left(1 - \left[\epsilon_0\left(x - \frac{1}{2}\right)^2 + 1 - \frac{\epsilon_0}{4}\right]^p\right) \tag{2.18}$$

It can be seen in Eq. 2.18, with $\epsilon_0 = 1$, Eq. 2.18 reduces to the Prodromakis window function. It exhibits that previously defined window functions can be derived using the proposed window function by choosing suitable values of *Error Parameter*. A behavioural study of the *Error Parameter* is given below so that it can be defined appropriately.

2.4.1.1 Behavioral Analysis of *Error Parameter*

For studying the dynamic behaviour of the *Error Parameter*, the following observations are made at low and high voltages for a particular frequency.

The window function mentioned below may be chosen at **low voltages** to generate PHL. It is because the maximum value of the window function is needed to obtain desired PHL at low voltages. Thus, the proposed window function mentioned in Eq. 2.19 allows memristor width to rise faster at low voltages; otherwise, PHL becomes a straight line.

$$g(x, p, j, order, \epsilon_0) \approx j^{order} \tag{2.19}$$

Further, substituting Eq. 2.19 to 2.18 leads to the mathematical expressions depicted below.

$$1 - \left[\epsilon_0 \left(x - \frac{1}{2}\right)^2 + 1 - \frac{\epsilon_0}{4}\right]^p \approx 1 \tag{2.20}$$

$$\left[\epsilon_0 \left(x - \frac{1}{2}\right)^2 + 1 - \frac{\epsilon_0}{4}\right]^p \approx 0 \tag{2.21}$$

For $x \approx \frac{1}{2}$, ϵ_0 becomes approximately 4. Thus, for $\left|x - \frac{1}{2}\right| < c_1$, where c_1 is a constant, $\epsilon_0 \to 4$ enables memristor utilizing the proposed window function to generate a PHL at the low voltages.

It is to mention that c_1 should be chosen appropriately through numerical simulations, so that desired device characteristics can be obtained at low voltages.

Similarly, at **high voltages**, the following window function may be chosen to generate PHL.

$$g(x, p, j, order, \epsilon_0) \approx j^{order}\delta \tag{2.22}$$

where $\delta \to 0$, but $\delta \neq 0$. Here, δ is the residue of function $g(x, p, \epsilon_0)$, when $x \to 0$ or $x \to 1$.

The condition mentioned above helps avoid boundary lock problems as much as possible. The boundary lock problem is avoided in the memristors employing our proposed window function at high voltages if the window function generates a value as close as zero but not the absolute zero. Further, substituting equation 2.22 into 2.18 reduces it to the mathematical expression below.

$$1 - \left[\epsilon_0 \left(x - \frac{1}{2}\right)^2 + 1 - \frac{\epsilon_0}{4}\right]^p \approx \delta \tag{2.23}$$

Eq. 2.23 can be further simplified to the following equations.

$$\left[\epsilon_0 \left(x - \frac{1}{2}\right)^2 + 1 - \frac{\epsilon_0}{4}\right]^p \approx 1 - \delta \tag{2.24}$$

$$\epsilon_0 \left(x - \frac{1}{2}\right)^2 + 1 - \frac{\epsilon_0}{4} \approx (1 - \delta)^{\frac{1}{p}} \tag{2.25}$$

Using binomial expansion for fractions and forcing the condition that x should not reach 0 or 1 quickly to avoid boundary lock for a large range of voltages, it is imperative to have $\epsilon_0 \to 0$ for $\delta \to 0$. Thus, in general, it can be stated that for $\left|x - \frac{1}{2}\right| > c_2$, where c_2 is a constant, $\epsilon_0 \to 0$ aids in generating desired PHL at high voltages.

Similar to c_1, c_2 should also be chosen appropriately so that desired characteristics of the memristor can be obtained at high voltages. It can be selected by analyzing the outcome of numerical simulations.

2.4.1.2 Definition of *Error Parameter*

The *Error Parameter*, which makes our proposed window function operate in a broader range of voltages and frequencies compared to earlier approaches, is described below. Note that this definition is derived using inferences from the analytical results presented in the previous section.

$$\epsilon_0(x) = \begin{cases} 3.99, & \left|x - \frac{1}{2}\right| < 0.4 \\ 0.01, & \left|x - \frac{1}{2}\right| \geq 0.4 \end{cases} \tag{2.26}$$

2.4.1.3 Condition for *Error Parameter*

The essential conditions derived with respect to ϵ_0 for modelling the proposed window function are as follows. It is found through numerical analysis of our proposed window function that the two distinct values of ϵ_0 are required at low and high voltages. At low voltages, ϵ_0 is closer to 4, while at high voltages, it is near 0.

2.4.2 Definition of the proposed window function

Based on the above mathematical analysis, the proposed novel window function with the dynamic parameter can be defined using the following expression.

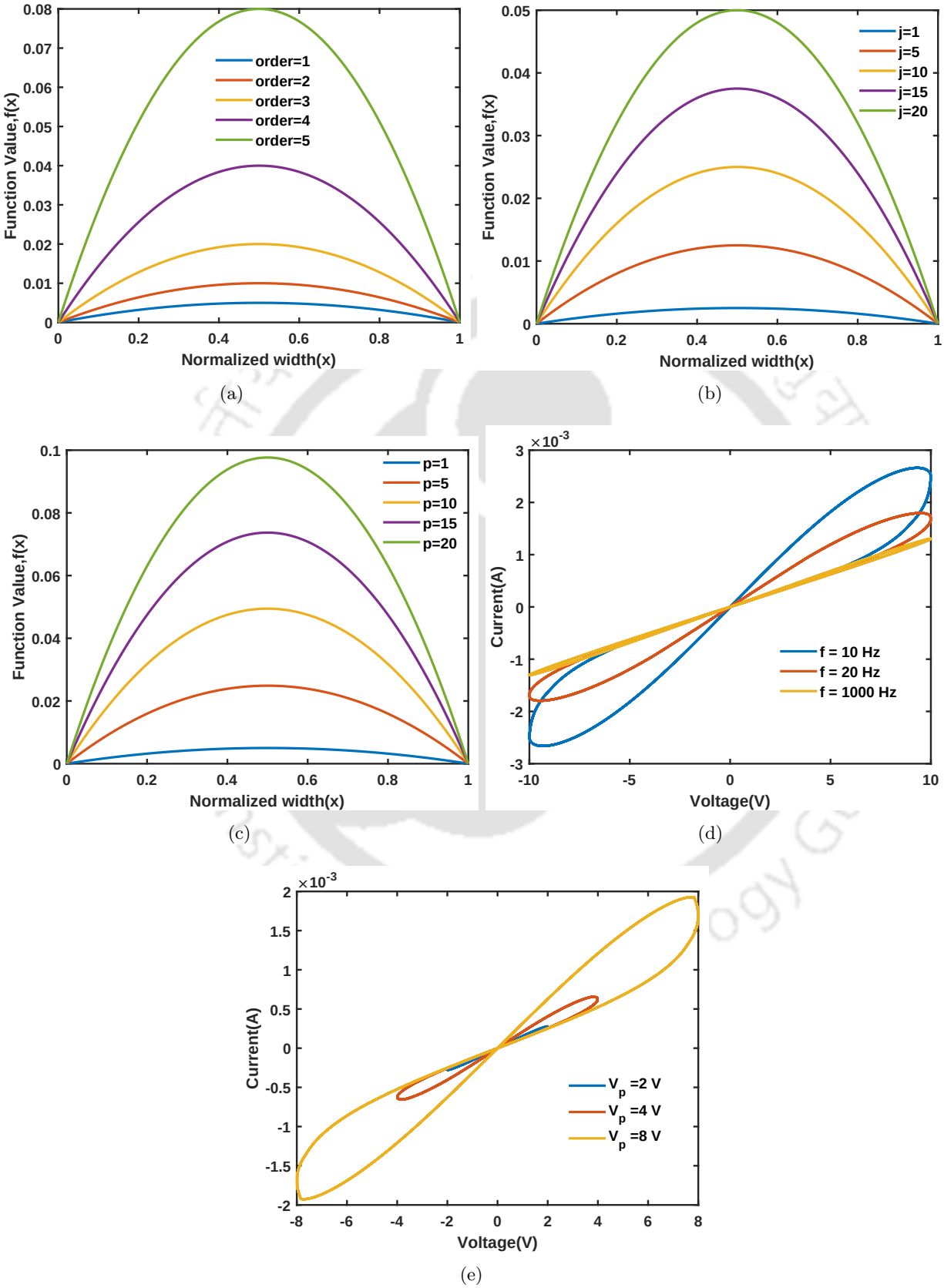


Figure 2.8: Parametric variation analysis of the proposed window function (a) at different values of *order* parameter (b) at different values of j parameter (c) at different values of p parameter (d) PHL at different operating frequencies and (e) PHL at different operating voltages

$$g(x, p, j, order, \epsilon_0) = j^{order}\left(1 - \left[\epsilon_0\left(x - \frac{1}{2}\right)^2 + 1 - \frac{\epsilon_0}{4}\right]^p\right)$$

where p, j, and $order$ are static parameters, ϵ_0 is a dynamic parameter termed as $Error\ Parameter$. This window function may be employed with the linear memristor model for the analysis of the properties of a memristor.

2.5 Parametric analysis of the proposed window function

This section presents a parametric study of the proposed window function and its comparison with other state-of-the-art methods.

2.5.1 Scalability of the proposed window function

Scalability is an essential aspect of a window function. It enables a window function to adapt to changing scenarios and perform as expected. The proposed window function is scalable with respect to all the static parameters, j, p, and $order$. As we know, the control parameters p and j are utilized in the proposed window function to retain advantages exhibited by other window functions. The scalability of the proposed window function is studied by performing its numerical analysis. In this study, only one parameter varies at a time, while other static parameters are kept at unity.

Fig. 2.8(a) exhibits the proposed window function when the $order$ is varied, keeping $j = 2$ and $p = 1$. Fig. 2.8(b) illustrates window functions at different values of j, while p and $order$ are fixed at unity. Finally, Fig. 2.8(c) showcases window functions when p is changed, having j and $order$ at unity. By varying controlled parameters, valid characteristics of the window function can be obtained. It indicates the scalability of the proposed window function, which is expected so that it can be employed in the linear model of the memristor to design various applications.

2.5.2 Analysis of memristor characteristics using proposed window function

It is utilized in the linear ion drift model of a memristor to validate the efficacy of our proposed window function. Later, numerical analysis is performed at different frequencies keeping the applied voltage constant, which results in the generation of the PHL, as shown in Fig. 2.8(d). This has the following observations as well. First, the $I - V$ characteristics contain a pinched hysteresis loop and second, an increase in the frequency decreases the lobe area of the hysteresis loop. It can also be anticipated that a further increase in the frequency would transform $I - V$ characteristics into a

linear function. These observations constitute vital fingerprints [85] of the memristor incorporating our proposed window function and validate its effectiveness.

Further, it can be seen that an increase in the voltage increases the current flowing through the memristor at the same frequency. This leads to an increase in the lobe area of PHL, as illustrated in Fig. 2.8(e). Thus, it can be said that at a specific voltage, the desired PHL can be obtained by tuning the static parameters of the memristor so that it can be utilized appropriately.

2.5.3 Comparative analysis of the window functions

Table 2.1 demonstrates the performance of various state-of-the-art and proposed window functions at various frequencies. This analysis employs a sinusoidal excitation of 5 V while varying the frequency. Through this analysis, it is ascertained whether a window function can generate PHL at different frequencies using static parameters, such as p, j and other parameters efficiently or not.

Table 2.1: Comparison of window functions at various frequency

Author	Year	Window function	1 Hz	10 Hz	100 Hz	1 KHz	1 MHz
Strukov et al.	2008	Strukov [3]	No	Yes	No	No	No
Joglekar et al.	2009	Joglekar [81]	Yes	Yes	No	No	No
Biolek et al.	2009	Biolek [82]	No	Yes	Yes	No	No
Prodromakis et al.	2011	Prodromakis [83]	Yes	Yes	Yes	Yes	Yes
Jinxiang et al.	2015	Jinxiang [84]	Yes	Yes	Yes	Yes	Yes
Ananda et al.	2023	**Proposed**	Yes	Yes	Yes	Yes	Yes

Table 2.1 exhibits that only Prodromakis, Jinxiang and the proposed window function can generate PHL for all the frequencies by tuning parameters accordingly. However, large values of j are needed for the first two window functions compared to ours. This comparison is depicted in Table 2.2 below.

Table 2.2: Control parameter j at different window functions at various frequencies

Author	Year	Window function	1 Hz	10 Hz	100 Hz	1 KHz
Prodromakis et al.	2011	Prodromakis [83]	0.5	2	20	220
Jinxiang et al.	2015	Jinxiang [84]	1	5	35	350
Ananda et al.	2023	**Proposed**	1	1	3	20

Table 2.2 highlights that previous window functions have limited nonlinearity leading to high dependence on large values of j as frequency increases. Our proposed window function owing to enhanced nonlinearity, requires nominal values of the control parameters. Note that large values of j lead to precision errors in the numerical analysis. Further, the significance of the dynamic parameter

used in the proposed window function is to eliminate the requirement of high values of parameters during numerical analysis at high frequencies. This makes the proposed window function the most suitable candidate for analyzing memristors in various frequencies.

2.6 Adaptive window function

We propose a novel window function incorporating an additional adaptive constant parameter. The features of the proposed adaptive window function are higher nonlinearity, scalability, and a longer range of voltage and frequency operations. The adaptive constant parameter introduces intelligence in the window function to estimate applied voltage and frequency for realizing the nonlinear behaviour of the memristor correctly. This aids in producing the desired PHL without any distortion. The key contributions of the proposed window function are as follows.

- The proposed window function incorporated with Adaptive constant (A_D) works for a higher voltage and frequency range than the standard window functions reported in the literature.
- No need to change any static parameters for operating voltage or frequency change.
- Not require a high value of j for higher frequency due to adaptive nonlinear behaviour.

2.6.1 Proposed adaptive window function

As we know, every device model has advantages and limitations. It is found in the literature that a memristor window function can be improvised further to depict realistic behaviour at a wide range of voltages and frequencies. Among many limitations imposed by the memristor model using various window functions [81–84, 86], producing a desired pinched hysteresis loop (PHL) by these window functions only in the range of 0.5 Hz to 100 Hz. Therefore, there is a need to extend the frequency and the voltage range of the memristor. This work presents a memristor model using a proposed window function to obtain desired PHL in a broader frequency and voltage range. The working mechanism and mathematical modelling of the proposed window function are described as follows.

2.6.2 Mathematical model of adaptive window function

An adaptive window function based memristor model is proposed. Initially, it evaluates the frequency and amplitude estimation of the applied input. Our proposed window function introduces

a new parameter for estimating the frequency and amplitude of the applied input signal. This new parameter is called an *Adaptive_constant*.

Also, the window function [83] is modified to achieve high nonlinear characteristics of a memristor and the mathematical expression for the new window function is formulated as follows.

$$f(x) = A_D \left[\left(1 - \frac{1}{2(e-1)} \right) \left(e^{\left((x-1)^{2q}-1\right)} + e^{\left(x^{2q}-1\right)} \right) \left(1 - \left((x-0.5)^2 + 0.75 \right)^p \right) \right] \tag{2.27}$$

where q and p are control parameters and A_D is an adaptive constant.

Now we have to analyze how the adaptive constant should change to get a pinched hysteresis loop for the chosen voltage and frequency range. According to an experiment, we have seen that using the expression in Eq. 2.28 for the adaptive constant gives a pinched hysteresis loop for the amplitude range (V_L, V_H) and the frequency range (f_L, f_H). The observed result of the analysis is presented in Table 2.3.

Table 2.3: Analysis of adaptive constant

Voltage (V) ***(in V)***	**Frequency (f)** ***(in Hz)***	**Golden ratio** $(\frac{f}{v})$	**Optimal value of** A_D
100	10	0.1	0.105
100	1	0.01	0.011
10	100	10	10.25
10	10	1	0.975
10	0.1	0.01	0.01075
1	100	100	100
1	10	10	10
0.1	100	1000	1000
0.1	10	100	100

As seen in Table 2.3, the optimal value of the adaptive constant, in any case, is approximately equal to the "golden ratio", defined as the ratio of frequency of the sinusoid and the amplitude of the sinusoid. The expression for Adaptive Constant (A_D) is given by the following mathematical expression.

$$A_D = \frac{estimated\ min.\ frequency\ of\ input}{estimated\ min.\ amplitude\ of\ input} \tag{2.28}$$

The detailed analysis and mathematical formulation of the proposed Adaptive Constant (A_D) are described in the following section.

2.6.3 Formulation of adaptive constant

The I-V characteristic of the device being nonlinear is due to different values of $\frac{\delta v}{\delta i}$ at different points of the curve. In the case of a memristor, its pinched hysteresis loop is generated because of different values of $\frac{\delta v}{\delta i}$ at different points of the curve, as stated in below mathematical model.

$$\frac{\delta v}{\delta i} = M(x) = [R_{off} - (R_{off} - R_{on})x] \tag{2.29}$$

The derivative of state variable x is described by the following mathematical expression.

$$\frac{dx(t)}{dt} = \mu_v \frac{R_{on}}{D^2} i(t) f(x) \tag{2.30}$$

To ensure the swing of the variable x is optimum, we have to ensure that the output of $f(x)$ needs to be compensated to a larger value when the pinched hysteresis loop starts to shrink to a straight line or it starts to lose its nonlinear behaviour (which happens when a low-amplitude and high-frequency input is applied). Alternatively, in order to compensate for the output of $f(x)$ to a smaller value, when the pinched hysteresis loop becomes too nonlinear and starts to become distorted (which happens when a high-amplitude and low-frequency input signal is applied). Therefore, encapsulation of the Adaptive Constant (A_D) in Eq. 2.28 with the proposed window function for memristor modelling to generate the desired PHL.

The mathematical expression of $AdaptiveConstant(A_D)$ is derived by considering an estimation of the maximum possible swing of the state variable x when the frequency f (Time-Period, $T = 1/f$) and amplitude A_m for an input signal $A_m \sin(2\pi f t)$. The range of window function and memristance is as follows,

- The range of the proposed window function is (0, *Adaptive_constant*), i.e., $0 < f(x) <$ Adaptive constant (A_D).
- The range of memristance is $R_{on} \leq M(x) \leq R_o ff$.

Consider the swing of the state variable x is Δx. Now, Δx can be approximated by the following expression.

$$\Delta x = 2 \int_0^{T/2} \frac{dx}{dt} dt \tag{2.31}$$

$$\Delta x = 2\int_0^{T/2} \mu_v \frac{R_{on}}{D^2} i(t) f(x) dt$$

$$\Delta x = 2\int_0^{T/2} \mu_v \frac{R_{on}}{D^2} \frac{v(t)}{M(x)} f(x) dt$$

$$\Delta x \leq 2\int_0^{T/2} \mu_v \frac{R_{on}}{D^2} \frac{v(t)}{R_{on}} f(x) dt$$

$$\Delta x < 2\int_0^{T/2} \mu_v \frac{A_m \sin(2\pi f t)}{D^2} f(x) dt$$

$$\Delta x < \frac{2\mu_v A_m A_D}{D^2} \int_0^{T/2} \sin(2\pi f t) dt$$

$$\Delta x < \frac{2\mu_v A_m A_D}{\pi f D^2}$$

Therefore,

$$(\Delta x)_{\max} \approxeq \frac{2\mu_v A_m A_D}{\pi f D^2} \tag{2.32}$$

From Eq. 2.32, we make $Adaptive\_constant = \frac{f}{A_m}$; the memristor response will be appropriately scaled for sinusoid of any amplitude and frequency.

Also, by considering the physical realization of the memristor, it has a specified range of frequency and amplitude, which needs to be incorporated into our proposed *Adaptive_constant* to obtain its complete mathematical model as follows.

$$A_D = \frac{\min(f_H, \max(f_L, estimated\ \min.\ freq.\ of\ input))}{\min(v_H, \max(v_L, estimated\ \min.\ ampl.\ of\ input))}$$

2.6.4 Design methodology of memristor model using proposed window function

To estimate the frequency and amplitude of an input signal, we have designed a memristor model by using a diode and capacitor in series with a copy of the input signal (a copy of the input signal can easily be made using a voltage-dependent voltage source with gain=1) using LTSpice. Also, a capacitor of 1 F is connected in parallel with the input signal, and the current flowing through the capacitor becomes $dv/dt = 2\pi A_m f \cos(2\pi f t)$. Additionally, a CCVS with trans-resistance=1 Ω with current flowing through the capacitor as the controlling current. Then its output becomes $2\pi A_m f \cos(2\pi f t)$.

The estimated frequency value is obtained by dividing the peak amplitude of this voltage signal by $2\pi A_m$.

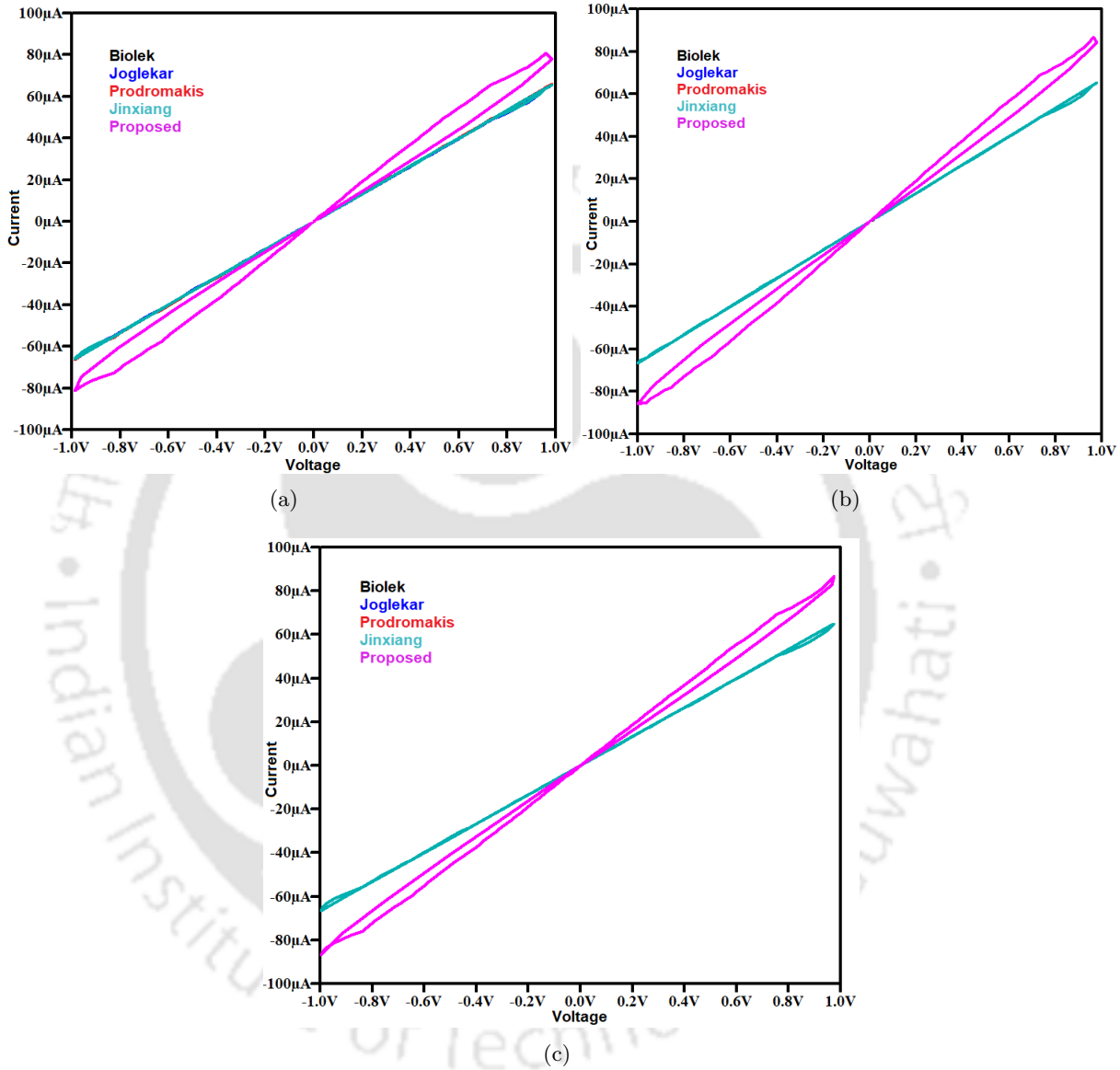


Figure 2.9: Numerical analysis of memristor model using different window functions with 1 V (a) PHL at 100 Hz (b) PHL at 1 kHz and (c) PHL at 10 kHz

2.7 Numerical analysis of the proposed window function

The numerical analysis of various window functions is performed using the LTSpice framework. As can be seen in Fig. 2.9, PHL (fingerprint of a memristor) is generated for various window functions [81–84] for different frequencies in the range of 100 Hz to 10 kHz at 1 V. However, PHL is generated

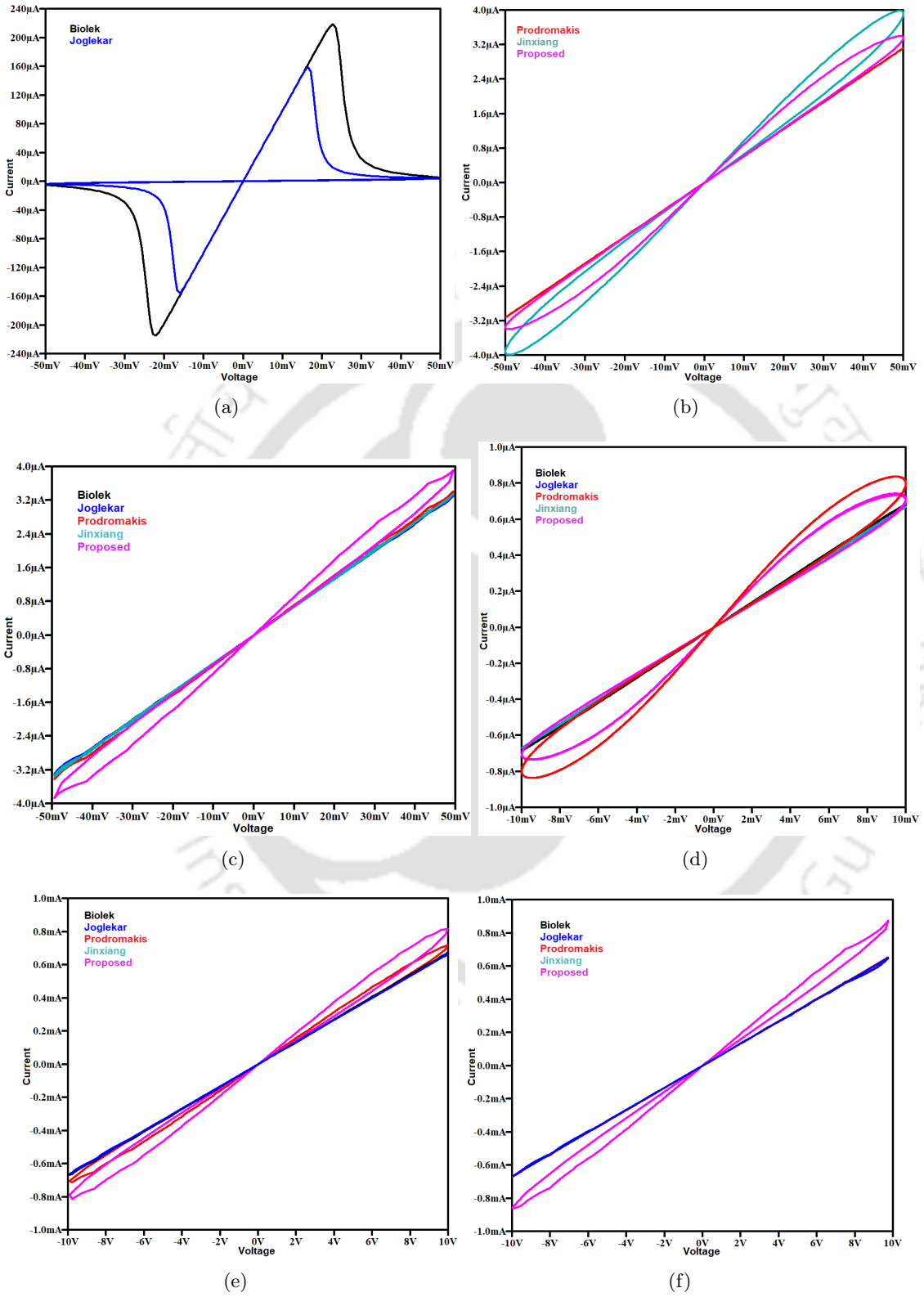


Figure 2.10: Numerical analysis of memristor model using different window functions (a) PHL using Biolek and Joglekar at 0.05 V and 0.01 Hz (b) PHL using Prodromakis, Jinxiang, and Proposed at 0.05 V and 0.01 Hz (c) PHL at 0.05 V and 1 Hz (d) PHL at 0.01 V and 0.05 Hz (e) PHL at 10V and 100 Hz and (f) PHL at 10 V and 1 kHz

Table 2.4: Comparison of different window functions

Window functions	**[3]**	**[81]**	**[82]**	**[83]**	**[84]**	**Proposed**
Scalability	No	Limited	Limited	Moderate	Moderate	**High**
Nonlinearity	Limited	Limited	Limited	Moderate	Moderate	**High**
Boundary lock	Yes	Yes	No	Yes	No	**No**
Operating voltage and frequency range	Limited	Limited	Limited	Moderate	Moderate	**High**

only for memristor model using a proposed window function at varied ranges of frequencies, as depicted in Fig. 2.9 and the lobe area of PHL starts shrinking when the frequency increases from 100 Hz to 10 kHz, which verifies the correctness of memristor behaviour [87] using a proposed window function. The functionality of different window functions is also verified for low voltage and low frequency range, as shown in Fig. 2.10. The distorted PHL is generated at 0.05 V and 0.01 Hz using Biolek and Joglekar, as shown in Fig. 2.10(a). No PHL is generated for the Prodromakis window function. However, PHL is generated for the Jinxiang and proposed window functions, as shown in Fig. 2.10(b). Increasing frequency to 1 Hz at 0.05 V, PHL is generated only for the proposed window function, as illustrated in Fig. 2.10(c). By reducing voltage to 0.01 V at frequency 0.05 Hz, PHL is generated for Prodromakis and proposed window functions, as depicted in Fig. 2.10(d). Applying a high voltage of 10 V at 100 Hz, PHL is generated slightly for the Prodromakis window function, and PHL of high lobe area is generated for the proposed window function, which is shown in Fig. 2.10(e). A stable PHL is generated only for the proposed window function at high voltage of 10 V with increased frequency up to 1 kHz, as shown in Fig. 2.10(f). The results of the numerical analysis show that the memristor model using the proposed window function generates PHL for different frequency ranges from 0.01 Hz to 10 kHz due to the incorporation of the *Adaptive_constant* (A_D), which further enhances the scalability and nonlinearity. Therefore, our proposed window function based memristor model provides desirable I-V characteristics for a higher range of voltage and frequency without any degradation compared to other approaches presented in Table 2.4.

2.8 Conclusion

The main features of the memristor model using the proposed window functions are higher nonlinearity, scalability, and adaptability. The dynamic window is simpler than the adaptive window function but requires j and *order* parameters to vary whenever the applied frequency changes. However, the

adaptive window function has four new user-defined parameters: V_L, V_H, f_L, and f_H, respectively. hus, it provides a PHL for a much broader amplitude and frequency range because the user can define the voltage and frequency range using those newly introduced parameters. For instance, our proposed window function based memristor model can provide a pinched hysteresis loop for 0.01 Hz to 10 kHz frequency than all other state-of-the-art window functions. The advantages of the proposed window functions are mentioned as follows.

- The adaptive constant (A_D) and dynamic parameter (ϵ_0) aid in enhancing the nonlinear behaviour of the memristor model compared to other window functions.
- No need to adjust any static parameters for any applied voltage or frequency variation.
- Not require a high value of j for higher frequency due to adaptive nonlinear behaviour.

Thus, the proposed window functions are substantially flexible for obtaining the desired characteristics of a memristor, which can be further employed to design a wide range of potential applications.

3

Memristor Emulator

Contents

Objective:

Implementation and analysis of a floating memristor emulator utilizing a minimum number of off-the-shelf components for area-efficient and low-power applications operating at high frequencies.

3.1 Introduction

The technique of realizing the behaviour of a memristor using existing components is termed as memristor emulation [19]. The key principle mechanism of memristor emulation is to exhibit three important fingerprints [87], viz., (1) $I-V$ characteristic exhibiting pinched hysteresis loop (PHL), (2) lobe area of PHL increases when frequency decreases, (3) lobe area shrinks as frequency increases and $I-V$ curve becomes linear at the maximum frequency.

A summary of existing memristor emulators is depicted in Table 3.1 for ready reference. It can be seen in Table 3.1 the need of the hour is to design a simple and efficient memristor emulator for its wider applicability in low to high frequency applications. Thus, it is imperative to employ a minimum number of existing nonlinear discrete devices with as few passive elements as possible to mimic the behaviour of a memristor. Not only will this enable optimizing the area, power, and delay of the memristor emulator, but it will also increase the feasibility of its integration with other circuit elements. The increasing demand for high-performance and low-power devices motivated us to propose a novel memristor emulator using four metal oxide semiconductor field effect transistors and an external capacitor. The novelty of the proposed emulator is depicted below.

The key features of the proposed emulator [92] are listed as follows.

(i) It needs four n-channel MOSFETs, which makes it suitable for monolithic IC fabrication

(ii) It is more area efficient than other emulators reported in the literature

(iii) The simplicity of the proposed emulator facilitates easy integration with other circuits/devices for designing potential applications to exploit key properties of the memristor

(iv) Unlike other emulators, the proposed emulator works without external bias

Numerical analyses of the proposed emulator for various parameters are conducted using Cadence Virtuoso EDA framework and TSMC 180 nm technology. Additionally, the post-layout simulation is performed to validate the correctness of the proposed memristor emulator. Further, the efficacy of

Table 3.1: Summary of existing memristor emulators

Ref., Year	Components used	Hardware Implementation	Power Consumption	Operating Frequency
[24], 2014	1OTA, 2CFOA, 3R, 2C	Complex	High	Low
[20], 2012	2Opamps, 1Multiplier, 2R, 1C			
[21], 2015	4CCIIs, 1Multiplier, 2R, 1C			
[22], 2014	4CCIIs, 1Multiplier, 1OPAMP, 8R, 1C			
[28], 2015	2CCIIs, 1Multiplier, 2R, 1C			
[29], 2017	1CCII, 1Multiplier, 1R, 1C			
[30], 2017	1MO-OTA, 1Multiplier, 1R, 1C			
[25], 2017	1CBTA, 1Multiplier, 2R, 1C			
[88], 2014	3CFOAs, 4R, 2C, 1D			
[27], 2016	3OTAs, 4CCIIs, 6R, 1C	Complex	Moderate	Low
[89], 2017	1OTA, 2Transistors, 1C			
[23], 2014	1DDCC, 1 Multiplier, 2R, 1C	Complex	High	High
[26], 2017	1DVCCTA, 1OTA, 3R, 1C			
[31], 2018	CCTA, CCII, 3R, 1C	Complex	-	High
[90], 2018	1VDTA, 1Multiplier, 2R, 1C			
[91], 2020	1OTA, 1CDTA, 1C			

Here, "-" represents no data available for the references given.

the proposed memristor emulator is validated by implementing memristor-based applications. Note that the proposed memristor emulator is realized physically using ALD1106 n-channel MOSFETs, which generates a pinched hysteresis loop as per our expectation at various frequencies. This further corroborates the correctness of the proposed memristor emulator topology.

This chapter is organized as follows. Section 3.2 presents detailed circuit analysis and mathematical formulation of the proposed memristor emulator. Section 3.3 describes performance analysis of the proposed emulator. Applications of our emulator is discussed in Section 3.4. Finally, section 3.5 concludes this chapter.

3.2 Proposed MOS-DTMOS memristor emulator

The main objective of this work is to realize the behaviour of the memristor using MOS transistors and an external capacitor. The proposed memristor emulator also incorporates a DTMOS, which is formed by connecting body of a MOSFET to its gate terminal. The circuit configuration and mathematical analysis of the proposed memristor emulator are discussed in this section.

3.2.1 DTMOS Transistor

A MOSFET should ideally have a high threshold voltage V_t at $V_{GS} = 0$ to achieve low leakage and low V_t at $V_{GS} = V_{DD}$ to achieve high speed. It is desired to have low leakage and high speed for improving the performance of a MOSFET at very low voltages. A *Dynamic Threshold voltage MOSFET* (DTMOS) is used to overcome these constraints by connecting gate and body terminals of a MOSFET. Note that the DTMOS transistor exhibits high threshold when it is off to minimize the leakage, whereas it presents a low threshold under low voltage supplies to drive high current. It also exhibits steeper subthreshold swing and higher carrier mobility than the conventional MOSFET. Due to dynamic body bias voltage, the threshold voltage (V_t) of the MOS transistor becomes a function of the input signal [93]. With an input signal applied at the gate terminal, body bias changes dynamically with the change in the input. Thus, $V_{GS} = V_{BS}$ is maintained as gate and body terminals are shorted together [94]. Note that the source-body junction gets slightly forward biased when the gate input of a MOSFET increases, but its V_t decreases because of the body effect. Due to dynamic body bias, gate and body terminals control potential in the channel region, leading to a high transconductance, which drives a faster current into the channel. As we know, threshold voltage of a DTMOS transistor can be modeled using Eq. 3.1 [95].

$$V_t = V_{t_0} + \gamma \left(\sqrt{|2\psi_S + V_{SB}|} - \sqrt{|2\psi_S|} \right) \tag{3.1}$$

Here, γ, ψ_S, and V_{SB} are the body effect coefficient, surface potential, and the voltage between the source and body. In the proposed memristor emulator, DTMOS transistor helps in the realization of memristor behaviour at different operating frequencies. This further aids in achieving the maximum operating frequency of the proposed memristor emulator. An analytical study of this emulator is given below.

3.2.2 Design and analytical model of the proposed emulator

Fig. 3.1(a) depicts the symbol of a memristor. An equivalent circuit emulating a memristor (emulator) is shown in Fig. 3.1(b). This memristor emulator consists of four MOSFETs and an external capacitor. Two MOSFETs, $M1$ and $M2$, are connected in parallel and are biased in the linear region, which converts the quadratic relationship between current and voltage into linear relationship to form an electronically tunable resistance. The gates of other MOSFETs, $M3$ and $M4$, are connected

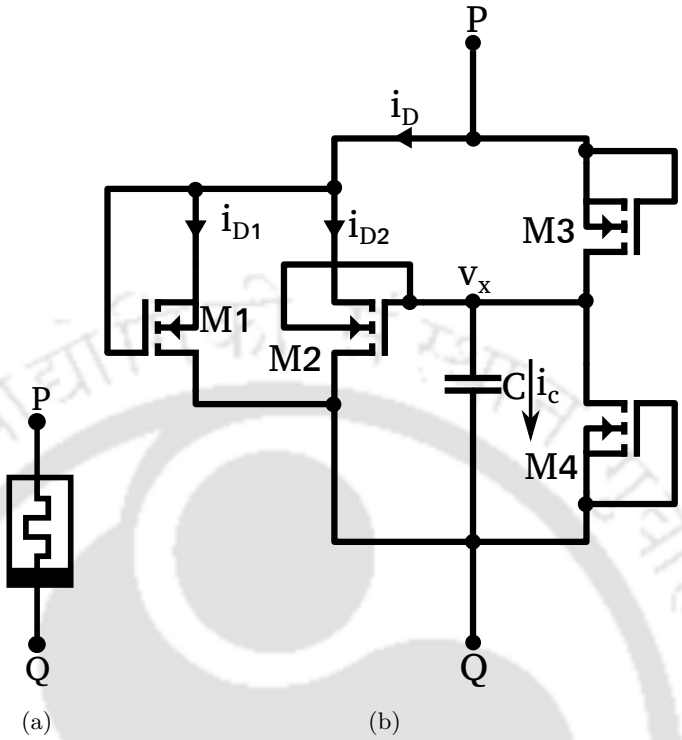


Figure 3.1: (a) Memristor symbol and (b) proposed MOS-DTMOS circuit topology for memristor emulator

to drain, which force them to operate in the saturation region. This forms a feedback system that samples the input voltage difference and controls the gate of $M2$. Note that $M2$ is configured as DTMOS. The threshold voltage of $M2$ varies dynamically with respect to the change in the input voltage change, which helps obtain the stable and desired characteristics of a memristor. A capacitor C is used to convert current into voltage, and is connected to the gate terminal of $M2$. It helps in exhibiting the non-volatile property of a memristor because there is no path for the drain current to flow through capacitor to the gate of $M2$. A detailed analysis of the proposed memristor emulator is given below.

The variable resistance of $M1$ and $M2$ can be obtained by adding the currents passing through these MOSFETs operating in the triode region and is expressed by Eq. 3.2.

$$i_D = i_{D1} + i_{D2} \tag{3.2}$$

After simplifying Eq. 3.2, the following mathematical expression is obtained.

$$i_D = k_{1,2}\left(V_{GS_{1,2}} - 2V_{t_{1,2}}\right) v_{PQ} \tag{3.3}$$

Here, $k_{1,2}$ is the process parameter of $M1$ and $M2$. V_{GS} and v_{PQ} are the voltage across the gate and source terminals of a MOSFET, and a time-varying input voltage is applied between terminals P and Q. The resistance of $M1$ and $M2$ can be derived as follows.

$$r_{ds_{1,2}} = \frac{1}{k_{1,2}\left(V_{GS_{1,2}} - 2V_{t_{1,2}}\right)} \tag{3.4}$$

By applying Kirchhoff's current law at node v_x, the current flowing through the capacitor is given by Eq. 3.5.

$$i_c = i_{M_3} + i_{M_4} \tag{3.5}$$

After substituting the current flowing through the capacitor, $M3$ and $M4$, Eq. 3.5 can be described as mentioned below.

$$C\frac{dv_x}{dt} = k_3\left(V_{GS_3} - V_{t_3}\right)^2 + k_4\left(V_{GS_4} - V_{t_4}\right)^2 \tag{3.6}$$

As mentioned above, the time-varying input voltage across two floating terminals, P and Q, of the memristor emulator is v_{PQ}. Thus, V_{GS_3} and V_{GS_4} are $\frac{v_{PQ}}{2}$ and $-\frac{v_{PQ}}{2}$, respectively. Considering $\frac{k_3}{k_4} = \frac{kM}{kN}$ and $V_{t_3} = V_{t_4} = V_t$, then Eq. 3.6 can be depicted as,

$$\begin{aligned} C\frac{dv_x}{dt} = Mk\left(\frac{v_{PQ}}{2} - v_x - V_t\right)^2 \\ +Nk\left(\frac{-v_{PQ}}{2} - v_x - V_t\right)^2 \end{aligned} \tag{3.7}$$

Here, $k = \mu_n C_{ox}\left(\frac{W}{L}\right)$, the common process parameter of $M3$ and $M4$, whereas M and N are constants. Eq. 3.7 can be further expressed as,

$$C\frac{dv_x}{dt} = k(M+N)v_x^2\left[4\left[1-\frac{(v_{PQ}+V_t)}{4v_x} + \frac{(v_{PQ}+V_t)}{2v_x}\right]^2 + \frac{3V_t^2}{4v_x^2} - \frac{(3M-N)}{2(M+N)}\left(\frac{v_{PQ}V_t}{v_x^2}\right) + \frac{\left(\frac{N-M}{M+N}\right)v_{PQ}+2V_t}{v_x} - 3\right] \tag{3.8}$$

After simplifying Eq. 3.8, node voltage v_x can be obtained as stated below.

$$C\frac{dv_x}{dt} = 2kv_x^2\left[\frac{v_{PQ}}{2v_x} + \frac{5V_t}{2v_x} - 3\right] \tag{3.9}$$

or,

$$\frac{1}{v_x^2}\frac{dv_x}{dt} = \frac{k}{C}\left(\frac{v_{PQ}+5v_t}{v_x}\right) - \frac{6k}{C} \tag{3.10}$$

Choosing $y = v_x^{-1}$, Eq. 3.10 can be formulated as,

$$\frac{dy}{dt} + \frac{k}{C}(v_{PQ}+5v_t) = \frac{6k}{C} \tag{3.11}$$

Eq. 3.11 implies a perfect first-order linear differential equation as $\frac{dy}{dt} + Ey = F$, and its solution is given as

$$ye^{-\int Edt} = \int -Fe^{-\int Edt}dt + Z \tag{3.12}$$

Here, Z is an integration constant. By comparing Eq. 3.11 and Eq. 3.12 and substituting the value of E and F, Eq. 3.12 can be formulated as mentioned below.

$$ye^{-\int \frac{k}{C}(v_{PQ}+5V_t)dt} = \int \frac{6k}{C}e^{-\int \frac{k}{C}(v_{PQ}+5V_t)dt}dt + Z \tag{3.13}$$

After solving Eq. 3.13, y can be approximated as,

$$y \approx Ze^{-\int \frac{k}{C}\left(v_{PQ}+5V_t\right)dt} \tag{3.14}$$

As we know, $\varphi(t) = \int (v_{PQ} + 5V_t)\, dt$, v_x can be formulated using Eq. 3.14 as mentioned below.

$$v_x \approx \frac{1}{Z} + \frac{k}{ZC}\varphi(t) \tag{3.15}$$

As mentioned above, the proposed memristor comprises of dynamic threshold MOS (DTMOS) transistor. The threshold voltage of DTMOS is depicted in Eq. 3.1 and can be simplified as illustrated in Eq. 3.16.

$$V_t \approx V_{t_0} + \alpha_{SB} V_{SB} \tag{3.16}$$

where, α_{SB} is body effect constant.

Substituting $M2$ gate voltage $V_{GS} = v_x$, input voltage $v_{PQ} = v_{in}(t)$, and DTMOS threshold voltage depicted in Eq. 3.16 to Eq. 3.3, the following mathematical expression for the proposed memristor emulator can be derived.

$$\frac{i_D}{v_{in}(t)} = k_{1,2}\left(1 + 2\alpha_{SB}\right) v_x \tag{3.17}$$

The above-mentioned mathematical expression states the memductance of a memristor, which can be further denoted as,

$$M^{-1}(\varphi(t)) = k_{1,2}(1 + 2\alpha_{SB}) \left(\frac{1}{Z} + \frac{k}{ZC}\varphi(t)\right) \tag{3.18}$$

Note that Eq. 3.18 converts linear resistance $r_{ds_{1,2}}$ of the MOSFET into the time-dependent drain to source resistance, which is used to emulate the characteristic behaviour of a memristor. The proposed memristor emulator also exhibits nonvolatility by storing charge in the capacitor.

For analyzing the frequency behaviour of the proposed memristor emulator, input excitation is considered as $v_{in}(t) = A_m sin(\omega t)$, where A_m and ω are its amplitude and operating frequency, respectively. Therefore, memductance of the proposed memristor emulator can be represented as mentioned below.

$$M^{-1}(\varphi(t)) = \underbrace{\frac{k_{1,2}(1+2\alpha_{SB})}{Z}}_{\text{linear time-invariant}} + \underbrace{\frac{k_{1,2}(1+2\alpha_{SB})kA_m cos(\omega t-\pi)}{ZC\omega}}_{\text{linear time-variant}} \tag{3.19}$$

Using Eq. 3.19, it can be observed, as frequency tends to infinity, the time-variant part of memductance becomes zero and behaves as a linear resistor. The time-dependent behaviour of the memristor can be obtained by Eq. 3.19, which is defined below.

$$\mathscr{A} \approx \frac{kA_m}{2\pi fC} = \frac{1}{\tau f} \tag{3.20}$$

Here,

$$\tau = \frac{2\pi C}{kA_m} \tag{3.21}$$

where τ is the time constant of the proposed emulator.

The time constant τ regulates the pinched hysteresis loop of the proposed emulator, and $T = 1/f$ is the period of excitation. τ is based on the parameters of circuit elements used in the memristor emulator. It can be changed according to the desired operating frequency. Only C can be changed effectively, whereas other parameters are considered constant. Therefore, the capacitor acts as a tuning parameter for τ. The following observations are derived using Eq. 3.20 and Eq. 3.21

- $\mathscr{A} \to 0$, when $f \to \infty$ or $A_m \to 0$, which drives the emulator to behave as a linear time-invariant resistor .
- $\mathscr{A} \to 1$, when $f \to 1/\tau$ or A_m is monotonically increased. In this case, the emulator generates maximum PHL to exhibit memristor behaviour.
- $\mathscr{A} \geq 1$, when $f \leq 1/\tau$ or A_m increases substantially, yielding distorted I-V characteristics.

3.2.3 Nonideal analysis

The proposed emulator employs ideal MOSFETs, but in reality, parasitic elements impact the behaviour of the memristor. The parasitic capacitances, resistances, and nonidealities are exhibited due to parameter mismatch of MOSFETs, affecting the overall performance and deviating the emulator

from its ideal behaviour.

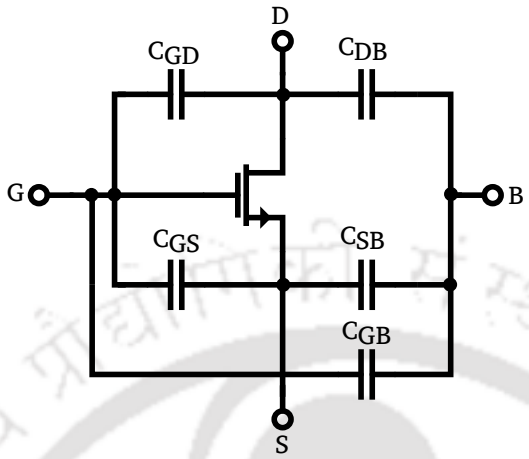


Figure 3.2: Parasitic capacitance in a MOSFET

As shown in Fig. 3.2, a MOSFET has parasitic capacitances due to charge in the depletion region and gate-to-source or gate-to-drain overlap. These capacitances exhibit dependence on source/drain voltage (biasing) in a MOSFET [95]. The equivalent capacitance of the proposed memristor emulator is $C_{eq} = C_{DB} + C_{GD} + C_{GS} + C = C_{par} + C$, where $C_{par} = C_{DB} + C_{GD} + C_{GS}$ is the parasitic capacitance and C is an external capacitor utilized in the proposed emulator. Let R_{par} denotes the parasitic resistance, then memductance can be expressed employing the following mathematical expression.

$$M^{-1}(\varphi(t)) = k_{1,2}(1 + 2\alpha_{SB}) \left(\frac{1}{Z} + \frac{k}{Z(Ceq)} \varphi(t) \right) + \frac{1}{R_{par}} \tag{3.22}$$

It can be observed that C_{par} affects memductance and with an increase in the frequency, the linear time-variant part of memductance becomes negligible. Therefore, it can be stated that the memductance of the circuit depends on the nonideal and parasitic components of the MOSFET.

Using the analytical model of the proposed emulator, numerical analysis is performed, and its characteristic is validated in various conditions while varying operating voltage and frequency and at different process corners, etc., which is described in the following section.

3.3 Performance analysis of the proposed memristor emulator

The numerical analysis of the proposed emulator is performed using TSMC 180 nm PDKs in Cadence Analog Design Environment, and its vital characteristics are verified extensively. Its detailed

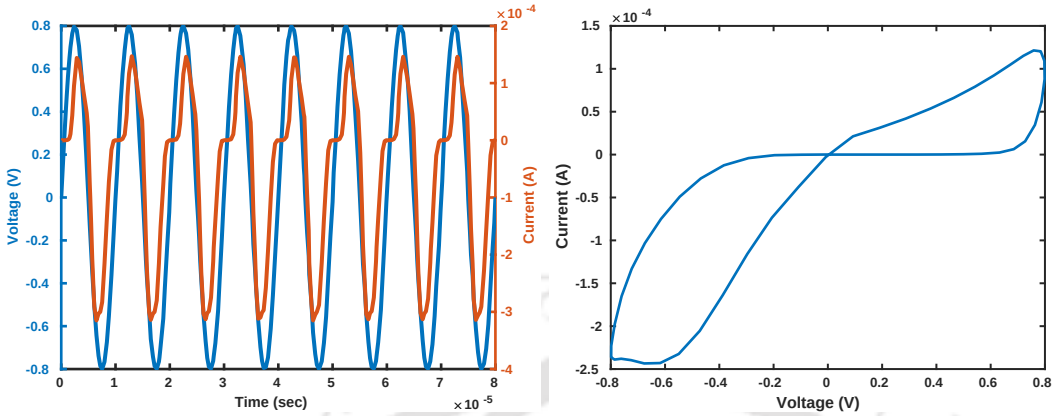
performance evaluation is described below.

3.3.1 Numerical analysis

The proposed memristor emulator is designed by choosing aspect ratios $(W/L)_1 = 220n/1\mu$, $(W/L)_2 = 40\mu/1\mu$, and $(W/L)_3 = (W/L)_4 = 1\mu/1\mu$. The sinusoidal input with a peak voltage of 800 mV and 100 kHz is applied to the terminals P to Q of the emulator. The transient response of the current flowing through the proposed emulator is shown in Fig. 3.3(a). The nonlinearity of the current waveform in the proposed memristor emulator demonstrates the nonlinear behaviour of memristors. This nonlinearity decreases with an increase in the frequency, and the memristive effect disappears [96, 97]. Fig. 3.3(a) exhibits a very little to no-phase shift between the current and the voltage, illustrating the memristor's resistive nature. Many earlier memristive devices, such as HP memristor models [3], do not show the nonlinear behaviour of the memristors. Hence, they illustrate a symmetrical current waveform. Although the HP memristor model enabled researchers to understand and analyze critical aspects of the memristor, it was later acknowledged that the HP model could not provide the actual nonlinear behaviour of the memristor [96]. The primary fingerprint of a memristor is the zero-crossing pinched hysteresis loop. The hysteresis lobe area of the first and the third quadrant may be unsymmetrical due to parasitic elements with the memristor emulator. These parasitic elements depend on the properties of the components used to mimic the memristor behaviour [98].

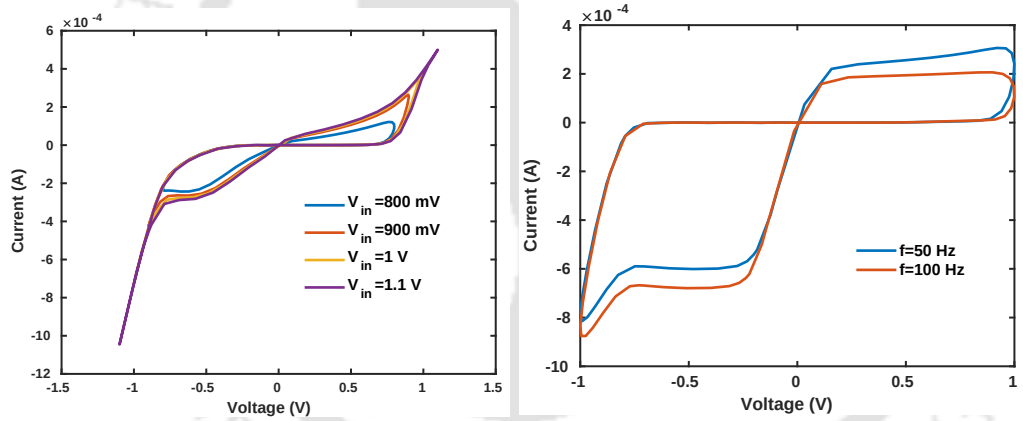
The physical memristor usually exhibits an unsymmetric PHL [99–101]. Similar unsymmetrical PHLs can also be observed in other emulators reported in the literature [27, 32, 102]. Therefore, the unsymmetrical current waveform shown in Fig. 3.3(a) of the proposed memristor emulator exhibits the nonlinear behaviour of the memristor and is due to the nonlinear characteristics of the MOSFETs and the parasitic elements [100, 103]. $I-V$ characteristics exhibiting nonlinear and nonvolatile properties of the memristor by generating a pinched hysteresis loop are depicted in Fig. 3.3(b). Further, PHLs of the proposed memristor emulator generated at different operating voltages are illustrated in Fig. 3.4(a). The lobe area of the PHL is directly proportional to the amplitude of the input voltage (A_m) and inversely proportional to its frequency (f), which is stated in Eq. 3.19 of the proposed emulator. The lobe area of the PHL increases with an increase in the amplitude of the applied voltage, as shown in Fig. 3.4(a). It can be observed that a higher amplitude of the input voltage causes a higher lobe area of the PHL, which verifies the correctness of the proposed memristor.

As we know, the external capacitor is employed for generating PHL at different operating frequen-

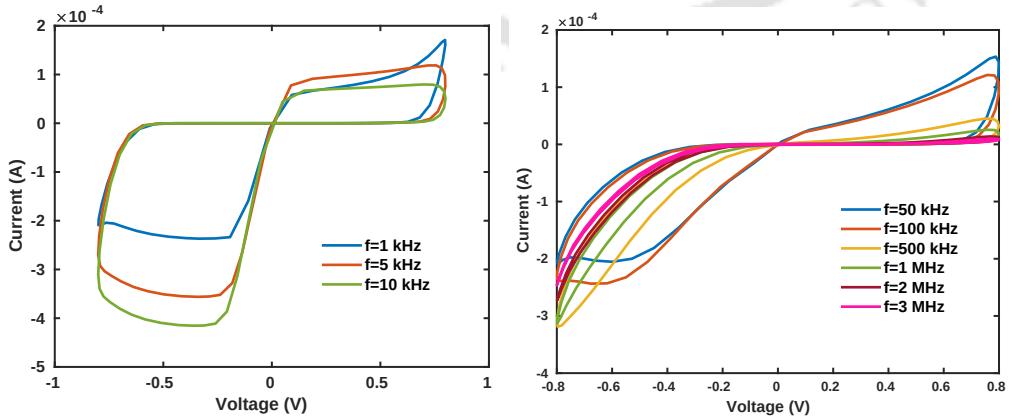


(a) (b)

Figure 3.3: (a) Transient response (b) $I-V$ characteristic (PHL) of a proposed memristor emulator



(a) (b)



(c) (d)

Figure 3.4: (a) PHLs at different input voltages and PHLs at different frequencies using (b) 10 nF, (c) 10 pF, and (d) 100 fF of a proposed memristor emulator

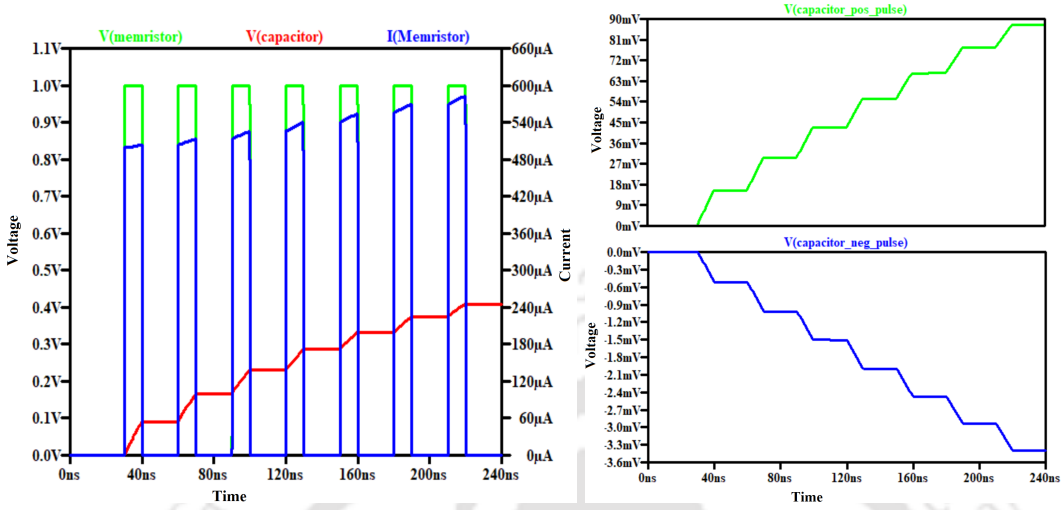
cies. The different external capacitors of 10 nF, 10 pF, and 100 fF are selected for low, medium, and high frequency operations. Fig. 3.4 exhibits the analytical results of the proposed memristor emulator at different operating frequencies using the capacitors mentioned above. It can be seen that upscaling the input frequency with smaller capacitors reduces lobe area of the PHL. Therefore, the proposed emulator validates important fingerprints of an actual memristor.

It can be observed in Fig. 3.5(a) that the current through memristor increases with respect to time. This change happens only when the pulse is ON. It can be seen that the voltage across the capacitor is proportional to memductance, which exhibits the nonvolatile property of the memristor. Since the voltage across the capacitor increases/decreases for the positive/negative pulse, as depicted in Fig. 3.5(b), in the absence of a voltage pulse, the memristor emulator retains previous information emulating the nonvolatile behaviour of an actual memristor.

The two memristors connected in series and parallel are used to the analyze characteristics of the proposed memristor emulator. It can be observed in Fig. 3.6(a) that PHL becomes a straight line due to an increase in the memristance when two memristors are connected in series. Similarly, PHL increases with a decrease in the memristance due to two memristors connected in parallel.

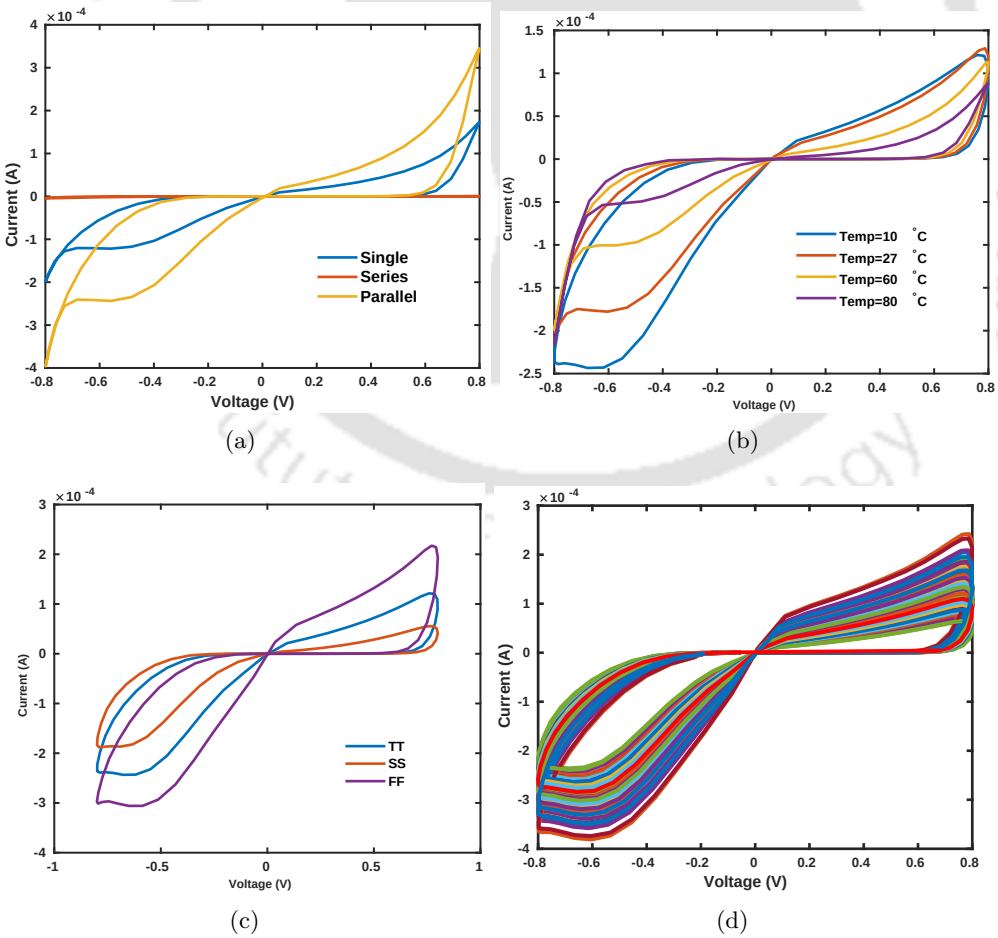
The correctness of the proposed memristor is evaluated by analyzing its behaviour at different process corners illustrated in Figs. 3.6(b) and 3.6(c). Its stability and reliability are validated at different process corners under varied temperature conditions. The PHL of our proposed memristor is generated without any distortion and is shown in Fig. 3.6(b) and Fig. 3.6(c). It can be seen that a rise in temperature reduces the current flowing through the memristor [104], which increases its memristance. It can also be seen in Fig. 3.6(b), the lobe area of PHL increases at low temperatures ($10°C$) and decreases at high temperatures ($80°C$). Further, the proposed memristor emulator is analyzed at different process corners, as shown in Fig. 3.6(c). The lobe area of the PHL varies with different process corners. Note that the proposed emulator consists of n-channel MOSFETs only, which directs us to choose FF, TT, and SS only to perform corner analysis. It can be seen in Fig. 3.6(c) that, at FF, the current through the proposed emulator is high, whereas, at SS, it is comparatively low. Thus, it can be summarized that the proposed emulator showcases stable and reliable behaviour at different temperatures for various process corners and illustrates its optimal characteristics at room temperature ($27°C$) for a typical (TT) process corner.

Monte Carlo analysis is employed to investigate the effect of process parameter variations and



(a) (b)

Figure 3.5: Transient response of the emulator using 1 pF capacitor employing an input pulse having 10 ns ON state and 40 ns time period of (a) 1 V amplitude, and (b) 0.4 V and -0.4 V amplitude



(a) (b) (c) (d)

Figure 3.6: PHLs of the proposed emulator at (a) series and parallel combination (b) different temperatures (c) different process corners and (d) Monte Carlo analysis

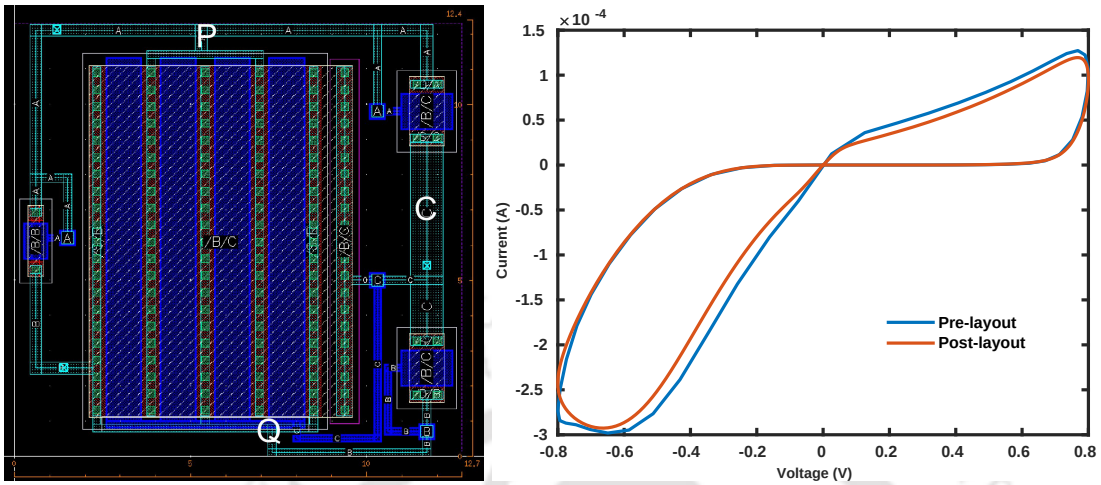
mismatch between transistors and to prove the robustness of the proposed emulator. The deviations in the parameters, such as aspect ratios, threshold voltages, capacitances, etc., are chosen as the uniform distribution within the tolerance limits of each parameter. By analyzing Fig. 3.6(d), it can be seen that the proposed emulator retains memristor behaviour by generating PHLs irrespective of the variations in the capacitance and device parameters exhibiting stable performance. It can be observed in Fig. 3.6(d) that the $I-V$ characteristic remains pinched at the origin, and the memristive nature is conserved. Note that the proposed memristor emulator provides stable PHL without any distortion up to the maximum operating frequency at 3 MHz.

3.3.2 Pre- and post-layout analysis

The physical design of the proposed memristor emulator is generated using the Cadence layout design platform employing TSMC 180 nm technology, as shown in Fig. 3.7(a). In this layout, there are three pins named P, Q, and C. P and Q are used to connect memristor emulator to an external input source, and C is connected to an external capacitor, which can be tuned with the frequency of input signal. Further, the post layout simulation is also performed to ensure reliable characteristic behaviour of the proposed emulator and the desired PHL is obtained, as shown in Fig. 3.7(b), which shows that there is a slight deviation in the post-layout PHL as compared to pre-layout PHL due to the effect of parasitic elements. The area and power utilization of the proposed emulator are estimated as 157.48 μm^2 and 8.24 μW, respectively. The DTMOS is an essential part of the proposed emulator. It reduces the circuit complexity and the number of MOSFETs required to design a memristor emulator. Due to this, the area utilization and the circuit complexity of the proposed memristor get reduced substantially. Note that the proposed memristor emulator consumes less area than most of the memristor emulators reported in the literature. The performance of the emulator presented in this work is validated experimentally, which is described below.

3.3.3 Experimental validation

The experiment to validate the memristive behaviour of the proposed memristor emulator shown in Fig.3.1(b) is performed by selecting suitable n-channel MOSFETs and capacitors. In this experiment, four ALD1106 n-channel MOSFETs [105] are employed. The capacitors of different values are chosen depending on the operating frequencies. Rigol DG1022 function generator is used to apply the sinusoidal input voltage to the proposed memristor emulator, and MDO3012 Mixed Domain Oscilloscope



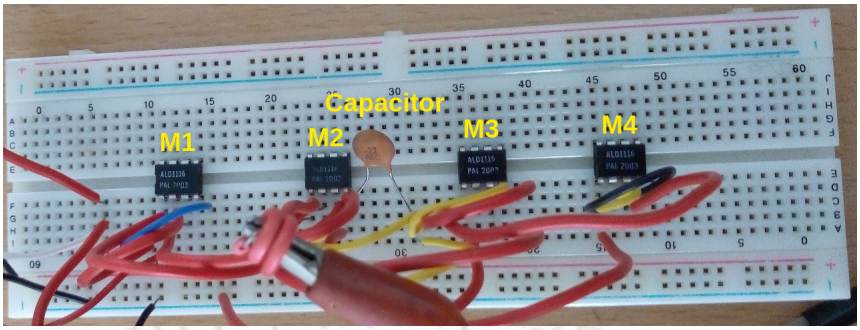
(a) (b)

Figure 3.7: (a) Layout design and (b) pre- and post-layout analyses of the proposed emulator

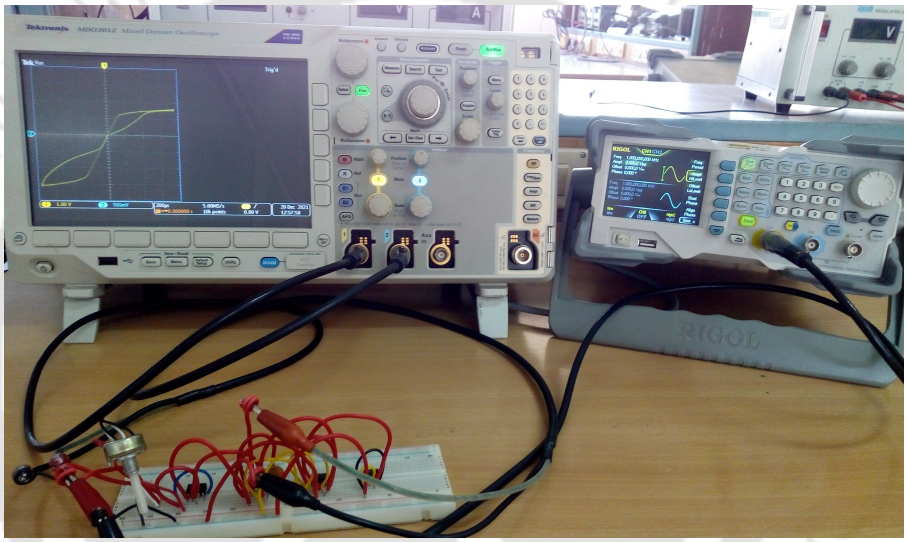
is utilized to observe the response of the memristor emulator.

The prototype of the proposed emulator circuit is assembled on a breadboard as depicted in Fig. 3.8(a), and its experimental setup is shown in Fig. 3.8(b). Transient response and $I-V$ characteristics of the proposed memristor emulator at an input having 1 V peak voltage and 500 Hz frequency using 0.22 μF capacitor is obtained, which is shown in Fig. 3.9(a) and Fig. 3.9(b), respectively. It can be observed that scaling the frequency to 1 kHz shrinks the lobe area of the PHL, which is illustrated in Fig. 3.9(c). Additionally, acceptable memristor behaviour is observed at different operating frequencies by selecting suitable capacitors. The outcome of this experiment states that an increase in frequency leads to reduce lobe area of the PHL, which is shown in Figs. 3.10 and 3.11. Note that the ALD1106 n-channel MOSFETs design parameters differ from those designed to realize the proposed emulator, employing TSMC 180 nm PDKs. Due to this, there is a difference in the shape of the PHLs of experimental analysis and the simulated results. It validates that the outcome of numerical and experimental analyses of the proposed memristor emulator is in coherence, which proves its correctness and reliability.

There are numerous memristor emulators [20–22,24–31,88–91,106] are available, which are designed using operational transconductance amplifiers (CA3080), Opamps, analog multipliers (AD633), second generation current conveyors (AD844) and other analog IC components. The hardware complexity of these emulators is high, and the operating frequency is limited in the kHz range. The other emulators [23, 31, 90, 91] are also configured using analog ICs and able to generate PHL in the range

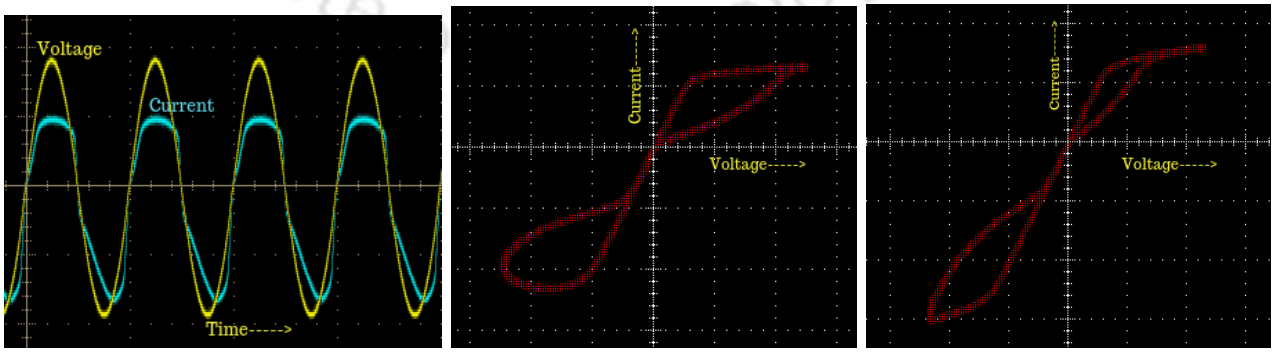


(a)



(b)

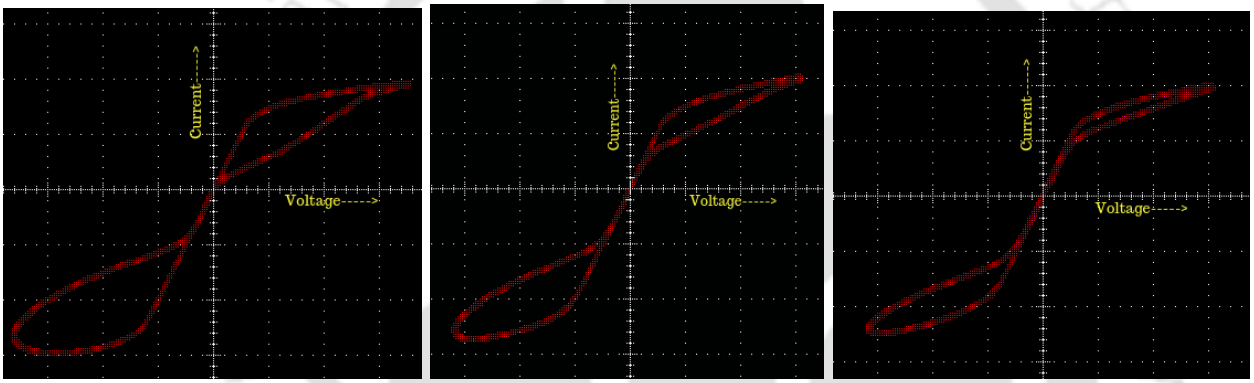
Figure 3.8: (a) Prototype circuit on breadboard and (b) experimental setup of the proposed emulator



(a) (b) (c)

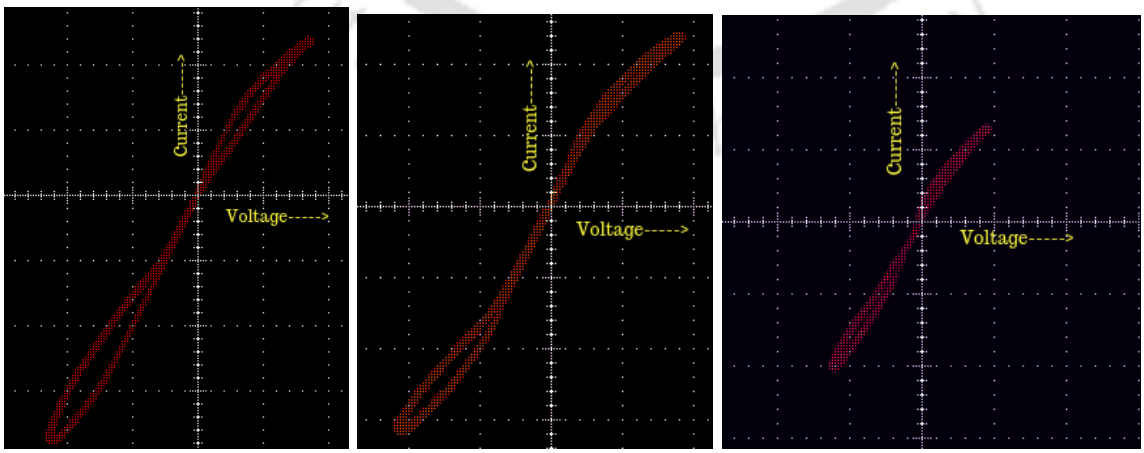
Figure 3.9: Proposed memristor emulator having 0.22 μF capacitor (a) transient analysis (b) PHL at 500 Hz (c) PHL at 1 kHz

of MHz, but these emulators require discrete analog ICs and passive components, which make them unsuitable for monolithic IC integration. The comparative analysis of the proposed emulator and other memristor emulators reported in the literature is shown in Table 3.2. It can be observed that our emulator consists of the least number of devices and is 592.2× more power efficient and, exhibits 3× better operating frequency range than [26]. Although [31] has a better operating frequency, but it utilizes more than 35 transistors to mimic memristive behaviour, and its power consumption is also higher. Similarly, [27] has the lowest power consumption, but its maximum operating frequency is only 10 kHz. Also, [89] has less power consumption than the proposed emulator, but its operating frequency is 30 Hz, which is the least among all the state-of-the-art emulators.



(a) (b) (c)

Figure 3.10: PHL of the proposed memristor emulator having 0.1 μF capacitor (a) at 8 kHz (b) at 16 kHz (c) at 25 kHz



(a) (b) (c)

Figure 3.11: PHL of the proposed memristor emulator having 4.7 nF capacitor (a) at 40 kHz (b) at 100 kHz (c) at 500 kHz

Table 3.2: Comparative analysis of proposed memristor emulator with available memristor emulators

Ref.	Active comp.	Passive comp.	Transistor counts	Sim./Exp.	Floating/ Grounded	Technology used	Power consumption	Max. operating freq.
[24]	1OTA, 2CFOA	3R, 2C	>56	Both	Grounded	-	260 mW	2 KHz
[20]	2OPAMPs, 1Multiplier, 10Transistors	2R, 1C	>150	Both	Grounded	-	1.81 W	800 Hz
[23]	1DDCC, 1 Multiplier	2R, 1C	50	Sim.	Floating	0.35 μm CMOS	74.5 W	1 MHz
[89]	1OTA, 2Transistors	1C	16	Sim.	Floating	0.18 μm TSMC	8.05 μW	30 Hz
[28]	2CCII, 1Multiplier	2R, 1C	>60	Both	Grounded	-	356 mW	160 KHz
[29]	1CCII, 1Multiplier	1R, 1C	>40	Both	Grounded	-	204 mW	860 KHz
[30]	1MO-OTA, 1Multiplier	1R, 1C	>40	Both	Grounded	-	-	5 KHz
[25]	1CBTA, 1Multiplier	2R, 1C	23	Sim.	Grounded	0.18 μm TSMC CMOS	-	10 KHz
[88]	3CFOAs	4R, 2C, 1D	-	Exp.	Floating	-	-	700 Hz
[26]	1 DVC-CTA, 1OTA	3R, 1C	29	Both	Grounded	0.18 μm TSMC CMOS	4.88 mW	1 MHz
[31]	CCTA, CCII	3R, 1C	>35	Both	Floating	-	-	5 MHz
[90]	1VDTA, 1Multiplier	2R, 1C	>32	Both	Floating	0.18 μm CMOS	-	2 MHz
[91]	1OTA, 1CDTA	1C	-	Sim.	Both	-	-	2 MHz
[106]	4Multipliers, 1OPAMP	5R, 3C	-	Both	Floating	-	-	8 KHz
[32]	4MOSFETs	-	4	Both	Grounded	0.18 μm TSMC CMOS	128.71 μW	100 MHz
Proposed	**4MOSFETs**	**1C**	4	**Both**	**Floating**	**0.18 μm TSMC CMOS**	8.24 μW	**3 MHz**

As we know, operating frequency of an emulator depends on the circuit topology and on the type of emulator, i.e., grounded type emulator [20,24–26,28–30,32,88] or floating type emulator [21–23,25,27, 31,88–91,106]. Designing a floating memristor is more complex than designing a grounded memristor circuit. However, grounded memristors have limited applications [10]. The proposed emulator is a floating two terminal device similar to a resistor, capacitor, and inductor. It can be easily incorporated into any circuit. Any terminal of the proposed emulator can be connected to the ground or any other device or circuit elements while designing an application. The proposed emulator occupies 157.48 μm^2 area as compared to 366 μm^2 utilized by grounded emulator [32] and other emulators available in the literature [20–31,88–91].

The memristor emulator proposed in [32] consists of a CMOS inverter, which exhibits high dynamic power dissipation, leakage current [104,107], etc. In contrast, our proposed emulator consists of only four NMOS transistors and an optional external capacitor. The maximum power consumption of the emulator presented in [32] is 128.71 μW, whereas the maximum power consumption of our memristor emulator is 8.24 μW. Thus, it can be stated that our proposed emulator is 36.02× better as compared to [32], considering area utilization and power consumption. Our proposed memristor emulator has an optional external capacitor, which is used to tune the frequency as per the requirement of the applications by changing its value. It works efficiently for a range of frequencies, i.e., a few Hz to MHz, which is thoroughly verified theoretically and experimentally. Although our proposed memristor may work with or without a capacitor up to 02 MHz comfortably, we choose to employ an external capacitor in the design to enhance its utilization in practical applications.

It can be observed that the operating frequency of the memristor emulator proposed in [32] is 100 MHz, which is higher compared to our emulator. As stated above, the operating frequency of an emulator depends on the circuit topology and its type. Note that the time constant of the emulator presented in [32] is $B\frac{C_2}{C_1}$ times lower than that of the time constant of our proposed emulator. Here, B is a constant, and C_1 and C_2 are the total capacitance of the proposed emulator and the emulator presented in [32]. It is to mention that due to different topologies, each emulator has different parasitic capacitances, which impact the time constants of the emulators. Since the time constant is inversely proportional to the operating frequency, because of the difference in the time constants, the maximum operating frequency of the proposed emulator is lower than the maximum operating frequency of the emulator described in [32]. Although the post-layout $I-V$ characteristics of the memristor presented

in [32] range up to 100 MHz, but it generates acceptable $I-V$ characteristics only up to 4 Hz, when it is physically validated using discrete transistor arrays (ALD1116 and ALD1117) and a single grounded capacitor of 100 nF. Further, ZnO based memristor fabricated using direct-current reactive magnetron sputter as described in [32] also exhibits acceptable $I-V$ characteristics only up to 10 Hz. It can also be observed in [32] that with varying frequencies, the PHL of the emulator also shifts its origin, which is not recommended for the reliable behaviour of a memristor. Moreover, the physical validation of our proposed memristor emulator depicts acceptable $I-V$ characteristics up to 500 kHz using ALD1106 n-channel MOSFETs and a 4.7 nF external capacitor exhibiting better reliability and performance.

Additionally, the maximum operating frequency of the memristor emulator presented in [102] is working up to 1 MHz, which is 3× less than the proposed emulator. The emulator presented in [102] requires an external DC supply and a capacitor additionally. However, the proposed emulator does not require a DC supply, making it a simple circuit element. The maximum area utilization of the emulator presented in [102] is 2803.25 μm^2, which is 17.8× higher than the proposed emulator. Srivastava et al. [108] presented a MOS-only memristor. The PHLs of this floating emulator are not pinched precisely at the origin, especially at high frequencies, and there is no variation in the positive lobe area of the PHL at 500 kHz and 1 MHz, which violates the frequency-dependent behaviour of a memristor. The post-layout analysis is not performed, which is required for the on-chip performance validation, and also, no application involving the memristor presented in [108] is reported. Due to this, area utilization and power consumption of the memristor proposed in [108] could not be estimated.

Further, the experimental result is validated only up to 24 kHz, whereas the proposed emulator is validated for a diverse range of frequencies numerically and experimentally, and the maximum frequency of the experimental result is up to 500 kHz. The emulator reported in [108] relies on the parasitic capacitances of MOSFETs to provide memristive nonlinear behaviour and nonvolatile property. As we know, parasitic capacitance gets affected by the applied voltage [109], thus, it becomes difficult to model the behaviour of the emulator reported in [108] accurately. The grounded memristor showcased in [110] requires seven MOSFETs, an external capacitor, and a dual power supply, which exhibits high design complexity and occupies 2.89× more area than the proposed emulator. The presence of DC bias also introduces static power consumption, which is zero in our circuit because of the absence of DC bias. Further, the experimental results are not pinched at the origin, which

violates the important fingerprint of a memristor, and the applications involving this emulator are not presented. Therefore, based on the experiments, the proposed emulator can be considered an optimal emulator with respect to area, power, and operating frequency.

3.4 Applications of the proposed memristor emulator

Memristor has several advantages as it requires less area (sub-nanometer range), less static power dissipation, and nonvolatile memory behaviour. To exploit the properties of the memristor, analog and digital applications are designed below using our proposed emulator for validating its adaptiveness as a circuit element.

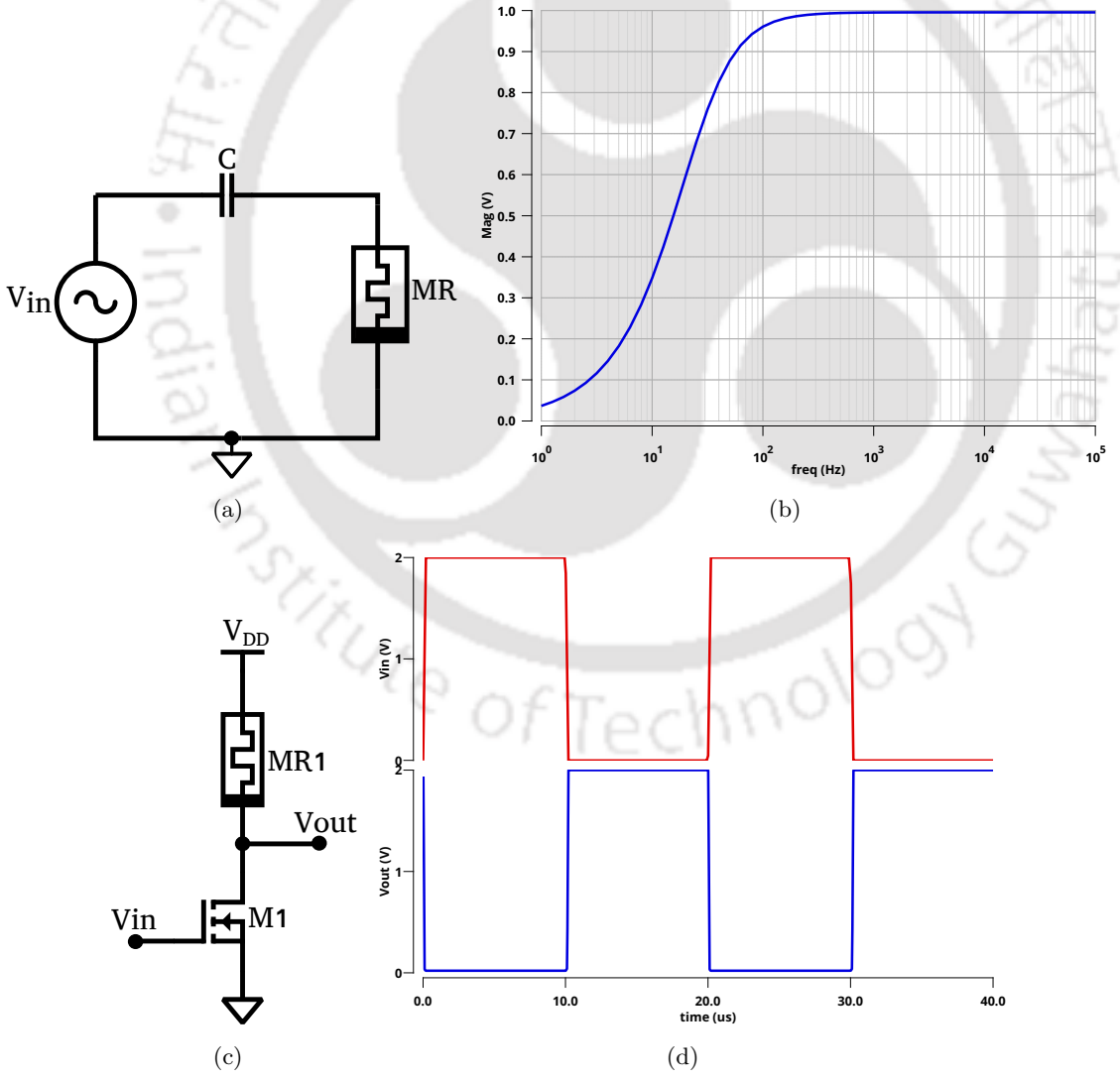


Figure 3.12: Memristor based (a) HPF (b) frequency response (c) inverter and (d) input and output waveforms

3.4.1 High pass filter

A memristor-based high pass filter is designed by employing the proposed emulator. The schematic representation of memristor-based HPF is depicted in the Fig. 3.12(a). By applying an AC magnitude of 1 V with a capacitor C of 10 pF to HPF, as shown in Fig. 3.12(a), and the corresponding frequency response of the filter is depicted in Fig. 3.12(b). The memristance of a memristor for the sinusoidal signal of $V_m Sin(2\pi ft)$ can be expressed by the following equation.

$$M_R = R_{avg} \pm R_{mem} Sin(\omega t + \phi) \tag{3.23}$$

where R_{avg} and $R_{mem}Sin(\omega t + \phi)$ are linear time-invariant and time-variant resistances, respectively. The value of R_{avg} and $R_{mem}Sin(\omega t + \phi)$ can be derived from Eq. 3.19. The memristance value depends on the amplitude, frequency, and excitation time of the applied input signal. The cut-off frequency of the high pass filter can be obtained by using the following equation.

$$f = \frac{1}{2\pi C M_R} \tag{3.24}$$

Therefore, the result of HPF exhibits the expected behaviour using the proposed emulator, which validates its applicability in analog circuit design.

3.4.2 Logic inverter design

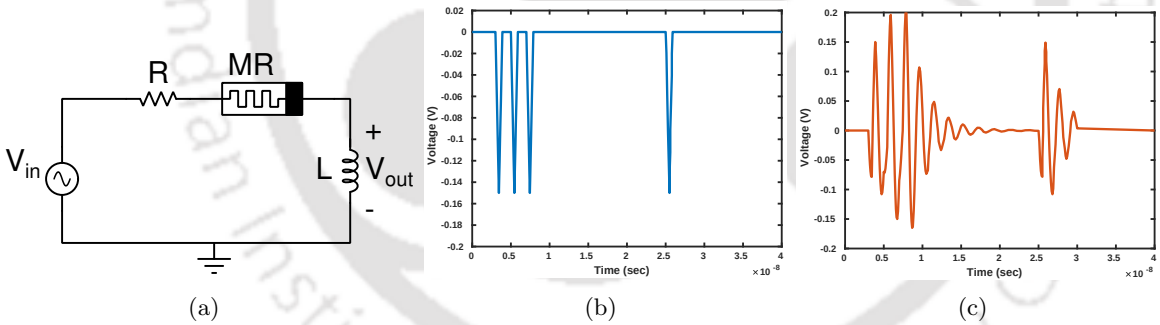
An inverter designed using a memristor is shown in Fig. 3.12(c). A NMOS transistor of aspect ratio $W/L = 30\mu/0.180\mu$ is employed in designing this inverter. A square wave of 2 V amplitude and 20μs period is applied to this circuit. The output of the inverter is illustrated in Fig. 3.12(d), which is the inverse of the input applied. Note that this aspect ratio, the voltage amplitude, and the time period are arbitrarily chosen to obtain the desired output and can be varied as per the design constraints. For example, the aspect ratios 8 μ/0.180 μ and 2 μ/0.180 μ, when square waveforms of 1.2 V and 900 mV having 20 ns and 80 ns time period are applied, it is verified that the proposed emulator based inverter produces the desired output.

The proposed emulator offers easier integration with other devices and its flexibility in analog and digital applications is thoroughly verified by designing applications in the domains mentioned above. Therefore, based on the detailed description provided, our proposed four transistor floating emulator

may be considered an optimal floating type memristor emulator among other memristor emulators.

3.4.3 Adaptive learning circuit

A memristor can be employed in the realization of neuromorphic circuits [111]. Synapses are the key elements for computation and information storage in natural and artificial neural networks. An artificial synapse must remember its past behaviour, and store a continuous set of states according to the pre-synaptic and post-synaptic neuronal activity [112]. The nonlinear dynamical behaviour of the memristor exhibits the feasibility of imitating the synaptic operation for neural cells, which is demonstrated in [113]. An Adaptive Neuromorphic Architecture (ANA) that self-adjusts its inherent parameters naturally following the stimuli frequency is presented in [114]. This circuit is based on the behaviour of the biological organism amoeba to its external stimulus. This unicellular organism illustrates puzzle and maze-solving abilities, recalling the past and learning and predicting future occurrences based on its past behaviour [115]. An amoeba slows down its locomotive speed in response to changes in temperature and other environmental conditions.



(a) (b) (c)

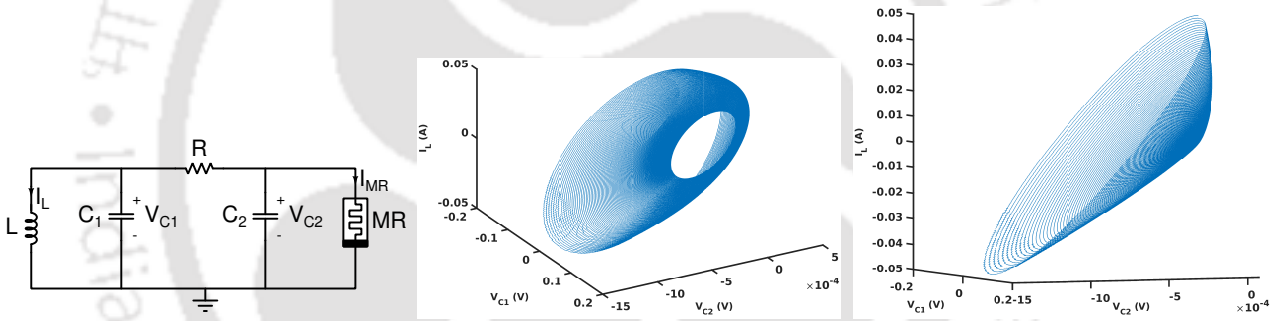
Figure 3.13: Adaptive learning (a) schematic (b) input voltage spikes and (c) response of the adaptive circuit

The circuit that realizes the behaviour of an amoeba is shown in Fig. 3.13(a), which consists of a resistor ($R = 900\ \Omega$), an inductor ($L = 1\ \mu H$), and the proposed memristor ($C = 0.1\ pF$). These three circuit elements are arranged in series to produce a resonance whenever the applied input varies. The applied voltage (V_{in}) signifies a change in the temperature, and the output voltage (V_{out}) across the inductor is analogous to the locomotive speed of an amoeba. The correctness of the circuit is verified by applying three negative spikes along with a fourth spike after some delay, as shown in Fig. 3.13(b). The first three spikes are employed to train the circuit, causing oscillations due to the resonant behaviour of the circuit, as illustrated in Fig. 3.13(c). At a fourth input spike, the circuit resonates with the same frequency as earlier, anticipating the next spike, as showcased in Fig. 3.13(c).

The amplitude of the output voltage diminishes in the absence of input spikes, generating damped oscillations [114]. This validates the behaviour of an amoeba by using a circuit employing the proposed emulator.

3.4.4 Chaotic circuit

The proposed memristor-based chaotic oscillator is designed to validate its effectiveness as a non-linear circuit element. A circuit for generating chaos was introduced by Leon O. Chua [116] using a well-known Chua circuit. Chua's circuit [117] is realized using one memristor (MR), three energy-storage elements, and a linear resistor. The nonlinear property of the proposed memristor (MR) is used to model a chaotic oscillator along with an inductor (L), two capacitors (C_1 and C_2), and a resistor R, as shown in Fig. 3.14(a).



(a) (b) (c)

Figure 3.14: Chaotic oscillator (a) Schematic (b) $C_1 = 10\ nF$, $V_{C1}(0) = 50\ mV$, $C_2 = 5\ nF$, $R = 1.5\ K\Omega$, $L = 0.1\ \mu H$ and (c) $C_1 = 10\ nF$, $V_{C1}(0) = 50\ mV$, $C_2 = 15\ nF$, $R = 500\ \Omega$, $L = 0.1\ \mu H$ attractors with circuit parameters

The chaotic oscillator is modeled by the following mathematical expressions.

$$\frac{d\varphi(t)}{dt} = V_{C1} \tag{3.25}$$

where $\varphi(t)$ is the flux associated with the inductor, L.

$$\frac{dV_{C1}}{dt} = \frac{1}{C_1}\left[\frac{V_{C2} - V_{C1}}{R_1} - I_L\right] \tag{3.26}$$

$$\frac{dV_{C2}}{dt} = \frac{1}{C_2}\left[\frac{V_{C1} - V_{C2}}{R_1} - I_{MR}\right] \tag{3.27}$$

where I_{MR} is the current flowing through MR. The following mathematical model gives the current

passing through the inductor.

$$\frac{dI_L}{dt} = \frac{V_{C1}}{L} \tag{3.28}$$

The behaviour of the chaotic oscillator is obtained by using two different combinations of the circuit parameters, as shown in Figs. 3.14(b) and 3.14(c). Due to the proposed memristor, irregular and unpredictable patterns [118] are generated by changing circuit parameters only. Any change in the circuit parameters causes variations in the characteristic of the chaotic oscillator, validating the generation of random and indeterministic attractors. Chaotic oscillators can be leveraged in applications ranging from cryptography, encryption, secure communications, random signal generators, through-wall radar, and robotics. Therefore, the proposed memristor aids in designing a chaotic circuit, reducing circuit complexity and area compared to other state-of-the-art chaotic oscillators [119]. Thus, the proposed emulator is highly flexible, versatile, and suitable for both general purpose and specific applications.

3.5 Conclusion

A new circuit topology for the floating memristor emulator is presented, which consists of four MOSFETs and an external capacitor to realize the expected behaviour of a memristor. Its numerical analysis is performed using a Cadence design environment with TSMC 180 nm PDKs. Its characteristics are validated at different operating frequencies, temperatures, and process corners using pre- and post-layout simulations. Our emulator exhibits acceptable characteristics while varying various parameters at different process corners. It is found that the proposed emulator functions reliably from a few Hz to 3 MHz producing acceptable $I-V$ characteristics. Its area utilization and power consumption are 157.48 μm^2 and 8.24 μW, respectively, at the maximum operating frequency of 3 MHz. The functional validation of the proposed emulator is performed experimentally using ALD1106 n-channel MOSFETs in the laboratory, which certifies its coherence with the numerical analysis. The acceptability and applicability of the proposed memristor emulator are showcased using various analog and digital applications. The main advantages of this emulator are its (1) suitability for monolithic IC fabrication, (2) stable and reliable behaviour, (3) high frequency operation, (4) low power consumption, and (5) less area utilization, which makes it a perfect candidate to be employed in the wide range of area and power optimal applications operating at high frequencies.

4

Inverse Memristor Emulator

Contents

Objective:

The realization of a memristor with inverse frequency behaviour using fewer off-the-shelf components for high-frequency applications exhibits the following advantages.

(i) Utilizes less area and lower power consumption.

(ii) Capable of operating at high frequency in the range of MHz.

(iii) Easier integration with other circuit elements for designing various applications.

4.1 Introduction

The $I-V$ characteristics of a memristor and memristive devices [120] exhibit a pinched hysteresis loop (PHL), one of the key fingerprints for any emulator circuit to behave as a memristor. Generally, the lobe area of a pinched hysteresis loop decreases with an increase in the frequency and becomes a single-valued function when the frequency reaches infinity [87]. On the contrary to this, when the lobe area of a PHL increases with an increase in the frequency, it is considered a memristor with an inverse frequency characteristic [121]. The memristor with inverse frequency characteristic was first discussed by ME Fouda et al. in 2015 [121], where some combination of circuit elements produced a pinched hysteresis loop whose lobe area increased with frequency. A memristor with inverse frequency characteristics can be described as an inverse memristor [122]. The research on memristors with inverse frequency characteristics will help us to better understand the behaviour and definition of memristors as a fundamental circuit element. Recently inverse frequency characteristics of a memristor have also been used to develop an electronic synaptic device for neuromorphic computing applications [123].

The memristor with inverse frequency behaviour (inverse memristor) is reported in [121] and employs Dual Operational Transconductance Amplifiers, an Op-Amp, and passive circuit elements to realize inverse memristor operation. Further, the operating frequency of this emulator is limited to only 700 Hz, and it has complex circuit topology making it unsuitable for monolithic IC fabrication. Hezayyin et al. [124] present inverse memristor emulators designed using second generation current conveyor (CCII) and current feedback operational amplifier (CFOA) with two bipolar junction transistors (BJTs) increasing its hardware complexity and extending maximum operating frequency up to 200 kHz. The inverse memristor emulator designed using two BJTs and two passive circuit components is demonstrated in [125]. Although it has less hardware complexity, the maximum operating

frequency of this emulator is limited to 200 Hz only. As per our knowledge, the inverse memristor emulators reported in the literature have complex circuit topologies consisting of active and passive elements with low or medium operating frequencies, limiting their applicability in the wide applications.

In the proposed work, we present a floating memristor emulator with inverse frequency behaviour composed of only four MOSFETs and a capacitor. The proposed emulator is designed using two DTMOS transistors, which aids in enhancing its operating frequency in the range of MHz with the minimum power consumption. The main advantage of the proposed inverse memristor is its less area utilization because of its simple circuit topology. This makes our proposed emulator suitable for commercial monolithic integrated circuit fabrication. The nonlinear and memory retention properties of the proposed emulator are utilized in designing a chaotic oscillator. Further, the floating behaviour of the proposed emulator is utilized in the realization of a logic NOR gate.

The rest of this chapter is organized as follows. Section 4.2 presents circuit topology, working principle and mathematical formulation of the proposed memristor emulator. Section 4.3 discusses the detailed analysis of the proposed emulator at different parameters, post-layout, and experimental validation. Section 4.4 showcases the proposed emulator based applications. Section 4.5 concludes the chapter.

4.2 Proposed emulator with inverse frequency characteristic

As we know, the pinched hysteresis loop (PHL) is considered one of the main characteristics of a memristor [126]. However, it is also observed in several other nonlinear devices, such as inductors or capacitors with quadratic current or voltage nonlinearity [121]. In some devices, it is seen that the area under the curve increases with frequency, which exhibits inverse memristive property [127]. In 2015, Mohammed E. Fouda et al. [122] proposed a mathematical model describing a circuit consisting of series or parallel-connected R, L, and C elements along with a memristor and an inverse memristor, which is represented below.

$$y = ax + (b + ex)\frac{dx}{dt} + (d + cx)\int_0^t x(\tau)d\tau \tag{4.1}$$

where x and y are normalized input and normalized output signals. Here, a, b, c, d, and e are the scaling constants.

Eq. 4.1 describes different cases of applying an input signal and/or the effect of integrating and differentiating an input signal. The equation exhibiting basic memristor characteristics is described below.

$$y(t) = x(t)\left(a + c\int_0^t x(\tau)d\tau\right) + b\frac{dx(t)}{dt} \tag{4.2}$$

In Eq. 4.2, $b = 0$ gives a symmetric case, which implies symmetric loops on both sides. The signs of coefficients in this equation determine the quadrants of the loops in which they lie. Similarly, inverse memristive characteristics can be obtained by equating $b = c = 0$, and then Eq. 4.1 can be rewritten as follows.

$$y = ax + (b + ex)\frac{dx}{dt} \tag{4.3}$$

An asymmetrical loop may be obtained by adding an integral term in Eq. 4.3 and setting $b = 0$. Inverse memristive devices consist of a differentiating term; therefore, an increase in the frequency increases the area of PHL [121]. This work proposes a novel memristor emulator using four MOSFETs and an external tunable capacitor. Its circuit realization is described below in detail.

4.2.1 Proposed circuit topology and its mathematical analysis

Fig.4.1(a) exhibits a symbolic representation of a memristor. In the proposed emulator illustrated in Fig. 4.1(b), MOSFETs $M1$ and $M2$ are employed as dynamic threshold MOS (DTMOS) transistors. MOSFETs $M3$ and $M4$ dynamically follow the voltage sampled at the input and keep it below the threshold voltage of $M1$ and $M2$. Note that $M1$ and $M2$ are used in DTMOS configuration for higher speed and lower power consumption than standard MOSFETs. Further, external tunable capacitor C is utilized in the circuit to mimic the nonvolatile property of the memristor emulator. It is also employed for a proposed emulator to function at different frequencies efficiently.

An input voltage, V_{in}, applied between two floating terminals A and B, as shown in Fig. 4.1(b), is V_{AB}, i.e. differential voltage ($\pm\frac{V_{AB}}{2}$).

The following expressions are obtained when KVL is applied across $M2$, V_X, and terminal B in

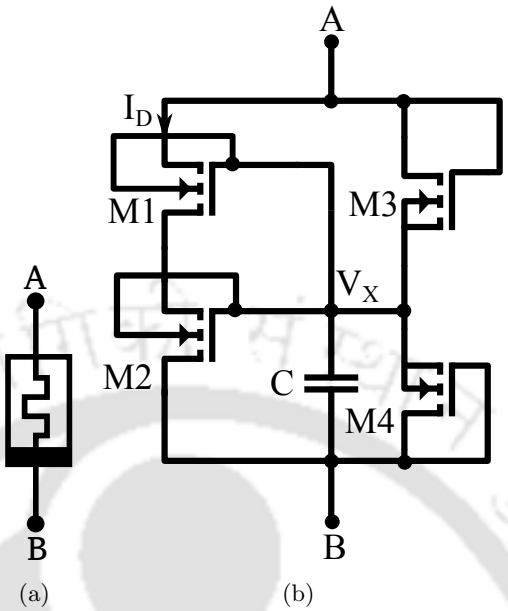


Figure 4.1: (a) Memristor symbol and (b) proposed circuit topology for memristor emulator with inverse frequency characteristic

Fig. 4.1(b).

$$-\left(\frac{-V_{AB}}{2}-V_{G2}\right)+\left(V_X-\frac{-V_{AB}}{2}\right)=0$$
$$\frac{V_{AB}}{2}+V_{G2}+V_X+\frac{V_{AB}}{2}=0 \tag{4.4}$$

Since $V_{G2}=V_X$, V_{in} can be expressed as follows.

$$V_{in}=-2V_X \tag{4.5}$$

Differentiating Eq. 4.5 leads to the following equation.

$$\frac{dV_{in}}{dt}=-2\frac{dV_X}{dt} \tag{4.6}$$

Considering the aspect ratio of $M3$ and $M4$ as $\frac{k_3}{k_4}=\frac{kM}{kN}$, and applying Kirchhoff's current law at the node X, the following mathematical expression is obtained after simplification. Note that, k_3 and k_4 are process parameters of $M3$ and $M4$, respectively. $k=\mu C_{ox}\frac{W}{L}$ is the common process parameter related with $M3$ and $M4$, and

$$V_x \approx \frac{1}{Y} + \frac{k}{YC}\varphi(t) \tag{4.7}$$

Here Y is a constant. Further, $\varphi(t)$ can be stated as,

$$\varphi(t) = \int (V_{in} + 5V_t)dt \tag{4.8}$$

Using Eq. 4.7, Eq. 4.6 can be represented as,

$$\frac{dV_{in}}{dt} = -2\frac{d}{dt}\left(\frac{1}{Y} + \frac{k}{YC}\varphi(t)\right) \tag{4.9}$$

$$\frac{dV_{in}}{dt} = -\frac{2k}{YC}\frac{d}{dt}(\varphi(t)) \tag{4.10}$$

Substituting Eq. 4.8 into Eq. 4.10 leads to the following mathematical expression.

$$\frac{dV_{in}}{dt} = -\frac{2k}{YC}V_{in} - \frac{10kV_t}{YC} \tag{4.11}$$

The threshold voltage of a DTMOS can be described by Eq. 4.12.

$$\begin{aligned} V_T &= V_{T0} + \gamma\left(\sqrt{\mid 2\psi_S + V_{SB} \mid} - \sqrt{2\psi_S}\right) \\ &\approx V_{T0} + \beta V_{SB} \end{aligned} \tag{4.12}$$

where β is the body effect constant. After substituting Eq. 4.12 into the Eq. 4.11, Eq. 4.13 is obtained.

$$\frac{dV_{in}}{dt} = -\frac{2k}{YC}\left(V_{in} + 5V_{t_0} + 5\beta V_{SB}\right) \tag{4.13}$$

Since body and gate terminals of a DTMOS transistor are connected together; therefore, $V_{SB} = V_{SG} = -V_{GS}$. Thus, Eq. 4.13 can be reformulated as mentioned below.

$$\frac{dV_{in}}{dt} = -\frac{2k}{YC}\left(V_{in} + 5V_{t0} - 5\beta V_{GS}\right) \tag{4.14}$$

As we know, $g_m = \frac{2I_D}{V_{GS}-V_T} = \sqrt{2K_n(\omega/L)}\sqrt{I_D}$, $V_{GS} = \frac{2I_D+g_mV_t}{g_m}$ and $I_D = \frac{g_m^2}{2K_n(W/L)}$. This leads

Eq. 4.14 to be described as depicted below.

$$\frac{dV_{in}}{dt} = -\frac{2k}{YC}\left(V_{in} + 5V_{t0} - \frac{10\beta I_D + 5\beta g_m V_t}{g_m}\right) \tag{4.15}$$

$$\begin{aligned}\frac{2k}{YC}g_m\frac{V_{in}}{I_D} = &-\frac{20kK_n(W/L)_{1,2}}{YCg_m}(V_{t0} + \beta V_t) \\ &-\frac{20k\beta}{BC} - \frac{2K_n(W/L)_{1,2}}{g_m}\frac{dV_{in}}{dt}\end{aligned} \tag{4.16}$$

By expanding $(V_{t_0} - \beta V_t)$ and neglecting small order terms along with constants, Eq. 4.16 can be simplified as stated below.

$$\begin{aligned}\frac{V_{in}}{I_D} = &-\frac{10K_n(W/L)_{1,2}}{g_m^2}(1-\beta)V_{t0} - \\ &\frac{K_n(W/L)_{1,2}}{kg_m}YC\frac{dV_{in}}{dt}\end{aligned} \tag{4.17}$$

Further, the memristance M of the proposed emulator can be derived using Eq. 4.17 and is described in Eq. 4.18.

$$\begin{aligned}M = \frac{V_{in}}{I_D} = &-\frac{10K_n(W/L)_{1,2}V_{t0}(1-\beta)}{g_m^2} \\ &-\frac{K_n(W/L)_{1,2}BC}{kg_m^2}\frac{dV_{in}}{dt}\end{aligned}$$

$$M = \frac{A(\beta-1)}{g_m^2} - \frac{D}{g_m^2}\frac{dV_{in}}{dt} \tag{4.18}$$

where $A = 10K_n(W/L)_{1,2}V_{t0}$ and $D = \frac{K_n(W/L)_{1,2}YC}{k}$.

4.2.2 Frequency behaviour

In order to study frequency behaviour of the proposed emulator, we assume that $v_{in}(t) = A_m sin(\omega t)$, where $\omega = 2\pi f$, and A_m are frequency and amplitude of the applied sinusoidal input, respectively. Thus, memristance of the proposed emulator can be elaborated using Eq. 4.19.

$$\begin{aligned}M = &\frac{10K_n(W/L)_{1,2}V_{t0}(\beta-1)}{g_m^2} \\ &-\frac{K_n(W/L)_{1,2}YC}{kg_m^2}A_m\cos\omega t \times \omega\end{aligned} \tag{4.19}$$

$$M = \underbrace{\frac{10K_n(W/L)_{1,2}V_{t0}(\beta-1)}{g_m^2}}_{\text{linear time-invariant}} + \underbrace{\frac{K_n(W/L)_{1,2}YC}{kg_m^2}A_m\cos(\pi-\omega t)\times\omega}_{\text{linear time-variant}} \tag{4.20}$$

It can be derived from Eq. 4.20 that the ON state memductance approaches to zero when the frequency tends to zero. The amplitude of ON state memductance can be described as mentioned below.

$$\mathscr{A} = \frac{\pi YCA_m f}{5kV_{t0}(\beta-1)} = \tau f = \frac{\tau}{T} \tag{4.21}$$

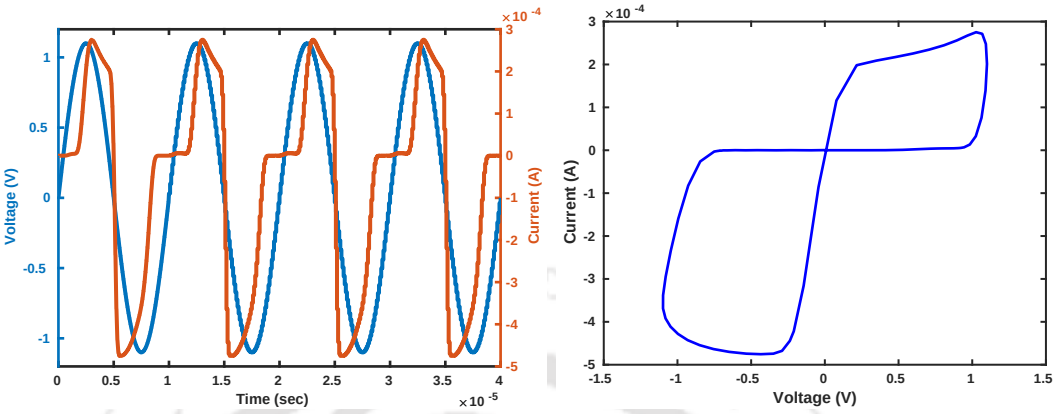
where $\tau = \frac{\pi YCA_m}{5kV_{t0}(\beta-1)}$ represents time constant of the proposed emulator, which controls PHL. Here, $T = \frac{1}{f}$ is the period of excitation. Note that τ changes as per the requirement of operating frequency. Generally, only C can be changed effectively, whereas other parameters are taken as constant; therefore, capacitor acts as a tuning parameter for varying the time constant. The frequency behaviour of our proposed emulator analyzed using Eq. 4.21 is mentioned below.

- $\mathscr{A} \to 0$ for $f \to 0$ or $A_m \to 0$, then resistance dominates time-invariant part.
- $\mathscr{A} \to 1$ for $f \to 1/\tau$, which leads the maximum lobe area of a PHL to be achieved.
- $\mathscr{A} \geq 1$ for $f > 1/\tau$, which tends to be a lossy curve.

The proposed emulator is validated by performing numerical analysis and conducting physical experiments, which are presented in the following section in detail.

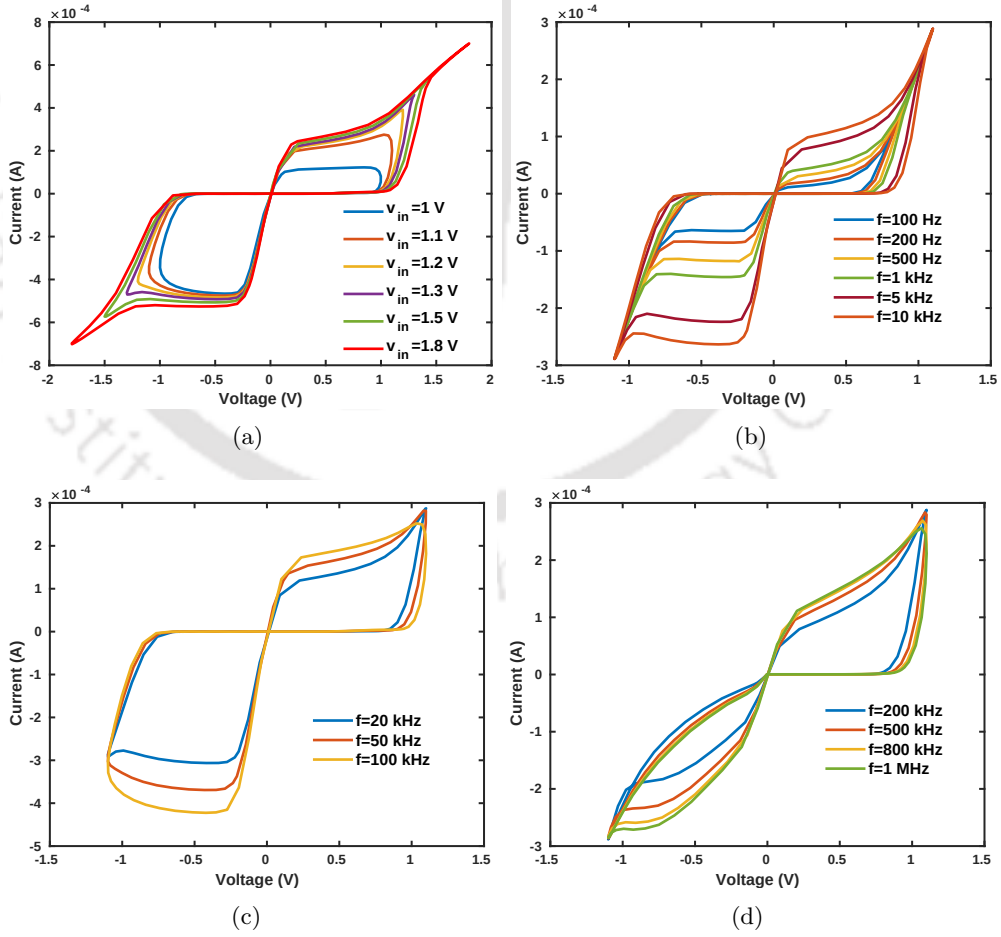
4.3 Performance analysis of the proposed emulator

The proposed emulator described in section 4.2 is validated by performing parametric analysis using Cadence Virtuoso and TSMC 180nm CMOS technology at various process corners. Further, the post-layout analysis is also conducted to validate the correctness of the proposed emulator. Later, physical experiments are conducted to establish the realistic behaviour of the emulator. A detailed description of these analyses is discussed below.



(a) (b)

Figure 4.2: (a) Transient response (b) $I-V$ characteristics (PHL) of the proposed emulator



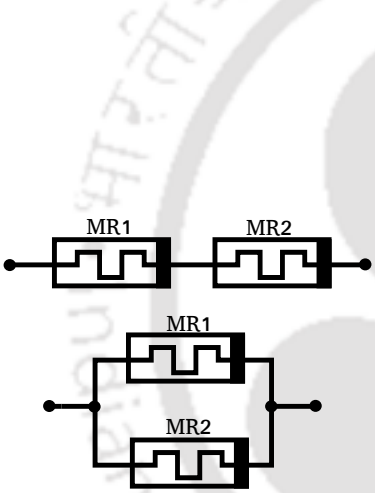
(a) (b)

(c) (d)

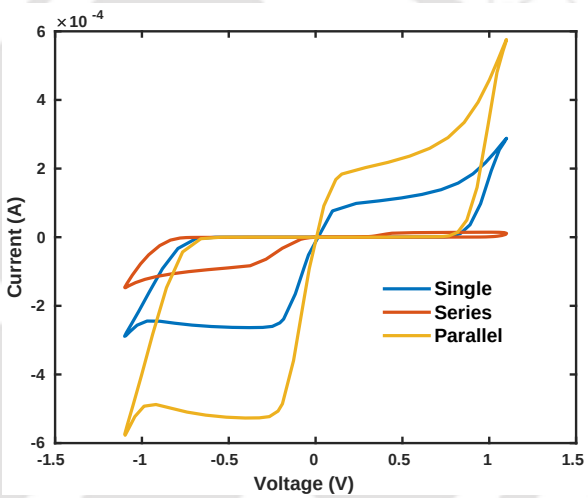
Figure 4.3: (a) PHLs at different operating voltages and PHLs at different frequencies using (b) 10 nF, (c) 10 pF, and (d) 100 fF of the proposed emulator

4.3.1 Numerical analyses

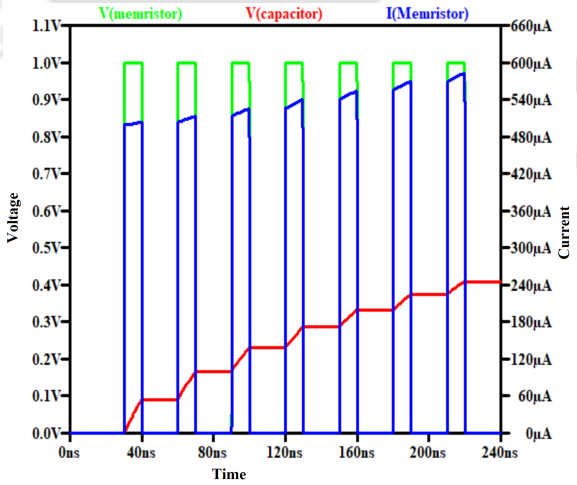
The desired characteristics of the proposed emulator shown in Fig.4.1(b) are obtained by selecting the aspect ratio of four NMOS transistors as $(W/L)_1 = (W/L)_2 = 50\mu/1\mu$ and $(W/L)_3 = (W/L)_4 = 1\mu/1\mu$, respectively. The transient characteristics of the emulator are shown in Fig. 4.2(a) when an input excitation having 100 kHz frequency and 1.1 V amplitude is applied. The PHL of the proposed inverse memristor emulator is illustrated in Fig. 4.2(b). It can be seen that the lobe area of PHL increases with the varying amplitude of the applied input due to an increase in the current flowing through the emulator, as illustrated in Fig. 4.3(a).



(a)



(b)



(c)

Figure 4.4: (a) Circuit diagram (b) PHLs of memristors connected in series and parallel combinations, and (c) Transient response of the emulator using 1 pF capacitor employing an input pulse having 10 ns ON state and 40 ns time period of 1 V amplitude

Our proposed emulator consists of an external capacitor, which is used to obtain PHL at different operating frequencies. Due to this, our proposed emulator generates PHL in the range of several hertz to MHz by varying the capacitor. Figs. 4.3(b), 4.3(c) and 4.3(d) exhibit an increase in the lobe area of PHLs, when operating frequency of the proposed emulator is varied. The results obtained in the numerical analysis verify the functionality and inverse frequency behaviour of the proposed emulator.

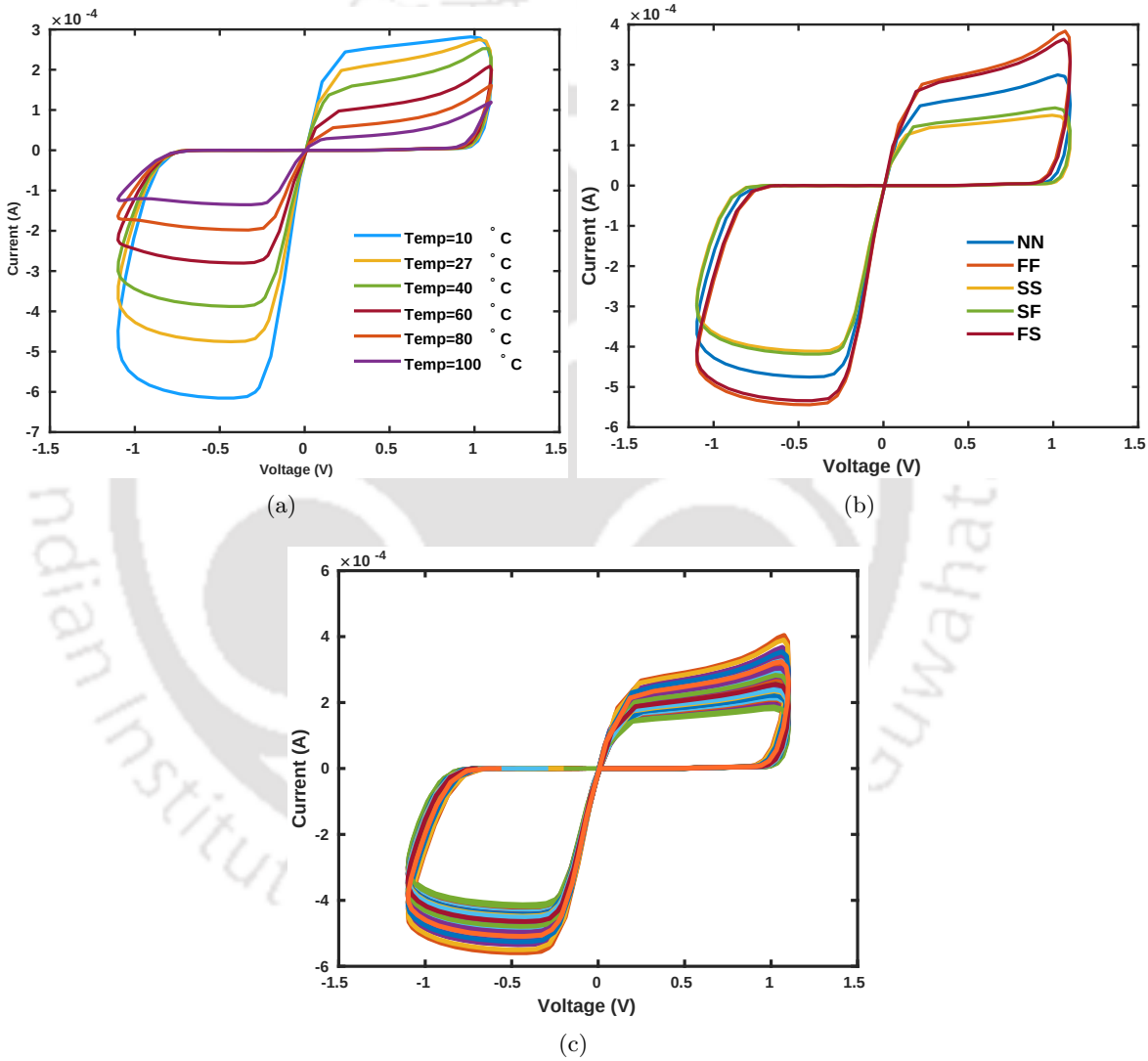


Figure 4.5: PHLs of the proposed memristor emulator at (a) Different temperatures (b) Different process corners and (c) Monte Carlo analysis

The proposed emulator is analyzed when two identical memristors, $MR1$ and $MR2$, are connected in series and parallel configurations, as shown in Fig. 4.4(a). In the series configuration, the memristance increases due to the decrease in the current flowing through the emulator, reducing the lobe area of the PHL compared to the lobe area of a single memristor PHL, shown in Fig. 4.4(b). Further,

the effective memristance is significantly reduced, and the lobe area of the PHL increases more than double the lobe are of a single memristor PHL when $MR1$ and $MR2$ are connected in parallel. Hence, the current flowing through $MR1$ and $MR2$ increases more than twice the current flowing in a single memristor. This further validates the correctness of the proposed emulator.

As we know, nonvolatility is one of the important properties of a memristor, which is realized by employing a capacitor C in our proposed emulator. When a voltage pulse train with a 40 ns time period having 10 ns ON pulse width is applied to the emulator, voltage across the capacitor increases during the ON period and remains constant during the OFF period, as shown Fig. 4.4(c). This enables emulator to retain the previous information during the absence of external voltage to exhibit the nonvolatile behaviour.

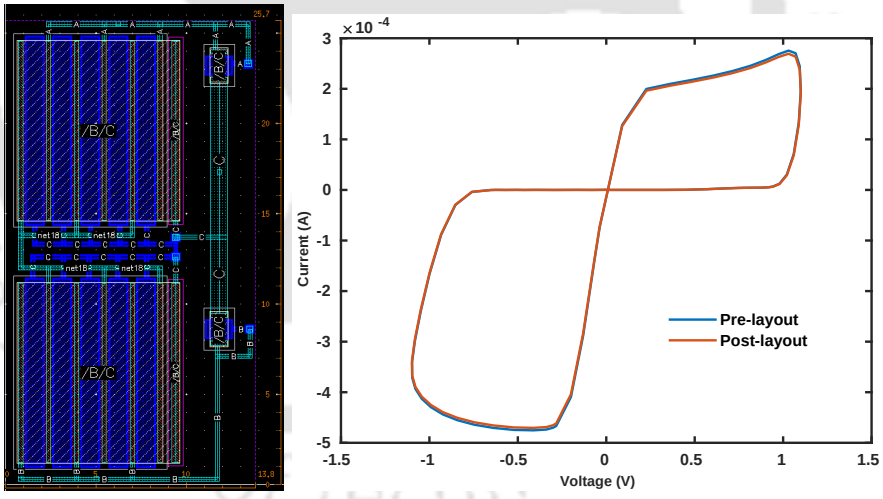
It can be observed in Fig. 4.5 that the proposed design produces acceptable PHLs at different temperatures and process corners. The memristor has a high current at a low temperature exhibiting low memristance, increasing lobe area of the PHL. Fig. 4.5(a) illustrates that the PHL of a memristor varies with the temperature. Further, it can be seen that the lobe area of the PHL of a memristor is more at a low temperature ($10°C$), and it gradually reduces with an increase in the temperature ($100°C$).

The reliability of the proposed emulator is further validated at different process corners. The PHL of the memristor varies slightly at the process corners, Nominal (NN), Fast (FF), Fast Slow (FS) and Slow Fast (SF). It can be observed that the PHL of the memristor has a large lobe area at FF and a small lobe area at SS, as shown in Fig. 4.5(b). The PHL changes at different process corners; however, it is pinched precisely at the origin, where the current and the voltage are zero. Therefore, our proposed emulator provides expected characteristic irrespective of the variations in the process parameters, showcasing its reliability.

Further, Monte Carlo analysis is performed for 250 runs to establish the robustness of the proposed emulator. Deviations in the device parameters, such as aspect ratio, threshold voltage and capacitance, are chosen as a uniform distribution. As depicted in Fig. 4.5(c), the PHL is generated as expected, but there are slight deviations in the PHL due to the variations in the capacitances and other device parameters. However, $I - V$ characteristic of the memristor remains pinched at the origin, and its memristive behaviour is conserved. This validates the robustness of the proposed emulator with respect to the variations of devices parameters.

4.3.2 Post-layout Analysis

The physical layout of the proposed emulator is designed using Cadence Virtuoso employing TSMC 180 *nm* PDKs, as shown in Fig. 4.6(a). This layout is validated by performing *Design Rule Check (DRC)*, *Layout v/s Schematic (LVS)*, and *RC extraction*. The correctness of the proposed emulator is validated by pre-layout and post-layout analyses. It utilizes 354.66 μm^2 area and consumes 291.78 μW power. Pre- and post-layout analyses of the proposed emulator are performed by employing sinusoidal signal of 1.1 V and 100 kHz, showcased in Fig. 4.6(b). It can be seen that PHL of the proposed emulator obtained during post-layout analysis is reduced compared to pre-layout analysis due to the presence of parasitic elements. It can be observed that both $I-V$ characteristics obtained during these analyses are in accordance with each other. This confides that the proposed emulator can be realized on silicon or using discrete components. Therefore, it is chosen to be validated experimentally in a laboratory using discrete components because of their easy availability. The details of the experimental setup are provided in the subsequent section.



(a) (b)

Figure 4.6: (a) Layout design and (b) PHL of pre- and post-layout analyses of the proposed emulator

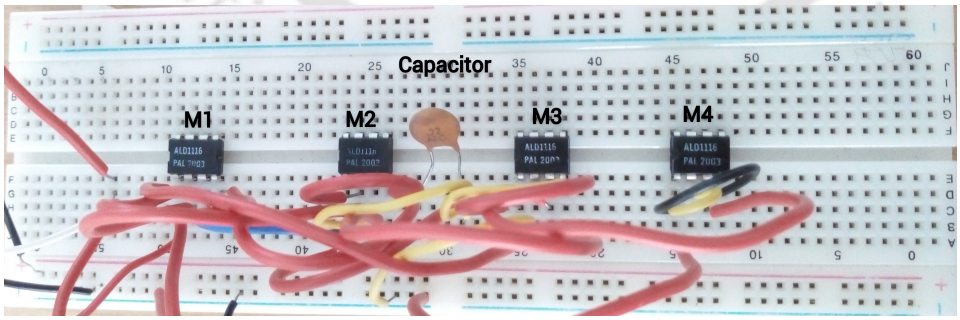
4.3.3 Experimental validation

The physical experiment of the proposed memristor emulator, as shown in Fig.4.1(b), is conducted by selecting suitable n-channel MOSFETs and capacitors to obtain desired characteristics of a memristor. In this experiment, four ALD1106 n-channel MOSFETs [105] are utilized and various capacitors are utilized to so the proposed emulator at different operating frequencies. An experimental setup

and a prototype of this emulator are shown in Fig. 4.7(a) and Fig. 4.7(b). A Rigol DG1022 function generator is used to provide a 3 V sinusoidal input to the proposed emulator and a MDO3012 mixed domain oscilloscope is employed to observe its response.

An input excitation of 3 kHz is applied to the proposed emulator configured on a breadboard employing 0.22 μF capacitor. Its transient response and corresponding $I - V$ characteristics are shown in Fig. 4.8(a) and Fig. 4.8(b). It can be seen in Fig. 4.9 that an increment in the lobe area of the PHL with an increase in the frequency validates the inverse frequency behaviour of the proposed emulator. Note that the capacitance is reduced to obtain desired characteristics at a high frequency. It can be seen that the experimental and numerical analyses are in congruence, validating the correctness of the proposed emulator using four NMOS transistors and an external capacitor.

(a)



(b)

Figure 4.7: (a) Experimental setup and (b) Prototype on the breadboard of the proposed emulator

The proposed emulator is compared with state-of-the-art work available in literature. The emulator presented in [121] requires analog ICs and passive components, exhibiting high hardware implementation complexity. Note that its operating frequency is limited to 900 Hz only. In [125], a simple inverse

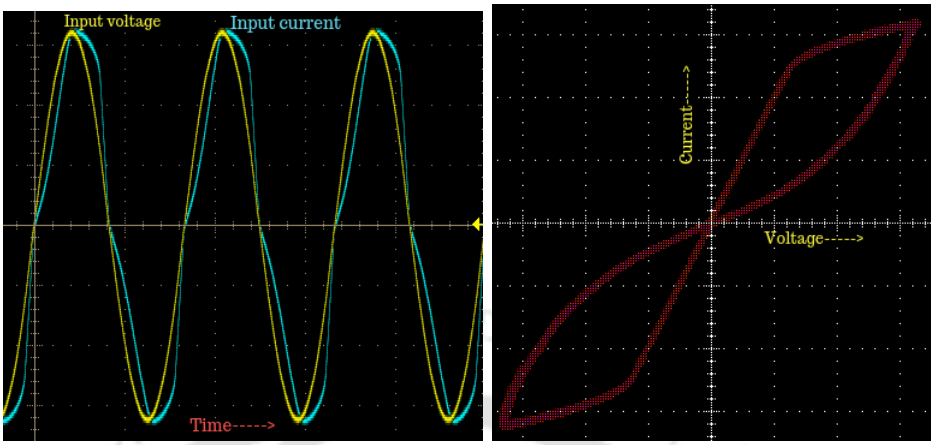


Figure 4.8: Experimental validation of the proposed emulator (a) Transient analysis and (b) PHL at 3 kHz using 0.22 μF capacitor

frequency characteristic of a memristor emulator is configured using two BJTs and two passive components operating at 200 Hz. Another emulator depicted in [124] operates at 200 kHz, and consists of many analog ICs and passive components. Note that the emulators reported in the literature showcase high hardware complexity, high power consumption, and limited operating frequency. This work presents an area and power-efficient memristive emulator with inverse frequency behaviour operating up to 1 MHz for the first time. Compared to existing emulators, it provides stable characteristics without any distortion up to the frequency mentioned above. Its comparison with other contemporary emulators is depicted in Table 4.1, corroborating our claim.

Table 4.1: Comparison of inverse memristor emulators

Ref.	Active comp.	Passive comp.	Sim./ Exp.	Max. operating freq.
[121]	1 LM13700, 1 TL084	8 R,2 C	Both	900 Hz
[125]	2 BJTs	1 R, 1 C	Both	200 Hz
[124]	2 OPAMP 2 CFOAs 2 BJTs	2 R, 1 C	Sim.	200 kHz
Proposed	**4 MOSFETs**	**1 C**	**Both**	**1 MHz**

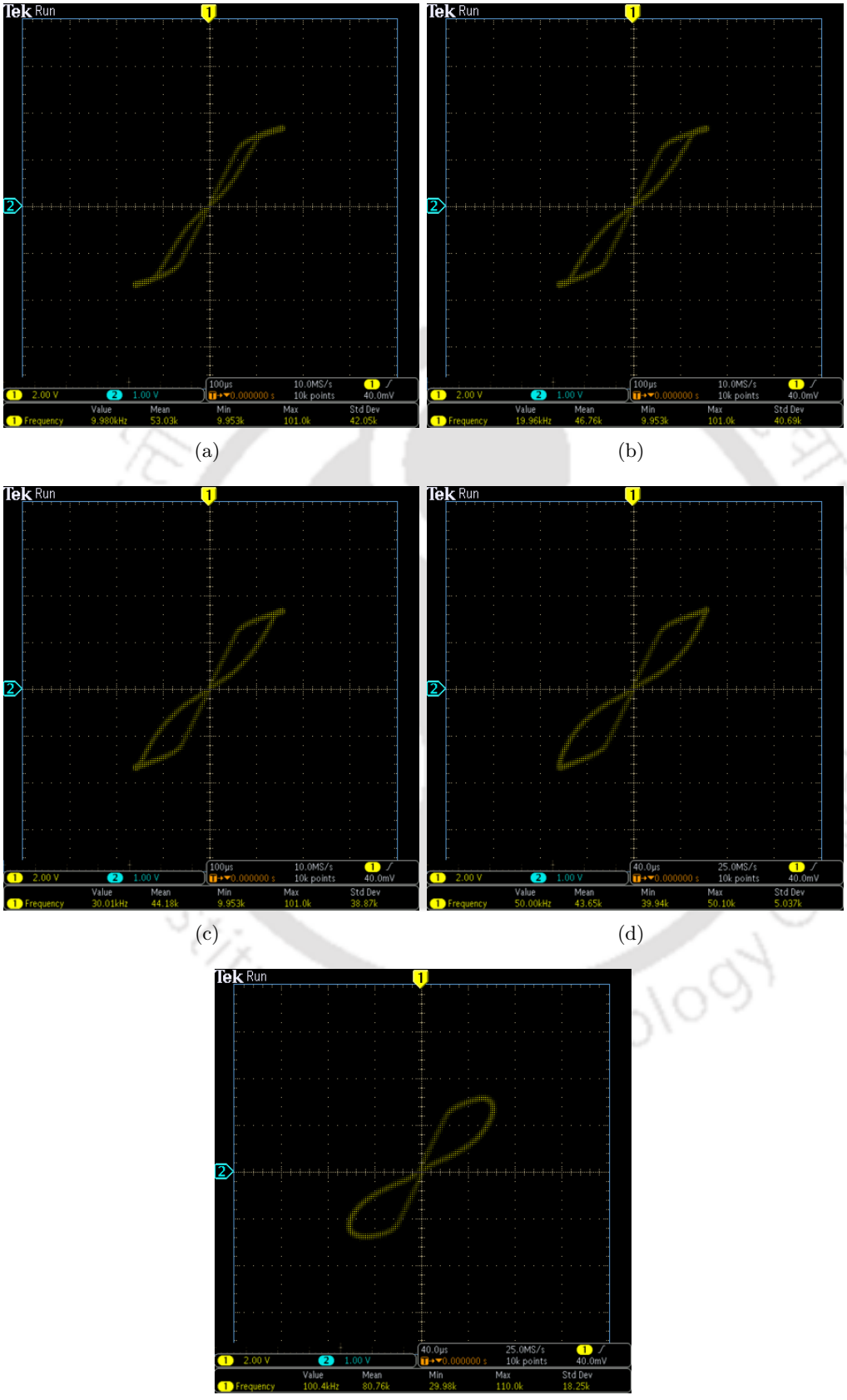


Figure 4.9: Experimental analysis at (a) 10 kHz (b) 20 kHz and (c) 30 kHz (d) 50 kHz and (e) 100 kHz using 0.1 μF capacitor.

4.4 Applications of the proposed emulator

This section elaborates on various applications incorporating the proposed emulator to establish its efficacy. The Cadence Virtuoso ADE and TSMC 180 nm PDKs are employed to design these applications.

4.4.1 Memristor based NOR logic gate

As we know, a conventional NOR gate requires four MOSFETs, whereas the NOR gate illustrated in Fig. 4.10(a) utilizes only two MOSFETs ($M1$ and $M2$) and two memristors ($MR1$ and $MR2$). The output, $Vout$, attained by applying a pulse voltage to inputs $Vin1$ and $Vin2$, is shown in Fig. 4.10(b). It can be observed that for valid inputs, a valid output is generated, exhibiting the applicability of memristors in designing digital circuits efficiently.

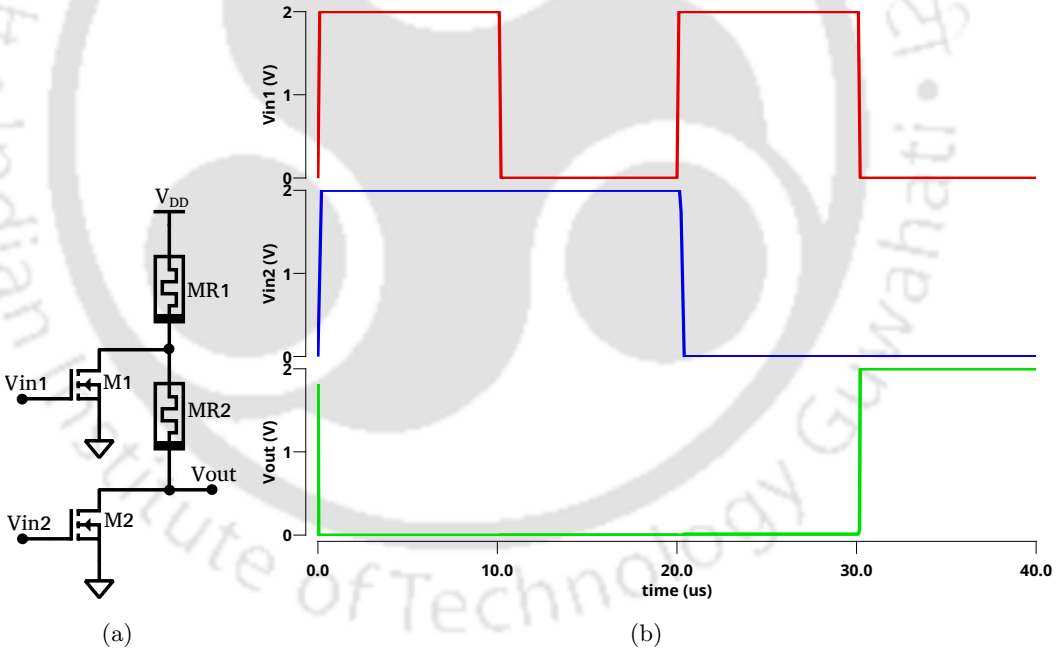


Figure 4.10: (a) Circuit diagram and (b) Input and output characteristics of memristor based NOR logic

4.4.2 Chaotic oscillator

A chaotic oscillator is designed using the proposed emulator for validating its viability as a nonlinear circuit element. Leon O. Chua developed a circuit to create chaos using a well-known Chua circuit [116]. Chua's circuit [117] is modelled using one memristor (MR), three energy-storage elements, and a linear resistor. The proposed emulator-based chaotic oscillator consists of an inductor (L), two capacitors

(C_1 and C_2), and a resistor R, as depicted in Fig. 4.11(a).

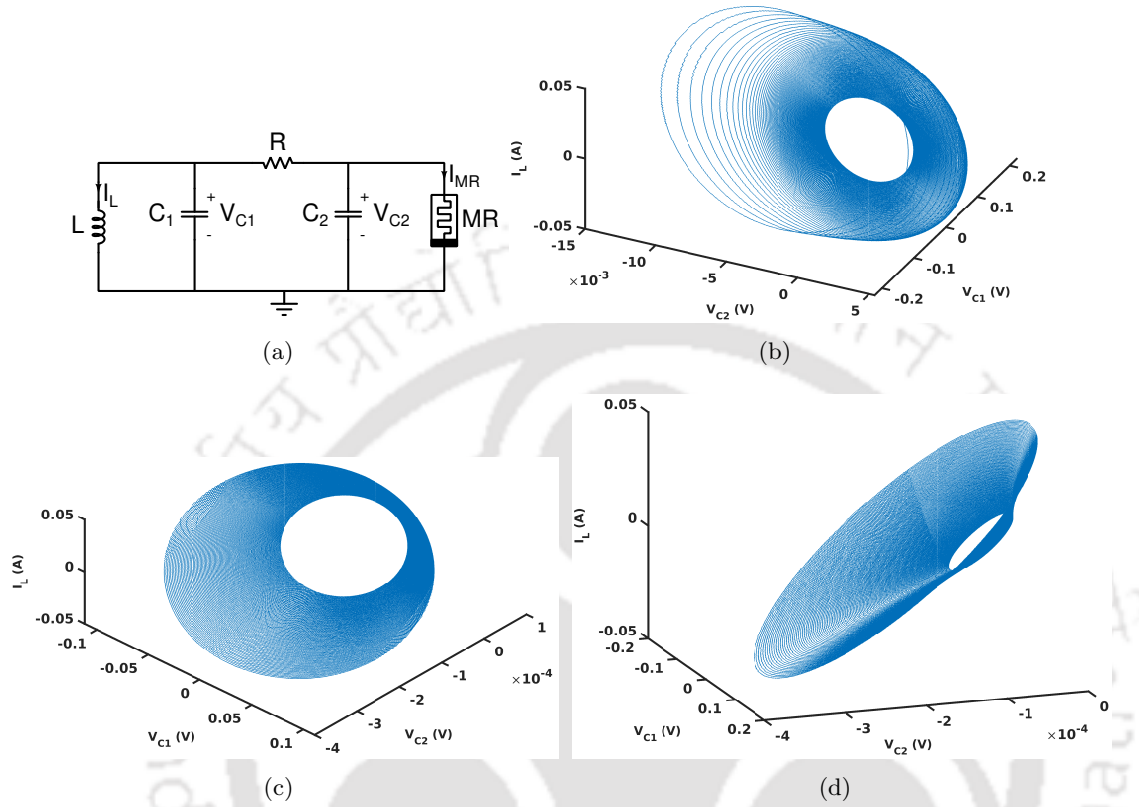


Figure 4.11: Chaotic oscillator (a) Schematic (b) $C_1 = 10\ nF$, $V_{C1}(0) = 50\ mV$, $C_2 = 1\ nF$, $R = 1.5\ K\Omega$, $L = 0.2\ \mu H$, (c) $C_1 = 20\ nF$, $V_{C1}(0) = 50\ mV$, $C_2 = 30\ nF$, $R = 1\ k\Omega$, $L = 0.1\ \mu H$, and (d) (c) $C_1 = 10\ nF$, $V_{C1}(0) = 50\ mV$, $C_2 = 30\ nF$, $R = 1\ k\Omega$, $L = 0.1\ \mu H$ attractors with circuit parameters

The following mathematical model describes the chaotic oscillator below.

$$\frac{d\varphi(t)}{dt} = V_{C1} \tag{4.22}$$

where $\varphi(t)$ is the flux associated with the inductor, L.

$$\frac{dV_{C1}}{dt} = \frac{1}{C_1}\left[\frac{V_{C2} - V_{C1}}{R_1} - I_L\right] \tag{4.23}$$

$$\frac{dV_{C2}}{dt} = \frac{1}{C_2}\left[\frac{V_{C1} - V_{C2}}{R_1} - I_{MR}\right] \tag{4.24}$$

where I_{MR} is the current flowing through MR, and the following mathematical equation defines the current flowing through the inductor.

$$\frac{dI_L}{dt} = \frac{V_{C1}}{L} \tag{4.25}$$

The functionality of the chaotic oscillator is verified by employing different circuit parameters, as shown in Figs. 4.11(b), 4.11(c), and 4.11(d). It can be observed that random and indeterministic characteristics [118] are generated due to variations in the circuit parameters. Note that chaotic oscillators can be employed in various applications ranging from robotics, secure communications, random signal generators, encryption, through-wall radar, and cryptography.

4.5 Conclusion

This work presents a memristor emulator with inverse frequency behaviour consisting of four MOSFETs and an external capacitor capable of operating at high frequencies. The novelty of this emulator is its simplicity and the use of the least number of nonlinear devices. Because of this, the proposed emulator can be realized on silicon without employing any complex process steps. The proposed emulator exhibits 354.66 μm^2 area utilization and 291.78 μW power consumption, which is less than other contemporary emulators available in the literature. Further, due to the absence of any biasing source in the emulator, its static power consumption is zero. Note that the proposed memristor emulator can operate without any external capacitor because of parasitic capacitances of the MOSFETs; however, an external capacitor provides freedom to tune it at different frequencies. This emulator is analyzed at different frequencies, temperatures and process corners, validating its reliability and robustness. A physical experiment conducted using ALD1106 NMOS transistors demonstrates the correctness of the proposed emulator. The effectiveness of the proposed emulator is verified by designing a chaotic oscillator and a NOR gate. Due to its simplicity, versatility, and other memristive properties, such as nonlinearity and memory retention, the proposed emulator is a suitable candidate for designing practical applications.

5

Meminductor Emulator

Contents

Objective:

The realization of a meminductor using only MOSFETs for area and power optimal applications capable of operating at high frequencies.

5.1 Introduction

A meminductance (memory-inductance, L_m) is constituted based on the electrical relationship between the charge (q) and the time integral of the flux (ρ) [4]. Depending upon the dependent term flux (φ) or current ($I(t)$), a meminductor is characterized as either a flux or a current-controlled device. The mathematical expressions of the ideal current-controlled and flux-controlled meminductors were postulated by Di Ventra et al. [4, 128] as follows.

$$\varphi(t) = L_m(x, i(t), t)\ i(t),\ \ \dot{x} = f(x, i(t), t) \tag{5.1}$$

$$i(t) = L_m^{-1}(x, \varphi(t), t)\ \varphi(t),\ \ \dot{x} = f(x, \varphi(t), t) \tag{5.2}$$

where x is an internal state variable, the $\varphi(t)$ and $i(t)$ are the flux and the current going through the meminductor, and L_m and L_m^{-1} are the meminductance and the inverse meminductance, respectively. The generalized mathematical model of the flux-controlled meminductor [4, 129] is mentioned below.

$$i(t) = [\beta + \alpha \int_{-\infty}^{t} \varphi(\tau)\, d\tau]\varphi(t) = [\beta + \alpha\rho(t)]\varphi(t) \tag{5.3}$$

where $\rho(t) = \int_{-\infty}^{t} \varphi(\tau)\, d\tau$ is the time integral of the flux (TIF) or flux momentum [130, 131], and α and β are the constants. Here $L_m^{-1}(\rho(t)) = [\beta + \alpha \int_{-\infty}^{t} \varphi(\tau)\, d\tau]$ represents the inverse meminductance controlled by the state variable $\rho(t)$ [129]. Note that $\rho(t)$ indicates the memory state of the meminductor, and it depends on the past history of the flux. As can be seen in Eq. 5.3, two components, the time integral of the voltage ($\varphi(t) = \int_{-\infty}^{t} V(\tau)\, d\tau$) and the time integral of the flux ($\rho(t) = \int_{-\infty}^{t} \varphi(\tau)\, d\tau$), are essential for designing a meminductor emulator using conventional circuit elements [129]. It can be noted that the presence of TIF is necessary for realizing a flux-controlled meminductor [54, 56–58, 129].

In this work, a simple and optimized circuit for emulating the characteristic behavior of a meminductor is proposed. The proposed meminductor is designed using only MOSFETs to integrate devices

on silicon easily. It implements a simple relationship between the inverse inductance and the TIF. Because of this, it exhibits less hardware complexity utilizing few active elements than other emulators. However, the proposed circuit cannot be employed for realizing other memelements (memristors and memcapacitors) because it is designed for emulating a meminductor. In contrast, mutator-based emulators are universal circuits with higher hardware complexity but can be transformed into memelements, such as memristor, memcapacitor, and meminductor, giving a circuit designer more freedom while designing an application as compared to the proposed emulator. The circuit operation of the proposed emulator is verified using a Cadence Virtuoso design environment with TSMC 180 nm PDKs and is validated experimentally using commercially available CA3080 analog ICs.

The key features of the proposed meminductor emulator [132] design are as follows.

(i) Completely MOSFET-based design suitable for monolithic IC fabrication.

(ii) Lower area utilization and power consumption and higher operating frequency as compared to other known meminductors.

The rest of the chapter is organized as follows. Section 5.2 describes the analytical model of the proposed meminductor. Section 5.3 presents its performance analysis, and section 5.4 depicts an application using the proposed emulator. The conclusion of this chapter is presented in section 5.5.

5.2 Proposed meminductor emulator design

The proposed emulator is designed using two functional blocks, voltage differencing transconductance amplifier (VDTA) and operational transconductance amplifier (OTA), along with two MOS capacitors to realize the meminductor characteristic. The detailed analysis of the proposed meminductor is described below.

5.2.1 Analysis of functional block-1

VDTA is an analog building block introduced by D. Biolek [133]. Fundamentally, VDTA is a transconductance amplifier with two transconductances, g_{m1} and g_{m2}. Further, it consists of differential inputs, and its outputs are controlled by either of the transconductances. The circuit is biased by utilizing a current mirror, and the transconductances can be tuned appropriately by controlling this current mirror.

Fig. 5.1 represents the VDTA symbol [134], which illustrates terminals P and N used for applying differential inputs, Z for obtaining the output of the first transconductance stage, $X+$ and $X-$ for acquiring current outputs of the second transconductance stage, and B_1 and B_2 are biasing terminals for controlling the current through current mirror circuits.

The working of VDTA is explained as follows. The differential input is applied to the input stage and converted into an equivalent current that flows through Z-terminal. The current at Z-terminal leads to the formation of voltage V_Z, which depends on the load connected at this terminal. The voltage V_Z acts as an input to the second stage of VDTA and causes I_{X+} and I_{X-} to flow through terminals $X+$ and $X-$, respectively. These currents (I_{X+} and I_{X-}) are equal in magnitude but opposite in direction, as shown in Fig. 5.1.

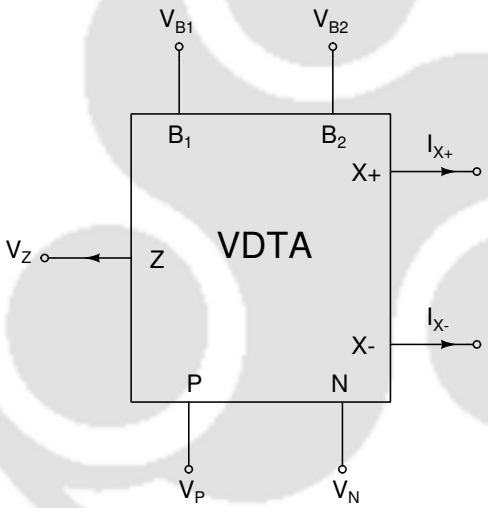


Figure 5.1: VDTA symbol

Further, the relation between the terminals of VDTA can be stated using the following mathematical equations.

$$\begin{bmatrix} I_Z \\ I_{X+} \\ I_{X-} \end{bmatrix} = \begin{bmatrix} g_{m1} & -g_{m1} & 0 \\ 0 & 0 & g_{m2} \\ 0 & 0 & -g_{m2} \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \end{bmatrix} \tag{5.4}$$

where g_{m1} and g_{m2} are transconductances of the first and second stages of VDTA, respectively.

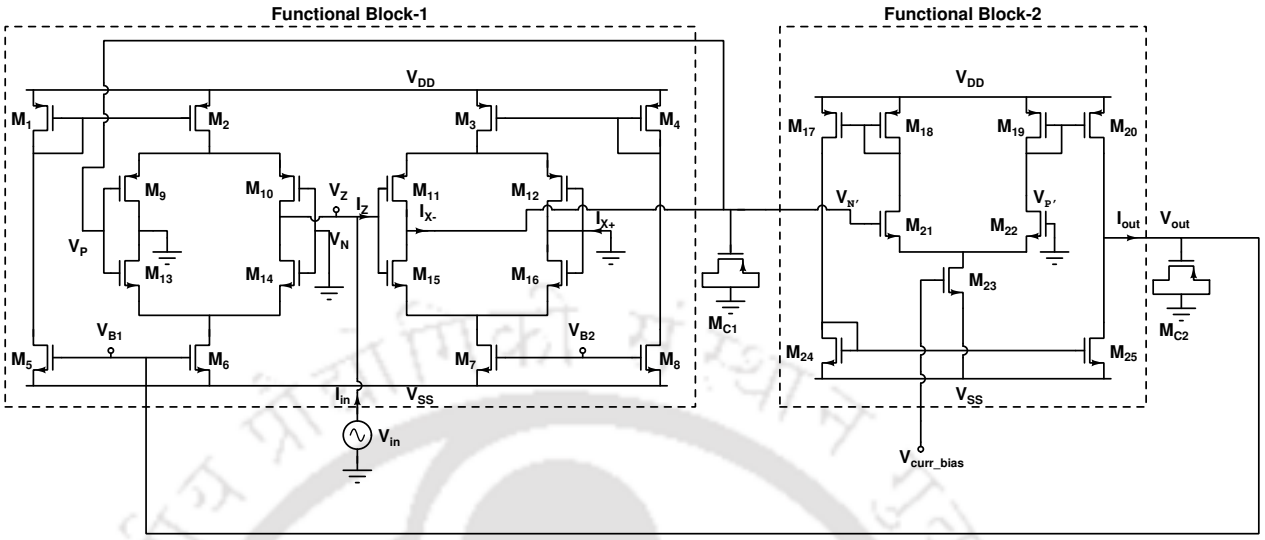


Figure 5.2: The schematic of the proposed meminductor emulator

The transconductances g_{m1} and g_{m2} are expressed in terms of transconductances of individual transistors, g_i, shown in functional block-1 (VDTA) of Fig. 5.2 using the mathematical equation mentioned below.

$$\begin{aligned} g_{m1} &= \frac{g_9 g_{10}}{g_9 + g_{10}} + \frac{g_{13} g_{14}}{g_{13} + g_{14}} \\ g_{m2} &= \frac{g_{11} g_{12}}{g_{11} + g_{12}} + \frac{g_{15} g_{16}}{g_{15} + g_{16}} \end{aligned} \tag{5.5}$$

Here, g_i, the transconductance of the i^{th} transistor, is defined as follows.

$$g_i = \sqrt{2 k_i I_i} \tag{5.6}$$

where k_i and I_i are the process parameter and the current flowing through the i^{th} transistor, respectively. Since VDTA is designed using the same aspect ratio for both PMOS ($M_9 - M_{12}$) and NMOS ($M_{13} - M_{16}$) transistors, g_{m1} and g_{m2} defined in Eq. 5.5 can be reformulated as,

$$\begin{aligned} g_{m1} &= \frac{g_{10} + g_{13}}{2} \\ g_{m2} &= \frac{g_{12} + g_{15}}{2} \end{aligned} \tag{5.7}$$

Using Eqs. 5.6 and 5.7, g_{m1} and g_{m2} can be remodeled as,

$$g_{m1} = \sqrt{2}\left[\frac{\sqrt{k_{10}I_{10}} + \sqrt{k_{13}I_{13}}}{2}\right]$$
$$g_{m2} = \sqrt{2}\left[\frac{\sqrt{k_{12}I_{12}} + \sqrt{k_{15}I_{15}}}{2}\right] \tag{5.8}$$

Employing symmetricity of the transistors, I_{10}, I_{12}, I_{13}, and I_{15} can be expressed in terms of I_6 and I_7. Using $I_6 = \sqrt{\frac{k_6}{2}\left[V_{B1} - V_{SS} - V_{th}\right]^2}$ and $I_7 = \sqrt{\frac{k_7}{2}\left[V_{B2} - V_{SS} - V_{th}\right]^2}$, g_{m1} and g_{m2} can be further simplified as mentioned below. Here, V_{B2} is an external biasing voltage of the second stage of VDTA, while $V_{B1} = V_{out}$.

$$I_{10} = I_{13} = \frac{I_6}{2}; I_{12} = I_{15} = \frac{I_7}{2} \tag{5.9}$$

$$g_{m1} = K_{M1}\left[V_{B1} - V_{SS} - V_{th}\right]$$
$$g_{m2} = K_{M2}\left[V_{B2} - V_{SS} - V_{th}\right] \tag{5.10}$$

where $K_{M1} = \sqrt{\frac{k_6}{2}}\left[\frac{\sqrt{k_{10}}+\sqrt{k_{13}}}{2}\right]$ and $K_{M2} = \sqrt{\frac{k_7}{2}}\left[\frac{\sqrt{k_{12}}+\sqrt{k_{15}}}{2}\right]$ are constants.

5.2.2 Analysis of functional block-2

The functional block-2 is designed for characterizing the time integral of flux (TIF) ($\rho(t) = \int_{-\infty}^{t} \varphi(t)\, dt$), which is realized using an OTA. Its schematic ($M_{17} - M_{25}$) represented as functional block-2 is depicted in Fig. 5.2, which takes differential voltage as an input and outputs current, I_{out}. The OTA consists of an input stage ($M_{21} - M_{22}$), a current sink (M_{23}), and a current mirror ($M_{17} - M_{20}$ and $M_{24} - M_{25}$). As we know, OTA can be modeled using the following equation mentioned below.

$$I_{out} = g_{m3}\left(V_{P'} - V_{N'}\right) \tag{5.11}$$

where g_{m3} is the transconductance of an OTA.

The proposed meminductor emulator consists of two MOS capacitors (M_{C1} and M_{C2}), which are realized using PMOS transistors by shorting their drain, source, and body terminals, as shown in Fig. 5.2. The first MOS capacitor, M_{C1}, is connected to the input terminal of OTA to obtain flux ($\varphi(t) = \int_{-\infty}^{t} V_{in}(t)\, dt$) equivalent to the applied voltage. The second MOS capacitor M_{C2} is connected to the output of OTA, which is employed to realize TIF in the circuit.

A sinusoidal signal, $I_{in}(t)$, is applied to the meminductor, which is connected to the Z-terminal of the VDTA block. The Z-terminal current, I_Z, can be modeled using Eq. 5.4 and is expressed below.

$$I_Z = I_{in}(t) = g_{m1} V_P \tag{5.12}$$

It can be observed in Fig. 5.2 that $V_{X-} = V_{N'}$ and are connected to M_{C1}. Using Eq. 5.4, $V_{N'}$ can be formulated as mentioned below.

$$\begin{aligned} V_{X-} = V_{N'} &= \frac{1}{C_{M_{C1}}} \int_{-\infty}^{t} I_{X-}\, dt \\ &= -\frac{g_{m2}}{C_{M_{C1}}} \int_{-\infty}^{t} V_{in}\, dt = -\frac{g_{m2}}{C_{M_{C1}}} \varphi(t) \end{aligned} \tag{5.13}$$

Since the terminals P of VDTA and N' of OTA are connected, therefore, Eq. 5.13 can be expressed as,

$$V_{N'} = V_P = -\frac{g_{m2}}{C_{M_{C1}}} \varphi(t) \tag{5.14}$$

The terminal $X-$ of VDTA is connected to the inverting input, $V_{N'}$, of the OTA. Thus, the output of OTA, V_{out}, can be determined by employing the following mathematical expression.

$$\begin{aligned} V_{out} = V_{B1} &= \frac{1}{C_{M_{C2}}} \int_{-\infty}^{t} I_{out}\, dt \\ &= -\frac{1}{C_{M_{C2}}} \int_{-\infty}^{t} g_{m3} V_{N'}\, dt \end{aligned} \tag{5.15}$$

After substituting $V_{N'}$, as mentioned in Eq. 5.14 in Eq. 5.15, the following equation can be obtained.

$$\begin{aligned} V_{out} = V_{B1} &= \frac{g_{m2} g_{m3}}{C_{M_{C1}} C_{M_{C2}}} \int_{-\infty}^{t} \varphi(t)\, dt \\ &= \frac{g_{m2} g_{m3}}{C_{M_{C1}} C_{M_{C2}}} \rho(t) = V_\rho \end{aligned} \tag{5.16}$$

Using Eq. 5.16, g_{m1} depicted in Eq. 5.10 can be further simplified as follows.

$$g_{m1} = K_{M1} \left[\frac{g_{m2} g_{m3}}{C_{M_{C1}} C_{M_{C2}}} \rho(t) - V_{SS} - V_{th} \right] \tag{5.17}$$

Here, $\rho(t)$ is the time integral of flux required for modelling meminductor behavior, which is explained in the following section.

5.2.3 Analysis of meminductor behavior

The analytical model of meminductor characteristics described in Eq. 5.3 and realized by substituting Eq.5.17 into Eq.5.12 is mentioned below.

$$I_{in}(t) = g_{m1}V_P = \underbrace{K_{M1}\left(\frac{g_{m2}^2 g_{m3}}{C_{M_{C1}}^2 C_{M_{C2}}}\right)\rho(t)\,\varphi(t)}_{\text{a nonlinear meminductor}} \underbrace{- K_{M1}\left(V_{SS}+V_{th}\right)\frac{g_{m2}}{C_{M_{C1}}}\varphi(t)}_{\text{a linear inductor}} \tag{5.18}$$

Eq. 5.18 can be further simplified as follows.

$$\begin{aligned} I_{in}(t) &= [\alpha\rho(t)+\beta]\varphi(t) \\ &= \alpha\rho(t)\dot{\rho}(t) + \beta\varphi(t) = \frac{\alpha}{2}\frac{d(\rho(t))^2}{dt} + \beta\varphi(t) \end{aligned} \tag{5.19}$$

where $\alpha = \frac{K_{M1}g_{m2}^2 g_{m3}}{C_{M_{C1}}^2 C_{M_{C2}}}$, $\beta = -(V_{SS}+V_{th})\frac{K_{M1}g_{m2}}{C_{M_{C1}}}$, and $\dot{\rho}(t) = \frac{d\rho(t)}{dt} = \varphi(t)$. $L_m^{-1}(\rho(t)) = [\beta + \alpha\rho(t)]$ represents the inverse meminductance governed by the state variable $\rho(t)$ [129].

The proposed emulator can mimic the meminductor whose inverse meminductance is proportional to $\rho(t)$ [129]. Note that the inductance value depends upon the term time definite integral of the flux. Thus, $\rho(t)$ explains the past dependence and is the memory state of the meminductor.

The equivalent circuit corresponding to the Eq. 5.19 is the parallel connection of two circuit elements shown in Fig. 5.3, having the following constitutive relations.

(a) a linear inductor $I'_{in}(t) = \beta\varphi(t)$

(b) an ideal meminductor $I''_{in}(t) = \frac{\alpha}{2}\frac{d(\rho(t))^2}{dt}$

The two constitutive relationships of the linear inductor and meminductor, (a) and (b), can be rewritten in the integral flux–charge domain [130]. Hence, (a) can be written as mentioned below.

$$I'_{in}(t) = \beta\varphi(t) \Rightarrow q'_{in}(t) = \beta\rho(t) \tag{5.20}$$

Further, (b) is defined as follows.

$$I''_{in}(t) = \frac{\alpha}{2}\frac{d(\rho(t))^2}{dt} \Rightarrow q''_{in}(t) = \frac{\alpha}{2}(\rho(t))^2 \tag{5.21}$$

where the charges $q'_{in}(t) = \int_{-\infty}^{t} I'_{in}(t)\,dt$ and $q''_{in}(t) = \int_{-\infty}^{t} I''_{in}(t)\,dt$.

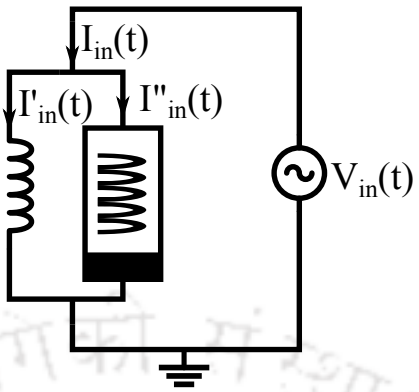


Figure 5.3: The equivalent circuit of the proposed emulator

The following observations are derived using Eqs. 5.18 and 5.19 for analyzing meminductor behavior.

- Meminductor depends on the nonlinear function of flux ($\varphi(t)$), which is realized by employing TIF ($\rho(t)$).
- It consists of a linear inductor and a nonlinear meminductor.
- The transconductances, g_{m2} and g_{m3}, are tunable parameters used to obtain desired characteristics of a meminductor.
- The characteristics of the meminductor exhibit pinched hysteresis loop (PHL). As the frequency of the applied signal increases, the lobe area of PHL decreases, becoming a straight line at very high frequencies.

The proposed meminductor is completely designed using active devices (MOSFETs) only, which makes it suitable for realizable on silicon. Note that the inherent properties of VDTA and OTA [135] are utilized to perform integration and multiplication operations without a multiplier. Further, MOS capacitors used in the meminductor aid in increasing operating frequency. The analytical model of the proposed meminductor is verified by performing parametric analyses, which are explained in the following section.

5.3 Performance analysis of the proposed meminductor

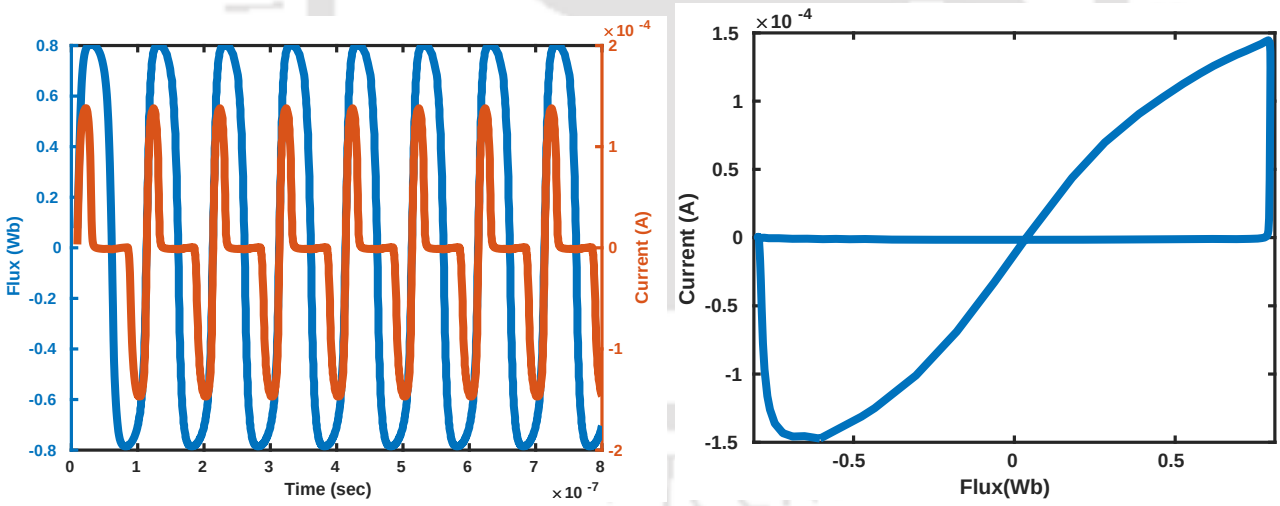
The mathematical model of the proposed meminductor is verified both numerically and experimentally. The numerical analysis is performed using Cadence Virtuoso analog and design environment

with TSMC 180 nm PDK. The aspect ratio of MOSFETs and MOS capacitors used for optimal performance in the proposed meminductor emulator are mentioned in Table 5.1.

Table 5.1: Transistor sizes

$Transistors$	$W/L\left(\frac{\mu m}{\mu m}\right)$
$M_1 - M_4, M_9 - M_{12}$	$\frac{13}{0.36}$
$M_5 - M_8, M_{13} - M_{16}$	$\frac{4}{0.36}$
$M_{17} - M_{25}$	$\frac{4}{2}$
M_{C1}	$\frac{200}{1.5}$
M_{C2}	$\frac{80}{1.5}$

The power supplies V_{DD} and V_{SS} of 900 mV and -900 mV are applied to the proposed meminductor circuit. Also, $V_{B2} = 100$ mV and $V_{curr\_bias} = -50mV$ are the bias voltage in the second stage of functional block-1 and the current source of functional block-2, respectively, as illustrated in Fig. 5.2.



(a) (b)

Figure 5.4: Proposed meminductor at 250 mV and 10 MHz (a) Transient analysis and (b) $I_{in}(t) - \varphi(t)$ characteristic (PHL)

5.3.1 Parametric analysis

Transient analysis of the proposed meminductor is analyzed by applying a sinusoidal signal having a peak voltage of 250 mV and frequency of 10 MHz, as depicted in Fig. 5.4(a). It can be observed that the input current $I_{in}(t)$ is zero whenever the input flux $\varphi(t)$ is zero [47, 87], which satisfies the

constitutive relationship of the proposed emulator defined in Eq. 5.19. Its device characteristic is a function of the input flux $\varphi(t)$ and the state variable $\rho(t)$. The $I_{in}(t) - \varphi(t)$ characteristic exhibits a pinched hysteresis loop (PHL), in which $I_{in}(t) = 0$ at $\varphi(t) = 0$ for a sinusoidal input signal [47], as shown in Fig. 5.4(b). However, the PHL of an ideal meminductor passes through the origin [136], but the PHL of the proposed emulator does not cross at the origin due to an initial current flowing through the meminductor [87, 137], causing an initial transient shown in 5.4(a). Further, the PHL of the ideal meminductor is odd-symmetric [136], but the proposed meminductor exhibits non-odd-symmetric PHL due to the parasitic elements and the non-ideal behaviour of the MOSFETs [138]. Note that the input current is the current flowing through the Z terminal of functional block-1, and the flux is measured as the voltage across $C_{M_{C1}}$.

The functionality of the proposed meminductor emulator evaluated at different frequencies is illustrated in Fig. 5.5(a), which shows that the lobe area of PHL decreases when frequency increases, and it becomes linear at very high frequencies [40, 41, 47, 87]. This analysis validates another fingerprint of the meminductor [87, 137]. Note that the maximum operating frequency of the proposed meminductor is 20 MHz to obtain an acceptable PHL. Thus, it can be stated that the proposed meminductor emulator mimics the behavior of a meminductor as per the expectations [87, 129].

It is observed that the rise in the input voltage (V_{in}) increases input current, which in turn expands the lobe area of the PHL, as shown in Fig. 5.5(b). Bias voltage V_{B2} controls transconductance g_{m2}, which is used to tune meminductor characteristics. It can be seen that a surge in V_{B2} increases g_{m2}, which leads to an expanded lobe area of the PHL, as illustrated in Fig. 5.5(c).

The proposed meminductor is examined at temperatures ranging from $-40°C$ to $40°C$, as shown in Fig. 5.5(d). It can be observed that the lobe area of PHL reduces and enlarges when temperature increases and decreases, respectively. It is due to the reduction in the current flowing through the circuit at higher temperatures, while at a lower temperature, current increases affecting the lobe area of the PHL.

The robustness of the proposed meminductor is verified at different process corners (FF, FS, SF, and SS) along with NN, which denotes nominal fabrication parameters as shown in Fig. 5.5(e). The lobe area of PHL is the maximum at FF (fast NMOS and fast PMOS transistors) and minimum at SS (slow NMOS and slow PMOS transistors) as expected. The proposed design is characterized with respect to both temperature and process corner variations, as illustrated in Fig. 5.5(f). It can be

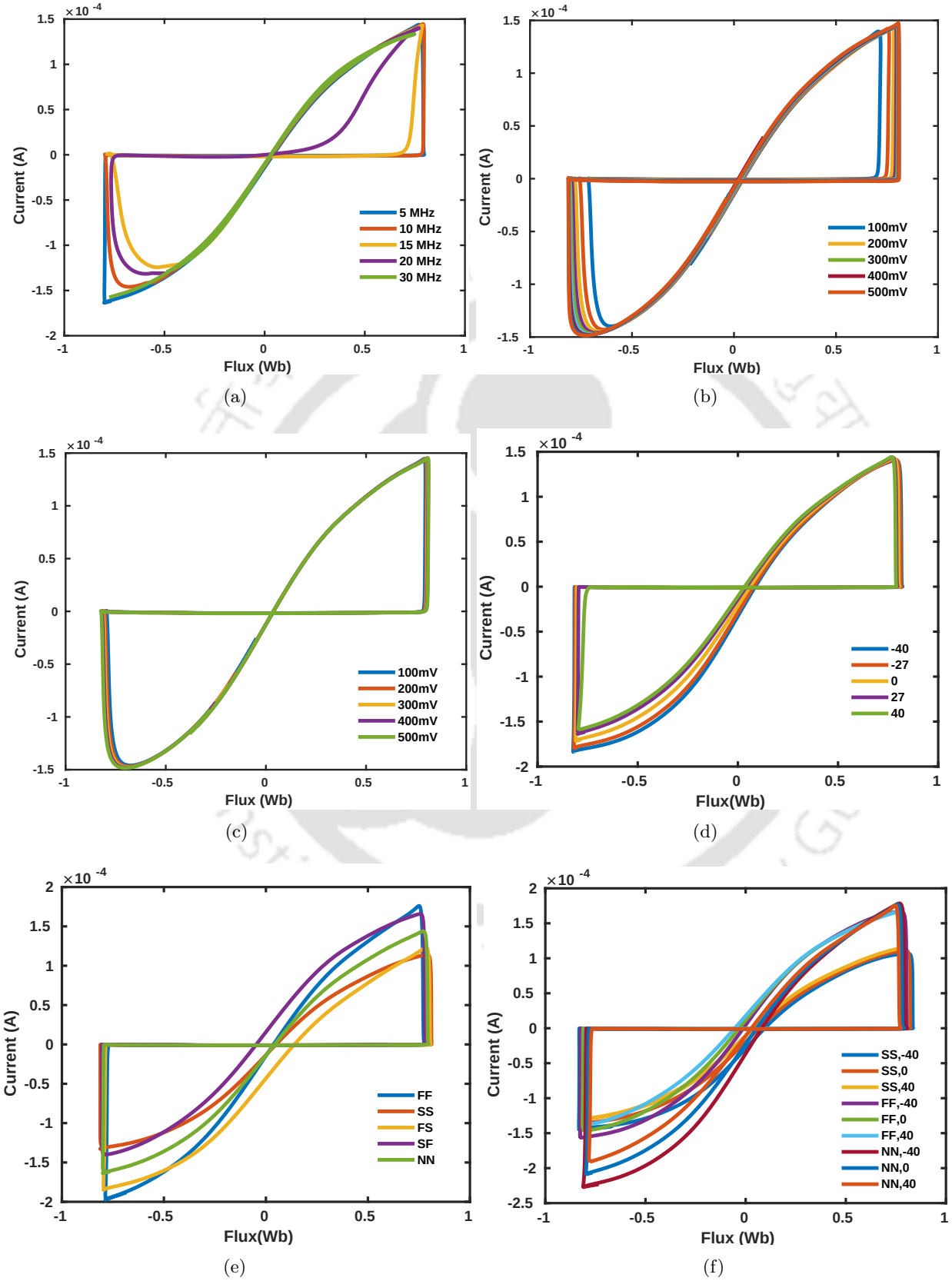


Figure 5.5: Numerical analysis at different (c) Frequencies (b) Input voltages (c) Bias voltages (d) Temperatures (e) Process corners and (f) Process corners with temperature

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seen that the behavior of the meminductor is maintained by generating PHL without any distortion irrespective of variations in temperature and process corners. It can be further observed that the proposed meminductor emulator exhibits acceptable characteristics in the worst-case scenarios, i.e., (SS, -40 C), (SS, 40 C), (FF, -40 C), (FF, 40 C), (NN, -40 C) and (NN, 40 C). The proposed emulator showcases similar characteristics in the normal scenarios, i.e., SS, NN, and FF at 0 C. Thus, it can be stated that parametric analyses verify the reliability and robustness of the proposed meminductor emulator.

5.3.2 Pre- and post-layout validation

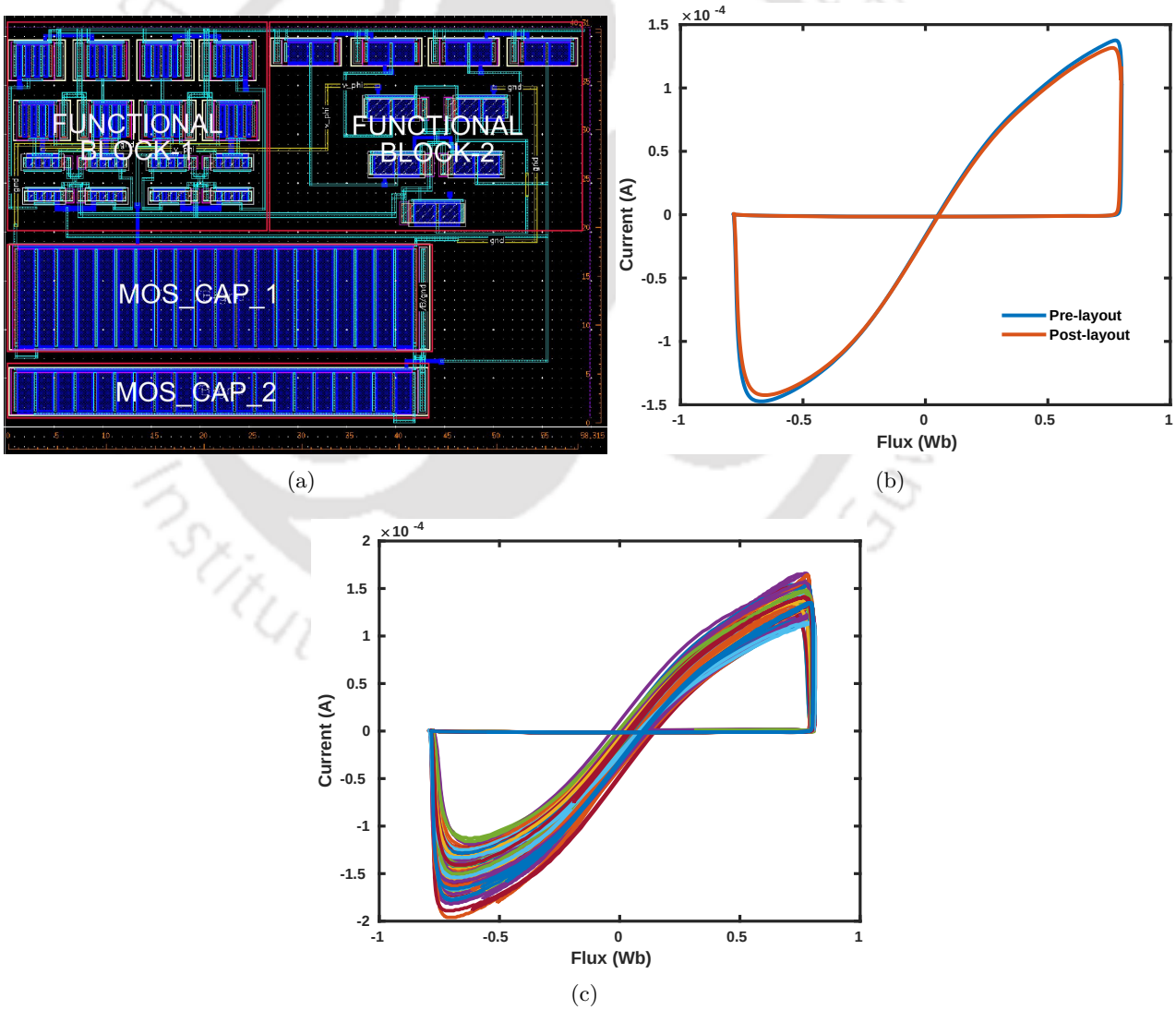


Figure 5.6: (a) Layout design (b) Pre and Post-layout analysis and (c) Monte Carlo analysis of the proposed meminductor emulator

The correctness of the proposed meminductor emulator is further validated through pre- and post-layout analyses performed using the Cadence Virtuoso framework employing TSMC 180 nm PDK. The layout of the proposed emulator includes two functional blocks (VDTA and OTA) integrated with two MOS-capacitors as shown in Fig. 5.6(a). Its area utilization is 2350.67 μm^2 (58.315 $\mu m^2 \times 40.31$ μm^2). PHLs obtained in the pre-and post-layout analyses are exhibited in Fig. 5.6(b). Note that the variation in post-layout PHL as compared to pre-layout PHL is due to the presence of parasitic elements. However, it is within the acceptable limits and differed by 6.89% at most. The proposed emulator realizes the meminductive behaviour by directly implementing the TIF ($\rho(t) = \int_{-\infty}^{t} \varphi(\tau)\, d\tau$) by using only a few active elements with a maximum operating frequency of 20 MHz than other emulators. The direct implementation of the TIF in the proposed emulator requires double integration causing instability, but the proposed emulator exhibits stable behaviour due to the presence of parasitic elements. The proposed emulator utilizes symmetric MOSFETs, but the non-ideal effects of MOSFETs lead to mismatches, and this can be evaluated by performing Monte Carlo analysis, as shown in Fig. 5.6(c). It can be observed that the deviations in the $I_{in}(t) - \varphi(t)$ characteristic are due to the process parameter variations and device mismatches. Also, PHLs shift from the origin [37] (non-zero crossing) compared to the ideal behaviour of the meminductor [136]. However, the meminductive behaviour is retained by generating the PHLs, exhibiting robustness of the process emulator. Note that the PHLs shifting from the origin and their non-zero crossings are due to an initial current flowing through the meminductor and the presence of parasitic elements, causing non-zero crossing and non-odd-symmetric PHL [37, 44, 137] compared to the ideal meminductor, exhibiting zero-crossing and odd-symmetric PHL [136].

5.3.3 Experimental analysis

The proposed meminductor emulator circuit is also validated by conducting physical experiments using commercially available off-the-shelf components. In this experiment, CA3080 [105] analog IC block is utilized to realize two functional blocks (VDTA and OTA) of the proposed meminductor. Further, CA3080 acts as a transconductance amplifier, and its transconductance is controlled externally by applying a voltage at the bias current terminal. The circuit diagram of the physical experiment for realizing a proposed meminductor emulator is shown in Fig. 5.7. It can be seen that the 1st, 2nd, and 3rd OTAs are connected to mimic the Functional Block-1 (VDTA). This VDTA and the 4th OTA emulate the behavior of the proposed meminductor, as shown in Fig. 5.2. It consists of R_{B2}, R_{B3}, and

R_F used as current limiting resistors, a potentiometer R_{var1} for adjusting meminductor characteristics, and two capacitors C_1 and C_2. Note that the transconductance g_m of CA3080 is controlled by the current flowing through its current bias terminal. The above mentioned components are connected to configure a meminductor on the breadboard, as illustrated in Fig. 5.8(a), to perform a physical experiment.

The experimental setup consists of a signal generator Rigol DG1022 for providing an input signal at different frequencies. Tektronix MDO3012 Mixed Domain Oscilloscope is utilized to observe respective signal waveforms, including transients and their corresponding I_{in}-φ characteristics (PHLs). An Aplab power supply is used for supplying regulated DC voltage to the circuit shown in Fig.5.8(b). The capacitors and transconductances are employed to tune the operating frequencies of the meminductor. In this experiment, for obtaining desired characteristics of a meminductor, $C_1 = 10\,pF$ and $C_2 = 0.1\mu F$ are used, and OTAs are biased with $V_{B2} = 3.6\,V$ and $V_{B3} = 6.4\,V$ using a regulated DC voltage source through $R_{B2} = 220\ k\Omega$ and $R_{B3} = 220\ k\Omega$, respectively. Additionally, $R_F = 260\ k\Omega$ is utilized to regulate the current in the acceptable range of CA3080, and supply voltages of $V_{DD} = 15\ V$ and $V_{SS} = -15\ V$ are applied to the OTAs of CA3080 IC. The transient characteristics and PHL of the meminductor are obtained by applying a 200 Hz signal having a peak voltage of 500 mV, as shown in Fig. 5.9. It can be observed that the outcome of this experiment is in concurrence with the outcome of numerical analysis.

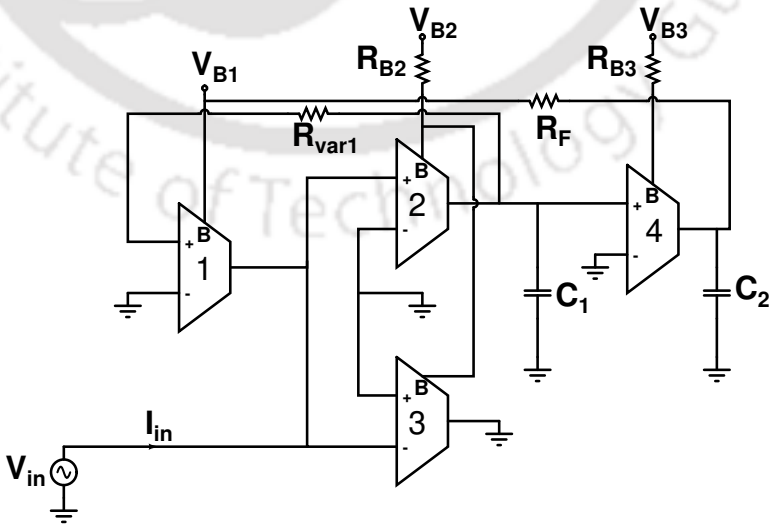
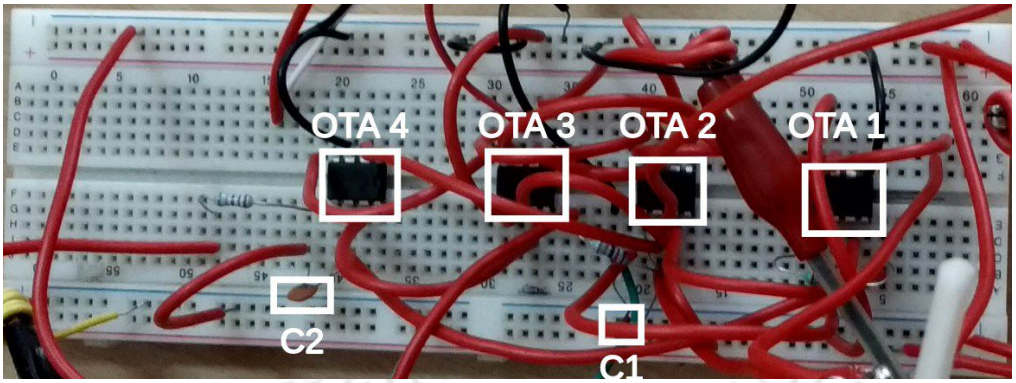
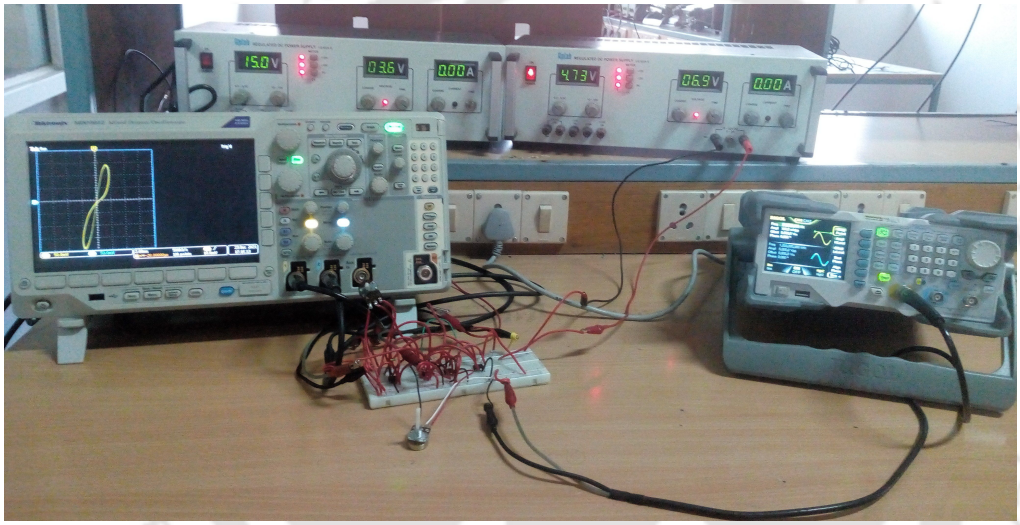


Figure 5.7: Experimental circuit of the proposed meminductor using CA3080

Further, the experiment is performed at different frequencies by applying 50 mV peak voltage,

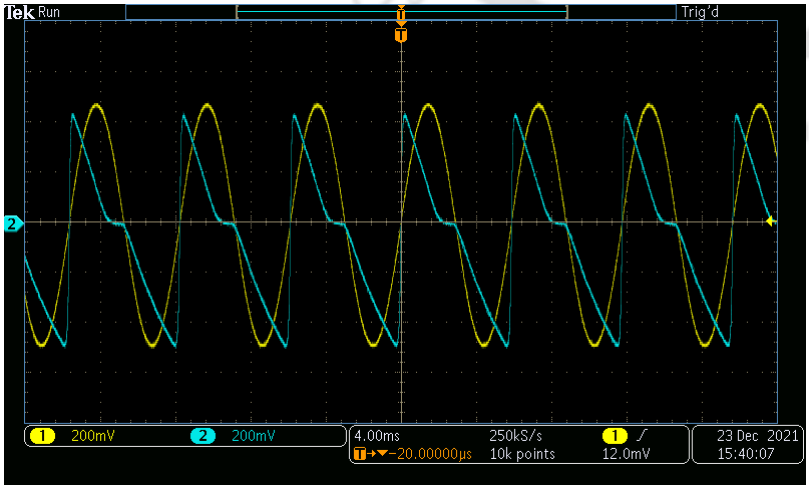


(a)

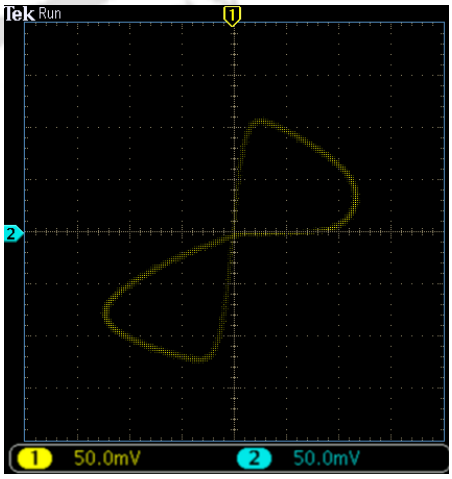


(b)

Figure 5.8: (a) Circuit configuration on breadboard and (b) Experimental setup of the proposed emulator

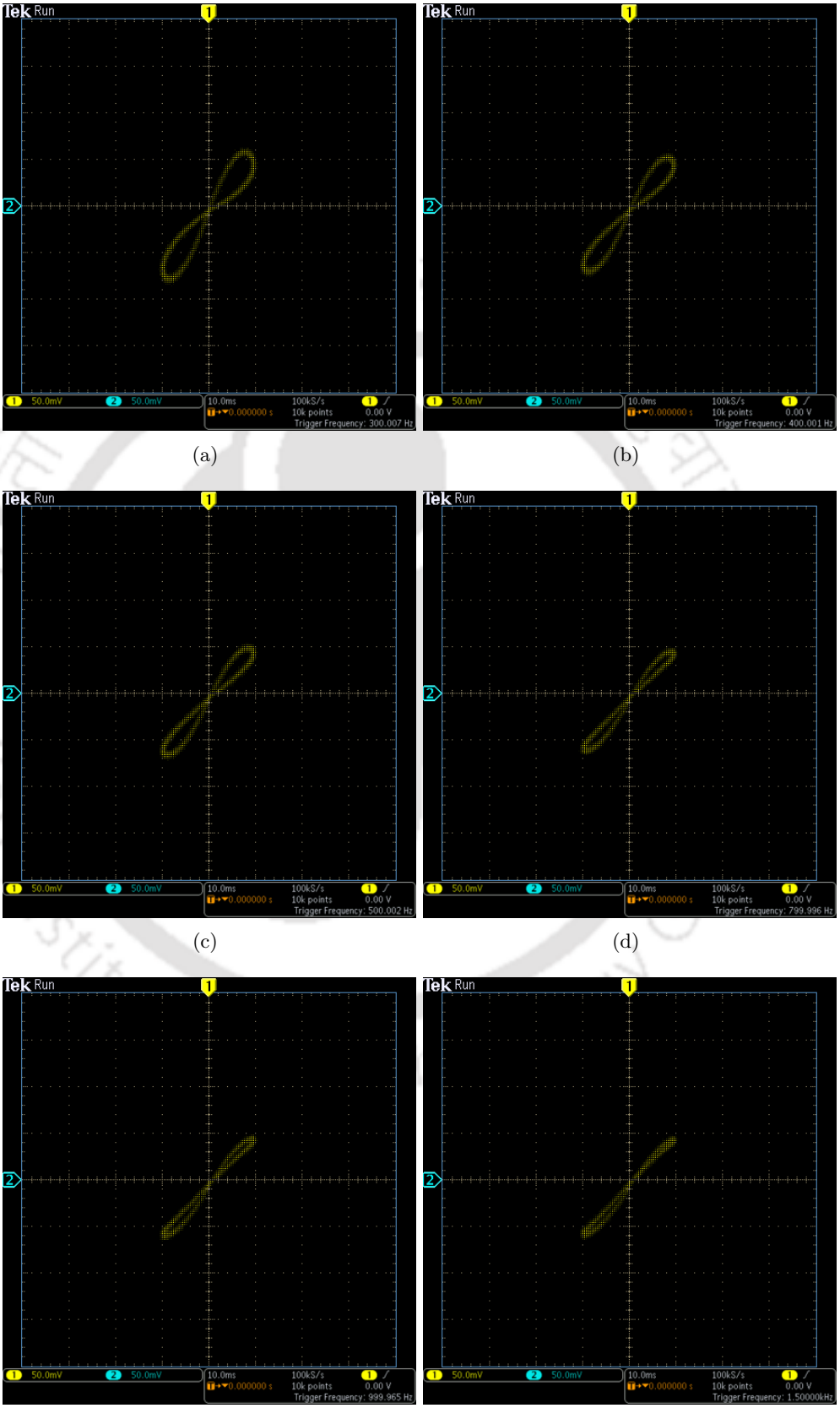


(a)



(b)

Figure 5.9: Experimental results (a) Transient analysis and (b) PHL at 200 Hz



(a) (b) (c) (d) (e) (f)

Figure 5.10: PHL at different frequencies using $C1$ of 10 pF and $C2$ of 0.1 μF (a) 300 Hz (b) 400 Hz (c) 500 Hz (d) 800 Hz (e) 1 kHz and (f) 1.5 KHz

Table 5.2: Comparative analysis of proposed meminductor with other state-of-the-art meminductor emulators

Ref.	Active components	Passive components	No. of transistors	Max. operating freq.	Expt/Sim.	Area	Technology used
[57]	2-OTA, 1-DVCC	1-resistor, 1-capacitor	34	10 MHz	Sim.	-	Cadence Virtuoso 180 nm
[58]	3-OTA	2-capacitors	33	10 MHz	Sim.	-	Cadence 180 nm
[54]	2-VDTA	2-capacitors	32	1 MHz	Both	-	Cadence 180 nm
[42]	3-CCII, 1-analog multiplier	2-resistor, 2-capacitor	-	5 kHz	-	-	Multisim
[45]	2-opamps	1-TIF controlled resistor, 1-capacitor, 3-resistors	-	10 KHz	-	-	SPICE
[55]	1-buffer, 3-opamps, 1-analog multiplier, 2-CCII	8-resistors, 2-capacitors	-	800 Hz	-	-	PSPICE
[39]	3-CCII, 1-analog adder, 1-analog multiplier	3-resistors, 2-capacitors	-	10 Hz	-	-	PSPICE
[56]	1-CCII, 1-OTA	2-capacitors, 2-resistors	43	900 kHz	Both	8061 μm^2	Cadence Virtuoso TSMC 180nm
[33]	4-CCII, 1-analog multipliers, 1-opamp	6-resistors, 2-capacitors	-	960 kHz	Expt.	375.4 mm^2	-
This work	**1-VDTA, 1-integrator**	-	**27**	**20 MHz**	**Both**	2350.67 μm^2	**Cadence Virtuoso TSMC 180nm**

as shown in Fig. 5.10. It is mentioned that the lobe area of PHL starts shrinking with an increase in the frequency of applied input and tends to become linear at high frequencies, which validates the frequency-dependent behaviour of the meminductor emulator. It can also be seen that all the PHLs of the experimental analysis are non-zero crossing and non-odd-symmetric. This behaviour of the proposed emulator is due to the parasitic elements [44] and the non-idealities of the components utilized in the physical experiments [138]. It can be observed in Fig. 5.10 that the experimental characteristics of the proposed meminductor emulator are in concurrence with the characteristics obtained through pre- and post-layout numerical analysis. Further, the off-the-shelf elements used in the experimental validation are connected to mimic the operation of the proposed circuit. Since the elements are not a replica of the CMOS circuit on the silicon, the operating frequency of the proposed meminductor realized physically is limited. Thus, this not only validates the correctness of the proposed emulator but also paves the way to be used in real-life applications. It is compared with various state-of-the-art meminductors mentioned below to showcase its effectiveness.

The meminductor emulators reported in the literature [33,39,42,45,55,56] consist of more analog IC blocks and passive components as compared to our proposed emulator. These emulators exhibit higher hardware complexity with limited operating frequency. The meminductors [54, 57, 58] are realized to obtain PHL at high frequencies (in the range of MHz) at the expense of higher complexity and design area. The proposed meminductor contains only 27 MOSFETs utilizing less area and power and operates at 20 MHz. A detailed comparison with other state-of-the-art emulators is presented in Table 5.2 for completeness. It can be observed that the proposed emulator exhibits $2\times, 20\times, 22.22\times$, and $20.83\times$ better operating frequency range as compared to [57] and [58], [54], [56], and [33], respectively. It also showcases $3.43\times$ less area than [56], which is its nearest contemporary meminductor in terms of area and operating frequency, whereas it is $258\times$ more power efficient than [33]. This comparison illustrates the effectiveness of the proposed meminductor to be used in area and power optimal high frequency applications.

5.4 Application of the proposed meminductor

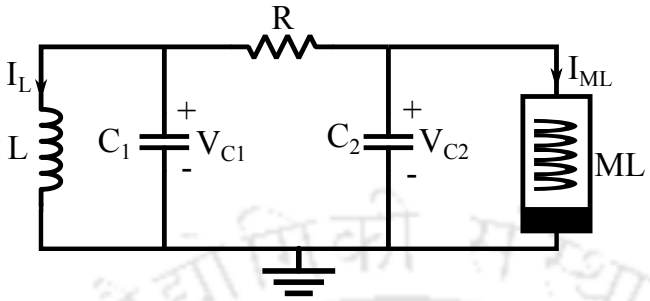


Figure 5.11: Circuit diagram of chaotic oscillator using meminductor

The efficiency of the proposed meminductor emulator is showcased by implementing a chaotic oscillator. As we know, the chaotic circuit was introduced by Leon O. Chua [139] using nonlinear circuit elements. It behaves like a chaotic oscillator [117], consisting of one or more nonlinear elements and other linear circuit elements (resistor, capacitor, and inductor). In this section, a chaotic oscillator is designed using the proposed meminductor as a nonlinear circuit element shown in Fig. 5.11. The components used in this oscillator include an inductor L, capacitors C_1 and C_2, a resistor R, and the proposed meminductor ML.

The chaotic oscillator is analyzed by the following mathematical expressions.

$$\frac{d\varphi_1(t)}{dt} = V_{C1} \tag{5.22}$$

$$\frac{d\varphi_2(t)}{dt} = V_{C2} \tag{5.23}$$

where $\varphi_1(t)$ and $\varphi_2(t)$ are the flux associated with L and ML.

$$\frac{dV_{C1}}{dt} = \frac{1}{C_1}\left[\frac{V_{C2} - V_{C1}}{R_1} - I_L\right] \tag{5.24}$$

$$\frac{dV_{C2}}{dt} = \frac{1}{C_2}\left[\frac{V_{C1} - V_{C2}}{R_1} - I_{ML}\right] \tag{5.25}$$

where I_{ML} is the current flowing through ML. The following mathematical model gives the current passing through the meminductor.

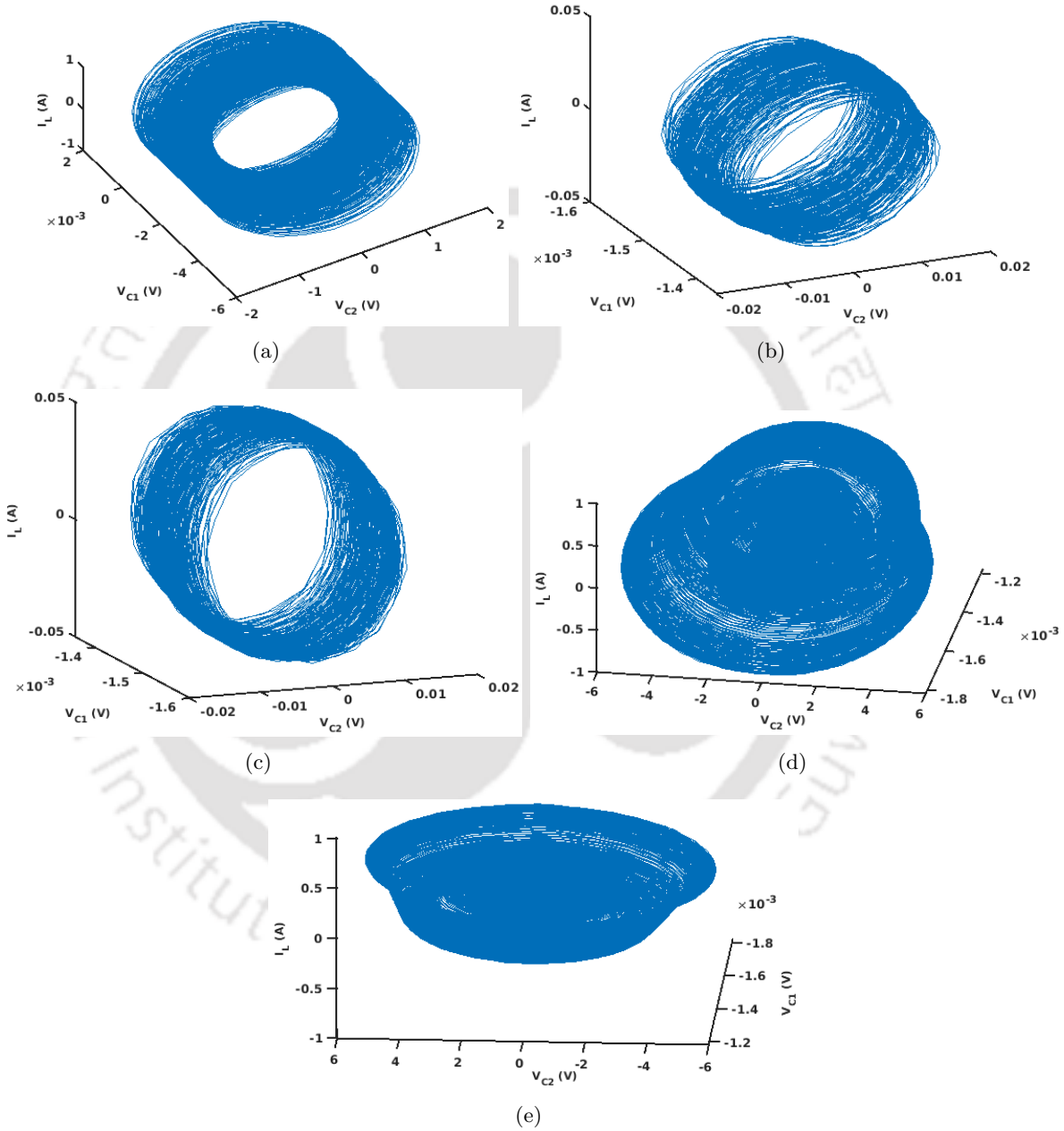


Figure 5.12: Chaotic oscillator attractors with circuit parameters (a) $C_1 = 10\ pF$, $C_2 = 100\ pF$, $V_{C2}(0) = 900\ mV$, $R = 20\ k\Omega$, $L = 0.4\ \mu H$ (b) and (c) $C_1 = 10\ nF$, $C_2 = 1\ nF$, $R = 2\ k\Omega$, $L = 1\ \mu H$ in different orientations, and (d) and (e) $C_1 = 10\ pF$, $C_2 = 1\ pF$, $R = 20\ k\Omega$, $L = 0.4\ \mu H$

$$I_{in}(t) = I_{ML} = [\alpha\rho(t) + \beta]\varphi(t)$$
$$= \alpha\rho(t)\dot{\rho}(t) + \beta\varphi(t) = \frac{\alpha}{2}\frac{d(\rho(t))^2}{dt} + \beta\varphi(t) \tag{5.26}$$

where $\alpha = \frac{K_{M1}g_{m2}^2 g_{m3}}{C_{M_{C1}}^2 C_{M_{C2}}}$, $\beta = -(V_{SS} + V_{th})\frac{K_{M1}g_{m2}}{C_{M_{C1}}}$, and $\dot{\rho}(t) = \frac{d\rho(t)}{dt} = \varphi(t)$.

Substituting Eq. 5.26 in Eq. 5.25, the following equation is obtained.

$$\frac{dV_{C2}}{dt} = \frac{1}{C_2}\left[\frac{V_{C2} - V_{C1}}{R_1} - \frac{\alpha}{2}\frac{d(\rho(t))^2}{dt} - \beta\varphi_2(t)\right] \tag{5.27}$$

$$\frac{dI_L}{dt} = \frac{V_{C1}}{L} \tag{5.28}$$

The output of the chaotic oscillator is obtained by using three different combinations of the circuit parameters, as shown in Fig. 5.12. It is to be noted that the different chaotic behaviors [51, 118] are obtained by changing circuit parameters only. Therefore, it can be stated that various attractors can be designed by changing circuit parameters. The resulting chaotic circuit produces an indeterministic behavior, which can be used for secure communication, cryptography, and random signal generators. Thus, the proposed meminductor is a potential candidate for a wide range of applications due to its less hardware complexity, optimized area, and higher operating frequency.

5.5 Conclusion

In this work, a flux-controlled meminductor emulator is proposed using MOSFETs consisting of two analog functional blocks and two MOS-capacitors. Its characteristics are validated using Cadence Virtuoso with TSMC 180 nm PDK in different scenarios. It is experimentally verified by employing off-the-shelf components, such as CA3080 analog IC, capacitors, and resistors. It is found that the outcome of the physical experiment is in accordance with theoretical and numerical analyses. Further, the proposed meminductor emulator exhibits less hardware complexity, less power consumption, and higher operating frequency. Its area utilization, power consumption, and maximum operating frequency are 2350.67 μm^2, 3.3 mW, and 20 MHz, respectively. Since this emulator is made up of MOS transistors only, it can be easily fabricated on silicon at the desired technology node. The applicability and effectiveness of the proposed emulator are evaluated by implementing a chaotic oscillator employing the proposed meminductor as a nonlinear element. Its easy integration with other circuit elements makes it suitable candidate for a wide range of applications.

6

Memcapacitor Emulator

Contents

Objective:

Design and analysis of an optimized memcapacitor emulator exhibiting minimal area utilization, consumes less power, capable of operating at higher frequency range and suitable for monolithic IC fabrication.

6.1 Introduction

The memcapacitor is the relation between two constitutive variables the time integral of the charge ($\sigma(t) = \int_{-\infty}^{t} q(t)$) and the flux ($\varphi(t)$) [4]. The generalized mathematical model of the charge-controlled memcapacitor is defined below.

$$C^{-1}(q) = \frac{V_{in}}{q(t)} = (\alpha + \beta\sigma(t)) \tag{6.1}$$

where $C^{-1}(q)$ is the inverse memcapacitance, and α and β are the constants.

As mentioned above, the memcapacitor can be used for several high-performance applications. Hence, there is a need of memcapacitors operating at a high frequency essential for designing these applications. This motivated us to propose a memcapacitor emulator using a minimal number of active and passive elements, making it suitable for monolithic IC fabrication with minimal area utilization, power consumption, and the capability to operate it at a high frequency than the other emulators for wider applicability. We have proposed two memcapacitor emulators, which are as follows

(i) Memcapacitor using VDTA and OTA [140]

(ii) Memcapacitor using two OTAs [141]

The rest of the chapter is delineated as follows. Section 6.2 describes an analytical model, numerical analysis, and experimental validation of the proposed memcapacitor emulator using VDTA and OTA. Section 6.3 elucidates the proposed memcapacitor emulator using two OTAs. Section 6.4 discusses the numerical and experimental analysis of the memcapacitor using two OTAs. The application of the proposed memcapacitor emulator is depicted in section 6.5. Finally, section 6.6 concludes this chapter by highlighting its efficacy among various contemporary memcapacitor emulators.

6.2 Proposed memcapacitor emulator using VDTA and OTA

The proposed emulator consists of three functional blocks: Functional block-1, Functional block-2, and Functional block-3. These functional blocks are connected to obtain the desired characteristic of the memcapacitor between input voltage, V_{in}, and charge, $q(t)$.

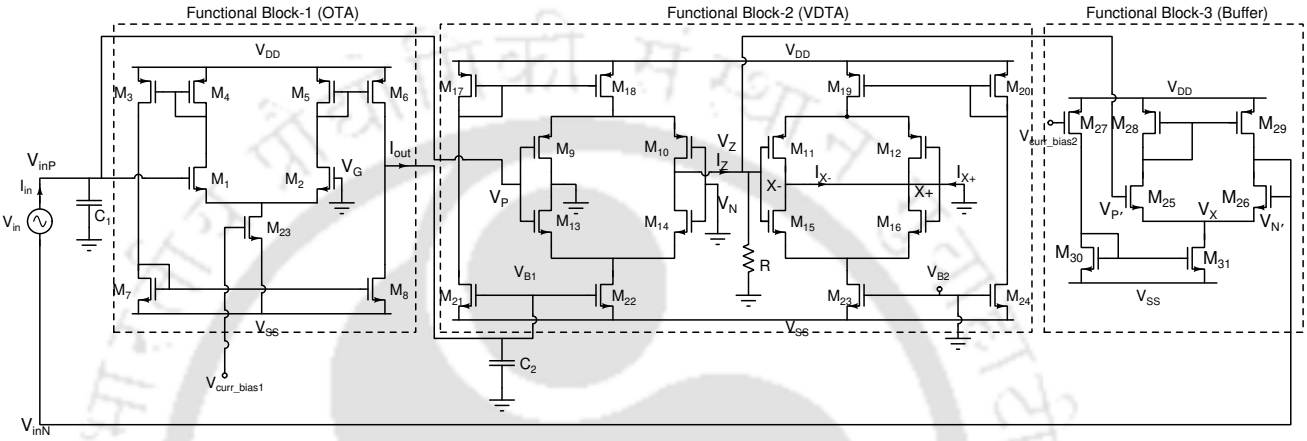


Figure 6.1: Schematic of the proposed MOSFET based memcapacitor

Fig. 6.1 represents the complete design of the proposed memcapacitor emulator. The body terminals of all the PMOS and NMOS transistors are connected to V_{DD} and V_{SS}, respectively. The working principle of the proposed emulator is analyzed in detail as follows.

Functional block-1 represents an OTA (operational transconductance amplifier), to which the positive terminal of an input signal V_{in} is connected. It is to mention that the positive and negative terminals of V_{in} are denoted as V_{inP} and V_{inN}, respectively. Transistors M_1 and M_2 form an input differential pair and are biased through a current sink transistor M_{23} as shown in Fig. 6.1. This functional block converts the differential voltage to an equivalent current, I_{out}, at its output terminal, which is depicted below.

$$I_{out} = g_{m1}(V_{inP} - V_G) = g_{m1}V_{inP} \tag{6.2}$$

where g_{m1} is the transconductance of Functional Block-1. Note that V_G is connected to the ground shown in Fig. 6.1.

Functional block-2 acts as a voltage difference transconductance amplifier (VDTA) [133]. The input-output relationship of VDTA shown in Fig. 6.1 can be stated using the following mathematical

expressions.

$$\begin{bmatrix} I_Z \\ I_{X+} \\ I_{X-} \end{bmatrix} = \begin{bmatrix} g_{m2} & -g_{m2} & 0 \\ 0 & 0 & g_{m3} \\ 0 & 0 & -g_{m3} \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \end{bmatrix} \tag{6.3}$$

where g_{m2} and g_{m3} are the transconductances of the first and second stages of VDTA, respectively. The differential inputs, V_P and V_P, are applied between P and N shown in Fig. 6.1. The voltage V_Z and current I_Z are the input to the second stage of VDTA, which cause I_{X+} and I_{X-} to flow through $X+$ and $X-$, respectively. Using Eq. 6.3, the following expressions are obtained.

$$I_Z = g_{m2}(V_P - V_N) \; ; \; I_{X\pm} = \pm g_{m3} V_Z \tag{6.4}$$

The transconductances g_{m2} and g_{m3} in terms of the transconductances of individual transistors are stated below.

$$g_{m2} = \frac{g_9 g_{10}}{g_9 + g_{10}} + \frac{g_{13} g_{14}}{g_{13} + g_{14}} \; ; \; g_{m3} = \frac{g_{11} g_{12}}{g_{11} + g_{12}} + \frac{g_{15} g_{16}}{g_{15} + g_{16}} \tag{6.5}$$

where $g_x = \sqrt{2 k_x I_x}$ is the transconductance of the x^{th} transistor. Here, k_x and I_x are the process constant and current of the x^{th} transistor. Further, due to the symmetry existing between all the PMOS and NMOS transistors of the VDTA depicted in Table 6.1, Eq. 6.5 can be simplified as mentioned below.

Table 6.1: Transistor sizing of the proposed emulator

$Transistors$	$W/L\left(\frac{\mu m}{\mu m}\right)$
$M_1 - M_8, M_{27} - M_{29}, M_{23}, M_{25}, M_{26}$	$\frac{4}{2}$
$M_{17} - M_{20}, M_9 - M_{12}$	$\frac{13}{0.36}$
$M_{13} - M_{16}, M_{21} - M_{24}$	$\frac{4}{0.36}$
$M_{30} - M_{31}$	$\frac{8}{2}$

$$g_{m2} = \sqrt{2}\left[\frac{\sqrt{k_{10} I_{10}} + \sqrt{k_{13} I_{13}}}{2}\right] ; g_{m3} = \sqrt{2}\left[\frac{\sqrt{k_{12} I_{12}} + \sqrt{k_{15} I_{15}}}{2}\right] \tag{6.6}$$

Due to the symmetry, the currents flowing through the circuit can be represented as follows.

$$I_{10} = I_{13} = \frac{I_{22}}{2}; I_{12} = I_{15} = \frac{I_{23}}{2} \tag{6.7}$$

Using Eqs. 6.6 and 6.7, g_{m2} and g_{m3} can be formulated below.

$$g_{m2} = K_{M2}\left[V_{B1} - V_{SS} - V_{th}\right]; g_{m3} = K_{M3}\left[V_{B2} - V_{SS} - V_{th}\right] \tag{6.8}$$

where $K_{M2} = \sqrt{\frac{k_{22}}{2}}\left[\frac{\sqrt{k_{10}}+\sqrt{k_{13}}}{2}\right]$ and $K_{M3} = \sqrt{\frac{k_{23}}{2}}\left[\frac{\sqrt{k_{12}}+\sqrt{k_{15}}}{2}\right]$ are the process constants. Here, V_{B1} and V_{B2} are the biasing voltages of the first and second stages of VDTA. Note that V_{th} is the threshold voltage of a transistor.

Functional block-3 acts as a buffer, where input is applied to the gate of transistor M_{25}. The gate of M_{26} is connected to its drain terminal for configuring the negative feedback, as shown in Fig. 6.1. The analytical model of Functional Block-3 is given below.

$$I_{25} = g_{25}(V_{P'} - V_X) = g_{26}(V_{N'} - V_X) \tag{6.9}$$

Since, $g_{25} = g_{26}$, therefore, $V_{P'} = V_{N'}$. Thus, it can be stated that $V_{N'}$ at the output terminal follows the input $V_{P'}$, which is desired for the reliable operation of the proposed emulator.

Memcapacitor behavior is realized by analyzing the functional blocks exhibited in Fig. 6.1. A sinusoidal input is applied to the proposed emulator between V_{inP} and V_{inN}, as depicted below.

$$V_{in} = V_{inP} - V_{inN} \tag{6.10}$$

Here, $V_{inP} = \frac{I_{out}}{g_{m1}}$, and is described using following mathematical expression.

$$V_{inP} = \frac{1}{C_1}\int_{-\infty}^{t} I_{in}\, dt = \frac{q(t)}{C_1} \tag{6.11}$$

The output current of OTA, $I_{out} = g_{m1}\frac{q(t)}{C_1}$. The output terminal of OTA is connected to V_{B1} of VDTA, which is the voltage across C_2 and can be expressed as,

$$V_{B1} = -\frac{1}{C_2}\int_{-\infty}^{t} g_{m1}V_{inP}\, dt = -\frac{g_{m1}}{C_1C_2}\sigma(t) \tag{6.12}$$

where $\sigma(t) = \int_{-\infty}^{t} q(t)$ is the time integral of the charge (TIC).

It can be seen that varying C_2 changes V_{B1} due to the variation in the charge. The V_{B1} can be termed as charge-controlled voltage. It can be seen in Fig. 6.1 that V_P of VDTA and V_{inP} of OTA are

connected together; thus, the current, $I_Z = g_{m2}V_P = \frac{g_{m2}q(t)}{C_1}$ at terminal Z. Further, V_Z across resistor R connected at terminal Z of VDTA and it is fed as an input to the buffer. Note that $V_{P'} = V_Z$. According to Eq. 6.9, $V_{N'} = V_{P'}$. It can be seen in Fig. 6.1, $V_{inN} = V_{N'}$, therefore, it can be stated that

$$V_{inN} = V_{N'} = V_{P'} = V_Z = \frac{g_{m2}q(t)}{C_1}R \tag{6.13}$$

Using Eqs. 6.11 and 6.13, Eq. 6.10 can be formulated to obtain the analytical model of the proposed memcapacitor emulator illustrated below.

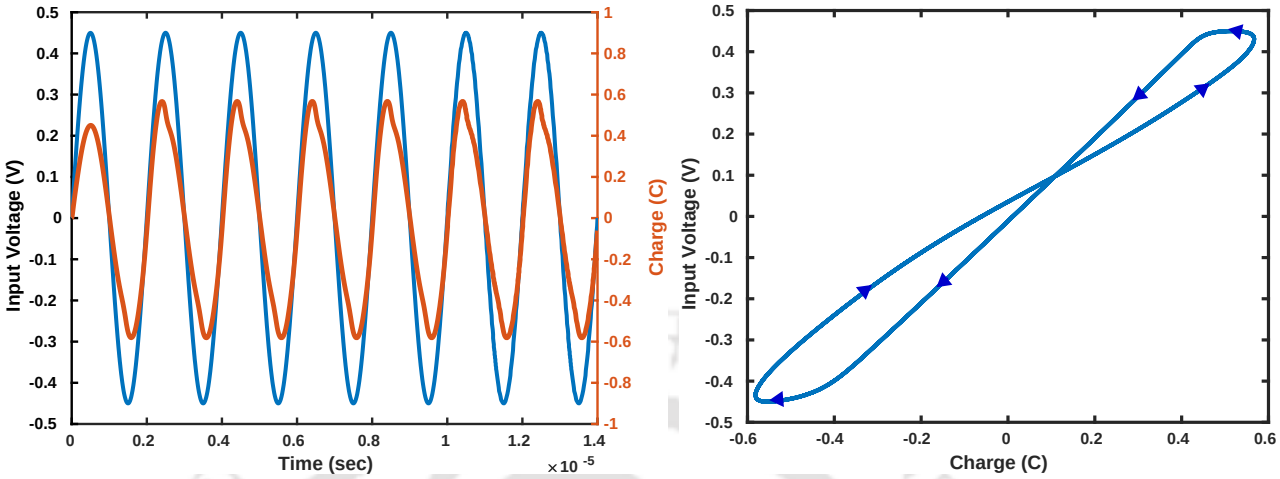
$$C^{-1}(q(t)) = \frac{V_{in}}{q(t)} = \frac{1}{C_1}\left[1 + \left(\frac{RK_{M2}g_{m1}}{C_1C_2}\sigma(t)\right) + \{(V_{SS} + V_{th})RK_{M2}\}\right] \tag{6.14}$$

Eq. 6.14 represents memcapacitance between charge, $q(t)$, and input voltage, V_{in}, and it satisfies Eq. 6.1.

6.2.1 Performance analysis of the proposed memcapacitor emulator

The numerical analysis of the proposed memcapacitor emulator is performed using *Cadence Virtuoso* with *TSMC* 180 *nm* PDKs. Aspect ratios of the MOS transistors employed for the designing of the proposed emulator are depicted in Table 6.1.

A dual power supply having $V_{DD} = 900\ mV$ and $V_{SS} = -900\ mV$ is applied to the emulator. Note that the proposed emulator is of a floating type and enables input to be connected between its terminals without any restrictions. A sinusoidal signal of 500 kHz and 450 mV amplitude is applied between V_{inP} and V_{inN} of the proposed emulator to obtain its transient response and $V_{in} - q$ characteristic (PHL), as shown in Fig. 6.2(a) and 6.2(b). It can be observed that the charge and applied voltage are proportional to each other, which verifies a vital property of the memcapacitor. The current bias voltages employed in the proposed design are $V_{curr\_bias1} = -150\ mV$ for the OTA and $V_{curr\_bias2} = -50\ mV$ for the buffer. The proposed emulator utilizes two capacitors, $C_1 = 0.5\ pF$ and $C_2 = 10\ pF$, and one resistor, $R = 1.3\ K\Omega$, for its realization.



(a) (b)

Figure 6.2: (a) Transient analysis and (b) $V_{in} - q$ characteristic (PHL) of the proposed memcapacitor

6.2.2 Numerical analysis

The proposed memcapacitor emulator is applied with input at different frequencies, as shown in Fig. 6.3(a). It can be observed that the lobe area of the PHL decreases with an increase in the frequency, verifying the frequency behavior of the proposed emulator. The maximum operating frequency of the proposed emulator is estimated to be 1.2 MHz.

The stability of the proposed emulator is evaluated at different temperatures and process corners. The response of the memcapacitor at different temperatures is showcased in Fig. 6.3(b). It can be observed that the lobe area of the PHL decreases with increasing temperature. Its reliability is verified at different process corners, such as NN (Nominal NMOS and Nominal PMOS), FF (fast NMOS and fast PMOS), SS (slow NMOS and slow PMOS), SF (slow NMOS and fast PMOS), and FS (fast NMOS and slow PMOS), as depicted in Fig. 6.3(c). It can be seen that the lobe area of PHL reaches maximum/minimum at FF/SS, respectively, whereas the optimal lobe area is obtained at NN. It is to mention that the proposed emulator exhibits stable behavior except for slight deviations due to temperature and process corners. The Monte Carlo analysis is performed for 100 runs to analyze the effect of variations in the process parameters and the mismatch between transistors of the proposed emulator, as shown in Fig. 6.3(d). It can be observed that there is a deviation in the $V_{in} - q$ characteristic of the proposed emulator due to the variations in the process parameters and device mismatch. These deviations do not affect the memcapacitive behaviour of the proposed

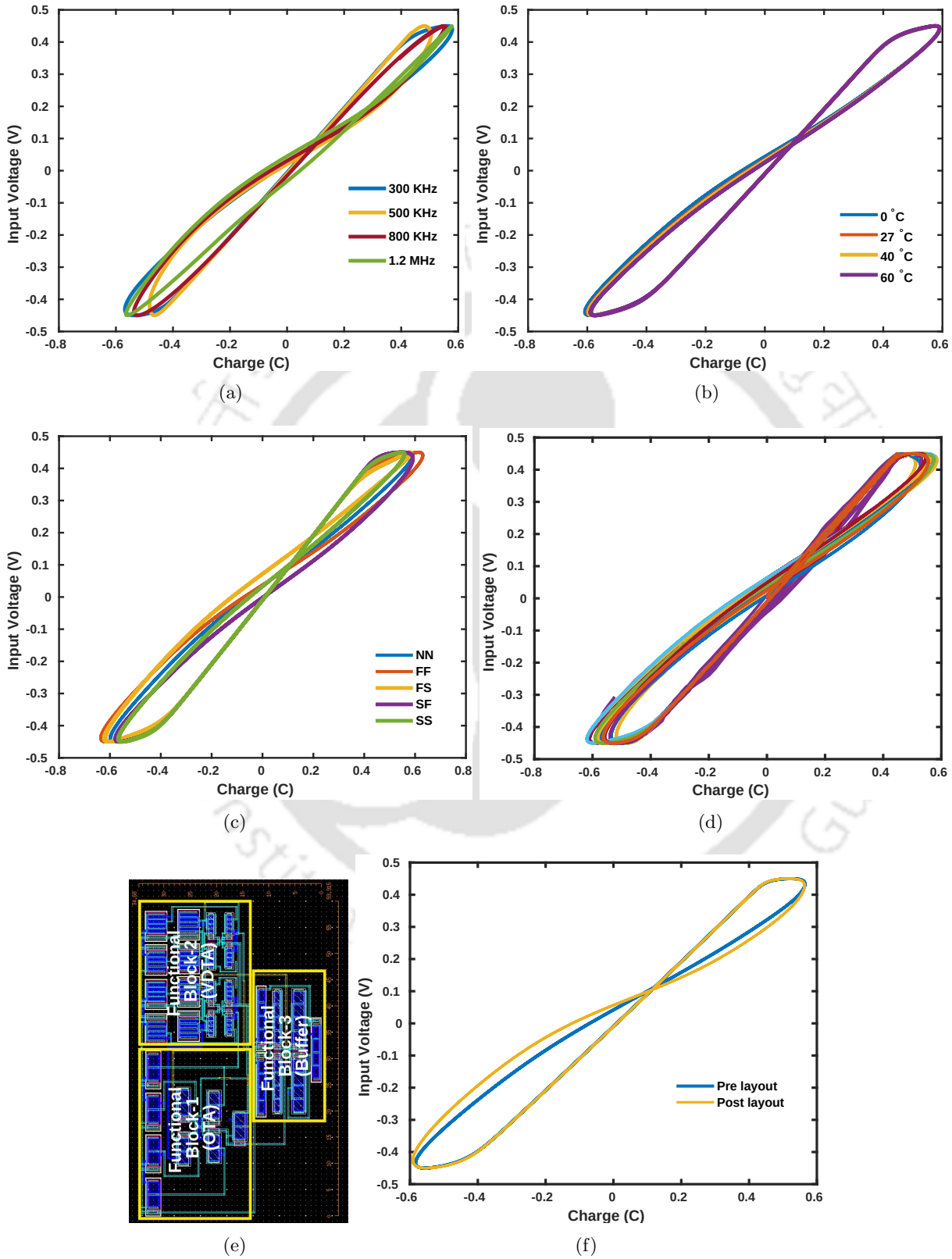


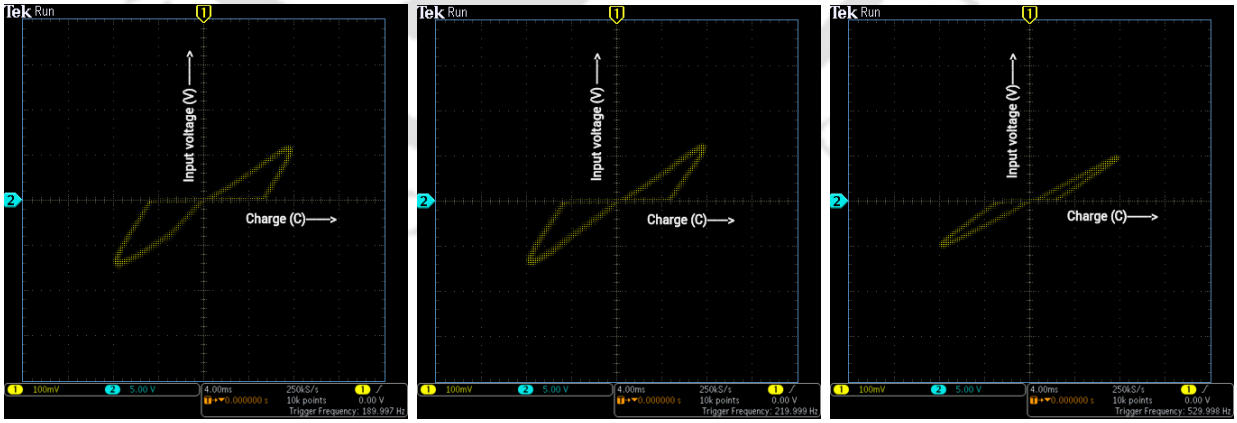
Figure 6.3: (a) PHLs at different frequencies (b) PHLs at different temperatures (c) PHLs at different process corners (d) Monte Carlo analysis (e) Layout and (f) Pre- and post-layout results of the proposed memcapacitor

emulator because its $V_{in} - q$ characteristic is retained, as showcased in Fig. 6.3(d). This validates the reliability of the proposed emulator and paves the way for it to be used efficiently in realizing various applications.

The layout of the proposed memcapacitor emulator is designed using *Cadence Virtuoso* with $TSMC$ 180 nm PDKs, as shown in Fig. 6.3(e). Later, its pre- and post-layout validation are performed, as illustrated in Fig. 6.3(f). It can be seen that the post-layout PHL slightly deviates compared to the pre-layout PHL due to the presence of parasitic elements [142]. The area utilization and power consumption of the proposed memcapacitor are 2077.85 μm^2 (59.915 μm X 34.68 μm) and 2.726 mW, respectively.

6.2.3 Experimental analysis

The physical model of the proposed emulator is implemented using $CA3080$ (OTA), $LM741$ (Opamp), and other passive elements. An Aplab DC power supply of ± 15 V is applied to the circuit, and an input sinusoidal signal of 300 mV is generated employing Rigol DG1022 function generator. The buffer circuit in the proposed emulator is realized using $LM741$. All the components are connected in accordance with the circuit diagram depicted in Fig. 6.1. The passive components utilized in the realization of the memcapacitor are $C_1 = 1$ pF, $C_2 = 1.5$ nF, and $R = 560$ Ω. While performing the experiment, the output is visualized using the MDO3012 Mixed Domain Oscilloscope. The response of



(a) (b) (c)

Figure 6.4: PHLs of the experiment at (a) 190 Hz (b) 220 Hz, and (c) 530 Hz

the physically implemented memcapacitor emulator at different input frequencies is exhibited in Figs. 6.4(a), 6.4(b), and 6.4(c). It can be seen that the behavior of the physical implementation is similar

Table 6.2: Comparative analysis of memcapacitor emulators

Author	Year	Ref.	Active components	Passive components	No. of transistors	Max. operating freq.
Dong et al.	2014	[63]	4-CCII, 1-AM, 2-Opamps	8-R, 2-C	-	15 Hz
Yu et al.	2013	[62]	4-CCII, 1-AM, 2-Opamps	9-R, 2-C	-	86.6 Hz
Abdullah et al.	2020	[66]	1-CCII, 1-OTA, 1- AM	3-C	-	2 kHz
Dongsheng et al.	2019	[143]	4-CCII, 1-varactor diode, 1-Opamp	6-R, 2-C	-	8 kHz
Sharma et al.	2020	[67]	2-CCII, 1-AM	2-R, 2-C	-	25 kHz
Zheng et al.	2019	[60]	4-CCII, 1-varactor diode	2-R, 2-C	> 40	180 kHz
Raj et al.	2021	[144]	2-CCII, 1-OTA	2-R, 2-C	> 40	700 kHz
Ananda et al.	**2023**	**This work**	**1-VDTA, 1-OTA, 1-buffer**	1-R, 2-C	**31**	**1.2 MHz**

to the numerical analysis of the proposed memcapacitor, and the lobe area of its PHL decreases with an increase in frequency.

Further, an additional Opamp is used as a buffer for connecting the output of the Functional Block-1 (OTA) to the Functional Block-2 for eliminating loading effects and maintaining the voltage V_{B1} for the reliable performance of the proposed memcapacitor. As we know, the Opamp has a DC-level shifter, due to which there is a shift of the crossing point of hysteresis curves in the experimentally emulated results compared to the simulated results. The comparison of the proposed emulator with other emulators is shown in Table 6.2. The operating frequency of the emulators [62, 63, 66, 67] is less due to the use of a multiplier, which reduces the characteristic of an emulator to 1/10 of the actual response [145] and decreases the lobe area of a PHL. Thus, the PHL becomes a straight line at high frequencies, losing the memcapacitive behaviour. Further, emulators depicted in [60, 143] are not independent memcapacitor emulators, but universal circuits are utilized to realize memelements by interchanging their components. The operating frequency of these emulators is also less due to minimal flexibility in the component selection for their high frequency operations. However, the emulator presented in [144] operates at 700 kHz, which is close to the operating frequency of the proposed emulator, but it requires many active and passive components. The fewer transistors used

by our proposed emulator and one less resistor as compared to [144] enable its operating frequency to be higher than all the contemporary emulators.

The proposed memcapacitor [140] is further optimized with respect to area and power and also replaces active MOS capacitors in place of passive capacitors for increasing the operating frequency, which aids in employing the proposed memcapacitor for broader utility in designing practical applications. Its details are discussed in the following section.

6.3 Proposed memcapacitor emulator design using two OTAs

The memcapacitor is constituted by a relation between the flux (φ) and the time integral of the charge (σ) [146]. An n^{th} order charge-controlled memcapacitor was hypothesized by Di Ventra et al. [4] as follows.

$$V_{in} = C^{-1}(x, q, t)\ q(t),\ \ \dot{x} = f(x, q, t) \tag{6.15}$$

where x is an internal state variable, the $q(t)$ and V_{in} are the charge and the input voltage of the memcapacitor, and C^{-1} is the inverse memcapacitance. Since in Eq. 6.15, C^{-1} is a function of the charge $q(t)$, it is stated as a charge-controlled memcapacitor. The mathematical model that emulates the behaviour of the charge-controlled memcapacitor [65, 69] is mentioned below.

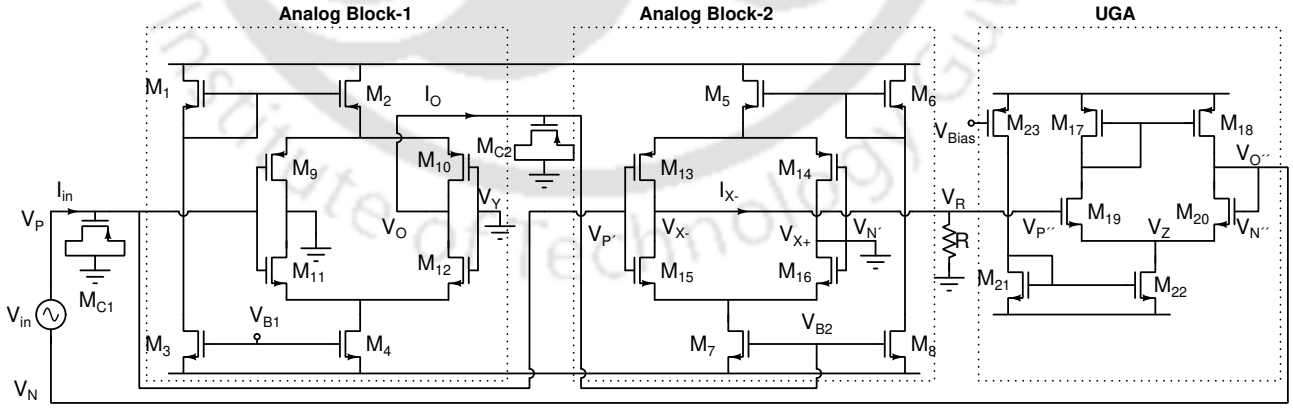


Figure 6.5: Schematic of the proposed MOS-based memcapacitor emulator

$$\begin{aligned} g_{m1} &= \frac{g_{10} + g_{11}}{2} \\ g_{m2} &= \frac{g_{14} + g_{15}}{2} \end{aligned} \tag{6.16}$$

$$C^{-1}[q(t)] = \frac{V_{in}}{q(t)} = \left[\alpha + \beta \int_0^t q(\tau)\, d\tau\right] \tag{6.17}$$

where α and β are the constants, $\sigma(t) = \int_0^t q(\tau)\, d\tau$ is the time integral of the charge (TIC).

The active analog blocks are utilized to realize the memcapacitive behaviour as shown in Eq. 6.17. The proposed memcapacitor emulator consists of three active blocks, viz. (a) Analog block-1, (b) Analog block-2, and (c) UGA (unity gain amplifier) along with a resistor, as shown in Fig. 6.5. The transconductance stages (Analog blocks 1 and 2) convert the voltage into its current equivalent, and with the help of MOS-capacitor integration is performed realizing memcapacitive behaviour. By utilizing bias terminals of the transconductance stages, multiplication operation is performed internally without an extra analog multiplier, reducing circuit complexity and lowering output voltage degradation. Further, the body terminals of all the PMOS and NMOS transistors are connected to V_{DD} and V_{SS}, respectively. The analog blocks, as mentioned earlier, have transconductances, g_{m1} and g_{m2}, and their mathematical formulations are described below.

$$\begin{aligned} g_{m1} &= \frac{g_9 g_{10}}{g_9 + g_{10}} + \frac{g_{11} g_{12}}{g_{11} + g_{12}} \\ g_{m2} &= \frac{g_{13} g_{14}}{g_{13} + g_{14}} + \frac{g_{15} g_{16}}{g_{15} + g_{16}} \end{aligned} \tag{6.18}$$

where $g_9 - g_{16}$, are transconductances of MOSFETs $M_9 - M_{16}$, respectively.

g_n denotes the transconductance of the n^{th} transistor and can be represented by the following equation.

$$g_n = \sqrt{2 k_n I_n} \tag{6.19}$$

where k_n represents the transistor process constant and I_n is the current of n^{th} transistor. The sizes of all the transistors depicted in Fig. 6.5 are mentioned in Table 6.1. Transconductances of NMOS and PMOS transistors of the proposed memcapacitor are chosen to be identical, which helps Eq. 6.18 to be simplified as follows.

Substituting Eq. 6.19 into Eq. 6.16, the following mathematical equation is obtained.

$$g_{m1} = \sqrt{2}\left[\frac{\sqrt{k_{10}I_{10}} + \sqrt{k_{11}I_{11}}}{2}\right]$$
$$g_{m2} = \sqrt{2}\left[\frac{\sqrt{k_{14}I_{14}} + \sqrt{k_{15}I_{15}}}{2}\right] \tag{6.20}$$

The current through transistors, I_{10} and I_{14}, are mentioned as follows.

$$I_{10} = I_{11} = \frac{I_4}{2}; I_{14} = I_{15} = \frac{I_7}{2} \tag{6.21}$$

Using Eq. 6.21, Eq. 6.20 can be rewritten as,

$$g_{m1} = \left[\frac{\sqrt{k_{10}} + \sqrt{k_{11}}}{2}\right]\sqrt{\frac{k_4}{2}\left[V_{B1} - V_{SS} - V_{th}\right]^2}$$
$$g_{m2} = \left[\frac{\sqrt{k_{14}} + \sqrt{k_{15}}}{2}\right]\sqrt{\frac{k_7}{2}\left[V_{B2} - V_{SS} - V_{th}\right]^2} \tag{6.22}$$

Here $M4$ and $M7$ are configured as the current source. Therefore, they are working in the above-threshold saturation region.

Eq. 6.22 is further simplified as mentioned below.

$$g_{m1} = K_{M1}\left[V_{B1} - V_{SS} - V_{th}\right]$$
$$g_{m2} = K_{M2}\left[V_{B2} - V_{SS} - V_{th}\right] \tag{6.23}$$

where K_{M1} and K_{M2} are the transistors' process constants.

The proposed emulator consists of two MOS-capacitors, which are designed by shorting source, drain, and body terminals of PMOS transistors. All three blocks consist of dual input terminals, viz. positive (V_P, V_P', V_P'') and negative (V_N, V_N', V_N'') terminals and output terminals (V_O, V_{X-}, V_O''). Note that the proposed emulator characterized using active blocks consists of MOS transistors only, making it suitable for the monolithic IC design.

6.3.1 Analog Block-1 (OTA)

The analog block-1 is characterized as an OTA (operational transconductance amplifier), which converts the voltage into the current. The bias is applied to the $B1$ terminal to obtain transconductance (g_{m1}), as shown in Eq. 6.23. A differential input signal is applied between the V_P and V_N terminals, and an output current I_O flows through terminal V_O, as illustrated in Fig. 6.5. In the proposed design,

V_Y is grounded, and a sinusoidal signal is applied to (V_{in}) across C_{MC1}, such that the input current (I_{in}) flows through it. The mathematical expression of the voltage across C_{MC1} is represented below.

$$V_{MC1} = V_P = \frac{\int I_{in}\, dt}{C_{MC1}} = \frac{q(t)}{C_{MC1}} \tag{6.24}$$

where $q(t) = \int I_{in}\, dt$ is the charge stored in C_{MC1}. Here V_P is the charge equivalent of the voltage.

The output current, $I_O = V_P g_{m1}$, flows through the MOS-capacitor (M_{C2}), and the output voltage V_O can be expressed using the following mathematical expression.

$$V_O = V_{MC2} = V_{B2} = \frac{\int V_P g_{m1}\, dt}{C_{MC2}} = \frac{g_{m1} \int q(t)\, dt}{C_{MC1} C_{MC2}} \tag{6.25}$$

6.3.2 Analog Block-2 (OTA)

Analog block-2 is also realized as an OTA, and its transconductance, g_{m2}, is obtained using Eq.6.23. The input applied to analog block-1 is also applied to analog block-2 at $V_{P'}$ producing an output current, I_{X-}, which can be represented by the following equation.

$$I_{X-} = -g_{m2} V_{P'} = -g_{m2} V_P \tag{6.26}$$

The current I_{X-} flows through R generating a voltage V_R as mentioned below.

$$V_R = I_{X-} R = -g_{m2} V_P R \tag{6.27}$$

Substituting V_{B2} depicted in Eq. 6.25 in Eq. 6.23, g_{m2}, can be reformulated as,

$$g_{m2} = K_{M2} \left[\frac{g_{m1} \int q(t)\, dt}{C_{MC1} C_{MC2}} - V_{SS} - V_{th} \right] \tag{6.28}$$

6.3.3 UGA (unity gain amplifier)

This block acts as a buffer, which takes voltage as an input that appears across R (V_R), and gives output voltage, $V_{O''}$. It is to mention that $V_{N''} = V_{O''}$, and $V_{O''}$ is directly connected back to V_N, as shown in Fig. 6.5. The operation of the buffer can be analyzed using following equations.

$$\begin{gathered} g_{19}(V_{P''} - V_Z) = I_{19} = \\ g_{20}(V_{N''} - V_Z) = g_{20}(V_N - V_Z) \end{gathered} \tag{6.29}$$

which gives $g_{19} = g_{20}$ due to symmetry in the transistors. Therefore,

$$V_{P''} = V_N \tag{6.30}$$

It can be observed that output $V_{P''}$ strictly follows input V_N as depicted in Eq. 6.30.

6.3.4 Analysis of the memcapacitor behaviour

The input signal is applied to terminals V_P and $V_{P'}$ of the first and second OTA of the proposed emulator, as shown in Fig. 6.5. The voltage across M_{C1} as a function of input current (I_{in}) exhibited in Eq. 6.24 is the charge equivalent of the voltage, $V_q = V_P = V_{P'} = \frac{q(t)}{C_{MC1}}$.

The output voltage V_O in Eq. 6.31 is the time-integral of charge V_σ, which is connected to the bias terminal V_{B2} of analog block-2. Note that $V_\sigma = V_{B2}$, which is expressed below.

$$V_\sigma = V_{B2} = \frac{g_{m1}\sigma(t)}{C_{MC1}C_{MC2}} \tag{6.31}$$

where $\sigma(t) = \int q(t)\,dt$ is the time integral of charge (TIC).

Using Eqs. 6.27 and 6.28, the output voltage V_R of analog block-2 is connected to the input terminal $V_{P''}$ of UGA and can be expressed by following mathematical equation.

$$V_R = V_{P''} = V_N = -\frac{q(t)RK_{m2}}{C_{MC1}}\left[\frac{g_{m1}\sigma(t)}{C_{MC1}C_{MC2}} - V_{SS} - V_{th}\right] \tag{6.32}$$

It can be seen in Fig. 6.5, the proposed memcapacitor emulator is floating, which aids in applying V_{in} between two terminals P and N without any restriction to connect it to the ground terminal always, thus, $V_{in} = V_P - V_N$. Using Eqs. 6.24 and 6.32, V_{in} can be modelled using following equation.

$$V_{in} = \frac{q(t)}{C_{MC1}}\left[1 + K_{M2}R\left(\frac{g_{m1}\sigma(t)}{C_{MC1}C_{MC2}} - V_{SS} - V_{th}\right)\right] \tag{6.33}$$

Using Eq. 6.33, the analytical model of the proposed memcapacitor emulator is characterized below.

$$C^{-1}[q(t)] = \frac{V_{in}}{q(t)} = \underbrace{\frac{1}{C_{MC1}}\left[1 - K_{M2}RV_{SS} - K_{M2}RV_{th}\right]}_{\text{time-invariant}} + \underbrace{\frac{1}{C_{MC1}}\left[\frac{RK_{M2}g_{m1}\sigma(t)}{C_{MC1}C_{MC2}}\right]}_{\text{time-variant}} \tag{6.34}$$

Here, $\alpha = \frac{1}{C_{MC1}}\left[1 - K_{M2}RV_{SS} - K_{M2}RV_{th}\right]$ and $\beta = \frac{1}{C_{MC1}}\left[\frac{RK_{M2}g_{m1}}{C_{MC1}C_{MC2}}\right]$. It can be seen that this model is similar to the ideal model stated in Eq. 6.17. The memcapacitance of the proposed emulator has a dependency on $\sigma(t)$, as shown in Eq. 6.34, which is time-variant and depends on the past behaviour of the memcapacitor. The memcapacitance is also calculated using the numerical simulations of the proposed emulator. The forward and backward path memcapacitances of the proposed memcapacitor estimated analytically using directly extracted parameters from TSMC 180 nm PDKs are 2.87 pF and 2.66 pF pF at 18 MHz; whereas the forward and backward path memcapacitances of the proposed memcapacitor calculated through numerical simulations are 0.86 pF and 0.77 pF at 18 MHz. The difference between the memcapacitances obtained analytically and numerically is due to the presence of parasitic elements. Therefore, to establish the accuracy of the proposed emulator, the essential characteristics of the memcapacitor derived from its mathematical model stated in Eq. 6.34 are also validated through numerical simulation, which is explained in Section 6.4. These characteristics are mentioned below for completeness.

- The $V_{in} - q$ characteristic exhibits zero crossing pinched hysteresis loop (PHL) for a bipolar periodic signal.
- Memcapacitor depends on the nonlinear function of charge ($q(t)$), which is realized by employing TIC ($\sigma(t)$).
- It consists of time-variant and time-invariant components.
- The transconductance g_{m1} is a tunable parameter used to obtain desired characteristics of a memcapacitor.
- Its behaviour depends on the input signal frequency due to the presence of the time integral of the charge.

- The lobe area of the PHL decreases when the input signal frequency increases because the memcapacitance is inversely proportional to the $\sigma(t)$ (TIC), which is a function of the frequency.

Note that the characteristics of the analytical model of the proposed emulator stated above are verified through numerical analysis, validating its correctness and accuracy as per the expectations. A detailed description of the performance analysis and experimental validation of the proposed memcapacitor emulator is provided in the following section.

6.4 Performance analysis of the proposed memcapacitor

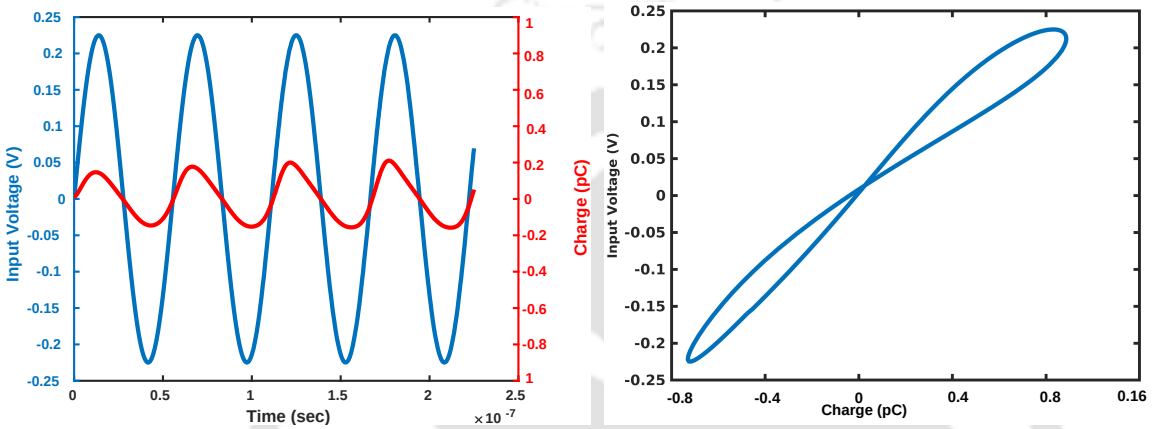
Numerical and experimental analyses of the proposed memcapacitor emulator are conducted to validate its correctness and reliability. Numerical analysis is performed using *Cadence Virtuoso* environment and $TSMC$ 180 nm $PDKs$ to verify its characteristics with respect to various parameters. Aspect ratios of MOS transistors utilized in the proposed emulator are mentioned in Table 6.3.

Table 6.3: Transistor sizes

$Transistors$	$W/L\left(\frac{\mu m}{\mu m}\right)$
$M_1, M_2, M_5, M_6, M_9, M_{10}, M_{13}, M_{14}$	$\frac{13}{0.36}$
$M_3, M_4, M_7, M_8, M_{11}, M_{12}, M_{15}, M_{16}$	$\frac{4}{0.36}$
$M_{17} - M_{20}, M_{23}$	$\frac{4}{2}$
M_{21}, M_{22}	$\frac{8}{2}$
M_{C1}	$\frac{100}{1.5}$
M_{C2}	$\frac{80}{1.5}$

A dual power supply is applied to the memcapacitor with $V_{DD} = 900\ mV$ and $V_{SS} = -900\ mV$. Note that $V_{B1} = 100\ mV$ and $V_{Bias} = -138\ mV$ are applied to analog block-1 and UGA of the proposed emulator for biasing. Fig. 6.6 showcases the transient and $V_{in} - q$ characteristics (PHL) of the proposed emulator, which is obtained by applying a sinusoidal signal of 225 mV amplitude and 20 MHz to the emulator. The proposed emulator exhibit that the charge $q(t)$ is zero whenever the input voltage V_{in} is zero, as shown in Fig. 6.6(a). The $V_{in} - q$ characteristic is pinched at the origin, providing PHL, which satisfies one of the fingerprints of the memcapacitor [60–63, 66, 67, 143, 144], as depicted in Fig. 6.6(b). Note that the charge, $q(t)$, is measured across the M_{C1} at the P terminal of the proposed emulator. The proposed memcapacitor emulator consists of two MOS capacitors (M_{C1} and M_{C2}), which are realized using PMOS transistors by shorting their drain, source, and body terminals.

The aspect ratios of these MOS capacitors are shown in Table 6.3 and the corresponding values of the capacitances are $C_{MC1} = 4\ pF$ and $C_{MC2} = 3\ pF$, respectively. Since the capacitors used in the proposed emulator is in the range of pF, the unit of the charge is in pC, which is determined using Eq. 6.24. Therefore, the charge $q(t)$ shown in the $V_{in} - q$ characteristics of the proposed emulator is in pC.



(a) (b)

Figure 6.6: Proposed memcapacitor at 225 mV and 20 MHz (a) Transient analysis and (b) $V_{in} - q$ characteristics (PHL)

6.4.1 Parametric analysis

The characteristics of the proposed emulator is analyzed at different operating frequencies with nominal temperature (27 C), as shown in Figs. 6.7(a) and 6.7(b). It can be observed that the lobe area of the PHL decreases when frequency increases, which verifies the frequency dependent behaviour of the proposed emulator. Further, the values of the capacitance during the forward path and backward path are 1.0688 pF and 0.7828 pF at 12 MHz, and 0.7972 pF and 0.7664 pF at 24 MHz, respectively. It can be observed that the value of the memcapacitance decreases with increasing frequency. Thus, it can be seen that the key features of the analytical model of the proposed emulator stated above are verified through numerical analysis, validating its correctness and accuracy. Note that the maximum operating frequency of the proposed emulator is 24 MHz.

The robustness and reliable behaviour of the proposed emulator are verified at different temperatures and process corners. As we know, MOSFET is a transconductance device that generates current by varying input voltage. At a high temperature, the current is reduced due to an increase in the collision of the charged carriers excited by the thermal energy. This causes an increase or decrease

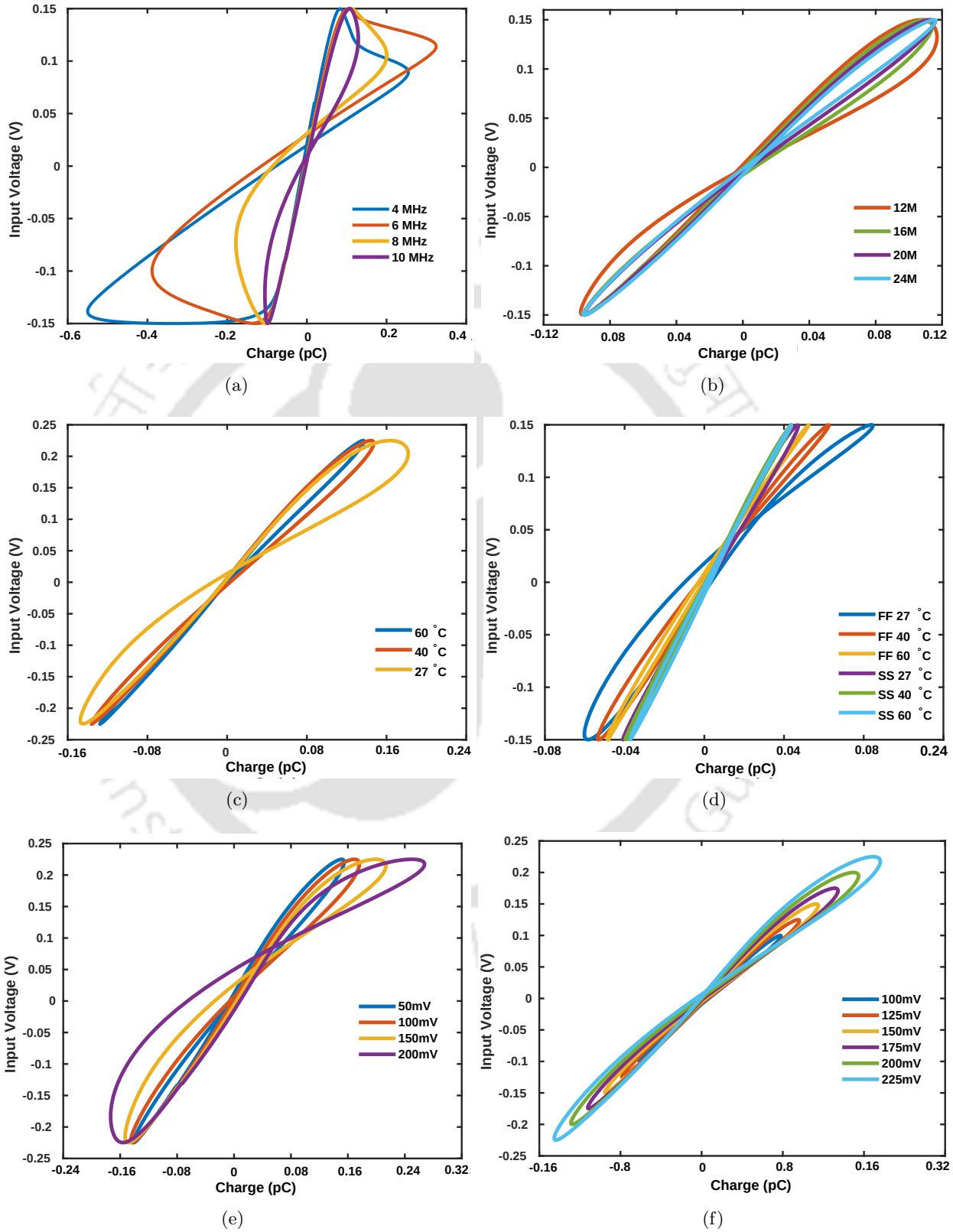


Figure 6.7: Numerical analysis at different (a) Low frequencies (b) High frequencies (c) Temperatures (d) Process corners (e) Bias voltages and (f) Input voltages

in the lobe area of PHL, as depicted in Fig. 6.7(c). The stability of the proposed emulator is also validated at different process corners, which include FF (fast NMOS and fast PMOS) and SS (slow NMOS and slow PMOS). It can be observed in Fig. 6.7(d), the lobe area increases for FF as the current flowing through the circuit is maximum, and the current reduces for SS, which decreases the lobe area of the PHL. Hence, the proposed emulator exhibits acceptable characteristics except for the slight deviation caused by the parameter variations at different process corners. This is due to the dependency of process parameters on the temperature mainly. Here, the temperature is one of the parameters that varied during this study, along with other process parameters.

Further, the characteristics of the proposed emulator is evaluated at different input and bias (V_{B1}) voltages, as illustrated in Figs. 6.7(e) and 6.7(f), respectively. It can be seen that the lobe area of the PHL increases due to the increase in the current flowing through the circuit when input and bias voltages are varied. It can also be seen that at different input and bias voltages, PHL shifts and is not pinched at the origin. This is due to the sizing and placement of the transistors while realizing it on the silicon. Therefore, for using a memcapacitor in a practical application, it is imperative to choose a suitable input voltage range and bias conditions for stable behaviour. Also, an optimal layout would aid in reducing the drift of PHLs. Note that the input frequency of 20 MHz is applied for these analyses shown in Figs. 6.7(c), 6.7(d), 6.7(e) and 6.7(f), respectively.

6.4.2 Post and pre-layout analysis

The proposed emulator is further validated by performing post layout analysis using $Cadence\ Virtuoso$ environment and $TSMC$ 180 nm $PDKs$ as shown in Fig. 6.8. Using the physical layout as depicted in Fig. 6.8(a), the total area utilization of the proposed emulator is 2034.65 μm^2(47.055 $\mu m \times 43.24\ \mu m$). The total power consumption of the proposed emulator is 1.86 mW measured at 16 MHz, which includes both dynamic and leakage power. The power consumption of the proposed emulator varies with respect to the variation in the input signal frequency, as shown in Table 6.4, and the average power consumption of the proposed emulator is 1.94 mW. It can be seen that power consumption decreases with an increase in frequency due to the reduction in the lobe area of the PHL. Its correctness is corroborated by simulating the circuit obtained after its synthesis in the post layout analysis of the proposed memcapacitor illustrated in Fig. 6.8(b). Note that deviation in the lobe area of post layout PHL as compared to pre layout PHL is due to the presence of parasitic elements. The post-layout design is verified at different temperatures, the lobe area of the PHL decreases with increasing temper-

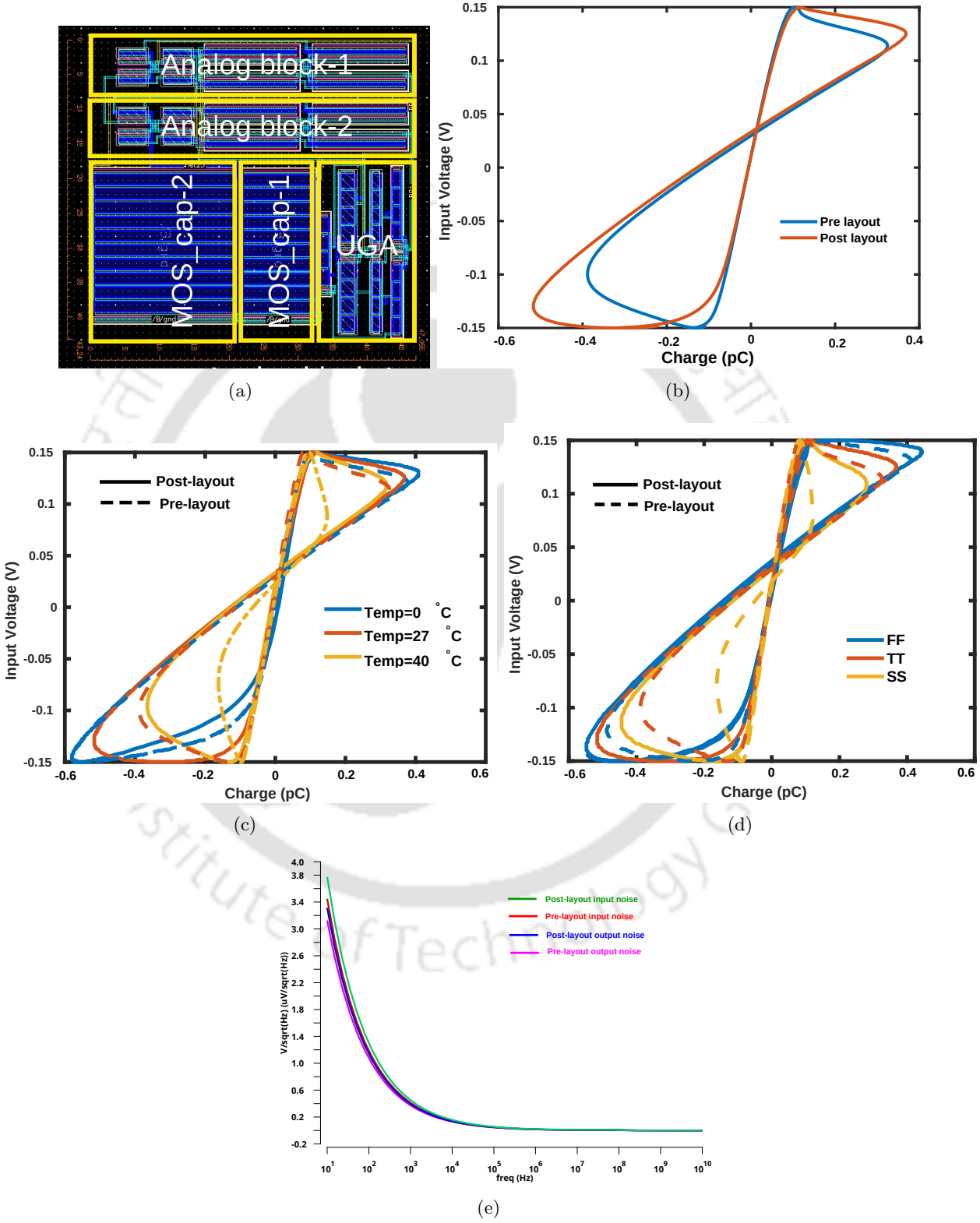


Figure 6.8: Post-layout analysis of the proposed emulator (a) Physical layout (b) Pre and Post-layout PHLs (c) PHLs at different temperature (d) PHLs at different process corners and (e) Noise analysis

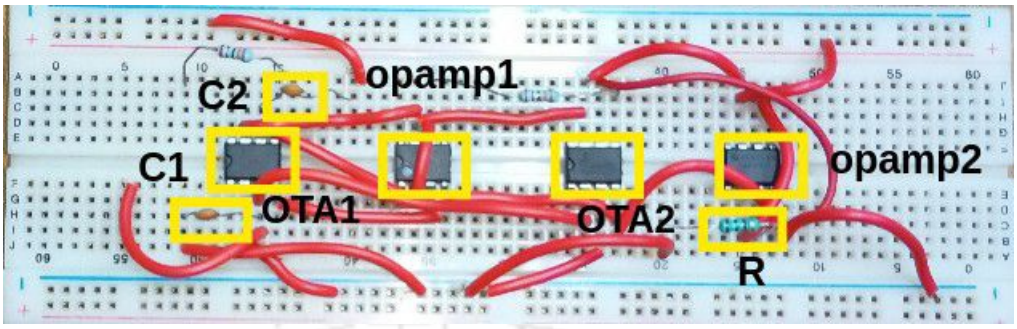
ature, as illustrated in Fig. 6.8(c). The correctness of the proposed emulator has been also verified for different process corners, as shown in Fig. 6.8(d). It can be seen that the lobe area of the PHL is wider for FF and smaller for SS. Note that there is a difference in the pre- and post-layout simulations due to the effect of parasitic elements. Further, the frequency domain noise analysis is performed for the pre- and post-layout designs of the proposed emulator shown in Fig. 6.5. The resulting noise densities (volts per square root hertz) are exhibited in Fig. 6.8(e). It can be observed that the noise ($\frac{1}{f}$) decreases with an increase in the frequency, which exhibits the expected noise behaviour. The large variation in the post-layout noise is obtained compared to pre-layout noise due to the presence of parasitic elements. Therefore, the post-layout analyses are in concurrence with the numerical analyses of the proposed emulator. The physical realization of the analytical model and numerical analyses are implemented by conducting experiments using off-the-shelf components described in the section below.

Table 6.4: Frequency-Power Analysis of Proposed Emulator

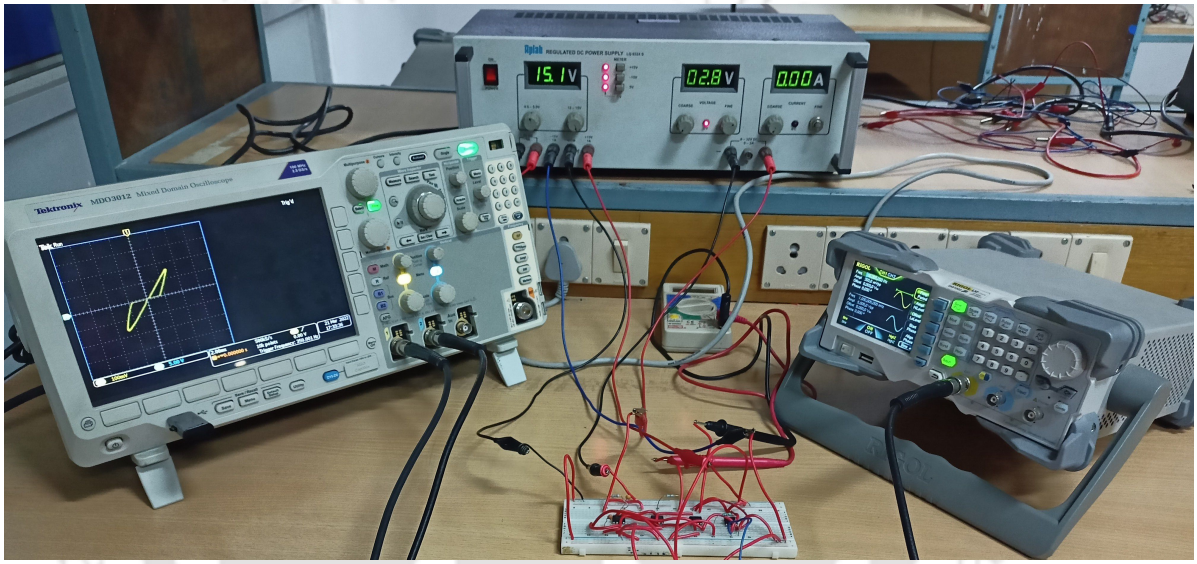
Frequency (MHz)	Power (mW)
1	2.34
6	2.08
8	2.01
10	1.96
12	1.92
16	1.86
18	1.83
20	1.82
22	1.80
24	1.78

6.4.3 Experimental analysis

The physical experiment of the proposed emulator is performed on the breadboard using commercially available solid state components to emulate its characteristics, as shown in Fig. 6.9(a). Experimental setup consists of Rigol DG1022 function generator and MDO3012 Mixed Domain Oscilloscope, which are employed for applying sinusoidal input signal with varied frequencies and for recording its characteristic. An Aplab power supply is utilized to provide regulated DC to the emulator, as showcased in Fig. 6.9(b). In this experiment, $CA3080$ analog ICs are employed to realize OTAs. Similarly, $\mu A741$ is used to configure UGA along with resistors and capacitors, as shown in Fig.



(a)



(b)

Figure 6.9: (a) Prototype on breadboard and (b) Experimental setup of the proposed emulator

6.10. In our experiment $C_1 = 1.5\ nF$, $C_2 = 1\ pF$ and $R = 1\ k\Omega$ are used, and the transconductance of the first OTA is controlled by applying $V_{B1} = 2.8\ V$. Note that $V_{DD} = 15\ V$ and $V_{SS} = -15\ V$ are applied to $CA3080$ in the experiment as mentioned above.

Input sinusoidal signal with a peak-to-peak voltage of 200 mV with an operating frequency of 200 Hz is applied to the emulator for analyzing its transient behaviour and $V_{in} - q$ characteristics (PHL), as depicted in Figs. 6.11(a) and 6.11(b). It can be seen that the flat transition in the blue curve of transient behaviour is due to the parasitic effects and the switching delay caused by the current limiting resistors used in the experiment of the proposed emulator. The frequency-dependent behaviour of the proposed emulator is also verified experimentally at different frequencies, as shown in Figs. 6.11(c), 6.11(d), and 6.11(e). It can be observed that the lobe area of the PHL decreases with the increase in frequency, and the lobe area of the PHL for negative voltage reduces slightly.

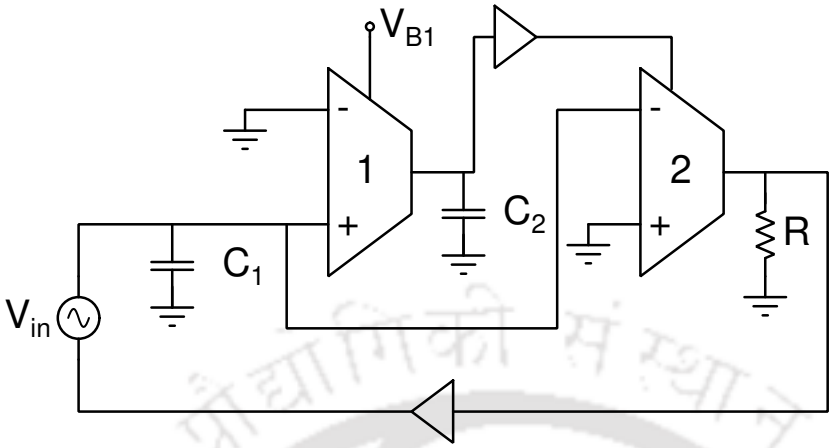


Figure 6.10: Memcapacitor experimental circuit

Since off-the-shelf elements used in the experimental validation are connected to mimic the proposed circuit, and it is not a replica of the CMOS circuit on the silicon, there is a variation in the lobe area of the PHLs at different frequencies compared to the simulated results. Moreover, asymmetrical PHLs are generated for the proposed circuit design and the physical implementation due to the presence of parasitic elements [142]. Thus, it can be stated that the experimental results are in good agreement with the analytical model and numerical analysis of the proposed emulator.

State-of-the-art memcapacitor emulators reported in the literature [61–63, 65] are realized using opamps, multipliers, CCII, and passive elements. They exhibit high circuit complexity and low operating frequency. Although some of the emulators with improved operating frequency are presented [60, 66, 67, 143, 144], but these emulators are designed using many active and passive components, including multipliers and mutators, for realizing a memcapacitor. Thus, these emulators exhibit high design complexity, and due to the use of multipliers, the lobe area of the PHL reduces, limiting their operating frequencies [78]. Note that for emulating the memcapacitor, the product of the time integral of charge ($\sigma(t)$) and charge ($q(t)$) are essential. This can be achieved directly by employing a multiplier. However, the use of a multiplier reduces the characteristic of an emulator to $1/10^{th}$ of the actual response, which leads to a decrease in the lobe area of the PHL and becomes a straight line at high frequencies, losing the memcapacitive behavior. Thus, it can be stated that the operating frequency of the emulators utilizing a multiplier is not very high. This can also be corroborated employing Table 6.5. The performance of the proposed emulator is significantly improved over other emulators by the following factors: (a) the multiplication of the time integral of charge ($\sigma(t)$) and

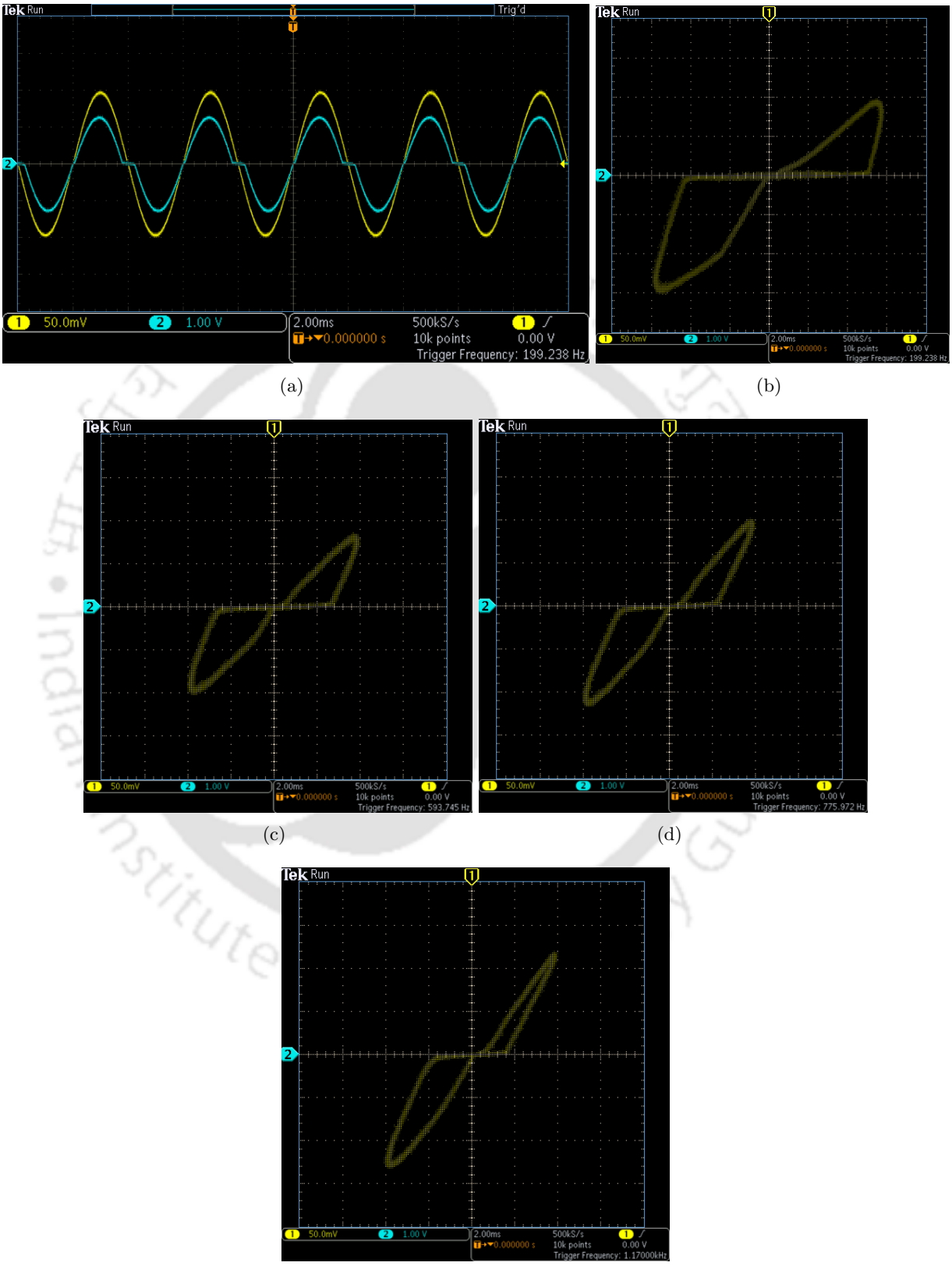


Figure 6.11: (a) Transient characteristics (b) PHL of experiment (c) PHL at 600 Hz (d) PHL at 775 Hz and (e) PHL at $1k$ Hz

Table 6.5: Comparative analysis of proposed memcapacitor emulator with available memcapacitor emulators

Ref.	Active components	Passive components	No. of transistors	Max. operating freq.	Expt./Sim.	Area	Power	Technology used
[65]	4-opamps, 1-AM, 1-current source	2-R, 3-C	-	10 Hz	Simulation	-	-	PSPICE
[61]	5-opamps, 1-diode	13-R, 2-C, 1-LDR	-	10 Hz	Both	-	-	Multisim
[63]	4-CCII, 1-AM, 2-opamps	8-R, 2-C	-	15 Hz	Both	-	-	SPICE
[143]	4-CCII, 1-varactor diode, 1-opamp	6-R, 2-C	-	8 kHz	Both	-	-	Multisim
[60]	4-CCII, 1-varactor diode	2-R, 2-C	> 40	180 kHz	Both	288 mm^2	780 mW	PSPICE
[144]	2-CCII, 1-OTA	2-R, 2-C	> 40	700 kHz	Both	8098 μm^2	14.741 mW	TSMC 180nm
[62]	4-CCII, 1-AM, 2-Opamps	9-R, 2-C	-	86.6 Hz	Both	-	-	SPICE
[66]	1-CCII, 1-OTA, 1- AM	3-C	> 30	2 kHz	Both	-	-	Macro Models
[67]	2-CCII, 1-AM	2-R, 2-C	> 40	25 kHz	Both	-	-	PSPICE
This work	**2-OTA, 1-UGA, 2-MOS-capacitors**	1-R	**25**	**24 MHz**	**Both**	2034.65 μm^2	**1.86 mW**	**TSMC 180nm**

Here, R, C, and AM represent resistor, capacitor, and analog multiplier.

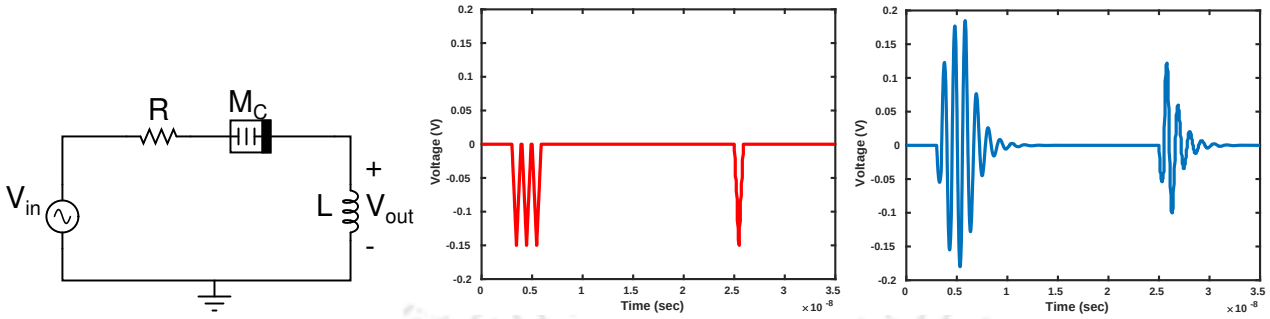
charge ($q(t)$) is performed using the transconductances (g_{m1} and g_{m2}) of the OTAs without using a multiplier, (b) as we know, the switching speed of the MOSFET is very high and suitable for low power high frequency applications. This property of the MOSFET is exploited in the proposed emulator by employing MOS capacitors, which aid in increasing the operating frequency [147], and (c) there is a reduction in the switching delay due to the least number of active and passive components used in the proposed emulator, which helps it to be operated at a high frequency.

Its area utilization and power consumption are substantially less along with the maximum operating frequency than the standard emulators mentioned in Table 6.5. It can be seen that the proposed memcapacitor has 34×, 4×, and 8.189× better operating frequency, area utilization, and power consumption than its nearest contemporary memcapacitors available in the literature. The feasibility of the proposed emulator in the real-time application is described in the following section.

6.5 Application of the proposed memcapacitor emulator

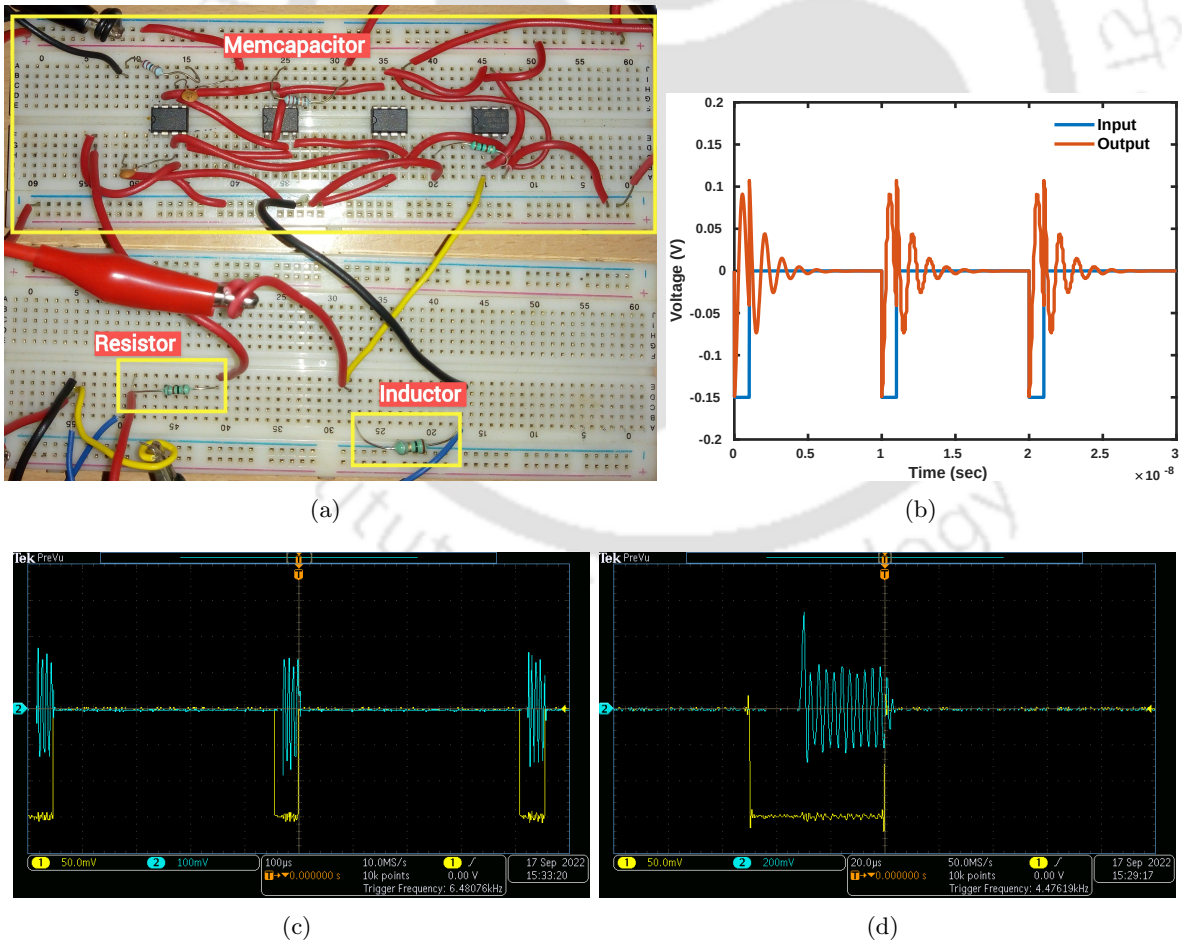
Effectiveness of the proposed emulator is validated by implementing a memcapacitor based adaptive learning circuit as depicted in Fig. 6.12(a). This circuit is based on the behaviour of the biological organism amoeba to its external stimulus. Despite of lacking a neural system, this unicellular organism is remarkably intelligent because of its ability to solve puzzles and mazes, recall the past, and learn and anticipate future occurrences based on its memory [115]. It exhibits three vital characteristics: (1) memorizing the previous history, (2) predicting the environmental change, and (3) following and understanding the period of events [114]. This unicellular being slows down its locomotive speed in response to changes in environmental parameters, such as humidity and temperature. These amoebic learning capabilities are translated into a memory element and other circuit elements, as discussed in [114]. Once exposed to a change, the amoeba remembers it and anticipates the change that might occur soon. Despite being unicellular, an amoeba can memorize the periodic sequence of environmental changes and responds accordingly, anticipating a change.

The adaptive circuit shown in Fig. 6.12(a) mimics the memory behaviour of the amoeba mentioned above. The schematic of the adaptive learning behaviour consists of three elements: resistor (R), inductor (L), and memcapacitor (M_C). All three components are connected to establish a series resonant circuit with a frequency of $f = \frac{1}{\sqrt{LM_C}}$. The simulation of the adaptive learning behaviour is performed using Cadence Virtuoso with TSMC 180 nm PDKs. The temperature and humidity that



(a) (b) (c)

Figure 6.12: Adaptive learning (a) Schematic (b) Input voltage spikes and (c) Response of the adaptive circuit



(a) (b)

(c) (d)

Figure 6.13: Adaptive learning (a) Breadboard setup (b) Simulated result (c) Experimental result and (d) Response at single pulse

Table 6.6: Parameters used in the adaptive learning circuit

Parameter	Description	Values	
		Simulation	Experiment
$V_{in}(t)$	Input voltage	-150 mV, Time period of 30 ns	-150 mV, 10% Duty cycle
R	Resistor	1 $K\Omega$	560 Ω
M_C	Memcapacitor	$C_{MC1} = 4\ pF$, $C_{MC2} = 3\ pF$	$C_1 = 1.5\ nF$, $C_2 = 1\ pF$
L	Inductor	1 μH	1 μH (axial lead type inductor)

govern the locomotive speed of the amoeba correspond to an input voltage, V_{in}. Further, an output voltage across the inductor (L), V_{out}, is analogous to the amoeba's locomotive speed. The parameters used to perform the numerical analysis are shown in Table 6.6.

Initially, three negative spikes were applied to train the circuit, as shown in Fig. 6.12(b). These input spikes also resulted in corresponding negative spikes on the output, as depicted in Fig. 6.12(c). Moreover, the circuit remembers this change and gives a larger response for the consecutive input spike. The presence of the memcapacitor increases the resonant frequency of the circuit with every negative spike applied, and after three negative spikes, the circuit tunes into the resonant frequency same as that of the input signal. A fourth input spike is applied after a short interval that re-initiates resonance in the circuit, followed by the trail of the output spikes observed due to the training of the circuit by the initial three voltage spikes. The amplitude of the voltage of output spikes reduces in the absence of input spikes, representing damped oscillations due to the presence of the resistor [114]. It can be observed that there is a delay at the output with respect to the input due to the memcapacitive switching behaviour in a memristive system [148]. In a memcapacitor-based adaptive learning circuit, the capacitor needs to change its internal state to match the frequency of temperature variations that inducts a small delay.

A physical experiment is also conducted to validate the viability of the proposed memcapacitor-based adaptive learning circuit. The breadboard implementation of the adaptive learning circuit was designed using the proposed memcapacitor emulator, as shown in Fig. 6.13(a). The components used in this experiment are depicted in Table 6.6. The correctness of the practical circuit is verified by applying a negative voltage pulse, as shown in Fig. 6.13(c). The damping oscillations are generated

for every negative pulse illustrated in Fig. 6.13(d), which is in congruence with the simulation result shown in Fig. 6.13(b), validating memory retention property and nonlinear behaviour of adaptive learning circuit numerically as well as experimentally.

6.6 Conclusion

In this work, an optimized charge-controlled floating memcapacitor emulator is proposed comprising of active elements and a resistor. Its analytical model is validated numerically and experimentally using *Cadence Virtuoso* analog design environment with $TSMC$ 180 nm $PDKs$, and off-the-shelf components, such as $CA3080$ ICs, resistors, and capacitors, respectively. The post-layout analysis is also performed to validate its correctness and reliable characteristics. The area utilization and power consumption of the proposed memcapacitor emulator are 2034.65 μm^2 and 1.86 mW, respectively. It can also perform high frequency operations up to 24 MHz as compared to other contemporary memcapacitor emulators. As per our knowledge, it exhibits the highest operating frequency among all these state-of-the-art emulators available in the literature, and illustrates 34×, 4×, 8.189× better operating frequency, area utilization, and power consumption compared to its nearest contemporary memcapacitor emulator. Further, its effectiveness is testified by designing a memcapacitor-based adaptive learning circuit, which also confirms that the proposed emulator can be efficiently utilized in practical applications due to its simple design, optimal performance, and easier integration as a circuit element.

7

Conclusion and Future Work

Contents

7.1 Conclusion

This thesis proposes two window functions for memristor modelling, which provide nonlinear characteristics to the memristor model. The proposed adaptive and dynamic window functions of a memristor are designed to achieve higher nonlinearity and scalability without any boundary effects and distortion in the PHL of memristor behaviour over a wide range of voltages and frequencies compared to other standard window functions presented in the literature.

The optimized MOS-DTMOS based emulators are proposed in this thesis to realize the memristor behaviour consisting of four transistors and an external capacitor, which help obtain high-frequency operation in the MHz range reliably. The correctness of the proposed emulators is validated by conducting various parametric analyses at different operating frequencies and process corners, and it generates acceptable pinched hysteresis loops (PHL) at various frequencies. Further, pre- and post-layout validations of the proposed emulators are also performed using Cadence Design Tool Virtuoso with TSMC 180 nm PDKs to prove their effectiveness as memristors. The proposed memristor emulators are validated physically using ALD1106 n-channel MOSFETs to characterize their functionality as a real-life memristor. They employed in the design of memristor-based applications to showcase their applicability in power and area optimal circuit design. The key features of the proposed emulator are listed below.

(i) It consists of four n-channel MOSFETs only, which makes it suitable for monolithic IC fabrication.

(ii) It is more area efficient than any other known emulator.

(iii) It works at a higher frequency range and exhibits low power consumption.

(iv) Unlike other emulators, the proposed emulator works without external bias.

The other memelements, such as meminductor and memcapacitor emulators, are realized by designing area and power-optimized circuits operating at high frequencies. The proposed meminductor emulator is realized using MOSFETs only without employing any passive elements, making it work at the maximum operating frequency, 20 MHz, compared to other meminductor emulators available in the literature. Further, the memcapacitor emulator is also designed utilizing a few active and passive components. The proposed memcapacitor emulator employs the minimum area and consumes less

power at the maximum operating frequency, 24 MHz, than the emulators reported in the literature. These emulators are thoroughly verified analytically and numerically using *Cadence Virtuoso* and $TSMC$ 180 nm PDKs. They are validated by conducting experiments using off-the-shelf components along with CA3080 OTAs. The proposed memcapacitor and meminductor emulators exhibit the following advantages.

(i) Utilize a minimal area of 2034.65 μm^2 and 2350.67 μm^2 than other contemporary emulators

(ii) Less power consumption of 1.86 mW and 3.3 mW

(iii) Simple circuit topologies using MOSFETs and fewer passive elements suitable for the monolithic IC fabrication

(iv) Easier integration with other circuit elements while designing practical applications

Further, various applications, such as filters, logic gates, chaotic oscillators, and adaptive learning circuits, are designed using the proposed memelements emulators for validating their applicability in various applications. Thus, as per the delineated objectives of this work, proposed emulators can be used to exploit versatile properties in future high-performance neuromorphic computing, synaptic design, spiking neural networks, and other bio-inspired applications due to their simplicity, adaptability, and flexibility.

The advantages of our proposed memelements emulators are mentioned below.

(i) Optimized MOSFET-based designs suitable for monolithic IC fabrication.

(ii) Lower area utilization and power consumption and higher operating frequency.

(iii) The simplicity of the proposed emulator facilitates easy integration with other circuits/devices for designing potential.

The disadvantages of our proposed memelements emulators are elaborated below.

(i) The characteristics of the proposed emulators are slightly deviated from the ideal behaviour due to the affect of nonidealities of MOSFETs.

(ii) Static power dissipation is more due to the utilization of MOSFETs than the actual solid-state memelements.

7.2 Future work

- The proposed memelements are designed using fewer active and passive components, making them suitable for silicon fabrication as they were validated by post-layout simulation. Therefore, fabricating on-chip emulators can make them easier for the practical applications.
- The proposed memelements emulators can be used to study and analyze the neural network design, programmable analog circuits, secure communication, cryptography, random signal generators, spiking neural networks, low-power biomedical signal processing circuits for cardiovascular diseases, low-power circuits for approximate computing, and other bio-computing applications due to their wide frequency operations.
- These emulators can be replaced by dedicated memelements devices when suitable materials with appropriate fabrication steps are provided for commercial usage.

List of Publications

Journal Publications

1. **Ananda Y R**, G. S. Satyanarayan, and Gaurav Trivedi, "A Flux Controlled MOS-Based Optimized High Frequency Meminductor Emulator," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (IEEE JETCAS)*, vol. 12, no. 4, pp. 774–784, 2022. (DOI: 10.1109/JETCAS.2022.3221305)

2. **Ananda Y R**, Nehal Raj, and Gaurav Trivedi, "A MOS-DTMOS Implementation of Floating Memristor Emulator for High-Frequency Applications," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 31, no. 3, pp. 355–368, 2023. (DOI: 10.1109/TVLSI.2022.3227201)

3. **Ananda Y R**, G. S. Satyanarayan, and Gaurav Trivedi, "An Optimized MOS-Based High Frequency Charge-Controlled Memcapacitor Emulator," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (IEEE JETCAS)*, vol. 12, no. 4, pp. 793–803, 2022. (DOI: 10.1109/JETCAS.2022.3221314)

4. **Ananda Y R**, G. S. Satyanarayan, and Gaurav Trivedi, "A High Frequency MOS-based Floating Charge-Controlled Memcapacitor Emulator," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 3, pp. 1189–1193, March 2023. (DOI: 10.1109/TCSII.2022.3221334)

Conference Publications

1. **Ananda Y R**, Arkadeep, and Gaurav Trivedi, "An Adaptive Window Function based Memristor Model," *33rd International Conference Radioelektronika 2023*, Pardubice, Czech Republic, 2023, pp. 1–5. (DOI: 10.1109/RADIOELEKTRONIKA57919.2023.10109029)

2. **Ananda Y R**, Subhashis Das, and Gaurav Trivedi, "A Novel Dynamic Memristor Window Function for High Frequency Applications," *2023 21st IEEE Interregional NEWCAS Conference (NEWCAS)*, Edinburgh, United Kingdom, 2023, pp. 1-5. (DOI: 10.1109/NEWCAS57931.2023.10198059).

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