DESIGN OF AMPLIFIERS AND FABRICATION OF HIGH PERFORMANCE THIN-FILM TRANSISTORS USING CARBON NANOTUBES

A

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By

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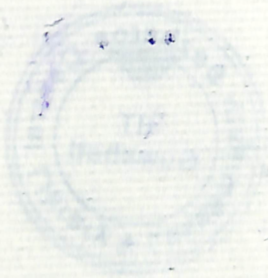

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Certificate

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TH-1861_07610208

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TH-1861_07610208

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Abstract

The work carried out in this thesis is divided into three parts. The first part discuss the study on carbon nanotube (CNT) interconnects. The second part will be dealing with the modeling of CNT based transistors and design of analog circuits based on CNTs. The final part will present the fabricated thin film transistors based on single walled carbon nanotubes (SWCNTs). The study on the SWCNT interconnects is focused on the estimation of their magnetic inductance at various bias voltages. The analysis of magnetic inductance is carried out for the ground-signal-ground (GSG) configuration of SWCNT based interconnects having various dimensions and different percentage of metallic SWCNT (m-SWCNT) purities. The results indicate a variation in the loop inductance value as high as 34% for closely spaced semi-global interconnects.

The study on the SWCNT transistor modeling aims to develop closed-form equations for the drain current and drain to source voltage for CNT field effect transistor (CNFET) in terms of its dimensions. Although these proposed models are based on curve fitting method, they provide a quick first order numerical estimate of drain current and drain to source voltage of the CNFET. The estimated values of the current and voltage using the proposed equations are in close agreement when compared to a SPICE compatible model and measured results of a fabricated device. The CNFET based analog circuits such as common source amplifiers and differential amplifier are designed using the proposed equations. The simulation results shows a better performance of the CNFET amplifiers in terms of the DC gain and gain band width product at the same power power consumption when compared to the conventional CMOS counterparts. A study on the performance of CNFET amplifiers for parameter variations like diameter, spacing and number of CNTs are also presented.

The final and major part of thesis presents the fabrication and characterization of various types of semiconducting nanotube thin-film transistors (SN-TFTs). Nine dif-

TH-1861_07610208

ferent SN-TFTs of various dimensions having HfO_x or SiO_2 as gate dielectric material, consisting of global, local, top or dual gate structures with the thin-film of 90% or 95% purity of semiconducting SWCNT (s-SWCNT) fabricated under similar process conditions are investigated. The wafer scale SN-TFTs consisting of nanotubes of 95% enriched s-SWCNTs have demonstrated a higher on-off current ratio compared to the devices with 90% purity s-SWCNTs. A technique to deposit the nanotube thin-film of densities 40-45 SWCNTs/μm^2 over the silanized HfO_x surface was introduced for the first time. The HfO_x based global back gate SN-TFTs have shown a lower threshold voltage, higher current density and higher mobility compared to the SiO_2 based devices. The HfO_x based local back gate SN-TFTs are fabricated on wafer scale and devices have exhibited the lowest threshold voltage, steeper subthreshold slope, higher current density and higher mobility compared to other reported devices. The dual gate SN-TFT has shown steepest subthreshold slope among the reported SN-TFTs and has a higher mobility and a lower threshold voltage compared to single gate SN-TFTs.

TH-1861_07610208

Contents

List of Figures xv

List of Tables xxiii

List of Acronyms xxv

1 Introduction 1

1.1 Introduction 2

1.2 Basics of Carbon Nanotube 2

1.3 Carbon Nanotube Interconnects 4

1.4 Modeling of Carbon Nanotube Transistors 5

1.5 Fabrication of Carbon Nanotube Transistors 7

1.6 Motivation and Problem Definition 8

1.7 Organization of the Thesis 9

1.8 Summary 11

2 Impact of Bias Voltage on Magnetic Inductance of Carbon Nanotube Interconnects 13

2.1 Introduction 14

2.2 Modeling of Resistance in an Isolated SWCNT 15

2.2.1 Intrinsic Resistance (R_i) 15

2.2.2 Contact Resistance (R_c) 15

2.2.3 Ohmic Resistance (R_o) 15

2.3 Modeling of Inductance in SWCNT bundles 16

2.3.1 Kinetic Inductance (l_k) 16

2.3.2 Magnetic Inductance 17

2.4 Bias Voltage Dependence of Loop Inductance in SWCNT Interconnect 18

2.5 Simulation Results of Loop Inductance 19

TH-1861_07610208

2.6 Summary 23

3 **Design and Simulation of Analog Amplifier Circuits using Carbon Nanotube Field-Effect Transistors** **25**

3.1 Introduction 26

3.2 Simplified Closed-Form Equations for CNFET 29

3.2.1 Saturation Drain Current Equation 31

3.2.2 Drain to Source Saturation Voltage Equation 35

3.3 Common-Source CNFET Amplifiers 40

3.3.1 Resistive-Load Common-Source Amplifier 41

3.3.2 Active-Load Common-Source Amplifier 45

3.4 Single-Stage CNFET Differential Amplifier 50

3.5 Summary 52

4 **Fabrication of Different Types of SN-TFTs** **55**

4.1 Introduction 56

4.2 Deposition of Carbon Nanotubes 59

4.2.1 Spin-Coat Technique 60

4.2.2 Dip-Coat Technique 61

4.2.3 Immersion Technique 62

4.3 Fabrication of SN-TFTs 64

4.3.1 Process Flow of Global Back Gate SN-TFTs 64

4.3.2 Process Flow of Local Back Gate SN-TFTs 67

4.3.3 Process Flow of Top Gate SN-TFT 70

4.3.4 Process Flow of Dual Gate SN-TFT 71

4.4 Summary 74

5 **Wafer Scale Global Back Gate SN-TFTs having SiO_2 or HfO_X as Gate Dielectric** **77**

5.1 Introduction 78

5.2 Results of Material Characterization 79

5.3 Electrical Characterization Results of SN-TFTs having Different Gate Dielectric Material 80

5.4 Summary 84

TH-1861_07610208

6 Wafer Scale Global Back Gate SN-TFTs having Thin-Film of 90% or 95% purity s-SWCNTs 87

6.1 Introduction 88

6.2 Results on Purity of s-SWCNTs 89

6.3 Electrical Characterization Results of Wafer Scale Interdigitated Type SN-TFTs . . 90

6.4 Performance Comparison of Wafer Scale SN-TFTs having Different Purity s-SWCNTs 94

6.5 High Performance and High On-Current SN-TFT 98

6.6 Summary 100

7 Wafer Scale High Performance Local Back Gate SN-TFTs 101

7.1 Introduction 102

7.2 Electrical Characterization of Local Back Gate SN-TFTs 103

7.2.1 Results of *I-V* Characterization 103

7.2.2 Results of *C-V* Characterization 111

7.3 Summary 113

8 SN-TFT Channel Control Using Various Gate Structures 115

8.1 Introduction 116

8.2 Electrical Characterization Results of Top, Bottom and Dual Gate SN-TFTs 117

8.3 Performance Comparison of Wafer Scale Global and Local back gate SN-TFTs . . . 121

8.4 Summary 124

9 Conclusion 127

9.1 Contributions 128

9.2 Directions for Future Research 130

Bibliography 133

List of Publications 141

TH-1861_07610208

List of Figures

1.1 The two dimensional graphene sheet, showing the lattice vectors and possible rolling orientation to form different types of carbon nanotubes. 3

2.1 GSG configuration of the SWCNT interconnect bundles implementing a signal line and two adjacent ground return paths. 18

2.2 Loop inductance at different bias voltages for a GSG configuration with $w_b = h_b = 10$ nm. (a) For a length of 10 μm. (b) For a length of 1000 μm. 20

2.3 Percentage change in loop inductance of a GSG configuration of length 10 μm and $w_b = h_b = 10$ nm. (a) For a separation of 1 nm. (b) For a separation of 100 nm. 21

2.4 Change in loop inductance as a function of V_{bias} for a constant P_m of 0.33 for interconnects having different lengths and spacing. 21

2.5 Comparison of loop inductance of copper and SWCNT bundles for different lengths and P_m values. 22

3.1 (a) The 3D structure of CNFET with multiple channels. (b) Cross sectional view of CNFET indicating different dimensions. (c) Top view of the device. 30

3.2 Dependency of CNFET drain current on different parameters. (a) shows the V_{GS} effect for different diameter of SWCNTs. For curves (b) to (f) V_{GS} is varied from 0.35 V to 0.65 V. (b) for various channel lengths. (c) for different L_{sd} values. (d) for various SWCNT diameter. (e) as a function of number of SWCNTs and (f) for different spacing between the SWCNTs. 33

TH-1861_07610208

3.3 Percentage deviation in the proposed equation current compared to J. Deng's model [32] for (a) V_{GS} = 0.55 V, L_{sd} = 32 nm and other parameters are varied within range indicated in Table 3.1 (b) L_{ch} = 32 nm, L_{sd}= 32 nm and other parameters are varied within range indicated in Table 3.1 (c) V_{GS} = 0.55 V, L_{ch} = 32 and other parameters are varied within range indicated in Table 3.1. 34

3.4 *I-V* characteristics of n-type CNFET device obtained by simulating the J. Deng's model [32] for device channel length (a) less than 100 nm (b) more than 100 nm. . 36

3.5 Dependency of CNFET drain to source saturation voltage on V_{GS}, L_{ch} and D_{CNT}. (a) shows the V_{GS} effect at a constant channel length of 40 nm for different SWCNT diameters. (b) shows the effect of SWCNT diameter for different channel length at a constant gate voltage of 0.35 V. (c) shows V_{DSsat} variation for different channel length at V_{GS} of 0.35 V for various SWCNT diameter. V_{DSsat} dependency of devices having channel length more than 100 nm for similar parameter variations are shown in (d), (e) and (f). 38

3.6 Comparison of current and voltage estimated by the proposed equations with the experimental results of Amlani et al. [74] and the simulation results of J. Deng et al. [32]. (a) Drain current for different gate source voltages. (b) V_{DSsat} for different gate source voltages. 40

3.7 Different capacitance of CNFET. (b) 3D view showing the fringing and inter electrode capacitance. (b) Cross sectional view showing gate to channel capacitance. 41

3.8 Resistive-load common-source amplifier. 42

3.9 Performance comparison of CNFET and MOSFET resistive-load common-source amplifiers. (a) Output voltage versus input voltage. (b) Gain versus supply voltage. (c) Output voltage swing versus supply voltage. 43

3.10 Active-load common-source amplifier. 46

3.11 Performance comparison of the CNFET active-load CS-amplifier with that of the MOSFET amplifier. (a) Gain versus supply voltage. (b) Output voltage swing versus supply voltage. (c) Frequency response of CNFET active-load CS-amplifier for different capacitive loads and inset shows the same for MOSFET amplifier. 48

TH-1861_07610208

3.12 (a) Single-stage differential amplifier circuit. (b) The frequency response of CNFET circuit for different capacitive loads and inset shows the same for MOSFET circuit. . 51

4.1 SEM images of SWCNT thin-film deposited on the non-functionalized oxidized surfaces. (a) SWCNTs over Si/SiO_2 surface. (b) SWCNTs over Si/HfO_x surface. 60

4.2 SEM images of the SWCNT thin-film deposited on the functionalized Si/HfO_x surface by spin-coat technique. (a) SWCNTs deposited at a spin rate of 2000 rpm. (b) SWCNTs deposited at a spin rate of 4000 rpm. 61

4.3 Water droplet on a functionalized Si/SiO_2 surface. 62

4.4 SEM images of SWCNT thin-film deposited on the functionalized surface by dip-coat method. (a) SWCNTs on Si/SiO_2 surface. (b) SWCNTs on Si/HfO_x surface. 62

4.5 Water droplet on a functionalized Si/HfO_x surface. 63

4.6 SEM image of SWCNT thin-film deposited on the functionalized Si/HfO_x surface by immersion method. 63

4.7 Process flow for the fabrication of back gate SN-TFT having IDE source/drain contacts. (a) HfO_x (SiO_2) deposited (grown) on Si substrate. (b) SWCNTs deposition over APTES functionalized HfO_x (SiO_2) surface. (c) Lift-off resist and positive photoresist layers after developing. (d) Pd and Au deposited over developed lift-off resist and positive photoresist layers. (e) Pd and Au on SWCNTs for source/drain contact after lift-off process. (f) Chromium/gold deposited as gate contact at the back side of wafer. 65

4.8 Wafer scale view of devices (right side) and zoom-in (left side) shows three different IDE source/drain patterns employed. 66

4.9 Layout pattern showing an array of global gate SN-TFTs with normal source/drain contacts and magnified view of an individual device. 67

4.10 Process flow for the fabrication of back gate SN-TFT with normal source/drain contacts. (a) Pd deposited over developed on the SWCNT thin-film. (b) Au patterns defining the contact probes for source/drain. (c) Chromium/gold deposited as gate contact at the back side of wafer. 68

4.11 Microscopic images of the fabricated global back gate SN-TFTs. (a) Typical IDE source/drain contacts. (b) Typical normal source/drain contacts. 68

TH-1861_07610208

4.12 Process flow for the fabrication of local back gate SN-TFT. (a) SiO_2 grown on Si substrate. (b) Pd film of 7 nm thickness deposited by RF sputtering as local back gate. (c) High-k HfO_X layer deposition as gate gate dielectric material. (d) Thin-film of SWCNTs deposited on the silanized oxide surface. (e) Pd deposition for source and drain contacts. (f) Gold deposition for large area contact pads. 69

4.13 Masks used for fabrication of local back gate SN-TFTs. An array of 4 device patterns are given on the left side. The magnified view of an individual device and details of different masks are given on the right side. 70

4.14 Images of local back gate SN-TFT. (a) Microscope image of a typical local back gate SN-TFT. (b) SEM image indicating the contact of SWCNT thin-film with palladium source/drain regions. 71

4.15 Process flow for the fabrication of top gate SN-TFT. (a) SiO_2 grown over the Si substrate. (b) HfO_X layer after deposition and lift-off process. (c) Thin-film of SWCNTs deposited on the silanized oxide surface. (d) Palladium deposition for source and drain contacts. (e) Gold deposition for large area contact pads. (f) Deposition of SiO_2 layer as dielectric material for the top gate. (g) Tungsten deposition to realize the top gate structure. 72

4.16 Process flow for the fabrication of dual gate SN-TFT. (a) SiO_2 grown over the Si substrate. (b) Back gate on Si/SiO_2 surface after lift-off process. (c) Deposition of HfO_X layer as dielectric for back gate. (d) Thin-film of SWCNTs deposited on the silanized oxide surface. (e) Palladium deposition for source and drain contacts. (f) Gold deposition for large area contact pads. (g) Deposition of SiO_2 layer as dielectric for top gate. (h) Tungsten deposition to realize the top gate structure of the dual gate SN-TFT. 73

4.17 Summary of different thin-film depositions carried out during the fabrication of SN-TFTs. 74

4.18 Summary of SN-TFTs fabricated which includes different gate structures, different source/drain contacts, different gate dielectric materials and different purity of s-SWCNTs. 75

TH-1861_07610208

5.1 Raman spectroscopy data of the SWCNT thin-film with 95% purity s-SWCNTs. (a) Raman data indicating characteristics peaks RBM, D band and G band. (b) RBM data of SWCNTs deposited on HfO_X surface. (c) RBM data of SWCNTs deposited on SiO_2 surface. 80

5.2 Atomic force microscopy data indicates that SWCNTs range in length from approximately 100 nm to 4 microns (Courtesy: NanoIntegris Inc.). 81

5.3 Experimental setup to characterize global gate SN-TFTs. 81

5.4 Electrical characteristics of SN-TFTs. (a) Output characteristics of SiO_2 based SN-TFT. (b) Triode region characteristics of SiO_2 based SN-TFT. (c) Transfer characteristics of both SiO_2 and HfO_X based SN-TFTs. 83

5.5 Electrical parameters of SN-TFTs based on both SiO_2 and HfO_X gate dielectric, as a function of channel length. (a) Current density, I_D/W (μA/μm). (b) On-resistance. (c) Normalized transconductance. 85

6.1 Raman spectroscopy data for the SWCNTs on silanized oxide surface. (a) RBM data obtained for 90% pure s-SWCNTs. (b) RBM data for sample with 95% s-SWCNTs. 90

6.2 Electrical characteristics of HfO_X based SN-TFTs. (a) Output characteristics of 95SN-TFT. (b) Transfer characteristics of both 90SN-TFT and 95SN-TFT. 91

6.3 Electrical parameters of wafer scale HfO_X based SN-TFTs having 90% or 95% purity s-SWCNTs plotted as a function of channel length. (a) Average drain current on-off ratio. (b) On-current density (I_D/W). (c) Normalized transconductance. (d) Carrier mobility. 92

6.4 Output characteristics of global back gate SN-TFTs. (a) *I-V* plot of 95SN-TFT for various V_{GS} and V_{DS} ranging from 0 to -10 V. (b) Output characteristics of 95SN-TFT to study the linear region of operation for small drain voltage range of -1 V to 1 V. (c). Drain current variations of 90SN-TFT for various V_{GS}. 95

6.5 Transfer characteristics of global back gate SN-TFTs having thin-film of 90% and 95% s-SWCNTs. 96

TH-1861_07610208

6.6 Statistical study of performance parameters of wafer scale global back gate SN-TFTs. (a) On-off ratio exhibited by both types of SN-TFTs based on 90 and 95% purity s-SWCNTs. (b) On-current exhibited by global gate SN-TFTs of various channel length having different channel width (solid line - 95SN-TFT, dash line - 90SN-TFT). (c) Average on-current density measured for both types of SN-TFTs for various channel length. (d) Normalized transconductance. (e) Mobility of devices with various channel length. 97

7.1 Experimental setup to characterize local gate SN-TFTs. 104

7.2 Electrical characterization of local gate SN-TFT having the channel length 20 μm and width 15 μm. (a) Output characteristics of the device for local gate voltages ranging from -1 V to -5 V in steps of -1 V. (b) Linear region of the output characteristics . . 105

7.3 Transfer characteristics of local back gate SN-TFT. (a) Drain current variations (logarithmic scale) for different V_{GS} at constant V_{DS} of -1 V and the corresponding gate leakage current. (b) Drain current variations (linear scale) and transconductance variation for various V_{GS} values. 106

7.4 Performance of wafer scale fabricated local back gate SN-TFTs. (a) Variation of drain current on-off ratio as a function of channel length. (b) Current on-off ratio distribution of fabricated SN-TFT devices. 107

7.5 Electronic properties of local back gate SN-TFTs. (a) Average on-current of SN-TFTs for various channel dimensions. (b) Average on-current of SN-TFTs for various channel dimensions in linear scale. (c) I_D/W variation as a function of channel length. (d) Average transconductance per unit channel width and average mobility of the SN-TFT as a function of channel length. 108

7.6 Experimental setup for C-V measurement. 111

7.7 Capacitance measurements of local back gate SN-TFTs. (a) C-V curves of the devices having different channel dimensions. (b) C-V measurements of a SN-TFT using different frequency ac signal. (c) C-V curve obtained by double sweep of the gate voltage. 112

TH-1861_07610208

8.1 The output characteristics of the SN-TFTs having different types gate structure. (a) *I*-*V* plots of dual gate SN-TFT for V_{GS} ranging from -0.4 V to -2 V. (b) p-type behavior of back gate SN-TFT. (c) I_D-V_{DS} plot of the top gate SN-TFT for V_{GS} ranging from -1 V to -5 V. 118

8.2 Transfer characteristics and transconductance of SN-TFTs for different V_{GS} and at a constant V_{DS} of -2 V. (a) for the dual gate SN-TFT. (b) for the back gate SN-TFT. (c) for the top gate SN-TFT. (d) Transfer characteristics of all 3 types of devices. . 120

8.3 Electrical parameters of global and local gate SN-TFTs as a function of channel length. (a) Drain current on-off ratio. (b) On-current density (I_D/W). (c) Normalized transconductance. (d) Carrier mobility. 122

TH-1861_07610208

List of Tables

3.1 Typical range of values for different parameters of CNFET device. 31

3.2 Comparison of V_{DSsat} of CNFET device estimated by the proposed equation (3.4) and the J. Deng's model [32]. 39

3.3 Comparison of V_{DSsat} of CNFET device estimated by the proposed equation equation (3.5) and the J. Deng's model [32] 39

3.4 Performance of the CNFET resistive-load CS-amplifier for different supply voltages. 42

3.5 Effects of variation in the SWCNT dimensions on the performance of CNFET resistive-load CS amplifier. 45

3.6 Details of CNFET device dimensions and performance of a CNFET active-load CS-amplifier for different supply voltages. 47

3.7 Details CNFET device dimensions and performance of the CNFET active-load CS-amplifier for various process variations of SWCNT dimensions. 49

3.8 Details of the CNFET dimensions and performance of the CNFET active-load CS-amplifier for various channel length. 50

3.9 Performance comparison of a CNFET single-stage differential amplifier with a MOS-FET single-stage differential amplifier. 51

5.1 Performance comparison of SiO_2 and HfO_X based wafer scale SN-TFTs. 85

6.1 Performance comparison of 4 different wafer scale fabricated SN-TFTs with interdigitated source/drain contacts. 93

6.2 The performance comparison of high on-current SN-TFTs. 100

7.1 Performance comparison of various wafer scale fabricated SN-TFTs. 110

8.1 The performance comparison of SN-TFTs having three different gate structures . . . 121

TH-1861_07610208

8.2 Performance comparison of global and local gate SN-TFTs of identical channel lengths. 123

9.1 Performance comparison of various SN-TFTs fabricated in this work. 132

TH-1861_07610208

List of Acronyms

1D	One dimensional
3D	Three dimensional
AFM	Atomic Force Microscopy
Al_2O_3	Aluminum oxide
APTES	Aminoisopropyltriehoxy silane
Au	Gold
BHF	Buffered Hydrofluoric Acid
CNFET	Carbon Nanotube Field Effect Transistor
CNT	Carbon Nanotube
CNTFT	Carbon Nanotube Thin-Film Transistor
CMRR	Common Mode Rejection Ratio
Cr	Chromium
CS	Common-Source
Cu	Copper
CVD	Chemical Vapor Deposition
DI	Deionized
FET	Field-Effect Transistor
FIB	Focused Ion Beam
FOM	Figure of Merit
GBW	Gain Bandwidth
GIS	Gas Injection System
GSG	Ground-Signal-Ground
HfO_x	Hafnium oxide
IC	Integrated Circuit

TH-1861_07610208

ICMR	Input Common Mode voltage Range
IDE	Interdigitated Electrode
IPA	Iso Propyl Alcohol
ITRS	International Technology Roadmap for Semiconductors
LOR	Lift-off Resist
MFP	Mean Free Path
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
m-SWCNT	Metallic Single Walled Carbon Nanotube
MWCNT	Multi Walled Carbon Nanotube
Pd	Palladium
PEEC	Partial Element Equivalent Circuit
PE-oxide	Plasma Enhanced oxide
PPR	Positive Photoresist
PTM	Predictive Technology Model
RBM	Radial Breathing Modes
RCA	Radio Corporation of America
RF	Radio Frequency
SB	Schottky Barrier
SDS	Sodium Dodecyl Sulfate
SEM	Scanning Electron Microscopy
SiO_2	Silicon di-oxide
SN-TFT	Semiconducting Nanotube Thin-Film Transistor
SOI	Silicon on Insulator
SPICE	Simulation Program with Integrated Circuit Emphasis
s-SWCNT	Semiconductive Single Walled Carbon Nanotube
SWCNT	Single Walled Carbon Nanotube
TFT	Thin-Film Transistor
THD	Total Harmonic Distortion
W	Tungsten
Zr_2O_3	Zirconium oxide

TH-1861_07610208

1

Introduction

Contents

1.1 Introduction 2
1.2 Basics of Carbon Nanotube 2
1.3 Carbon Nanotube Interconnects 4
1.4 Modeling of Carbon Nanotube Transistors 5
1.5 Fabrication of Carbon Nanotube Transistors 7
1.6 Motivation and Problem Definition 8
1.7 Organization of the Thesis 9
1.8 Summary 11

TH-1861_07610208

1.1 Introduction

The carbon nanotube (CNT) can be conceptually viewed as a rolled-up graphene sheet and is one of the best alternate materials to meet the challenges due to the dimension scaling of future VLSI devices. Significant progress has been made in both understanding the fundamental properties and exploring possible engineering applications of CNTs since the earliest observations of nanotube-like structures were made by Iijima in 1991 [1]. The potential applications of CNTs spread to many diverse fields such as nanotechnology, electronics, optics and material science, nevertheless the two important electrical applications of the CNT are interconnects and transistors. An important factor for the CNTs to be in the forefront of the current research is that the fabrication of CNT based transistor is compatible with the existing CMOS fabrication facilities. High performance carbon nanotube field effect transistors (CNFETs) of both n- and p-type using individual CNTs have been demonstrated. Many digital and few analog circuits have been successfully fabricated and have exhibited better performances compared to the CMOS counterparts. Because of the challenges in the synthesis of CNTs and in the scaling up of individual CNT based devices, researchers have developed thin-films of CNTs and transistors based on them. CNT thin-film transistors (CNTFTs) have shown a high carrier mobility compared to the conventional TFTs based on organic materials and amorphous silicon. The deposition of high density CNT thin-film, use of high-k dielectric material and wafer scale fabrication are the major challenges to realize high performance CNTFTs.

This chapter is organized as follows. Section 1.2 deals with basics of the CNTs. In section 1.3, a review of CNTs for interconnect application is presented. The modeling of CNFETs is discussed in section 1.4 and the fabrication of CNT based transistors is presented in section 1.5. The section 1.6 presents the motivation for various topics investigated in this thesis. The organization of the thesis is given in section 1.7 and finally section 1.8 summarizes the chapter.

1.2 Basics of Carbon Nanotube

Carbon is the sixth element of the periodic table and its six electrons occupy $1s^2$, $2s^2$, and $2p^2$ atomic orbitals. Hybridization i.e. mixing phenomenon of 2s and 2p atomic orbitals is more in carbon because the energy difference between the 2s and 2p level is small compared to the binding energy

TH-1861_07610208

of the chemical bonds. The three possible hybridizations of the carbon are sp, sp^2 and sp^3. Three outer-shell electrons of each carbon atom occupy the planar sp^2 hybrid orbital to form three in-plane σ bonds with an out-of-plane π orbital (bond). This makes a planar hexagonal network. CNTs can be viewed as a hollow cylinder formed by rolling graphite sheets and are classified as single walled carbon nanotube (SWCNT) and multi walled carbon nanotube (MWCNT), depending on the number of sheets. The SWCNTs are categorized as metallic (m-SWCNT) and semiconducting (s-SWCNT) depending on the chirality of rolling. The circular curvature will cause quantum confinement and σ-π rehybridization in which three σ bonds are slightly out of plane. For compensation, the π orbital is more delocalized outside the nanotube. This makes SWCNTs mechanically stronger, electrically and thermally more conductive, and chemically and biologically more active than graphite [2].

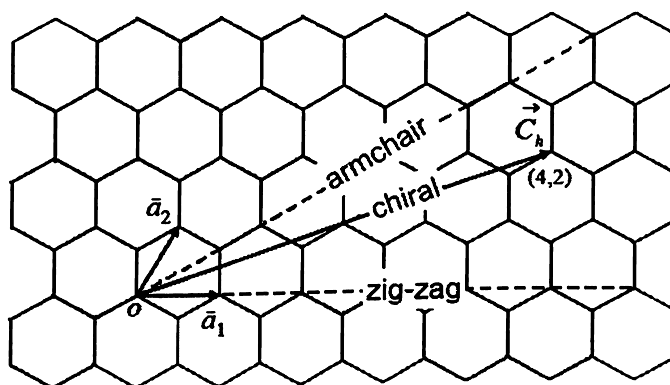

Figure 1.1: The two dimensional graphene sheet, showing the lattice vectors and possible rolling orientation to form different types of carbon nanotubes.

SWCNT can be uniquely represented by a vector **C** in terms of a set of two integers (n, m) corresponding to graphite vectors $\mathbf{a}_1$ and $\mathbf{a}_2$ Fig. 1.1 [3],

$$C = n\mathbf{a}_1 + m\mathbf{a}_2 \tag{1.1}$$

The SWCNT is constructed by rolling up the sheet such that the two end-points of the vector **C** are superimposed. This nanotube is denoted as (n, m) nanotube with diameter given by

$$D_{CNT} = \frac{a\sqrt{n^2 + m^2 + nm}}{\pi} \tag{1.2}$$

where $a = |a_1| = |a_2|$ is the lattice constant of graphite. The SWCNTs with $n = m$ are commonly

TH-1861_07610208

referred to as armchair SWCNTs and $m=0$ as zigzag SWCNTs. Others are called chiral SWCNTs in agreement with the chiral angle, θ, defined as that between the vector **C** and the zigzag direction a_1, $\theta = \tan^{-1}[3^{1/2}m/(m+2n)]$, θ ranges from 0 for zigzag ($m=0$) and 30° for armchair ($m=n$) SWCNTs. Different SWCNTs are distinguished by their chirality and are described by the nanotube chiral vectors (n_1 and n_2). The integer values of n_1 and n_2 will affect the conductance, density and lattice structure of the SWCNT. The conducting characteristics of the SWCNT is considered as metallic if (n_1-n_2) is divisible by 3, otherwise it is semiconducting. Typically, the as-grown SWCNTs consists of 33% m-SWCNTs and the remaining will be semiconducting. The diameter of the SWCNT is ranging from 0.4 to 3 nm.

SWCNTs possess many remarkable properties. Some of the important properties are as follows. The defect-free CNTs have long mean free paths of for phonons (~1.5 μm [4,5]) and electron transport (~ 1 μm [6,7]). Long mean free paths of the electrons makes the CNTs excellent 1D materials. The ballistic transport has been observed in up to micron long metallic [6,7] as well as s-SWCNTs [7]. The current densities as high as 10^9A/cm^2 have been observed in both m- [8] and s-SWCNTs [9]. The SWCNT is as stiff as or stiffer than diamond with the highest Young's modulus and tensile strength. The Young's modulus of SWCNTs along the axial direction has been reported to be as high as 2 TPa (compare with 200 GPa value of steel). Theoretical calculations and experimental measurements showed that the thermal conductivity for a SWCNT at room temperature could vary between 1800 and 6000 W/mK as compare to 385 W/mK for copper (Cu).

Since all the atoms in a CNT are on the surface, they are free to interact with the environment. The absence of any dangling bonds makes CNTs stable at high temperatures. The substitutional doping with boron (B) and nitrogen (N) dopants was pursued to make SWCNTs p- and n-type, respectively. Additionally, molecular adsorption provides a simple, non-covalent doping approach to turn SWCNTs into p-type with oxygen or water adsorption or n-type with C_6H_{12}.

1.3 Carbon Nanotube Interconnects

The most advanced integrated circuits consist of several millions of transistors, interconnected by kilometers of Cu wires within 1 cm^2 silicon chip. Increasing resistivity of Cu with scaling and rising demands on-current density requirements are driving the need to identify new wiring solutions for deep nanometer scale VLSI technologies. The m-SWCNTs have aroused a lot of research interest

TH-1861_07610208

in their applicability as VLSI interconnects due to their desirable properties such as high mechanical and thermal stability, high thermal conductivity and large current carrying capacity [10]. An isolated CNT can carry current densities in excess of 10^9 A/cm^2 without any signs of damage even at an elevated temperature of 250°C [11], thereby eliminating electromigration reliability concerns that plague Cu interconnects. The model developed by P. J. Burke [11] for electrical properties of the CNTs working up to gigahertz (GHz) is useful in evaluating the performance of CNT interconnects. The first comparison between Cu and CNT interconnects were reported by K. Roy et al. [12] and J. D. Meindl et al. [13]. Performance modeling of the CNT bundles as a global interconnect was reported by Saraswat et al. [14]. Naeemi and Meindl proposed that an optimally customized SWCNT interconnects at local, semiglobal and global levels and achieved a significant improvements in power dissipation, propagation delay, crosstalk and bandwidth density [15]. Massoud et al. [16] have evaluated the impact of resistance in the CNT bundles for VLSI interconnects. A suitable CNT interconnect model for the circuit simulation was suggested by K. Roy et al. [17]. Nieuwoudt et al. [18] and Kreupl et al. [19] have suggested that on-chip vias are the prime candidates for the use of CNT bundles as the current carrying limit of the small dimension Cu interconnect is severely limited. Banerjee et al. [20] have studied the insertion of buffers (repeaters) to drive signals faster and more than 20% of power can be saved using the CNT global interconnects, as the number and size of the repeaters are considerably reduced. Gael et al. [21] have demonstrated that CNT interconnects can transmit GHz digital signals between the transistors. The conductance of a SWCNT is evaluated using the two-terminal Landauer-Buttiker formula. An important consideration for the conductance in SWCNTs is its dependence on the bias voltage. At high electric fields, the current through a SWCNT saturates. The consideration of magnetic inductance of SWCNTs is important not only in the study of the interconnects, but also for their potential applications as a passive inductor [22].

1.4 Modeling of Carbon Nanotube Transistors

Having considered the applications of m-SWCNTs, the application of s-SWCNTs as FETs is presented. The s-SWCNTs with near ballistic transport nature and very high aspect ratio are used as the channel material to realize the devices of few nanometer dimensions without second order effects. A review on the modeling of CNFET is presented here. Endued with properties such as ballistic transport with a long mean free path (about 1 μm), high band gap and extraordinarily

TH-1861_07610208

high mobility (100,000 $cm^2/V{\cdot}s$) [23], s-SWCNTs offer enormous potential for realizing an electronic device such as FET both as an alternative to silicon technology beyond the conventional scaling limits and as a way to implement high-speed devices and circuits on the flexible substrates. The device modeling is essential in order to address the design and automation aspects in the rapidly developing field of carbon nanotube electronics. A model is necessary to theoretically analyze the CNFET and it should be simple, compact and preferably an analytical one for analyzing the circuit performance using the device. For circuit simulation using the conventional simulation program with integrated circuit emphasis (SPICE) simulators, one need an analytical expression for the device e.g. *I-V* and *C-V* characteristics in terms of the applied terminal voltage such as V_{DS} and V_{GS}. The electrical transport properties of SWCNTs have been studied and observed that the conductance of a nanotube is quantized, and the SWCNT acts as a ballistic conductor. It is almost impossible to obtain an exact closed-form expression leading to an analytical *I-V* characteristics with respect to the terminal voltages due to the complex non-linear simultaneous nature of equations. As a result, most developed physical device models use the numerical techniques to obtain the device characteristics, where the reference point is the surface potential, not the terminal potential such as V_G, V_D and V_S.

CNFETs are classified into two categories, based on their mechanism of operation - Schottky Barrier (SB) controlled CNFETs (SB-CNFETs) and MOSFET-like CNFETs. Arash Hazeghi et al. [24] proposed a SPICE compatible model for SB contacted ballistic co-axial CNFET, which reaches self-consistency in four to five iterations. Another model for co-axial SB-CNFET device is proposed by Guo Jing et al. [25], assuming a zero metal/SWCNT contact resistance and ballistic carrier transport for the charge carriers. The effects of reflections at the intersection barrier of source/SWCNT and drain/SWCNT are considered in the model for co-axial SB-CNFET [26]. A scalable, non-iterative and surface-potential model for CNFET is proposed by A. Balijepalli et al. [27]. A SPICE compatible model for CNFET device with multiple number of SWCNTs is proposed by Arijit Raychowdhury et al. [28]. A quasi-analytical circuit compatible model for an intrinsic ballistic CNFET which can be used on any conventional circuit simulators, is reported by B. C. Paul et al. [29]. An analytical model for the CNFET proposed by Deji Akinwande et al. [30] suggests that the CNFET drain current is exponentially related to the gate voltage. The scattering phenomena in SWCNT and the inter tube capacitance effects in the CNFET device are considered in a HSPICE [31]

TH-1861_07610208

compatible model proposed by J. Deng et al. [32].

The conventional CMOS circuit designs are carried out using the closed-form equations based on the device dimensions, so that designer has the flexibility of choosing the device dimensions to meet the design specifications. Then, the circuit designs are verified and optimized using simulation tools. The layouts are drawn and post-layout simulations are performed to verify the circuit design for the specifications and final device fabrication will be based on these layouts. Similarly to realize the electronic circuits using CNFET devices, it is necessary to design the circuit in terms of device dimensions and verify it using the simulation tool before the fabrication.

1.5 Fabrication of Carbon Nanotube Transistors

Nanoelectronics devices have been extensively explored since 1998, with the demonstration of first CNFET [33] and transistors based on individual s-SWCNTs have shown better performance compared to those of state of the art silicon FETs. For example, CNFETs having a subthreshold swing close to the room temperature limit of 60 mV/decade [7], transconductance as large as 30 S [34, 35] and an on-off current ratio of 10^7 [36] have been demonstrated. By utilizing high-k gate dielectric materials, the CNFETs can be operated at a lower gate voltage. High performance CNFETs of both n- and p-type using individual SWCNTs have been demonstrated. Like silicon FETs, CNFETs with individually addressable (i.e. patterned) gate electrodes can be connected into logic circuits. Unfortunately, the fabrication of large scale integrated circuits based on the individual SWCNTs is not yet practical due to the difficulties in synthesis and accurately positioning large numbers of individual, electrically homogeneous SWCNTs. Therefore, current application of the SWCNTs has mostly been limited to the use of bulk SWCNTs, which is a mass of rather unorganized fragments of SWCNTs. The CNTFTs have shown high carrier mobility compared to the conventional TFTs based on organic materials and amorphous silicon. The use of densely packed arrays of SWCNTs as an effective thin-film electronic material has the potential to overcome SWCNT positioning difficulty, while retaining the attractive properties of the individual tubes. The multiple, aligned/random transport pathways in these arrays provide large current outputs with small device-to-device variations in properties, even with the CNTs that individually have widely different transport characteristics. Efforts to deposit SWCNT networks using solution-based assembly techniques have shown significant promise as an alternative technology for large area TFT applications.

TH-1861_07610208

The performance of CNTFTs depends on the nature of the SWCNT thin-film network, purity of the s-SWCNTs and the density of SWCNTs. Many groups have demonstrated CNTFTs using as-grown SWCNTs [37, 38] with better performance compared to the conventional organic TFTs and amorphous silicon TFTs. However, CNTFTs with as-grown SWCNTs exhibited a poor on-off current ratio due to the co-existence of m- and s-SWCNTs. This drawback can be resolved using the pre-separated (sorted) s-SWCNTs [39, 40]. Many groups have developed individual semiconducting nanotube TFTs (SN-TFTs) [41–45], but few groups have fabricated SN-TFTs on a wafer scale [46–49]. The SN-TFTs fabricated using the pre-separated 99% and 95% purity s-SWCNTs [46, 49] have been demonstrated. Most of the SN-TFTs reported in the literature have the thin-film of SWCNTs deposited on the modified SiO_2 surface [37,38,46–49], and a maximum of 32 nanotubes/μm^2 has been reported in [46]. Some of the performance indexes such as high on-off ratio, high mobility, high current density and steeper subthreshold swing are achieved separately in different SN-TFTs. Nevertheless, it is desirable to have an individual SN-TFT to exhibit all these performance parameters so that these devices can be readily used for real applications.

1.6 Motivation and Problem Definition

There are many challenges in the area of SWCNT based interconnects and transistor research and the few important motivations considered for the present work are summarized below.

(i) **Need to study the magnetic inductance of interconnects at various bias voltages**

The bundle of SWCNTs used for the interconnect application has exhibited excellent improvement in the propagation delay, power dissipation, response time, immunity to electromigration and thermal management compared to Cu interconnect. In an integrated circuit, the interconnects provide power supply, ground, clock and control signal to all blocks and will result in a closed path for the current conduction. A magnetic field will be induced in the interconnect because of this closed path nature of the interconnects and not only the study of the magnetic inductance contribution by different dimensions of local, intermediate and global interconnects but also their dependence on the bias voltage are also important.

(ii) **Need of closed-form equation for CNFET in terms of device dimensions**

To realize the electronic circuit using CNFETs, it is first necessary to design the circuit in

TH-1861_07610208

terms of device dimensions and predict its performance using an appropriate simulation tool before the actual fabrication. There are many models proposed in the literature to estimate the performance of CNFETs, but none of them have a closed form expression for the CNFET drain current in terms of its physical and process parameters. Due to the complex nature of equations involved, it is almost impossible to obtain a closed-form physical model at least in the present scenario and therefore, we have considered the curve fitting method to arrive on an equation. The obtained closed-form equation of the drain current in terms of the device dimensions enabled us to optimally design and simulate the analog circuits using the CNFETs and also to compare their performance with the CMOS counterparts.

(iii) **Need of high performance SN-TFTs**

Realizing SN-TFTs that exhibit large transconductance, steep subthreshold swing, lower threshold voltage, higher current density and large on-off ratio simultaneously (i.e. in the same device) remains a significant challenge. We have made efforts to fabricate high performance SN-TFTs using simple fabrication methods and affordable purity of SWCNTs by employing methods to improve the SWCNT density, by judiciously selecting the length of the SWCNTs and by incorporating a high-k dielectric material.

(iv) **Need of performance comparison of various types of SN-TFTs**

A systematic study of different aspects of the SN-TFT performance dependency on factors such as purity of s-SWCNTs, methods of channel control by different gate structure, dielectric constant of the gate material etc. are essential. For a fair comparison, such a study requires many devices of identical dimensions processed under similar conditions. The wafer scale device demonstrations are also important as they provide added information such as repeatability, yield of the process involved and performance variations among the devices across the wafer.

1.7 Organization of the Thesis

The work carried out in this thesis can be divided into three parts. The first part presented the study on SWCNT interconnects, the second part dealt with the modeling of SWCNT transistors and design of analog circuits based on SWCNTs. Finally the third and major part addressed the fabrication and characterization of 9 different thin film transistors based on SWCNTs.

TH-1861_07610208

Chapter 2 presents the magnetic inductance dependency on the bias voltage of SWCNT based interconnects. The simulation study of loop inductance of the interconnect is carried out using the GSG configuration having various dimensions considering different percentage of m-SWCNTs.

Chapter 3 gives the details of equations derived for drain current and drain to source voltage of MOSFET-like CNFET in terms of the device dimensions using curve fitting technique. The simulation results of analog circuits such as common-source amplifier and differential amplifier designed using the proposed equations are presented. The effect of process variations of SWCNT such as diameter, spacing and number of SWCNTs, on the performance of the CNFET based analog circuits are analyzed. The performance of CNFET based circuits are compared with the conventional MOSFET counterparts.

Chapter 4 presents the fabrication process flow of wafer scale thin-film transistors of various channel dimensions using sorted SWCNTs. The SWCNT thin-film is deposited on the silanized oxide surface over a 2 inch silicon wafer. A method to deposit high density SWCNTs over the silanized HfO_X surface is proposed. SWCNTs of 90% and 95 % semiconducting purity are deposited on the modified SiO_2 and HfO_X surface using different techniques. The process flow of wafer scale global back gate SN-TFTs having either interdigitated electrode (IDE) or normal source/drain contacts are discussed. The process flow of local, back, top and dual gate SN-TFTs are presented separately.

Chapter 5 shows the characterization results of the wafer scale global back gate SN-TFTs with SiO_2 or HfO_X dielectric material having IDE contacts for source/drain terminal. The output and transfer characteristics of SN-TFTs are considered for the analysis. The performance such as on-current, on-off current ratio, transconductance, mobility etc. of both types SN-TFTs having identical channel dimensions are compared.

Chapter 6 presents the performance of wafer scale global back gate SN-TFTs having a thin-film of 90% or 95% purity s-SWCNTs. The wafer scale devices having IDE and normal source/drain contacts are considered for the analysis. This chapter presents the high on-current SN-TFTs having 95% s-SWCNTs and their results are compared with similar type of devices reported in the literature.

Chapter 7 addresses the performance of a wafer scale local gate SN-TFTs having a thin-film of 95% purity s-SWCNTs deposited on the silanized HfO_X surface. The wafer scale devices having various channel dimensions are considered for the analysis. The performance of local back gate SN-TFTs such as threshold voltage, subthreshold swing, on-off current ratio, current density, mobility

etc. are compared with other reported wafer scale devices having global back and top gate structures. The *C-V* characteristics of local gate SN-TFTs are also presented.

Chapter 8 deals the performance of three different SN-TFTs with top or bottom or dual gate structure and having a thin-film of 95% enriched s-SWCNTs deposited on the silanized HfO_x surface. The performance these devices are compared by measuring the parameters such as subthreshold swing, threshold voltage and transconductance. Finally, the performance of wafer scale SN-TFTs having global and local gate structure are also compared.

Chapter 9 summarizes the key findings and contributions of this thesis and proposes some directions of future work.

1.8 Summary

In this chapter, a brief summary on the structure, classification and properties of CNTs are presented. A discussion on the use of CNT for the interconnect application is followed by a review on the modeling of CNT based interconnects. The modeling of CNT based transistors and the necessity of the closed-form current/voltage equations based on the device dimensions in order to carry out the design of analog circuits using CNFETs was discussed next. A review on the fabricated CNT based transistors of individual as well as thin-film of SWCNTs are presented subsequently. Finally this chapter is concluded with the motivation for the present work and the organization of the thesis.

TH-1861_07610208

2

Impact of Bias Voltage on Magnetic Inductance of Carbon Nanotube Interconnects

Contents

2.1 Introduction 14
2.2 Modeling of Resistance in an Isolated SWCNT 15
2.3 Modeling of Inductance in SWCNT bundles 16
2.4 Bias Voltage Dependence of Loop Inductance in SWCNT Interconnect . 18
2.5 Simulation Results of Loop Inductance 19
2.6 Summary 23

TH-1861_07610208

2.1 Introduction

The International Technology Roadmap for Semiconductors (ITRS) predicts that the traditional interconnects will be a major performance and reliability bottleneck when feature sizes become smaller [50]. The SWCNT is a graphene roll with a diameter of 0.5 nm to a few nanometers and depending on its chirality, they can be either metallic or semiconducting. The SWCNT is very close to 1D system of electrons that gives rise to many unique electrical and thermal properties. In the literature there many SWCNT interconnects models [14–17] have been proposed. Using theses models the potential use of SWCNTs as global, semi-global and local interconnects and their performance are compared with the conventional Cu interconnects [12,13,19,20]. Some CNT based interconnects are also experimentally demonstrated [21,51,52].

Typically, the inductance is seen as a parasitic component in the metal interconnects. In analog VLSI integrated circuit (IC) design, inductor is one of the major components. Passive inductors using the SWCNT bundles are reported [22] to have high quality factor and high inductance compared to the metal inductors. Since the radius of SWCNT is several nanometers, the magnetic field (H) induced by the current in SWCNT is about one thousand times larger than that induced by the current in the Cu wire whose radius is about several micrometers. In this chapter, we have investigated the loop inductance of SWCNT interconnect and its dependency on the bias voltage. To the best of our knowledge there has been no work addressing the inductance variation with respect to the bias voltage. The SWCNTs will be incorporated in future ICs and the voltage levels across the SWCNTs will be varying due to clock switching and data transitions. This study is relevant to the cases in which inductance is considered as a parasitic as well as a passive device element. In both cases, a change in the inductances of SWCNTs will definitely affect the circuit functionality and its performance. An assessment of nature and quantity of the inductance variation will be pertinent. The sections of this chapter are as follows. Section 2.2, briefly describe the modeling of SWCNT resistance which is essential to appreciate the variation of the inductance of SWCNT bundles. In section 2.3, the modeling of inductance of SWCNT is discussed. Section 2.4 discusses the effect of bias voltage on the inductance. The simulation results of SWCNT interconnect at different bias voltage are analyzed in section 2.5 and finally chapter is concluded in section 2.6.

TH-1861_07610208

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2.2 Modeling of Resistance in an Isolated SWCNT

Intrinsic resistance, contact resistance and ohmic resistance are the three different resistances associated with an SWCNT and are discussed below.

2.2.1 Intrinsic Resistance (R_i)

The conductance of a SWCNT is evaluated using the two-terminal Landauer-Buttiker formula. This formula states that, for a 1D system with N channels in parallel, the conductance $G = (Ne^2/h)T$, where T is the transmission coefficient for electrons through the sample, h is the Planck's constant and e is the charge of an electron. Due to the spin degeneracy and sub lattice degeneracy of electrons in graphene, each nanotube has four conducting channels in parallel ($N = 4$). Hence the conductance of a single ballistic SWCNT assuming perfect contacts ($T = 1$), is given by $(4e^2/h) = 155\ \mu S$ which results in a resistance of 6.45 KΩ. This is the intrinsic resistance (R_i) associated with an SWCNT that cannot be avoided [16]. Therefore, every individual SWCNT will have a minimum resistance (R_i) regardless of its length. The intrinsic resistance of a SWCNT is expressed as

$$R_i = \frac{h}{4e^2} \tag{2.1}$$

2.2.2 Contact Resistance (R_c)

The contact resistance (R_c) is to represent the imperfect contact between the metal and the SWCNTs. As the SWCNT fabrication and bonding techniques have improved, the additional resistance due to imperfect metal contacts has been significantly reduced and in several experimental cases has approached zero ohm [53]. In this chapter R_c value is assumed as zero.

2.2.3 Ohmic Resistance (R_o)

Electrons moving along a SWCNT can get scattered by defects and also by phonons, and their mean free path lengths (MFP) are finite. Therefore SWCNT resistance is a function of length. The ohmic resistance (R_o) of an SWCNT is defined as

$$R_o = \frac{hl_b}{4e^2\lambda_{ap}} \tag{2.2}$$

where l_b is the length of the nanotube, and λ_{ap} is the mean free path for acoustic phonon scattering [16]. Experimental evidence and theoretical formulations have demonstrated that λ_{ap} depends on

TH-1861_07610208

the diameter of the SWCNT [54, 55]. The typical value of the λ_{ap} ranges in few micro meters. The resistance of an individual SWCNT also depends on the applied bias voltage (V_{bias}) [16]. The SWCNT resistance at low bias voltages (V_{bias}< 0.1 Volt) depends on the values of R_c, R_i and R_o. The value of R_o, which is a function of SWCNT length is negligible compared to the value of R_i for nanotubes of length less than λ_{ap}. Similarly, for longer length SWCNT, the value of R_i is negligible compared to the value of R_o. Therefore the resistance of a SWCNT at low bias voltage for different lengths with respect to λ_{ap} are given below.

$$R_{low} = R_i + R_c \quad if \;\; l_b < \lambda_{ap} \tag{2.3}$$

$$R_{low} = R_o + R_c \quad if \;\; l_b > \lambda_{ap} \tag{2.4}$$

The resistance of an individual SWCNT at high bias voltages (V_{bias} > 0.1 Volt) is expressed in terms of R_{low} and the bias voltage [16]. The expression for the SWCNT resistance at high bias (R_{high}) is given below.

$$R_{high} = R_{low} + \frac{V_{bias}}{I_o} \tag{2.5}$$

where I_o is the maximum current that can flow through an individual nanotube, which is approximately 20-25 μA [56]. The R_{high} will be dependent on the length of the SWCNT through the term R_{low}.

2.3 Modeling of Inductance in SWCNT bundles

A graphene shell has a magnetic inductance which depends on its distance to return path and other conductors. This magnetic inductance includes both self and mutual inductances. However, quantum wire has a small density of states that gives rise to another kind of inductance called kinetic inductance. Two kinds of inductances associated with the SWCNT are discussed separately below.

2.3.1 Kinetic Inductance (l_k)

In a m-SWCNT, the kinetic inductance (l_k) is dependent on the net sum of the kinetic energy of left and right moving electrons in the nanotube, and, as a result, it is a per unit length quantity [11]. The theoretical expression for kinetic inductance for one quantum channel (l_{kone}) is given by the equation below.

TH-1861_07610208

$$l_{kone} = \frac{h}{2v_f\, e^2} \approx 16\ nH/\mu m \tag{2.6}$$

The Fermi velocity (v_f) for grapheme and CNTs is usually taken as $v_f = 8\times10^5$ m/s. The individual SWCNTs have two propagating channels due to the band structure of carbon with spin up or spin down electrons, which results in a total of four channels per nanotube. Therefore, the kinetic inductance (l_k) of an individual SWCNT is given by $l_k = l_{kone}/4 = 4$ nH/μm [11].

2.3.2 Magnetic Inductance

The magnetic inductance captures the impact of voltage induced by the magnetic fields produced by time varying currents, which is encapsulated in Ampere's and Faraday's laws [57]. Resistance, capacitance and kinetic inductance which are per unit length quantities at frequencies where magnetoquasistatic assumptions are valid, but the magnetic inductance is dependent on the entire current loop, which typically consists of a signal line and its associated ground return paths [58]. Since the distribution of the current in the loop may not be known a priori, the concept of partial inductance is used to model [59] the magnetic inductance.

The partial inductance is a mathematical construct that assumes that the current in a particular conductor in the case of partial self-inductance, or the current flowing in adjacent conductors in the case of partial mutual inductance, has a current return path at infinity. The partial inductance construct has no physical meaning by itself. However, when the partial self and mutual inductances are combined in a particular manner over an entire current loop, the total loop inductance is enhanced [60].

The partial self-inductance (L_m) of a SWCNT and the mutual inductance (M_m) between two parallel current carrying SWCNTs of the length l_b and diameter d can be calculated using equations below [61].

$$L_m = 200\ l_b \left(\ln \frac{l_b}{d} + 0.5 + \frac{2d}{3l_b} \right) \tag{2.7}$$

$$M_m = 200\ l_b \left(\ln \left(r + \sqrt{1+r^2} \right) - \sqrt{1 + \left(\frac{1}{r}\right)^2} + \frac{1}{r} \right) \tag{2.8}$$

where $r = l_b/s$ and s is the spacing between the two nanotubes. To model the magnetic inductance of SWCNT bundles, the equivalent width model [18] is utilized, in which the discrete SWCNTs in

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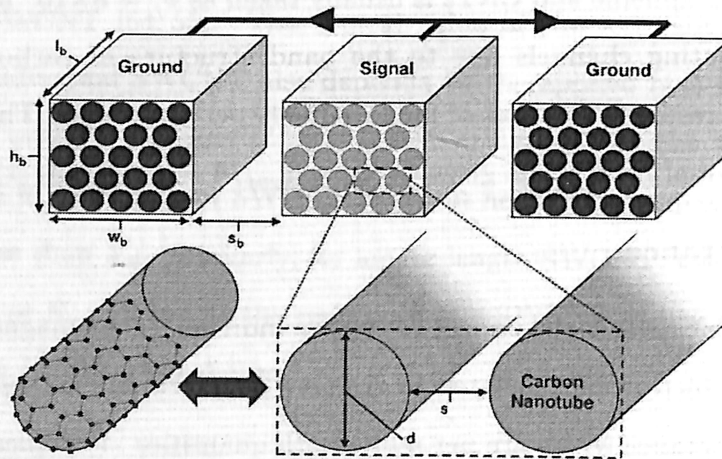

Figure 2.1: GSG configuration of the SWCNT interconnect bundles implementing a signal line and two adjacent ground return paths.

the bundle are replaced by a smaller number of conductors with same resistivity as that of ohmic resistivity of an individual nanotube ρ_t. Using this model the magnetic inductance of a SWCNT bundle can be effectively extracted.

2.4 Bias Voltage Dependence of Loop Inductance in SWCNT Interconnect

The effect of high bias voltage (V_{bias} > 0.1 Volt) particularly on the inductance performance of the SWCNT based interconnect is analyzed in this study. To analyze this, an interconnect configuration with a signal line sandwiched between two ground return paths as shown in Fig. 2.1 which is commonly referred as ground-signal-ground (GSG) is considered. Different dimensions of the SWCNT bundles in the GSG structure are, l_b is the length of the interconnect, w_b is the bundle width, h_b is the bundle height, s_b is the edge to edge spacing between bundles and d is the SWCNT diameter and d of 1 nm is assumed in the analysis.

At high bias voltage (V_{bias} > 0.1 Volt), the resistance of the SWCNT is a function of the bias voltage as in equation (2.5). The SWCNT bundle resistance is also a function of the bundle length as in equation (2.2). So at high bias, the current nonlinearly varies with the supply voltage. This property of SWCNT bundle may be exploited to change the loop inductance value of GSG configuration. In conventional Cu interconnects the current linearly varies with the bias voltage.

To model the magnetic inductance of the GSG configuration, each SWCNT bundle is represented

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by an equivalent conductor with a resistivity same as that of an individual SWCNT at low bias. At different bias voltages the width and height of the equivalent conductor are adjusted to equate the resistance of equivalent conductor to that of the SWCNT bundle, as in the equivalent width model [18]. The loop inductance of the conductor representing the SWCNT bundle [18] is given by the expression below.

$$L_{loop} = I^T L_{mat} I \tag{2.9}$$

$$L_{mat} = \begin{bmatrix} L_{m1} & M_{m12} & \cdots & M_{m1n} \\ M_{m21} & L_{m2} & & M_{m2n} \\ \vdots & & \ddots & \\ M_{mn1} & M_{mn2} & & L_{mn} \end{bmatrix} \tag{2.10}$$

where I is a vector (2.10) with normalized current in each nanotube and L_{mat} is the partial inductance matrix which is constructed from the partial self and mutual inductances for all n number of SWCNTs in the GSG interconnect configuration.

The size of L_{mat} is proportional to the number of SWCNTs in the bundle. For a low complexity system of SWCNT bundles, equation (2.10) can be used directly to calculate the loop magnetic inductance. However, to evaluate the loop inductance over a wide range of geometries, "FastHenry" a version of multipole-accelerated field solver, which uses a partial element equivalent circuit (PEEC) formulation similar to the equation (2.10) is used in this study.

2.5 Simulation Results of Loop Inductance

The loop inductance of GSG configuration is estimated using FastHenry a simulator available in public domain. The SWCNTs are incorporated as a conductor by modifying its resistivity equivalent to that of SWCNTs. The w_b and h_b of the conductor at different bias voltages (0.1V to 1V) are calculated by equating resistance of the SWCNT bundle and equivalent conductor, as in the equivalent width model [18]. We simulated about 1000 GSG configuration of the SWCNT bundles with the following geometric parameters; 10 μm $\leq l_b \leq$ 1000, μm, $10d \leq w_b \leq 20d$ and $0.1w_b \leq s_b \leq 10w_b$. The as-grown bundle of SWCNTs contain about 33% m-SWCNTs and the rest is semiconducting, but using sorting process it is possible to obtain higher percentage of m-SWCNTs. Therefore in this study, the probability P_m that a given SWCNT in the bundle is metallic is varied from 0.33 to 1.

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During the simulation of GSG structure each conductor is represented by 4 filaments to reduce the simulation time without compromising in the value of the estimated loop inductance.

The loop inductance of interconnect in GSG configuration for different length at various bias voltages is shown in Fig. 2.2. It is noticeable in Fig. 2.2(a) that there is a variation in the loop inductance for a shorter length interconnect (10 μm) as the bias voltage changes from 0.1 V to 1 V. The increment in the loop inductance for the bias voltage increase is constant irrespective of the P_m value. However, the variation in loop inductance of a longer length interconnect (1000 μm) for various bias voltage is negligible as shown in Fig. 2.2(b). The value of loop inductance is proportional to the length of the interconnect line as per equations (2.7 - 2.9).

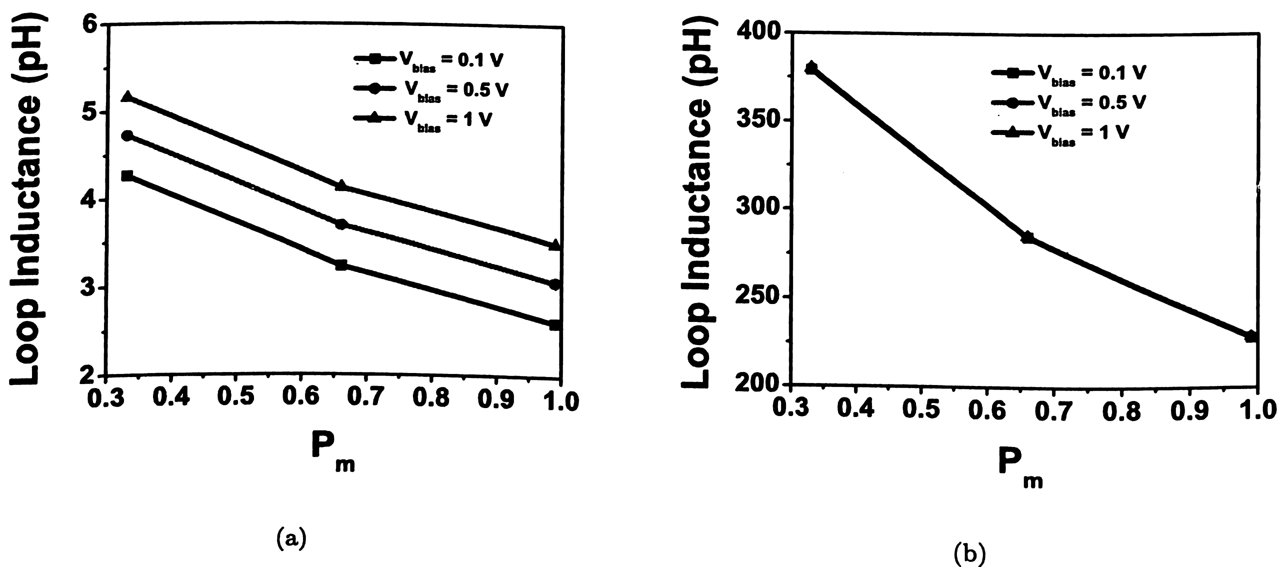

Figure 2.2: Loop inductance at different bias voltages for a GSG configuration with $w_b = h_b = 10$ nm. (a) For a length of 10 μm. (b) For a length of 1000 μm.

A common observation in both the short and long interconnects is that the loop inductance decreases as the P_m value increases from 0.33 to 1 (as-grown SWCNTs to 100% m-SWCNTs). For a given bias voltage, the variations in loop inductance with respect to P_m is 45% for an interconnect of length 10 μm and it is 70% when the length is of 1000 μm. This large variation in the inductance value due to the metallic content in the SWCNT bundle is to be considered while using the SWCNTs for analog circuit applications. That means, if the SWCNT interconnect line is a part of the analog tuned circuit, then the change in the P_m value of the SWCNT bundle may considerably affect tuning of the circuit. Therefore, it is essential to have good control over the chirality during synthesis of

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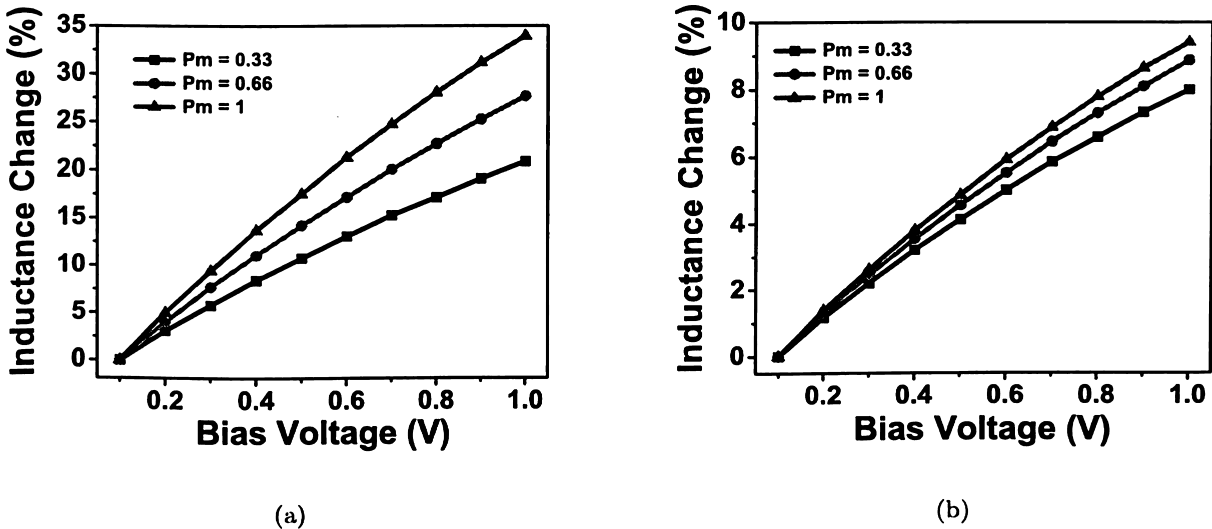
SWCNT, to use them in analog circuit applications. However, it has been reported that there will be no change in the capacitance of the SWCNT bundle even if the percentage of m-SWCNTs in the bundle changes [15].



(a) (b)

Figure 2.3: Percentage change in loop inductance of a GSG configuration of length 10 μm and $w_b = h_b =$ 10 nm. (a) For a separation of 1 nm. (b) For a separation of 100 nm.

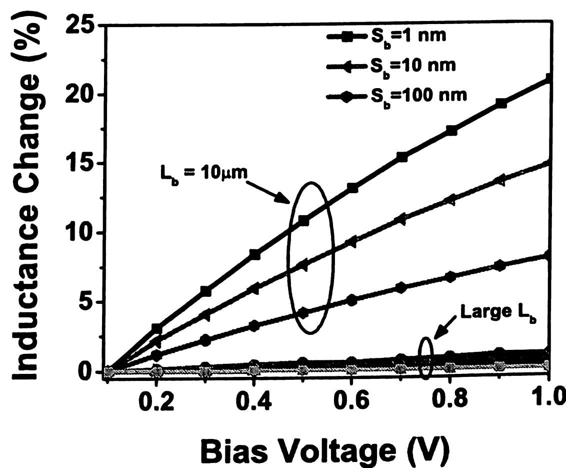


Figure 2.4: Change in loop inductance as a function of V_{bias} for a constant P_m of 0.33 for interconnects having different lengths and spacing.

Fig. 2.3 shows percentage change in the loop inductance as a function bias voltage of an interconnect having a length of 10 μm and $w_b = h_b = 10$ nm, but with different s_b and P_m values. Fig. 2.3(a) shows variation in the loop inductance at various bias voltage for a s_b of 1 nm is 34% and 21%

TH-1861_07610208

for P_m of 1 and 0.33, respectively. Similarly, for a GSG configuration with s_b of 100 nm, variation in the loop inductance is 9.5% and 8% for a P_m of 1 and 0.33, respectively with respect to given V_{bias} change. This shows that as the separation increases, variations in the loop inductance with respect to bias voltage decreases. The change in the loop inductance with respect to V_{bias} is minimized for large values of s_b and is valid for other dimension of width and height ($w_b = h_b$) also. The above analysis is extended to different lengths and same is plotted in Fig. 2.4.

The variations in loop inductance for various bias voltages of a SWCNT interconnect at a constant P_m of 0.33, with different length and separation is shown in Fig. 2.4. The interconnects of lengths 10, 200, 600, 1000 μm, s_b of 1, 10, 100 nm and $w_b = h_b = 10$ nm are considered for the analysis. The loop inductance variation is 21%, 14% and 8% for s_b of 1, 10 and 100 nm, respectively for a line with length 10 μm. However, for longer lengths, the variation in inductance for various bias voltage is less than 1%. Therefore, the loop inductance variation at different bias voltage is critical for intermediate interconnects. Typically for local interconnects SWCNTs are not used because of their high intrinsic resistance and Cu is preferred for such cases.

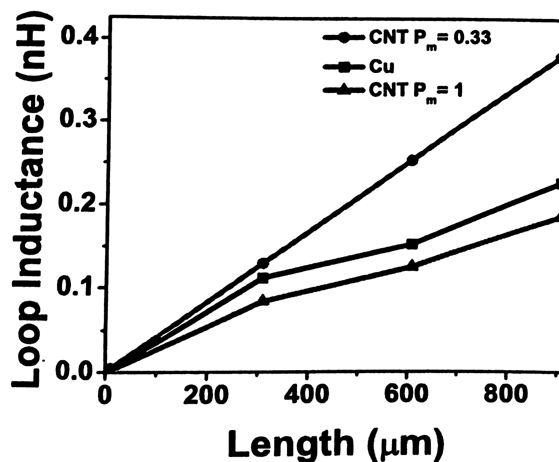


Figure 2.5: Comparison of loop inductance of copper and SWCNT bundles for different lengths and P_m values.

Fig. 2.5 shows the loop inductance exhibited by interconnects of Cu and CNTs of different P_m value. The loop inductance of GSG configurations of Cu is obtained using FastHenry. While calculating the resistivity of Cu, the surface scattering and the scattering due to grain boundary are also considered. Fig. 2.5 shows a large deviation in the loop inductance between the Cu and

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SWCNT especially for lower P_m. Even though the loop inductance of SWCNT is more, at nanometer dimensions SWCNT is preferred over Cu, because Cu resistance is very large compared to SWCNT. For interconnect applications SWCNTs having rich metallic property is preferred.

2.6 Summary

In this chapter the modeling of various resistances and inductances associated with the SWCNT was presented. The impact of bias voltage on the loop inductance of SWCNT bundle was evaluated for various dimensions of the interconnect GSG configuration. The purity of the m-SWCNT was also considered during the analysis. The study shows that the inductance change with respect to bias voltage ranges from 1% to 34% for different interconnect lengths. The highest change in the inductance was for intermediate interconnects of length 10 μm and high P_m values. The SWCNT is a promising candidate to replace the Cu interconnects for intermediate and global interconnects [62] for improving propagation delay, power and bandwidth. There are reports of selective production of long, horizontally aligned SWCNTs (> 1 mm) [63], but the selective and lateral growth of SWCNT is a challenge. It is anticipated that with improved processing technology, the SWCNT will replace existing Cu interconnects and the presented study will be very relevant in such cases.

TH-1861_07610208

3

Design and Simulation of Analog Amplifier Circuits using Carbon Nanotube Field-Effect Transistors

Contents

3.1 Introduction 26
3.2 Simplified Closed-Form Equations for CNFET 29
3.3 Common-Source CNFET Amplifiers 40
3.4 Single-Stage CNFET Differential Amplifier 50
3.5 Summary 52

TH-1861_07610208

3.1 Introduction

For the past many decades, dimensions of the silicon Metal Oxide Semiconductor Field-Effect Transistors (MOSFET) have been shrinking to meet the performance requirements. However, dimension scaling of MOSFET device will reach an ultimate-limit after various innovations like high-k dielectric [64], metal gate [65], Fin FETs [66] and strained FETs [67]. As an alternative, new devices such as single electron transistor [68], resonant tuning devices [69] and CNFET [33] are in the forefront of research activity. Among these new devices, CNFET has shown a greater potential of taking the place of MOSFET device in the post silicon era. A SWCNT exhibits metallic or semiconducting characteristics, which enables it to be used for interconnect or transistor applications, respectively. Due to ballistic transport nature [35], adjustable band gap [70] and very low intrinsic capacitance [71], SWCNTs are highly recommended for high performance circuit applications. Another important factor for the CNFET devices to be in the forefront of current research is that, their fabrication is compatible with the existing CMOS process.

CNFET devices are classified into two categories, based on their mechanism of operation - Schottky Barrier (SB) controlled CNFETs (SB-CNFETs) and MOSFET-like CNFETs. In a SB-CNFET device, the conductivity is governed by the tunneling of majority carriers through the SBs at the end contacts. The conductivity of the device can be modulated electrostatically using the gate voltage by changing height and width of the SB [72] and SB-CNFETs show an am-bipolar transport behavior [73]. However, in MOSFET-like CNFET devices the conductivity is controlled by the gate voltage, which modulates the non-tunneling potential behavior of channel region of the device. The MOSFET-like CNFET device can be made unipolar by suppressing either electron carriers thereby results in p-type or hole carriers which results in n-type transport with heavily-doped source/drain and the doping of SWCNTs can be carried out either electrostatically [74] or chemically [75].

In the last decade, many different types of CNFET devices have been fabricated such as back gate [33], top gate [76] and dual gate [75] and they are fabricated either using individual SWCNTs [7], aligned [46] or random network of SWCNTs [46, 49]. The CNFET based digital circuits like inverter, basic logic gates [77–79] and ring oscillators [80] have been fabricated and have shown better performance compared to the CMOS counterparts. Using the aligned SWCNTs, wafer scale CNFET devices and CNFET based digital integrated circuits are demonstrated by Koungmin Ryu et al. [81]. CNFET analog circuits like common-source amplifier [74] and high-speed analog circuit [82]

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are also demonstrated. A study of high frequency effects on CNFET has been carried out by Pulfrey et al. [83]. Apart from these experimental validations, CNFET based simulation results of digital circuits [84–90] and of an analog inverter [91] are reported.

The behavior of devices can be modeled using analytical expressions based on fundamental physics or by SPICE compatible models which need not generally derived from the underlying physics. Large-signal nonlinear device models may be categorized into two types - physical models and empirical models. Physical models are based upon device physics, and parameters within these models are based upon physical properties such as oxide thicknesses, substrate doping concentrations, carrier mobility, etc. Empirical models are entirely based upon curve fitting and unlike a physical model, the parameters in an empirical model need have no fundamental basis. In the literature physical models for CNFET based on Landauer expression are reported. Arash Hazeghi et al. [24] proposed a SPICE compatible model for SB contacted ballistic co-axial CNFET, which reaches self-consistency in four to five iterations. Another model for a co-axial SB-CNFET device is proposed by Guo Jing et al. [25], assuming a zero metal/SWCNT contact resistance and ballistic carrier transport for charge carriers. The effects of reflections at the intersection barrier of source/SWCNT and drain/SWCNT are considered in the model for co-axial SB-CNFET [26]. A scalable, non-iterative and surface-potential model for CNFET [27] is also proposed. A SPICE compatible model for CNFET with multiple number of SWCNTs is proposed by Arijit Raychowdhury et al. [28]. A quasi-analytical circuit compatible model for an intrinsic ballistic CNFET [29] which can be used on any conventional circuit simulators, is also reported. An analytical model for CNFET proposed by Deji Akinwande et al. [30] shows that the CNFET drain current is exponentially related to the gate voltage. The scattering phenomena in CNT and inter CNT capacitance effects in the CNFET are considered in a HSPICE [31] compatible model for MOSFET-like CNFET proposed by J.Deng et al. [32]. It is almost impossible to obtain an exact closed-form expression leading to an analytical *I-V* characteristics with respect to the terminal voltages due to the complex non-linear simultaneous nature of equations. As a result, most developed physical device models use the numerical techniques to obtain the device characteristics, where the reference point is the surface potential, not the terminal potential such as V_G, V_D and V_S.

The conventional CMOS circuit designs are carried out using the closed-form analytical equations based on the device dimensions, so that the designer has the flexibility of choosing the device

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dimensions to meet the design specifications. Then, the circuit designs are verified and optimized using simulation tools. The layouts are drawn and post-layout simulations are performed to verify the circuit design for the specifications and final device fabrication will be based on these layouts. Similarly to realize the electronic circuits using CNFET devices, it is necessary to design the circuit in terms of device dimensions and verify it using simulation tool before fabrication. As discussed earlier, CNFET has both analytical and SPICE compatible models, among them the MOSFET-like CNFET model [32] proposed by J. Deng et al. is useful in terms of practical implementation. In this model user can specify the dimensions of device such as number, spacing, diameter of the SWCNTs, etc. and some process parameters.

Even though there are many models for CNFET device available in literature, to the best of our knowledge there is no report available comparing the performance of the CNFET analog circuits with that of the MOSFET circuits. One reason for lack of such a study may be due to the non-availability of closed-form expression for the drain current of CNFET in terms of device dimensions. Such expressions are needed at the conceptual stage of circuit design and are useful for quick hand analysis. Without the closed-form current expression in terms of device and process parameters it is difficult to design and optimize the circuit to the required specifications. When one is not sure whether the designed CNFET circuit is optimized, a comparison to the CMOS counterpart cannot be carried out appropriately. Hence an equation for the drain current of CNFET that includes the device dimensions like channel length, SWCNT diameter, spacing, number of SWCNTs, gate voltage and process parameters similar to MOSFET quadratic-form drain current equation is highly desirable. In this chapter, closed-form equations for the drain current and drain to source saturation voltage of the MOSFET-like CNFETs are derived using curve fitting method. These equations are obtained by performing accurate simulations on MOSFET-like CNFET model proposed by J. Deng et al. [32]. Although these proposed models are based on curve fitting method, but they provide a quick first order numerical estimate of drain current and drain to source voltage of the CNFET. Using these closed-form models it is possible to design CNFET based amplifier circuits for the given specifications. The optimized CNFET device dimensions for the desired circuits are estimated for a given specifications by quick hand calculations and later the design is verified by simulation. Subsequently, it is also possible to compare the CNFET circuit's performance with corresponding CMOS circuits.

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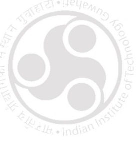

The sections of this chapter are arranged as follows. Section 3.2 discusses the equations for saturated drain current and drain to source saturation voltage of MOSFET-like CNFET. Design of CNFET common-source amplifier and its performance comparison with CMOS counterpart are presented in section 3.3. A single-stage differential amplifier circuit using CNFETs as well as MOSFETs is presented in section 3.4. Finally, section 3.5 summarizes the chapter.

3.2 Simplified Closed-Form Equations for CNFET

In this section, the closed-form equations for drain current and drain to source voltage of the CNFET are discussed. The structure and dimensions of the MOSFET-like CNFET is discussed first. Fig. 3.1 shows the 3D structure of the MOSFET-like CNFET device and related device dimensions. CNFET device consists of one or more s-SWCNTs deposited over the bulk dielectric acting as conducting channel, bridging the source/drain contacts [92]. The gate terminal of device will electrostatically turn on or off the CNFET device through the capacitive control achieved by the gate dielectric. The SWCNTs under the channel region is intrinsic, but the other regions of SWCNT are heavily doped [75, 88]. In this chapter, MOSFET-like CNFET is mentioned a as CNFET unless otherwise specified.

The different dimensions of the CNFET device are shown in Fig. 3.1, where L_{ch} is the channel length, which is the length of undoped SWCNT and lies underneath the gate contact, L_{sd} is the length of doped SWCNT source/drain extension region, N is the number of SWCNTs, S is the separation between SWCNTs (pitch), D_{CNT} is the diameter of the SWCNT, T_{phys} is the physical thickness of gate-oxide and K_{gate} is the dielectric constant of the gate-oxide material.

Next, some important parameters of CNFET model are discussed. The mean free path length (MFP) is a major factor that decides the ballistic or near-ballistic carrier transport property of a SWCNT. The experimentally observed ultra long elastic scattering MFP of SWCNT is 1 μm [35]. However, by considering the effects of optical phonon scattering [93] and acoustic phonon scattering [94] in the SWCNT, MFP of intrinsic SWCNT (L_{ceff}) is chosen as 100 nm [74] and same for p^+/n^+ doped SWCNT (L_{eff}) is 15 nm. To reduce the effect of SB in CNFET device, the work function of SWCNT and metal is chosen as 4.5 eV [95] and 4.6 eV respectively. The relative dielectric constant (K_{bulk}) of the substrate is chosen as 4. To reduce the interconnect parasitic capacitance in the CNFET device an inter-electrode material with relative dielectric constant (K_{lowk}) of value of 2 is

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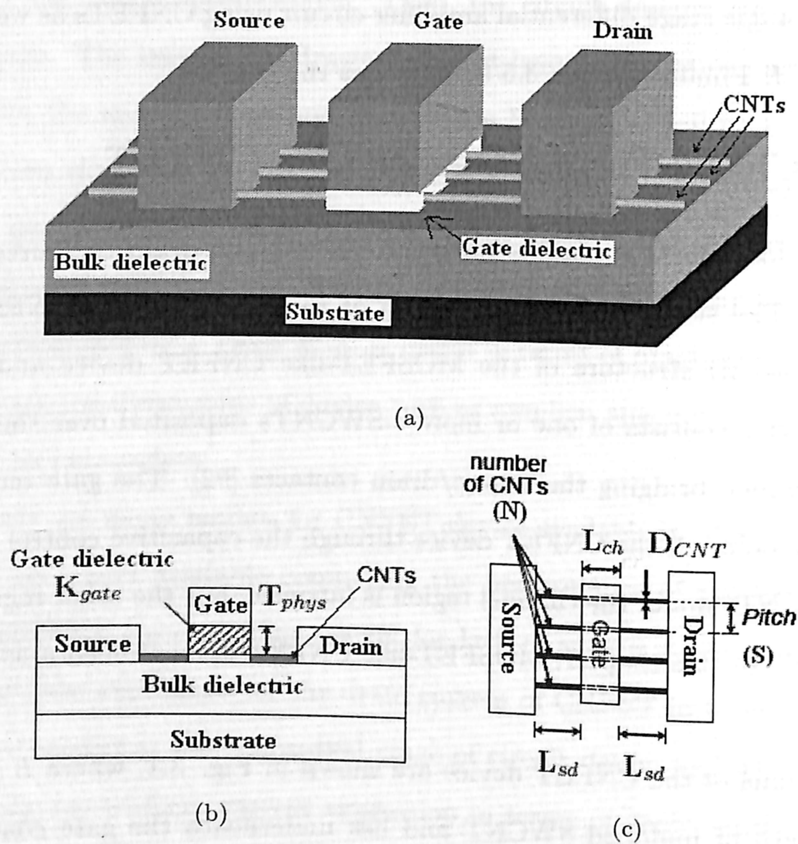

Figure 3.1: (a) The 3D structure of CNFET with multiple channels. (b) Cross sectional view of CNFET indicating different dimensions. (c) Top view of the device.

used. A value of relative dielectric constant of the gate-oxide (K_{gate}) of 16 and physical thickness of gate dielectric layer (T_{phys}) of 10 nm are selected for CNFET device. Other parameters of the CNFET model assumed to have default values mentioned in the data sheet of J. Deng's model [96].

The diameter of the SWCNT is related to the carbon lattice constant (a) and chirality (n_1, n_2) of the SWCNT, as expressed in equation (1.2). In this work, CNFET device is assumed to have only s-SWCNTs as the channel material. The threshold voltage (V_{TO}) is an important parameter which decides the performance of CNFET and is related to the diameter of SWCNT [32] as expressed in the equation (3.1).

$$V_{TO} = \frac{a V_{\pi}}{\sqrt{3}\, e D_{CNT}} \tag{3.1}$$

Where $a = 2.49$ Å, $e =$ electron charge, V_{π} is carbon $\pi - \pi$ bond energy $= 3.033$ eV

Various range of values for different device and voltage parameters used during the simulation are summarized in Table 3.1.

Table 3.1: Typical range of values for different parameters of CNFET device.

Parameter	Range of values	Units
L_{ch}	30 - 100	nm
S	5 - 20	nm
T_{phys}	2 - 10	nm
D_{CNT}	1 - 2	nm
V_{GS}	0.35 - 1.5	V
N	1 - 100	–
K_{gate}	4 - 20	–

3.2.1 Saturation Drain Current Equation

In this subsection, a closed-form equation for the drain current (I_D) of CNFET in terms of the device parameter is presented. The CNFET drain current dependency on different parameters such as V_{GS}, L_{ch}, N, D_{CNT}, S, L_{sd}, T_{phys} and K_{gate} are considered. This is done by carrying out suitable simulations by varying different parameters of the CNFET. Fig. 3.2 summarizes the dependency of I_D on different parameters of the CNFET device. Fig. 3.2(a) shows the dependency of CNFET drain current on V_{GS} for various SWCNT diameters. Fig. 3.2(b) shows effect of the channel length on the I_D at different gate voltages. Fig. 3.2(c) shows that for lower gate voltages, I_D is almost constant for the given range of L_{sd} values. Fig. 3.2(d) shows that the drain current is directly proportional to the SWCNT diameter. Fig. 3.2(e) shows that I_D is affected by the number of SWCNTs substantially. Fig. 3.2(f) shows that the drain current is not affected by spacing of the SWCNTs. The drain current is also a function of the physical thickness (T_{phys}) and the dielectric constant (K_{gate}) of the gate oxide material. The curve fitting method is used to find the influence of each parameter on the saturated drain current of CNFET. Finally, the combined effect of all parameters on the saturated drain current has been computed and is expressed as given below.

$$I_D = C_1 \frac{K_{gate} N D_{CNT}^{1.8} S^{0.2} L_{ch}^{0.18}}{L_{sd}^{0.31} T_{phys}^{0.35}} (V_{GS} - V_{TO})^{1.2} \times 10^{-6} \tag{3.2}$$

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where I_D is in Amps, L_{ch}, L_{sd}, D_{CNT}, S, T_{phys} are in nm. V_{GS} and V_{TO} are in Volts.
C_1 is the curve fitting constant and 1.3 is its value. The unit of C_1 will be such that left side and right side of equation (3.2) is matched unit wise.

Even though the proposed drain current equation of CNFET expressed in equation (3.2) is based on curve fitting method, it gives a good estimation of the drain current for the given device specification. In a special case, CNFET with only one SWCNT as the channel material, the pitch value of 20 nm is used to estimate the drain current. The range of the channel length of CNFET is restricted to 100 nm because the study shows that as the channel length of CNFET increases the I_D increases until L_{ch} reaches 100 nm and saturates for L_{ch} beyond 100 nm [32].

To investigate the accuracy of the proposed equation, the saturated drain current of CNFET estimated by the proposed equation is compared with J. Deng's model [32] over a wide range of different parameter values shown in Table 3.1. The percentage deviation in I_D is calculated using the equation given below.

$$\%\ deviation\ in\ I_D = \frac{(I_D\ of\ proposed\ equation - I_D\ of\ J.\ Deng's\ model)}{I_D\ of\ J.\ Deng's\ model} \times 100$$

The comparisons are grouped into three categories as given below and in all the cases the % deviation in I_D is plotted against D_{CNT}. In the first category, CNFET device dimensions L_{ch} and L_{sd} are maintained constant at 32 nm and % deviation in I_D are obtained by varying parameters like V_{GS}, D_{CNT}, T_{phys}, K_{gate}, S and N over a wide range of values shown in Table 3.1. Fig. 3.3(a) shows the percentage deviation in I_D versus the CNT diameter for the first category. For a particular value of D_{CNT} = 1.03 nm, the drain current obtained by the proposed equation underestimates drain current of the J. Deng's model by -7% with a spread over ±4%. The combined effect of all the above mentioned parameter variations causes the spread over of ±4% around the mean value. In other words, the extreme % deviations in I_D ranges between -3% and -11% for D_{CNT} = 1.03 nm.

In the second category, V_{GS} and L_{sd} are kept at a constant value of 0.55 V and 32 nm, respectively and L_{ch}, D_{CNT}, T_{phys}, K_{gate}, S and N are varied over the range as shown in Table 3.1. The percentage deviation in I_D for the second category are plotted in Fig. 3.3(b). For a particular value of D_{CNT} = 1.34 nm, the CNFET drain current obtained by the proposed equation underestimates the I_D of the

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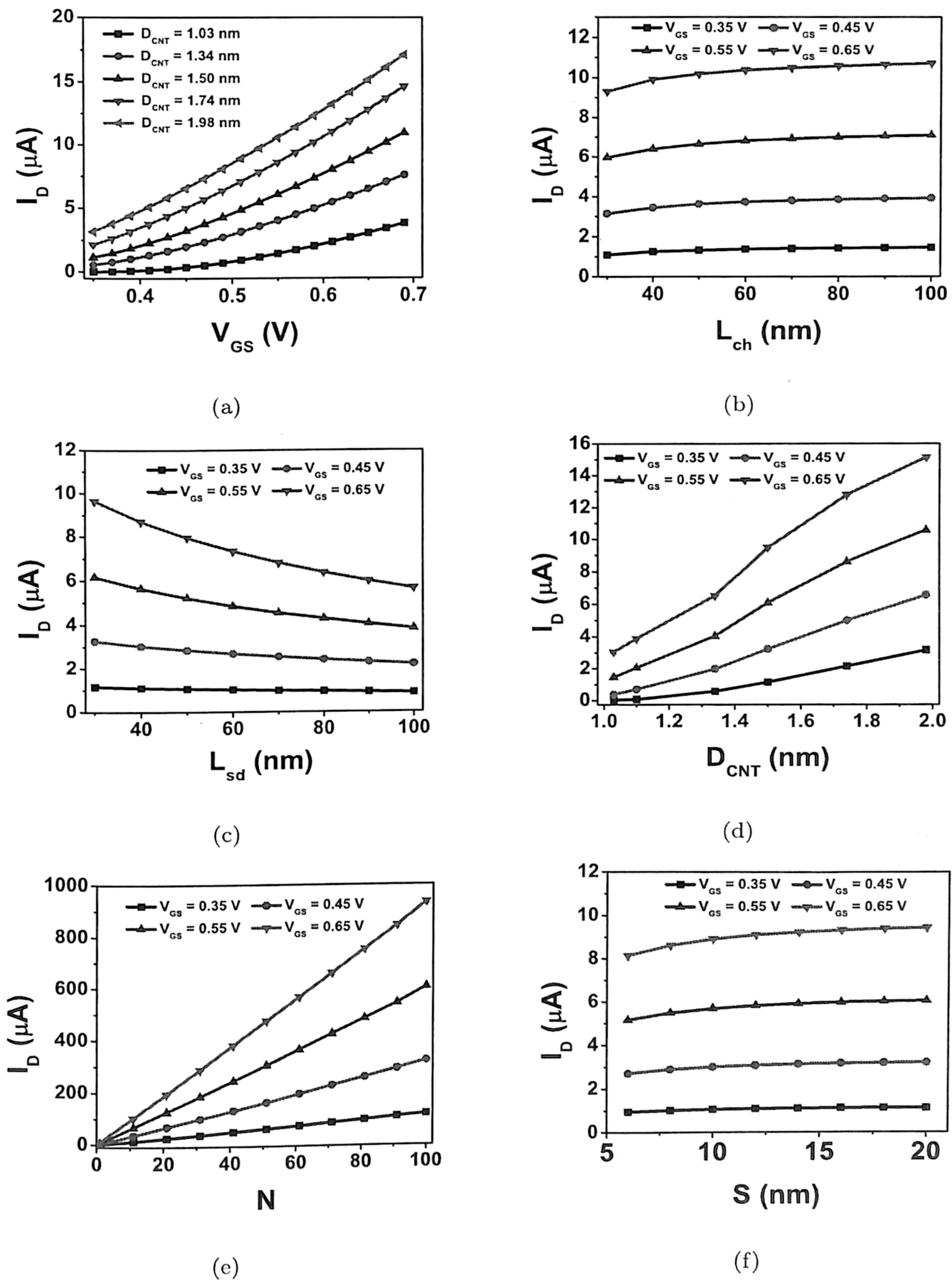

Figure 3.2: Dependency of CNFET drain current on different parameters. (a) shows the V_{GS} effect for different diameter of SWCNTs. For curves (b) to (f) V_{GS} is varied from 0.35 V to 0.65 V. (b) for various channel lengths. (c) for different L_{sd} values. (d) for various SWCNT diameter. (e) as a function of number of SWCNTs and (f) for different spacing between the SWCNTs.

J. Deng's model by - 6.3% and a spread over of ±4.3% resulting in extreme deviations ranging from -2% to -10.6%.

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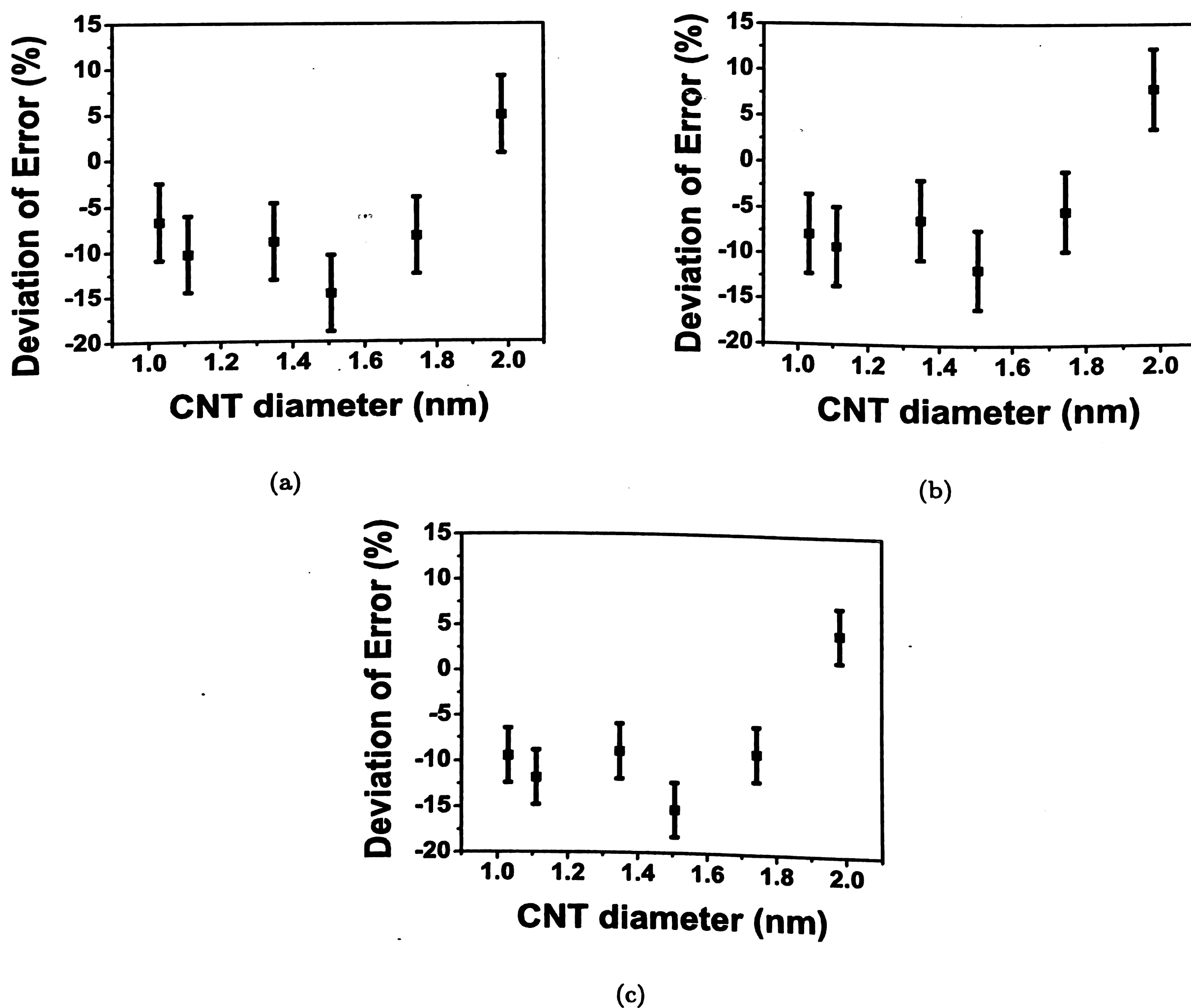

Figure 3.3: Percentage deviation in the proposed equation current compared to J. Deng's model [32] for (a) V_{GS} = 0.55 V, L_{sd} = 32 nm and other parameters are varied within range indicated in Table 3.1 (b) L_{ch} = 32 nm, L_{sd}= 32 nm and other parameters are varied within range indicated in Table 3.1 (c) V_{GS} = 0.55 V, L_{ch} = 32 and other parameters are varied within range indicated in Table 3.1.

In the third category, the CNFET drain current estimation is carried out by varying T_{phys}, K_{gate}, S and N over the range as shown in Table 3.1, L_{sd} is varied from 30 nm to 100 nm, but V_{GS} and L_{ch} are kept at a constant value of 0.55 V and 32 nm, respectively. Fig. 3.3(c) shows the percentage deviation in I_D for the third category. From this error plot, it may be noted that for a particular value of D_{CNT} = 1.98 nm, the proposed equation overestimates the drain current by 4% with a spread over of ±3% causing deviations ranging between 1% and 7%.

Considering all the three categories in Fig. 3.3, the proposed equation (3.2) estimates the drain current within about ±10% when compared to the J. Deng's model for most of the parameter

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variations mentioned in Table 3.1. However, for SWCNT diameter of 1.1 nm and 1.5 nm, the proposed equation underestimates the drain current below 15% and this happens only when the SWCNTs in the device are widely spaced. On the other extreme, as seen in Fig. 3.3(b) for a D_{CNT} of 1.98 nm, the proposed equation overestimates the drain current with a maximum deviation of +13%, again for the widely spaced SWCNTs. In summary, the proposed equation estimates the drain current satisfactorily for most of the device dimensions, gate voltages and process parameters. Therefore using the proposed equation it is possible to estimate the drain current for the given device specifications or conversely estimate the device dimensions of CNFET for the given drain current.

To verify the timing efficiency of the proposed equation, a CNFET device with typical device dimensions, gate voltage and process parameters is considered. To estimate the drain current of CNFET, Matlab is used for the proposed equation and HSPICE for the J. Deng's model. For the fair timing comparison, both Matlab and HSPICE are executed on a Intel Pentium-4 system with the CPU operating at 3.00 GHz on Linux platform. The proposed equation estimated the CNFET drain current in 98 μsec, where as the J. Deng's model estimated the same in 280 msec for the same device parameters. Because of a closed-form nature, the proposed equation estimates the drain current much faster than the J. Deng's model. It is observed that the drain current estimation time of both the models is independent of device dimensions.

The transconductance (g_m) is an important parameter of the active device during the design of analog circuits. The g_m of CNFET is obtained by differentiating the drain current equation with respect to V_{GS} and is given below.

$$g_m = \frac{1.2 I_D}{(V_{GS} - V_{TO})} \tag{3.3}$$

3.2.2 Drain to Source Saturation Voltage Equation

In this subsection, the modeling of drain to source voltage (V_{DSsat}) at which the CNFET drain current saturates is presented. It is one of important parameters of the device that is to be considered during the amplifier design because, the V_{DSsat} value of individual transistor will decide the overall output voltage swing of the amplifier. It is observed that the V_{DSsat} value of the CNFET is not only a function of the voltages V_{GS} and V_{TO}, but also depends on the device dimensions L_{ch} and L_{sd}. The dependency on L_{ch} and L_{sd} is in contrast to the conventional MOSFETs. The dependency of V_{DSsat} on V_{TO} is represented in terms of the SWCNT diameter, because V_{TO} depends on D_{CNT}

TH-1861_07610208

as shown in equation (3.1). The CNFET device dimensions such as number of SWCNTs, L_{sd} and spacing between SWCNTs will not affect the V_{DSsat} value.

The dependency of V_{DSsat} on the channel length of CNFET can be examined from the output characteristics shown in Fig. 3.4 . The variations in V_{DSsat} value with respect to the channel length of short channel CNFET devices is less compared to the variations in V_{DSsat} of the longer channel length CNFET devices. This phenomenon is clearly observed in the output characteristics of the CNFET having channel lengths less than 100 nm in Fig. 3.4(a) and for channel lengths more than 100 nm in Fig. 3.4(b). The CNFET device dimensions considered during the analysis are; L_{sd} = 32 nm, D_{CNT} = 1.5 nm, S = 20 nm, N = 1 and other parameters assumed to have default values mentioned in the users guide [96].

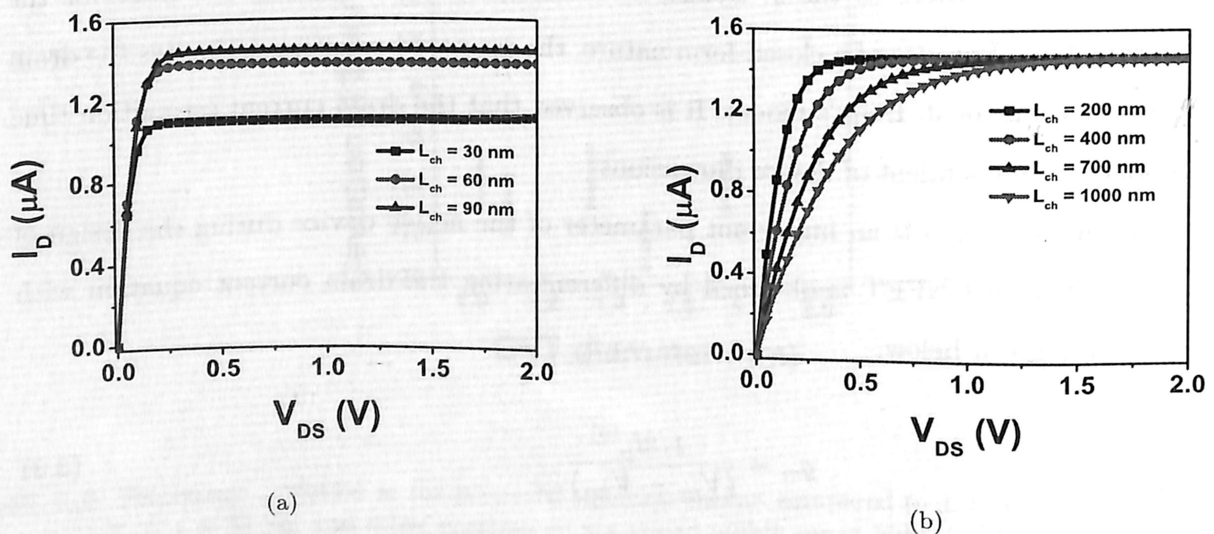

Figure 3.4: *I-V* characteristics of n-type CNFET device obtained by simulating the J. Deng's model [32] for device channel length (a) less than 100 nm (b) more than 100 nm.

The dependency of V_{DSsat} with respect to V_{GS}, L_{ch} and D_{CNT} for both short and long channel CNFETs are shown in Fig. 3.5. Fig. 3.5(a) shows the variations in V_{DSsat} of a short channel (40 nm) CNFET for various SWCNT diameters at various V_{GS} values. The variations in V_{DSsat} value of short channel devices for various D_{CNT} values at a constant V_{GS} of 0.35 V is shown in Fig. 3.5(b). The effect of device channel length on V_{DSsat} for a short channel device for various SWCNT diameter and a constant V_{GS} of 0.35 V are shown in Fig. 3.5(c). Similar to the study of V_{DSsat} variations for short channel CNFET device, the analysis of long channel CNFET device is also considered. Fig. 3.5(d) shows the variations in V_{DSsat} for variation in V_{GS} of a long channel (200 nm) CNFET device

TH-1861_07610208

with different SWCNT diameters. The variations in V_{DSsat} for different SWCNT diameters at a constant V_{GS} of 0.35 V is shown in Fig. 3.5(e). The influence of the channel length on V_{DSsat} for various SWCNT diameter and at constant V_{GS} is shown in Fig. 3.5(f). The curve fitting method was used to find the influence of the parameters on the V_{DSsat} of CNFET. The V_{DSsat} dependency on device parameter is different for short and long channel length CNFETs. Therefore, two different equations for V_{DSsat} are suggested, one for L_{ch} less than 100 nm and the other for L_{ch} more than 100 nm.

The proposed V_{DSsat} equation for L_{ch} less than 100 nm is

$$V_{DSsat} = C_2 V_{GS}^{1.18} L_{ch}^{0.3} D_{CNT}^{0.7} \tag{3.4}$$

The proposed V_{DSsat} equation for L_{ch} greater than 100 nm is

$$V_{DSsat} = C_3 V_{GS}^{0.95} L_{ch}^{0.55} D_{CNT}^{0.45} \tag{3.5}$$

Where V_{GS} and V_{DSsat} are in Volts, L_{ch} and D_{CNT} are in nm. C_2 and C_3 are the curve fitting constants having values 0.172 and 0.55 respectively. The units of C_2 and C_3 will be such that left side and right side of the equations (3.4) and (3.5) is matched unit wise respectively.

Derived expressions for the V_{DSsat} of CNFET shows that the short channel length devices are more dependent on the SWCNT diameter and V_{GS} compared to the longer channel length devices. These V_{DSsat} models are useful in designing the CNFET based analog circuits, because they estimate the voltage drop across CNFET. The accuracy in estimating the V_{DSsat} value of CNFET by the proposed equations (3.4) and (3.5) for various channel lengths, SWCNT diameters and gate voltages are shown in Table 3.2 and 3.3, respectively. The estimated V_{DSsat} value of both equations resemble reasonably well with the simulation results. The maximum deviation of proposed V_{DSsat} equations is within 9% when compared to the J. Deng's model for parameter variations mentioned in Table 3.1. The proposed closed-form equations for the I_D, g_m and V_{DSsat} are applicable for both n- and p-type CNFETs.

The proposed equations for drain current and drain to source saturation voltage of CNFET are validated with the experimental results of MOSFET-like CNFET by Amlani et al. [74]. The devices used for comparison have identical dimensions. Some the parameter values of the device are; MFP of SWCNT is 100 nm, channel length is 700 nm, source and drain length is 400 nm, SWCNT diameter

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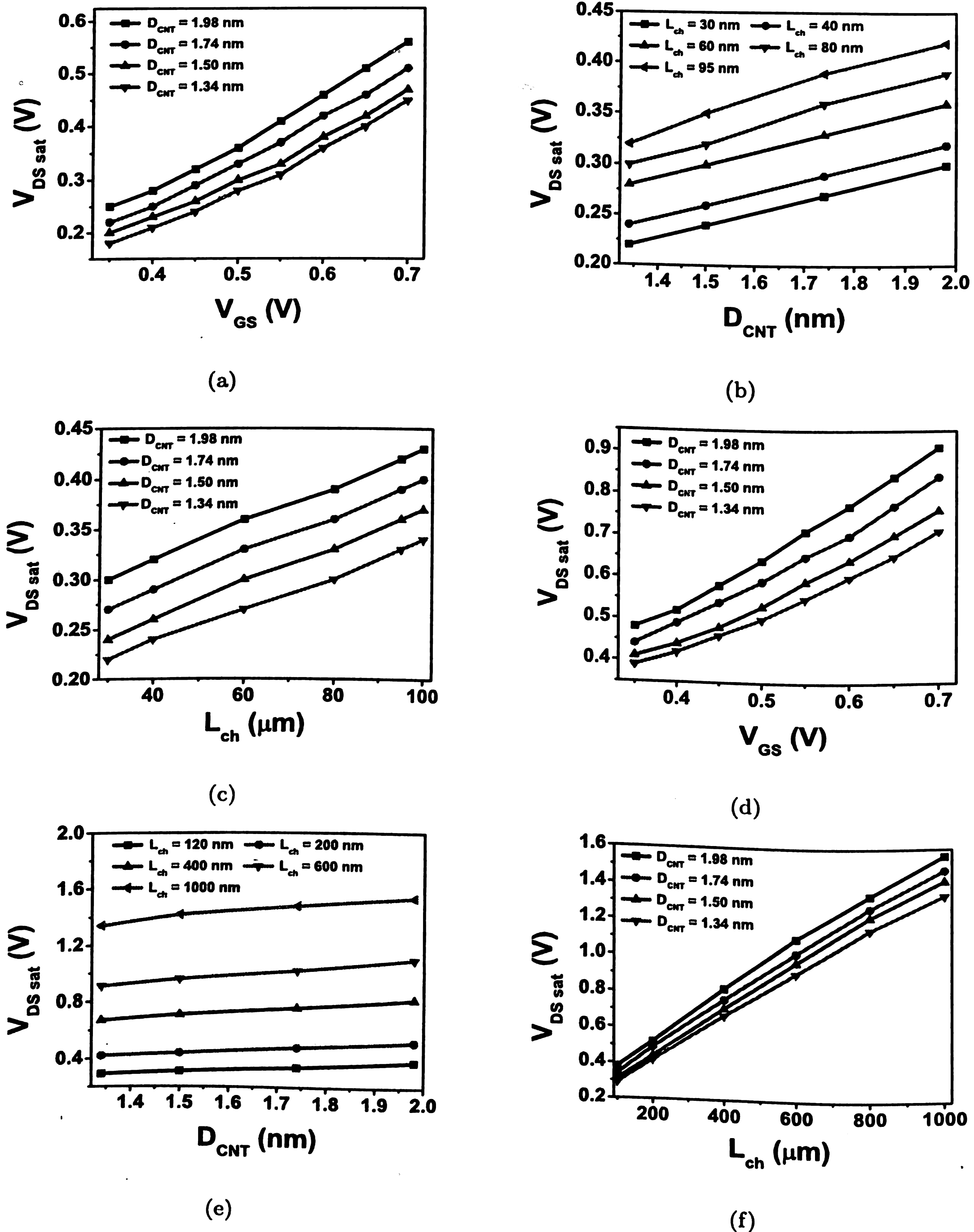

Figure 3.5: Dependency of CNFET drain to source saturation voltage on V_{GS}, L_{ch} and D_{CNT}. (a) shows the V_{GS} effect at a constant channel length of 40 nm for different SWCNT diameters. (b) shows the effect of SWCNT diameter for different channel length at a constant gate voltage of 0.35 V. (c) shows V_{DSsat} variation for different channel length at V_{GS} of 0.35 V for various SWCNT diameter. V_{DSsat} dependency of devices having channel length more than 100 nm for similar parameter variations are shown in (d), (e) and (f).

TH-1861_07610208

Table 3.2: Comparison of V_{DSsat} of CNFET device estimated by the proposed equation (3.4) and the J. Deng's model [32].

L_{ch} (nm)	V_{GS} (V)	D_{CNT} (nm)	V_{DSsat} [Equation 3.4] (V)	V_{DSsat} J. Deng's [32] (V)	Error (%)
30	0.4	1.98	0.29	0.27	6.8
40	0.55	1.5	0.37	0.34	8.1
50	0.35	1.74	0.23	0.24	-4.34
60	0.45	1.34	0.28	0.27	3.57
80	0.6	1.98	0.56	0.54	3.57
100	0.65	1.5	0.54	0.54	0

Table 3.3: Comparison of V_{DSsat} of CNFET device estimated by the proposed equation equation (3.5) and the J. Deng's model [32]

L_{ch} (nm)	V_{GS} (V)	D_{CNT} (nm)	V_{DSsat} [Equation 3.5] (V)	V_{DSsat} J. Deng's [32] (V)	Error (%)
200	0.4	1.98	0.52	0.52	0
400	0.35	1.74	0.69	0.71	-2.89
600	0.45	1.34	0.91	0.97	-6.59
800	0.6	1.98	1.66	1.66	0
1000	0.65	1.5	1.78	1.72	3.37

is 2 nm, gate oxide thickness is 10 nm and dielectric constant is 9. The experimentally measured values of the I_D and the V_{DSsat} are compared with the estimated values by the proposed equations and the simulated results [32]. Fig. 3.6(a) shows the drain current values of CNFET device obtained by the experimental measurement, the simulation results and the proposed analytical equation. It may be noted that the proposed equation (3.2) estimates the I_D value within 10% of tolerance when compared with experimental and simulated values. Similarly, the proposed V_{DSsat} equation of CNFET is validated by experimentally measured and simulated values in Fig. 3.6(b). Similar to the I_D equation, the proposed V_{DSsat} equation also estimates the saturation drain voltage within 10% of tolerance. The other experimental measurement results of MOSFET-like CNFET reported in [34] are considered for validation of the proposed equations, but they could not be compared with the

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proposed equations because of non-availability of the details.

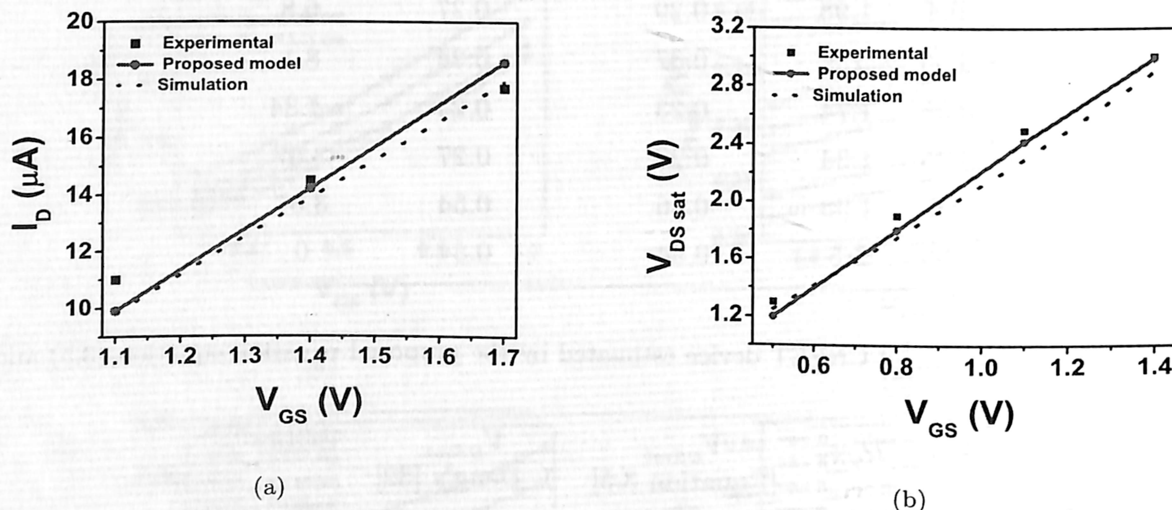

Figure 3.6: Comparison of current and voltage estimated by the proposed equations with the experimental results of Amlani et al. [74] and the simulation results of J. Deng et al. [32]. (a) Drain current for different gate source voltages. (b) V_{DSsat} for different gate source voltages.

The proposed drain current equation and drain to source saturation voltage equations of CNFET are useful in estimating the device dimensions for the design of CNFET analog circuits. Using these proposed equations it is also possible to estimate the drain current and V_{DSsat} value of CNFET for the given specifications. To justify the benefit of the proposed equations, CNFET analog circuits are successfully designed, simulated and their performances are compared with CMOS counterpart.

3.3 Common-Source CNFET Amplifiers

Common-source amplifiers (CS-amplifier) having a resistive-load and an active current mirror load are designed using the proposed equations. The simulations of the designed CNFET CS-amplifiers are carried out using a HSPICE compatible CNFET model proposed by J. Deng et al. [32]. Similar CS-amplifiers are designed using the MOSFETs and are simulated using 32 nm node Predictive Technology Model (PTM) for MOSFET [97]. The performance of both types of amplifiers are compared at different supply voltages keeping a constant bias current.

The capacitances considered for CNFET are gate to channel G_{gc}, fringing capacitance C_f between gate to doped region of SWCNT and coupling capacitance between gate/source or drain contacts C_{gtg} are shown in Fig. 3.7. The dimensions of the terminal contacts of CNFET device are; height

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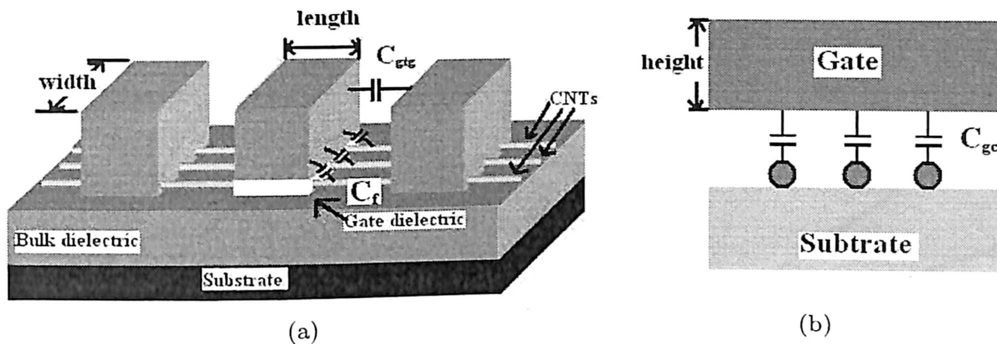

(a) (b)

Figure 3.7: Different capacitance of CNFET. (b) 3D view showing the fringing and inter electrode capacitance. (b) Cross sectional view showing gate to channel capacitance.

of gate/source/drain contact is 64 nm, length of source/drain is 32 nm, length of gate contact it is equal to the channel length and the contact width depends on number of SWCNTs and spacing between the SWCNTs.

3.3.1 Resistive-Load Common-Source Amplifier

A typical resistive-load CS-amplifier shown in Fig. 3.8 is designed using CNFETs with the help of proposed equations (3.2 - 3.5). A supply voltage of 0.9 V and drain current of 50 μA are initially considered for the CNFET CS-amplifier design. The gate voltage of 0.35 V is selected to minimize the voltage drop across the CNFET device. The proposed CNFET drain current equation (3.2) is used to estimate the dimensions of the CNFET device for the given specifications. The CNFET dimensions obtained are L_{ch} = 32 nm, L_{sd} = 32 nm, D_{CNT} = 1.5 nm, S = 20 nm, N = 45 and other parameters assumed to have default values as mentioned in users guide of the J. Deng's model [96]. For the given specifications, the V_{DSsat} value of CNFET estimated by the proposed equation is 0.24 V. The open circuit voltage gain of the circuit is estimated using the equation (3.6). The g_m and g_{ds} are the transconductance and the output conductance of the circuit, respectively. Value of the load resistor, R_D is chosen to have the optimum voltage gain and output voltage swing for the CNFET CS-amplifier.

$$A_{vo} = -g_m(R_D||(1/g_{ds})) \tag{3.6}$$

The CNFET CS-amplifier performance for a reference bias current of 50 μA and different supply

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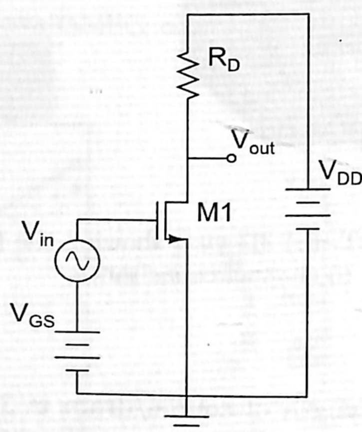

Figure 3.8: Resistive-load common-source amplifier.

Table 3.4: Performance of the CNFET resistive-load CS-amplifier for different supply voltages.

V_{DD} (V)	DC gain (V/V)	Output voltage (mV)
0.5	1.8	105
0.7	3.3	189
0.9	4.7	271
1.2	6.8	388
1.4	8.3	468
1.6	9.7	550
1.8	11.2	630
2.0	12.6	710

voltages is studied. The voltage gain and output voltage swing of the CS-amplifier are optimized by selection of proper value of the load resistor. Table 3.4 summarizes the values of supply voltage, voltage gain and output voltage swing of the CNFET CS-amplifier. It is observed that CNFET CS-amplifier has a large voltage gain and more output swing for higher supply voltages. The CNFET amplifier analysis will be incomplete without comparing its performance with the CMOS counterpart. A MOSFET resistive-load CS-amplifier using the conventional MOSFET current equation is designed and simulated using PTM model of 32 nm node MOSFET on a HSPICE simulator. The supply voltage and bias currents of both MOSFET and CNFET based circuits are kept identical so that all the performance comparison are carried out at constant power.

The linearity, voltage gain and output voltage swing of the CNFET CS-amplifier are compared

TH-1861_07610208

(a)

(b)

(c)

Figure 3.9: Performance comparison of CNFET and MOSFET resistive-load common-source amplifiers. (a) Output voltage versus input voltage. (b) Gain versus supply voltage. (c) Output voltage swing versus supply voltage.

with the MOSFET amplifier. Fig. 3.9(a) shows that at higher output voltage swings the CNFET amplifier has a better linearity as compared to the MOSFET amplifier. The plot also shows that the MOSFET CS-amplifier require more input voltage compared to the CNFET CS-amplifier to obtain the same output voltage.

The performance of CNFET resistive-load CS-amplifier and MOSFET CS-amplifier is compared in terms of voltage gain. The voltage gain of both amplifiers for different supply voltages are shown in Fig. 3.9(b). Slope of the line shown in Fig. 3.9(b) is a measure of performance of the amplifier. The slope of the line indicates the gain/supply voltage of the amplifier, the slope of the CNFET

TH-1861_07610208

amplifier is 7.15 per volt as compared to 3.67 per volt for the MOSFET amplifier. The slope shows that the CNFET CS-amplifier has exhibited more than two times of voltage gain increment per volt, when compared to the MOSFET CS-amplifier. However, Fig. 3.9(c) shows that the output voltage swing of the MOSFET CS-amplifier is always more compared to the CNFET amplifier. During the simulation result measurement of both CS-amplifiers, the total harmonic distortion (THD) of the output voltage waveform is maintained at 5%. Two parallel lines of the plot in Fig. 3.9(c) shows proportional increment in the output voltage of both CS-amplifiers for various supply voltages. In summary, the lower g_{ds} value of CNFET results in a higher voltage gain, but it has less output voltage swing compared to the MOSFET amplifier.

Wafer scale fabrication of CNFET device is not yet streamlined due to the challenges in large scale growth of aligned SWCNTs and control over the number of SWCNTs. The dimensions of channel length and width of the CNFET can be controlled lithographically. However, the SWCNT diameter and spacing between SWCNTs are growth dependent. Since the SWCNT diameter and spacing between the SWCNTs (pitch) are not fully controllable therefore, these two parameters are chosen in the analysis for effects of process variation on the performance of CNFET amplifiers. The performance of CNFET resistive-load CS-amplifier for various process parameters are studied at a supply voltage of 0.9 V. During the analysis for every process variation, the CNFET amplifier design is optimized to achieve better voltage gain and output voltage swing.

Process variations in the SWCNT dimensions of the CNFET will affect the performance of the CNFET resistive-load CS-amplifier as shown in Table 3.5. The first two columns give the values of process variation parameters i.e. SWCNT diameter and pitch. The third column gives the corresponding value of the number of SWCNTs which mitigate these process variations by maintaining the same current through the device. As the SWCNT diameter increases, the number of SWCNTs required to meet the specifications will reduce, which reduces the effective capacitance of the device thus resulting in a lesser gain of the amplifier. Table 3.5 shows that for a given SWCNT diameter the CNFET amplifier exhibits a constant voltage gain irrespective of the pitch value. The output voltage swing of the CNFET amplifier is not affected by the changes in process variations.

The gain per unit area is considered as one of the performance characteristics to compare the area efficiency of the CNFET amplifier with that of the MOSFET amplifier. Table 3.5 shows that the gain per unit area of a CNFET amplifier having larger diameter SWCNTs is always more because

TH-1861_07610208

Table 3.5: Effects of variation in the SWCNT dimensions on the performance of CNFET resistive-load CS amplifier.

SWCNT diameter (nm)	Pitch (nm)	Number of SWCNTs	Gain (V/V)	Output voltage (mV)	$(\frac{Gain}{Unit\ area})_{CNFET}$ $[(V/V)/\mu m^2]$	FOM
1.34	5	171	6.33	215	57.8	10.5
	10	105	6.02	230	44.7	8.1
	20	90	5.96	240	25.8	4.6
1.5	5	82	4.87	251	92.7	16.8
	10	52	4.74	261	71.2	12.9
	20	45	4.72	271	40.9	7.4
1.74	5	45	3.82	280	132.6	24.0
	10	28	3.67	282	101.0	18.3
	20	24	3.62	283	58.9	10.6
1.98	5	30	3.15	278	188.5	34.2
	10	19	3.11	287	127.8	23.2
	20	14	3.01	297	83.9	15.2

it needs less physical area for the device to accommodate lesser number of SWCNTs. The Figure of Merit (FOM) is defined as the ratio of gain per area of a CNFET CS-amplifier to that of a MOSFET CS-amplifier. The study of FOM in Table 3.5 shows that the CNFET amplifiers designed with lower pitch value are always more area efficient than larger pitch values irrespective of the SWCNT diameter. The study of process variations also shows that either SWCNT diameter or pitch will not affect the output voltage of the CNFET CS-amplifier. Table 3.5 shows that the CNFET amplifier exhibits a constant voltage gain for a given SWCNT diameter irrespective of the pitch value. The CNFET resistive-load CS-amplifiers with a large diameter SWCNTs and a less pitch have shown a higher FOM value.

3.3.2 Active-Load Common-Source Amplifier

After the detailed study of resistive-load amplifiers, CNFET active-load CS-amplifiers are analyzed. A typical active-load CS-amplifier shown in Fig. 3.10 is designed using CNFET devices with

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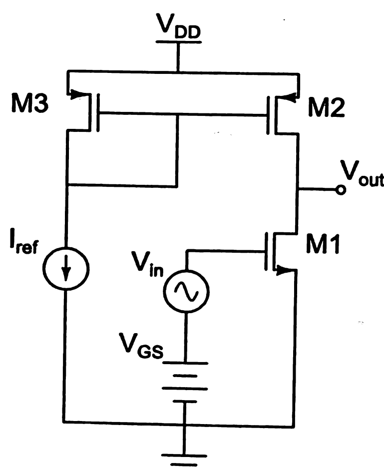

Figure 3.10: Active-load common-source amplifier.

the help of proposed equations (3.2 - 3.6). During the design of CNFET active-load CS-amplifiers for different supply voltages a constant reference current of 50 μA and a capacitive load C_L of 10 pF are considered. While designing the CNFET active-load CS-amplifier for a given supply voltage the dimensions of three CNFETs (M1, M2 and M3) are estimated to obtain a large voltage gain and a large output voltage swing. Table 3.6 shows the DC voltage gain and the output voltage swing of the CNFET active-load CS-amplifier for different channel lengths and number of SWCNTs of M1, M2 and M3 and for different supply voltages. The other device parameters of three CNFETs have the following parameter values; L_{sd} = 32 nm, D_{CNT} = 1.5 nm, S = 20 nm and remaining parameters assumed to have default values as mentioned in the users guide [96]. The lower g_{ds} value of the CNFETs can be attributed to the gain boosting of a CNFET active-load CS-amplifier at higher supply voltages. Compared to the resistive-load, the active-load CS-amplifier has a voltage gain which is improved by a factor of 46 at a supply voltage of 0.5 V. However, the output voltage swing of the CNFET active-load CS-amplifier is low compared to the resistive-load amplifier because the longer channel length CNFETs are used in the active-load amplifier.

To compare the performance of the CNFET active-load CS-amplifier with its CMOS counterpart, a MOSFET active-load CS-amplifier for the same power is designed. The voltage gain, output voltage and frequency response of the CNFET active-load CS-amplifier are compared with the MOSFET CS-amplifier. The gain of CNFET active-load common-source amplifier for different supply voltages compared with gain of the MOSFET CS-amplifier is shown in Fig. 3.11(a). For higher supply

TH-1861_07610208

Table 3.6: Details of CNFET device dimensions and performance of a CNFET active-load CS-amplifier for different supply voltages.

V_{DD}	L_{ch} (nm)			Number of SWCNTs			DC gain	Output voltage
(V)	M1	M2	M3	M1	M2	M3	(dB)	(mV)
0.5	50	32	32	38	39	39	38.4	76
0.7	57	62	62	37	39	39	54.9	100
0.9	90	82	82	35	36	36	64.4	123
1.2	90	83	83	35	34	34	91.3	290
1.4	90	90	90	35	24	24	104.6	413
1.6	89	64	64	35	28	28	118.7	744

voltages the CNFET CS-amplifier exhibits a larger voltage gain when compared to the MOSFET CS-amplifier. The increase in voltage gain of the CNFET CS-amplifier at higher voltage is due to a lower value of g_{ds}. The output voltage swing for different supply voltage of both circuits is shown in Fig. 3.11(b). For the design optimization of CNFET active-load CS-amplifier at a supply voltage of 1.6 V, CNFET of lesser channel lengths are used as shown in Table 3.6. Due to this output voltage swing is more compared to that of MOSFET CS-amplifier. During the comparison, the THD of output voltage is maintained at 5%.

The frequency response of the CNFET active-load CS-amplifier is compared with the MOSFET amplifier to know the ac performance. Fig. 3.11(c) shows the frequency response of CNFET CS-amplifier obtained for a supply voltage of 0.9 V with different capacitive loads. The frequency response of MOSFET CS-amplifier obtained under identical condition is shown in the inset. CNFET (MOSFET) CS-amplifier showed an open loop gain of 64.4 dB (35 dB) and gain bandwidth product (GBW) of 10.9 MHz (6.02MHz) for a capacitive load of 10 pF. The CNFET and MOSFET amplifier circuits with a zero capacitive load have exhibited a GBW of 370 GHz and 30.6 GHz, respectively. Ten times improvement in the GBW value of the CNFET amplifier can be attributed to a lower value of intrinsic capacitance of CNFETs. The study of frequency responses of both amplifiers shows that the CNFET active-load CS-amplifier performs better compared to the MOSFET amplifier in terms of DC open loop gain and GBW.

The effect of process variations in terms of the SWCNT diameter and pitch for a CNFET active-load CS-amplifier is examined. In the this study, the SWCNT diameter of range 1.34 nm to 1.98 nm

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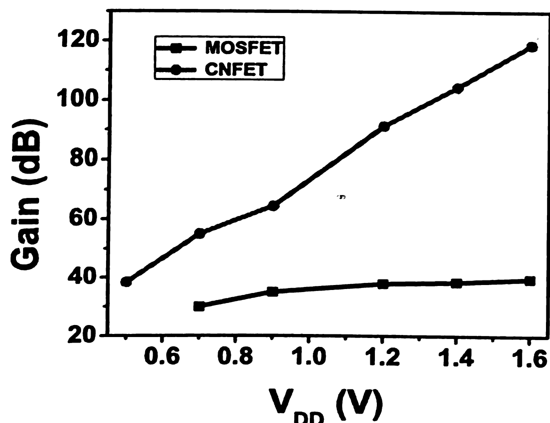
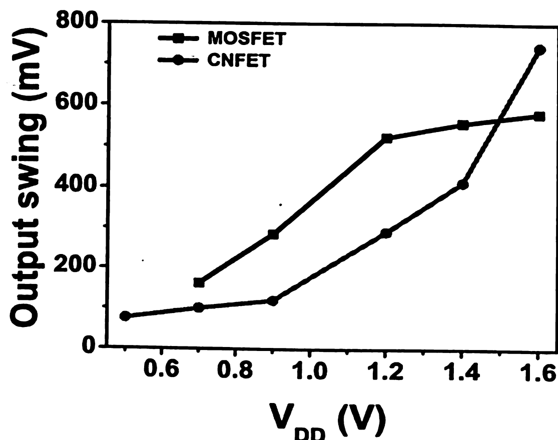


(a)



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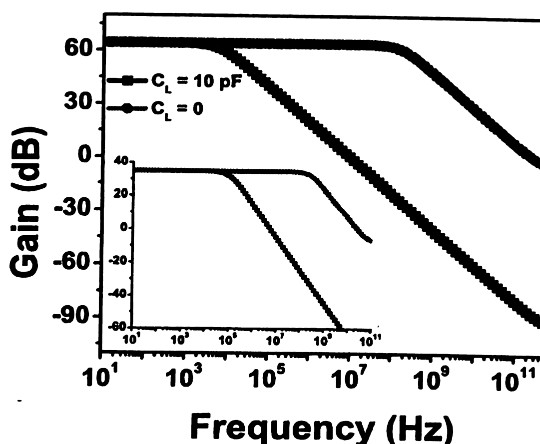

(c)

Figure 3.11: Performance comparison of the CNFET active-load CS-amplifier with that of the MOSFET amplifier. (a) Gain versus supply voltage. (b) Output voltage swing versus supply voltage. (c) Frequency response of CNFET active-load CS-amplifier for different capacitive loads and inset shows the same for MOSFET amplifier.

and the pitch of range 5 nm to 20 nm are considered. The details of CNFET device dimensions such as, channel length and number of SWCNTs of M1, M2 and M3 CNFET devices for various possible process variations are listed in Table 3.7. The effect of process variations on the performance of CNFET active-load CS-amplifier in terms of output voltage swing and DC gain is listed in Table 3.7. The study of process variation shows that the DC gain of CNFET CS-amplifier decreases with increase in the SWCNT diameter. However, it is observed that for a given SWCNT diameter, the DC gain of CNFET CS-amplifier remains constant irrespective of the pitch value. It is noticeable that

TH-1861_07610208

the process variation of the SWCNT diameter or pitch does not affect the output voltage of the CS-amplifier. The output voltage swing of CNFET CS-amplifier is less because the longer channel length devices are used. The gain per unit area of CNFET amplifier mentioned in Table 3.7 shows that amplifiers with a larger SWCNT diameter are more area efficient than circuits with smaller SWCNT diameter. The FOM of the active-load amplifiers in Table 3.7 shows that CNFET amplifier performs better than the MOSFET amplifier, as FOM value is always of the order 2 and even reaching order 3.

Table 3.7: Details CNFET device dimensions and performance of the CNFET active-load CS-amplifier for various process variations of SWCNT dimensions.

SWCNT diameter	Pitch	L_{ch} nm			Number of SWCNTs			DC gain	Output voltage	$(\frac{Gain}{Unit\ area})_{CNFET}$	FOM
(nm)	(nm)	M1	M2	M3	M1	M2	M3	(V/V)	(mV)	(V/V/μm^2)	
1.34	5	90	110	110	137	400	400	2500	130	71.4	212
	10	90	90	90	85	75	75	2697	129	157.0	499
	20	90	90	90	73	95	95	2739	129	70.3	226
1.5	5	90	90	93	62	66	66	1799	119	358.9	803
	10	90	90	83	40	40	40	1749	120	294.3	642
	20	90	82	82	35	36	36	1672	120	116.8	350
1.74	5	90	90	83	31	22	22	930	120	860.7	1098
	10	90	90	80	21	25	25	930	120	458.2	581
	20	90	90	66	18	18	18	1000	120	312.1	421
1.98	5	90	90	65	20	15	15	507	110	1212.3	920
	10	90	90	65	14	13	13	520	114	763.5	591
	20	90	90	53	12	12	12	505	112	432.4	327

During the study of CNFET amplifiers, we noticed that the channel length of CNFET device is one of the important device parameters that affects the performance. The performance of CNFET active-load CS-amplifier is examined for different channel length of CNFET device. All CNFET devices of the amplifier under test has L_{sd} of 32 nm, D_{CNT} of 1.5 nm and the other parameters assumed to have default values as mentioned in [96]. However, number of SWCNTs for the given

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channel length of CNFET device is estimated to optimize the amplifier performance and are listed in Table 3.8. It is observed from Table 3.8 that for designs with a longer channel lengths, the voltage gain of CNFET CS-amplifier reduces because of increased g_{ds} value of CNFET. It is noticeable in Table 3.8 that, as the channel length of CNFETs increases the output voltage swing of the CNFET CS-amplifier circuit reduces. This is because, as the channel length of CNFET increases, its V_{DSsat} value also increases as expressed in the V_{DSsat} equations.

Table 3.8: Details of the CNFET dimensions and performance of the CNFET active-load CS-amplifier for various channel length.

L_{ch} (nm)			Number of SWCNTs			DC gain	Output voltage
M1	M2	M3	M1	M2	M3	(dB)	(mV)
90	83	83	35	34	34	91.45	290
92	107	107	35	34	34	85.0	231
95	127	127	35	38	38	79.3	200
100	154	154	35	33	33	74.57	179
150	156	156	35	30	30	66.26	160
180	153	153	35	31	31	62.6	120
250	138	138	35	35	35	53.8	110

In this section, the practical applications of the proposed equations was demonstrated by designing the CNFET based analog amplifiers. It was shown that it is possible to have an estimate of the dimensions of the CNFET device and its performance can be compared with MOSFET counterparts.

3.4 Single-Stage CNFET Differential Amplifier

The differential amplifier is one of the most widely used circuit configuration in the analog integrated circuit design due to its superior noise suppression performance. A typical single-stage differential amplifier is shown in Fig. 3.12(a). As in the the previous designs of CNFET and CMOS amplifiers, differential amplifier circuit is also carried out for a constant power budget. The CNFET single-stage differential amplifier is designed using the proposed equations (3.2) - (3.5). All CNFET devices of the single-stage differential amplifier have the following device parameters; L_{ch} = 32 nm, L_{sd} = 32 nm, D_{CNT} = 1.5 nm, S = 20 nm and the other parameters assumed to have default values mentioned in [96]. The channel length of CNFET is chosen as 32 nm to reduce V_{DSsat} value of

TH-1861_07610208

CNFET which in turn increase the output voltage of the amplifier. The number of SWCNTs for the devices M1 - M6 are estimated as 29, 29, 3, 3, 60 and 60, respectively to meet the specifications. The MOSFET single-stage differential amplifier is also designed for identical specifications. Both single-stage differential amplifiers are simulated with supply voltages of V_{DD} = +0.9 V and V_{SS} = -0.9 V.

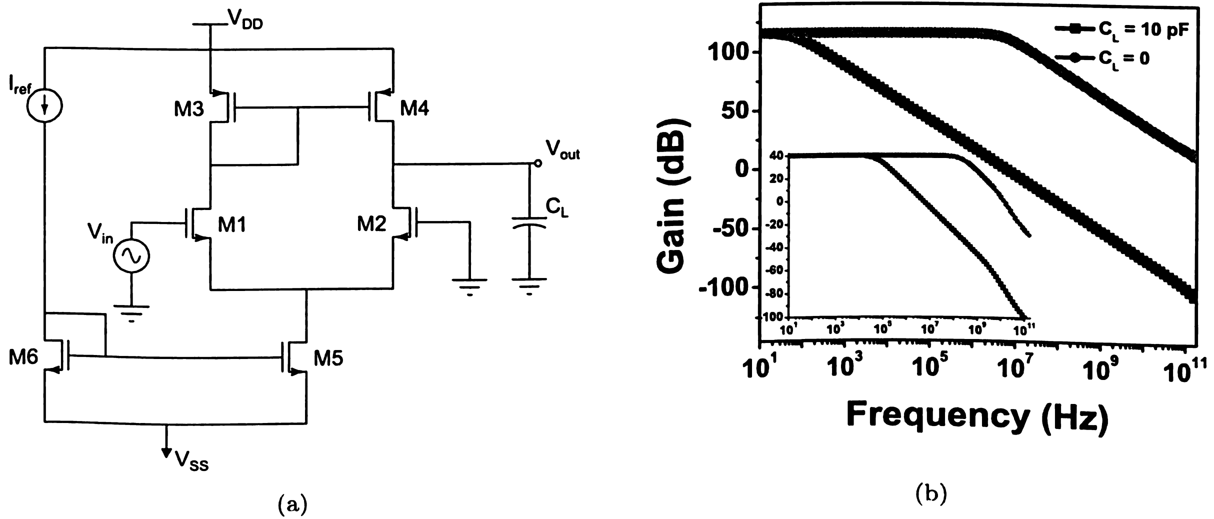

Figure 3.12: (a) Single-stage differential amplifier circuit. (b) The frequency response of CNFET circuit for different capacitive loads and inset shows the same for MOSFET circuit.

Table 3.9: Performance comparison of a CNFET single-stage differential amplifier with a MOSFET single-stage differential amplifier.

Parameter	CNFET	MOSFET
DC gain (dB)	116	40
CMRR (dB)	154	75
Slew rate (V/μs)	5	6.4
Phase margin	90°	90.4°
ICMR (mV)	-430 to +600	-300 to +750
Output voltage swing (mV)	620	1000
Power (μW)	160	160
GBW (MHz)(C_L = 10 pF)	7.4	5.6
GBW (GHz)(C_L = 0 pF)	328	15.8

The performance of a CNFET single-stage differential amplifier is compared with that of a MOS-

TH-1861_07610208

FET amplifier. Table 3.9 shows that the CNFET single-stage differential amplifier's DC gain is superior compared to the MOSFET amplifier. This phenomenon of large voltage gain of CNFET amplifier is due to a lower g_{ds} value of CNFET devices. The CNFET amplifier's performance in terms of the common mode rejection ratio (CMRR) is better compared to the MOSFET amplifier. Some of the performance parameters like slew rate, phase margin and input common mode range (ICMR) value of both CNFET and MOSFET amplifiers are comparable. However, output voltage swing of the MOSFET amplifier is more compared to the CNFET amplifier. Fig. 3.12(b) shows the frequency response of CNFET single-stage differential amplifier obtained with different capacitive loads. The frequency response of MOSFET amplifier obtained for similar load conditions is shown in the inset. The ac performance of CNFET single-stage differential amplifier is also better compared to MOSFET amplifier. The GBW value of CNFET amplifier for a capacitive load and no load conditions are greater compared to that of MOSFET amplifier. This large GBW value of CNFET amplifier can be attributed to the lower value of intrinsic capacitance of CNFETs.

3.5 Summary

An analytical closed-form equation to estimate the drain current of CNFET device was proposed. The proposed equation is obtained by the curve fitting technique and it includes the device dimensions, process parameters and gate voltage. The drain current estimated by the proposed equation deviated from the drain current of CNFET model reported by J. Deng et al. only by ±10% for most of the device parameters. Another equation was proposed for V_{DSsat} of CNFET and it includes the device parameters L_{ch}, D_{CNT} and the gate voltage. Both the proposed equations were validated with the available experimental result and were found matching within 10% error.

The proposed equations of saturated drain current and saturated drain to source voltage of the CNFET devices were used to design CNFET based analog amplifiers. The progress of the prospective CNFETs as a post silicon era device depends not only on the design of digital circuits but also on the analog circuit designs. There are very few reports of analog circuit implementation using CNFETs. Using proposed equations, the analog circuits like common source amplifiers and differential amplifiers were designed, simulated and performance of these circuits was compared with that of the CMOS counterparts. It may be noted that without the closed-form expression

TH-1861_07610208

in terms of device and process parameters, it is difficult to optimize the design to the required specifications. There are no reports available comparing the performance of the CNFET analog circuits with that of the CMOS counterparts and therefore this work is relevant. The gain, frequency response, linearity and output voltage swings are some of the factors used for comparison. The CNFET CS-amplifiers exhibit a high DC voltage gain and large GBW values compared to the MOSFET amplifiers. The CNFET differential amplifier showed better performance in terms of DC voltage gain, GBW. The impact of process variations in SWCNT diameter and pitch of the CNFET devices on the performances of CNFET amplifier was also examined.

TH-1861_07610208

4

Fabrication of Different Types of SN-TFTs

Contents

4.1 Introduction 56
4.2 Deposition of Carbon Nanotubes 59
4.3 Fabrication of SN-TFTs 64
4.4 Summary 74

TH-1861_07610208

4.1 Introduction

For the past 50 years, VLSI industry more or less follows the trend observed by Gordon E. Moore who predicted that number of transistors in a chip doubles in every 18 months. However, there are many challenges such as quantum mechanical tunneling through thin gate oxide, finite subthreshold slope, high on-off current ratio etc. and therefore innovative solutions are required to maintain the device scaling. There are two possible approaches to overcome these challenges; in the first, new devices that depart from the conventional scaling techniques such as high dielectric constant (high-k) gate dielectrics, metal gate electrodes, double-gate FETs, Fin-FETs, silicon on insulator (SOI) and strained-silicon FETs are employed. In the second approach, non-conventional fabrication techniques are used to make devices such as Single-electron transistors, Quantum dots, Resonant tunneling diodes, Organic TFTs and CNFETs. Among these, CNFETs which uses SWCNTs as their channel have attracted great interest due to the extraordinary structural, electrical and mechanical properties.

Carbon nanotubes which are rolled version of graphene sheet and produced using techniques such as arc discharge, laser ablation and chemical vapor deposition (CVD). In the year 1993, Bethune et al. [98] found the arc discharge method for the synthesis of SWCNT. The laser ablation technique was developed by Guo et al. [99] in the year 1995. In both arc discharge and laser ablation techniques along with the desired SWCNTs, a large amount of unwanted non-nanotube graphitic and amorphous carbon material are also produced, and a cleaning process is necessary before the SWCNTs can be used. The chemical vapor deposition based SWCNT growth was demonstrated by Hongjie Dai et al. [100] in the year 1996. The advantage of CVD SWCNT production is that the catalyst seed particles can be placed at the desired locations on a wafer and hence the SWCNTs can be selectively grown where they are required.

All synthesis methods discussed above produce SWCNTs with both semiconducting and metallic chiralities. Typically one third of the SWCNTs grown will be metallic in nature and there are different techniques to separate them from the as-grown SWCNTs. Guangyu Zhang, et al. [101] selectively etched m-SWCNTs from the as-grown SWCNTs using gas phase reaction. Philip Collins et al. [102] proposed an approach based on-current induced electrical breakdown to eliminate m-SWCNTs. Ralph Krupke et al. used dielectrophoresis process to separate m-SWCNTs from the as-grown SWCNTs [103]. Preferential growth of only s-SWCNTs during a synthesis process is desirable than separating them after the growth or eliminating after the fabrication process. Yiming Li et

TH-1861_07610208

al. [104] have demonstrated growth of nearly 90% of s-SWCNTs. Liangti Qu et al. [105] have grown vertically aligned SWCNTs consisting of 96% enriched s-SWCNTs by PECVD process.

In the following outline, a SWCNT based transistor is presented initially from a process perspective and later from a device perspective. Either the *in situ* grown or the pre-grown SWCNTs may be used to form the channel in a SWCNT based transistor. In case of the *in situ* method, the SWCNTs are grown during the transistor fabrication process and as of now only the CVD technique is compatible for such a synthesis. A pre-deposition of catalysts on the substrate are needed to initiate the SWCNT growth during the CVD process. The SWCNTs can be either grown from a patterned catalytic island [106] or from a thin-film of catalyst. After the growth of SWCNTs, source and drain contacts are deposited [107]. The advantage of this process is that the origin of the SWCNTs can be known and most importantly, by choosing a desired catalytic island dimensions, it possible to have the required density of SWCNTs. The atomic force microscope (AFM) method is also used to make source and drain electrical contacts over the SWCNTs. In the *in situ* growth method, the control on chirality, length, number and spacing of the SWCNTs is difficult and the process is presently not scaled-up to wafer scale.

In the pre-grown method, SWCNTs dispersed in the aqueous surfactant solution is readily available and the pre-grown SWCNTs can be deposited on the wafer using either spin-coat, dip-coat or immersion techniques. Alternatively, the pre-grown SWCNTs available on any other surface can also be transferred onto the Si surface using a thermal tape [81]. The SWCNTs deposited using the *in situ* method will typically consists of 67% of s-SWCNTs, but in case of the pre-grown method it is possible to use sorted SWCNTs of desired purity and even upto 99% s-SWCNTs are demonstrated. Another advantage of using the pre-grown SWCNTs is that the process can be scaled-up easily to a wafer scale and transistors of the desired channel dimensions can be fabricated.

The SWCNT channel for transistors can be formed either by an aligned [48, 49] or a random network of SWCNTs [46, 47]. It has been established that by the use of densely packed, an aligned horizontal arrays of non-overlapping linear SWCNTs as an effective thin-film electronic material will provide a large current outputs with a small device-to-device variations, even with SWCNTs that individually have widely different transport characteristics [49]. For the same device dimensions, aligned tubes yield a higher on-current (typically 3 times) than random ones [47]. The deposition techniques for a random network of SWCNTs are relatively simpler compared to the aligned type.

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The material and process considerations of the SWCNT based transistors are discussed so far. From a device perspective, the SWCNT transistors can be made using either individual SWCNTs or a thin-film of SWCNTs. The first CNFET reported is based on an individual SWCNT by Tans et al. in the year 1998. The CNFETs have exhibited an excellent subthreshold swing [7], transconductance [34, 35], mobility and on-off current ratio [36]. Another advantage of the CNFET is that multiple transistors can be fabricated on the same SWCNT [80]. Although CNFETs can potentially achieve the intrinsic mobility of a SWCNT, the method to assemble individual SWCNTs is extremely challenging to scale up and not technologically practical for large-area applications. Therefore, instead of individual SWCNTs, a thin-film of SWCNTs can be used as channel material for the fabrication of carbon nanotube thin-film transistors (CNTFTs). The CNTFTs having different purity of s-SWCNTs have been reported in the literature [46–49]. These CNTFTs have exhibited a much lower mobility compared to the CNFETs but, achieved better mobility compared to the conventional organic TFTs [108–110].

Another way to classify the SWCNT devices is based on the gate structure employed to control the transistor channel and therefore global back, local back and top gate devices are possible. In global back gate devices substrate itself acts as the gate electrode for all the transistors on the wafer and therefore control of the individual transistor is not possible. However, in case of the devices having local back or top gate structure it is possible to control wafer scale transistors individually. Many research groups have demonstrated transistors having different gate structures using both individual SWCNTs [78, 111, 112] and thin-film of SWCNTs [46, 47, 49, 113].

In this chapter, fabrication steps for different types of thin-film transistors using the pre-grown SWCNTs are presented. The deposition of random network of pre-grown SWCNTs are carried out using a solution based approach. The devices having different purity s-SWCNTs deposited on different gate oxide surfaces are fabricated. The process flow for global, local, top and dual gate transistors are presented separately. Many devices are fabricated simultaneously on multiple wafers and therefore process variations and repeatability of SN-TFTs are also studied. The sections of this chapter are arranged as follows. Section 4.2 describe different methods to deposit the SWCNT thin-film. Section 4.3 gives the complete process flow for the fabrication of different types of SN-TFTs and finally section 4.4 summarizes the chapter.

TH-1861_07610208

4.2 Deposition of Carbon Nanotubes

In this section, different methods of depositing the SWCNT thin-film are presented. As semiconducting type channel needed for SN-TFTs and the s-SWCNTs are procured from NanoIntegris Inc., USA. These SWCNTs were synthesized by the arc discharge and sorted to enrich the s-SWCNTs to 90% and 95% purity. These SWCNTs are obtained in the solution form containing ionized water, SWCNTs, and a proprietary combination of ionic surfactants. The SWCNT solutions also contain some iodixanol, a non-ionic, water-soluble iodine derivative which are used as a density gradient medium. The SWCNTs are deposited on the oxidized Si surface either by spin-coat, dip-coat or immersion technique. A uniform and high density thin-film of SWCNT is necessary for the wafer scale fabrication of SN-TFTs. The oxidized surfaces are modified to improve the density of SWCNTs and the thin-film densities obtained over the non-modified and the modified surfaces are compared. In order to improve the device performance of SN-TFTs, a high-k dielectric, i.e. hafnium oxide (HfO_X) is used as the gate dielectric material. In this work, SWCNT thin-film is deposited on both types of Si surface oxidized by HfO_X and SiO_2, and to the best of our knowledge, this is the first time deposition of SWCNTs over the silanized HfO_X surface is being reported.

First, the SWCNT deposition on the non-functionalized surface is presented. The process starts with rinsing of the oxidized wafers (Si/SiO_2 and Si/HfO_X) in 2-Iso propyl alcohol (IPA) followed by deionized (DI) water and then dried using nitrogen gas. The wafers are immersed in SWCNT solution for 20 min, followed by rinsing in IPA, DI water and drying in nitrogen. The images of SWCNTs deposited on the wafer are captured by the scanning electron microscopy (SEM) using Raith 150^{TWO} system. Fig. 4.1 presents the SEM images of the SWCNTs deposited on the non-modified oxide surfaces. Fig. 4.1(a) shows the SWCNTs deposited on the Si/SiO_2 surface and Fig. 4.1(b) shows the SWCNTs on Si/HfO_X surface. It may be noted that the uniformity of SWCNTs is poor and average density of SWCNTs is about < 2 SWCNTs/μm^2 on Si/SiO_2 surface. The SWCNT density is even worse on Si/HfO_X surface and these values are unacceptable for field-effect transistor fabrication. As the density of the SWCNT obtained on a simple surface is not suitable for the device fabrication, the subsequent sections discuss SWCNT deposition over modified surfaces.

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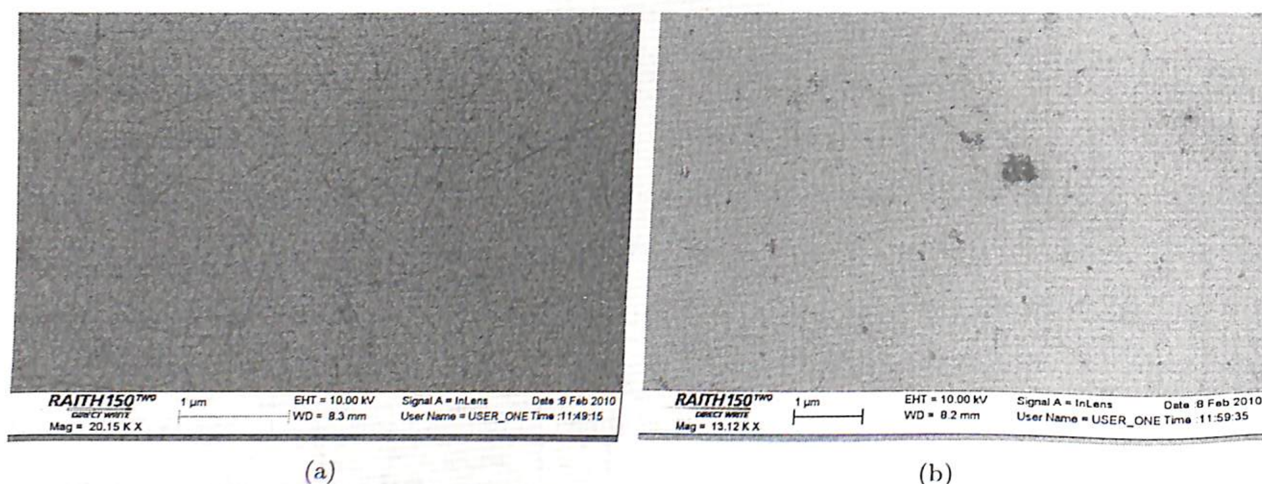

(a) (b)

Figure 4.1: *SEM images of SWCNT thin-film deposited on the non-functionalized oxidized surfaces. (a) SWCNTs over Si/SiO_2 surface. (b) SWCNTs over Si/HfO_x surface.*

4.2.1 Spin-Coat Technique

In order to increase the density of SWCNTs in the thin-film, the oxidized Si surface is functionalized before depositing the SWCNTs. Aminoisopropyltriehoxy silane (APTES), known for its affinity to the SWCNTs [42, 114] is used to functionalize the oxidized silicon surface. Spin-coat is one of the methods to deposit the random network of SWCNTs.

In spin-coat technique, a thin-film of random network of SWCNTs is deposited using the following procedure. First, the oxidized silicon wafer (Si/HfO_x or Si/SiO_2) is immersed in sulfo-chromic acid for 5 min and then rinsed in DI water thoroughly to create OH bonds. A solution containing 60 μl of 3-aminoisopropyltriehoxy silane and 20 ml of IPA is prepared and the wafer is immersed in this solution for 10 min in an argon ambient, because argon gas avoids polymerization of APTES. Subsequently the wafer is rinsed in IPA and dried using argon gas. After the wafer is treated with amino-silane, SWCNT solution of 100 μl is carefully dropped via pipette near the surface and at the center of the wafer spinning at speeds between 2000 and 4000 rpm. The density of SWCNTs deposited over the functionalized wafer at a spinning rate of 2000 and 4000 rpm are shown in the SEM images of Fig. 4.2(a) and 4.2(b), respectively. In both images, the average density of SWCNTs are found to be less than 5 SWCNTs/μm^2 and is not suitable for transistor fabrication. Therefore in order to improve the SWCNT density, other methods for deposition of SWCNTs are examined in the following section.

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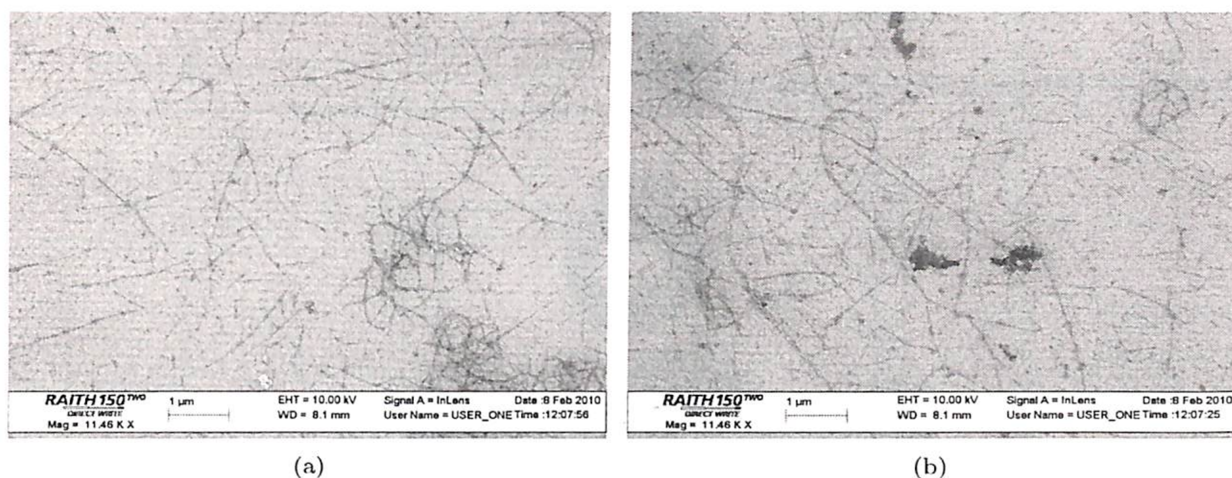

Figure 4.2: SEM images of the SWCNT thin-film deposited on the functionalized Si/HfO_x surface by spin-coat technique. (a) SWCNTs deposited at a spin rate of 2000 rpm. (b) SWCNTs deposited at a spin rate of 4000 rpm.

4.2.2 Dip-Coat Technique

In order to deposit high density SWCNT thin-film, the oxidized Si wafer is immersed in sulfochromic acid for 5 min and then rinsed in DI water thoroughly in order to create OH bonds. The wafer is dehydrated by heating it to 110°C for 1 hour at a pressure of 10^{-2} mbar. A solution containing 60 μl of 3-aminoisopropyltriehoxy silane and 20 ml of IPA is prepared and the wafer is immersed in this solution for 10 min in an argon ambient. Subsequently, the wafer is rinsed in IPA and dried using argon gas. The water contact angle of the amino-silane treated Si/SiO_2 surface shown in Fig. 4.3 is measured and the obtained value is 68.7°. A contact angle between 38°- 80° range is reported to be suitable for the deposition of SWCNTs [42]. From the contact angle, the physical properties of interaction between the solid and the liquid such as wettability, affinity, adhesiveness and repellency can be studied.

After the APTES treatment, the wafer is dipped in SWCNT solution for 20 min [46]. In order to remove the sodium dodecyl sulfate (SDS) residual on the SWCNTs, the wafer is dipped in IPA followed by rinsing in DI water and finally dried with nitrogen. The SEM images in Fig. 4.4(a) and 4.4(b) shows the density of SWCNTs deposited on both Si/SiO_2 and Si/HfO_x surfaces, respectively by the dip-coat method. The average density of the SWCNTs on the modified Si surface is found to be about 30 SWCNTs/μm^2. Wafers with the SWCNTs deposited using the dip-coat method are used to fabricate the devices of different dimensions.

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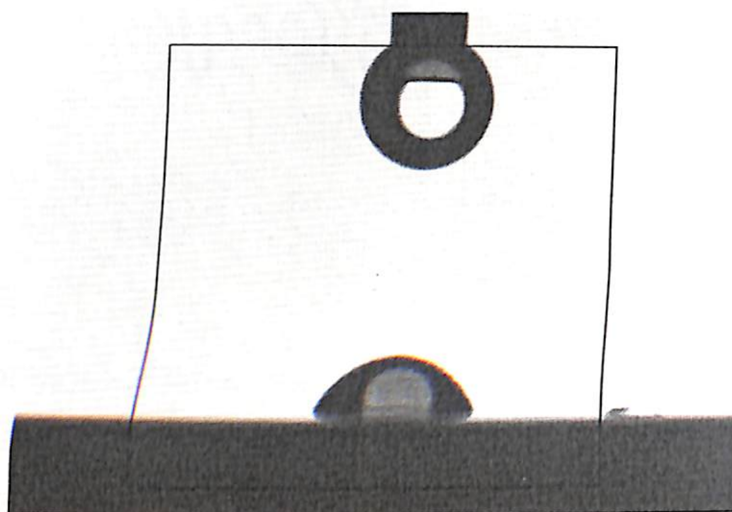

Figure 4.3: Water droplet on a functionalized Si/SiO_2 surface.

(a) (b)

Figure 4.4: SEM images of SWCNT thin-film deposited on the functionalized surface by dip-coat method. (a) SWCNTs on Si/SiO_2 surface. (b) SWCNTs on Si/HfO_X surface.

4.2.3 Immersion Technique

This technique is similar to the dip-coat method, but has simple process steps. In this method, the oxidized surface modified by immersing the wafer in sulfo-chromic acid for 5 min followed by DI rinsing and then the wafer is immersed in a solution containing 60 μl of 3-aminoisopropyltriehoxy silane and 20 ml of IPA for 10 min in an argon ambient. Subsequently, the wafer is rinsed in IPA and dried using argon gas as discussed in the dip-coat method. A water contact angle of 69.4° is obtained on an amino-silane treated surface as shown in Fig. 4.5, and such a value is suitable for the deposition of SWCNTs on the Si surface [42].

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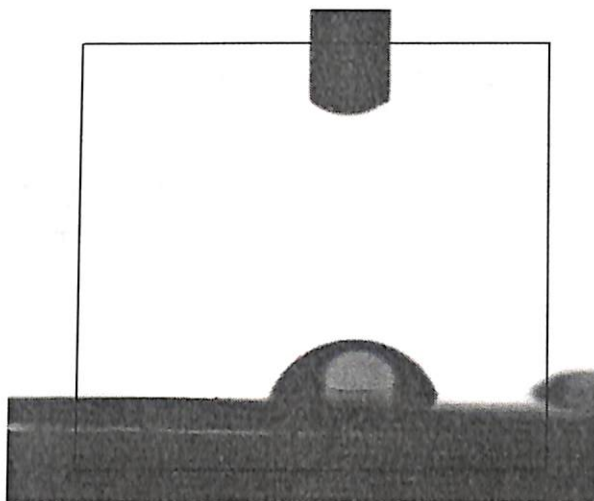

Figure 4.5: Water droplet on a functionalized Si/HfO_x surface.

To deposit the SWCNTs, the wafer is immersed in the SWCNT solution for 20 min. The wafer is rinsed in IPA, followed by rinsing in DI water and finally dried with nitrogen. The SEM image in Fig. 4.6 shows the density of SWCNTs deposited on the Si/HfO_x surface by the immersion technique. The average density of SWCNTs on the modified surface is 40-45 CNTs/μm^2. As the immersion method yields better SWCNT density, the same is used to deposit the SWCNTs during the fabrication of wafer scale SN-TFTs.

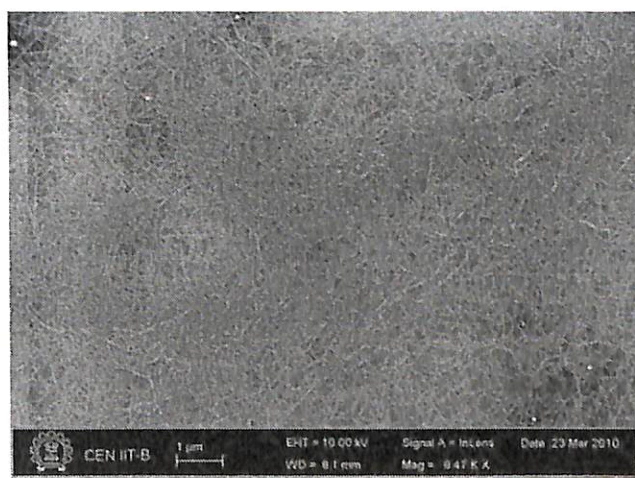

Figure 4.6: SEM image of SWCNT thin-film deposited on the functionalized Si/HfO_x surface by immersion method.

In this section, the deposition of SWCNTs over the oxidized Si substrate were studied. The SWCNT density over the non-functionalized wafers was found to be $<$ 2 SWCNTs/μm^2 and is

TH-1861_07610208

unsuitable for SN-TFT fabrication. The spin-coat, dip-coat and immersion methods are examined to deposit the SWCNTs on the amino-silane modified oxidized Si surfaces. The deposition of SWCNTs using dip-coat and immersion method have yielded higher density SWCNTs than the spin-coat technique. The next section discusses the fabrication of different types of SN-TFTs.

4.3 Fabrication of SN-TFTs

In this section, the fabrication of different types of SN-TFTs are presented. The SWCNT thin-films are deposited on both modified SiO_2 and HfO_X surfaces. The fabrication of SN-TFTs having different gate structures namely global back, local back, top and dual gate are discussed separately. The wafer scale fabrication include the devices of various channel dimensions and thin-film of different purity s-SWCNTs.

4.3.1 Process Flow of Global Back Gate SN-TFTs

The fabrication of global back gate SN-TFTs with interdigitated electrode (IDE) source/drain contacts are summarized in Fig. 4.7. A 2 inch p-type Si <100> wafer having resistivity in the range of 0.01 - 0.1 Ωcm is used as a substrate. The wafer is cleaned by the standard Radio Corporation of America (RCA) process to remove the organic contaminants from the surface. The SiO_2 or HfO_X is used as the gate dielectric material for the devices. In order to grow the SiO_2 over the Si surface, the dry thermal oxidation process is used. A 50 nm SiO_2 layer is grown over the Si at a furnace temperature of 1100°. To deposit a high-k dielectric HfO_X layer, the RF sputtering technique is employed. The HfO_X of 200 nm is deposited on the wafer at room temperature and the chamber is maintained at a pressure of 1.2×10^{-3} mbar. The cross sectional view of the wafer after the deposition of the gate oxide layer is shown in Fig. 4.7(a).

The dip-coat technique is used to deposit high density SWCNT thin-film having 90% or 95% purity of s-SWCNTs on the SiO_2 or HfO_X gate oxide layer. The cross sectional view of the structure after the deposition of SWCNTs on the amino-silane modified wafer is shown in Fig. 4.7(b). Large dimensions in the range of 10s to 100s of micrometers are chosen in order to verify the uniformity of SWCNT deposition over a large area and the IDE type electrodes are used for the same purpose as shown in Fig. 4.8. Each quarter of the wafer contains 20 SN-TFTs and the same is repeated in other three quarters of the wafer and therefore a total of 80 devices are accommodated per wafer. The 20 devices on each quarter is organized in 3 different patterns such that 12 devices have 3 finger

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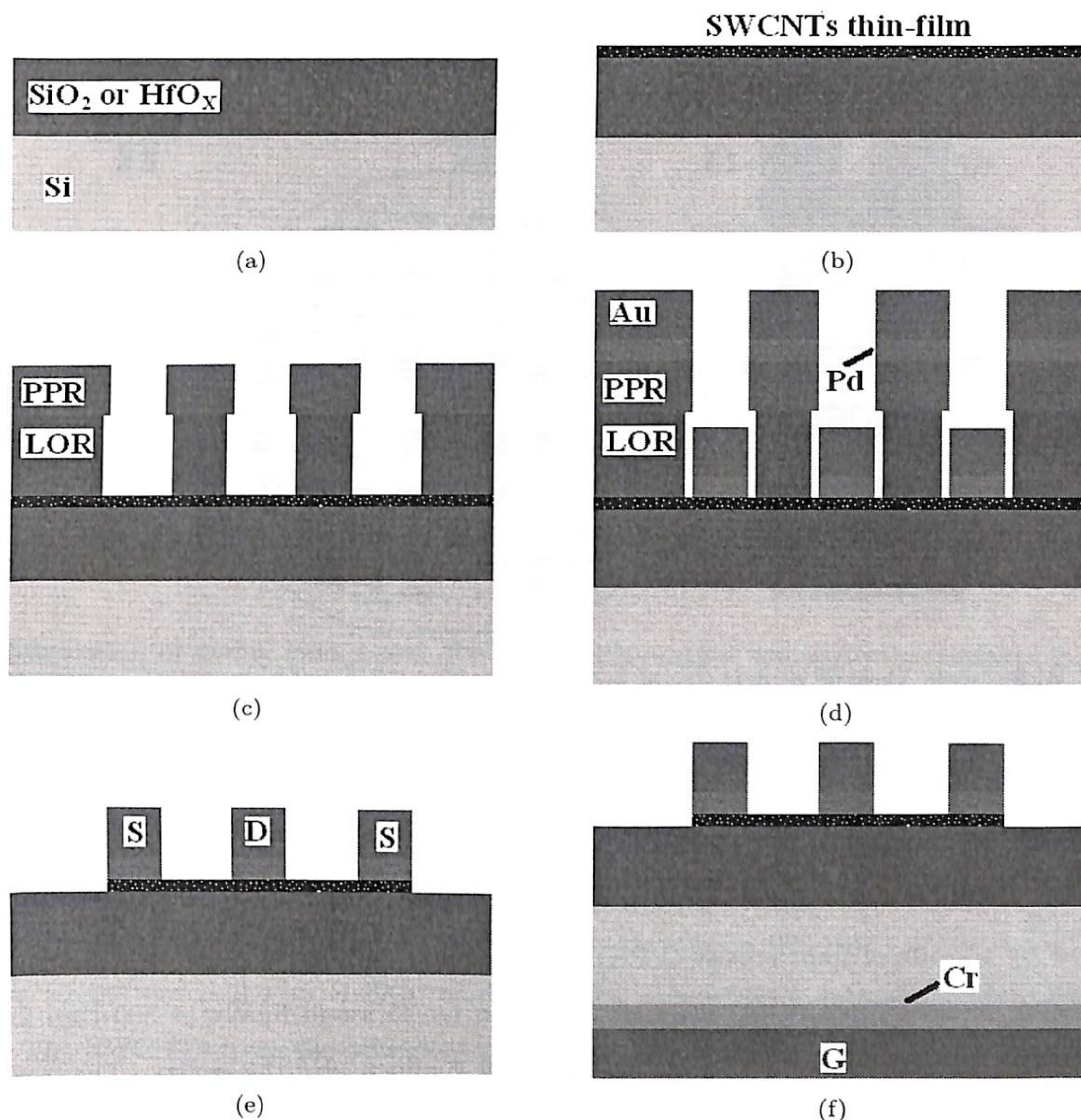

Figure 4.7: Process flow for the fabrication of back gate SN-TFT having IDE source/drain contacts. (a) HfO_x (SiO_2) deposited (grown) on Si substrate. (b) SWCNTs deposition over APTES functionalized HfO_x (SiO_2) surface. (c) Lift-off resist and positive photoresist layers after developing. (d) Pd and Au deposited over developed lift-off resist and positive photoresist layers. (e) Pd and Au on SWCNTs for source/drain contact after lift-off process. (f) Chromium/gold deposited as gate contact at the back side of wafer.

pattern, 6 devices have 6 finger pattern and 2 devices have 16 finger pattern. The lengths of the fingers are 1000, 1500 and 2000 μm and gaps between the fingers are 20, 50 and 100 μm and the width of the finger is maintained at 100 μm. The resulting channel length of the devices are 20, 50 and 100 μm and the width varied from a minimum 2300 μm to a maximum of 31600 μm. The mask patterns are written over Iron Oxide (FeO) coated mask plates using Laser Write LW405.

Photolithography is carried out using the double sided aligner DSA EVG620. The patterns for

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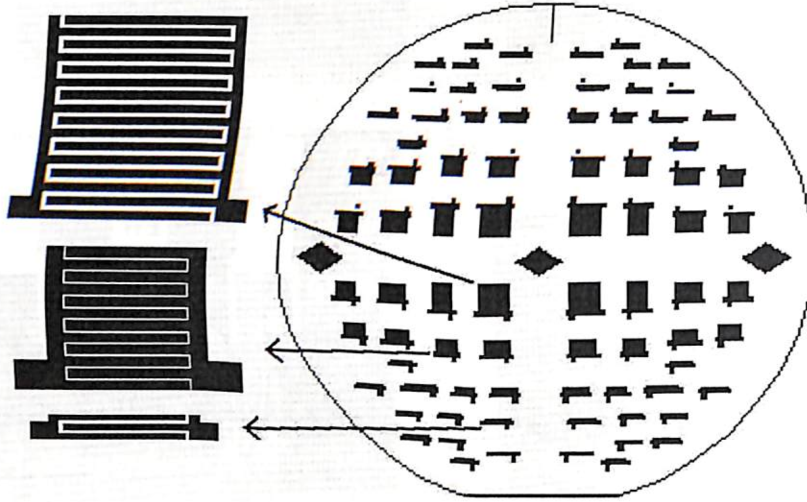

Figure 4.8: Wafer scale view of devices (right side) and zoom-in (left side) shows three different IDE source/drain patterns employed.

different layers are obtained on the wafer using the following process. The wafer is dehydrated at 150°C for 15 min before the lithography process. Initially a lift-off resist (LOR) is spun on the wafer and is followed by a positive photo-resist (PPR) S-1813. The spinning of resists was carried at a speed of 300 rpm for 30 s initially, followed by 6000 rpm for 45 s and finally at 500 rpm for the last 5 s. The wafer is baked at 90°C using a hotplate for 2 min to dry the resists. The exposure by UV rays was carried out for 8 s and a separation of 30 μm between the mask and the wafer is maintained during the exposure. Finally, the softened resists are removed form the wafer by rinsing in a developer solution and the resulting cross sectional view is shown in Fig. 4.7(c).

The palladium (Pd) film of thickness of 7 nm is deposited by the RF sputtering technique at room temperature at a pressure of 2.6×10^{-3} mbar and is followed by the deposition of gold (Au) film of thickness 55 nm under same conditions. The cross sectional view after the metals deposition is shown in the Fig. 4.7(d). The lift-off process is carried out by immersing the wafer in acetone solution for 45 s and followed by sonication for 1 min and will result in a structure shown in Fig. 4.7(e). The gate contact for the global back gate SN-TFTs is obtained by sputtering chromium (Cr) followed by Au in a single process at the back side of the wafer. Before this sputtering process, contents on the front side of the wafer are protected by the PPR layer and the back side is treated with the buffered hydrofluoric acid (BHF) to remove the native oxide. The cross sectional view of the gate contact of the device using Cr/Au of thickness 5/55 nm is shown in Fig. 4.7(f). The SWCNTs from the unwanted region are removed using O_2 plasma after protecting the channel region with

PPR.

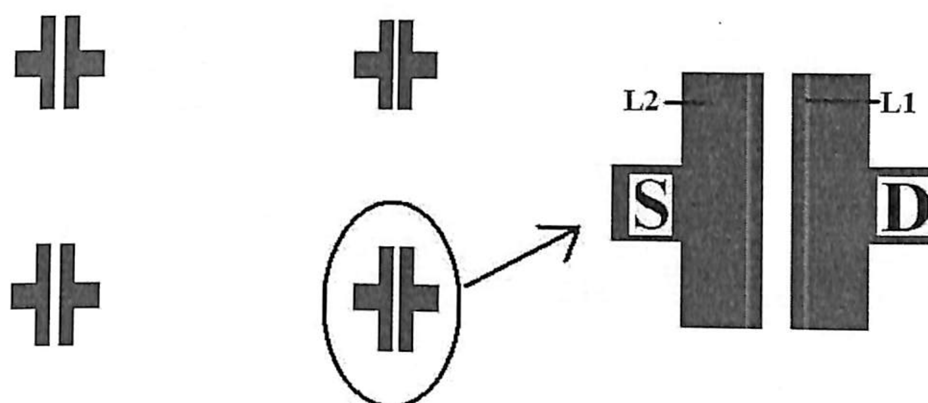

Figure 4.9: Layout pattern showing an array of global gate SN-TFTs with normal source/drain contacts and magnified view of an individual device.

The fabrication of global back gated SN-TFTs with normal source/drain contacts is similar to above discussed steps, except the deposition of Pd and Au for source/drain contacts. In this type of SN-TFTs, the source/drain contact regions are not of the IDE type and are defined by level L1 and L2 masks shown in Fig. 4.9. The mask consists of layouts for 50 devices of different dimensions - channel lengths are 5, 10, 20, 30 and 40 μm and widths are 10, 50, 100, 400 and 500 μm. Fig. 4.10(a) shows the cross sectional view of Pd source/drain contacts deposited over the SWCNT thin-film using L1 pattern and Fig. 4.10(b) shows the Au source/drain terminal pads defined by L2 pattern. The SWCNTs from the unwanted region are removed by the O_2 plasma after protecting the channel region with the PPR. The gate contact of the device is obtained by sputtering 5 nm of Cr and 55 nm of Au in a single process at the back side of the wafer. The final structure of the global back gate SN-TFT is shown in Fig. 4.10(c).

The optical images of two fabricated global back gate SN-TFTs are shown in Fig. 4.11. A typical SN-TFT with an IDE source/drain contacts having a channel length of 20 μm and a width of 23200 μm is shown in Fig. 4.11(a). A global back gate SN-TFT having channel length of 40 μm and width of 500 μm is shown in Fig. 4.11(b).

4.3.2 Process Flow of Local Back Gate SN-TFTs

In this subsection, the process steps involved in the fabrication of local back gate SN-TFTs are discussed. To examine the uniformity of the SWCNT deposition, an array of wafer scale SN-TFTs having various dimensions are fabricated using HfO_X as the gate oxide, 95% enriched s-SWCNT for

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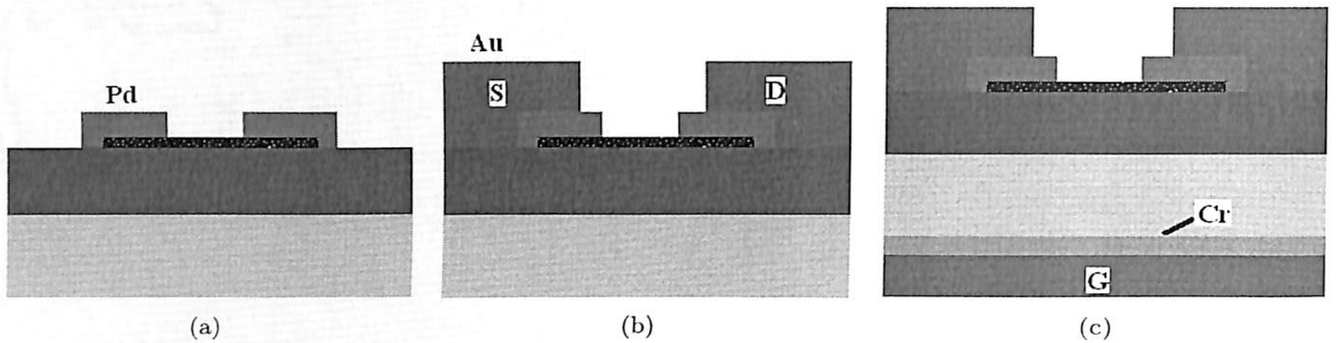

Figure 4.10: Process flow for the fabrication of back gate SN-TFT with normal source/drain contacts. (a) Pd deposited over developed on the SWCNT thin-film. (b) Au patterns defining the contact probes for source/drain. (c) Chromium/gold deposited as gate contact at the back side of wafer.

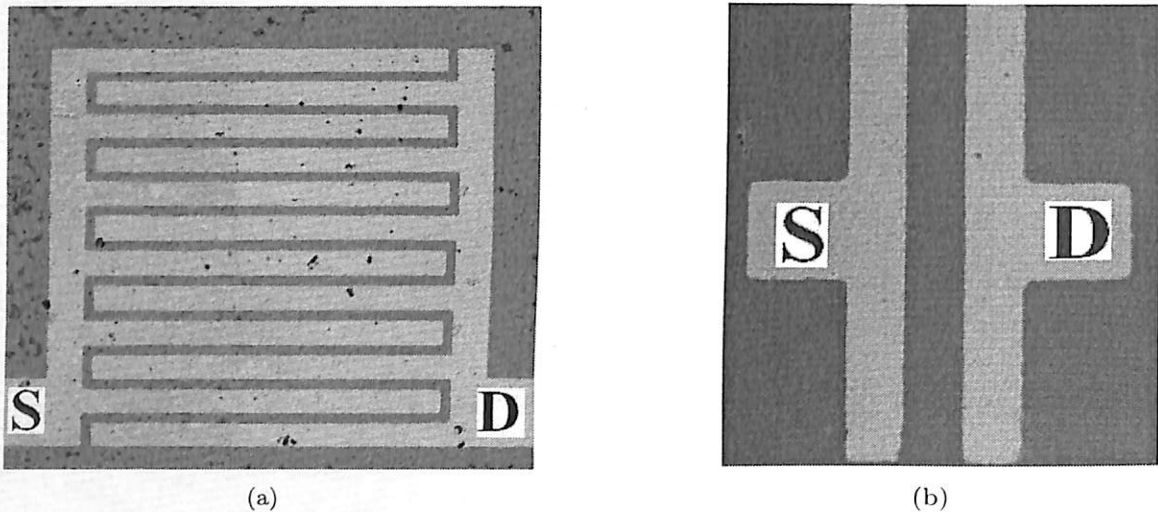

Figure 4.11: Microscopic images of the fabricated global back gate SN-TFTs. (a) Typical IDE source/drain contacts. (b) Typical normal source/drain contacts.

thin-film channel. The major process steps involved in the fabrication of SN-TFT is summarized in Fig. 4.12. A 2 inch p-type Si <100> wafer having resistivity in the range of 0.01 - 0.1 Ωcm is used as a substrate. Over the RCA cleaned Si wafer, the SiO_2 of 50 nm thickness is grown using the dry thermal oxidation process to isolate the SN-TFTs from the substrate. The cross sectional view of after the oxidation process is shown in Fig. 4.12(a).

The masks used for the fabrication of local gate SN-TFTs have 5 levels and are shown in the Fig. 4.13. An array of 4 devices are shown on the left side and one device is enlarged on the right side to show the details. To define the gate region of the device, resist coated wafer is exposed to UV source using L1 pattern as shown in Fig. 4.13. Pd film of 7 nm thickness is deposited by the RF sputtering

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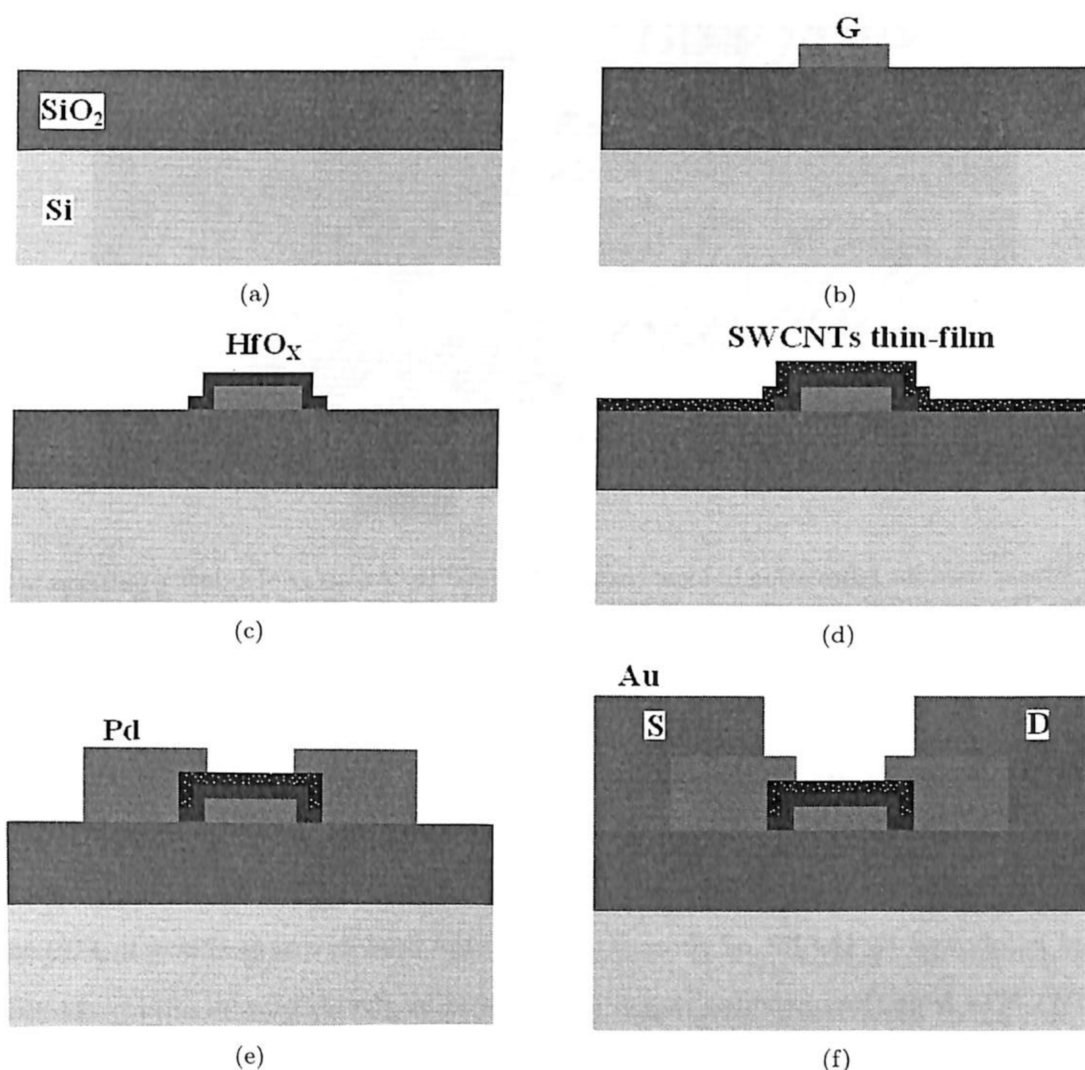

Figure 4.12: Process flow for the fabrication of local back gate SN-TFT. (a) SiO_2 grown on Si substrate. (b) Pd film of 7 nm thickness deposited by RF sputtering as local back gate. (c) High-k HfO_X layer deposition as gate gate dielectric material. (d) Thin-film of SWCNTs deposited on the silanized oxide surface. (e) Pd deposition for source and drain contacts. (f) Gold deposition for large area contact pads.

technique to realize the local back gate structure as shown in Fig. 4.12(b). The gate dielectric region of the device is defined using L2 mask as shown Fig. 4.13. This is followed by HfO_X deposition (10 nm) using the RF sputtering method at room temperature. HfO_X from the unwanted region is removed by the lift-off process and the resulting cross sectional view is shown in Fig. 4.12(c).

The next process is SWCNT thin-film deposition on the HfO_X layer. In order to deposit high density SWCNT thin-film, the immersion technique discussed in earlier section is employed. The cross sectional view of the structure after the deposition of SWCNTs is shown in Fig. 4.12(d). The source and drain contacts of the SN-TFT are defined by L3 mask as shown in Fig. 4.13 to deposit

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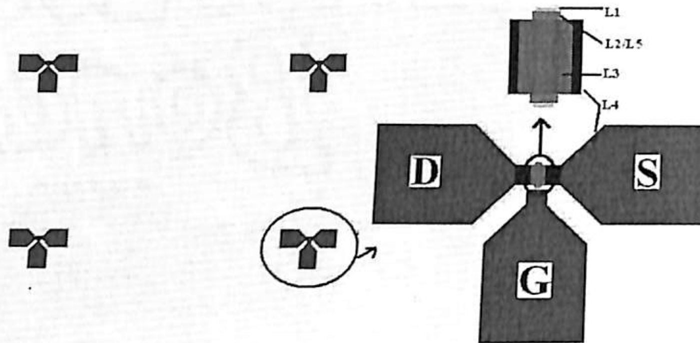

Figure 4.13: Masks used for fabrication of local back gate SN-TFTs. An array of 4 device patterns are given on the left side. The magnified view of an individual device and details of different masks are given on the right side.

Pd of 7 nm thickness by the RF sputtering and the structure obtained is shown in Fig. 4.12(e). The source, drain and the gate electrode contact pads each of dimensions 100 × 100 μm for probing purpose are defined using L4 mask as shown in Fig. 4.13. Au of 55 nm is deposited using the RF sputtering and is followed by the lift-off process to obtain the final device as shown in Fig. 4.12(f). Finally, the SWCNTs from the unwanted region are removed by the O_2 plasma after protecting the channel region with the PPR using L2/L5 masks. Total of 5 levels lithography are required to realize the local back gate SN-TFTs. The wafer scale array of SN-TFTs have the following dimensions - channel lengths are 2, 5, 8, 10, 15, 20, 30, 40, 50, 75 and 100 μm and channel widths are 2, 5, 8, 10, 15 and 20 μm. An optical image in Fig. 4.14(a) shows the local gate SN-TFT of channel length 8 μm and width 20 μm. The SEM image in Fig. 4.14(b) indicates visually that a good contact is established between The SWCNTs and Pd. The contact properties will be further explored by electrical characterization.

4.3.3 Process Flow of Top Gate SN-TFT

The fabrication of top gated SN-TFT is illustrated in Fig. 4.15. The process starts with the growth of 50 nm SiO_2 on the Si surface to isolate the SN-TFT from the substrate as shown in Fig. 4.15(a). The patterns of level L2 shown in Fig. 4.13 are used to define HfO_x of 10 nm thickness over the oxidized Si surface as shown in Fig. 4.15(b). Fig. 4.15(c) shows the cross sectional view of the SWCNT thin-film deposited on the HfO_x surface modified by amino-silane.

Fig.4.15(d) shows the source/drain regions defined by L3 mask after the deposition of 7 nm thin-film of Pd. The probe contacts for source/drain are realized by L4 mask patterns. The deposition

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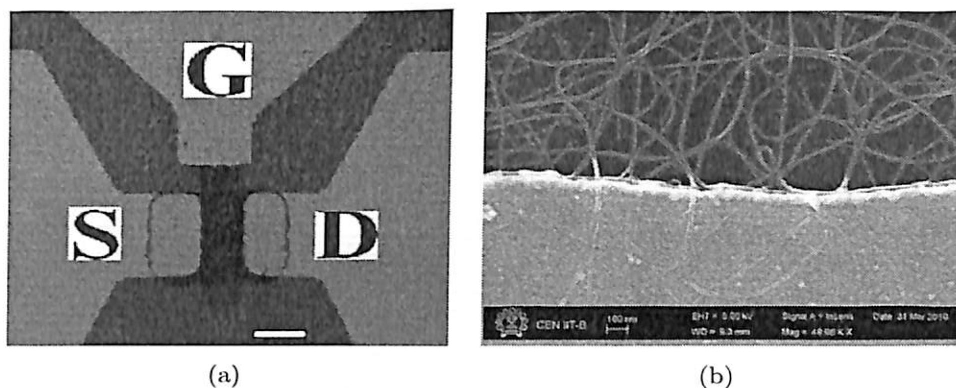

(a) (b)

Figure 4.14: Images of local back gate SN-TFT. (a) Microscope image of a typical local back gate SN-TFT. (b) SEM image indicating the contact of SWCNT thin-film with palladium source/drain regions.

of 55 nm of Au is followed by a lift-off process and results in a structure shown in Fig. 4.15(e). The focused ion beam (FIB) based gas injection system (GIS) process is used to deposit 10 nm thick SiO_2 as the gate oxide. During the gate oxide deposition, Raith 150^{TWO} is operated at a system vacuum of 6.68×10^{-6} mbar and gun vacuum of 6.79×10^{-9} mbar and Fig. 4.15(f) shows the corresponding cross sectional view.

The top gate contact for the SN-TFTs are realized by depositing 10 nm thick Tungsten (W) using the GIS technique resulting in a cross sectional view shown in Fig. 4.15(g). As the deposition rate of GIS technique is low, the effective length of the top gate device is restricted to 5.6 μm. However, the total channel length for the top gate i.e. combined the lengths of spacers and W is 10 μm and the channel width is 18.5 μm.

4.3.4 Process Flow of Dual Gate SN-TFT

The fabrication of dual gate SN-TFT is discussed in this subsection. The processing of dual gate SN-TFT starts with RCA cleaning of a p-type Si substrate followed by the dry thermal oxidation process for the growth of 50 nm thick SiO_2 to isolate the SN-TFT from the substrate as shown in the Fig. 4.16(a).

The cross sectional view of the back gate structure is shown in Fig. 4.16(b) and is obtained by depositing Pd of 7 nm thickness and subsequent patterning by L1 mask. The back gate oxide regions shown in Fig. 4.16(c) is obtained by depositing the high-k HfO_X of 10 nm thickness and subsequent patterning by L2 mask. The 95% enriched semiconducting SWCNTs are deposited on the HfO_X surface modified by an amino-silane to form a thin-film of SWCNTs as shown in the cross sectional

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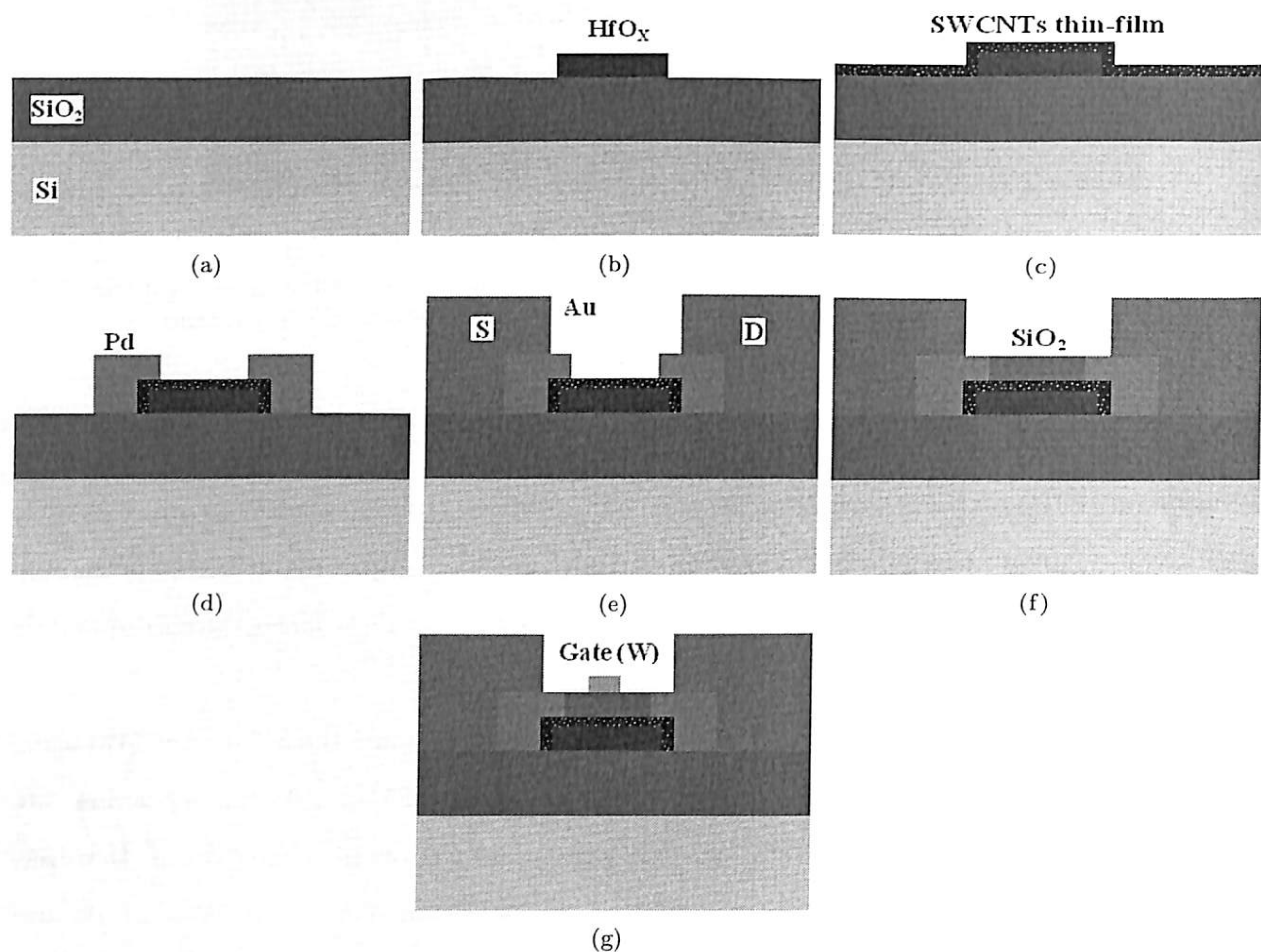

Figure 4.15: Process flow for the fabrication of top gate SN-TFT. (a) SiO_2 grown over the Si substrate. (b) HfO_X layer after deposition and lift-off process. (c) Thin-film of SWCNTs deposited on the silanized oxide surface. (d) Palladium deposition for source and drain contacts. (e) Gold deposition for large area contact pads. (f) Deposition of SiO_2 layer as dielectric material for the top gate. (g) Tungsten deposition to realize the top gate structure.

view of Fig. 4.16(d). Over this SWCNT thin-film, the source and drain regions are obtained by depositing 7 nm of Pd and subsequent patterning by L3 mask as shown in Fig. 4.16(e). The probing contacts of the source/drain/gate regions are defined by the mask L4 after sputtering Au of thickness 55 nm as shown in Fig. 4.16(f). The top gate of the device is realized by depositing 10 nm thick SiO_2 layer as the top gate oxide over the SWCNT thin-film as shown in Fig. 4.16(g) and is followed by a 10 nm thin layer of W as the top gate contact as shown in Fig. 4.16(h) both using GIS technique of Raith 150^{TWO} equipment. The top gate is shorted with the back gate contact to have an identical electrical potential on either side of the channel.

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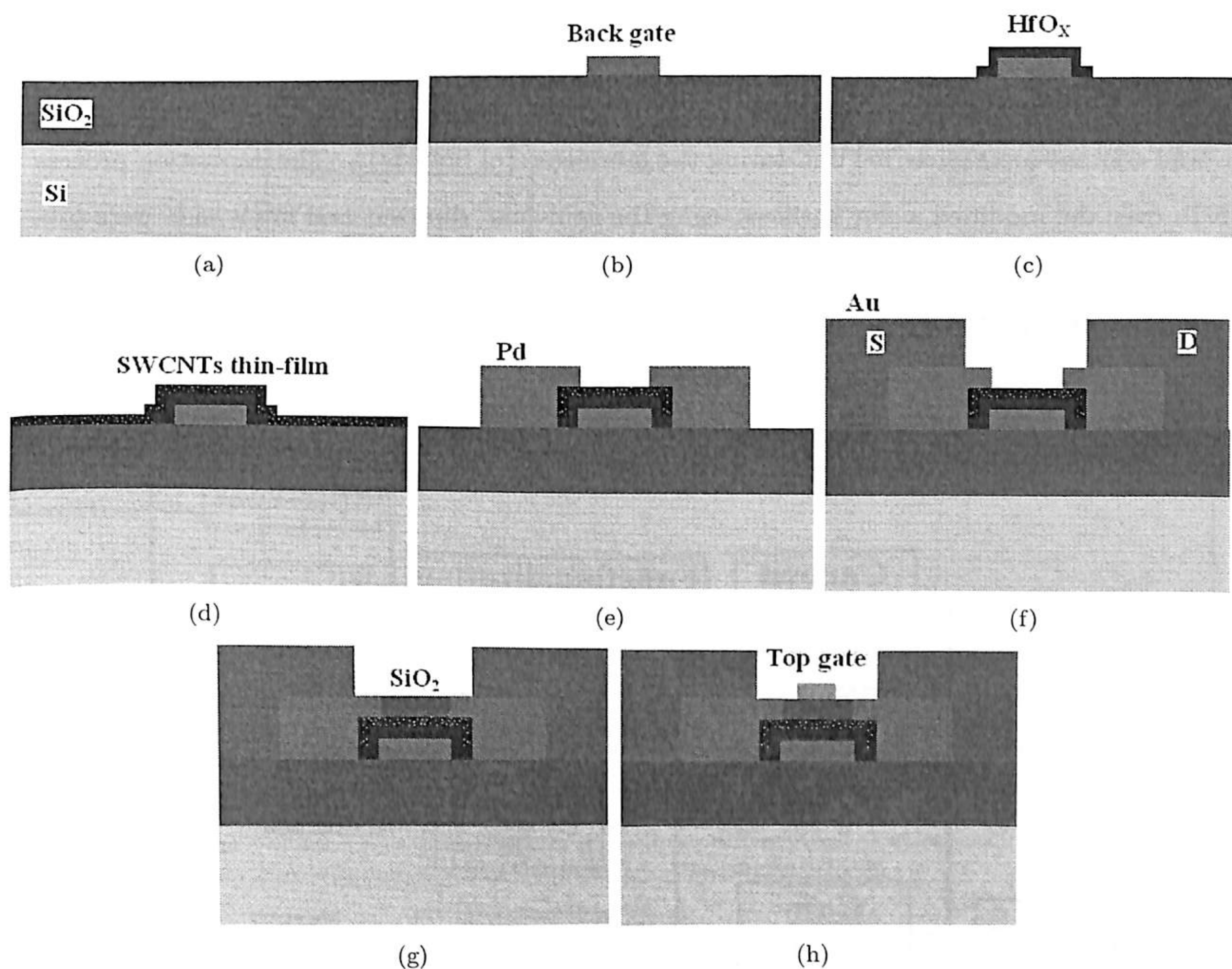

Figure 4.16: Process flow for the fabrication of dual gate SN-TFT. (a) SiO_2 grown over the Si substrate. (b) Back gate on Si/SiO_2 surface after lift-off process. (c) Deposition of HfO_X layer as dielectric for back gate. (d) Thin-film of SWCNTs deposited on the silanized oxide surface. (e) Palladium deposition for source and drain contacts. (f) Gold deposition for large area contact pads. (g) Deposition of SiO_2 layer as dielectric for top gate. (h) Tungsten deposition to realize the top gate structure of the dual gate SN-TFT.

TH-1861_07610208

4.4 Summary

In this chapter, process flow for various types of SN-TFTs using different gate dielectric material, source/drain contact geometries and gate structures having different purity of s-SWCNTs are discussed. Fig. 4.17 summarizes the different thin-film depositions such as SWCNT, gate dielectric materials and contact metals carried out during the fabrication of SN-TFTs. The deposition process of SWCNTs over the modified wafer surfaces using the spin-coat, dip-coat and immersion were presented separately. SiO_2 is grown by the thermal oxidation and deposited by the FIB technique, and HfO_X is deposited by the RF sputtering. The deposition of Au, Pd and Cr for the terminal contacts were carried out using the RF sputtering and W by the FIB technique.

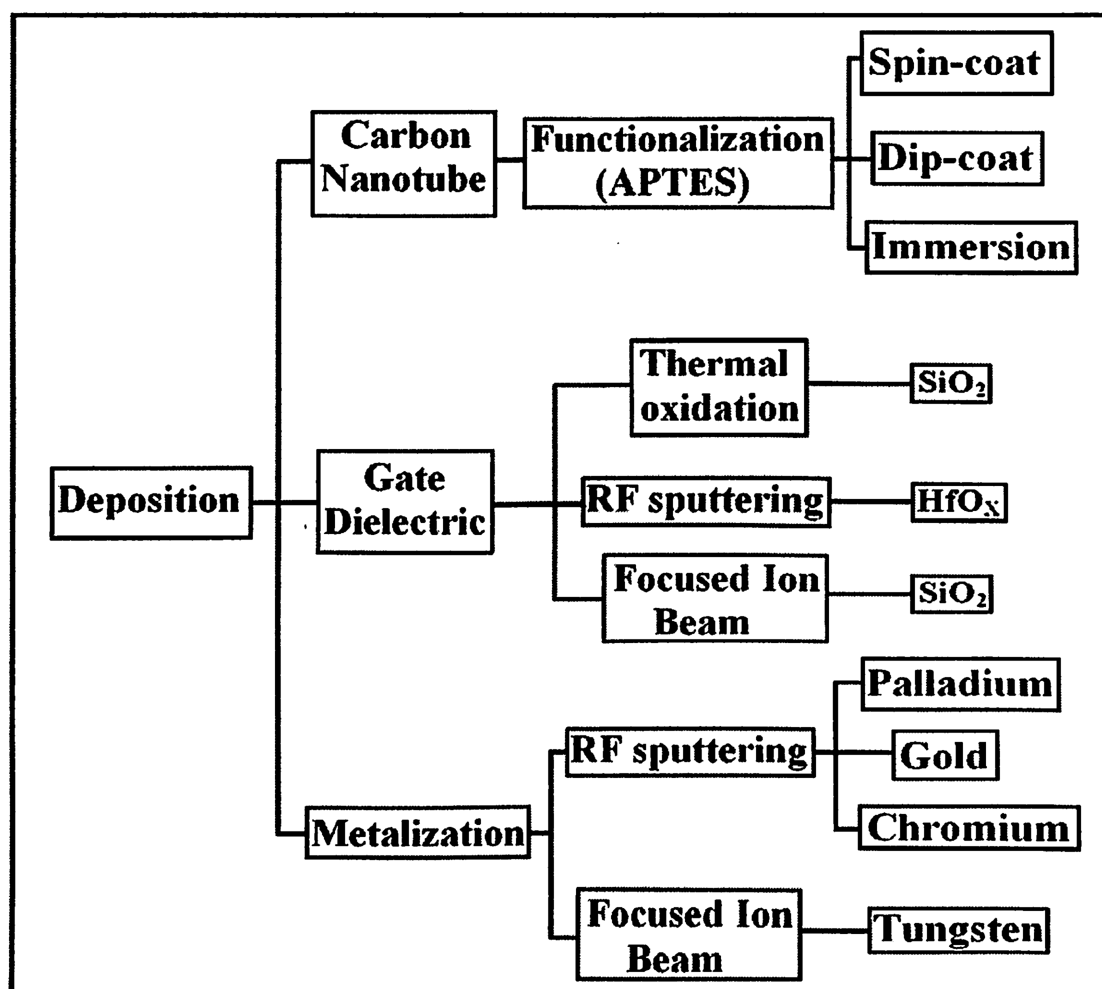

Figure 4.17: Summary of different thin-film depositions carried out during the fabrication of SN-TFTs.

Fig. 4.18 shows 9 different types of SN-TFTs fabricated in this work. The process flow of wafer

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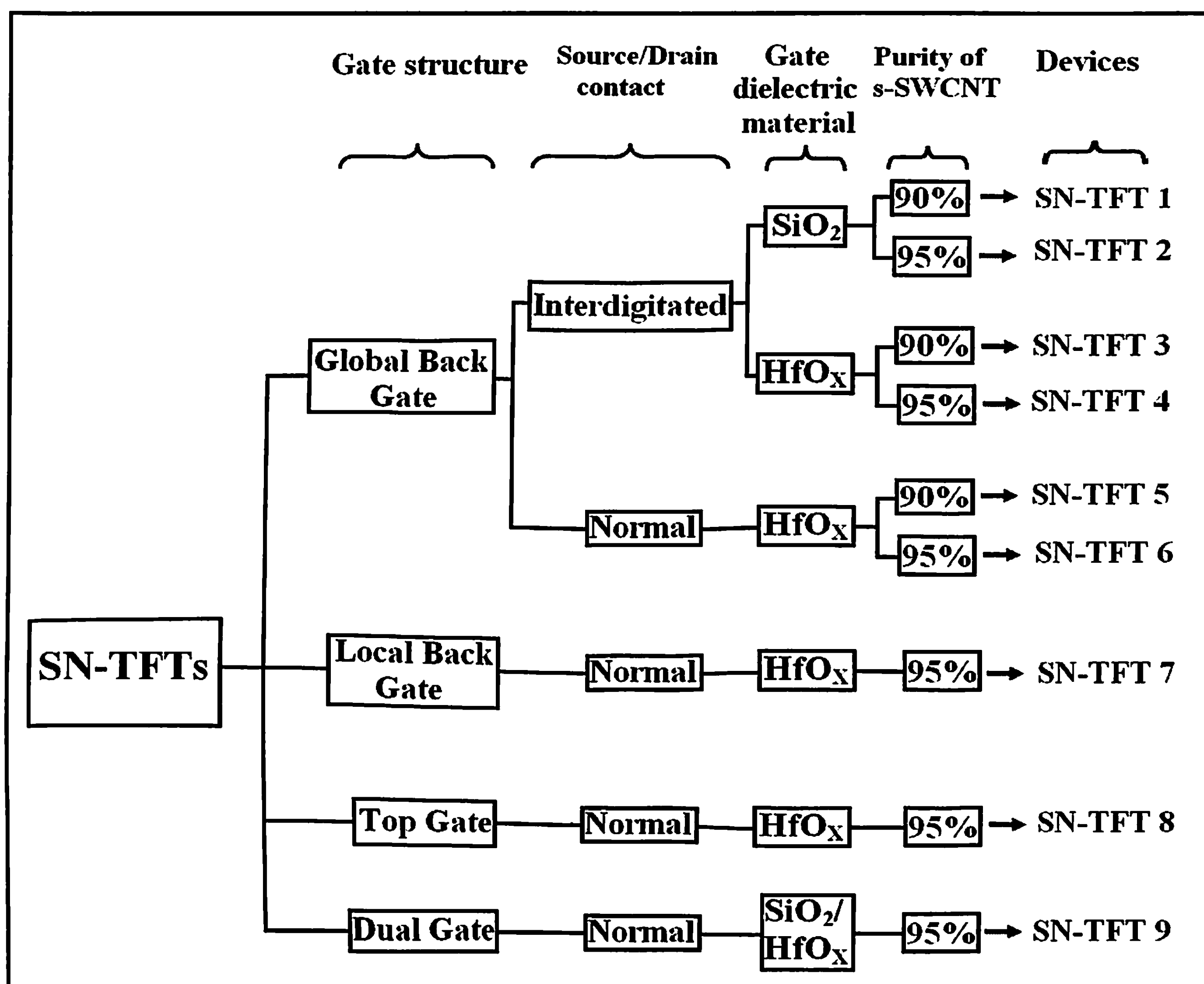

Figure 4.18: Summary of SN-TFTs fabricated which includes different gate structures, different source/drain contacts, different gate dielectric materials and different purity of s-SWCNTs.

scale global gate SN-TFTs having SiO_2 and HfO_X as the gate dielectric with thin-film of 90% and 95% purity s-SWCNTs with IDE and normal structures for source and drain contacts was presented. Wafer scale fabrication of local gate SN-TFTs with HfO_X as the gate dielectric were discussed in detail. Fabrication of a top gate SN-TFT using the FIB technique was presented and finally a dual gate SN-TFT with SiO_2 and HfO_X as the dielectric material for the top and the back gate, respectively was also presented.

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5

Wafer Scale Global Back Gate SN-TFTs having SiO_2 or HfO_X as Gate Dielectric

Contents

5.1 Introduction 78
5.2 Results of Material Characterization 79
5.3 Electrical Characterization Results of SN-TFTs having Different Gate Dielectric Material 80
5.4 Summary 84

TH-1861_07610208

5.1 Introduction

Bulk nanotube materials may never achieve electrical performance similar to that of the individual tubes, but they may nevertheless sufficient for many applications. In last decade, SN-TFTs have made significant progress in terms of developing techniques to deposit high density thin-film of aligned or random SWCNTs [46, 47, 49], achieving good performance wafer scale devices [46, 48, 49] and fabricating devices on flexible surfaces [115, 116]. The SN-TFTs with SWCNT thin-film of different purity of s-SWCNT [37, 38, 46, 47, 49] have shown a higher mobility compared to the conventional organic TFTs. A systematic investigation of the gate dielectric material based SN-TFTs are targeted in this study. The survey of CNFETs, which are based on individual SWCNTs shows the use of HfO_2 [34], zirconium oxide [117] and aluminum oxide (Al_2O_3) [118] as the gate dielectric material. However, a survey of the fabricated SN-TFTs indicates that most of the devices use SiO_2 as the gate oxide material and Even though Al_2O_3 is used as the gate dielectric material for a top gate SN-TFT fabrication [113], the thin film of SWCNTs was deposited over the SiO2 surface.

Replacing the SiO_2 gate dielectric with a high-k material allows an increased gate capacitance without the adverse leakage effects. While extensive literature is available on the high-k material incorporation in SN-TFTs, it has been observed that no studies have been reported exclusively comparing the effects of the dielectric material on SN-TFTs. In this chapter, electrical performance of wafer scale SN-TFTs having SWCNT thin-film deposited over the silanized HfO_X or SiO_2 surface is presented. The wafer scale demonstration is important as it provide added information such as repeatability, yield of the process involved and performance variations among the devices across the wafer. For a fair performance comparison, the SN-TFTs of identical dimensions fabricated under similar process conditions are considered.

The sections of the chapter are arranged as follows. Section 5.2 presents the characterization of SWCNT thin-film deposited over different gate dielectric surfaces. In section 5.3 electrical characterization results of wafer scale SN-TFTs of various channel dimensions fabricated under similar process conditions using SiO_2 or HfO_X as gate oxide material are discussed. Section 5.4 summarizes the chapter.

TH-1861_07610208

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5.2 Results of Material Characterization

In this section, the SWCNT material characterization is presented. The details of SWCNT thin-film deposition over the modified HfO_x and SiO_2 surfaces is done using the dip-coat technique as discussed in the chapter 4. The characteristics of the SWCNT thin-film having 95% purity s-SWCNTs such as diameter, length and semiconducting purity are presented.

Raman spectroscopy is a good tool for examining the structural and electronic properties of CNTs and in particular SWCNTs [119]. Diameter, chirality, and phonon structure are reflected in first- and second-order Raman frequencies, i.e. radial breathing modes (RBM, 150 - 350 cm^{-1}) and carbon-carbon stretching in the graphene plane (G band, 1565 - 1595 cm^{-1}). The Raman spectra of the SWCNT thin-film with 95% purity of s-SWCNTs deposited on the APTES functionalized HfO_x and SiO_2 surfaces are measured using Horiba Jobin HR 800 system with a laser excitation frequency of 514.5 nm.

The RBM and G-mode are diameter sensitive. Fig. 5.1 shows the Raman spectroscopy data recorded for the samples deposited with 95% enriched s-SWCNT thin-film. The Raman data recorded over a wide range of Raman shift from 50 - 3000 cm^{-1} has clear characteristic peaks such as RBM, disordered band (D band), graphite band (G band) and G$'$ band in Fig. 5.1(a). The spectroscopic details over the RBM and G-band regions for the SWCNTs give a qualitative indication of the relative population of semiconducting to metallic SWCNTs over the wafer surface. Kataura et al. [120] reported that the Raman peaks around 160 - 200 cm^{-1} and 200 - 280 cm^{-1} are due to semiconducting and metallic SWCNTs respectively. The Raman spectrum data obtained for a wafer with SWCNTs deposited on the HfO_x surface has intensity peaks at Raman shift of ranging from 160.2 to 180.2 cm^{-1} in the RBM region as shown in Fig. 5.1(b). Similarly the Raman data of the SWCNTs deposited on the SiO_2 surface is shown in the Fig. 5.1(c) and the intensity peaks are located at less than 200 cm^{-1} indicates that the SWCNT thin-film has majority of s-SWCNTs thus confirming its high purity and a much narrower G band characteristics of the SWCNTs in Fig. 5.1(a) further supports the same. RBM can be used to study the SWCNT diameter through its frequency ω_{RBM}. The SWCNT diameter is calculated using the equation (5.1), where A and B parameter values are determined experimentally as 248 cm^{-1} and 10 cm^{-1} respectively [121], and d_t is the SWCNT diameter in nm. The obtained range of the SWCNT diameters are from 1.37 nm to 1.56 nm. The Raman data of these plots confirm the high purity of s-SWCNTs with very less traces of

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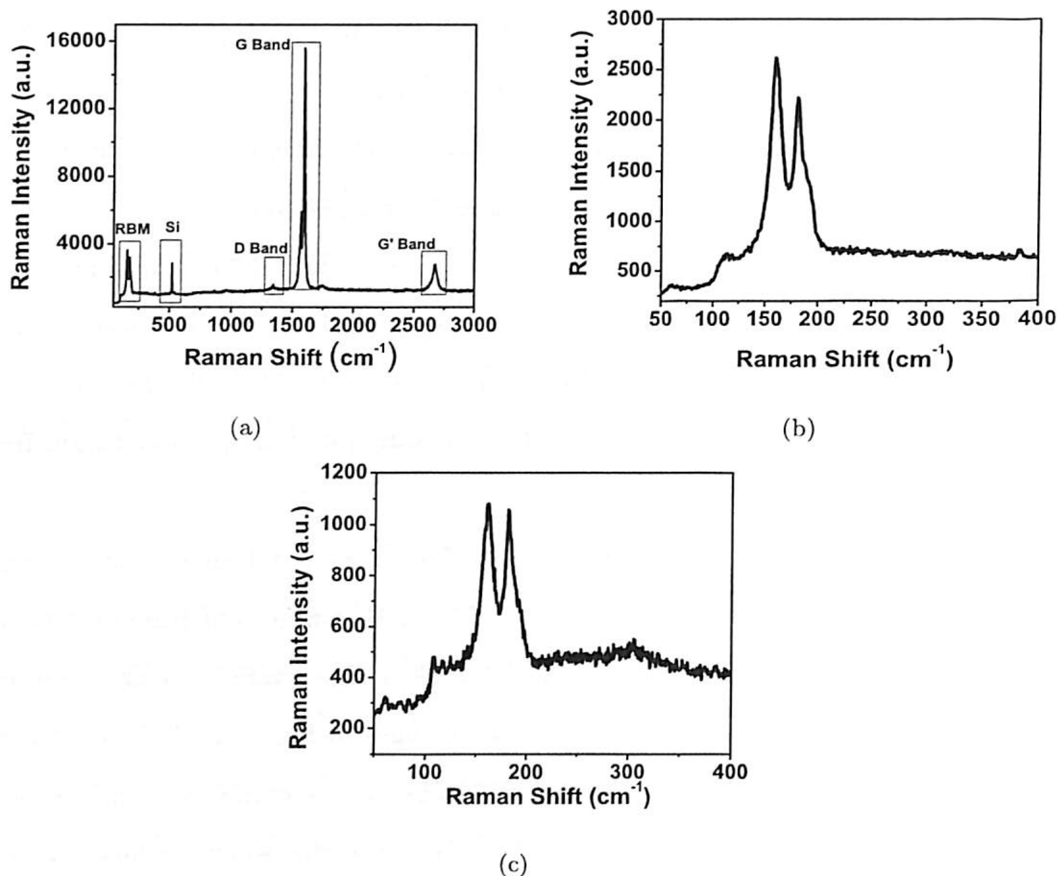

Figure 5.1: Raman spectroscopy data of the SWCNT thin-film with 95% purity s-SWCNTs. (a) Raman data indicating characteristics peaks RBM, D band and G band. (b) RBM data of SWCNTs deposited on HfO_X surface. (c) RBM data of SWCNTs deposited on SiO_2 surface.

m-SWCNTs.

$$\omega_{RBM} = \frac{A}{d_t} + B \tag{5.1}$$

The SWCNTs used in this work are synthesized using the arc discharge technique. The data provided by the vendor indicated that SWCNTs have length ranging from 100 nm to 4 μm with a mean length of 1 μm as shown in Fig. 5.2.

5.3 Electrical Characterization Results of SN-TFTs having Different Gate Dielectric Material

In this section, the electrical performance of wafer scale global gate SN-TFTs fabricated under similar process conditions with an identical channel dimensions having either SiO_2 or HfO_X as the gate dielectric material is analyzed. The SN-TFTs having IDE source/drain contact and a thin-film

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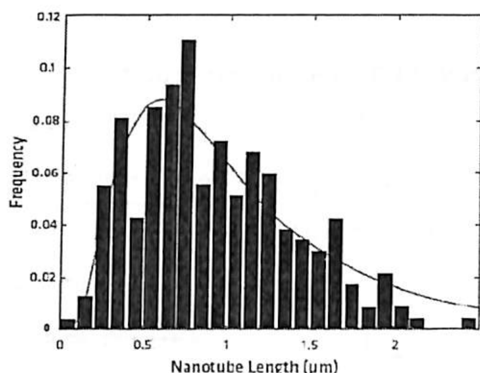

Figure 5.2: Atomic force microscopy data indicates that SWCNTs range in length from approximately 100 nm to 4 microns (Courtesy: NanoIntegris Inc.).

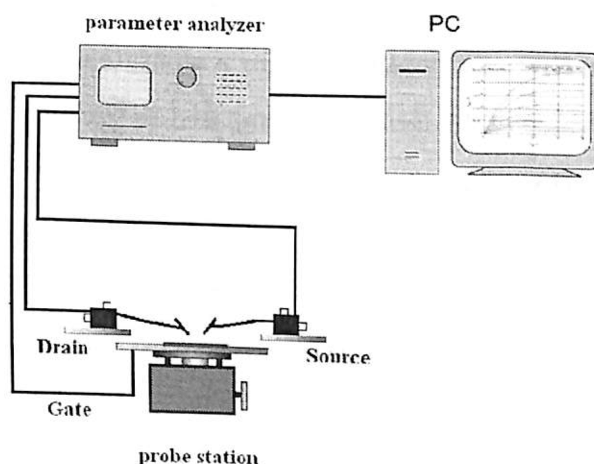

Figure 5.3: Experimental setup to characterize global gate SN-TFTs.

of 95% purity s-SWCNTs are considered.

The electrical characterization of the SN-TFTs is carried out using Keithley Polaris system probe station. The current-voltage (*I*-*V*) characteristics of the wafer scale devices fabricated on the 2 inch Si wafer are carried out at room temperature using the experimental setup shown in Fig. 5.3. The global back gate SN-TFTs in which the back side of the substrate itself acts as the gate contact. The wafer is placed on the chuck of the probe-station and contact probes are carefully placed over the source and drain contacts without damaging the pads. Depending on the required characteristics, the voltage of the corresponding terminal is varied as per the required resolution. The recorded *I*-*V* values are further used to plot the relevant characteristics of the device.

Each of the wafer consists of 80 transistors of various dimensions. The SN-TFTs considered

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for the analysis have IDE source/drain contacts of channel lengths 20, 50 and 100 μm and width ranges from 2300 to 31600 μm. Both SiO_2 and HfO_X based SN-TFTs have exhibited a p-type output characteristics with distinct linear and saturation region of characteristics. The output characteristics of a typical device having the channel length of 50 μm and the width of 2300 μm are shown in Fig. 5.4(a). The output conductance ($g_{ds} = dI_D/dV_{DS}$) of the typical device is 2.32 μS at V_{GS} of -3 V. The linear region of the output characteristics shown in Fig. 5.4(b) indicates an ohmic contact between SWCNTs and source/drain electrode (Pd) of the device.

The dielectric constant of the HfO_X is found to be 12 by a separate capacitance measurement and is substantially higher than the value of 3.9 for SiO_2. Compared to the 50 nm thickness of SiO_2, the equivalent electrical thickness of HfO_X layer is 65 nm, though the corresponding physical thickness is 200 nm. The oxide capacitance is estimated using the equation $C_{OX} = \varepsilon_{ox}/T_{eq}$, where ε_{ox} and T_{eq} are the gate dielectric constant and equivalent thickness respectively. The oxide capacitance of HfO_X based SN-TFTs is 1.3 times smaller compared to the device with SiO_2 as the gate dielectric. Fig. 5.4(c) shows the transfer characteristics exhibited by SiO_2 and HfO_X based SN-TFTs. It may be noted that the device based on the HfO_X has a lower threshold voltage of -1.5 V as against -1.8 V for the SiO_2 based SN-TFT. The improvement in the threshold voltage by 300 mV for the HfO_X based SN-TFTs may be attributed to the difference in charge in the oxide or at the CNT/oxide interface. It may be noted that the difference in on-current of the two types of devices is increasing for higher gate voltages. This is due to the lower threshold voltage of high-k based device compared to the other. The subthreshold swing of the HfO_X based SN-TFT is measured to be 750 mV/decade and is found to be steeper compared to 850 mV/decade for devices with SiO_2 as the gate oxide. The steeper subthreshold swing of HfO_X based device is again due to the incorporation of high-k dielectric material as gate oxide. The current-voltage relationship obtained for these SN-TFTs is not square law dependent like in the case of a conventional MOSFET, but may be approximated that drain current of HfO_X based SN-TFT is proportional to $(V_{GS} - V_T)^{1.28}$ and for devices with SiO_2 gate dielectric material it is $(V_{GS} - V_T)^{1.38}$.

The electrical parameters of the wafer scale SN-TFTs having various dimensions with SiO_2 or HfO_X as gate dielectric are analyzed. Fig. 5.5 shows the performance such as, the on-current density (drain current/channel width I_D/W) and the transconductance normalized to the channel width (g_m/W) for various channel length of both SiO_2 and HfO_X based SN-TFTs. Fig. 5.5(a) shows the

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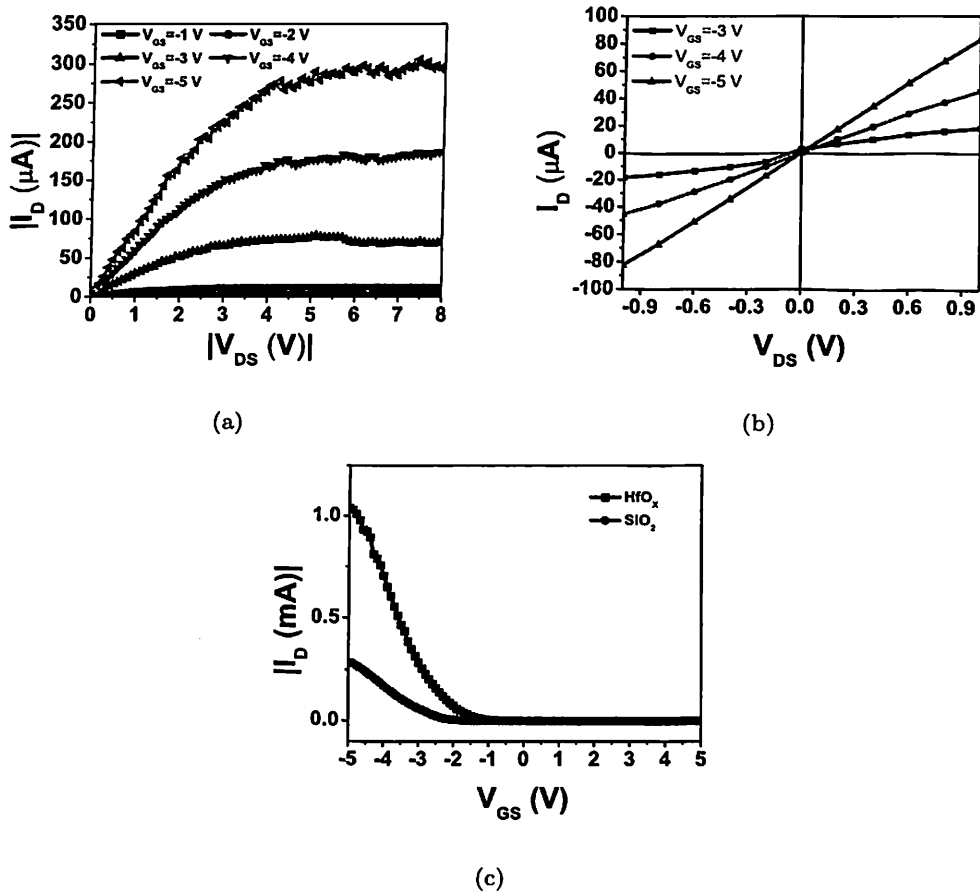

Figure 5.4: Electrical characteristics of SN-TFTs. (a) Output characteristics of SiO_2 based SN-TFT. (b) Triode region characteristics of SiO_2 based SN-TFT. (c) Transfer characteristics of both SiO_2 and HfO_X based SN-TFTs.

I_D/W measured at V_{DS} of -2 V and V_{GS} of -5 V for both types of devices having various channel lengths. Due to higher dielectric constant and reduced threshold voltage, the average on-current of the HfO_X based devices is about two times more compared to the devices with SiO_2 gate oxide. Due to high on-current, HfO_X based SN-TFTs have more current density compared to the SiO_2 based devices for various channel length. However, for each case, the current density decrease as the channel length increases, due to the larger thin-film resistance of longer channels and also due to the possible non-continuity between the SWCNTs along the length of channel as the average length of the SWCNT is only about 1 μm. The resistance of the thin-film channel for various channel lengths of both SiO_2 and HfO_X based devices is measured from the linear region of output characteristics and the same is shown in Fig. 5.5(b). The on-resistance of a typical SiO_2 based SN-TFT of channel

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length 20 μm is 38.14 MΩ and the same for devices having channel lengths of 50 and 100 μm is 81.25 and 172.65 MΩ, respectively and all obtained at a V_{GS} of -5 V. The on-resistance of the HfO_X based SN-TFTs for identical dimensions is lower compared to the SiO_2 based devices as shown in Fig. 5.5(b). Even though the intrinsic resistance of the individual SWCNT is 6.5 KΩ, the thin-film consists of many random SWCNTs of average length 1 μm and therefore the resistance of the SWCNT thin-film is in the order of MΩs due to several high resistance tube-to-tube contacts [38]. The contact resistance is larger for longer channel devices as there will be more number of tube-to-tube contacts for the formation of a longer channel device. Another important device parameter, the transconductance (g_m) is calculated using the slope of SN-TFTs transfer characteristics at V_{DS} of -2 V. Because of higher dielectric constant, the SN-TFTs based on HfO_X have shown a maximum g_m value at V_{GS} of -3.7 V, which is lower by 400 mV compared to SiO_2 based devices. The slope at a V_{DS} of -2 V from the transfer characteristics of SN-TFTs is considered for the calculation of transconductance. The plots in Fig. 5.5(c) indicate a higher normalized transconductance values for the HfO_X based SN-TFTs compared to the SiO_2 based devices of various channel length.

The electrical parameter of SiO_2 and HfO_X based SN-TFTs are compared in the Table 5.1. The HfO_X based SN-TFTs have shown reduced threshold voltage and steeper subthreshold slope compared to devices with SiO_2 gate oxide. The on-off current ratio of SN-TFTs with high-k gate oxide device is comparable to SiO_2 based device. However, the SN-TFT with high-k gate oxide has exhibited greater current density when compared to SiO_2 based device. The carrier mobility (μ) of the device is calculated using the standard formula (5.2) [49]. Where L_{ch} is the channel length, T_{ox} is the gate oxide thickness, ε_{eff} is the effective dielectric constant of the oxide material and W is the channel width. For SiO_2 and HfO_X based SN-TFTs, the maximum carrier mobility obtained for a channel length of 100 μm is 4.68 and 32.6 cm^2/V·s respectively. The higher mobility value for the HfO_X based SN-TFT is corresponding to their higher g_m value obtained at a lower gate voltage.

$$\mu = \frac{L_{ch} T_{ox} g_m}{\varepsilon_{eff} V_{DS} W} \tag{5.2}$$

5.4 Summary

In this chapter, the material characteristics of the SWCNT thin-film deposited on different gate dielectric material was presented. A study on the electrical performance of various SN-TFTs based

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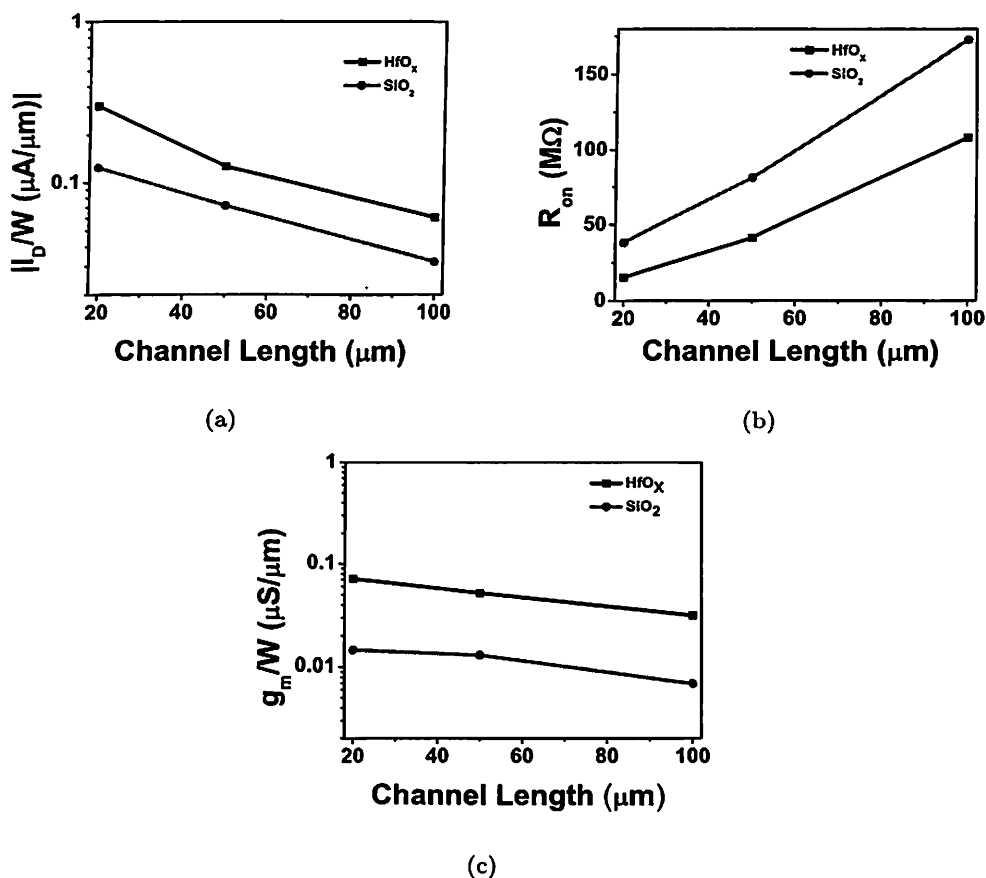

Figure 5.5: Electrical parameters of SN-TFTs based on both SiO_2 and HfO_X gate dielectric, as a function of channel length. (a) Current density, I_D/W (μA/μm). (b) On-resistance. (c) Normalized transconductance.

Table 5.1: Performance comparison of SiO_2 and HfO_X based wafer scale SN-TFTs.

Parameter	SN-TFT$_{SiO_2}$	SN-TFT$_{HfO_X}$
Gate-dielectric	SiO_2	HfO_X
Dielectric thickness (nm)	50	200
Threshold voltage (V)	-1.8	-1.5
Subthreshold slope (V/decade)	0.85	0.75
On-off current ratio	6×10^4	7.45×10^4
Current density I_D/W (μA/μm)	0.12	0.302
Normalized transconductance g_m/W (μS/μm)	0.013	0.071
Carrier mobility (cm^2/V·s)	4.68	32.6

TH-1861_07610208

on SiO_2 and HfO_X gate dielectric material was presented. The devices having an identical dimensions fabricated under identical process conditions were considered for the performance comparison. SN-TFTs based on the HfO_X gate dielectric had shown reduced threshold voltage by 300 mV compared to the SiO_2 based devices. The SN-TFTs with a high-k dielectric gate oxide also have exhibited a steeper subthreshold slope, large on-current and higher transconductance compared to the SiO_2 based devices of identical channel dimensions.

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6

Wafer Scale Global Back Gate SN-TFTs having Thin-Film of 90% or 95% purity s-SWCNTs

Contents

6.1 Introduction 88
6.2 Results on Purity of s-SWCNTs 89
6.3 Electrical Characterization Results of Wafer Scale Interdigitated Type SN-TFTs 90
6.4 Performance Comparison of Wafer Scale SN-TFTs having Different Purity s-SWCNTs 94
6.5 High Performance and High On-Current SN-TFT 98
6.6 Summary 100

TH-1861_07610208

6.1 Introduction

The SWCNTs to be used for the transistor application must exhibit semiconducting property and the percentage of the m-SWCNTs of the thin-film plays a significant role in the device performance. The as-grown SWCNTs typically consist of only 67% of s-SWCNTs and the remaining will be metallic in nature. As most of the current conduction is through the m-SWCNTs especially at lower gate voltages, their on-currents will be higher, but the off-currents are also significantly higher and therefore SN-TFTs fabricated using thin-film of as-grown SWCNT suffer from a poor on-off current ratio [37,38] which leads to power consumption even during the switched-off condition. Depending on the purity of s-SWCNTs, the properties of SN-TFTs vary. Therefore it is possible to have SWCNT thin-films of various purity of s-SWCNTs. The SN-TFTs with as-grown SWCNT thin-film [37,38,47] have shown a higher mobility compared to the conventional organic TFTs, but suffer from a low on-off current ratio. This disadvantage is resolved by using sorted nanotubes with higher percentage of s-SWCNTs. A review of the literature reveals a number of demonstrations of SN-TFTs using SWCNTs with different semiconducting purity [46–49, 113]. Wang et al. [46] have reported a wafer scale SN-TFTs using 95% s-SWCNTs and Engel et al. [49] have reported the SN-TFTs using 99% s-SWCNTs achieving better performance compared to the lower purity s-SWCNTs. In reality, the performance of a SN-TFT is also influenced by the channel dimensions and the process conditions. In this chapter, a systematic investigation on the impact of SWCNT semiconductive purity on the device performance is carried out for the wafer scale devices of identical dimensions fabricated under similar process conditions. For this investigation, both SiO_2 and HfO_x based wafer scale SN-TFTs having 90% and 95% purity s-SWCNTs are considered.

The analysis of the high performance SN-TFTs with the high on-current capability is also presented. There are many applications wherein it is desirable to have a TFT capable of providing relatively high output currents and operating at high speeds. One such application is the large area liquid crystal displays wherein the transistors are called upon to drive the individual pixels of the displays. The organic TFTs have received significant attention, but suffer from relatively a low device mobility. The SN-TFTs have recently attracted lot of attention due to their potential to replace amorphous or polycrystalline silicon TFTs for active matrix liquid crystal displays. The back gate SN-TFTs have exhibited a maximum on-current in the range of 2 to 6 mA [46, 47] and the top gate SN-TFTs have exhibited 1 mA [49]. The top gate SN-TFTs need additional process steps such as

TH-1861_07610208

the metallization and the lithography over the deposited SWCNTs. In order to use SN-TFTs for the display applications one requires not only the high current, but also adequate values of other device parameters such as the threshold voltage, on-off ratio, on-state conductance and carrier mobility. Most of the SN-TFTs reported in the literature have the thin-film of SWCNTs deposited on the modified Si/SiO_2 surface [37, 38, 46–49]. In this work, HfO_x is used as the gate dielectric material and the thin-film of SWCNTs are deposited over the modified HfO_x surface. This helped to achieve a low voltage operation, much steeper subthreshold voltage swings and higher transconductance values. The report indicates that the short channel length devices formed with an average SWCNT lengths of 1.7 μm [46] have exhibited a high on-current, but with a poor on-off ratio. In this work, SWCNTs with shorter average lengths (1 μm) are used and thereby mitigated poor on-off ratio caused by the presence of longer length m-SWCNTs. However, shorter average length of SWCNTs would increase the contact resistance between SWCNTs and care must be taken to retain the device performance such as mobility and transconductance. The high density SWCNTs are deposited to exploit the high current carrying capacity of the SWCNTs at reduced channel lengths.

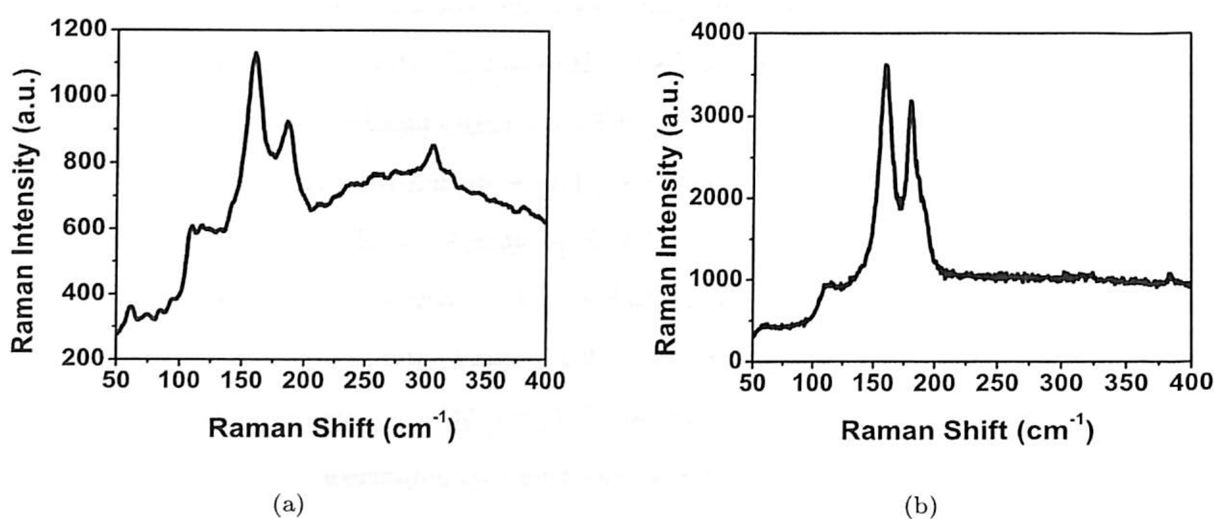
The sections of the chapter are arranged as follows. The section 6.2 gives the details of the semiconducting purity of the SWCNTs. The section 6.3 presents the analysis of electrical characterization results of wafer scale IDE SN-TFTs having 90% and 95% purity s-SWCNTs deposited on SiO_2 and HfO_x surface. Section 6.4 deals with the performance comparison of wafer scale SN-TFTs with different purity s-SWCNTs. Section 6.5 presents a discussion on the high performance and high on-current SN-TFT. Finally the chapter is summarized in section 6.6.

6.2 Results on Purity of s-SWCNTs

In this section, the purity of s-SWCNTs deposited on different silanized gate oxide surfaces are presented. The semiconducting purity the SWCNT thin-film deposited on the wafer are verified using the Raman spectroscopy data obtained using Horiba Jobin HR 800 system with a laser excitation frequency of 514.5 nm. The Raman spectra of the SWCNT thin-film of different semiconducting purity deposited on the APTES functionalized HfO_x surfaces are shown in Fig. 6.1. The spectroscopic details over the RBM region for the SWCNTs give a qualitative indication of the relative population of semiconducting to metallic SWCNTs deposited over the wafer surface. Kataura et al. [120] reported that the Raman peaks around 160 - 200 cm^{-1} and 200 - 280 cm^{-1} are due to s-

TH-1861_07610208

and m-SWCNTs, respectively. The Raman spectrum of the random network of SWCNTs in RBM region for 90% purity sample showed a peak beyond 200 cm^{-1} and such a Raman shift shown in Fig. 6.1(a) indicates the presence of the m-SWCNTs. However, RBM data for 95% semiconducting purity case in Fig. 6.1(b) is dominated by spectroscopic features of the s-SWCNTs as there are no peaks beyond 200 cm^{-1} [120]. The peaks before 200 cm^{-1} indicates the presence of high percentage of s-SWCNTs.



(a) (b)

Figure 6.1: Raman spectroscopy data for the SWCNTs on silanized oxide surface. (a) RBM data obtained for 90% pure s-SWCNTs. (b) RBM data for sample with 95% s-SWCNTs.

6.3 Electrical Characterization Results of Wafer Scale Interdigitated Type SN-TFTs

In this section, the electrical characterization of the global gate SN-TFTs having IDE source/drain contacts is presented. The electrical measurements are carried out using Keithley Polaris system probe station. The electrical performances of SN-TFTs having thin-film of 90% or 95% enriched s-SWCNTs deposited on an amino-silane modified HfO_x or SiO_2 surfaces are considered for the analysis.

90SN-TFT and 95SN-TFT abbreviations are used hereafter to indicate SN-TFT having SWCNTs of 90% and 95% semiconducting purities, respectively. Fig. 6.2 shows the electrical characteristics exhibited by the 95SN-TFT of a typical dimension of channel length 20 μm and width 16600 μm. Fig. 6.2(a) shows an excellent p-type output characteristics exhibited by 95SN-TFT with a distinct

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linear and saturation region of operation for the V_{GS} ranging from -1 V to -5 V in steps of -1 V. The g_{ds} of 95SN-TFT is 8 μS measured at a V_{GS} of -3 V. The transfer characteristics of back gated SN-TFTs shown in Fig. 6.2(b) are obtained by varying the gate voltage from -5 V to 5 V, at a constant V_{DS} of -2 V. It may be noted in Fig. 6.2(b) that the drain currents of both SN-TFTs are almost identical at larger negative values of V_{GS}, as both s-SWCNTs and m-SWCNTs carry same currents. However, at lower negative and positive values of V_{GS}, the drain current of the 90SN-TFT is more compared to the 95SN-TFT. This is because m-SWCNTs do not need V_{GS} driven channel formation for the current conduction. The drain currents of 90SN-TFT and 95SN-TFT are 2.17 mA and 1.91 mA, respectively at a V_{GS} of -5 V. However, the drain current measured at V_{GS} of 5 V for a 90SN-TFT is 1.83 μA and it is 98.6 nA for a 95SN-TFT. In other words, the on-off current ratio of the 90SN-TFT is 1.18×10^3 and that of the 95SN-TFT it is 1.93×10^4. The on-off current ratios of SN-TFTs with SWCNT thin-film on the HfO_x dielectric are comparable to SN-TFTs with SWCNTs on the SiO_2 surface reported in the literature [46].

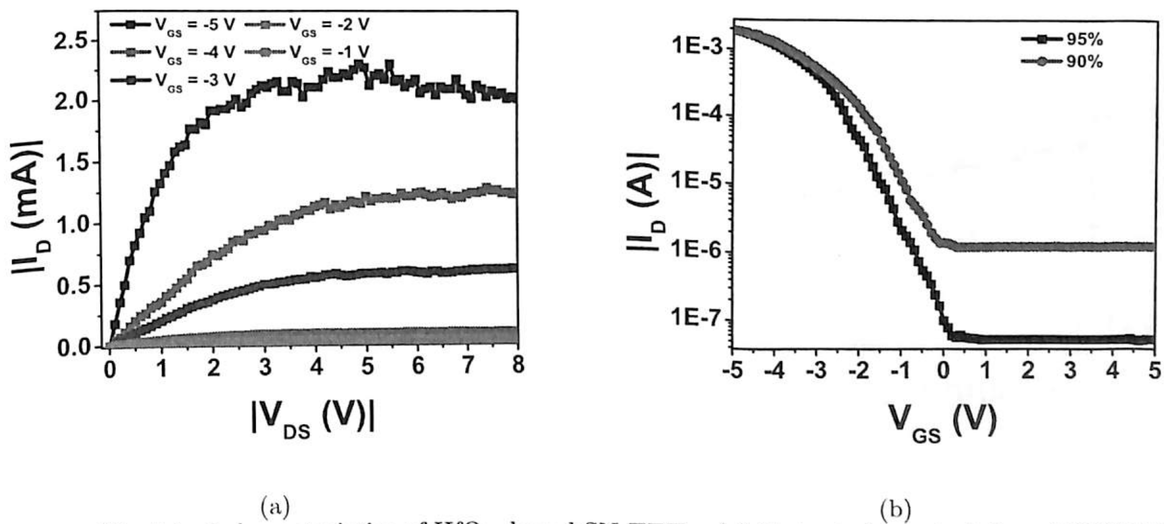

Figure 6.2: Electrical characteristics of HfO_x based SN-TFTs. (a) Output characteristics of 95SN-TFT. (b) Transfer characteristics of both 90SN-TFT and 95SN-TFT.

Fig. 6.3 shows the electrical parameters of SN-TFTs having 90% and 95% purity s-SWCNTs such as on-off current ratio, current density, normalized transconductance and carrier mobility as a function of the channel length. Fig. 6.3(a) shows the ratio of on and off currents measured at V_{GS} of -5 V and V_{GS} of 5 V, respectively at a constant V_{DS} of -2 V. The on-off current ratio of the 95SN-TFT is always higher compared to the 90SN-TFT. The reason for reduction in on-off current ratio

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(a)

(b)

(c)

(d)

Figure 6.3: Electrical parameters of wafer scale HfO_x based SN-TFTs having 90% or 95% purity s-SWCNTs plotted as a function of channel length. (a) Average drain current on-off ratio. (b) On-current density (I_D / W). (c) Normalized transconductance. (d) Carrier mobility.

of 90SN-TFT is the high off-state current of the device due to the presence of more m-SWCNTs in the channel, which will anyhow conduct even without the gate potential. Nevertheless, the obtained on-off current ratio of the 90SN-TFTs is higher when compared to other reported devices using the as-grown SWCNTs [37,47]. In order to obtain better on-off current ratio devices, much higher purity s-SWCNTs are required and in literature a highest on-off ratio more than 10^5 is reported for the devices using 99% enriched s-SWCNTs [49].

The I_D / W of both 90% and 95% purity s-SWCNTs for various channel lengths are plotted in

TH-1861_07610208

Table 6.1: Performance comparison of 4 different wafer scale fabricated SN-TFTs with interdigitated source/drain contacts.

Parameter	95SN-TFT	90SN-TFT	95SN-TFT	90SN-TFT
On-off current ratio	6×10^4	4×10^3	7.45×10^4	4.5×10^3
Current density (μA/μm)	0.12	0.16	0.302	0.41
Normalized transconductance (μS/μm)	0.013	0.014	0.071	0.075
Carrier mobility (cm^2/V·s)	4.68	5.02	32.6	33.8
s-SWCNT purity (%)	95	90	95	90
Gate-dielectric	SiO_2	SiO_2	HfO_X	HfO_X

Fig. 6.3(b). Because of the presence of more number of m-SWCNTs, the 90SN-TFTs have exhibited a maximum I_D/W of 0.41 μA/μm, slightly higher value compared to the 95SN-TFTs. As explained earlier for longer channel lengths, due to non-continuity of the SWCNTs and higher channel resistance the on-current reduces and hence the current density also reduces with increase in the channel length as shown in Fig. 6.3(b).

Similarly Fig. 6.3(c) and 6.3(d) show the normalized transconductance and the carrier mobility of SN-TFTs as a function of the channel length. The mobility exhibited by SN-TFTs having 90% and 95% purity s-SWCNTs are higher compared to the devices which employed spin coating technique to deposit SWCNTs [49]. The carrier mobility of the SN-TFTs is higher than the mobility of the organic TFTs [109, 110]. However, the mobility values of the presented SN-TFTs are lower when compared to mobility values of 1-2 $\times$ 10^3 cm^2/V·s obtained for the transistors fabricated using individual SWCNTs [7, 122]. This may be because of very large tube-to-tube contact resistance of random SWCNTs network reported in thin-films [38].

Table 6.1 shows the comparison of electrical parameters exhibited by the SN-TFTs having SWCNTs of s-SWCNT purity 90% and 95% deposited on the silanized SiO_2 and HfO_X surface. Only the best parameter values exhibited by both types of devices are listed in Table 6.1. Compared to the 90SN-TFTs, the on-off ratio of the 95SN-TFTs is greater by at least by an order, and are suitable for digital switching applications. Because of higher percentage of m-SWCNTs, the current density of the 90SN-TFTs is higher compared to 95SN-TFTs. The normalized transconductance and mobility exhibited by SN-TFTs with 90% and 95% purity s-SWCNTs are comparable to each other.

In this section, the electrical characteristics of global gate SN-TFTs having IDE contacts with

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HfO_X and SiO_2 dielectric material and having different purity of s-SWCNTs are discussed. The SN-TFTs with 95% pure s-SWCNTs have shown a higher on-off current ratio compared to devices with 90% purity s-SWCNTs having identical channel dimensions processed under similar process conditions. The 90SN-TFTs have exhibited higher current density compared to the 95SN-TFTs due to higher percentage of m-SWCNTs.

6.4 Performance Comparison of Wafer Scale SN-TFTs having Different Purity s-SWCNTs

In this section, the electrical characterization of HfO_X based global gate SN-TFTs are presented. It may be noted that from henceforth the gate contact geometry is non-IDE type (normal) unless otherwise it is specifically mentioned as IDE type. The electrical performances of SN-TFTs are examined by obtaining the current-voltage characteristics using the Keithley Polaris probe station. The electrical characteristics of SN-TFTs having channel lengths 5, 10, 20, 30 and 40 μm and widths 10, 50, 100, 400 and 500 μm are obtained. The electrical performance of wafer scale HfO_X based SN-TFTs having s-SWCNTs of 90% or 95% purity, fabricated under similar process conditions is presented. The output and transfer characteristics of both types (90% and 95%) of SN-TFTs having identical channel dimension of length 30 μm and width 100 μm are presented here. The output characteristics of both types of devices shown in Fig. 6.4 are obtained for various V_{GS} ranging from -1 V to -5 V. Fig. 6.4 shows the p-type output characteristics exhibited by both types of devices with a distinct linear and saturation region. Fig. 6.4(a) shows the output characteristics of 95SN-TFT and has exhibited a maximum current of 113 μA at a V_{GS} of -5 V and the g_{ds} value is 0.307 μS at V_{GS} of -3 V. The triode region of the same for lower V_{DS} values shown in Fig. 6.4(b) indicates an ohmic contact between the source/drain contact and the SWCNTs as expected when Pd metal is used. Because of more m-SWCNTs, the 90SN-TFT of similar channel dimension has exhibited an on-current of 116.8 μA at a V_{GS} of -5 V which is marginally greater than the 95SN-TFT.

The transfer characteristics of both types of SN-TFTs are shown in Fig. 6.5. The 95SN-TFT's on-state current measured at V_{GS} of -5 V is 31.05 μA and the off-state current at V_{GS} of 5 V is 0.826 nA, resulting in an on-off current ratio of 3.75 $\times$ 10^4. The 95SN-TFT with HfO_X gate dielectric material has exhibited a steep subthreshold slope 600 mV/decade, when operated with V_{DS} of -2 V which is steeper than earlier reported similar type of devices [46]. Similarly, the transfer characteristics of 90SN-TFT is shown in Fig. 6.5. The device has exhibited an on-current of 32.25

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(a)

(b)

(c)

Figure 6.4: Output characteristics of global back gate SN-TFTs. (a) *I-V* plot of 95SN-TFT for various V_{GS} and V_{DS} ranging from 0 to -10 V. (b) Output characteristics of 95SN-TFT to study the linear region of operation for small drain voltage range of -1 V to 1 V. (c). Drain current variations of 90SN-TFT for various V_{GS}.

μA at at V_{GS} of -5 V and an off-current at V_{GS} of 5 V is 8.39 nA. This results in an on-off current of 3.84×10^3, which is less compared to the 95SN-TFT. The subthreshold slope of the 90SN-TFT is found to be 650 V/decade and is better than the SN-TFT having 95% s-SWCNTs reported in [46]. This improved performance of the lower purity s-SWCNT SN-TFT may be attributed to the use of a high-k gate oxide.

The yield obtained was 100% and all the back gate SN-TFTs of various channel dimensions are

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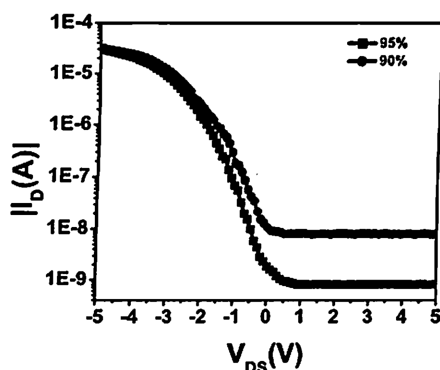

Figure 6.5: Transfer characteristics of global back gate SN-TFTs having thin-film of 90% and 95% s-SWCNTs.

characterized to compare their performance. The plots in Fig. 6.6 shows the performances of both types SN-TFTs of various dimensions fabricated on separate wafers. Fig. 6.6(a) shows performance of the SN-TFTs in terms of on-off current ratio, current density, transconductance and mobility for various channel dimensions. The on-off ratio exhibited by both types of devices as a function of the channel length, obtained by varying the V_{GS} from -5 V to 5 V, at a constant V_{DS} of -2 V are shown in Fig. 6.6(a). The 95SN-TFTs with the channel length more than 20 μm have shown an on-off ratio more than 10^4 and a maximum on-off ratio of 4×10^4 is exhibited by devices having a channel length 40 μm. The deposited SWCNT thin-film contains 95% s-SWCNTs and rest will be metallic. The on-off ratio of the devices of lower channel length is due to the possible bridging of source and drain contact by the m-SWCNTs. The on-off ratio exhibited by the proposed 95SN-TFT are in comparison with the similar type of devices reported in [46]. However, the gate voltage swing to obtain the on-off ratio is -10 V to 10 V for the reported devices [46] as against to, -5 V to 5 V for the proposed devices. This low voltage drive of the proposed device is due to high-k HfO_X gate oxide. For the given channel length, because of higher m-SWCNTs the on-off ratio exhibited by the 90SN-TFTs are less compared to the 95SN-TFTs as shown in Fig. 6.6(a).

The on-current exhibited by both types of SN-TFTs for various channel length as a function of channel width are plotted in Fig. 6.6(b). In both cases, wider channel SN-TFTs have exhibited larger on-current, as more SWCNTs are involved in the current conduction activity compared to narrow channel devices. As the channel length increases, due to non-continuity of the SWCNTs involved in the channel formation, the on-current reduces as shown in Fig. 6.6(b). However, the

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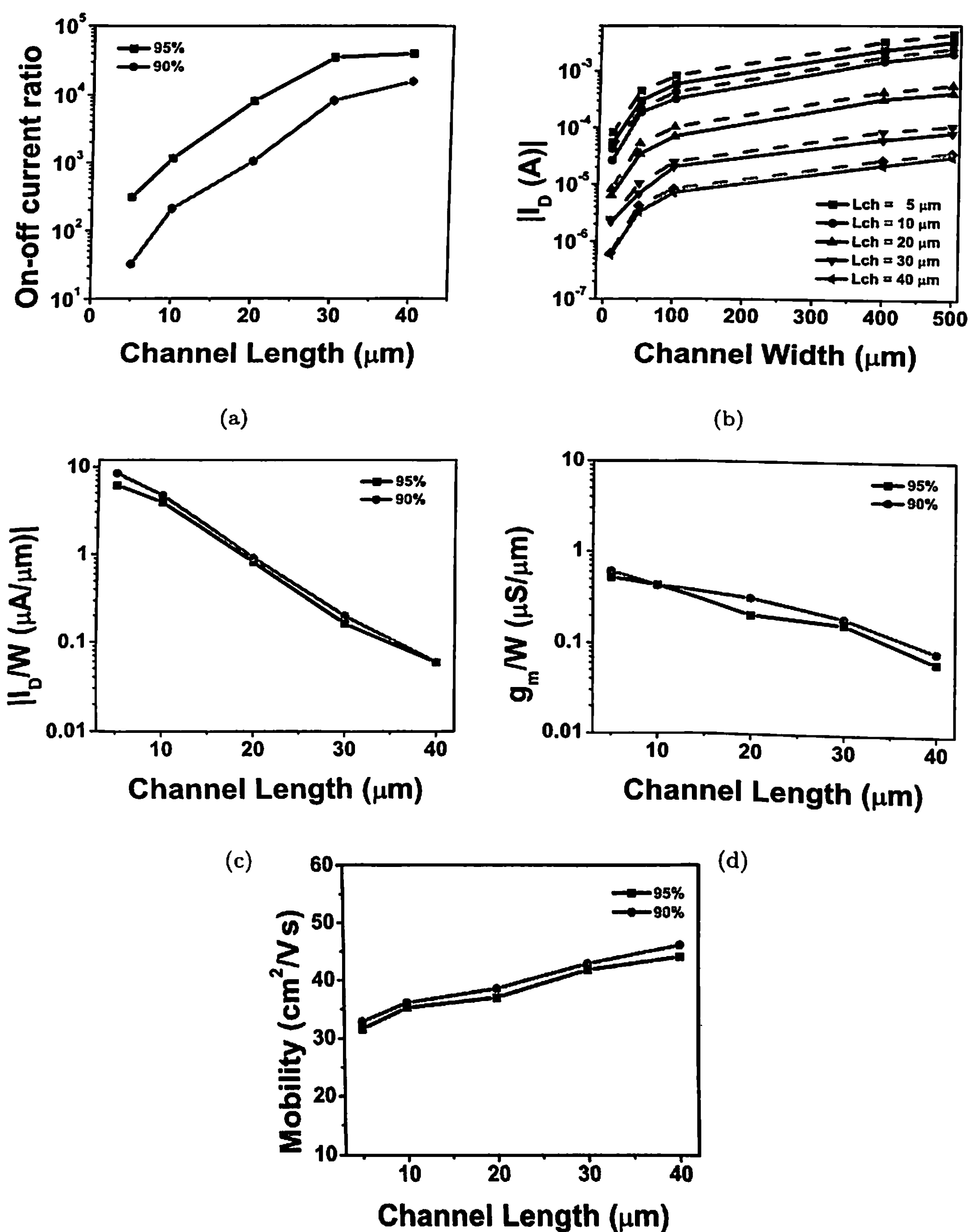

Figure 6.6: Statistical study of performance parameters of wafer scale global back gate SN-TFTs. (a) On-off ratio exhibited by both types of SN-TFTs based on 90 and 95% purity s-SWCNTs. (b) On-current exhibited by global gate SN-TFTs of various channel length having different channel width (solid line - 95SN-TFT, dash line - 90SN-TFT). (c) Average on-current density measured for both types of SN-TFTs for various channel length. (d) Normalized transconductance. (e) Mobility of devices with various channel length.

TH-1861_07610208

on-current is proportional to the channel width, because as the channel width increases the number of SWCNTs involved in the current conduction activity also increases. A maximum on-current of 3.1 mA (4.2 mA) is measured for a 95SN-TFT (90SN-TFT) having a channel length 5 μm and width 500 μm. Similarly the least on-current of 580 μA (620 μA) is measured for a 95SN-TFT (90SN-TFT) having channel length 40 μm and width 5 μm. It may noted that due to higher % of m-SWCNTs, the 90SN-TFTs have exhibited slightly larger on-current compared to the 95SN-TFTs of identical channel dimensions.

The I_D/W as a function of the channel length is plotted in Fig. 6.6(c). The proposed 95SN-TFTs of 5 μm channel length have exhibited a maximum current density of 6.2 μA/μm. Due to the higher m-SWCNTs the 90SN-TFTs have exhibited a maximum I_D/W of 8.4 μA/μm. The g_m/W of the proposed SN-TFTs of various channel length is shown in Fig. 6.6(d). The proposed 95SN-TFTs have exhibited a maximum g_m/W of 0.7 μS/μm for a channel length of 5 μm and the corresponding value for similar dimension 90SN-TFT is 0.74 μS/μm. The on-current of the device reduces with the increase in the channel length as explained earlier, therefore g_m/W also reduces with increase in the channel length as shown in Fig. 6.6(d). The average carrier mobility of the SN-TFTs as a function of the channel length are plotted in Fig. 6.6(e). The mobility of the device increases with the channel length and 95SN-TFT with channel length of 40 μm has exhibited a maximum carrier mobility of 44.2 cm^2/V·s and 90SN-TFT of similar dimension has a maximum mobility of is 46 cm^2/V·s. The μ exhibited by both types of SN-TFTs having channel length of 40 μm is greater compared to 30 cm^2/V·s exhibited by the device with 95% purity s-SWCNTs and having identical channel length reported in [46].

6.5 High Performance and High On-Current SN-TFT

In this section, the electrical performance of HfO_x based SN-TFT with 95% purity S-SWCNT having a channel length of 5 μm and width of 500 μm is presented. The performance of this high on-current SN-TFT is compared with previously reported high on-current devices. For a fair performance comparison, SN-TFTs exhibiting an on-current larger than 1 mA are considered. The global back gate SN-TFTs reported by H. Ko et al. [47] and C. Wang et al. [46] along with a top gated device demonstrated by M. Engel et al. [49] are considered in Table 6.2. The top gate SN-TFT [49] has exhibited the largest on-off ratio due to two reasons; one is because of the highest (99%) purity

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of s-SWCNTs and another is due to the aligned nature of SWCNTs in the thin-film. The on-off ratio of the device with as-grown SWCNTs [47] is poor because of presence of 33% of m-SWCNTs. This may leads to the possible bridging of the source contact with the drain contact by m-SWCNTs and will result in a greater off-state current. The SN-TFT of this work has exhibited the best on-off ratio among the global gate devices [46, 47]. This improvement in the on-off ratio of the proposed device is achieved by the use of SWCNTs of average length 1 μm compared to 1.7 μm for the other devices [46] and also due to a higher density of SWCNTs. The probability of bridging the source contact with drain contact by the m-SWCNT network will be higher in the case of longer SWCNTs compared to the shorter tubes.

The proposed device is operated at a lower gate voltage compared to the other devices [46, 47] due to the use of high-k gate oxide. The threshold voltage of the proposed device is 3 times lower compared to the SN-TFTs of similar purity s-SWCNTs reported in [46]. This reduction in the threshold voltage can be attributed to use of high-k gate dielectric material. The subthreshold swing of the HfO_X based SN-TFT is at least 2 times steeper compared to other the wafer scale devices [46, 49]. Due to high density SWCNTs, the on-current of the presented device is better compared to other devices except for the SN-TFT reported in [47]. The on-current is at least 2 times higher compared to the devices with same purity s-SWCNTs reported in [46]. The highest on-current of devices reported in [47] is due to the presence of 33% m-SWCNTs in the as-grown SWCNTs as against 5% in the proposed device and could also be due to the aligned nature of the SWCNTs. The I_D/W of the proposed device is 3 times larger compared to the devices with similar dimension and identical purity s-SWCNTs reported in [46].

The high on-current SN-TFT presented has shown a 2 times better value of g_m/W compared to other the device reported in [46]. The carrier mobility of the proposed device is higher compared to devices with identical s-SWCNT purity [46] and also devices having as-grown SWCNTs of random network [47], nevertheless lower compared to aligned version of as-grown SWCNTs [47]. Even though the devices with as-grown SWCNT thin-film [47] have shown a higher on-current, larger current density and higher carrier mobility, they cannot be used for display applications as their off-currents are appreciable, leading to the power consumption even when the devices are switched off. The proposed global back gate SN-TFT based on the thin-film of SWCNTs deposited on the high-k dielectric material, using a simple fabrication methods and affordable purity of SWCNTs have exhibited suf-

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Table 6.2: The performance comparison of high on-current SN-TFTs.

Parameter	[PW]	[47]	[47]	[46]	[49]
Nanotube density (SWCNTs/μm^2)	40-45	NR	NR	21-32	NR
Threshold voltage (V)	-1.5	NR	NR	-4.5	NR
Subthreshold slope(V/decade)	0.6	NR	NR	2	1.2
Maximum on-current (mA)	3.1	6	2	1-2	1
Current density ($\mu A/\mu m$)	6.2	NR	NR	2	NR
On-off current ratio	>320	<3	<3	>15	500
Normalized transconductance ($\mu S/\mu m$)	0.7	0.2	0.02	0.3	NR
Carrier mobility ($cm^2/V \cdot s$)	33.4	60	8	28	NR
s-SWCNT purity (%)	95	67	67	95	99
Gate-dielectric	HfO_X	SiO_2	SiO_2	SiO_2	Al_2O_3
Nanotube orientation	Random	Aligned	Random	Random	Aligned
Gate structure	G	G	G	G	T

PW-Present Work, NR-Not reported, G-Global back gate, T-Top gate

ficient on-current, large current density, adequate on-off current ratio, lower threshold voltage and steeper subthreshold swing, good carrier mobility and these balanced performance matrices make them highly desirable for the display applications.

6.6 Summary

In this chapter, the purity of the s-SWCNT thin-film deposited on different gate oxide surfaces are verified using the Raman spectroscopy data. The electrical performances of global gate SN-TFTs having thin-film of 90% and 95% purity s-SWCNTs are presented. The SWCNT thin-film having different purity s-SWCNTs, deposited on both SiO_2 and HfO_X silanized surface are considered for the analysis. To compare their electrical performance, wafer scale devices of various channel dimension are considered. It is observed that the 95SN-TFTs have shown a higher on-off current ratio compared to the 90SN-TFTs having identical channel dimensions processed under similar process conditions. The 90SN-TFTs have exhibited a higher current density compared to the 95SN-TFTs due to the presence of higher percentage of m-SWCNTs. The proposed high on-current SN-TFT having shorter length SWCNTs deposited on the HfO_X surface has exhibited better on-off current ratio, reduced threshold voltage and steep subthreshold swing and therefore suitable for display application.

TH-1861_07610208

7

Wafer Scale High Performance Local Back Gate SN-TFTs

Contents

7.1 Introduction 102
7.2 Electrical Characterization of Local Back Gate SN-TFTs 103
7.3 Summary 113

TH-1861_07610208

7.1 Introduction

Researchers have developed TFTs for applications such as lightweight flexible displays, smart materials and radio frequency identification tags achieving low cost per unit area, compatibility with large area and non-crystalline substrates [108–110]. TFTs can be made using a wide variety of semiconductor materials such as amorphous silicon, microcrystalline silicon, polysilicon, compound semiconductors, metal oxides and organic materials. Polycrystalline-Si TFT technology requires high process temperatures. Amorphous-Si and organic semiconductor can be processed at lower temperatures, but are limited by poor carrier mobility and are unsuitable for higher speed applications. The SWCNTs have emerged as highly promising channel material for the thin-film transistors due to their excellent electrical and mechanical properties. A SWCNT offers high carrier mobility and current carrying capacity.

The SN-TFTs are classified depending on the gate structure i.e. they have their gate contact either at bottom [42, 46, 47] or at top of the channel [49, 113] and are known as back gate and top gate devices, respectively. Many groups have developed individual SN-TFTs [41–45], but few groups have fabricated SN-TFTs on a wafer scale [46–49]. Wafer scale demonstrations are important as they provide added information about performance variations among the devices across the wafer. Yet another way to group the fabricated devices are based on either a random [46, 47] or an aligned [47–49, 113] network of the SWCNT thin-film. A major roadblock for using aligned SWCNTs is the lack of a growth process to precisely assemble SWCNTs for the device fabrication. Because of the simplicity in the deposition process, a random oriented SWCNT thin-film is preferred over the oriented SWCNT network.

In this chapter, focus is on the performance of local back gate devices and also on wafer-scale processing of SN-TFTs and includes the following essential components. (1) In the reported wafer scale fabricated global back gate SN-TFTs, the individual transistors cannot be switched independently and this limits the integration of devices to form a circuit. A local back gate device on an individual SWCNT has been demonstrated [111]. However in this work, a local back gate structure is employed at the wafer scale and therefore the individual transistors could be independently controlled. (2) Typical threshold voltage values reported for wafer scale back gate devices are in the range of -2.5 V to - 5 V. The device on-off currents are typically reported for gate voltage swings ranging from -10 V to 10 V. In order to realize low-voltage operations, We have employed a high-k dielectric material for

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the gate oxide and this also helped to achieve much steeper subthreshold voltage swings and higher transconductance values. Another advantage of high-k dielectric is that the physical thickness of the insulator film can be increased, which could prevent tunneling of the electrons through the gate insulator layer [123–126], thus reducing the leakage power and maintaining a high value capacitance. This chapter reports for the first time, the wafer scale fabrication of local back gate SN-TFTs using HfO_x as the gate dielectric material and the SWCNT thin-film is deposited over HfO_x surface. (3) It is important to consider the deposition of CNTs over the HfO_x surface, for achieving good density of SWCNTs because the current carrying capability depends mainly on the density of SWCNTs. In addition, the device on-off current ratio and mobility parameters should not be degraded. (4) Most of the s-SWCNTs were deposited using a sophisticated evaporation self-assembly method. Like other researchers [46–48] an uniform and high density random oriented SWCNT thin-film is deposited onto a 2 inch wafer using a simple solution-based assembly method and demonstrate that good TFT performance can be achieved with separated SWCNTs of less demanding purities and illustrated the same using 95%.

The sections of the chapter are arranged as follows. The section 7.2 presents the analysis of electrical characterization results of the wafer scale local gate SN-TFTs. Section 7.3 summarizes the chapter.

7.2 Electrical Characterization of Local Back Gate SN-TFTs

In this section, the electrical characteristics of local back gate SN-TFTs are presented. The current-voltage and capacitance-voltage characteristics of the local back gate SN-TFTs of various dimensions are presented separately. The output and transfer characteristics of local gate SN-TFTs are presented. The performances parameters such as on-off ratio, current density, transconductance, mobility of SN-TFTs having various channel dimensions are discussed. The C-V characteristics of SN-TFTs having different dimensions is also presented.

7.2.1 Results of *I-V* Characterization

Electrical performances of proposed the local back gate SN-TFTs are studied using a Keithley Polaris system probe-station. The *I-V* characteristics of the wafer scale devices fabricated on the 2 inch Si wafer are carried out using the experimental setup shown in Fig. 7.1. The wafer is placed on the chuck of the probe-station and three contact probes are carefully placed over the source, drain,

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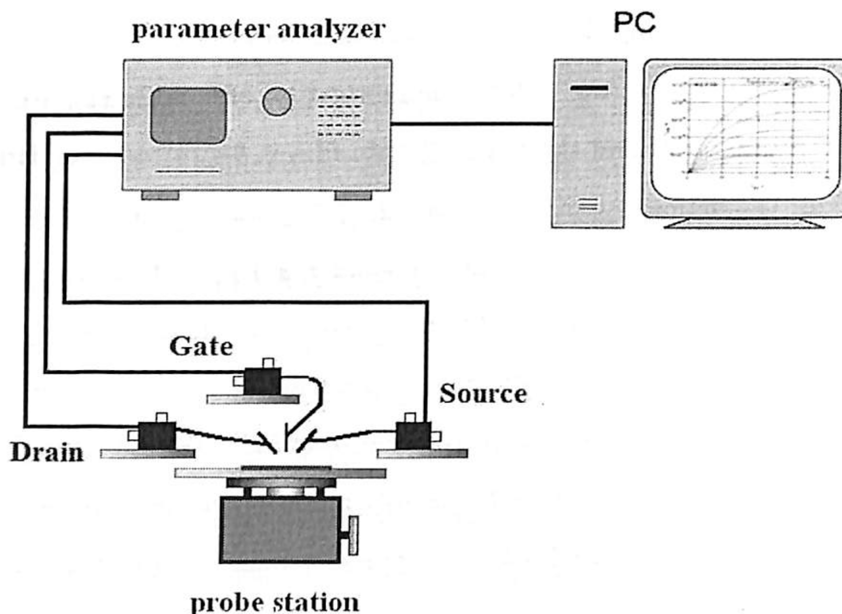

Figure 7.1: Experimental setup to characterize local gate SN-TFTs.

gate contacts without damaging the pads. Depending on the required characteristics, the voltage of the corresponding terminal is varied as per the required resolution.

The current-voltage characteristic of a typical SN-TFT device having channel dimensions of length 20 μm and width 15 μm is shown in Fig. 7.2. The output characteristic of the device shown in Fig. 7.2(a) is obtained for various local back gate voltage (V_{GS}) ranging from -1 V to -5 V in steps of -1 V. The device has exhibited a p-type transistor behavior with distinct triode and saturation regions. It may be observed from the output characteristics that for lower V_{GS} values of the device, the drain current (I_D) is saturated between -1 V and -2 V of the drain voltage (V_{DS}). However, for larger V_{GS} values of the device requires more V_{DS} for I_D to reach the saturation level. The peak on-current of this SN-TFT is 93.16 μA at a V_{DS} of -8 V for a V_{GS} of -5 V and it corresponds to a I_D/W of 6.21 μA/μm. The current density achieved in the proposed local back gate SN-TFT is about 30 times greater than identical channel length global back gate device reported in [46]. The local gate SN-TFT has exhibits an output conductance g_{ds} of 0.402 μS when operated at a V_{GS} of -3 V. Fig. 7.2(b) shows the linear region of the output characteristic of the device obtained by varying the V_{DS} value from -1 V to 1 V . The I_D-V_{DS} curves obtained are linear, indicating an ohmic contact between SWCNTs and source/drain electrodes.

The transfer characteristics of the device measured at a constant V_{DS} of -1 V are shown in Fig.

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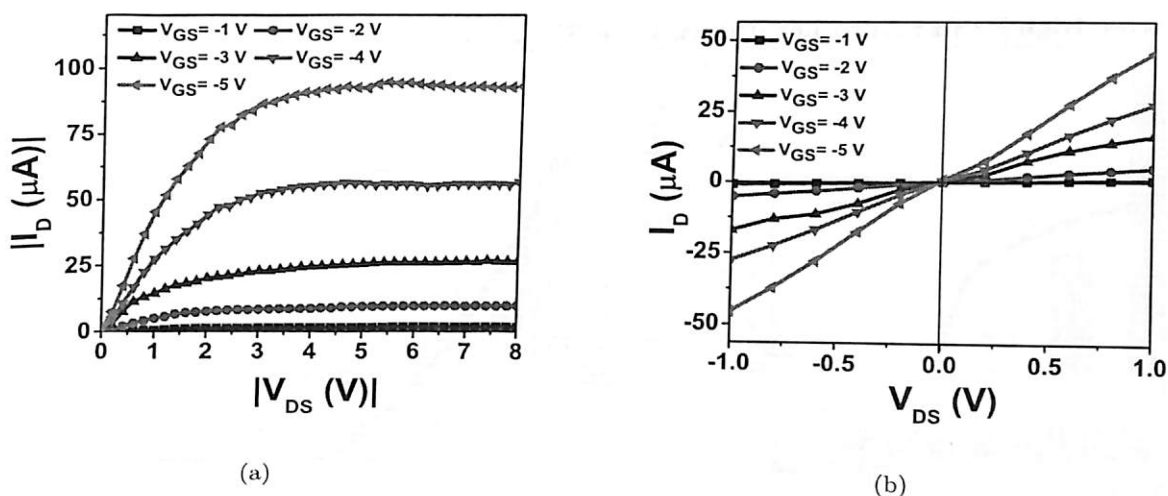

Figure 7.2: Electrical characterization of local gate SN-TFT having the channel length 20 μm and width 15 μm. (a) Output characteristics of the device for local gate voltages ranging from -1 V to -5 V in steps of -1 V. (b) Linear region of the output characteristics

7.3. The drain current and gate leakage current (I_G) of the typical SN-TFT for a V_{GS} sweep from -5 V to 3 V are shown in Fig. 7.3(a). The on-current of the local back gate SN-TFT at V_{GS} of -5 V is 43.4 μA and the off-current at V_{GS} of 3 V is 3.49 nA measured at a constant V_{DS} of -1 V. Therefore, the on-off current ratio exhibited by this local back gate SN-TFT is found to be 1.24×10^4 which is two orders of magnitude higher compared to earlier demonstrated global back gate SN-TFTs [46] for the same range of V_{GS} values. The average gate leakage current is found to be 1 pA over a wide range of gate voltages and is comparable to the reported gate leakage current values in the literature [42, 48]. The threshold voltage, an important parameter of the proposed SN-TFT device is -0.5 V; this value is very less compared to -5 V reported for global back gate device with similar purity s-SWCNTs [46]. The reduction of the threshold voltage of the proposed device is attributed to the use of high-k gate dielectric and local back gate structure.

The fabricated SN-TFTs exhibited an excellent subthreshold slope of 400 mV/decade, which is steeper compared to the previously reported values [46, 48, 122]. This improvement in subthreshold slope of the SN-TFTs of the present work may be attributed to the use of HfO_X as the gate dielectric material. The drain current in linear scale and the corresponding transconductance variations of the device at a V_{DS} of -1 V are shown in Fig. 7.3(b). The peak transconductance of the device is 21 μS at a V_{GS} of -4.75 V.

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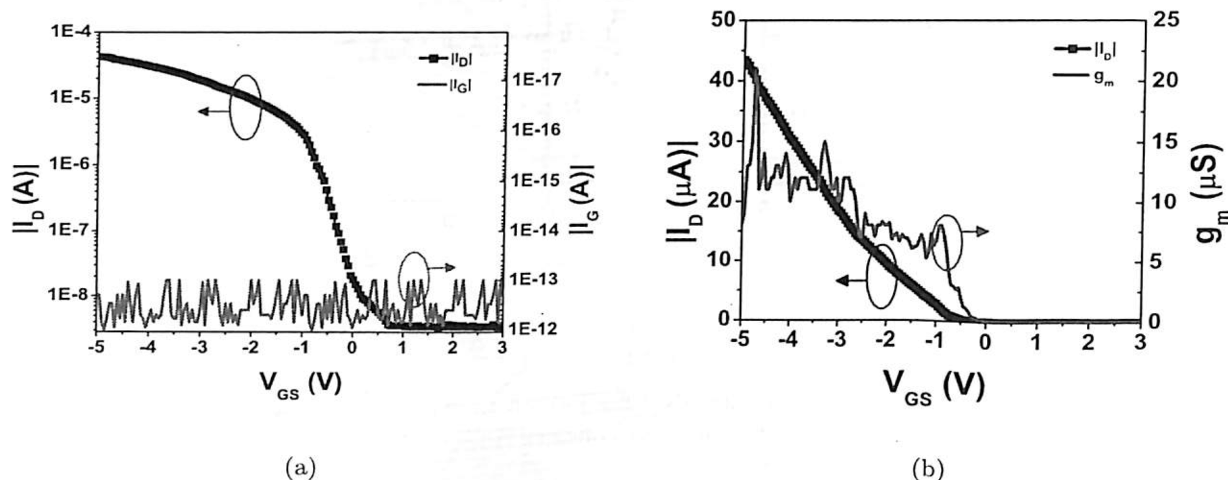

(a) (b)

Figure 7.3: Transfer characteristics of local back gate SN-TFT. (a) Drain current variations (logarithmic scale) for different V_{GS} at constant V_{DS} of -1 V and the corresponding gate leakage current. (b) Drain current variations (linear scale) and transconductance variation for various V_{GS} values.

Electrical characteristics of local back gate SN-TFTs having different channel dimensions are studied to compare their performances. Fig. 7.4 shows the performances of wafer scale local back gate SN-TFTs in terms of the on-off current ratio. It is noticeable in Fig. 7.4(a) that, for SN-TFTs with channel length less than 10 μm the current ratio is less than 1000, due to the possible bridging of source and drain contacts by m-SWCNTs in the short channel length. However, as the channel length of the device exceeds 20 μm, the drain current on-off ratio is more than 10^4. The on-off current measurements of all SN-TFTs are carried out by varying the V_{GS} from -5 V to 3 V and the V_{DS} is maintained at -1 V.

The statistical distribution of on-off ratio for the wafer scale fabricated SN-TFTs is shown in Fig. 7.4(b). In this fabrication process, device yield on the wafer is 90%. Few devices are not working due to the peel-off of the metal contacts during the process. About 94% of the working SN-TFTs have exhibited the on-off ratio more than 10^3 and about 64% of them have shown a current ratio of greater than 10^4.

The average drain current of SN-TFTs for different channel dimensions at a constant V_{DS} of -1 V and a V_{GS} of -5 V are plotted in the Fig. 7.5(a). The maximum on-current measured is 230 μA for a SN-TFT with channel length of 2 μm and width of 20 μm. The length of the deposited nanotubes ranges from 100 nm to 4 μm with a mean value of 1 μm. In case of longer channel devices, many individual nanotubes are involved in the channel formation and number of tube to

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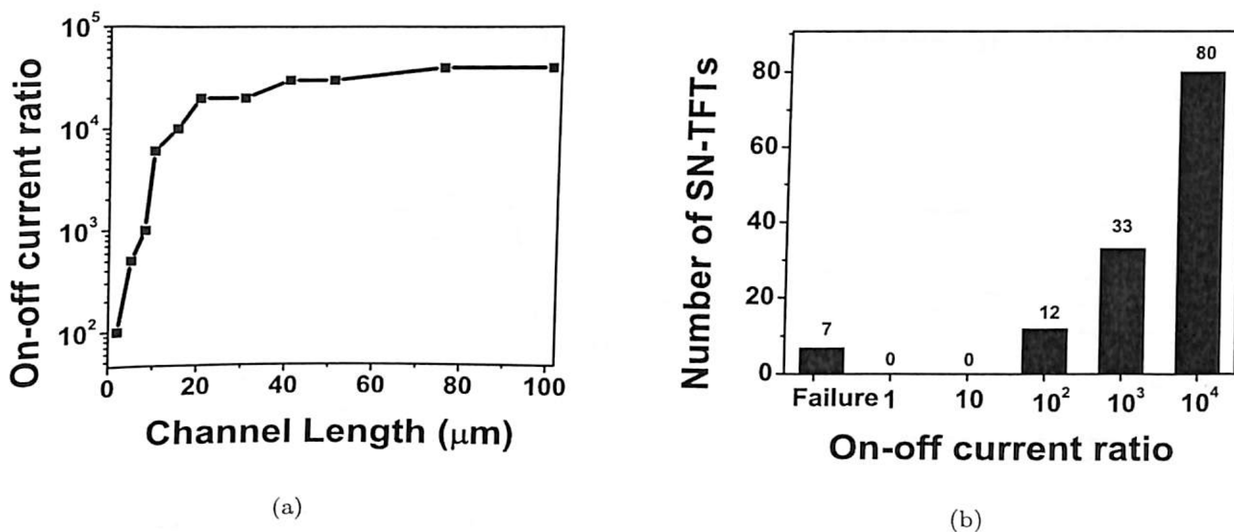

Figure 7.4: Performance of wafer scale fabricated local back gate SN-TFTs. (a) Variation of drain current on-off ratio as a function of channel length. (b) Current on-off ratio distribution of fabricated SN-TFT devices.

tube contacts will be increased and this leads to lower on-currents as shown in Fig. 7.5(a). However, I_D is proportional to device channel width because more number of SWCNTs takes part in the current conduction activity as width increases. The liner variation of the drain current versus the channel width of various channel length devices is shown in the Fig. 7.5(b). It may be noted that, as the channel width reduces the on-current of the SN-TFT also reduces. Due to very small dimensions of the SWCNT which is nm, there is a possibility of current flowing through the devices even as the channel width approaches 0 (few nm) width. The maximum value of I_D/W is 13.03 μA/μm for a SN-TFT of channel length 2 μm. This high value of I_D/W is attributed to the high density of SWCNTs on the amino-silane modified HfO_X surface. The average on-current density of SN-TFTs for different channel lengths is plotted in Fig. 7.5(c). The on-current density decreases as the channel length increases.

Two important parameters of the device, transconductance and carrier mobility values of the devices, are also determined. The slope of SN-TFTs transfer characteristics at a V_{DS} of -1 V is considered for the calculation of transconductance. The variations of average transconductance normalized to the channel width and average carrier mobility of the proposed SN-TFTs as a function of channel length are shown in Fig. 7.5(d). Due to better control of the transistor channel, proposed local gate SN-TFTs of channel length 2 μm have exhibited maximum normalized transconductance

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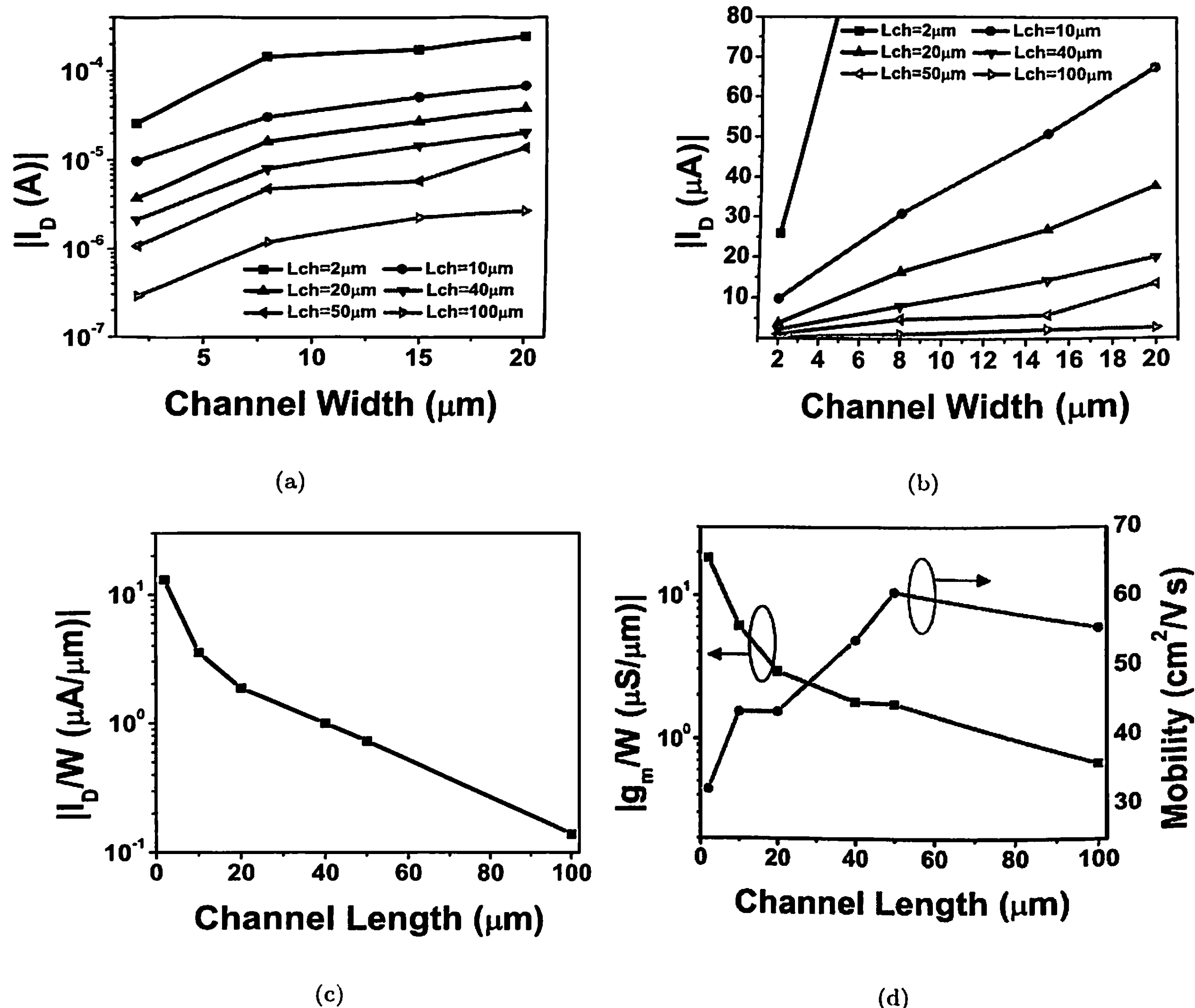

Figure 7.5: Electronic properties of local back gate SN-TFTs. (a) Average on-current of SN-TFTs for various channel dimensions. (b) Average on-current of SN-TFTs for various channel dimensions in linear scale. (c) I_D / W variation as a function of channel length. (d) Average transconductance per unit channel width and average mobility of the SN-TFT as a function of channel length.

of 18.5 $\mu S/\mu m$. The high value of normalized transconductance exhibited by proposed SN-TFTs can be attributed to the use of local gate structure, high density SWCNT thin-film and high-k gate dielectric. The on-current of the device reduces with the increase in the channel length as explained earlier; therefore, transconductance reduces with the increase in the channel length. The plot in Fig. 7.5(d) shows that normalized transconductance reduces as the channel length of the SN-TFTs increases.

The charge carrier mobility of the SN-TFT is calculated using the equation (5.2) [49]. To account

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for the inhomogeneous dielectric environment, the $\varepsilon_{eff} = (\varepsilon_{SiO_2} + \varepsilon_{HfO_X})/2$ is considered [49]. The dielectric constant of HfO_X is found to be 12, by a separate capacitance measurement and a value of 3.9 is used for the SiO_2 finally gives $\varepsilon_{eff} = 7.95\ \varepsilon_o$. The mobility of local back gate SN-TFTs for various channel length are plotted in Fig. 7.5(d). The μ of the device the increase with the channel length up to 50 μm and then decreases. The maximum carrier mobility of 60.6 $cm^2/V{\cdot}s$ is obtained for a SN-TFT having the channel length 50 μm. The carrier mobility of the local back gate devices are more compared to the similar type of wafer scale SN-TFTs reported in [46, 48, 49]. However, the mobility of SN-TFT is less compared to single CNT-FETs because of high coupling resistance between SWCNTs in the thin-film. A coupling resistance between the SWCNTs is reported [38] to be as high as 100 MΩ and it dominates the SWCNT resistance.

To explore the advantages of the proposed local back gate SN-TFTs, their performances are compared with other global back gate [46–48] and top gate [49, 113] SN-TFTs reported in the literature. Only the wafer scale fabricated SN-TFTs are considered for a fair comparison. SN-TFTs having random/aligned SWCNT thin-film and SWCNTs of various semiconducting purity are chosen to examine the effect of SWCNT orientation and semiconducting purity of the SWCNTs on the device performance. Table 7.1 lists various physical and performance parameters of different SN-TFTs. A random network of SWCNTs deposited on the silanized HfO_X layer in this work is found to be having the highest SWCNT density compared to other reported values. Due to higher SWCNT density, the proposed devices have exhibited a greater I_D/W compared to the device with similar purity s-SWCNTs reported in [46]. Local back gate devices of the present work with HfO_X as the gate oxide have exhibited a low threshold voltage, which is ten times less compared to the value reported for global back gate SN-TFTs with similar s-SWCNT purity [46]. The proposed local back gate SN-TFTs have exhibited a subthreshold swing which is fivefold steeper compared to global gate devices with random network SWCNTs [46] and it is comparable to the top gate devices with 99% s-SWCNT purity [49] and global back gate devices having the aligned SWCNT network [48].

Table 7.1 shows that the local gate SN-TFTs of this work have exhibited the maximum on-off current ratio of 5×10^4 which is about two times greater compared to similar type of devices with global back gate structure [46]. It should be noted that to achieve the on-off currents gate voltage swing for the the proposed device ranges from -5 V to 3 V compared to -10 V to 10 V for the global back gate devices [46]. However, the on-off current ratio of the proposed devices is lower

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Table 7.1: Performance comparison of various wafer scale fabricated SN-TFTs.

Parameter	[PW]	[46]	[47]	[48]	[49]	[113]
Nanotube density (SWCNTs/μm^2)	40-45	21-32	3	18	NR	25
Current density (μA/μm)	13.03	10	NR	NR	NR	NR
Threshold voltage (V)	-0.5	-5	NR	NR	NR	-2.5
Subthreshold slope (V/decade)	0.4	2	NR	1	0.5	5
On-off current ratio	5×10^4	2×10^4	3	10^5	10^5	10^5
Normalized transconductance (μS/μm)	18.5	0.6	0.02-0.2	NR	NR	NR
Carrier mobility (cm^2/V·s)	60.6	52	125	2	5-20	8
Gate-dielectric	HfO_X	SiO_2	SiO_2	SiO_2	Al_2O_3	Al_2O_3
Gate-oxide thickness (nm)	10	50	200	300	15	50
s-SWCNT purity (%)	95	95	67	NR	99	NR
Nanotube orientation	Random	Random	Aligned	Aligned	Aligned	Aligned
Gate structure	L	G	G	G	T	T

PW- Present work, NR-Not reported, L-Local back, G-Global back, T-Top

when compared to devices reported in [49] and [48]. The main reasons for a higher on-off ratio of the devices [48, 49] are use of higher purity s-SWCNTs (99%) and an aligned network of SWCNTs. Even though, the gate voltage can modulate the current through a s-SWCNT, it will not change the current in a m-SWCNT. In case of lower purity s-SWCNTs (95%), more m-SWCNTs are present compared to 99% purity film. In 95% purity case more m-SWCNTs will be involved in the channel formation between source and drain and this will lead to a reduced on-off current ratio.

Normalized transconductance of the proposed device is 30 times greater compared to the SN-TFTs with similar purity s-SWCNTs [46] and this can be attributed to the high density of SWCNTs, local back gate control and the use of a high-k gate dielectric material. Important performance parameter of SN-TFT, the charge carrier mobility of various types of devices is also discussed. The proposed local back gate SN-TFT with a random network of SWCNTs has exhibited the highest average carrier mobility compared to other SN-TFTs, except for the devices reported in [47]. The reason for greater mobility for devices reported in [47] is the use of as-grown SWCNTs, which contains 33% m-SWCNTs as compared to 5% of the proposed device. The improved carrier mobility of the proposed device compared to other devices is due to high density SWCNTs, high-k gate dielectric and local gate structure. In summary, proposed local back gate SN-TFTs with a random network of

TH-1861_07610208

SWCNTs deposited over the amino-silane treated HfO_X surface have exhibited an excellent on-off ratio, threshold voltage, subthreshold swing, normalized transconductance and carrier mobility when compared to global back/top gate devices having a random/aligned network of SWCNTs having the same/greater semiconducting purity.

7.2.2 Results of *C-V* Characterization

The gate to source capacitance (C_{GS}) versus V_{GS} of the local gate SN-TFT is measured using Agilent B1500A Semiconductor Device Analyzer. The experimental setup used for *C-V* characterization is shown in Fig. 7.6. The *C-V* curves of the local gate SN-TFTs are obtained by sweeping V_{GS} from -5 V to +5 V in steps of 50 mV dc voltage superimposed with a sinusoidal ac signal of amplitude 25 mV and frequency ranging from 100 KHz to 1 MHz. Fig. 7.7 shows the *C-V* curves obtained for devices having various channel dimensions. Even though there is no bulk region present in this case, the *C-V* curves obtained are similar to a MOS capacitor. For large negative gate voltages, there is accumulation of holes near the SWCNT - dielectric interface and the capacitance obtained are maximum. For positive gate voltages, the holes are depleted from the thin-film and finally reaches a maximum depletion width and therefore the corresponding capacitance saturates to a minimum value. The C_{GS} plots for various dimension local gate SN-TFTs at 100 kHz are shown in the Fig. 7.7(a). As the device channel area increases, the capacitance values also increases. The experimentally obtained maximum capacitance value (C_{MAX}) is closely matched within 3% compared to the calculated gate capacitance using the formula $C_{MAX} = \varepsilon_{OX}\ L_{ch}\ W / T_{ox}$, where ε_{OX} is a dielectric constant of the gate oxide, L_{ch} is the channel length, W is the channel width and T_{ox} is the thickness of gate oxide.

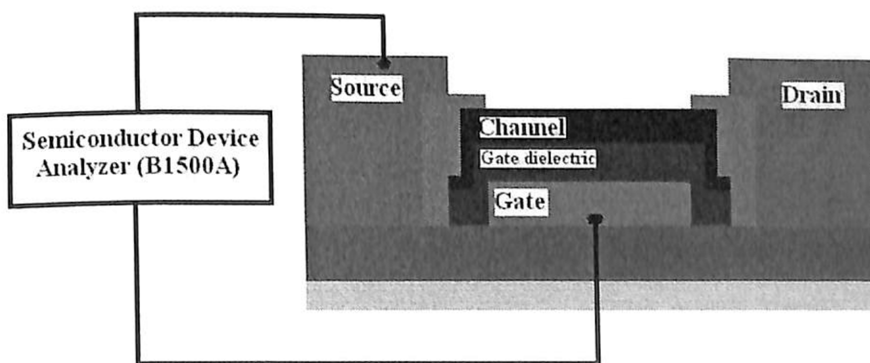

Figure 7.6: Experimental setup for *C-V* measurement.

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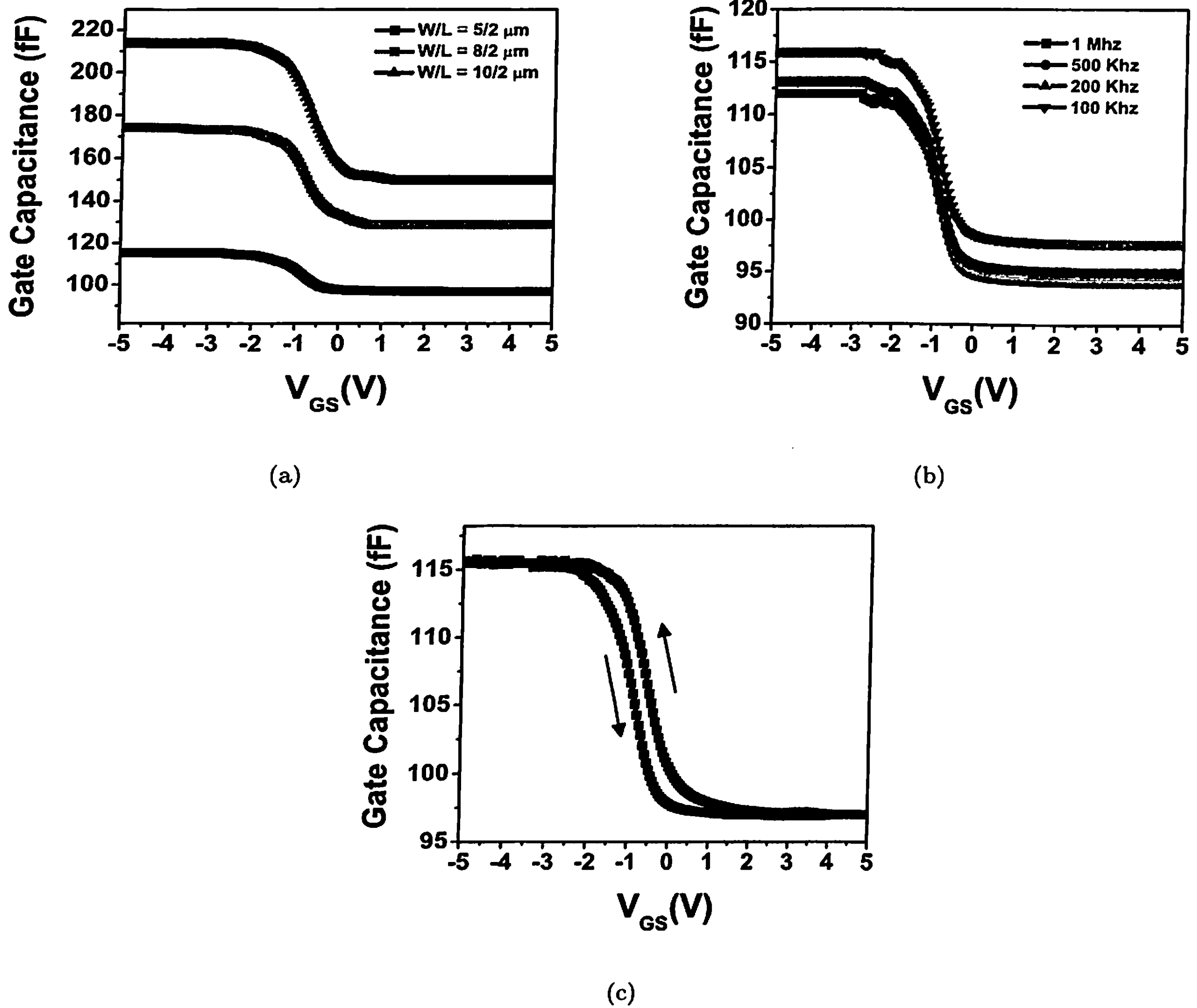

Figure 7.7: Capacitance measurements of local back gate SN-TFTs. (a) *C-V* curves of the devices having different channel dimensions. (b) *C-V* measurements of a SN-TFT using different frequency ac signal. (c) *C-V* curve obtained by double sweep of the gate voltage.

In order to study the effect of trapped interface charges, ac signals of different frequencies are used to obtain the *C-V* curves shown in Fig. 7.7(b). The capacitance values increased rapidly at lower frequencies, which is probably due to the faster response of the trapped charges in the interface regions. When the device was operated at higher frequencies, the charges present at lower frequencies were localized and did not response to voltages at 1 MHz. Almost similar frequency dispersion has occurred at higher values of negative as well as positive gate biases which probably indicates that the charges are trapped at SWCNT-dielectric as well as SWCNT-source metal contact interfaces, respectively.

Fig. 7.7(c) shows the *C-V* curves obtained at 100 kHz for a device of channel length 2 μm and width 5 μm obtained by double sweeping of the gate voltages from -5 V to +5 V followed by +5 V to -5 V. The *C-V* curve showed a counterclockwise hysteresis with flat-band voltage shifted towards positive direction by 400 mV which probably suggests that the trapped holes in the SWCNT-dielectric interface during the positive direction sweep is not fully de-trapped during the negative direction sweep. These trapped charges will also affect the carrier mobility of the device. To the best of our knowledge, this is the first *C-V* characteristics reported for a SWCNT thin-film and an exact mechanism of frequency dispersion and hysteresis is yet to be understood clearly.

7.3 Summary

In this chapter, electrical characterization of the high performance wafer scale HfO_x based local back gate SN-TFTs having high density of SWCNTs with various channel dimensions are discussed. The advantages of the local back gate structure, high density of SWCNTs and high-k gate dielectric are evident from the performance of the proposed local back gate devices. The proposed SN-TFTs have exhibited an excellent performance in terms of on-off ratio, current density, threshold voltage, subthreshold swing, transconductance and carrier mobility as compared to the other reported wafer scale SN-TFTs in the literature as well as other types of SN-TFTs presented in the previous chapters. As the devices can be switched individually, the circuit realization is possible by using n-type SN-TFTs. The *C-V* characteristics of local gate SN-TFTs are also discussed. In the next chapter, the advantages of dual gate SN-TFTs over the single gate SN-TFTs are examined by studying the electrical performances of identical channel dimension devices. The performance of local and global gated wafer SN-TFTs of identical dimension and processed under same process conditions are presented.

TH-1861_07610208

TH-1861_07610208

8

SN-TFT Channel Control Using Various Gate Structures

Contents

8.1 Introduction 116

8.2 Electrical Characterization Results of Top, Bottom and Dual Gate SN-TFTs 117

8.3 Performance Comparison of Wafer Scale Global and Local back gate SN-TFTs 121

8.4 Summary 124

TH-1861_07610208

8.1 Introduction

The conventional TFTs based on the organic material [108–110] and the amorphous silicon exhibit a poor carrier mobility and require a higher processing temperature. To overcome these drawbacks, SWCNTs have emerged as highly promising channel material for TFTs due to their excellent electrical and mechanical properties. So far most of the SN-TFTs reported in the literature have only one gate contact either at bottom [37, 38, 46] or at top [49, 113] of the channel. In case of back gate SN-TFTs with substrate as the gate contact [37, 38, 42, 44, 46–48], switching of individual transistor is not possible. Even though the devices are controlled individually in the top gate SN-TFTs [49, 113], these single gate devices suffer from a poor subthreshold slope and a high threshold voltage because of the limited control over the transistor channel. In this chapter, a dual gate SN-TFT having planar gate structures at top and bottom of the SWCNT thin-film channel to mitigate performance limitations of single gate devices are presented. In this work, to improve the electrical performance of SN-TFTs, the RF sputtered high-k HfO_x is used as the back gate dielectric material. To explore the advantages of the dual gate structure over the single gate, SN-TFTs having dual, back and top gate structures with similar channel dimensions are fabricated. The dual gate SN-TFT is expected to exhibit better performance compared to the single gate devices.

A number of researchers have demonstrated wafer scale fabrication of global gate SN-TFTs, but to realize integrated circuits using SN-TFTs, it is important not only to fabricate many SN-TFTs on the same wafer but also necessary to control individual transistors. A global back gate is known to lower device speed and to produce unwanted hysteresis in the gate response [75, 127]. Therefore, the local gate control is introduced and several types of locally-gated SN-TFTs have been fabricated and studied [49, 111, 113]. They can be classified as top and bottom gate SN-TFTs, depending on the position of the gate. A top gate is known to exert pressure on the underlying SWCNTs and may change its electric transport property [35, 128]. A bottom gate structure is a viable option for an effective local gating, however it requires additional fabrication steps compared to top gate SN-TFTs and also the gate electrode should be fabricated before the SWCNT deposition. The local back gate device having individual SWCNT has been demonstrated [111]. However in this work, the local back-gate structure is employed at the wafer scale and therefore each of the individual transistors could be independently controlled. In order to understand the transistor channel control by the gate structure, the wafer scale SN-TFTs having local and global gate of identical channel dimensions are

TH-1861_07610208

presented.

The sections of the chapter are arranged as follows. Section 8.2 presents the analysis of electrical performance of three SN-TFTs of identical channel dimension having top, bottom and dual gate structure. Section 8.3 presents the analysis of electrical characterization results of wafer scale SN-TFTs with local and global gate structures. Finally the chapter is summarized in section 8.4.

8.2 Electrical Characterization Results of Top, Bottom and Dual Gate SN-TFTs

In this section, the electrical performances of top, bottom and dual gate HfO_x based SN-TFTs are presented. These SN-TFTs have thin-film of 95% s-SWCNTs deposited on the silanized HfO_x using the immersion technique. The Electrical performances of these SN-TFTs are studied using a Keithley Polaris system having an experimental setup shown in Fig. 7.1. In order to make a fair comparison of different gate structured SN-TFTs, the devices fabricated with identical dimension are considered for the analysis.

The output characteristics of three SN-TFTs with different gate structures are shown in Fig. 8.1. The dual gate SN-TFT exhibits a p-type behavior for various V_{GS} ranging from -0.4 V to -2 V as shown in Fig. 8.1(a). The device has exhibited a maximum I_D of 9.51 μA for a V_{GS} of -2.0 V and has g_{ds} of 0.052 μS at a V_{GS} of -0.8 V. The back and top gate SN-TFTs have also exhibited p-type output characteristics for various V_{GS} from -1 V to -5 V as shown in Fig. 8.1(b) and 8.1(c), respectively. The back and top gate SN-TFTs have exhibited a maximum on-current of 4.5 μA and 2.47 μA, respectively for a V_{GS} of -5 V and the output conductance of the back gate device is 0.061 μS and for the top gate SN-TFT it is 0.112 μS both calculated at a V_{GS} of -2 V. The study of output characteristics of three SN-TFTs shows that due to better control of the transistor channel, the dual gate SN-TFT has exhibited higher on-current at a lower V_{GS} and has the least output conductance compared to the other two single gate SN-TFTs.

The transfer characteristics of three SN-TFTs are obtained by varying the V_{GS} at a constant V_{DS} of -2 V and the corresponding g_m of the devices are shown in Fig. 8.2. The transfer characteristics of the dual gate SN-TFT plotted in Fig. 8.2(a) is obtained by varying V_{GS} from -2 V to 2 V at a constant V_{DS} of -2 V, shows the steepest subthreshold slope of 280 mV/decade. To the best our knowledge this is the lowest value reported for the SN-TFTs. The dual gate SN-TFT has exhibited an on-off current ratio greater than 10^3. The transfer characteristics of the back and top gate SN-TFTs

TH-1861_07610208

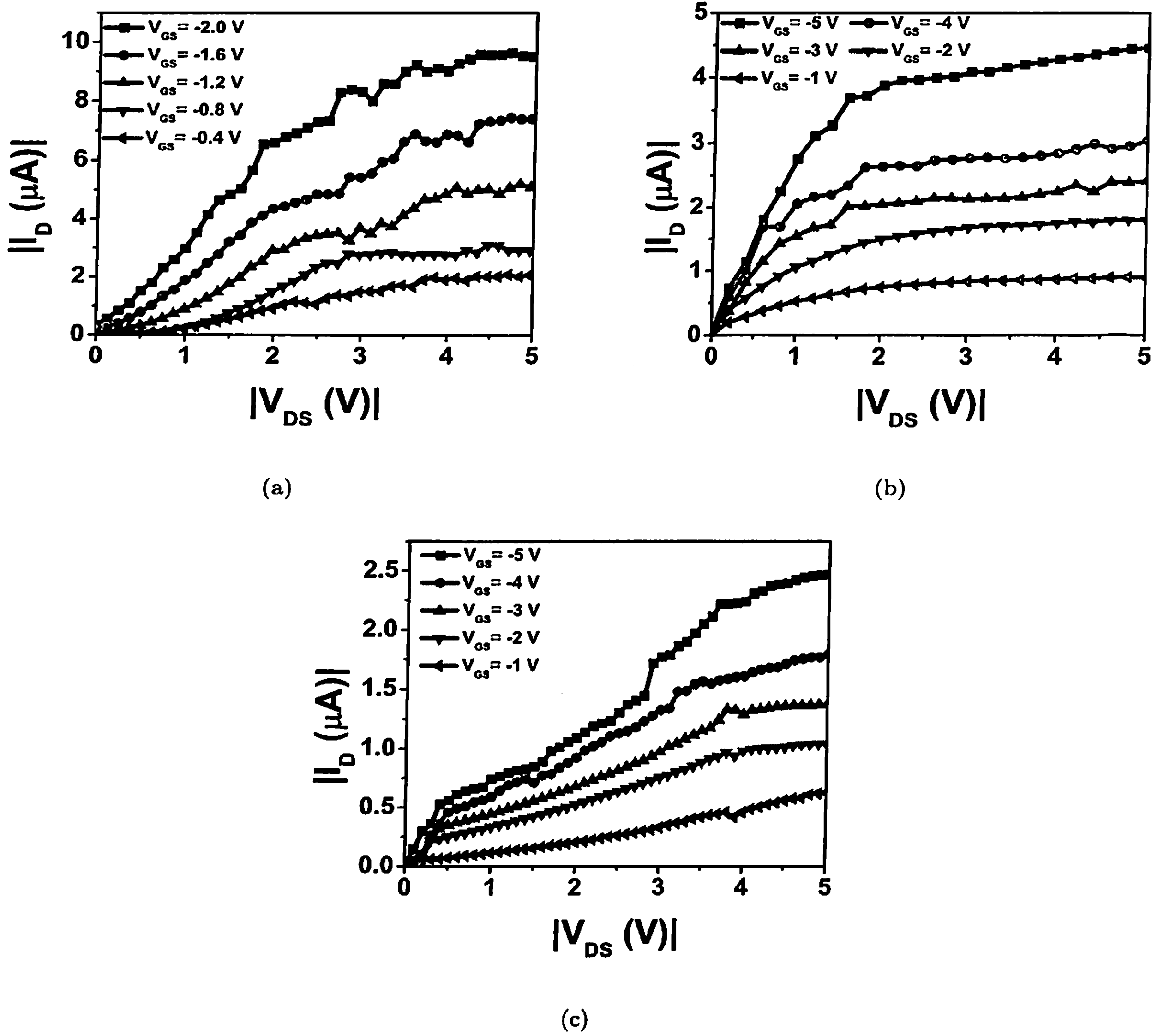

Figure 8.1: The output characteristics of the SN-TFTs having different types gate structure. (a) *I*-*V* plots of dual gate SN-TFT for V_{GS} ranging from -0.4 V to -2 V. (b) p-type behavior of back gate SN-TFT. (c) I_D- V_{DS} plot of the top gate SN-TFT for V_{GS} ranging from -1 V to -5 V.

are obtained by varying V_{GS} from -5 V to 3 V at a constant V_{DS} of -2 V are shown in Fig. 8.2(b) and 8.2(c), respectively along with the corresponding g_m value. The dual, back and top gate SN-TFTs fabricated under same process conditions, have exhibited a maximum g_m of 5.89 μS, 1.36 μS and 0.48 μS at V_{GS} of -1.44 V, -3.6 V and -4.2 V, respectively. The carrier mobility of three SN-TFTs are calculated using the equation (5.2). To account for the inhomogeneous dielectric environment, the ε_{eff} of 7.95 ε_o is considered. The dual gate device has the highest μ of 2.26 cm^2/V·s compared

TH-1861_07610208

to 0.54 $cm^2/V \cdot s$ and 0.1 $cm^2/V \cdot s$ for back and top gate devices, respectively. It is clearly observed from Fig. 8.2(d), which shows the transfer characteristics of all three devices that the dual gate device has the lowest threshold voltage of -0.65 V compared to -1 V and -1.2 V for top and back gate SN-TFTs respectively, achieving at the least 350 mV reduction compared to single gate devices. Since only one gate controls the conduction of the transistor channel, both single gate SN-TFTs exhibited poor subthreshold slope, higher threshold voltage and lower on-off current ratio compared to dual gate SN-TFT as shown in Table 8.1. The top gate SN-TFT has exhibited lowest gate control over the channel compared to other two devices due to the presence of spacers in the channel region. In summary, the comparison of three SN-TFTs with different gate structure fabricated under similar process conditions in this work shows that the dual gate SN-TFT has the best control over the transistor channel compared to other single gate devices.

In order to validate the present work, the performance of three SN-TFTs are compared with previously reported similar type of devices. Table 8.1 lists the subthreshold slope, on-off current ratio and threshold voltage of dual, back and top gate SN-TFTs. The double gate SN-TFT reported by Bae-Horng Chen et al. [129] using plasma enhanced oxide (PE-oxide) as the gate dielectric material, has exhibited a poor subthreshold slope and a comparable on-off current ratio when compared to the proposed dual gate SN-TFT. The V_{GS} swing for on-off current for the SN-TFT of the present work is ranging from -2 V to 2 V, where as for the reported device [129] it is from -10 V to 10 V. This lower gate voltage swing of the proposed dual gate SN-TFT is due to the use of high-k HfO_x gate oxide.

The back gate SN-TFT of the present work is compared with a device having identical channel dimension and fabricated with same purity SWCNT reported by Chuan Wang et al. [46]. Table 8.1 shows that the back gate SN-TFT with HfO_x gate oxide has exhibited steep subthreshold slope, high on-off current ratio and low threshold voltage compared to corresponding values reported for device having SiO_2 as the gate oxide [46]. The other back gate devices reported by A. Schindler et al. [130] and M.E. Roberts et al. [44] exhibited a much better on-off current ratio compared to proposed device. The information on semiconducting purity of SWCNTs for devices in [130] and [44] is not reported and moreover these devices have longer channel length which further increases the on-off current ratio.

The performance of the top gate SN-TFT with SiO_2 gate oxide deposited by the GIS technique

TH-1861_07610208

(a)

(b)

(c)

(d)

Figure 8.2: Transfer characteristics and transconductance of SN-TFTs for different V_{GS} and at a constant V_{DS} of -2 V. (a) for the dual gate SN-TFT. (b) for the back gate SN-TFT. (c) for the top gate SN-TFT. (d) Transfer characteristics of all 3 types of devices.

is compared with the devices of identical channel length having Al_2O_3 as the gate oxide deposited by the ALD process [49, 113]. The subthreshold slope exhibited by the top gate SN-TFT of this work is better compared to the device reported in [113], but the on-off ratio is inferior, nevertheless the corresponding gate voltage swing is from -5 V to 3 V as against -40 V to 40 V [113] and purity of s-SWCNTs for the devices in [113] is not reported. The other top gate device [49] has 99% enriched s-SWCNTs and therefore has a higher on-off ratio compared to present work SN-TFT having 95% purity s-SWCNTs. From above discussions, it may be concluded that the dual gate SN-TFT of this work has better electrical performances in terms of subthreshold slope and threshold voltage, compared to the previously reported double gate SN-TFT [129] and other single gate devices.

TH-1861_07610208

Indian Institute of Technology Guwahati

Table 8.1: The performance comparison of SN-TFTs having three different gate structures

Parameter	Dual gate		Back gate				Top gate		
	[PW]	[129]†	[PW]	[46]	[130]†	[44]†	[PW]	[113]	[49]*
Subthreshold slope (V/decade)	0.28	1.2	1	2	1.1	0.5	1.3	5	0.5
On-off current ratio	1.2×10^3	2×10^3	3×10^2	20	10^4	10^3	2×10^2	10^5	10^5
Threshold voltage (V)	-0.65	NR	-1.2	-5	-4.7	0.24	-1.0	-2	NR

PW Present Work, † Longer channel lengths, * Device with 99% purity s-SWCNTs, NR Not reported

8.3 Performance Comparison of Wafer Scale Global and Local back gate SN-TFTs

The electrical performance of the wafer scale SN-TFTs having local and global back gate structures are presented. The HfO_X based SN-TFTs having thin-film of 95% purity s-SWCNTs deposited using the immersion technique having identical channel dimensions and processed under similar conditions are considered for the analysis. The electrical performances of these SN-TFTs are studied using a Keithley Polaris system. The Experimental setup shown in Fig. 5.3 and 7.1 are used for characterizing global and local back gate SN-TFTs, respectively. Both global and local back gate SN-TFTs have exhibited p-type output characteristics. The advantage of local back gate SN-TFTs is that the devices can be controlled individually and therefore the performance of the devices is expected to be better compared to the globally controlled devices. Fig. 8.3 shows the electrical parameters such as on-off current ratio, current density, transconductance and mobility of both global and local gate SN-TFTs. Fig. 8.3(a) shows the ratio of on- and off-currents measured at V_{GS} of -5 V and 3 V, respectively at a constant V_{DS} of -2 V. Due to the bridging of source and drain by m-SWCNTs in the shorter channel devices of both global and local category, their on-off current ratio is lower compared to devices with the longer channel lengths. The local gate devices have higher on-off current ratio, due to the close proximity of the gate structure to the SWCNT thin-film resulting in better control over the channel compared to global gate devices.

The on-current density of both global and local gate devices for various channel lengths measured at V_{GS} of -5 V are plotted in Fig. 8.3(b). The current densities of local gate SN-TFTs are always higher compared to global gate devices. The on-current density difference between the local and global gate devices increases as a function of channel length, because local gate has better control

TH-1861_07610208

over the channel than global gate structure. The transconductance of the local gate SN-TFTs is greater compared to the global gate SN-TFTs again because of better control over the transistor channel. Fig. 8.3(c) shows the normalized transconductance of local and global back gate SN-TFTs as a function of the channel length. Similarly, the carrier mobility of the local back gate SN-TFT is higher compared to the global gate devices for various channel dimensions as plotted in Fig. 8.3(d).

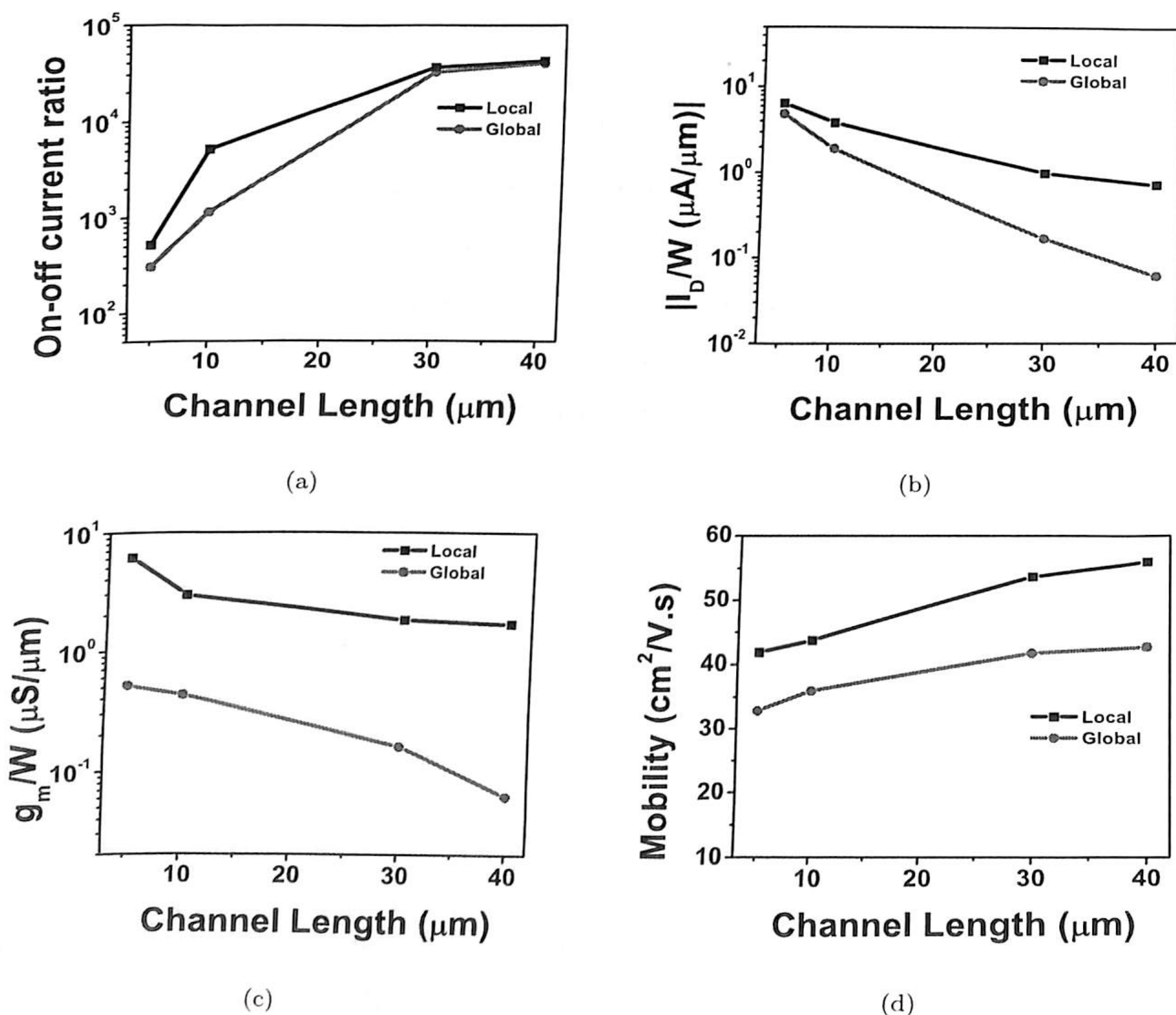

Figure 8.3: Electrical parameters of global and local gate SN-TFTs as a function of channel length. (a) Drain current on-off ratio. (b) On-current density (I_D/W). (c) Normalized transconductance. (d) Carrier mobility.

The local gate SN-TFTs are compared with other global gate [46,47] and top gate [113] SN-TFTs reported in the literature. The channel length of 10 μm is considered for comparison purpose. The

TH-1861_07610208

Table 8.2: Performance comparison of global and local gate SN-TFTs of identical channel lengths.

Parameter	[PW]	[PW]	[46]	[47]	[47]	[113]
Nanotube density (SWCNTs/μm^2)	40-45	40-45	21-32	3	3	25
Threshold voltage (V)	-0.5	-1.5	-5	NR	NR	-2.5
Subthreshold slope (V/decade)	0.4	0.6	2	NR	NR	5
Current density ($\mu A/\mu m$)	3.8	1.9	1.2	NR	NR	NR
On-off current ratio	5.4×10^3	1.2×10^3	2×10^2	3	3	10^5
Normalized transconductance ($\mu S/\mu m$)	2.9	0.42	0.1	0.07	0.01	NR
Carrier mobility ($cm^2/V{\cdot}s$)	43	36	32	80	12	8
Gate-dielectric	HfO_X	HfO_X	SiO_2	SiO_2	SiO_2	Al_2O_3
s-SWCNT purity (%)	95	95	95	67	67	NR
Nanotube orientation	Random	Random	Random	Aligned	Random	Aligned
Gate structure	L	G	G	G	G	T

PW-Present work, NR-Not reported, L-Local back, G-Global back, T-Top

SN-TFTs with thin-film of random and aligned SWCNTs having various semiconducting purities are considered to examine the effect of SWCNT orientation and purity of the s-SWCNTs on the device performance. Table 8.2 lists various process and the electrical parameters of different SN-TFTs. A random network of SWCNTs deposited on the silanized HfO_X have higher SWCNT density compared to other reported values. Because of higher SWCNT density, the proposed devices have exhibited larger current density compared to reported device in [46] with similar purity s-SWCNTs. the local back gate devices of the present work with HfO_X as the gate oxide have exhibited the lowest threshold voltage, which is tenfold lower compared to the value reported for global back gate SN-TFTs with similar s-SWCNT purity [46]. Our global back gate device has exhibited 3 times lower threshold voltage when compared to other global gate device with same purity SWCNTs [46]. Among the local and global categories, the local back gate SN-TFTs have exhibited a steep subthreshold swing compared to global back gate devices. It may be noticed that local gate SN-TFT of the present work has a subthreshold swing which is ten fold steeper compared to top gate devices having aligned SWCNT network [113] and is fivefold steeper than global gate devices with random network SWCNTs [46].

Table 8.2 shows that the local gate SN-TFT of the present work has exhibited an on-off current ratio of 5.3×10^3 which is about twenty five times higher compared to similar type of devices with global back gate structure of identical channel length [46]. In order to obtain the on-off current, the

TH-1861_07610208

gate voltages for the present local gate SN-TFT, is varied from -5 V to 3 V compared to -10 V to 10 V for reported global back gate devices [46]. This improvement in the on-off ratio of the proposed devices is achieved by the use of SWCNTs of average length 1 μm compared to 1.7 μm for other devices [46] and also by higher density of SWCNTs. The probability of bridging the source contact with drain contact by the m-SWCNT network will be higher in the case of the longer SWCNTs compared to the shorter tubes. However, the on-off current ratio of the proposed devices is lower when compared to the devices reported in [113]. The main reasons for higher on-off ratio of the devices [113] are use of higher purity s-SWCNTs (99%) and the aligned network of SWCNTs.

The normalized transconductance of the proposed local and global gate devices is greater compared to the other reported global gate SN-TFTs [46, 47] and this can be attributed to the high density of SWCNTs and the use of high-k gate dielectric material. The charge carrier mobility of different devices is also discussed. The SN-TFTs of the present work with random network of SWCNTs have exhibited higher average μ compared to other SN-TFTs, except for the devices reported in [47]. The reason for greater mobility for devices reported in [47] is probably the presence of as-grown SWCNTs, which contains 33% m-SWCNTs as compared to 5% in the proposed device. The improved μ of the local gate device compared to other devices is due to it's high density SWCNTs, high-k gate dielectric and localized gate control. In summary, the local back gate SN-TFTs with random network of SWCNTs deposited over the amino-silane treated HfO_x surface have exhibited adequate on-off ratio, reduced threshold voltage, steeper subthreshold swing, higher normalized transconductance and better mobility when compared to global back gate or top gate devices having random or aligned network of SWCNTs.

8.4 Summary

In this chapter, electrical performance of SN-TFTs with the gate structure located at top, bottom, and both at top-bottom (dual) of the SWCNT thin-film channel having identical dimensions fabricated under same process conditions were compared. The dual gate SN-TFT has shown an on-off ratio more than 10^3, subthreshold slope of 280 mV/decade and threshold voltage of -0.65 V. To the best of our knowledge, the obtained subthreshold slope for the dual gate device is the lowest value reported for SN-TFTs. The threshold voltage of the dual gate SN-TFT was reduced by at the least of 350 mV when compared to the single gate SN-TFTs of similar dimensions. These performance

TH-1861_07610208

improvements are mainly due to better control of the transistor channel by the dual gate structure and HfO_x as the gate oxide. The wafer scale SN-TFTs with SWCNT thin-film deposited on the HfO_x having local and global back gate contact are also compared. Because of better control over the transistor channel, the local back gate SN-TFTs have exhibited better performance compared to the global gate devices of identical dimensions. The local back gate device with HfO_x gate dielectric material had showed a higher current density and higher mobility compared not only to the this work global gate devices, but also previously reported SN-TFTs.

TH-1861_07610208

9 Conclusion

Contents

9.1 Contributions 128
9.2 Directions for Future Research 130

TH-1861_07610208

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9.1 Contributions

The work carried out in this thesis can be divided into three parts. The first part presented the study on SWCNT interconnects, the second part dealt with the modeling of SWCNT transistors and design of analog circuits based on SWCNTs. Finally the third and major part addressed the fabrication and characterization of 9 different thin film transistors based on SWCNTs. The major contributions of the entire thesis are briefly categorized as follows.

(i) **Impact of bias voltage on magnetic inductance of carbon nanotube interconnects**

The magnetic inductance of the carbon nanotube interconnects at various bias voltages was estimated. The analysis of magnetic inductance was carried out for the GSG configuration of SWCNT based interconnects having various dimensions and different percentage of m-SWCNT purity. The simulation study of the interconnects having the as-grown SWCNTs showed a 21% change in the loop inductance when the bias voltage was varied from 0.1 to 1 V for the closely spaced lines of length 10 μm, but for longer length interconnects it was less than 1%. It was observed that the percentage of m-SWCNT content in the nanotube bundle also influence the inductance and therefore it is essential to have a good control over the chirality during the synthesis of SWCNTs, in order to use them for the analog circuit applications.

(ii) **Design of CNFET based analog amplifiers**

To enable the analog circuit design based on the CNFETs, closed-form equations for drain current and drain to source voltage in terms of the device dimensions were derived for a MOSFET-like CNFET using the curve fitting method. The performance of common source amplifiers and a single stage differential amplifier were compared with the CMOS counterparts. This performance comparison study showed that the CNFET based analog circuits have higher DC gain and large gain band width product at the same power dissipation. The effect of process variations in terms of the diameter, spacing and number of SWCNTs on the performance of CNFET analog circuits were also analyzed.

(iii) **Fabrication and characterization of wafer scale global back gate thin-film transistors using different semiconducting purity nanotubes and dielectric materials**

Wafer scale global gate SN-TFTs of various channel dimensions having SiO_2 and HfO_X as the gate oxide using 90% and 95% s-SWCNTs were fabricated. A systematic study of the

TH-1861_07610208

Indian Institute of Technology Guwahati

electrical performance of devices having different gate dielectric material has been carried out for identical dimension SN-TFTs. The HfO_x based SN-TFTs have shown a reduction of 300 mV in the threshold voltage compared to the devices based on SiO_2. Due to the higher gate capacitance, HfO_x based SN-TFTs have exhibited a maximum current density compared to SiO_2 based device. The performance of identical channel dimension SN-TFTs having 90% and 95% s-SWCNTs fabricated under identical process conditions were compared. A 100 μm channel length SN-TFT with 95% pure s-SWCNTs has exhibited an on-off ratio of 6×10^4 as against 4×10^3 for an identical channel dimension device with 90% s-SWCNTs. The devices with 90% purity have exhibited higher current density compared to 95% purity s-SWCNTs. The high performance and high on-current global gate SN-TFT has also been demonstrated and has obtained higher on-current, lower threshold voltage, higher on-off ratio and steeper subthreshold swing compared to other reported high on-current SN-TFTs.

(iv) **Fabrication and characterization of high performance wafer scale local gate SN-TFTs**

For the first time wafer scale local back gate SN-TFTs with HfO_x as the gate oxide and a technique to deposit the SWCNT thin-film of densities 40-45 SWCNTs/μm^2 over the silanized HfO_x surface is reported. The local back gate SN-TFT has exhibited a low threshold voltage of -500 mV and a steep subthreshold swing of 400 mV/decade. The obtained current density, normalized transconductance and mobility values were better when compared to reported devices. The *C-V* characteristics on the local back gate SN-TFTs was measured and to our knowledge this is the first *C-V* curves on SN-TFTs reported.

(v) **Performance comparison of SN-TFTs having different gate structures**

The SN-TFTs having top, back and dual gate structures of identical channel dimensions were demonstrated. The dual gate SN-TFT having a subthreshold slope of 280 mV/decade was the steepest value obtained so far for SN-TFTs. The dual gate SN-TFT has also exhibited better performance in terms of the threshold voltage and the mobility compared to similar dimension single gate devices of present work due to greater control over the transistor channel. The wafer scale SN-TFTs having the local and global back gate structures were also compared. Because of the better control over the transistor channel, the local back gate devices have exhibited

TH-1861_07610208

better performance compared to the global gate devices of identical dimensions. The local back gate device having HfO_x gate dielectric material had showed a higher current density and higher mobility compared to both present work global gate devices and also previously reported SN-TFTs.

The process and performance parameters all 9 different types of SN-TFTs fabricated in this work are summarized in Table 9.1. The table includes SN-TFTs having different gate structure, gate dielectric material, purity of s-SWCNTs and source/drain contacts. The dip-coat as well as the immersion techniques were employed to deposit the SWCNT thin-film. The dry thermal oxidation, the RF sputtering and the FIB technique were used to deposit different gate oxides. The threshold voltage of -500 mV obtained for SN-TFT 7 was the minimum compared to all other types of SN-TFTs and this can be attributed to the high-k gate dielectric, the local gate structure and high density SWCNT thin-film employed. Due to the better channel control, the dual gate device (SN-TFT 9) has exhibited a subthreshold swing of 280 mV/decade, which was the steepest slope not only among the devices fabricated in this work, but also for the devices reported in the literature. The SN-TFTs using 95% s-SWCNT thin-film have exhibited an on-off current ratio in excess of 10^4 and for the devices with 90% s-SWCNT thin-film the ratio was in excess of 10^3. The maximum I_D/W of 13 μA/μm was exhibited by the local gate device (SN-TFT 7) having a channel length of 2 μm and it has been been observed the current density depends on various factors such as channel length, the gate structure and the SWCNT density. Similarly, the maximum mobility was also exhibited by the local gate device and wide range variation in the mobility values among the devices may attributed to various reasons such as trapped charges in the oxide layers, the channel dimensions, the density of SWCNTs and the gate dielectric material. Except the top gate (SN-TFT 8) and the dual gate (SN-TFT 9) devices, all other cases multiple devices were fabricated simultaneously on wafer scale.

9.2 Directions for Future Research

(i) **Study of transistor dimensions mismatch in CNFET based differential amplifier**

The reliable circuit design based on SWCNT devices is really a challenging task because of large process variations and device mismatches involved. The influence of process variations and device mismatches and its implications on the analog circuit performance should be investigated. Offering many useful properties, differential operation has become the dominant

TH-1861_07610208

choice in today's high performance analog and mixed signal circuits and therefore an investigation on how much device dimension mismatch a classical differential pair between signal or load transistors can tolerate will be relevant.

(ii) **High density SWCNT thin-film**

Presently the achieved densities of SWCNTs in thin films are less than 50 nanotubes/μm^2 and theoretically one could accommodate a maximum of 500 SWCNTs having average diameter of 2 nm in a micrometer width. As the performance of SN-TFTs depends heavily on the density of SWCNTs of thin-film, there is a need for methods to deposit high density (hundreds of SWCNTs/μm^2) on wafer scale to achieve high performance operations.

(iii) **Flexible SN-TFTs**

Lightweight and flexible devices such as mobile phones, Radio Frequency Identification (RFID) tags, flexible displays and electronic papers are gaining attention for their roles in achieving a smarter and green ubiquitous information society. The demonstrated high performance local back SN-TFTs of the current work may be considered for fabrication on flexible surfaces with appropriate process modifications.

TH-1861_07610208

Table 9.1: Performance comparison of various SN-TFTs fabricated in this work.

Parameter	SN-TFT 1	SN-TFT 2	SN-TFT 3	SN-TFT 4	SN-TFT 5	SN-TFT 6	SN-TFT 7	SN-TFT 8	SN-TFT 9
Threshold voltage (V)	-1.85	-1.8	-1.55	-1.5	-1.2	-1.0	-0.5	-1	-0.65
Subthreshold slope (V/decade)	0.9	0.85	0.85	0.75	0.7	0.6	0.4	1.3	0.28
On-off current ratio	4×10^3	6×10^4	4.5×10^3	7.45×10^4	6.2×10^3	4×10^4	5×10^4	2×10^2	1.2×10^3
Current density I_D/W (μA/μm)	0.16	0.12	0.41	0.302	8.4	6.2	13.03	0.13	0.51
Normalized transconductance g_m/W (μS/μm)	0.014	0.013	0.075	0.071	0.74	0.7	18.5	0.02	0.31
Carrier mobility (cm^2/V·s)	5.02	4.98	33.8	32.6	46	44.2	60.6	0.1	2.26
s-SWCNT purity (%)	90	95	90	95	90	95	95	95	95
Gate-dielectric	SiO_2	SiO_2	HfO_X	HfO_X	HfO_X	HfO_X	HfO_X	SiO_2	SiO_2/HfO_X
Gate structure	G	G	G	G	G	G	L	T	D
Dielectric structure	DT	DT	DT	DT	RF	RF	RF	FIB	FIB/RF
Nanotube Deposition	D	D	D	D	I	I	I	I	I
Source/drain contact	IDE	IDE	IDE	IDE	N	N	N	N	N
Device quantity	WS	WS	WS	WS	WS	WS	WS	S	S

L-Local back, G-Global back, T-Top, IDE-Interdigitated, N-Normal, DT-Dry thermal oxidation, RF-RF sputtering, FIB-Focused Ion Beam, D-Dip coat, *I-Immersion, WS-Wafer scale, S-Single*

TH-1861_07610208

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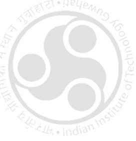

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List of Publications

Journal Publications

1. K. C. Narasimhamurthy and Roy Paily, "Fabrication of Carbon Nanotube Field-Effect Transistor," *IETE Technical Review*, vol. 28, pp. 57-69, Jan.-Feb. 2011.

2. K. C. Narasimhamurthy and Roy Paily, "Fabrication and Performance Comparison of Interdigitated Thin-Film Field-Effect Transistors using Different Purity Semiconducting Carbon Nanotubes," *Advanced Materials Research*, vol. 181-182, pp. 343-348, Jan. 2011.

3. K. C. Narasimhamurthy and Roy Paily, "High Performance Local Back Gate Thin-Film Field-Effect Transistors using Sorted Carbon Nanotubes on an Amino-Silane Treated Hafnium-Oxide Surface," *Semiconductor Science and Technology.*, publication scheduled for vol. 26 Mar. 2011.

Manuscripts Submitted:

1. K. C. Narasimhamurthy and Roy Paily, "Design and Simulation of Analog Amplifier Circuits using Carbon Nanotube Field-Effect Transistors," Oct. 2010, submitted to *IETE Journal of Research.*

2. K. C. Narasimhamurthy and Roy Paily, "Performance Comparison of Single Gate and Dual Gate Carbon Nanotube Thin-Film Field-Effect Transistors," Nov. 2010, submitted to *IEEE Trans. Electron Devices.*

3. K. C. Narasimhamurthy and Roy Paily, "Fabrication and Characterization of High Performance and High Current Back Gate Thin-Film Field-Effect Transistors using Sorted Single Walled Carbon Nanotubes," Dec. 2010, submitted to *Circuits, Devices and Systems.*

4. K. C. Narasimhamurthy and Roy Paily, "Wafer Scale Thin-Film Transistors using Different Semiconducting Purity Nanotubes, Dielectric Materials and Gate Control" Jan. 2011 submitted to *IEEE Trans. Nanotechnology.*

TH-1861_07610208

Conference Publications

1. K. C. Narasimhamurthy and Roy Paily, "Impact of Bias Voltage on Magnetic Inductance of Carbon Nanotube Interconnects.," *Proc. 22nd Int. Conf. on VLSI Design*, Dec. 2009, New Delhi, India, pp. 505-510.

2. K. C. Narasimhamurthy and Roy Paily, "Fabrication and Characterization of Carbon Nanotube thin-film Field Effect Transistor using sorted SWCNTs," *Proc. Int. Conf. on Advanced Material and Science*, Oct. 2010, Trivandrum, Kerala, India, pp. 52-57.

3. K. C. Narasimhamurthy and Roy Paily, "Performance Comparison of Thin-Film Transistors Fabricated using Different Purity Semiconducting Nanotubes," *Proc. 24th Int. Conf. on VLSI Design*, Jan. 2011, Chennai, India. pp. 208-213.

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