INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI
SHORT ABSTRACT OF THESIS

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SHORT ABSTRACT

With the advancement of technology and autonomous systems, such as electric vehicles, high electron mobility transistor (HEMT) have gained prominence in the present era. However, the reliability of HEMTs depends on many factors, viz. electric field, electron temperature, self-heating and converse piezoelectric effect, leakage current. In this thesis, various techniques for the mitigation of electric field are proposed. Electric field is primarily responsible for the degradation of a device as it induces majority of the degradation mechanisms. In a conventional device, the gate edge is rectangular in shape and electric field crowding is observed at the gate edge toward the drain side. In this thesis, a method is proposed to mitigate electric field at the gate edge of a device by modifying shape of the gate edge. Although gate shape engineering is well-known for the enhancement of device performance with slant gate, a particular gate–shape (rounded gate edge) is depicted in this thesis. The electric field reduces by ~45% and ~68% for rounded gate device without and with field plate, respectively. The moderation in electric field further assists in the reduction of electron temperature for rounded gate device without and with field plate by ~12% and ~85%, respectively. Similarly, breakdown voltage for rounded gate device is found to increase by 10% as compared to breakdown voltage of rectangular gate device.

Field plate technology is widely implemented to moderate high electric field at the drain edge of the gate of a device. The field plate topology assists in the uniform distribution of electric field in the gate–drain access region, and aids in the increase of breakdown voltage of a device. Additionally, as a consequence of shorter device gate length in the field plate structure, the gate to drain spacing shrinks, which results in an electric field peak at the field plate edge, when the device is biased in the SEMI-ON state. In this thesis, to mitigate this issue, the use of diamond layer is proposed on the top of a passivation layer with a SiO_2 pocket at the edge of a field plate. It is observed that employing diamond layer with a SiO_2 pocket at the edge of a field plate on the top of a passivation layer reduces electric field profile, carrier temperature, self heating and thermal resistance of the device by 43%, 20%, 13%, and 47%, respectively. This helps in the reduction of device degradation, which is initiated at the edge of a field plate, and increases device reliability.