Abstract

The throughput requirement of latest OFDM based IEEE 802.11ay WLAN standard is between 20 to 40 Gbps. Also, the FFT processor needed for OFDM must work in continuous mode for real time communication. The number of FFT points can be variable. In this thesis, we propose a Continuous flow architecture for a 512 point FFT to meet this requirement at about 28 Gbps. The number of points are kept fixed here to illustrate the essential features of the design. They can be varied, if desired, with minimal architectural modifications. Architectures to meet the throughput requirement (10 Gbps) of earlier WLAN standard IEEE 802.11ad have been reported in the literature. The proposed architecture achieves more than double this throughput at 28 Gbps with similar chip area and clock as the best existing 10 Gbps designs. This is made possible through a specialized design for OFDM unlike the earlier FFT chips which were designed for general purpose FFT. The proposed architecture uses two radix-16 and one radix-2 stages to meet the high throughput requirement. Standard continuous flow (CF) FFT designs use two memories. The proposed design exploits the smaller wordlength of 4 bit (for 64 QAM) of OFDM to introduce an additional smaller input memory and a simpler processing element (PE) for the input stage. Combined with the existing two memories, there are now three memories for the three stage FFT. Thus this design allows memories to assume dedicated roles for each stage. Compared to the existing practice of switching of memories, dedicated memories need a novel addressing scheme to maintain CF as data is replaced in same memory rather than switching the memories.

Another feature of the architecture is that each memory feeds a single stage PE and is not shared with other stages. Thus, a simplified conflict free memory bank access circuit is developed which saves area. Conflict-free addressing (CFA) techniques are necessary for all FFT hardware. For low radices, well-proven XOR-based addressing architectures are available in the literature. In the previous CFA techniques, the complexity increases with increasing radices or memory sets. In the proposed technique, the higher number of memory sets and radix is an advantage. A novel scheme is suggested to reduce the complexity using a progressive shifting technique. The mathematical basis of the scheme is derived here and illustrated with an example of 512-point radix-16 FFT. The proposed and existing CFA architectures are designed using verilog and synthesized in the SCL library. The result of synthesis shows that the proposed scheme achieves a 33% area reduction compared to the XOR-based scheme. The area reduction factor further improves with a higher number of FFT points.

A comprehensive theory for CF is formulated and two CF schemes are proposed both of which save significant switching area and power. CF of data for mixed-radices is a challenge because the output index bit-pattern is asymmetric to that of the input. Reported CF techniques are all based on data reordering to make the address symmetric. Mostly, they are specific to an architecture and lack any mathematical framework. Additionally, the presented solutions are applicable only for particular stages of the architecture. In this thesis, group theory is used to develop a universal data reordering scheme for CF. It is proved to be valid for all mixtures of radices and is applicable to all the stages viz. input, intermediate and output. This thesis further proposes that an alternative to shifting of data is to shift the addresses instead. A mathematical framework is developed which uses group theory to prove that a circular periodicity in addresses exists for FFT algorithms. This periodicity allows new addresses to be generated without any reordering of data. Depending on the FFT architecture, either technique may result in minimum hardware. A mixed radix-16 FFT processor with 512 points is designed using both the techniques and the ASIC synthesis results on SCL technology show that the overall designs are about 70% more area efficient compared to the existing designs. The 512-point chip accomplishes FFT symbol processing in 32 clock cycles compared with 74 clock cycles of earlier processors. The design synthesized in 90 nm technology meets the 4.8 GSps (28 Gbps) processing rate at a clock speed of 300 MHz. To test its functionality, the chip is fabricated in SCL 180 nm technology and packaged in 120 pin package.