SHORT ABSTRACT

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Title: LongLiveNoC: Wear Levelling, Write Reduction and Selective VC allocation for Long lasting Dark Silicon aware NoC Interconnects

Short Abstract of PhD Thesis: Increasing processing demand has led to the development of chip multiprocessors which can have multiple to many cores connected with each other and with the on-chip caches. These connections are established by an on-chip packet switched Network-on-Chip (NoC). Scaling of technology nodes increases the power dissipated by the chips leading to thermal restrictions. To control the chip thermal design power, certain components (like cores and caches) may be turned off. However, in this scenario of dark silicon, the interconnect is expected to be available.

The thesis aims to save power consumed by this always ON interconnect by replacing the power hungry SRAM buffers in the routers with low leakage Non-Volatile Memory (NVM) based buffers.However, the major challenges with the employment of the NVMs are slower writes and weak write endurance.

The thesis proposes:

1. Methods to evenly distribute the writes across these NVM buffers in order to increase their lifetime. This is done by static and dynamic allocation of buffers to the virtual channels and their selection during packet transmission.
2. Power can also be saved by using frequency scaling of the routers and/or turning off certain buffers when the usage is less. Investigation is done for all such approaches and power savings is demonstrated.
3. Endurance can be improved and energy can be saved if we can reduce the number of writes performed on the buffers. This is achieved by proposing two compression techniques leading to reduced network traffic and improved lifetime.

All the above methods help in improving the lifetime of the NVM based NoC interconnects in the context of dark silicon.