DESIGN, OPTIMIZATION, AND MODELLING OF HYBRID ORGANIC INORGANIC PEROVSKITE MEMRISTORS

A Thesis submitted for the award of the degree of
Doctor of Philosophy

By
Himangshu Jyoti Gogoi

Under the supervision of
Dr. Arun Tej Mallajosyula

Department of Electronics and Electrical Engineering
Indian Institute of Technology Guwahati
Guwahati-781039, Assam, India
August, 2022

DECLARATION

This is to declare that the thesis entitled "**Design, Optimization, and Modelling of Hybrid Organic Inorganic Perovskite Memristors**", submitted by me to the *Department of Electronics and Electrical Engineering, Indian Institute of Technology Guwahati*, for the award of the degree of Doctor of Philosophy. This is an original research work carried out under the supervision of **Dr. Arun Tej Mallajosyula**. The contents of this thesis, in full or parts, have not been submitted to any other institute or university for the award of any degree or diploma.

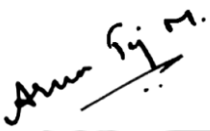
Signed: 

Himangshu Jyoti Gogoi
Department of Electronics and Electrical Engineering,
Indian Institute of Technology Guwahati,
Guwahati-781039, Assam, India.

Date: 12/5/2023

CERTIFICATE

This is to certify that the thesis entitled "**Design, Optimization, and Modelling of Hybrid Organic Inorganic Perovskite Memristors**", submitted by **Himangshu Jyoti Gogoi** (166102004), a research scholar in the *Department of Electronics and Electrical Engineering, Indian Institute of Technology Guwahati*, for the award of the degree of **Doctor of Philosophy**, is a record of an original research work carried out by him under my supervision and guidance. The thesis has fulfilled all requirements as per the regulations of the institute and, in my opinion, has reached the standard needed for submission. The results embodied in this thesis have not been submitted to any other institute or university for the award of any degree or diploma.

Signed: 

Dr. Arun Tej Mallajosyula
Department of Electronics and Electrical Engineering,
Indian Institute of Technology Guwahati,
Guwahati-781039, Assam, India.

Date: 12/5/2023

Acknowledgements

I am highly privileged to take this opportunity to express my sincere and honest gratitude to my thesis supervisor, Dr. Arun Tej Mallajosyula, for his constant guidance, support, and motivation throughout the research work. His clear vision helped me work on such an emerging field of research as memristive devices, fabrication, and characterization of hybrid organic-inorganic perovskite devices. During the regular group meetings and individual discussions, I have gained a lot of technical and non-technical knowledge from his deep theoretical knowledge and vast experimental experiences, which will surely help me in my future endeavours.

I would like to thank my doctoral committee members, Prof. Roy P. Paily (chairman), Prof. Harshal B. Nemade, and Prof. Parameswar K Iyer, for sparing their valuable time to evaluate my progress in the research work and providing insightful suggestions leading to the improvement of my thesis. I am also thankful to the Head of the Department of Electronics and Electrical Engineering for allowing me to use the department facilities that was required for my research work. I further thank all the technical and office staff of the EEE department who helped me access various lab resources and with various official works. I am also highly thankful to Prof. Aditya Mohite, (Rice University, USA) and Dr. Ankur Solanki (Pandit Deendayal Energy University, Gujrat, India) for their valuable comments and suggestions over the multiple online and offline discussions, which gave my research work a better focus and direction.

I am highly grateful to Prof. Parameswar Iyer for allowing me to work in DST sponsored Organic Electronics Laboratory. Furthermore, I am thankful to Dr. Mohammad Adil Afroz and Dr. Rahul Narasimhan, my seniors from Organic Electronic Lab in IIT Guwahati, who, helped me learn all the fabrication and characterization tools required for my research, despite their hectic research work. I would also like to thank the staff and operators of the instruments I have used in Center for Nanotechnology and Central

Instrument facility for giving me access to the instruments and helping me analyse the results in the best possible way.

I would like to thank my friends and colleagues I have worked with in various labs at IIT Guwahati. I am delighted to express my sincere thanks to my research groupmates under the same supervisor, namely Abdul Basit Andrabi, Atanu Purukayastha, Abinash Baruah, and Muddam Rajashekhar, for the numerous technical discussions, as well as the wonderful time we have spent together in the laboratory and outside, over these years. I would also like to thank Mr. Paban Bujor Baruah, technical officer in the EEE department and my friend since our graduation days, for all the help and support over the years, from multiple technical and generic discussions/arguments to various favours at the personal level.

The acknowledgement section would be incomplete without mentioning my loving family members. I am truly grateful to my mother and father for providing all kinds of support and freedom to pursue my dream without any worry. I want to thank my brother and his family for being there and taking care of me and my responsibilities while I am away from home for all these years. I am also thankful to my parents in-law for their utmost love and trust in me. Lastly, but definitely, the most important person in my life, my wife, Dr. Priyanka Borah, who has been like the anchor through all my ups and downs in life since our school days. I am sincerely thankful for her unconditional love, care, support, and encouragement.

Himangshu Jyoti Gogoi

Abstract

Memristor (memory + resistor) is the fourth basic circuit element beyond resistor, capacitor and inductor. It establishes a relationship between flux and charge and its present resistance depends on its past state. With fast switching speeds (~picoseconds), low power consumption (~femto-joule/bit), long write/erase endurance, and high scalability (nano-meter scale), memristors have strongly captured the attention of research community in the fields of neuromorphic computation, artificial intelligence, ultra-dense data storage, and logic circuits.

On the other hand, hybrid organic-inorganic perovskites (HOIPs) have recently become strong candidates for high-efficiency low-temperature solution processable solar cells. HOIPs show a mixed ionic-electronic conduction where the halide counter ions are mobile under an electric field. Due of this, the current-voltage (I-V) characteristics of HOIP devices can be tuned to exhibit the signature memristor property of pinched hysteresis. Also, HOIPs tend to have longer carrier diffusion lengths and higher crystallinity than the organic semiconductors, making them more suitable for flexible memristors. Development of a resistive random-access memory (ReRAM) technology based on HOIP memristors, thus, can realize flexible and fast non-volatile memories. In this context, understanding their switching mechanisms and modelling their I-V characteristics are necessary for performance optimization and circuit simulation. However, to date, there is neither a standard characterization procedure nor a device model are available for these memristors. This thesis work attempts to bridge some of these research gaps.

The effects of electroforming and measurement processes on the performance of commercial memristors have been analyzed to identify the critical parameters determining their switching behaviour. Memristors using 3D methyl ammonium lead iodide ($MAPbI_3$) on glass and on flexible substrates have been fabricated and optimized

to obtain reproducible characteristics. A procedure to extract the best possible switching parameters such as ON/OFF ratio, SET voltage, RESET voltage etc. from 3D HOIP memristors has been developed. Two different types of bipolar resistive switching (BRS) have been obtained from the same $MAPbI_3$ device by changing the polarity of the applied field. In addition, by controlling the compliance current, complementary resistive switching, which is highly useful in minimizing sneak-path currents in ReRAMs, has also been obtained from these devices. Dominant current conduction mechanisms under high and low resistance states, for both types of BRSs, have been identified and used in developing an algorithm for SPICE-based simulation of 3D HOIP memristors. The model has been validated by fitting with the experimental data. Layered 2D Ruddelson-Popper (RP) butyl ammonium lead iodide (BA_2PbI_4) memristors, which have better environmental stability than their 3D counterparts, have also been fabricated and characterized at low temperatures. The model developed for 3D $MAPbI_3$ devices has been found to fit these RP devices as well.

TABLE OF CONTENTS

List of Acronyms

0D	Zero-Dimensional
1D	One-Dimensional
1D1M	One Diode One Memristor
2D	Two-Dimensional
3D	Three-Dimensional
AFM	Atomic Force Microscope
AI	Artificial Intelligence
BE	Bottom Electrode
BRS	Bipolar Resistive Switching
CAD	Computer Aided Design
CBRAM	Conductive Bridge Resistive Random Access Memory
CDF	Cumulative Distribution Function
CF	Conductive Filament
CRS	Complementary Resistive Switching
DFT	Density Function Theory
DIP	Dual-in-Line Package
DJ	Dion-Jacobson
DLTS	Deep Level Transient Spectroscopy
DRAM	Dynamic Random-Access Memory
ECM	Electrochemical Metallization
EPSC	Excitatory Postsynaptic Current
ETL	Electron Transport Layer
FEM	Finite Element Method
FESEM	Field Emission Scanning Electron Microscope
HDD	Hard-Disk Drive
HOIP	Hybrid Organic-Inorganic Perovskite
HRS	High Resistance State
HTL	Hole Transporting Layer
IC	Integrated Circuit

IEEE	Institute of Electrical and Electronics Engineers
IoT	Internet of Things
IRDS	International Roadmap for Devices and Systems
IRS	Intermediate Resistance State
KMC	Kinetic Monte Carlo
LRS	Low Resistance State
LTP	Long-Term Plasticity
MRS	Multifunctional Resistive Switching
MSS	Meta-Stable Switch
PCM	Phase Change Memory
PUF	Physical Unclonable Function
ReRAM	Resistive Random-Access Memory
RP	Ruddlesden-Popper
RS	Resistive Switching
SCLC	Space Charge Limited Current
SCS	Semiconductor Characterization System
SDC	Self-Directed Channel
STDP	Spike-Timing-Dependent Plasticity
STP	Short-Term Plasticity
STT RAM	Spin-Transfer Torque Random-Access Memory
SR	Scan Rate
SRAM	Static Random Access Memory
SRDP	Spike Rate-Dependent Plasticity
TEAM	Threshold Adaptive Memristor
URS	Unipolar Resistive Switching
VCM	Valance Change Memristor
WM	Window Margin
XRD	X-Ray Diffraction
ZB	Zettabytes

List of Symbols

α	Coefficient of temperature
ε	Permittivity of the material
ϕ_b	Energy barrier at the metal-semiconductor interface
η	Direction of voltage sweep
μ	Carrier mobility
a	Height of the substrate during bending
b	Distance between two edges of the substrate during bending
d	Device thickness
E	Applied field
E_a	Thermal activation energy
E_{RESET}	RESET field
f	Reduced electric field due to barrier lowering
F	Minimum feature size
$F_X(x)$	Cumulative distribution function
I_{CC}	Compliance current
I_i	Iodine interstitial
I_{RESET}	RESET current
I_{HRS}	Current during the HRS
I_{LRS}	Current during the LRS
I_o	HRS current at absolute zero
J	Current density
J_{Th}	Thermionic emission limited current density
J_{Tl}	Tunnelling limited current density
M	Neutral metal atom
MA_i	Methyl ammonium interstitial
MA_I	Methyl ammonium antisite substitution in lead
$M(q)$	Memristance
M^{z+}	Positive metal cation
N_o	Charge density
O_o	Oxygen atom on the regular lattice
O_i^{2-}	Oxygen atom not on the regular lattice
Pb_i	Lead interstitial

Pb_I	Lead antisite substitution in methyl ammonium
R_{HRS}	HRS resistance
R_{LRS}	LRS resistance
R_b	Bending radius
R_o	Resistance at absolute zero
t_{exe}	Execution time
t_{RESET}	Reset pulse width
$V_{FORMING}$	Forming voltage
V_I	Iodine vacancy
V_{MA}	Methyl ammonium vacancy
V_{Pb}	Lead vacancy
V_{pp}	Peak-to-peak voltage
V_{Range}	Voltage sweep range
V_{READ}	Read voltage
V_{RESET}	RESET voltage
V_{SET}	SET voltage
V_{STOP}	STOP voltage
V_p	Voltage threshold during the positive applied voltage
V_n	Voltage threshold during the negative applied voltage
V_o^{2+}	Oxygen vacancy on a regular lattice
X	Random variable
$x(v,t)$	State variable
x_p	State variable threshold during the positive applied voltage
x_n	State variable threshold during the negative applied voltage
w_p	Window function during the positive applied voltage
w_n	Window function during the negative applied voltage

List of Figures

List of Tables

CHAPTER 1

Introduction

Contents

1.1 Introduction

The dramatic shift toward digitization of almost every aspect of our lives resulted in the growth of the digital data creation and consumption from 2 zettabytes (ZB) to 64 ZB from 2010 to 2020. By 2025, global data creation is projected to cross 180 ZB, added, partly, by the enhanced data demand due to the COVID-19 pandemic [1]. This high growth rate resulted in an increased desire for a "universal memory" device with outstanding capabilities such as high data transfer speed, high storage capacity, non-volatility, and low-voltage operation. In terms of the dominant memories existing today, these requirements necessitate a device that combines the merits of flash memory, hard-disk drive (HDD), and dynamic random-access memory (DRAM). With a simple two-terminal device structure, nanoscale dimensions, and multiple resistance states, the *memristor* could be a viable solution.

Memristor (memory + resistor) was predicted in 1971 by Leon Chua as the fourth basic circuit element beyond resistor, capacitor, and inductor [2]. The resistance state of a memristor remains unchanged until and unless a new input is applied, which is the basis of non-volatile memory. In addition, the unique feature of the dependence of resistance state on past states makes memristors useful to mimic the synaptic behaviour in the brain, unfolding the possibility of their use in neuromorphic computation [3]. Since the first report on its physical realization in 2008 from Hewlett-Packard (HP) Labs [4], memristor has captured tremendous attention of the researchers in various fields such as data storage, neuromorphic computation, quantum computing, etc. (see figure 1.1). Furthermore, the emergence of artificial intelligence (AI), the internet of things (IoTs), and cloud computing augmented the use of semiconductor devices in areas such as wearable electronics, implantable personal healthcare, and smart medical applications. All these applications require mechanically flexible memories, which can be realized with memristors.

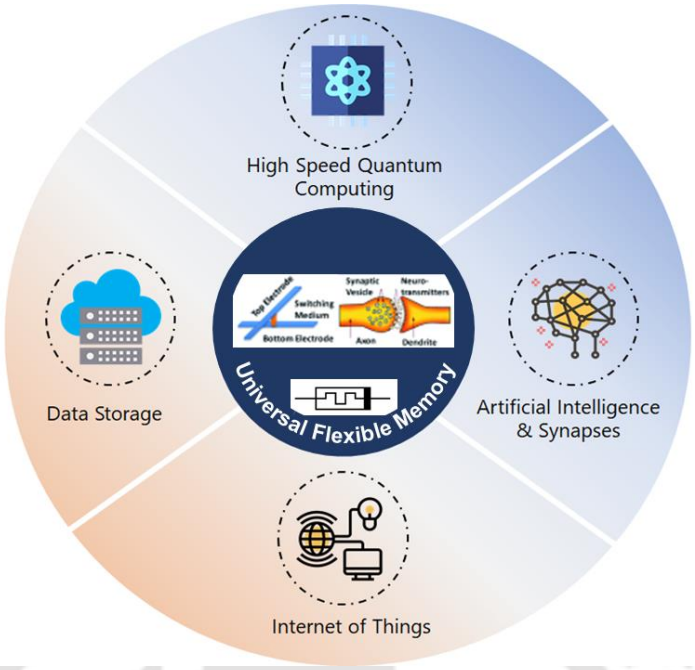


Figure 1.1: Various applications of memristors such as data storage, quantum computing, artificial intelligence, and internet of things [5].

1.1.1 The Fourth Basic Circuit Element

The three classical circuit elements we come across in our basic circuit theory are resistors (R), capacitors (C) and inductors (L). They relate the four fundamental circuit variables, namely voltage (v), current (i), charge (q), and flux (φ), with one another according to the equations (1.1), (1.2), and (1.3) below.

$$R = \frac{dv}{di} \tag{1.1}$$

$$C = \frac{dq}{dv} \tag{1.2}$$

$$L = \frac{d\varphi}{di} \tag{1.3}$$

Chua noted, on theoretical grounds, that these four variables lead to six possible combinations, out of which only five were established, as can be seen from the symmetry diagram in figure 1.2(a). This figure shows the four basic circuit parameters and their relation with basic circuit elements. Chua argued that there has to be another basic element which relates q and φ, from both a logical point of view as well as for the sake of completeness. He found that the resistance of the missing element changes depending on

the charge flowing through it and that this resistance remains unchanged until the next flow of charge is introduced [2]. In other words, this element is a variable resistor which remembers its previous resistance state. Hence, he coined the name memristor (short for memory resistor) for the newly proposed element. Mathematically, it can be defined as

$$M(q) = \frac{d\varphi(q)}{dq} \tag{1.4}$$

where M is the dynamic resistance of the memristor, termed as memristance. Chua showed that the memristor could not be realized by any combination of other passive elements, no matter how nonlinear these elements are. This proved the fundamental and passive nature of the memristor [6]. The current-voltage (I-V) characteristics of a memristor bear a pinched hysteresis loop, which is shown in figure 1.2(b) for a sinusoidal input and a random $\varphi(q)$ function.

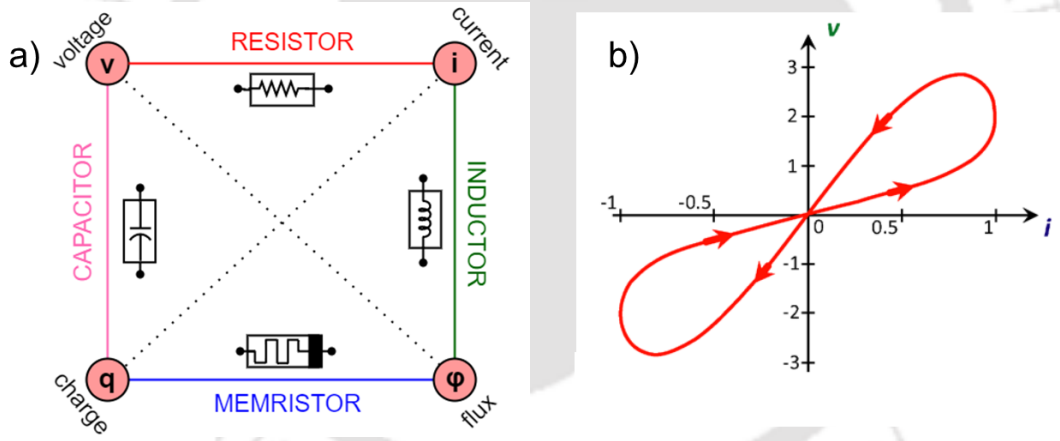


Figure 1.2: (a) The four fundamental two-terminal circuit elements: resistor, capacitor, inductor, and memristor. (b) Pinched hysteresis loop obtained from an ideal memristor for a sinusoidal input and a random $\varphi(q)$ function [7].

1.1.2 The First Memristor

Over the next four decades, many researchers reported anomalous/hysteresis behaviour that resembles memristive behaviour. However, no physical memristor has been realized over these years. In the year 2008, Strukov and Williams from HP Labs came up with a nano-size device comprising a titanium dioxide (TiO_2) layer sandwiched between two platinum electrodes [4]. Figure 1.3(a) shows an atomic force microscope (AFM) image of seventeen such nano-memristors in parallel [8]. Some part of the TiO_2

layer is made with oxygen vacancies, giving rise to a composition of TiO_{2-x} instead of TiO_2. Figure 1.3(b) and 1.3(c) show the working schematic and the experimental resistive switching (RS) I-V characteristics of the HP Labs memristor, respectively. While TiO_2 is electrically insulating by nature, TiO_{2-x} is conductive because its oxygen vacancies are donors of electrons. This makes the vacancies themselves to be positively charged and they can be driven by an external field. On the application of an external bias, the boundary between two resistive regions shifts, which changes the internal resistance of the device and, hence, the current through it [4].

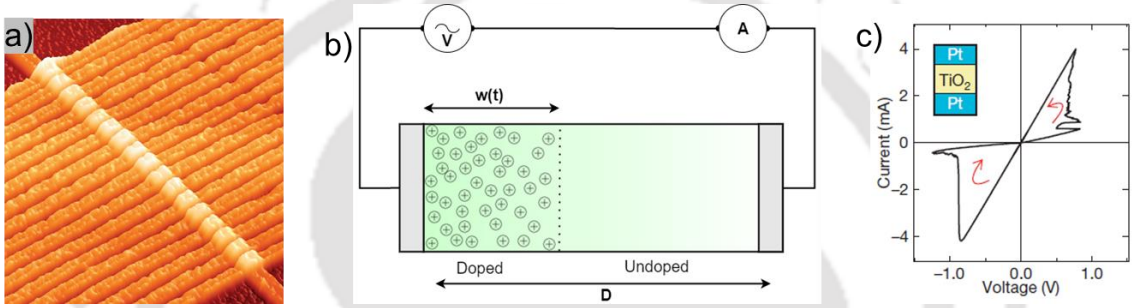


Figure 1.3: (a) AFM image of seventeen nano-memristor in parallel fabricated by HP Labs [8]. (b) A simplified equivalent model of a typical memristor with an external bias V. D represents the total thickness of the switching layer and w(t) is the state variable, which represents the length of the doped region. (c) experimental bipolar RS I-V plot obtained from $Pt/TiO_{2-x}/Pt$ memristor by HP Labs [4].

1.2 Types of Memristors

Because of their wide ranging structures, switching mechanisms, materials, and applications, memristors can be classified in various ways. Based on the switching phenomena, they are broadly divided into two types - Filament Type Memristors and Barrier Type Memristors [9-11].

1.2.1 Filament-Type Memristor

In this type of memristor, formation and rupture of conductive filament/s (CFs) occur inside an insulating layer, showing either bipolar resistive switching (BRS) or unipolar resistive switching (URS). This process is shown in figure 1.4. The filament/s can form due to the movement of vacancies, ions, charged atoms, or any other mobile species of the material. Depending upon the chemical composition, these memristors can

be further divided into two - Valance Change Memristor (VCM) and Electrochemical Metallization Memristor (ECM) [9].

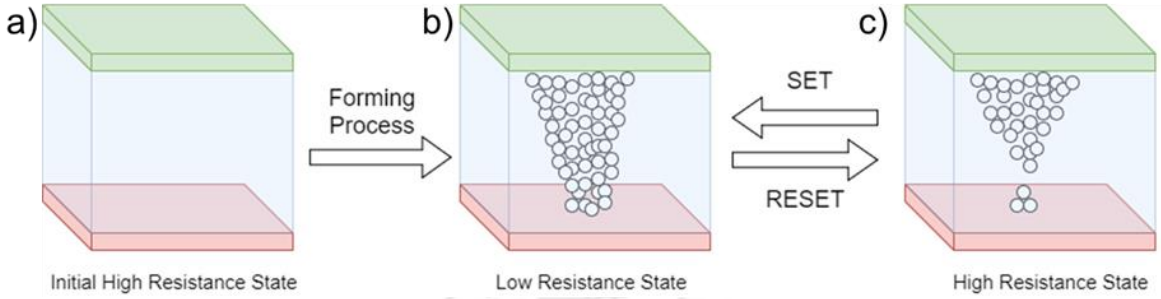


Figure 1.4: Schematic illustration of filamentary RS process in MIM structure. (a) Pristine device before electroforming. (b) Formation of conducting filament in the insulating medium under an external field, leading to low resistance state (SET process). (c) Rupture of the filament in reverse field direction, leading to high resistance state (RESET process) [9].

In case of VCMs, anions in the insulating layer migrate on the application of a voltage, resulting in the formation/rupture of CFs. During the forming/SET process, defects (e.g., oxygen anion-vacancy pairs) can be created inside the insulating layer through impact ionization, which can be described by:

$$O_o \rightarrow V_o^{2+} + O_i^{2-} \tag{1.5}$$

at anode $$O_i^{2-} \rightarrow 2e^- + \frac{1}{2}O_2 \tag{1.6}$$

at cathode $$M^{z+} + ne^- \rightarrow M^{(z-n)+} \tag{1.7}$$

where O_o and O_i^{2-} denote oxygen atoms on and not on the regular lattice, respectively, V_o^{2+} represents the oxygen vacancy on a regular lattice, and M^{z+} denotes the positive metal cation. The reduction process at the cathode (see equation (1.7)) leads to valence change of the metal cations, and hence the name valance change memristors [12].

In the ECM type of memristors, metallic cations are the migratory species, and the insulating layer is a solid electrolyte film in which metal ions have high mobility. One electrode is electrochemically active, supplying the metal cations, and the counter electrode is inert. Metallic cations migrate towards the other electrode, driven by an electric field, or a concentration gradient, or both. The dynamic chemical changes are as follows:

At the active anode, $M \rightarrow M^{z+} + ze^{-}$ (1.8)

At the inert cathode, $M^{z+} + ze^{-} \rightarrow M$ (1.9)

When a complete CF is established between the two electrodes, the device resistance switches from the high resistance state (HRS) to low resistance state (LRS). An opposite electric field ruptures the CF and switches back the device from LRS to HRS. Both the electric field and thermal effects are involved in this RS process. While the electric field effect dominates in the case of bipolar switching, the thermal effect plays a major role in unipolar switching [3].

1.2.2 Barrier-Type Memristor

Like the filament-type memristors, the barrier-type memristors also have an insulating layer sandwiched between two electrodes. However, the resistance switching (RS) in them originates from the modification of the barrier at one or both of the metal|insulator interfaces. These memristors can further be classified as Schottky barrier-type and ferroelectric tunnel barrier-type devices.

In the case of a Schottky barrier-type memristor, a Schottky barrier is formed at one of the metal|insulator interfaces and an ohmic contact at the other interface. Due to the redistribution of the atoms/vacancies/ions in the insulating layer, the barrier width and height change and, as a result, the resistance state of the device changes. As schematically shown in figure 1.5(a), when ions/vacancies accumulate at the interface, the depletion region width reduces, leading the device to its LRS. When the ions/vacancies migrate away from the interface due to the application of an electric field having opposite polarity, the donor density decreases and the depletion region widens, leading the device from LRS to HRS [13].

Ferroelectric tunnel barrier memristors consist of an ultrathin (~nm) ferroelectric material sandwiched between two electrodes, forming a tunnelling resistance at the metal|insulator interface [14]. By applying an electric field, the ferroelectric film

modulates the barrier, which is different for leftward and rightward polarizations. Switching the ferroelectric polarization creates a significant change in tunnel resistance and the memristor changes its resistance state accordingly. The schematic of the RS phenomena in this device is illustrated in figure 1.5(b) below.

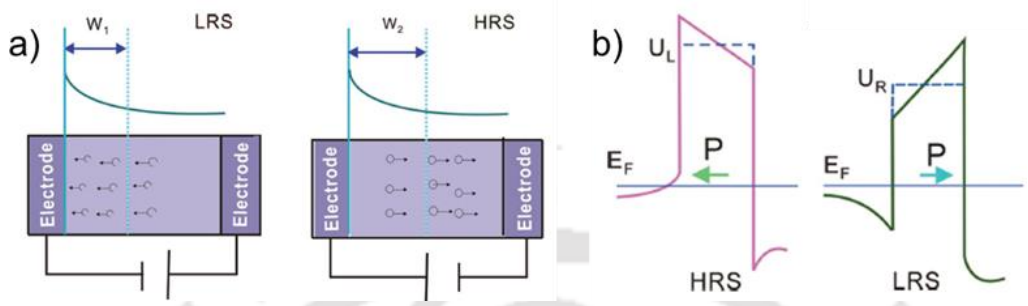


Figure 1.5: (a) Schematic representation of oxygen vacancies redistribution under external electric field in a Schottky barrier type memristor; when the vacancies accumulate at the interface, the barrier width decreases, and the device switched to LRS (left figure), when the vacancies move away from the interface, the barrier width increases and the device switched to HRS (right figure). (b) Schematic representation of a ferroelectric barrier type memristor, where the uneven potential profiles under opposing ferroelectric polarization give rise to the HRS (left figure) and LRS (right figure) [9].

1.3 Memristor as Non-Volatile Memory

Memristive devices have the potential to be used in ultra-high density computing technologies. One immediate application for these devices is Resistive Random-Access Memories (ReRAMs) with digital-type current switching characteristics and large ON/OFF ratio. ReRAMs are non-volatile and can have a performance that is at least comparable to, if not better than, that of DRAMs and flash memories. As shown in figure 1.6(a), the device resistance switches sharply between two of its extreme states, R_{ON} (LRS or ON state) and R_{OFF} (HRS or OFF state). Owing to their simple Metal-Insulator-Metal (MIM) type of structures, the size of a single cell can be scaled down to 10 nm or below. In the MIM structure, the two metals are top electrode (TE) and the bottom electrode (BE). When implemented in the form of a cross-point array, the memory cells have an area of about $4F^2$, where F is the minimum feature size (see figure 1.6(b)), allowing realization of dense memories. Next generation high-density non-volatile memories are expected to have properties such as small write voltage (few hundred mV),

small write time (~10 ns), small read voltage (V_{READ}) so that there is no change of internal resistance, high OFF to ON resistance ratio (~10), high endurance (~10^7 cycles), high retentivity (~10 years), three-dimensional stacking ability, and compatibility with complementary metal oxide semiconductor technology [16]. Table 1.1 shows the properties of the memristor as a memory cell compared to other state-of-the-art memory technologies and a few emerging technologies. From the table, it can be seen that the memristor has all the desired properties of the universal non-volatile memory [16].

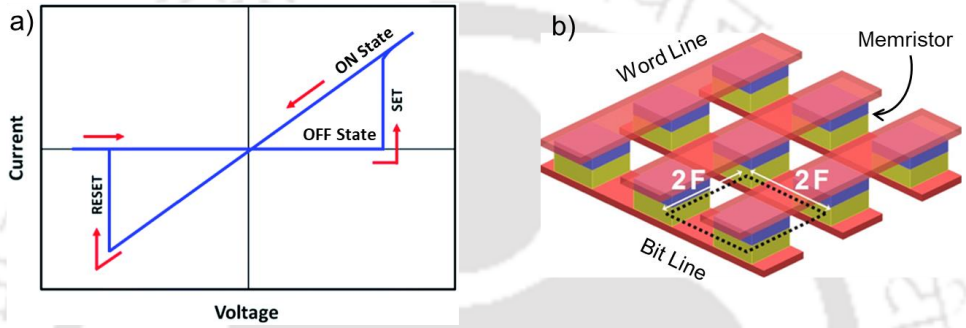


Figure 1.6: (a) Digital type RS current-voltage characteristics useful for the application of memristors in ReRAMs [13]. (b) Schematic of a memristor cross-point array with per cell area of $4F^2$, where F is the minimum feature size; the TEs and the BEs are called 'word line' and 'bit lines', respectively [17].

Table 1.1: Comparison of memory and storage technologies (DRAM: Dynamic Random Access Memory; SRAM: Static Random Access Memory; PCM: Phase Change Memory; STT RAM: Spin-Transfer Torque Random-Access Memory) [3,9]

	Current Baseline Technologies			**Emerging Technologies**		
	DRAM	SRAM	Flash NAND	PCM	STT RAM	Memristor
Feature Size (nm)	36-65	45	16	45	65	5
Cell Area (xF^2)	6-30	140	4	4	20	4
Read Time	2-10 ns	0.2 ns	0.1 ms	12 ns	35 ns	<10 ns
Write Time	2-10 ns	0.2 ns	0.1–1.0 ms	100 ns	35 ns	<10 ns
Retention	4-64 ms	N/A	10 years	>10 years	> 10 years	> 10 years

Traditional computing systems suffer from the well-known Von Neumann bottleneck, where frequent data transfers between the processor and memory units incur large energy consumption and limit the throughput (shown schematically in figure 1.7(a)) [18]. Memristor cross-point arrays have the ability of 'in-memory' computing, where data storage and information processing take place simultaneously. Figure 1.7(b) demonstrates an example of such an in-memory computing to perform vector-matrix multiplication. The voltage on each bit line represents the input, which gets multiplied with the conductance (data) of the corresponding cell stored locally as per Ohm's law. The current collected from each word line as per Kirchhoff's law, gives vector product. This potential technology, integrating memory and processor into a single unit can help computation go beyond the conventional Von Neumann architecture and realize massive parallel computing [9].

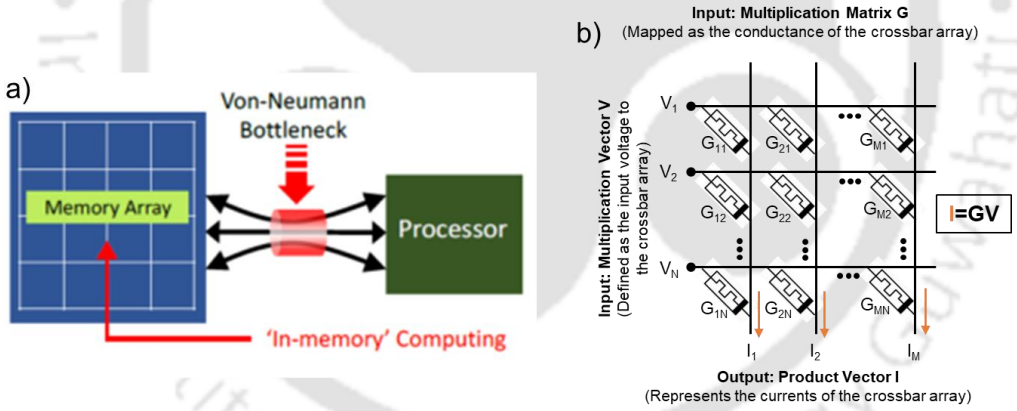


Figure 1.7: (a) Schematic representation of Von-Neumann bottleneck, where the processor and memory units are separately located and frequent data transfers between them incur large energy consumption and limit the throughput [18]. (b) In-memory computation of vector-matrix multiplication directly using Ohm's and Kirchhoff's laws. Applied (read) voltages and conductance of memristor devices in a crossbar array define an input vector and an input matrix, whereas sensed currents provide a resulting vector multiplication.

1.4 Memristor as Artificial Synapse

Brain-inspired computing or neuromorphic computing has emerged as a new computing paradigm to enable massively parallel analog computing. Table 1.2 lists some of the terms frequently encountered in this field of research. When an action potential reaches the end of a preneuron, exchange of certain ions (e.g., Ca^{2+}, Na^{+}, etc.) takes place

in the synapse, which causes the change of synaptic plasticity. Considering the involvement of combined ionic and electronic conduction mechanism, as well as low power operation, low cost, and easy high-density fabrication processes, memristors are most suitable for realizing a two-terminal artificial synapse [19]. The BE and TE of the memristor act as the preneurons and postneurons, respectively (see figure 1.8(a)). Memristors with analog-type switching behaviour are characterized by the continuous and incremental change of device resistance (see figure 1.8(b)), which is used to represent the synaptic weights. Several synaptic devices based on various functional materials and their synaptic behaviours in response to external stimulation signals have been reported [20]. These signals mainly include electrical and optical pulses, which alter certain physical properties of the functional materials and, thereby, mimic synaptic functions such as memorizing and forgetting, learning, and decision making (e.g., STDP, SRDP, EPSC, STP, and LTP, as described in table 1.2) in neural circuits [21].

Table 1.2: Terminology associated with neuromorphic computing

Terminology	**Description**
Neuromorphic Computing	It is a method of computation which is modelled similar to that in the human brain and nervous system.
Biological Synapse	Synapse acts as a bridge between two neurons (human brain cells) and information in the form of signals are transmitted from one neuron to other by the exchange of ions (e.g., Na^+, K^+, Ca^{2+}, etc.) chemically.
Preneuron	It is the cell that sends the signal.
Postneuron	It is the cell that receives the signal.
Artificial Synapse	Artificial synapses emulate biological synaptic functions in neuromorphic computing systems to attain brain-like computation.
Synaptic Plasticity	It is the strength of the connection between the preneuron and postneuron.
Synaptic Weight	Synaptic plasticity is quantitatively represented in terms synaptic weight (ΔW). In case of memristor based artificial synapse, ΔW can be considered as the change of conductance.
Synaptic Functions	Synaptic functions are the variety of cognitive functions performed by the biological synapse such as learning, thinking, reasoning, remembering, problem solving, decision making, etc.

Presynaptic spike	When an action potential reaches the end of a preneuron, it triggers a potential spike, which is called presynaptic spike.
Postsynaptic spike	Based on the chemical changes in the synapse, a potential spike is triggered at the postneuron, which is called postsynaptic spike.
Potentiation	It is the increase in synaptic weight.
Depression	It is the decrease in synaptic weight.
Spike-Timing-Dependent Plasticity (STDP)	It is the change of synaptic weight based on the relative timing between the presynaptic spike and postsynaptic spike.
Spike Rate-Dependent Plasticity (SRDP)	It is the change of synaptic weight based on the rate of presynaptic spike and postsynaptic spike.
Long-Term Plasticity (LTP)	It is the persistent strengthening of the synaptic weight due to application of repeated spikes with short interval. This is the mechanism the governs learning and memory in human brain.
Short-Term Plasticity (STP)	It is the persistent strengthening of the synaptic weight due to application of repeated spikes with short interval.
Excitatory Postsynaptic Current (EPSC)	It is the abrupt change in the postsynaptic current due to application of a presynaptic spikes, which is also a measure of synaptic weight.

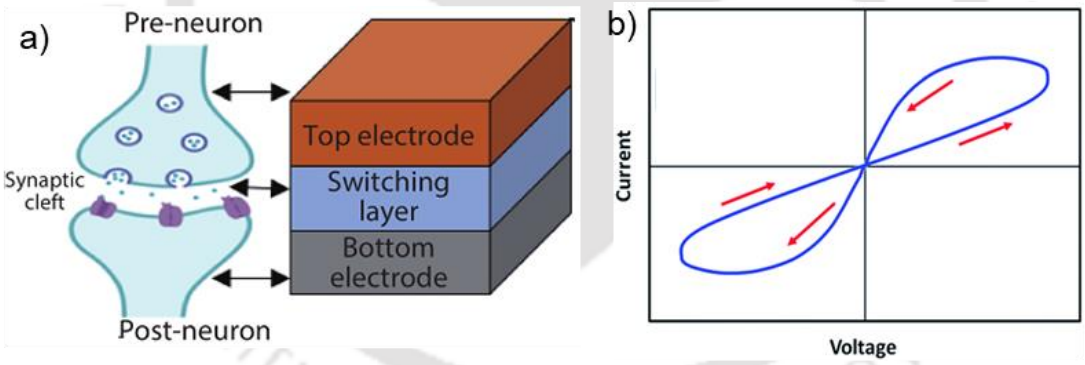


Figure 1.8: (a) Schematic diagram of a biological synapse, including presynaptic membrane, postsynaptic membrane, and the synaptic cleft; they are represented by the TE, BE and the switching layer respectively in a memristor structure. b) Analog type (incremental) of RS current-voltage characteristics that can be used for the application of memristor as artificial synapse [15].

1.5 Motivation and Research Gaps

To date, several materials have been proposed for the functional layer of memristors, including metal oxides [22-24], chalcogenides [25-27], organic semiconductors [28,29], amorphous silicon [30], and amorphous carbon [31]. Unlike these, hybrid organic-inorganic perovskites (HOIPs) benefit considerably from their mixed ionic-electronic conduction behaviour, i.e., the halide counter ions of HOIPs are

mobile under an electric field [32]. In addition, HOIPs have several other excellent electronic properties such as band gap tunability, long carrier diffusion lengths, strong optical absorption etc., which make them the materials of choice for applications such as solar cells, light-emitting diodes, photodetectors, lasers, thin film transistors, and terahertz devices [33]. Another advantage of HOIPs is that high crystallinity can be achieved relatively easily using low-temperature solution processing methods, which allows them to be used with low-cost, flexible substrates [5]. The I-V characteristics of these HOIP devices show the property of hysteresis which, when controlled, can resemble that of a memristor. Memory technology based on HOIP memristors, thus, can realize flexible and non-volatile ultra-dense ReRAMs useful for several applications including logic design.

It is imperative that, to be made applicable for commercial next-generation non-volatile memory applications and alternative logic architectures, HOIP memory performance, at the very least, must be comparable to state-of-the-art technologies based on SRAM, DRAM, and flash memories. However, a major issue with HOIPs is their inherent instability under the presence of oxygen and moisture. Using 2D layered HOIPs can, in principle, mitigate this effect. In addition, since different physical mechanisms have been proposed for driving the hysteresis, there remains an ambiguity regarding how one can control and model the switching properties of HOIP memristors. Moreover, the characterization procedure itself can affect the device parameters. Thus, there are major gaps in the path to achieve stable HOIP memristors with well-defined and optimized switching characteristics.

In general, since memristive action have been reported for a wide range of materials involving different physical phenomena, arriving at an all-encompassing analytical model for memristors is a difficult task. Moreover, these devices exhibit an inherent stochasticity. Thus, the development of device specific models could be of help.

From the stand point of HOIP memristors, no compact model is available that can be readily used for their simulation in crossbar arrays and in other logic circuits.

1.6 Formulation of the Problem Statement

With the major aim of realizing an optimized solution-processed HOIP-based memristor with reproducible characteristics and analyze its switching behaviour, this work attempts to achieve the same by including the following as the thesis objectives:

1. Study the effect of characterization and electroforming procedure on the memristor behaviour. Using the commercially available chalcogenide memristors, determine the critical control parameters and extract the most optimized performance from them.

2. Using the chalcogenide memristor behaviour as a reference, develop a characterization protocol for solution-processed Methyl ammonium lead iodide ($MAPbI_3$) memristors. Fabricate flexible devices, optimize them for their ON/OFF ratio and switching voltages, and test their bendability.

3. Understand the current conduction and switching mechanisms of $MAPbI_3$ devices using I-V, pulse I-V, C-V, and low-temperature I-V characterization. Develop a simulation algorithm to mimic the memristive characteristics that fit the experimental results in order to facilitate numerical analysis and to be useful in circuit design tools.

4. Develop a fabrication and characterization process for low-dimensional HOIP memristors. Compare the stability of these devices with their 3D counterparts.

1.7 Organization of the Thesis

The thesis is divided into seven chapters including the present chapter 1. Chapter 2 presents a thorough literature review on the materials for memristive systems, focusing on HOIPs, their properties, and the different physical mechanisms of RS action. In addition, the state-of-the-art of HOIP memristive systems and their applicability to various fields such as non-volatile memories, artificial synapse, photonics and logic

applications, etc., are also reviewed. Finally, the chapter ends with a brief review of the analytical models for memristors available in the literature.

Chapter 3 describes the studies done to understand the effect of the measurement method and electroforming procedure on the performance of memristors, using commercially available devices. Different characterizations that were carried out using these memristors and the inferences from these are summarized in this chapter.

Chapter 4 explains the fabrication procedure and the RS characteristics of solution-processed 3D $MAPbI_3$ memristors along with their electroforming process. It also describes a characterization protocol that is proposed to extract optimum switching characteristics, in general, from any HOIP-based memristive device. The performance of the devices fabricated on flexible substrates is also described in this chapter.

Chapter 5 shows two different types of RS obtained from the same $MAPbI_3$ device using electric fields of opposing polarities. In addition, based on the experimental data fitting and SPICE simulations, an algorithm is proposed to emulate memristive I-V characteristics.

In chapter 6, studies on low-dimension HOIP memristors are presented, which are inherently more moisture-resistant. The thickness- and temperature-dependent I-V characteristics are analyzed to understand the current conduction and switching mechanisms in these devices.

Finally, chapter 7 summarises the major contributions and limitations of this work, and presents a brief on the future prospects.

1.8 References

[1] "Total data volume worldwide 2010-2025," by Statista Research Department, May 23, 2022. [Online]. Available: https://www.statista.com/statistics/871513/worldwide-data-created/.

[2] L. Chua, "Memristor-The missing circuit element," IEEE Transactions on Circuit Theory, vol. 18, no. 5, pp. 507–519, 1971.

[3] J. J. Yang *et al.*, "Memristive switching mechanism for metal/oxide/metal nanodevices," Nature Nanotechnology, vol. 3, no. 7, pp. 429–433, 2008.

[4] D. B. Strukov *et al.*, “The missing memristor found,” Nature, vol. 453, no. 7191, pp. 80–83, 2008.
[5] H. J. Gogoi *et al.*, “Advances in flexible memristors with hybrid perovskites,” Journal of Physical Chemistry Letters, vol. 12, no. 36, pp. 8798–8825, 2021.
[6] L. Chua, “If it’s pinched it’s a memristor,” Semiconductor Science and Technology, vol. 29, no. 10, p. 104001, 2014.
[7] L. Chua, “Resistance switching memories are memristors,” Applied Physics A: Materials Science and Processing, vol. 102, no. 4, pp. 765–783, 2011.
[8] R. S. Williams, “How we found the missing memristor,” IEEE Spectrum, 28-Nov-2008. [Online]. Available: https://spectrum.ieee.org/how-we-found-the-missing-memristor.
[9] S. G. Hu *et al.*, “Review of nanostructured resistive switching memristor and its applications,” Nanoscience Nanotechnology Letters, vol. 6, no. 9, 2014.
[10] J. Borghetti *et al.*, “Memristive switches enable 'stateful' logic operations via material implication," Nature, vol. 464, no. 7290, pp. 873–876, 2010.
[11] A. G. Radwan and M. E. Fouda, "On the mathematical modeling of memristor, memcapacitor, and meminductor," Cham: Springer International Publishing, 2015.
[12] R. Waser *et al.*, “Redox-based resistive switching memories-nanoionic mechanisms, prospects, and challenges," Advanced Materials, vol. 21, no. 25–26, pp. 2632–2663, 2009.
[13] J. J. Yang *et al.*, “Memristive devices for computing," Nature Nanotechnology, vol. 8, no. 1, pp. 13–24, 2013.
[14] J. Rodríguez Contreras *et al.*, “Resistive switching in metal–ferroelectric–metal junctions," Applied Physics Letters, vol. 83, no. 22, pp. 4595–4597, 2003.
[15] N. Ahmadabadi, H. "High performance CMOS-compatible perovskite oxide memristors: compositional control and nanoscale switching characteristics.", School of Electrical and Computer Engineering, PhD Thesis, RMIT University, 2015.
[16] Y. Chen *et al.*, “Polymer memristor for information storage and neuromorphic applications,” Materials Horizons, vol. 1, no. 5, pp. 489–506, 2014.
[17] D. Panda and T.-Y. Tseng, “Perovskite oxides as resistive switching memories: A review,” Ferroelectrics, vol. 471, no. 1, pp. 23–64, 2014.
[18] G. W. Burr *et al.*, “Phase change memory technology,” Vacuum Science and Technology B:Nanotechnology and Microelectronics, vol. 28, no. 2, pp. 223–262, 2010.
[19] T. Ohno *et al.*, “Short-term plasticity and long-term potentiation mimicked in single inorganic synapses,” Nature Materials, vol. 10, no. 8, pp. 591–595, 2011.
[20] S. Hamdioui *et al.*, “Memristor based computation-in-memory architecture for data-intensive applications,” in Proceedings of the 2015 Design, Automation and Test in Europe Conference and Exhibition, Grenoble, France, pp. 1718–1725, 2015.
[21] W. Huang *et al.*, “Memristive artificial synapses for neuromorphic computing,” Nano-Micro Letters, vol. 13, no. 1, p. 85, 2021.
[22] D. Kuzum et al., “Synaptic electronics: materials, devices and applications,” Nanotechnology, vol. 24, no. 38, p. 382001, 2013.
[23] Y. Wang *et al.*, "Investigation of resistive switching in Cu-doped HfO_2 thin film for multilevel non-volatile memory applications," Nanotechnology, vol. 21, no. 4, p. 045202, 2010.
[24] Y. T. Li *et al.*, "Investigation of resistive switching behaviours in WO_3-based RRAM devices," Chinese Physics B, vol. 20, no. 1, p. 017305, 2011.
[25] D. H. Kwon *et al.*, "Atomic structure of conducting nanofilaments in TiO_2 resistive switching memory," Nature Nanotechnology, vol. 5, no. 2, pp. 148–153, 2010.

[26] J. van den Hurk *et al.*, "Ag/GeS_x/Pt-based complementary resistive switches for hybrid CMOS/nanoelectronic logic and memory architectures," Scientific Reports, vol. 3, no. 1, p. 2856, 2013.

[27] S. J. Choi *et al.*, "Multibit operation of Cu/Cu-GeTe/W resistive memory device controlled by pulse voltage magnitude and width," IEEE Electron Device Letters, vol. 32, no. 3, pp. 375–377, 2011.

[28] A. Nayak *et al.*, "Controlling the synaptic plasticity of a Cu_2S gap-type atomic switch," Advanced Functional Materials, vol. 22, no. 17, pp. 3606–3613, 2012.

[29] S. Wu *et al.*, "A polymer-electrolyte-based atomic switch," Advanced Functional Materials, vol. 21, no. 1, pp. 93–99, 2011.

[30] S. Gao *et al.*, "Conductance quantization in a Ag filament-based polymer resistive memory," Nanotechnology, vol. 24, no. 33, p. 335201, 2013.

[31] S. H. Jo *et al.*, "High-density crossbar arrays based on a Si memristive system," Nano Letters, vol. 9, no. 2, pp. 870–874, 2009.

[32] W. Tress, "Metal Halide perovskites as mixed electronic–ionic conductors: Challenges and opportunities—from hysteresis to memristivity," Journal of Physical Chemistry Letters, vol. 8, no. 13, pp. 3106–3114, 2017.

[33] J. Choi *et al.*, "Organic-inorganic hybrid Halide perovskites for memories, transistors, and artificial synapses," Advanced Materials, vol. 30, no. 42, p. e1704002, 2018.

CHAPTER 2

Literature Survey

Contents

2.1 Introduction

Hybrid-organic inorganic perovskites (HOIPs) based memristors have captured strong attention of the research community not only as emerging candidates not only for the next generation high-density information storage technology but also for healthcare technology and the Internet of Things (IoT). This is attributed to their unique properties of lightweight, flexibility, stretchability, low-temperature processability, low power consumption etc. In this chapter, we retrospect the recent advancements in various aspects of memristors, including the selection of the active materials. Several RS mechanisms of HOIP memristors have been summarized, along with a systematic review of the state-of-the-art in the application of memristors for artificial synapse, light-induced RS, and logic gates. Several analytical and circuit equivalent models are available in the literature, which attempt to mimic the memristor characteristics. At the end of this chapter, we present a comparative summary of these memristor models along with their advantages and limitations.

2.2 Materials for Memristors

Herein, we have divided the functional materials for memristive applications into three broad categories: inorganic, organic, and hybrid materials (HOIPs), as discussed below.

2.2.1 Inorganic Materials

As mentioned in chapter 1, the first memristor prepared by Strukov *et al.* consists of a capacitor-like structure, sandwiching a bilayer composed of a stoichiometric titanium oxide layer (TiO_2) and a non-stoichiometric titanium sub-oxide layer (TiO_{2-x}) between two platinum (Pt) electrodes [1] (see figure 2.1). Since then, several research groups have focused on developing new functional materials and electrodes to achieve efficient memristors for different applications. Various oxides such as HfO_2, SiO_2, TiO_2, CuO,

NiO, WO_x, etc., have been used for memristive devices, showing promising RS performance [2-4]. Beyond the above-mentioned three-dimensional (3D) oxides, two-dimensional (2D) materials such as graphene, nitrides (e.g., BN), transition metal dichalcogenides (e.g., MoS_2 and WS_2), InSe, SnS, TiS_2, etc., have also emerged in this category [5-7]. Some of the memristors based on these materials have low power consumption, high efficiency, non-volatile characteristics, and can be fabricated at nanoscale. However, most of them involve sophisticated and costly fabrication technologies requiring high-temperature processing, which limits their applicability.

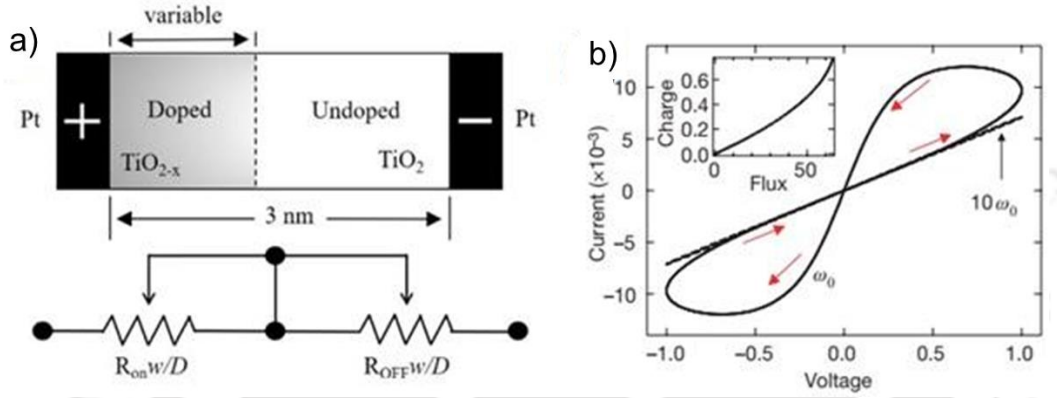


Figure 2.1: (a) Schematic of the Pt/TiO_{2-x}/TiO_2/Pt memristor structure and its representation in the form of two discrete resistances. (b) Simulated I-V characteristics of memristors from HP Labs [1].

2.2.2 Organic Materials

Compared to traditional oxides and low-dimensional materials, organic compounds seem to be more attractive for RS memory applications due to their higher intrinsic flexibility, easier solution processability, and non-toxicity. Certain organic semiconductors such as poly(3-hexylthiophene) (P3HT), poly(,4-ethylenedioxythiophene): polystyrene sulphonate (PEDOT:PSS), phenyl-C_{61}-butyric acid methyl ester (PCBM), etc. have been the pillars in the advancement of organic photovoltaics, light-emitting diodes, and transistors [8-10]. As functional materials, they have also been successfully used for demonstrating memristive action, along with others such as phenanthro[9,10-d]imidazole (PFT-PI), polyaniline (PANI), copper-

tetracyanoquinodimethane (Cu-TCNQ), poly(N-vinylcarbazole) (PVK), etc. [11-13]. However, these organic materials have significantly lesser carrier mobilities, which result in devices with relatively higher operating voltages.

2.2.3 Hybrid Organic-Inorganic Perovskites (HOIPs)

Perovskites are compounds having a generic chemical formula ABX_3 (see figure 2.2(a)). In this structure, A is a monovalent organic cation (methylammonium (MA^+), formamidinium (FA^+), guanidinium (GA^+), etc.) that resides at the eight corners of the cubic unit cell, B is, typically, a divalent metal cation that resides at the body centre of the cube (Pb^{2+}, Sn^{2+}, Eu^{2+}, Cu^{2+}etc.), and X is a halide anion (Cl^-, Br^-, I^-, etc.). Six face-centred X anions form an $[BX_6]^{4-}$ octahedral cluster. There are a wide variety of HOIPs due to the several possible combinations for each of A, B, and X. For example, the $[PbI_6]^{4-}$ octahedral can form 3D, 2D, one-dimensional (1D) or zero-dimensional (0D) networks. To form a 3D structure (say, with $MAPbI_3$, Formamidinium lead iodide ($FAPbI_3$), or Guanidinium lead triiodide ($GAPbI_3$), $[PbI_6]^{4-}$ octahedron is connected with six neighbours at the iodide, and the corresponding counter cation (MA^+, FA^+, or GA^+) is located at the void of the network (see figure 2.2(b)). For the 2D structure (e.g., $(CH_3NH_3)_2PbI_4$), each $[PbI_6]^{4-}$ octahedron is connected with four neighbours at the halide, forming a 2-D network layer that is sandwiched between two consecutive organic cation layers (see figure 2.2(c)). For the 1-D case (e.g., $(C_{10}H_{21}NH_3)_2PbI_4$), each octahedron is connected at two opposite corners with its neighbour, forming separate infinite chains (see figure 2.2(d)). Lastly, $(CH_3NH_3)_4PbI_6{\cdot}2H_2O$ manifests as a quantum dot (0D) analogue, where each $[PbI_6]^{4-}$ complex is neutralized by four $CH_3NH_3^+$ ions to form a molecule (see figure 2.2(e)) [14].

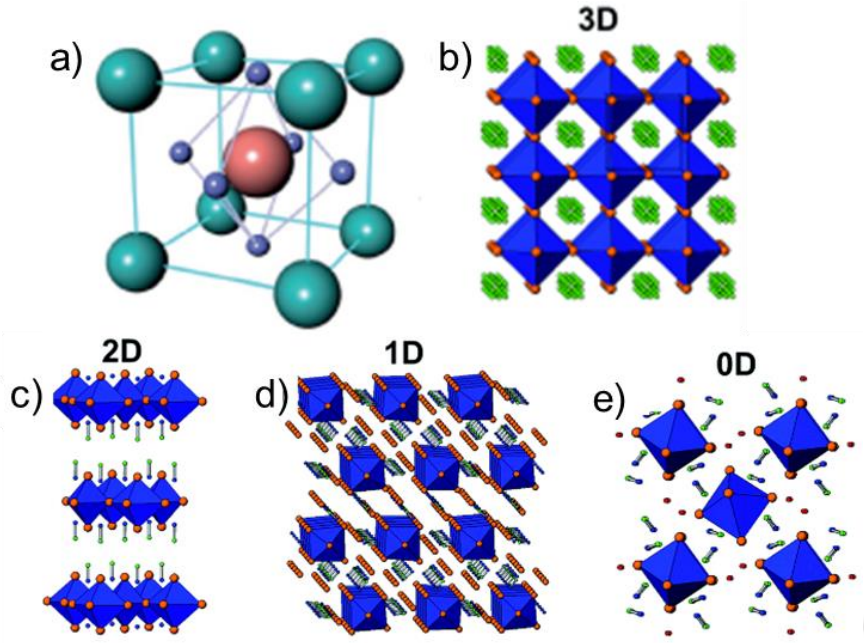


Figure 2.2: (a) A cubic cell of ABX_3 perovskite, where pink, green, and purple spheres are the A cation, B cations, and X (halide) anions, respectively; Halide perovskite crystal structures of (b) 3D ($CH_3NH_3PbI_3$) (c) 2D ($(CH_3NH_3)_2PbI_4$), (d) 1D ($(C_{10}H_{21}NH_3)_2PbI_4$), and (e) 0D ($(CH_3NH_3)_4PbI_6{\cdot}2H_2O$) HOIPs. Here, blue polyhedra and orange spheres represent BX_6 octahedra and halogens respectively [14].

3D HOIPs (e.g., $MAPbI_3$, $FAPbI_3$, $CsPbI_3$ etc.) are the earliest and have been most commonly used for memristors as well as for other optoelectronic devices [15,16]. However, these are highly environment-sensitive and degrade quickly. Attempts have been made to overcome this stability challenge by synthesizing low-dimensional or mixed-layered perovskites known as Ruddlesden-Popper (RP) [17] and Dion-Jacobson (DJ) perovskites [18], which are defined by the charge of the interlayer spacing cation. The layered perovskites, as a family, are considered natural quantum well materials where the inorganic slabs, as semiconductors, are separated by organic spacers serving as dielectric barriers. They exhibit varying degrees of quantum confinement by varying the organic spacer; accordingly, their structural and charge transport properties can be tuned. In particular, unique novel functions can be developed with HOIP-based memristors that take advantage of the remarkable photo absorption ability of this emerging material system through the synergistic coupling of photonic, electronic, and ionic processes.

2.3 Fabrication Methods of HOIP Memristors

While spin coating is the most commonly used method to fabricate HOIP memristors, thermal evaporation has also been used by a few research groups.

a) Spin Coating: It is one of the simplest laboratory-scale methods, offering precise control over the film thickness. During the early stages of HOIP device development, a two-step deposition method was employed to grow an $MAPbI_3$ film, where a PbI_2 solution in dimethylformamide (DMF) was spin-coated first, followed by the spin-coating of MAI solution in 2-propanol on top of it [19]. Subsequently, to achieve a better film coverage and to reduce the pinholes, a one-step deposition method has been developed for the later devices. However, films grown with this method had a porous or mesoporous morphology due to the slow nucleation of perovskite during the spin time. An antisolvent method was developed to overcome these issues, which reduces the solubility of perovskites and increases rapid nucleation and crystallization [20]. Even though both the one- and two-step deposition methods involve a large wastage of precursor materials, most of the HOIP memristors reported in the literature have been fabricated using them, in inert ambient. Variations between different reports include the form of precursor solutions, spinning parameters, type of antisolvent used, annealing conditions, etc.

b) Thermal Evaporation: In this method, the perovskite precursors (organic and inorganic) are heated under a high vacuum to convert them into the vapour phase and deposit on the substrate. This process can be used for all types of substrates since it does not require an annealing treatment. However, the setup is relatively expensive and complex, which limits the throughput of the production. Hwang *et al.* prepared an Au|$MAPbI_3$|Pt memristor by sequential vapour deposition using 250 nm via-holes patterned on a silicon wafer [21]. In another report, a BA_2PbBr_4 2D perovskite memristor was fabricated using a similar vapour-assisted sequential deposition technique. It was

found that higher perovskite grain sizes results in lower HRS currents, which decreases consequently, improve the ON/OFF ratio [22].

2.4 Resistive Switching in HOIP Memristors

RS in a memristor is a physical phenomenon where the resistance of the functional layer changes in response to a strong electric field. The device resistance changes from HRS to LRS on applying a positive voltage pulse higher than a threshold value. This process of transition of resistance is known as the SET or WRITE process, and the required voltage for this is known as the SET voltage (V_{SET}). On the other side, the resistance of the device can be changed from LRS to HRS (i.e., the ERASE process) by applying a reverse voltage pulse or a RESET voltage (V_{RESET}). Various mechanisms including CF formation, ion migration, charge trapping/detrapping, chemical reactivity at the perovskite|electrode interface, and lattice distortion due to the shift of A-site organic cations by an external electric field, have been proposed as the origins of the hysteresis in HOIP memristors.

2.4.1 Formation and Rupture of Conducting Filaments

Here, forming and rupturing a metal filament in the functional layer (thus, changing the device resistance) is considered as the origin of RS in HOIP memristors [23,24]. This phenomena is shown schematically in figure 2.3. When a positive bias is applied to the active metal electrode, the metal ions are partially oxidized at the perovskite|electrode interface. Metal cations thus generated will migrate through the HOIP layer towards the counter electrode, along the electric field direction, and form a conducting channel across the device. These channels act like highways to transport the electrons injected from the other electrode and, thus, the device switches to LRS. However, applying a negative bias to the active metal electrode reverses the electric field direction leading to a reverse migration of metal cations and, eventually, to the

breaking/rupturing of the CFs by Joule heating, subsequently turning the device to its HRS.

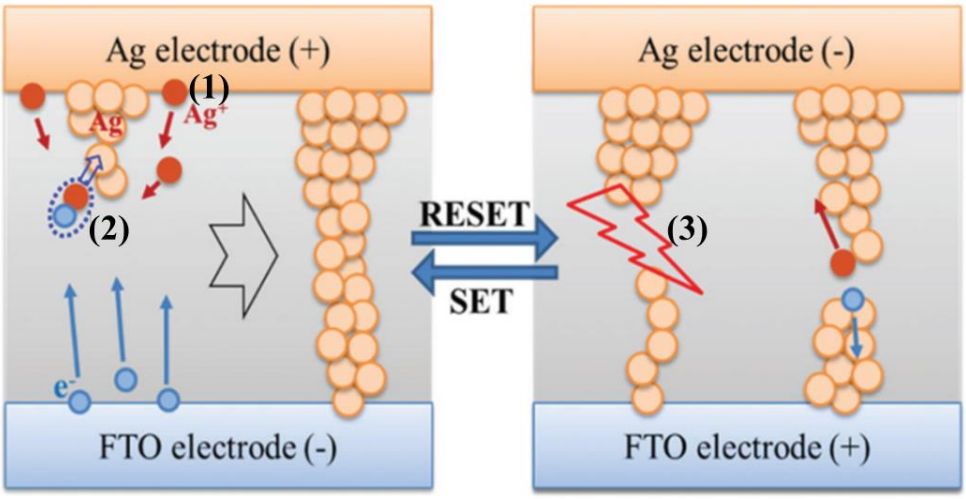


Figure 2.3: Illustration of the formation (left) and the rupture (right) of the conducting Ag filaments; (1) oxidation of the Ag electrode and migration of Ag cations under the applied bias, (2) reduction of Ag cations at the TE and Ag filament growth and (3) the rupture of Ag filaments by Joule heating [23].

2.4.2 Redistribution of Halide Ions and Vacancies or Ion Migration

It is noteworthy that HOIP thin films contain various types of defects (iodine vacancies V_I, methyl ammonium vacancies V_{MA}, and lead vacancies V_{Pb}), interstitials (MA_i, Pb_i , and I_i), and antisite substitutions (MA_I, Pb_I). Vacancy defects could be acceptor-type (V_{MA}, V_{Pb}) and donor-type (V_I), and vacancy-mediated diffusion is a common process in the ABX_3 structure [15]. The defects in the crystal lattice lead to the formation of trap states in HOIPs at the grain boundaries and/or at the interfaces. The occurrence of ion migration (or redistribution of ions) at the interface differs from that in the bulk and shows a strong influence on the electrostatic potential distribution [25]. The role of ionic defects at the interfaces is widely discussed as one of the current limiting factors in optoelectronic devices [26]. Also, surface defects have been mostly accepted as the contributing factor for current hysteresis in some HOIP devices [27].

2.4.3 Competition between CFs formed by Metal Ions and by Halide Ions/Vacancies

Some reports indicate that there will be a competition between two types of CFs – one that is formed from the active metal electrode and the other from V_Is - to be dominant in initiating RS action in HOIP memristors. Sun *et al*. investigated these mechanisms by varying the active layer thickness of FTO|$MAPbI_3$|Ag memristors [28]. When a positive bias is applied to the Ag electrode, Ag atoms are oxidized to Ag^+ ions and start migrating towards the FTO electrode, while I^- ions in $MAPbI_3$ start migrating towards the Ag electrode. In the case of a relatively thick $MAPbI_3$ layer, CFs from Ag^+ ions remain incomplete and, therefore, the switching mechanism is dominated by I^- ions and V_I migration. On the other hand, a relatively thin $MAPbI_3$ film allows the formation of CFs from both Ag^+ and I^- ions simultaneously across the device. In this case, both the CFs can contribute to the switching mechanism. However, the migration of I^- ions and vacancies continues until all the I^- ions and V_Is accumulate at the Ag and FTO electrodes respectively and switch the memristor from HRS to LRS.

2.4.4 Physicochemical Interaction at Perovskite|Electrode Interface

It has also been proposed that the migration of I^- ions and the subsequent physicochemical reaction at the $MAPbI_3$|electrode interface is the origin of RS in HOIP memristors, independent of the HOIP layer thickness [29]. According to this theory, when the bias is applied initially during switching, V_Is get accumulated at the HOIP|Ag interface to form an insulating layer, creating a high energy barrier. Because of this, charge transfer to the electrode gets impeded and the device remains in HRS. When a positive bias is applied to the Ag (active metal) electrode, I^- ions migrate towards the interface and chemically react with Ag^+ ions to form a thin AgI_x layer. Since this layer is highly conductive, it facilitates charge transfer to switch the memristor from HRS to LRS eventually. A negative bias to Ag electrode reverses the direction of I^- migration and

accumulates V_Is at HOIP|Ag interface. Therefore, the device switches back to HRS from LRS.

2.4.5 Hysteresis due to Electric Field-Driven Lattice Distortion

Ferroelectric dielectric phenomenon has been reported to be present in many oxide perovskites [30] as well as in HOIPs (particularly in $MAPbI_3$), both from theoretical [31] and experimental studies [32]. HOIPs often undergo reversible phase transitions and exhibit cubic, tetragonal, orthorhombic, trigonal, and monoclinic polymorphs depending on the tilting and rotation of the metal halide polyhedra in the lattice. Such reversible phase changes can be induced by various stimuli, including electric field, temperature, and pressure [31]. Ferroelectric materials allow easy and long diffusion of carriers along the domain boundaries or 'ferroelectric highways' generated by local dipole disorder. The applied voltage significantly influences the carrier density of these ferroelectric boundaries and the domain orientation, resulting in a hysteresis behaviour during electrical measurements [33]. The hysteretic behaviour of $MAPbI_3$ has also been attributed to the reorientation of the permanent dipoles of MA^+ on the application of an external electric field, in addition to the intrinsic resistance of the PbI_6 lattice [33].

2.5 Applications and State-of-the-Art of HOIP Memristors

2.5.1 Data Storage

HOIP memristors can potentially be useful in ultra-high storage density computing technologies. An immediate application for these devices is the resistive random-access memory (ReRAM). The first memristor based on HOIP was reported by Yoo *et al.* on a glass substrate [23]. This memristor was made up of a 2.5μm-thick layer of highly crystalline $MAPbI_{3-x}Cl_x$, sandwiched between Au and FTO electrodes, using the one-step spin coating method. Yan *et al.* demonstrated an HOIP-based memristor with

an excellent ON/OFF ratio of 10^9. The RS in the device was attributed to the formation of a single filament due to ion migration [34]. The first flexible $MAPbI_3$ memristor on a PET substrate, reported by Gu and Lee, showed V_{SET}, V_{RESET}, endurance, and retention of 0.7 V, -0.5 V, 400 cycles, and 10^4 s, respectively (see figure 2.4) [15]. Tensile and compressive stresses were applied to this device at different bending radii of up to 1.5 cm.

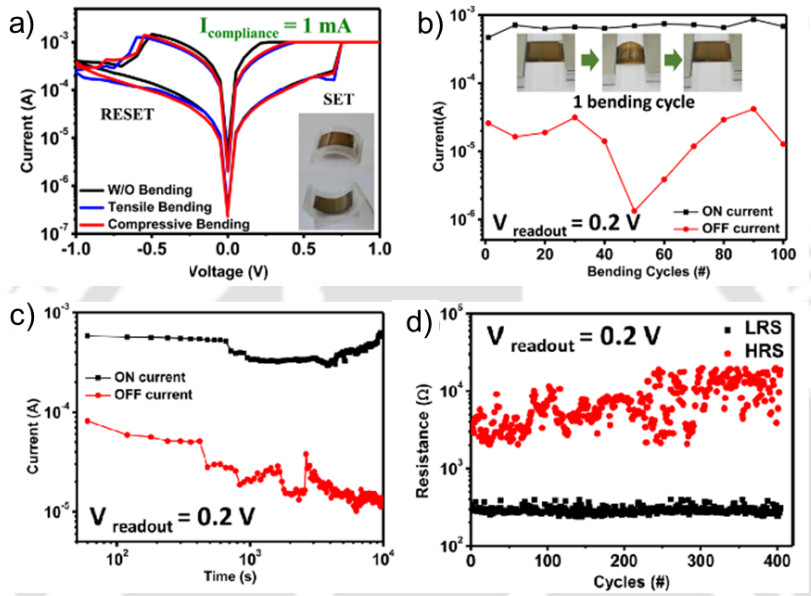


Figure 2.4: Mechanical flexibility of hybrid organic−inorganic perovskite RS memory devices, (a) I−V characteristics without and with bending stress, (b) bending stability with repetitive bending cycles, (c) retention test, and (d) endurance test of the flexible device [15].

Recently, Kim *et al*. reported a quasi-2D $Ag|(PEA)_2Cs_3Pb_4I_{13}|Pt$ memristor with a high ON/OFF ratio (>10^8), which was two orders of magnitude larger than that of its pure 3D counterpart ($CsPbI_3$) [35]. Beyond the polycrystalline films, Zhao *et al*. reported a memristor with one-dimensional (1D) $MAPbI_3$ nanofibres [36]. However, its RS properties are inferior to those of its 3D and 2D counterparts. Yang *et al*. demonstrated a memristor using $MAPbBr_3$ quantum dots (PeQDs) with the device structure as ITO|PMMA|PeQDs:PMMA|PMMA|Ag [37]. Furthermore, a multilevel RS for up to 1000 bending cycles was obtained, with the levels distinguished by changing the compliance current (I_{CC}). By controlling the I_{CC}, multilevel conductance states have been achieved in an inorganic perovskite flexible memristor ($Al|RbPbBr_3|ITO|PET$), which could be

beneficial for high-density data storage in flexible electronic applications [35]. Table 2.1 compares the RS parameters of memristors prepared with various perovskite compositions and device configurations.

Table 2.1: Resistive switching parameter comparison between various HOIP-based memristors.

Device Structure	V_{SET}/ V_{RESET} **(V)**	**ON/OFF Ratio**	**Endurance (no. of cycles)**	**Retention (s)**	I_{RESET} **(A)**	**Ref.**
Au|$MAPbI_{3-x}Cl_x$|FTO	0.86/-0.65	~3	100	10^4	$4.5x10^{-3}$	[24]
ITO|PEDOT:PSS|$MAPbI_3$|Cu	-0.6/2	10^4	3000	$3x10^4$	-	[38]
FTO|$MAPbI_{3-x}Cl_x$|Al	1.1/-1.65	$1.9x10^9$	160	$2x10^3$	$6x10^{-2}$	[34]
Au|$MAPbI_3$|ITO|PET	0.7/-0.5	~10	400	10^4	$1.2x10^{-3}$	[15]
Ag|$MAPbI_3$|Pt	0.13/-0.15	$1.12x10^6$	350	$1.1x10^4$	$3x10^{-3}$	[39]
ITO|PMMA|$MAPbI_3$|PMMA|Ag	1.2/-3.3	10^3	-	120	$4x10^{-2}$	[40]
Ag|$MAPbI_{3-x}Cl_x$|FTO	1.5/-0.8	~40	1000	$4x10^4$	$8x10^{-4}$	[23]
Au|$MAPbI_{3-x}Br_x$|ITO	1.9/-0.56	10^2	30	$2x10^4$	$1.5x10^{-3}$	[41]
PET|ITO|PMMA|PeQDs:PMMA| PMMA|Ag	1/-1.2	10^3	-	$4x10^3$	$2x10^{-4}$	[37]
ITO|$CH_3NH_3PbI_3$|MoO_3|Ag	0.25/-1.25	10^2	-	10^3	$9x10^{-2}$	[42]
Au|$MAPbI_3$|Pt	1/-1	10^3	500	10^5	$3x10^{-6}$	[21]
Au|$MAPbI_3$|Au	0.32/ -0.13	10^7	1000	44	$5x10^{-5}$	[6]
Ag/$CH_3NH_3PbI_3$/Pt/SiO_2/Si	0.18/ −0.1	10^6	1338	$2.98x10^4$	$5x10^{-4}$	[43]
Ag|BA_2PbI_4|Pt|Ti|SiO_2|Si	0.5/-0.6	10^7	250	10^3	$5x10^{-3}$	[44]
ITO/$MAPbI_3$/Au	0.7/-0.6	20	500	10^4	$9x10^{-2}$	[45]
Graphene|$(PEA)_2PbBr_4$|Au	2.8/-1	100	100	10^3	$3x10^{-12}$	[46]
PET|ITO|$MA_2PbI_2(SCN)_2$|Al (Two different write-once-read-many (WORM) type of RSs)	−1.59	10^3	-	10^4	-	[47]
	−3.20	10^7	-	10^4	-	
Au|$CH_3NH_3BiI_3$|ITO	1.6/-0.6	100	300	10^4	$2x10^{-3}$	[48]
FTO|ZuO|$(C_4H_9NH_3)_2PbBr_4$|NiO	1.2/-2	<10	-	10^3	$5x10^{-2}$	[49]
Ag|$MAPbI_3$|FTO	0.8/-0.4	10^6	1000	10^5	10^{-3}	[28]
FTO|$CH_3NH_3PbI_3$-Oelic Acid|W	3.1/-1.1	100	100	-	10^{-2}	[50]
Ag|$MAPbI_3$ (nano fiber)|Ag	0.42/−0.42	~7	75	478	-	[36]
ITO|PEDOT:PSS|$MAPbBr_3$|Al	-0.2/~3	$3.6x10^6$	120	10^4	10^{-1}	[22]
Ag|$FA_{0.83}MA_{0.17}Pb(I_{0.82}Br_{0.18})_3$|FTO	0.65/-0.5	>10	40	$5.2x10^3$	10^{-4}	[51]
Si|Ti|Pt|$MAPbI_3$|PEA_2PbI_4| PMMA|Ag	0.18/-0.14	10^6	2700	10^4	10^{-3}	[52]
ITO|$(FA_{0.75}MA_{0.25})_{1-x}Cs_xPbI_3$| PMMA|Al	0.4/-2.5	10^4	130	10^4	$9x10^{-2}$	[53]
Ag|$(PEA)_2Cs_3Pb_4I_{13}$|Pt|SiO_2|Si	0.40/-0.10	10^9	230	$2x10^3$	10^{-2}	[35]
Al|$CH_3NH_3PbI_3$|FTO	1.5/−1.4	~40	1500	-	$2.8x10^{-2}$	[54]

2.5.2 Artificial Synapse

A synapse acts as a bridge to transmit signals between two neurons. The synaptic weight can be altered by an external stimulant and is quantitatively represented by the change in conductivity of the artificial synapse. Therefore, controlling the conductivity by adjusting the form of the synaptic plasticity is a goal of an artificial synapse [55]. Considering their superior electrical properties, low power consumption, low cost, and easy high-density fabrication processes, HOIP memristors are most suitable for realizing a two-terminal artificial synapse. The first HOIP-based artificial synapse (Au|$MAPbI_3$|PEDOT:PSS|ITO) was demonstrated by Huang and Xiao in 2016, where ITO BE and Au TE represented the pre- and post-synaptic neurons, respectively (see figure 2.5) [56]. Several synaptic functions of biological synapses that we have mentioned in section 1.4 of chapter 1 (e.g., STDP, SRDP, STP, LTP, and learning and forgetting behaviour, etc.) have been demonstrated using this structure. In another work, Xu *et al*. showed that, by precise adjustment of the conductivity of Al|$MAPbBr_3$|BCCP|ITO memristor (here, BCCP is a buffer-capped conducting polymer), the energy consumption of the device (20 fJ per event) was as low as that in a biological synapse [57]. Several other HOIPs, low-dimensional layered perovskites, and all-inorganic perovskites were also employed to demonstrate synaptic behaviour for neuromorphic computing [58-61]. Showing the promise of applicability in the field of flexible electronics, a lead-free two-dimensional (2D) perovskite $(PEA)_2SnI_4$ memristor was demonstrated on flexible polyethylene terephthalate (PET) substrates. Reduced graphene oxide|PEDOT:PSS electrodes were used in this case [62].

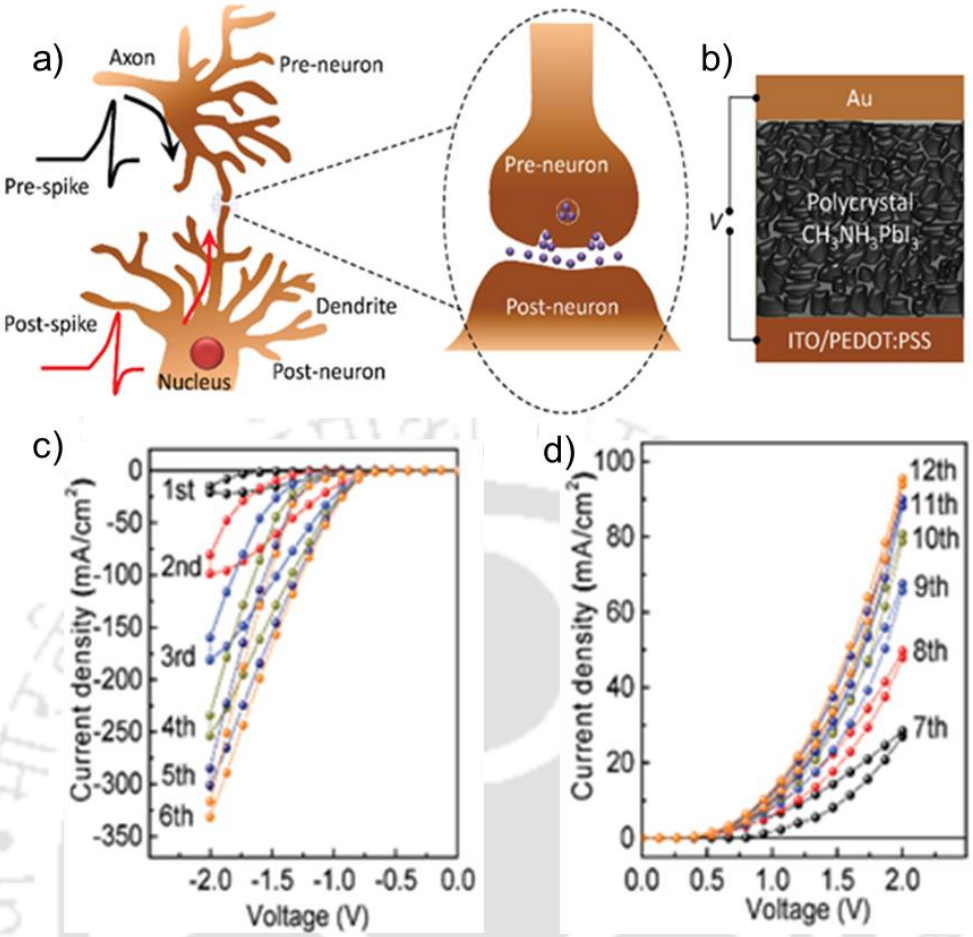
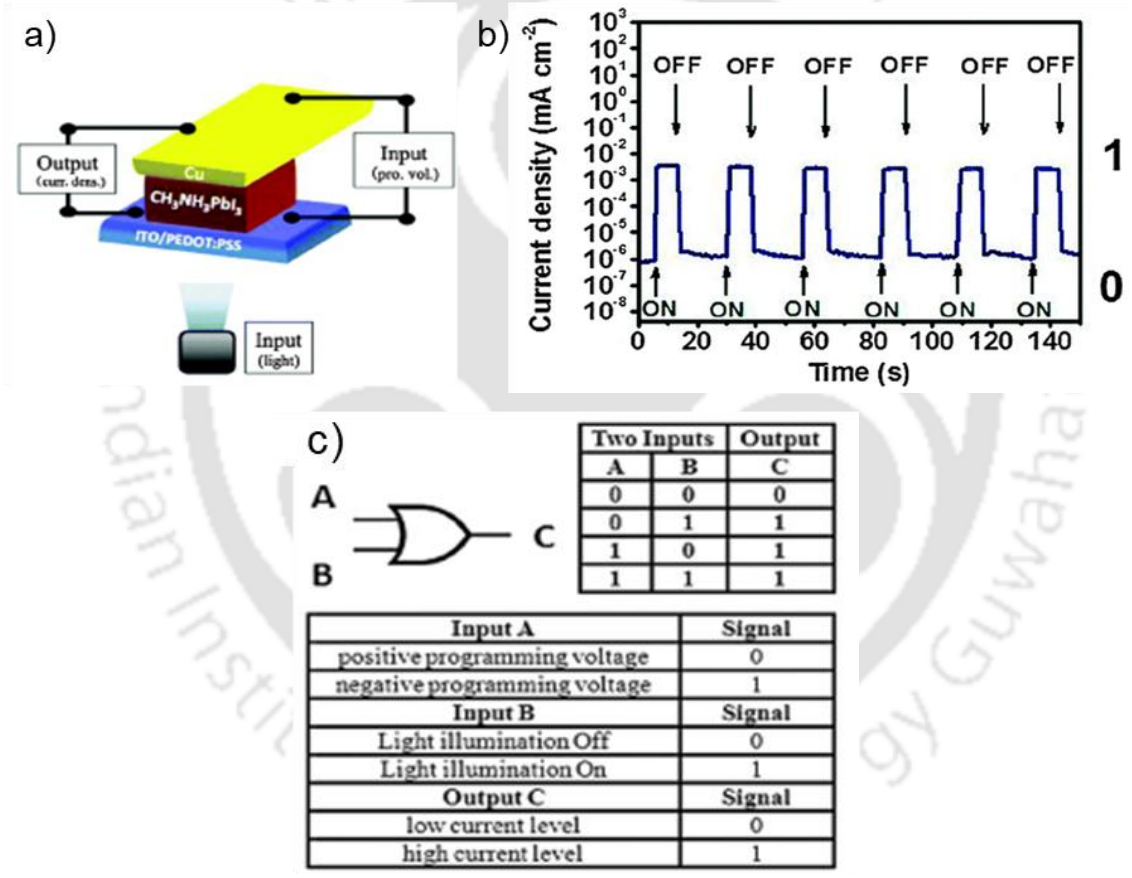


Figure 2.5: a) Schematic of a biological synapse. b) Schematic of the HOIP synaptic device structure. c, d) Memristive characteristics of the device under the positive and negative biases at a scanning rate of 0.1 Vs^{-1} [56].

2.5.3 Photonic and Logic Applications

The light sensitivity of HOIPs has expanded their importance for various photonic and energy harvesting applications including photovoltaics, light-controlled diodes and transistors, logic gates, and photonic computing. Huang *et al*. reported an HOIP memristor in vertical and lateral cell configurations where the direction of photocurrent was switched repeatedly by applying an electric field of less than 1 V/μm [63]. This memristor can simultaneously read the signals from both electrical and light pulses. An all-inorganic photonic ReRAM-based on $CsPbBr_3$ quantum dots was used to realize light-sensitive artificial synapses [64]. The ON/OFF ratio of this device could be enhanced significantly by illuminating the device. An HOIP memristor

(ITO|PEDOT:PSS|$MAPbI_3$|Cu) was reported in 2015 by Lin *et al*, where the two distinct photo-responsive resistance states allow the memristor to function as a logic OR gate (see figure 2.6(a)) [38]. As shown in figure 2.6(b), by turning 'ON' and 'OFF' the light illumination, device current can be switched with an ON/OFF ratio of ~10^4. Out of the two inputs of the designed logic gate, input A was the programming voltage, and input B was the light illumination. The corresponding state diagram of the logic OR device, along with the gate symbol are shown in figure 2.6(c).



Two Inputs		Output
A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

Input A	Signal
positive programming voltage	0
negative programming voltage	1
Input B	**Signal**
Light illumination Off	0
Light illumination On	1
Output C	**Signal**
low current level	0
high current level	1

Figure 2.6: (a) Schematic diagram of the light illumination induced logic OR gate using HOIP memristor, (b) $J-t$ response of the device under light ON/OFF switching irradiation, with a V_{READ} of 10 mV, and (c) State diagram of the logic OR device with two types of input sources and one output terminal. For the electrical field source (input A), signals ''1'' and ''0'' represent the negative and positive fields, respectively. For the light illumination source (input B), signals ''0'' and ''1'' represent light OFF and light ON states, respectively [38].

A physical unclonable function (PUF) is a security building block that exploits inherent randomness present in the device during manufacturing to form secret keys on

the fly [65]. Considered as a unique 'fingerprint' for a particular device, it can be useful in a variety of applications such as anti-counterfeiting, identification, authentication, and key generation. As the memristor parameters possess inherent device-to-device and cycle-to-cycle stochasticity, it is an obvious choice for the implementation of PUFs. John *et al.* recently reported a printable and flexible hybrid perovskite memristor-based PUF [66]. Here, a memristor with the structure of PET|ITO|PEDOT:PSS|PrPyr[PbI_3]|PMMA|Ag, included 1D propyl pyridinium lead iodide (PrPyr[PbI_3]) as the active layer. The HRS state of the memristor was considered as the source of entropy or randomness to secure key generation and device authentication. This work demonstrated both strong and weak PUFs that allow in-action modification of the security information, opening a new paradigm in the field of digital cyber security.

2.6 Memristor Modelling

To cater to the wide range of memristor materials, device structures, and their working mechanisms, various analytical models have been proposed over the years. These include material-level atomistic models, semiconductor physics-based device models, and compact models for large-scale circuit implementation [67]. Figure 2.7 shows a schematic of these modelling approaches based on their scale, physical details, capability, computational cost, and significance in terms of applicability to the existing technology. The most elementary of these is the atomistic level modelling (a few nm^3) based on density function theory (DFT) simulations. The physics-based device models use Kinetic Monte Carlo (KMC) and finite element method (FEM) simulations, which are carried out at a scale of a few tens of nm^3. The compact models utilize some simplified set of equations inferred from the device models and allow circuit scale (a few hundreds of nm^3) simulation of memristor characteristics.

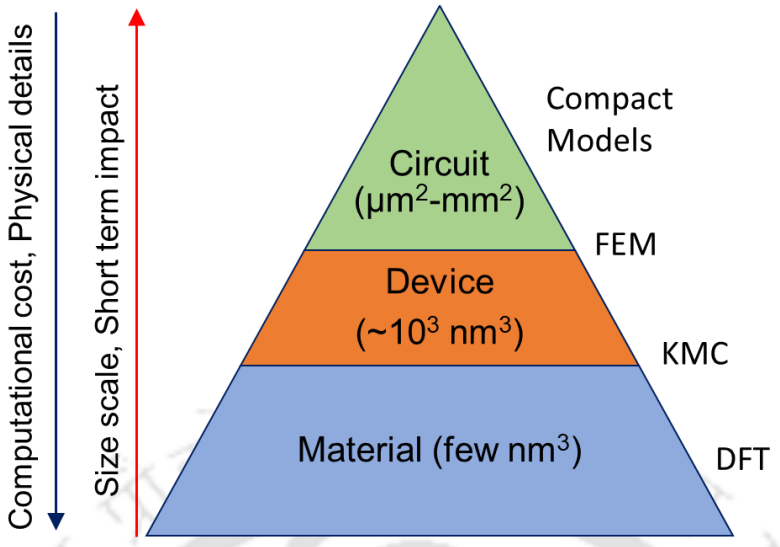


Figure 2.7: Schematic representation of physical modelling approaches for RS memory. These models are broadly classified into three groups, based on scale, physical details and computational cost. Material models (in blue) are based on atomistic DFT simulations, device models (in orange) are based on FEM or KMC simulations, and compact models (in green) are simplified device models for circuit level simulation [67].

The following section briefly reviews the progress in memristor modelling approaches. We restrict our discussion to the modelling attempts that can be described by simple mathematical expressions or be represented by an equivalent circuit. These models can be incorporated as a compact model for circuit simulation using different simulation tools such as SPICE, Comsol Multiphysics etc.

2.6.1 Dopant-Drift Model

Linear Ion Drift Model [1] is the first and simplest model based on the TiO_2 memristor from HP labs. The oxygen vacancies originating from the oxygen-deficient titanium dioxide layer (TiO_{2-x}), acting as donors of electrons, are assumed to drift linearly in a uniform field. The device resistance is dependent on the ratio between the value of the dynamic state variable *w(t)*, representing the thickness of the non-stoichiometric TiO_{2-x} layer, and the device thickness *D* (see figure 2.8(a)). Considering Ohmic electronic conduction, linear drift in a uniform field, and average ion mobility (μ_v), the model is represented as

$$v(t) = \left(R_{ON}\frac{w(t)}{D} + R_{OFF}\left(1 - \frac{w(t)}{D}\right)\right) i(t) \quad (2.1)$$

$$\frac{dw(t)}{dt} = \mu_v \frac{R_{ON}}{D} i(t) \quad (2.2)$$

Here, $v(t)$ is the voltage across the memristor, $i(t)$ is the current through the memristor, R_{ON} and R_{OFF} are the device resistances when $D = 0$ and $D = L$, respectively (see figures 2.8(b) and (c)).

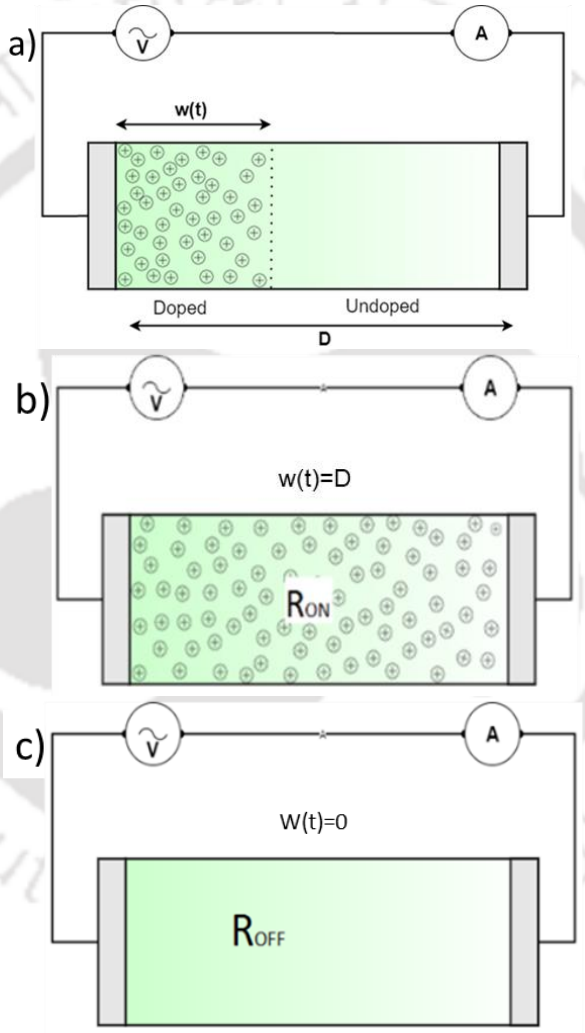


Figure 2.8: (a) Simplified equivalent model considered by linear ion drift model. Here, D represents the total thickness of the switching layer and $w(t)$ represents the length of the doped region. (b, c) The two boundary cases, when (b) $w(t) = D$ (device resistance = R_{ON}), and (c) $w(t) = 0$ (device resistance = R_{OFF}) [1].

This model is very inaccurate considering the highly non-linear nature of the motion of ions in practical devices, with a significant reduction of their drift velocity at the boundary regions. To address the non-linearity at the boundaries, various window

functions ($f(w)$) have been introduced [68-70]. The window functions are different mathematical expressions which, when multiplied with the derivative of state variable (i.e., equation (2.2)), make the change of state variable non-linear at the boundary regions. Table 2.2 compares some of the different window functions. Although window functions address the issue of non-linearity at the boundary, they cannot substitute for non-linear drift. In the work of Lehtonen *et al*., the state variable derivative has been modelled as a non-linear function of the voltage [71]. The state equation is given by equation (2.3), where α and m are experimental fitting parameters, and *w(t)* is normalized between [0,1].

$$\frac{dw(t)}{dt} = \alpha v^m(t) f(w) \tag{2.3}$$

Table 2.2: Comparison of various window functions, their mathematical representation, symmetry, capability of resolving boundary issues, addressing non-linear drift, and scalability.

	Joglekar [68]	Biolek [69]	Prodromakis [70]	Kvatinsky [72]
$f(w)$	$1-\left(\frac{2w}{D}-1\right)^{2p}$	$1-\left(\frac{w}{D}-\text{stp}(-i)\right)^{2p}$	$k\left(1-\left[\left(\frac{w}{D}-0.5\right)^2+0.75\right]^p\right)$	$\exp\left[-\exp\left(\frac{w-w_{on,off}}{w_c}\right)\right]$
Symmetric	Yes	Yes	Yes	Not necessarily
Resolve Boundary Conditions	No	Yes	Yes	Yes
Impose non-linear drift	Partially	Partially	Partially	Yes
Scalable	No	No	Yes	No

2.6.2 Memristor–Rectifier Model

Yang *et al*. proposed a parallel combination of a memristor and a rectifier to realize the hysteretic I-V characteristics [73]. This model assumes asymmetric switching where, the I-V curve follows a tunnelling process during the ON state, and the behaviour of a PN junction during the OFF state. This model is given by the following phenomenological equation,

$$i(t) = w^n(t)\beta \sinh\big(\alpha v(t)\big) + \chi[\exp(\Upsilon v(t) - 1] \quad (2.4)$$

Here α, β, Υ, χ, and n are experimental fitting parameters, and $w(t)$ is the normalized state variable between [0,1]. The first term on the right-hand side (RHS) of the equation (2.4) is an approximated representation of a flux-controlled memristor taken from the tunnelling barrier model. The second term on the RHS represents the rectifier when the memristor is switched OFF. The authors demonstrated that the potential barrier height modifications at the Pt|TiO_2 interfaces due to the drift of positively charged oxygen vacancies lead to ohmic-type or rectifying-type characteristics and, subsequently, the device resistance switches (see figure 2.9).

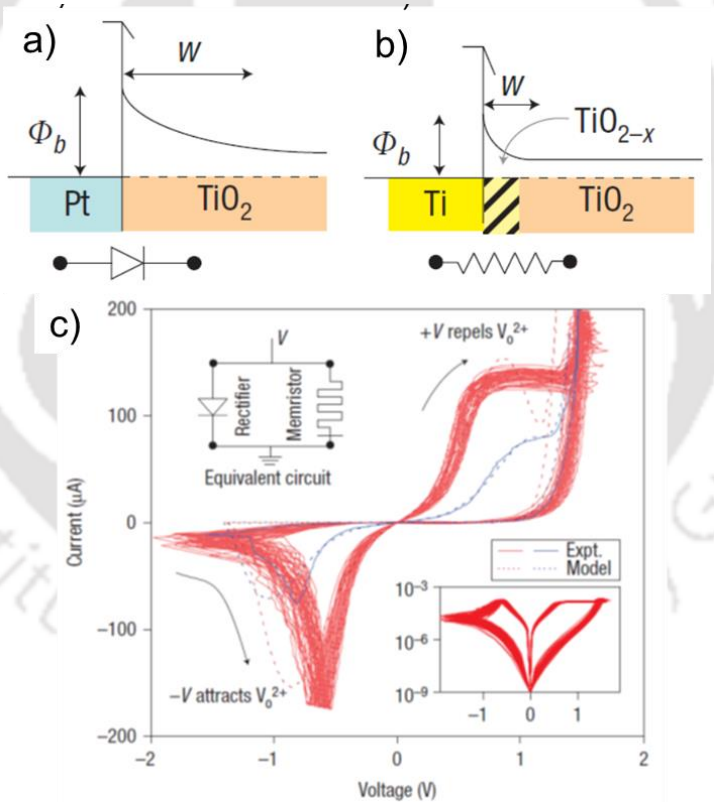


Figure 2.9: (a) Schottky junction is formed at the Pt|TiO_2 interface (noted by a rectifier) under low oxygen vacancy concentration. (b) With a higher vacancy concentration in Ti, the Ti|Pt Schottky barrier is converted into ohmic (denoted by a resistor). Here ϕ_b and W represent the barrier height and depletion layer width, respectively. (c) Experimental (solid line) and simulated (dotted line) I-V curves for repeated voltage sweep. [73]

Chang *et al*. proposed a modified memristor-rectifier model based on WO_x memristors, where non-linearity was introduced into the state variable function [74]. The

model considered the conductive region area as the state variable, and a hyperbolic sine function was used to represent it, reflecting the exponential dependence of the velocity of the vacancy front on the applied field. In another work, a meta-stable switch (MSS) model has been presented recently by Molter *et al*., which considered the memristor as a parallel combination of a memory-dependent current element (I_m) and a Schottky diode (I_s) [75]. The overall memristor current is given by,

$$I = \phi I_m(v,t) + (1-\phi) I_s(v) \tag{2.5}$$

Here, ϕ lies in between [0,1] indicating whether the current is Schottky component dominant ($\phi = 0$) or memory element dominant ($\phi = 1$). The Schottky component results from the Schottky barrier at the metal-semiconductor junction. The memory-dependent current element is modelled by considering the memristor as a collection of conducting channels which can switch between two states probabilistically, as a function of applied bias and temperature. The MSS model was demonstrated to accurately fit the hysteresis behaviour of the W-Ag-chalcogenide memristor, as well as the stochastic nature of the device [76].

2.6.3 Tunnelling Barrier Model

Pickett *et al*. developed a memristor model based on the Simmons tunnel barrier for a rectangular potential barrier with an image force effect at the top metal-insulator-metal junction [77]. A conducting channel is formed as a result of the electroforming step, along with a remnant tunnel gap between the conducting channel and the opposite electrode. This tunnel gap can be modulated by applying a voltage and inducing the motion of ionized defects. As shown in figure 2.10, the model assumes that the memristor is a series connection of a resistor (R_s) with an electron tunnel barrier, and the width of the tunnel barrier is considered as the state variable.

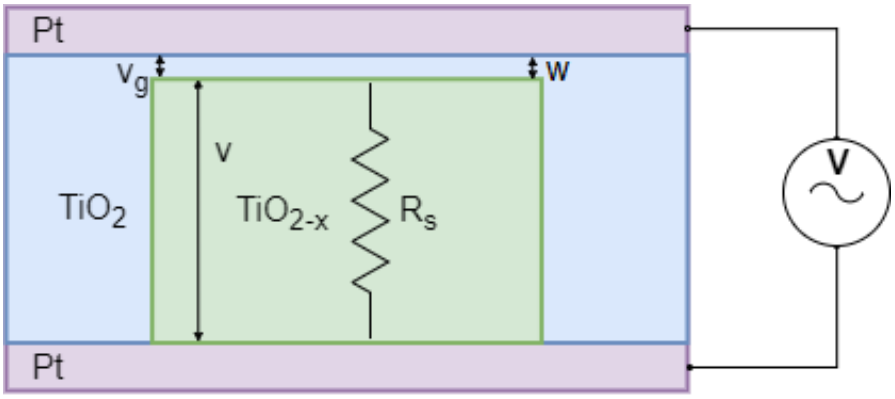


Figure 2.10: Schematic diagram of a TiO_2 layer sandwiched between two platinum electrodes. After an electroforming process, oxygen vacancies are formed, resulting in a highly conductive channel (TiO_{2-X}) that shunts most of the oxide film except for a narrow tunnel barrier W [83].

However, the mathematical expressions in this model are considerably complex, with no implicit relation between voltage and current. A simplified model based on the Simmons tunnel barrier model was proposed by Kvatinsky *et al*., namely 'threshold adaptive memristor model (abbreviated as TEAM by the authors)' [72]. According to this model, there is no change in the state variable below a certain threshold value, and the state variable can be modelled as the product of two functions, one of which depends only on the state variable and the other on the current. Yakopcic *et al*. proposed another simplified tunnelling-based model that assumes a voltage threshold and an implicit memristance [78]. It considers two types of electronic conduction represented by two different sine hyperbolic functions and controlled by the state variable 'x' (see equation (2.6)). In their subsequent work on the same model, these two electronic conductions were developed as exponential conduction during HRS and linear conduction during LRS [79]. The rate of change of the state variable, as shown in equation (2.7), depends on the product of composite functions $g(v(t))$ and $f(x(t))$, η is the direction of voltage sweep and a_1, a_2, and b are the fitting parameters.

$$I(t) = \begin{cases} a_1 \sinh(bv(t))\, x(t) \\ a_2 \sinh(bv(t))\, x(t) \end{cases} \tag{2.6}$$

$$\frac{dx}{dt} = \eta g(v(t)) f(x(t)) \tag{2.7}$$

2.6.4 SPICE Modelling

To incorporate memristors in the form of high-density arrays and integrate them into the circuit design process, the available analytical models should be suitable for implementation in CAD environments, such as SPICE. Several attempts were made to realize the linear ion drift model by HP labs [71,80,81] in SPICE. Although some of these simulations consider non-linear ion drift by using window functions, these models are based on simple Ohmic transmission, and no threshold for resistive programming is considered. In the report by Abdulla *et al*., the SPICE model considers tunnelling through similar electrodes (with equal work function) that gives rise to a rectangular tunnel barrier [82]. As shown in figure 2.11(a), two different current-controlled sources, G_{off} and $G_{on,}$ are used to model the state derivative equation of the Simmons tunnel barrier model. The change of state variable, i.e., the tunnelling width, was modelled by the voltage across the capacitor. However, using this model, the ON state current was observed to be 20% more than that from experimental results of TiO_2 memristor for a certain voltage. Owing to the complicated equations, the model leads to poor computational efficiency. The TEAM model can be described in a SPICE micromodel, as shown in figure 2.11(b), where the internal state variable is represented by the voltage across the capacitor *C*, and the bounds of the state variable are enforced by diodes D1 and D2. Compared to the Simmons tunnel barrier model, the simplified model equations boost the simulation time by 47.5% and are highly accurate, with a mean error of 0.2% [72]. To incorporate the Yakopcic model equations in SPICE, a simple subcircuit was designed, as shown in figure 2.11(c), where the current source G_m gives the memristor current [71]. A capacitor was used to obtain the value of x from i_{Gx}, which equals dx/dt. The validity of the model was tested over a wide range of memristive systems such as TiO_2, Si, Ag, chalcogenide-based devices, as well as with spintronic and phase change memories [79].

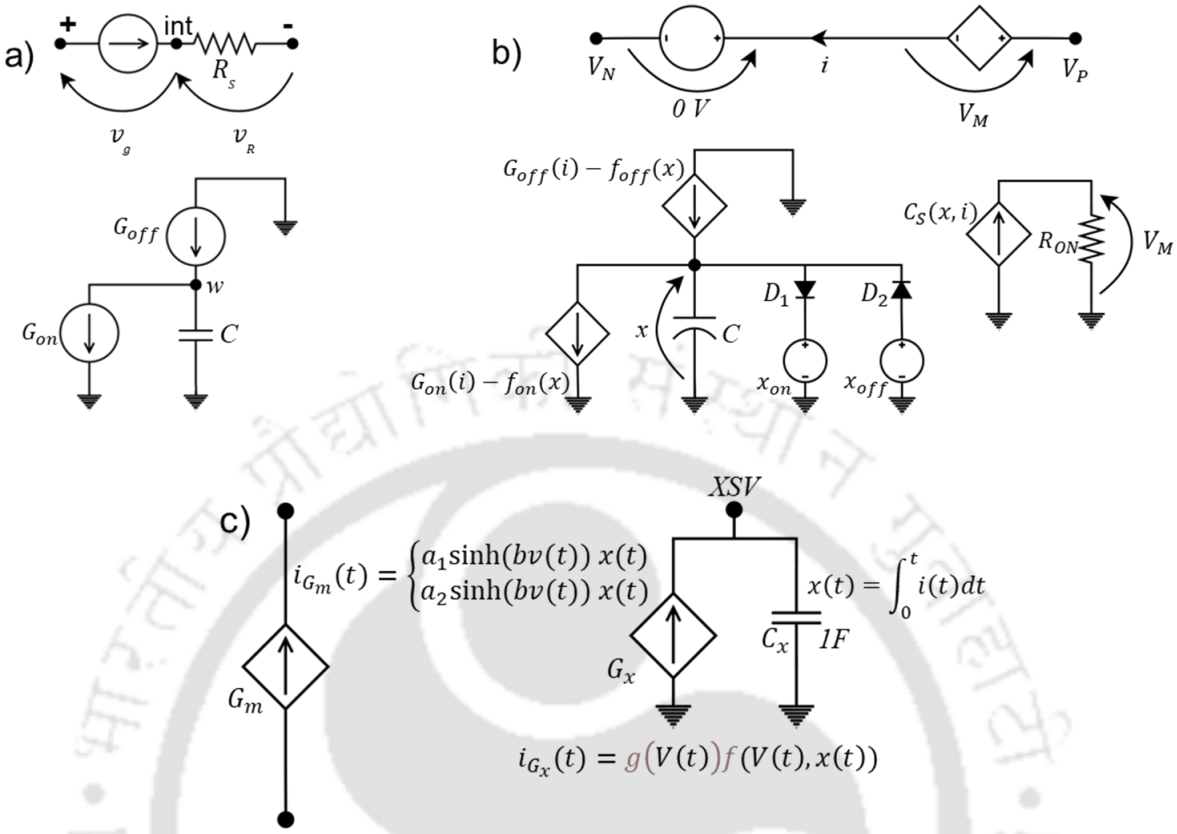


Figure 2.11: (a) SPICE subcircuit models with a voltage-dependent current source in series with a fixed resistance; the barrier width (w) is modelled as the voltage across the capacitor, dependent current sources G_{off} and G_{on} [82], (b) SPICE micromodel for the TEAM model, x is the voltage across the capacitor and D1 and D2 constrain the bounds of the state variable [72], and, (c) the simple SPICE subcircuit for Yakopcic model [78].

Several other SPICE models were proposed over the years to simulate memristive action, which were, more or less, fast and stable within specific ranges of the parameters [83,84]. Table 2.3 presents a qualitative comparison of some of the models we discussed in the previous sections. The comparison parameters include the state variable and its range, memristor control mechanism, flexibility to fit different types of memristive systems (i.e., whether generic or not), accuracy while fitting to the matching memristive system, threshold switching capability, capability to operate at high frequencies, and model complexity.

Table 2.3: Comparison of different memristor models and their properties

Model	Linear ion drift [15]	Non-linear ion drift [71]	Schottky barrier model [73]	MSS model [75]	Simmons tunnel barrier model [77]	TEAM model [72]	Yakopcic model [79]
State variable	$0 \leq w \leq D$ Doped region physical width	$0 \leq w \leq 1$ Doped region normalized width	$0 \leq w \leq 1$ Schottky barrier length	$0 \leq \phi \leq 1$ No physical explanation	$a_{off} \leq x \leq a_{on}$ Undoped region width	$x_{off} \leq x \leq x_{on}$ Undoped region width	$0 \leq x \leq 1$ No physical explanation
Control mechanism	Current Controlled	Voltage Controlled	Voltage Controlled	Voltage Controlled	Current Controlled	Current Controlled	Voltage Controlled
Accuracy of fit to the specified memristor	Lowest	Low	Moderate	High	High	Moderate	High
Generic	No	No	No	Yes	No	Yes	Yes
Threshold exists	No	No	No	No	Practically yes	Yes	Yes
Complexity	Low	Low	Low	High	High	Moderate	Moderate

2.7 Analytical Modelling of HOIP Memristors

Although significant experimental research has been carried out on HOIP memristors, only a few attempts were made to develop an analytical model to incorporate these devices as crossbar arrays and in other circuits. Yan *et al*. studied the memristive property in the I-V characteristics of perovskite solar cell (PSC) in light of the linear ion drift model and perovskite equivalent circuit model [85]. This model can address the hysteresis behaviour in PSC and is suitable to study the origin of memristive action in HOIPs. However, it cannot account for the typical non-linear and threshold switching in perovskite memristors. In another work, by Ren *et al.*, an analytical model was proposed to account for the I-V characteristics of a $MAPbI_3$-based memristor [86]. The SET and RESET processes in the device were modelled by the evolution of the length and radius of the CF, driven by electrical and thermal forces (see figure 2.12(a)). The time evolution of CF gap length (g) was expressed (see equation (2.8)) by combining carrier drift and Fick diffusion equations, whereas the time evolution of CF radius (r) was expressed (see equation (2.9)) by combining Fick diffusion and Soret diffusion equations.

$$\frac{dg}{dt} = D\alpha_1 e^{-\frac{\beta_1}{0.5(L-g)}} - v \tag{2.8}$$

$$\frac{dr}{dt} = D\left(\alpha_2 e^{-\frac{\beta_2}{r-r_o}} - S_{soret}\alpha_3 e^{-\frac{\beta_3}{r-r_o}}\right) \tag{2.9}$$

Here, D is the diffusivity coefficient, L is the thickness of perovskite film, v is the drift velocity, r_o is the constant radius of the CF after electroforming, S_{soret} is the Soret diffusion coefficient, α_1, α_2, α_3, β_1, β_2, and β_3 are fitting parameters. By solving these differential equations numerically, I-V characteristics of the $MAPbI_3$ memristor could be simulated accurately (see figure 2.12(b)). However, due to the deterministic nature of the model, it cannot address the stochastic characteristics of the HOIP memristor. In addition, the model cannot fit the characteristics of the devices with threshold switching behaviour.

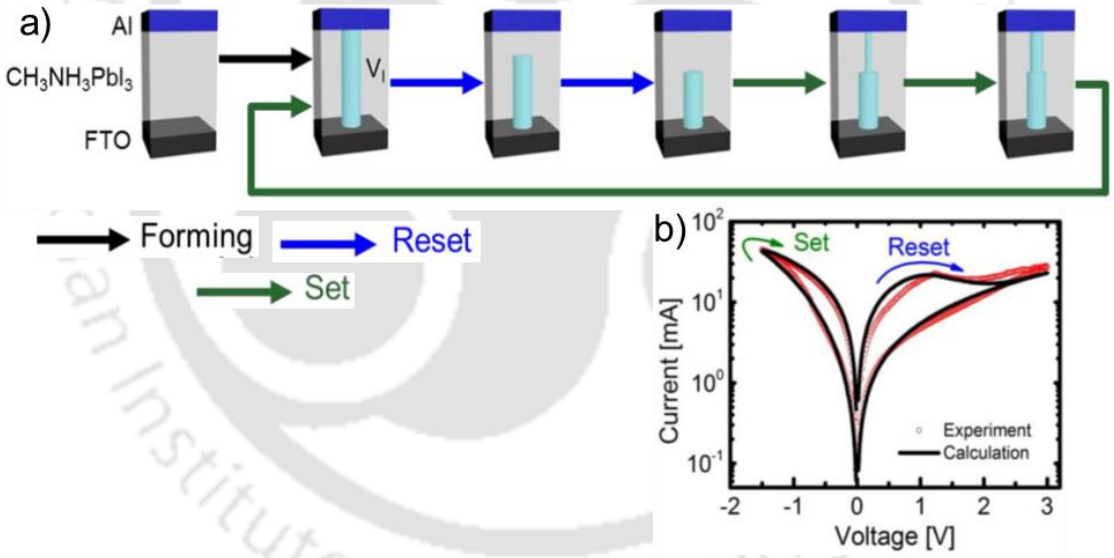


Figure 2.12: a) Schematic illustration of RS modelling in Al|$CH_3NH_3PbI_3$|FTO memristor, including CF evolution during forming, RESET and SET processes. (b) Measured and calculated I–V characteristics of the perovskite memory device, evidencing SET and RESET transitions for negative and positive voltages, respectively [86].

2.8 Summary

In this chapter, major advances in HOIP-based memristors have been discussed, including active materials used for their fabrication and their structures from 3D to 0D configurations. Several RS mechanisms proposed for these memristors have been explained. The state-of-the-art of these memristors as data storage devices, artificial

synapses, light-induced RS devices, and logic gates, have been comprehensively reviewed. It was observed that the $MAPbI_3$ has been the most commonly used HOIP memristor material, along with a few electrochemically active electrodes such as Ag, Cu, etc. for non-volatile memories and for artificial synapses. However, a variety of resistive switching characteristics have been reported from the same material, which basically resulted from different film morphologies, device structures, and characterization methods. Importantly, a standard method for forming or switching characteristics and for the selection of suitable range of measurement parameters such as scan rate (SR), I_{CC}, etc. is not available.

Several analytical and circuit equivalent models have been reported, which attempt to mimic the memristor characteristics. From a comparative review of these modelling approaches, it was understood that KMC and FEM-based device models are most accurate, considering the physics of memristors. However, they have high computational complexity and cost, and do not address the stochastic nature of the memristors. On the other hand, SPICE-based compact models are simple, computationally more efficient, and applicable to high-density crossbar arrays and other circuits consisting of memristors. Out of different SPICE models, the Yakopcic model offers great flexibility to fit the characteristics of a wide range of memristive systems. As presented in one of the later chapters, we have developed a modified Yakopcic SPICE simulation model that fits our fabricated HOIP memristor data.

Based on this review, we began with commercial memristor characterization to understand the effect of measurement procedure on switching parameters. Then we used $MAPbI_3$ as the functional material, ITO as the BE, and Ag as the TE to fabricate of our memristors. Using this simple structure, the characterization methods were optimized, and studies on their effects on various device parameters are presented in the subsequent

chapters of this thesis. These findings can be extended to any other similar materials based on the specific requirement and applications. For example, to explore a HOIP material with better stability, we have tested BA_2PbI_4 memristors using a similar device architecture and characterization methods, and these are discussed in the penultimate chapter of this thesis.

2.9 References

[1] D. B. Strukov *et al.*, "The missing memristor found," Nature, vol. 453, no. 7191, pp. 80–83, 2008.

[2] J. Yao *et al.*, "Highly transparent nonvolatile resistive memory devices from silicon oxide and graphene," Nature Communications, vol. 3, no. 1, p. 1101, 2012.

[3] N. Gergel-Hackett *et al.*, "A Flexible Solution-Processed Memristor," IEEE Electron Device Letters, vol. 30, no. 7, pp. 706–708, 2009.

[4] H.-P. Cui *et al.*, "Bending effect on the resistive switching behavior of a NiO/TiO_2 p-n heterojunction," RSC Advances, vol. 8, no. 35, pp. 19861–19867, 2018.

[5] X. Wu *et al.*, "Thinnest nonvolatile memory based on monolayer h-BN," Advanced Materials, vol. 31, no. 15, p. e1806790, 2019.

[6] M. Wang *et al.*, "Robust memristors based on layered two-dimensional materials," Nature Electronics, vol. 1, no. 2, pp. 130–136, 2018.

[7] M. M. Rehman *et al.*, "Resistive switching in all-printed, flexible and hybrid MoS_2-PVA nanocomposite based memristive device fabricated by reverse offset," Scientific Reports, vol. 6, no. 1, pp. 1–10, 2016.

[8] Y. Ji *et al.*, "Flexible and twistable non-volatile memory cell array with all-organic one diode-one resistor architecture," Nature Communications, vol. 4, no. 1, p. 2707, 2013.

[9] U. S. Bhansali *et al.*, "Metal-free, single-polymer device exhibits resistive memory effect," ACS Nano, vol. 7, no. 12, pp. 10518–10524, 2013.

[10] A. Solanki *et al.*, "Correlation between blend morphology and recombination dynamics in additive-added P3HT:PCBM solar cells," Physical Chemistry Chemical Physics, vol. 17, no. 39, pp. 26111–26120, 2015.

[11] H. C. Wu *et al.*, "A poly(fluorene-thiophene) donor with a tethered phenanthro[9,10-d]imidazole acceptor for flexible nonvolatile flash resistive memory devices," Chemical Communications, vol. 48, no. 73, pp. 9135–9137, 2012.

[12] A. Chiolerio *et al.*, "Bridging electrochemical and electron devices: fast resistive switching based on polyaniline from one pot synthesis using $FeCl_3$ as oxidant and co-doping agent," Synthetic Metals, vol. 229, pp. 72–81, 2017.

[13] B. Mukherjee *et al.*, "High-performance molecular memory device using Ag−TCNQ crystals grown by solution process," The Journal of Physical Chemistry C, vol. 114, no. 1, pp. 567–571, 2010.

[14] T. C. Sum and N. Mathews, "Advancements in perovskite solar cells: photophysics behind the photovoltaics," Energy & Environmental Science, vol. 7, no. 8, pp. 2518–2534, 2014.

[15] C. Gu and J. S. Lee, "Flexible hybrid organic-inorganic perovskite memory," ACS Nano, vol. 10, no. 5, pp. 5413–5418, 2016.

[16] J. S. Han *et al.*, "Air-stable cesium lead iodide perovskite for ultra-low operating voltage resistive switching," Advanced Functional Materials, vol. 28, no. 5, p. 1705783, 2018.
[17] C. C. Stoumpos *et al.*, "Ruddlesden–popper hybrid lead iodide perovskite 2D homologous semiconductors," Chemistry of Materials, vol. 28, no. 8, pp. 2852–2867, 2016.
[18] L. Mao *et al.*, "Hybrid Dion–Jacobson 2D lead iodide perovskites," Chemistry of Materials, vol. 140, no. 10, pp. 3775–3783, 2018.
[19] J. H. Im *et al.*, "Morphology-photovoltaic property correlation in perovskite solar cells: One-step versus two-step deposition of $CH_3NH_3PbI_3$," APL Materials, vol. 2, no. 8, p. 081510, 2014.
[20] M. Xiao *et al.*, "A fast deposition-crystallization procedure for highly efficient lead iodide perovskite thin-film solar cells," Angewandte Chemie, vol. 53, no. 37, pp. 9898–9903, 2014.
[21] B. Hwang and J.-S. Lee, "A strategy to design high-density nanoscale devices utilizing vapor deposition of metal Halide perovskite materials," Advanced Materials, vol. 29, no. 29, p. 1701048, 2017.
[22] D. Lee *et al.*, "Impact of grain sizes on programmable memory characteristics in two-dimensional organic-inorganic hybrid perovskite memory," ACS Applied Materials & Interfaces, vol. 11, no. 22, pp. 20225–20231, 2019.
[23] E. Yoo *et al.*, "Bifunctional resistive switching behavior in an organolead halide perovskite based Ag/$CH_3NH_3PbI_{3-x}Cl_x$/FTO structure," Journal of Materials Chemistry C, vol. 4, no. 33, pp. 7824–7830, 2016.
[24] E. J. Yoo *et al.*, "Resistive switching behavior in organic-inorganic hybrid $CH_3NH_3PbI_{3-x}Cl_x$ perovskite for resistive random access memory devices," Advanced Materials, vol. 27, no. 40, pp. 6170–6175, 2015.
[25] C. Stecker *et al.*, "Surface defect dynamics in organic-inorganic hybrid perovskites: From mechanism to interfacial properties," ACS Nano, vol. 13, no. 10, pp. 12127–12136, 2019.
[26] D. J. Kim *et al.*, "Resistive switching properties through iodine migrations of a hybrid perovskite insulating layer," Advanced Materials Interfaces, vol. 4, no. 6, p. 1601035, 2017.
[27] D. Moia and J. Maier, "Ion transport, defect chemistry, and the device physics of hybrid perovskite solar cells," ACS Energy Letters, pp. 1566–1576, 2021.
[28] Y. Sun *et al.*, "Competition between metallic and vacancy defect conductive filaments in a $CH_3NH_3PbI_3$-based memory device," The Journal of Physical Chemistry C, vol. 122, no. 11, pp. 6431–6436, 2018.
[29] A. Solanki *et al.*, "Interfacial mechanism for efficient resistive switching in ruddlesden-Popper perovskites for non-volatile memories," Journal of Physical Chemistry Letters, vol. 11, no. 2, pp. 463–470, 2020.
[30] R. E. Cohen, "Origin of ferroelectricity in perovskite oxides," Nature, vol. 358, no. 6382, pp. 136–138, 1992.
[31] J. M. Frost *et al.*, "Atomistic origins of high-performance in hybrid halide perovskite solar cells," Nano Letters, vol. 14, no. 5, pp. 2584–2590, 2014.
[32] Y. Rakita *et al.*, "Tetragonal $CH_3NH_3PbI_3$ is ferroelectric," Proceedings of the National Academy of Sciences of the USA, vol. 114, no. 28, pp. E5504–E5512, 2017.
[33] C. C. Stoumpos *et al.*, "Semiconducting tin and lead iodide perovskites with organic cations: phase transitions, high mobilities, and near-infrared photoluminescent properties," Inorganic Chemistry, vol. 52, no. 15, pp. 9019–9038, 2013.

[34] K. Yan *et al.*, "High-performance perovskite memristor based on methyl ammonium lead halides," Journal of Materials Chemistry C, vol. 4, no. 7, pp. 1375–1381, 2016.
[35] H. Kim *et al.*, "Quasi-2D halide perovskites for resistive switching devices with ON/OFF ratios above 10^9," NPG Asia Materials, vol. 12, no. 1, pp. 1–11, 2020.
[36] J. Zhao *et al.*, "Light-induced anomalous resistive switches based on individual organic-inorganic Halide perovskite micro-/nanofibers," Advanced Electronic Materials, p. 1800206, 2018.
[37] K. Yang *et al.*, "A facile synthesis of $CH_3NH_3PbBr_3$ perovskite quantum dots and their application in flexible nonvolatile memory," Applied Physics Letters, vol. 110, no. 8, p. 083102, 2017.
[38] G. Lin *et al.*, "An organic–inorganic hybrid perovskite logic gate for better computing," Journal of Materials Chemistry C, vol. 3, no. 41, pp. 10793–10798, 2015.
[39] J. Choi *et al.*, "Organolead Halide perovskites for low operating voltage multilevel resistive switching," Advanced Materials, vol. 28, no. 31, pp. 6562–6567, 2016.
[40] Y. Liu *et al.*, "Resistive switching memory based on organic/inorganic hybrid perovskite materials," Vacuum, vol. 130, pp. 109–112, 2016.
[41] B. Hwang *et al.*, "Effect of halide-mixing on the switching behaviors of organic-inorganic hybrid perovskite memory," Scientific Reports, vol. 7, no. 1, pp. 1–8, 2017.
[42] Z. Xu *et al.*, "To probe the performance of perovskite memory devices: defects property and hysteresis," Journal of Materials Chemistry C, vol. 5, no. 23, pp. 5810–5817, 2017.
[43] J. Choi *et al.*, "Enhanced endurance organolead Halide perovskite resistive switching memories operable under an extremely low bending radius," ACS Applied Materials & Interfaces, vol. 9, no. 36, pp. 30764–30771, 2017.
[44] J. Y. Seo *et al.*, "Wafer-scale reliable switching memory based on 2-dimensional layered organic-inorganic halide perovskite," Nanoscale, vol. 9, no. 40, pp. 15278–15285, 2017.
[45] J. H. Heo *et al.*, "Memory effect behavior with respect to the crystal grain size in the organic-inorganic hybrid perovskite nonvolatile resistive random-access memory," Scientific Reports, vol. 7, no. 1, pp. 1–8, 2017.
[46] H. Tian *et al.*, "Extremely low operating current resistive memory based on exfoliated 2D perovskite single crystals for neuromorphic computing," ACS Nano, vol. 11, no. 12, pp. 12247–12256, 2017.
[47] X. F. Cheng *et al.*, "Pseudohalide-induced 2D $(CH_3NH_3)_2PbI_2(SCN)_2$ perovskite for ternary resistive memory with high performance," Small, vol. 14, no. 12, p. 1703667, 2018.
[48] B. Hwang and J.-S. Lee, "Lead-free, air-stable hybrid organic-inorganic perovskite resistive switching memory with ultrafast switching and multilevel data storage," Nanoscale, vol. 10, no. 18, pp. 8578–8584, 2018.
[49] M. Kumar *et al.*, "Compliance-free multileveled resistive switching in a transparent 2D perovskite for neuromorphic computing," ACS Applied Materials & Interfaces, vol. 10, no. 15, pp. 12768–12772, 2018.
[50] H. Cai *et al.*, "A remarkable performance of $CH_3NH_3PbI_3$ perovskite memory based on passivated method," Organic Electronics, vol. 58, pp. 301–305, 2018.
[51] Y. Huang *et al.*, "Conductive metallic filaments dominate in hybrid perovskite-based memory devices," Science China materials, vol. 62, no. 9, pp. 1323–1331, 2019.

[52] S. Lee *et al.*, "Tailored 2D/3D Halide perovskite heterointerface for substantially enhanced endurance in conducting bridge resistive switching memory," ACS Applied Materials & Interfaces, vol. 12, no. 14, pp. 17039–17045, 2020.
[53] Y.-W. Hsiao *et al.*, "Resistive switching property of organic-inorganic Tri-cation lead iodide perovskite memory device," Nanomaterials (Basel), vol. 10, no. 6, p. 1155, 2020.
[54] Y. Ren *et al.*, "Cycling-induced degradation of organic-inorganic perovskite-based resistive switching memory," Advanced Materials Technologies, vol. 4, no. 1, p. 1800238, 2019.
[55] S. Hamdioui *et al.*, "Memristor based computation-in-memory architecture for data-intensive applications," in 2015 Design, Automation & Test in Europe Conference & Exhibition, pp. 1718–1725, 2015.
[56] Z. Xiao and J. Huang, "Energy-efficient hybrid perovskite memristors and synaptic devices," Advanced Electronic Materials, vol. 2, no. 7, p. 1600100, 2016.
[57] W. Xu *et al.*, "Organometal Halide perovskite artificial synapses," Adv. Mater., vol. 28, no. 28, pp. 5916–5922, 2016.
[58] R. A. John *et al.*, "Ionotronic Halide perovskite drift-diffusive synapses for low-power neuromorphic computation," Advanced Materials, vol. 30, no. 51, p. e1805454, 2018.
[59] L. Yang et al., "Transparent and flexible inorganic perovskite photonic artificial synapses with dual-mode operation," Advanced Functional Materials, vol. 31, no. 6, p. 2008259, 2021.
[60] Q. B. Zhu *et al.*, "A flexible ultrasensitive optoelectronic sensor array for neuromorphic vision systems," Nature Communications, vol. 12, no. 1, p. 1798, 2021.
[61] H. Yu *et al.*, "Mixed-halide perovskite for ultrasensitive two-terminal artificial synaptic devices," Materials Chemistry Frontiers, vol. 3, no. 5, pp. 941–947, 2019.
[62] L. Qian *et al.*, "A lead-free two-dimensional perovskite for a high-performance flexible photoconductor and a light-stimulated synaptic device," Nanoscale, vol. 10, no. 15, pp. 6837–6843, 2018.
[63] Z. Xiao *et al.*, "Giant switchable photovoltaic effect in organometal trihalide perovskite devices," Nature Materials, vol. 14, no. 2, pp. 193–198, 2015.
[64] Y. Wang *et al.*, "Synergies of electrochemical metallization and valance change in all-inorganic perovskite quantum dots for resistive switching," Advanced Materials, vol. 30, no. 28, p. e1800327, 2018.
[65] Y. Gao *et al.*, "Physical unclonable functions," Nature Electronics, vol. 3, no. 2, pp. 81–91, 2020.
[66] R. A. John *et al.*, "Halide perovskite memristors as flexible and reconfigurable physical unclonable functions," Nature Communications, vol. 12, no. 1, p. 3681, 2021.
[67] D. Ielmini and V. Milo, "Physics-based modeling approaches of resistive switching devices for memory and in-memory computing applications," Journal of Computational Electronics, vol. 16, no. 4, pp. 1121–1143, 2017.
[68] Y. N. Joglekar and S. J. Wolf, "The elusive memristor: properties of basic electrical circuits," European Journal of Physics, vol. 30, no. 4, pp. 661–675, 2009.
[69] Z. Biolek *et al.*, "Spice model of memristor with nonlinear dopant drift." Radioengineering, vol. 18, no. 2, 2009.
[70] T. Prodromakis *et al.*, "A versatile memristor model with nonlinear dopant kinetics," IEEE Transactions on Electron Devices, vol. 58, no. 9, pp. 3099–3105, 2011.

[71] E. Lehtonen and M. Laiho, "CNN using memristors for neighborhood connections," in 12th International Workshop on Cellular Nanoscale Networks and their Applications (CNNA), pp. 1–4, 2010.
[72] S. Kvatinsky *et al.*, "TEAM: ThrEshold Adaptive Memristor Model," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 60, no. 1, pp. 211–221, 2013.
[73] J. J. Yang *et al.*, "Memristive switching mechanism for metal/oxide/metal nanodevices," Nature Nanotechnology, vol. 3, no. 7, pp. 429–433, 2008.
[74] T. Chang *et al.*, "Synaptic behaviors and modeling of a metal oxide memristive device," Applied Physics A, vol. 102, no. 4, pp. 857–863, 2011.
[75] T. W. Molter and M. A. Nugent, "The generalized metastable switch memristor model," in 15th International workshop on cellular nanoscale networks and their applications (CNNA), pp. 1-2, 2016.
[76] A. S. Oblea *et al.*, "Silver chalcogenide based memristor devices," in 2010 International Joint Conference on Neural Networks (IJCNN), pp. 1-3, 2010.
[77] M. D. Pickett *et al.*, "Switching dynamics in titanium dioxide memristive devices," Journal of Applied Physics, vol. 106, no. 7, p. 074508, 2009.
[78] C. Yakopcic *et al.*, "A Memristor Device Model," IEEE Electron Device Lett., vol. 32, no. 10, pp. 1436–1438, 2011.
[79] C. Yakopcic *et al.*, "Memristor model optimization based on parameter extraction from device characterization data," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 39, no. 5, pp. 1084–1095, 2020.
[80] S. Benderli and T. A. Wey, "On SPICE macromodelling of TiO_2 memristors," Electronics Letters, vol. 45, no. 7, p. 377, 2009.
[81] D. B. Strukov and R. S. Williams, "Exponential ionic drift: fast switching and low volatility of thin-film memristors," Applied Physics A, vol. 94, no. 3, pp. 515–519, 2009.
[82] H. Abdalla and M. D. Pickett, "SPICE modeling of memristors," in 2011 IEEE International Symposium of Circuits and Systems (ISCAS), pp. 1832-1835, 2011.
[83] Y. V. Pershin and M. Di Ventra, "Spice model of memristive devices with threshold," Radioengineering, vol. 22, no. 2, 2013.
[84] D. Biolek *et al.*, "Reliable spice simulations of memristors, memcapacitors and meminductors," Radioengineering, vol. 22, no. 945, 2013.
[85] K. Yan *et al.*, "Memristive property's effects on the I-V characteristics of perovskite solar cells," Scientific Reports, vol. 7, no. 1, p. 6025, 2017.
[86] Y. Ren *et al.*, "Analytical modeling of organic-inorganic $CH_3NH_3PbI_3$ perovskite resistive switching and its application for neuromorphic recognition," Advanced Theory And Simulations, vol. 1, no. 4, p. 1700035, 2018.

CHAPTER 3

Understanding the Effect of Measurement Procedure on Memristor Characteristics

Contents

3.1 Introduction

While the switching parameters of a memristor depend on its active layer and structure, they are also significantly affected by the procedure used for its forming and the measurement itself. For example, electroforming a pristine memristor can alter the material composition, morphology of the film, effective thickness of the device, etc., thereby altering its electrical resistance [1,2]. Forming acts as a vital step to optimize the devices for memory applications and distinct switching characteristics can be obtained from similar devices formed differently [3-6]. Thus, an understanding and comparison of forming methods are essential before one begins to work on any new material or structure for use in memristors. For this purpose, we began with the characterization of chalcogenide memristors which are stable, commercially available, and packaged in the form of ICs.

In these devices, the active layer is sandwiched between silver and tungsten electrodes and their operation is based on the migration of silver ions into the active layer. Different electroforming methods, such as the use of sinusoidal signal, linear voltage sweep, linear current sweep, constant voltage bias, and fast voltage pulse have been used, and their effects on memristor performance have been studied in this work. The devices formed using the positive voltage sweep method have been found to give the most repeatable characteristics essential to study their switching and current conduction mechanisms. Furthermore, the effects of certain characterization parameters such as voltage SR, I_{CC}, etc., have also been analyzed.

3.2 Chalcogenide Memristor

3.2.1 Device Structure and Working Principle

A photograph of the memristor IC and its internal arrangement are shown in figures 3.1 (a) and (b), respectively. The 16-pin DIP IC (Knowm Inc.) has eight separate

chalcogenide memristors with Ge_2Se_3 as the active layer. The multilayer schematic of these memristors is given in figure 3.1 (c). Each of the layers in the memristor structure have been deposited by in-situ sputtering on a 100 nm p-type Si wafer in a stacked manner. The via size is in the range of 0.25 µm to 4 µm in diameter, and the device operation is claimed to be independent of the via size within this range [7].

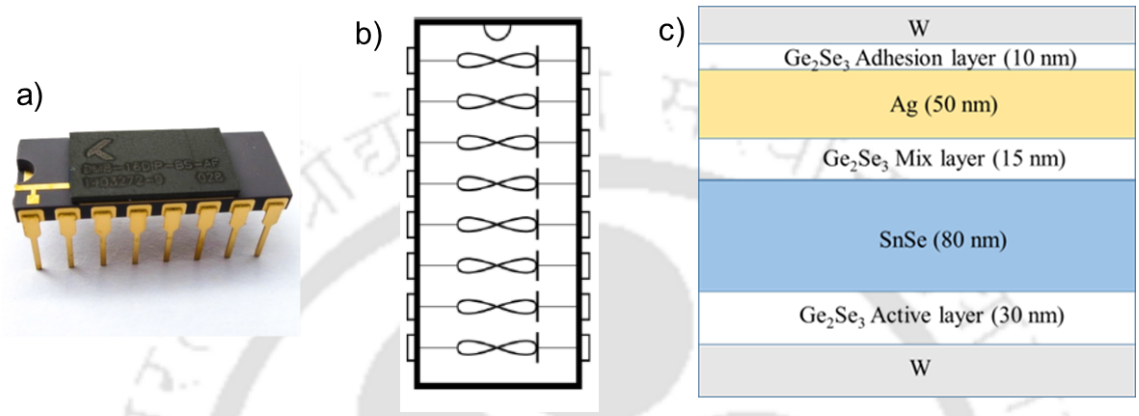


Figure 3.1: (a) Photograph of a Knowm 16 pin DIP package memristor IC. (b) Schematic of the internal arrangement of 8 memristors inside the DIP package. (c) Schematic of the material stack inside the chalcogenide memristor.

The Ge_2Se_3 adhesion layer is required as the W TE does not adhere well directly to the Ag layer. During deposition, the Ge_2Se_3 mix layer gets mixed with Ag and Ge_2Se_3 adhesion layers and jointly forms the Ag-source layer. It also separates the Ag layer from direct contact with the active layer and, subsequently, the auto migration of Ag ions (Ag^+) into the active layer is prevented during the high-temperature processing (~250°C to 350°C). As a result, these memristors can be operated over a wide range of temperatures (up to 150°C). The Ag^+ ions can migrate through this thin layer upon proper biasing, without hampering the working of device [8]. The working principle in these chalcogenide memristors is termed as the Self-Directed Channel (SDC) mechanism [7,8]. It is a type of ECM, which is different from the typical Conductive Bridge Resistive Random Access Memory (CBRAM) [9]. Here, silver ions (Ag^+) migrate inside the Ge_2Se_3 active layer and change the device resistance. In the forming step, with the positive potential at the TE, tin ions (Sn^{2+}) from the SnSe layer move into the Ge_2Se_3

active layer and enable the formation of an electron pair near Ge-Ge dimer. Ag^+ ions can selectively attract these negatively charged dimers to form a neutral Ag-Ge bond [10]. Due to this reaction, Ge-rich active layer gets distorted, which creates an opening to grow conductive Ag channels in the subsequent cycles. The device resistance changes based on the amount of Ag^+ ions in these channels. The chalcogenide memristors have also been reported to show a phase change response when operated at comparatively higher voltages [11]. We have also observed this phase change behaviour during their characterization, which is mentioned in the relevant sections that follow.

3.2.2 Manufacturer-Recommended Method

To observe the pinched hysteresis loop, sinusoidal voltage signals (1 V_{pp}) were applied to the devices, as recommended by the manufacturer. The I-V characteristics obtained from pristine memristors for four different frequencies show pinched hysteresis loops [12]. Due to the periodic nature of these signals, the forming step and the initial switching cycles could not be differentiated. Typically, these devices have been reported to show an endurance of the order of 10^8 cycles using a sinusoidal signal of 1.5 V_{pp} at 500 Hz, as can be found from the Knowm memristor datasheet [11].

As can be observed from figure 3.2, V_{SET} increases as the frequency of the applied sinusoidal signal increases. The device showed V_{SET} values of 0.38 V, 0.59 V, and 0.7 V at 1 Hz, 50 Hz, and 500 Hz, respectively and the corresponding ON/OFF ratios were 3.36, 3.19, and 2.96, respectively. The V_{RESET} values were -0.34 V, -0.20 V, and -0.41 V at 1 Hz, 50 Hz, and 500 Hz, respectively, showing a non-monotonic variation. Notably, at frequencies approaching 1 kHz, the pinched hysteresis loop nearly vanishes, with the ON/OFF ratio reducing to ~1 and making the memristor unsuitable for memory applications. Clearly, the ON/OFF ratios obtained from this method are too small for ReRAM applications and other ways to electroform these memristors should be explored.

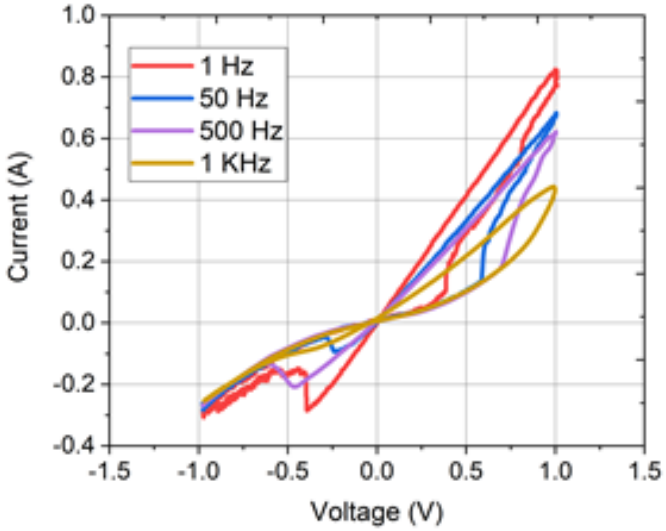


Figure 3.2: Pinched hysteresis loop obtained from the chalcogenide memristor using sinusoidal inputs (1 V_{pp}) of different frequencies.

3.3 Alternative Electroforming Methods

The switching characteristics of chalcogenide memristors formed by different methods have been summarized in the following sub-sections.

3.3.1 Constant Voltage Bias

The simplest way to form the chalcogenide memristor is to apply a constant voltage for a certain time, switching the device from a HRS to an LRS. This method can be used to find the time required for forming, switching, and retainting the HRS/LRS [13,14]. Here, constant voltage biases of different amplitudes were applied to the pristine devices for a finite time. Figures 3.3(a) and 3.3(b) show four I-V hysteresis loops of devices formed at 0.4 V and 0.3 V, respectively. The currents through these devices during forming were constant throughout the forming process, as shown in the insets of the respective plots, implying that both the devices formed right at the moment when a bias signal was applied to them. Figure 3.3(c) shows the RS during forming step, obtained from the application of 0.2 V. The first RS was observed at 54 seconds after the application of forming bias began. The subsequent switching cycles, obtained by using a voltage sweep with an SR of 800 mV/s, resulted in switching the device ON from HRS to LRS at 0.25 V and switching OFF from LRS to HRS at -0.6 V (the black plot in figure

3.3 (d)). An ON/OFF ratio of 16 was obtained from 0.2 V bias which was higher than that from the sinusoidal signal forming method. However, other methods shown in the subsequent sections provided even better ON/OFF ratios.

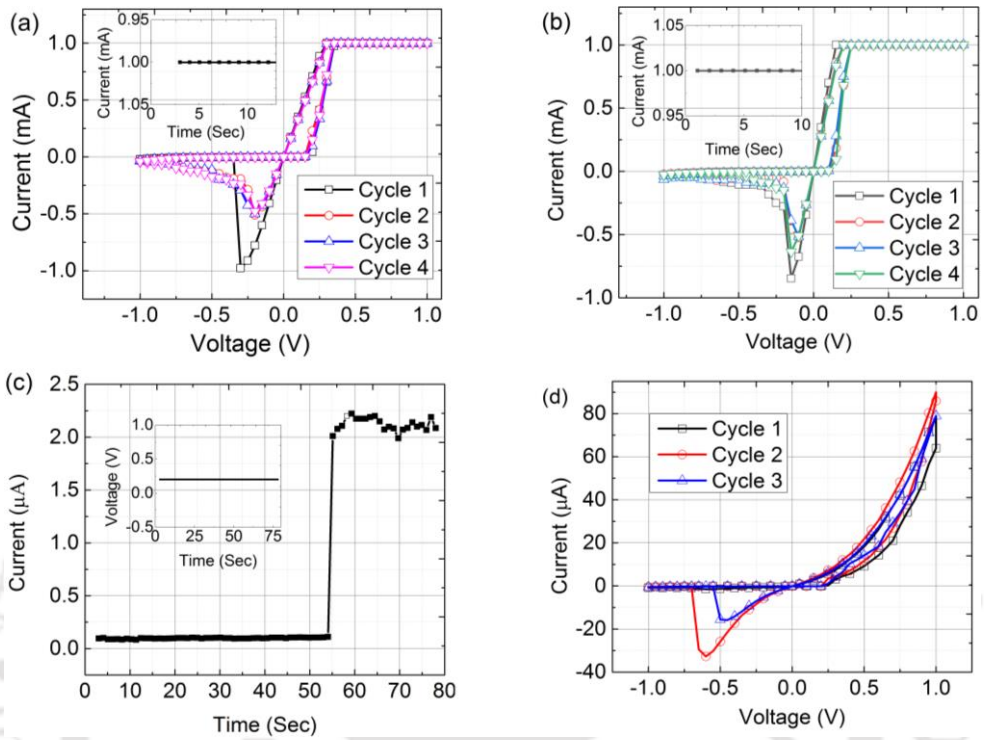


Figure 3.3: Switching cycles from devices formed using constant voltage bias of (a) 0.4 V, and (b) 0.3 V. Insets of (a) and (b) show the currents in the respective devices, which have a value of 1mA throughout, indicating that the devices are in LRS from the beginning of the forming sweep. (c) Forming current step. (d) The switching cycles of the device formed with a constant bias of 0.2 V.

The selection of adequate forming voltage ($V_{FORMING}$) level is critical in applying this forming method. Using a smaller voltage such as 0.2 V or lesser takes a substantially long time to form the device. On the other hand, a voltage greater than or equal to 0.3 V forms the device instantly, allowing 1 mA current to flow through the device. This high current may alter device morphology because of Joule heating and change the device operation to unipolar switching, which in a worst-case scenario, can destroy the switch permanently [6]. However, the rate of forming process and SET process can be controlled by selecting a proper constant voltage level. Application of different bias levels during forming and switching can manifest as different LRSs, which may help in realizing multi-level ReRAM devices [15].

3.3.2 Linear Voltage Sweep

A linearly increasing positive voltage sweep with an SR of 8 mV/sec, as shown in the inset of figure 3.4(a), was applied to the pristine device, with an I_{CC} of 1 mA. In our characterization system, we have set the voltage step size as 0.5 mV from which we have calculated SR as the ratio of the range of voltage sweep (V_{Range}) to the total execution time (t_{exe}). It was observed that electroforming occurred at 0.31 V. At this voltage, the device resistance changed from 1 MΩ (HRS) to 0.36 kΩ (LRS). This forming method produces RS characteristics with the required pinched hysteresis loop. A bipolar triangular signal has been applied at an SR of 800 mV/sec to observe its switching characteristics, as shown in figure 3.4(b). The device switched ON at 0.25 V and switched OFF at -0.25 V. In the positive cycle of the pinched hysteresis loops, the device current in the LRS reached the set compliance of 1 mA. However, in the negative cycle, the device current reached only up to 0.6 mA. The ON/OFF ratios in the positive and negative half-cycles were 616 and 924 respectively (measured at 0.1 V and -0.1 V respectively), which are much higher than those from the previously described methods. The repeatability of the switching cycles has been found to be excellent, as we observed that the average deviation of V_{SET} and V_{RESET} from five consecutive voltage sweep cycles are as small as ±0.01 V and ±0.02 respectively.

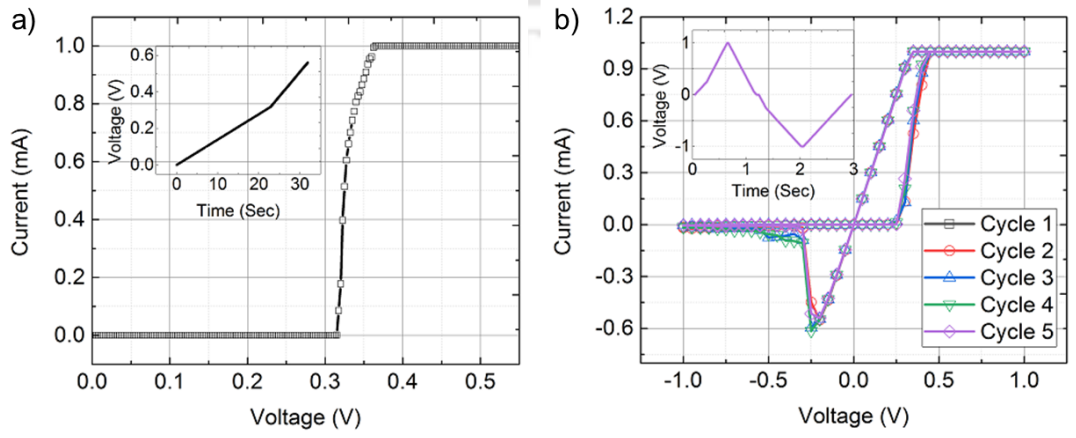


Figure 3.4: (a) Forming current step. (b) Switching cycles of the device formed with a positive voltage sweep. The insets of both (a) and (b) show the applied voltage signal.

To observe the phase change phenomenon, we gradually increased the applied voltage to a pristine device. When a negative voltage sweep was applied, we observed that the device current switched to an LRS at a voltage of -4.3 V (see figure 3.5(a)). The subsequent switching characteristics obtained from this device are shown in figure 3.5(b). These are markedly different from those obtained using low positive $V_{FORMING}$, and resemble the typical phase change behaviour of the chalcogenide material, as mentioned in the manufacturer data sheet.

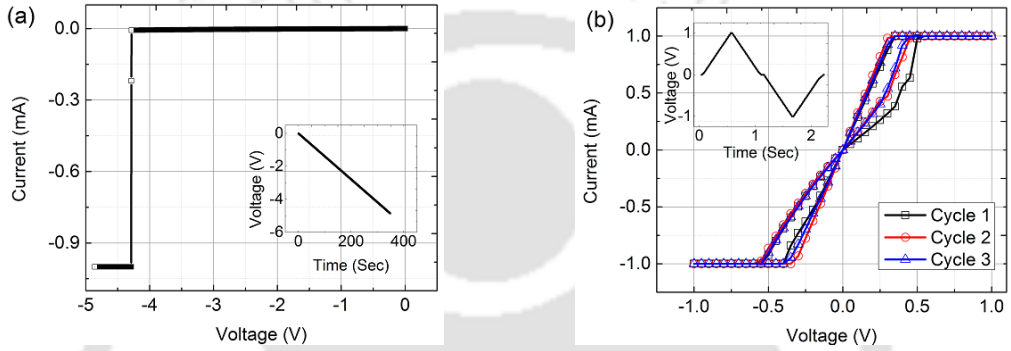


Figure 3.5: (a) Forming current step. (b) Switching cycles of the device formed with a negative voltage sweep. Insets of both (a) and (b) show the applied voltage signal.

3.3.3 Linear Current Sweep

Memristors have been reported to be formed using current sweep as well [16,17]. As shown in figure 3.6(a), when formed with a current sweep, pristine chalcogenide devices do go to an LRS. However, the corresponding resistance is not as low as that obtained from voltage sweep forming. The voltage in the device automatically drops once the first Ag channel is formed, thereby avoiding any new channel formation [5,18]. To check the possibility of these devices switching to the actual LRS, current sweeps up to 10 mA have been applied. But no further lowering of LRS could be observed even at these high current levels. Three switching cycles obtained from this device are shown in figure 3.6(b), where the inset shows the applied bipolar triangular signal. The positive cycle switching characteristics are similar to those obtained for the negative voltage sweep forming case (figure 3.5(b)). However, there is much difference in the negative

cycles of both the characteristics. Due to the high currents, the devices seem to undergo a phase change.

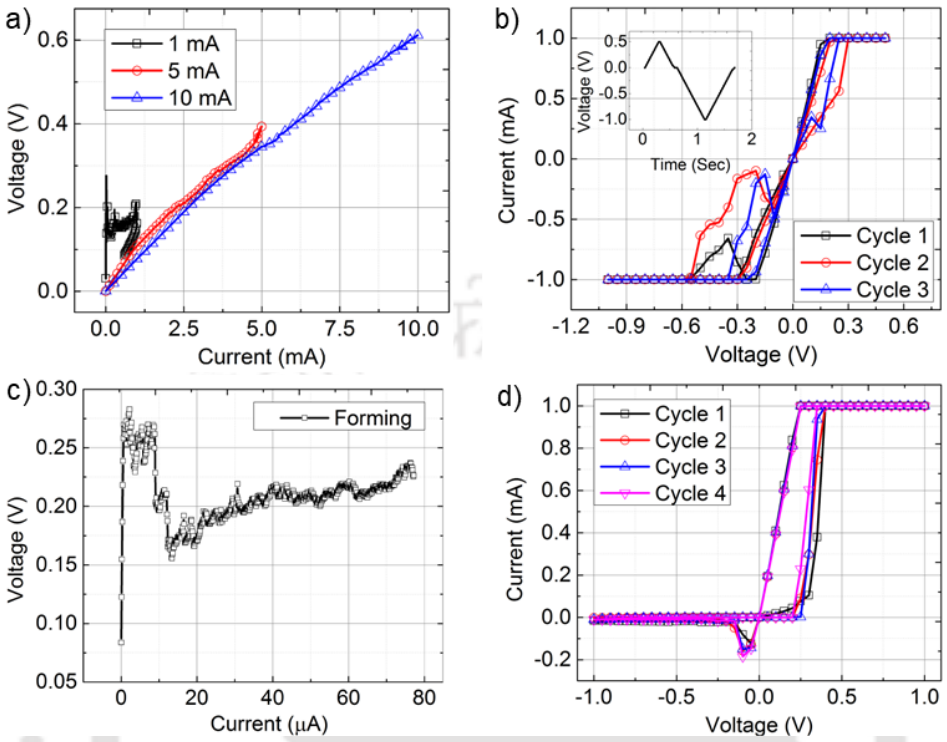


Figure 3.6: (a) Forming a pristine device using current sweeps up to 10 mA, (b) switching cycles of those devices, (c) forming step of another pristine memristor limiting current to the first resistance switch, and (d) switching cycles of those devices.

The applied current sweep was limited to the first RS point to avoid this phase change behaviour. Figure 3.6(c) shows the first RS point during forming current sweep, where the device resistance switched from 385.7 kΩ to 13.5 kΩ, giving a poor ON/OFF ratio of 29. This was followed by voltage sweeps to observe switching behaviour in the device. As can be seen from figure 3.6(d), the first switch ON cycle occurred at 0.3 V and, surprisingly, the ON/OFF ratio was at least two orders of magnitude higher than that observed during the forming step. It indicates that the first voltage sweep itself acts as a forming step, apparently rendering the previous current sweep redundant. The subsequent switching cycles gave high ON/OFF ratios of 3685 and 1193 in the positive and negative cycles, respectively. The ON and OFF voltages were 0.25 V and -0.1 V, respectively.

An important point to note is that the current sweep before the actual forming using voltage sweep seems to improve the memristor properties by lowering switching

voltages and increasing ON/OFF ratio. This is because a current stress before the forming process introduces additional defects inside the active layer that enhance the RS performance [19].

3.3.4 Pulse Voltage

In practical products, fast pulse programming (upto sub-ns) is used for the read, write, and erase operations of memory devices [20,21]. Similar to the constant voltage stress, voltage pulses can also be used to get short forming, SET, and RESET times. To start with, a single voltage pulse with an amplitude of 5 V has been applied to the memristor using the set-up shown in figure 3.7(a). The pulse width has been varied from a few µs to a few hundred µs, and the change in resistance has been observed in terms of voltage change in the oscilloscope. A two-channel oscilloscope was used to observe the voltage changes across a standard resistor R_{Load} (V_A at channel 1) and across the memristor (V_B at channel 2). A voltage pulse of amplitude 5 V made the memristor switch from HRS to LRS, indicating completion of forming process, at around 370 µs (see figure 3.7(b)). To optimize the minimum voltage required for this forming, the pulse amplitude has been varied starting from 1 V until forming is completed, as shown in figure 3.7(c). The devices formed only at a pulse amplitude of 4.8 V, after 420 µs of application of the pulse signal.

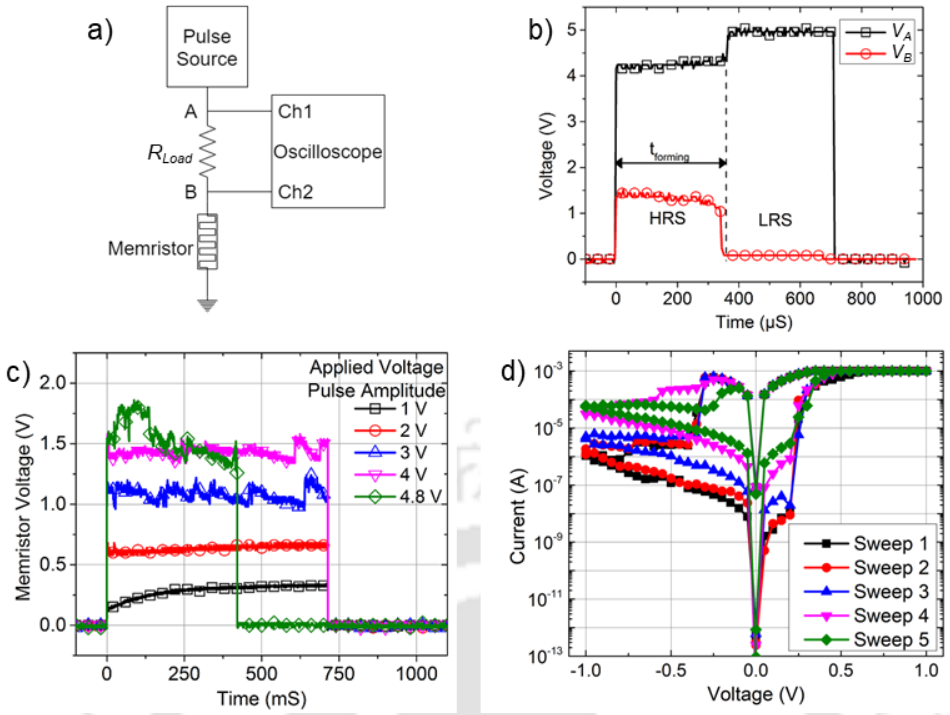


Figure 3.7: (a) Schematic of experimental set up for voltage pulse characterization; (b), (c) Voltage across memristor during forming using voltage pulses; (b) varying pulse width with constant amplitude and (c) varying pulse amplitude with constant pulse width. (d) Switching cycles obtained from a memristor formed with a voltage pulse.

The I-V characteristics obtained from a device formed using voltage pulse are shown in figure 3.7(d). The V_{SET} was 0.2 V, and the V_{RESET} ranged from -0.3 V to -0.1 V. The ON/OFF ratios obtained for the five consecutive cycles were 1.1×10^5, 6.5×10^4, 1.2×10^4, 1133, and 238 in positive half cycles and 1.2×10^4, 6796, 2190, 319, and 104 in the negative half-cycles, measured at 0.1 V and -0.1 V respectively. The ON/OFF ratios for the initial few cycles were much higher than those obtained from other forming methods. However, they reduce significantly with subsequent sweeps. The use of voltage pulse for forming may be considered the same as that of a DC bias, but for a small period of time. During forming via these methods, the current is not properly controllable, which can result in a large power consumption during the operation. Due to this, the device resistance during the subsequent switching cycles is unpredictable, which may have led to such an inconsistent behaviour. However, with the optimization of amplitude and width of the ultra-fast voltage pulses, the flow of leakage current in the device can be controlled and, subsequently, the power consumption can be minimized.

In ReRAM devices, the V_{SET} and V_{RESET} voltages are preferred to be small as they are directly associated with the power consumption during switching [22]. However, they should not be too small so that any noise signal may not alter the logic state of the memory device. The resistance in LRS is preferred to be as low as possible to obtain a high ON/OFF ratio and, in return, a better noise margin. Considering all these factors, out of all the methods of electroforming summarized above, the positive voltage sweep method gives the best switching parameters with sufficiently large repeatability, making it most suitable for chalcogenide memristors.

3.4 Role of Characterization Parameters

Apart from the forming step, two other characterization parameters, namely SR and I_{CC}, also play an important role in altering the switching performance [23]. Therefore, the selection of proper ranges for these parameters is of utmost importance. We have varied these parameters systematically to understand their effect on the switching performance of the chalcogenide memristors.

3.4.1 Effect of Scan Rate Variation

The effect of voltage SR variation during forming and switching cycles can be seen from the plots given in figure 3.8. It was observed that $V_{FORMING}$ increases with SR. For example, the forming steps of two pristine memristors, as given in figure 3.8(a), show that the device formed at SR= 18 mV/s had $V_{FORMING}$= 3.1 V, and that formed at SR= 0.14 mV/s showed $V_{FORMING}$= 2.2 V. A similar trend, though relatively less prominent, has also been observed with V_{SET} during the switching cycles. From the three switching cycles, given in figure 3.8(b), it can be observed that the use of voltage sweeps with SRs of 800 mV/s, 18 mV/s, and 8 mV/s, resulted in V_{SET} values of 0.2 V, 0.15 V, and 0.13 V, respectively.

It is important to note here that a faster SR, leading to a relatively higher switching voltage, is associated with higher power consumption during switching. On the other hand, a smaller switching voltage obtained by using a very slow changing voltage sweep may be affected by noise signals, resulting in a state error. Hence, the selection of an adequate SR is essential to obtain suitable $V_{FORMING}$ and switching voltages.

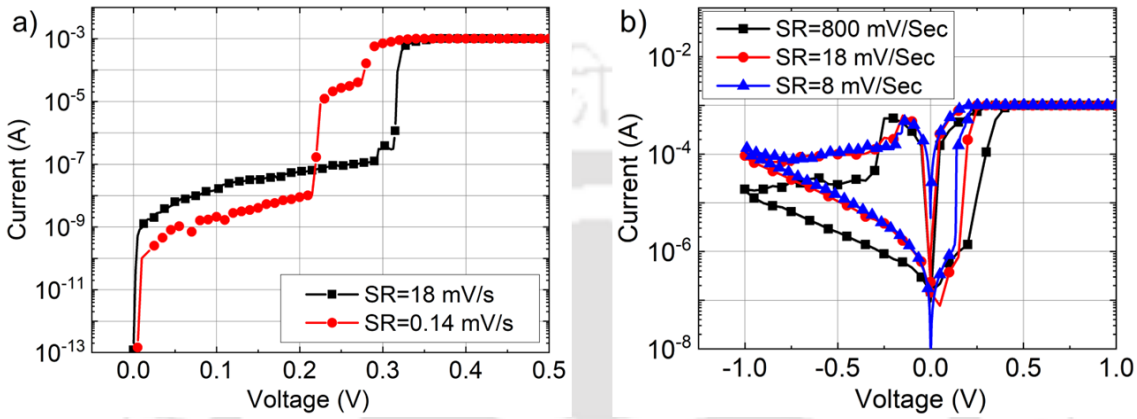


Figure 3.8: (a) The forming step of two pristine memristors using two different SRs. (b) Switching cycles using three different SRs.

3.4.2 Effect of Compliance Current Variation

The I_{CC} and the stop voltage (V_{STOP}) during RESET are the two operational parameters that alter the HRS and LRS of the memristor. While V_{STOP} changes HRS by altering the residual resistance during the gradual RESET process [24], I_{CC} affects the size and cross-section of the CF during the forming and SET processes. A higher I_{CC} results in the formation of a stronger Ag channel with less resistance in the LRS, which requires more energy and power to get ruptured during RESET [25,26]. Forming step I-V plotsof three different devices, with I_{CC} values of 0.5 mA, 1 mA, and 5mA, are shown in figure 3.9(a).Figure 3.9(b) shows the corresponding switching cycles of these devices. In contrast to V_{SET}, a large increase in V_{RESET} can be observed from the device formed with I_{CC} = 5mA relative to those with lower I_{CC} values. This is due to the migration of excess Ag^+ ions into the active layer during the positive half of the switching cycle as a result of the large current flow. If I_{CC} is further increased, the phase of the active layer may get

changed due to the large heat generated in the device. In such a case, completely different I-V characteristics will be obtained, as discussed in the previous section.

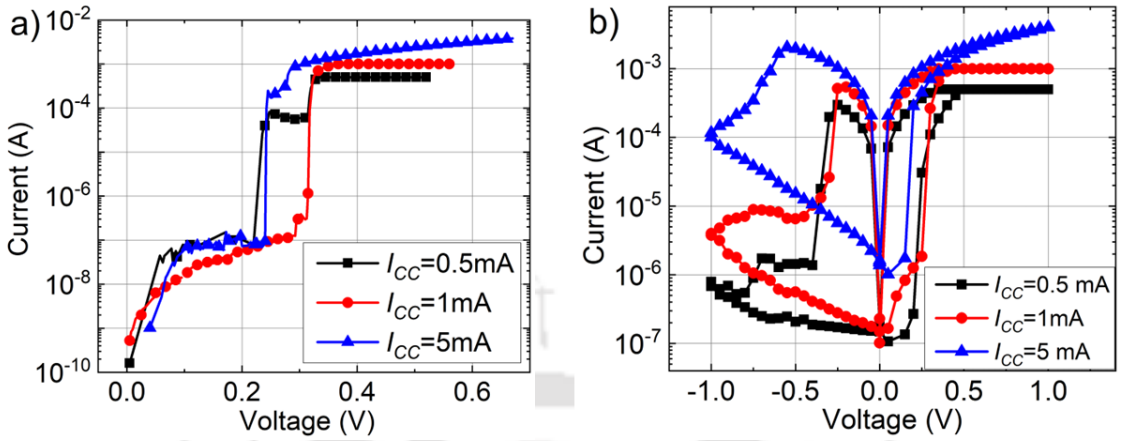


Figure 3.9: a) Comparison of $V_{FORMING}$ sweep with 3 different I_{CC} values. (b) Switching cycles of the devices formed at 3 different I_{CC}.

Ideally, a memristor, when used for memory applications, is preferred to have fast switching with small operating voltages. As the switching phenomenon involves an electrochemical redox reaction inside the active layer, SET/RESET times exponentially decrease with an increase in the applied voltage. Therefore, a trade off needs to be made between the operating voltage and the switching time in any ECM memristors. The results and observations inferred from this chapter have been used as the background for the characterization of hybrid perovskite memristive devices, as described in the subsequent chapters.

3.5 Summary

Five different forming methods, namely sinusoidal signal, linear voltage sweep, linear current sweep, constant voltage stress, and fast voltage pulse, have been used to form pristine chalcogenide memristors. The effect of each of these methods on the memristor switching performance has been investigated. The ON/OFF ratio obtained by forming with manufacturer recommended sinusoidal signal method is significantly less than those obtained from other methods. With proper optimization of SR, I_{CC}, frequency, etc., the ON/OFF ratio and switching voltages can be improved significantly. Using the

constant voltage bias, V_{SET} and V_{RESET} can be brought down to values less than 0.1 V. However, the selection of optimum $V_{FORMING}$ is a major challenge in using this method. Using a smaller voltage, in case of constant voltage forming method, takes a substantially long time to form the device. On the other hand, higher voltages form the device instantly, allowing a high current to flow through the device. With the voltage sweep method, SR and I_{CC} are the two important parameters that must be optimized to obtain uniform and repeatable switching performance. The current sweep forming method ensures a single filament formation during the forming and SET process, without the requirement of any I_{CC}. However, forming using this method does not provide sufficient electric field to shift the resistance to an optimum low value. In fact, it is the subsequent voltage sweep, applied for RS, that actually forms the device. Interestingly, this results in an ON/OFF ratio higher than that from the voltage sweep method. Although the pulse forming method is faster than the DC forming methods presented here, the forming time is higher than that of state-of-the-art memory devices. This forming time can be reduced by increasing the pulse amplitude. With proper optimization of the forming time, leakage current during the operation can be reduced, thereby minimizing power consumption. However, the switching characteristics obtained from the devices formed with voltage pulses are inconsistent.

Obtaining the optimum performance out of the memristor involves a trade-off between power consumption and noise margin, and, hence, the selection of proper characterization parameters is essential for any new memristive device. Other characterization methods, such as illumination and magnetism, can also be explored, which may open up new application areas for memristors.

3.7 References

[1] J. J. Yang *et al.*, "The mechanism of electroforming of metal oxide memristive switches," Nanotechnology, vol. 20, no. 21, p. 215201, 2009.
[2] R. Tetzlaff, Ed., **"**Memristors and Memristive Systems**,"** Springer**,** New York, 2014.

[3] D. S. Jeong *et al.*, "Emerging memories: resistive switching mechanisms and current status," Reports on Progress in Physics, vol. 75, no. 7, p. 076502, 2012.
[4] L. Chua, "Everything you wish to know about memristors but are afraid to ask," Radioengineering, vol. 24, no. 2, pp. 319–368, 2015.
[5] C. Nauenheim *et al.*, "Investigation of the electroforming process in resistively switching TiO_2 nanocrosspoint junctions," Applied Physics Letters, vol. 96, no. 12, p. 122902, pp. 1–3, 2010.
[6] D. S. Jeong *et al.*, "Characteristic electroforming behavior in Pt/TiO_2/Pt resistive switching cells depending on atmosphere," Journal of Applied Physics, vol. 104, no. 12, p. 123716, 2008.
[7] A. S. Oblea *et al.*, "Silver chalcogenide-based memristor devices," in 2010 International Joint Conference on Neural Networks (IJCNN), pp. 1–3, 2010.
[8] K. A. Campbell, "Self-directed channel memristor for high-temperature operation," Microelectronics, vol. 59, pp. 10–14, 2017.
[9] M. Kund *et al.*, "Conductive bridging RAM (CBRAM): an emerging non-volatile memory technology scalable to sub 20nm," in 2005 IEEE International Electron Devices Meeting, (IEDM), pp. 754–757, 2005.
[10] A. H. Edwards *et al.*, "Electron self-trapping in Ge_2Se_3 and its role in Ag and Sn incorporation," Materials Research Society Symposium Proceedings, vol. 1431, no. mrss12-1431-f01-03, 2012.
[11] "Self-Directed Channel Memristors," Knowm.org, 2019. [Online]. Available: https://knowm.org/downloads/Knowm_Memristors.pdf. [Accessed: 05-Mar-2022].
[12] L. Chua, "If it's pinched it's a memristor," Semiconductor Science and Technology, vol. 29, no. 10, p. 104001, 2014.
[13] Y. S. Chen *et al.*, "Highly scalable hafnium oxide memory with improvements of resistive distribution and read disturb immunity," in 2009 IEEE International Electron Devices Meeting (IEDM), pp. 1–4, 2009.
[14] W. C. Luo *et al.*, "RRAM SET speed-disturb dilemma and rapid statistical prediction methodology," in 2012 International Electron Devices Meeting (IEDM), pp. 951-954, 2012.
[15] J. Lin *et al.*, "Multi-level switching of Al-doped HfO_2 RRAM with a single voltage amplitude set pulse," Electronics (Basel), vol. 10, no. 6, p. 731, 2021.
[16] U. Russo *et al.*, "Impact of electrode materials on resistive-switching memory programming," IEEE Electron Device Letters, vol. 30, no. 8, pp. 817–819, 2009.
[17] B. Gao *et al.*, "Identification and application of current compliance failure phenomenon in RRAM device," in Proceedings of 2010 International Symposium on VLSI Technology, System and Application, pp. 144–145, 2010.
[18] Y. Li *et al.*, "Resistive switching performance improvement via modulating nanoscale conductive filament, involving the application of two-dimensional layered materials," Small, vol. 13, no. 35, p. 1604306, 2017.
[19] H. Xie *et al.*, "Effect of low constant current stress treatment on the performance of the Cu/ZrO_2/Pt resistive switching device," Semiconductor Science and Technology, vol. 27, no. 10, p. 105007, 2012.
[20] H. Y. Lee *et al.*, "Evidence and solution of over-RESET problem for HfO_X based resistive memory with sub-ns switching speed and high endurance," in 2010 International Electron Devices Meeting (IEDM), pp. 1971-1974, 2010.
[21] P. Shrestha *et al.*, "Accurate RRAM transient currents during forming," in Proceedings of Technical Program - 2014 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA), pp. 1–2, 2014.

[22] G. Molas *et al.*, "Advances in oxide-based conductive bridge memory (CBRAM) technology for computing systems," in Advances in Non-Volatile Memory and Storage Technology, B. Magyari-Köpe and Y. Nishi, Eds. Elsevier, 2019.

[23] D. Ielmini, "Modeling the universal set/reset characteristics of bipolar RRAM by field- and temperature-driven filament growth," IEEE Transactions on Electron Devices, vol. 58, no. 12, pp. 4309–4317, 2011.

[24] H. Y. Lee *et al.*, "Low power and high-speed bipolar switching with a thin reactive Ti buffer layer in robust HfO_2 based RRAM," in 2008 IEEE International Electron Devices Meeting (IEDM), pp. 1–4, 2008.

[25] C. Rohde *et al.*, "Identification of a determining parameter for resistive switching of TiO_2 thin films," Applied Physics Letters, vol. 86, no. 26, p. 262907, 2005.

[26] U. Russo *et al.*, "Conductive-filament switching analysis and self-accelerated thermal dissolution model for reset in NiO-based RRAM," in 2007 IEEE International Electron Devices Meeting (IEDM), pp. 775–778, 2007.

[27] S. A. Moiz *et al.*, "Space Charge–Limited Current Model for Polymers", in Conducting Polymers. London, United Kingdom: IntechOpen, 2016.

CHAPTER 4

$MAPbI_3$ based Memristors

Contents

4.1 Introduction

Using the understanding of how the characterization process can affect the switching parameters of chalcogenide memristors as the background, we have systematically optimized methylammonium lead iodide ($MAPbI_3$)-based bipolar switching devices. In this chapter, the effects of SR, I_{CC}, pulse amplitude, and pulse width, on the performance of these devices is analyzed. The effects of the area and thickness scaling of the devices are also discussed. In addition, the characteristics of flexible devices showing repeatable BRS under applied stress are given. Based on these results, we arrive at a general characterization protocol for optimal operation of memristors made of HOIPs and other such materials.

4.2 Device Fabrication Process

A perovskite precursor was prepared by mixing lead iodide (PbI_2) and methylammonium iodide (CH_3NH_3I) in dimethylformamide (DMF). PbI_2 (99.9% pure) and anhydrous DMF were purchased from Sigma Aldrich and used directly without further processing. CH_3NH_3I powder (99% pure) was purchased from Great Cell Solar. In addition to the molar ratio of the solution, the stirring time and temperature were also varied for its optimization. A molar ratio of 1.2:1.2:1 yields the most homogenous precursor solution when stirred for 30 minutes at a temperature of 70˚C. Indium tin oxide (ITO) coated glass substrates of areas 25 cm^2 and 40 cm^2 were sequentially cleaned in soap water, deionized water, acetone, and isopropanol. The cleaned substrates were then exposed to UV/ozone treatment for 15 minutes to remove the residual molecular organic contaminants on the ITO surface, increase ITO work function, and induce hydrophilicity. On top of the ITO coated glass, poly(3,4-ethylene dioxythiophene) polystyrene sulfonate (PEDOT:PSS) was spin-coated at a speed of 4000 rpm for 45 seconds, followed by annealing at 85˚C for 15 minutes. PEDOT:PSS is a hole transporting layer (HTL) and helps in preventing shorts due to the rough ITO. The perovskite layer was coated on top

of HTL at a speed of 5000 rpm for 12 seconds. Several organic solvents such as toluene, chlorobenzene, diethyl ether, etc., have been utilized as antisolvents by various research groups [1-3]. Of these, toluene has been chosen in this work since it results in films with relatively good morphology [4]. We have added 180 μL of toluene while spin coating the perovskite layer. Then, a layer of [6,6]-phenyl-C61-butyric acid methyl ester (PCBM) was spin-coated at 3000 rpm for 45 seconds. PCBM is an electron transport layer (ETL) and, in our devices, it controls the diffusion of Ag^+ ions into $MAPbI_3$. Finally, a 100 nm thick silver layer was evaporated, for the TE, under high vacuum ($<10^{-6}$ mbar). Figures 4.1 (a) and (b) show the step-wise fabrication process and a schematic of the HOIP memristive device respectively.

It has been reported that the RS action in relatively thin (<100 nm) $MAPbI_3$ devices was due to metal ion migration from the electrode [7], which is difficult to control during electrode deposition as well as during operation. Thicker active layers, on the other hand, require higher operating voltages and result in inferior endurance and retention [8,9]. In general, devices with $MAPbI_3$ thicknesses below 400 nm seem to work reliably. When antisolvent method was used for our fabrication, we have obtained a thickness of 380.19±13.4 nm (median ± standard deviation) for the HOIP film. This thickness was calculated by taking 16 readings from different locations on the substrate using a profilometer (Make: Veeco, Model no. Dektak 150). Custom designed shadow masks, obtained from Asahitec Stencils Pvt. Ltd., were used during evaporation to yield circular TEs with different areas ranging from 0.0018 cm^2 to 0.00008 cm^2. Figure 4.1(c) shows the custom design of the shadow mask and figure 4.1(d) shows a photograph of the fabricated HOIP memristors with different areas. The substrate holder was slowly rotated during the evaporation step for obtaining a uniform deposition of metal. As $MAPbI_3$ is highly sensitive to oxygen and moisture, the whole process was carried out in an inert argon ambient inside a glovebox.

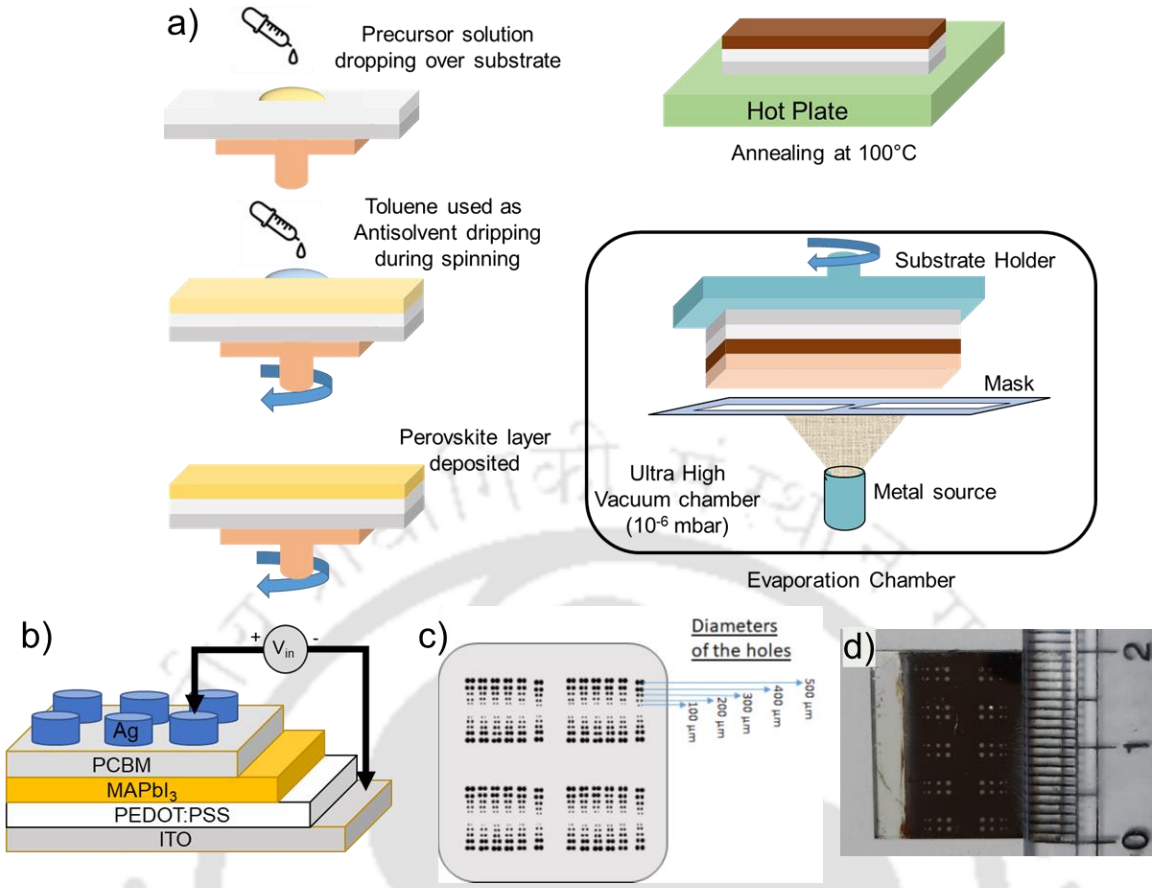


Figure 4.1: (a) Schematic of the fabrication process of HOIP memristive devices, (b) Schematic of a fabricated ITO/PEDOT:PSS (50 nm)/$MAPbI_3$ (380 nm)/PCBM (30 nm)/Ag (100 nm) memristor, (c) design of the shadow mask used for the TE deposition that has circular holes with 5 different diameters from 100 µm to 500 µm, and (d) A photograph of HOIP memristors with different areas, fabricated on an ITO coated glass substrate.

4.3 Thin Film Characterization

A critical step in achieving high-performance devices is to obtain a smooth and uniform perovskite film. To characterize the film for its quality and crystallinity, field emission scanning electron microscope (FESEM) (Make: Jeol Ltd., Model no. JSM-7610F) images, atomic force microscope (AFM) (Make: Bruker, Model no. Innova SPM) images, and X-ray diffraction (XRD) (Make: Rigaku, Model No. TTRAX III) plots were taken.

4.3.1 Effect of Antisolvent

An antisolvent decreases the solubility of the perovskite precursor in the solvent during spinning, facilitating the formation of uniform nucleation centers over the entire substrate. Antisolvent crystallization improves the active layer morphology and, hence, is

widely used in HOIP device fabrication. Toluene is the most commonly used antisolvent for DMF-based perovskite precursor washing [1,4]. It helps in the fast crystallization of perovskite film, resulting in a uniform film with large grain sizes and improved electrical characteristics. Here, toluene was dripped 2 seconds after starting the spin coating of the precursor, and the resulting film morphology was compared with the one coated without using any antisolvent.

The 2D and 3D AFM images of the films coated with and without antisolvent are shown in figures 4.2 (a) and (b), respectively. The average RMS roughnesses of these films were found to be 9.51 nm and 37.4 nm, respectively. Even though the spin speed was same, films prepared without antisolvent had relatively higher thicknesses (571.75 ± 47.87 nm). XRD spectra of both the films, given in figure 4.2 (c), show peaks at the same angles. The large peak at 14˚ (for both films) indicates the formation of the proper perovskite phase (110). There also remain a few undesired peaks and these are marked as #, *, ϕ, δ, γ, and λ in the figure. In the case of films without antisolvent treatment, the ratios of the intensity of the desired peak (110) to the undesired peaks were found to be 3.8, 8.9, 6.5, 7.4, 2.0, and 9.5, respectively. However, the antisolvent washing method resulted in improving these ratios to 48.4, 16.6, 11.2, 7.9, 3.2, and 15.1, respectively. From the roughness and XRD data, it is evident that antisolvent dripping during the perovskite layer coating resulted in superior film morphology. A performance comparison of the devices fabricated using these films is illustrated in the next section.

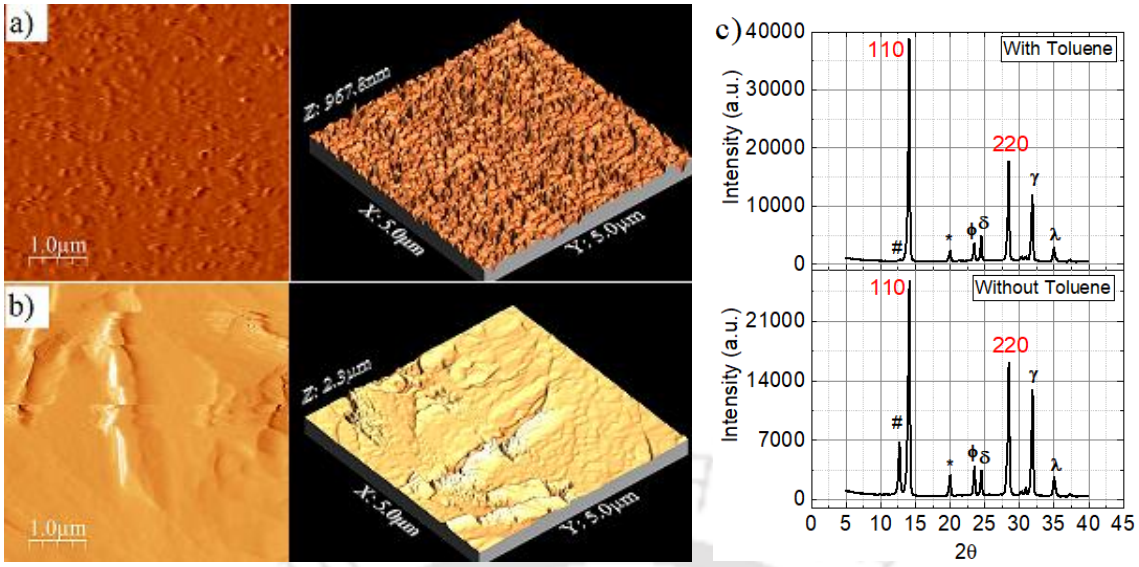


Figure 4.2: AFM images of the $MAPbI_3$ films coated (a) using antisolvent washing yielding an average RMS roughness of 9.51 nm and (b) without using antisolvent washing yielding an average RMS roughness of 37.4 nm. (c) XRD spectra of the $MAPbI_3$ films, coated using (top) and without using (bottom) antisolvent washing; the desired perovskite phase (110) at 14° is clearly visible, along with a few undesired peaks in both the films marked as #, *, ϕ, δ, γ, and λ. The intensity ratios of desired to undesired peaks improved with the use of antisolvent.

4.4 Electrical Characterization

Room temperature electrical characterization of the fabricated memristors was done using a semiconductor characterization system (SCS) (Keithley 4200) in combination with a probe station (Make: Lakeshore, model no. EMPX-H2), with the devices kept under vacuum (<0.01 mbar) to minimize their degradation. The current flowing from the top silver electrode to the bottom ITO electrode was considered positive.

As discussed in the previous chapter, pristine memristive devices require a forming step to initiate the RS. Once formed, the device can be switched from HRS to LRS by applying a voltage of positive polarity (i.e., the SET step). Subsequently, the device can be switched from LRS to HRS with the application of a negative voltage (i.e., the RESET step). One such BRS cycle is plotted in figure 4.3 (a), where the device showed a V_{SET} of 0.17 V, a V_{RESET} of -0.13 V, and an ON/OFF ratio of 1.3×10^3 (measured with a V_{READ} of 50 mV). The inset of the figure shows the forming step ($V_{FORMING}$ = 1.18

V). Figure 4.3 (b) shows the BRS cycle obtained from a device fabricated without using the antisolvent washing method. The $V_{FORMING}$, V_{SET} and V_{RESET} values (1.68 V, 1.15 V and -1.75 V, respectively) are significantly higher than those with antisolvent dripping. Also, these devices show a poor ON/OFF ratio of 11. Such an inferior performance is a consequence of the poor morphology of the $MAPbI_3$ layer. Without toluene dripping, the crystallization of $MAPbI_3$ becomes slow, ensuing a non-uniform film. Coupled with smaller domain sizes, this results in an increased contact resistance which, eventually, degrades the device performance [10].

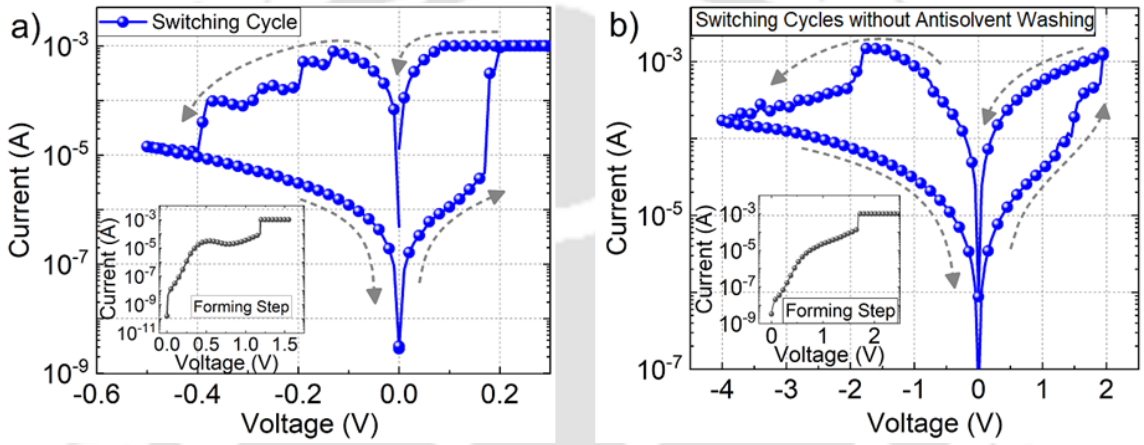


Figure 4.3: I-V characteristics of the memristive devices fabricated (a) with the use of toluene as the antisolvent and (b) without the use of antisolvent. Insets of these plots show the corresponding forming steps. The use of antisolvent lowers forming and switching voltages.

4.4.1 Role of Scan Rate

To study the effects of the measurement process on the switching behaviour of these devices, we have applied voltage sweeps at five different SRs. To set different SRs in our characterization system, we have changed the voltage step size from 0.5 mV to 50 mV that resulted in SRs ranging from 15 mV/s to 141 mV/s respectively. The I-V characteristics obtained from the same device with these five SRs are shown in figure 4.4(a). It can be seen that, while the positive side of the hysteresis loop remained consistent, showing only a slight increase in V_{SET}, the negative side of the loop showed a strong dependence on the SR.

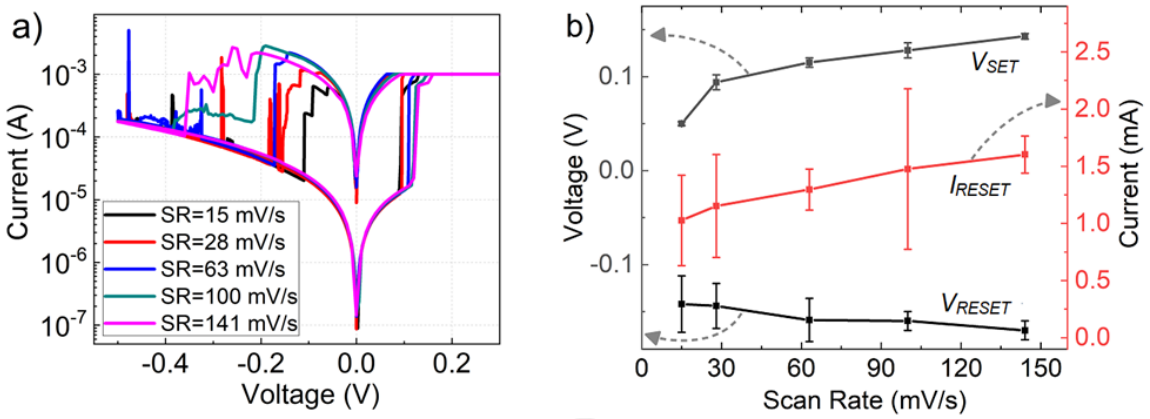


Figure 4.4: (a) I-V characteristics obtained at five different SRs for the same device, and (b) variation of V_{SET}, V_{RESET}, and I_{RESET} (right y-axis) with SR. As the SR increases, V_{SET}, V_{RESET}, and I_{RESET} are found to be increasing magnitude wise.

I_{RESET}, which is the minimum current required to switch from LRS to HRS, is an important parameter during the RESET cycle, in addition to the switching voltage. Another such parameter is the reset field, E_{RESET}. It is the electric field required to RESET the device and it equals the ratio of V_{RESET} to the device thickness (assuming uniform electric field over the entire thickness). The variations of switching voltages and I_{RESET} with SR are shown in figure 4.4(b), along with the device-to-device error calculated from 5 different devices. The magnitudes of both V_{RESET} (negative) and I_{RESET} significantly increased with SR. Also, E_{RESET} increased from 3.74 to 4.47 kV/cm when SR was changed from 15 to 141 mV/s. At low SRs, the migrating species inside $MAPbI_3$ will be under the influence of electric field for longer times and, thus, require less voltage to initiate the RS process [11]. The ON/OFF ratio remained close to 100 for all the five SRs that we have tested. Table 4.1 summarizes the extracted V_{SET}, V_{RESET}, E_{RESET}, and I_{RESET} for the different SRs. These are the median values ± standard deviation (SD) obtained from 5 different devices for each SR.

Table 4.1: Variation of memristor properties with SR (Values are written as the median ± standard deviation (SD))

SR (mV/s)	V_{SET} (V)	V_{RESET} (V)	E_{RESET} (kV/cm)	I_{RESET} (mA)
15	0.050±0.002	-0.142±0.030	3.74±0.789	1.026±0.396
28	0.094±0.008	-0.144±0.024	3.80±0.632	1.152±0.450
63	0.115±0.005	-0.159±0.023	4.18±0.605	1.296±0.180
100	0.128±0.008	-0.160±0.010	4.21±0.263	1.476±0.702
141	0.143±0.003	-0.170±0.010	4.47±0.263	1.602±0.162

4.4.2 Role of Compliance Current

The heat generated inside the device, directly related to the maximum current flowing through it, may lead to a change in film morphology and, hence, the device characteristics. This can be mitigated by adjusting the I_{CC} during characterization. The setting of an I_{CC} limit protects the device from hard breakdown and controls the size of the CF. A pristine memristor formed without setting any I_{CC} was used as a reference for our analysis. This reference device formed at 2.85 V, as can be seen from figure 4.5(a). However, resetting of this device was not possible even at low SRs and high negative voltages (as high as -3V). Because of the high current flow and the subsequent excess Joule heating, the device had likely failed and permanently became resistive. To realize the importance of I_{CC} during RESET, another HOIP memristor was formed with an I_{CC} of 1 mA, and different compliances were applied. It has been found that this device could not be RESET unless the compliance was raised to more than 1 mA (see figure 4.5(b)). These findings indicate that an applied field is not the only factor determining the rupture of the CF and the RESET process is more likely a combined effect of the electric field and Joule heating.

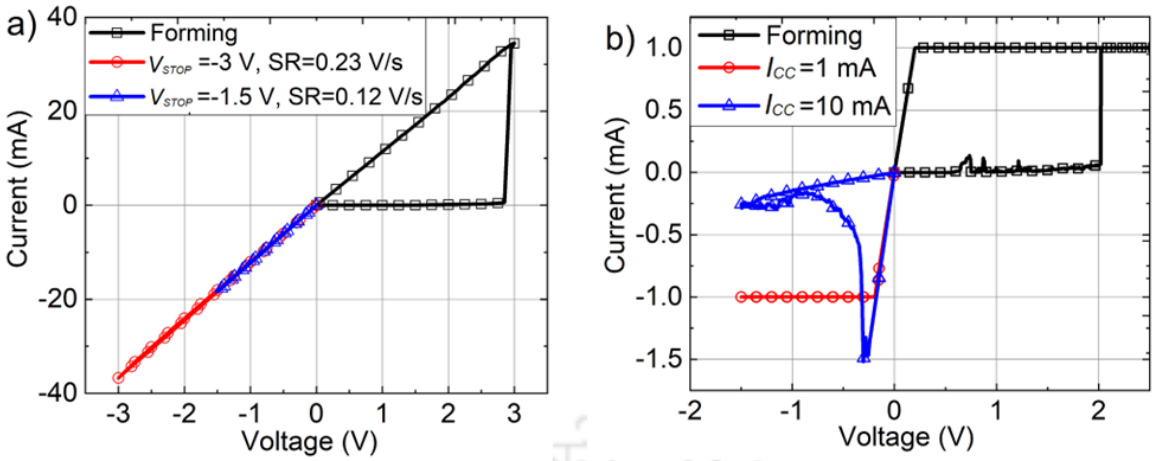


Figure 4.5: (a) Forming step of a device without any I_{CC} set. The subsequent attempts to RESET this device are also shown (red and blue plots). (b) I-V characteristics of the device formed with I_{CC} = 1mA and subsequent RESET steps. For such devices RESET happened only when I_{CC} was increased above 1mA.

Five I_{CC} values, ranging from 0.5 mA to 10 mA, were used to switch the same device and the corresponding I-V characteristics obtained are shown in figure 4.6(a). The corresponding variations of the switching parameters with I_{CC} are plotted in figure 4.6(b), along with the device-to-device error calculated from 5 different devices for each value of I_{CC}. It has been observed that while V_{RESET}, I_{RESET}, and ON/OFF ratio increase in magnitude with the increase in I_{CC}, V_{SET} remains nearly unaffected. These parameters, along with E_{RESET}, are shown in Table 4.2. It can be seen that when I_{CC} was changed from 0.1 mA to 10 mA, E_{RESET} increased from 3.68 kV/cm to 9.21 kV/cm. The I_{CC} likely affects the size and cross-section of the CF during the forming and SET processes [12]. A higher I_{CC} results in the formation of a stronger CF which requires more energy and power to get ruptured during the RESET. Consequently, V_{RESET}, E_{RESET}, and I_{RESET} increase with I_{CC} [13,14]. In addition, a stronger CF also results in a the higher LRS current which accounts for the observed increase in the ON/OFF ratio [13].

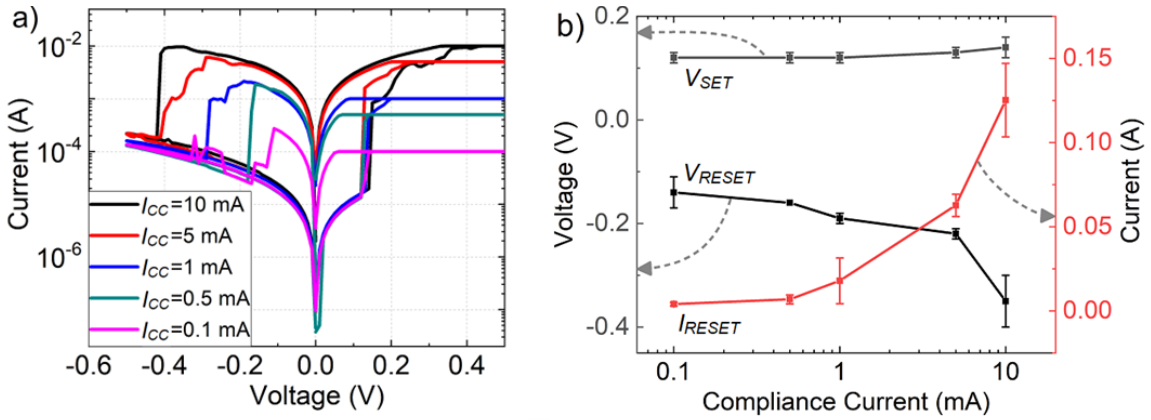


Figure 4.6: (a) I-V characteristics obtained by applying five different I_{CC} for the same device. (b) Variation of V_{SET}, V_{RESET}, and I_{RESET} (right y-axis) with I_{CC}. The magnitude of V_{SET}, V_{RESET} (negative values), and I_{RESET} increase with increase in I_{CC}.

Table 4.2: Variation of memristor properties with I_{CC} (Values are written as the median ± standard deviation (SD))

I_{CC} (mA)	V_{SET} (V)	V_{RESET} (V)	E_{RESET} (kV/cm)	I_{RESET} (mA)	ON/OFF ratio
0.1	0.12±0.01	-0.14±0.03	3.68±0.789	4.0±1.06	11±3
0.5	0.12±0.01	-0.16±0.00	4.21±0.000	6.8±2.63	71±11
1	0.12±0.01	-0.19±0.01	5.00±0.263	17.8±13.55	107±22
5	0.13±0.01	-0.22±0.01	5.79±0.263	62.7±6.60	536±81
10	0.14±0.02	-0.35±0.05	9.21±1.316	125.2±21.82	947±68

4.4.3 Role of Device Area

To understand the scaling trends of the HOIP memristors, devices with five different areas from 0.008 mm^2 to 0.2 mm^2 were fabricated and characterized. It has been found that $V_{FORMING}$ monotonically decreases with device area, as illustrated by the box and whisker plot in figure 4.7(a). Such a behaviour is expected since the probability of forming a CF increases as the device area increases [15]. On the other hand, both V_{SET} and V_{RESET} were observed to remain independent of the device area. Although CF gets ruptured during the RESET process, some portion of the filament always remains near the electrode interface(s) depending on the device structure and working mechanism. Once a

pristine device was electroformed, the subsequent switching processes take place from the already formed CF(s), irrespective of the device area. In fact, this is the reason behind the smaller switching voltages (as compared to the $V_{FORMING}$) after forming as there is no residual filament present in a pristine memristive device.

The residual filaments are not uniform every time the device switches, which leads to a distribution of the total HRS resistance (R_{HRS}) in any RS device with filamentary conduction. In addition to these filaments, R_{HRS} also depends on the rest of the device. As shown in figure 4.7(b), the R_{HRS} decreases sharply with device area (error bars show the variation from median values obtained from five different devices). However, no significant change was observed in the LRS resistance (R_{LRS}) as it was predominantly controlled by the fully formed CF(s) [16]. Consequently, the ON/OFF ratio decreases with device area, as shown by the red plot in figure 4.7(b).

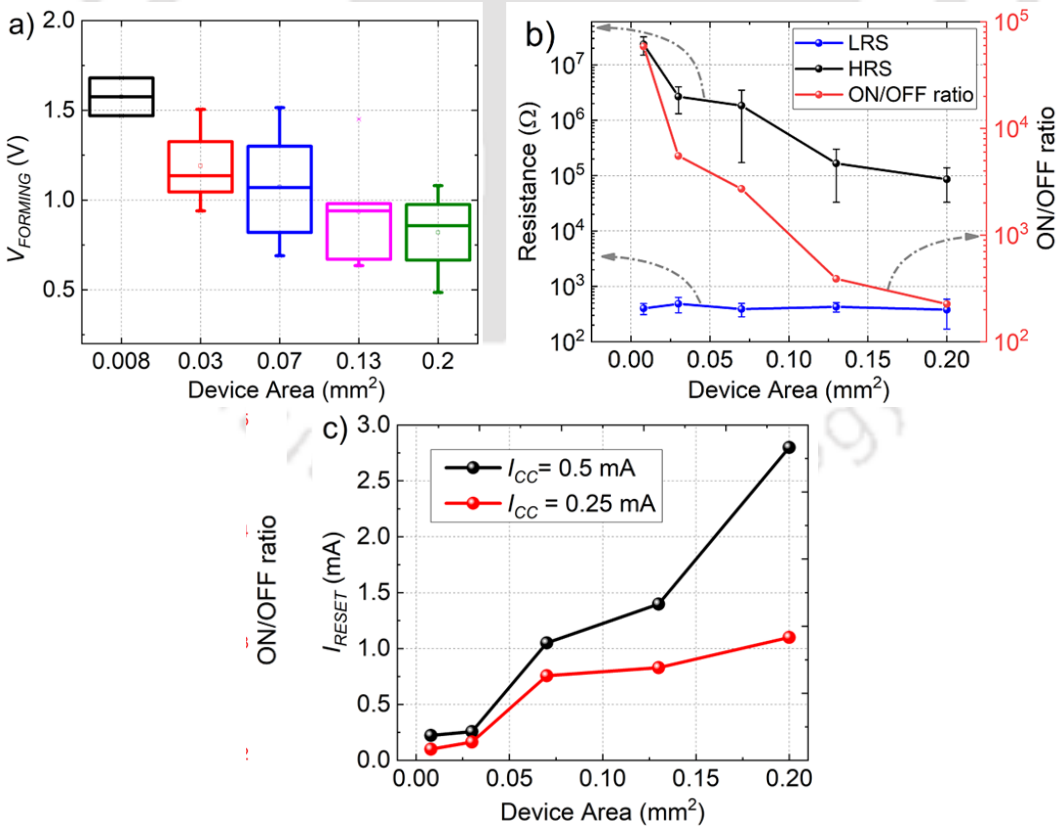


Figure 4.7: Variation of memristor parameters with device area; (a) $V_{FORMING}$ decreases with device area, (b) HRS resistance decreases with device area due to which ON/OFF ratio also drops (R_{LRS} does not change with area) and (c) I_{RESET} increases with device area, which aggravates with a higher I_{CC}.

We also observe that the I_{RESET} increases as the device area increases (see figure 4.7(c)). It was previously reported that a smaller device area leads to a smaller SET current threshold (I_{SET}), which in turn scales down the I_{RESET} [15,16]. In other words, the I_{RESET} can scale down with the device size, which aligns with our observation. As the peak power consumption of the device depends on I_{RESET}, small area devices are desirable. On the other hand, the power consumption can be also reduced by using a smaller I_{CC} which is associated with lower I_{RESET} for a given device area (see the red plot in figure 4.7(c)).

4.4.4 Cycle-to-Cycle and Device-to-Device Variation

To study the cycle-to-cycle variation in our device, we have applied 100 voltage sweep cycles with an SR 63 mV/s and an I_{CC} of 1 mA. These are the middle values for devices that we have discussed in the subsections 4.4.1 and 4.4.2 (see Tables 4.1 and 4.2) so that we achieve optimum values of operating voltages, I_{RESET}, and ON/OFF ratio. The I-V characteristics obtained are shown in figure 4.8(a) for 5 cycles. The spread of V_{SET} and V_{RESET} are shown in the histogram plot in figure 4.8(b) and these have median values of 0.17 V and -0.2 V respectively. The ON/OFF ratio decreases with successive sweeps applied. To examine the device-to-device variability, 10 out of 20 equal-area devices (0.002 cm^2) on a single substrate were chosen randomly. From their I-V characteristics, the statistical variations of V_{SET}, V_{RESET}, and I_{RESET} were calculated and plotted, as shown in figure 4.9(c), in the form of a cumulative distribution function (CDF). The CDF plots the parameter values on the x-axis against the fraction of all parameter values that are less than or equal to a particular parameter value. Mathematically, for any given value x and a random variable X, the CDF, $F_X(x)$, can be represented as shown in equation 4.1 below ($f_X(u)$ is the given function in case of a continuous variable u) [17].

$$F_X(x) = Probability[X < x] = \int_{-\infty}^{x} f_X(u)du \qquad (4.1)$$

In order to calculate this CDF distribution from the discrete parameter values obtained over multiple switching cycles, we have first arranged them in an increasing order and then divided each value by the sum of all the values smaller than that. From the slope of the CDF distributions, we can have a qualitative idea of the inherent device-to-device stochastic variation present in the HOIP memristors. From figure 4.8(c), we have found that V_{SET}, V_{RESET}, and I_{RESET} vary over the ranges of 0.15 V, 0.18 V, and 2.56 mA respectively.

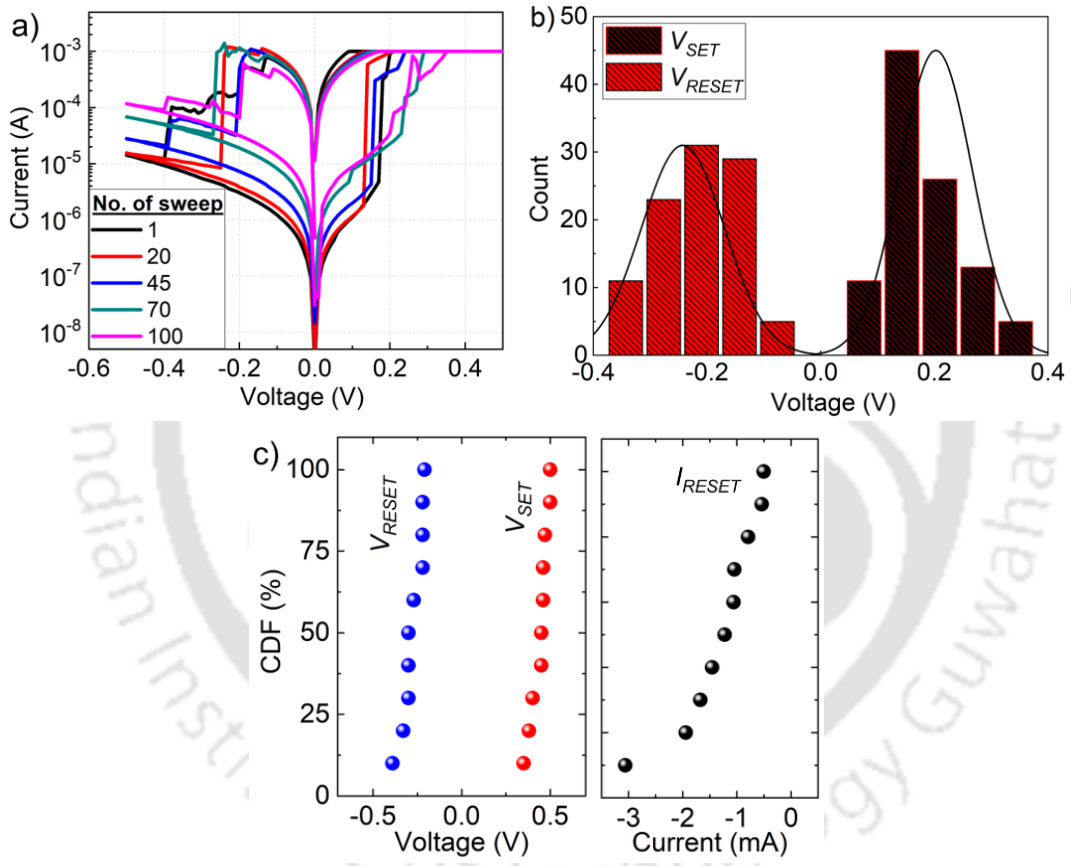


Figure 4.8: (a) I-V characteristics for a HOIP memristor repeated for 100 cycles with SR = 0.63 mV/s (I_{CC} equals 1 mA during SET and 5 mA during RESET), (b) histogram of V_{SET} and V_{RESET} for 100 repeated cycles on the same device, and (c) the device-to-device variation of V_{SET}, V_{RESET}, and I_{RESET} obtained from 10 different devices.

Ideally, for data storage applications, these parameter variations are expected to be as minimum as possible. However, emerging cyber security applications such as PUFs, true random number generators, etc. utilize the stochastic nature of the memristive devices [18,19]. While designing such an application, CDF is very useful to find the the

suitable threshold levels that may allow to operate a certain fraction of devices in a memristor array. For example, we can see from figure 4.8(c) that usage of a V_{RESET} of -0.3 V will RESET only 50% of devices in our case.

Application of fast voltage pulses is required to obtain cyclic endurance and data retention characteristics. Such data can help undertake a comprehensive stability and reliability analysis for practical applications as elaborated in the following section.

4.5 Voltage Pulse Characterization

Cyclic endurance is the maximum number of SET/RESET cycles a memristor can withstand while maintaining a predefined ON/OFF ratio. For this purpose, voltage pulse trains were applied to SET-READ-RESET-READ the memristor in sequence, as illustrated by the schematic in figure 4.9(a). A positive voltage pulse was used to SET the device first, followed by a small pulse of 50 mV to read the resistance state of the memristor (referred to as READ pulse here). After this, a negative pulse was applied to RESET the memristor, followed by another READ pulse to read the final resistance state. Figure 4.9(b) shows 20 such pulse trains (in red) with the corresponding current switching (in blue). To differentiate the HRS and LRS during the current switching, one single cycle is shown separately in the inset of figure 4.9(c). The two V_{READ} pulses and the corresponding currents in the figure are magnified from which it can be observed clearly that the current levels corresponding to the two READ pulses after the SET pulse and after the RESET pulse are 0.023 mA and 0.0046 mA respectively. This indicates that the SET and RESET pulses can switch the device resistance from 2.83 kΩ to 10.87 kΩ resulting in an ON/OFF ratio of nearly 5, which can be improved following the methods discussed in the next section.

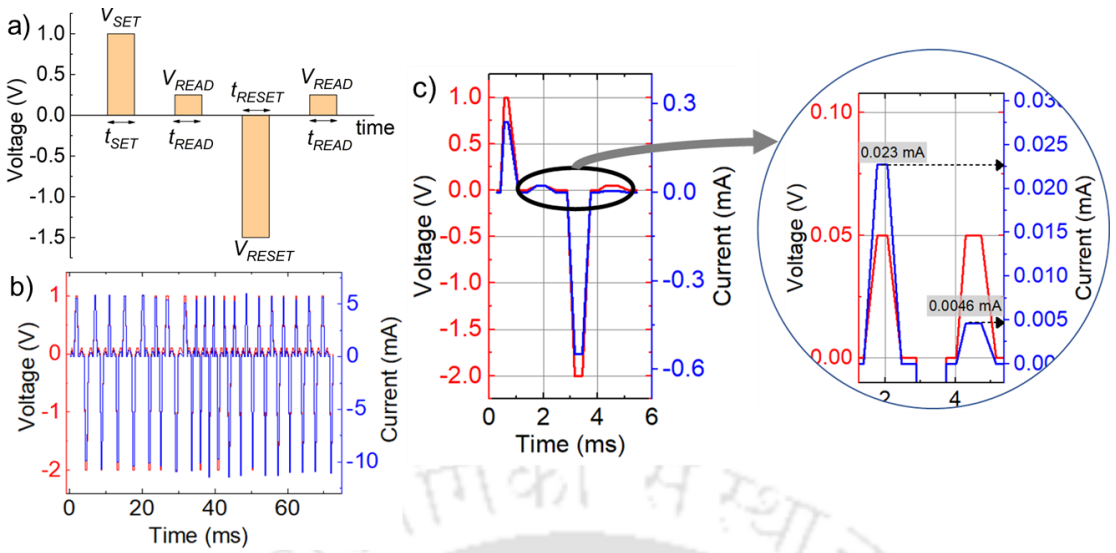


Figure 4.9: (a) The schematic of one single cycle of the voltage pulse train that was used to carry out the endurance characterization, (b) 20 such cycles applied to the HOIP memristor (in red) and corresponding current switching (in blue), and (c) one of the cycles is shown separately, where the currents during the two READ pulses shown in a magnified-view.

An inappropriate SET/RESET pulse may lead to the premature and permanent breakdown of the memristors. If the SET pulse is too strong, it causes a flow of excess current, resulting in the formation of toughened CFs that do not get ruptured by a normal RESET pulse. On the other hand, a too weak RESET pulse may not be sufficient to rupture the CF(s), and a too strong RESET pulse may lead to the permanent breakdown of the memristors [20]. The widths of SET/RESET pulses have similar effects on the CFs. The selection of adequate voltage pulses for endurance analysis is also important to achieve the desired ON/OFF ratio. It has been observed with our devices that the SET pulses do not have a significant impact on the LRS. We have varied the amplitude (V_{RESET}) and width (t_{RESET}) of the RESET pulse for 10 initial cycles and determined their optimum values based on the ON/OFF ratios obtained. The ON/OFF ratio was found to increase from 2.18 to 48.05 with increasing magnitude of V_{RESET} (from -2 to -5 V) and from 2.42 to 10.01 with increasing t_{RESET} (from 0.1 µs to 10 µs), as shown in figures 4.10(a) and (b) respectively.

Ideally, when used for memory applications, a memristor is preferred to have fast switching speed with small operating voltages for low power consumption. Switching

speed is defined as how fast the device can be switched from HRS to LRS and vice versa. However, operating the device with a small switching voltage requires electric field to be applied for longer duration of time to complete the formation/rupture of CF. This leads to a dilemma between the operating voltages for power optimization on one hand and the switching speed on the other, which is known as the *voltage-time dilemma* [9,21]. We have experimentally demonstrated this dilemma between the RESET pulse amplitude and width in order to optimize the ON/OFF ratio of the memristor. Therefore, a trade-off between these two parameters is necessary to achieve a certain ON/OFF ratio, i.e., a robust noise margin. From the ranges of V_{RESET} and t_{RESET} that we have varied, we have chosen V_{RESET}=-3 V and t_{RESET}=1 µs to test the endurance of our HOIP device. As shown in figure 4.10(c), we have obtained a consistent ON/OFF ratio of nearly 7 for at least 10^3 cycles.

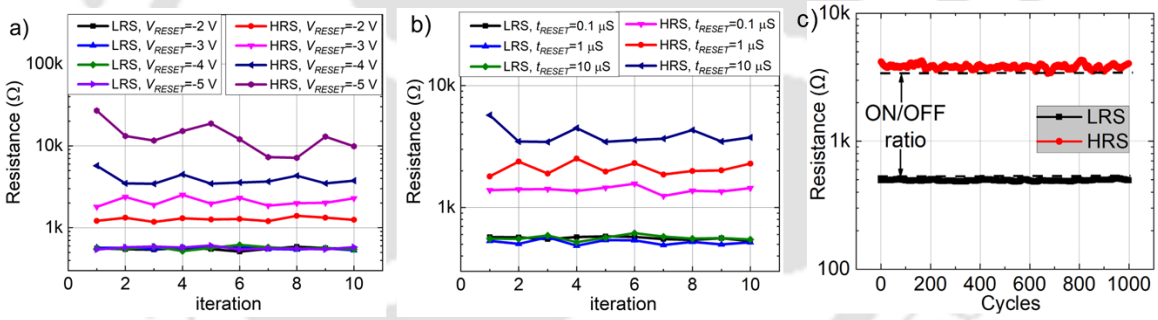


Figure 4.10: (a,b) Optimization of ON/OFF ratio by varying (a) RESET pulse and (b) RESET width for 10 cycles; the ratio tend to increase with increasing RESET pulse width, however, no significant change was observed when the SET pulse is varied. (c) Endurance characteristics for 10^3 cycles maintaining an ON/OFF ratio of 7.

4.6 Protocol for Memristor Characterization

Considering the voltage-time dilemma, we obtained the optimum performance from our device at an SR of 63 mV/s, I_{CC} of 1 mA, RESET pulse amplitude of -3 V, and pulse width of 1 µs. These parameters depend on various factors such as perovskite composition, thickness, and other interfacial layers in the memristor structure. However, based on the results obtained here, we have identified a generic protocol for the

characterization of HOIP memristors to achieve switching parameters that are closer to their optimum values.

4.6.1 Linearly Increasing Voltage Sweep Signal

(a) An SR between 1 mV/s to 1 V/s should be selected with an aim to observe significant hysteresis in the I-V characteristics.

(b) To start with, the smallest possible I_{CC} should be taken, which should be just high enough to allow the minimum current required to SET the memristor, i.e., I_{SET}. The I-V characteristics should be taken repeatedly with increasing I_{CC}, to find the right value, until the current modulation is observed. Once a consistent RS is observed, the ranges of SR and I_{CC} can then be varied to obtain better switching parameters.

(c) If the operating voltages are found to be too high, resulting in high power consumption, one may consider lowering the SR. A lower SR will, in general, reduce V_{SET}, V_{RESET}, and I_{RESET}. It should be noted that choosing too small a value for SR (indicating a slowly varying voltage signal) necessitates a significantly long time to complete the characterization. More importantly, this can result in a drop in the ON/OFF ratio.

(d) To obtain a higher ON/OFF ratio, one can increase the I_{CC} at which the device is allowed to go into its LRS. It may be noted, however, that this comes at the cost of a higher I_{RESET} and, consequently, a higher power consumption.

4.6.2 Voltage Pulse Characterization

(a) Generally, the voltage pulses used for endurance, retention, and other pulse characterizations are very fast signals whose pulse widths lie in the range of a few μs to tens of ns. To start with, one can choose any pulse width in that range and a pulse amplitude close to the range of V_{SET} and V_{RESET} values obtained from the linear voltage sweep method.

(b) To obtain RS using such fast voltage pulses, the pulse amplitude required is much higher than V_{SET} and V_{RESET} mentioned in the previous step. Therefore, with the fixed pulse width, the pulse amplitude can be increased until RS is visible in the memristor.

(c) To obtain a better ON/OFF ratio, the pulse amplitude and/or the pulse width can be increased one after the other or simultaneously until the desired ON/OFF ratio is achieved. However, the pulse amplitude and the width cannot be increased indefinitely, as higher pulse amplitude leads to higher power consumption, and larger pulse width makes the memristor not suitable for fast switching applications. This also leads to unstable HRS with each repeated cycle, making the switching inconsistent. In short, the voltage-time dilemma has to be addressed carefully while optimizing with the voltage pulse characterization.

4.7 Flexible HOIP Memristors

To expand the applicability of the HOIP memristors into flexible electronics, we fabricated them on flexible polyethylene terephthalate **(**PET) substrates. The device structure and the fabrication procedure adopted were the same as those for glass substrate. For the convenience of spin coating, the PET substrate was stuck on a glass slide using scotch tape. The device schematic is shown in figure 4.11(a). The $MAPbI_3$ layer had a thickness a 342 nm, which is the median value of 9 readings taken at different positions on the substrate using a profilometer. The XRD plot of $MAPbI_3$ film on PET shows that the film is highly crystalline with a three-dimensional phase conformation at the peak of 14^o, corresponding to the (110) plane (see figure 4.11(b)). The broad peak at ~26^o corresponds to PET [22].

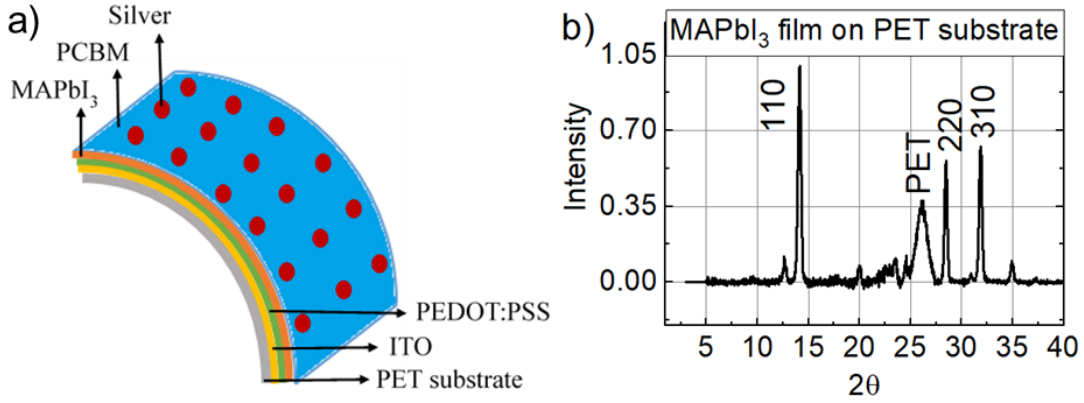


Figure 4.11: (a) Schematic of the flexible memristor device. (b) XRD spectrum of the $MAPbI_3$ film coated on the PET substrate, showing formation of desired (110) perovskite phase at 14°.

The FESEM and AFM images of the $MAPbI_3$ films coated on glass and PET substrate are shown in figure 4.12 and 4.13 respectively. The FESEM image of the film coated on rigid glass substrate clearly shows polycrystalline grains (see figure 4.12(a)). The average grain size was found to be 155 nm measured from 100 grains in an area of 1.8x1.3 μm^2 using ImageJ software, where the grain size ranges between 51.5 nm, and 338.2 nm (see the grain size distribution in figure 4.12(b)). The film has an average RMS roughness of 1.46 nm, as obtained from the AFM image of 1x1 μm^2 scan area (see figure 4.12(c)).

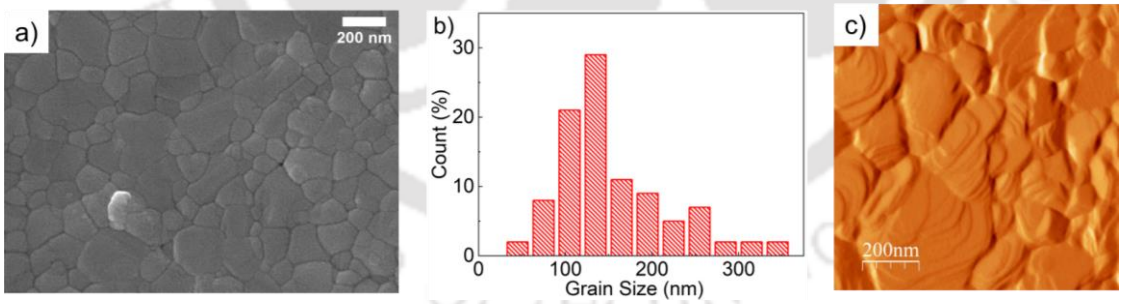


Figure 4.12: Morphological characterization of the fabricated $MAPbI_3$ films on ITO coated glass substrates. (a) FESEM image taken over an area of 1.8x1.3 μm^2 with a scale of 200 nm. (b) The grain size distribution for 100 grains. The average grain size is 155 nm. (c) AFM image taken over an area of 1x1 μm^2. The average RMS roughness is 1.46 nm.

From the FESEM image of the $MAPbI_3$ film coated on flexible PET substrate (see figure 4.13(a)), the average grain size has been found to be 125 nm (measured from 100 grains in an area of 1.8x1.3 μm^2), which is slightly higher than that for glass substrate. The distribution in the figure 4.13(b) shows the grain sizes ranging between 38.9 nm, and

348.6 nm. From the AFM image, an RMS surface roughness of 1.51 nm was obtained over an area of 1x1 μm^2.

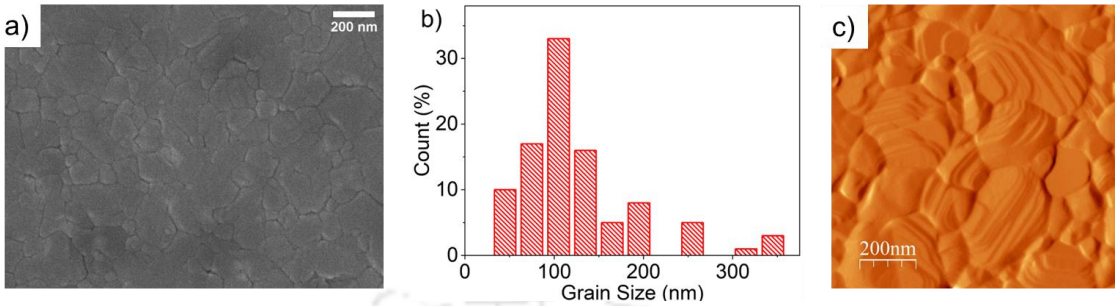


Figure 4.13: Morphological characterization of the fabricated $MAPbI_3$ films on ITO coated PET substrates. (a) FESEM image taken over an area of 1.8x1.3 μm^2 with a scale of 200 nm. (b) The grain size distribution for 100 grains. The average grain size is 125 nm. (c) AFM images taken over an area of 1x1 μm^2. The average RMS roughness is 1.9 nm.

4.7.1 I-V Characteristics

The I-V characteristics were taken by applying a linear voltage sweep, with a compliance limit of 1 mA. The representative device characteristics, given in figure 4.14(a), show a $V_{FORMING}$ of 0.6 V, a V_{SET} of 0.45 V, a V_{RESET} of -0.28 V, and an ON/OFF ratio of 610. The RS behaviour was repeatable, as shown in the endurance plot in figure 4.14(c). The inset of this figure shows a single pulse train applied to realize the endurance characteristics. The device maintained an ON/OFF ratio of 98 for 1000 such cycles. The HRS and LRS could be retained with a consistent ON/OFF ratio of 103 for 1350 seconds, measured at 100 mV (see figure 4.14(d)). The ON/OFF ratio obtained in case of pulse characterization is comparatively lesser (~6 times) that that in case of characterization using linear voltage sweep. It can be improved by using a higher pulse width or a higher pulse amplitude as discussed in section 4.5. However, this improvement in the ON/OFF ratio comes at the cost of device speed and/or power consumption.

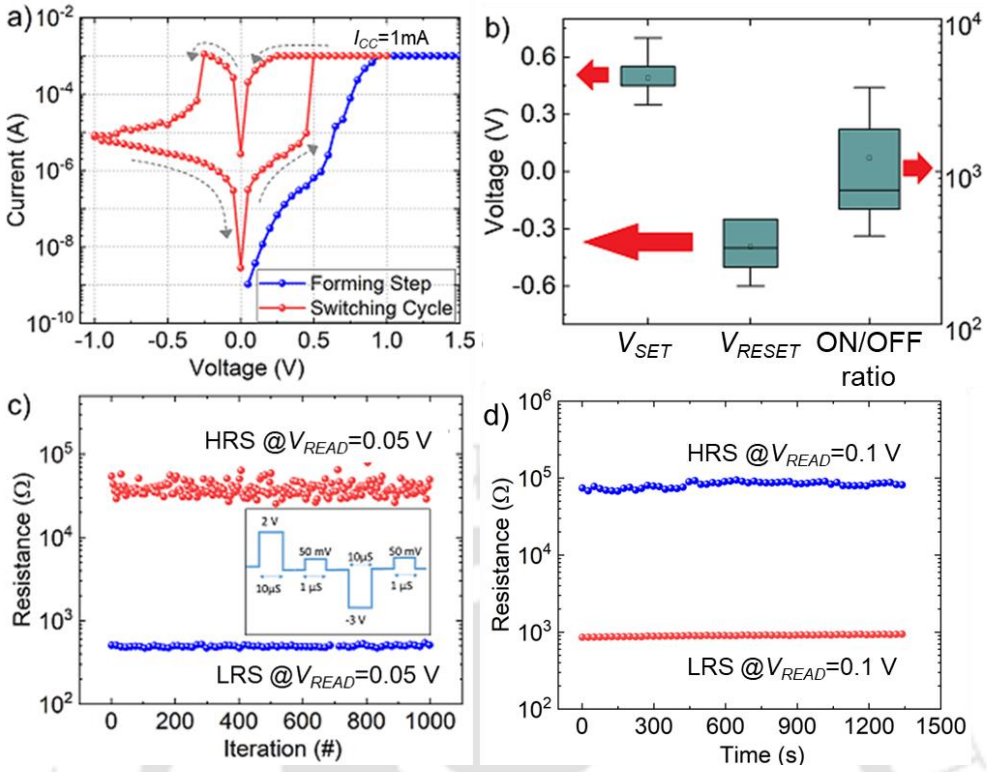


Figure 4.14: (a) I-V plots of flexible HOIP memristors. (b) Variation of V_{SET}, V_{RESET}, and ON/OFF ratio from 10 different devices. (c) Endurance plot showing a consistent ON/OFF ratio of 98 for 1000 cycles. (d) Retention plot showing ON/OFF ratio of 103 for 1350 seconds, measured at 100 mV.

4.7.2 Effect of Mechanical Stress

I-V characterization was carried out under applied tensile stress to understand the bending effect on the switching performance. To apply stress to the device during measurement, a simple setup has been made as shown in figure 4.15(a). A geometrical schematic used for bending radius calculation is shown in this figure 4.15(b). The degree of bending is defined in terms of bending radius (R_b) and was calculated by the equation (4.2) below, where, a and b are the height and the distance between two edges of the substrate during bending.

$$R_b = \frac{b^2}{8a} + \frac{a}{2} \qquad (4.2)$$

The device performance has been compared for two different bending radii of 1.3 cm and 0.9 cm for the forming and switching steps as shown in figure 4.15(c) and (d) respectively.

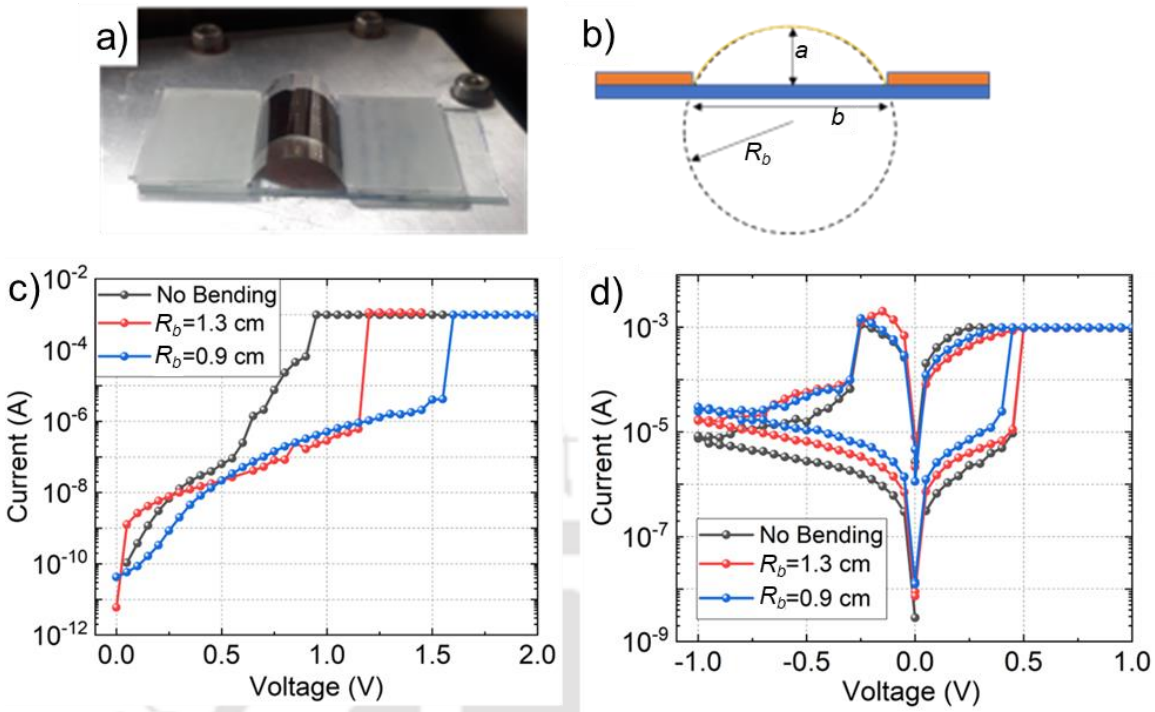


Figure 4.15: (a) A photograph of the measurement setup to characterize the devices under stress. (b) A geometrical schematic of the device in the bending state. (c) Variation of forming step with different applied stress; $V_{FORMING}$ tends to increase with bending. (d) Variation of switching cycles with applied stress. While the ON/OFF ratio tends to reduce with increasing bending radius, only a small change is observed in the values of V_{SET} and V_{RESET}.

The $V_{FORMING}$ was observed to increase with an increase in bending, being equal to 1.15 V for R_b=1.3 cm and 1.55 V for R_b=0.9 cm. On the other hand, V_{SET} and V_{RESET} did not change significantly in the range of stress applied, as seen from the I-V plots in figure 4.15(d). However, the ON/OFF ratio tends to reduce with increasing bending radius, which may be due to the degradation of the HOIP layer and the subsequent decrease in R_{HRS}. Table 4.3 compares the performance of our device with similar flexible HOIP devices found in literature. From the table, we can see that our flexible memristors show promising results, which can be improved with further film optimization and device engineering.

Table 4. 3: Bending radii and ON/OFF ratio of various flexible HOIP memristors

Device Structure	R_b	ON/OFF ratio	Ref.
PET|ITO|PEDOT:PSS|$CH_3NH_3PbI_3$|PCBM|Ag	13 mm	112	Our devices
	9 mm	96	
Au|$MAPbI_3$|ITO|PET	15 mm	9	[10]
PET|ITO|PMMA|PeQDs:PMMA|PMMA|Ag	7 mm	100	[23]
PET|ITO|$CH_3NH_3PbI_3$|MoO_3|Ag	9.2 mm	15	[24]
Ag|$CH_3NH_3PbI_3$|Pt|COP	5 mm	10^5	[25]
PET|ITO|$(CH_3NH_3)_2PbI_2(SCN)_2$|Al	8.8 mm	10^3	[26]

The next chapter presents two different types of RS obtained from the same 3D HOIP memristor under different operating conditions and a novel approach to simulate these HOIP memristor characteristics.

4.8 Summary

Using a simple, low-cost, and low-temperature solution processing technique, we have demonstrated consistent RS in $MAPbI_3$-based memristive devices. Devices fabricated using toluene as an antisolvent showed superior performance owing to improved perovskite film morphology. Toluene decreases the solubility of perovskite precursors in DMF and creates nucleation centers uniformly over the entire film which helps in fast crystallization of perovskite film. The effects of measurement procedure and device area on the memristor performance have been studied. It has been found that higher values of I_{CC} and SR lead to higher switching voltages and I_{RESET}. The reduction in switching voltages with slower SR may be due to the migrating species being under the influence of an applied electric field for longer times. A higher I_{CC} leads to the formation of a stronger conductive filament that requires larger RESET power to get ruptured. On the other hand, selecting very small values of I_{CC}, pulse amplitude and pulse width may lead to improper switching of the memristor that results in reduced reliability of the

memristors. The scaling of the device has little effect on the LRS, while HRS decreases rapidly as device area decreases.

Based on these findings we formulated a characterization protocol that can be useful for extracting the optimum performance for single-layer HOIP memristors sandwiched between an HTL and an ETL. However, this protocol is quite general in nature and can be employed for any other memristor structure based on HOIPs and other related materials. The low-temperature fabrication method enabled us to use the same device structure and fabrication process on flexible substrates. The $MAPbI_3$ based memristors fabricated on flexible PET substrate showed repeatable resistive switching action even at a bending radius as small as 0.9 cm. No significant change in V_{SET} and V_{RESET} has been observed with bending. The resistive switching maintains an ON/OFF ratio of ~100 for an endurance stress of >1000 cycles and both LRS and HRS were retained for 1350seconds. However, $V_{FORMING}$ and ON/OFF ratio of these devices have been found to deteriorate with increasing stress.

4.9 References

[1] M. Konstantakou *et al.*, "Anti-solvent crystallization strategies for highly efficient perovskite solar cells," Crystals (Basel), vol. 7, no. 10, p. 291, 2017.
[2] T. Bu *et al.*, "Synergic interface optimization with green solvent engineering in mixed perovskite solar cells," Advanced Energy Materials, vol. 7, no. 20, p. 1700576, 2017.
[3] S. Paek *et al.*, "From nano- to micrometer scale: The role of antisolvent treatment on high performance perovskite solar cells," Chemistry of Materials, vol. 29, no. 8, pp. 3490–3498, 2017.
[4] K. Kara *et al.*, "Solvent washing with toluene enhances efficiency and increases reproducibility in perovskite solar cells," RSC Advances, vol. 6, no. 32, pp. 26606–26611, 2016.
[5] S. Kavadiya *et al.*, "Crystal reorientation in methylammonium lead iodide perovskite thin film with thermal annealing," Journal of Materials Chemistry A, vol. 7, no. 20, pp. 12790–12799, 2019.
[6] Y. Sun *et al.*, "Competition between metallic and vacancy defect conductive filaments in a $CH_3NH_3PbI_3$-based memory device," Journal of Physical Chemistry C, vol. 122, no. 11, pp. 6431–6436, 2018.
[7] Y. Ren *et al.*, "Cycling-induced degradation of organic-inorganic perovskite-based resistive switching memory," Advanced Materials Technologies, vol. 4, no. 1, p. 1800238, 2019.

[8] H. Y. Lee *et al.*, "Low power and high speed bipolar switching with a thin reactive Ti buffer layer in robust HfO_2 based RRAM," in 2008 IEEE International Electron Devices Meeting (IEDM), pp. 1–4, 2008.
[9] C. Schindler *et al.*, "Electrode kinetics of Cu–SiO_2-based resistive switching cells: Overcoming the voltage-time dilemma of electrochemical metallization memories," Applied Physics Letters, vol. 94, no. 7, p. 072109, 2009.
[10] C. Gu and J.-S. Lee, "Flexible hybrid organic-inorganic perovskite memory," ACS Nano, vol. 10, no. 5, pp. 5413–5418, 2016.
[11] E. Yoo *et al.*, "Bifunctional resistive switching behavior in an organolead halide perovskite based Ag/$CH_3NH_3PbI_{3-x}Cl_x$/FTO structure," Journal of Materials Chemistry C, vol. 4, no. 33, pp. 7824–7830, 2016.
[12] B. Butcher *et al.*, "High endurance performance of 1T1R HfO_x based RRAM at low (<20μA) operative current and elevated (150°C) temperature," in 2011 IEEE International Integrated Reliability Workshop Final Report, pp. 146–150, 2011.
[13] C. Rohde *et al.*, "Identification of a determining parameter for resistive switching of TiO_2 thin films," Applied Physics Letters, vol. 86, no. 26, p. 262907, 2005.
[14] S. Larentis *et al.*, "Resistive switching by voltage-driven ion migration in bipolar RRAM—part II: Modeling," IEEE Transactions on Electron Devices, vol. 59, no. 9, pp. 2468–2475, 2012.
[15] R. Tetzlaff, Ed., Memristors and Memristive Systems. New York, NY: Springer New York, 2014.
[16] H. S. P. Wong *et al.*, "Metal–Oxide RRAM," Proceedings of the IEEE, vol. 100, no. 6, pp. 1951–1970, 2012.
[17] J. S. Arora, "Introduction to Optimum Design," Elsevier Science & Technology, third edition, 2004.
[18] R. A. John *et al.*, "Halide perovskite memristors as flexible and reconfigurable physical unclonable functions," Nature Communications, vol. 12, no. 1, p. 3681, 2021.
[19] Y. Sun and D. Wen, "Logic function and random number generator build based on perovskite resistive switching memory and performance conversion via flexible bending," ACS Applied Electronic Materials, vol. 2, no. 2, pp. 618–625, 2020.
[20] Y. Y. Chen *et al.*, "Balancing SET/RESET Pulse for $>10^{10}$ Endurance in HfO_2/Hf 1T1R Bipolar RRAM," IEEE Transactions on Electron Devices, vol. 59, no. 12, pp. 3243–3249, 2012.
[21] H. Schroeder *et al.*, "Voltage-time dilemma of pure electronic mechanisms in resistive switching memory cells," Journal of Applied Physics, vol. 107, no. 5, p. 054517, 2010.
[22] X. Liu *et al.*, "A high-performance UV/visible photodetector of Cu_2O/ZnO hybrid nanofilms on SWNT-based flexible conducting substrates," Journal of Materials Chemistry C, vol. 2, no. 44, pp. 9536–9542, 2014.
[23] K. Yang *et al.*, "A facile synthesis of $CH_3NH_3PbBr_3$ perovskite quantum dots and their application in flexible nonvolatile memory," Applied Physics Letters, vol. 110, no. 8, p. 083102, 2017.
[24] Z. Xu *et al.*, "To probe the performance of perovskite memory devices: defects property and hysteresis," Journal of Materials Chemistry C, vol. 5, no. 23, pp. 5810–5817, 2017.
[25] J. Choi *et al.*, "Enhanced endurance organolead Halide perovskite resistive switching memories operable under an extremely low bending radius," ACS Applied Materials & Interfaces, vol. 9, no. 36, pp. 30764–30771, 2017.

[26] X.-F. Cheng *et al.*, "Pseudohalide-induced 2D $(CH_3NH_3)_2PbI_2(SCN)_2$ perovskite for ternary resistive memory with high performance," Small, vol. 14, no. 12, p. 1703667, 2018.

CHAPTER 5

Multifunctional RS and SPICE Simulation of HOIP Memristors

Contents

5.1 Introduction

Based on the properties of active, interfacial, and metal layers in a memristive device, various types of RS are possible [1,2]. These include BRS, URS, complementary resistive switching (CRS), and their combinations. Also, depending on the device area and thickness, different switching mechanisms can be obtained from the same structure [3]. Thus, the same structure could be tuned as per the requirement of a specific application. For example, while URS is essential for a memory with One Diode One Memristor (1D1M) configuration, the CRS is inherently resistant to sneak current issues in crossbar circuits. Interestingly, a unique multifunctional RS (MRS) behaviour has been observed in our $MAPbI_3$ devices. We found that this MRS can be controlled by (a) polarity of the electric field and (b) I_{CC}.

The ability to simulate the I-V characteristics of memristors is essential to incorporate them into circuits and systems. As discussed previously in chapter 2, several analytical models have been proposed for memristor behavior, which can be useful for this purpose [4-9]. However, these models are not generic in nature and, as such, cannot mimic the memristive action in a wide range of materials and device structures. In this chapter, we developed a strategy to mimic the I-V characteristics of our memristors by SPICE simulation using fitting parameters extracted from experimental data. We obtained a per-cycle mean error of ~7% for the data fit to our devices. The proposed simulation algorithm has been inspired by the Yakopcic model of memristor, which is also SPICE-based [10].

5.2 Multifunctional Resistive Switching

Occurrences of multiple RS in the same cell were reported with various devices based on materials such as TiO_2, $BiFeO_3$, ZnS-Ag/$CuAlO_2$, MoS_2, CeO_2, etc. [11–14]. However, most of them needed either memristive devices connected anti-serially (see figure 5.1(a)) or multiple active layers stacked between electrodes (see figure 5.1(b)),

which are associated with reduced device volume density in a crossbar architecture. In order to address this device density issue, several attempts were made to demonstrate MRS intrinsic to a single MIM structure with materials such as $SrTiO_3$, TiO_2, Ta_2O_5, HfO_2, etc. [15-18]. However, no such reports have been found on HOIP memristors to date.

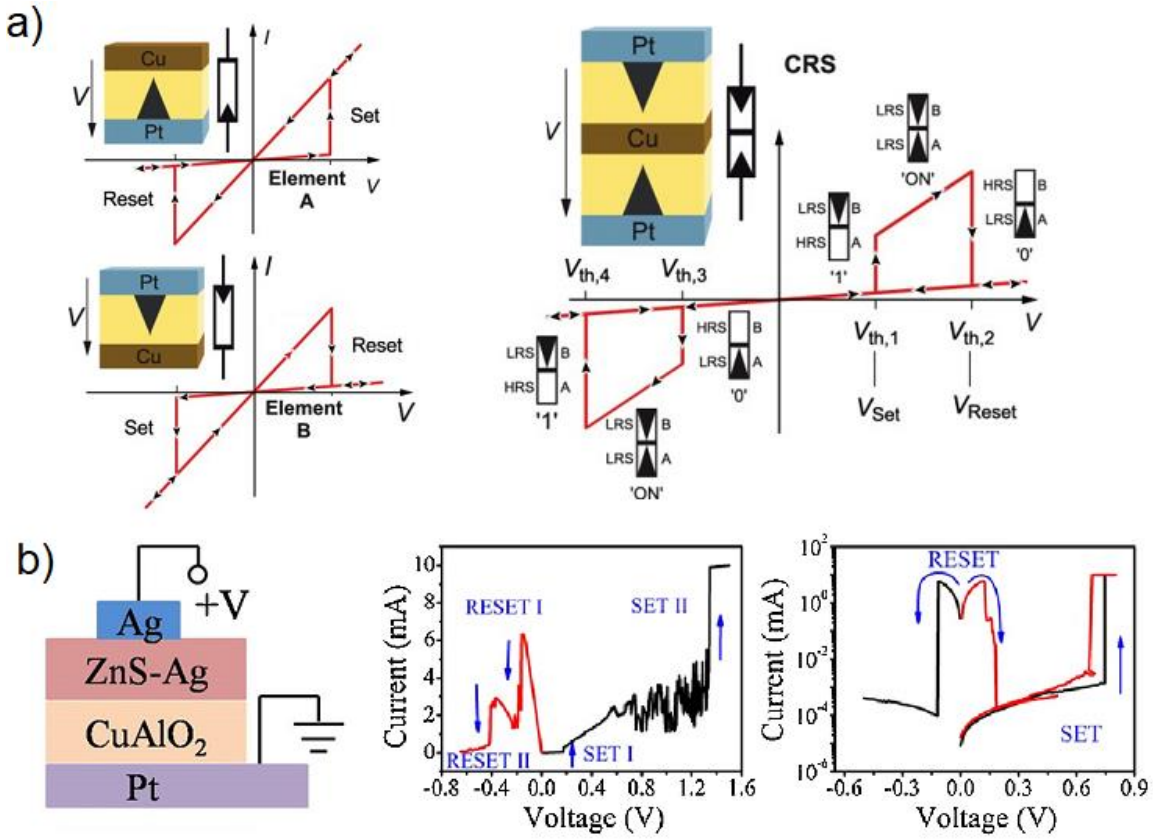


Figure 5.1: (a) Examples of the BRS and CRS characteristics along with the device schematics [19]. (b) The schematic of a two-layer device and the BRS and URS characteristics obtained from it [11].

5.3 Multiple BRS in HOIP Memristors

5.3.1 Two Types of BRS in the Same Device

By controlling the I_{CC} during the SET process, two types of switching can be obtained with the same $MAPbI_3$ memristor, as shown in figure 5.2. These two types of switching, referred to as Type A and Type B here, differ with respect to their corresponding V_{SET} and V_{RESET} values. For Type A switching (see figure 5.2(a)), a positive voltage was applied to TE, keeping BE grounded, with an I_{CC} of 1 mA during the

SET process. Here, the device switched from HRS to LRS (step 1) at V_{SET} = 0.47 V and switched back to HRS (step 3) at V_{RESET} = -0.32 V. An ON/OFF ratio of 369.91, measured at a V_{READ} of 50 mV before and after the SET process, was obtained for this type of switching. In contrast, with a lower I_{CC} (0.5mA) and a negative voltage sweep applied in HRS, BRS of Type B has been obtained (see figure 5.2(b)). Here, the device switches from HRS to LRS (step 1) under a negative field and switches back to HRS (step 3) under a positive field. The values of V_{SET}, V_{RESET}, and ON/OFF ratio for Type B switching were -0.32 V, 0.42 V, and 5882.32, respectively.

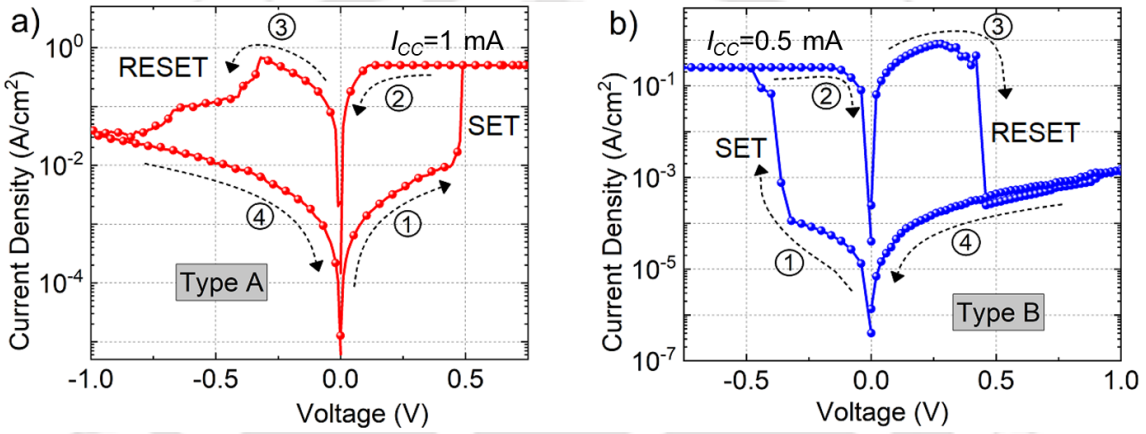


Figure 5.2: J-V characteristics of the devices corresponding to (a) Type A and (b) Type B switching.

It is important to note that the ON/OFF ratio for Type B switching is >15 times higher than that for Type A switching. This could be due to the involvement of Joule heating in the RESET process in the case of Type B switching [20]. Here, the large heat generated during the Type B RESET helps the rupture of CF to a greater extent. This allows the device to reach a comparatively larger HRS (1470.58 kΩ), which in turn yields a higher ON/OFF ratio. The parameters for both types of switching are summarised in table 5.1. The difference in the HRS of the two types of switching is evident from the table, whereas the LRS in both cases are comparable.

Table 5.1: Switching parameters corresponding to the two types of switching

Switching Parameters	Type A switching	Type B switching
V_{SET} (V)	0.47	-0.32
V_{RESET} (V)	0.32	0.42
I_{RESET} (mA)	1.36	1.63
R_{HRS} (kΩ)	40.69	1470.58
R_{LRS} (kΩ)	0.11	0.25
ON/OFF ratio	369.91	5882.32

5.3.2 Effect of STOP Voltage

Apart from the variations in V_{SET}, V_{RESET}, and ON/OFF ratio for the two types of switching, a striking difference can be observed in their RESET cycles (see figures 5.2 and 5.3). In the case of Type A switching, the device resistance changed gradually after the V_{RESET} and reached the R_{HRS}, depending on the maximum applied negative voltage or the V_{STOP}. In contrast, the RESET step of Type B switching was abrupt and the device resistance remained nearly constant for voltages higher than V_{RESET}. The insets of figure 5.3(a) and (b) show the respective changes in device current during RESET process in the linear scale. To understand the role of V_{STOP}, we have taken a device in its LRS initially and varied V_{STOP} from -0.5 V to -1 V (positive for Type B) in the subsequent switching cycles. In the case of Type A switching, it was found that the R_{HRS} of the device was dependent on the V_{STOP} applied in the previous cycle. Figure 5.3(a) shows that, in the first cycle (blue coloured plot), a V_{STOP} of -0.5 V results in a HRS current of 32.47 μA in the corresponding SET cycle. In the subsequent cycles, V_{STOP} values of -0.75 V and -1 V result in comparatively higher R_{HRS} (corresponding currents of 13.79 μA and 6.58 μA, respectively) in their corresponding SET cycles. When V_{STOP} was increased every cycle, each subsequent SET cycle started with a higher R_{HRS} than the previous one. Such

intermediate resistance states (IRS) may facilitate realization of multilevel switching in our HOIP memristor. In contrast, such a V_{STOP}-dependent multilevel switching was not present for Type B switching, as shown in figure 5.3(b). These observations indicate that the two types of switching involve two different mechanisms.

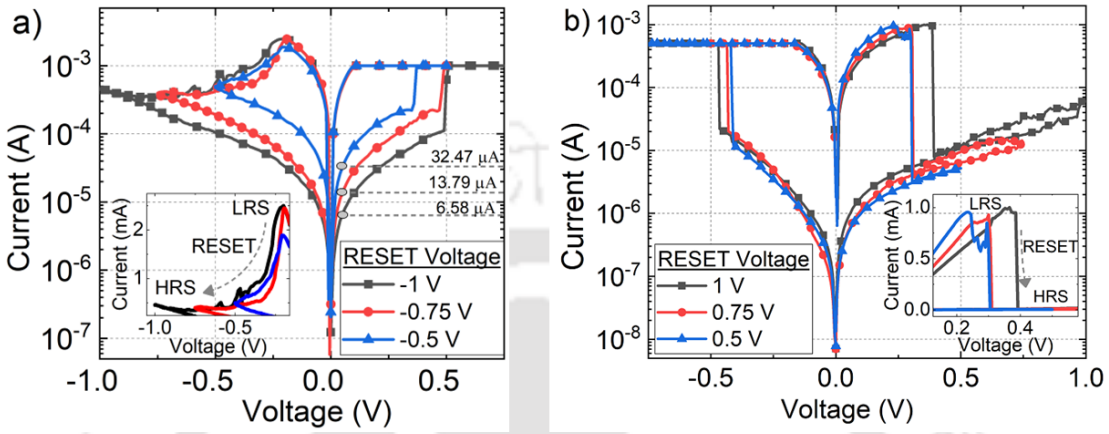


Figure 5.3: Three cycles of I-V characteristics with different V_{STOP} values for (a) Type A and (b) Type B switching. The insets show the respective changes in device resistance during RESET process in the linear scale.

5.3.3 Endurance and Retention of the Two BRSs

The endurance of both Type A and Type B RS was tested by applying voltage pulses (pulse width of 1 µs) and measuring the corresponding a change of device resistance state) nor too low (which can be affected by random noise resistance states with a V_{READ} pulse. The selection of an optimum read pulse is important for any memristive device. Its magnitude should be chosen such that it is neither too high (which can lead to signal in a practical circuit). We found that a V_{READ} of 50 mV is reasonable for our HOIP devices which were tested using low-noise cables (Keithley 237-ALG-2). Figure 5.4(a) shows the endurance plot obtained from 1000 cycles for Type A switching. However, Type B switching exhibited cyclic endurance only for 500 cycles, as shown in figure 5.4(b). This inferior cyclic endurance could be due to thermal effects as reported in the literature [21] and is discussed in the following section. The insets of the respective figures show the cycle-to-cycle variation of the HRS and LRS in the form of CDF. The

difference between the tails of the two CDF distributions is the window margin (WM), which is the actual noise margin between the HRS and LRS.

As shown in the insets of figures 5.4 (a) and (b), the WM for Type A and that for Type B switchings are 9.02 and 147.29, respectively. These WMs are lesser than the ON/OFF ratios obtained from linear voltage sweep and can be improved by optimizing the amplitude and width of the pulses, as discussed previously in section 4.5. Figures 5.4(c) and 5.4(d) show the retention plots for both types of switching (V_{READ} = 50mV). We have taken the maximum number of sample points during the retention measurement (i.e., 4096 points) limited by our equipment, which lasted for 3270 seconds. Thus, the actual retention time will be higher than this time. These plots show that the R_{HRS} and R_{LRS} vary over a range of 11.7 kΩ and 34 Ω, respectively, in the case of Type A switching. The corresponding variations are 500 kΩ and 280 Ω, respectively, in the case of Type B switching.

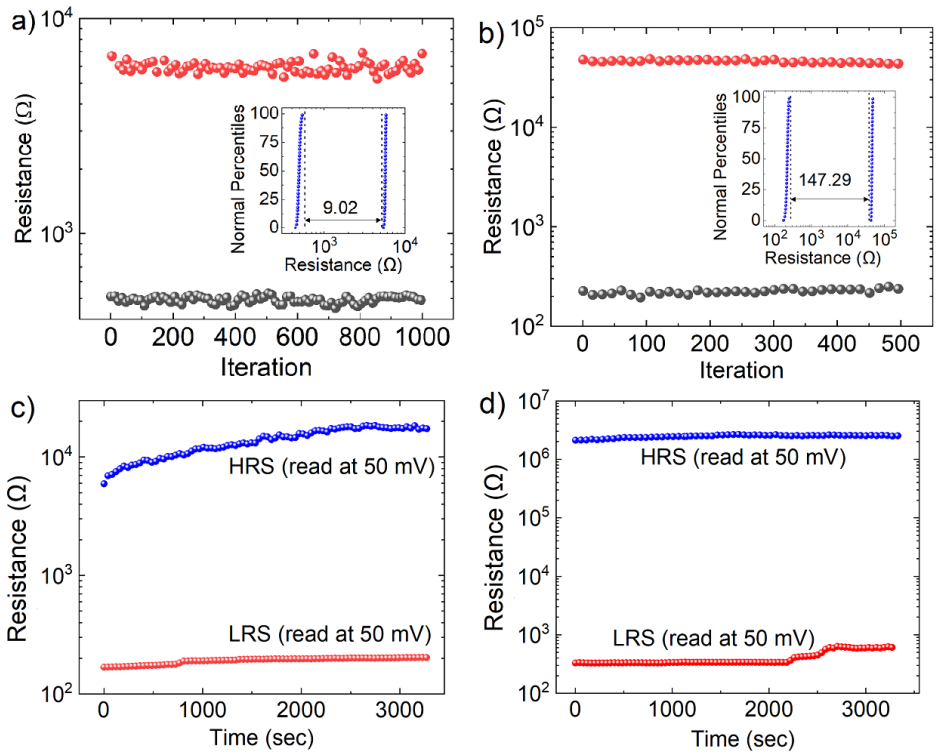


Figure 5.4: (a, b) Endurance plots corresponding to (a) Type A (1000 cycles) and (b) Type B (500 cycles) switching. The respective insets demonstrate the window margins of HRS and LRS calculated from the CDF distributions. (c, d) Retention plots for 3270 seconds corresponding to (c) Type A and (d) Type B switching.

5.3.4 CRS behaviour in HOIP Memristor

For practical data storage applications, these memristors have to be integrated in the form of a crossbar array. Such arrays allow the realization of high device density with individual cell area being as low as $4F^2$ (in comparison, conventional DRAM/SRAM cells require areas ranging from $6F^2$ to $140F^2$), where F is the minimum feature size (see figure 5.5(a)) [22]. However, a common problem in such memristor arrays is the sneak-current, which is an undesired current through unselected devices. In the schematic in figure 5.5(b), a possible case of the sneak-current path is shown by the red dashed lines in a 3x3 crossbar array, and its equivalent circuit is shown in figure 5.5(c). The sneak-current depends on the components of each cell in the array and aggravates in case of low resistance paths [23]. CRS is one of the solutions to this problem, in addition to the other methods such as the use of selector devices and biasing the unselected cells. As we have already seen in figure 5.1(a), in the case of CRS I-V characteristics, the device is always in a HRS for the low voltage regime (read-window) [24]. Such high resistance during the read-window minimizes the current sneaking through the unselected devices. Usually, this CRS behaviour is achieved by connecting two normal memristor cells anti-serially. However, with a proper selection of voltage polarities and I_{CC}, followed by the optimization of switching voltages, R_{HRS}, and R_{LRS}, we demonstrate CRS behaviour from a single HOIP memristor cell.

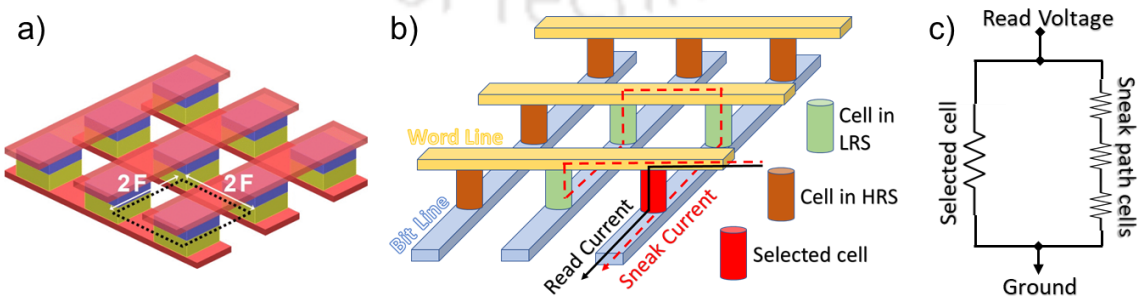


Figure 5.5: (a) Schematic of a crossbar array showing minimum cell area of $4F^2$, where F is the minimum feature size of the array, (b) demonstration of a sneak-current path in a 3x3 array, and (c) its electrical equivalent circuit indicating both desired path and the leakage path.

Figure 5.6(a) shows one such cycle that resembles to the CRS characteristics shown in figure 5.1(a). It starts with a negative sweep first, where Type B SET action (step 1) happens at -0.25 V. Using an I_{CC} value of 1 mA or higher during this phase allowed the device to reach an R_{LRS} as low as 113.68 Ω at V_{RESET}=-0.42 V (step 2), which was similar to the R_{LRS} of Type A switching, as was shown in table 5.1. This was followed by a gradual Type A RESET that resulted in a maximum R_{HRS} of 1.18 kΩ with a V_{STOP} of -1 V. During the subsequent positive sweep, the device switched to R_{LRS} (480 Ω at 0.48 V) through Type A SET process at 0.45 V (step 3). When the voltage was swept back from 1 V to 0 V with an I_{CC} of 0.5 mA, the device was seen to RESET sharply at 0.76 V (step 4), similar to that of the Type B RESET. The device resistance switched from 1.5 kΩ to 6.1 MΩ during this RESET step.

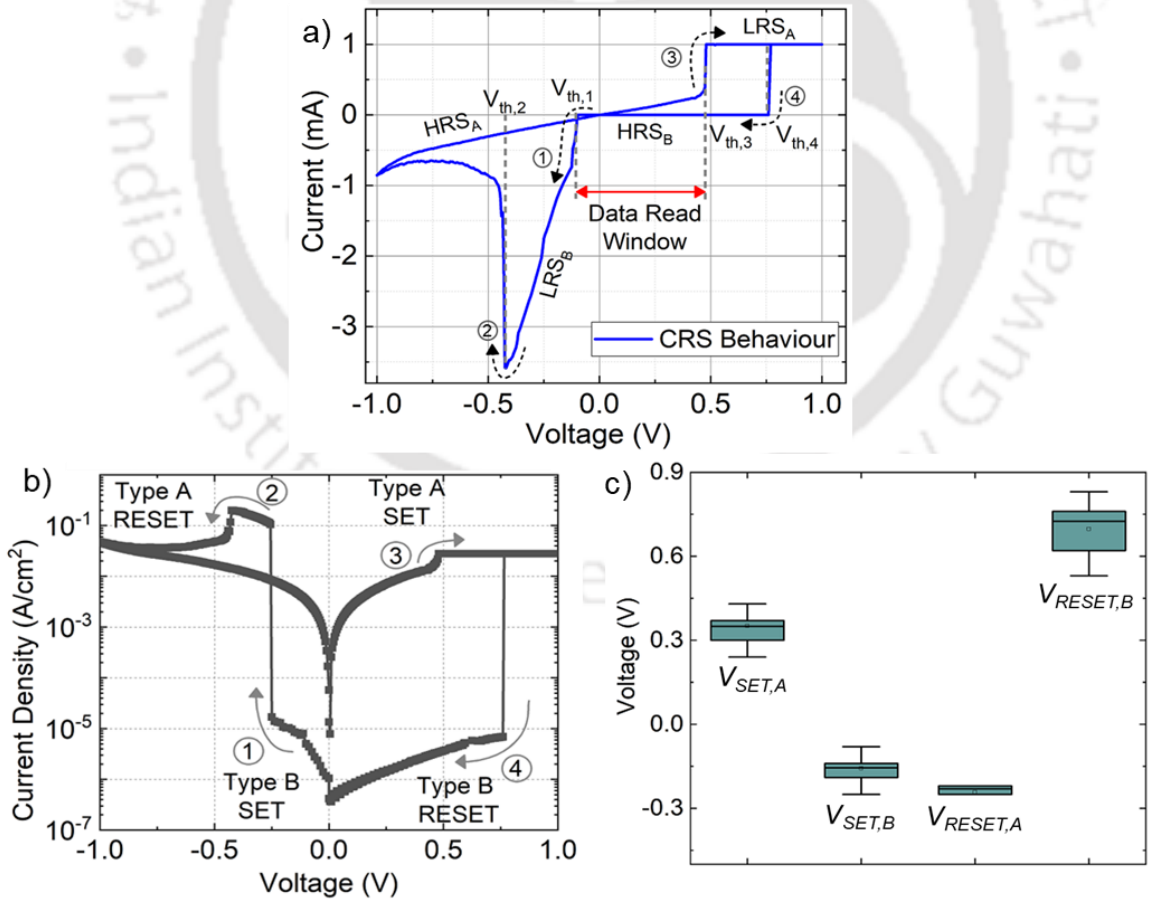


Figure 5.6: (a,b) Two different types of switching obtained in the same cycle; (a) I-V plot in linear scale, (b) *J-V* plot in log-linear scale, and (c) the statistical variation of $V_{SET,A}$, $V_{SET,B}$, $V_{RESET,A}$, and $V_{RESET,B}$ obtained from the 10 CRS cycles.

In the voltage range between -0.2 V and 0.4 V, the device remains in a HRS (resistance ≥1.5 kΩ), which is the signature of a CRS type of behaviour. To distinguish between the HRS and LRS, we have plotted the current density versus voltage in semi-log scale in figure 5.6(b). The statistical variation of $V_{SET,A}$, $V_{SET,B}$, $V_{RESET,A}$, and $V_{RESET,B}$ obtained from 10 such CRS cycles are shown in figure 5.6(c), from which their median values were found to be 0.35 V, -0.15 V, -0.22 V, and 0.72 V respectively.

5.4 Resistive Switching Mechanism

It has been well established that the RS in $MAPbI_3$ can be due to either the formation of metallic filaments or the redistribution of halide ions and vacancies [3,25,26]. In some cases, the formation and rupture of CFs are assisted by a physical or chemical interaction at the perovskite|electrode interface that modifies the injection properties of the contact and, thereby, alters the charge transfer resistance [27,28]. It is possible that the CF involved in the devices presented here is made of iodine vacancies (V_I^+s), as the activation energy of I^- ion (0.58 eV) is minimum among all the migrating species in $MAPbI_3$ [29].

The possible operating mechanisms for both types of switching are shown schematically in figures 5.7(a) and 5.7(b). In the case of Type A switching, a positive voltage at the TE attracts I^- ions, leading to their accumulation near TE [11,12]. Subsequently, the formation of CF made of V_I^+s takes place from BE, as represented in figure 5.7(a)(i). As the I_{CC} used in the Type A switching is higher than that in Type B, the CF formed is comparatively stronger, requiring a higher E_{RESET} of 11.6 kV/cm [30]. The gradual switching during the Type A RESET indicates the migration of I^- ions back into V_I^+s in the CF, due to applied negative voltage at TE, followed by an oxidation reaction and gradual annihilation of CF (see figure 5.7(a)(ii)). In this case, the strength of the electric field controls the RESET process by controlling the extent of CF annihilation.

Thus, different R_{HRS} values can be obtained by varying the applied voltage during the RESET step. This fact is further supported by the multiple HRSs obtained from different V_{STOP} values, as observed in figure 5.3(a). In contrast, during the Type B switching (see figure 5.7(b)(i)), a positive voltage at the BE attracts I^- ions which, instead of getting accumulated, out-diffuse through BE [16]. Therefore, the RESET process in Type B switching is dominated by Joule heating (see figure 5.7(b)(ii)) rather than field-assisted migration of I^- ions, due to the lack of I^- ions in the BE to react with V_I^+s in the CF. The use of lower I_{CC} aids this process by forming a comparatively weaker CF that can be broken using the heating effect from the applied field (7.89 kV/cm), which is lower than that in the case of Type A switching [30]. The invariability of HRS with V_{STOP}, as demonstrated in figure 5.3(b), further supports the fact that there is little role of field-driven migration in Type B switching.

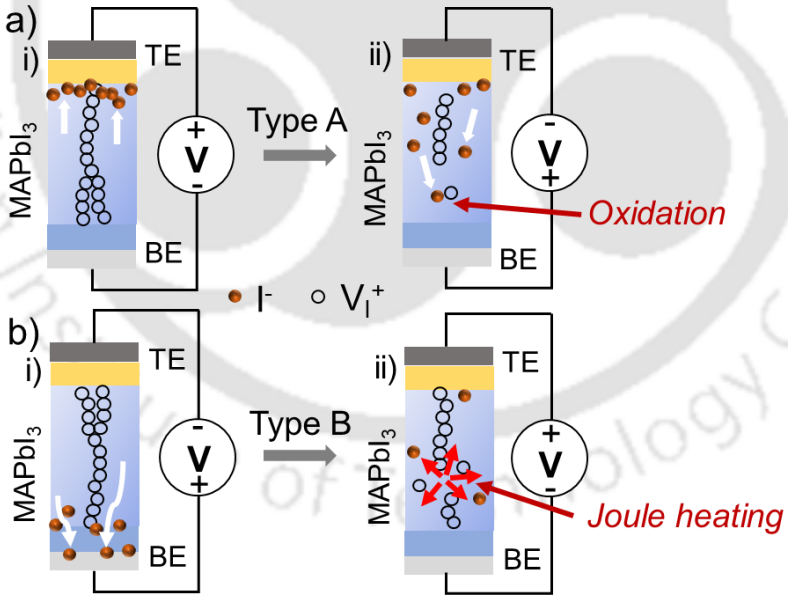


Figure 5.7: Diagrams representing the possible working mechanism of the HOIP memristor for (a) Type A and (b) Type B switching.

5.5 Memristor Models

A range of analytical models based on the use of numerical methods to solve sets of differential equations [4,5], Monte Carlo simulations [6,7], and SPICE simulations [8,9] have been proposed for the conduction and switching mechanisms in memristors.

Most of these models are either structure-specific or material-specific with limited consideration of internal physical processes, such as temperature dependence, ion migration, formation and rupture of CFs etc. Ren *et al.* proposed a physics-based deterministic model for $MAPbI_3$ memristor that modelled temperature dependence and the subsequent filament formation in the active layer [5]. However, all memristors exhibit an inherent stochastic behaviour, showing device-to-device and cycle-to-cycle variations in their characteristics. The model presented by Yakopcic *et al.* is applicable to a wide range of memristors and considers stochasticity [10,31]. In this model, as shown in equations (5.1) and (5.2), the two different current conduction mechanisms in LRS and HRS are combined by a state variable $x(v,t)$.

$$i(t) = i_{LRS}x(v,t) + i_{HRS}(1 - x(v,t)) \quad (5.1)$$

$$\frac{dx}{dt} = \eta g(v(t))f(x(v,t)) \quad (5.2)$$

Here $i(t)$ is the memristor current, $v(t)$ is the applied voltage, and i_{LRS} and i_{HRS} are the currents during the LRS and HRS, respectively. The rate of change of the state variable, as shown in equation (5.2), depends on two functions $g(v(t))$ and $f(x(t))$, while η is the direction of voltage sweep (+1 for the sweep in the positive direction and -1 for the sweep in the negative direction). The function $g(v(t))$ dictates how fast the state variable changes after the applied voltage crosses the voltage thresholds, V_p and V_n. The function $f(x(t))$ changes exponentially only above a certain threshold (x_p, x_n) and this variation could be asymmetric for opposite polarities of applied bias, which is controlled by using two window functions w_p and w_n. The fitting functions are given below, from equations (5.3) to (5.10), where A_p, A_n, $g_{pk,p}$, $g_{pk,n}$, g_{max}, g_{min}, $g_{slow,p}$, $g_{slow,n}$ are parameter extracted from experimental data. The extraction procedure is explained in the subsequent sections. The fitting parameters are related to device dimensions and material properties.

$$g(v(t)) = \begin{cases} A_p\left(e^{v(t)} - e^{v_p}\right), & v(t) > v_p \\ A_n\left(e^{-v(t)} - e^{v_n}\right), & v(t) < -v_n \\ 0, & -v_n \le v(t) \le v_p \end{cases} \quad (5.3)$$

$$f(x(t)) = \begin{cases} e^{-(x(t)-x_p)} w_p(x(t), x_p), & x(t) \ge x_p \\ e^{(x(t)+x_n-1)} w_n(x(t), x_n), & x(t) \le 1 - x_n \\ 1, & 1 - x_n \le x(t) \le x_p \end{cases} \quad (5.4)$$

$$A_p = \frac{g_{pk,p}}{g_{max} - g_{min}} \quad (5.5)$$

$$A_n = \frac{g_{pk,n}}{g_{max} - g_{min}} \quad (5.6)$$

$$x_p = \frac{g_{slow,p} - g_{min}}{g_{max} - g_{min}} \quad (5.7)$$

$$x_n = \frac{g_{slow,n} - g_{min}}{g_{max} - g_{min}} \quad (5.8)$$

$$w_p(x, x_p) = \frac{x_p - x}{1 - x_p} + 1 \quad (5.9)$$

$$w_n(x, x_n) = \frac{x}{1 - x_n} \quad (5.10)$$

5.6 Simulation of HOIP Memristor IV Characteristics

5.6.1 Modified Yakopcic Model Algorithm

The simulation algorithm starts by considering the I-V data of the HOIP memristor followed by separating the ON state (LRS) and OFF state (HRS) ranges from it. Then, these two ranges are fitted individually to different mathematical functions to deduce the current conduction mechanisms in the respective regions. Once the suitable mathematical functions are found with adequate fitting accuracy, the model equations are modified (for example, i_{LRS} and i_{HRS} in equation (5.1)) to adapt the parameters of the fitted functions. To realize the threshold switching hysteresis behaviour of the memristors, several other parameters such as V_p, V_n, $g_{pk,p}$, $g_{pk,n}$, $g_{slow,p}$, and $g_{slow,n}$ are extracted from the time domain current and conductance data of the device. After all the necessary fitting parameters are extracted, an equivalent circuit is made in SPICE to incorporate the model equations. The circuit schematic is shown in figure 5.8(a), where

the current source G_m gives the memristor current, and the memristor subcircuit is designed as shown in figure 5.8(b). A 1F capacitor is used to obtain the value of x from i_{Gx}, which equals dx/dt. The process flow of the simulation algorithm is illustrated in figure 5.9.

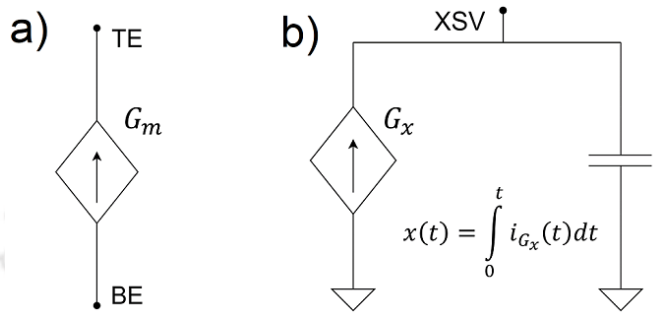


Figure 5.8: The equivalent model circuit designed in SPICE; (a) the current source from which overall memristor current is achieved and (b) memristor subcircuit equivalent consisting of a dependent current source and a 1 F capacitor. The voltage at the XSV node gives the state variable value, as calculated from the time integral of the current through the capacitor.

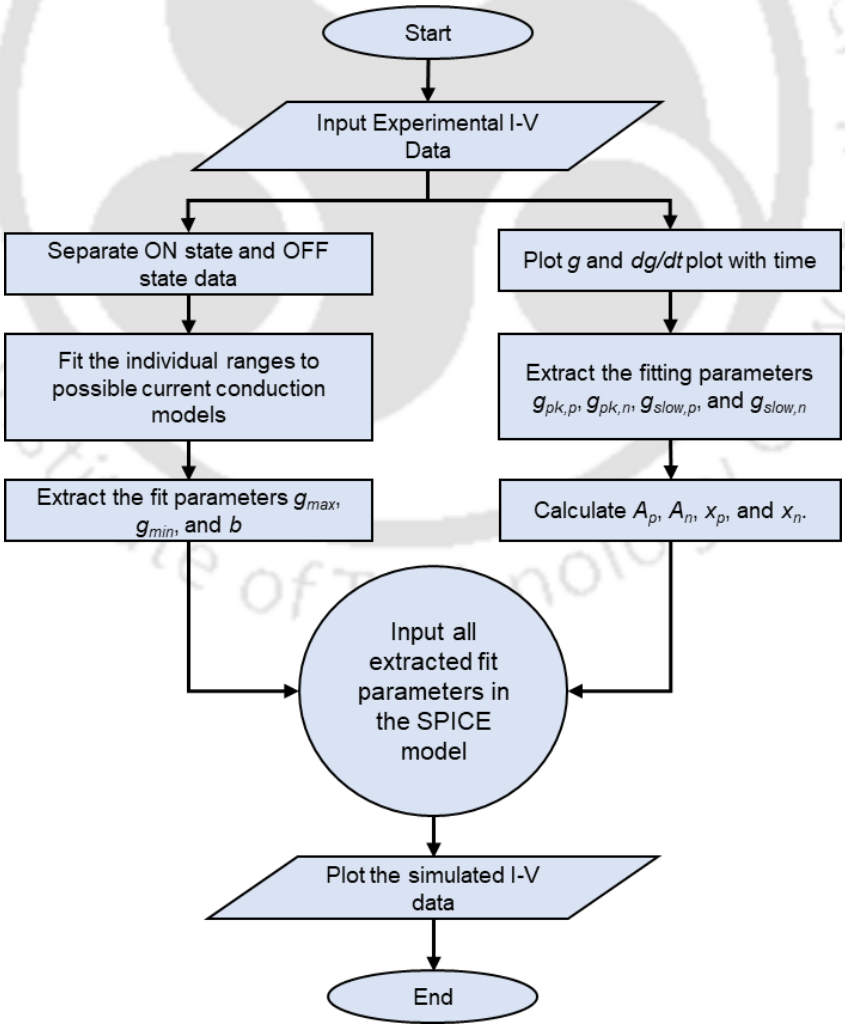


Figure 5.9: A flowchart explaining the HOIP memristor I-V simulation strategy.

5.6.2 Fitting Parameter Extraction for HOIP Memristor

For our HOIP memristors, the I-V plots for the two types of switching fit to different analytical models separately for HRS and LRS regions. The LRS regions of both TYPE A and Type B switching fit to linear I-V relation with good agreement, dictating ohmic conduction in this state. The HRS region of Type A switching fits a hyperbolic sine function which indicates that the conduction during this phase is likely to be limited by tunnelling mechanism [10,32]. On the other hand, the HRS region of Type B switching fits an exponential function along with a linear term. This indicates conduction is likely to be limited by diffusion mechanism, possibly in the presence of shunt paths. [33]. These functions are shown in the equations (5.11), (5.12), and (5.13), where $i_{LRS,A}(v,t)$ is the LRS current, $i_{HRS,A}(v,t)$ and $i_{HRS,B}(v,t)$ are the HRS current in the two cases, g_{max}, $g_{min,a}$, $g_{min,b}$, b, c, and d are fitting parameters.

$$i_{LRS,A}(v,t) = g_{max}v(t) \tag{5.11}$$

$$i_{HRS,A}(v,t) = g_{min,a}\sinh\{bv(t)\} \tag{5.12}$$

$$i_{HRS,B}i(v,t) = g_{min,b}\{e^{cv(t)} + dv(t)\} \tag{5.13}$$

The fitting results are shown in figures 5.10(a) and (b) for Type A and Type B switching, respectively. Here, the red plots show the LRS regions, blue plots show the HRS regions, and the black lines show the model fittings in the respective cases.

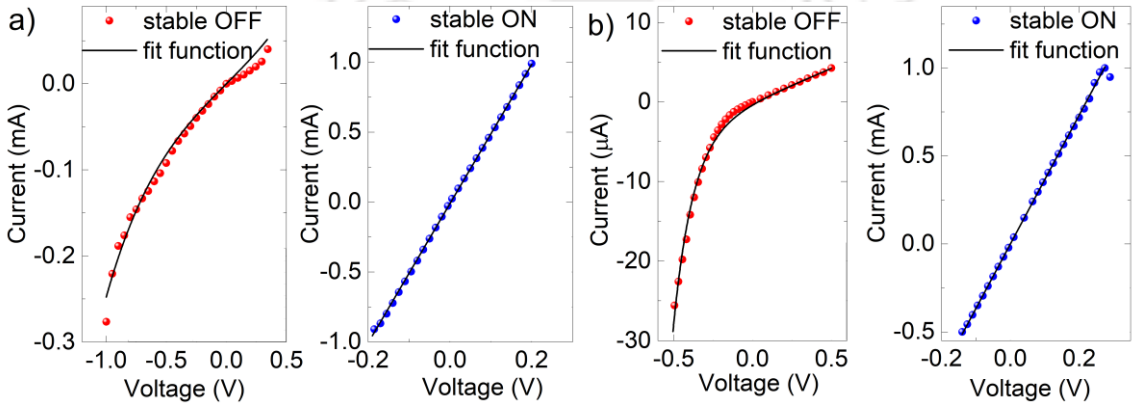


Figure 5.10: Piecewise fitting of experimental I-V plots to analytical models; the LRS of both types of switching fit a linear function, (a) HRS of Type A switching fits to a hyperbolic sine function, and (b) HRS of Type B switching fits to an exponential function with a linear term.

The threshold voltages V_p and V_n were extracted from the peak values of the rate of change of current in the positive and negative voltage regime, respectively. The peaks in the rate of change of conductance plot give the values of maximum conductivity changes, $g_{pk,p}$ and $g_{pk,n}$ from which A_p and A_n were calculated using equations (5.5) and (5.6), respectively. The points next to these values in the conductivity plot correspond to the parameters $g_{slow,p}$ and $g_{slow,n}$ from which x_p and x_n were calculated using equations (5.7) and (5.8), respectively. The red circles in figure 5.11(a) and (b) are the points from which the values of $g_{pk,p}$, $g_{pk,n}$, $g_{slow,p}$, and $g_{slow,n}$ were calculated. The extracted fitting parameter values for Type A and Type B are listed in table 5.2.

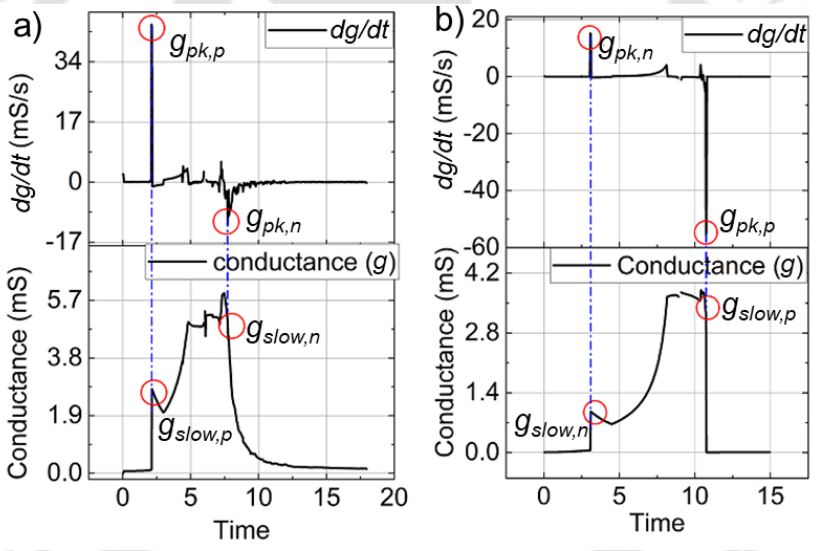


Figure 5.11: Conductance and rate of conductance change versus time plots for (a) Type A and (b) Type B switching.

Table 5.2: Extracted values of the fitting parameters for the two types of switching.

Parameters	**Type A**	**Type B**
V_p (V)	0.355	0.29
V_n(V)	-0.255	-0.515
g_{max}(mS)	5.0	3.7
g_{min}(μS)	72	0.43
$A_p(s^{-1})$	8.93x10^2	14.8x10^2
$A_n(s^{-1})$	3.537	4.05x10^2
x_p	0.5536	0.0019

x_n	0.2002	0.2599
b	1.95	-
c	-	7.97
d	-	0.2

5.6.3 SPICE Simulation of HOIP Memristor I-V Characteristics

The fitting parameters extracted from these piecewise functions are further used in SPICE for the complete emulation of memristor I-V curves. Figures 5.12(a) and (b) show the fitting results of the experimental I-V plots to the model equations for Type A and Type B switching with per-cycle mean errors of 6.93% and 7.28%, respectively. The mean errors in the SET and RESET cycles for Type A switching were 2.39% and 9.50%, respectively, whereas those for Type B switching were 3.89% and 7.87%, respectively. It can be observed that unlike in the SET cycle, the resistance changes more gradually in a RESET cycle, resulting in relatively lower accuracy. This could be because, with the longer duration of applied voltage, factors such as the presence of dynamic residual filaments, Joule heating etc., have not been considered in the model. The fit parameters g_{max} and g_{min} are related to the perovskite thickness as conductivity increases with increased tunnelling. As the rate of change of device state is directly proportional to the parameters A_p and A_n, they are associated with the mobility of the moving ions in the perovskite. The parameters x_p and x_n may be related to one or both the electrodes of the memristor as they dampen the rate of change of the state variable [33].

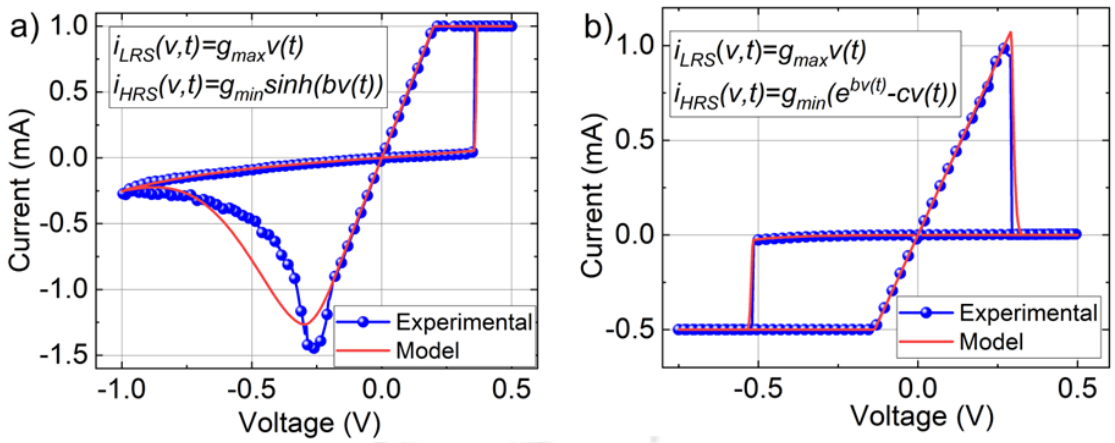


Figure 5.12: Fitting experimental I-V plots to analytical models for the HOIP memristor; (a) Type A and (b) Type B switching.

Although 3D HOIP memristors display reliable RS behaviour, it is difficult to control the shape, uniformity, and strength of the CFs. Such uncontrollable conducting pathways in the film deteriorate the endurance and retention capacity of the device. In addition, the 3D HOIP materials are unstable under external stimuli, such as moisture, light, heat, and oxygen. The reason for their vulnerability against moisture is that water molecules easily interact with the structure and break it into its constituents. However, the hydrophobic nature of the organic spacer cation and its unique crystal structure render lower- or mixed-dimensional perovskites more stable in air and, therefore, these are more promising candidates for RS. In the next chapter, we demonstrate a lower-dimensional HOIP memristor, which exhibits better ambient stability and improved electrical performance.

5.7 Summary

Two different types of BRS behaviours, referred to as Type A and Type B switching, have been demonstrated for the first time in a HOIP memristor by applying an electric field of opposite polarities. Type A switching can be observed when a positive field is used for SET and a negative field is used for RESET, with an I_{CC} of 1 mA. Whereas, Type B switching occurs when a negative field is used for SET and a positive field is used for RESET, with an I_{CC} of 0.5 mA. Interestingly, the RESET steps of the two types

of switching, as observed from their respective I-V plots, are strikingly different, which indicate the involvement of two different mechanisms for the two cases. In Type A, the device resistance during the negative voltage sweep changes gradually after V_{RESET}, whereas, it is abrupt in the other case. This leads to a V_{STOP}-dependent IRS in case of Type A switching, which can be explored to obtain multilevel RS. The RS mechanism in Type A could be due to the field-driven redox reaction of migrating iodine ions and the corresponding vacancies. The usage of comparatively lesser I_{CC} and the observation of abrupt RESET in case of Type B switching indicate the formation of similar CFs but they get ruptured due to Joule heating. This assumption is also supported by its V_{STOP}-independent switching. The analysis of the I-V characteristics showed that the current during HRS is dominated by tunnelling mechanism for Type A switching and by diffusion current for Type B switching. On the other hand, both types show ohmic conduction in their ON state. We have observed that the two BRSs can be observed in the same device by using proper sequence of applied filed along with adequate I_{CC}. RS characteristics resembling CRS behaviour have also been demonstrated, which can be useful in mitigating sneak currents without the requirement of any additional selector devices. Unlike typical CRS devices, two anti-serially connected memristors are not required in this case, making it possible to achieve higher device densities in crossbar arrays.

Simulation of memristor characteristics is essential to incorporate them into circuit and system design tools. However, no such simulation tools are readily available for circuit design engineers for emerging materials such as HOIPs. We proposed and validated a new algorithm for simulating the I-V characteristics of $MAPbI_3$ memristors. This algorithm is a modification of the standard SPICE-based Yakopcic model. The complete simulation of Type A and Type B switchings in our devices yielded per-cycle

mean errors of 6.93% and 7.28% respectively. However, finding the exact relation between the fit parameters and the physical quantities requires additional analysis of experimental data varied over a wider range of parameters.

5.8 References

[1] R. Waser *et al.*, "Redox-based resistive switching memories - nanoionic mechanisms, prospects, and challenges," Advanced Materials, vol. 21, no. 25–26, pp. 2632–2663, 2009.

[2] R. Waser and M. Aono, "Nanoionics-based resistive switching memories," Nat. Mater., vol. 6, no. 11, pp. 833–840, 2007.

[3] Y. Sun *et al.*, "Competition between metallic and vacancy defect conductive filaments in a $CH_3NH_3PbI_3$-based memory device," Journal of Physical Chemistry C, vol. 122, no. 11, pp. 6431–6436, 2018.

[4] D. Ielmini, "Modeling the universal set/reset characteristics of bipolar RRAM by field- and temperature-driven filament growth," IEEE Transactions on Electron Devices, vol. 58, no. 12, pp. 4309–4317, 2011.

[5] Y. Ren *et al.*, "Analytical modeling of organic-inorganic $CH_3NH_3PbI_3$ perovskite resistive switching and its application for neuromorphic recognition," Advanced Theory And Simulations, vol. 1, no. 4, p. 1700035, 2018.

[6] P. Sun *et al.*, "Simulation study of conductive filament growth dynamics in oxide-electrolyte-based ReRAM," Journal of Semiconductors, vol. 35, no. 10, p. 104007, 2014.

[7] J. Guy *et al.*, "Investigation of forming, SET, and data retention of conductive-bridge random-access memory for stack optimization," IEEE Transactions on Electron Devices, vol. 62, no. 11, pp. 3482–3489, 2015.

[8] H. Abdalla and M. D. Pickett, "SPICE modeling of memristors," in 2011 IEEE International Symposium of Circuits and Systems (ISCAS), pp. 1832–1835, 2011.

[9] J. Borghetti *et al.*, "Electrical transport and thermometry of electroformed titanium dioxide memristive switches," Journal of Applied Physics, vol. 106, no. 12, p. 124504, 2009.

[10] C. Yakopcic *et al.*, "Generalized memristive device SPICE model and its application in circuit design," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 32, no. 8, pp. 1201–1214, 2013.

[11] L. Liu *et al.*, "Coexistence of unipolar and bipolar resistive switching in $BiFeO_3$ and $Bi_{0.8}Ca_{0.2}FeO_3$ films," Journal of Applied Physics, vol. 111, no. 10, p. 104103, 2012.

[12] L. Zhang *et al.*, "Coexistence of bipolar and unipolar resistive switching behaviors in the double-layer Ag/ZnS-Ag/$CuAlO_2$/Pt memory device," Applied Surface Science, vol. 360, pp. 338–341, 2016.

[13] X. Zhao *et al.*, "Reversible alternation between bipolar and unipolar resistive switching in Ag/MoS_2/Au structure for multilevel flexible memory," Journal of Materials Chemistry C, vol. 6, no. 27, pp. 7195–7200, 2018.

[14] W. Wang *et al.*, "Forming-free bipolar and unipolar resistive switching behaviors with low operating voltage in Ag/Ti/CeO_2/Pt devices," Results in Physics, vol. 16, no. 103001, p. 103001, 2020.

[15] X. Sun *et al.*, "Bipolar resistance switching characteristics with opposite polarity of Au/$SrTiO_3$/Ti memory cells," Nanoscale Research Letters, vol. 6, no. 1, p. 599, 2011.

[16] A. R. Lee *et al.*, "Multifunctional resistive switching behaviors employing various electroforming steps," Journal of Materials Chemistry C, vol. 4, no. 4, pp. 823–830, 2016.
[17] H. Zhang *et al.*, "Understanding the coexistence of two bipolar resistive switching modes with opposite polarity in Pt/TiO_2/Ti/Pt nanosized ReRAM devices," ACS Applied Materials & Interfaces, vol. 10, no. 35, pp. 29766–29778, 2018.
[18] S. A. Khan and S. Kim, "Comparison of diverse resistive switching characteristics and demonstration of transitions among them in Al-incorporated HfO_2-based resistive switching memory for neuromorphic applications," RSC Advances, vol. 10, no. 52, pp. 31342–31347, 2020.
[19] E. Linn *et al.*, "Complementary resistive switches for passive nanocrossbar memories," Nature Materials, vol. 9, no. 5, pp. 403–406, 2010.
[20] X. Zhang *et al.*, "Effect of Joule heating on resistive switching characteristic in AlO_x cells made by thermal oxidation formation," Nanoscale Res. Lett., vol. 15, no. 1, p. 11, 2020.
[21] W. Banerjee, "Challenges and applications of emerging nonvolatile memory devices," Electronics (Basel), vol. 9, no. 6, p. 1029, 2020.
[22] S. Yu and P.-Y. Chen, "Emerging memory technologies: Recent trends and prospects," IEEE Solid-State Circuits Magazine, vol. 8, no. 2, pp. 43–56, Spring 2016.
[23] X. X. Xu *et al.*, "Resistive switching memory for high density storage and computing," Chinese Physics B, vol. 30, no. 5, p. 058702, 2021.
[24] W. Banerjee *et al.*, "Complementary switching in 3D resistive memory array," Advanced Electronic Materials, vol. 3, no. 12, p. 1700287, 2017.
[25] E. J. Yoo *et al.*, "Resistive switching behavior in organic-inorganic hybrid $CH_3NH_3PbI_{3-x}Cl_x$ perovskite for resistive random access memory devices," Advanced Materials, vol. 27, no. 40, pp. 6170–6175, 2015.
[26] C. Gu and J.-S. Lee, "Flexible hybrid organic-inorganic perovskite memory," ACS Nano, vol. 10, no. 5, pp. 5413–5418, 2016.
[27] A. Solanki *et al.*, "Interfacial mechanism for efficient resistive switching in ruddlesden-Popper perovskites for non-volatile memories," Journal of Physical Chemistry Letters, vol. 11, no. 2, pp. 463–470, 2020.
[28] S. Ge *et al.*, "Silver iodide induced resistive switching in $CsPbI_3$ perovskite-based memory device," Advanced Materials Interfaces, vol. 6, no. 7, p. 1802071, 2019.
[29] J. M. Azpiroz *et al.*, "Defect migration in methylammonium lead iodide and its role in perovskite solar cell operation," Energy & Environmental Science, vol. 8, no. 7, pp. 2118–2127, 2015.
[30] V. Rana and R. Waser, "Redox-based memristive devices," in Memristors and Memristive Systems. Springer, pp. 223–251, 2014.
[31] C. Yakopcic *et al.*, "Memristor model optimization based on parameter extraction from device characterization data," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 39, no. 5, pp. 1084–1095, 2020.
[32] M. D. Pickett *et al.*, "Switching dynamics in titanium dioxide memristive devices," Journal of Applied Physics, vol. 106, no. 7, p. 074508, 2009.
[33] M. A. Green, "Solar cells: operating principles, technology, and system applications," Englewood Cliffs, 1982.

CHAPTER 6

Lower Dimensional HOIP Memristors

Contents

6.1 Introduction

This chapter discusses memristors that use lower-dimensional perovskites in Ruddlesden–Popper (RP) phase. RP phase is a HOIP structure consisting of 2D perovskite-like slabs interleaved with large cations. Due to the layered structure of RP perovskites, these films have better resistance to atmospheric oxygen and moisture [1,2]. In addition, the electrical conduction in these films is anisotropic, making the random migration of charge carriers less likely [3]. As a result, they have a comparatively smaller HRS current, resulting in a better ON/OFF ratio [4]. The strong environmental stability, good electrical conductivity, and reduced ion migration make RP perovskites a strong candidate for future ReRAM devices.

We have fabricated and characterized memristors based on RP perovskites to study their RS properties. The differences between the current conduction mechanisms in LRS and HRS were studied from the low-temperature I-V characteristics. Also, the performance of these devices was compared with that of their 3D counterparts.

6.2 Lower-Dimensional HOIPs

In recent times, RP perovskites have commonly been used for realizing stable solar cells [1, 5]. In this work, we added different fractions of butyl ammonium iodide (BAI) to $MAPbI_3$, resulting in RP structures with a general formula $BA_2MA_{n-1}Pb_nI_{3n+1}$. Figure 6.1(a) shows that the butyl ammonium cation has a long chain to separate the interlayers composed of PbI_6 octahedra. By varying the ratio of MAI and BAI, the dimensionality of the film can be changed from 3D $MAPbI_3$ ($n=\infty$) to quasi-2D (for n=2, 3, 4…) and, finally, to the pure 2D BA_2PbI_4 (for n=1). Figure 6.1(b) shows the change of the perovskite layered structures with n (i.e., fraction of BA^+).

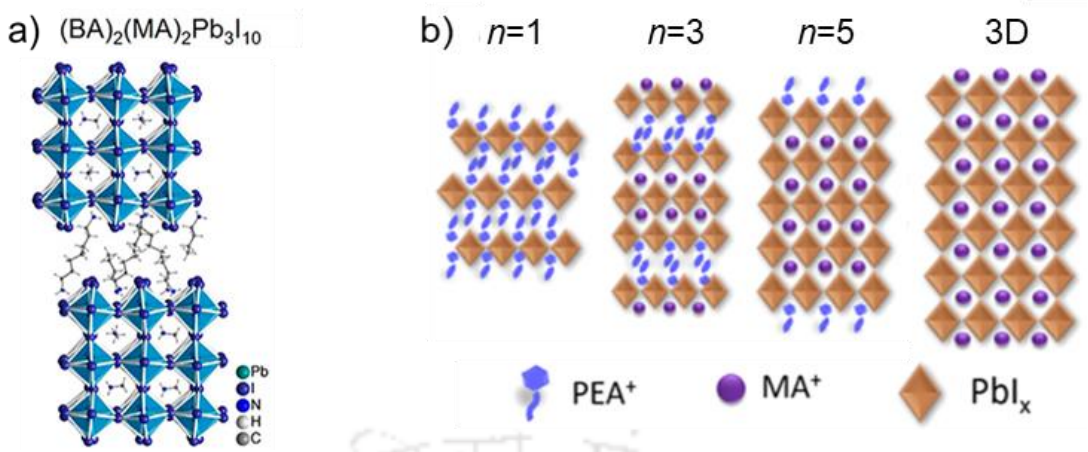


Figure 6.1: (a) Schematic structure of $BA_2MA_{n-1}Pb_nI_{3n+1}$ (n=3) [6]. (b) Change of dimensionality with increasing n value in RP perovskite films, for n=1,3,5, and ∞ (3D) [3].

To prepare the precursor solution for such RP perovskite films, we have mixed 1 mmol PbI_2 with x mmol BAI, y mmol of MAI, and 2 mmol DMSO in 1mL of DMF [7]. For n=1, 2, and 3, the values used for x and y were (1, 0.5, 0.25) and (0, 0.5, 0.75) respectively. The films were spin-coated at 3000 rpm for 40 sec with an acceleration of 1200 rpm/s. Chlorobenzene (CB) was used as an antisolvent after 10 seconds from the start of the spinning. CB as antisolvent has the ideal combination of properties such as low solubility for the precursor components, and miscibility with the DMF:DMSO host solvent. This effectively removes the excess solvent mixture, making the antisolvent washing process less affected by the duration of antisolvent application [9]. Spin coating was followed by annealing the substrate at 55°C for 5 minutes, and then at 70°C for 55 minutes. The thicknesses of the films were found to be 390 nm for $MAPbI_3$ (n=∞), 551 nm for BA_2PbI_4 (n=1), 470 nm for $BA_2MAPb_2I_7$ (n=2), and 297 nm for $BA_2MA_2Pb_2I_{10}$ (n=3). These thickness values were obtained by taking the median of 16 readings at different locations on each substrate using a thickness profilometer. Figure 6.2(a) shows a photograph of the fabricated RP films, where the dark brown films are of $MAPbI_3$, the yellow films are of BA_2PbI_4, the red films are of $BA_2MAPb_2I_7$, and the blackish yellow films are of $BA_2MA_2Pb_2I_{10}$. The corresponding XRD spectra are shown in figure 6.2(b). The $MAPbI_3$ film has a preferential orientation of (110) crystallographic plane, along

with multiple minor peaks, including (310), (200), (211), (202), (312), etc. The peaks corresponding to $BA_2MA_2Pb_2I_{10}$ film are nearly similar to those of $MAPbI_3$ film. However, BA_2PbI_4 and $BA_2MAPb_2I_7$ films have preferential orientations of (002) and (020), respectively, suggesting the formation of layered structures. These observations align with the reported DFT calculations and other experimental data [7]. The BA_2PbI_4 film is highly orientated along the (002) crystal plane without the presence of any other phase.

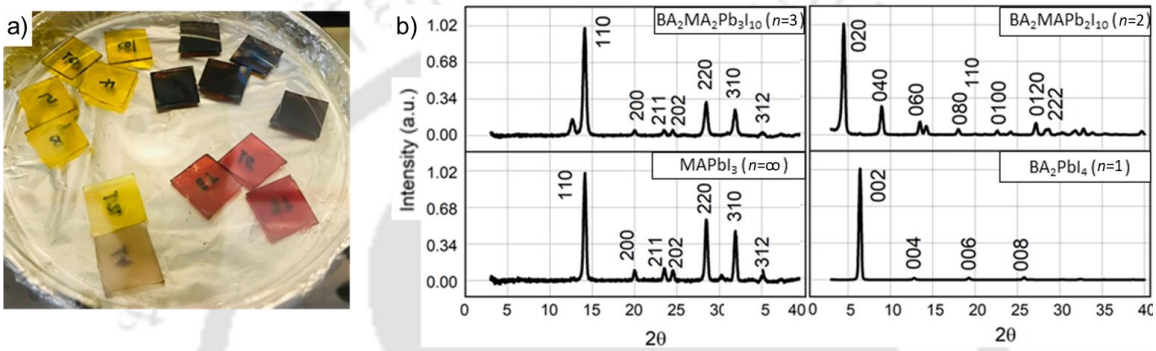


Figure 6.2: (a) Photograph of the spin-coated RP perovskite films for *n*=1 (yellow film), *n*=2 (red film), *n*=3 (blackish yellow film), and *n*=∞ (dark brown) and (b) the corresponding XRD spectra. Here, the films with *n*=∞ shows a preferential orientation of (110), whereas the film with *n*=1 shows preferential orientation of (001).

Figure 6.3(a) shows the normalized UV-vis absorption spectra obtained from these HOIP films over the wavelength range of 400-700 nm. The corresponding Tauc plots were obtained by plotting $(\alpha h\nu)^2$ vs photon energy, where α is the absorption coefficient, $h\nu$ is the photon energy (see figure 6.3(b)). The extrapolation of the linear region of the Tauc plot to the x-axis gives the optical band gap of the material. The band gaps of the HOIP films for *n*= ∞, 3, 2, and 1 were found to be 1.95 eV, 2.05 eV, 2.10 eV, and 2.33 eV, respectively, which match the values reported in the literature [9,10]. For the fabrication of memristors, we have chosen the BA_2PbI_4 RP films. Their electrical characterization results are discussed in the following sections.

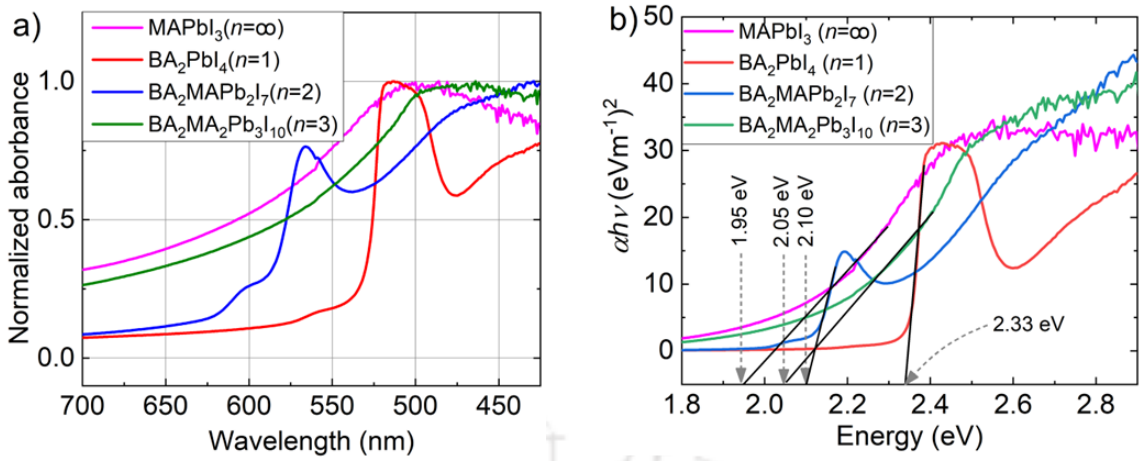


Figure 6.3: (a) Normalized UV-vis absorption spectra over the wavelength range of 400-700 nm, and (b) the corresponding Tauc plots of the 4 RP perovskite films, from which band gaps were estimated as 1.95 eV, 2.05 eV, 2.10 eV, and 2.33 eV for *n*= ∞, 3,2, and 1 respectively.

6.3 2D Perovskite Memristors

6.3.1 Characterization of 2D BA_2PbI_4 Memristors

Memristors with the structure ITO|PEDOT:PSS|BA_2PbI_4|PCBM|Ag (schematic in figure 6.4(a)) were fabricated using the procedure described earlier. While the device areas and deposition processes of other layers were the same as that of 3D $MAPbI_3$ devices described in chapter 4, the spin speed for the BA_2PbI_4 layer was kept at 4000 rpm. The AFM images show an RMS roughness of 17.72 nm when scanned over an area of 5x5 μm^2 (see figure 6.4(b)). The thickness of these RP films was found to be 485 nm ± 25 nm, confirmed by the cross-sectional FESEM taken on ITO glass substrate (see figure 6.4(c)), taking 8 measurements at different locations. The FESEM image was taken over an area of 1.44x0.96 μm^2, which clearly shows the formation of polycrystalline grains (see figure 6.4(d)). The grain size distribution in figure 6.4(e) indicates an average grain size of 151 nm, measured from 30 grains in the image area using ImageJ software, where the grain size ranged between 59.78 nm and 408.22 nm.

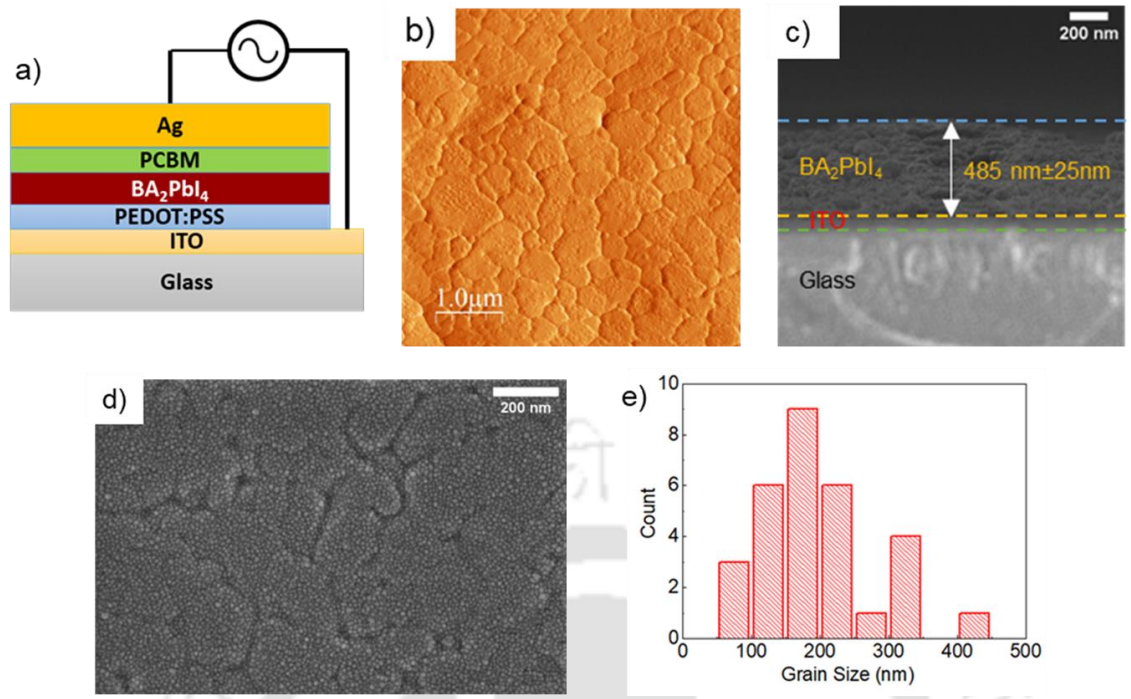


Figure 6.4: (a) A schematic of the 2D BA_2PbI_4 memristor. (b) AFM image of BA_2PbI_4 film taken over an area of 5x5 μm^2. The average RMS roughness is 17.72 nm. (c) Cross-sectional FESEM image of BA_2PbI_4 films deposited on ITO coated glass substrate; the thickness of HOIP layer is 485 nm ± 25 nm. (d) Surface FESEM image of the BA_2PbI_4 film taken over an area of 1.44x0.96 μm^2, with a scale of 200 nm. (e) Grain size distribution obtained from the FESEM image showing an average grain size of 197.26 nm.

Three cycles of the I-V characteristics of a memristor are shown in figure 6.5(a). The median values of V_{SET}, V_{RESET}, and ON/OFF ratio calculated from these three I-V cycles were 0.64 V, -0.33 V, and $1.36x10^3$, respectively. The inset of figure 6.5(a) shows a photograph of the fabricated devices with different areas ranging from 0.0018 cm^2 to 0.00008 cm^2. When an unencapsulated device under ambient conditions was tested right after fabrication and subsequently after every 2 days, the ON/OFF ratio was observed to drop from $1.14x10^3$ to 55, with a slight increase in V_{SET} from 0.74 V to 0.90 V (see figure 6.5(b)). It may be noted that, during the device characterization, the relative humidity in the laboratory was ~80%. Such a high humidity significantly decreases the life span of HOIPs. The variations of R_{HRS} and R_{LRS} with time for 3D $MAPbI_3$ and 2D BA_2PbI_4 devices are shown in figure 6.5(c). For both cases, the R_{LRS} did not change significantly for up to 96 hours. However, within this time, the R_{HRS} degraded by more than two orders for 3D $MAPbI_3$ device and by one order for 2D BA_2PbI_4 device. Consequently, the

ON/OFF ratio of 3D $MAPbI_3$ device reduced to 6, making it susceptible to random noise and unsuitable for data storage applications for a longer duration. Over the period of 96 hours, the ON/OFF ratios reduced by factors of 52 and 22 for 3D and 2D devices respectively. These results confirm that 2D HOIP devices, with their RP structure, are relatively more stable in the ambient atmosphere.

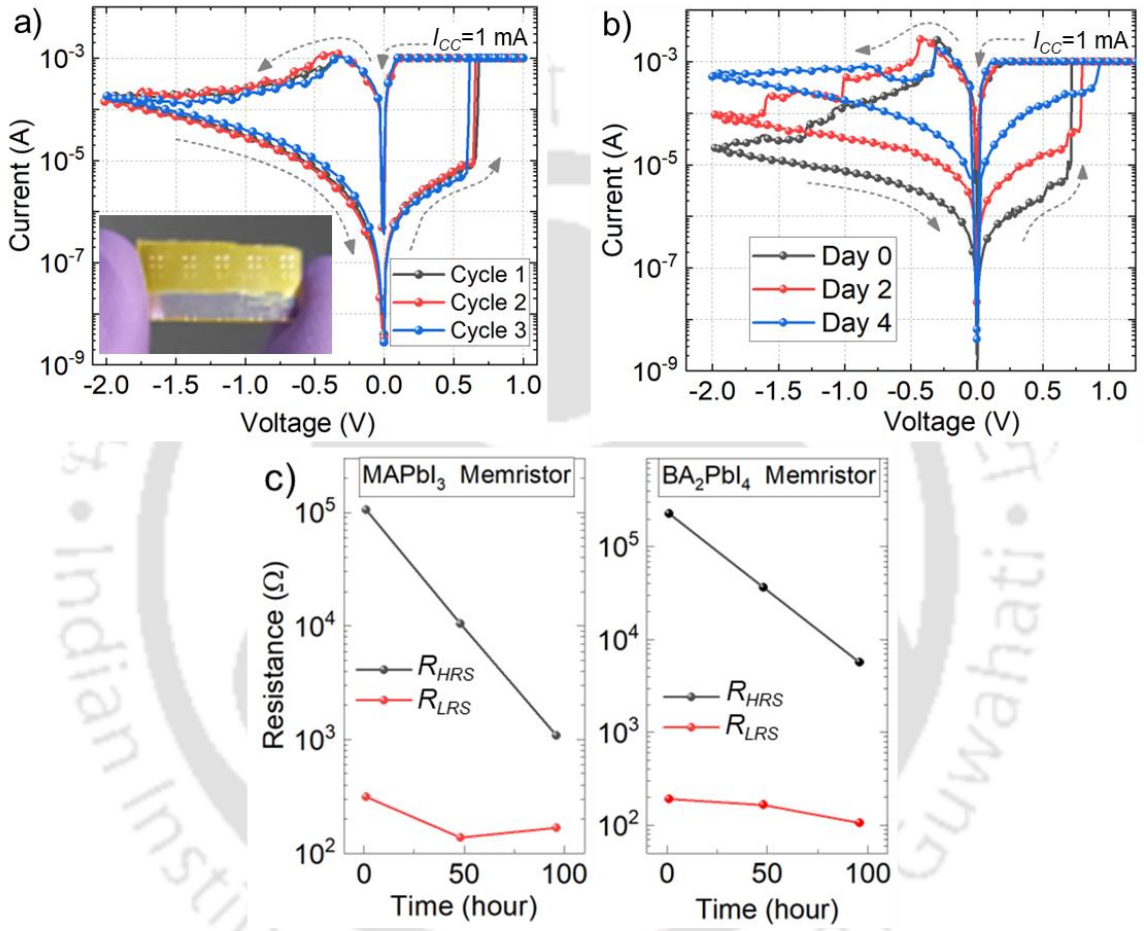


Figure 6.5: (a) I-V characteristics of a 2D HOIP memristor for 3 different cycles, the inset figure shows a photograph of the fabricated devices with areas ranging from 0.0018 cm^2 to 0.00008 cm^2. (b) I-V characteristics of a 2D HOIP memristors taken right after fabrication (black plot), after 2 days (red plot), and after 4 days (blue plot); the R_{HRS} of the device decreases with time. (c) Comparison of degradation of R_{HRS} and R_{LRS} for $MAPbI_3$ devices (left plot) and BA_2PbI_4 devices (right plot). The ON/OFF ratio of $MAPbI_3$ memristor reduces to just 6, while that of BA_2PbI_4 device is ~55.

The 2D devices maintained an ON/OFF ratio >10 for over 1000 cycles, as seen from the endurance plot in figure 6.6(a). Furthermore, it has been observed that a previously SET or RESET device can retain its state for at least 1350 seconds (see the retention plot in figure 6.6(b)). It is important to note that the number of endurance cycles

and the retention time mentioned here were not limited by the performance of the device. It is the maximum number of cycles and time that we were able to apply in our characterization setup in one run, which is limited by the maximum number of data points (i.e. 4096 points).

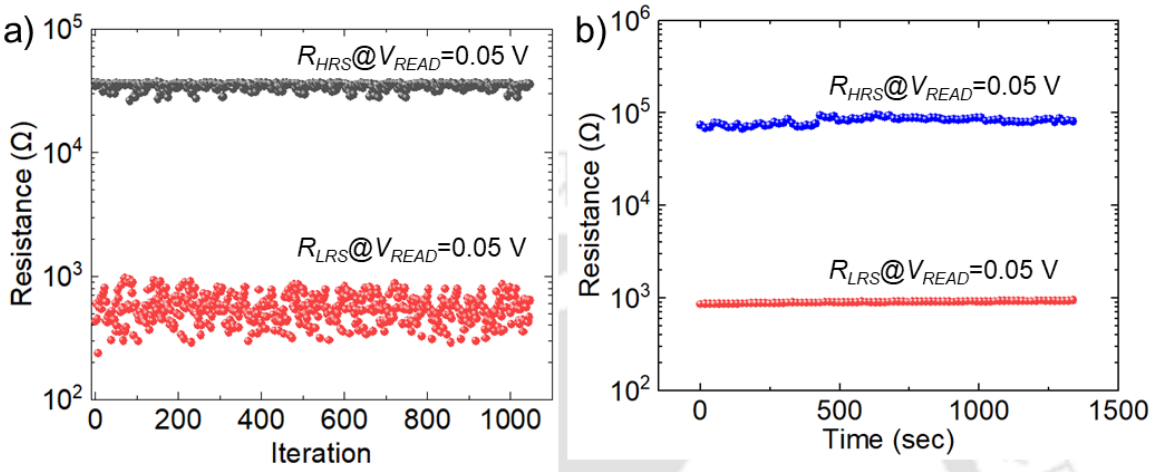


Figure 6.6: (a) The endurance plot obtained from 2D BA_2PbI_4 memristor for 1050 cycles. (b) Retention plot obtained for 1350 seconds.

6.3.2 Thickness Variation of BA_2PbI_4 Layer

We have varied the thickness of the BA_2PbI_4 layer to study its effect on the memristor parameters such as $V_{FORMING}$, V_{SET}, V_{RESET}, and ON/OFF ratio. By varying the spin speed from 6000 to 3000 rpm, thicknesses in the range of 385 nm to 518 nm were obtained. From the figure 6.7(a) and its inset, it can be seen that $V_{FORMING}$ increases with the thickness of BA_2PbI_4. This could be due to the requirement to form longer filaments over thicker HOIP films [10]. The linear fitting of the $V_{FORMING}$ vs thickness plot indicates that the pristine 2D HOIP memristors require an electric field of 60 kV/cm to form a complete filament. The I-V plots for one set of devices with four different perovskite thicknesses are shown in figure 6.7(b), where we see that V_{SET} and ON/OFF ratio tend to increase with thickness.

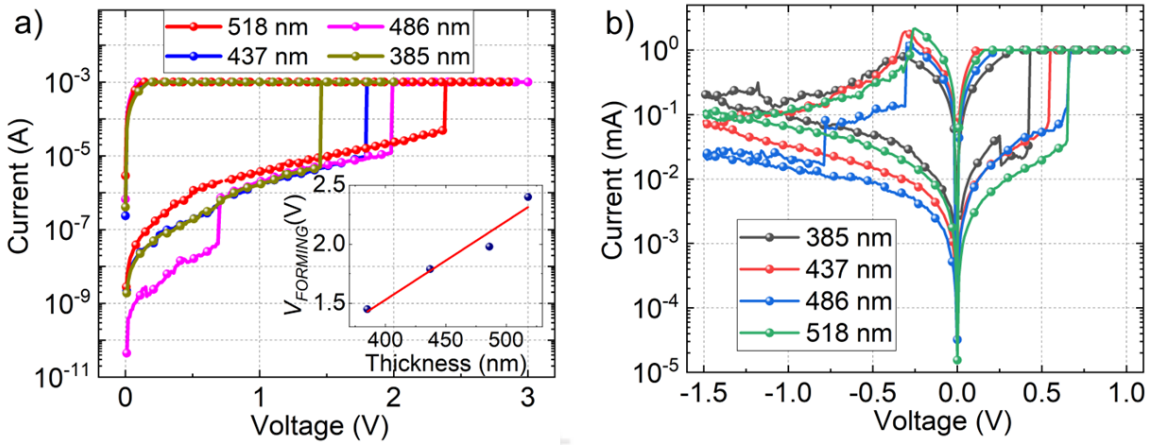


Figure 6.7: I-V plots corresponding to four different 2D BA_2PbI_4 layer thicknesses. (a) Forming step; the inset shows that $V_{FORMING}$ increases with thickness and that the memristors require a forming field of 60 kV/cm. (b) Switching cycles obtained from these four devices.

To reconfirm these observations, we have tested 15 devices for each thickness and observed the variations of V_{SET}, V_{RESET}, and ON/OFF ratio with thickness from the corresponding median values. These median values are summarized in Table 6.1 and represented graphically in figure 6.8.

Table 6.1: Variation of memristor properties with HOIP thickness

HOIP Thickness (nm)	$V_{FORMING}$ (V)	V_{SET} (V)	V_{RESET} (V)	ON/OFF ratio
385	1.45	0.55	-0.23	167.84
437	1.79	0.63	-0.30	482.43
486	1.98	0.64	-0.31	953.53
518	3.33	0.67	-0.33	1457.14

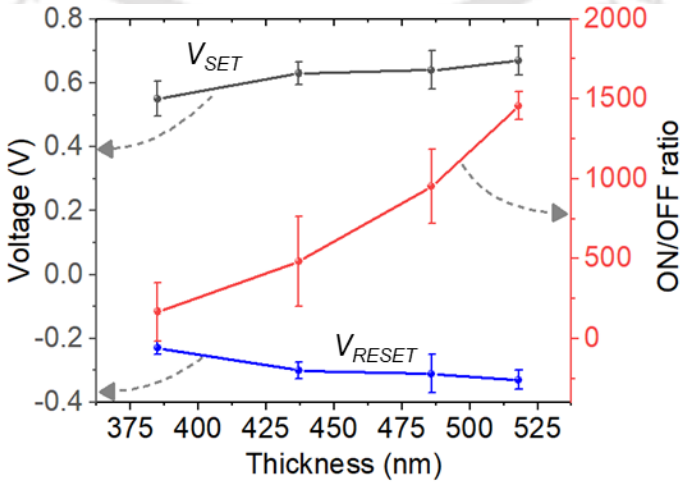


Figure 6.8: The variation of V_{SET}, V_{RESET}, and ON/OFF ratio with BA_2PbI_4 thickness. Magnitude of both V_{SET} (black plot) and V_{RESET} (blue plot) increase with the perovskite thickness. The ON/OFF ratio increases by more than an order of magnitude (red plot).

The electric field required to form these BA_2PbI_4 devices, as well as the operating voltages, are comparatively higher than those we obtained for 3D $MAPbI_3$ memristors (refer to subsection 4.4 in chapter 4). As reported in the literature, BA_2PbI_4 has a wider band gap (2.33 eV) compared to that of $MAPbI_3$ (1.95 eV) [11]. Besides, both the conduction band minima and valance band maxima get altered as the HOIP dimensionality changes from 3D to 2D. This results in the increase of the injection barriers at both the electrodes and a reduced density of injected carriers [12]. The higher values for forming and operating voltages/electric fields in the case of 2D BA_2PbI_4 device are a consequence of these effects [7]. However, compared to other 2D HOIP memristors reported [12], the forming electric field requirement in our case is much lesser. A complete forming-free memristive device can also be designed by reducing the film thickness, which may help optimize the power consumption. However, reducing the device thickness leads to a reduction in the ON/OFF ratio (see the red plot in figure 6.8), which may affect the noise margin of the device. Therefore, the trade-off between the power consumption and noise margin needs to be addressed while determining the device thickness and its structure.

6.4 Low-Temperature Performance of 2D HOIP Memristors

The I-V characteristics were also taken at low temperatures from which the current conduction mechanisms in the device were studied. To perform these low-temperature measurements, the two electrodes of the device were connected to the tungsten probes inside a cryo-chamber (make: Janis), and liquid nitrogen was used, which can lower temperature to ~78K. It has been reported that the typical orthogonal phase of the HOIP changes to cubic when the temperature goes above 300K. On the other hand, the phase changes from tetragonal to orthorhombic when temperatures are below ~150K [13-15]. Therefore, we have restricted our measurements in the range of 200K to 300K to discard any influence of phase transformation on the device performance. Figure 6.9

shows the I-V characteristics taken at five different temperatures in the range of 200K to 300K. Although memristive action was present at all the temperatures, we did not observe a consistent monotonic dependence of the operating voltages on temperature (see the inset of figure 6.9). However, analysis of R_{HRS} and R_{LRS} data obtained from these plots shed light on the current conduction mechanisms, which are discussed in the following subsections.

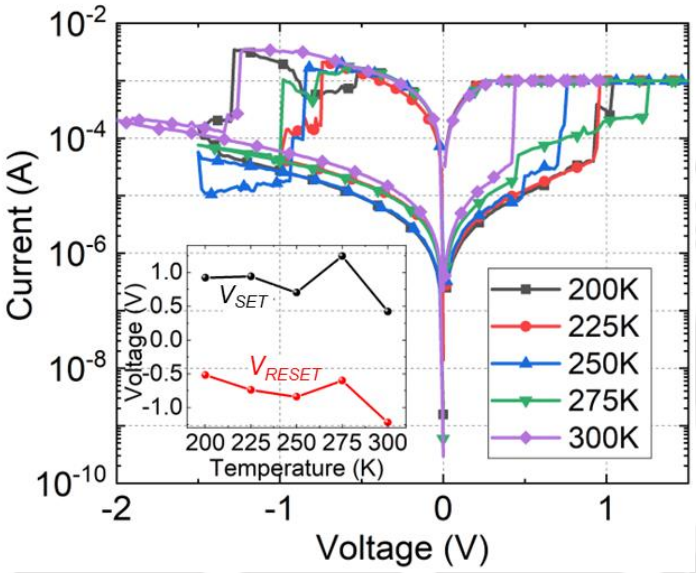


Figure 6.9: I-V plots BA_2PbI_4 memristor taken at different temperatures, ranging from 200K to 300K. Inset shows the variation of V_{SET} and V_{RESET} with temperature. These voltages do not show a monotonic trend over the given temperature range.

6.4.1 Temperature Dependence of LRS Current

The positive halves of the I-V characteristics obtained at different temperatures are plotted in figure 6.10(a). Linear fittings of the LRS currents in log-log scale show a slope of 1, indicating ohmic conduction after the SET process. Besides, the R_{LRS} values (read at 50mV) have been found to increase linearly with temperature as shown in figure 6.10(b), which is a typical signature of filamentary conduction, as reported from other HOIP memristive devices [12-14]. In order to investigate the type of the constituents of the CF, the linear variation of R_{LRS} with temperature is compared to the linear temperature coefficient of resistance for metals which follow the equation (6.1) below [16,17].

$$R_t = R_o(1 + \alpha T) \quad (6.1)$$

Here, R_t is the resistance at an absolute temperature T, R_o is the resistance at absolute zero, and α is the coefficient of temperature. We have obtained a slope of 0.529 and an intercept of 159.03 from the linear fitting of R_{LRS} vs T, yielding an α of 3.30×10^{-3} K^{-1} which is slightly less than that of the bulk silver (3.80×10^{-3} K^{-1} at room temperature) [18-19]. As compared to bulk silver, the α value for a silver nanowire may be lesser by about 25% depending on the wire thickness [20]. Bid *et al.* varied the silver nanowire thickness from 15 nm to 200 nm, which resulted in the α values in the range of 2.5×10^{-3} K^{-1} to 4×10^{-3} K^{-1} [21]. Due to the nano-wire like behaviour of CF, it might have a lower value of α relative to that of bulk silver. This, in turn, indicates that the CFs in our device may have been formed by the diffusion of Ag^+ ions from the TE, as cited in other reports [22-24]. However, the method we employed here is only one indirect method to investigate the constituents of the CF.

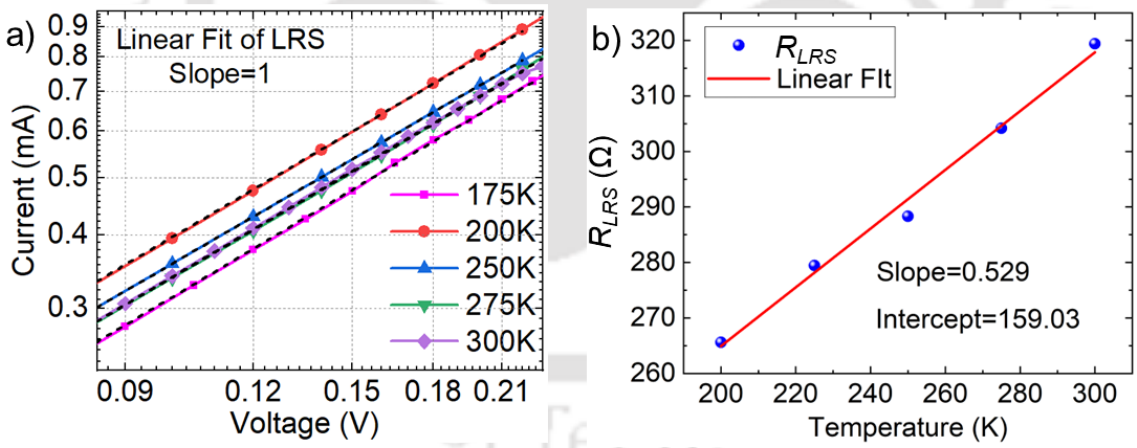


Figure 6.10: (a) The I-V plots of the BA_2PbI_4 memristor in log-log scale taken at different temperatures (200K to 300K). The black lines show the linear fitting of the LRS regions. (b) Variation of R_{LRS} values with temperature. The linear fitting of this plot yields a slope of 0.529 and intercept of 159.03, from which the temperature coefficient of resistance is found to be 3.30×10^{-3} K^{-1}.

In another indirect method, the resistivity of the CF was calculated from the typical diameter of a CF, which was reported to be 8-10 nm in the literature [25]. Assuming a diameter of 10 nm and length of 486 nm (i.e., thickness of BA_2PbI_4 film

here), a resistivity of 5.17×10^{-8} Ω.m has been calculated at 300K. Bid *et al.* showed that the resistivity of silver nanowire is indirectly proportional to its diameter and is much greater than that of bulk silver [21]. They have obtained a resistivity value of 4.11×10^{-8} Ω.m for a nanowire diameter of 15 nm. This appears to support our argument that the CF is composed of silver with a minimum diameter of 10 nm and a resistivity of 5.17×10^{-8} Ω.m. However, to find a conclusive evidence of the CF constituents, advanced characterization techniques need to be used such as cross-sectional FESEM with EDEX microscopy for in-situ visualization of the formation/rupture of the CF, deep level transient spectroscopy (DLTS) to analyze the ionic landscape in the device during operation, etc.

6.4.2 Temperature Dependence of HRS Current

Figure 6.11(a) shows that the R_{HRS} decreases with temperature, indicating a negative temperature coefficient that is typically semiconductor-like. An Arrhenius plot was generated by plotting the HRS current in log scale ($\ln(I_{HRS})$) against inverse temperature $(1/kT)$, where k is the Boltzmann constant and T is the absolute temperature (see figure 6.11(b)). The thermal activation energy (E_a) was estimated using the equation (6.2) below [7,26].

$$\ln(I_{HRS}) = \ln(I_o) - \frac{E_a}{kT} \tag{6.2}$$

Here, I_o is the device HRS current at absolute zero. We obtained two different values of E_a in two temperature ranges - 0.03 eV between 200K to 250K and 0.11 eV near room temperature. The smaller E_a value at low temperatures may be associated with the shallow traps near the conduction band. The E_a value increases as the deeper traps get activated at higher temperatures, and subsequently, the HRS of the device decreases [7].

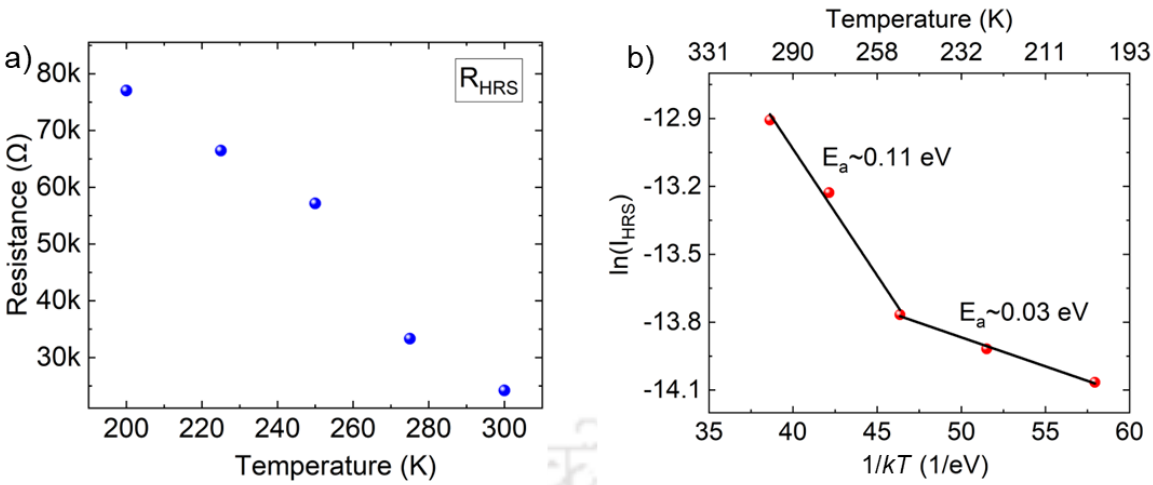


Figure 6.11: (a) Variation of R_{HRS} values in the temperature range 200K to 300K, and (b) $\ln(I_{HRS})$ vs $1/kT$ plot and corresponding E_a values obtained from linear fit (I_{HRS} was calculated from the I-V plots at 0.05 V).

6.5 SPICE Simulation of 2D HOIP Memristors

To simulate the I-V characteristics 2D HOIP memristor using the algorithm that has been discussed in the previous chapter, we first plotted the I-V and *di/dv* plots, as shown in figure 6.12. The threshold voltages V_p and V_n were extracted from the peak values of the rate of change of current, which were found to be 0.60 V and 0.26 V in the positive and negative voltage regimes, respectively. The peaks in the rate of change of conductance plot (see the points marked in red circles in the top plot of figure 6.12(b)) give the values of maximum conductivity changes $g_{pk,p}$ and $g_{pk,n}$. The points next to these values in the conductivity plot correspond to the parameters $g_{slow,p}$ and $g_{slow,n}$ (see the points marked in red circle in the bottom plot of figure 6.12(b)). From these extracted parameters, A_p, A_n, x_p, and x_n were calculated and listed in table 6.2.

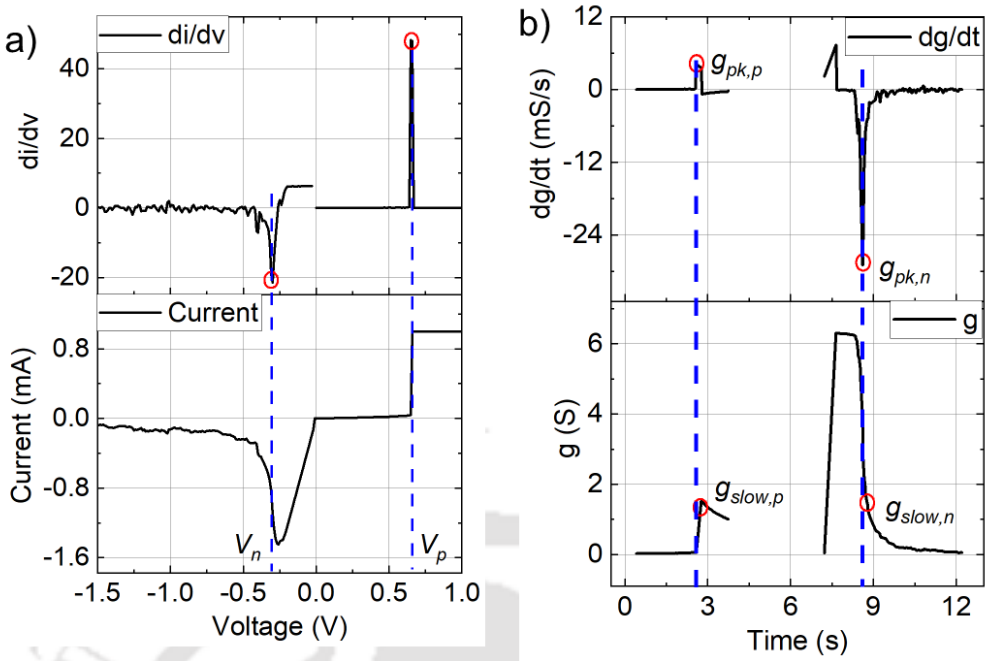


Figure 6.12: (a) Calculation of threshold voltages (V_p and V_n) from the maximum slope points of the I-V characteristics. (b) Conductance and rate of conductance change versus time plots from which the values of $g_{pk,p}$, $g_{pk,n}$, $g_{slow,p}$, and $g_{slow,n}$ were calculated.

Table 6.2: Extracted values of the fitting parameters for the 2D HOIP memristor

Parameters	**Type A**
V_p (V)	0.60
V_n(V)	-0.26
g_{max}(mS)	6.11
g_{min}(µS)	33.10
$A_p(s^{-1})$	2.67x10^2
$A_n(s^{-1})$	9.86
x_p	0.2458
x_n	0.4469
b	0.9738

Piecewise fitting of the 2D memristor I-V characteristics shows that the LRS region fits to a linear function indicating ohmic conduction. The HRS region fits to a sine hyperbolic function indicating that the current is limited by a tunnelling mechanism. These fitting results are shown in figure 6.13(a), from which g_{max}, g_{min}, and b have been

calculated. These fitting parameters were then used in SPICE for the complete emulation of I-V curves of 2D memristor. Figure 6.13(b) shows the fitting results of the experimental I-V plots to the model equations which yields a per-cycle mean error <9.49%. The mean errors in the SET and REST cycles were 2.76% and 11.67%, respectively.

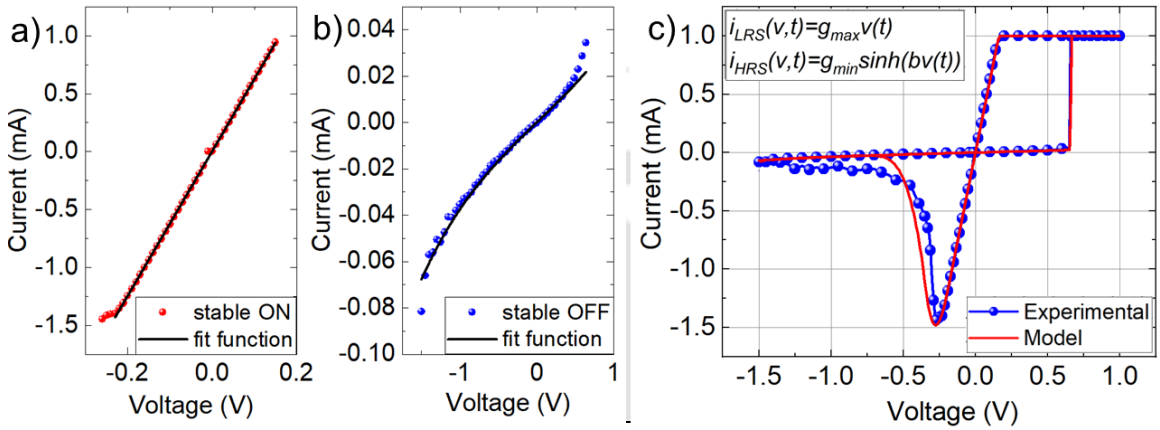


Figure 6.13: (a) Piecewise fitting of the LRS and HRS regions of the experimental I-V characteristics and their corresponding fitting to linear and sin hyperbolic function. (b) Fitting of experimental I-V plot to the analytical model for the HOIP memristor.

6.6 Summary

We have prepared pure 2D (n=1) and quasi-2D (n=2 and 3) Ruddleson Popper perovskite films using $BA_2MA_{n-1}Pb_nI_{3n+1}$. XRD and UV-vis absorption spectroscopy confirm the formation of the desired dimensionality in each of these films. The Tauc plots derived from the UV-vis absorption spectroscopy show that the band gap of the HOIP films increases from 1.95 eV to 2.33 eV as the dimensionality reduces from n= ∞ to 1. Subsequently, following the similar fabrication methods that were used for 3D HOIP memristor, pure 2D BA_2PbI_4 memristors were fabricated. These devices exhibited V_{SET} and V_{RESET} of 0.64 V and -0.33 V, respectively, along with an ON/OFF ratio of 1.36×10^3. The repeatability of RS in these devices was tested by using voltage pulses, which yielded a cyclic endurance of 1050 cycles and state retention for 1350 seconds with a consistent ON/OFF ratio of ~100. When tested over a period of 96 hours, the unencapsulated 2D devices showed more stable RS action compared to their 3D counterparts. At the end of

fourth day, the ON/OFF ratio of 2D HOIP memristor was reduced by a factor of only 22. It was also found that the ON/OFF ratio increases with the thickness of the HOIP layer. However, devices with thicker HOIP require higher magnitudes of $V_{FORMING}$, V_{SET}, and V_{RESET}. Low temperature analysis of 2D HOIP memristor characteristics in LRS indicates filamentary conduction via silver ions from the top electrode. The activation energies of traps in HRS were 0.03 eV in the temperature range 200K to 250K and 0.11 eV near room temperature. The smaller E_a value at low temperatures may be associated with the shallow traps near the conduction band. The E_a value increases as the deeper traps get activated at higher temperatures, and subsequently, the R_{HRS} of the device decreases. Furthermore, the current conduction in the LRS is found to be ohmic and that in HRS is tunneling dominated. SPICE simulation of the I-V characteristics of 2D HOIP memristors using the modified Yakopcic model yielded a per cycle mean error of 9.49%.

6.7 References

[1] H. Tsai *et al.*, "High-efficiency two-dimensional Ruddlesden-Popper perovskite solar cells," Nature, vol. 536, no. 7616, pp. 312–316, 2016.

[2] E. B. Kim *et al.*, "A review on two-dimensional (2D) and 2D-3D multidimensional perovskite solar cells: Perovskites structures, stability, and photovoltaic performances," Journal of Photochemistry and Photobiology C, vol. 48, no. 100405, p. 100405, 2021.

[3] A. Solanki *et al.*, "Interfacial mechanism for efficient resistive switching in ruddlesden-Popper perovskites for non-volatile memories," Journal of Physical Chemistry Letters, vol. 11, no. 2, pp. 463–470, 2020.

[4] H. Kim *et al.*, "Quasi-2D halide perovskites for resistive switching devices with ON/OFF ratios above 10^9," NPG Asia Materials, vol. 12, no. 1, pp. 1–11, 2020.

[5] X. Zhang *et al.*, "Phase transition control for high performance ruddlesden–popper perovskite solar cells," Advanced Materials, vol. 30, no. 21, p. 1707166, 2018.

[6] L. Mao *et al.*, "Hybrid Dion–Jacobson 2D lead iodide perovskites," Journal of the American Chemical Society, vol. 140, no. 10, pp. 3775–3783, 2018.

[7] J.-Y. Seo *et al.*, "Wafer-scale reliable switching memory based on 2-dimensional layered organic-inorganic halide perovskite," Nanoscale, vol. 9, no. 40, pp. 15278–15285, 2017.

[8] A. D. Taylor *et al.*, "A general approach to high-efficiency perovskite solar cells by any antisolvent," Nature Communications, vol. 12, no. 1, p. 1878, 2021.

[9] K. A. Parrey *et al.*, "Synthesis and characterization of an efficient hole-conductor free Halide perovskite $CH_3NH_3PbI_3$ Semiconductor absorber based photovoltaic device for IoT," Journal of the Electrochemical Society, vol. 165, no. 8, pp. B3023–B3029, 2018.

[10] S. Y. Kim *et al.*, "Layered $(C_6H_5CH_2NH_3)_2CuBr_4$ perovskite for multilevel storage resistive switching memory," Advanced Functional Materials, vol. 30, no. 27, p. 2002653, 2020.
[11] D. H. Cao *et al.*, "2D homologous perovskites as light-absorbing materials for solar cell applications," Journal of the American Chemical Society, vol. 137, no. 24, pp. 7843–7850, 2015.
[12] H. Tian *et al.*, "Extremely low operating current resistive memory based on exfoliated 2D perovskite single crystals for neuromorphic computing," ACS Nano, vol. 11, no. 12, pp. 12247–12256, 2017.
[13] "Halide Perovskite: Observing Phase Transitions in a Halide Perovskite," Edinburgh Instruments, 15-May-2018. [Online]. Available: https://www.edinst.com/in/phase-transitions-halide-perovskite/.
[14] H. R. Byun *et al.*, "Temperature driven phase transition of organic-inorganic Halide perovskite single crystals," Journal of the Korean Physical Society, vol. 73, no. 11, pp. 1729–1734, 2018.
[15] F. Lehmann *et al.*, "The phase diagram of a mixed halide (Br, I) hybrid perovskite obtained by synchrotron X-ray diffraction," RSC Advances, vol. 9, no. 20, pp. 11151–11159, 2019.
[16] J. Sun *et al.*, "In situ observation of nickel as an oxidizable electrode material for the solid-electrolyte-based resistive random access memory," Applied Physics Letters, vol. 102, no. 5, p. 053502, 2013.
[17] S. Gao *et al.*, "Dynamic processes of resistive switching in metallic filament-based organic memory devices," Journal of Physical Chemistry C, vol. 116, no. 33, pp. 17955–17959, 2012.
[18] R. A. Serway, and J. W. John, "Principles of physics," Vol. 1. Fort Worth, TX: Saunders College Pub., 1998.
[19] D. J. Griffiths, "Introduction to electrodynamics." 574-574, 2005.
[20] D. Kojda *et al.*, "Temperature-dependent thermoelectric properties of individual silver nanowires," Physical Review B, vol. 91, no. 2, p. 024302, 2015.
[21] A. Bid *et al.*, "Temperature dependence of the resistance of metallic nanowires of diameter⩾15nm: Applicability of Bloch-Grüneisen theorem," Physical Review B, vol. 74, no. 3, p. 035426, 2006.
[22] K. Yan *et al.*, "High-performance perovskite memristor based on methyl ammonium lead halides," Journal of Materials Chemistry C, vol. 4, no. 7, pp. 1375–1381, 2016.
[23] E. Yoo *et al.*, "Bifunctional resistive switching behavior in an organolead halide perovskite based Ag/$CH_3NH_3PbI_{3-x}Cl_x$/FTO structure," Journal of Materials Chemistry C, vol. 4, no. 33, pp. 7824–7830, 2016.
[24] Y. Sun *et al.*, "Competition between metallic and vacancy defect conductive filaments in a $CH_3NH_3PbI_3$-based memory device," Journal of Physical Chemistry C, vol. 122, no. 11, pp. 6431–6436, 2018.
[25] Z. Wei *et al.*, "Demonstration of high-density ReRAM ensuring 10-year retention at 85°C based on a newly developed reliability model," in 2011 International Electron Devices Meeting (IEDM), p. 31.4.1-31.4.4, 2011.
[26] C. Gu and J.-S. Lee, "Flexible hybrid organic-inorganic perovskite memory," ACS Nano, vol. 10, no. 5, pp. 5413–5418, 2016.
[27] K. Yan *et al.*, "First fiber-shaped non-volatile memory device based on hybrid organic-inorganic perovskite," Advanced Electronic Materials, vol. 2, no. 8, p. 1600160, 2016.

[28] Z. Xu *et al.*, "To probe the performance of perovskite memory devices: defects property and hysteresis," Journal of Materials Chemistry C, vol. 5, no. 23, pp. 5810–5817, 2017.

[29] N. F. Mott, , and R. W. Gurney. Electronic processes in ionic crystals. Clarendon Press, 1948.

[30] P. N. Murgatroyd, "Theory of space-charge-limited current enhanced by Frenkel effect," Journal of Physics D: Applied Physics, vol. 3, no. 2, pp. 151–156, 1970.

[31] J. C. Scott and G. G. Malliaras, "Charge injection and recombination at the metal-organic interface," Chemical Physics Letters, vol. 299, no. 2, pp. 115–119, 1999.

CHAPTER 7

Conclusion, Limitations and Future Prospects

Contents

In this chapter, we summarize the major contributions of this thesis on design, characterization, and modelling of HOIP memristors. To get a perspective on the limitations and future prospects, we compare the switching parameters of our devices with the values targeted by the research community, as given in the Institute of Electrical and Electronics Engineers' (IEEE) International Roadmap for Devices and Systems (IRDS), 2021, and also with those of the state-of-the-art oxide-based memristors.

7.1 Summary of Contributions

7.1.1 Characterization of Chalcogenide Memristors

Five different forming methods have been used to form pristine chalcogenide memristors. The devices formed using the positive voltage sweep method have been found to give the most repeatable switching characteristics. It has been found that a slower SR leads to relatively small forming and switching voltages that help to reduce the power consumption during switching. On the other hand, a higher I_{CC} leads to a better ON/OFF ratio, but at the cost of higher V_{RESET}. Therefore, obtaining the optimum performance out of the memristor involves a trade-off between power consumption and noise margin; hence, selecting proper characterization parameters is essential for any new memristive device and such parameters have been identified.

7.1.2 Fabrication and Characterization of 3D HOIP Memristors

We have fabricated 3D HOIP memristive devices using $MAPbI_3$ perovskite, using simple solution processing at low temperatures. Toluene as an antisolvent during perovskite layer coating gave superior performance owing to improved perovskite film morphology. $V_{FORMING}$, R_{HRS}, and ON/OFF ratios were found to be area dependent. In case of voltage pulse characterization, the ON/OFF ratio can be enhanced by increasing the pulse amplitude and width. We have incorporated the same $MAPbI_3$ memristors on flexible PET substrates, which gave repeatable RS. The flexible devices showed stable switching under normal conditions as well as under applied mechanical stress.

7.1.3 Model for SPICE Simulation of HOIP Memristor Characteristics

Two different types of BRS have been demonstrated in the same HOIP device with the application of electric fields of opposite polarities for the first time. The type of switching can be controlled by the proper selection of the polarity of the operating field and I_{CC}. RS characteristics resembling CRS behaviour have also been demonstrated using the same memristor. This could be useful in mitigating sneak-path currents without the requirement of any additional selector devices in crossbar ReRAMs, making it possible to achieve higher device densities. Furthermore, a novel strategy to mimic memristive characteristics using extraction of fitting parameters from experimental data has been developed, inspired from the standard SPICE-based Yakopcic model of memristor. This simulation model has been validated by fitting to the two different types of switching obtained from the fabricated $MAPbI_3$ memristors. The piecewise experimental data fitting showed that the HRS current in our HOIP memristors was dominated by the tunnelling mechanism in one case and by diffusion current in the other. On the other hand, both types of switching showed ohmic conduction in their ON state.

7.1.4 Fabrication and Characterization of 2D HOIP Memristors

Lower dimensional RP perovskites were prepared by solution processing techniques, and the dimensionality of the HOIP films has been varied. We have fabricated memristors using 2D BA_2PbI_4 perovskite. The ambient stability of the unencapsulated 2D HOIP memristors has been found to be superior as compared to their 3D counterparts. In addition to the typical I-V characterization, endurance and retention tests were performed using fast voltage pulses to evaluate the reliability of the devices. Furthermore, low-temperature electrical characterization in the range 200K to 300K showed that R_{HRS} decrease and R_{LRS} increase with temperature. The device current during LRS was found to be ohmic due to filamentary conduction and HRS current conduction was tunneling

dominated. The algorithim for SPICE simulation developed for 3D HOIP memristors worked resonably well for these 2D devices as well.

7.2 Limitations and Future Prospects

The desirable characteristics for a memory device include fast write/read speed, low operation voltage, low energy consumption, long data retention time, long write/read cycling endurance, and excellent scalability. However, no practical memory device has been reported to simultaneously satisfy all these characteristics to date. Among the various emerging memory technologies, oxide-based ReRAMs have been extensively studied for the longest time and their parameters, relative to other technologies, are closer to the projected values. On the other hand, HOIP memristors are promising, but still are in a very nascent research stage, not withstanding the fact that a few of its parameters have already reached close to the ideal values as was shown in chapter 2.

The best projected values of parameters for any RS-based non-volatile memory technology and the best performance obtained from oxide-based ReRAM are shown in Table 7.1 [1-3], along with the parameters of three different memristors fabricated in this thesis work.

Table 7.1: Comparison of memristor parameters fabricated in this thesis work with the IEEE IRDS target values and with those of the best oxide-based ReRAMs [1-3].

Memristor Parameters	**Roadmap Values**	**Best Values Demonstrated in Oxide-based ReRAM**	**Parameter Values Obtained from Our Work**		
			3D HOIP Memristor	**3D HOIP Flexible Memristor**	**2D HOIP Memristor**
Operation Voltage	<1 V	0.1 V	0.17 V	0.49 V	0.64 V
Endurance	>10^{12} cycles	10^{12} cycles	>10^3 cycles*	>10^3 cycles*	>10^3 cycles*
Feature Size	<5 nm	3 nm	100 µm	100 µm	100 µm
Write/Read Speed	<1 ns	85 ps	<1 µs*	<1 µs*	<1 µs*
Energy Consumption	~0.1 fJ	20 fJ	3.44 nJ*	7.31 nJ*	10.61 nJ*
Retention Time	>10 years	>10 years (50 days @250°C)	3.3x10^3 s @RT#	1.2x10^3 s @RT#	1.4x10^3 s @RT#
ON/OFF Ratio	>10^6	3x10^6	1.3×10^3	7.6x10^2	1.36x10^3

*These values were limited by the smallest voltage pulse that can be applied in our characterization setup, which is 1 µs. #To get accelerated retention data in years, this characterization needs to be done at varying temperatures, which was not possible in our characterization setup.

It is clear from the Table 7.1 that, although the optimized results from our HOIP memristors are promising, the structure and fabrication process need to be improved to reach the performance of oxide-based ReRAMs. However, it is important to note here that, many of the parameters that we have calculated for our devices are limited by the fabrication facilities and the characterization systems used for this work. The performance parameters can be further optimized with the use of different HOIPs and more capable characterization systems. In future, different fabrication methods also need to be explored to reduce device sizes.

Although lower dimensional HOIPs result in better ambient stability than their 3D counterparts, to implement them in practical commercial devices, the toxicity of lead and stability issue need to be addressed. This demands the use of lead-free perovskites based on tin (Sn), bismuth (Bi), germanium (Ge) etc. Encapsulating the devices and redesigning the device architecture with an additional protective layer between HOIP and the electrode is another necessary future work, which can improve the stability further.

In addition, our work explored only discrete type memristor I-V characteristics (abrupt switching) which are suitable for non-volatile memory applications. However, the gradual type of I-V characteristics (smooth switching) also has immense potential in the field of artificial synapse and brain-inspired computing applications. Physical Unclonable Functions (PUFs) is one of the most promising hardware cryptographic primitives capable of generating random, unique, secret bit-strings on the fly. Due to their inherent stochastic nature, the HOIP memristors are promising candidates for such data security applications and other true random number generators. In future, such emerging applications of the HOIP memristors can be explored using them in the form of a crossbar array.

The memristor model demonstrated in this thesis for SPICE simulation, in its current form, is elementary in nature. The physical significance of all the fitting

parameters used in the model need to be understood in terms of device dimensions and measurement parameters. In such a case, our model can be extended to a complete automated package for memristor simulation with HOIPs or any other similar materials.

The next logical step of this research work is to implement the HOIP memristors in the form of crossbar architecture. This architecture can achieve the theoretical lithographically realizable minimum cell size of $4F^2$, where F is the minimum feature size. In addition, multilevel RS memristors can also be realized by exploiting some IRS that were observed. This will enhance the storage density without much change in the technology and will open up the application of these memristors for 'in-memory computing'.

7.3 References

[1] "International roadmap for devices and systems (IRDSTM)," 2021, Available online at: https://irds.ieee.org/editions/2021.
[2] S. Yu, "Resistive Random Access Memory (RRAM): From devices to array architectures," Cham: Springer International Publishing, 2016.
[3] M. Lanza *et al.*, "Recommended methods to study resistive switching devices," Advanced Electronic Materials, vol. 5, no. 1, p. 1800143, 2019.

List of Publications

Journal Publications

1. H. J. Gogoi and A. T. Mallajosyula, “Multifunctional bipolar and complementary resistive switching in HOIP memristors by the control of compliance current,” ACS Appl. Electron. Mater., vol. 4, no. 3, pp. 1039–1046, 2022.
2. H. J. Gogoi *et al.*, **“**Advances in flexible memristors with hybrid perovskites,” J. Phys. Chem. Lett., vol. 12, no. 36, pp. 8798–8825, 2021.
3. H. J. Gogoi and A. T. Mallajosyula, “Enhancing the switching performance of $CH_3NH_3PbI_3$ memristors by the control of size and characterization parameters,” Adv. Electron. Mater., vol. 7, no. 11, p. 2100472, 2021.
4. H. J. Gogoi and A. T. Mallajosyula, “A comparative study on the forming methods of chalcogenide memristors to optimize the resistive switching performance,” J. Phys. D Appl. Phys., vol. 53, no. 44, p. 445108, 2020.

Conference Publications

1. H. J. Gogoi *et al.*, **“**Effect of antisolvent method on the performance of HOIP based memristive devices,” in 2018 4th IEEE International Conference on Emerging Electronics (ICEE), pp. 1–5, 2018.
2. H. J. Gogoi *et al.*, “Ionic Defect Analysis in Flexible Hybrid Perovskite Memristor using Deep Level Transient Spectroscopy” in IEEE International Flexible Electronics Technology Conference 2022, China, August 21-24, 2022.

Oral Talks and Presentations

1. “SPICE Simulation of Hybrid Organic-Inorganic Perovskite Memristive Devices” in the 7th International Conference on Advanced Nanomaterials and Nanotechnology (ICANN2021), 14-17 December 2021.
2. “Measurement Process-Dependent Performance and Conduction Mechanism of Hybrid Perovskite Memristors” in International Conference on Perovskite Memristors and Electronics 2021 (ICPME21), 13 and 14th December 2021.