**INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI**
**SHORT ABSTRACT OF THESIS**

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Thesis Title : **Large scale circuit placement and partitioning using nonlinear analytical optimization methods**

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## SHORT ABSTRACT


VLSI circuit placement and partitioning are critical steps of the VLSI circuit design flow. Adoption of an optimal placement policy is essential to the optimal performance of the electronic circuit. Due to technology scaling and integration of a large number of transistors on silicon, efficient floorplanning, placement and routing have become of paramount importance. Rapid prototyping of the electronic systems has been linked with placement directly and it has become an important parameter of the process yield. Therefore, partitioning and circuit placement methodologies need to be revisited again for improving yield during the process steps and to optimize post-fabrication performance of the electronic circuits.

In this thesis, an analytical approach is presented which is based on the nonlinear programming to perform VLSI standard cell placement and an indigenous placement tools Kapees3 has been developed incorporating our proposed method. Kapees3 first clusters a netlist to reduce the number of cells and then performs quadratic optimization on the reduced netlist to initialize the placement solution. Finally, it uses Nesterov's method to analyze nonlinear equations for the given problem. Kapees3 is capable of performing placements of large size circuits, for example circuit composed of 12 Million cells, efficiently and its results have been verified by using standard benchmark evaluation methods. The experimental results for PEKO Suite 1, PEKO Suite 2, MMS and Free MMS benchmarks show promising improvements in terms of Half Perimeter Wirelengh (HPWL).

Kapees3 outperforms NTUPlace3, Dragon, Feng Shui, Capo by 46%, 57%, 48% and 25%, respectively, on PEKO Suite 1, while for PEKO Suite 2, it demonstrates better performance as compared to NTUPlace3, Dragon, Feng Shui, Capo and mPL6 by 30%, 47%, 57%, 69% and 2.7%, respectively. On MMS benchmarks, Kapees3 obtains wirelength improvement over Capo by 56.62%, FLOP by 7.84%, FastPlace by 11.55%, ComPLx by 4.58%, POLAR by 23.67%, mPL6 by 9.96%, NTUPlace3-NR by 0.74% and NTUPlace3 by 0.46%. On Free MMS benchmarks, it outperforms NTUPlace3 and ComPLx by 32.52% and 5.73%, respectively, in terms of HPWL.

The proposed methodology is applied to the placement of 3D-ICs. Kapees3 exhibits 16.4% improvement over F3D when wirelength is considered for the optimization and demonstrates an improvement of 52% in the number of Through Silicon Vias (TSVs) when the goal is to minimize usage of TSVs. This method has also been extended for the placement of cells over FPGA where a speedup of 750% is illustrated by Kapees3 when compared to a well-known FPGA placement tool VPR without affecting HPWL greatly.

Hypergraph partitioning is commonly used in solving VLSI placement problem, data mining, sparse matrix multiplication, and parallel computing. For a balanced partitioning, it is imperative to achieve equal size blocks with minimum interconnection among the blocks. In this thesis a novel heuristic is presented for partitioning hypergraphs based on nonlinear programming. In the proposed method, one dimensional physically adjacent bins are considered for the placement of vertices. Since the reduction of min-cuts is equivalent to reducing wirelength of the nets across two bins, the vertices are moved across the bins in such a way that the density of vertices in each bin is balanced and wirelength is optimized as per the constraints imposed for obtaining balance partitions. The proposed method produces better cut-cost as compared to FMpart, which is an open source hypergraph partitioner based on the Fiduccia Mattheyses (FM) heuristic. It is validated for producing 2-way optimal hypergraph partitions and can be extended for k-way hypergraph partitioning.

A nonlinear analytical partitioning tool, NAP, has been developed using proposed methodology and has been tested with various standard benchmarks. For the Walshaw hypergraph partitioning benchmarks, performance of NAP is consistently comparable with the performance of Chaco. It produces better min-cuts than Chaco on 22 out of 29 testcases. On ISPD98 hypergraph partitioning benchmarks, NAP outperforms FMpart on 17 out of 18 testcases and obtains an improvement of 111.5% in terms of quality of cut.

Further, partition driven placement approach is also explored and it is further improved by applying simulated annealing method for wirelength reduction. The experiments verify that the half perimeter wire lengths (HPWLs) obtained for the benchmark circuits designs by our proposed methodology are on an average 9% and 5% less as compared to HPWLs obtained using Amoeba and Capo, respectively.

In this thesis, we have investigated placement of large scale VLSI circuits in detail using nonlinear programming and partitioning based approaches and exhibits better performance of the proposed methodology to well-known standard placement and partitioning heuristics.