DESIGN AND ANALYSIS OF BALANCED-TO-UNBALANCED AND UNBALANCED-TO-BALANCED POWER DIVIDERS

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DESIGN AND ANALYSIS OF BALANCED-TO-UNBALANCED AND UNBALANCED-TO-BALANCED POWER DIVIDERS

A

Thesis submitted

for the award of the degree of

DOCTOR OF PHILOSOPHY

By

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GUWAHATI - 781 039, ASSAM, INDIA

March 2018

Certificate

This is to certify that the thesis entitled "**DESIGN AND ANALYSIS OF BALANCED-TO-UNBALANCED AND UNBALANCED-TO-BALANCED POWER DIVIDERS**", submitted by **Amar Nath Yadav** (136102026), a research scholar in the *Department of Electronics and Electrical Engineering, Indian Institute of Technology Guwahati*, for the award of the degree of **Doctor of Philosophy**, is a record of an original research work carried out by him under my supervision and guidance. The thesis has fulfilled all requirements as per the regulations of the institute and in my opinion has reached the standard needed for submission. The results embodied in this thesis have not been submitted to any other University or Institute for the award of any degree or diploma.

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To

My dear parents

Radhey Shyam Yadav and Narbada Yadav

&

My Wife

Neha Yadav

for their love and support

Acknowledgements

First and foremost, I feel it as a great privilege in expressing my deepest and most sincere gratitude to my supervisor Prof. Ratnajit Bhattacharjee, for his excellent guidance throughout my study. His kindness, dedication, hard work and attention to detail have been a great inspiration to me. My heartfelt thanks to you sir for the unlimited support and patience shown to me. I have no doubts that finishing my degree in a proper and timely manner was impossible without his help, suggestions and advices.

I am also very thankful to my doctoral committee members Prof. Anup Kumar Gogoi, Prof. Kshetrimayum Rakhesh Singh and Dr. Nagarjuna Nallam for sparing their precious time to evaluate the progress of my work. I am also thankful to Director IIIT Guwahati, Prof. Gautam Barua for providing proper support for carrying out my research.

I would also like to thank the Head of the Department and the other faculty members for their kind help in carrying out this work. I am also grateful to all the members of the research and technical staff of the department without whose help I could not have completed this thesis. My special thanks to Utpal Kumar Sarma sir and Dimpul Gogoi sir, for helping me to fabricate all circuits.

Thanks go out to all my friends at the Microwave Engineering research group and my colleagues from IIIT Guwahati. They have always been around to provide useful suggestions, companionship and created a peaceful research environment. They all contributed directly or indirectly to this thesis, be it academic help, proofreading and volunteering to be a test subject.

I have no words to express my thanks to my colleagues and friends at IIIT Guwahati, Mohd. Mansoor Khan, Sanjay Moulik and Gitimoni Saikia. My work in this remote place definitely would not be possible without their love and care that helped me to enjoy my new life in IITG and IIITG.

My special thanks to Head of the Department ECE at IIIT Guwahati, Dr. Bidisha Dasgupta for her timely help in all respects. I am very thankful to her for providing all necessary infrastructure to carry out my research in IIIT Guwahati.

My deepest gratitude goes to my family for their continuous love and support throughout my studies. The opportunities that they have given me and their unlimited sacrifices are the reasons where I am and what I have accomplished so far.

Amar Nath Yadav

Abstract

This research deals with various types of balanced-to-unbalanced and unbalanced-to-balanced power dividers. Balanced circuits are used to suppress common-mode noise and it has high immunity to crosstalk. To design a fully balanced transceiver, various types of balanced circuits are required. Among those balanced circuits, balanced power dividers are very important. It is used to divide the power equally or in a specific ratio. A balanced-to-unbalanced power divider, with a balanced input and several single-ended outputs, is suitable to feed unbalanced loads such as monopole antenna elements from a balanced amplifier. Similarly, an unbalanced-to-balanced power divider is suitable to feed a balanced antenna array from an unbalanced source.

In this thesis, various types of balanced-to-unbalanced power dividers are proposed. Two Gysel type equal power dividers are analyzed, designed and fabricated, one for in-phase (phase difference between output signals is 0°) and the other for out-of-phase (phase difference between output signals is 180°) application. Another Wilkinson type equal power divider is also analyzed, designed and fabricated for out-of-phase application. Complete theoretical analysis of balanced-to-unbalanced power divider for arbitrary power division is also presented. Two power dividers of power division ratio 1:2 have been designed, fabricated and measured, one for in-phase and other is for out-of-phase application.

Two unbalanced-to-balanced power divider configurations are proposed, which are of Gysel type. First one is for equal power division and the second one is for arbitrary power division ratio. Complete theoretical analysis of the power divider is presented. The power divider for arbitrary power division ratio is designed and fabricated for power division ratio of 1:2.

For dual-band applications, one balanced-to-unbalanced power divider is analyzed, designed and fabricated. The proposed power divider is for equal power division and phase difference between output signals is 180°. Another dual-band single-ended power divider for arbitrary power division ratio is also designed and fabricated. This is a coupled line based power divider. This power divider is designed for power division ratio of 1:2. The measured results for different power dividers are found close to analytical and simulation results.

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List of Acronyms

BTU	Balanced-to-Unbalanced
DUT	Device Under Test
HFSS	High Frequency Structural Simulator
MM	Mixed Mode
OC	Open Circuit
PD	Power Divider
RF	Radio Frequency
S	Scattering
SC	Short Circuit
UTB	Unbalanced-to-Balanced
VNA	Vector Network Analyzer

List of Publications

Journal Publications

1. A. N. Yadav and R. Bhattacharjee, "Balanced to Unbalanced Power Divider With Arbitrary Power Ratio," in *IEEE Microwave and Wireless Components Letters*, vol. 26, no. 11, pp. 885-887, Nov. 2016.

2. A. N. Yadav and R. Bhattacharjee, "Unbalanced-to-Balanced Power Divider With Arbitrary Power Division" in *Progress in Electromagnetic Research C*, vol. 76, pp. 43-54, 2017.

3. A. N. Yadav and R. Bhattacharjee, "Dual-band balanced-to-unbalanced out-of-phase equal power divider" in *Microwave and Optical Technology Letters*, vol. 59, pp. 2078-2083, 2017.

4. A. N. Yadav and R. Bhattacharjee, "Coupled line based unequal dual band power divider" in *Microwave and Optical Technology Letters*, vol. 58, pp. 953-956, 2016.

Conference Publications

1. A. N. Yadav and R. Bhattacharjee, "Balanced to Unbalanced Out of Phase Equal Power Divider for Wide-band Application," *2016 Asia-Pacific Microwave Conference (APMC)*, New-Delhi, 2016.

2. A. N. Yadav and R. Bhattacharjee, "Balanced-to-Unbalanced Out-of-Phase Wilkinson Equal Power Divider," *2017 Twenty Third National Conference on Communication (NCC)*, Chennai, 2017.

3. A. N. Yadav and R. Bhattacharjee, "Gysel Type Unbalanced-to-Balanced Equal Power Divider," *2017 47th European Microwave Conference (EuMC)*, Nuremberg, 2017.

4. A. N. Yadav and R. Bhattacharjee, "Balanced-to-Unbalanced In-Phase Power Divider" *2017 International Microwave and RF Conference (IMaRC), Ahmedabad, 2017.*

1

Introduction

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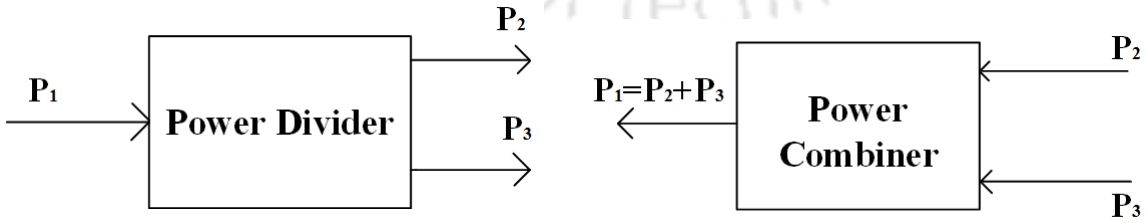
To meet the requirement of the emerging wireless communication technologies, radio frequency (RF) circuits having compact size, tunability and multi-band operations are required to be designed. Power dividers (PDs) are used for power splitting/combining in various microwave applications such as power amplifiers, mixers, and frequency multipliers [1–7]. Power dividers used in various microwave and wireless communication systems, require to provide low insertion loss and high isolation between output ports. In many cases, power dividers are designed with equal power division to different outputs [1]. However, in some cases, power dividers with arbitrary power division ratios are also desired, especially as feed networks of antenna arrays [8–15]. For the high power application, Gysel power divider configuration is very useful as it can transfer heat to the ground plane effectively [2, 16–20].

In this chapter, some basic concepts related to power divider are presented. This chapter also presents the motivation for the works presented in the thesis, highlights thesis contribution and organization of the thesis.

1.1 Conventional Power Divider

A basic power divider is a three-port device. Power divider/combiner is used to divide/combine the power. Basic block diagram of power divider/combiner is shown in Fig. 1.1. As shown in Fig. 1.1(a), input power P_1 is divided into output powers P_2 and P_3. The output power can be divided equally or in a specific power division ratio $k^2 = \frac{P_2}{P_3}$. For an equal power divider, $k^2 = 1$. A power divider can be used as power combiner if it operated as shown in Fig. 1.1(b). In this case, output power (P_1) is the sum of input powers (P_2 and P_3). Power divider can be further categorized as in-phase and out-of-phase power divider. In an in-phase power divider, phase difference between output signals is 0°. For an out-of-phase power divider, phase difference between output signals is 180°.



(a) (b)

Figure 1.1: (a) Power divider (b) Power combiner

As mentioned, a power divider is a three-port device. A three-port device can not be lossless, reciprocal and matched to all ports at the same time [3]. Therefore, in order to design a power divider, any one of these conditions has to be relaxed. Based on the above discussion, basically there are two types of power divider available in the literature, which are given as:

(i) Lossless Power Divider

(ii) Lossy Power Divider

1.1.1 Lossless Power divider

A power divider which is lossless and reciprocal but not matched to all ports is called as a lossless power divider. T-junction power divider is a basic form of lossless power divider. A T-junction power divider cannot be matched simultaneously at all ports. T-junction power divider can be modeled as a junction of three transmission lines, which is shown in Fig. 1.2. As shown in Fig. 1.2, power is divided from the input transmission line of characteristic impedance Z_0 to two transmission lines of characteristic impedances Z_1 and Z_2. If transmission lines are assumed to be lossless, then for power divider to be matched to input line, parallel combination of two output lines of characteristic impedances Z_1 and Z_2 should be equal to the characteristic impedance of input line Z_0 (neglecting junction discontinuity).

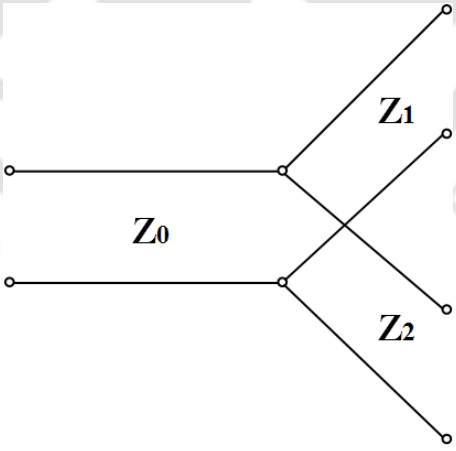


Figure 1.2: Transmission line model of T-junction power divider [3].

$$\frac{1}{Z_0} = \frac{1}{Z_1} + \frac{1}{Z_2} \tag{1.1}$$

To provide various power division ratios, output lines characteristic impedances Z_1 and Z_2 can be selected. For equal power division, if input line characteristic impedance is chosen as 50 Ω, then output lines characteristic impedance can be obtained from (1.1) as 100 Ω. By choosing an input line characteristic impedance as 50 Ω, input line is matched and output lines are not matched. To match output lines, quarter-wave transformer can be used. If output lines characteristic impedance is chosen as 50 Ω, then input line characteristic impedance can be obtained from (1.1) as 25 Ω. Therefore, in this case, the output lines are matched, but input line is not matched. One of the major drawback of this type of power divider is isolation. In this type of power divider, no isolation is there between two output ports.

1.1.2 Lossy Power divider

T-junction power divider is a lossless power divider, but has the disadvantage of not being matched at all ports and not providing isolation between output ports. A three-port power divider containing lossy elements can be reciprocal and made to be matched at all ports, although the two output ports may not be isolated [3]. An example of such circuit is a resistive power divider shown in Fig. 1.3.

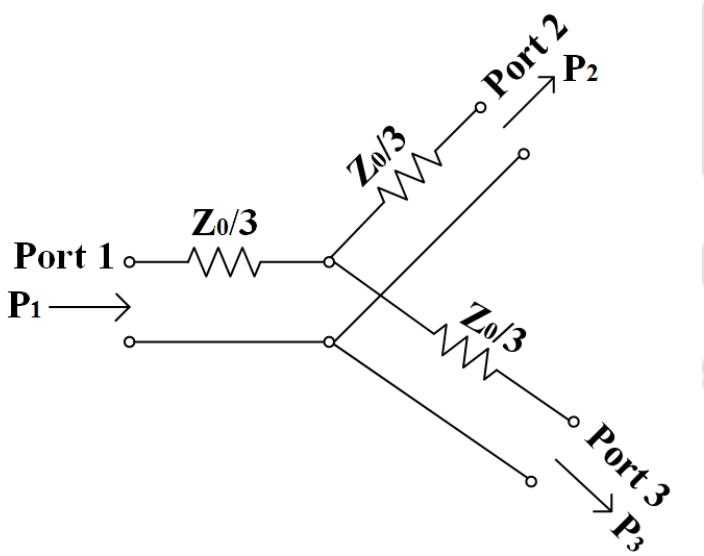


Figure 1.3: Three-port resistive power divider [3].

A resistive divider can be matched at all ports, and even though it is lossy, isolation between the output ports is still not achieved. From the properties of a three-port junction, it is known that for a lossy three-port network, all the ports can be matched with isolation between output ports. Two very

popular configuration of power dividers containing lossy elements and providing isolation between the output ports are:

(i) Wilkinson Power Divider

(ii) Gysel Power Divider

1.2 Wilkinson Power Divider

A Wilkinson power divider configuration contains a resistive element. Such configuration has the property of appearing lossless when the output ports are matched; the lossy element dissipates reflected power, if any, from the output ports. It can be designed for equal power division and for any specific power division ratio. It was first proposed by E.J. Wilkinson [1]. It provides the isolation between output ports. In Wilkinson power divider, isolation resistor is connected between the output arms [21–25]. Wilkinson power divider for equal power division is discussed first; followed by discussion on the power division in any specified ratio.

1.2.1 Wilkinson Equal Power Divider

The block diagram of basic Wilkinson equal power divider [3] is shown in Fig. 1.4. As shown in Fig. 1.4, there are two transmission lines of characteristic impedance Z_1 and electrical length $\pi/2$. Isolation resistor R is used to provide isolation between two output ports. Incoming power from input port 1 is equally divided between output ports 2 & 3, respectively. This is an in-phase power divider. This can be used as power combiner. Incoming power from ports 2 & 3 are combined at port 1.

Wilkinson equal power divider, as shown in Fig. 1.4, is symmetrical. To analyze a symmetrical circuit, even- and odd-mode analysis are used to derive the design equations (detailed derivation is available in [3], included here in Appendix-A for ready reference). The design equations for this power divider are given as:

$$Z_1 = \sqrt{2}Z_0 \tag{1.2}$$

$$R = 2Z_0 \tag{1.3}$$

If the port impedance Z_0 is taken as 50 Ω, then Z_1 and R are obtained from (1.2) and (1.3) as 70.71 Ω and 100 Ω, respectively.

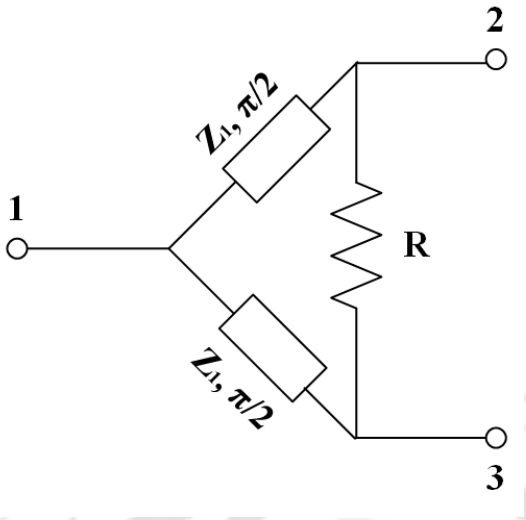


Figure 1.4: Wilkinson equal power divider [1].

1.2.2 Wilkinson Arbitrary Power Divider

Wilkinson power divider can be designed for specific power division ratio. A simplified arbitrary power divider is described in [3]. The block diagram of the arbitrary power divider is shown in Fig. 1.5.

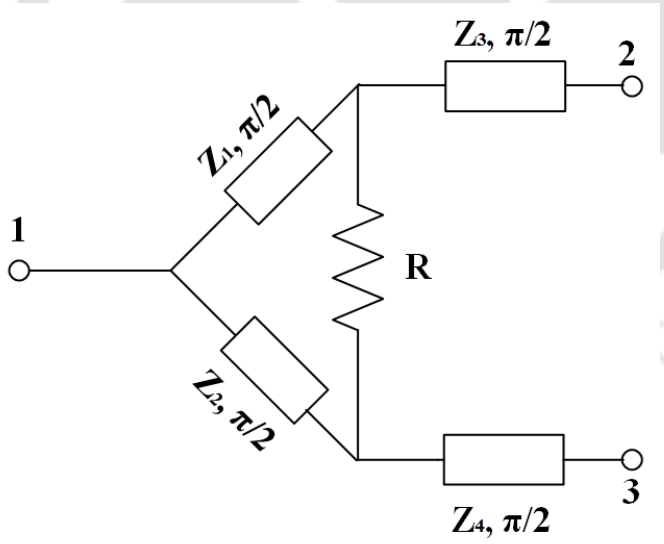


Figure 1.5: Wilkinson arbitrary power divider.

As shown in Fig. 1.5, there are four transmission lines of characteristic impedances Z_1, Z_2, Z_3, Z_4, respectively. Each transmission line is of electrical length $\pi/2$. Isolation resistor R is connected between the output arms.

If power dividing ratio $k^2 = \frac{P_3}{P_2}$, design equations for power divider are given as (detailed derivation is given in Appendix-B):

$$Z_1 = Z_0\sqrt{k(1+k^2)} \tag{1.4}$$

$$Z_2 = Z_0\sqrt{\frac{1+k^2}{k^3}} \tag{1.5}$$

$$Z_3 = Z_0\sqrt{k} \tag{1.6}$$

$$Z_4 = \frac{Z_0}{\sqrt{k}} \tag{1.7}$$

$$R = Z_0\left(k+\frac{1}{k}\right) \tag{1.8}$$

If the power dividing ratio $k^2 = 2$ and port impedance $Z_0 = 50\ \Omega$, all the design parameters are obtained using (1.4)-(1.8) as: $Z_1 = 102.98\ \Omega$, $Z_2 = 51.49\ \Omega$, $Z_3 = 59.46\ \Omega$, $Z_4 = 42.04\ \Omega$ and $R = 106.06\ \Omega$.

1.3 Gysel Power Divider

The Gysel power divider is another kind of power divider, which is used for high power application. It was proposed by U.H. Gysel in 1975 [2]. The block diagram of Gysel power divider for equal power division is shown in Fig. 1.6. As shown in Fig. 1.6, there are three pairs of transmission line of characteristic impedances Z_1, Z_2 and Z_3, respectively. Each transmission line is of electrical length $\pi/2$. There are two isolation resistors, each denoted as R connected with the ground. Incoming power from port 1 is equally divided between ports 2 & 3.

In Gysel power divider, isolation resistors are connected with the ground, so that heat can be transferred to the ground effectively. Therefore, this configuration can be used for high power application as well.

Close form solution for the design parameters are not presented in [2]. Computer-aided techniques had used in [2] to find optimum design parameters. For equal power division, optimum values of design parameters are given as:

$$Z_1 = \sqrt{2}Z_0 \tag{1.9}$$

$$Z_2 = Z_0 \tag{1.10}$$

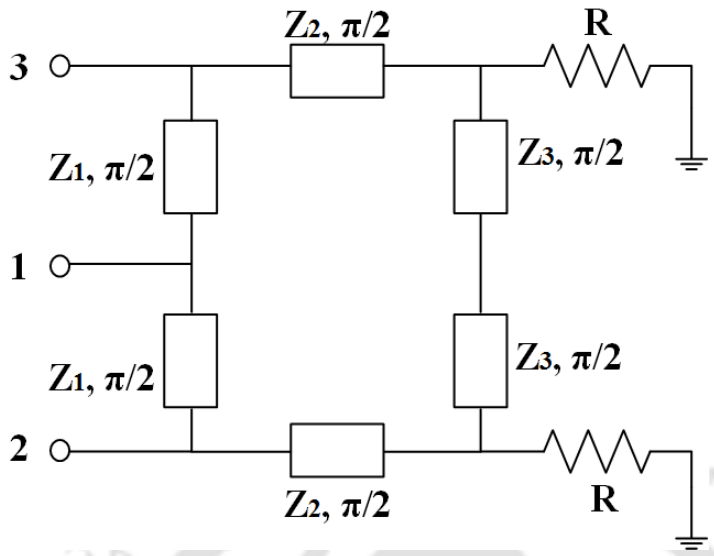


Figure 1.6: Gysel equal power divider [2].

$$Z_3 = \frac{Z_0}{\sqrt{2}} \tag{1.11}$$

$$R = Z_0 \tag{1.12}$$

If port impedance Z_0 is taken as 50 Ω, design parameters obtained using (1.9)-(1.12) are given as: $Z_1 = 70.71\ \Omega$, $Z_2 = 50\ \Omega$, $Z_3 = 35.35\ \Omega$, $R = 50\ \Omega$.

1.3.1 Difference between Wilkinson and Gysel Power Divider

Wilkinson and Gysel are two types of power divider that provides the isolation between output signals. The difference between these two types of power divider are illustrated in Table 1.1.

Table 1.1: Difference between Wilkinson and Gysel power divider.

Wilkinson Power Divider	Gysel Power Divider
It is a very compact power divider.	Size of Gysel power divider is larger than Wilkinson.
Insertion loss is very small.	Insertion loss is greater than Wilkinson.
This configuration cannot be used for high power application.	This configuration can be used for high power application because heat can be transferred to the ground effectively.

1.4 Balanced-to-Balanced Power Divider

Differential circuits are very useful because they reduce the common-mode noise and highly immune to environmental noises. Therefore, differential transceiver is getting lots of attention. To design differential transceiver, various passive and active differential circuits are required. Among various passive circuits, differential filters [26–40], differential couplers [41–44] and differential power dividers are used. Differential amplifier [45–53], differential mixer [54–62] are the examples of active circuit used in the transceiver. Differential or balanced-to-balanced power divider is used to divide or combine differential power [63–73].

Balanced-to-balanced power divider can be designed using single-ended power divider. If the single-ended power divider is followed by balun at each port, it is equivalent to a balanced-to-balanced power divider as shown in Fig. 1.7.

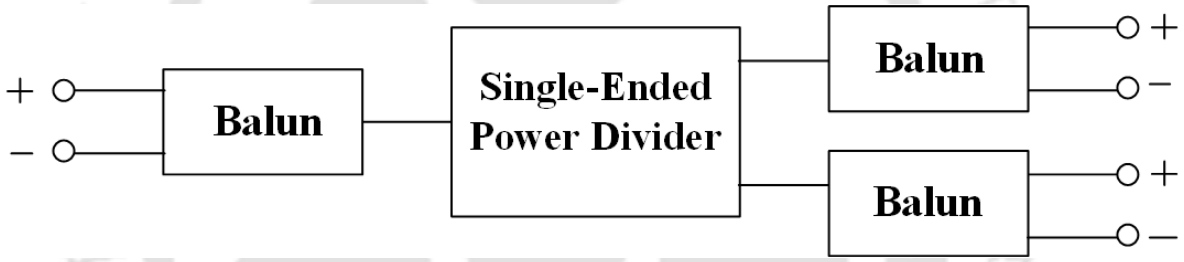


Figure 1.7: Single-ended power divider with balun at each port.

Balun is a special circuit which is used to convert single-ended port to balanced port [74–79]. A large space is required if balanced-to-balanced power divider is designed using single-ended power divider followed by baluns at each port. A Lot of emphasis is given these days to reduce the size of circuits. Single-ended power divider with baluns at each port is not a viable option. Therefore, power divider with fully balanced port is required for balanced circuit applications.

Block diagram of a balanced-to-balanced power divider is shown in Fig. 1.8. As shown in Fig. 1.8, balanced power divider is essentially a six-port device. Balanced ports A, B and C consist of ports 1 & 4, 2 & 3 and 5 & 6, respectively. Incoming power from balanced port A is divided between balanced ports B and C. It can be used as power combiner. In case of power combiner, incoming power from balanced ports B and C are combined into balanced port A.

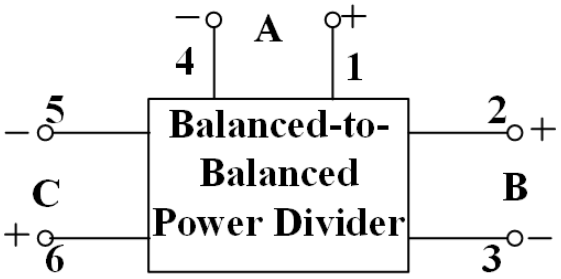


Figure 1.8: Block diagram of balanced-to-balanced power divider [63].

1.5 Balanced-to-Unbalanced Power Divider

Balanced-to-Unbalanced (BTU) power divider is used to feed single-ended (unbalanced) circuits from a balanced source. An example of application of such device is the division of power from a balanced amplifier to several single-ended antennas. This kind of power divider has the properties of balanced circuit and it can be easily connected with single-ended devices [80–89].

Block diagram of BTU power divider is shown in Fig. 1.9. As shown in Fig. 1.9, balanced port is consists of ports 2 & 4. Output unbalanced ports are ports 1 & 3. Incoming power from balanced port A is divided between unbalanced ports 1 & 3. For power combiner, power coming from unbalanced ports 1 & 3 are combined into port A.

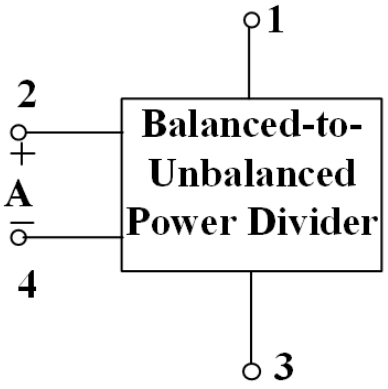


Figure 1.9: Block diagram of BTU power divider.

1.6 Unbalanced-to-Balanced Power Divider

Unbalanced-to-Balanced (UTB) power divider is used to feed balanced circuits from an unbalanced source. Feeding elements of a balanced antenna array system from an unbalanced source is an example of application of such power divider. As in the case of a BTU power divider, this type of power divider also has the properties of balanced circuit and it can be easily connected to unbalanced devices [90–93].

Block diagram of the UTB power divider is shown in Fig. 1.10. As shown in Fig. 1.10, unbalanced input port is port 1. Balanced ports are ports A and B, which consists of ports 2 & 3 and ports 4 & 5, respectively. Incoming power from unbalanced port 1 is divided between output balanced ports A and B. As a power combiner, power coming from balanced ports A and B are combined into unbalanced port 1.

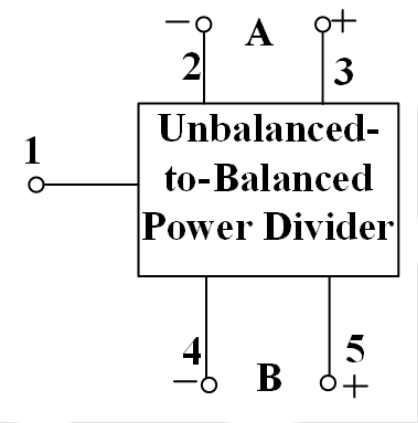


Figure 1.10: Block diagram of UTB power divider.

1.7 Microstrip Line

The circuits of all power dividers which are described in this thesis are designed using a microstrip line. Microstrip technology is used to implement planar microwave circuit. The structure of microstrip line is shown in Fig. 1.11. A microstrip line consists of a conducting strip of width W and thickness t on the top of a dielectric substrate having a relative dielectric constant ϵ_r and thickness h. The bottom of the substrate is a ground plane.

The fields in the microstrip configuration, extend in both air and dielectric, so the structure is in-homogeneous. Due to this in-homogeneous nature, the microstrip does not support a pure TEM wave. Because of the presence of the two guided-wave media (the dielectric substrate and the air),

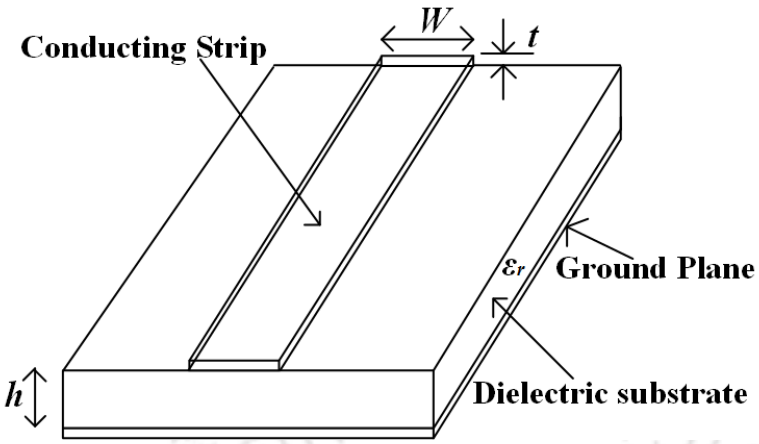


Figure 1.11: General microstrip structure [94].

the waves in a microstrip line have non vanishing longitudinal components of electric and magnetic fields. The propagation velocities depend not only on the material properties, but also on the physical dimensions of the microstrip.

For very thin conductors ($t \to 0$), closed form expressions for the design of microstrip lines are reported in [94]. These relations are summarized as:

For $W/h \leq 1$:

$$\epsilon_{re} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2}\left[\left(1 + 12\frac{h}{W}\right)^{-0.5} + 0.04\left(1 - \frac{W}{h}\right)^2\right] \tag{1.13}$$

$$Z_c = \frac{\eta}{2\pi\sqrt{\epsilon_{re}}} \ln\left(\frac{8h}{W} + 0.25\frac{W}{h}\right) \tag{1.14}$$

For $W/h \geq 1$:

$$\epsilon_{re} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2}\left(1 + 12\frac{h}{W}\right)^{-0.5} \tag{1.15}$$

$$Z_c = \frac{\eta}{\sqrt{\epsilon_{re}}}\left[\frac{W}{h} + 1.393 + 0.677\ln\left(\frac{W}{h} + 1.444\right)\right]^{-1} \tag{1.16}$$

where, ϵ_{re}, Z_c and η are effective dielectric constant, characteristic impedance of the transmission line and wave impedance in free space, respectively.

The relation between electrical length θ and physical length L are also reported in [94], which are summarized as:

$$\theta = \beta L = \frac{2\pi}{\lambda_g} L \tag{1.17}$$

$$\lambda_g = \frac{\lambda_0}{\sqrt{\epsilon_{re}}} \tag{1.18}$$

$$\lambda_0 = \frac{c}{f} \tag{1.19}$$

where, λ_g, λ_0, c and f are guided-wavelength, free space wavelength, velocity of light and operating frequency, respectively.

Based on (1.13)-(1.19), width W and length L can be obtained for a given transmission line of characteristic impedance Z_c and electrical length θ.

1.8 Motivation of the Present Work

As mentioned in the preceding section, in general, there are two types of power dividers which provide isolation between output signals, i.e. Wilkinson and Gysel power divider. As microwave circuits move towards the balanced configuration, balanced power dividers which reduces common-mode noise are getting lots of attention. Instead of the fully balanced power divider, there are several applications where BTU and UTB power dividers are required. This thesis mainly deals with BTU and UTB types of power dividers. The motivation for the same is elaborated as follows:

(i) In general, the focus of most of the power dividers is in terms of single-ended power divider. For compact and low insertion loss application, Wilkinson power dividers are used. For high power applications, Gysel power dividers are used. Various forms of these two types of power dividers are investigated over the last several decades such as: dual-band or multi-band power divider [15, 17], filtering power divider [9], multi-way power divider [13], compact power divider using coupled lines or EBG material [18]. A lot of research has been done on these single-ended types power dividers. Recently, BTU and UTB power dividers are getting lots of attention because they have the properties of balanced circuits and easily able to connect with single-ended devices.

(ii) In case of BTU power dividers, very limited investigation is reported in the literature. BTU in-phase Wilkinson power divider for equal power division has been investigated in [87] for single-band application. Therefore, there is a need to investigate other forms of power dividers such as: out-of-phase equal power divider, out-of-phase and in-phase power divider for arbitrary power division ratio. The dual-band nature of the circuits provides the additional advantage of using

the same circuit for different frequency band applications. Therefore, investigation of dual-band nature of BTU devices will give added advantage.

(iii) In case of UTB power dividers, Wilkinson type equal power dividers have been investigated in [91,92]. Power dividers reported in [91,92] cannot be used for high power application. Therefore, for high power applications, Gysel type equal power divider and power divider providing arbitrary power division ratio need to be investigated.

1.9 Thesis Contribution

This thesis presents analysis, design and measured results on different types of BTU and UTB power dividers. Following are the main contribution of this thesis.

This thesis analyzes six types of BTU power dividers, which are given as:

(i) **Gysel type out-of-phase and in-phase equal power divider:** Gysel type BTU power dividers are designed for equal power division. Two power dividers have designed, one for in-phase and one for out-of-phase applications.

(ii) **Gysel type out-of-phase and in-phase power divider with arbitrary power division:** Power dividers which can be used for arbitrary power division ratio are designed. If the power division ratio is unity, then this power divider is equivalent to the Gysel type equal power divider. Therefore, this power divider explains a general theory of Gysel type BTU power divider. Two power dividers have been designed, one for in-phase and the other for out-of-phase application.

(iii) **Wilkinson type out-of-phase equal power divider:** Another BTU power divider is designed which is of Wilkinson type. This power divider is designed for equal power division.

(iv) **Gysel type dual-band equal power divider:** A dual-band Gysel type power divider is designed, analyzed and fabricated for equal power division.

This thesis analyzes two UTB power dividers, which are given as:

(i) **Gysel type equal power divider:** An equal power divider which is of Gysel type is designed and fabricated.

(ii) **Gysel type power divider with arbitrary power division:** Gysel type power divider which can be used for arbitrary power division is designed. This provides the general theory of Gysel type UTB power divider.

This thesis also analyzes one single-ended dual-band arbitrary power divider. This single-ended power divider work is done in the initial phase of the research to understand the basic concepts related to dual-band operation of a power divider.

1.10 Organization of the Thesis

This thesis is divided into six chapters. Summary of the thesis organization is given as:

Chapter 1 describes the problem statements and the motivation behind carrying out the research work presented in this thesis. This chapter includes an introduction to power dividers and discusses different types of power dividers that are available in the literature. This chapter also includes discussions on the merits of using balanced circuits. This chapter summarizes the thesis contribution and provides a brief outline of thesis organization.

Chapter 2 presents a literature survey on balanced-to-balanced, BTU and UTB power dividers. It discusses gaps that exist for the research in the related fields.

Chapter 3 proposes various types of BTU power divider for single band applications. In this chapter, the details of Gysel type power divider for equal and arbitrary power division are presented. Design of power dividers for in-phase and out-of-phase applications have been carried out. Wilkinson type out-of-phase equal power divider is also proposed in this chapter.

Chapter 4 proposes two UTB power dividers for single band applications. Two power dividers, one for equal power division and one for arbitrary power division are presented in this chapter. The proposed power dividers are of Gysel type. The design equations for such power divider are derived. This chapter also presents simulation results as well as measurement results of the fabricated prototype.

Chapter 5 proposes two power dividers for dual-band applications. First one is a BTU equal power divider and the second one is a single-ended arbitrary power divider.

Chapter 6 concludes the thesis and presents the summary of the works done in this thesis. This chapter also discusses some directions in which the present work can be extended in future.

2

Literature Survey: Review of Related Work

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Balanced circuits are getting a lot of attention because they reduce common-mode noise and can be used for high speed applications. Single-ended microwave circuits are characterized by standard Scattering (S) parameters. To characterize balanced circuit, mixed-mode (MM) scattering parameters are required [95–101]. In this chapter, theory related to mixed-mode S parameters is presented. Mathematical transformation between mixed-mode S parameters and standard S parameters are also presented in this chapter. Literature survey related to different types of balanced-to-balanced, BTU and UTB power dividers are presented in this chapter.

2.1 Mixed-Mode Scattering Parameter

To characterize single-ended devices, standard S parameters are used. Let us consider a four-port network as shown in Fig. 2.1. The ground plane is common to all ports in Fig. 2.1. For this type of single-ended devices, voltage and current at each terminal of the device are define relative to the ground. Let the normalized incident and reflected power waves are defined as a_i and b_i, where $i = 1, 2, 3, 4$. a_i and b_i are given as:

$$a_i = \frac{1}{2\sqrt{Z_0}}[V_i + Z_0 I_i] \tag{2.1}$$

$$b_i = \frac{1}{2\sqrt{Z_0}}[V_i - Z_0 I_i] \tag{2.2}$$

where, Z_0 is the port impedance. V_i and I_i are the voltage and current of respective ports.

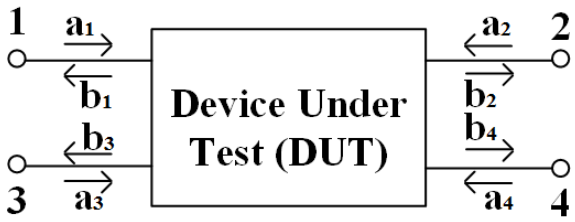

Figure 2.1: Single-ended fourt-port network.

Standard S matrix ($[S_{std}]$) for single-ended four-port network is defined as:

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix} \tag{2.3}$$

where, S_{11} to S_{44} are different S parameters of single-ended device.

For a balanced circuit, differential and common-mode signals are defined at each port. A balanced two-port network is shown in Fig. 2.2. As shown in Fig. 2.2, there are two balanced ports A & B. Normalized incident and reflected power waves at single-ended ports are defined as a_i and b_i, where $i = 1, 2, 3, 4$.

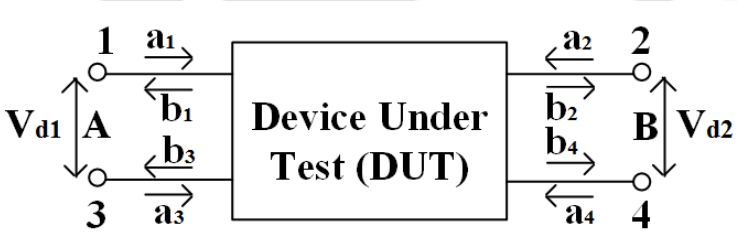

Figure 2.2: Balanced two-port network.

To define the differential signal, differential forward wave and reflected wave are defined as:

$$V_d^F = \frac{1}{2}(V_d + Z_d I_d) \tag{2.4}$$

$$V_d^R = \frac{1}{2}(V_d - Z_d I_d) \tag{2.5}$$

where, V_d is the difference in voltage and I_d is the difference in current. Z_d is the differential-mode impedance. If the node voltages are V_1 and V_3 and node currents are I_1 and I_3, V_d and I_d are defined as:

$$V_d = V_1 - V_3 \tag{2.6}$$

$$I_d = \frac{1}{2}(I_1 - I_3) \tag{2.7}$$

Similarly for common-mode signal, common-mode forward wave and reflected wave are defined as:

$$V_c^F = \frac{1}{2}(V_c + Z_c I_c) \tag{2.8}$$

$$V_c^R = \frac{1}{2}(V_c - Z_c I_c) \tag{2.9}$$

where, V_c is the common-mode voltage and I_c is the common-mode current. Z_c is the common-mode impedance. If the node voltages are V_1 and V_3 and node currents are I_1 and I_3, V_c and I_c are defined as:

$$I_c = I_1 + I_3 \tag{2.10}$$

$$V_c = \frac{1}{2}(V_1 + V_3) \tag{2.11}$$

Differential-mode and common-mode impedance are defined as:

$$Z_d = 2Z_0 \tag{2.12}$$

$$Z_c = \frac{Z_0}{2} \tag{2.13}$$

Normalized differential and common-mode incident and reflected power waves (a_d, a_c, b_d and b_c) in terms of differential and common-mode forward and reflected wave are defined as:

$$a_d = \frac{V_d^F}{\sqrt{Z_d}},\ b_d = \frac{V_d^R}{\sqrt{Z_d}},\ a_c = \frac{V_c^F}{\sqrt{Z_c}},\ b_c = \frac{V_c^R}{\sqrt{Z_c}} \tag{2.14}$$

Differential and common-mode scattering (S) matrix are defined as:

$$\begin{bmatrix} b_{dA} \\ b_{dB} \end{bmatrix} = \begin{bmatrix} S_{ddAA} & S_{ddAB} \\ S_{ddBA} & S_{ddBB} \end{bmatrix} \begin{bmatrix} a_{dA} \\ a_{dB} \end{bmatrix} \tag{2.15}$$

$$\begin{bmatrix} b_{cA} \\ b_{cB} \end{bmatrix} = \begin{bmatrix} S_{ccAA} & S_{ccAB} \\ S_{ccBA} & S_{ccBB} \end{bmatrix} \begin{bmatrix} a_{cA} \\ a_{cB} \end{bmatrix} \tag{2.16}$$

In addition to differential and common-mode S parameters as defined in (2.15) and (2.16), there are cross-modes as well. In cross-mode, input balanced port is driven by one mode, but output balanced port signal is in a different mode. The cross-mode parameters are of two forms: drive a differential

incident wave and measure a common-mode scattered wave; or drive a common-mode incident wave and measure a differential-mode scattered wave. These parameters are defined as:

$$\begin{bmatrix} b_{cA} \\ b_{cB} \end{bmatrix} = \begin{bmatrix} S_{cdAA} & S_{cdAB} \\ S_{cdBA} & S_{cdBB} \end{bmatrix} \begin{bmatrix} a_{dA} \\ a_{dB} \end{bmatrix} \tag{2.17}$$

$$\begin{bmatrix} b_{dA} \\ b_{dB} \end{bmatrix} = \begin{bmatrix} S_{dcAA} & S_{dcAB} \\ S_{dcBA} & S_{dcBB} \end{bmatrix} \begin{bmatrix} a_{cA} \\ a_{cB} \end{bmatrix} \tag{2.18}$$

So, there are 16 mixed-mode scattering parameters that define a two-port balanced network. Using (2.15)-(2.18), combined mixed-mode scattering parameters are given as [95]:

$$\begin{bmatrix} b_{dA} \\ b_{dB} \\ b_{cA} \\ b_{cB} \end{bmatrix} = \begin{bmatrix} S_{ddAA} & S_{ddAB} & S_{dcAA} & S_{dcAB} \\ S_{ddBA} & S_{ddBB} & S_{dcBA} & S_{dcBB} \\ S_{cdAA} & S_{cdAB} & S_{ccAA} & S_{ccAB} \\ S_{cdBA} & S_{cdBB} & S_{ccBA} & S_{ccBB} \end{bmatrix} \begin{bmatrix} a_{dA} \\ a_{dB} \\ a_{cA} \\ a_{cB} \end{bmatrix} \tag{2.19}$$

S_{ddAA} and S_{ddBB} are differential reflection coefficient of ports A & B, defined as:

$$S_{ddAA} = \left.\frac{b_{dA}}{a_{dA}}\right|_{a_{dB}=a_{cA}=a_{cB}=0} \tag{2.20}$$

$$S_{ddBB} = \left.\frac{b_{dB}}{a_{dB}}\right|_{a_{dA}=a_{cA}=a_{cB}=0} \tag{2.21}$$

S_{ccAA} and S_{ccBB} are common-mode reflection coefficient of ports A & B, defined as:

$$S_{ccAA} = \left.\frac{b_{cA}}{a_{cA}}\right|_{a_{dA}=a_{dB}=a_{cB}=0} \tag{2.22}$$

$$S_{ccBB} = \left.\frac{b_{cB}}{a_{cB}}\right|_{a_{dA}=a_{dB}=a_{cA}=0} \tag{2.23}$$

S_{ddAB} and S_{ddBA} are the differential transmission coefficient from port B to A and port A to B, defined as:

$$S_{ddij} = \left.\frac{b_{di}}{a_{dj}}\right|_{a_{di}=a_{ci}=a_{cj}=0} \tag{2.24}$$

where, $i, j = A$ or B

S_{ccAB} and S_{ccBA} are the common-mode transmission coefficient from port B to A and port A to

B, defined as:

$$S_{ccij} = \left.\frac{b_{ci}}{a_{cj}}\right|_{a_{di}=a_{dj}=a_{ci}=0} \tag{2.25}$$

where, $i, j = A$ or B

S_{cdAA} and S_{dcAA} are the differential to common-mode and common-mode to differential conversion parameters, defined as:

$$S_{cdAA} = \left.\frac{b_{cA}}{a_{dA}}\right|_{a_{dB}=a_{cA}=a_{cB}=0} \tag{2.26}$$

$$S_{dcAA} = \left.\frac{b_{dA}}{a_{cA}}\right|_{a_{dA}=a_{dB}=a_{cB}=0} \tag{2.27}$$

Similarly, S_{cdBB} and S_{dcBB} can be defined.

S_{dcAB} and S_{dcBA} are the common-mode to differential transmission coefficient from port B to A and port A to B, defined as:

$$S_{dcij} = \left.\frac{b_{di}}{a_{cj}}\right|_{a_{di}=a_{dj}=a_{ci}=0} \tag{2.28}$$

where, $i, j = A$ or B

S_{cdAB} and S_{cdBA} are the differential to common-mode transmission coefficient from port B to A and port A to B, defined as:

$$S_{cdij} = \left.\frac{b_{ci}}{a_{dj}}\right|_{a_{di}=a_{ci}=a_{cj}=0} \tag{2.29}$$

where, $i, j = A$ or B

2.1.1 Mathematical Transformation between Mixed-Mode and Single-ended S Parameters

Mixed-mode scattering parameters can be directly related to single-ended scattering parameters. Normalized differential-mode, common-mode, incident and reflected power wave can be represented in-terms of single-ended normalized incident and reflected power wave as [95]:

$$a_{dA} = \frac{1}{\sqrt{2}}(a_1 - a_3) \tag{2.30}$$

$$a_{cA} = \frac{1}{\sqrt{2}}(a_1 + a_3) \tag{2.31}$$

$$b_{dA} = \frac{1}{\sqrt{2}}(b_1 - b_3) \tag{2.32}$$

$$b_{cA} = \frac{1}{\sqrt{2}}(b_1 + b_3) \tag{2.33}$$

$$a_{dB} = \frac{1}{\sqrt{2}}(a_2 - a_4) \tag{2.34}$$

$$a_{cB} = \frac{1}{\sqrt{2}}(a_2 + a_4) \tag{2.35}$$

$$b_{dB} = \frac{1}{\sqrt{2}}(b_2 - b_4) \tag{2.36}$$

$$b_{cB} = \frac{1}{\sqrt{2}}(b_2 + b_4) \tag{2.37}$$

S_{ddAA} is defined in (2.20). If $a_{cA} = 0$, then using (2.31), relationship between a_1 and a_3 are obtained as:

$$a_1 = -a_3 \tag{2.38}$$

Using (2.20), (2.30), (2.32) and (2.38), S_{ddAA} can be written as:

$$S_{ddAA} = \frac{b_1 - b_3}{2a_1} \tag{2.39}$$

If $a_{dB} = a_{cB} = 0$, then using (2.34) and (2.35), a_2 and a_4 are related as:

$$a_2 = a_4 = 0 \tag{2.40}$$

Using (2.3), b_1 and b_3 can be written as:

$$b_1 = S_{11}a_1 + S_{12}a_2 + S_{13}a_3 + S_{14}a_4 \tag{2.41}$$

$$b_3 = S_{31}a_1 + S_{32}a_2 + S_{33}a_3 + S_{34}a_4 \tag{2.42}$$

Using (2.40)-(2.42), b_1 and b_3 can be obtained as:

$$b_1 = S_{11}a_1 + S_{13}a_3 \tag{2.43}$$

$$b_3 = S_{31}a_1 + S_{33}a_3 \tag{2.44}$$

Using (2.39), (2.43) and (2.44), S_{ddAA} can be written as:

$$S_{ddAA} = \frac{[S_{11}a_1 + S_{13}a_3] - [S_{31}a_1 + S_{33}a_3]}{2a_1} \tag{2.45}$$

Using (2.38) and (2.45), S_{ddAA} can be written as:

$$S_{ddAA} = \frac{1}{2}\left(S_{11} - S_{13} - S_{31} + S_{33}\right) \tag{2.46}$$

Similarly, all other mixed-mode scattering parameters can be obtained. The relationship between mixed-mode scattering parameters and single-ended scattering parameters can be summarized as [95]:

$$[S^{mm}] = [M][S_{std}][M]^{-1} \tag{2.47}$$

where, $[S^{mm}]$ is the mixed-mode scattering matrix, $[S_{std}]$ is the standard scattering matrix and $[M]$ is the conversion matrix.

$$[M] = \frac{1}{\sqrt{2}}\begin{bmatrix} 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & -1 \\ 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \end{bmatrix} \tag{2.48}$$

To convert single-ended scattering parameters into mixed-mode scattering parameters or vice versa, mathematical transformation summarized in (2.47) is used.

2.2 Balanced-to-Balanced Power Divider

Balanced-to-balanced power divider as described in section 1.4, is balanced at both input and output side. It is used in high speed communication transceiver and reduces common-mode noise as well. Fully balanced power dividers such as an equal power divider and power divider for arbitrary power division are reported in [63, 64]. To completely analyze a balanced-to-balanced power divider, power divider is required to be characterized in-terms of its mixed-mode scattering parameters. The block diagram of a balanced-to-balanced power divider is shown in Fig. 1.8, requirements of mixed-mode parameters for this power divider are summarized below:

(i) Ideally, when a differential-mode signal is fed to the balanced port A, no differential-mode power should be reflected, no power should get converted as common-mode outputs at the balanced ports B and C, power should not be converted as common-mode reflection at the balanced port A and differential-mode power at the balanced ports B and C should be divided according to the specified power division ratio. In terms of mixed-mode S parameters, these conditions can

be written as:

$$|S_{ddAA}| = 0 \quad (2.49)$$

$$|S_{dcAB}| = |S_{dcAC}| = |S_{cdAB}| = |S_{cdAC}| = 0 \quad (2.50)$$

$$|S_{cdAA}| = |S_{dcAA}| = 0 \quad (2.51)$$

$$|S_{ddAB}| = \alpha \quad (2.52)$$

$$|S_{ddAC}| = \sqrt{1-\alpha^2} \quad (2.53)$$

where, α is the transmission coefficient from port A to port B. For equal power division, $\alpha = \frac{1}{\sqrt{2}}$.

(ii) All the common-mode signal should be reflected from each balanced port.

$$|S_{ccAA}| = |S_{ccBB}| = |S_{ccCC}| = 1 \quad (2.54)$$

(iii) When the differential-mode signal is fed into the balanced port B (C), no differential-mode power should be reflected, no power should be converted into differential-mode and common-mode reflection, no power should be transmitted to the balanced port C (B) in the form of differential-mode or common-mode.

$$|S_{ddBB}| = |S_{ddCC}| = 0 \quad (2.55)$$

$$|S_{dcBB}| = |S_{dcBB}| = |S_{cdBB}| = |S_{cdBB}| = 0 \quad (2.56)$$

$$|S_{dcCC}| = |S_{dcCC}| = |S_{cdCC}| = |S_{cdCC}| = 0 \quad (2.57)$$

$$|S_{dcBC}| = |S_{dcBC}| = |S_{cdBC}| = |S_{cdBC}| = 0 \quad (2.58)$$

$$|S_{dcCB}| = |S_{dcCB}| = |S_{cdCB}| = |S_{cdCB}| = 0 \quad (2.59)$$

$$|S_{ddBC}| = 0 \quad (2.60)$$

Based on the above requirements, several balanced-to-balanced power dividers are reported in the literature [63–66]. Theoretical results of different mixed-mode scattering parameters for single-band balanced power divider are shown in Figs 2.3-2.5. In Figs. 2.3-2.4, mixed-mode results of balanced ports A, B, C and isolation between two output ports are shown. In Fig. 2.5(a), theoretical results of balanced power division from input balanced port A to output balanced ports (B & C), are shown.

The power division ratio between two output signals are $1 : 3^2$ [64]. Fig. 2.5(b) shows the phase difference between two output signals. Some of the reported balanced power dividers are discussed in this section.

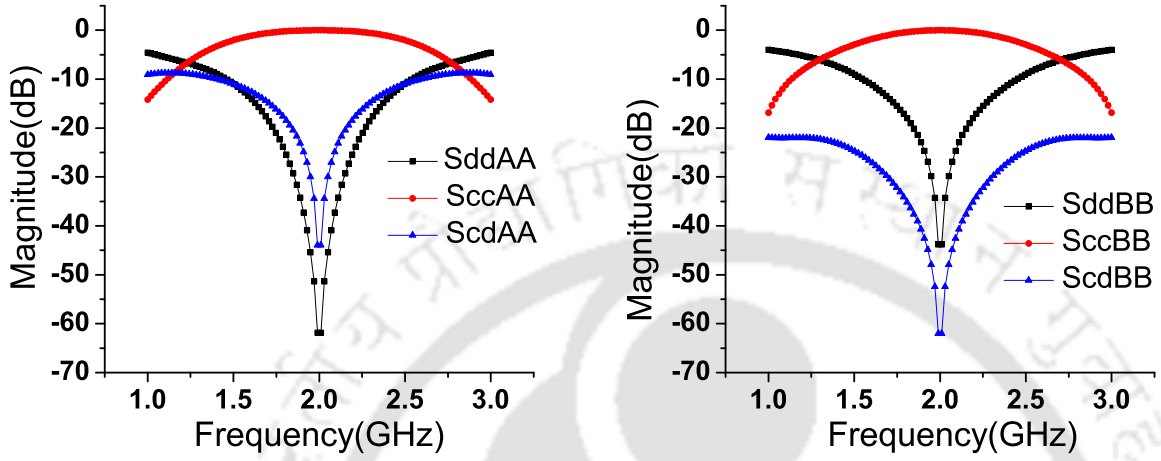

Figure 2.3: (a) Theoretical results of $|S_{ddAA}|$, $|S_{ccAA}|$ and $|S_{cdAA}|$. (b) Theoretical results of $|S_{ddBB}|$, $|S_{ccBB}|$ and $|S_{cdBB}|$.

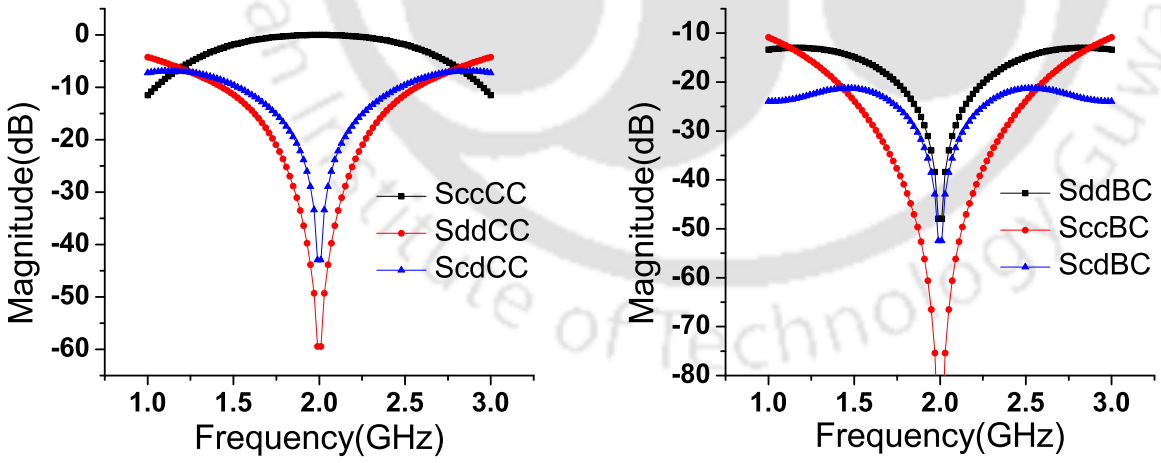

Figure 2.4: (a) Theoretical results of $|S_{ddCC}|$, $|S_{ccCC}|$ and $|S_{cdCC}|$. (b) Theoretical results of $|S_{ddBC}|$, $|S_{ccBC}|$ and $|S_{cdBC}|$.

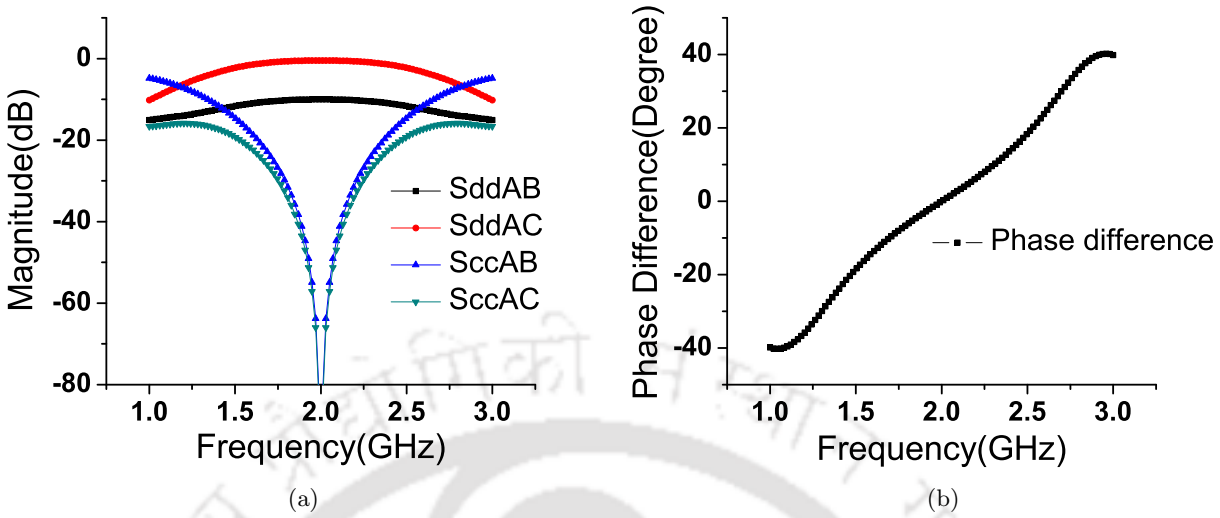

Figure 2.5: (a) Theoretical results of $|S_{ddAB}|$, $|S_{ddAC}|$, $|S_{ccAB}|$ and $|S_{ccAC}|$. (b) Theoretical result of phase difference.

2.2.1 Balanced-to-Balanced Equal power divider

Balanced-to-balanced equal power divider is reported in [63]. The reported power divider structure is shown in Fig. 2.6. As shown in Fig. 2.6, combination of ports 1 & 4 is the input balanced port and combination of ports 2 & 3 , 5 & 6 are the output balanced ports of the power divider. There are two pairs of transmission lines of characteristic impedances Z_{12} and Z_{23} of electrical lengths θ_{12} and θ_{23}, respectively. Other three transmission lines are of characteristic impedances Z_{14}, Z_{25} and Z_{36} of electrical lengths θ_{14}, θ_{25} and θ_{36}, respectively. There are two pairs of isolation resistors R_2 and R_3, which provides isolation between two output balanced ports.

This reported power divider is of Wilkinson type because isolation resistors are connected between output arms of the power divider. Even- and odd-mode analysis have been used to derive design equations for this power divider. At the center frequency, $\theta_{12} = \pi/2$ and $\theta_{14} = \theta_{25} = \theta_{36} = \theta_{23} = \pi$. The design equations for this power divider are summarized as:

$$Z_{12} = \frac{\sqrt{2}Z_0}{2} \tag{2.61}$$

$$\frac{1}{R_2} + \frac{1}{R_3} = \frac{2}{Z_0} \tag{2.62}$$

Transmission lines of characteristic impedances Z_{14}, Z_{25}, Z_{36} and Z_{23} are of half wavelength long,

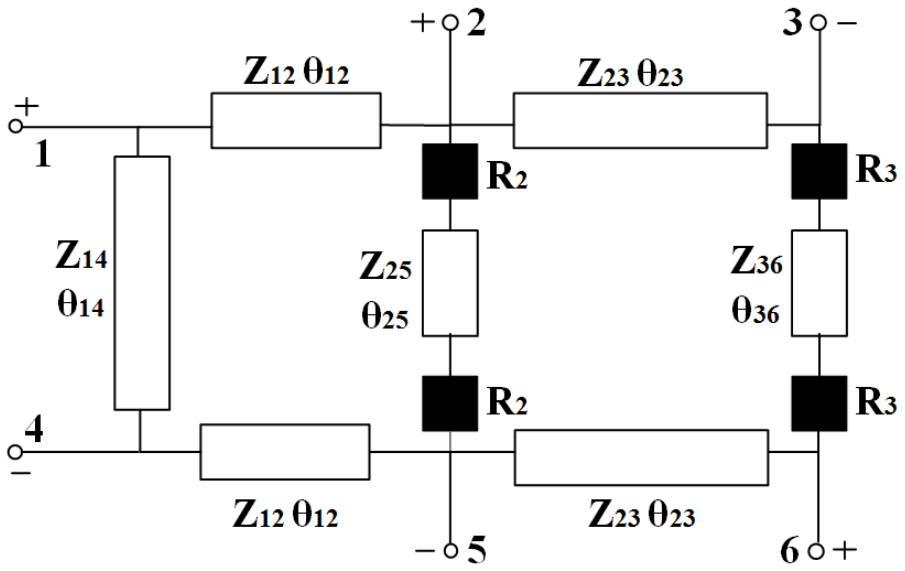

Figure 2.6: Balanced-to-balanced equal power divider [63].

therefore, characteristic impedances Z_{23}, Z_{14}, Z_{25} and Z_{36} can be chosen independently.

This reported equal power divider is designed and fabricated at 2 GHz. This reported balanced power divider shows in-phase characteristic. If polarity of one balanced output port is changed, then it work as out-of-phase power divider. The reported values for maximum differential-mode transmission coefficient is -3.2 dB and differential-mode isolation is 47.2 dB. The fractional bandwidth of this reported power divider is 20.8%.

The balanced-to-balanced power divider reported in [63] can be designed using two isolation resistors [102, 103]. As shown in Fig. 2.6, at the center frequency Z_{25} and Z_{36} are of electrical length π or $\lambda_g/2$ and impedance of a transmission line repeats after $\lambda_g/2$. Therefore, instead of using four isolation resistors power divider can be designed using two isolation resistors, as shown in Fig. 2.7. As shown in Fig. 2.7, there are two ways to realize power divider with following relation.

$$R_b = R_c = 2R_a \tag{2.63}$$

2.2.2 Balanced-to-Balanced Power Divider With Arbitrary Power Division

Balanced-to-balanced power divider for arbitrary power division is reported in [64]. The structure of the arbitrary power divider is shown in Fig. 2.8. Input balanced port is A and two output balanced

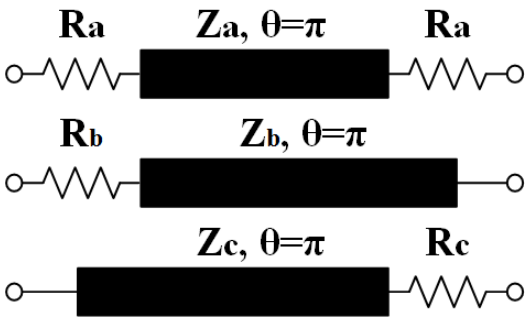

Figure 2.7: Simplified balanced-to-banalced power divider [102].

ports are B and C. As shown in Fig. 2.8, there are three transmission lines of characteristic impedance Z_x and electrical length of π. There are six transmission lines of electrical length $\pi/2$ and characteristic impedances Z_{T1}, Z_{T2}, Z_{T3}, Z_{T4}, Z_{T5} and Z_{T6}, respectively. Two isolation resistors R_1 and R_2 provide the isolation between two balanced output ports.

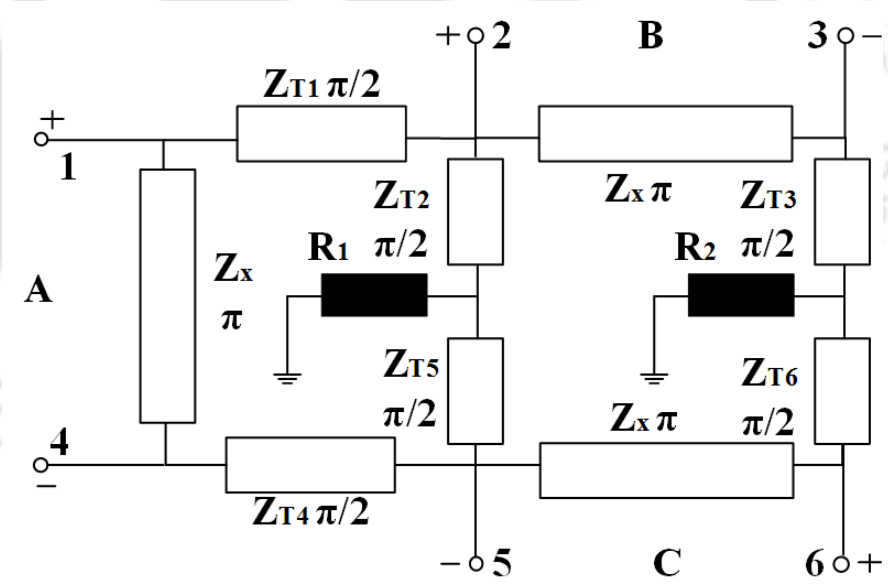

Figure 2.8: Balanced-to-balanced power divider with arbitrary power division [64].

This reported power divider is of Gysel type because isolation resistors are connected to ground. This reported power divider is analyzed by converting it into two port network while all other ports are matched terminated and using the properties of transmission and scattering matrices. The design equations are derived in [64]. The maximum achievable power division ratio is $1 : 4.69^2$ when the characteristic impedances are limited within the realizable range of 20 to 120 Ω. The reported power divider has been designed for power division ratio $1 : 3^2$. This reported power divider is fabricated at

2 GHz. The reported fractional bandwidth is 15.5%, while theoretical fractional bandwidth is 23%.

2.2.3 Dual-band Balanced-to-Balanced Equal Power Divider

A dual-band balanced-to-balanced equal power divider is reported in [66]. The structure of this dual-band power divider is shown in Fig. 2.9. This structure is similar to the single-band power divider reported in [63] and shown in Fig. 2.6. The only difference is that all 90° and 180° transmission lines are replaced by dual-band phase shifters.

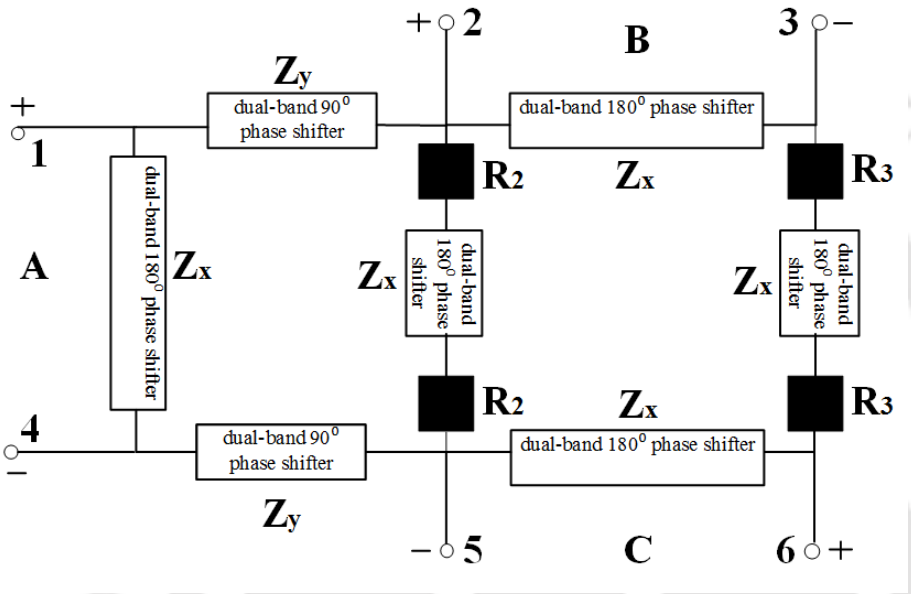

Figure 2.9: Dual-band balanced-to-balanced equal power divider [66].

Dual-band phase shifter for 90° transmission line is designed using a T shaped model shown in Fig. 2.10. This T shape model consists of two transmission lines of characteristic impedance Z_a and electrical length θ_a, one open circuited stub of characteristic impedance Z_b and electrical length θ_b. Design equations for this model are reported in [66]. For transmission lines of electrical length 180°, two T shape models are connected in cascade.

The reported dual-band power divider is of Wilkinson type because isolation resistors are not connected with the ground. The reported dual-band power divider is designed and fabricated at 2.45 GHz and 5.2 GHz. The first pass band is from 2.395 GHz to 2.550 GHz and the second pass band is from 5.245 GHz to 5.30 GHz. The maximum isolation for the first pass band and the second pass band are 17.8 dB and 17.6 dB, respectively.

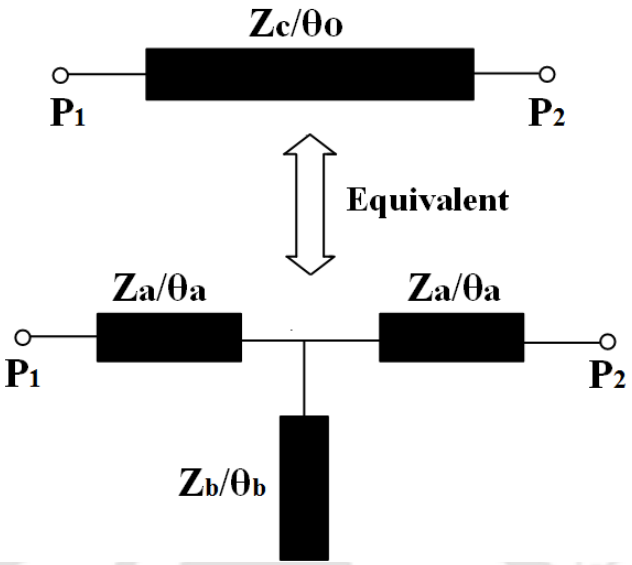

Figure 2.10: Dual-band 90° phase shifter with T model [66].

2.3 Balanced-to-Unbalanced Power Divider

BTU power divider as described in section 1.5, is balanced on the input side and unbalanced at the output sides. This type of power divider is used to feed signal from a balanced source to single-ended antennas.

There are several BTU power dividers for equal power division are reported in the literature [80–89], some of them are discussed in this section.

2.3.1 BTU In-phase Equal Power Divider

BTU equal power divider for in-phase application is reported in [87]. The structure of this power divider is shown in Fig. 2.11. In this structure, input balanced port is consists of ports 1+ & 1− and ports 2 & 3 are the two unbalanced output ports. Power going into input balanced port is equally divided into two unbalanced ports. There are two transmission lines of characteristic impedance Z_1 and electrical length of 90° and −90°, respectively. One isolation resistor is connected between two unbalanced output ports.

This reported power divider is of Wilkinson type because the isolation resistor is connected between two output arms. Even- and odd-mode analysis are used to derive design equations which are reported in [87]. To realize a transmission line of electrical length −90°, two short circuited parallel coupled

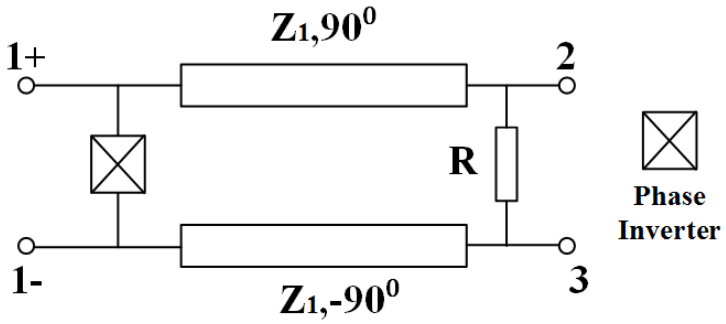

Figure 2.11: BTU equal power divider [87].

transmission lines are used. To reduce the size of the power divider, phase inverter is realized using two cascaded T shaped structure. This reported power divider is designed and fabricated at 2 GHz. The reported operating bandwidth of this power divider is 25%.

2.3.2 Coupled-Line Based BTU Equal Power divider

A compact coupled-line based BTU equal power divider is reported in [82]. The circuit diagram of this reported power divider is shown in Fig. 2.12. The input balanced port consists of ports 1 & 2 and ports 3 & 4 are the unbalanced output ports. The circuit structure which consists of three pairs of cascaded coupled lines and one resistor, is shown in Fig. 2.12. The even and odd-mode characteristic impedances of coupled lines are Z_{ei} and Z_{oi}, respectively (where, $i = 1, 2, 3$). The electrical lengths of coupled lines are θ_1, θ_2 and θ_3, respectively. The isolation resistor R_0 is connected to ground.

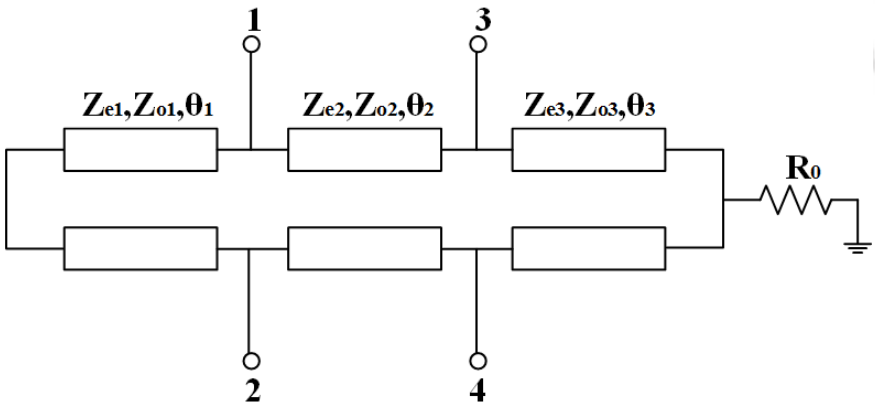

Figure 2.12: Coupled-line based BTU equal power divider [82].

This reported power divider is of Gysel type because the isolation resistor is connected to ground.

This reported power divider has features such as: a) 37.2% bandwidth; b) good matching at ports with high isolation and common-mode suppression.

Closed-form design equations have been provided using the even and odd-mode analysis. The circuit structure is compact because of the use of coupled lines. However, phase information is not reported in this paper.

2.3.3 BTU Filtering Equal Power Divider

In a communication system, power divider is generally followed by the filter. Therefore, to reduce the size of the circuit, power divider with filtering characteristic is a viable option in-place of power divider followed by the filter.

BTU power divider with filtering characteristic is reported in [81]. In this article, three structures are reported. The first structure is shown in Fig. 2.13. Input balanced port consists of ports 1 & 3 and output unbalanced ports are ports 2 & 4. In this structure, there are two pairs of transmission lines of characteristic impedances Z_1 and Z_2, a pair of coupled line of even and odd-mode impedances Z_e and Z_0, respectively. The electrical length of all lines is same as θ. Isolation resistor R is connected to ground.

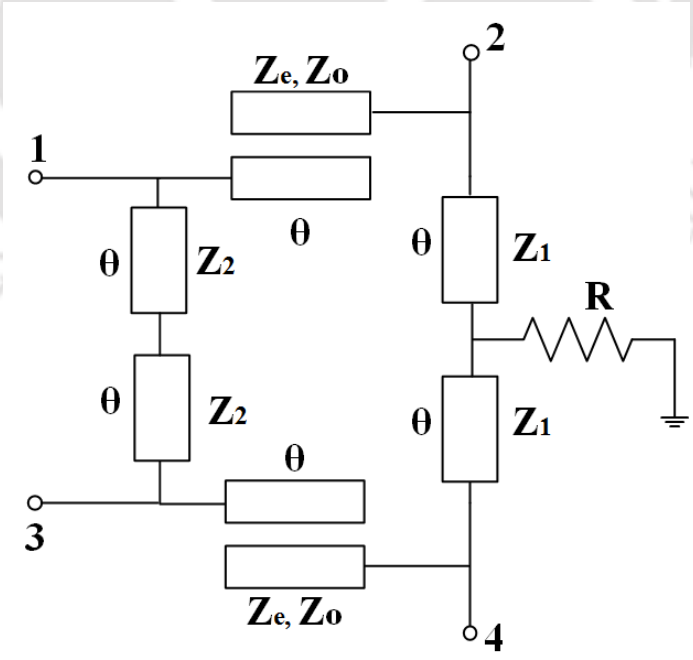

Figure 2.13: BTU filtering equal power divider (structure I) [81].

Even- and odd-mode analysis are used to derive design equations. This reported power divider

shows a wideband response. The selectivity of differential-mode passband is not so ideal due to the lack of transmission zeros near the passband.

To overcome the selectivity problem, second structure of power divider is used which is shown in Fig. 2.14. Compared with the structure I of Fig. 2.13, the transmission lines connected between input balanced port are replaced by the half-wavelength coupled lines and other parts are same as the structure shown in Fig. 2.13.

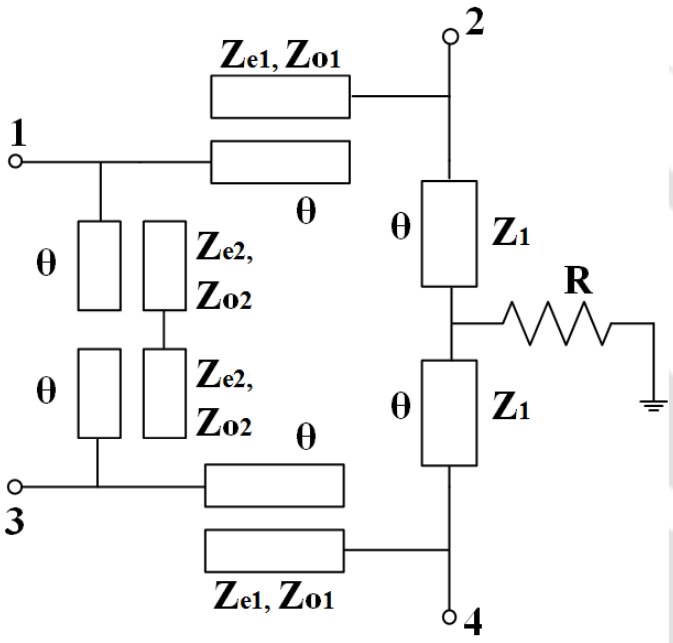

Figure 2.14: BTU filtering equal power divider (structure II) [81].

Even- and odd-mode analysis are used to derive design equations. This structure produced two transmission zeros near the passband of power divider. The two transmission zeros are independently adjustable by the open/shorted coupled lines, therefore improves the selectivity.

Due to fabrication precision, a parallel coupled line cannot be realized for large coupling coefficient. To overcome this disadvantage, another high selectivity wideband BTU filtering power divider with two transmission zeros using half-wavelength open stubs are reported using structure III as shown in Fig. 2.15.

Compared with the structure in Fig. 2.13, two half-wavelength open stubs are shunt connected to ports 2 and 4, respectively. Again, even- and odd-mode analysis are used to derive design equations. These two half-wavelength open stubs produced two transmission zeros near the center frequency.

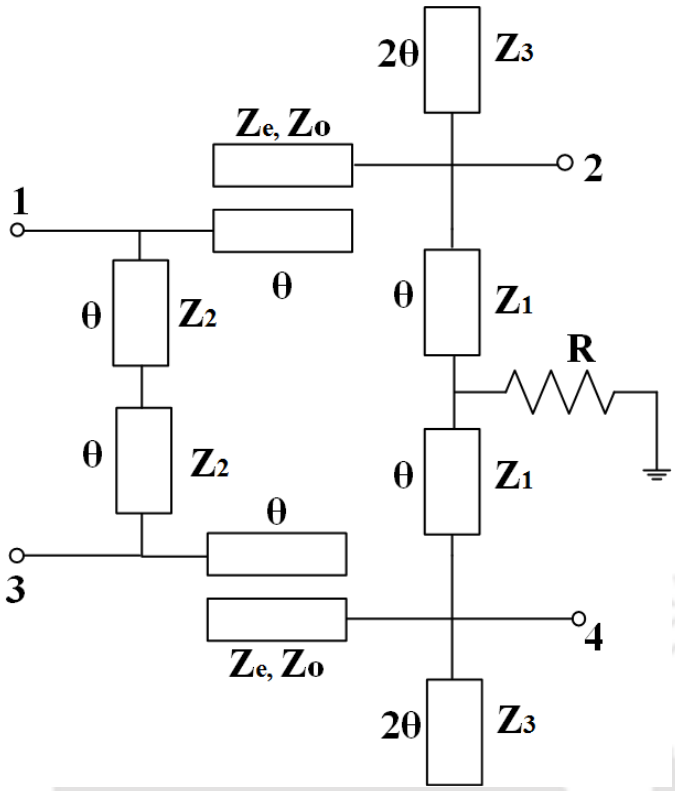

Figure 2.15: BTU filtering equal power divider (structure III) [81].

2.3.4 Dual-band BTU Equal Power Divider

Dual-band BTU equal power divider is reported in [85]. The circuit diagram of this equal power divider is shown in Fig. 2.16. The input balanced port consists of ports 1 & 2, while the output balanced ports are ports 3 & 4. It consists of two pairs of cascaded coupled lines, two identical dual-band 90° phase shifters and one grounded resistor R_0. The even (odd)-mode characteristic impedance of the coupled line is $Z_{ei}(Z_{oi})$, where $i = 1$ and 2. In addition, the electrical lengths of two coupled-lines are same and equal to θ, which guarantee the dual-band performance.

This reported structure is symmetrical, therefore even- and odd-mode analysis are used to derive design equations. This reported power divider is designed for a frequency ratio of 2 ($\frac{f_2}{f_1} = 2$). The two design frequencies are 0.9 GHz and 1.8 GHz.

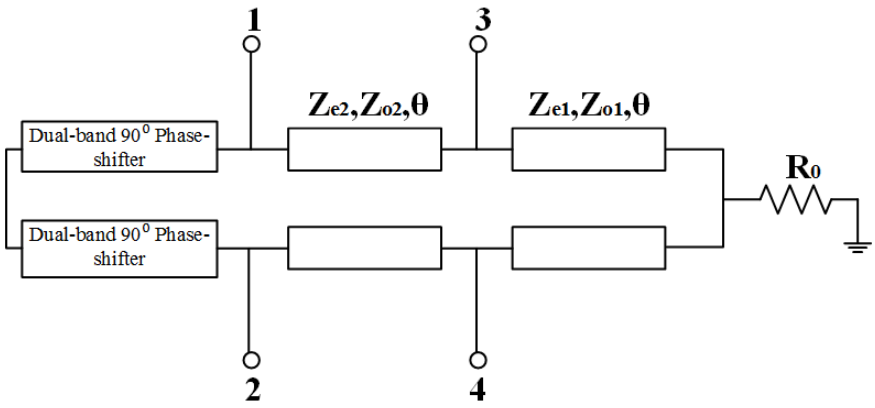

Figure 2.16: Dual-band BTU equal power divider [85].

2.4 Unbalanced-to-Balanced Power Divider

UTB power divider as described in section 1.6, is unbalanced at the input side and balanced on the output sides. This type of power divider is used to feed signal from unbalanced source to balanced circuits and balanced antennas.

Few UTB power dividers for equal power division are reported in [91–93].

2.4.1 UTB Equal Power Divider

In [91] and [92], Wilkinson type UTB equal power dividers are reported. These two power dividers have a similar structure, but the performance of [92] is better than [91]. These two power dividers which are reported in [91,92] are Wilkinson type, so these power divider configurations cannot be used for high power applications.

The structure of the reported power divider in [91, 92] is shown in Fig. 2.17. Port 1 is the unbalanced input port, port 2 (combination of ports 2+ and 2−) and port 3 (combination of ports 3+ and 3−) are the two balanced output ports of the power divider. There are two pairs of transmission line of characteristic impedances Z_1 and Z_2 and electrical lengths of θ_1 and θ_2, respectively. Isolation resistors R_1 and R_2 provide the isolation between two output signals.

In [91], the reported power divider is designed and fabricated at 10 GHz while in [92], power divider is designed at 1.8 GHz.

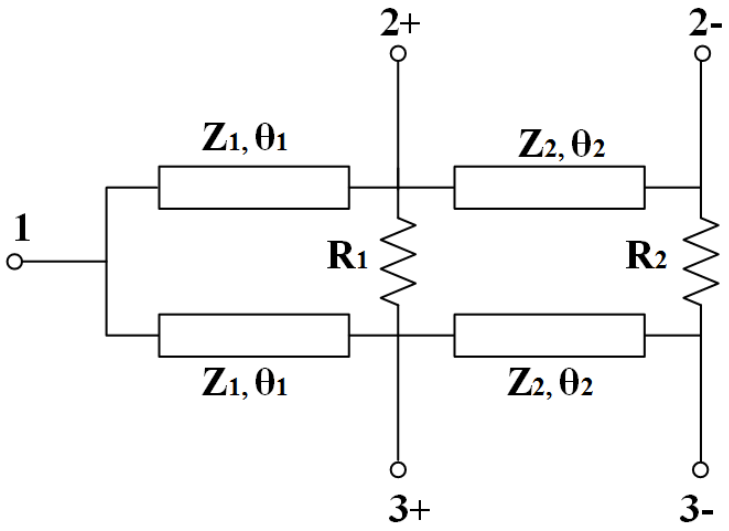

Figure 2.17: UTB equal power divider [91].

Table 2.1: Comparison of various types of reported power dividers.

Ref.	Power Divider	Type	Power Division	Phase	Band
[63]	Balanced-to-Balanced	Wilkinson	Equal	In-phase	Single-band
[64]	Balanced-to-Balanced	Gysel	Arbitrary	In-phase	Single-band
[66]	Balanced-to-Balanced	Wilkinson	Equal	In-phase	Dual-band
[87]	BTU	Wilkinson	Equal	In-phase	Single-band
[82]	BTU	Gysel	Equal	Out-of-phase	Single-band
[81]	BTU	Gysel	Equal	Out-of-phase	Single-band
[85]	BTU	Gysel	Equal	Out-of-phase	Dual-band
[91, 92]	UTB	Wilkinson	Equal	In-phase	Single-band

2.5 Summary

This chapter provides the basic concepts of mixed-mode scattering parameters which are required for the characterization of the balanced microwave network. Further, standard mathematical transformation is derived which is used to transform between single-ended and balanced scattering parameters. This chapter provides a brief literature review related to balanced-to-balanced, balanced-to-unbalanced and unbalanced-to-balanced power dividers. Various types of reported power dividers are summarized in Table 2.1. Further, in following chapters, mixed-mode scattering parameters are used to design and analyze several BTU and UTB power dividers.

3

Balanced-to-Unbalanced Power Divider

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3.6 Conclusion 84

In this chapter, different types of BTU power dividers are presented. The analysis of these BTU power dividers is based on mixed-mode scattering parameters which are presented in chapter 2. All these BTU power dividers are for single band applications. First, two BTU equal power dividers for out-of-phase application are presented. Among two equal power dividers, one is of Gysel type and another is of Wilkinson type. One in-phase Gysel type equal power divider is also presented. In this chapter, two BTU power dividers for arbitrary power division are also presented. Both these arbitrary power dividers are of Gysel type. Among two arbitrary power dividers, one is for out-of-phase application and the other is for in-phase application. All power dividers presented in this chapter provide good amount of isolation between two unbalanced output ports.

3.1 Gysel Type Out-of-Phase Equal Power Divider

3.1.1 Structure

The structure of the proposed Gysel type out-of-phase equal power divider is shown in Fig. 3.1. Ports 1 & 3 are the two unbalanced output ports. Combination of ports 2 & 4 (combined as A) represent the input balanced port. There are two pairs of transmission lines of characteristic impedances Z_X and Z_Y and electrical length of each line is $\pi/2$. There is one transmission line of characteristic impedance Z_A and electrical length π. In Fig. 3.1; R is the isolation resistor, one end of which is connected to ground.

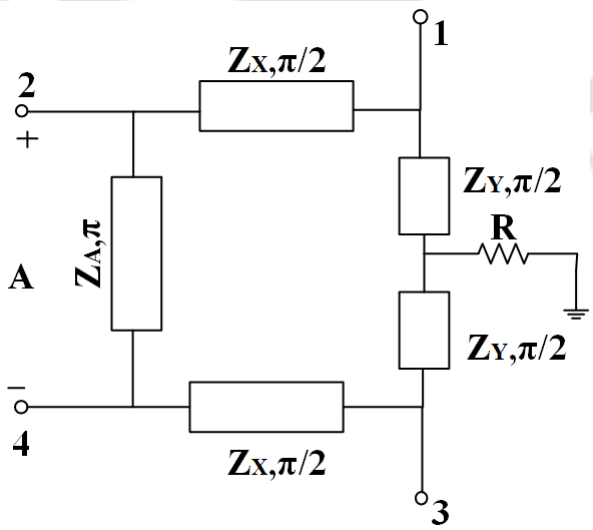


Figure 3.1: BTU out-of-phase Gysel equal power divider.

3.1.2 Standard S Matrix Realization

The proposed power divider is a four port network. A standard scattering matrix of a four port symmetrical and reciprocal network is given as:

$$[S_{std}] = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{12} & S_{22} & S_{23} & S_{24} \\ S_{13} & S_{23} & S_{33} & S_{34} \\ S_{14} & S_{24} & S_{34} & S_{44} \end{bmatrix} \tag{3.1}$$

A balanced circuit is characterized by its mixed-mode S matrix as mentioned in chapter 2. To obtain S-parameters of (3.1), mixed-mode scattering parameters need to be found out based on the requirements of the equal power divider. The mixed-mode scattering matrix is given as:

$$[S^{mm}] = \begin{bmatrix} S_{ddAA} & S_{cdAA} & S_{dsA1} & S_{dsA3} \\ S_{dcAA} & S_{ccAA} & S_{csA1} & S_{csA3} \\ S_{sd1A} & S_{sd3A} & S_{ss11} & S_{ss13} \\ S_{sc1A} & S_{sc3A} & S_{ss31} & S_{ss33} \end{bmatrix} \tag{3.2}$$

where, S_{sd1A} and S_{sd3A} represent differential-mode to single-ended (to ports 1 and 3) transmission coefficients. S_{sc1A} and S_{sc3A} denote CMS (common-mode suppression) to single-ended (to ports 1 and 3). S_{ddAA}, S_{ccAA} and S_{dcAA} denote differential-mode reflection coefficient, common-mode reflection coefficient and differential to common-mode conversion coefficient, respectively. S_{ss11}, S_{ss33}, S_{ss13} are the reflection coefficients of unbalanced ports and isolation between the output ports, respectively.

Based on the requirements of the equal power divider, constraints for the mixed-mode parameters are given as:

(i) Single-ended S parameters such as reflection coefficient and coupling should be zero.

$$|S_{ss11}| = |S_{ss33}| = |S_{ss13}| = 0 \tag{3.3}$$

(ii) Differential-mode reflection coefficient and differential-mode to common-mode conversion coefficient should be zero.

$$|S_{ddAA}| = |S_{cdAA}| = |S_{dcAA}| = 0 \tag{3.4}$$

(iii) Common-mode reflection should be unity.

$$|S_{ccAA}| = 1 \tag{3.5}$$

(iv) CMS should be zero.

$$|S_{csA1}| = |S_{csA3}| = |S_{sc1A}| = |S_{sc3A}| = 0 \tag{3.6}$$

(v) Power should be divided equally from input balanced port into output unbalanced ports.

$$|S_{dsA1}| = |S_{dsA3}| = |S_{sd1A}| = |S_{sd3A}| = 1/\sqrt{2} \tag{3.7}$$

Based on (3.3)-(3.7), mixed-mode S matrix is derived and given in (3.8).

$$[S^{mm}] = \begin{bmatrix} 0 & 0 & \frac{1}{\sqrt{2}}e^{j\phi_1} & \frac{1}{\sqrt{2}}e^{j\phi_2} \\ 0 & e^{j\phi_3} & 0 & 0 \\ \frac{1}{\sqrt{2}}e^{j\phi_1} & \frac{1}{\sqrt{2}}e^{j\phi_2} & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \tag{3.8}$$

where, ϕ_1, ϕ_2, ϕ_3 represent the phase of different mixed-mode S parameters.

Now, to convert the mixed-mode S parameters into standard S parameters, following equations are used [87]:

$$|S_{ddAA}| = \frac{1}{2}|S_{22} - S_{24} - S_{42} + S_{44}| \tag{3.9}$$

$$|S_{ccAA}| = \frac{1}{2}|S_{22} + S_{24} + S_{42} + S_{44}| \tag{3.10}$$

$$|S_{dcAA}| = \frac{1}{2}|S_{22} - S_{24} + S_{42} - S_{44}| \tag{3.11}$$

$$|S_{cdAA}| = \frac{1}{2}|S_{22} + S_{24} - S_{42} - S_{44}| \tag{3.12}$$

$$|S_{sd1A}| = \frac{1}{\sqrt{2}}|S_{12} - S_{14}| \tag{3.13}$$

$$|S_{sd3A}| = \frac{1}{\sqrt{2}}|S_{32} - S_{34}| \tag{3.14}$$

$$|S_{sc1A}| = \frac{1}{\sqrt{2}}|S_{12} + S_{14}| \tag{3.15}$$

$$|S_{sc3A}| = \frac{1}{\sqrt{2}}|S_{32} + S_{34}| \tag{3.16}$$

For out-of-phase characteristic, $\phi_1 = -\pi/2$, $\phi_2 = \pi/2$, $\phi_3 = -\pi$. Using (3.1), (3.8) and (3.9)-(3.16), standard S matrix is derived and given in (3.17).

$$[S_{std}] = \begin{bmatrix} 0 & -j\frac{1}{2} & 0 & j\frac{1}{2} \\ -j\frac{1}{2} & -\frac{1}{2} & j\frac{1}{2} & -\frac{1}{2} \\ 0 & j\frac{1}{2} & 0 & -j\frac{1}{2} \\ j\frac{1}{2} & -\frac{1}{2} & -j\frac{1}{2} & -\frac{1}{2} \end{bmatrix} \tag{3.17}$$

3.1.3 Even-Mode Analysis

The equivalent circuit of the proposed power divider for even-mode excitation is shown in Fig. 3.2. Using impedance transformation property of a quarter wave transformer in Fig. 3.2, Z_Y can be obtained as:

$$Z_Y = \sqrt{2RZ_0} \tag{3.18}$$

where, Z_0 is the port impedance.

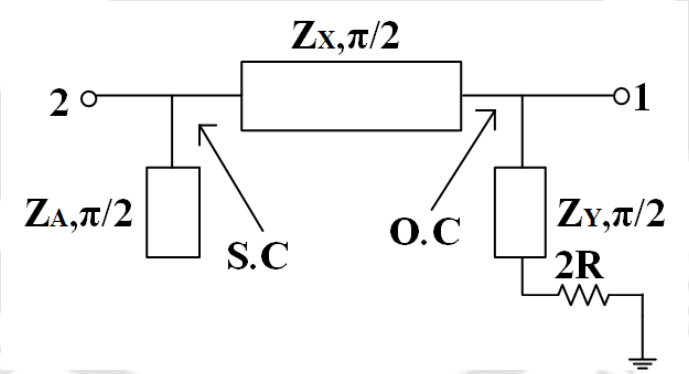


Figure 3.2: Equivalent circuit for carrying out even-mode analysis.

3.1.4 Odd-Mode Analysis

The equivalent circuit corresponding to odd-mode excitation of the proposed power divider is shown in Fig. 3.3. From Fig. 3.3, it can be seen that Z_X can be chosen as the port impedance Z_0.

$$Z_X = Z_0 \tag{3.19}$$

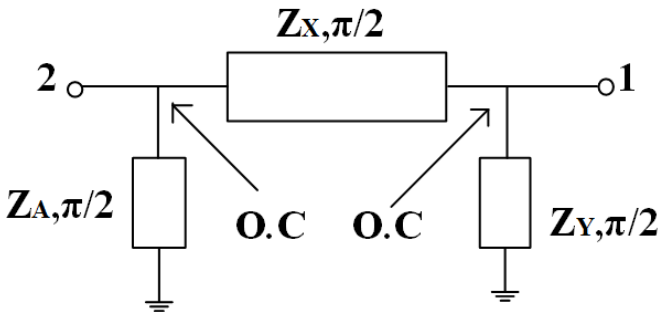
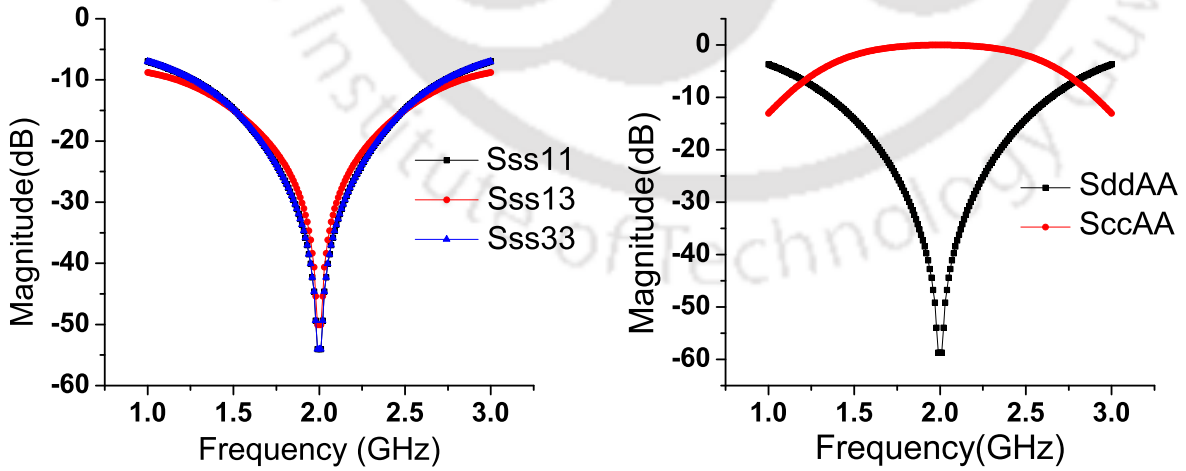


Figure 3.3: Equivalent circuit for carrying out odd-mode analysis.

3.1.5 Theoretical Results

The proposed Gysel type out-of-phase equal power divider is designed at 2 GHz. Both Z_A and R are chosen as 50 Ω. From the design equations (3.18) and (3.19), Z_X and Z_Y are obtained as 50 Ω and 70.71 Ω, respectively.

Figs. 3.4-3.5 show theoretical results of the Gysel type out-of-phase equal power divider. Fig. 3.4(a) shows the return losses of unbalanced ports and isolation between output ports. At the center frequency, $|S_{ss11}|$, $|S_{ss13}|$ and $|S_{ss33}|$ are -54 dB, -50 dB and -54 dB, respectively. Fig. 3.4(b) shows the differential return loss and common-mode reflection of the balanced port A. At the center frequency, $|S_{ddAA}|$ and $|S_{ccAA}|$ are -58 dB and 0 dB, respectively.



(a) (b)

Figure 3.4: (a) Theoretical results of $|S_{ss11}|$, $|S_{ss13}|$ and $|S_{ss33}|$. (b) Theoretical results of $|S_{ddAA}|$ and $|S_{ccAA}|$.

Fig. 3.5(a) shows the differential-mode transmission coefficient and common-mode suppression from balanced port to unbalanced ports. At the center frequency, $|S_{sd1A}|$, $|S_{sd3A}|$, $|S_{sc1A}|$ and $|S_{sc3A}|$ are -3 dB, -3 dB, -45 dB and -45 dB, respectively. Fig. 3.5(b) shows the phase difference ($Ang(S_{sd1A}/S_{sd3A})$) between two output signals. This shows out-of-phase characteristic of the power divider.

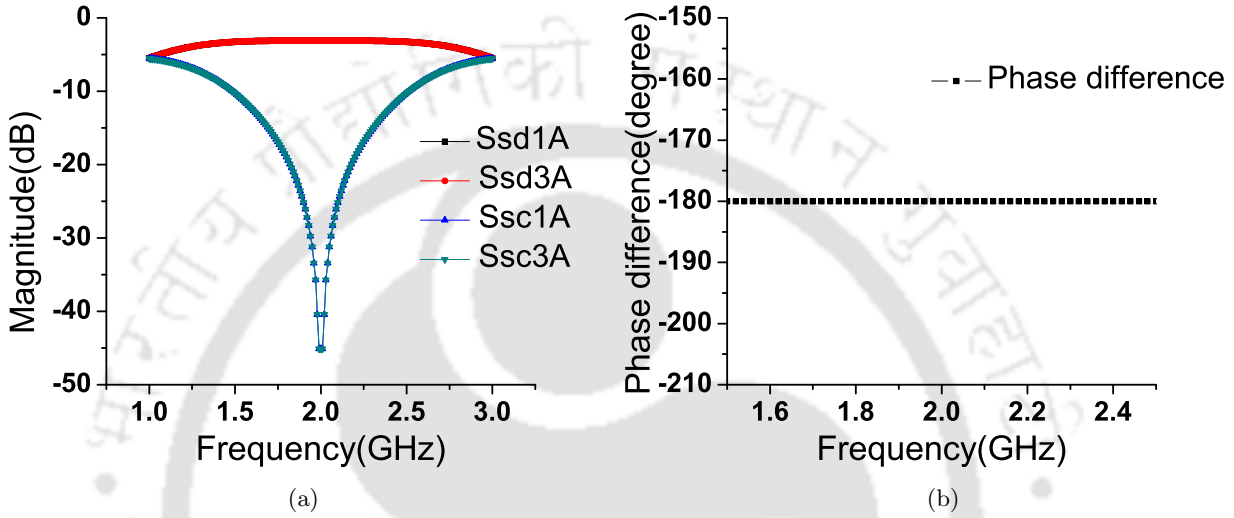


Figure 3.5: (a) Theoretical results of $|S_{sd1A}|$, $|S_{sd3A}|$, $|S_{sc1A}|$ and $|S_{sc3A}|$. (b) Theoretical result of phase difference.

3.1.6 Simulation and Measured Results

Design equations are formulated and theoretical results are computed considering ideal transmission line sections. To evaluate the performance of the proposed power divider, when implemented using practical microstrip lines, first simulation studies are performed.

Simulation of the proposed power divider is carried using HFSS from Ansys Inc. To verify the simulation results a prototype of the proposed power divider is fabricated and shown in Fig. 3.6. Fabrication has been done on FR-4 substrate having $\epsilon_r = 4.4$ and $h = 1.6\ mm$.

Measurement is performed using two port Rohde & Schwarz ZVA24 vector network analyzer. Two port network analyzer directly gives the single-ended S parameters and mixed-mode S parameters obtained using (3.9)-(3.16). The comparisons of simulated and measured results are shown in Figs. 3.7-3.8.

Figure 3.6: Fabricated prototype of proposed Gysel type out-of-phase equal power divider.

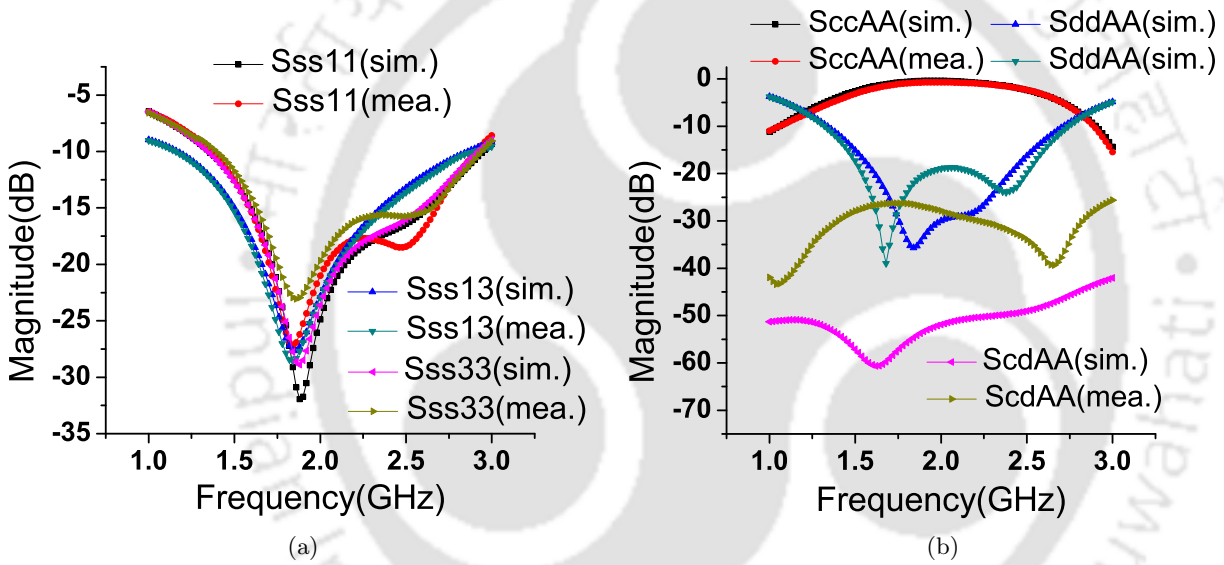
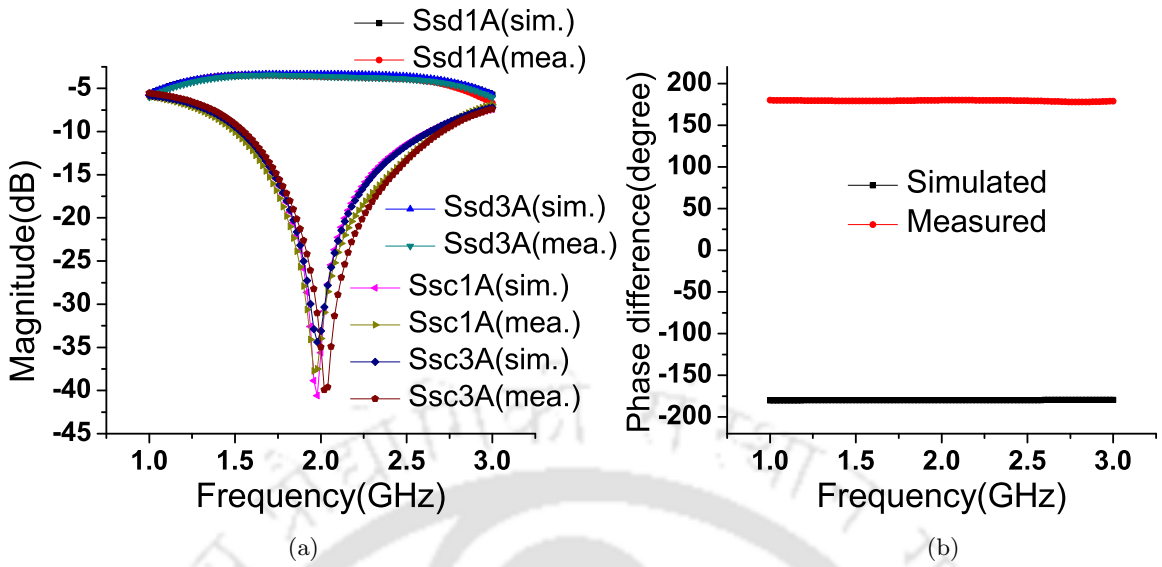


Figure 3.7: (a) Comparison of unbalanced ports S parameters. (b) Comparison of balanced port return loss, common-mode reflection and mode conversion.

In Fig. 3.7(a), return losses of two unbalanced output ports are better than 15 dB over the band 1.64 to 2.64 GHz. Isolation between two unbalanced output ports is better than 15 dB over the band 1.50 to 2.38 GHz. In Fig. 3.7(b), common-mode reflection is better than 1 dB over the frequency range from 1.78 to 2.22 GHz. Differential return loss of balanced port is better than 15 dB over 1.46 GHz to 2.85 GHz band. Mode conversion of balanced port is better than 25 dB over the entire frequency range of simulation and measurement, i.e. from 1 to 3 GHz. In Fig. 3.8(a), insertion loss at the center frequency is 0.6 dB and CMS to unbalanced ports is better than 20 dB over 1.86 to 2.18



(a) (b)

Figure 3.8: (a) Comparison of differential-mode transmission and CMS to unbalanced ports. (b) Comparison of phase difference.

GHz band. Fig. 3.8(b), shows the comparison of the phase difference. Simulation result shows that phase difference is almost constant at $-180°$ and measurement result shows that phase difference is almost constant at $+180°$, which is equivalent to the same angle.

To obtain fractional bandwidth, performance of all mixed-mode S parameters are included. The criteria to obtained relative bandwidth are: (i) Insertion loss is less than 0.8 dB (ii) Common mode reflection is better than 3 dB (iii) Phase variation from out-of-phase characteristic is less than 3° (iv) All other mixed-mode S parameters are better than 10 dB. After including all the above criteria, fractional bandwidth is 41% (from 1.56 GHz to 2.38 GHz).

3.2 Wilkinson Type Out-of-Phase Equal Power Divider

3.2.1 Circuit Model

Circuit model of the proposed Wilkinson type out-of-phase equal power divider is shown in Fig. 3.9. The two unbalanced ports are : ports 1 & 3. Ports 2_+ and 2_- (combined as port A) represent the input balanced port. There is one pair of transmission lines of characteristic impedance Z_1 and electrical length of $\pi/2$. There are two transmission lines of electrical length π and characteristic impedances Z_X and Z_Y. Two isolation resistors each marked as R, are connected between ports 1

and 3.

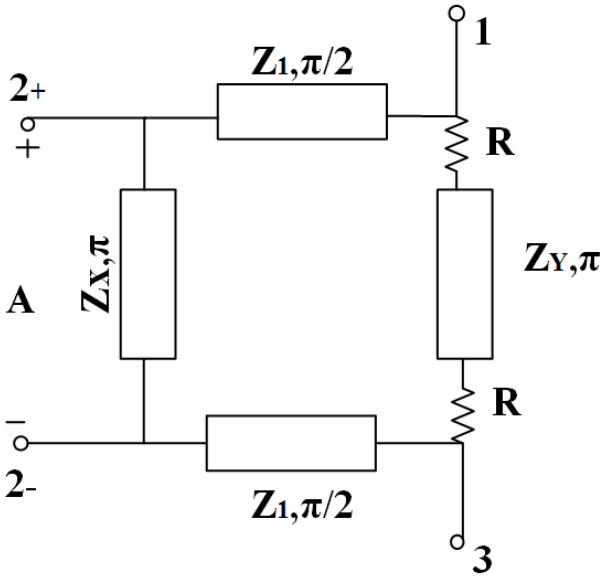


Figure 3.9: Wilkinson type out-of-phase equal power divider.

3.2.2 Standard S Matrix Realization

Basic operation of the out-of-phase Wilkinson equal power divider is similar to the Gysel type equal power divider, as described in section 3.1. Therefore, the standard S matrix of this power divider is same as given in (3.17). A standard S matrix of the Wilkinson equal power divider is given as:

$$[S_{std}] = \begin{bmatrix} 0 & -j\frac{1}{2} & 0 & j\frac{1}{2} \\ -j\frac{1}{2} & -\frac{1}{2} & j\frac{1}{2} & -\frac{1}{2} \\ 0 & j\frac{1}{2} & 0 & -j\frac{1}{2} \\ j\frac{1}{2} & -\frac{1}{2} & -j\frac{1}{2} & -\frac{1}{2} \end{bmatrix} \tag{3.20}$$

3.2.3 Even-Mode Analysis

Fig. 3.10 shows the even-mode equivalent circuit of the proposed power divider. From Fig. 3.10, using quarter-wave impedance transformation property, isolation resistor can be obtained as:

$$R = Z_0 \tag{3.21}$$

where, Z_0 is the port impedance.

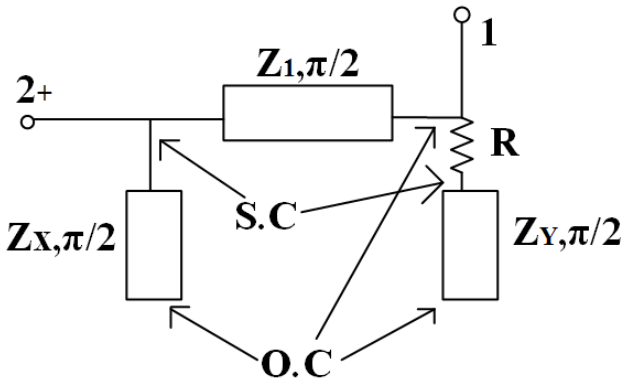


Figure 3.10: Equivalent circuit for carrying out even-mode analysis.

3.2.4 Odd-Mode Analysis

Fig. 3.11 shows the odd-mode equivalent circuit of the proposed power divider. From Fig. 3.11, Z_1 can be chosen as port impedance Z_0.

$$Z_1 = Z_0 \tag{3.22}$$

It may be noted that Z_X and Z_Y can be chosen independently.

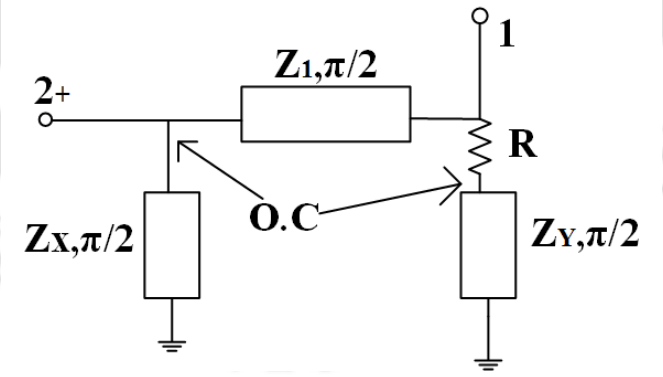


Figure 3.11: Equivalent circuit for carrying out odd-mode analysis.

3.2.5 Implementation of Power Divider Using One Isolation Resistor

As shown in the Fig. 3.9, there are two isolation resistors connected between output ports 1 & 3. The proposed power divider can be implemented using only one isolation resistor. Fig. 3.12 shows the realization of power divider using one isolation resistor. From Fig. 3.12, $[ABCD]$ matrix of the

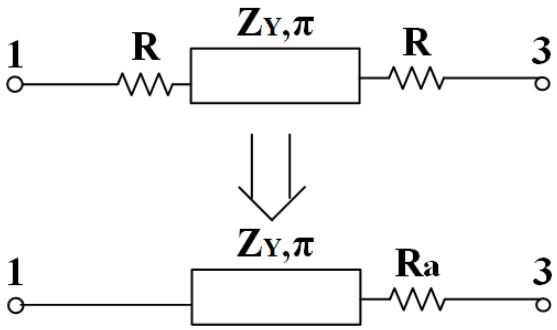


Figure 3.12: Implementation of power divider using one isolation resistor.

circuit consists of two isolation resistors between ports 1 & 3 is obtained as:

$$\begin{bmatrix} 1 & R \\ 0 & 1 \end{bmatrix} \begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} 1 & R \\ 0 & 1 \end{bmatrix} = \begin{bmatrix} -1 & -2R \\ 0 & -1 \end{bmatrix} \tag{3.23}$$

Similarly, From Fig. 3.12, $[ABCD]$ matrix of the circuit consists of one isolation resistor between ports 1 & 3 is obtained as:

$$\begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} 1 & R_a \\ 0 & 1 \end{bmatrix} = \begin{bmatrix} -1 & -R_a \\ 0 & -1 \end{bmatrix} \tag{3.24}$$

Comparing (3.23) & (3.24), R_a is obtained as:

$$R_a = 2R \tag{3.25}$$

Therefore, instead of two isolation resistors, one isolation resistor can be used to realize the proposed power divider.

3.2.6 Theoretical Results

The proposed Wilkinson type out-of-phase equal power divider is designed at 2 GHz. Both Z_X and Z_Y are chosen as 50 Ω. From the design equations (3.21), (3.22) and (3.25), Z_1 and R_a are obtained as 50 Ω and 100 Ω, respectively.

Figs. 3.13-3.14 show theoretical results of the Wilkinson type out-of-phase equal power divider. Fig. 3.13(a) shows the return losses of unbalanced ports and isolation between output ports. At the

center frequency, ports 1 & 3 are perfectly matched and isolated. Fig. 3.13(b) shows differential return loss and common-mode reflection of the balanced port. At the center frequency, balanced port A is perfectly matched and $|S_{ccAA}|$ is 0 dB.

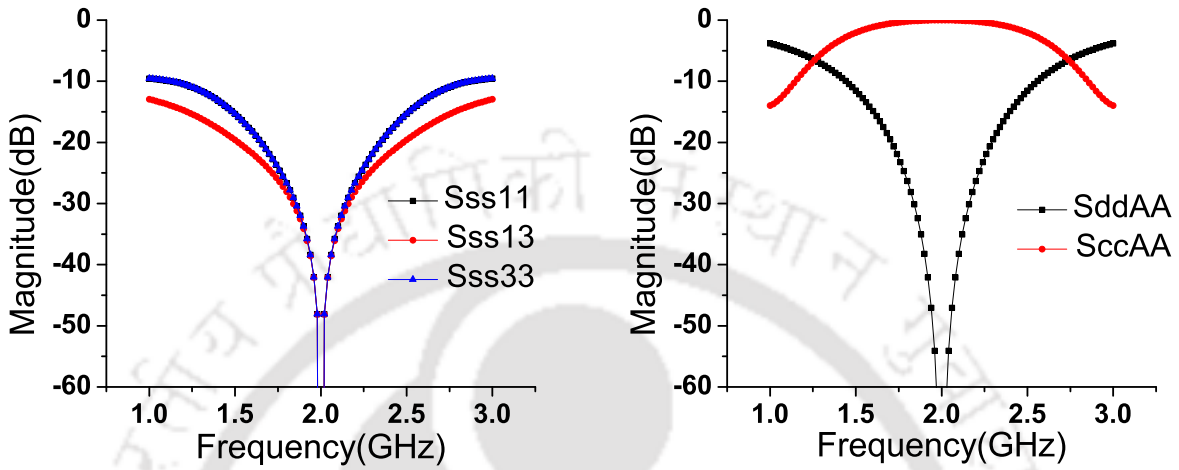


Figure 3.13: (a) Theoretical results of $|S_{ss11}|$, $|S_{ss13}|$ and $|S_{ss33}|$. (b) Theoretical results of $|S_{ddAA}|$ and $|S_{ccAA}|$.

Fig. 3.14(a) shows the differential-mode transmission coefficient and common-mode suppression from balanced port to unbalanced ports. At the center frequency, $|S_{sd1A}|$, $|S_{sd3A}|$ are -3 dB, -3 dB, respectively. Results of $|S_{sc1A}|$ and $|S_{sc3A}|$ show that common-modes are perfectly suppressed. Fig. 3.14(b) shows the phase difference ($Ang(S_{sd1A}/S_{sd3A})$) between two output signals. This shows out-of-phase characteristic of the power divider.

3.2.7 Simulation and Measured Results

HFSS from Ansys Inc. is used for carrying out simulation. The fabricated prototype of the Wilkinson type out-of-phase equal power divider is shown in Fig. 3.15. The FR-4 substrate having $\epsilon_r = 4.4$ is used for fabrication purpose. The comparisons of simulated and measured results are shown in Figs. 3.16-3.17.

In Fig. 3.16(a), measured return losses of two unbalanced output ports are better than 15 dB over the band 1.88 to 2.32 GHz and measured isolation between two unbalanced ports is better than 20 dB over 1.88 to 2.34 GHz band. In Fig. 3.16(b), measured differential return loss of balanced port is better

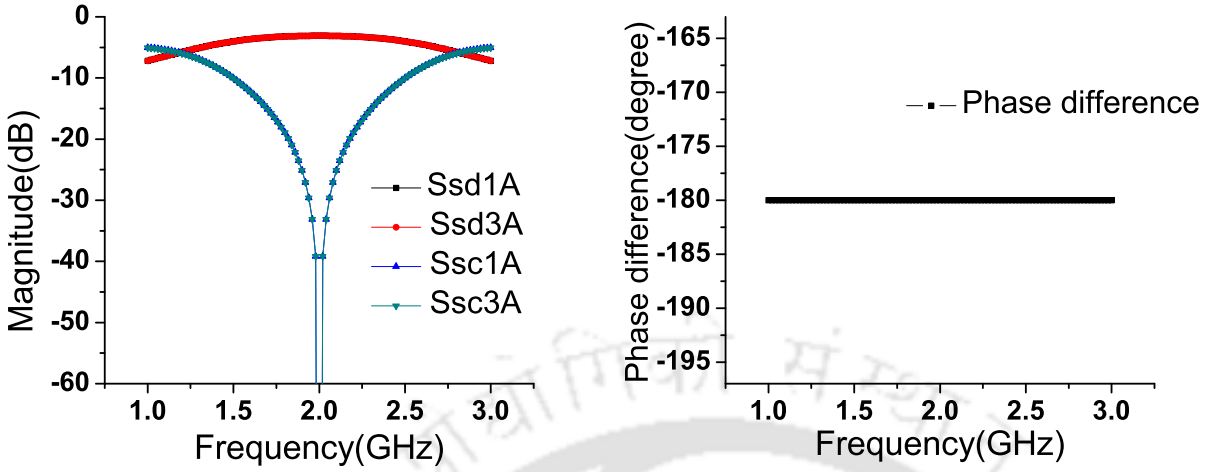


Figure 3.14: (a) Theoretical results of $|S_{sd1A}|$, $|S_{sd3A}|$, $|S_{sc1A}|$ and $|S_{sc3A}|$. (b) Theoretical result of phase difference.

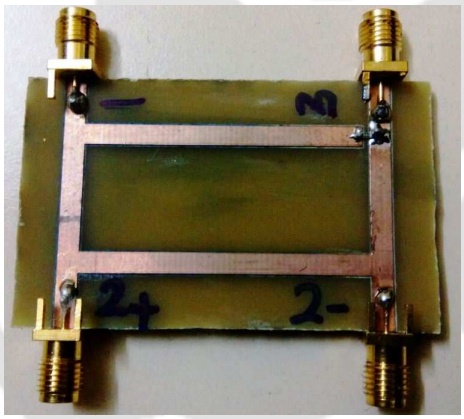
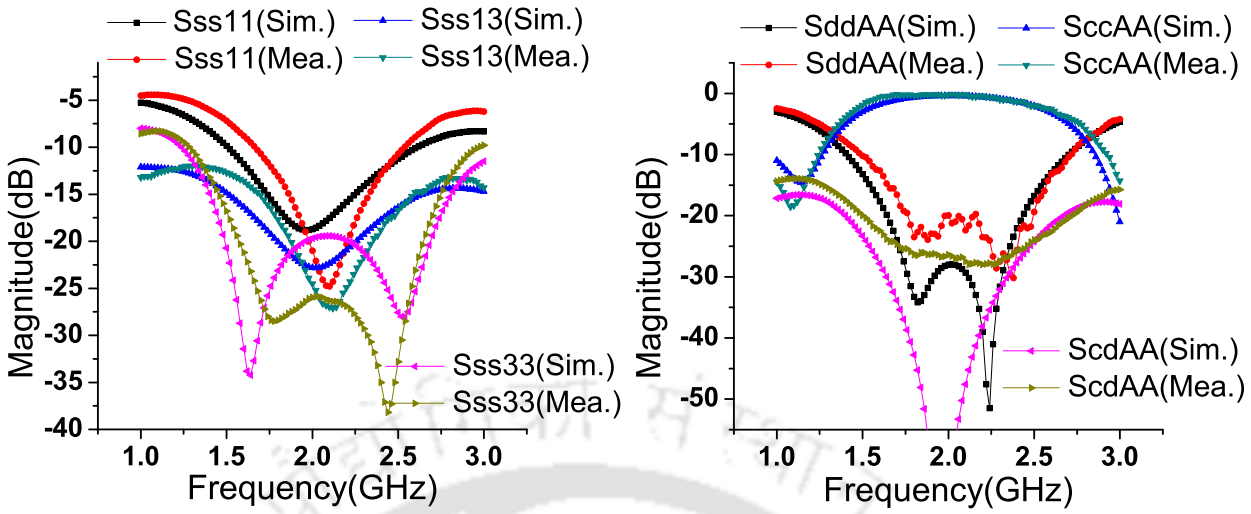


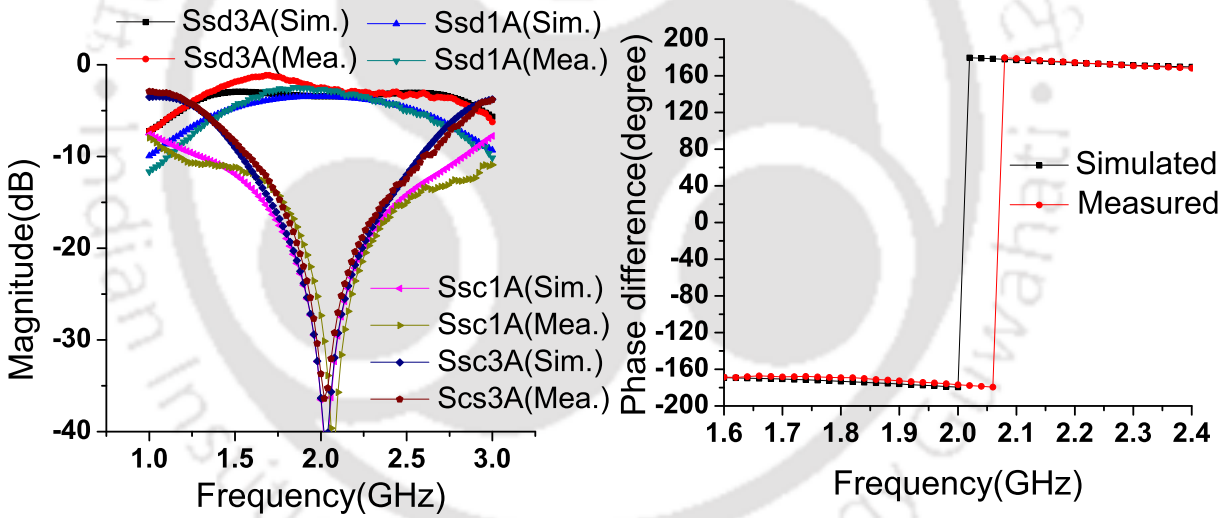
Figure 3.15: Fabricated prototype of proposed Wilkinson type equal power divider.

than 15 dB over the frequency range from 1.66 to 2.56 GHz (fractional bandwidth of 45%). Measured common-mode reflection is better than 1 dB over 1.58 to 2.30 GHz band. Simulated mode conversion is better than 40 dB over the band 1.78 to 2.16 GHz while measured mode conversion of balanced port is better than 25 dB over the same frequency range. In Fig. 3.17(a), shows that differential-mode power is equally divided into unbalanced ports and measured CMS to unbalanced ports is better than 20 dB over the frequency range from 1.92 to 2.20 GHz. In Fig. 3.17(b), comparison of simulated and measured phase difference ($Ang(Ssd1A/Ssd3A)$) shows the out-of-phase characteristic (within $\pm 10°$) of power divider over 1.80 to 2.3 GHz band.



(a) (b)

Figure 3.16: (a) Comparison of unbalanced port S parameters. (b) Comparison of balanced port return loss, common-mode reflection and mode conversion.



(a) (b)

Figure 3.17: (a) Comparison of differential-mode transmission and CMS to unbalanced port. (b) Comparison of phase difference.

3.3 Gysel Type In-phase Equal Power Divider

3.3.1 Structure

The structure of Gysel type in-phase equal power divider is shown in Fig. 3.18. Port A (combination of ports 2 & 4) is the input balanced port and ports 1 & 3 are the unbalanced output ports. There is one pair of transmission lines of electrical length θ_2 and characteristic impedances Z_2 and Z_3. Another pair of transmission lines of electrical length θ_3 and characteristic impedances Z_2 and Z_3. There is one transmission line of characteristic impedance Z_1 and electrical length π. Isolation resistor R is connected to ground.

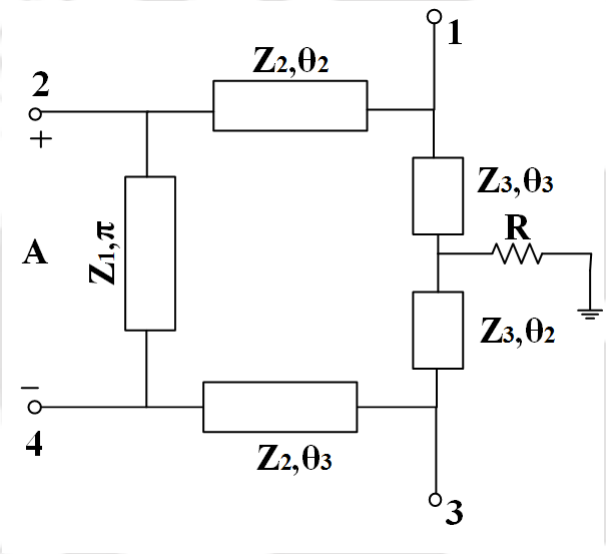


Figure 3.18: Gysel type in-phase equal power divider.

3.3.2 Standard S Matrix Realization

A mixed-mode matrix of in-phase power divider is similar to the out-of-phase power divider given in (3.8). For an in-phase divider, $\phi_1 = -\pi/2$, $\phi_2 = -\pi/2$, $\phi_3 = -\pi$. From (3.8), (3.9)-(3.16), the standard S matrix of an in-phase equal power divider is given in (3.26).

$$[S_{std}] = \begin{bmatrix} 0 & -j\frac{1}{2} & 0 & j\frac{1}{2} \\ -j\frac{1}{2} & -\frac{1}{2} & -j\frac{1}{2} & -\frac{1}{2} \\ 0 & -j\frac{1}{2} & 0 & j\frac{1}{2} \\ j\frac{1}{2} & -\frac{1}{2} & j\frac{1}{2} & -\frac{1}{2} \end{bmatrix} \tag{3.26}$$

3.3.3 Power Transmission from Balanced Port to Output Ports

Under the ideal condition, when balanced port is excited, power should get divided equally to output ports. No power should be dissipated in isolation resistor [16, 20]. Under this condition, ground point moves to the other end of the resistor. Therefore, one end of the transmission lines of characteristic impedance Z_3 is short circuited, as shown in Fig. 3.19.

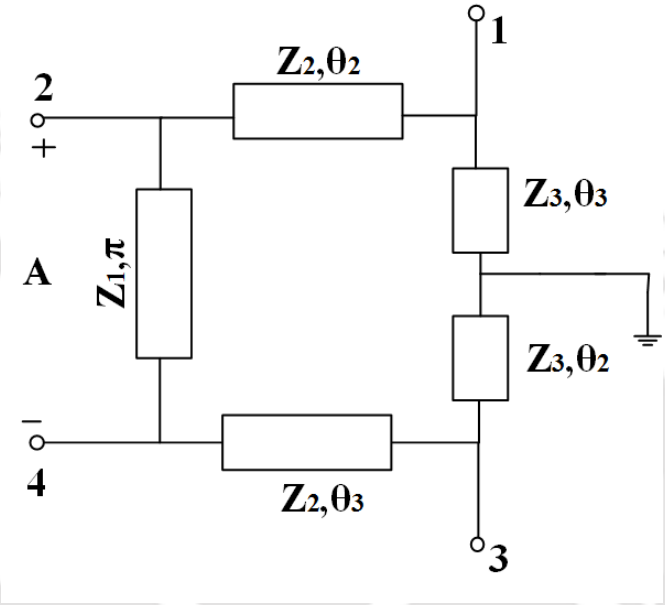


Figure 3.19: Equivalent circuit for power transmission from balanced port to output ports.

The proposed power divider is for in-phase application. Therefore, two output signals should be in-phase. The condition for in-phase equal power is given as:

$$S_{sd1A} = S_{sd3A} \tag{3.27}$$

$$\frac{1}{\sqrt{2}}(S_{21} - S_{41}) = \frac{1}{\sqrt{2}}(S_{23} - S_{43}) \tag{3.28}$$

$$S_{21} + S_{43} = S_{23} + S_{41} \tag{3.29}$$

To satisfy the above condition, S parameters given in (3.29) are required. First the transmission matrix is derived and then using parameter conversion technique, S parameters are obtained.

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{21} = \begin{bmatrix} \cos\theta_2 & jZ_2\sin\theta_2 \\ \frac{j\sin\theta_2}{Z_2} & \cos\theta_2 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{jZ_3\tan\theta_3} & 1 \end{bmatrix} \tag{3.30}$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{21} = \begin{bmatrix} \cos\theta_2 + \frac{Z_2 \sin\theta_2}{Z_3 \tan\theta_3} & jZ_2 \sin\theta_2 \\ \frac{j\sin\theta_2}{Z_2} + \frac{\cos\theta_2}{jZ_3 \tan\theta_3} & \cos\theta_2 \end{bmatrix} \tag{3.31}$$

Now, S_{21} can be obtained using:

$$S_{21} = \frac{2}{A + \frac{B}{Z_0} + CZ_0 + D} \tag{3.32}$$

using (3.31) and (3.32), S_{21} is obtained as:

$$S_{21} = \frac{2}{2\cos\theta_2 + \frac{Z_2 \sin\theta_2}{Z_3 \tan\theta_3} + j\sin\theta_2 \left(\frac{Z_2}{Z_0} + \frac{Z_0}{Z_2}\right) - j\frac{Z_0 \cos\theta_2}{Z_3 \tan\theta_3}} \tag{3.33}$$

Similarly, S_{43} can be obtained by replacing θ_2 with θ_3 and θ_3 with θ_2 in (3.33).

$$S_{43} = \frac{2}{2\cos\theta_3 + \frac{Z_2 \sin\theta_3}{Z_3 \tan\theta_2} + j\sin\theta_3 \left(\frac{Z_2}{Z_0} + \frac{Z_0}{Z_2}\right) - j\frac{Z_0 \cos\theta_3}{Z_3 \tan\theta_2}} \tag{3.34}$$

Similarly, $[ABCD]_{41}$ is obtained as:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{41} = \begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{Z_0} & 1 \end{bmatrix} \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{21} \tag{3.35}$$

Using (3.31) and (3.35), S_{41} is obtained as:

$$S_{41} = -\frac{2}{3\cos\theta_2 + \frac{2Z_2 \sin\theta_2}{\tan\theta_3} + j\frac{2Z_2 \sin\theta_2}{Z_0} + j\frac{Z_0 \sin\theta_2}{Z_2} - j\frac{Z_0 \cos\theta_2}{Z_3 \tan\theta_3}} \tag{3.36}$$

Similarly, S_{23} is obtained as:

$$S_{23} = -\frac{2}{3\cos\theta_3 + \frac{2Z_2 \sin\theta_3}{\tan\theta_2} + j\frac{2Z_2 \sin\theta_3}{Z_0} + j\frac{Z_0 \sin\theta_3}{Z_2} - j\frac{Z_0 \cos\theta_3}{Z_3 \tan\theta_2}} \tag{3.37}$$

For in-phase power divider, condition given in (3.29) is to be satisfied. The condition given in (3.29) is satisfied when θ_2 and θ_3 are related as:

$$\theta_3 = \theta_2 + \pi \tag{3.38}$$

To derive design equations under the condition that no power is dissipated in the isolation resistor, Fig. 3.20 is used.

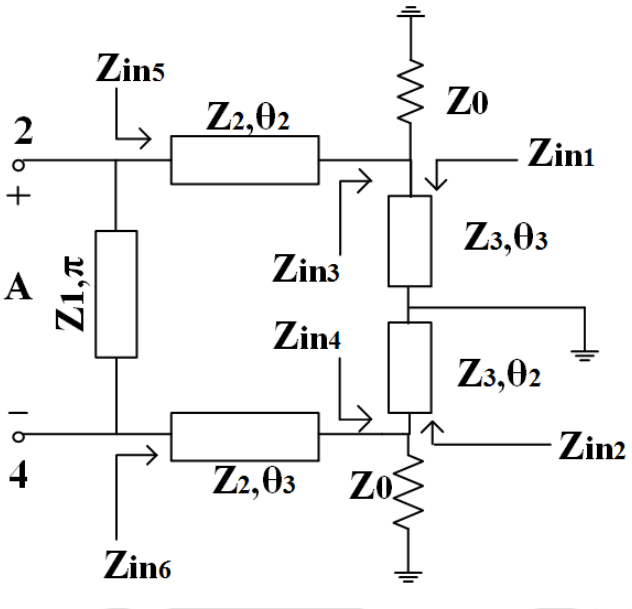


Figure 3.20: Equivalent circuit for power transmission from balanced port to output ports.

From Fig. 3.20, Z_{in1} and Z_{in2} are obtained as:

$$Z_{in1} = jZ_0 \tan\theta_3 = jZ_0 \tan\theta_2 \tag{3.39}$$

$$Z_{in2} = jZ_0 \tan\theta_2 \tag{3.40}$$

Z_{in3} is the parallel combination of Z_0 and Z_{in1}. Z_{in4} is the parallel combination of Z_0 and Z_{in2}. Therefore, Z_{in3} and Z_{in4} are obtained using (3.39) and (3.40) as:

$$Z_{in3} = Z_{in4} = \frac{jZ_3Z_0 \tan\theta_2}{Z_0 + jZ_3 \tan\theta_2} \tag{3.41}$$

From Fig. 3.20, Z_{in5} and Z_{in6} are obtained as:

$$Z_{in5} = Z_{in6} = Z_2 \frac{Z_{in3} + jZ_2 \tan\theta_2}{Z_2 + jZ_{in3} \tan\theta_2} \tag{3.42}$$

For two-port network between ports 2 & 4, $[ABCD]_{24}$ is obtained as:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{24} = \begin{bmatrix} 1 & 0 \\ \frac{1}{Z_{in5}} & 1 \end{bmatrix} \begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{Z_{in6}} & 1 \end{bmatrix} \tag{3.43}$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{24} = \begin{bmatrix} -1 & 0 \\ -\frac{1}{Z_{in5}} - \frac{1}{Z_{in6}} & -1 \end{bmatrix} \tag{3.44}$$

For matching of balanced port A, differential reflection coefficient of balanced port A should be zero.

$$S_{ddAA} = 0 \tag{3.45}$$

$$S_{22} - S_{24} - S_{42} + S_{44} = 0 \tag{3.46}$$

Using parameter conversion process, (3.46) can be written in terms of transmission parameters as:

$$CZ_0 = -2 \tag{3.47}$$

Using (3.44) and (3.47), Z_{in5} is obtained as:

$$Z_{in5} = Z_0 \tag{3.48}$$

Using (3.41), (3.42) and (3.48), following equation is obtained:

$$Z_0^2 Z_3 - Z_2^2 Z_3 - \frac{Z_0^2 Z_2}{\tan^2\theta_2} + j\frac{Z_2^2 Z_0}{\tan\theta_2} = 0 \tag{3.49}$$

To satisfy (3.49), real and imaginary part of (3.49) should be zero. This condition leads to following two equations:

$$\theta_2 = \frac{\pi}{2} \tag{3.50}$$

$$Z_2 = Z_0 \tag{3.51}$$

3.3.4 Isolation Analysis

Under this analysis, if port 1 is excited, no power should flow to port 3. This happens when port 3 is short circuited [16,20]. If port 3 is short circuited then other ends of the transmission lines connected to it are open circuited (using quarter-wave transformer). Under this condition, the equivalent circuit of the power divider is shown in Fig. 3.21.

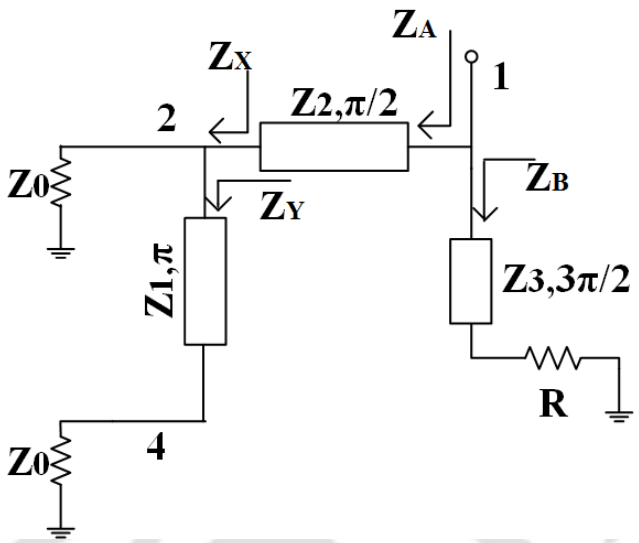


Figure 3.21: Equivalent circuit for isolation analysis.

From Fig. 3.21, Z_Y is obtained as:

$$Z_Y = Z_0 \tag{3.52}$$

Z_X is the parallel combination of Z_0 and Z_Y, as shown in Fig. 3.21.

$$Z_X = Z_0 || Z_Y = \frac{Z_0}{2} \tag{3.53}$$

Z_A can be obtained using quarter-wave transformer property as:

$$Z_A = \frac{Z_2^2}{Z_X} = \frac{2Z_2^2}{Z_0} \tag{3.54}$$

Using (3.51) and (3.54), Z_A can be written as:

$$Z_A = 2Z_0 \tag{3.55}$$

From Fig. 3.21, Z_B is obtained using quarter-wave transformer property as:

$$Z_B = \frac{Z_3^2}{R} \tag{3.56}$$

The parallel combination of Z_A and Z_B should be equal to port impedance Z_0.

$$Z_A||Z_B = Z_0 \tag{3.57}$$

Using (3.55)-(3.57), Z_3 is obtained as:

$$Z_3 = \sqrt{2RZ_0} \tag{3.58}$$

Z_1 and R can be chosen independently.

3.3.5 Implementation of Transmission Line of Electrical Length $3\pi/2$

Using (3.38) and (3.50), $\theta_3 = 3\pi/2$. Therefore, there are two lines of electrical length $3\pi/2$ in this power divider. The size of the circuit will be very large because of two lines of electrical length $3\pi/2$. For size reduction of the circuit, an alternative method is used to implement the two lines of electrical length $3\pi/2$.

A coupled line of electrical length θ, short circuited at both ends can be used as a line of electrical length $180 + \theta$ [104], as shown in Fig. 3.22.

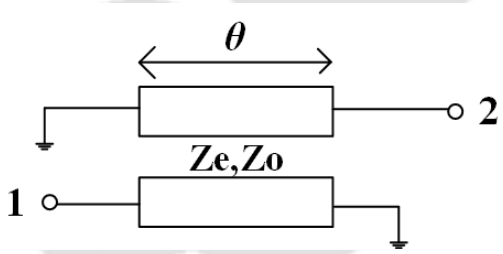


Figure 3.22: Short circuited coupled line of electrical lenght θ.

For a short circuited coupled line, even- and odd-mode impedances are given as [105]:

$$Z_e = Z_i\left(\sqrt{1 + csc^2\theta} + csc\theta\right) \tag{3.59}$$

$$Z_o = Z_i\left(\sqrt{1 + csc^2\theta} - csc\theta\right) \tag{3.60}$$

$$Z_i = \sqrt{Z_e Z_o} \tag{3.61}$$

If $\theta = \pi/2$, even- and odd-mode impedances are given as [105]:

$$Z_e = Z_i\left(\sqrt{2}+1\right) \tag{3.62}$$

$$Z_o = Z_i\left(\sqrt{2}-1\right) \tag{3.63}$$

Very tight coupling is required to implement short circuited coupled line based on (3.59)-(3.63). Due to very tight coupling, coupled line gap is very narrow which is very difficult to fabricate.

Parallel coupled lines are widely used for implementing various passive components [106–108]. Therefore, two parallel-coupled lines are introduced and their equivalent even- and odd-mode impedances Z_{e1} and Z_{o1} are given in [105] as:

$$Z_{e1} = \frac{Z_o + Z_e}{3Z_o + Z_e} Z_e \tag{3.64}$$

$$Z_{o1} = \frac{Z_o + Z_e}{3Z_e + Z_o} Z_o \tag{3.65}$$

where, Z_e & Z_o are the even- and odd-mode impedances of individual coupled line.

To further enhance the coupling, a large aperture is etched [109] and floating conductor [110] is used under the coupled lines. Fig. 3.23 shows the modified coupled line structure.

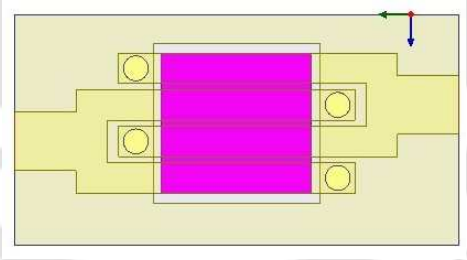


Figure 3.23: Modified coupled line structure.

3.3.6 Theoretical Results

The in-phase power divider is designed at 2 GHz. Both Z_1 and R are chosen as 50 Ω. From the design equations (3.51) and (3.58), Z_2 and Z_3 are obtained as 50 Ω and 70.71 Ω, respectively.

Theoretical results based on short circuited coupled line structure are shown in Figs. 3.24-3.25. Fig. 3.24(a) shows the return losses of unbalanced ports and isolation between output ports. At the center frequency, both unbalanced ports are perfectly matched and isolated. Fig. 3.24(b) shows

differential return loss of balanced port, common-mode reflection of the balanced port and differential to common-mode conversion. At the center frequency, balanced port is perfectly matched, common-mode reflection is 0 dB and no mode conversion between differential and common-mode.

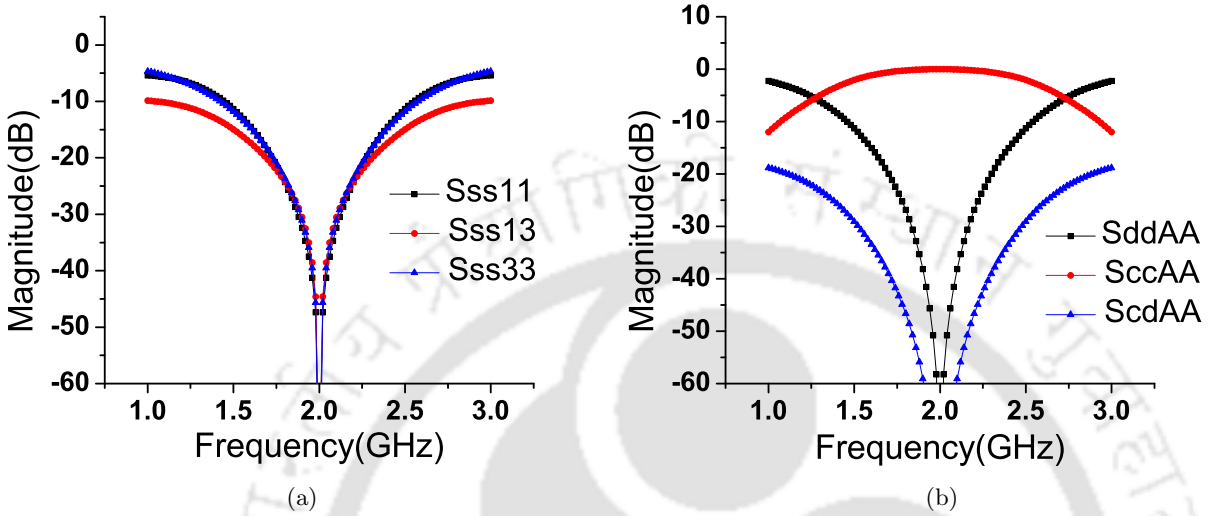


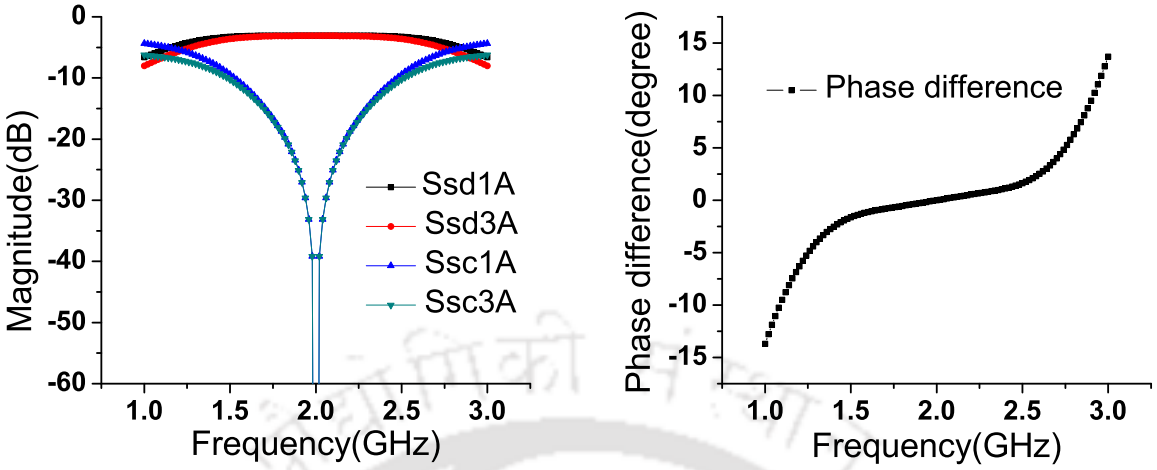
Figure 3.24: (a) Theoretical results of $|S_{ss11}|$, $|S_{ss13}|$ and $|S_{ss33}|$. (b) Theoretical results of $|S_{ddAA}|$, $|S_{ccAA}|$ and $|S_{cdAA}|$.

Fig. 3.25(a) shows the differential-mode transmission coefficient and common-mode suppression from balanced port to unbalanced ports. At the center frequency, both $|S_{sd1A}|$ and $|S_{sd3A}|$ are -3 dB. Results of $|S_{sc1A}|$ and $|S_{sc3A}|$ show that common-modes are perfectly suppressed. Fig. 3.25(b) shows the phase difference ($Ang(S_{sd1A}/S_{sd3A})$) between two output signals. This shows in-phase characteristic of the power divider.

3.3.7 Simulation and Measured Results

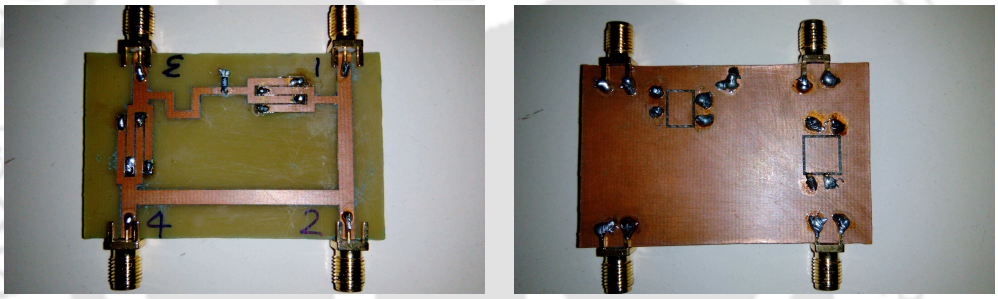
Simulation has been carried on HFSS. A prototype of in-phase power divider has been fabricated and shown in Fig. 3.26. Fig. 3.26(a) shows the top layer and Fig. 3.26(b) shows the bottom layer of the fabricated prototype. Comparisons of simulated and measured results are shown in Figs. 3.27-3.28.

In Fig. 3.27(a), measured return losses of two unbalanced output ports are better than 15 dB over 1.84 to 2.14 GHz band. Isolation between two unbalanced output ports is better than 15 dB over the frequency range from 1.32 to 2.20 GHz. In Fig. 3.27(b), measured common-mode reflection is better



(a) (b)

Figure 3.25: (a) Theoretical results of $|S_{sd1A}|$, $|S_{sd3A}|$, $|S_{sc1A}|$ and $|S_{sc3A}|$. (b) Theoretical result of phase difference.

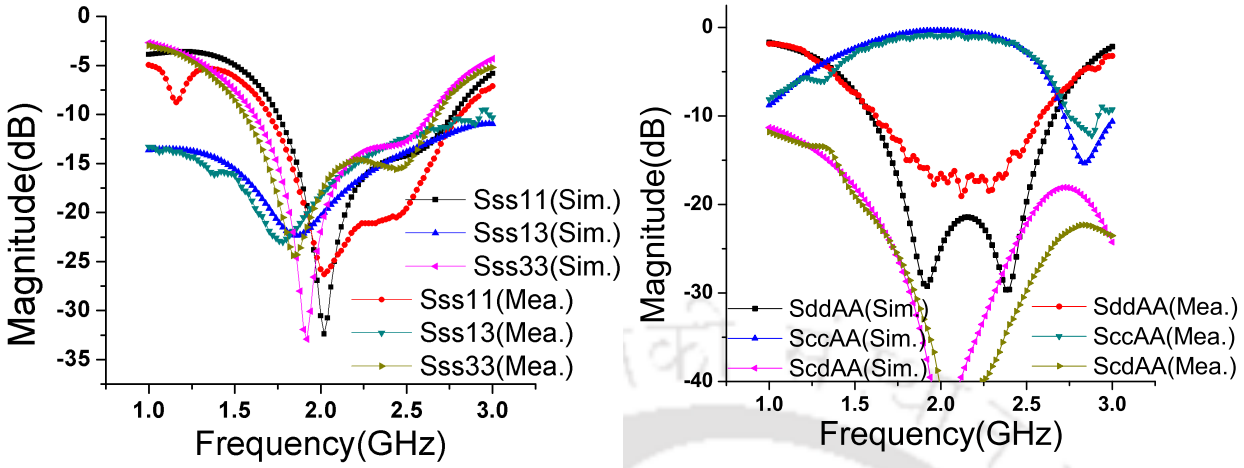


(a) (b)

Figure 3.26: (a) Top layer of power divider. (b) Bottom layer of power divider.

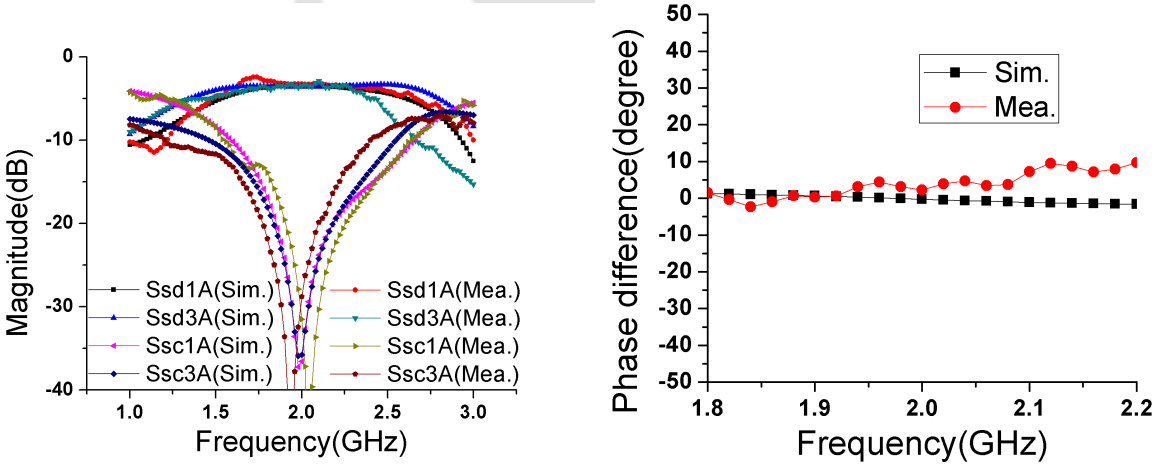
than 1.5 dB over 1.7 to 2.34 GHz band. Measured differential return loss of balanced port is better than 15 dB over the band 1.88 GHz to 2.4 GHz. Measured mode conversion of balanced port is better than 30 dB over the band 1.86 to 2.48 GHz. In Fig. 3.28(a), power is divided equally to unbalanced ports around design frequency and measured CMS to unbalanced ports is better than 15 dB over 1.84 to 2.20 GHz band. In Fig. 3.28(b), measured phase difference shows that maximum phase deviation of 10° from in-phase characteristic over the frequency range from 1.80 to 2.20 GHz.

The fractional bandwidth of the proposed in-phase power divider is obtained by considering following parameters: (i) $|S_{cc24}|$ is less than 1.5 dB (ii) Phase variation from in-phase characteristic is less than 10° (iii) S parameters ($|S_{ss11}|$, $|S_{ss13}|$, $|S_{ss33}|$, $|S_{ddAA}|$, $|S_{cdAA}|$, $|S_{sc1A}|$, $|S_{sc3A}|$) are greater than



(a) (b)

Figure 3.27: (a) Comparison of unbalanced port S parameters. (b) Comparison of balanced port return loss, common-mode reflection and mode conversion.



(a) (b)

Figure 3.28: (a) Comparison of differential-mode transmission and CMS to unbalanced port. (b) Comparison of phase difference.

10 dB. Fractional bandwidth is 20% (1.80 GHz to 2.20 GHz) after including all the above parameters.

3.4 Gysel Type Out-of-Phase Arbitrary Power Divider

3.4.1 Structure

The structure of the power divider with arbitrary power division is shown in Fig. 3.29. Output ports 1 and 3 are the two unbalanced ports. Balanced input port comprises of ports 2 & 4 (combined as A). There are four transmission lines of electrical length $\pi/2$ and characteristic impedances Z_1, Z_2, Z_4 and Z_5, respectively. A transmission line of characteristic impedance Z_3 is of electrical length π. One end of the isolation resistance R is connected to the ground, as shown in Fig. 3.29.

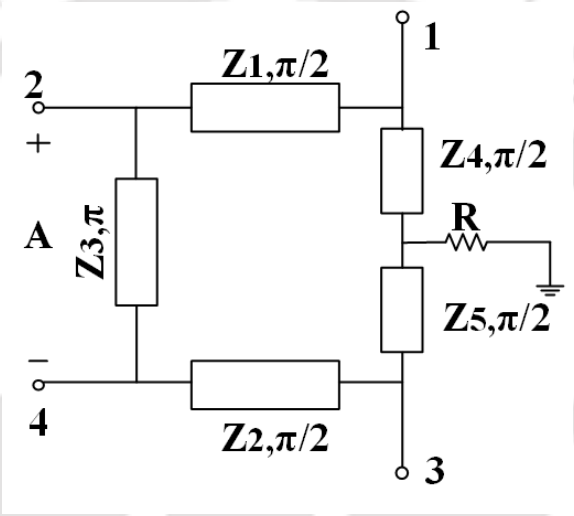


Figure 3.29: BTU power divider with arbitrary power division.

3.4.2 Standard S Matrix Realization

The BTU power divider with arbitrary power division is a four port network. The required mixed-mode scattering matrix of such power divider is given as:

$$[S^{mm}] = \begin{bmatrix} S_{ddAA} & S_{dcAA} & S_{dsA1} & S_{dsA3} \\ S_{cdAA} & S_{ccAA} & S_{csA1} & S_{csA3} \\ S_{sd1A} & S_{sd3A} & S_{ss11} & S_{ss13} \\ S_{sc1A} & S_{sc3A} & S_{ss31} & S_{ss33} \end{bmatrix} \tag{3.66}$$

Based on the requirements of the power divider with arbitrary power division, constraints for the mixed-mode parameters are given as:

(i) Single-ended S parameters such as reflection coefficient of unbalanced ports and coupling should be zero.

$$|S_{ss11}| = |S_{ss33}| = |S_{ss13}| = 0 \tag{3.67}$$

(ii) Differential-mode reflection coefficient and differential-mode to common-mode conversion coefficient should be zero.

$$|S_{ddAA}| = |S_{cdAA}| = |S_{cdAA}| = 0 \tag{3.68}$$

(iii) Common-mode reflection should be unity.

$$|S_{ccAA}| = 1 \tag{3.69}$$

(iv) CMS should be zero.

$$|S_{csA1}| = |S_{csA3}| = |S_{sc1A}| = |S_{sc3A}| = 0 \tag{3.70}$$

(v) Power should be divided in the specific power division ratio from balanced port to unbalanced ports.

$$|S_{dsA1}| = |S_{sd1A}| = \alpha \tag{3.71}$$

$$|S_{dsA3}| = |S_{sd3A}| = \sqrt{1-\alpha^2} \tag{3.72}$$

where, $0 < \alpha < 1$ is the transmission coefficient from balanced port A to unbalanced port 1. Based on (3.66)-(3.72), mixed-mode S matrix is derived and given in (3.73).

$$[S^{mm}] = \begin{bmatrix} 0 & 0 & \alpha e^{j\phi_1} & \frac{\sqrt{1-\alpha^2}}{e^{-j\phi_2}} \\ 0 & \alpha e^{j\phi_3} & 0 & 0 \\ \alpha e^{j\phi_1} & \frac{\sqrt{1-\alpha^2}}{e^{-j\phi_2}} & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \tag{3.73}$$

where, ϕ_1, ϕ_2, ϕ_3 are the phases of different mixed-mode S parameters.

To convert the mixed-mode S parameters into standard S parameters, (3.9)-(3.16) are used. The

standard S matrix for the BTU power divider with arbitrary power division is obtained as:

$$[S_{std}] = \begin{bmatrix} 0 & \frac{\alpha}{\sqrt{2}}e^{j\phi_1} & 0 & -\frac{\alpha}{\sqrt{2}}e^{j\phi_1} \\ \frac{\alpha}{\sqrt{2}}e^{j\phi_1} & \frac{1}{2}e^{j\phi_3} & \frac{\sqrt{1-\alpha^2}}{\sqrt{2}e^{-j\phi_2}} & \frac{1}{2}e^{j\phi_3} \\ 0 & \frac{\sqrt{1-\alpha^2}}{\sqrt{2}e^{-j\phi_2}} & 0 & -\frac{\sqrt{1-\alpha^2}}{\sqrt{2}e^{-j\phi_2}} \\ -\frac{\alpha}{\sqrt{2}}e^{j\phi_1} & \frac{1}{2}e^{j\phi_3} & -\frac{\sqrt{1-\alpha^2}}{\sqrt{2}e^{-j\phi_2}} & \frac{1}{2}e^{j\phi_3} \end{bmatrix} \tag{3.74}$$

For out-of-phase property, $\phi_1 = -\pi/2$, $\phi_2 = \pi/2$, $\phi_3 = -\pi$.

3.4.3 Two-port Network between Ports 1 and 3

The structure of the two-port network between ports 1 and 3 is shown in Fig. 3.30. Ports 2 and 4 are terminated with matched loads. From (3.74), the S matrix of the two port network between ports 1 and 3 while the other ports are terminated with matched load is given as:

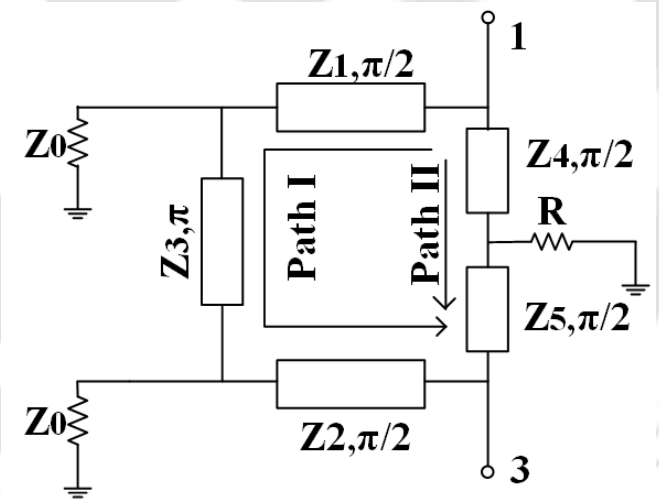


Figure 3.30: Two port network between ports 1 and 3.

$$[S]_{13} = \begin{bmatrix} S_{11} & S_{13} \\ S_{31} & S_{33} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{3.75}$$

The Y matrix which corresponds to $[S]_{13}$ is:

$$[Y]_{13} = \begin{bmatrix} Y_{11} & Y_{13} \\ Y_{31} & Y_{33} \end{bmatrix} = \begin{bmatrix} Y_0 & 0 \\ 0 & Y_0 \end{bmatrix} \tag{3.76}$$

From the structure as shown in Fig. 3.30, Y matrix between ports 1 and 3 can be obtained as:

$$[Y]_{13} = [Y]_{pathI} + [Y]_{pathII} \tag{3.77}$$

To derive $[Y]_{pathI}$ and $[Y]_{pathII}$ matrix, first $[ABCD]_{pathI}$ and $[ABCD]_{pathII}$ matrices are derived from Fig. 3.30 and then matrix transformations are used. $[ABCD]_{pathI}$ is derived from Fig. 3.30 as:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{pathI} = \begin{bmatrix} 0 & jZ_1 \\ \frac{j}{Z_1} & 0 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ Y_0 & 1 \end{bmatrix} \begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ Y_0 & 1 \end{bmatrix} \begin{bmatrix} 0 & jZ_2 \\ \frac{j}{Z_2} & 0 \end{bmatrix} \tag{3.78}$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{pathI} = \begin{bmatrix} \frac{Z_1}{Z_2} & 2Y_0Z_1Z_2 \\ 0 & \frac{Z_2}{Z_1} \end{bmatrix} \tag{3.79}$$

$[ABCD]_{pathII}$ is derived from Fig. 3.30 as:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{pathII} = \begin{bmatrix} 0 & jZ_4 \\ \frac{j}{Z_4} & 0 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{R} & 1 \end{bmatrix} \begin{bmatrix} 0 & jZ_5 \\ \frac{j}{Z_5} & 0 \end{bmatrix} \tag{3.80}$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{pathII} = \begin{bmatrix} -\frac{Z_4}{Z_5} & \frac{-Z_4Z_5}{R} \\ 0 & -\frac{Z_5}{Z_4} \end{bmatrix} \tag{3.81}$$

Using matrix transformation, $[Y]_{pathI}$ and $[Y]_{pathII}$ are obtained from $[ABCD]_{pathI}$ and $[ABCD]_{pathII}$ as:

$$[Y]_{pathI} = \begin{bmatrix} \frac{1}{2Y_0Z_1^2} & -\frac{1}{2Y_0Z_1Z_2} \\ -\frac{1}{2Y_0Z_1Z_2} & \frac{1}{2Y_0Z_2^2} \end{bmatrix} \tag{3.82}$$

$$[Y]_{pathII} = \begin{bmatrix} \frac{R}{Z_4^2} & \frac{R}{Z_4Z_5} \\ \frac{R}{Z_4Z_5} & \frac{R}{Z_5^2} \end{bmatrix} \tag{3.83}$$

$[Y]_{13}$ is obtained using (3.77), (3.82) and (3.83) as:

$$[Y]_{13} = \begin{bmatrix} \frac{R}{Z_4^2} + \frac{1}{2Y_0Z_1^2} & \frac{R}{Z_4Z_5} - \frac{1}{2Y_0Z_1Z_2} \\ \frac{R}{Z_4Z_5} - \frac{1}{2Y_0Z_1Z_2} & \frac{R}{Z_5^2} + \frac{1}{2Y_0Z_2^2} \end{bmatrix} \tag{3.84}$$

Comparing (3.76) and (3.84), following equations are obtained:

$$2Y_0 Z_1 Z_2 R = Z_4 Z_5 \tag{3.85}$$

$$\frac{R}{Z_4^2} + \frac{1}{2Y_0 Z_1^2} = Y_0 \tag{3.86}$$

$$\frac{R}{Z_5^2} + \frac{1}{2Y_0 Z_2^2} = Y_0 \tag{3.87}$$

3.4.4 Two-port Network between Ports 1 and 2

The structure of the two-port network between ports 1 and 2 is shown in Fig. 3.31. Ports 3 and 4 are terminated with matched loads. From (3.74), the S matrix of the two port network between ports 1 and 2 while the other ports are terminated with matched load is given as:

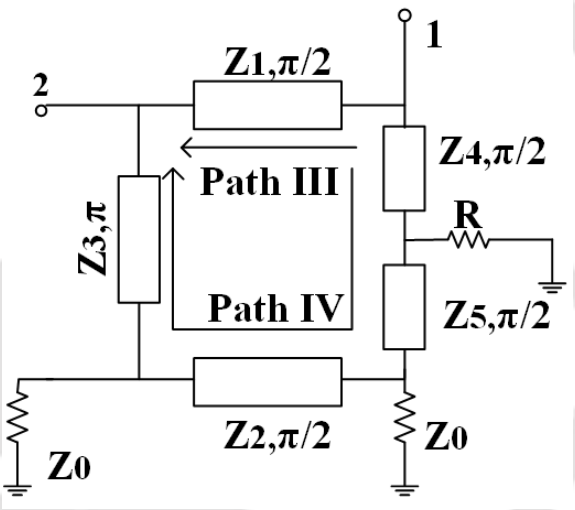


Figure 3.31: Two port network between ports 1 and 2.

$$[S]_{12} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} 0 & -j\frac{\alpha}{\sqrt{2}} \\ -j\frac{\alpha}{\sqrt{2}} & -\frac{1}{2} \end{bmatrix} \tag{3.88}$$

Using matrix transformation, corresponding $[Y]_{12}$ matrix is obtained as:

$$[Y]_{12} = \begin{bmatrix} \frac{1-\alpha^2}{1+\alpha^2} Y_0 & j\frac{2\sqrt{2}\alpha}{1+\alpha^2} Y_0 \\ j\frac{2\sqrt{2}\alpha}{1+\alpha^2} Y_0 & \frac{3-\alpha^2}{1+\alpha^2} Y_0 \end{bmatrix} \tag{3.89}$$

From Fig. 3.31, $[Y]_{12}$ matrix between ports 1 and 2 can be obtained as:

$$[Y]_{12} = [Y]_{pathIII} + [Y]_{pathIV} \tag{3.90}$$

$[Y]_{pathIII}$ is derived from $[ABCD]_{pathIII}$ using matrix transformation. $[ABCD]_{pathIII}$ is obtained from Fig. 3.31 as:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{pathIII} = \begin{bmatrix} 0 & jZ_1 \\ \frac{j}{Z_1} & 0 \end{bmatrix} \tag{3.91}$$

$[Y]_{pathIII}$ is obtained from $[ABCD]_{pathIII}$.

$$[Y]_{pathIII} = \begin{bmatrix} 0 & \frac{j}{Z_1} \\ \frac{j}{Z_1} & 0 \end{bmatrix} \tag{3.92}$$

Using (3.89), (3.90) and (3.92), $[Y]_{pathIV}$ is obtained as:

$$[Y]_{pathIV} = [Y]_{12} - [Y]_{pathIII} \tag{3.93}$$

$$[Y]_{pathIV} = \begin{bmatrix} \frac{1-\alpha^2}{1+\alpha^2}Y_0 & j\frac{2\sqrt{2}\alpha}{1+\alpha^2}Y_0 - \frac{j}{Z_1} \\ j\frac{2\sqrt{2}\alpha}{1+\alpha^2}Y_0 - \frac{j}{Z_1} & \frac{3-\alpha^2}{1+\alpha^2}Y_0 \end{bmatrix} \tag{3.94}$$

$[Y]_{pathIV}$ from (3.94) is converted into $[ABCD]_{pathIV}$ using matrix transformation. All the elements of $[ABCD]_{pathIV}$ are derived and given in (3.95)-(3.98).

$$A_{pathIV} = j\frac{\left(3-\alpha^2\right)Z_1Y_0}{\left(2\sqrt{2}\alpha Z_1Y_0 - 1 - \alpha^2\right)} \tag{3.95}$$

$$B_{pathIV} = j\frac{\left(1+\alpha^2\right)Z_1}{\left(2\sqrt{2}\alpha Z_1Y_0 - 1 - \alpha^2\right)} \tag{3.96}$$

$$C_{pathIV} = j\frac{Z_1\left(1-\alpha^2\right)\left(3-\alpha^2\right)Y_0^2}{\left(2\sqrt{2}\alpha Z_1Y_0 - 1 - \alpha^2\right)\left(1+\alpha^2\right)} + j\frac{\left(2\sqrt{2}\alpha Z_1Y_0 - 1 - \alpha^2\right)}{\left(1+\alpha^2\right)Z_1} \tag{3.97}$$

$$D_{pathIV} = j\frac{\left(1-\alpha^2\right)Y_0Z_1}{\left(2\sqrt{2}\alpha Z_1Y_0 - 1 - \alpha^2\right)} \tag{3.98}$$

$[ABCD]_{pathIV}$ can also be obtained in another way from Fig. 3.31. $[ABCD]_{pathIV}$ is derived from

Fig. 3.31 as:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{pathIV} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{pathII} \begin{bmatrix} 1 & 0 \\ Y_0 & 1 \end{bmatrix} \begin{bmatrix} 0 & jZ_2 \\ \frac{j}{Z_2} & 0 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ Y_0 & 1 \end{bmatrix} \begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix} \tag{3.99}$$

All the elements of $[ABCD]_{pathIV}$ from (3.99) are derived and given in (3.100)-(3.103).

$$A_{pathIV} = j\frac{Z_2 Y_0 Z_4}{Z_5} + j\frac{Z_2 Y_0^2 Z_4 Z_5}{R} + j\frac{Z_4 Z_5}{R Z_2} \tag{3.100}$$

$$B_{pathIV} = j\frac{Z_2 Z_4}{Z_5} + j\frac{Z_4 Z_5 Y_0 Z_2}{R} \tag{3.101}$$

$$C_{pathIV} = j\frac{Z_2 Z_5 Y_0^2}{Z_4} + j\frac{Z_5}{Z_4 Z_2} \tag{3.102}$$

$$D_{pathIV} = j\frac{Z_5 Y_0 Z_2}{Z_4} \tag{3.103}$$

From (3.95), (3.96), (3.100) and (3.101), ratio of A_{pathIV} and B_{pathIV} $\left(\frac{A_{pathIV}}{B_{pathIV}}\right)$ gives following equation:

$$\frac{1}{Z_2^2} - \frac{2RY_0(1-\alpha^2)}{(1+\alpha^2)}\frac{1}{Z_5^2} = \frac{2Y_0^2(1-\alpha^2)}{(1+\alpha^2)} \tag{3.104}$$

From (3.96), (3.98), (3.101) and (3.103), ratio of B_{pathIV} and D_{pathIV} $\left(\frac{B_{pathIV}}{D_{pathIV}}\right)$ gives following equation:

$$\frac{1}{Z_5^2} - \frac{(1+\alpha^2)}{(1-\alpha^2)}\frac{1}{Z_4^2} = -\frac{Y_0}{R} \tag{3.105}$$

From (3.87) and (3.104), Z_2 and Z_5 are obtained as:

$$Z_2 = \frac{Z_0/\sqrt{2}}{\sqrt{1-\alpha^2}} \tag{3.106}$$

$$Z_5 = \frac{\sqrt{RZ_0}}{\alpha} \tag{3.107}$$

From (3.105) and (3.107), Z_4 is obtained as:

$$Z_4 = \sqrt{\frac{RZ_0}{1-\alpha^2}} \tag{3.108}$$

From (3.86) and (3.108), Z_1 is obtained as:

$$Z_1 = \frac{Z_0/\sqrt{2}}{\alpha} \tag{3.109}$$

From (3.85), isolation resistor R is obtained as:

$$R = \frac{Z_4 Z_5}{2Y_0 Z_1 Z_2} \tag{3.110}$$

Let the power division ratio between ports 1 and 3 be $1 : k^2$. Therefore, $\frac{|S_{dsA1}|}{|S_{dsA3}|} = \frac{1}{k}$. From (3.73), α can be obtained as: $\alpha = \frac{1}{\sqrt{1+k^2}}$. It may be noted that Z_3 can be chosen independently.

3.4.5 Variation of Impedance and Phase Difference with Power Division Ratio

Fig. 3.32(a) shows the required values for different characteristic impedance (Z_1, Z_2, Z_4, Z_5) as a function of power division ratio. Z_1 and Z_5 increases with power division ratio, whereas Z_2 and Z_4 decreases with power division ratio.

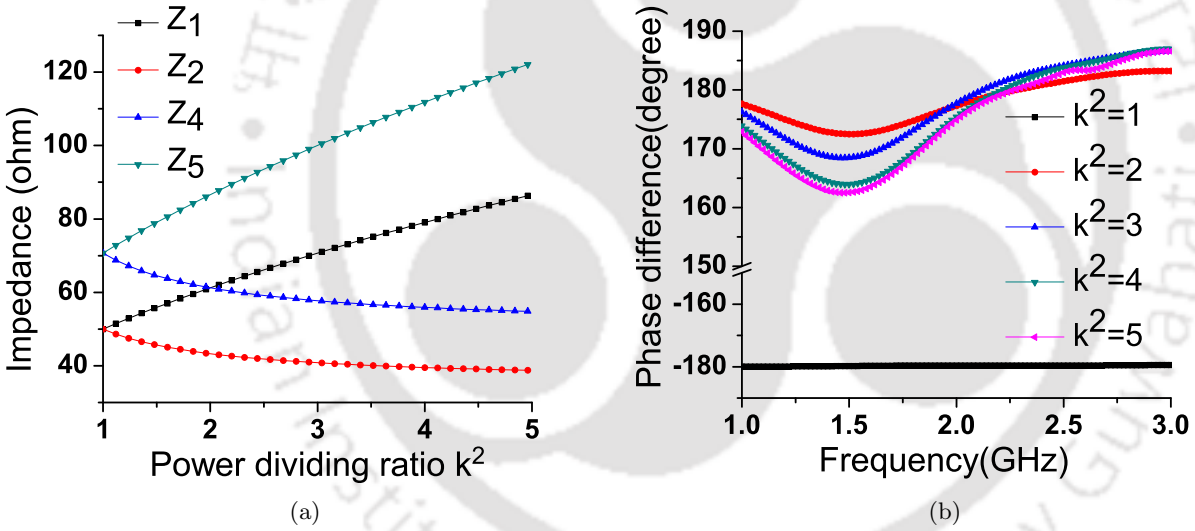


Figure 3.32: (a) Impedance vs Power division ratio (k^2). (b) Unwrapped phase difference for different power division ratio (k^2).

Fig. 3.32(b) shows the simulation results of unwrapped phase difference $(Ang(S_{sd1A}/S_{sd3A}))$ between output signals for different power division ratio as a function of frequency. For power division ratio $k^2 = 1$, the phase difference is almost constant at $-180°$ for all frequencies. As power division ratio increases, the deviation of phase difference from 180° increases.

3.4.6 Theoretical Results

The BTU power divider with arbitrary power division is designed at 2 GHz for power division ratio $k^2 = 2$. Z_3 is taken as 50 Ω. From the design equations (3.106)-(3.110), design parameters are obtained as: $Z_1 = 61.27\ \Omega$, $Z_2 = 43.28\ \Omega$, $Z_4 = 61.21\ \Omega$, $Z_5 = 86.65\ \Omega$, $R = 50\ \Omega$. Theoretical results of the proposed power divider are shown in Figs. 3.33-3.34.

Fig. 3.33(a) shows the return losses of unbalanced ports and isolation between output ports. At the center frequency, $|S_{ss11}|$, $|S_{ss13}|$ and $|S_{ss33}|$ are -56 dB, -50 dB and -52 dB, respectively. Fig. 3.33(b) shows differential return loss of balanced port, common-mode reflection of the balanced port and differential to common-mode conversion. At the center frequency, $|S_{ddAA}|$, $|S_{ccAA}|$ and $|S_{cdAA}|$ are -63 dB, 0 dB and -51 dB, respectively.

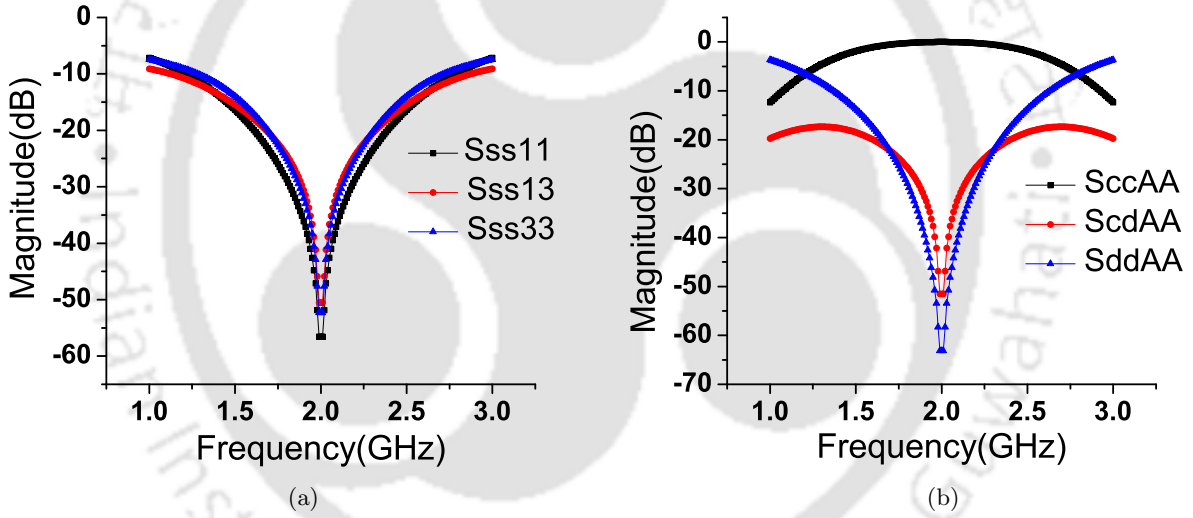


Figure 3.33: (a) Theoretical results of $|S_{ss11}|$, $|S_{ss13}|$ and $|S_{ss33}|$. (b) Theoretical results of $|S_{ddAA}|$, $|S_{ccAA}|$ and $|S_{cdAA}|$.

Fig. 3.34(a) shows the differential-mode transmission coefficient and common-mode suppression from balanced port to unbalanced ports. At the center frequency, $|S_{sd1A}|$, $|S_{sd3A}|$, $|S_{sc1A}|$ and $|S_{sc3A}|$ are -4.8 dB, -1.8 dB, -46 dB and -43 dB, respectively. Fig. 3.34(b) shows the phase difference ($Ang(S_{sd1A}/S_{sd3A})$) between two output signals. This shows out-of-phase characteristic of the power divider.

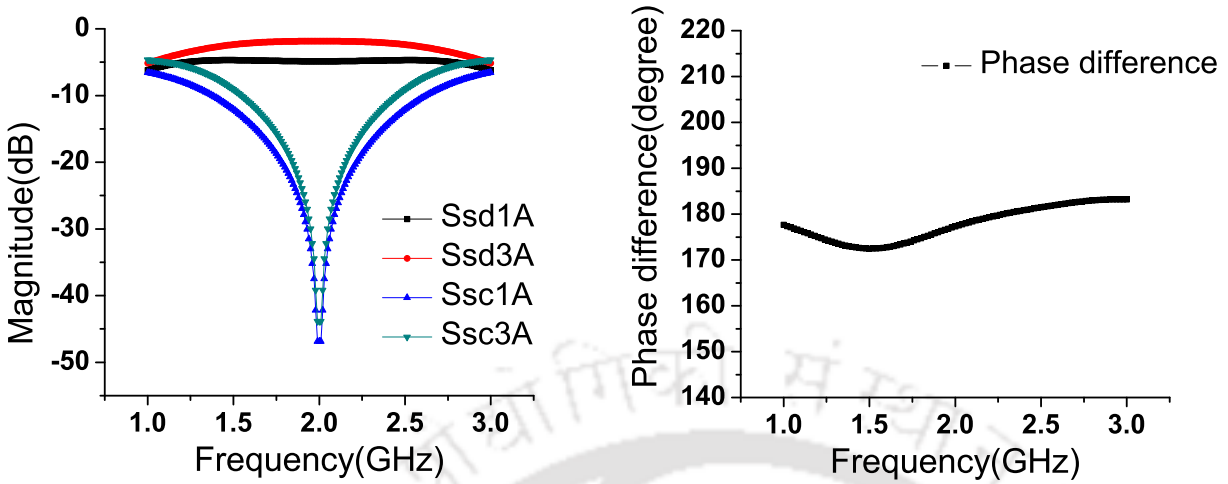


Figure 3.34: (a) Theoretical result of $|S_{sd1A}|$, $|S_{sd3A}|$, $|S_{sc1A}|$ and $|S_{sc3A}|$. (b) Theoretical result of unwrapped phase difference.

3.4.7 Simulation and Measured Results

Simulation is carried by HFSS from Ansys Inc. The fabricated prototype of BTU power divider with power division ratio $k^2 = 2$ is shown in Fig. 3.35. Fabrication is done on FR-4 substrate having $\epsilon_r = 4.4$ and $h = 1.6\ mm$.

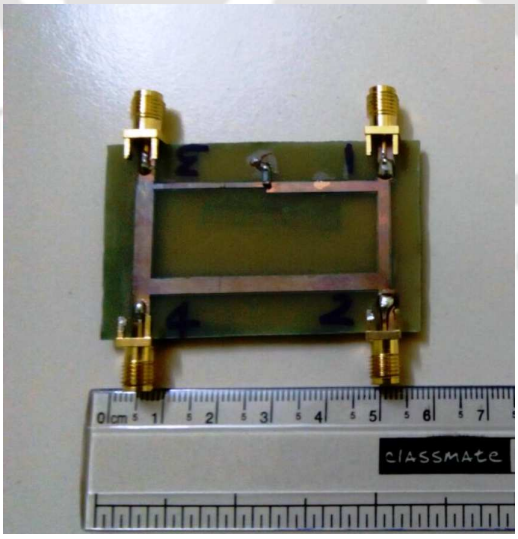
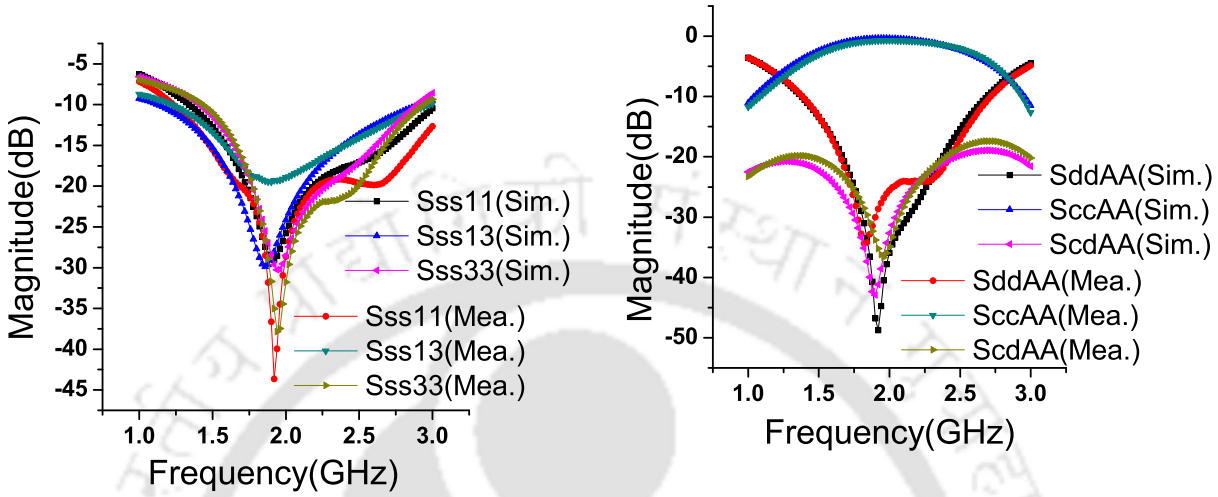


Figure 3.35: Fabricated prototype of power divider for power division ratio $k^2 = 2$.

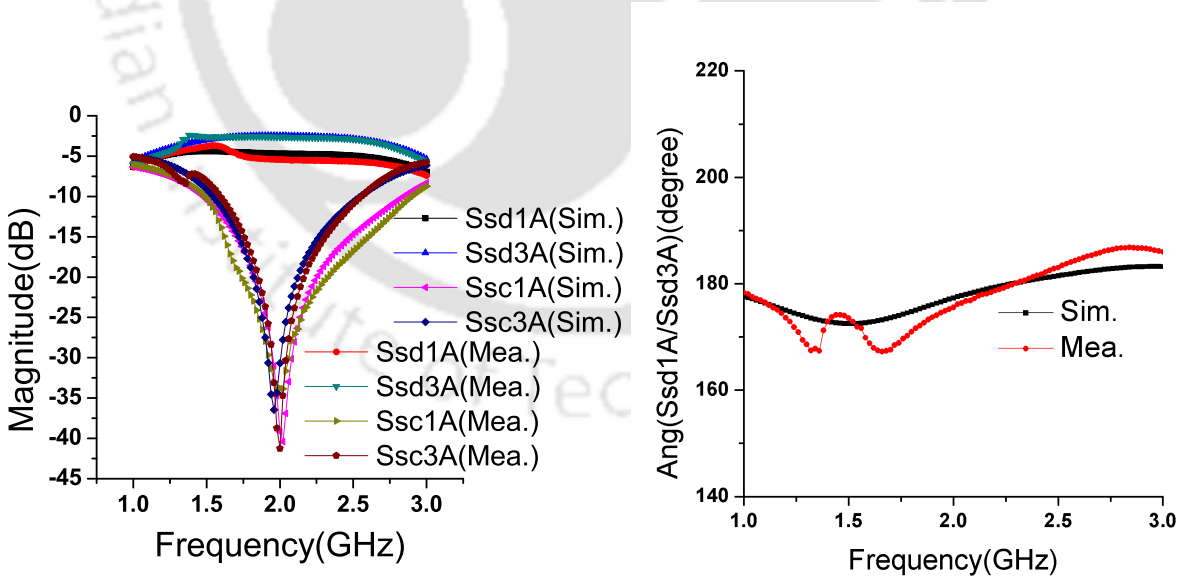
The measurement is done using a two port Rohde & Schwarz ZVA24 vector network analyzer.

Single-ended S parameters measured directly by VNA and (3.9)-(3.16) are used to find mixed-mode S parameters from single-ended scattering parameters. The comparisons of simulated and measured results are shown in Figs. 3.36-3.37.



(a) (b)

Figure 3.36: (a) Comparison of unbalanced port S parameters. (b) Comparison of balanced port return loss, common-mode reflection and mode conversion.



(a) (b)

Figure 3.37: (a) Comparison of differential-mode transmission and CMS to unbalanced ports. (b) Comparison of unwrapped phase difference.

In Fig. 3.36(a), return losses of two unbalanced output ports are better than 20 dB over the frequency range from 1.78 to 2.20 GHz. Isolation between two unbalanced output ports is better than 15 dB over the band 1.60 to 2.40 GHz. In Fig. 3.36(b), differential return loss is better than 20 dB over the frequency range from 1.66 to 2.42 GHz, equivalent to 38% fractional bandwidth. Common-mode reflection is better than 1 dB over the band 1.78 to 2.26 GHz. Mode conversion of balanced port is better than 15 dB over the entire frequency range of simulation and measurement, i.e. from 1 to 3 GHz. In Fig. 3.37(a), common-mode suppression to unbalanced ports is better than 20 dB over 1.86 to 2.16 GHz band. Difference between $|S_{sd3A}|$ and $|S_{sd1A}|$ is almost 3 dB around the center frequency. In Fig. 3.37(b), the unwrapped phase difference ($Ang(S_{sd1A}/S_{sd3A})$) shows excellent out-of-phase characteristic around the center frequency.

3.5 Gysel Type In-Phase Arbitrary Power Divider

The circuit diagram of the proposed in-phase power divider with arbitrary power division is shown in Fig. 3.38. The combination of ports 2 & 4 (also denoted as port A) is the input balanced port and two unbalanced ports are ports 1 & 3, as shown in Fig. 3.38. The Fig. 3.38 shows that the circuit consists of five transmission lines of characteristic impedances Z_1, Z_2, Z_3, Z_4 and Z_5 of electrical lengths π, $\pi/2$, $3\pi/2$, $\pi/2$ and $3\pi/2$, respectively. The isolation resistor R is connected with the ground, as shown in Fig. 3.38.

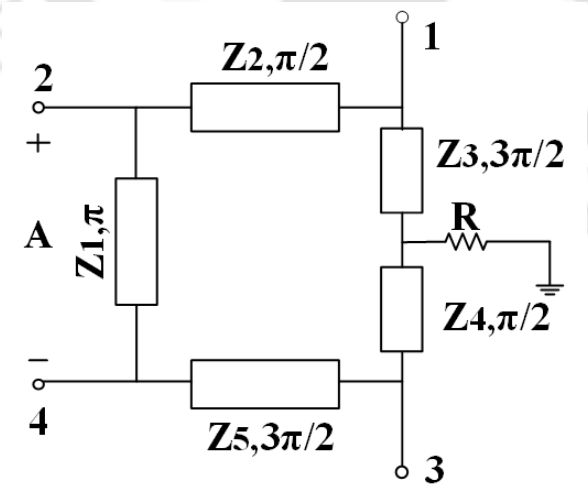


Figure 3.38: Circuit diagram of the proposed in-phase power divider with arbitrary power division.

3.5.1 Analysis of Power Transmission from Port A to Ports 1 and 3

For the ideal scenario, when port A is excited, power should be divided into ports 1 & 3. No power should be dissipated in isolation resistor [16, 20] and no power should be reflected from port A.

When no power is dissipated in resistor R, the ground point shifts to the other end of the resistor. Equivalent circuit of the proposed power divider under this condition is shown in Fig. 3.39.

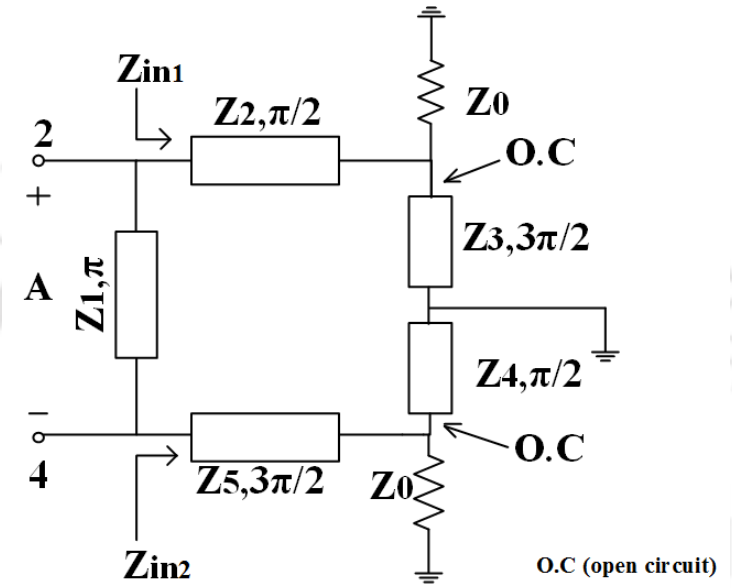


Figure 3.39: Equivalent circuit for power transmission from port A to ports 1 & 3.

As shown in Fig. 3.39, Z_{in1} and Z_{in2} are obtained as:

$$Z_{in1} = Z_2^2/Z_0,\ Z_{in2} = Z_5^2/Z_0 \tag{3.111}$$

Let the power is divided from port A to ports 1 & 3 in a power division ratio $1 : k^2$. Therefore, relationship between Z_{in1} and Z_{in2} can be written as:

$$Z_{in1} = k^2 Z_{in2} \tag{3.112}$$

Using (3.111) and (3.112), Z_2 and Z_5 are related as:

$$Z_2 = kZ_5 \tag{3.113}$$

For the circuit shown in Fig. 3.39, $[ABCD]$ matrix between ports 2 & 4 can be written as:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{24} = \begin{bmatrix} 1 & 0 \\ \frac{1}{Z_{in1}} & 1 \end{bmatrix} \begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{Z_{in2}} & 1 \end{bmatrix} \tag{3.114}$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{24} = \begin{bmatrix} -1 & 0 \\ -\frac{Z_0}{Z_2^2} - \frac{Z_0}{Z_5^2} & -1 \end{bmatrix} \tag{3.115}$$

The $[S]$ matrix parameters equivalent to $[ABCD]_{24}$ of (3.115) are derived and given in (3.116)-(3.118).

$$S_{22} = -\frac{Z_0^2(Z_5^2 + Z_2^2)}{Z_0^2(Z_5^2 + Z_2^2) + 2Z_2^2Z_5^2} \tag{3.116}$$

$$S_{24} = S_{42} = -\frac{2Z_2^2Z_5^2}{Z_0^2(Z_5^2 + Z_2^2) + 2Z_2^2Z_5^2} \tag{3.117}$$

$$S_{44} = -\frac{Z_0^2(Z_5^2 + Z_2^2)}{Z_0^2(Z_5^2 + Z_2^2) + 2Z_2^2Z_5^2} \tag{3.118}$$

Under the condition that no power should be reflected from port A, port A should be matched.

$$S_{ddAA} = \frac{1}{2}(S_{22} - S_{24} - S_{42} + S_{44}) = 0 \tag{3.119}$$

where, S_{ddAA} is the differential reflection coefficient of port A.

Using (3.113) and (3.116)-(3.119), Z_2 and Z_5 are obtained as:

$$Z_2 = Z_0\sqrt{\frac{1+k^2}{2}} \tag{3.120}$$

$$Z_5 = \frac{Z_0}{k}\sqrt{\frac{1+k^2}{2}} \tag{3.121}$$

3.5.2 Analysis of Isolation between Two Output Ports

For this analysis, when port 1 is excited, no power should flow to port 3. This happens when the voltage at port 3 is zero [16, 20]. Under this condition, equivalent circuit diagram of the proposed power divider is shown in Fig. 3.40. As shown in Fig. 3.40, Z_Y is obtained as:

$$Z_Y = Z_0 \tag{3.122}$$

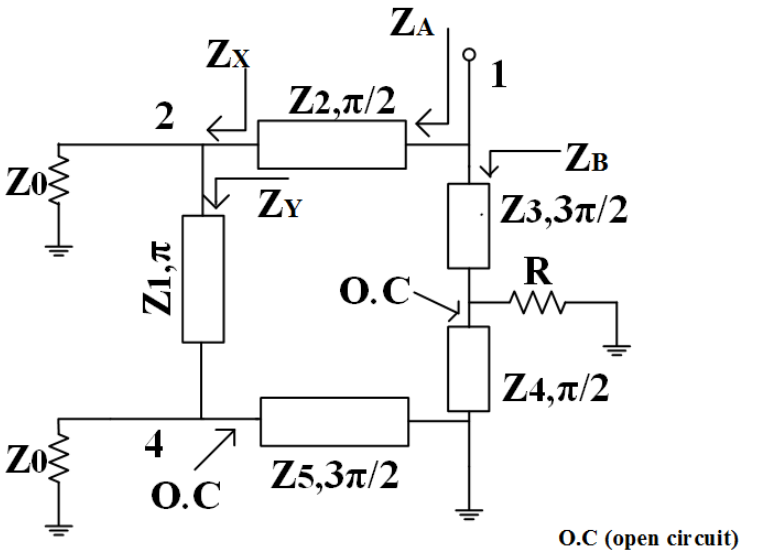


Figure 3.40: Equivalent circuit diagram of proposed PD when port 1 is excited.

From Fig. 3.40, Z_X is obtained as:

$$Z_X = Z_0 || Z_Y = \frac{Z_0}{2} \tag{3.123}$$

From Fig. 3.40, Z_A and Z_B are obtained as:

$$Z_A = \frac{Z_2^2}{Z_X} = \frac{2Z_2^2}{Z_0},\ Z_B = \frac{Z_3^2}{R} \tag{3.124}$$

For port 1 to be matched, port impedance Z_0 should be equal to the parallel combination of Z_A and Z_B.

$$\frac{Z_0}{2Z_2^2} + \frac{R}{Z_3^2} = \frac{1}{Z_0} \tag{3.125}$$

If Isolation resistor R is assumed to be equal to port impedance Z_0, then from (3.125), Z_3 is obtained as:

$$Z_3 = \frac{Z_0}{\sqrt{1 - \frac{Z_0^2}{2Z_2^2}}} \tag{3.126}$$

Similarly, if port 3 is excited no power should flow to port 1. By doing the same steps Z_4 can be

obtained and given as:

$$Z_4 = \frac{Z_0}{\sqrt{1 - \frac{Z_0^2}{2Z_5^2}}} \tag{3.127}$$

Equations (3.120), (3.121), (3.126) and (3.127) are the design equations of the proposed power divider. Z_1 and R are independent variables.

Short circuited parallel coupled lines described in section 3.3.5 are used to implement transmission lines of electrical length $3\pi/2$ in this power divider.

3.5.3 Theoretical Results

The arbitrary in-phase power divider is designed at 2 GHz for power division ratio $k^2 = 2$. Z_1 and R are taken as 50 Ω. From the design equations, design parameters are obtained as: $Z_2 = 61.23$ Ω, $Z_3 = 61.24$ Ω, $Z_4 = 86.60$ Ω, $Z_5 = 43.30$ Ω.

Theoretical results are shown in Figs. 3.41-3.42. Fig. 3.41(a) shows the return losses of unbalanced ports and isolation between output ports. At the center frequency, $|S_{ss11}|$, $|S_{ss13}|$ and $|S_{ss33}|$ are -72 dB, -81 dB and -66 dB, respectively. Fig. 3.41(b) shows the differential return loss of balanced port, common-mode reflection of the balanced port and differential to common-mode conversion. At the center frequency, balanced port is perfectly matched, common-mode reflection is 0 dB and no mode conversion between differential and common-mode.

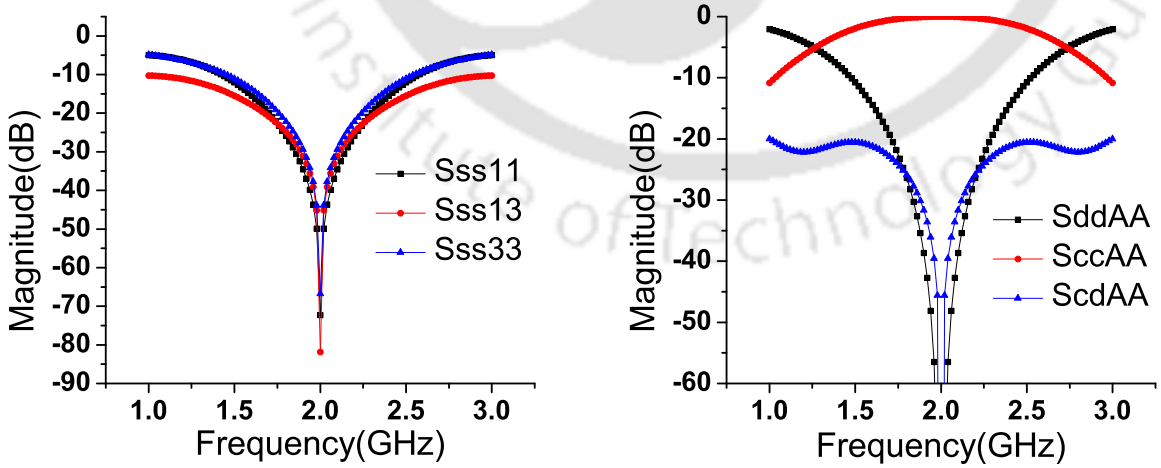


Figure 3.41: (a) Theoretical results of $|S_{ss11}|$, $|S_{ss13}|$ and $|S_{ss33}|$. (b) Theoretical results of $|S_{ddAA}|$, $|S_{ccAA}|$ and $|S_{cdAA}|$.

Fig. 3.42(a) shows the differential-mode transmission coefficient and common-mode suppression from balanced port to unbalanced ports. At the center frequency, $|S_{sd1A}|$, $|S_{sd3A}|$ are -4.8 dB, -1.8 dB, respectively. Results of $|S_{sc1A}|$ and $|S_{sc3A}|$ show that common-modes are perfectly suppressed. Fig. 3.42(b) shows the phase difference ($Ang(S_{sd1A}/S_{sd3A})$) between two output signals. This shows in-phase characteristic of the power divider.

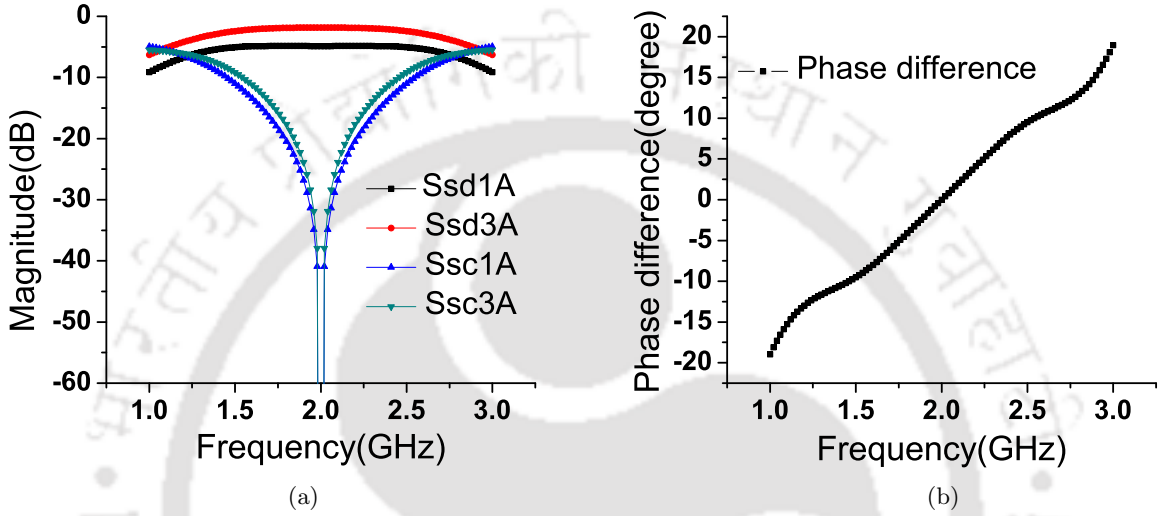
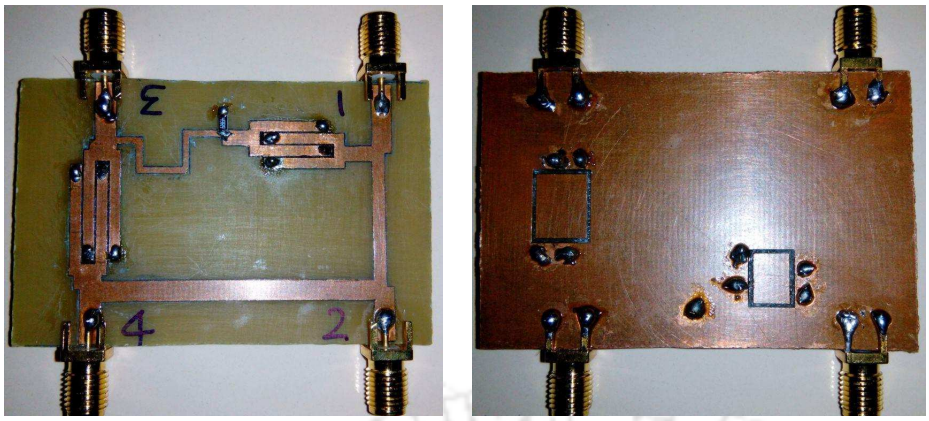


Figure 3.42: (a) Theoretical results of $|S_{sd1A}|$, $|S_{sd3A}|$, $|S_{sc1A}|$ and $|S_{sc3A}|$. (b) Theoretical result of phase difference.

3.5.4 Simulation and Measured Results

The fabricated prototype of the proposed in-phase power divider with power division ratio $k^2 = 2$ is shown in Fig. 3.43. FR-4 substrate of $\epsilon_r = 4.4$ and substrate thickness $h = 1.6\ mm$ is used for fabrication. Fig. 3.43(a) and Fig. 3.43(b) show the top layer and the bottom layer of the fabricated prototype of in-phase power divider, respectively.

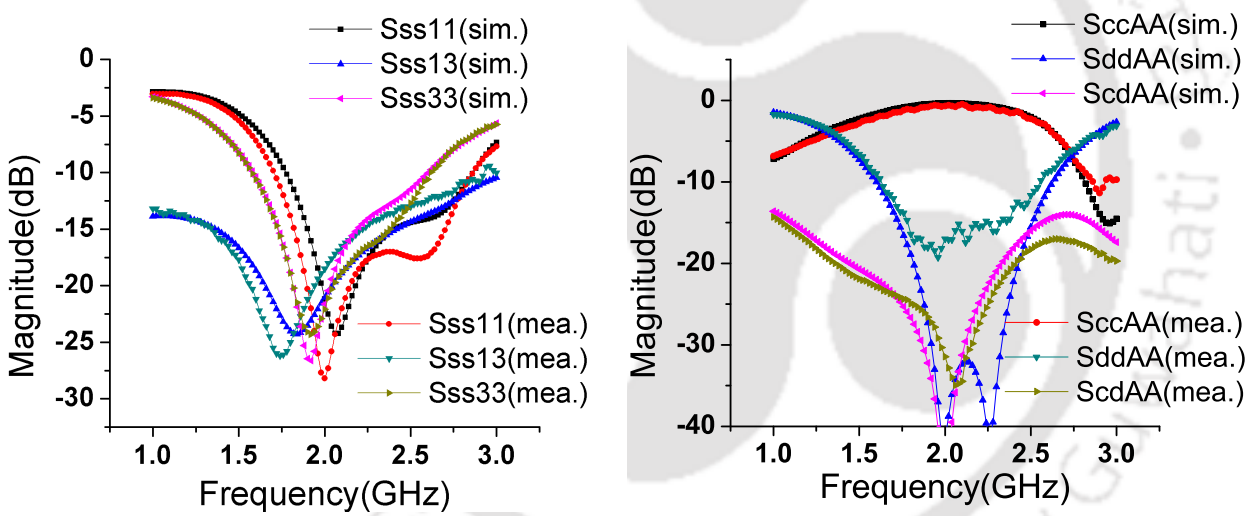
Comparisons of simulated and measured results are shown in Figs. 3.44-3.45. As shown in Fig. 3.44(a), measured $|S_{ss11}|$, $|S_{ss33}|$ (return losses of unbalanced ports 1 & 3) and $|S_{ss13}|$ (isolation between unbalanced ports 1 & 3) are greater than 15 dB from 1.84 to 2.38 GHz and 1.36 to 2.22 GHz, respectively. As shown in Fig. 3.44(b), measured $|S_{ddAA}|$ (differential-mode return loss of port A) is greater than 15 dB from 1.80 to 2.30 GHz, measured $|S_{ccAA}|$ (common-mode reflection of port A) is less than 1 dB from 1.86 to 2.28 GHz and measured $|S_{cdAA}|$ (mode conversion of port A) is greater



(a) (b)

Figure 3.43: (a) Top layer of power divider. (b) Bottom layer of power divider.

than 25 dB from 1.82 to 2.24 GHz.

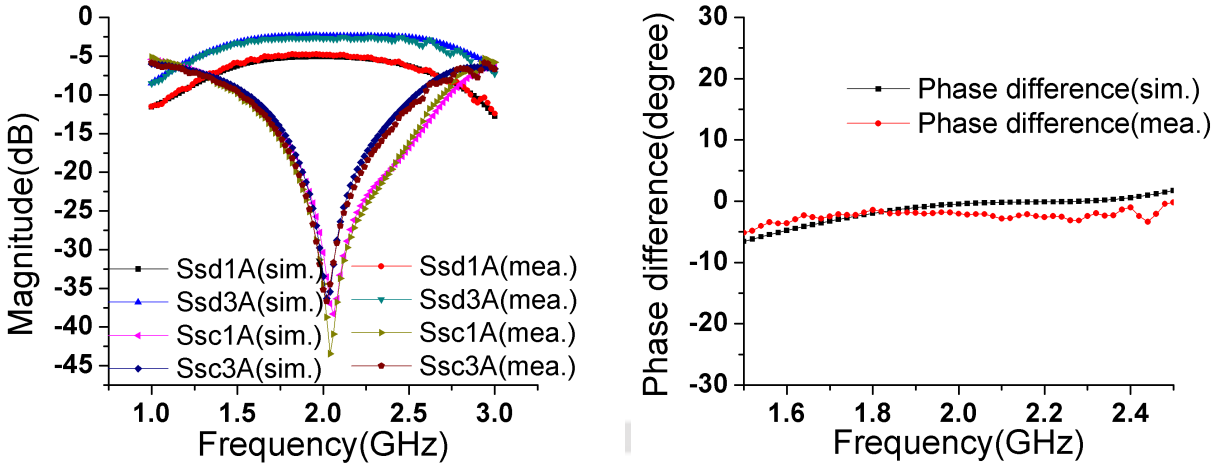


(a) (b)

Figure 3.44: (a) Comparison of unbalanced port S parameters. (b) Comparison of balanced port return loss, common-mode reflection and mode conversion.

In Fig. 3.45(a), measured $|S_{sc1A}|$, $|S_{sc3A}|$ (CMS to unbalanced ports 1 & 3) are greater than 20 dB from 1.88 to 2.22 GHz and $|S_{sd1A}|$, $|S_{sd3A}|$ (differential-mode power division) show that power is divided in power division ratio (1:2). Phase difference ($Ang(S_{sd1A}/S_{sd3A})$) between two unbalanced port signals is shown in Fig. 3.45(b). This shows the in-phase characteristic of the power divider.

The following parameters have been considered to obtain bandwidth of the in-phase power divider: (i) Less than 10° phase variation from in-phase characteristic (ii) $|S_{ccAA}|$ is less than 1.5 dB (iii) All



(a) (b)

Figure 3.45: (a) Comparison of differential-mode transmission and CMS to unbalanced ports. (b) Comparison of phase difference.

other S parameters ($|S_{ss11}|$, $|S_{ss13}|$, $|S_{ss33}|$, $|S_{ddAA}|$, $|S_{cdAA}|$, $|S_{sc1A}|$, $|S_{sc3A}|$) are greater than 10 dB. After including all the parameters fractional bandwidth is 34% (from 1.72 to 2.4 GHz).

Table 3.1: Comparison of proposed BTU power dividers with previous reported works.

Ref.	Type	Power Division	Phase	Bandwidth
[87]	Wilkinson	Equal	In-phase	25%
[82]	Gysel	Equal	Out-of-phase	37.2%
[81]	Gysel	Equal	Out-of-phase	71.5% (4 dB bandwidth)
PD in section 3.1	Gysel	Equal	Out-of-phase	41%
PD in section 3.2	Wilkinson	Equal	Out-of-phase	45% (15 dB return loss)
PD in section 3.3	Gysel	Equal	In-phase	20%
PD in section 3.4	Gysel	Arbitrary (Prototype for 1:2)	Out-of-phase	38% (20 dB return loss)
PD in section 3.5	Gysel	Arbitrary (Prototype for 1:2)	In-phase	34%

3.6 Conclusion

In this chapter, several types of BTU power dividers are proposed. Comparison of BTU power dividers with the reported power dividers are presented in Table 3.1. Gysel type out-of-phase and in-phase power divider for equal power division and for arbitrary power division are analyzed and designed. One Wilkinson type out-of-phase power divider is also designed. Complete theoretical analysis is presented to obtain design equations for each type of power divider. To validate design equations, all power dividers are fabricated and measurement has been performed. Simulation and measured results of all the power dividers are in good agreement.

4

Unbalanced-to-Balanced Power Divider

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In this chapter, two Gysel type UTB power dividers are proposed. First one is an UTB equal power divider and the second one is an UTB power divider with arbitrary power division. The requirements of mixed-mode parameters for the UTB power dividers are explained in this chapter. Standard 5×5 scattering matrix for a five-port UTB power divider is derived from mixed-mode scattering matrix. Design equations are derived analytically. Two prototypes are fabricated and measurement is performed to verify theoretical and simulation results.

4.1 Gysel Type Equal Power Divider

4.1.1 Circuit Model

Circuit model of the proposed equal power divider is shown in Fig. 4.1. Port 1 represents the input unbalanced port, port A (combination of ports 2 & 3) and port B (combination of ports 4 & 5) represent the balanced output ports of the proposed power divider, as shown in Fig. 4.1. In the circuit model, the two transmission lines of electrical length $\pi/2$ and $3\pi/2$, have characteristic impedance Z_1. There are two pairs of transmission lines of characteristic impedance Z_3 and electrical length $\pi/2$ and one pair of transmission lines of characteristic impedance Z_2 and electrical length π. Two isolation resistors, each marked as R, provide the isolation between ports A & B, are connected with the ground.

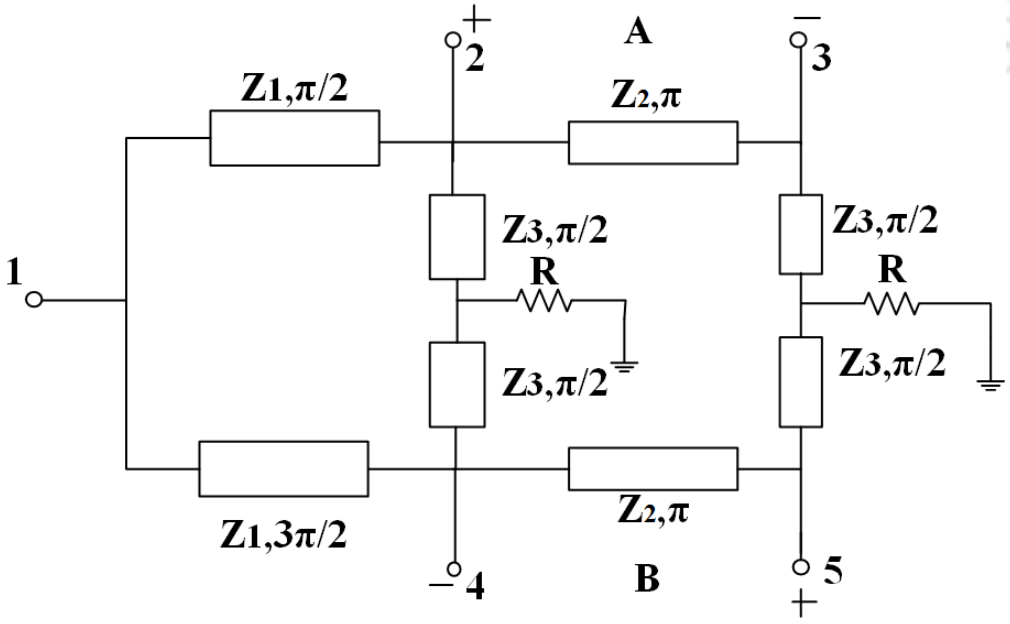


Figure 4.1: Circuit model of the proposed equal power divider.

At the input end of the circuit shown in Fig. 4.1, two transmission lines of lengths $\pi/2$ and $3\pi/2$ are used. The phase difference of 180° between these two transmission lines is required to maintain the phase characteristic of output signals.

4.1.2 Standard Scattering Matrix Realization

To completely analyze the UTB power divider, it has to be characterized in-terms of its mixed-mode scattering parameters. The circuit diagram of an UTB equal power divider is shown in Fig. 4.1, requirements of mixed-mode parameters for this power divider are summarized given below.

(i) Reflection coefficient of unbalanced port and coupling between balanced ports are zero.

$$|S_{ss11}| = |S_{ddAB}| = 0 \tag{4.1}$$

(ii) Differential-mode reflection coefficient and differential to common-mode conversion coefficient should be zero for balanced ports A and B.

$$|S_{ddAA}| = |S_{cdAA}| = |S_{ddBB}| = |S_{cdBB}| = |S_{cdAB}| = 0 \tag{4.2}$$

(iii) Common-mode reflection should be unity for balanced ports A and B.

$$|S_{ccAA}| = |S_{ccBB}| = 1 \tag{4.3}$$

(iv) Common-mode suppression should be zero.

$$|S_{csA1}| = |S_{csB1}| = |S_{sc1A}| = |S_{sc1B}| = |S_{ccAB}| = |S_{ccBA}| = 0 \tag{4.4}$$

(v) Power should be divided equally from unbalanced port 1 to balanced ports A and B.

$$|S_{dsA1}| = |S_{sd1A}| = \frac{1}{\sqrt{2}} \tag{4.5}$$

$$|S_{dsB1}| = |S_{sd1B}| = \frac{1}{\sqrt{2}} \tag{4.6}$$

Based on (4.1)-(4.6), mixed-mode scattering matrix is derived and given in (4.7).

$$[S^{mm}] = \begin{bmatrix} 0 & \frac{1}{\sqrt{2}}e^{j\theta_1} & \frac{1}{\sqrt{2}}e^{j\theta_2} & 0 & 0 \\ \frac{1}{\sqrt{2}}e^{j\theta_1} & 0 & 0 & 0 & 0 \\ \frac{1}{\sqrt{2}}e^{j\theta_2} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & e^{j\theta_3} & 0 \\ 0 & 0 & 0 & 0 & e^{j\theta_4} \end{bmatrix} \tag{4.7}$$

where, $\theta_1, \theta_2, \theta_3, \theta_4$ represent the angle of different mixed-mode S parameters. For an UTB power divider, $\theta_1 = \theta_2 = -\pi/2$ and $\theta_3 = \theta_4 = -\pi$.

Following mathematical transformations are used to convert mixed-mode scattering parameters into standard scattering parameters of the proposed power divider [93].

$$S_{ddAA} = \frac{1}{2}(S_{22} - S_{23} - S_{32} + S_{33}) \tag{4.8}$$

$$S_{ddBB} = \frac{1}{2}(S_{55} - S_{54} - S_{45} + S_{44}) \tag{4.9}$$

$$S_{ddAB} = \frac{1}{2}(S_{25} - S_{24} - S_{35} + S_{34}) \tag{4.10}$$

$$S_{cdAA} = \frac{1}{2}(S_{22} + S_{23} - S_{32} - S_{33}) \tag{4.11}$$

$$S_{cdBB} = \frac{1}{2}(S_{55} + S_{54} - S_{45} - S_{44}) \tag{4.12}$$

$$S_{cdAB} = \frac{1}{2}(S_{25} + S_{24} - S_{35} - S_{34}) \tag{4.13}$$

$$S_{ccAA} = \frac{1}{2}(S_{22} + S_{23} + S_{32} + S_{33}) \tag{4.14}$$

$$S_{ccBB} = \frac{1}{2}(S_{55} + S_{54} + S_{45} + S_{44}) \tag{4.15}$$

$$S_{ccAB} = \frac{1}{2}(S_{25} + S_{24} + S_{35} + S_{34}) \tag{4.16}$$

$$S_{sd1A} = \frac{1}{\sqrt{2}}(S_{21} - S_{31}) \tag{4.17}$$

$$S_{sd1B} = \frac{1}{\sqrt{2}}(S_{51} - S_{41}) \tag{4.18}$$

$$S_{sc1A} = \frac{1}{\sqrt{2}}(S_{21} + S_{31}) \tag{4.19}$$

$$S_{sc1B} = \frac{1}{\sqrt{2}}(S_{51} + S_{41}) \tag{4.20}$$

Using (4.7)-(4.20), standard S matrix $[S_{std}]$ is obtained and given in (4.21).

$$[S_{std}] = \begin{bmatrix} 0 & -j\frac{1}{2} & j\frac{1}{2} & j\frac{1}{2} & -j\frac{1}{2} \\ -j\frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} & 0 & 0 \\ j\frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} & 0 & 0 \\ j\frac{1}{2} & 0 & 0 & -\frac{1}{2} & -\frac{1}{2} \\ -j\frac{1}{2} & 0 & 0 & -\frac{1}{2} & -\frac{1}{2} \end{bmatrix} \tag{4.21}$$

4.1.3 Analysis of Power Transmission from Unbalanced Port to Balanced Ports

Under this condition, power should get equally divided from unbalanced input port into two balanced output ports, no power should be dissipated in the two isolation resistors [16,20]. This means that ground point effectively moves to other ends of the resistors. Using impedance transformation property of quarter-wave transmission lines of characteristic impedance Z_3, the other ends of these lines become open circuited. The equivalent circuit model for this analysis is shown in Fig. 4.2.

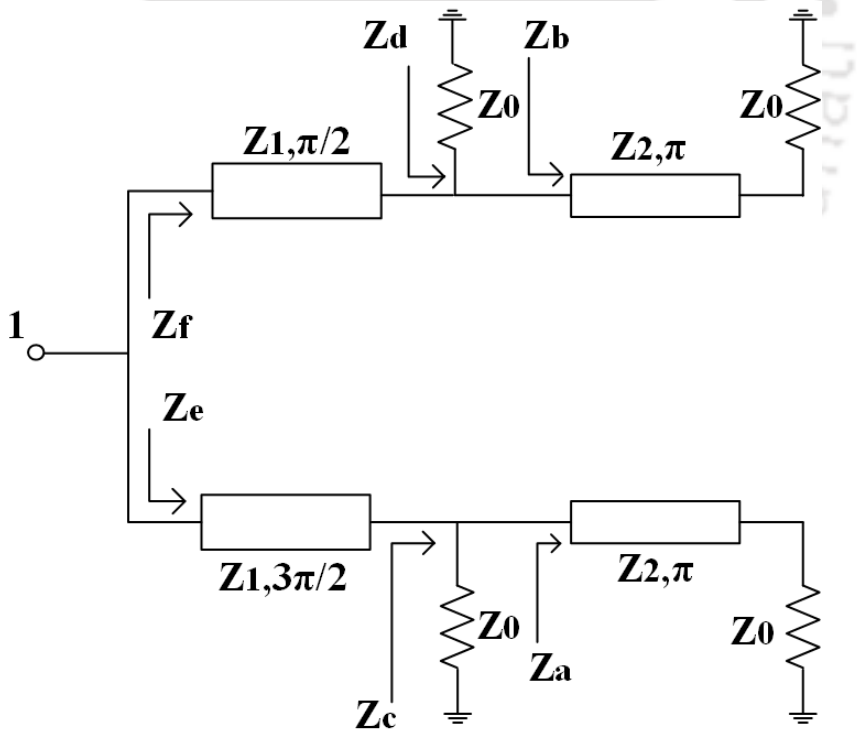


Figure 4.2: Equivalent circuit for power transmission from unbalanced input port to balanced output ports.

From Fig. 4.2, Z_a and Z_b are obtained as:

$$Z_a = Z_b = Z_0 \tag{4.22}$$

As seen from Fig. 4.2,

$$Z_c = Z_0 || Z_a \tag{4.23}$$

and

$$Z_d = Z_0 || Z_b \tag{4.24}$$

Using (4.22)-(4.24), Z_c and Z_d are obtained as:

$$Z_c = Z_d = Z_0/2 \tag{4.25}$$

Z_e and Z_f are obtained using impedance transformation property of quarter wave transmission line of characteristic impedance Z_1. Z_e and Z_f are obtained as:

$$Z_e = \frac{Z_1^2}{Z_c},\ Z_f = \frac{Z_1^2}{Z_d} \tag{4.26}$$

Using (4.25) and (4.26), Z_e and Z_f are obtained as:

$$Z_e = Z_f = \frac{2Z_1^2}{Z_0} \tag{4.27}$$

The parallel combination of Z_e and Z_f is equal to Z_0 (port impedance of port 1).

$$Z_e || Z_f = Z_0 \tag{4.28}$$

Using (4.27) and (4.28), Z_1 is obtained and given in (4.29).

$$Z_1 = Z_0 \tag{4.29}$$

4.1.4 Analysis of Isolation between Two Balanced Output Ports

For isolation analysis, when port A is exited, then no power should flow to port B. This happens when the voltage at ports 4 & 5 (combined as port B) is zero (as in [16, 20] for single-ended power divider). Therefore, one end of the pair of transmission lines of characteristic impedance Z_3 and one of the transmission line of characteristic impedance Z_1 are connected to ground. Then, using quarter-wave transformer property, the other ends of these transmission lines are open circuited. The equivalent circuit model for this analysis is shown in Fig. 4.3.

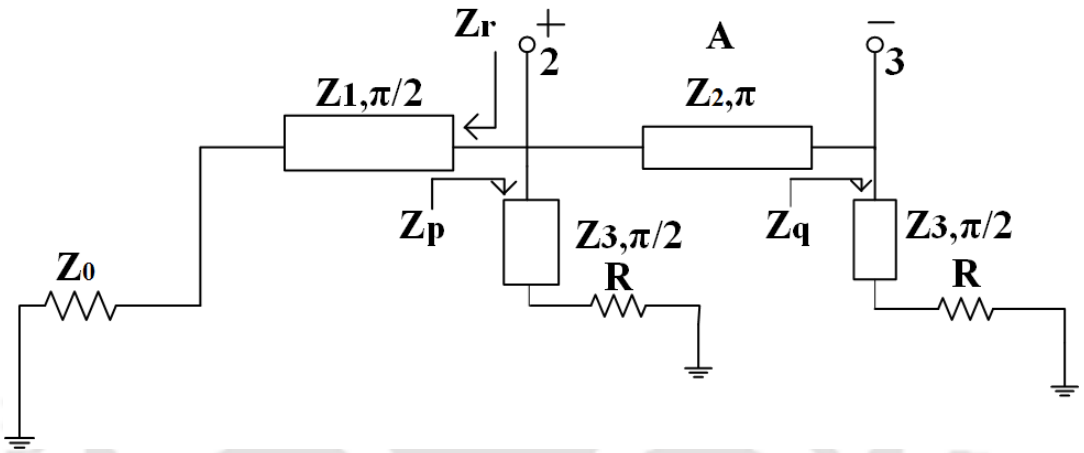


Figure 4.3: Isolation analysis between two output ports.

From Fig. 4.3, Z_p and Z_q are obtained using quarter wave transformer property of transmission line of characteristic impedance Z_3.

$$Z_p = Z_q = \frac{Z_3^2}{R} \tag{4.30}$$

From Fig. 4.3, Z_r is obtained as:

$$Z_r = \frac{Z_1^2}{Z_0} \tag{4.31}$$

Using (4.29) and (4.31), Z_r is obtained as:

$$Z_r = Z_0 \tag{4.32}$$

Let Z_t is the parallel combination of Z_r and Z_p. Using (4.30) and (4.32), Z_t is obtained as:

$$Z_t = Z_r || Z_p = \frac{Z_0 Z_3^2}{R Z_0 + Z_3^2} \tag{4.33}$$

Now, $[ABCD]_{23}$ matrix between ports 2 & 3 is obtained as:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{23} = \begin{bmatrix} 1 & 0 \\ \frac{RZ_0+Z_3^2}{Z_0Z_3^2} & 1 \end{bmatrix} \begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{R}{Z_3^2} & 1 \end{bmatrix} \tag{4.34}$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{23} = \begin{bmatrix} -1 & 0 \\ -\frac{1}{Z_0} - \frac{2R}{Z_3^2} & -1 \end{bmatrix} \tag{4.35}$$

$[S]_{23}$ can be obtained by matrix conversion of $[ABCD]_{23}$. The elements of matrix $[S]_{23}$ are derived and given in (4.36) and (4.37).

$$S_{22} = S_{33} = -\frac{Z_3^2 + 2RZ_0}{3Z_3^2 + 2RZ_0} \tag{4.36}$$

$$S_{23} = S_{32} = -\frac{2Z_3^2}{3Z_3^2 + 2RZ_0} \tag{4.37}$$

For port A (combination of ports 2 & 3) to be matched, differential reflection coefficient (S_{ddAA}) of port A should be zero.

$$S_{ddAA} = \frac{1}{2}(S_{22} - S_{23} - S_{32} + S_{33}) = 0 \tag{4.38}$$

Using (4.36)-(4.38), Z_3 is obtained as:

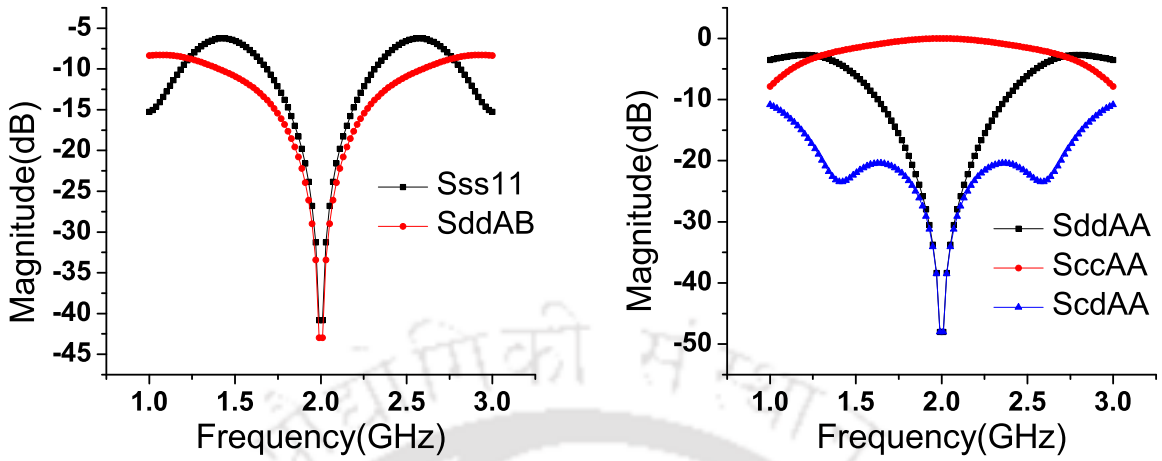
$$Z_3 = \sqrt{2RZ_0} \tag{4.39}$$

Further, R and Z_2 can be chosen independently.

4.1.5 Theoretical Results

The proposed Gysel type equal power divider is designed at 2 GHz. Both R and Z_2 are taken as 50 Ω. Using design equations (4.29) and (4.39), Z_1 and Z_3 are obtained as 50 Ω and 70.71 Ω, respectively. Theoretical results of the proposed power divider are shown in Figs. 4.4-4.6.

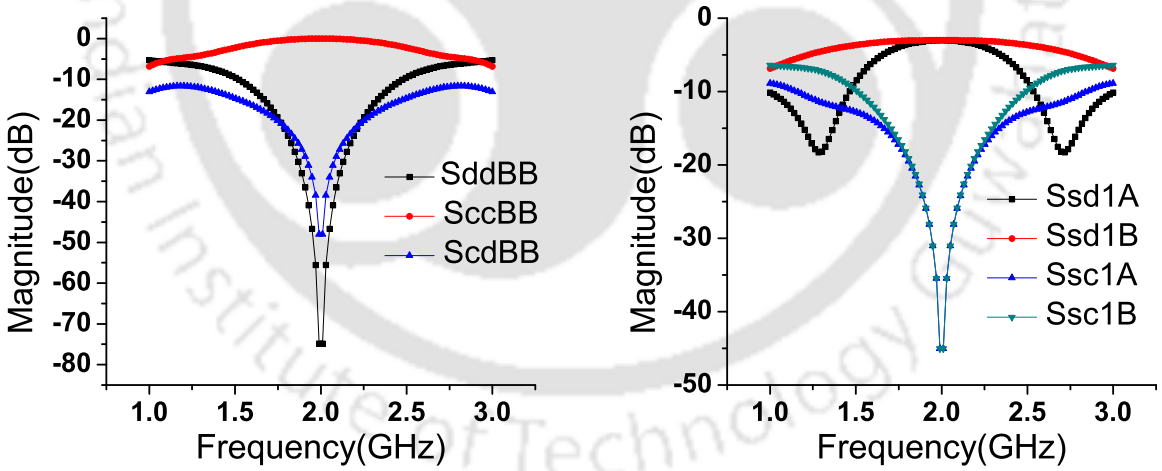
As shown in Fig. 4.4(a), theoretical return loss of unbalanced port and isolation between balanced ports are -40 dB and -42 dB at the center frequency, respectively. As shown in Fig. 4.4(b), theoretical results of $|S_{ddAA}|$, $|S_{ccAA}|$ and $|S_{cdAA}|$ are -48 dB, 0 dB and -48 dB at the center frequency, respectively. In Fig. 4.5(a), theoretical results of $|S_{ddBB}|$, $|S_{ccBB}|$ and $|S_{cdBB}|$ are -74 dB, 0 dB and -48 dB at the center frequency, respectively. In Fig. 4.5(b), theoretical results of $|S_{sd1A}|$, $|S_{sd1B}|$, $|S_{sc1A}|$ and $|S_{sc1B}|$



(a) (b)

Figure 4.4: (a) Theoretical results of $|S_{ss11}|$ and $|S_{ddAB}|$. (b) Theoretical results of $|S_{ddAA}|$, $|S_{ccAA}|$ and $|S_{cdAA}|$.

are -3 dB, -3 dB, -45 dB and -45 dB at the center frequency, respectively. Fig. 4.6 shows the theoretical



(a) (b)

Figure 4.5: (a) Theoretical results of $|S_{ddBB}|$, $|S_{ccBB}|$ and $|S_{cdBB}|$. (b) Theoretical results of $|S_{sd1A}|$, $|S_{sd1B}|$, $|S_{sc1A}|$ and $|S_{sc1B}|$.

result of phase difference. This shows the in-phase characteristic of the proposed power divider.

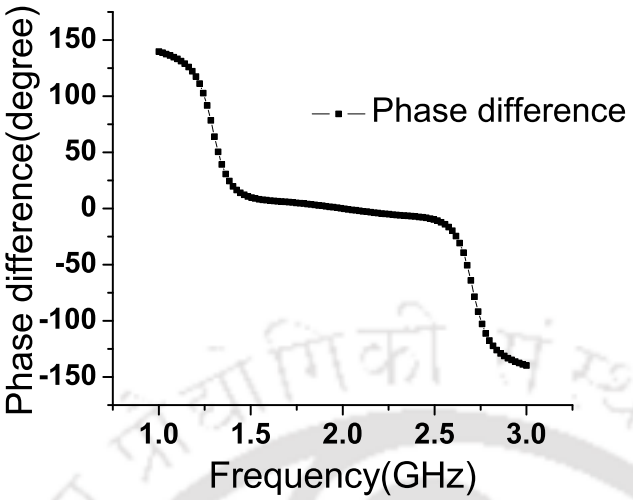


Figure 4.6: Theoretical result of phase difference.

4.1.6 Simulation and Measured Results

Simulation has been carried out using HFSS. Fig. 4.7 shows the fabricated prototype of the proposed power divider. FR-4 substrate of dielectric constant $\epsilon_r = 4.4$ and thickness $h = 1.6\ mm$ is used for fabrication. Two port VNA (vector network analyzer) is used for measurement. Single-ended

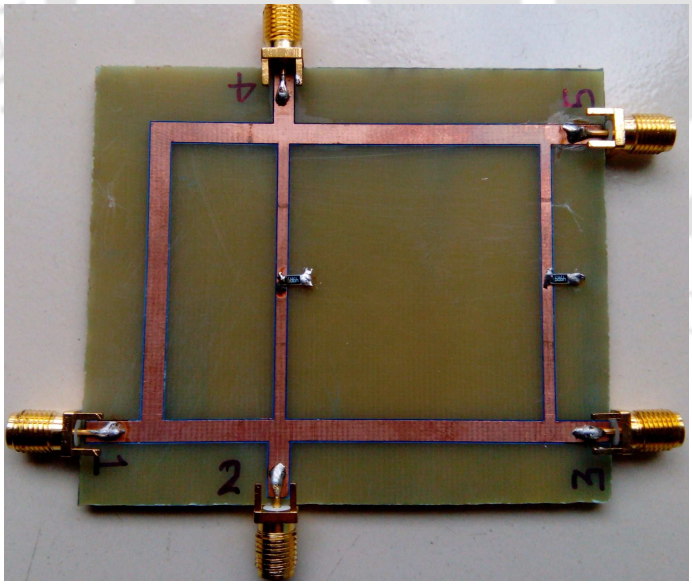


Figure 4.7: Fabricated prototype of proposed Gysel type equal power divider.

S parameters are measured directly from VNA while mathematical transformations given in (4.8)-(4.20) are used to obtain mixed-mode S parameters. Comparisons of simulated and measured results

are shown in Figs. 4.8-4.10.

Comparison of simulated and measured return loss of single-ended input port ($|S_{ss11}|$) and isolation ($|S_{ddAB}|$) between two balanced output ports are shown in Fig. 4.8(a). Measured $|S_{ss11}|$ is greater than 15 dB from 1.86 GHz to 2.18 GHz and measured $|S_{ddAA}|$ is greater than 20 dB from 1.82 GHz to 2.08 GHz. Comparison of common-mode reflection ($|S_{ccAA}|$), differential-mode return loss ($|S_{ddAA}|$) and differential to common-mode conversion ($|S_{cdAA}|$) of balanced port A are shown in Fig. 4.8(b). Measured $|S_{ccAA}|$ is less than 1 dB from 1.78 GHz to 2.28 GHz, measured $|S_{ddAA}|$ is greater than 10 dB from 1.66 GHz to 2.58 GHz and measured $|S_{cdAA}|$ is greater than 15 dB from 1.3 GHz to 2.96 GHz. Comparison of common-mode reflection ($|S_{ccBB}|$), differential-mode return loss ($|S_{ddBB}|$)

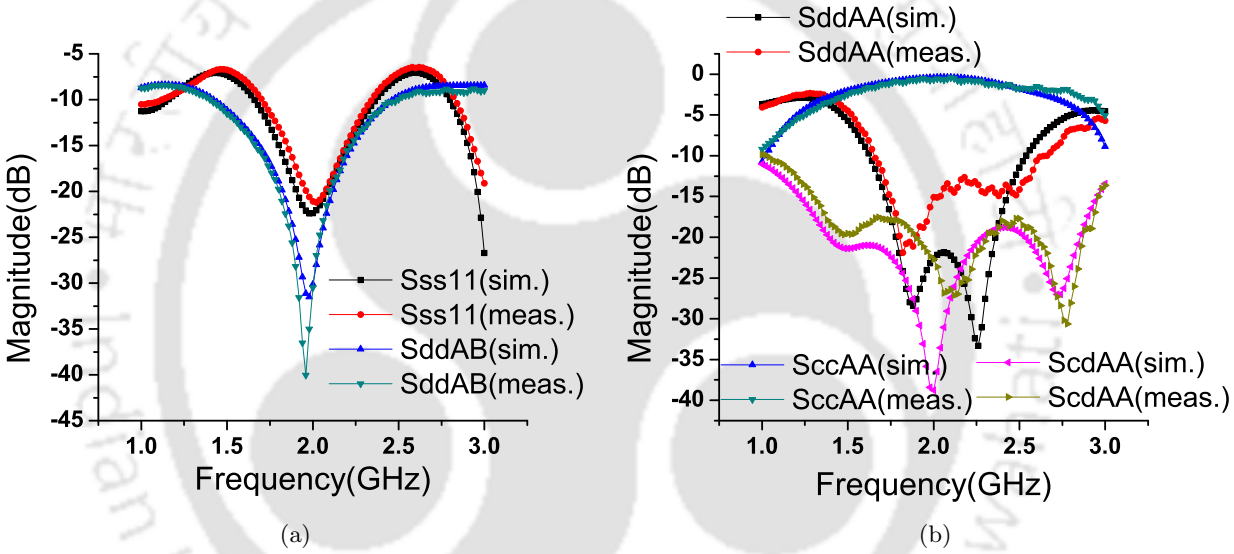
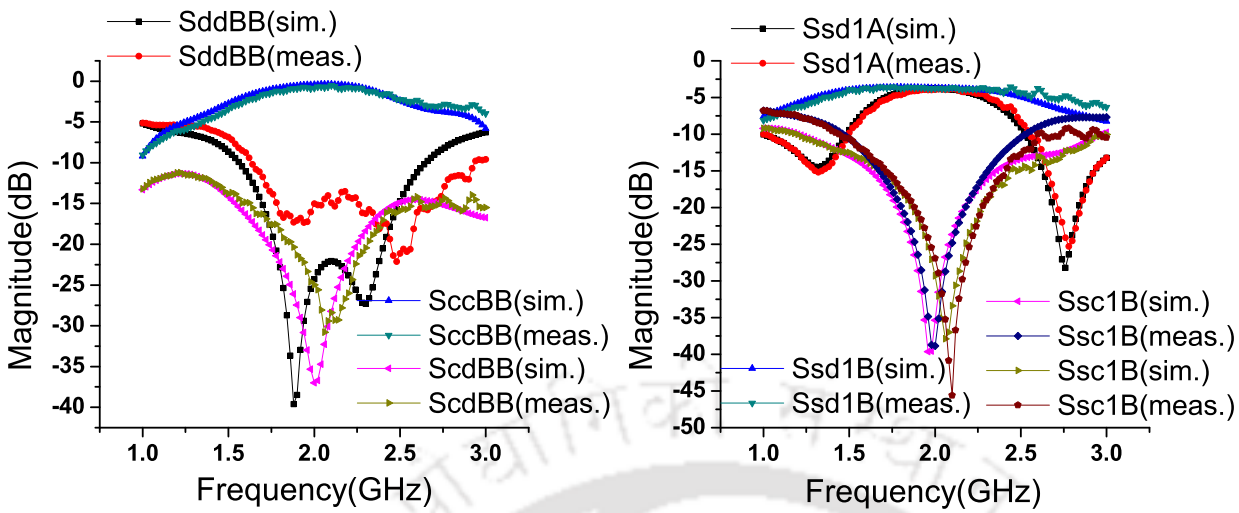


Figure 4.8: (a) Comparison of $|S_{ss11}|$ and $|S_{ddAB}|$. (b) Comparison of $|S_{ddAA}|$, $|S_{ccAA}|$ and $|S_{cdAA}|$.

and differential to common-mode conversion ($|S_{cdBB}|$) of balanced port B are shown in Fig. 4.9(a). Measured $|S_{ccBB}|$ is less than 1 dB from 1.86 GHz to 2.30 GHz, measured $|S_{ddBB}|$ is greater than 10 dB from 1.64 GHz to 2.92 GHz and measured $|S_{cdBB}|$ is greater than 15 dB from 1.64 GHz to 2.88 GHz. In Fig. 4.9(b), measured common-mode suppression to balanced ports ($|S_{sc1A}|$ and $|S_{sc1A}|$) is greater than 20 dB from 1.9 GHz to 2.26 GHz. Differential-mode power ($|S_{sd1A}|$ and $|S_{sd1B}|$) is equally divided at the design frequency. Comparison of simulated and measured phase difference ($Ang(S_{sd1A}/S_{sd1B})$) is shown in Fig. 4.10, which represent in-phase characteristic of the power divider.

The measured fractional bandwidth is 12% (from 1.90 GHz to 2.14 GHz). The conditions for calculating the fractional bandwidth are: (i) $|S_{sd1B}|$ and $|S_{sd1A}|$ are less than 4 dB (ii) $|S_{ccAA}|$ and



(a) (b)

Figure 4.9: (a) Comparison of $|S_{ddBB}|$, $|S_{ccBB}|$ and $|S_{cdBB}|$. (b) Comparison of $|S_{sd1A}|$, $|S_{sd1B}|$, $|S_{sc1A}|$ and $|S_{sc1B}|$.

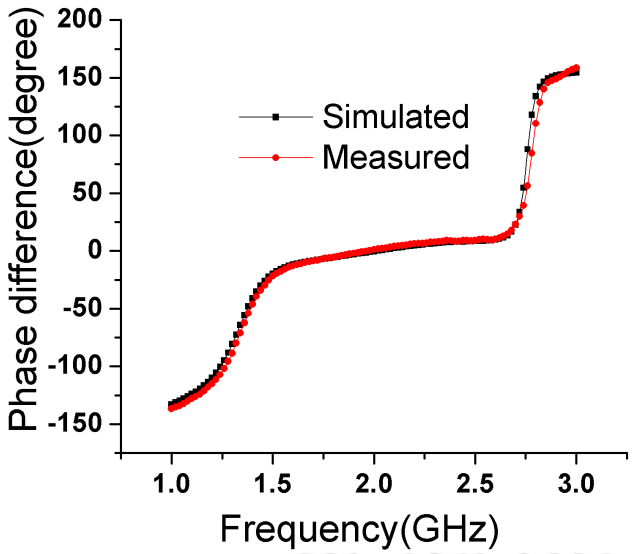


Figure 4.10: Comparison of phase difference.

$|S_{ccBB}|$ are less than 1 dB (iii) All other scattering parameters are greater than 10 dB.

4.2 Gysel Type Arbitrary Power Divider

4.2.1 Circuit Diagram

The circuit diagram of an UTB arbitrary power divider is shown in Fig. 4.11. Port 1 is the input unbalanced port, port A (combination of ports 2 & 3) and port B (combination of ports 4 & 5) are the balanced output ports of the proposed power divider. In the circuit diagram shown, there are two transmission lines of characteristic impedances Z_1 and Z_2, having electrical lengths $\pi/2$ and $3\pi/2$, respectively. There is one pair of transmission lines, having an electrical length $\pi/2$ and characteristic impedances Z_3 and Z_4. There is another pair of transmission lines of electrical length π having characteristic impedances Z_A and Z_B. As shown in Fig. 4.11, two isolation resistors (both marked as R) which provide isolation between ports A & B are connected with the ground.

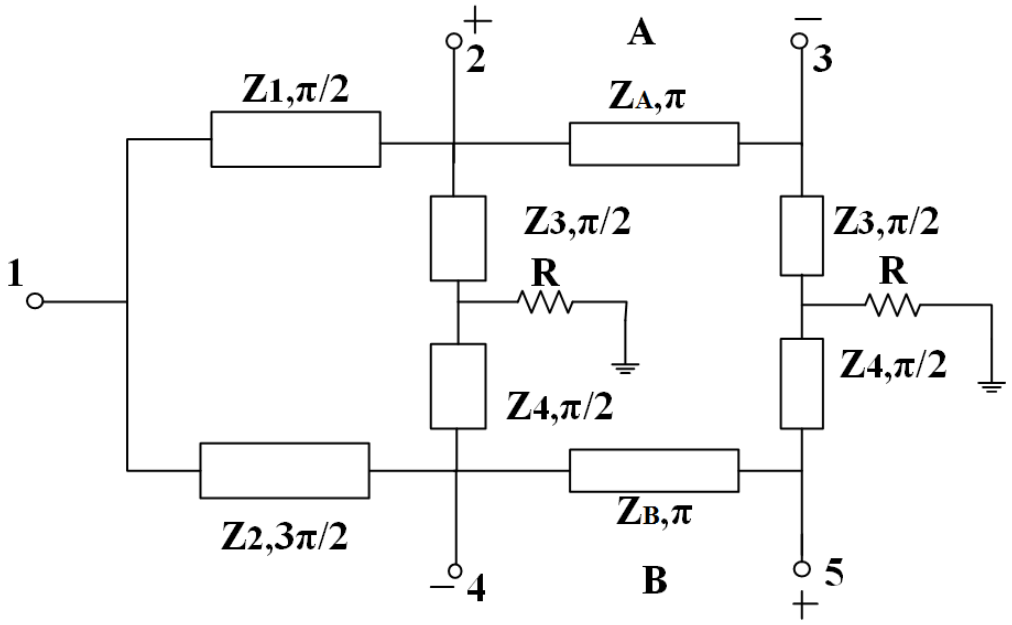


Figure 4.11: Circuit diagram of the proposed arbitrary power divider.

Again, at the input end of the circuit shown in Fig. 4.11, two transmission lines of lengths $\pi/2$ and $3\pi/2$ are used. The phase difference of 180° between these two transmission lines is required to maintain the phase characteristic of output signals.

4.2.2 Formulation of Standard Scattering Matrix

The proposed UTB power divider is defined by its mixed-mode S parameters. The mixed-mode scattering matrix is given as:

$$[S^{mm}] = \begin{bmatrix} S_{ss11} & S_{sd1A} & S_{sd1B} & S_{sc1A} & S_{sc1B} \\ S_{dsA1} & S_{ddAA} & S_{ddAB} & S_{dcAA} & S_{dcAB} \\ S_{dsB1} & S_{ddBA} & S_{ddBB} & S_{dcBA} & S_{dcBB} \\ S_{csA1} & S_{cdAA} & S_{cdAB} & S_{ccAA} & S_{ccAB} \\ S_{csB1} & S_{cdBA} & S_{cdBB} & S_{ccBA} & S_{ccBB} \end{bmatrix} \tag{4.40}$$

The requirements of an UTB power divider with arbitrary power division in-terms of mixed-mode parameters are given as:

(i) Reflection coefficient of unbalanced port and coupling between balanced ports are zero.

$$|S_{ss11}| = |S_{ddAB}| = 0 \tag{4.41}$$

(ii) Differential-mode reflection coefficient and differential to common-mode conversion coefficient should be zero for balanced ports A and B.

$$|S_{ddAA}| = |S_{cdAA}| = |S_{ddBB}| = |S_{cdBB}| = |S_{cdAB}| = 0 \tag{4.42}$$

(iii) Common-mode reflection should be unity for balanced ports A and B.

$$|S_{ccAA}| = |S_{ccBB}| = 1 \tag{4.43}$$

(iv) CMS should be zero.

$$|S_{csA1}| = |S_{csB1}| = |S_{sc1A}| = |S_{sc1B}| = |S_{ccAB}| = |S_{ccBA}| = 0 \tag{4.44}$$

(v) Power should be divided from unbalanced port 1 to balanced ports A and B in a specific ratio.

$$|S_{dsA1}| = |S_{sd1A}| = \alpha \tag{4.45}$$

$$|S_{dsB1}| = |S_{sd1B}| = \sqrt{1-\alpha^2} \tag{4.46}$$

where, α $(0 < \alpha < 1)$ is the transmission coefficient from port 1 to port A.

Based on (4.40)-(4.46), mixed-mode scattering matrix is obtained and given in (4.47).

$$[S^{mm}] = \begin{bmatrix} 0 & \alpha e^{j\theta_1} & \sqrt{1-\alpha^2}e^{j\theta_2} & 0 & 0 \\ \alpha e^{j\theta_1} & 0 & 0 & 0 & 0 \\ \sqrt{1-\alpha^2}e^{j\theta_2} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & e^{j\theta_3} & 0 \\ 0 & 0 & 0 & 0 & e^{j\theta_4} \end{bmatrix} \tag{4.47}$$

where, $\theta_1, \theta_2, \theta_3, \theta_4$ represent the angle of different mixed-mode S parameters. For an UTB power divider, $\theta_1 = \theta_2 = -\pi/2$ and $\theta_3 = \theta_4 = -\pi$. Let the power division ratio from port 1 to ports A and B is $1 : k^2$. Then from (4.47), α and k are related as: $\alpha = \frac{1}{\sqrt{1+k^2}}$. Using (4.8)-(4.20) and (4.47), standard S matrix $[S_{std}]$ is derived and given in (4.48).

$$[S_{std}] = \begin{bmatrix} 0 & -j\frac{\alpha}{\sqrt{2}} & j\frac{\alpha}{\sqrt{2}} & j\frac{\sqrt{1-\alpha^2}}{\sqrt{2}} & -j\frac{\sqrt{1-\alpha^2}}{\sqrt{2}} \\ -j\frac{\alpha}{\sqrt{2}} & -\frac{1}{2} & -\frac{1}{2} & 0 & 0 \\ j\frac{\alpha}{\sqrt{2}} & -\frac{1}{2} & -\frac{1}{2} & 0 & 0 \\ j\frac{\sqrt{1-\alpha^2}}{\sqrt{2}} & 0 & 0 & -\frac{1}{2} & -\frac{1}{2} \\ -j\frac{\sqrt{1-\alpha^2}}{\sqrt{2}} & 0 & 0 & -\frac{1}{2} & -\frac{1}{2} \end{bmatrix} \tag{4.48}$$

4.2.3 Analysis of Power Transmission from Input Port to Output Ports

Under this condition, equivalent circuit of the proposed power divider is shown in Fig. 4.12. Under the ideal condition, power should be divided from input port into two output ports according to the power division ratio, no power gets dissipated in two isolation resistors [16, 20]. Therefore, ground point moves to the other ends of the resistors. This means that one ends of the pair of transmission lines of characteristic impedances Z_3 and Z_4 is connected to the ground. Then, the other ends of these

transmission lines become open circuited (using the property of a quarter wave transformer).

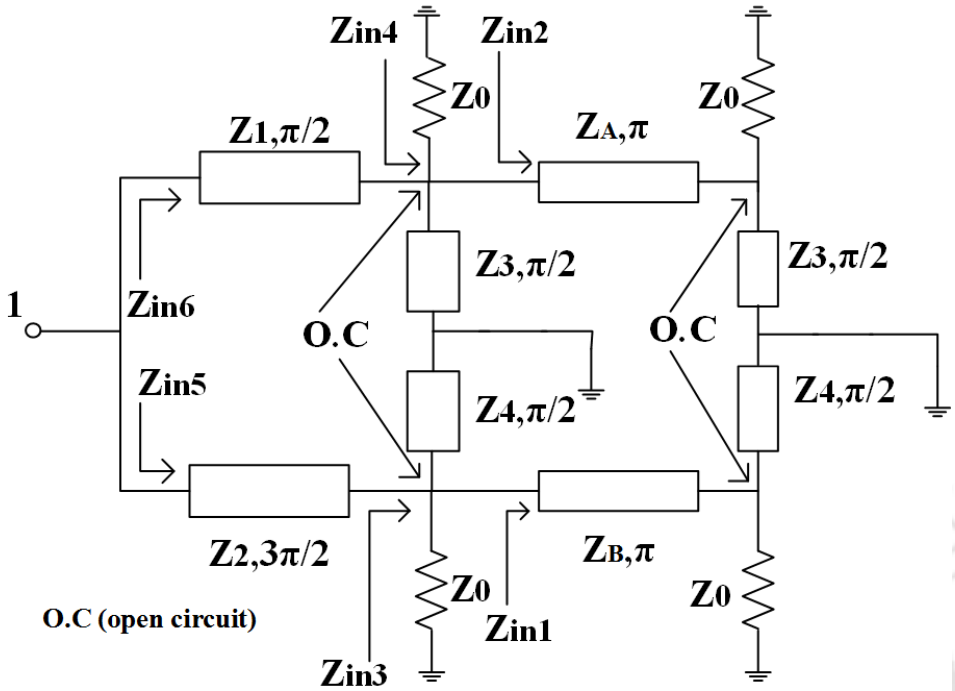


Figure 4.12: Equivalent circuit for power transmission from unbalanced input port to balanced output ports.

From Fig. 4.12, Z_{in1} and Z_{in2} are obtained as:

$$Z_{in1} = Z_{in2} = Z_0 \tag{4.49}$$

Z_{in3} is the parallel combination of Z_0 and Z_{in1} while Z_{in4} is the parallel combination of Z_0 and Z_{in2}. Z_{in3} and Z_{in4} are given as:

$$Z_{in3} = Z_{in4} = Z_0/2 \tag{4.50}$$

From Fig. 4.12, Z_{in5} and Z_{in6} are obtained using properties of quarter wave transformer.

$$Z_{in5} = \frac{2Z_2^2}{Z_0} \quad Z_{in6} = \frac{2Z_1^2}{Z_0} \tag{4.51}$$

If the power division ratio from port 1 to ports A and B is $1 : k^2$. Then Z_{in5} and Z_{in6} are related as:

$$Z_{in6} = k^2 Z_{in5} \tag{4.52}$$

Using (4.51) and (4.52), Z_1 and Z_2 are related as:

$$Z_1 = kZ_2 \tag{4.53}$$

The parallel combination of Z_{in5} and Z_{in6} is equal to Z_0 (port impedance of port 1).

$$Z_{in5}||Z_{in6} = Z_0 \tag{4.54}$$

Using (4.51), (4.53) and (4.54), Z_1 and Z_2 are obtained as:

$$Z_1 = Z_0\sqrt{\frac{1+k^2}{2}} \tag{4.55}$$

$$Z_2 = \frac{Z_0}{k}\sqrt{\frac{1+k^2}{2}} \tag{4.56}$$

4.2.4 Isolation Analysis between Two Output Ports

Fig. 4.13 shows the equivalent circuit of proposed power divider for this analysis. When port A is exited, then no power should flow to port B. This happens when the voltage at ports 4 and 5 (combined as port B) is zero [16, 20]. Therefore, one end of the transmission lines of characteristic impedance Z_4 and transmission line of characteristic impedance Z_2 are connected to ground. Then, using quarter-wave transformer property, the other ends of these transmission lines are open circuited.

From Fig. 4.13, using quarter wave transformer property, Z_{in7}, Z_{in8} and Z_{in9} are obtained as:

$$Z_{in7} = Z_{in8} = \frac{Z_3^2}{R},\ Z_{in9} = \frac{Z_1^2}{Z_0} \tag{4.57}$$

Let Z_{in10} is the parallel combination of Z_{in7} and Z_{in9}. Using (4.57), Z_{in10} is obtained as:

$$Z_{in10} = Z_{in7}||Z_{in9} = \frac{Z_1^2 Z_3^2}{RZ_1^2 + Z_0 Z_3^2} \tag{4.58}$$

Now, the transmission matrix between ports 2 & 3 ($[ABCD]_{23}$) is obtained as:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{23} = \begin{bmatrix} 1 & 0 \\ \frac{Z_0}{Z_1^2} + \frac{R}{Z_3^2} & 1 \end{bmatrix} \begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{R}{Z_3^2} & 1 \end{bmatrix} \tag{4.59}$$

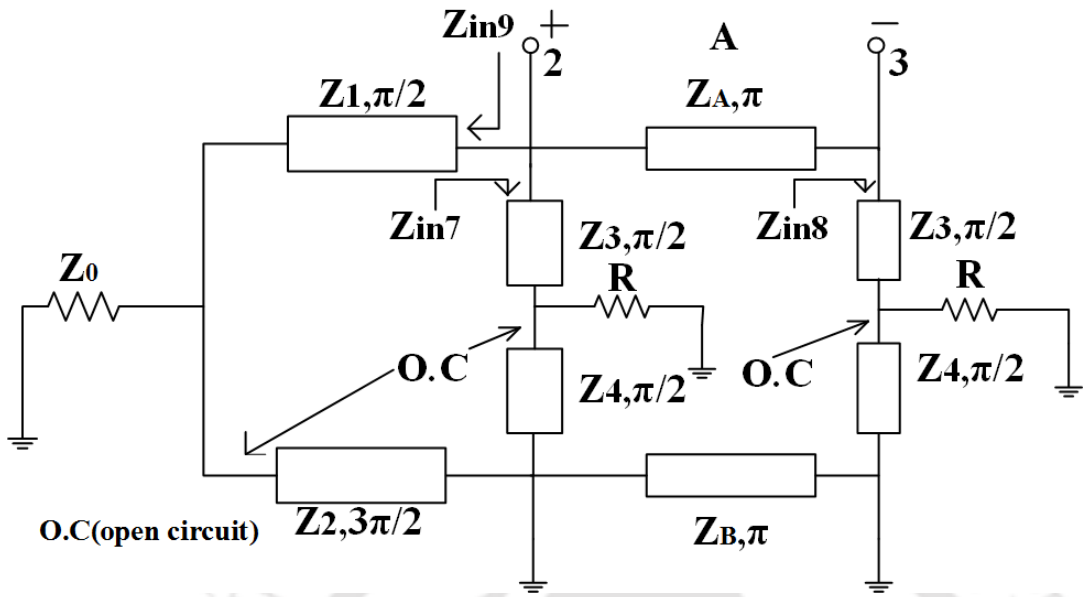


Figure 4.13: Isolation analysis between two output ports.

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{23} = \begin{bmatrix} -1 & 0 \\ -\frac{Z_0}{Z_1^2} - \frac{2R}{Z_3^2} & -1 \end{bmatrix} \tag{4.60}$$

Scattering matrix between ports 2 & 3 ($[S]_{23}$) can be obtained by the matrix conversion from $[ABCD]_{23}$. The elements of matrix $[S]_{23}$ are derived and given in (4.61) and (4.62).

$$S_{22} = S_{33} = -\frac{Z_0^2 Z_3^2 + 2RZ_0 Z_1^2}{2Z_1^2 Z_3^2 + Z_0^2 Z_3^2 + 2RZ_0 Z_1^2} \tag{4.61}$$

$$S_{23} = S_{32} = -\frac{2Z_1^2 Z_3^2}{2Z_1^2 Z_3^2 + Z_0^2 Z_3^2 + 2RZ_0 Z_1^2} \tag{4.62}$$

For port A (combination of ports 2 & 3) to be matched, differential reflection coefficient (S_{ddAA}) of port A should be zero.

$$S_{ddAA} = \frac{1}{2}(S_{22} - S_{23} - S_{32} + S_{33}) = 0 \tag{4.63}$$

Using (4.61)-(4.63) and if R is assumed as Z_0, Z_3 is obtained as:

$$Z_3 = \sqrt{\frac{2Z_1^2}{(2Z_1^2/Z_0^2) - 1}} \tag{4.64}$$

Similarly, if port B is excited, then no power should flow to port A. After doing the same process,

Z_4 can be obtained as:

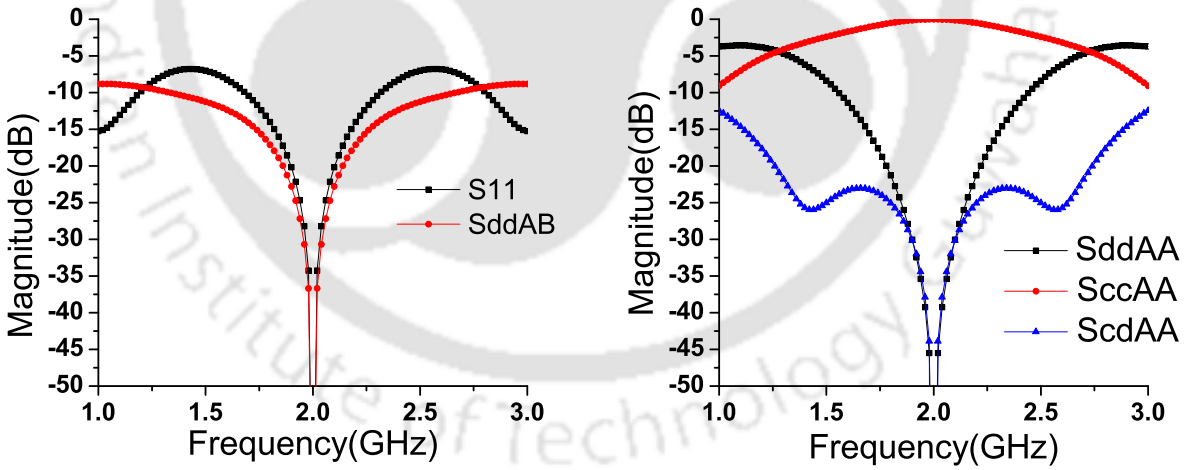
$$Z_4 = \sqrt{\frac{2Z_2^2}{(2Z_2^2/Z_0^2) - 1}} \tag{4.65}$$

Z_A and Z_B can be chosen independently.

4.2.5 Theoretical Results

The proposed UTB power divider is designed at 2 GHz for power division ratio ($k^2 = 2$). Isolation resistor R is taken as 50 Ω. Using design equations (4.55), (4.56), (4.64) and (4.65), Z_1, Z_2, Z_3 and Z_4 are obtained as 61.23 Ω, 43.30 Ω, 61.23 Ω and 86.88 Ω, respectively. Z_A is taken same as the Z_1 and Z_B is taken same as Z_2. Figs. 4.14-4.16 show theoretical results of the proposed power divider. For theoretical results, lossless transmission line and ideal lumped components are used.

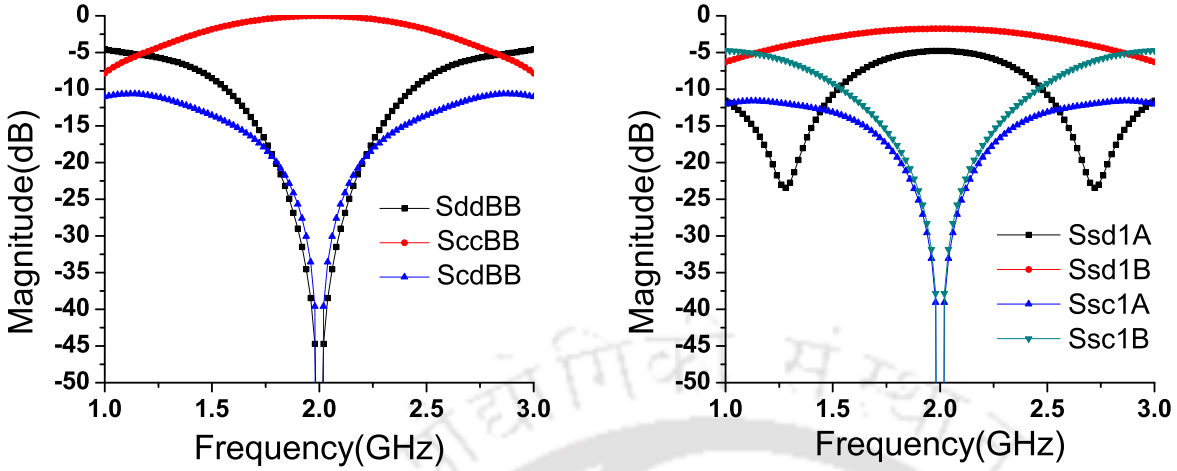
As shown in Fig. 4.14(a), unbalanced port is perfectly matched and both balanced ports are perfectly isolated at the center frequency. As shown in Fig. 4.14(b) and Fig. 4.15(a), balanced ports A and B are perfectly matched, common-mode reflections are 0 dB and no mode conversion between differential and common-mode. Theoretical results of $|S_{sd1A}|$, $|S_{sd1B}|$ are -4.7 dB, -1.7 dB at the design



(a) (b)

Figure 4.14: (a) Theoretical results of $|S_{ss11}|$ and $|S_{ddAB}|$. (b) Theoretical results of $|S_{ddAA}|$, $|S_{ccAA}|$ and $|S_{cdAA}|$.

frequency, respectively shown in Fig. 4.15(b). Results of $|S_{sc1A}|$ and $|S_{sc1B}|$ show that common-mode signals are perfectly suppressed. The difference between differential-mode power divided in ports A and B is 3 dB. Fig. 4.16 shows theoretical results of phase difference as a function of the power



(a) (b)

Figure 4.15: (a) Theoretical results of $|S_{ddBB}|$, $|S_{ccBB}|$ and $|S_{cdBB}|$. (b) Theoretical results of $|S_{sd1A}|$, $|S_{sd1B}|$, $|S_{sc1A}|$ and $|S_{sc1B}|$.

division ratio. It shows that as power division ratio increases, variation of phase difference from in-phase characteristic increases.

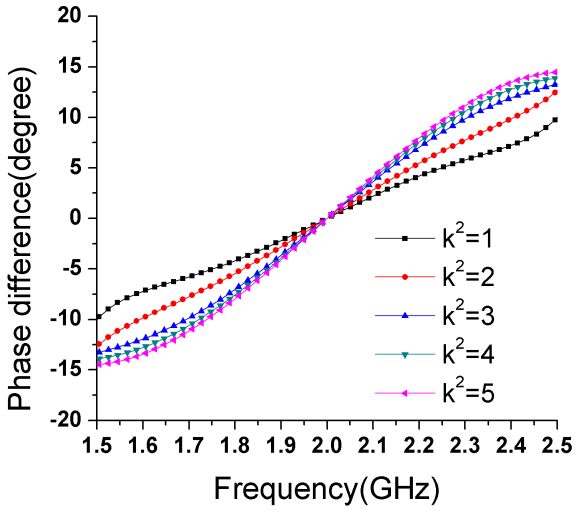


Figure 4.16: Theoretical results of phase difference for different power division ratio.

4.2.6 Simulation and Measured Results

The proposed power divider has been fabricated on FR-4 substrate of dielectric constant $\epsilon_r = 4.4$ and thickness $h = 1.6\ mm$. Fig. 4.17 shows the fabricated prototype of the proposed UTB power divider. Figs. 4.18-4.20 show the comparison of simulated (using HFSS) and measured results.

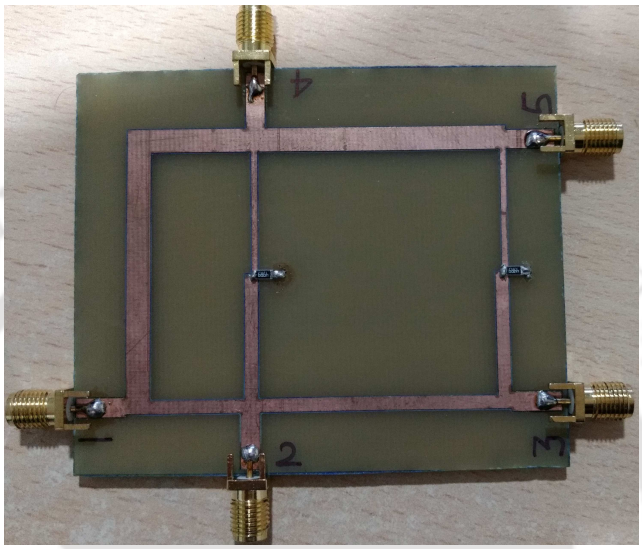
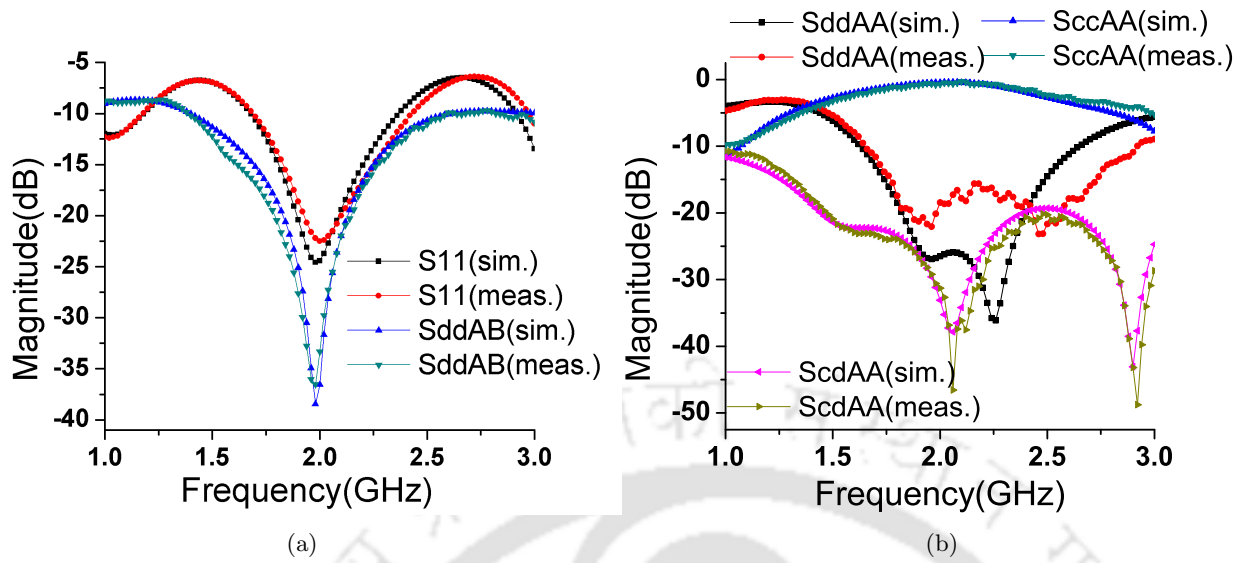


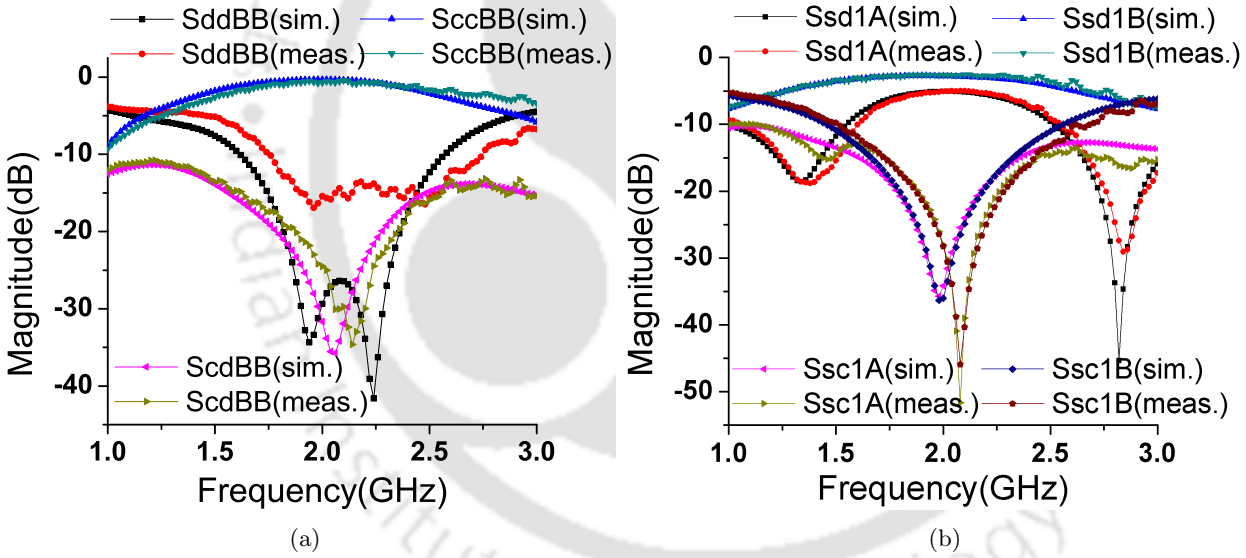
Figure 4.17: Fabricated prototype of proposed Gysel type power divider for $k^2 = 2$.

Fig. 4.18(a) shows the comparison of simulated and measured return loss of single-ended input port ($|S_{ss11}|$) and isolation ($|S_{ddAB}|$) between two balanced output ports. Measured $|S_{ss11}|$ is greater than 15 dB from 1.84 GHz to 2.24 GHz and measured $|S_{ddAB}|$ is greater than 20 dB from 1.80 GHz to 2.14 GHz. Fig. 4.18(b) shows common-mode reflection ($|S_{ccAA}|$), differential-mode return loss ($|S_{ddAA}|$), differential to common-mode conversion ($|S_{cdAA}|$) of the balanced port A, respectively. Measured $|S_{ccAA}|$ is less than 1 dB from 1.86 GHz to 2.28 GHz. Measured $|S_{ddAA}|$ is greater than 15 dB from 1.78 GHz to 2.72 GHz. Measured $|S_{cdAA}|$ is greater than 25 dB from 1.86 GHz to 2.26 GHz. Fig. 4.19(a) shows common-mode reflection ($|S_{ccBB}|$), differential-mode return loss ($|S_{ddBB}|$), differential to common-mode conversion ($|S_{cdBB}|$) of the balanced port B, respectively. Measured $|S_{ccBB}|$ is less than 1 dB from 1.76 GHz to 2.28 GHz. Measured $|S_{ddBB}|$ is greater than 10 dB from 1.76 GHz to 2.74 GHz. Measured $|S_{cdBB}|$ is greater than 20 dB from 1.88 GHz to 2.34 GHz. In Fig. 4.19(b), measured common-mode suppression to balanced ports A and B ($|S_{sc1A}|$ and $|S_{sc1B}|$) are greater than 20 dB from 1.9 GHz to 2.18 GHz. Differential-mode power ($|S_{sd1A}|$ and $|S_{sd1B}|$) is divided in the power division ratio 1 : 2 around design frequency. Fig. 4.20 shows the comparison of simulated and



(a) (b)

Figure 4.18: (a) Comparison of $|S_{ss11}|$ and $|S_{ddAB}|$. (b) Comparison of $|S_{ddAA}|$, $|S_{ccAA}|$ and $|S_{cdAA}|$.



(a) (b)

Figure 4.19: (a) Comparison of $|S_{ddBB}|$, $|S_{ccBB}|$ and $|S_{cdBB}|$. (b) Comparison of $|S_{sd1A}|$, $|S_{sd1B}|$, $|S_{sc1A}|$ and $|S_{sc1B}|$.

measured phase difference ($Ang(S_{sd1A}/S_{sd1B})$). This shows the in-phase characteristic of the proposed power divider.

The measured fractional bandwidth is 21% (from 1.86 GHz to 2.28 GHz). The conditions for calculating the fractional bandwidth are: (i) Difference between $|S_{sd1B}|$ and $|S_{sd1A}|$ is less than 4 dB (ii) $|S_{ccAA}|$ and $|S_{ccBB}|$ are less than 1 dB (iii) All other scattering parameters are greater than 10 dB.

Comparison of measured results of proposed UTB power dividers with the reported works are

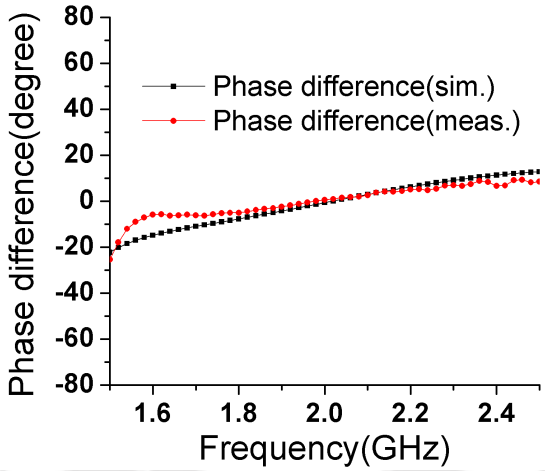


Figure 4.20: Comparison of phase difference.

Table 4.1: Comparison of proposed UTB power dividers with previous related works.

Ref.	Freq(GHz)	Type	Isolation (dB)	Bandwidth	Transmission Loss (dB)
[92]	1.8	Equal (Wilkinson)	> 20	17% (Isolation)	0.15
[93]	1	Equal (Wilkinson)	> 20	37%	0.34
PD in section 4.1	2	Equal	> 20	12%	0.70
PD in section 4.2	2	Arbitrary (Prototype for 1:2)	> 20	21%	0.56

summarized in Table 4.1. As mentioned in the first chapter, section 1.3.1, insertion loss of Gysel power divider is higher than Wilkinson power divider because of the large size, therefore proposed Gysel power dividers are having higher insertion loss. The bandwidths of the proposed power dividers are narrower than the Wilkinson power dividers, as mentioned in Table 4.1. This is because of the transmission line of electrical length $3\pi/2$ used in both the power dividers. This causes two zeros in the characteristic of $|S_{sd1A}|$ near the design frequency, which results in bandwidth reduction. If the transmission line of electrical length $3\pi/2$ is replaced by the short circuited coupled transmission line as described in third chapter, section 3.3.5, then there will be no zeros in the characteristic of $|S_{sd1A}|$ near the design frequency and bandwidth can be increased.

4.3 Conclusion

In this chapter, two UTB power dividers are proposed. The first power divider is for equal power division and other one is for arbitrary power division ratio. Both the proposed power dividers are of Gysel type, therefore these configurations can be used for high power application as well. Theoretical analysis is provided for deriving the design equations for each power divider. For each power divider, a prototype has been fabricated and tested. Both fabricated prototypes show good agreement between simulation and measured results. Major limitations of the proposed Gysel power dividers are of narrower bandwidth and large size. Both these limitation of the proposed power dividers are because of the use of transmission line of electrical length $3\pi/2$. If this transmission line of electrical length $3\pi/2$ is replaced by short circuited coupled transmission line as described in third chapter, section 3.3.5, both these limitation can be removed. In the future work, power dividers with shorts circuited coupled line will be implemented to remove the limitations of the proposed power dividers.

5

Dual-band Power Divider

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5.3 Conclusion 124

In this chapter, two dual-band power dividers are presented. First one is of BTU type out-of-phase equal power divider. This BTU power divider is of Gysel type. The second one is a Wilkinson type single-ended arbitrary power divider.

5.1 Dual-band Balanced-to-Unbalanced Equal Power Divider

5.1.1 Circuit Diagram

The proposed dual-band BTU out-of-phase equal power divider is shown in Fig. 5.1. As shown in Fig. 5.1, balanced port of the circuit is represented as port A which is the combination of ports 2 & 4. Ports 1 & 3 are the unbalanced ports of the power divider as shown in Fig. 5.1. Resistor R, which provides the isolation between the two output ports is connected to ground. As shown in Fig. 5.1, there are three pairs of transmission lines of characteristic impedances Z_1, Z_2 and Z_3 respectively, and an open circuited stub of characteristic impedance Z_4. All the transmission lines are of electrical length θ.

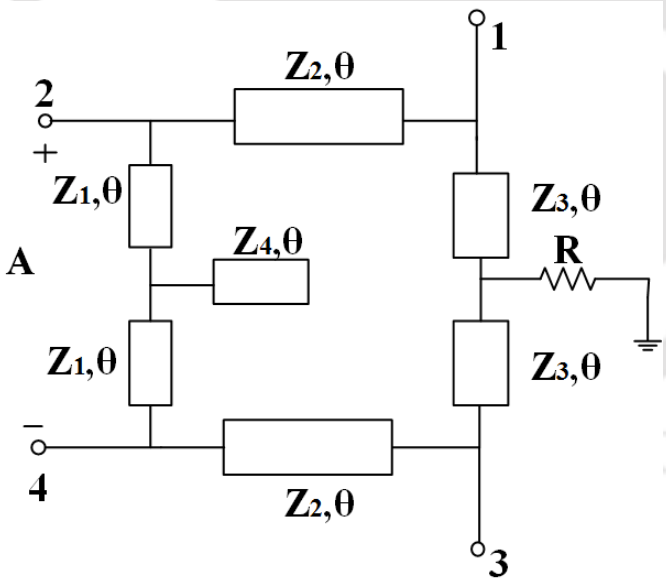


Figure 5.1: Circuit diagram of the proposed dual-band power divider.

A standard scattering matrix of this power divider is similar to the one derived in chapter 3, for

out-of-phase equal power divider. The standard scattering matrix is same as given in (3.17).

$$[S_{std}] = \frac{1}{2}\begin{bmatrix} 0 & -j & 0 & j \\ -j & -1 & j & -1 \\ 0 & j & 0 & -j \\ j & -1 & -j & -1 \end{bmatrix} \tag{5.1}$$

5.1.2 Odd-Mode Analysis

Circuit of the proposed power divider is symmetrical. Therefore, odd-mode analysis can be applied to this circuit. The odd-mode equivalent circuit of the proposed power divider is shown in Fig. 5.2. The odd-mode matrix $[S]_o$ of the proposed power divider is obtained from (5.1) and given in (5.2).

$$[S]_o = \begin{bmatrix} 0 & -j \\ -j & 0 \end{bmatrix} \tag{5.2}$$

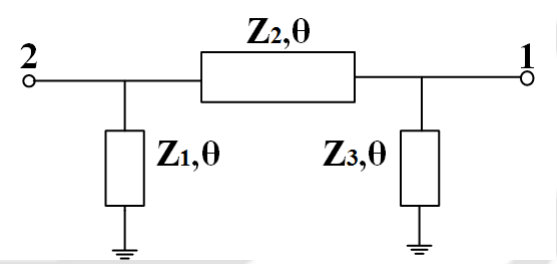


Figure 5.2: Odd-mode equivalent circuit of proposed power divider.

$[ABCD]_o$ matrix of the odd-mode equivalent circuit shown in Fig. 5.2 is obtained as:

$$[ABCD]_o = \begin{bmatrix} 1 & 0 \\ \frac{1}{jZ_1\tan\theta} & 1 \end{bmatrix}\begin{bmatrix} \cos\theta & jZ_2\sin\theta \\ \frac{j\sin\theta}{Z_2} & \cos\theta \end{bmatrix}\begin{bmatrix} 1 & 0 \\ \frac{1}{jZ_3\tan\theta} & 1 \end{bmatrix} \tag{5.3}$$

$$[ABCD]_o = \begin{bmatrix} \cos\theta(1+\frac{Z_2}{Z_3}) & jZ_2\sin\theta \\ \frac{\cos\theta}{j\tan\theta}(\frac{1}{Z_1}+\frac{1}{Z_3})+\frac{j\sin\theta}{Z_2}+\frac{Z_2\cos\theta}{jZ_1Z_3\tan\theta} & \cos\theta(1+\frac{Z_2}{Z_1}) \end{bmatrix} \tag{5.4}$$

Odd-mode matrix $[S]_o$ can be obtained from the $[ABCD]_o$ by matrix transformation. For diagonal elements (S_{11o} and S_{22o}) of this $[S]_o$ matrix and of (5.2) to be equal, following conditions should be

full-filled:

$$A_o = D_o \tag{5.5}$$

$$\frac{B_o}{Z_0} = C_o Z_0 \tag{5.6}$$

where, Z_0 is the port impedance.

Using (5.4) and (5.5), the relationship between Z_1 and Z_3 is obtained as:

$$Z_1 = Z_3 \tag{5.7}$$

Using (5.4) and (5.6), Z_2 is obtained as:

$$Z_2 = \frac{-Z_0^2 Z_1 + Z_0 Z_1 \sqrt{Z_0^2 + (Z_0^2 + Z_1^2 \tan^2\theta)\tan^2\theta}}{Z_0^2 + Z_1^2 \tan^2\theta} \tag{5.8}$$

5.1.3 Analysis of Two-port Network between Ports 2 and 4

The two-port network between ports 2 & 4 is shown in Fig. 5.3. In Fig. 5.3, Z_X and Z_Y are the equivalent impedance of the network looking at the ports 2 & 4, respectively. $[S]_{24}$ matrix of the two-port network between ports 2 & 4 is obtained from (5.1) and given in (5.9).

$$[S]_{24} = \begin{bmatrix} -\frac{1}{2} & -\frac{1}{2} \\ -\frac{1}{2} & -\frac{1}{2} \end{bmatrix} \tag{5.9}$$

$[ABCD]_{24}$ matrix which is equivalent to $[S]_{24}$ is obtained by matrix transformation and given in (5.10).

$$[ABCD]_{24} = \begin{bmatrix} -1 & 0 \\ -\frac{2}{Z_0} & -1 \end{bmatrix} \tag{5.10}$$

For the circuit shown in Fig. 5.3, $[ABCD]_{24}$ is obtained as:

$$[ABCD]_{24} = \begin{bmatrix} 1 & 0 \\ \frac{1}{Z_X} & 1 \end{bmatrix} \begin{bmatrix} \cos\theta & jZ_1 \sin\theta \\ \frac{j\sin\theta}{Z_1} & \cos\theta \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{j\tan\theta}{Z_4} & 1 \end{bmatrix} \begin{bmatrix} \cos\theta & jZ_1 \sin\theta \\ \frac{j\sin\theta}{Z_1} & \cos\theta \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{Z_Y} & 1 \end{bmatrix} \tag{5.11}$$

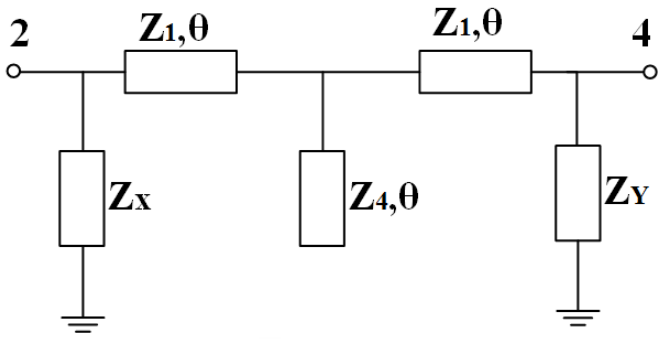


Figure 5.3: Two-port network between ports 2 & 4.

From (5.11), A_{24} is obtained and given in (5.12).

$$A_{24} = \cos^2\theta - Z_1 \sin^2\theta\left(\frac{1}{Z_1} + \frac{1}{Z_4}\right) + j\frac{Z_1 \sin\theta}{Z_Y}\left(2\cos\theta - \frac{Z_1 \sin\theta \tan\theta}{Z_4}\right) \tag{5.12}$$

Comparing A_{24} from (5.10) and (5.12), the imaginary part of A_{24} from (5.12) should be zero.

$$2\cos\theta - \frac{Z_1 \sin\theta \tan\theta}{Z_4} = 0 \tag{5.13}$$

$$Z_4 = \frac{Z_1}{2}\tan^2\theta \tag{5.14}$$

5.1.4 Analysis of Two-port Network between Ports 1 and 3

The two-port network between ports 1 & 3 is shown in Fig. 5.4. In Fig. 5.4, Z_P and Z_Q are the equivalent impedance of the network looking at ports 1 & 3, respectively. The $[S]_{13}$ matrix between ports 1 & 3 is obtained from (5.1) and given in (5.15).

$$[S]_{13} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{5.15}$$

$[Y]_{13}$ matrix which is equivalent to $[S]_{13}$ is obtained from the matrix transformation and given in (5.16).

$$[Y]_{13} = \begin{bmatrix} Y_0 & 0 \\ 0 & Y_0 \end{bmatrix} \tag{5.16}$$

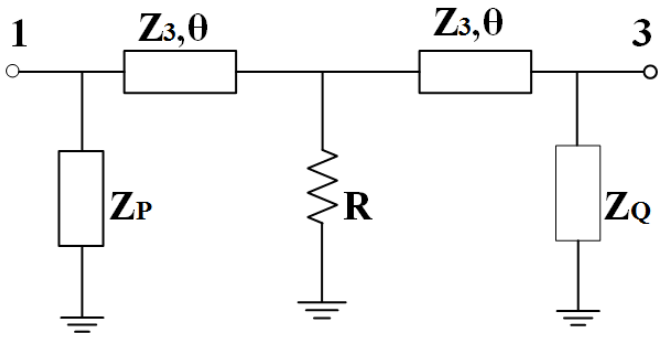


Figure 5.4: Two-port network between ports 1 & 3.

For the circuit shown in the Fig. 5.4, $[ABCD]_{13}$ can be obtained as:

$$[ABCD]_{13} = \begin{bmatrix} 1 & 0 \\ \frac{1}{Z_P} & 1 \end{bmatrix} \begin{bmatrix} \cos\theta & jZ_3\sin\theta \\ \frac{j\sin\theta}{Z_3} & \cos\theta \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{R} & 1 \end{bmatrix} \begin{bmatrix} \cos\theta & jZ_3\sin\theta \\ \frac{j\sin\theta}{Z_3} & \cos\theta \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{Z_Q} & 1 \end{bmatrix} \tag{5.17}$$

A_{13} and B_{13} are obtained from (5.17) and given in (5.18) and (5.19).

$$A_{13} = \cos^2\theta - Z_3\sin^2\theta\left(\frac{Z_3}{RZ_Q} + \frac{1}{Z_3}\right) + jZ_3\sin\theta\cos\theta\left(\frac{1}{R} + \frac{2}{Z_Q}\right) \tag{5.18}$$

$$B_{13} = -\frac{Z_3^2\sin^2\theta}{R} + j2Z_3\sin\theta\cos\theta \tag{5.19}$$

$[ABCD]_{13}$ from (5.17) is converted into $[Y]_{13}$ by matrix transformation. For diagonal elements ($Y_{11_{13}}$ and $Y_{22_{13}}$) of this $[Y]_{13}$ and of (5.16) to be equal, following conditions should be full-filled:

$$\frac{A_{13}}{B_{13}} = Y_0 \tag{5.20}$$

$$\frac{D_{13}}{B_{13}} = Y_0 \tag{5.21}$$

Using (5.18)-(5.20), following two equations are obtained.

$$\frac{1}{R} + \frac{2}{Z_Q} - 2Y_0 = 0 \tag{5.22}$$

$$\cot^2\theta - 1 - \frac{Z_3^2}{R}\left(\frac{1}{Z_Q} - Y_0\right) = 0 \tag{5.23}$$

From (5.22) and (5.23), Z_3 is obtained as:

$$Z_3 = R\sqrt{2(1-\cot^2\theta)} \tag{5.24}$$

5.1.5 Dual-band Design

The proposed power divider is designed for the dual-band application. Let the two design frequencies of the proposed power divider are f_1 and f_2. These two frequencies are related as:

$$f_2 = mf_1 \tag{5.25}$$

where, m is the frequency ratio and $m > 1$. The electrical length θ of transmission line is related to frequency ratio as:

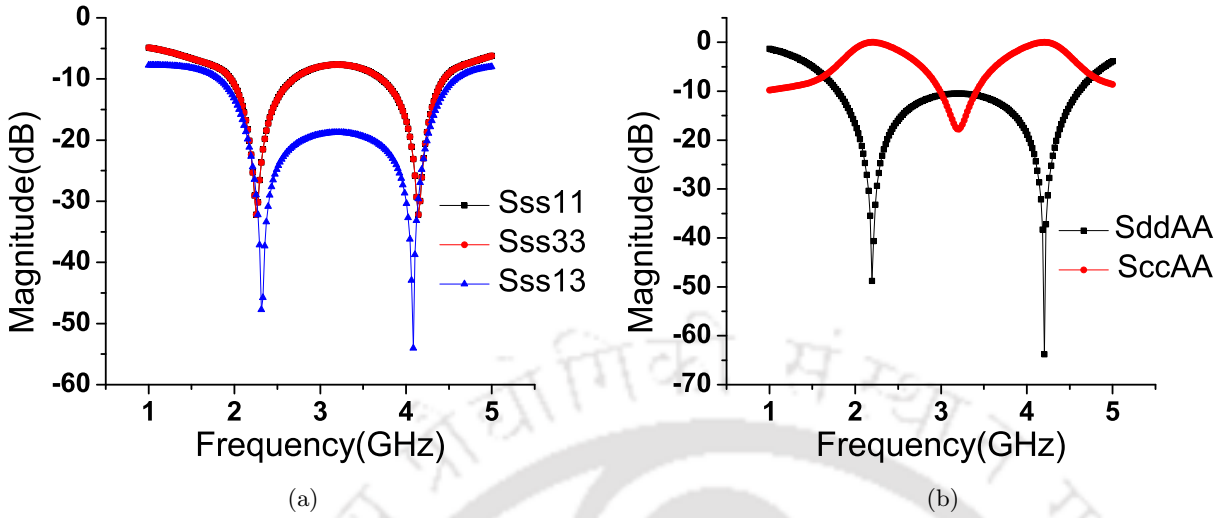
$$\theta = \frac{\pi}{1+m} \tag{5.26}$$

5.1.6 Theoretical Results

The proposed dual-band out-of-phase equal power divider is designed for frequency ratio $m = 1.91$. The two design frequencies are 2.2 GHz and 4.2 GHz. $\theta = 61.85°$ is obtained from (5.26). Isolation resistor R is taken as 50 Ω. Using design equations (5.7), (5.8), (5.14) and (5.24), Z_1, Z_2, Z_3, Z_4 are obtained as: $Z_1 = 59.73$ Ω, $Z_2 = 36.72$ Ω, $Z_3 = 59.73$ Ω, $Z_4 = 104.31$ Ω. Theoretical results are shown in Figs. 5.5-5.6.

Fig. 5.5(a) shows the return losses of unbalanced port and isolation between output ports. At the center frequency 2.2 GHz, $|S_{ss11}|$, $|S_{ss13}|$ and $|S_{ss33}|$ are -32 dB, -32 dB and -28 dB, respectively. At the center frequency 4.2 GHz $|S_{ss11}|$, $|S_{ss13}|$ and $|S_{ss33}|$ are -22 dB, -22 dB, -32 dB, respectively. Fig. 5.5(b) shows differential return loss and common-mode reflection of the balanced port A. At the center frequency 2.2 GHz, $|S_{ddAA}|$ and $|S_{ccAA}|$ are -40 dB and 0 dB, respectively. At the center frequency 4.2 GHz, $|S_{ddAA}|$ and $|S_{ccAA}|$ are -63 dB and 0 dB, respectively.

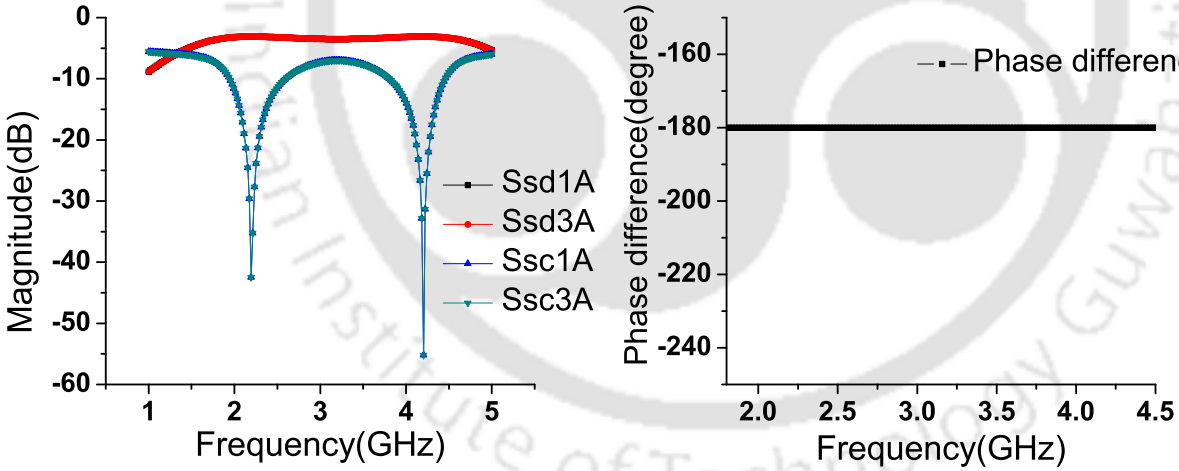
Fig. 5.6(a) shows the differential-mode transmission coefficient and common-mode suppression from balanced port to unbalanced ports. At the center frequency 2.2 GHz, $|S_{sd1A}|$, $|S_{sd3A}|$, $|S_{sc1A}|$ and $|S_{sc3A}|$ are -3 dB, -3 dB, -35 dB and -35 dB, respectively. At the center frequency 4.2 GHz, $|S_{sd1A}|$, $|S_{sd3A}|$, $|S_{sc1A}|$ and $|S_{sc3A}|$ are -3 dB, -3 dB, -55 dB and -55 dB, respectively. Fig. 5.6(b) shows the phase difference ($Ang(S_{sd1A}/S_{sd3A})$) between two output signals. This shows out-of-phase



(a) (b)

Figure 5.5: (a) Theoretical results of $|S_{ss11}|$, $|S_{ss13}|$ and $|S_{ss33}|$. (b) Theoretical results of $|S_{ddAA}|$ and $|S_{ccAA}|$.

characteristic of the power divider.



(a) (b)

Figure 5.6: (a) Theoretical results of $|S_{sd1A}|$, $|S_{sd3A}|$, $|S_{sc1A}|$ and $|S_{sc3A}|$. (b) Theoretical results of phase difference.

5.1.7 Simulation and Measured Results

HFSS has been used for the simulation. Fabrication has been done on a FR-4 substrate of dielectric constant $\epsilon_r = 4.4$ and substrate thickness $h = 1.6\ mm$. The optimized value of isolation resistor is

taken as 100 Ω. The fabricated prototype is shown in Fig. 5.7. Figs. 5.8-5.9 show the comparison of simulated and measured results.

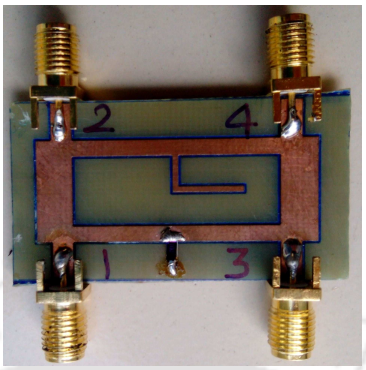
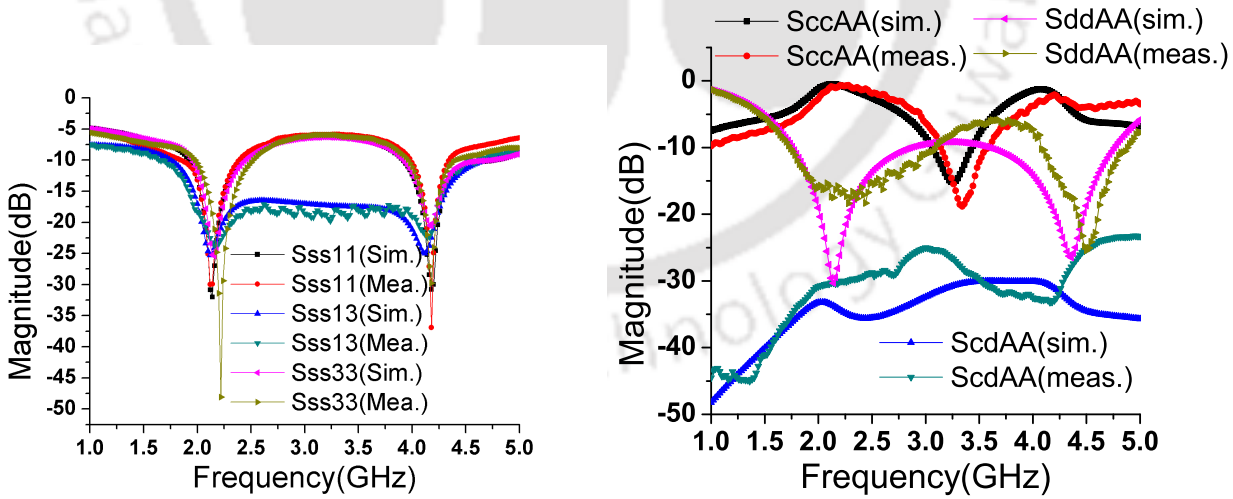


Figure 5.7: Fabricated prototype of dual-band power divider.

In Fig. 5.8(a), measured $|S_{ss11}|$ is greater than 15 dB from 2.04 to 2.24 GHz and 4.10 to 4.24 GHz, measured $|S_{ss33}|$ is greater than 15 dB from 2.10 GHz to 2.34 GHz and 4.10 GHz to 4.26 GHz. Measured $|S_{ss13}|$ is greater than 15 dB from 1.94 GHz to 4.28 GHz. In Fig. 5.8(b), measured $|S_{ccAA}|$ is less than 1 dB from 2.1 to 2.32 GHz and less than 2.5 dB from 4.16 to 4.24 GHz. Measured $|S_{cdAA}|$ is greater than 20 dB from 1 to 5 GHz. Measured $|S_{ddAA}|$ is greater than 10 dB around the two center frequencies. In Fig. 5.9(a), measured $|S_{sc1A}|$ is greater than 15 dB from 2.08 to 2.40 GHz and 4.06

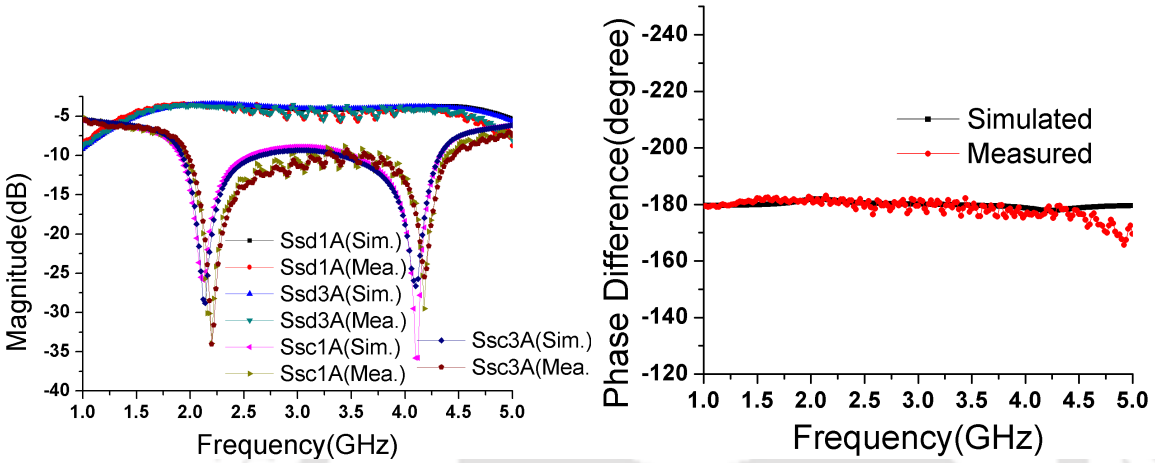


(a) (b)

Figure 5.8: (a) Comparison of unbalanced port S parameters. (b) Comparison of balanced port return loss, common mode reflection and mode conversion.

to 4.28 GHz, measured $|S_{sc3A}|$ is greater than 15 dB from 2.10 to 2.42 GHz and 4.06 to 4.28 GHz.

Power is almost equally divided around two design frequencies from port A to port 1 & 3 ($|S_{sd1A}|$, $|S_{sd3A}|$). Fig. 5.9(b), shows the unwrapped phase difference ($Ang(S_{sd1A}/S_{sd3A})$) between two output signals. This shows the out-of-phase characteristic of the proposed power divider around the two design frequencies.



(a) (b)

Figure 5.9: (a) Comparison of differential-mode transmission and CMS to unbalanced ports. (b) Comparison of phase difference.

5.2 Dual-band Single-ended Power Divider

This section presents the details of a dual-band single-ended power divider which is studied in the initial phase of the research work to understand the basic of dual-band operation of a power divider.

5.2.1 Block Diagram

In this section, a dual-band single-ended arbitrary power divider is presented. The structure of the power divider is shown in Fig. 5.10. It consists of five transmission line sections of impedances ($Z_1 - Z_5$) and two coupled lines of even and odd-mode impedances Z_e, Z_{od} & $Z_e^{'}, Z_{od}^{'}$, respectively. Between two output ports of power divider, a complex isolation of impedance Z is connected.

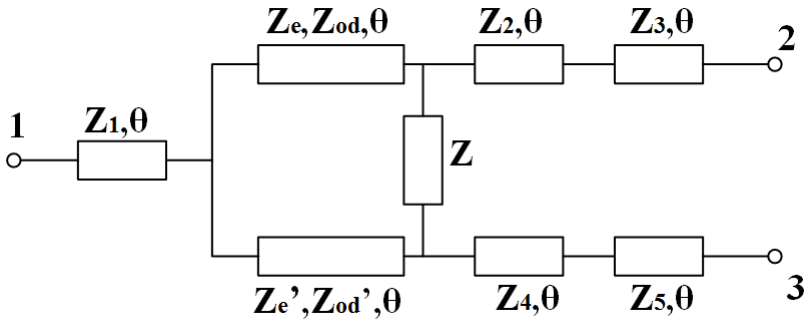


Figure 5.10: Dual-band arbitrary power divider.

5.2.2 Even-Mode Analysis

Two sources of equal amplitude and same phase are applied to ports 2 & 3. Analysis method described in [111] is used for this design. Let the power division ratio is equal to $k^2(\frac{P_3}{P_2} = k^2)$. Under this condition, equivalent circuit is shown in Fig. 5.11. Z_1 is divided into two parts Z_{12} and Z_{13} and parallel combination of Z_{12} and Z_{13} is equal to Z_1. To divided the power, according to the power

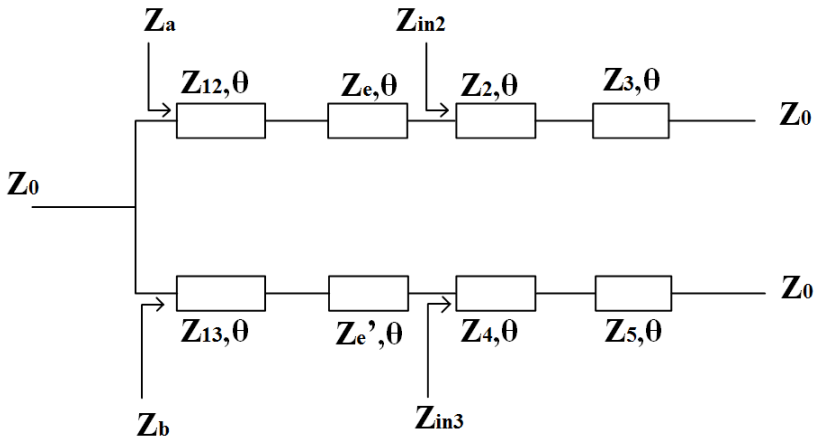


Figure 5.11: Equivalent circuit for even-mode analysis.

division ratio, Z_a, Z_b and Z_{in2}, Z_{in3} are related as:

$$Z_a = k^2 Z_b,\ Z_{in2} = k^2 Z_{in3} \tag{5.27}$$

In order to satisfy (5.27), Let,

$$Z_{in2} = kZ_0,\ Z_{in3} = \frac{Z_0}{k} \tag{5.28}$$

The parallel combination of Z_a and Z_b is equal to Z_0.

$$Z_a||Z_b = Z_0 \tag{5.29}$$

Using (5.27) and (5.29), Z_a and Z_b are obtained as:

$$Z_a = (1+k^2)Z_0,\ Z_b = \frac{1+k^2}{k^2}Z_0 \tag{5.30}$$

In upper half of Fig. 5.11, input impedance is Z_a and output impedance is Z_{in2}. In between there are two transmission lines which are to be matched at two frequencies. Using Monzon's theory [112], Z_e and Z_{12} are obtained as:

$$Z_e = Z_0\sqrt{\frac{k}{2\alpha}(k^2-k+1)+\sqrt{\left[\frac{k}{2\alpha}(k^2-k+1)\right]^2+k^3(1+k^2)}} \tag{5.31}$$

$$Z_{12} = \frac{Z_a Z_{in2}}{Z_e} \tag{5.32}$$

where,

$$\alpha = \tan^2\theta_{f1} \tag{5.33}$$

$$\theta_{f1} = \frac{\pi}{1+m} \tag{5.34}$$

$$\theta_{f2} = \frac{m\pi}{1+m} = \pi - \frac{\pi}{1+m} = \pi - \theta \tag{5.35}$$

$$f_2 = mf_1 \tag{5.36}$$

where, f_1 and f_2 are the two design frequencies and m is the frequency ratio. Using the same theory in the lower half of the circuit, $Z_e^{'}$ and Z_{13} are obtained as:

$$Z_e^{'} = \frac{Z_0}{k_2}\sqrt{\frac{k}{2\alpha}(k^2-k+1)+\sqrt{\left[\frac{k}{2\alpha}(k^2-k+1)\right]^2+k^3(1+k^2)}} \tag{5.37}$$

$$Z_{13} = \frac{Z_b Z_{in3}}{Z_e^{'}} \tag{5.38}$$

The Monzon's theory also used to obtain Z_2, Z_3, Z_4 and Z_5, the impedances are given as:

$$Z_2 = Z_0\sqrt{\frac{k}{2\alpha}(1-k)+\sqrt{\left[\frac{k}{2\alpha}(1-k)\right]^2+k^3}} \tag{5.39}$$

$$Z_3 = \frac{kZ_0Z_0}{Z_2} = \frac{kZ_0^2}{Z_2} \tag{5.40}$$

$$Z_4 = \frac{(Z_0/k)Z_0}{Z_5} = \frac{Z_0^2}{kZ_5} \tag{5.41}$$

$$Z_5 = \frac{Z_0}{k}\sqrt{\frac{k}{2\alpha}(1-k)+\sqrt{\left[\frac{k}{2\alpha}(1-k)\right]^2+k^3}} \tag{5.42}$$

5.2.3 Isolation Analysis

A voltage source V_s is connected at port 2 with resistance R_2 as shown in Fig. 5.12. Characteristic impedances of coupled lines are defined as:

$$Z_c = \sqrt{Z_eZ_{od}},\ Z_c{}' = \sqrt{Z_e'Z_{od}'} \tag{5.43}$$

For isolation, if port 2 is excited, then port 3 should be short circuited.

$$V_3 = 0 \tag{5.44}$$

Using transmission line theory and circuit analysis method, isolation impedance Z is obtained as:

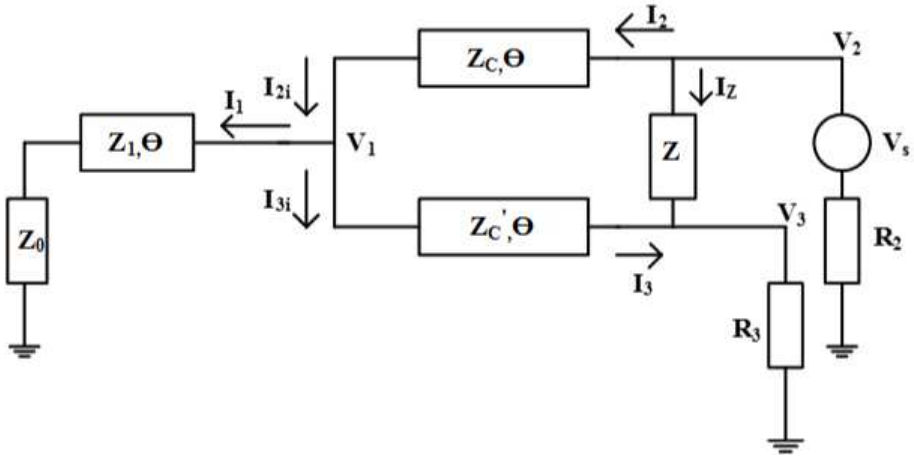


Figure 5.12: Equivalent circuit for isolation analysis.

$$Z = Z_r + jZ_i \tag{5.45}$$

where,

$$Z_r = \frac{Z_c Z_c' Z_0 \sin^2\theta}{Z_0^2\cos^2\theta + Z_1^2\sin^2\theta} \tag{5.46}$$

$$Z_i = \frac{-Z_0^4 \sin\theta\cos\theta}{Z_1[Z_0^2\cos^2\theta + Z_1^2\sin^2\theta]} \tag{5.47}$$

Z can be represented at two different frequencies ω_1 and ω_2 as:

$$Z = Z_r \pm jZ_i \tag{5.48}$$

The isolation structure used for this design is shown in Fig. 5.13. At two different frequencies, isolation impedances are obtained as:

$$Z(\omega_1) = \frac{1}{\frac{1}{R} + \frac{1}{\frac{1}{j\omega_1 C} + j\omega_1 L + \frac{1}{j\omega_1 C}}} \tag{5.49}$$

$$Z(\omega_2) = \frac{1}{\frac{1}{R} + \frac{1}{\frac{1}{j\omega_2 C} + j\omega_2 L + \frac{1}{j\omega_2 C}}} \tag{5.50}$$

Using (5.48)-(5.50), values of R, L and C are derived and given in (5.51)-(5.53).

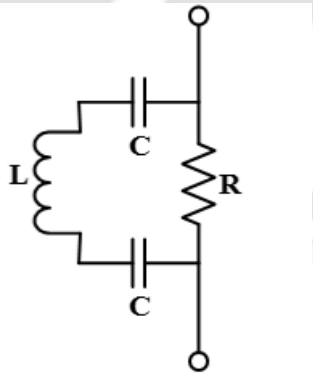


Figure 5.13: Circuit used for isolation structure.

$$R = \frac{Z_r^2 + Z_i^2}{Z_r} \tag{5.51}$$

$$L = \frac{Z_r^2 + Z_i^2}{Z_i(\omega_2 - \omega_1)} \tag{5.52}$$

$$C = \frac{2Z_i(\omega_2 - \omega_1)}{\omega_1\omega_2(Z_r^2 + Z_i^2)} \tag{5.53}$$

5.2.4 Simulation and Measured Results

For verification of the above design, parameters are chosen as: $f_1 = 1$ GHz, $f_2 = 2$ GHz, $m = 2$, $k = \sqrt{2}$, $Z_0 = 50\ \Omega$. Using (5.34) and (5.35) electrical lengths of the transmission lines are: $\theta_1 = \pi/3$ at f_1 and $\theta_2 = 2\pi/3$ at f_2. Using design equations, design parameters are obtained as: $Z_1 \approx 31\ \Omega$, $Z_2 \approx 62\ \Omega$, $Z_3 \approx 56\ \Omega$, $Z_4 \approx 39\ \Omega$, $Z_5 \approx 55\ \Omega$, $Z_e \approx 90\ \Omega$, $Z_e^{'} \approx 45\ \Omega$. In coupled line design, generally odd-mode impedance is less than even-mode impedance. Z_{od} and $Z_{od}^{'}$ is chosen 56 Ω and 36 Ω, respectively. Lumped parameters obtained using (5.51)-(5.53) are given as: $R \approx 87\Omega$, $C \approx 1$ pF, $L \approx 21$ nH.

The circuit is fabricated on a FR-4 substrate with dielectric constant of 4.4 and a thickness of 1.6 mm. Measurement setup is shown in Fig. 5.14. Comparison of simulation and measured results of the proposed power divider are shown in Figs. 5.15-5.16 and Table 5.1.

Figure 5.14: Setup for isolation measurement.

From the results presented in Figs. 5.15-5.16 and Table 5.1, it can be seen that dual-band arbitrary (1 : 2) power division is achieved which validates the theoretical design. There are some differences between the simulated and measured results which may be attributed to the inaccuracies in fabrication and measurements which are carried out using in-house laboratory facilities. Nevertheless, the measured results validate the theoretical approach based on which the dual-band arbitrary power divider is designed.

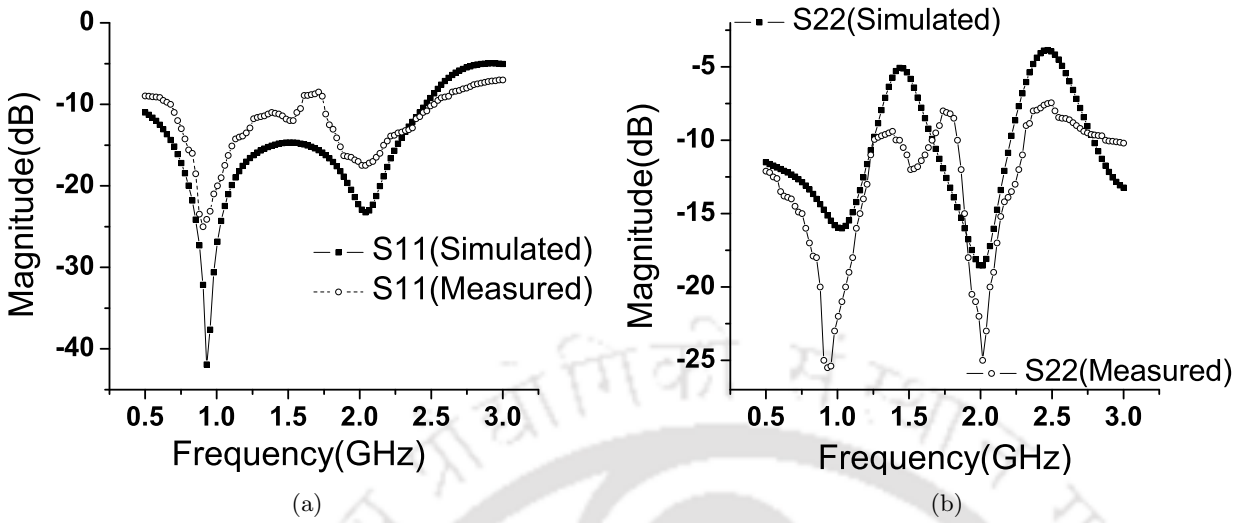


Figure 5.15: (a) Comparison of simulated and measured results of $|S_{11}|$. (b) Comparison of simulated and measured results of $|S_{22}|$.

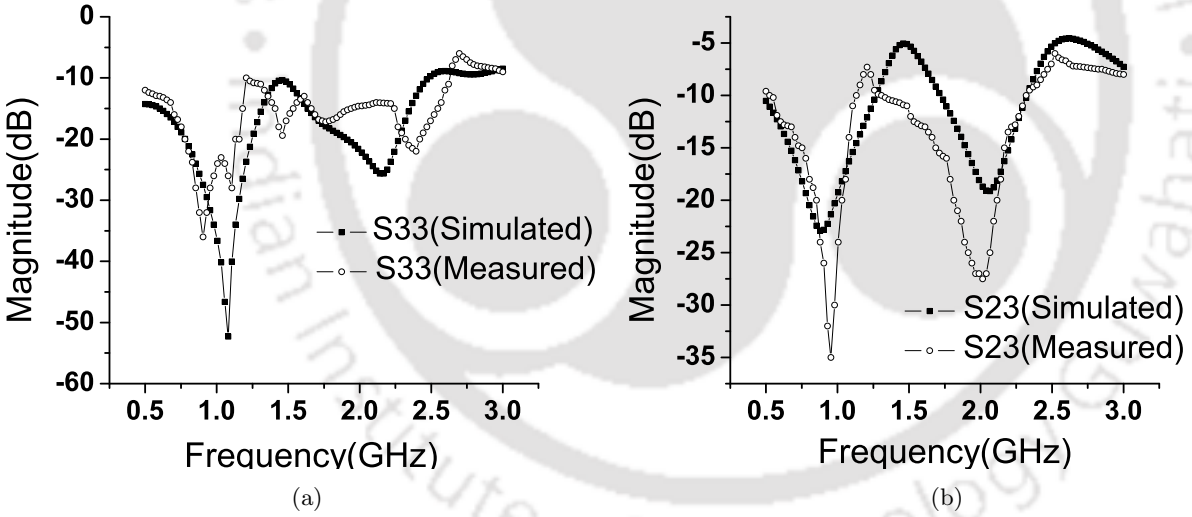


Figure 5.16: (a) Comparison of simulated and measured results of $|S_{33}|$. (b) Comparison of simulated and measured results of $|S_{23}|$.

5.3 Conclusion

In this chapter, two dual-band power dividers are presented. The first one is of BTU type equal power divider and the second one is of single-ended arbitrary power divider. For both power dividers, complete theoretical analysis is presented. Design equations are derived, prototypes are fabricated

Table 5.1: Comparison of simulated and measured results of $(|S_{31}| - |S_{21}|)$(dB).

Freq(GHz)	Simulated $(|S_{31}| - |S_{21}|)$(dB)	Measured $(|S_{31}| - |S_{21}|)$(dB)
0.8	2.4	2.2
0.9	2.6	2.7
1.0	2.7	2.5
1.1	2.6	2.6
1.2	2.4	2.2
1.8	2.4	2.4
1.9	2.6	2.8
2.0	2.8	2.8
2.1	3.0	2.9
2.2	3.7	3.5

and measurements are performed. The simulation and measured results for both the power dividers are in good agreement.

6

Conclusion and Future Work

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6.1 Conclusion

In this thesis, several types of balanced-to-unbalanced (BTU), unbalanced-to-balanced (UTB) and one single-ended power dividers are designed and analyzed. In the first chapter, basic theory related to power divider is presented. In the second chapter, mixed-mode scattering parameters and literature review related to our work are presented.

In the third chapter, five BTU power dividers are presented. First Gysel and Wilkinson type out-of-phase equal power dividers are presented. Because of the symmetrical nature of the circuit, out-of-phase power dividers are analyzed using even and odd-mode analysis. One Gysel type in-phase equal power divider is also presented. Two Gysel type power dividers for arbitrary power division are also presented. One is for out-of-phase and other is for in-phase applications. Equal power divider is a special case of the arbitrary power divider. To reduce the size of in-phase power divider, two parallel coupled short circuited lines are used. BTU power dividers presented in third chapter are simulated and optimized using HFSS. All BTU power dividers are fabricated using FR-4 substrate and measured using two port VNA. Simulation and measured results of all the power dividers are in good agreement. Performance comparisons of proposed power dividers with the reported power dividers are mentioned in Table 3.1. Designing of arbitrary and equal power divider for in-phase and out-of-phase applications, which can be used for power division from balanced amplifier to several single-ended antennas, is the major contribution of this chapter.

In the fourth chapter, two Gysel type UTB power dividers are presented. First one is for equal power division and the second one is for arbitrary power division. Both power dividers designed for in-phase applications. Design equations are obtained analytically and verified by theoretical and simulation results. Both UTB power dividers are simulated and optimized using HFSS. The FR-4 substrate has been used to fabricate UTB power dividers. Measurement results of fabricated prototype are in good agreement with simulation results. Performance comparisons of proposed power dividers with the reported power dividers are mentioned in Table 4.1. The major contribution of this chapter's work is to implement an arbitrary and equal power divider which can be used in feeding of balanced antenna array system from an unbalanced source.

In the fifth chapter, two dual-band power divider are presented. First one is a dual-band BTU power divider for equal power division and the second one is a coupled line based single-ended power

divider for arbitrary power division. Both dual-band power dividers are analyzed analytically and design equations have been derived. Simulation and measured results validate the design methods of both dual-band power dividers.

For each power divider, complete theoretical analysis has been carried out to derive the design equations. Based on the design equations, different power dividers have been designed and fabricated. All BTU and UTB power dividers are having the characteristic of balanced circuit which reduces the common-mode noise and easily able to connect with conventional single-ended devices. Based on the design equations, the proposed power dividers can be designed for any frequency application. The objective of this thesis is to find out design equations for different types of balanced-to-unbalanced and unbalanced-to-balanced power dividers. For implementations of each single-band power divider, 2 GHz design frequency has been selected because of the available resources for fabrication and measurement. The design frequency can be change depending on the different applications.

6.2 Future Work

Several types of power dividers are presented in this thesis. However, scope exists to extend these works in different directions which are briefly outline below.

(i) In a communication system, generally power divider is followed by a filter, therefore filter integrated power divider can be used instead of power divider followed by the filter. This makes the power divider, multi-functional. Therefore, filtering BTU and UTB types power dividers can be analyzed in the future.

(ii) The proposed dual-band power dividers are not having the property of independent controllable bandwidth. This characteristic of dual-band nature can be explored in the future. Further, multi-band version of the UTB type power divider can be a possible extension of the present work.

(iii) A lot of emphasis is now given to reduce the size of the circuits. The size of the presented power dividers can also be reduced by using several miniaturization techniques. Therefore, compact BTU and UTB power dividers can be analyzed in the future. As mentioned in the section 4.3, limitation of bandwidth and size of UTB power dividers can be resolved and implemented in the future.

A

Wilkinson Equal Power Divider

Contents

A.1 Even-Mode Analysis 132

A.2 Odd-Mode Analysis 133

The detail derivation of design equations of basic Wilkinson equal power divider is derived here. The derivation is based on the even- and odd-mode analysis. In this analysis, circuit is exited with even- and odd-modes. In this analysis, equivalent circuit is analyzed and design equations are derived.

A.1 Even-Mode Analysis

The block diagram of Wilkinson equal power divider shown in Fig. 1.4 can be redrawn as shown in Fig. A.1. Z_0 is the port impedance, V_{g1} and V_{g2} are two sources connected to ports 2 & 3 respectively, as shown in Fig. A.1.

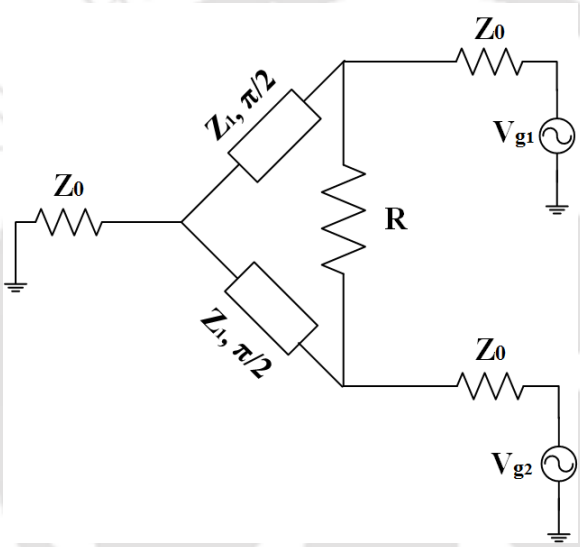

Figure A.1: Wilkinson equal power divider.

In even-mode excitation, circuit is excited with two equal and same phase sources. In this case, $V_{g1} = V_{g2} = V_0$. Under this excitation, electric fields have even symmetry about the centerline, no current flows into the isolation resistor R. Since the circuit is symmetrical, the circuit can be divided into two parts and analysis can be done using only half part of the circuit. Half part of the circuit is shown in the Fig. A.2.

Using quarter-wave transformer property, Z_1 can be obtained as:

$$Z_1 = \sqrt{2Z_0Z_0} \tag{A.1}$$

$$Z_1 = \sqrt{2}Z_0 \tag{A.2}$$

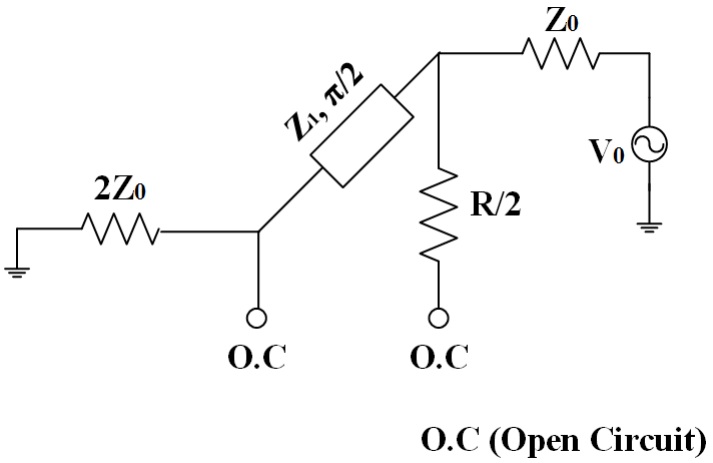

Figure A.2: Even-mode equivalent circuit.

A.2 Odd-Mode Analysis

In odd-mode excitation, circuit is excited with two equal and opposite phase sources. In this case, $V_{g1} = -V_{g2} = V_0$. Under this excitation, the electric fields have odd symmetry about the centerline, voltage null exists on the symmetrical plane. The equivalent circuit under this analysis is shown in Fig. A.3.

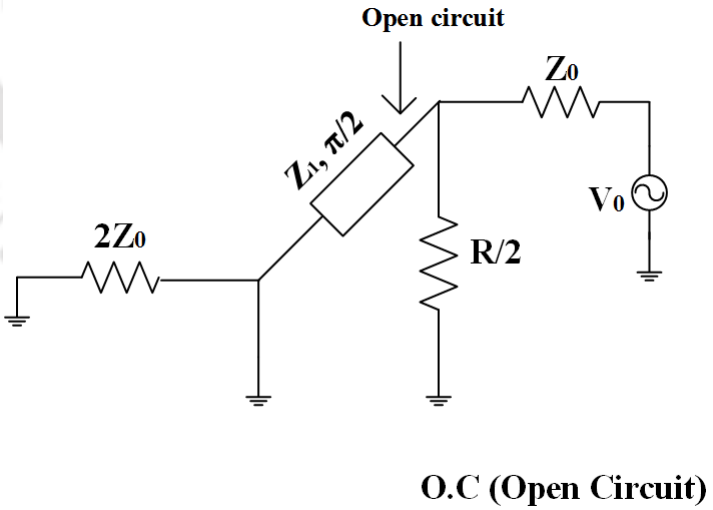

Figure A.3: Odd-mode equivalent circuit.

As shown in Fig. A.3, one end of quarter-wave transmission line is short circuited, therefore the other end of the transmission line become open circuited. From Fig. A.3, isolation resistor R can be

obtained as:

$$\frac{R}{2} = Z_0 \quad \text{(A.3)}$$

$$R = 2Z_0 \quad \text{(A.4)}$$

For equal power divider, (A.2) and (A.4) are the design equations.

B

Wilkinson Arbitrary Power Divider

Contents

B.1 Power Transmission from Input Port to Output Ports 136

B.2 Isolation Analysis 138

The basic Wilkinson arbitrary power divider described in chapter 1. The block diagram is shown in Fig. 1.5. The detailed derivation of design equations are given here. The design equations are derived in two parts. First one is ideal power transmission from input port to two output ports. In this case no power is dissipated in isolation resistor. Second part is the isolation analysis. In this case, both the output ports are to be isolated.

B.1 Power Transmission from Input Port to Output Ports

Under the ideal condition, when input port is excited, no power should be dissipated in isolation resistor [16,20]. All the power should be divided in two output ports according to power division ratio. Under this analysis, equivalent circuit of Fig. 1.5 is shown in Fig. B.1. Let the power division ratio

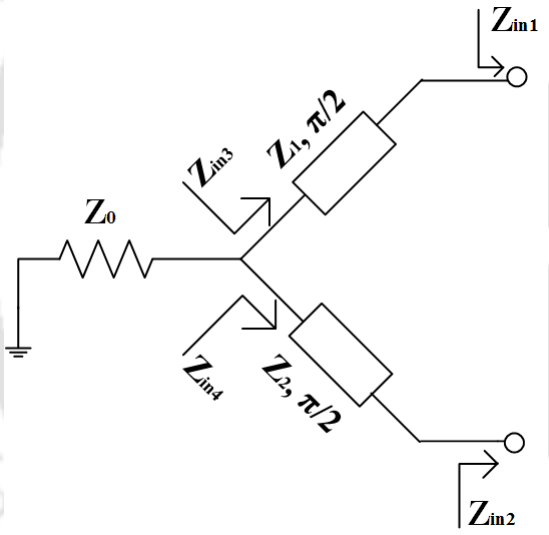

Figure B.1: Equivalent circuit under power transmission from input port to outports.

is k^2. Therefore, power at ports 2 and 3 can be written as:

$$\frac{P_3}{P_2} = k^2 \tag{B.1}$$

$$P_3 = k^2 P_2 \tag{B.2}$$

If the power division ratio between ports 2 and 3 is k^2, then from Fig. B.1, Z_{in1}, Z_{in2}, Z_{in3} and Z_{in4} can be related as:

$$Z_{in1} = k^2 Z_{in2} \tag{B.3}$$

$$Z_{in3} = k^2 Z_{in4} \tag{B.4}$$

To satisfy (B.3), Z_{in1} and Z_{in2} can be assumed as:

$$Z_{in1} = Z_0 k \tag{B.5}$$

$$Z_{in2} = \frac{Z_0}{k} \tag{B.6}$$

From Fig. B.1, the parallel combination of Z_{in3} and Z_{in4} is equal to the port impedance Z_0.

$$Z_{in3} || Z_{in4} = Z_0 \tag{B.7}$$

Simplifying (B.7), Z_{in3} and Z_{in4} can be related as:

$$Z_{in3} = \frac{Z_0 Z_{in4}}{Z_{in4} - Z_0} \tag{B.8}$$

Using (B.4) and (B.8), Z_{in3} and Z_{in4} are obtained as:

$$Z_{in3} = Z_0 \left(1 + k^2\right) \tag{B.9}$$

$$Z_{in4} = Z_0 \frac{\left(1 + k^2\right)}{k^2} \tag{B.10}$$

From Fig. B.1, using quarter-wave transformer property, Z_{in3}, Z_{in1} and Z_{in4}, Z_{in2} are related as:

$$Z_{in3} = \frac{Z_1^2}{Z_{in1}} = \frac{Z_1^2}{Z_0 k} \tag{B.11}$$

$$Z_{in4} = \frac{Z_2^2}{Z_{in2}} = \frac{Z_2^2 k}{Z_0} \tag{B.12}$$

Using (B.9), (B.10), (B.11) and (B.12), Z_1 and Z_2 are obtained as:

$$Z_1 = Z_0\sqrt{k\left(1+k^2\right)} \tag{B.13}$$

$$Z_2 = Z_0\sqrt{\frac{1+k^2}{k^3}} \tag{B.14}$$

B.2 Isolation Analysis

Under this analysis, when port 2 is excited, no power should flow to port 3. This happens when port 3 is short circuited [16, 20]. Under this analysis equivalent circuit of Fig. 1.5 is shown in Fig. B.2. If port 3 is short circuited, then using quarter-wave transformer property of transmission line of characteristic impedance Z_2, the other end of this line become open circuited, as shown in Fig. B.2

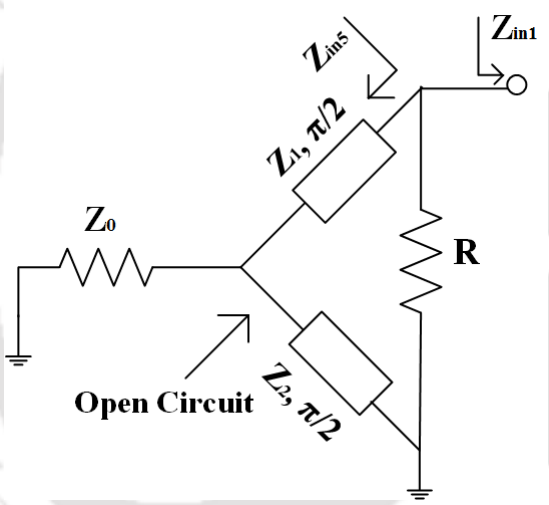

Figure B.2: Equivalent circuit under isolation analysis.

From Fig. B.2, using quarter wave transformer property Z_{in5} can be written as:

$$Z_{in5} = \frac{Z_1^2}{Z_0} \tag{B.15}$$

Using (B.13) and (B.15), Z_{in5} can be written as:

$$Z_{in5} = Z_0 k\left(1+k^2\right) \tag{B.16}$$

From Fig. B.2, the parallel combination of Z_{in5} and R is equal to Z_{in1}.

$$Z_{in5}||R = Z_{in1} \tag{B.17}$$

Using (B.5), (B.16) and (B.17), isolation resistor R is obtained as:

$$R = Z_0\left(k + \frac{1}{k}\right) \tag{B.18}$$

As shown in Fig. 1.4, Z_3 and Z_4 can be obtained using output matching. In a transmission line of characteristic impedance Z_3, Z_{in1} is to be matched with Z_0 (port 2 impedance) and for transmission line of characteristic impedance Z_4, Z_{in2} is to be matched with Z_0 (port 3 impedance).

$$Z_3 = \sqrt{Z_{in1}Z_0} \tag{B.19}$$

$$Z_4 = \sqrt{Z_{in2}Z_0} \tag{B.20}$$

Using (B.5), (B.6), (B.19) and (B.20), Z_3 and Z_4 are obtained as:

$$Z_3 = Z_0\sqrt{k} \tag{B.21}$$

$$Z_4 = \frac{Z_0}{\sqrt{k}} \tag{B.22}$$

For Wilkinson arbitrary power divider, (B.13), (B.14), (B.18), (B.21) and (B.22) are the design equations.

C

Transformation between Scattering and Transmission Parameters

Contents

C.1 Parameter Conversion 142

To derive design equations for BTU and UTB power dividers as described in chapter 3, 4 and 5, conversion between scattering and transmission parameters are required. Here, mathematical transformations are derived which are used to convert transmission parameters into scattering parameters.

C.1 Parameter Conversion

A two-port network is shown in Fig. C.1. At port 1, voltage and currents are V_1 and I_1, respectively. Similarly, at port 2, voltage and currents are V_2 and I_2, respectively. For this two-port network,

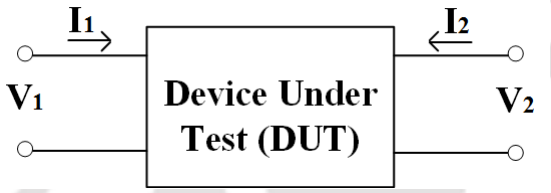

Figure C.1: Two port network.

transmission parameters are defined as:

$$V_1 = AV_2 - BI_2 \tag{C.1}$$

$$V_2 = CV_2 - DI_2 \tag{C.2}$$

where, A, B, C and D are the transmission parameters. For any port, voltage and currents can be defined as [3]:

$$V_n = V_n^+ + V_n^- \tag{C.3}$$

$$I_n = \frac{V_n^+ - V_n^-}{Z_0} \tag{C.4}$$

where, $n = 1, 2$. Scattering parameters for two-port network are defined as [3]:

$$V_1^- = S_{11}V_1^+ + S_{12}V_2^+ \tag{C.5}$$

$$V_2^- = S_{21}V_1^+ + S_{22}V_2^+ \tag{C.6}$$

where, S_{11}, S_{12}, S_{21} and S_{22} are the scattering parameters of two-port network. Using (C.3) and (C.4), (C.1) and (C.2) can be written as:

$$V_1^+ + V_1^- = A\left(V_2^+ + V_2^-\right) - B\frac{\left(V_2^+ - V_2^-\right)}{Z_0} \tag{C.7}$$

$$V_1^+ - V_1^- = C\left(V_2^+ + V_2^-\right) Z_0 - D\left(V_2^+ - V_2^-\right) \tag{C.8}$$

From (C.5) and (C.6), S_{11} and S_{21} are defined as [3]:

$$S_{11} = \left.\frac{V_1^-}{V_1^+}\right|_{V_2^+=0} \tag{C.9}$$

$$S_{21} = \left.\frac{V_2^-}{V_1^+}\right|_{V_2^+=0} \tag{C.10}$$

Putting $V_2^+ = 0$ in (C.7) and (C.8), both equations can be written as:

$$V_1^+ + V_1^- = \left(A + \frac{B}{Z_0}\right) V_2^- \tag{C.11}$$

$$V_1^+ - V_1^- = \left(CZ_0 + D\right) V_2^- \tag{C.12}$$

Putting V_2^- from (C.12) into (C.11), (C.11) can be written as:

$$V_1^+ + V_1^- = A + \frac{A + \frac{B}{Z_0}}{CZ_0 + D}(V_1^+ - V_1^-) \tag{C.13}$$

From (C.13), S_{11} is obtained as:

$$S_{11} = \left.\frac{V_1^-}{V_1^+}\right|_{V_2^+=0} = \frac{A + \frac{B}{Z_0} - CZ_0 - D}{A + \frac{B}{Z_0} + CZ_0 + D} \tag{C.14}$$

Putting V_1^- from (C.12) into (C.11), (C.11) can be written as:

$$2V_1^+ = \left(A + \frac{B}{Z_0} + CZ_0 + D\right) \tag{C.15}$$

From (C.16), S_{21} is obtained as:

$$S_{21} = \left.\frac{V_2^-}{V_1^+}\right|_{V_2^+=0} = \frac{2}{A + \frac{B}{Z_0} + CZ_0 + D} \tag{C.16}$$

From (C.5) and (C.6), S_{22} and S_{12} are defined as [3]:

$$S_{22} = \left.\frac{V_2^-}{V_2^+}\right|_{V_1^+=0} \tag{C.17}$$

$$S_{12} = \left.\frac{V_1^-}{V_2^+}\right|_{V_1^+=0} \tag{C.18}$$

Putting $V_1^+ = 0$ in (C.7) and (C.8), both equations can be written as:

$$+V_1^- = \left(A - \frac{B}{Z_0}\right) V_2^+ + \left(A + \frac{B}{Z_0}\right) V_2^- \tag{C.19}$$

$$-V_1^- = (CZ_0 - D)\, V_2^+ + (CZ_0 + D)\, V_2^- \tag{C.20}$$

Putting V_1^- from (C.20) into (C.19), (C.19) can be written as:

$$\left(A - \frac{B}{Z_0} + CZ_0 - D\right) V_2^+ + \left(A + \frac{B}{Z_0} + CZ_0 + D\right) V_2^- = 0 \tag{C.21}$$

From (C.21), S_{22} is obtained as:

$$S_{22} = \left.\frac{V_2^-}{V_2^+}\right|_{V_1^+=0} = \frac{-A + \frac{B}{Z_0} - CZ_0 + D}{A + \frac{B}{Z_0} + CZ_0 + D} \tag{C.22}$$

Eliminating V_2^- from (C.19) and (C.20), S_{12} is obtained as:

$$S_{12} = \left.\frac{V_1^-}{V_2^+}\right|_{V_1^+=0} = \frac{2\,(AD - BC)}{A + \frac{B}{Z_0} + CZ_0 + D} \tag{C.23}$$

(C.14), (C.16), (C.22) and (C.23) are the mathematical transformations used to convert transmission parameters into scattering parameters.

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