



INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI
SHORT ABSTRACT OF THESIS

Name of the Student : SURYA PRAKASH MATCHA
Roll Number : 09610218
Programme of Study : Ph.D.
Thesis Title: HIGH PERFORMANCE ARCHITECTURES FOR ADAPTIVE
EQUALIZERS USING DISTRIBUTED ARITHMETIC
Name of Thesis Supervisor(s) : Dr. SHAIK RAFI AHAMED
Thesis Submitted to the Department/ Center : ELECTRONICS AND ELECTRINCAL ENGINEERING
Date of completion of Thesis Viva-Voce Exam : 24-09-2016
Key words for description of Thesis Work : ADAPTIVE FILTER, DECISION FEEDBACK EQUALIZER,
DISTRIBUTED ARITHMETIC, LEAST-MEAN SQUARES ALGORITHM.

SHORT ABSTRACT

In communications, adaptive decision feedback equalizers (ADFEs) are an effective means of countering the intersymbol interference (ISI) introduced by the channel and also to keep track on the changes in the channel characteristics. However, high speed applications demand for a large number of taps in the feed forward filter (FFF) and feedback filter (FBF) of ADFE and hence the implementation and real-time operation of such an equalizer becomes difficult due to increased complexity and very small intersymbol period. This thesis focuses on the implementation of adaptive equalizers based on the design aspect of distributed arithmetic (DA) since DA based realization of DSP algorithms can lead to low computational cost while achieving high system throughputs. Further, the modular and memory-based structure of DA can lead to the resultant equalizers in enjoying the advantages of ease of implementation making them more suitable for implementing on field-programmable-gate-arrays (FPGAs) and the design of applications specific integrated circuits (ASICs).