



INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI
SHORT ABSTRACT OF THESIS

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Programme of Study : **Ph.D.**

Thesis Title: **Test Pattern Generation and Fault Localization for Some Fault Models in Reversible Circuits**

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SHORT ABSTRACT

In this thesis, we consider some of the fault models to generate the test patterns to detect these faults in reversible circuits. In the first phase of our work, we consider the bridging faults at the input level. We identify a test set to detect all possible input bridging faults in a reversible circuit and establish that the test set is minimal and complete. It is also indicated that by adding one particular test vector to this test set, input stuck-at fault can also be detected.

In the next work, we consider intra-level bridging faults, i.e., single and multiple bridging faults that may occur at any level of the reversible circuits. The concept of path-level expression is introduced in this work to generate the test set to detect all possible intra-level bridging faults. It is also established that the generated test set is complete and minimal. Stuck-at and bridging fault models are also used in conventional digital circuits to detect faults.

There are some special fault models, which are applicable for reversible circuits only. One such fault model is the missing gate fault model and in the third work we consider the missing gate fault model. We propose a method to generate the test set to detect single missing gate faults in a reversible circuit. Next, we enhance the test set to detect multiple missing gate faults. The generated test set is not a minimal one, so we use Integer Linear Programming (ILP) techniques to find the minimal test set. It is also established that the generated test set is complete. In this work, a correlation of other fault models is shown with missing gate fault model.

Since the missing gate fault model is specific to reversible circuits, so in our last work, we propose a method to locate the missing gate faults in reversible circuits. The test set generated to detect the missing gate faults is used to construct a fault localization tree and with the help of fault location tree, a method is proposed to locate the fault positions of missing gate faults.