Reliability Enhancements in AlGaN/GaN HEMTs through Gate Shaping

A

Thesis submitted

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By

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This is to certify that this thesis entitled **"Reliability Enhancements in AlGaN/GaN HEMTs through Gate Shaping"** being submitted by Mr. Ashok Kumar Ray to the Department of Electronics and Electrical Engineering, Indian Institute of Technology Guwahati, is a record of bonafide research work under our supervision and is worthy of consideration for the award of the degree of Doctor of Philosophy of the Institute.

The results contained in this thesis have not been submitted in part or full to any other university or institute for the award of any degree or diploma.

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Dedicated

To

Maai, Babuji

Sangita

Akshansh and Vedant

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Abstract

With the rapid industrialization, there is a huge demand for electricity to cater the needs of ever expanding industry and in every walks of life. Thus, managing the utilization of electricity is of utmost importance. With the growth of semiconductor market and emergence of newer semiconductor materials, the ancestry of devices have changed from Silicon to Wide Bandgap (WBG) based semiconductors. Gallium Nitride (GaN), a WBG semiconductor has emerged as the next generation material for semiconductor device applications. Device operation at high frequency with elevated power is simultaneously possible using GaN technology. A High Electron Mobility Transistor (HEMT) is designed using an AlGaN/GaN heterostructure and has proved to have great potential both in high power and Radio Frequency (RF) applications.

The performance of a device directly affects its demand. Existing capability and reliability of the devices can be improved by the use of newer structure and design approaches. Technology Computer Aided Design (TCAD) aids engineers to improve and design newer devices, and to understand the internal phenomenon, thus, improving its capabilities.

An AlGaN/GaN HEMTs have been chosen to understand reliability issues that are being currently faced by it in the high power applications. In this thesis, a detailed numerical study is performed to observe the impact of gate shaping (filleting) and the use of an elevated substrate pillar on the performance of an AlGaN/GaN HEMT. It is observed that the converse piezoelectric strain in the AlGaN barrier layer, electron and lattice temperatures get suppressed due to filleting of the gate geometry. To substantiate, a comparison is presented be-

tween field plate rectangular gate HEMTs and filleted gate HEMT with and without field plate. In case of HEMTs without field plate, filleted gate has 44 % lower converse piezoelectric strain than the conventional HEMT. For filleted gate HEMTs with and without field plate, the electric field and converse piezoelectric strain is lower by 38% and 30%, respectively, as compared to rectangular gate HEMT with a field plate. With the increase in filleting radius, the gate leakage current reduced by two orders of the magnitude as compared to a conventional HEMT. The reduction in OFF state converse piezoelectric strain and electron temperature are observed due to filleting, which enhances OFF state reliability. Gate shaping and elevated substrate pillar in HEMTs are able to reduce operational temperature by 4 and 19 K, respectively. Analysis presented in this thesis concludes that filleted gate and elevated substrate pillar can help to improve the reliability of HEMTs.

Keywords: AlGaN/GaN HEMT, Converse piezoelectric strain, Electric field, Electron temperature, Elevated substrate pillar, Gate geometry, Joule heating, TCAD.

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List of Acronyms

2D	2 Dimension
3D	3 Dimension
2DEG	2 Dimensional Electron Gas
2DHG	2 Dimensional Hole Gas
Al	Aluminium
AlN	Aluminium Nitride
AlGaAs	Aluminium Gallium Arsenide
AlGaN	Aluminium Gallium Nitride
Au	Gold
BARITT	Barrier Injected Transit-Time
BFOM	Baliga Figure of Merit
BHFFOM	Baliga High Freq. FOM
BJT	Bipolar Junction Transistor
BTE	Boltzmann's Transport Equation
CMOS	Complementary Metal Oxide Semiconductor
CPE	Converse Peizoelectric
Cu	Copper
DC	Direct Current
DD	Drift-Diffusion
EL	Electroluminescence
E-Mode	Enhancement Mode
ET	Electro-Thermodynamics

eTemp.	Electron Temperature
FDM	Finite Difference Method
FDTD	Finite Difference Time Domain
Fe	Iron
FEM	Finite Element Method
FET	Field Effect Transistor
FG	Filleted Gate
FP	Field Plate
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GUI	Graphical User Interface
HEMT	High Electron Mobility Transistor
HFET	Heterojunction Field Effect Transistor
HD	Hydrodynamics
InAlGaN	Indium Aluminium Gallium Nitride
IR	Infrared
I-V	Current Voltage
IMPATT	Impact Ionization Avalanche Transit-Time
LED	Light Emitting Diode
MC	Monte Carlo
MESFET	Metal Semiconductor Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NC	Nanocrystalline
NDC	Negative Differential Output Conductance
Ni	Nickel
NiO	Nickel Oxide
PDE	Partial Differential Equation
PF	Poole-Frenkel

RADAR	Radio Detection and Ranging
RF	Radio Frequency
RCA	Radio Corporation of America
RG	Rectangular Gate
SiC	Silicon Carbide
SiO_2	Silicon-dioxide
TCL	Tool Command Language
TCAD	Technology Computer Aided Design
Ti	Titanium
TRAPATT	Trapped Plasma Avalanche Triggered Transit
T_{MAX}	Maximum Channel Temperature
WBG	Wide Bandgap

List of Symbols

Δ	Penetration of the conduction band edge below the Fermi level
ΔE_C	Conduction band offset
Γ	Direct conduction band
ϵ_0	Permittivity of air/vacuum
ϵ_r	Relative dielectric constant
ϵ_{ik}	Strain
Θ	Temperature
σ	Polarization induced charge
σ_{ik}	Stress
Φ_b	Barrier height
Φ_n	Electron quasi-fermi potential
Φ_p	Hole quasi-fermi potential
μ	Mobility
Ω_0	Volume occupied by a single dipole
$a(0)$	Lattice constants of an unstrained GaN
$a(x)$	Lattice constants of strained $Al_xGa_{1-x}N$ layer
C_{ij}	Elastic constant
c_L	Lattice heat capacity
D	Electric displacement vector
D_n	Electron diffusivity
D_p	Hole diffusivity
d	Piezoelectric moduli

e	Electronic charge
E	Electric field
E_0	Lowest subband level of the 2DEG
E_C	Conduction band edge
E_V	Valence band edge
E_F	Fermi level
E_{Cr}	Critical field
$E_{F,n}$	quasi-Fermi energies for electrons
$E_{F,p}$	quasi-Fermi energies for holes
E_g	Energy bandgap
e_{ij}	Piezoelectric constants
f	Frequency
$\mathtt{g_m}$	Transconductance
G^{opt}	Optical generation rate
H	Enthalpy
$\hbar$	Dirac constant
J_n	Electron current density
J_p	Hole current density
k_t	Thermal conductivity
k	Boltzmann's constant
L	Indirect conduction band
L_D	Length of the drain access region
L_G	Gate length
L_{GD}	Gate drain spacing
m_n	Electron effective mass
m_p	Hole effective mass
N_s	Carrier density of 2DEG
P_n	Absolute thermoelectric power of electrons

P_p	Absolute thermoelectric power of holes
$\overrightarrow{P}$	Total dipole moment per unit volume
P	Polarization
P_{PZ}	Piezoelectric polarization
P_{SP}	Spontaneous polarization
p	Dipole moment
Q_{gen}	Heat generated
S	Entropy
T	Temperature
U	Internal energy
V_{BV}	Breakdown voltage
V_{th}	Threshold voltage
V_{DS}	Drain source voltage
V_{GS}	Gate source voltage
R_{CH}	Channel resistance
R_D	Drift region resistance
R_{ON}	ON resistance
$R_{net,n}$	Electron recombination rate
$R_{net,p}$	Hole recombination rate
T	Temperature
W_G	Gate width

1

Introduction

Contents

1.1 Background

The first patent on field-effect transistor like device "Method and Apparatus for Controlling Electric Currents" was filed by Julius Edgar Lilienfeld in 1926. His idea was implemented by M. M. (John) Atalla and Dawon Kahng of Bell Labs when they developed the first successful insulated gate Field Effect Transistor (FET) in 1959. Kahng vouched for its ease of fabrication and the possibility of it being implemented in integrated circuit technology. After some initial hiccups, 16-transistor integrated device was demonstrated by Radio Corporation of America (RCA). Most of the success story of Silicon has to be credited to the popularity of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). Researchers have been working hard to invent ingenious approaches to satisfy the fundamental laws of semiconductor physics just to continue scaling and keep Silicon alive.

Success of Silicon has been challenged by the emergence of High Electron Mobility Transistors (HEMTs) using Wide Bandgap (WBG) semiconductor material, first among them being the Aluminium Gallium Arsenide/Gallium Arsenide (AlGaAs/GaAs) HEMTs. Takashi Mimura and his colleagues at Fujitsu Laboratories Ltd., developed the first AlGaAs/GaAs based HEMT in December, 1979. They employed modulation-doped heterojunction with a Schottky gate contact to confine the carriers (electrons) in the GaAs [12]. It is to mention that HEMTs work on the same underlying principle of confining electrons in a narrow channel.

In the year 1985, using the GaAs-HEMT amplifier, the Nobeyama Radio Observatory of Japan, for the first time reported the discovery of a hydrocarbon molecule unknown to humanity in a dark space. It was only possible for the low noise amplification capability of the HEMT, which the contemporary devices lacked. The technology was bound to progress as it matured quickly and found a market within five years of its invention. Due to the high gain of these amplifiers, the parabolic antenna size could be reduced to half and they revolutionized the electronic communication systems.

In the past decade, Gallium Nitride (GaN) has emerged as a promising alternative to

GaAs-HEMTs. Gallium Nitride has a bandgap of 3.49 eV as compared to 1.42 eV for GaAs [13]. This large bandgap enables fabricating devices with high breakdown field, resilience and immunity to radiation. A breakdown field of 3300 kV/cm has been reported [14] for GaN. Polarization fields in AlGaN/GaN HEMTs are five times higher as compared to GaAs HEMTs, resulting in carrier densities well above 10^{13}cm^{-2} [14]. It is to mention that there is no need for a modulation doped barrier layer in Gallium Nitride High Electron Mobility Transistors (GaN-HEMTs) which was required in GaAs based HEMTs. Due to these advantages, record power densities up to 40 Wmm^{-1} [15, 16] have been obtained. GaN-HEMTs have better linearity, capability to handle large load impedance, high breakdown voltage, high power density, high efficiency, safe operation at high temperature, etc. Silicon may be the winner at low power but GaN-HEMTs have proven their capability in military RADARs, where stringent norms are applied.

1.2 Reliability Issues in AlGaN/GaN HEMTs

GaN-HEMTs are one of the few such devices whose advertised performance matches with the actual circuit performance. However, temperature and electric field are known to play key roles in its degradation. The presence of a strong electric field and high temperature in any critical device region accelerates its degradation and adversely impact the reliability. Hence, for the development of successful commercial, defence or space applications of GaN devices, the device designers must develop methodologies to improve their long term reliability [17–21] and mitigate the effect of traps, current collapse [22, 23], parasitic and deep level effects [24], requirement of rugged gate supply circuitry [25, 26], etc. Since the GaN devices are making their presence globally, the need for enhancing the reliability is gaining importance every year.

One of the critical reliability issues in AlGaN/GaN HEMTs is the generation of converse piezoelectric (CPE) strain in AlGaN barrier layer. During the OFF state operation, rectangular gated HEMTs suffer from the presence of a high electric field at the gate edge on the drain side. This strong electric field under the gate gives rise to CPE strain in the

AlGaN barrier layer [17, 27]. Due to this strain, when the stored elastic energy inside the AlGaN barrier layer increases significantly above a critical value, the AlGaN layer relaxes by forming crystallographic defects. These additional defects act as charge-trap centres in the AlGaN barrier layer [17, 28]. Furthermore, the presence of a strong electric field can fill these traps with electrons, thereby, lowering the 2-dimensional electron gas (2DEG) density and reducing the drain current during the HEMT ON state operation [29]. The CPE strain induced defects can also initiate a leakage path between the channel and gate increasing the gate leakage current [30]. In the worst case scenario, the CPE strain induced defects can also lead to the permanent failure of the HEMT [17, 29]. Figure 1.1 pictorially shows the most common issues that arise at the gate edge towards the drain side.

AlGaN/GaN HEMT suffers from a variety of degradation mechanisms. A few among them are initiated by electrons having a higher temperature, and these hot electrons are responsible for increasing the trap density beneath the gate [31] as well as in the gate-drain access region. It has been reported that electron energy is responsible for inciting a small negative differential output conductance (NDC), irrespective of the operational power in the device. This suggests that the electron temperature has a major role to play rather than the lattice temperature. This NDC has been ascribed to the capturing of hot electrons in bulk traps [31, 32].

Self-heating in GaN-HEMT results in the decrease of mobility and saturation velocity

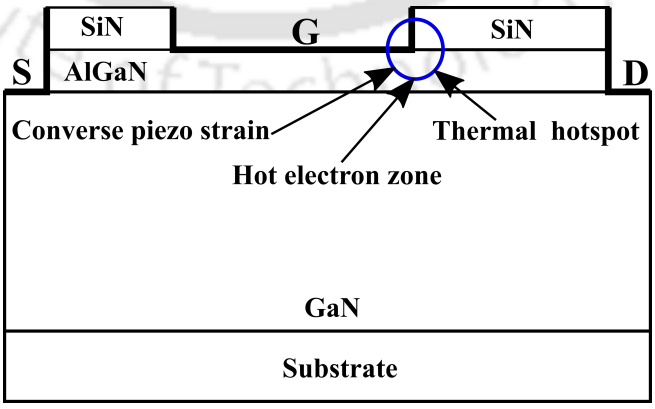

Figure 1.1: Common issues at the right gate edge towards the drain side of conventional AlGaN/GaN HEMT.

of electrons, causing significant performance degradation. Even, the failure rate of GaN-HEMTs is linked with peak temperature in the device. The failure of GaN-HEMTs can be caused by any of the several temperature and field dependent phenomena. However, it is generally accepted that temperature is likely to have a bearing on almost all such phenomena. Hence, to ensure a reliable operation and to mitigate the chances of time-dependent or catastrophic device failure, GaN-HEMTs are usually mandated to operate below "safe" levels of power, current as well as temperature. The maximum permissible channel temperature, T_{MAX} not only determines the maximum power delivering capability and expected life of the device, but it also plays a important role in the design of the heat sinks, device package, etc. [33]. Therefore, quantification of self-heating is vital for predicting device performance, assessing lifetime and reliability, and system design. Two out of the three parameters determining the device "safe" operation region, namely output power and current can be easily measured, but the determination of temperature distribution across the device [34] and identification of hot-spots is a difficult task.

1.3 Motivation

As discussed above, AlGaN/GaN HEMT faces a number of challenges as far as its reliability and stability is concerned. Some of the issues are listed below in these devices, which has motivated to undertake the present work reported in the thesis. In the thesis, a reliability enhancement approach by gate shaping of AlGaN/GaN HEMT is proposed which is validated by numerical simulations the proposed device structure. The motivation behind the proposed work is summarized below.

(i) The piezoelectric nature of AlGaN/GaN composite layered structure causes the devices to fail by generating additional strain through CPE in the presence of an electric field. In a HEMT very high electric field exists at the gate edge towards the drain side, this initiates the CPE. As CPE is directly proportional to field applied, hence, it is essential to tailor the electric field at the gate edge particularly on the drain side to improve device reliability.

(ii) Hot electrons are also a major concern as has been outlined in the prior art on AlGaN/GaN HEMT (refer Chapter 2 section 2.7). The primary cause again is the presence of a high electric field. Gate leakage, reduced breakdown voltage, distortion of transconductance and trapping of electrons are a few issues that occur due to the hot electrons.

(iii) Managing self-heating is a non-trivial and critical issue. Joule heating gets concentrated at the gate edge towards the drain side and it encourages other degradation mechanisms to quickly get into action, which might have been inactive in its absence. It is worth reiterating that the self-heating peaks up in the same region where electric field peaks. The Schottky contact which is responsible for controlling the device operation, has exhibited instability due to the self-heating. Gate metal interdiffusion has also been reported due to the self-heating.

1.4 Objectives

Based on the motivations identified, an attempt has been made to address the following objectives.

(i) To resolve the issue of a high vertical electric field, filleted gate shape HEMT is proposed to be used to perform the numerical analysis to understand its advantage in suppressing the electric field which leads to a lower CPE. It is also reported in the literature that field plates can be employed to reduce the electric field in the gate drain access region, hence, they are proposed to be used individually as well as in combination with filleted gate HEMT to observe the impact they have in reducing the electric field as well as mitigating CPE.

(ii) Similar approach of tailoring the vertical electric field by adopting a filleted gate establishes the need for experimentation to prove its suitability in mitigating the hot electron effects.

(iii) Considering the self-heating aspect, the use of filleted gate to control electric field in the proximity of the gate edge is anticipated to mitigate self-heating.

(iv) Innovative approaches for heat extraction from the active heat generating region of the device has been explored in the past. In the thesis, an elevated substrate pillar of Silicon Carbide (SiC) is proposed to be used underneath the gate so that a low thermal resistance path is provided for the heat to flow. It is anticipated that the SiC pillar structure due to its high thermal conductivity might increase the heat flux, which would reduce the channel temperature. A comparison between standard structure (without elevated substrate pillar) and the proposed structure is aimed to be performed for establishing efficacy of the proposed method (refer Fig. 6.4 in Chapter 6).

1.5 Thesis Outline

The report is organized as follow:

- **Chapter 2** illustrates detailed information about the material properties and comparison thereof, highlighting the advantages of GaN as a material meant for fabricating HEMTs. Formation of 2DEG, which is the critical part of AlGaN/GaN HEMTs, is presented. Later, in this Chapter, the working principle of HEMTs are explained. Finally, a review of various degradation and reliability issues being reported by other researchers on AlGaN/GaN HEMTs are depicted.

- **Chapter 3** discusses the simulation setup, tools used and the device design approach followed in the work. This Chapter also mentions the various considerations incorporated while designing the structure encompassing various physics based modelling strategies.

- **Chapter 4** describes the reliability issue due to converse piezoelectric phenomena in GaN devices. Converse piezoelectric strain inside the AlGaN barrier is one of the critical reliability issue in AlGaN/GaN HEMTs. In the OFF state, presence of a high

electric field at the gate edge towards the drain side creates CPE in the AlGaN barrier layer. Under the condition when the stored elastic energy inside the AlGaN barrier layer increases significantly above a critical value, defects are created. This Chapter outlines the CPE concern and an approach to resolve it.

- **Chapter 5** discusses the hot electron issues in HEMTs. These promote trapping, leading to an increase in leakage current and other associated ill effects. Hydrodynamic simulation has been employed to visualize the existence of hot electrons and to estimate the leakage current in the proposed device structure.

- **Chapter 6** presents the self-heating in an AlGaN/GaN HEMT. As a very high current flows in the channel of the HEMT, significant Joule heating occurs. This self-heating in association with the other degradation mechanism mentioned above leads to other associated degradations. Mechanisms to suppress self-heating it in AlGaN/GaN HEMTs has been discussed in this Chapter.

- **Chapter 7** presents the summary of the results obtained and future directions of the work presented in this thesis.

2

Fundamentals and Prior Art of AlGaN/GaN HEMT

Contents

2.1 Introduction

Gallium Nitride belongs to the III-V group and it occurs in two forms, wurtzite and zinc blende. Among these, wurtzite is more stable and it manifests strong polarization fields. It is the channel material for various heterojunction devices. It is a wide bandgap semiconductor and is a popular material having excellent physical properties making it a suitable candidate for the applications in the power electronics and Radio Frequency (RF) domains. Devices based on GaN have a reliable performance at elevated temperatures and are known to operate at very high switching speeds. Hence, these are the natural choice for power electronics applications as these have better power conversion efficiency, and are capable of reliable power distribution. Among the various advantages of using a wide bandgap semiconductor, the most important is the large reduction of chip area due to the drastic fall in gate width, which reduces power loss. The power density increases due to a decrease in the transistor size, hence, packaging needs improvement to dissipate the generated heat. While comparing the material properties of the popular semiconductors, it can be seen that GaN is a suitable material for high power and RF applications.

2.2 Material Considerations and Properties

Silicon has primarily dominated semiconductor development from the beginning. Silicon dioxide (SiO_2) appeared as a boon for Silicon as it is it's native oxide that could be grown by oxidizing Silicon and the interface between the two is excellent. Due to the development of semiconductor domain and the emergence of associated manufacturing accessories, the compound semiconductors surfaced. The first infra-red LED was invented by Robert Biard and Gary Pittman in 1961 using GaAs at Texas Instruments. Subsequently, in 1962, Nick Holonyak, Jr. invented the first LED that emitted visible red light using GaAs. The long awaited GaN based blue LED was invented by Shuji Nakamura along with Isamu Akasaki and Hiroshi Amano in 1993. Further, white light emitting LED was invented which revolu-

Table 2.1: Comparison of physical parameters of popular semiconductors [4].

Parameter (Units)	Si	GaAs	4H-SiC	GaN	AlN
Energy bandgap (eV)	1.12	1.42	3.23	3.39	6.2
Relative dielectric constant, (ϵ_r)	11.7	12.9	9.66	8.9	8.5
Breakdown electric field (MV/cm)	0.3	0.4	2.5	3.75	11.7
Saturated electron velocity (10^7cm/s)	1	2	1.9	2.5	1.4
Electron mobility at 300 K (cm^2/Vs)	1350	8500	900	1265	300
Baliga figure of merit (BFOM) ($\epsilon\mu_n E_{Cr}^3$)	0.051	0.716	0.668	1	1.386
Baliga high freq. FOM (BHFFOM) ($\mu_n E_{Cr}^2$)	0.007	0.076	0.316	1	2.309

tionized panel display technology. In 1993, Khan *et al.,* demonstrated the first AlGaN/GaN HEMT [35]. In reality, GaN which was considered to be useless as a semiconductor suddenly resurfaced as an unbeatable choice for the power semiconductor device [36]. While comparing the material properties, it can be observed that the prospect of GaN HEMT is immense. In this Chapter, the fundamentals of AlGaN/GaN material and HEMT are presented. Material properties of a few popular semiconductors are enlisted in Table 2.1. It is apparent from Table 2.1 that GaN is a promising material for various applications and emerging device technologies. A pictorial representation of comparison between competing semiconductor materials is shown in Fig. 2.1.

2.2.1 Bandgap

It is essential to use a large bandgap, high thermal conductivity, lower dielectric constant and high value of critical electric field for the material that has to be used for designing devices which operate either at high power or at RF. A high electric field can be supported and sustained by the materials having wide bandgap and they are also intrinsically radiation hardened. The terminal impedance of a device depends on the dielectric constant of the material which dictates its capacitive loading as well. As compared to a conventional semi-

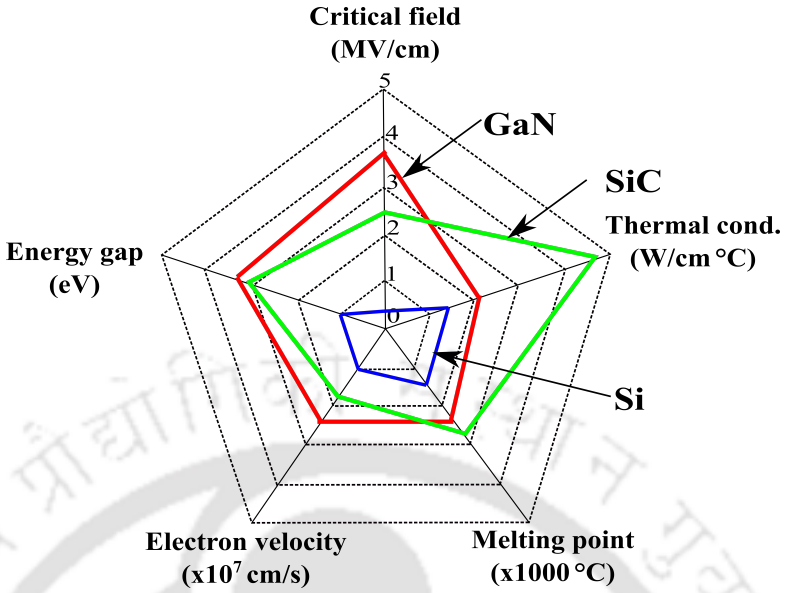

Figure 2.1: Comparison of material properties of popular semiconductor materials.

conductor, the dielectric constant of a wide bandgap semiconductor is lower by 20%, which enables the device sizes to be increased by 20% while maintaining the same impedance. The increased area allows devices to handle higher current [37]. It can be seen in Table 2.1, that GaN has a large bandgap of 3.39 eV, which has two main advantages. First, the material can be used over a wide range of temperatures and second, a very high breakdown electric field can be sustained by it. Another aspect of wide bandgap semiconductors is that these materials have very low intrinsic leakage. Among all the materials enlisted in Table 2.1, only GaN has the capability to form a 2DEG (with AlGaN, but not limited to), hence AlGaN/GaN heterostructure is widely used to design HEMTs. The lattice constant [6] is also crucial to select the right lattice match between layers to avoid strain among them (refer Fig. 2.2).

2.2.2 Critical Electric Field

Breakdown voltage, V_{BV}, of a device depends on the critical field of the material which is employed for its fabrication. Since GaN has a large bandgap, it can withstand a high electric field. The high electric field in the materials enables to design devices having higher

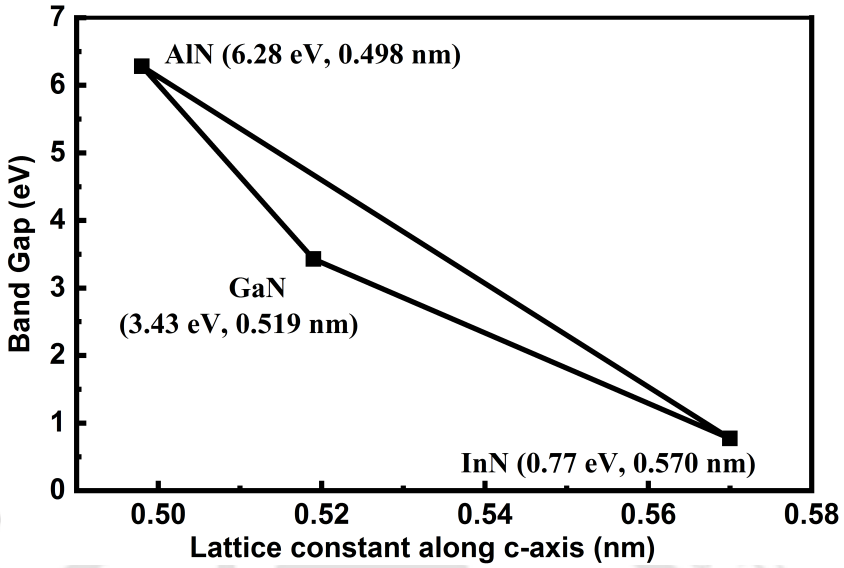

Figure 2.2: Bandgap and lattice constants of Nitride semiconductors.

breakdown voltage. Due to a large electric field, these devices (HEMTs) have lower switching losses, which is evident from Eq. 2.1

$$P_{Losss,min} \frac{\sqrt{f}}{\sqrt{\mu}E_{Cr}} \tag{2.1}$$

where, $P_{Losss,min}$ is the minimum power loss, μ is the carrier mobility, f is the frequency of operation, and E_{Cr} is the critical electric field. It is well known that an AlGaN/GaN HEMTs does not have ionized donors, hence, these devices have higher mobility. The only scattering that may happen is due to Gallium (Ga) and Aluminium (Al) atoms that are randomly distributed in the AlGaN layer. It can be concluded from the above deliberations that the critical electric field has a very significant contribution to the electrical aspect of the device. The breakdown mechanism is largely dependent on material aspects of AlGaN and GaN as well as that of substrates, hence, an appropriate choice of substrate is crucial.

2.2.3 ON Resistance

ON resistance is a fundamental parameter that is related to the efficiency of the device. Devices having higher resistance lose efficiency because of the large voltage drop across the

devices' internal resistance. The ON resistance of an AlGaN/GaN HEMT is the sum of the channel (R_{CH}) and drift region (R_D) resistances. The drift region is the zone between the drain and gate, also called as gate drain access region. The resistance R_{CH} and R_D can be expressed as,

$$R_{CH} = \frac{L_G}{W_G}\frac{1}{q\mu_n N_s} \tag{2.2}$$

$$\begin{aligned} R_D &= \frac{L_D}{W_G}\frac{1}{q\mu_n N_s} \\ &= \frac{1}{W_G}\left(\frac{V_{BV}}{E_{Cr}}\frac{1}{q\mu_n N_s}\right) \end{aligned} \tag{2.3}$$

where, μ_n is the mobility of the electrons in 2DEG, W_G and L_G are the gate width and length, respectively, L_D is the length of the drain access region, N_s is the carrier density of 2DEG, E_{Cr} is the critical electric field and other symbols have their usual meaning. The total ON resistance is determined by adding (R_{CH}) and (R_D) components of resistances,

$$R_{ON} = R_{CH} + R_D \tag{2.4}$$

There are several kinds of losses in an energized semiconductor device, viz. conduction loss, driving loss and switching loss. Conduction loss is always present and it is due to the R_{ON} resistance of the device. The conduction loss is by itself frequency independent whereas, the duty cycle does affect the average conduction power loss. The origin of driving loss is related to the removal and addition of charge to the gate to turn the device ON/OFF. Driving loss is dependent on the applied voltage to the gate and its switching frequency. Switching loss is due to the device's internal capacitances. The switching loss also depends on the device's gate resistance and the switching frequency.

2.3 Substrate Selection

Native substrate for growth of GaN was unavailable for a long time. Hence, GaN was grown on foreign substrates [38]. Substrate selection is an important criterion as it affects the device electrical aspect as well as its reliability. GaN devices fabricated on Silicon substrate have a premature breakdown due to the abrupt rise of vertical component of the electric field

Table 2.2: Common substrates used for growth of GaN [5, 6].

Substrate	Diamond	Sapphire	SiC	AlN	Si
Lattice mismatch with GaN (%)	11	13	3.4	1	17
Thermal conductivity (Wm^{-1} K^{-1})	2000	50	490	200	150
Thermal expn. coeff. ($10^{-6}K^{-1}$)	0.8	7.5	4.2	4.2	3.59
Electrical isolation (Ωcm)	$10^{13} - 10^{16}$	-	$\geq 10^{11}$	$\geq 10^{12}$	1-3 $\times 10^4$

as the Silicon substrate is grounded. Hence, the breakdown in this, case is largely dependent on the GaN epitaxial layers. Silicon is a popular substrate and is very cheap, but there is a compromise in the performance. Various considerations for substrate selection are: (i) Lattice mismatch of the GaN layer with the substrate, (ii) Substrate thermal conductivity as well as coefficient of thermal expansion, (iii) Device electrical isolation with the substrate, (iv) Bowing and warping of wafers (v) Defect density on the substrate surface (vi) Substrate diameter (vii) Wafer cost, etc. Basic properties of common substrates used in an AlGaN/GaN HEMTs are listed in Table 2.2. It is to mention that, before the growth of GaN on any substrate, a thin nucleation layer is grown. This helps in stopping the migration of defects from substrate to upper GaN layer. This inter layer increases the thermal resistance of the composite layer, which leads to an increase in the channel temperature of HEMT. Among the substrates enlisted in Table 2.2, Diamond has the highest thermal conductivity, followed by Silicon Carbide (SiC), which is a popular substrate having better lattice match with GaN. Silicon Carbide is one of the most preferred substrates as all the parameters like lattice mismatch, coefficient of thermal expansion, thermal conductivity and electrical isolation are of an optimum numerical value. In applications, where performance is the key, HEMT on SiC substrates are utilized. Sapphire is also a popular choice for growing GaN and it has been widely used in developing HEMTs. Power density of ≥ 12 Wmm^{-1} [39] have been reported even though it has a very high lattice mismatch with GaN. Sapphire faces a major

issue in thermal management as it has low thermal conductivity. Since it is a very hard material, thinning it to improve the thermal characteristics is challenging. Also, due to large lattice mismatch, the wafer bows which impacts lithography process. Silicon is a low cost, popular substrate material. Due to the maturity in Silicon based growth technologies, the HEMTs grown on Silicon substrate are cheaper, but they suffer from premature breakdown. Lattice mismatch is of Silicon with GaN is high (17%), yet they are great substrate because of Silicon is almost defect free.

2.4 Polarization

Nitrides belonging to the III-N family are commonly grown on the c-plane of the hexagonal wurtzite structure. Such a growth approach, when followed, creates polarization charges located at the opposite surface layers. These charges create internal electric fields and, the direction of this electric field depends on the internal strain and the face of the hexagonal crystal (N or Ga face). The polarization that occurs naturally at equilibrium due to built-in polarization field is referred to as spontaneous polarization. The strength of spontaneous polarization in Nitrides is shown in Fig. 2.3. The same concept of polarization in III–Nitride materials is also applicable to the AlGaN/GaN HEMT. It is this crucial material property that enables these devices to be extremely successful as a high speed transistor, capable of handling large amounts of current. The macroscopic polarization arises in materials having bound charges primarily due to microscopic polarization as there is an asymmetry in charge distribution. The individual polarized dipole atoms have a dipole moment, p. Polarization in these materials is expressed by a vector $\overrightarrow{P}$ and it referred to as electric polarization. The electric polarization the dipole moment per unit volume is related as,

$$\overrightarrow{P} = n\overrightarrow{p} = \frac{\overrightarrow{p}}{\Omega_0} \tag{2.5}$$

where, Ω_0 is the volume occupied by an individual dipole and n it the total concentration of dipole. In a specific group of crystals (like GaN) which has a single rotation axis or no rotation axis, exhibit pyroelectricity, thus, they have inbuilt spontaneous polarization P_{SP}

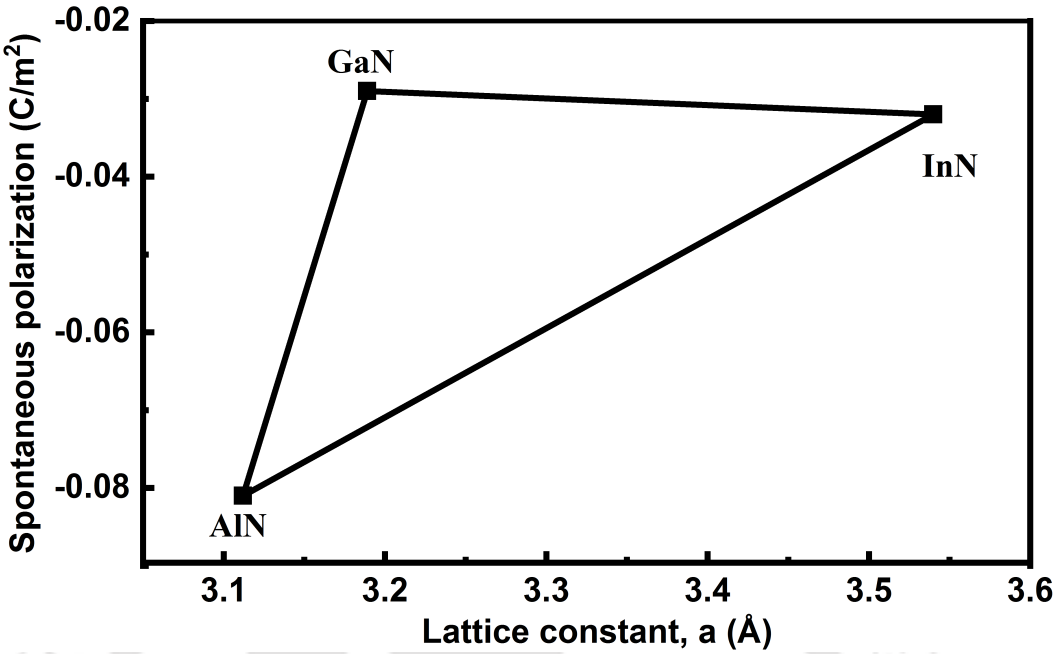

Figure 2.3: Spontaneous polarization of group III Nitride materials [1].

(even without application of mechanical or electrical forces). The ionicity of the constituent atoms determines the intensity of the spontaneous polarization. In GaN-HEMTs, the GaN layer is thicker (in μm range) than AlGaN layer, as shown in Fig. 2.5. The AlGaN layer in an AlGaN/GaN heterostructure develops a strain which is expressed as,

$$\varepsilon = \frac{a(0) - a(x)}{a(x)} \tag{2.6}$$

where, x is the Al fraction in AlGaN layer, $a(0)$ and $a(x)$ are lattice constants of an unstrained GaN and strained $Al_xGa_{1-x}N$ layer, respectively. Figure 2.4 exhibits an arrangement (left side image in Fig.2.4) depicting the difference in lattice constants of the heterostructure. During the growth of an AlGaN/GaN heterostructure, lattice constant of AlGaN has to increase to adjust itself with the underlying GaN layer. This increase in lattice constant of AlGaN creates a strong strain in AlGaN layer (right side image in Fig.2.4). The unstrained AlGaN layer is shown by dashed line in Fig.2.4. This strain creates a piezoelectric polarization, P_{PZ}, in the piezoelectric materials. Thus, the total polarization is obtained by adding spontaneous and piezoelectric polarizations, $P = P_{SP} + P_{PZ}$. The middle structure (in

Fig.2.4) represents the hexagonal crystal orientation of wurtzite structure (both AlGaN and GaN). The polarization induced charge, (σ) is associated with the gradient of polarization

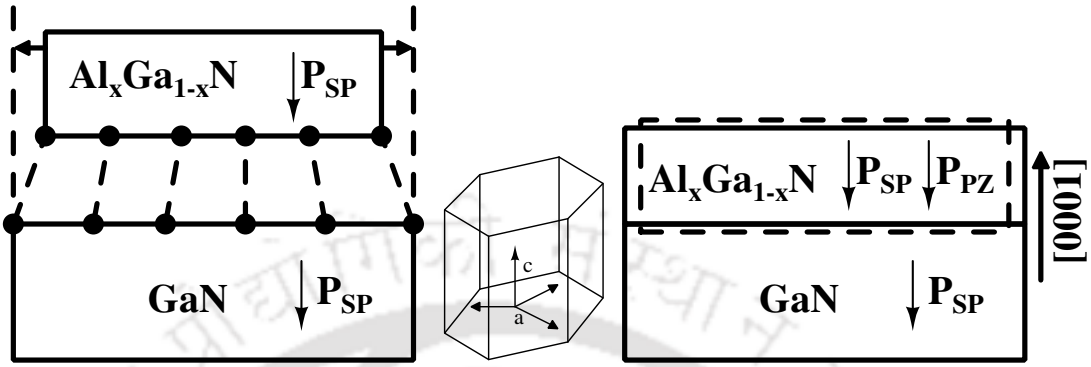

Figure 2.4: Strain representation in an AlGaN/GaN heterostructure.

($\sigma = \nabla P$). At an abrupt interface where AlGaN is the top layer and GaN is the bottom layer, the polarization sheet charge density is defined as [1],

$$\begin{aligned} \sigma &= P_{GaN} - P_{AlGaN} \\ &= P^{SP}_{GaN} + P^{PZ}_{GaN} - P^{SP}_{AlGaN} - P^{PZ}_{AlGaN} \\ &= P^{SP}(0) + P^{PZ}(0) - P^{SP}(x) - P^{PZ}(x) \end{aligned} \tag{2.7}$$

where, x is the Al mole fraction in $Al_xGa_{1-x}N$. Here, GaN layer does not contribute to piezoelectric polarization as it is relaxed, therefore, $P_{PZ}(0) = 0$. The AlGaN layer has higher spontaneous polarization as compared to GaN, hence, a positive charge develops at the AlGaN/GaN interface. A very high value of sheet charge σ/e of 1.4×10^{13} cm^{-2} has been found in the AlGaN/GaN heterostructure for an Al mole fraction of 0.25. This sheet charge at the AlGaN/GaN interface is about ten times higher than in other III-V heterostructure [40], therefore, a higher sheet carrier charge inducted by polarization can be observed.

2.5 Formation of Two Dimensional Electron Gas

When a thin layer of AlGaN (20-25 nm) is grown on a thick GaN layer, a very dense concentration of electrons forms at the AlGaN/GaN interface but in the GaN layer (in the

lower bandgap material) due to strong polarization fields. These electrons get confined in a very narrow triangular potential well. As the density of the electrons are very high, they appear like a cloud of dense gas, hence, popularly known as two dimensional electron gas (2DEG).

In the wurtzite compounds, there is a hexagonal basal plane and the growth happens on this plane, and perpendicular to the plane is c-axis (growth axis). In case of GaN and AlGaN, the growth happens along the c-axis. During growth, one of the hexagonal layers become anionic and the other catatonic, whereby the faces turn polar. Thus, while moving in any of the directions along c-axis, ([0001] or $[000\bar{1}]$), either Gallium or Nitrogen atoms can be encountered first. Moreover, due to strong ionicity of Nitrogen atoms, the charges are displaced, causing it to be polarized. This is the reason for the GaN being anisotropic. This anisotropy governs the growth of heterostructure for HEMT applications as Gallium face is used to grow AlGaN layer above it, which facilitates the formation of 2DEG. Due to the strain in AlGaN layer, a piezoelectric polarization develops, which is given as,

$$P_{PZ} = 2\frac{a - a_0}{a_0}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right) \tag{2.8}$$

where, C_{13} and C_{33} are elastic constant, a and a_0 are unstrained lattice constants of the GaN and AlGaN layer, respectively, e_{31} and e_{33} are piezoelectric constants. In Eq. 2.8, the term, $[e_{31} - e_{33}(C_{13}/C_{33})]$ is always < 0 for any mole fraction of AlGaN, thus, the piezoelectric polarization is always negative for tensile strain.

As polarization induced charge at the AlGaN/GaN interface is positive ($+\sigma$) for Fig. 2.5 (a) and negative ($-\sigma$) for Fig. 2.5 (b) due to change in face of terminating atom. This ($+\sigma$) introduces a cloud of negative charge in Fig. 2.5 (a), which gets trapped in a triangular well and is referred to as 2DEG. However, in Fig. 2.5 (b), due to change in atom face, the $-\sigma$ charge introduces a concentration of holes in GaN and is generally referred as two dimensional hole gas (2DHG). When strain is changed in the system, as shown in Fig. 2.5 (c) and (d), the charges that get generated at the interface, changes. In case of Fig. 2.5 (c), $-\sigma$ charge appears at the interface, which creates 2DHG in GaN, whereas, in Fig. 2.5 (d)

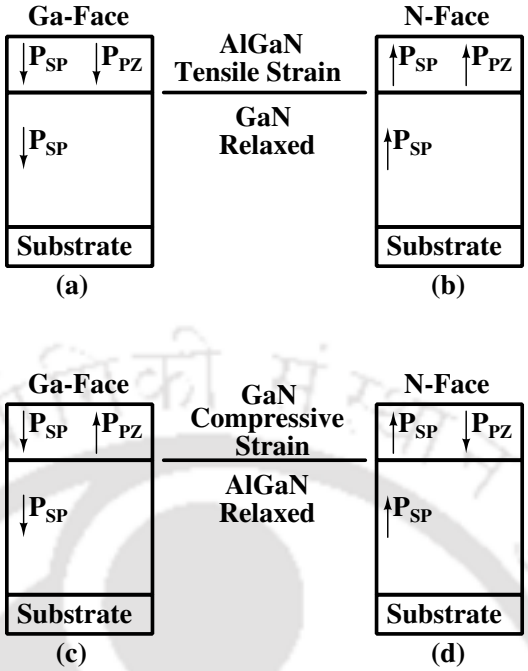

Figure 2.5: Figure (a) and (b) depicts the polarization field condition when AlGaN (thin layer) is under tensile strain for Ga and N face, respectively. The direction of polarization field in the heterostructure changes when the strain and the atom face is varied, as shown in Fig. (c) and (d). When GaN thickness is reduced and AlGaN thickness is increased, GaN experiences a compressive force as AlGaN in now thick and relaxed.

2DEG is formed in GaN as $+\sigma$ charge appears at the interface, but the polarization fields are opposite, hence, it is not relevant for HEMT applications. Figure 2.5 (a) is suited for the AlGaN/GaN HEMTs [41] and the charge distribution for this is shown in Fig. 2.6, wherein, complete charge balancing is shown (except 2DEG, all other are bound charges). In the case of HEMTs, both the polarizations are negative, which add up and point towards the substrate. At a critical barrier thickness, which is shown in Fig. 2.7, the surface states reach the Fermi level and electrons from these states are released and get driven into the 2DEG by strong polarization induced electric field in AlGaN [42]. Figure 2.6 shows a typical charge generation and its balancing in an AlGaN/GaN HEMT. The large polarization difference at the heterostructure interface produces a high concentration of bound charge ($+\sigma$), which in turn generates a high electron sheet density referred as 2DEG, whose concentration is denoted as n_s . The electron density is influenced by the barrier height ϕ_b [43], and the

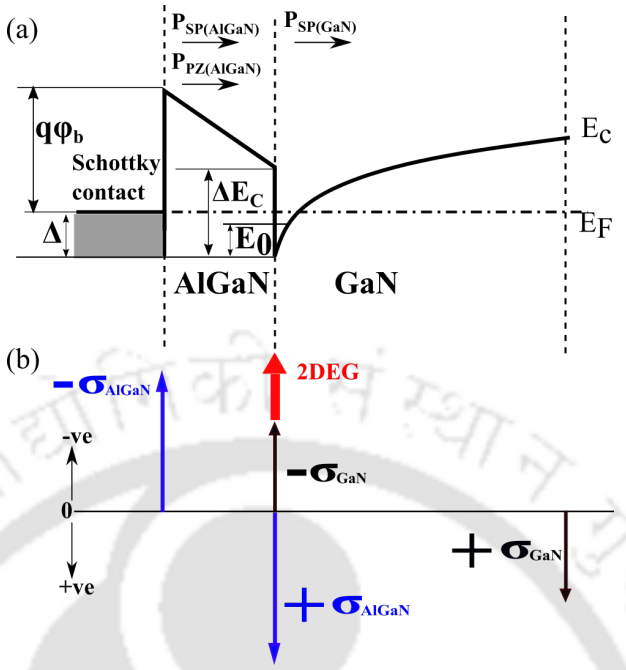

Figure 2.6: Charge generation and balancing in an AlGaN/GaN heterostructure. Due to a positive sheet of bound charge, $+\sigma_{AlGaN}$, a 2DEG ($-\sigma_{GaN}$) is formed in GaN.

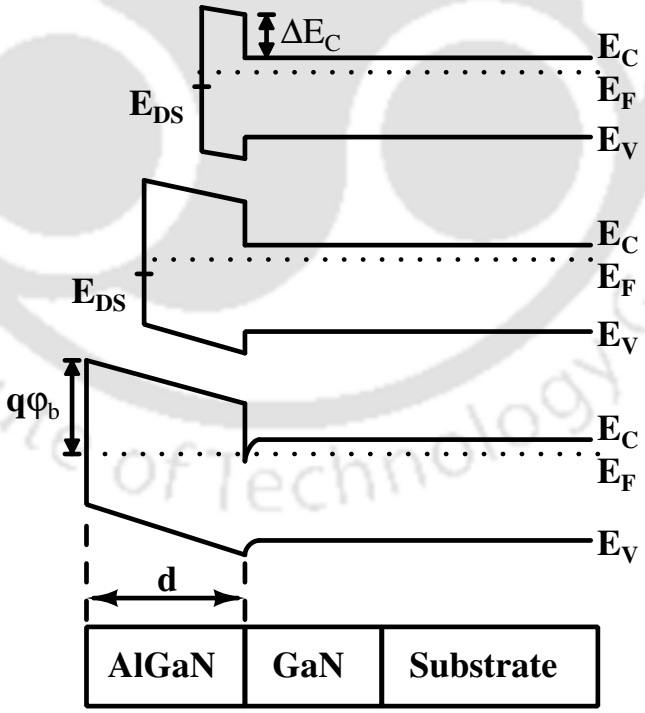

Figure 2.7: A representation showing the variation of the surface donor level energy in conduction band as the AlGaN layer thickness (d), is varied.

electron sheet charge density, (n_s), can be calculated [41] as,

$$n_s(x,d) = \frac{\sigma(x)}{q} - \frac{\varepsilon_0 \varepsilon(x)}{q^2 d}\left(q\phi_b(x) + E_F(x) - \Delta E_c(x)\right) \tag{2.9}$$

where, x is the Al mole fraction in AlGaN, σ is the charge induced by polarization, E_F is the Fermi level, ΔE_C is the offset in conduction band, $q\phi_b$ is the Schottky barrier height, ε_0 is the vacuum permittivity and ε is the relative permittivity of barrier layer, d is the width of the barrier layer.

2.6 Device Operation

A HEMT working principle is similar to other field effect devices. The electrons in 2DEG travel along the GaN channel without facing ionized donor atoms, hence, these have high mobility, favouring fast response time. The source and drain contacts are formed on GaN using a metal stack of Ti/Al/Ni/Au, whereas, the gate contact is formed by Ni/Au on AlGaN and is Schottky in nature. The basic underlying principle is the depletion of the conducting channel (2DEG) to stop the carrier flow from source to drain. Since channel is naturally present, therefore, a negative bias at the gate is required to deplete the channel. When the channel depletes, the current flow is obstructed and under this condition, the drain bias is not capable of driving the current through the device, thus, the device is driven to OFF state. Figure 2.8 presents various bias condition and their corresponding electrical operating point. For instance, Fig. 2.8 (a) exhibits the scenario in which gate bias is higher than the threshold voltage. Under this condition, 2DEG exists but there is no current flow as drain source bias (V_{DS}) is held at zero. In Fig. 2.8 (b), it can be seen that the channel depletes because gate bias is held lower than the threshold voltage. In this circumstance, the drain source bias cannot initiate the current to flow as the channel is no longer continuous, hence, the device is in OFF state. Whereas, in Fig. 2.8 (c), when the 2DEG is continuous ($V_G > V_{th}$), a positive V_{DS} can initiate a current flow from the source to drain, thus, turning the device on.

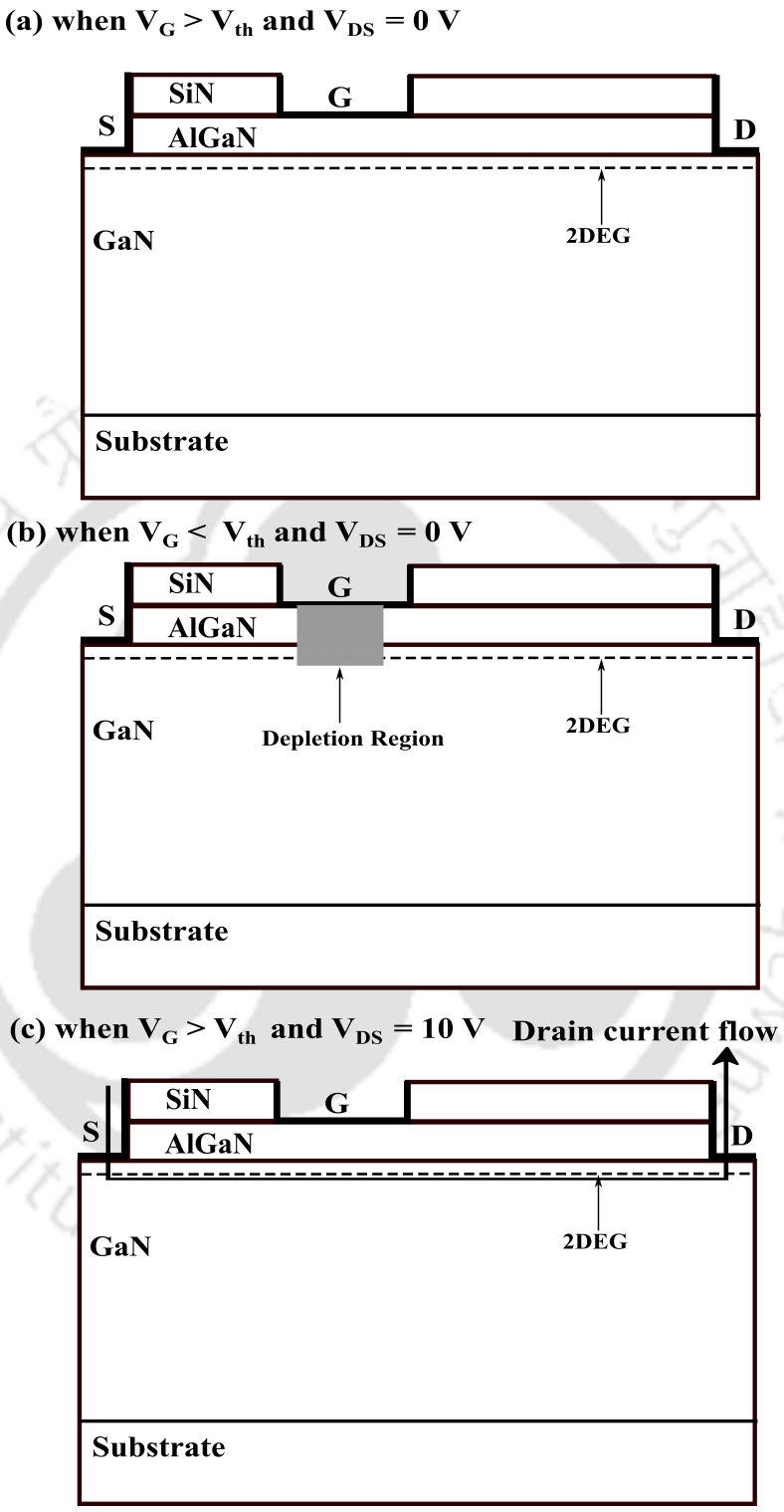

Figure 2.8: Schematic of an AlGaN/GaN HEMT structure, showing its working. Figure (a) shows the condition when channel is present, (b) demonstrates the situation when the channel is depleted, even if V_{DS} is greater than 0 V, hence, the drain current cannot flow in this case and (c) represents the scenario when extant channel helps in current conduction when V_{DS} is greater than 0 V.

2.7 Prior Art on AlGaN/GaN HEMT

AlGaN/GaN HEMT technology has turned as an ultimate choice for application in defence, space, power conversion and control, to name a few. However, there are various reliability aspects which are responsible for the failure of these high power devices. Material aspects of III-V semiconductors acted as a boon for AlGaN/GaN power devices by enabling the formation of 2DEG and withstanding high electric field. However, when devices are fabricated using these semiconductors, the devices start exhibiting nonidealities and failures mostly attributed to their inherent material properties. The 2DEG is a physical phenomenon harboured at the heterojunction which gave birth to HEMTs. However, numerous physical mechanisms create conditions that at times may be a threat to the existence of 2DEG. Hence, this section summarizes various challenges encountered by both academia and industry on HEMTs.

Ambacher *et.al.*, [41] discussed the material properties that are necessary for the formation of the 2DEG in an AlGaN/GaN heterostructure. In the $Al_xGa_{1-x}N$ layer, the Al mole fraction (x) is varied from 0.15 to 0.5 and its thickness is varied from 20 to 65 nm. The charge carrier profiles are evaluated for various combinations of thickness and mole fraction of AlGaN. The most important result of the study relevant for HEMTs is that GaN layer has to be Gallium (Ga) face and in a relaxed state, whereas, the AlGaN layer deposited on GaN needs to be in the strained state. Such a condition aligns the spontaneous and piezoelectric polarization in the same direction, thus creating a 2DEG in GaN. For Nitrogen (N) faced GaN, with the same strain condition as discussed above, a two dimensional hole gas (2DHG) is formed instead of the 2DEG in the GaN. Therefore, it is essential to maintain the crystal face as well as the strain conditions for the formation of a 2DEG. As Aluminium (Al) mole fraction is increased, the sheet carrier concentration of 2DEG increases due to an increase in the strain in AlGaN layer. A detailed discussion of the properties of piezoelectric materials relevant for an AlGaN/GaN heterostructure has been presented and the work depicts

the guidelines for the selection of material composition and their thickness for achieving a required carrier concentration in the channel. This work is a classic and forms the basis for all kinds of fundamental understanding regarding an AlGaN/GaN heterostructured devices based on spontaneous and piezoelectric polarizations.

Jogai *et.al.*, [44] studies the effect of electromechanical coupling on the strain in an AlGaN/GaN HEMT. In the presence of an electric field, a coupling happens between mechanical and electrical properties of heterostructure because the AlGaN/GaN layer is piezoelectric. Thus, it is important to understand the effect of electromechanical coupling and its effect on device performance. In their work, Jogai *et.al.*, coupled the mechanical and electrical properties of an AlGaN/GaN layer and proposed corrections in strain, electric field and electron concentration. The coupling modifies several physical parameters as compared to that of an uncoupled case (uncoupled case correspond to initial studies which do not consider electromechanical coupling). The 2DEG charge in HEMT reduces built-in electric field through screening effect, created by fixed space charge that is associated with it. As a result of the shielding effect, electromechanical coupling is lowered. Therefore, the result obtained from a fully coupled model agrees with that of an uncoupled case. Nevertheless, corrections are essential as they help in proper estimation of charge and strain, thus, leading to accurate calculation of drain current.

In another work, Sarua *et.al.*, [45] explored the effect of bias on the piezoelectric strain in an AlGaN/GaN HEMTs using Micro-Raman spectroscopy. They were aware of the fact that the converse piezoelectric effect arose due to an external electric field and measured the CPE strain in the HEMT using Micro-Raman spectroscopy. They observed the CPE strain by employing phonon shift emerging from a biased heterostructured device, and the recorded shift was directly proportional to the applied electric field. A TCAD simulation was also performed by them to observe CPE arising out of the vertical electric field. The strain results observed using Micro-Raman measurements matched with that of the TCAD simulation, hence, it is concluded that the vertical electric field is crucial for studying CPE in HEMTs.

Joh *et.al.*, [28] proposed that the applied electric field causes degradation in an AlGaN/GaN HEMTs. They suggested the concept of critical voltage for electrical degradation of HEMTs. They also mentioned that the degradation arising due to the CPE phenomenon results in crystallographic defect formation. It is observed, the mechanical strain produced by the electric field adds to the already present residual tensile strain in HEMT due to lattice mismatch. Strain in AlGaN layer also depends on the vertical electric field and is linearly dependent on it, whereas, the elastic energy in AlGaN layer is proportional to the square of the strain. The moment this elastic energy exceeds a threshold value, crystallographic defects are generated, which in turn act as trapping sites for electrons. It is also reported that the strain field contributed by the source gate voltage (V_{SG}), is also responsible for influencing the critical voltage. Their emphasis is on the electric field related issues faced by HEMTs.

Alamo *et.al.*, [17] emphasized the role of vertical electric field in creating CPE in an AlGaN/GaN HEMT. They supported the idea that the basic cause of defect formation and degradation is through CPE. They were of the idea that the CPE is not a current driven mechanism. There is a sudden and a large increase in gate leakage current due to this phenomena. It has also been reported by them that transistors having a short gate length are more prone to such a mechanism, wherein, the source to gate voltage (V_{SG}) influences the critical voltage. The critical field for device degradation was evaluated by the same group [27], in which the role of V_{SG} was emphasized. Once traps are formed due to strain relaxation, newly formed traps get filled by the presence of high electric field, thus, lowering the concentration of electrons in the channel [29]. High strain can also lead to the permanent failure of the devices. The fundamental approach to resolve such an issue is to contain the intensity of vertical electric field. Hence, Alamo *et.al.*, [17] suggested that a device redesign approach either with a slant or rounded gate could reduce the intensity of CPE. Simulation showing the effect of gate filleting has not been explored. Therefore, this thesis aims to understand the influence of such a gate shape on the internal phenomena of the device.

Ancona *et.al.*, [46] also used the coupled model to study degradation mechanism in an

AlGaN/GaN HEMT. They reported that both bias strain/stress are responsible for the degradation in a HEMT. The co-existence of high vertical electric field along with high current and high working temperatures are the main contributors that initiate defect formation in the heterostructured devices. It has also been pointed out that the degradation centres start creating defects at a localized location where the CPE strain, electron temperature, self-heating and electric field are the highest. At high temperatures, there can be degradation caused due to chemical processes. They also highlighted the significance of gate shaping without detailed simulation and suggested that such an approach might spread the electric field in the gate vicinity, thereby, enhancing the breakdown voltage, minimizing the gate leakage current, and subsiding the hot electron related damages. In a typical experiment of slant gate, they found that the electric field and CPE were lower as compared to a conventional rectangular gate HEMT. They also used an initial crack intentionally incorporated in a device and observed that it relocated itself during bias stress.

Meneghesso *et.al.*, [14] resorted to EL measurements for studying hot-electron phenomena in GaN-HEMT. Even the gate current is mostly due to tunnelling of carriers, therefore, it cannot act as an indicator for the presence of hot electrons. Hence, EL measurement was the only way out to observe the hot electrons and their dependence on bias state. When EL spectra were observed at high drain bias, there was no indication of electron/hole recombination in these spectra. The light emission in these devices is primarily due to highly energetic electrons which negotiate intraband transition. The degradation due to hot electron is maximum when both the drain current and the electric field are the highest. It was observed that in ON state (V_{DS} = 20 V and V_{GS} = 0 V), EL signature from HEMT channel was same throughout indicating uniformity in the energy of channel electrons, whereas, in OFF state (V_{DS} = 20 V and V_{GS} = – 6 V), EL became nonuniform and particular locations had higher EL as compared to others due to the injection of hot electrons from gate electrode. In the OFF state, electrons acquire high energy as the gate drain bias is sufficiently large, which facilitates enhanced photon emission. It was concluded by observing the EL spectra that V_{GS} played a significant role in enhancing/depleting and imparting energy to electrons.

To ascertain the degradation, DC tests were performed and it was found that the partial ON state (V_{DS} = 20 V and V_{GS} = – 5.5 V) proved to be fatal for the device as there was a fall in transconductance, (g_m), and the devices under such a test also exhibited gate lag. The strain relaxation after very high CPE leads to an increase in gate leakage current through trap assisted tunnelling and hopping in the AlGaN layer.

Zhu *et.al.*, [47] discussed the various stress conditions that a HEMT can undergo during its operational life. The stress can be elaborated as: bias stress due to reverse bias of gate, OFF/ON state high field stress and ON state low field stress. The hot electrons created due to electrical stress of reverse biased gate could distort the typical bell-shaped transconductance curve, and it introduced a double peak in it. The distortion got prominent as the duration of stress increased. This feature evolution in transconductance is credited to the filling of donor traps at low field and subsequent emptying because of a high electric field. This emptying of electrons somehow attempted to restore the characteristic shape of transconductance. They concluded that the electric field at the gate edge is to be held accountable for most of the trapping in its vicinity.

Braga *et.al.*, [32] report that electron energy is responsible for inciting a small negative differential output conductance (NDC), irrespective of the operational power in the device. Hence, they suggested that the electron temperature has a major role to play rather than lattice temperature and that the NDC has been attributed primarily to the capturing of hot electrons in bulk traps. The electrons after attaining high energy from gate edge on the drain side may get spilt over the AlGaN barrier into GaN bulk. They also proposed that trapping lifts conduction band under the gate leading to a potential barrier, thus, obstructing the carrier flow. They further deliberated that these hot electrons also play an important role in altering the breakdown voltage of the device. In this thesis, hydrodynamic simulations have been performed to observe the presence/variation of electron energy in the proposed HEMT structure.

Tapajna *et.al.*, [31] discussed various degradation mechanisms in InAlGaN/GaN HEMT due to hot electrons. Hydrodynamic simulations were performed to arrive at the conclu-

sion. These hot electrons having a higher temperature are responsible for increasing the trap density underneath the gate as well as on the surface and interface in the gate-drain access region. They reported that the electron temperature could locally reach up to 30,000 K and the degradation was maximum in the semi-ON state. The 6 and 12 μm drain to source spacing devices had a similar value of electron temperature, which implied that it was independent of source to drain spacing. The electron temperature increased from 27,000 to 29,000 K as the gate bias was varied from 0 to – 2.5 V, respectively. In their experimental measurement, the measured electron temperature was found to increase from 4700 K to 8000 K with decreasing V_{GS} (V_{GS} becoming more negative, causing the electric field to increase). However, the temperature rise was not monotonic but fell when V_{GD} was increased beyond a certain value (carrier velocity falls), thus ascribing a typical bell-shaped characteristics to the electron temperature. Semi ON state stress promoted an increase in the density of pre-existing traps. The V_{th} transients were very sensitive to trap locations underneath the gate, whereas the I_D was not much sensitive. In the stressed devices, the already existing traps further increased in number due to the stress. When the electrons are emitted by gate, they could be trapped in these traps. These traps were also responsible for the increase in the channel resistance. Hot electrons could also initiate the physical mechanism of Hydrogen removal. For reference, an AlGaN/GaN HEMT was also used in their work, and the electron temperature in those devices was found to be 11,400 K at $V_{GS} = 0$ V.

Meneghini *et.al.*, [48] discussed about E_2 trap in GaN buffer. Their work used a Iron (Fe) doping in the GaN and they focused mainly on analyzing the effects of these traps on current collapse in HEMTs. These traps originate due to the native defect and are not dependent on Fe doping as generally believed. They found that capturing of electrons in these traps are bias dependent. In the OFF state, the trapping takes place due to gate leakage current, whereas in semi-ON state, the trapping occurs due to hot electrons injection from the 2DEG into the GaN buffer as the electric field is high at the gate edge towards the drain. In another work, Meneghini *et.al.*, [49] performed a study on a vertical Au/Ni/AlGaN/GaN/n-GaN/AlN/Si Schottky diode to observe reverse bias leakage mechanism. It was found that

the high energy electrons were responsible for the creation of shallow donor traps at 0.12 eV from the conduction band. Meneghini *et.al.*, [50] carried another experiment to distinguish the effect of ON and OFF state stress conditions in influencing the trapping. Their observation was that in OFF state stress, a trapping occurred in the gate drain access region and it was dependent on the drain bias. In the ON state bias stress, the trapping was due to injection of hot electrons into the traps from the channel.

Zanoni *et.al.*, [51] reported the reliability of the gate edge of Schottky junction in an AlGaN/GaN HEMT. A numerical simulation was performed to understand the effect of gate length on the critical voltage. It was found to increase with the increase in gate length. Regarding the CPE, it has been pointed out that a 0.076% increase in uniaxial strain decreased the critical voltage from 25 V to 20 V. It was also reported that a unison between lattice temperature, electric filed and CPE led to the initiation of crack formation, which later migrates. They also found that the degradation was electric field driven. As the reverse voltage was further increased, the number of defects increased rather than enlargement of the already defective areas. In EL measurement, the EL spots were found at both the gate edges. Even they have reported the electrochemical degradation of AlGaN and GaN. Interdiffusion between metal and semiconductor due to thermal mismatch, strain and defects has also been reported. Gold diffusion occurred in Ni/Au metallization of Schottky contacts and in some cases it was observed that Au reached AlGaN layer through migration along gate edges.

Binari *et.al.* [52] reported that the presence of traps promoted trap assisted tunneling, thus degrading devices' performance. When the drain was biased at a high voltage, hot electrons spilt into the buffer and upon being captured by the buffer traps under the channel, creating a virtual gate which depleted the 2DEG. They also proposed that it was possible that these hot electrons spilt over the channel and get captured by the traps outside the channel.

Sarua *et.al.* [53] discussed the thermal and piezoelectric stress in an AlGaN/GaN HFET devices with doping of GaN buffer layer by Iron (Fe). In the undoped buffer, peak electric

field stood at 0.7 MV/cm, whereas, for the Fe doped GaN buffer, electric field increased to 2.4 MV/cm, this would be detrimental to the device in the pinched OFF state, where electric field was very high. They observed that in ON state near the thermal hot-spot, thermal and piezoelectric stresses were of the same order of magnitude but opposite in sign, as a result, the gate edge at the drain side had lower stress, unlike the source side gate edge, where there was no hot spot. This implied that in OFF state when the self-heating was absent, the devices had higher strain, which resulted in higher degradation in OFF state as compared to ON state.

Shur [54] predicted the high power capability of GaN by demonstrating higher velocity overshoot of approximately 1.5 times in GaN as compared to GaAs, when electrons were injected into these materials with low velocities in a region of a constant electric field. It was also commented that the temperature did not have much effect on the electron velocity in GaN as compared to that of GaAs. The higher power dissipation capability of these devices were also studied, and this high power finally exhibited itself in the form of self-heating.

Hosch *et.al.* [55] discussed field dependent self-heating in AlGaN/GaN HEMTs. They found that as the drain voltage was increased, the temperature profile broadened, and it shifted towards the drain side where a higher temperature was recorded. They also observed that the channel temperature increased when drain voltage was increased even if the power level was held constant. This may be happening due to an increase in the electric field at gate edge due to the drain bias coupling through gate electrode. In such a scenario, it is expected that gate shaping would cut the intensity of electric field in and around gate vicinity.

Singhal *et.al.* [56] reported that those devices which operated at an elevated temperature had a higher drift (reduction) in drain current for a fixed operational lifetime of 20 years and had an exponential decrease in the mean time to failure. They also demonstrated that there was a degradation of the interfacial layer in the gate contact region leading to an increase in Schottky barrier height thus leading to an increase in threshold voltage, which reduced the drain current [56]. They also pointed out that self-heat has a major impact on the gate

contact and leads to its permanent degradation.

Jung *et.al.* [57] reported that the Gold from Ni/Au contact tend to migrate to the AlGaN surface through the gate edges at around a stress voltage of $V_{DS} = 50$ V with wafer backside temperature of 100 °C. The outcome of this migration is an increases in gate leakage current. An anomaly that needs to be pointed here is that, even though the barrier height of both Gold (5.1 eV) and Nickel (5.15 eV) are almost the same, there is still an increase in gate leakage current.

Zanoni *et.al.* [58] observed that the Schottky and Ohmic contacts in an AlGaN/GaN HEMTs were stable in the absence of electric field even when the temperature was very high. They observed gate edge degradation either in OFF state bias or during the reverse bias of Schottky junction due to very high gate-drain bias. A sudden increase in gate leakage was observed within minutes of applying the bias conditions mentioned above. An increase in the trap density in AlGaN layer was also noted due to this bias state. This mechanism of degradation was referred to as "Gate edge degradation" Therefore, in order to improve reliability of the gate edges at high temperature in the presence of an electric field, tailoring of electric field is essential.

Hodges *et.al.* [59] discussed the impact of thin GaN device channel on the thermal behaviour of an AlGaN/GaN HEMTs. The idea behind their work was that as any material is thinned, its thermal conductivity reduces. Raman thermography was used to measure the operating temperature. As per their observation, the thermal conductivity of thin GaN layer was found to be about 50% lower than the bulk GaN leading to higher channel temperature. Therefore, they suggested that the GaN layer should not be thinned below 10 nanometers.

Wu *et.al.* [60] reported unusual degradation of the gate edge on the source side. As the gate edge degrades, gate leakage increases, the increased gate leakage further worsens the degradation. They also reported that gate sinking and permanent positive threshold voltage shift issue when the device operated at higher temperatures. Hence, it is essential to lower the interface temperature of the gate/metal contact.

Chatterjee *et.al.* [61] performed the coupled thermoelectric reliability study of AlGaN/GaN

HEMTs. The devices used in their work were symmetric (equal spacing between source gate and drain gate). Infrared (IR) thermal microscopy and thermoreflectance thermal imaging systems were used to measure the device temperature. Both the measurement techniques produced the same pattern of heating and they found that very high temperature was observed when the channel was pinched-off (V_{DS} was high). In contrast, for low V_{DS} (no pinch-off), the temperature was evenly distributed around the gate. One crucial observation was that the 2D thermal simulations yielded a higher temperature as compared to 3D simulation as the third axis was missing.

Hwang *et.al.* [62] performed a numerical simulation of a device structure on Silicon substrate which had a copper plug below the active heat dissipating junction. A via-hole through the substrate was formed, and the thermally resistive AlN layer was removed. The plug was later electroplated with Copper. It was found that the temperature reduced from 146 to 120 °C at 5 W/mm power density. The copper plug was able to reduce the junction temperature, but the work presented in this paper did not discuss the issues that would arise due to thermal expansion of Copper.

Mohanty *et.al.* [63] measured temperature of the hot-spot in HEMT by Infrared thermometry. A Silicon substrate was employed to fabricate HEMT. Silicon substrate was etched (AlN layer left intact) to create a micro-trench which was later electroplated with Copper. They could demonstrate a 22 °C fall in hot-spot temperature in a micro-trenched device as compared to an identical device without trench at the same bias power. An improvement in drain current and transconductance was reported to be 17% and 26%, respectively. The threshold voltage was almost the same for both the devices.

2.8 Summary

Evolution of newer materials has led to the emergence of the state of the art devices with improved performance and power handling capability. Ingenious device concepts, aided by a better understanding of solid state physics concepts led to the emergence of (AlGaAs/GaAs) HEMTs. The same concept was utilized in AlGaN/GaN layered structure to create HEMTs.

Since then, HEMTs have benefited from the material properties of AlGaN/GaN heterostructure. Several issues which limit the utilization of full potential of HEMTs have been reported. As the issues get resolved, GaN HEMTs are poised to capture the high power device market.

3

Simulation Approach and Setup

Contents

Technology Computer Aided Design (TCAD) simulation of a semiconductor device has always been a primary approach in understanding solid state electronics and to frame guidelines for the evolution of next generation technology. Design of a semiconductor device requires the basic understanding of physical phenomena and mechanism occurring in the semiconductor material as well as in the device structure under study. A TCAD tool assists designers in visualizing the internal fields and carrier dynamics in a device structure. This helps in further improvement of device characteristics. Device structures evolve on a regular basis which increases design complexity. The responsibility of TCAD designers is of paramount importance, whereby they need to develop advanced device models and improved mathematical solvers possessing enhanced predictive capabilities.

Electronics design and technology is advancing fast. Hence, there is a need as well as compulsion to keep up with the developments. Ability to quickly design and test devices based on emerging materials is the need of the hour in the post CMOS era. The responsibility to quickly design such devices, not only lies on the designer but also on a device simulator. TCAD plays a vital role in pushing the advancements in research and development of semiconductor devices by optimizing the existing semiconductor processing technology. Different types of device structures and geometries can be studied with a TCAD simulator. With the help of various semiconductor models (such as; Drift-Diffusion, Hydrodynamics, Boltzmann (Monte Carlo), Quantum Corrected Boltzmann, Non-equilibrium Greens Function [64]), these device structures can be analyzed to predict approximate device characteristics.

Numerous physical models that mimic the behaviour of semiconductors are already incorporated in a simulator. These models are a set of mathematical equations which replicate the device physics. A general model is in the form of a partial differential equations (PDEs). These PDEs needs to be converted into a numerically solvable problem with the help of various discretization schemes. Among the various discretization techniques available, finite difference method (FDM) and finite element method (FEM) are popular. FDM is faster and computationally less intensive for simpler one dimensional (1D) structures, but it tends to perform poorly when the structure complexity increases. These PDEs with suitable bound-

ary conditions are solved on a specific device geometry to simulate different transport models of a semiconductor device. The computation complexity of such kind of problems increases if the device structure becomes complicated. For regular and simple structures, these PDEs can be analytically solved, but one has to resort to numerical methods, if the structure is complicated. This Chapter presents the simulation setup and outlines the basics of all the tools employed and methodology adopted for simulation in this thesis. All the design and simulations presented in this thesis have been carried out using Sentaurus TCAD engine [65].

3.1 TCAD Software Engine

Sentaurus TCAD [65] comprises of various modules each intended to perform specific tasks. It has a GUI based operating environment for creating, organizing, simulating and analysis of devices through simulation. The graphical design of the interface easily allows a designer to quickly setup a simulation environment. A large set of simulation with numerous design parameters can be setup easily. There are various features of Sentaurus TCAD, and only the relevant ones that have been used in this thesis are being discussed.

3.1.1 Workbench

Sentaurus workbench [66] aptly referred to as SWB, is a GUI based visual environment which binds together all the important tools in Sentaurus TCAD bundle. All the simulation tools are integrated together in a graphical interface, which allows easy access to the simulation process flow. All the simulations are arranged as per user planning in the form of projects which can be easily explored. This frontend also helps in easy setup of simulation tool, parameterizing the experiments and easy retrieval of results for visualization. Once a simulation is planned using a set of tools, the flow of information is automatically routed from the tool which completes its task to the next waiting in queue. Figure 3.1 shows a typical workbench frontend in which a parametric simulation has been planned. As we know, that workbench has the capability to accept parameters and variables which help in running comprehensive parametric analyses to observe the change in device performance *w.r.t* the

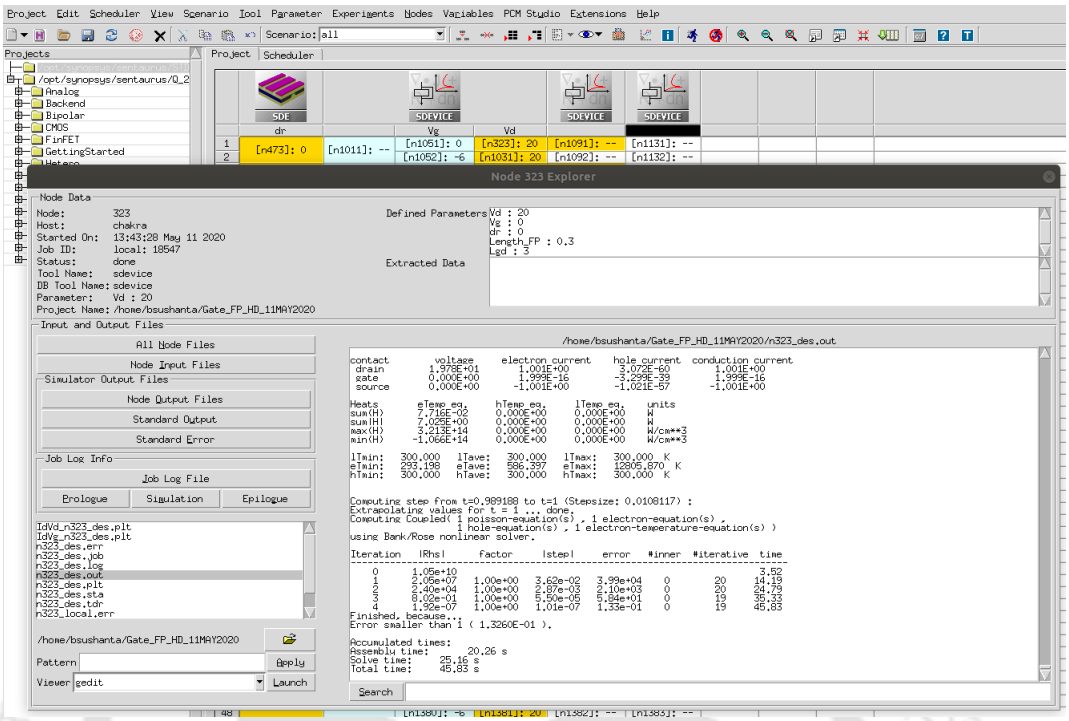

Figure 3.1: Main GUI window of Sentaurus Workbench, overlaid image shows the intermediary results obtained during a device simulation.

variation in one or many parameters. Figure 3.1 exhibits Structure Editor (SDE) and SDEVICE (right side) in workbench GUI. It can be seen in Fig. 3.1 that the Structure Editor has a device parameter "dr" which can be varied as per design requirement. SDEVICE has also been included in simulation flow. It has two other parameters, V_g and V_d for gate and drain bias voltage, respectively. The SDEVICE solves the devices structures for the bias conditions set for the parameters V_g and V_d to obtain its electrical characteristics. Each simulation has a unique node number assigned to it (e.g., n323). An overlayed window on SWB (refer Fig. 3.1) is showing the intermediary result of Node-323. Once the simulation is set up, the flow of information takes place as depicted in Fig. 3.2.

3.1.2 Structure Editor

Device structure are designed using Sentaurus Structure Editor (SDE) [67]. It helps in designing 2D/3D structures using various materials available in its database, and existing structures can also be edited with it. The devices can be designed using Tool Command

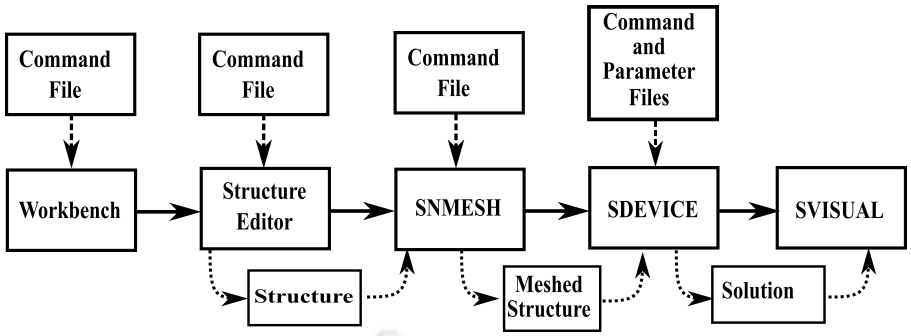

Figure 3.2: A representation of files required and device simulation process in Sentaurus TCAD.

Language (TCL) commands by writing TCL scripts. Structure Editor's GUI is shown in Fig. 3.3. As the structures keep getting designed, SDE prints the related script commands (in

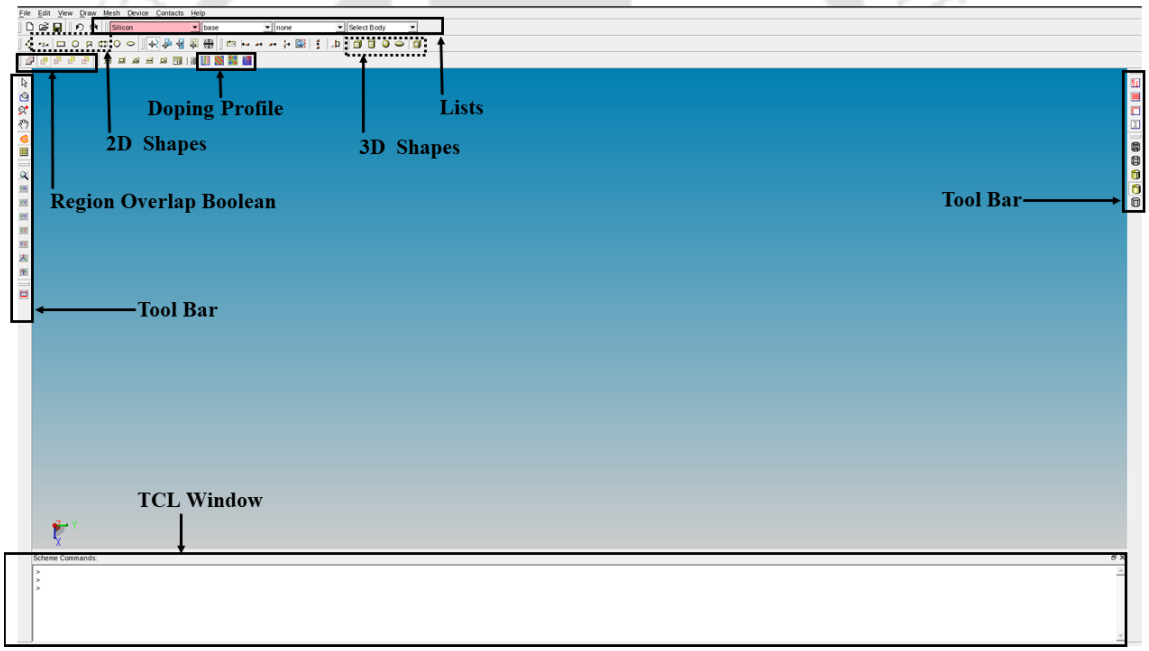

Figure 3.3: Structure editor GUI window showing important tools for structure design. The TCL window at the bottom of GUI displays the commands corresponding to each process in the structure design using the Tools of the toolbar.

the window labelled Scheme Commands in Fig. 3.3) which corresponds to a GUI operation. All the important properties of a device are fixed here, like device structure and dimensions, material selection, doping, contact placement and meshing, to name a few. With the help of workbench, the Structure Editor can even generate parametric device models.

3.1.3 Sentaurus Mesh

Sentaurus Mesh (SNMESH) [68] discretizes the device using a mesh and then the semiconductor equations are solved in it. Therefore, meshing is a very important part of device design. SNMESH can generate modular Delaunay 2D and 3D meshing on the device and can also create axis-aligned as well as tensor meshes that can be used for discretization of device structure either through finite-difference time-domain (FDTD) or box discretization scheme. This tool also acts as a doping profile generator and all the information required for a device simulation is available on a meshed device. Sentaurus mesh has to work in close association with any tool (like Sprocess and Structure Editor) to generate meshings on device structures.

3.1.4 Device Simulator

Numerical analysis of the device structure is performed using Sentaurus Device (SDEVICE) [69]. It can simulate electrical, thermal and optical characteristic of any semiconductor device and is capable of simulating 1D, 2D, and 3D device behaviour. Various kinds of operating conditions can be incorporated into the simulation. The flow of information and instructions among the tools, along with input and output files are shown in Fig. 3.4. The various kinds of input and output files generated by the tools and their description is mentioned below.

- A grid file generated by Structure Editor is in TDR format and contains information regarding device geometry, wherein, additional mandatory specifications like materials involved with their corresponding region name, meshing, contact placement and doping profiles are mentioned. This is an input file for the simulation using SDEVICE. Along with all these information, the physical parameters of the materials involved need to be supplied for numerical simulation to proceed.

- After the simulation is over a file with extension _des.tdr is generated in which solutions of various variables like carrier densities, electrostatic potential, electric field,

carrier density, etc. are present. A user can generate additional record which contains information of electrode current, charge, time, and temperature if a thermal simulation is also activated.

- A log file with extension _des.log is generated and it has very useful information about the simulation like the progression of iteration, intermediary results obtained at all the iterations. It also displays error and convergence related issues and can help in locating region on the device structure having convergence problem.

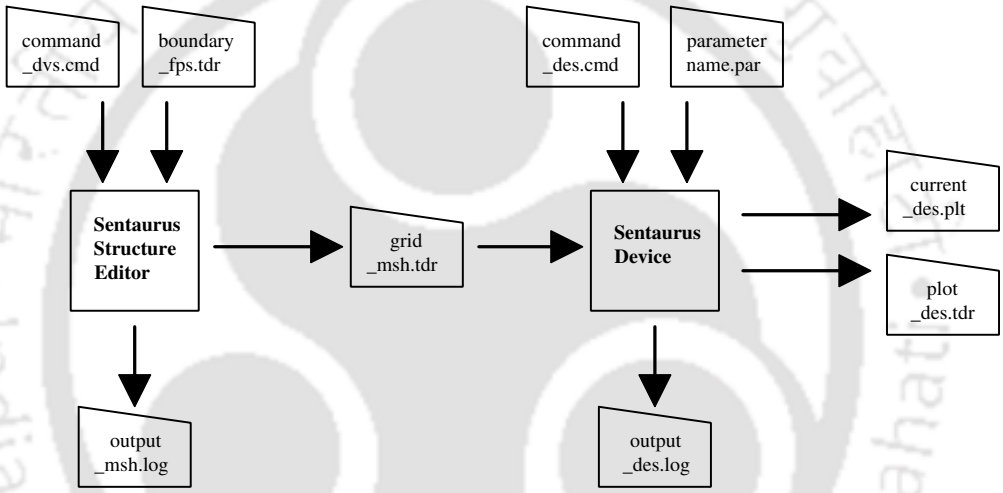

Figure 3.4: Flow of command, information and input and output files required and generated in Sentaurus Structure Editor and Sentaurus Device.

3.1.5 Visualization Tool

The visualization tool in Sentaurus is Sentaurus Visual (SVISUAL) [70] and can visualize results of 1D, 2D and 3D devices. Cutlines can be marked on the structure to observe a physical parameter, such as carrier density, potential, etc. Structures can be superimposed to observe differences in the solution obtained because of parameter variations. Band diagrams can be observed in any region of the structure. Various mathematical operations can also be performed on the results using SVISUAL. Data export in ASCII format is also possible for plotting and further analysis. A SVISUAL window is shown in Fig. 3.5 with a HEMT_1139_000000_des.tdr file opened for visualization. The meshings overlayed on the

device structure is shown in Fig. 3.5. In the same SVISUAL window on the right side, there are various short cuts (X/Y - cutline, integration, overlay, measurement tool, etc.) to observe the results. On the right side of the scalars tab, various results obtained for a structure can be selected and then it appears on the structure displayed in the centre. The vector tab allows the selection of vector fields of the simulated device. In the selection tab, various materials appear, and they can be checked/unchecked to view/overlook a particular region. A host of other features can be explored using Menu tabs on the top right of SVISUAL window.

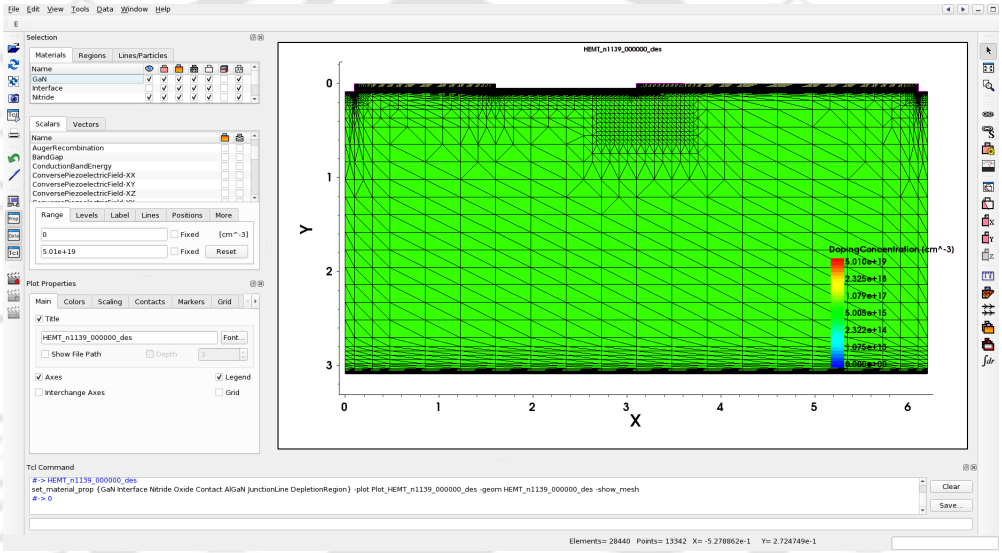

Figure 3.5: Visualization tool, "SVISUAL" of Sentaurus TCAD.

3.2 Proposed Device Model

It has been previously suggested that the gate geometry modification during HEMT device design can reduce electric field at gate edge [17]. Endoh *et al.* have reported a redistribution of electric field from the gate edge towards the substrate using a staircase gate HEMT [71]. In this thesis, a filleted gate geometry, which has subdued electric field at the gate edge, has been used. To validate the claim, two $Al_{0.25}Ga_{0.75}N/GaN$ HEMT structures with (a) traditionally used rectangular gate (RG) and (b) filleted gate (FG) with a varying filleting radius (dr) have been simulated using Sentaurus-TCAD engine [65]. The electric

field at the gate edge can also be reduced using field plates (FP), wherein a metal layer in contact with the gate is laid over the passivation dielectric [72]. Hence, another set of similar simulations have been performed by incorporating the field plates to both RG and FG structures (discussed in the subsequent chapters). The device geometry of the simulated HEMTs are shown together in Fig. 3.6, wherein all the gate shapes under consideration, are exhibited. All the devices have an effective gate length of 1.5 μm, gate-to-source and gate-to-drain spacing of 1.5 μm and 3 μm, respectively. For FG HEMT structure, a gate filleting or rounding radius (dr) of 0.02, 0.05 and 0.07 μm have been employed. Henceforth, in all the references to the gate shape, the nomenclature would be $RG = dr0$; $dr = 0.02$ μm $= dr2$; $dr = 0.05$ μm $= dr5$; $dr = 0.07$ μm $= dr7$. The filleted gate is also collectively referred as FG HEMT and it refers to the entire group of such devices unless a special distinction is indicated. RG HEMT refers to HEMTs with a vertical gate edge ($dr = 0$). Another device group, in which field plate has been incorporated is referred to as rectangular gate with field plate as $RGFP$ and filleted gate with field plate as $FGFP$. The filleting radius of $FGFP$ is the same as mentioned above for FG HEMTs. Beyond $dr = 0.07$ μm, a slant gate would be preferable approach as the numerical values of results obtained in this thesis starts saturated and no major changes are observed (between $dr5$ and $dr7$ variants of FG and $FGFP$ gate type, refer Table 4.1, in the next Chapter, Section 4.2). Hence, simulations are not performed beyond $dr = 0.07$ μm. The field plate lengths of 0.5, 0.7, 1.0 and 1.5 μm are considered in the simulations, for both the RG and FG HEMT, however, the peak local electric field at the right gate edge on the drain side is not much sensitive to the field plate length variation. Hence, the results of a field plate for a length 1.0 μm are reported in this thesis. The proposed structure is shown in Fig. 3.6. Table 3.1 lists the parameters of the device that has been used in the simulation.

3.2.1 Simulation Setup

The initial simulations on the above mentioned structures have been performed using drift diffusion (DD) model. In this model, drift diffusion, continuity and Poisson's equations

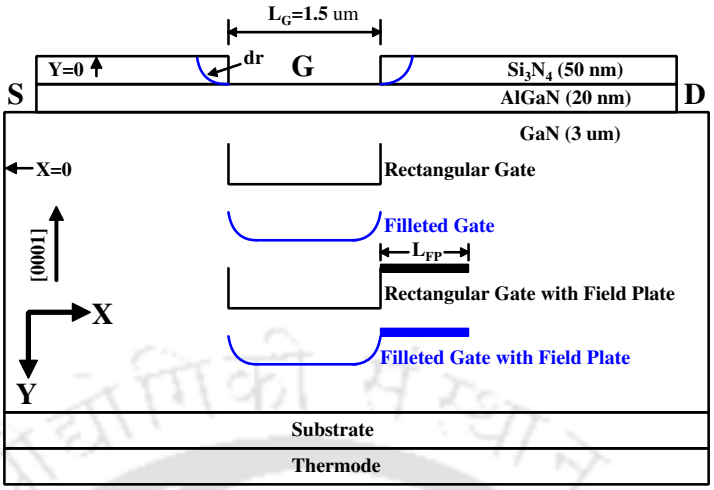

Figure 3.6: Simulated HEMT device structures showing the rectangular and filleted gate geometries with and without field plate. The gate length of the device is 1.5 μm, gate-to-source and gate-to-drain spacing is 1.5 μm and 3 μm, respectively. The gate footprint (gate length) has been held constant to a value of 1.5 μm irrespective of the filleting radius.

are solved at each mesh point of the device structure [73]. The DD model is computationally less intensive and produces reasonably accurate results. However, the limitation of this model is that it cannot exhibit effects like self-heating and predict electron temperature in a device. The main objective behind performing DD simulation is to obtain current-voltage (I-V) characteristics exhibiting the difference in currents due to variation in piezoelectric polarization because of gate shaping. Another consideration in this thesis is the variation of carrier temperature in the device. Since HEMT is a heterostructured device, an energy transfer takes place across the interface. To model this phenomenon, a hydrodynamic carrier transport model is employed [69]. Hence, the carrier energy distribution is extracted in the proposed and conventional device structures using this model to understand the role played by hot electrons in affecting the device performance. The electron temperature results thus obtained showcases the actual carrier temperature. This helps in understanding the degradation mechanisms which are initiated by carriers having a high temperature.

Typically, high current flows through HEMT channel, which results in a significant Joule heating (popularly known as self-heating). This necessitates the use of thermodynamic transport model [74] to perform coupled electro-thermal calculations over the device region.

Table 3.1: Device parameters used in TCAD simulation

Description	Parameter	Dimension
Gate Length	L_G	1.5 μm
Source to Gate Spacing	L_{SG}	1.5 μm
Gate to Drain Spacing	L_{GD}	3.0 μm
Field Plate Length	L_{FP}	1 μm
Fillet Radius	dr	0.0 - 0.07 μm
Thickness of Si_3N_4 layer	$t_{Si_3N_4}$	50 nm
Thickness of AlGaN layer	t_{AlGaN}	25 nm
Thickness of GaN layer	t_{GaN}	3.0 μm
Thickness of Substrate layer	t_{SUB}	0.5 μm

Electron concentration affects heating which affects electron concentration subsequently, hence, thermodynamic transport model uses a set of coupled device equations along with lattice heat flow equation to perform device simulation. This approach aids in understanding the influence of internal device temperature on basic physical phenomena, such as, Shockley-Read-Hall (SRH) generation-recombination, carrier mobility, and avalanche generation. An equivalent thermal boundary resistance of 3.3×10^{-4} cm^2KW^{-1} is employed at thermode contact [75]. The source and drain contacts are set as Ohmic. The gate is considered to form a Schottky contact (gate metal work-function = 5.2 eV) on AlGaN barrier layer. Recombination–generation model for heat is employed to account for the heat generated during recombination and generation process. Temperature-dependent thermal conductivity model, carrier density with no band-gap narrowing, Shockley generation-recombination as a function of doping and temperature are employed as well. Anisotropic model is incorporated to account for asymmetry along *c*-axis, which also happens to be the growth axis (Ga-face [0001] direction) of GaN crystal structure. The polarization model is activated for charge generation at AlGaN/GaN hetero-interface. Additional gate-dependent polarization is included in the simulation to account for adjusting the polarization charge due to

converse piezoelectric effect. Deep acceptor type traps having a uniform concentration of 5 $\times 10^{16}$ cm^{-3} located at 0.9 eV above the valance band are used in GaN buffer [76]. This concentration of acceptor traps in GaN helps to create a semi-insulating GaN buffer [77]. In the AlGaN layer, a uniform donor type trap concentration of 5 $\times 10^{13}$ cm^{-3} located at 1 eV below conduction band is used [78]. For estimating CPE strain, following equation (expressed in the strain-charge form) is considered.

$$[\varepsilon_i]_{6\times1} = [d_{ij}]_{6\times3}\,[E_j]_{3\times1} \qquad (i = 1, 2, ..., 6; j = 1, 2, 3) \tag{3.1}$$

where, ε is a dimensionless strain matrix; d is the CPE coefficient (m/V), and E is the applied electric field (V/m) [69]. The device structure, along with dimensions and simulation coordinates, is shown in Fig. 3.6, in which Y-axis runs through the (negative) c-axis and X-axis lies in the basal plane. The voltage bias for the simulation are: V_{DS} is ramped to 20 V, whereas V_{GS} is kept as – 6/0 V for simulating HEMT OFF/ON state, respectively. The devices are intentionally driven to ON/OFF state stress to increase the density of existing traps [31]. Since *RG* HEMT has a corner, there can be a singularity in the simulation result. The meshing around corners play a significant role and it is suggested in [46] to observe results at a distance greater than 3 Å from the corners at the interface. All the graphs (X-Y plots) presented in this paper have been obtained by performing a cutline along the channel (Y- cut) at a distance of 2 nm below the SiN/AlGaN interface in AlGaN layer. This thesis aims to perform a physics based TCAD device simulation to understand degradation mechanism that has been practically observed. We also aim at minimizing degradation promoting mechanism employing gate shaping approach.

4

Converse Piezoelectric Phenomena

Contents

Piezoelectricity is the best known form of electromechanical coupling. It was discovered by Jacques and Pierre Curie in the year 1880. They proposed that when pressure is applied to certain crystals, charges of opposite nature develop on its opposite surface. Few examples of such crystals are zinc blende, quartz and Rochelle salt. There are two forms of piezoelectricity, direct and indirect (converse). In case of direct piezoelectricity, an electric polarization develops on the faces of the crystal which is directly proportional to the mechanical strain applied on it [79]. The indirect effect occurs when a crystal develops a strain upon application of an electric field to its faces. Equation 4.1 and 4.2 represents the direct and indirect (converse piezoelectric) effect, respectively.

$$P_i = e_{ijk}\epsilon_{jk} \tag{4.1}$$

$$\epsilon_{ij} = d_{ijk}P_k \tag{4.2}$$

Where, P stands for the polarization, ϵ denotes the strain tensor, e is the piezoelectric constant and d is the piezoelectric moduli. To deduce the constitutive equation for electromechanical effect in a semiconductor, it is considered to be a dielectric in which the change in total energy stored can be mentioned as

$$\begin{aligned} dU &= dU^{mech} + dU^{elect} \\ &= \Theta dS + \sigma_{ik}d\epsilon_{ik} + E_i dD_i \end{aligned} \tag{4.3}$$

where, Θ stands for temperature, the change in entropy is denoted by dS, σ_{ik} is stress, ϵ_{ik} is the strain, E is the electric field and dD is the change in electric displacement vector. To proceed with the derivation, electric enthalpy, H, is depicted as,

$$H^{elect} = U - E_i D_i \tag{4.4}$$

where U is the total internal energy. The equation has to meet the condition mentioned below.

$$dH^{elect} = \Theta dS + \sigma_{ik}d\epsilon_{ik} - D_i dE_i \tag{4.5}$$

Now, differentiating Eq.4.5, by chain rule, the following is obtained.

$$e_{ikl} = \left(\frac{\partial D_i}{\partial \epsilon_{kl}}\right)_E = -\left(\frac{\partial^2 H^{elect}}{\partial \epsilon_{kl}\partial E_i}\right) = -\left(\frac{\partial^2 H^{elect}}{\partial E_i \partial \epsilon_{kl}}\right) = -\left(\frac{\partial \sigma_{kl}}{\partial E_i}\right)_E \tag{4.6}$$

The electric permittivity as

$$K_{ik}^{\sigma(\epsilon)} = \left(\frac{\partial D_i}{\partial E_k}\right)_{\sigma(\epsilon)} \tag{4.7}$$

and elastic (stiffness) coefficient as,

$$C_{klmn}^{D(E)} = \left(\frac{\partial \sigma_{kl}}{\partial \epsilon_{mn}}\right)_{D(E)} \tag{4.8}$$

The physical parameters $\sigma(\epsilon)$ and $D(E)$ in Eq. 4.7 and Eq. 4.8, respectively are held constant while performing the differentiation. In a condition where both electric field and strain are absent, and only physical component present being the spontaneous polarization, then the contribution of P^{sp} to electric displacement can be denoted as,

$$\begin{aligned} D_i &= P_i^{sp} + \left(\frac{\partial D_i}{\partial E_k}\right)_\epsilon E_k + \left(\frac{\partial D_i}{\partial \epsilon_{kl}}\right)_E \epsilon_{kl} \\ &= P_i^{sp} + K_{ik}^{\epsilon} E_k + e_{ikl}\epsilon_{kl} \end{aligned} \tag{4.9}$$

$$\begin{aligned} \sigma_{kl} &= \left(\frac{\partial \sigma_{kl}}{\partial E_i}\right)_\epsilon E_i + \left(\frac{\partial \sigma_{kl}}{\partial \epsilon_{mn}}\right) \epsilon_{mn} \\ &= -e_{ikl}E_i + C_{klmn}^{E}\epsilon_{mn} \end{aligned} \tag{4.10}$$

The above equations (Eq. 4.9 and 4.10) are employed to understand and analyze electromechanical effects in semiconductors [79]. The interplay among various parameters relevant to electromechanical coupling of crystals can be summarized as shown in Fig. 4.1.

4.1 Converse Piezoelectric Related Degradation

Recent advancement in AlGaN/GaN technology has resulted in the aggressive adoption of HEMTs in commercial high power and high-speed devices [80]. However, several reliability issues have been limiting the full potential of AlGaN/GaN HEMTs [20, 81]. One of the critical reliability issues in AlGaN/GaN HEMTs is the generation of converse piezoelectric (CPE) strain in AlGaN barrier layer. During the OFF state operation, traditionally used

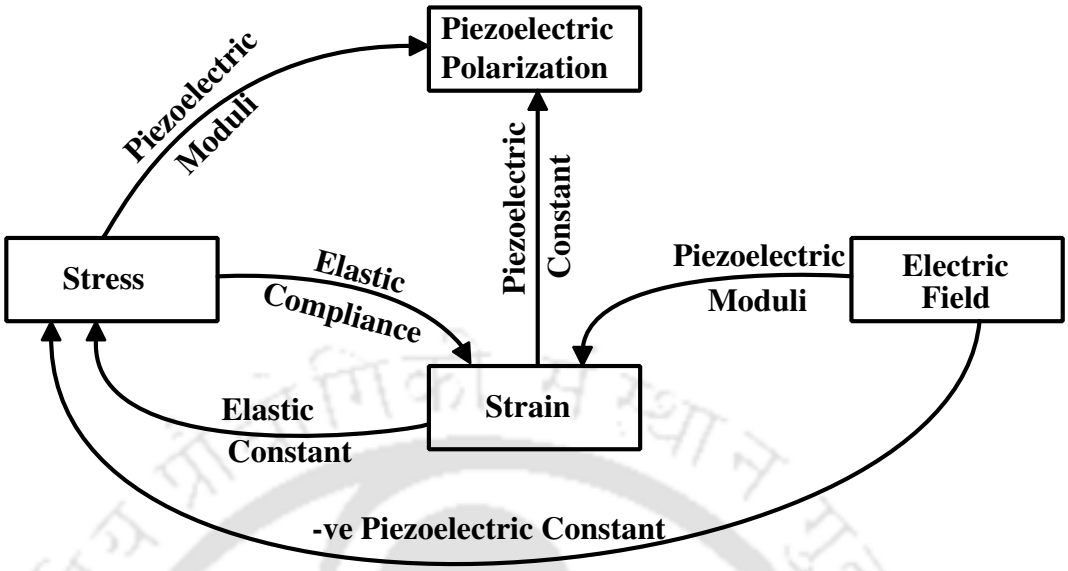

Figure 4.1: Relation between various physical parameters related to the electromechanical coupling in a crystal [2].

rectangular gated HEMTs suffer from the presence of a high electric field at the gate edge on the drain side. This strong electric field under gate gives rise to a CPE strain in AlGaN barrier layer [17, 27]. Due to CPE strain, when stored elastic energy in AlGaN barrier layer increases significantly above a critical value, AlGaN layer relaxes by the formation of crystallographic defects. These additional defects act as charge-trap centres in AlGaN barrier layer [17, 28]. Furthermore, the presence of a strong electric field can fill those traps with electrons, thereby lowering the 2DEG density and reducing the drain current during HEMT ON state operation [29]. The CPE strain induced defects can also introduce a leakage path between the gate and the channel, thus, increasing the gate leakage current [30]. In the worst case scenario, the CPE strain induced defects can also lead to permanent failure of HEMT [17, 29]. Thus, framing guidelines to reduce CPE strain in future high power AlGaN/GaN HEMTs is necessary.

In this Chapter, the aim is to reduce CPE strain in AlGaN/GaN HEMTs by adopting a gate geometry modification. Simulations have been performed on 2D HEMT structures to analyse the distribution of electric field and CPE strain under the gate. A filleted gate geometry is shown to outperform other gate geometries in reducing CPE strain in AlGaN barrier layer.

The analysis reported in this thesis highlights the importance of modifying gate geometry to mitigate CPE strain induced damages in future AlGaN/GaN HEMTs. Both AlGaN and GaN belong to wurtzite family and they are piezoelectric materials. They exhibit piezoelectric and converse piezoelectric effects. The piezoelectric effect occurs due to (residual/inbuilt) strain, whereas, CPE develops by application of electric field in these materials [17]. The effect of both of these phenomena is the creation of strain in the device. It has been pointed out that a 0.076% increase in uniaxial strain decreases the critical voltage of the device from 25 to 20 V [51]. Converse piezoelectric effect adds to already present piezoelectric strain and has been found to affect not only AlGaN/GaN HEMT [17,28] but AlGaN/GaN Schottky barrier diodes as well, in which donor like traps are created in the GaN layer [49]. The co-existence of high vertical electric field along with high current and high working temperatures are the main contributors that initiate defect creation in the heterostructured devices [46]. All of these physical effects are present together in an energized device. This thesis aims to reduce the CPE in AlGaN layer by tailoring vertical electric field as lateral electric field does not create large scale degradation [45].

4.1.1 Modelling CPE in AlGaN/GaN HEMT

During growth, both GaN and AlGaN crystallize in hexagonal closed packaging (HCP) structure and have different lattice constants in the unstrained state. For device applications, an AlGaN layer is grown on the top of a thick GaN layer. Since both the materials are of HCP family, they share a common growth axis, also called as c-axis around which there exists a rotational symmetry on all six sides of the hexagonal structure (in the basal plane). When an AlGaN layer is grown above the underlying GaN, the lattice constant of the AlGaN needs to increase to match the lattice constant of the relaxed GaN (thick layer); as a result AlGaN layer comes under the influence of strain in the basal plane (xy-plane). The strain in x and y directions are denoted as ϵ_1 and ϵ_2, respectively. Due to symmetry of the crystal in the basal plane, strain redistributes itself uniformly in x and y directions, hence, $\epsilon_1 = \epsilon_2$ [82].

The basal plane strain in an AlGaN/GaN layered structure is estimated by using Eq. 4.11.

$$\epsilon_1 = \frac{a - a_0}{a_0} \tag{4.11}$$

where, a and a_0 are the unstrained lattice constants of GaN and AlGaN, respectively. This strain is responsible for producing piezoelectric effect. For a wurtzite crystal, only five piezoelectric constants (responsible for transforming strain to piezoelectric polarization) are nonzero, which is exhibited in the matrix form below.

$$e = \begin{pmatrix} 0 & 0 & 0 & 0 & e_{15} & 0 \\ 0 & 0 & 0 & e_{15} & 0 & 0 \\ e_{31} & e_{31} & e_{33} & 0 & 0 & 0 \end{pmatrix} \tag{4.12}$$

The crystal structure symmetry makes constants $e_{24} = e_{15}$ and $e_{32} = e_{31}$ equal, hence, they have already been replaced by their counterparts in the above matrix. In actual HEMT device, the piezoelectric constant e_{15} is related to the polarization induced by shear strain. Since this does not contribute to the polarization, hence, it is assumed to be zero [82]. Finally, the strain matrix relevant to AlGaN/GaN HEMT can be denoted as,

$$e = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ e_{31} & e_{31} & e_{33} & 0 & 0 & 0 \end{pmatrix} \tag{4.13}$$

For estimating piezoelectric polarization field, only three nonzero elements e_{31}, e_{31}, e_{33} are needed [2], as mentioned in Eq. 4.13. These nonzero constants in combination with the basal plane strain can be used to obtain piezoelectric polarization vector along the c-axis. Using the piezoelectric constants, e_{31} and e_{33}, and $\epsilon_1 = \epsilon_2$, the nonzero component of the piezoelectric polarization vector along the c-axis (P_3^{pz}) can be stated as shown in Eq. 4.14.

$$\begin{aligned} P_3^{pz} &= e_{31}(\epsilon_1 + \epsilon_2) + e_{33}\epsilon_3 \\ &= 2e_{31}\epsilon_1 + e_{33}\epsilon_3 \end{aligned} \tag{4.14}$$

Since the basal plane strain is already known, Eq. 4.14 needs to be modified to express the piezoelectric polarization vector along the c-axis (P_3^{pz}) only in terms of ϵ_1. Interestingly, the strain ϵ_1 and ϵ_3 are related, so this relation is employed to eliminate (ϵ_3) from Eq. 4.14. The relation between ϵ_1 and ϵ_3 can be depicted in Eq. 4.15.

$$\epsilon_3 = -2\frac{C_{13}}{C_{33}}\epsilon_1 \tag{4.15}$$

where, C_{13} and C_{33} are the stiffness constants of the crystal. Using the value of ϵ_3 from Eq. 4.15 and replacing it in Eq. 4.14, the final expression for polarization vector in the c-axis can be formulated as shown in Eq. 4.16.

$$P_3^{pz} = 2\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right)\epsilon_1 \tag{4.16}$$

The polarization vector P_3^{pz} of Eq. 4.16 is responsible for creating piezoelectric polarization and acts along the c-axis. This piezoelectric polarization adds to spontaneous polarization to create charge at the interface of AlGaN/GaN heterostructure. It is to mention that Eq. 4.16 is an uncoupled equation as it does not include electromechanical effect (converse piezoelectric effect) which arises due to vertical electric field at the gate edges. Therefore, to account for the presence of an electric field at the gate edges, additional CPE needs to be incorporated in Eq. 4.16 to make it fully coupled [83]. In addition to strained AlGaN layer already present, CPE creates additional strain in AlGaN, which is additive. The CPE is responsible for the device degradation and failures [17, 28, 30, 49, 51]. Work presented in this thesis, focuses on reducing this converse piezoelectric polarization which has its roots in the high electric field at the gate edges. For incorporating the effect of CPE in an AlGaN/GaN system, a relation between strain and stress has to be utilized, in which an additional term corresponding to the stress arising because of electric field has to be added. Using Vigot's notation, an expression to address the above mentioned issue can be described below [83].

$$\sigma_i = C_{ij}\epsilon_j - e_{ki}E_k \qquad (i,j = 1,2,...,6; \quad k = 1,2,3) \tag{4.17}$$

where, σ is the stress; ϵ is the strain; e is the piezoelectric constant and E is the electric field. Using Eq. 4.17 and later applying simplifying assumption of clamped model [83], the planar stress, can be modeled as,

$$\sigma_2 = \sigma_1 = (C_{11} + C_{12})\epsilon_1 + C_{13}\epsilon_3 - e_{31}E_3 \tag{4.18}$$

where, E_3 is the vertical electric field. From Eq. 4.18, in order to eliminate ϵ_3, the equation for the stress along the c-axis (σ_3) needs to be expressed using Eq. 4.17. It is assumed that the stress along the c-axis, (σ_3), in AlGaN is zero. Hence, $\sigma_3 = 0$ and the resultant equation is,

$$\sigma_3 = 0 = 2C_{13}\epsilon_1 + C_{33}\epsilon_3 - e_{33}E_3 \tag{4.19}$$

Rearranging Eq. 4.19 to obtain strain along the c-axis,

$$\epsilon_3 = -2\frac{C_{13}}{C_{33}}\epsilon_1 + \frac{e_{33}}{C_{33}}E_3 \tag{4.20}$$

In the absence of a vertical electric field (E_3), it is to mention that only first term in Eq. 4.20 is dominant and is negative. This depicts that the system (along the z-axis) is under compressive strain because of tensile basal strain in AlGaN in the x and y directions. Using the expression for ϵ_3 from Eq. 4.20 and replacing ϵ_3 in Eq. 4.18, the expression for planar stress including the CPE can be depicted as,

$$\sigma_2 = \sigma_1 = \left(C_{11} + C_{12} - 2\frac{C_{13}^2}{C_{33}}\right)\epsilon_1 + \left(\frac{C_{13}}{C_{33}}e_{33} - e_{31}\right)E_3 \tag{4.21}$$

4.2 Moderation of CPE Using Filleted Gate HEMT

The proposed device structure along with all the gate shape and field plate combinations used for the numerical analysis are exhibited in Fig. 4.2. The device dimensions and simulation coordinates are indicated on the proposed structures. When gate bias is held at zero or is reversed biased, the vertical electric field (E_3) is positive. This further adds to the planar strain (σ_1 and σ_2), since $e_{31} < 0$, $e_{33} > 0$ and all C_{ij} are positive [30, 69]. Since the electric field for a RG HEMT is higher at the gate edges, the planar strain becomes higher,

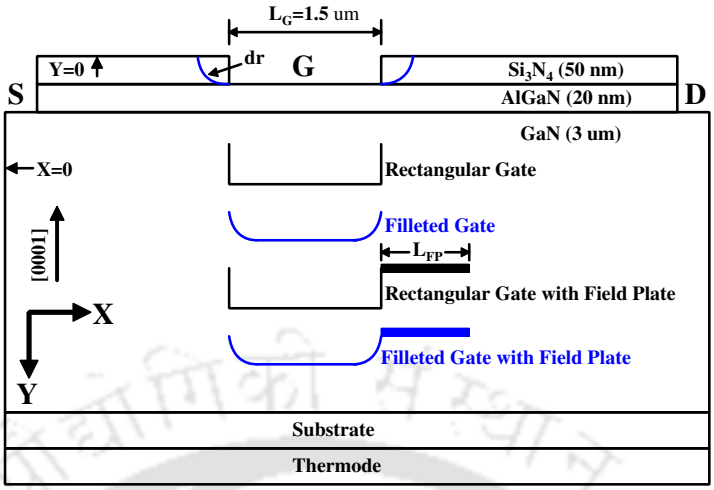

Figure 4.2: Simulated HEMT device structures showcasing rectangular and filleted gate geometries with and without field plate. The gate length of the device is 1.5 μm, gate-to-source and gate-to-drain spacing is 1.5 μm and 3 μm, respectively. The gate footprint (gate length) is held constant to 1.5 μm irrespective of the filleting radius.

which in combination with self-heating acts as a centre point for initiating all degradation mechanism. This increased planar strain also increases the piezoelectric polarization for a *RG* HEMT, and due to this, it has the highest current. This can be validated from the I − V characteristic as shown in Fig. 4.3 which compares the drain current for various filleting radii of the gate. Figure 4.4 (a) and (b) exhibits $I_D - V_G$ characteristics of the HEMTs having similar threshold voltage. Since *FG* HEMTs have a lower vertical electric field (E_3), the total strain including CPE is low, because of which the total piezoelectric polarization in these gates is less. This may be confirmed by a lower drain current as shown in Fig. 4.3. Due to the reduction in electric field at the edges, *FG* HEMTs have a lower localized strain at the gate edges. Therefore, higher reliability is expected from them. Since the spontaneous polarization contributes a major fraction to the total charge at the interface (in 2DEG) as compared to the piezoelectric polarization, even though there is a large change in the electric field, the current changes only by a fraction. Due to the gate shaping, it is seen that the CPE strain diffuses as well as reduces significantly. Table 4.1 lists reduction of CPE and electric field because of gate shaping as well as introduction of FP on RG and FG HEMTs.

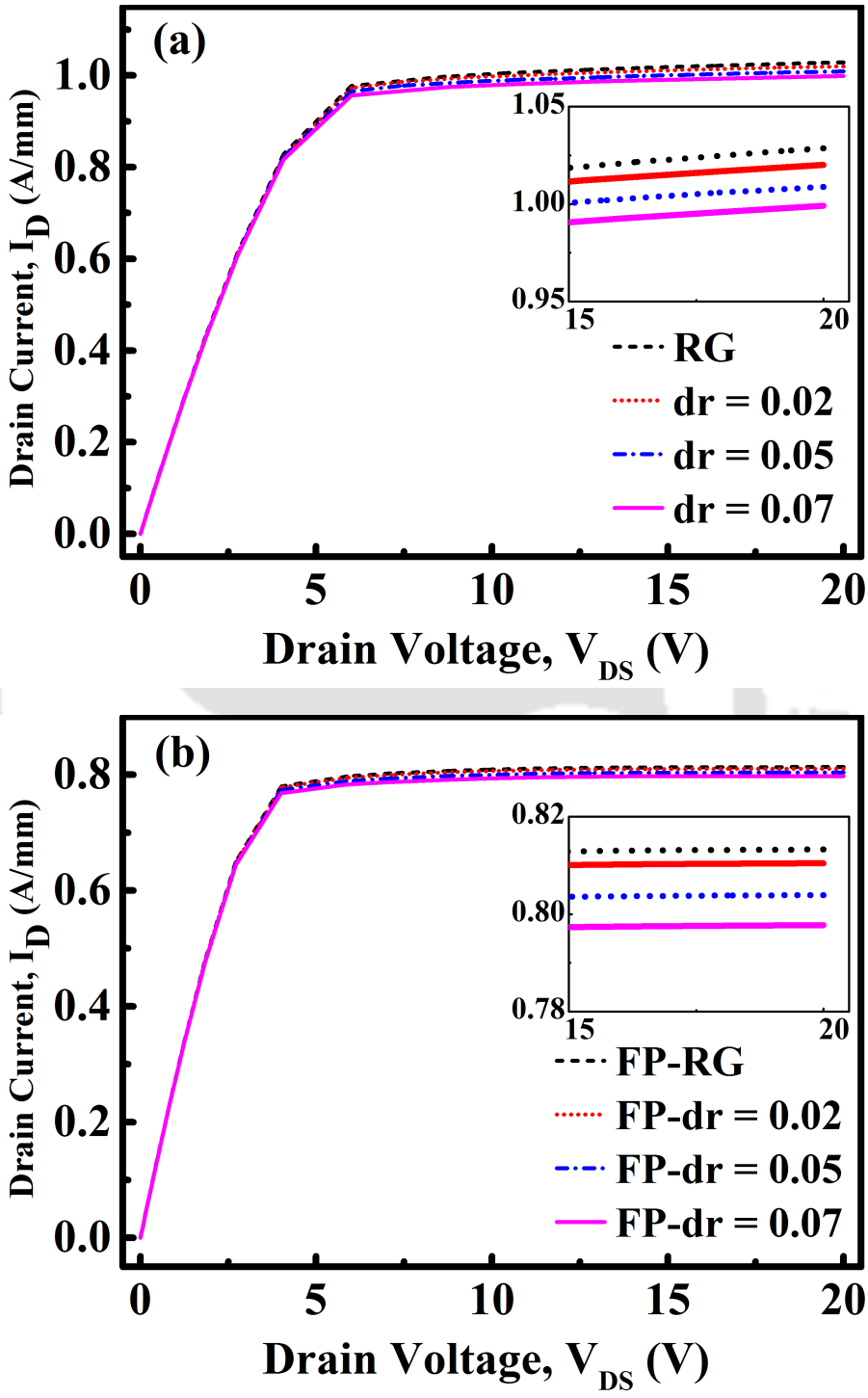

Figure 4.3: ON state I – V characteristic for (a) HEMT without FP and (b) with FP, at a bias of $V_G = 0$ V and $V_{DS} = 20$ V, respectively. The drain current varies due to change in filleting radius. Inset showing zoomed section of I – V from V_{DS} of 15 V to 20 V.

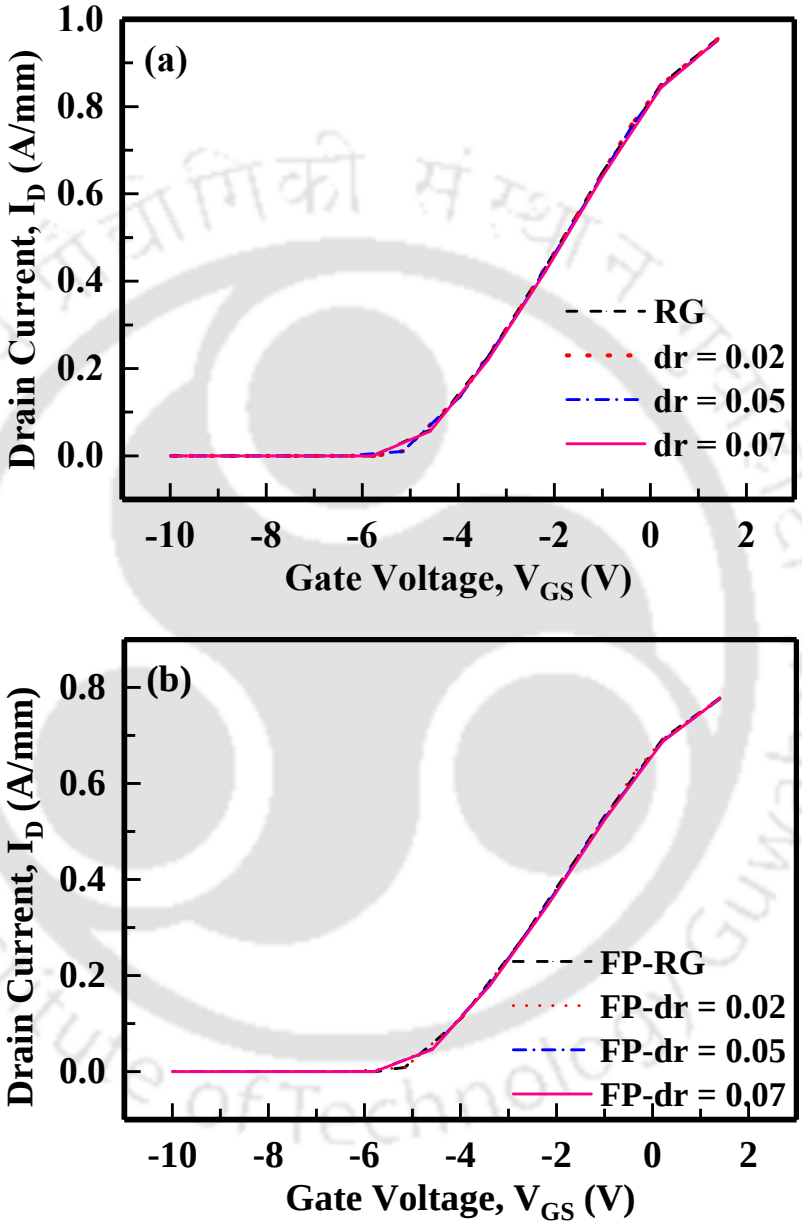

Figure 4.4: $I_D - V_G$ characteristic for (a) HEMT without FP and (b) with a FP length of 1 μm. The drain current shows minimal variation due to change in filleting radius and incorporation of field plate. The gate bias, (V_{GS}) has been swept from – 10 to 1.5 V at a constant drain bias, (V_{DS}) of = 5 V.

Table 4.1: Comparison of peak electric field and CPE strain observed in different HEMT gate geometries for with and without field plate obtained by a Y-cut.

Gate Type	State	Parameter	***RG***	***dr2***	***dr5***	***dr7***
Without FP	OFF	$E_{Vertical}$ (MV/cm)	-9.42	-6.29	-5.21	-5.20
		CPE – YY (10^{-3})	3.46	2.31	1.92	1.91
		CPE – ZZ (10^{-3})	-1.62	-1.09	-0.9	-0.88
	ON	$E_{Vertical}$ (MV/cm)	-6.49	-4.41	-3.68	-3.64
		CPE – YY (10^{-3})	2.39	1.62	1.35	1.34
		CPE – ZZ (10^{-3})	-1.12	-0.761	-0.636	-0.627
With FP	OFF	$E_{Vertical}$ (MV/cm)	-7.50	-5.35	-4.64	-4.62
		CPE – YY (10^{-3})	2.76	1.97	1.70	1.69
		CPE – ZZ (10^{-3})	-1.29	-0.92	-0.80	-0.79
	ON	$E_{Vertical}$ (MV/cm)	-3.09	-2.31	-2.09	-2.08
		CPE – YY (10^{-3})	1.13	0.85	0.77	0.76
		CPE – ZZ (10^{-3})	-0.53	-0.40	-0.36	-0.35

Table 4.2: Comparison of peak lateral electric field as observed in different HEMT gate geometries without field plate obtained by a Y-cut.

Gate Type	State	Parameter	***RG***	***dr2***	***dr5***	***dr7***
Without FP	ON	$E_{Lateral\ left\ gate\ edge}$ (MV/cm)	0.91	0.46	0.32	0.32
		$E_{Lateral\ right\ gate\ edge}$ (MV/cm)	-4.74	-2.55	-1.85	-1.76
	OFF	$E_{Lateral\ left\ gate\ edge}$ (MV/cm)	2.93	1.51	1.03	1.00
		$E_{Lateral\ right\ gate\ edge}$ (MV/cm)	-7.02	-3.81	-2.82	-2.72

Table 4.3: Extracted value of different parameters in GaN region for various device structures without FP *(the indicated results are integrated values of the physical parameters in GaN).*

Region	Parameter	*RG*	*dr2*	*dr5*	*dr7*
GaN	Piezo Charge (10^6 μ^{-1})	-1.8232	-1.8231	-1.8219	-1.8214
	Current Density–X (10^{-3} A)	-6.1445	-6.0923	-6.0258	-5.9682
	eDensity (10^5 μ^{-1})	8.4403	8.3602	8.3475	8.2800

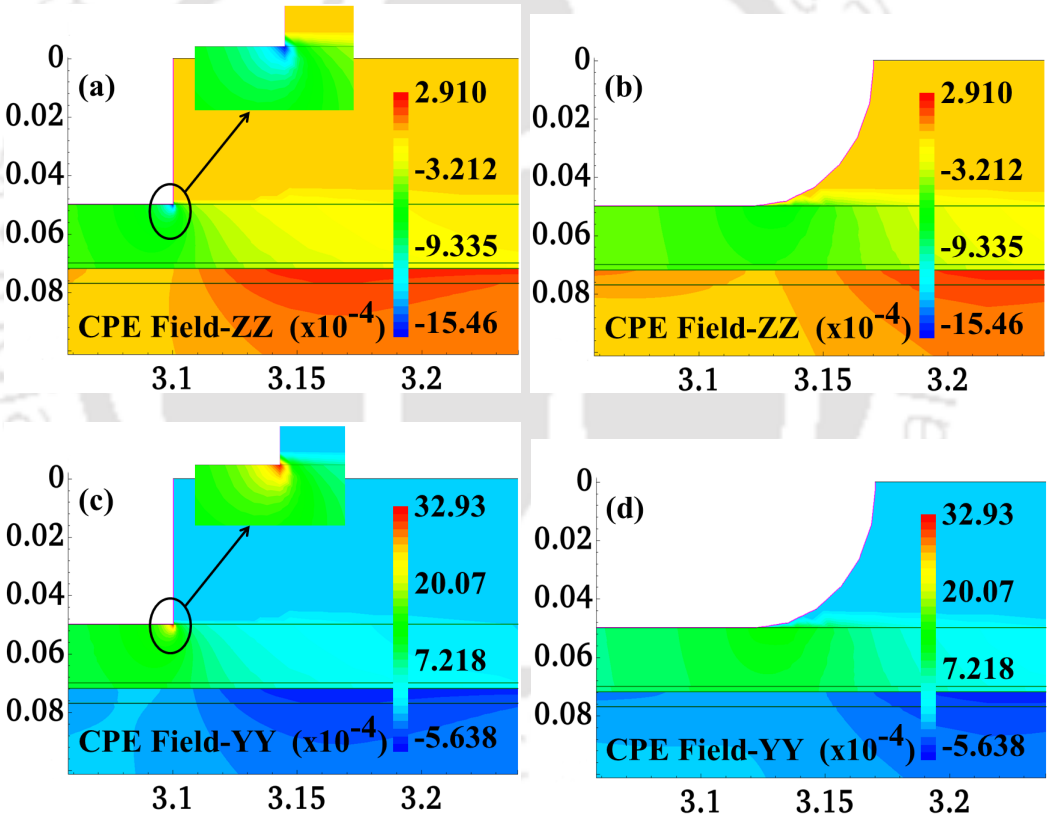

Figure 4.5: Figure exhibiting ON state CPE field for HEMTs without FP (bias condition: V_{GS} = 0 V and V_{DS} = 20 V). Figure (a) and (b) shows compressive CPE-ZZ field for ON state in HEMTs with fillet radius of 0 and 0.07 μm, respectively. Very high compressive CPE-ZZ is observed at the gate edge towards the drain side for *RG* HEMT (see inset of Figure (a)), whereas the same field gets diffused due to gate filleting (see Figure (b)) and no localized CPE field is observed. Figure (c) and (d) corresponds to CPE-YY with dr = 0 and 0.07 μm, respectively in the ON state. Again very high tensile planar CPE-YY strain at the gate corner (see inset Figure (c)) is observed for *RG* HEMT which again reduces to a low value due to filleting (see Figure (d)).

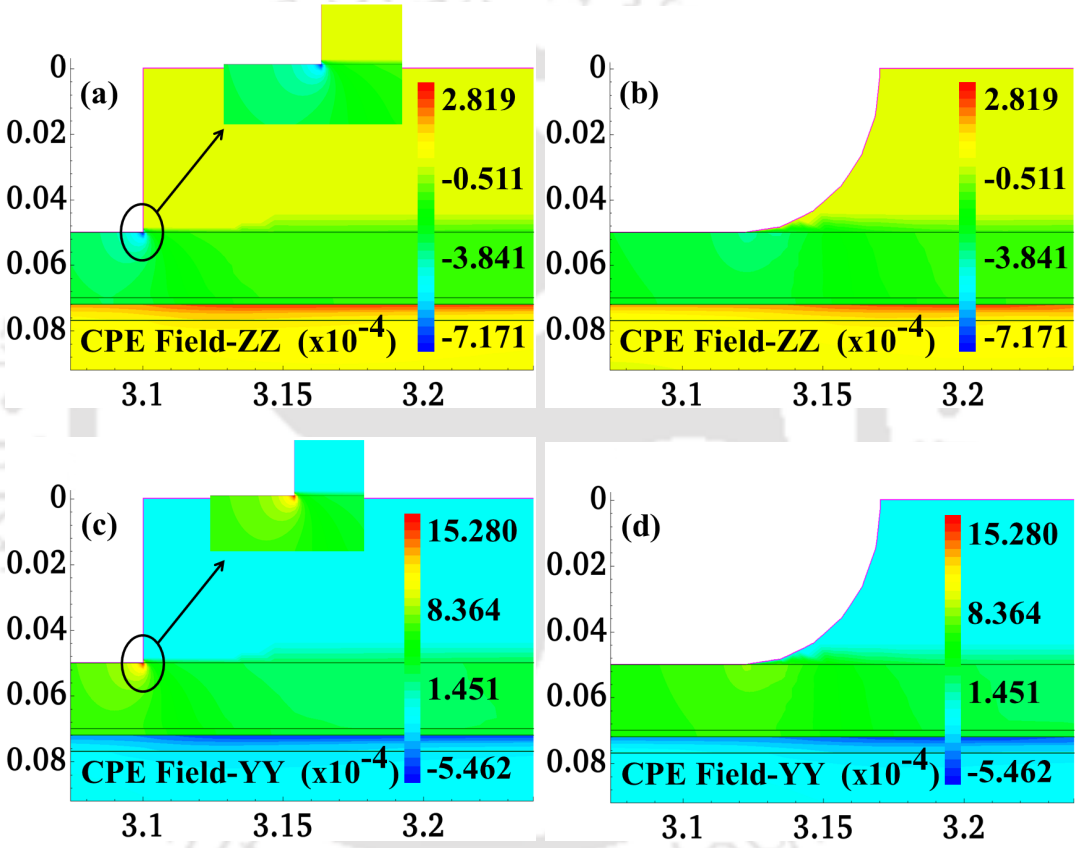

Figure 4.6: Figure showing ON state CPE field (bias condition: $V_{GS} = 0$ V and $V_{DS} = 20$ V) for HEMTs with FP. The peak CPE field at the vertical gate edge persists for $RGFP$ and diminishes for $FGFP$ HEMT.

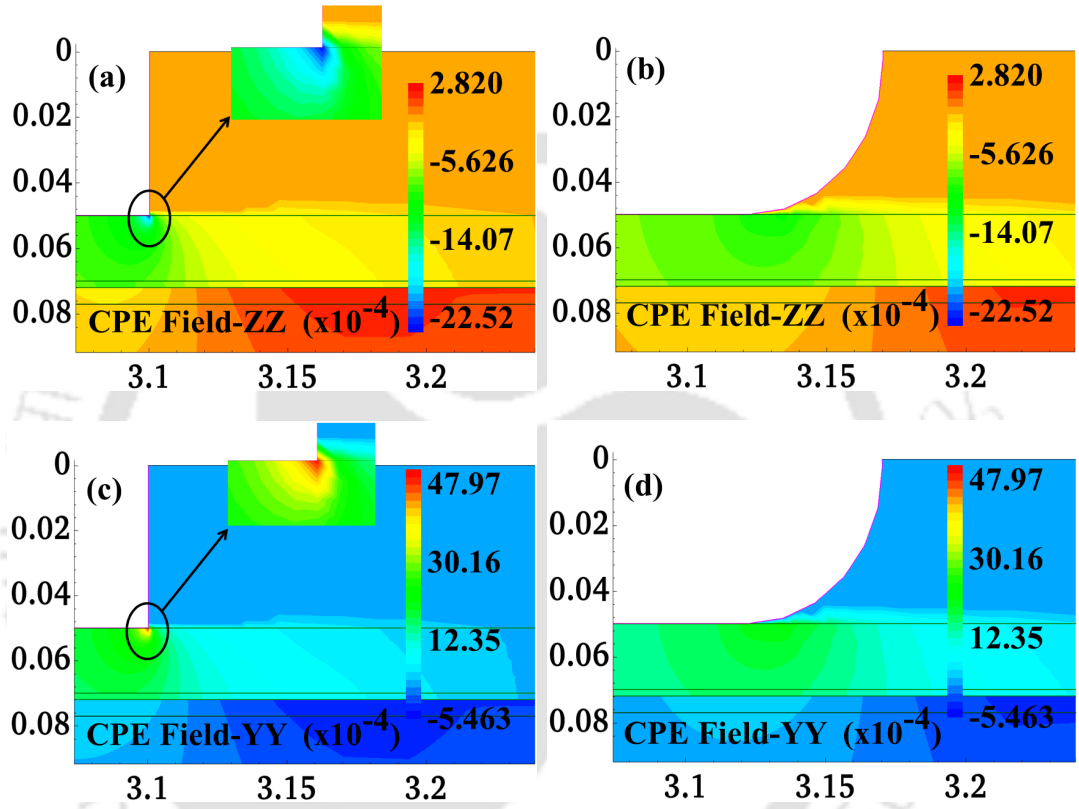

Figure 4.7: Plot corresponding to CPE field in OFF state operation with a bias of $V_{GS} = -6$ V and $V_{DS} = 20$ V for structures without FP. Figure (a) and (b) shows compressive CPE-ZZ field in HEMTs with fillet radius of 0 and 0.07 μm, respectively. Similar results with higher CPE-ZZ are observed for $dr = 0.02$ and 0.05 μm as compared to $dr = 0.07$ μm. Very high compressive CPE-ZZ is seen at the gate edge towards the drain side for *RG* HEMT in the OFF state (see inset of Figure (a)), whereas the same field gets diffused due to gate filleting (see Figure (b)). Figure (c) and (d) corresponds to CPE-YY with $dr = 0$ and 0.07 μm respectively. Again very high tensile planar CPE-YY strain at the gate corner (see inset Figure (c)) is observed for *RG* HEMT which again reduces to a low value due to filleting (see Figure (d)).

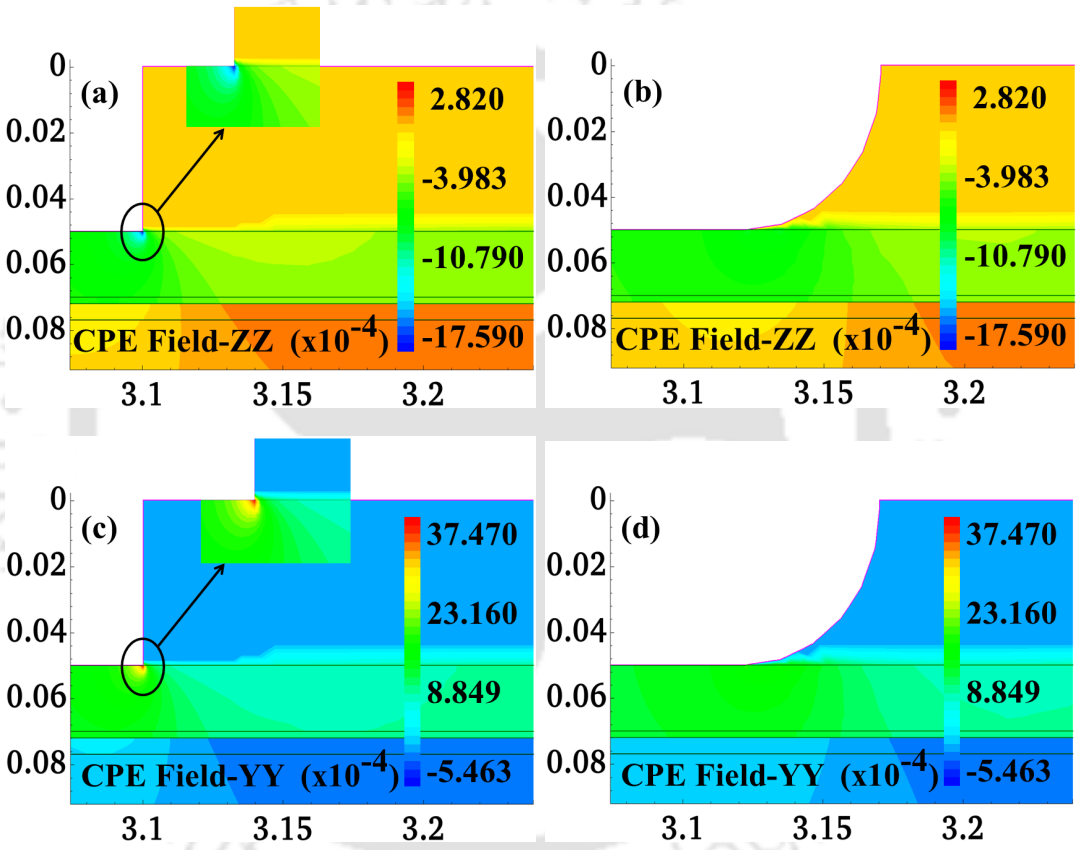

Figure 4.8: Plot corresponding to CPE field in the OFF state operation with a bias of $V_{GS} = -6$ V and $V_{DS} = 20$ V for HEMTs with FP. The peak CPE field at the vertical gate edge gets diffused due to filleting. The CPE field reduces because of the introduction of FP in both HEMT types.

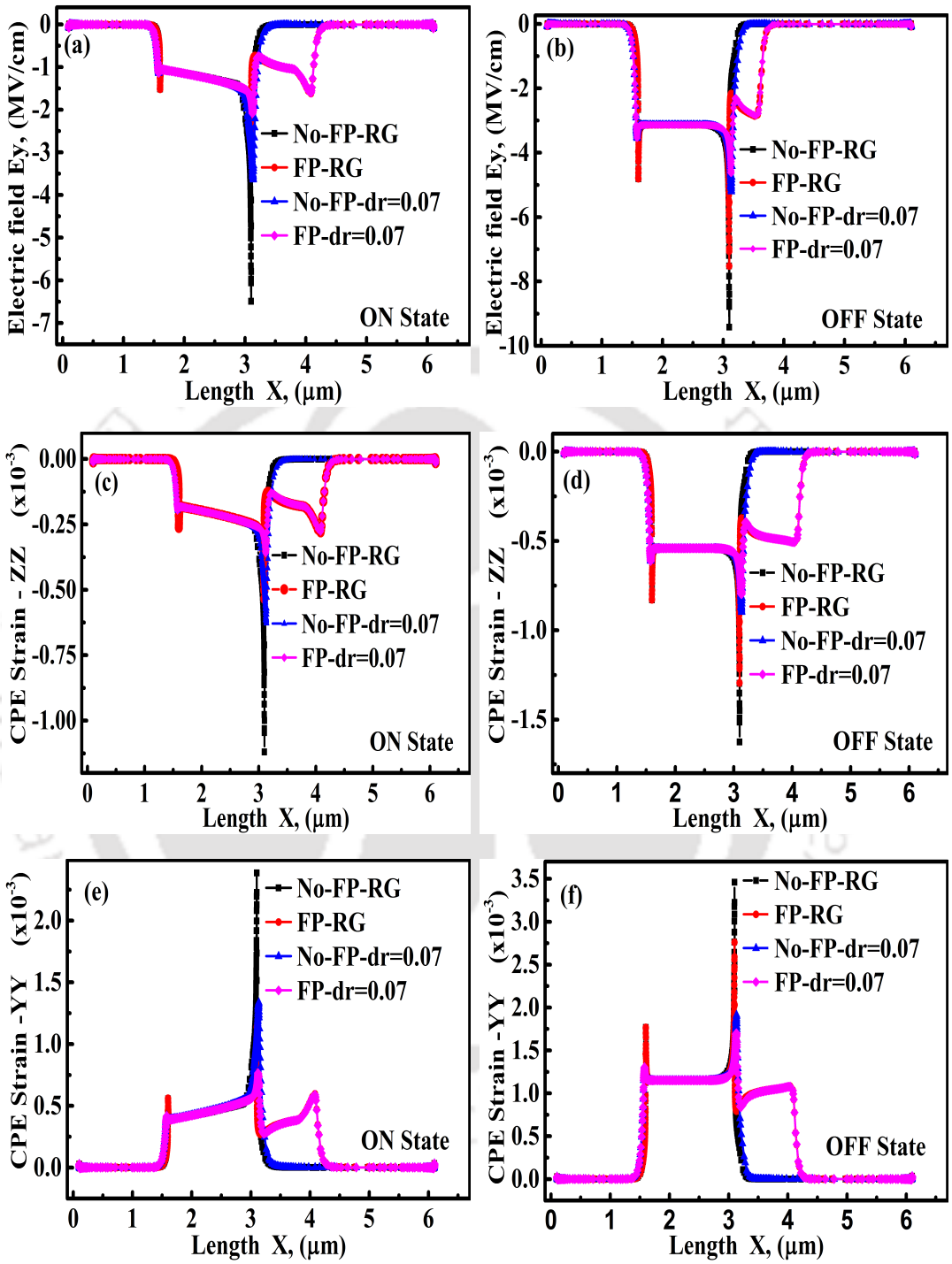

Figure 4.9: Figure (a) and (b) illustrates electric field in the ON and OFF states, respectively. Figure (c) and (d) exhibits CPE strain along *c*-axis (ZZ) in the ON and OFF states, respectively. Figure (e) and (f) depicts CPE strain along the basal plane (YY) in the ON and OFF state, respectively. Both compressive (ZZ) and tensile (YY) CPE fields increase in the OFF state. CPE field as well as electric field shows a reducing trend with the increase in filleting radius and also due to the introduction of FP. They attain the lowest value for $dr = 0.07$ μm fillet radius.

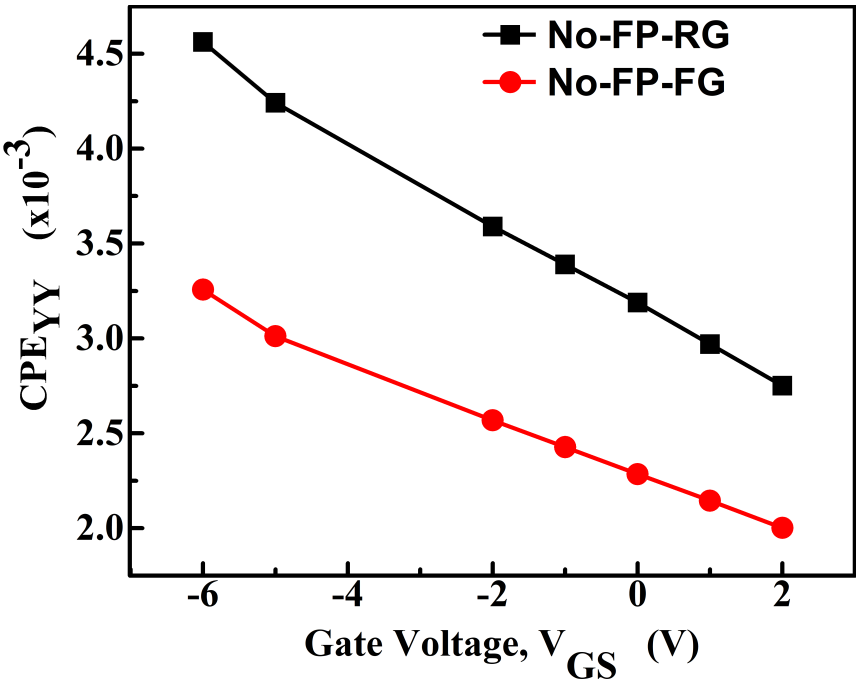

Figure 4.10: Variation of CPE *w.r.t* the gate bias while the drain bias (V_{DS}) is held at 20 V.

The peak lateral electric field for the devices without FP has been listed in Table 4.2 and it can be noted that there is a reduction in lateral electric field as the filleting radius increases. There is a trend in the reduction of the electric field, when all the parameters related to it reduce. Locally, the electric field at the gate edge on the drain side for $FGdr7$ is about 44% lower as compared to RG HEMT and CPE reduces in the same proportion according to Eq. 3.1 (refer Chapter 3). The electric field in $FGdr7$ and $FGFPdr7$ is lower by 30% and 38%, respectively as compared to $RGFP$. Filleting is the key to the reduction in peak local electric field by diffusing effect. However, when field plate is added to FG HEMT, the electric field reduces further (refer Table 4.1). Incorporating FP in a RG HEMT shrinks the local peak electric field at the gate edge, however, the field is still higher as compared to $FGdr7$. The electric field for FP HEMTs varies slowly over FP length and peaks at the end of FP. However, for $FGdr7$ HEMT without FP, the peak local electric field is lower, which would lower the CPE at the gate edge. The drain current in Fig. 4.3 (b) is lowered as compared to (a). This is because of the fact that the 2DEG concentration reduces due to trapping in AlGaN layer for HEMTs with FP, which has also been reported in [84]. Therefore, the

depletion region width in the vicinity of the gate edge is thinner in FP HEMTs, which leads to higher leakage as well as lowering the drain current [85]. It is pointed out in [46] that the degradation centres start creating defects at a localized location, where CPE strain, electron temperature, self-heating and the electric field is the highest. Since in the proposed structure, the ill effects just mentioned above are not localized but are spread out with the values lower than the peak value of either $RGFP$ or RG HEMT. Therefore, in this condition, it is expected that the local defect creation can be minimized in FG gate HEMT. It can be observed from Fig. 4.5 and 4.7 (non FP HEMTs), Fig. 4.6 and 4.8 (with FP) that the prominent peak around the gate edge is reduced significantly. It can also be seen from Table 4.3, that the physical parameters inside GaN have a direct effect on the gate shaping. Results for $dr2$ and $dr5$ are not been shown in Fig. 4.5, 4.6, 4.7 and 4.8 for brevity as the similar behaviour can be observed from Table 4.1.

Reducing trend of both CPE-YY (tensile) and CPE-ZZ (compressive) fields are observed from $dr0$ (RG HEMT) to $dr7$, with the lowest for $dr7$, hence, for comparison only $dr7$ with and without FP is fielded against RG and $RGFP$ HEMTs (as shown in Fig. 4.5, 4.6, 4.7 and 4.8). As apparent from Fig. 4.5 to Fig. 4.8, rectangular gate HEMTs have higher CPE fields at the gate edge, whereas, it diffuses for the filleted gate. A consolidated graph of CPE strain and electric field obtained in the ON/OFF state is exhibited in Fig. 4.9 for all HEMT types considered for the analysis. Either in the ON or the OFF state, the peak local electric field and CPE strain have the lowest value for $dr7$. It is also described in section 6.4 of Chapter 6 that the self-heating at the interface reduces because of filleting. Therefore, the magnitude of the degradation contributing mechanism, all of which needs to act together to degrade the device shrinks. Thus, the OFF as well as the ON state degradation is the lowest for filleted gate with $dr = 0.07$ μm. It is evident from the preceding discussion that the filleted gate without FP performs better as compared to rectangular gate HEMT with FP. Therefore, in subsequent Chapters, an attempt has been made to highlight the advantages of FG HEMTs without FP. The strain in AlGaN layer depends on the vertical electric field and is linearly dependent on it as illustrated in Fig. 4.10. The elastic energy in AlGaN

layer is proportional to square of the strain. The moment this elastic energy exceeds the threshold value, crystallographic defects gets generated, which in turn acts as trapping sites for electrons [28]. It is to mention that FG HEMT has a lower CPE as compared to RG HEMT at all the gate biases.

4.3 Summary

In this Chapter, a comparative study of electric field distribution and converse piezoelectric strain for different HEMT geometries is presented. Locally, the electric field at the gate edge on the drain side for $FGdr7$ is about 44% lower as compared to RG HEMT, and CPE reduces in the same proportion. The electric field in $FGdr7$ and $FGFPdr7$ is lowered by 30% and 38%, respectively, than $RGFP$. Filleting is the key to reduce peak local electric field by diffusing effect, however, when field plate is added to FG HEMT, the electric field reduces further (refer Table 4.1). Incorporating FP in a RG HEMT decreases local peak electric field at the gate edge, however, the field is still higher than $FGdr7$. The electric field for FP HEMTs varies slowly over FP length and peaks at the end of FP, whereas, for the $FGdr7$ HEMT without FP, the peak local electric field is lower, which reduces CPE at the gate edge. Thus, it can be concluded that the filleted gate HEMT geometry can be a potential candidate to mitigate converse piezoelectric strain induced damages in the future high power AlGaN/GaN HEMTs.

5

Hot Electron Related Issues in HEMTs

Contents

The first step in understanding any semiconductor's device physics is to know the distribution of carriers in it. This is accomplished by utilizing a well known Fermi-Dirac (FD) distribution function. This distribution function explains the distribution of electrons either in energy or in momentum space. The FD distribution function describes a system under thermal equilibrium in the presence of external influences, thus, it is necessary to put Boltzmann's transport equation (BTE) to use. BTE describes charge transport in a semi-classical approach, which implies that the transport is described by classical equations of motion and, the occurrence of collisions and scattering phenomena is described by the laws of quantum mechanics [86]. BTE including the quantum effects is expressed by the following equation given below.

$$\partial_t f + \mathbf{u}.\nabla_{\mathbf{r}} f + \frac{\mathbf{F}}{\hbar}.\nabla_{\mathbf{k}} f = C[f] \tag{5.1}$$

where $f(\mathbf{k}, \mathbf{r}, t)$ denotes six dimensional phase space distribution of carriers; $\mathbf{u}$ is the group velocity; $\mathbf{F}$ is the force exerted on carriers in the presence of magnetic and electric fields and $C[f]$ estimates change in f caused by random collision. From the above equation, the group velocity is given by,

$$\mathbf{u}(\mathbf{k}, \mathbf{r}) = \frac{1}{\hbar}\nabla_{\mathbf{k}}\varepsilon(\mathbf{k}, \mathbf{r}) \tag{5.2}$$

where, $\mathbf{u}$ represents group velocity and ε denotes kinetic energy of the carriers. The inverse of the effective mass tensor ($\otimes$ denotes tensor product) is depicted as,

$$\hat{m}^{-1}(\mathbf{k}, \mathbf{r}) = \frac{1}{\hbar}\nabla_{\mathbf{k}} \otimes \mathbf{u}(\mathbf{k}, \mathbf{r}) = \frac{1}{\hbar^2}\nabla_{\mathbf{k}} \otimes \nabla_{\mathbf{k}}\varepsilon(\mathbf{k}, \mathbf{r}) \tag{5.3}$$

When a charged particle moves in an inhomogeneous medium in the presence of both electric and magnetic field, it experiences a force. This force depends on the magnitude of wave vector, $\mathbf{k}$ and position $\mathbf{r}$ and is expressed as,

$$\mathbf{F}(\mathbf{k}, \mathbf{r}) = -\nabla_{\mathbf{r}}(E_{c,0}(\mathbf{r}) + \varepsilon(\mathbf{k}, \mathbf{r})) - q(\mathbf{E}(\mathbf{r}) + \mathbf{u}(\mathbf{k}, \mathbf{r}) \times \mathbf{B}(\mathbf{r})) \tag{5.4}$$

where, $\nabla_{\mathbf{r}}$ is responsible for accounting change at the bottom of conduction band $E_{c,0}$ and shape of the conduction band; $(\varepsilon(\mathbf{k}, \mathbf{r}))$, $\mathbf{E}$ and $\mathbf{B}$ are electric and magnetic fields, respectively.

When the influence of magnetic field is ignored, Eq. 5.4 simplifies to an electrostatic force,

$$\mathbf{F}(\mathbf{r}) = -q\mathbf{E}(\mathbf{r}) \tag{5.5}$$

BTE is computationally very intensive, therefore, its various simplifications are being readily employed in various applications. There are several other popular models based on simplified BTE and are being used to study carrier dynamics in engineering domain; notable among them are Monte Carlo (MC), Electro-thermodynamics (ET), Hydrodynamics (HD) and Drift-Diffusion (DD). Again MC is accurate, but is also computationally intensive, hence, at many times it serves as a benchmark for lesser accurate models which are popular for being fast and fairly accurate. It is to mention that a Hydrodynamic device simulation is a good approach to visualize the internal carrier dynamics considering its accuracy and also for being computationally less intensive. It is a compromise between computationally intensive Monte Carlo and Drift-Diffusion models. The DD model fails to generate accurate results as the device lengths approach towards characteristic thermal wavelength. The hydrodynamic model employs carrier temperature as an additional parameter for describing the carrier transport. This Chapter discusses hydrodynamic modelling that has been used to study the proposed structure. The HD model that has been incorporated in this thesis, is described by Eq. 5.6 and 5.7.

$$J_n = \mu_n(n\nabla E_C + kT_n\nabla n - nkT_n\nabla \ln\gamma_n + \lambda_n f_n^{td} kn\nabla T_n - 1.5nkT_n\nabla \ln\, m_n) \tag{5.6}$$

$$J_p = \mu_p(p\nabla E_V - kT_p\nabla p + pkT_p\nabla \ln\gamma_p - \lambda_p f_p^{td} kp\nabla T_p + 1.5pkT_p\nabla \ln\, m_p) \tag{5.7}$$

In the above equations, the first term ($n\nabla E_C$ and $p\nabla E_V$) estimates spatial variations of bandgap, electron affinity and electrostatic potential. The second term ($kT_n\nabla n$ and $kT_p\nabla p$) captures concentration gradient, whereas, the third term ($nkT_n\nabla \ln\gamma_n$ and $pkT_p\nabla \ln\gamma_p$) is related to Fermi statistics, where $\gamma_n = \frac{n}{N_C} exp\left(\frac{E_C - E_{F,n}}{kT}\right)$ and $\gamma_p = \frac{p}{N_V} exp\left(\frac{E_{F,p} - E_V}{kT}\right)$. The fourth term ($\lambda_n f_n^{td} kn\nabla T_n$ and $\lambda_p f_p^{td} kp\nabla T_p$) is an important part of HD model, which captures temperature gradient of the carriers. Here, constants f_n^{td} and f_p^{td} are thermal diffusion parameters. The spatial variation in effective masses is supervised employing the last term

($1.5nkT_n\nabla \ln\, m_n$ and $1.5pkT_p\nabla \ln\, m_p$) [69].

5.1 Hot Electrons

When a group of electrons gain higher energy as compared to their other counterparts under the influence of high electric field, they become hot. However, the temperature is simply a measure to indicate their kinetic energy, as they are no more in thermal equilibrium with the crystal lattice. The energy that these electrons achieve is either due to high electric field or excitation by light. These hot electrons also exchange energy with the electron cloud and can affect their distribution. The impact of hot electron on the breakdown of insulator was first reported by von Hippel in 1937. He advanced the idea of the inability of the electrons to lose energy gained from the electric field during inelastic collision, hence, leading to breakdown by initiating avalanche breakdown. These hot electrons are also responsible for influencing and initiating breakdown in semiconductors [87]. The scattering mechanism largely affects the properties of hot electrons and makes the study of breakdown more complex. A better understanding of the behaviour of these carriers could only be possible in semiconductors, wherein the concentration is midways between a metal and an insulator. This low concentration of carriers could enable the application and sustenance of high electric field. Also in a non-degenerate semiconductor, the average energy of an electron is anywhere between 1-50 meV, so it is easier to bring a change in energy as compared to metal, where electrons have an average energy of around 1 eV [88].

Hot electrons are not only bane but they are boon also for transferred electron devices like Gunn-effect diode (in GaAs), impact ionization avalanche transit-time diode (IMPATT), trapped plasma avalanche triggered transit (TRAPATT), barrier injected transit-time (BARITT), etc. In Gunn effect, the electrons jump from lower Γ valley to higher L valley of the conduction band. These valleys in GaAs are separated by an energy difference of 0.36 eV. To surmount this energy difference, the electrons need to be hot. In devices like IMPATT, TRAPATT and BARITT, impact ionization plays an important role, and the electrons involved in impact ionization are hot. These hot electrons also have a negative effect and degrade the

material and device, leading to catastrophic failures.

5.2 Hot Electron Induced Degradation

A HEMT can undergo various stress condition during its operational life. The stress can be elaborated as, bias stress due to reverse bias of gate, OFF/ON state high field stress and ON state low field stress. The hot electron created due to electrical stress of reverse biased gate may distort typical bell-shaped transconductance (g_m) curve and introduce a double peak in it. The distortion gets prominent as the duration of stress is increased. This feature evolution in g_m is credited to the filling of donor traps at low field and subsequent emptying because of high electric field. This emptying attempts to restore the characteristic shape of g_m curve. The electric field at the gate edge is to be held accountable for most of the trapping in its vicinity [47]. There are various other kind of degradations that are promoted by these hot electrons and are discussed in this Chapter. Hot electron presence in AlGaN/GaN HEMT is determined using Electroluminescence (EL) measurements. Since GaN is a direct bandgap semiconductor, inter-band transition of very high energy electrons leads to the generation of EL in the channel [89,90]. It is observed that during ON state (V_{DS} = 20 V and V_{GS} = 0 V), EL signature captured from HEMT channel is same throughout indicating uniformity in energy of channel electrons, whereas, in the OFF state (V_{DS} = 20 V and V_{GS} = – 6 V), the EL becomes non-uniform and particular locations have higher EL as compared to others due to the injection of hot electrons from gate electrode. In the OFF state bias, the electrons acquire large energy as the gate drain bias is very high which facilitates enhanced photon emission. It is concluded by observing EL that V_{GS} plays a major role in enhancing/depleting and imparting energy to the electrons. To ascertain the degradation, DC tests are performed and it is found that the partial ON state (V_{DS} = 20 V and V_{GS} = – 5.5 V) proves to be fatal for the devices because of fall in (g_m). The devices under test also exhibits gate lag [14]. A simple conclusion is drawn that hot electrons lead to degradation by trapping when devices are stressed for a longer duration. A study is conducted on a vertical Au/Ni/AlGaN/GaN/n-GaN/AlN/Si Schottky diode to

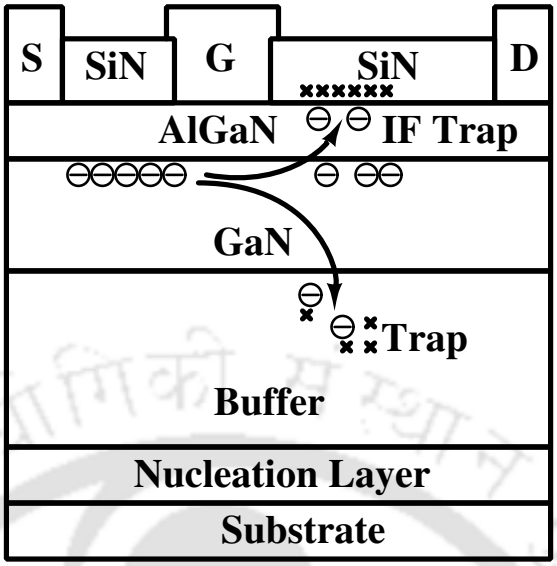

Figure 5.1: Trapping at various sites in AlGaN/GaN HEMT initiated by the hot electrons.

observe the reverse bias leakage mechanism. It is found that the high energy electrons are responsible for the creation of shallow donor traps at 0.12 eV below the conduction band [49]. Hot electron have also shown to promote hydrogen poisoning (trapped hydrogen in device package) resulting in threshold voltage shift, drain current reduction and increase of trap density [91]. These traps increase trap assisted tunnelling and degrades device's performance. When the drain is biased at a high voltage, the hot electrons spill into a buffer and upon being captured by the buffer traps under the channel, thus, creates a virtual gate which depletes 2DEG. It can also happen that hot electrons spill over the channel and get trapped by traps outside the channel [52]. Hence, the primary aim of designing a HEMT should be the reduction of electric field, which could prohibit electrons from picking up energy. The GaN buffer has a E2 trap. The capturing of electrons in this trap is bias dependent. In the OFF state, the trapping takes place due to gate leakage current, whereas in semi-ON state, the trapping occurs due to hot electrons injection from 2DEG into GaN buffer because of the electric field being high enough at the gate edge towards the drain [48] end. Figure 5.1 illustrates various trappings that can happen in an AlGaN/GaN HEMT.

5.3 Electron Temperature Related Reliability Issues

AlGaN/GaN HEMT suffers from a variety of degradation mechanisms. A few among them are initiated by electrons having a higher temperature, and these hot electrons are responsible for increasing the trap density underneath the gate [31] as well in the gate-drain access region. It has been reported that electron energy is responsible for introducing a slight negative differential conductance in the output (NDC), irrespective of the operational power in the device. This suggests that the electron temperature has a crucial role to play rather than the lattice temperature. The NDC occurs due to capturing hot electrons in the bulk traps [31, 32]. It has been shown earlier that the moment drain voltage reaches 5

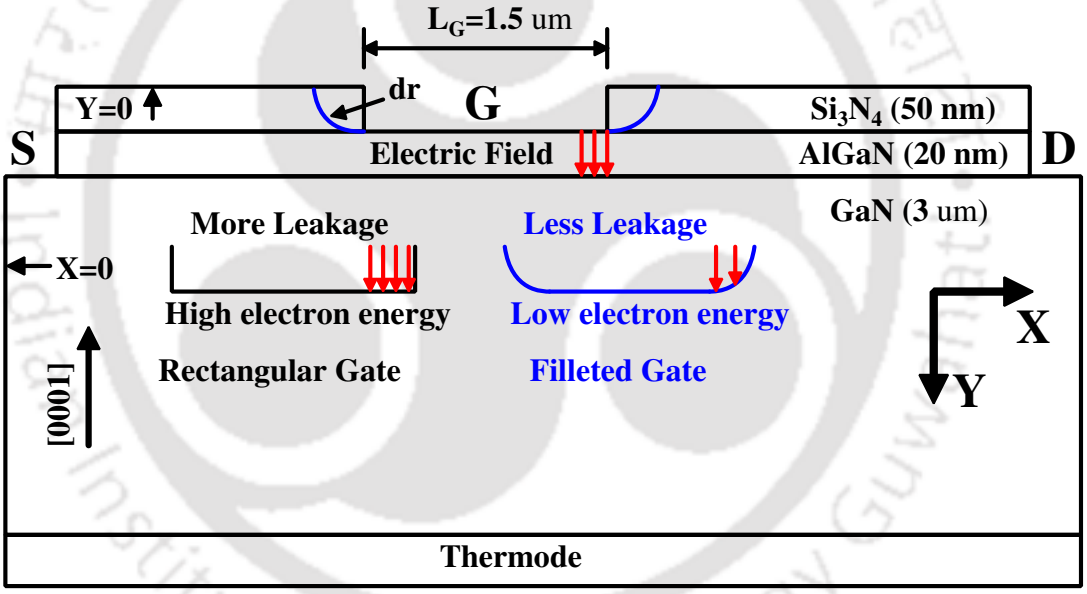

Figure 5.2: Simulated HEMT device structures showing rectangular and filleted gate geometries and the effect of these gates on electric filed and leakage current.

V, electrons are already in the high electron temperature (eTemperature) domain [92]. On the other hand, it is expected that at such a low drain voltage, there may not be significant Joule heating in the device causing this effect. Therefore, the aim of this thesis is to estimate eTemperature in the structures considered through hydrodynamic TCAD simulations. This approach helps in portraying correct eTemperature variations in the device [74,93]. Although hydrodynamic simulations are not suitable for long channel devices, however, it is a powerful

method to study and understand the role played by hot electrons in degrading the device performance. These hot electrons also play an important role in altering breakdown voltage of the device [32]. Thus, hydrodynamic simulation is an indispensable tool to study and understand the internal physics of a device. Thus, a similar approach is followed in the present work to observe the variations of eTemperature in the structure shown in Fig. 5.2 (without FP).

5.3.1 OFF State Electron Temperature Reduction

The HEMTs having various gate shapes are analyzed by driving them in DC ON/OFF state bias stress to study the effect of gate filleting on eTemperature map in the device. Subsequent effect on the gate leakage and drain currents due change in eTemperature are also studied. During ON state bias stress, V_{GS} is set to 0 V and V_{DS} is ramped to 20 V. It is observed that due to increase in the filleting radius, electric field magnitude reduces and field strength diffuses around the gate edge on the drain side. It is because of the diffusing effect of electric field that the cross-sectional area of the region where eTemperature is high gets reduced. This also causes eTemperature hot-spot region to shift towards GaN bulk as shown in Fig. 5.3 and Fig. 5.4, which correspond to ON and OFF state bias stress, respectively. There is also a minor shift in the eTemperature local peak towards bulk with an increase in filleting radius. It is believed that this region creates a channelling path through which electrons get injected into AlGaN [51]. Since this channelling region shifts towards bulk, the carrier leakage into AlGaN reduces. Due to the shift in local eTemperature peak towards bulk, the electron trapping in AlGaN region decreases, while the drain current remains constant for $dr7$ gate HEMT. This is apparent from I-V characteristic shown in Fig. 5.5 (a). Contrary to this, *RG* HEMT has a higher eTemperature over a larger area, thus creating a larger channelling region promoting siphoning of electrons towards AlGaN layer, which reduces drain current as shown in Fig. 5.5 (a). It can be observed, due to this, there is a drop in drain current for *RG* HEMT. This implies that there is leakage of carriers in AlGaN because of that the gate current also rises fast as shown in Fig. 5.5 (b). This

decrease in drain current is attributed to the creation of deep level traps in the device [51].

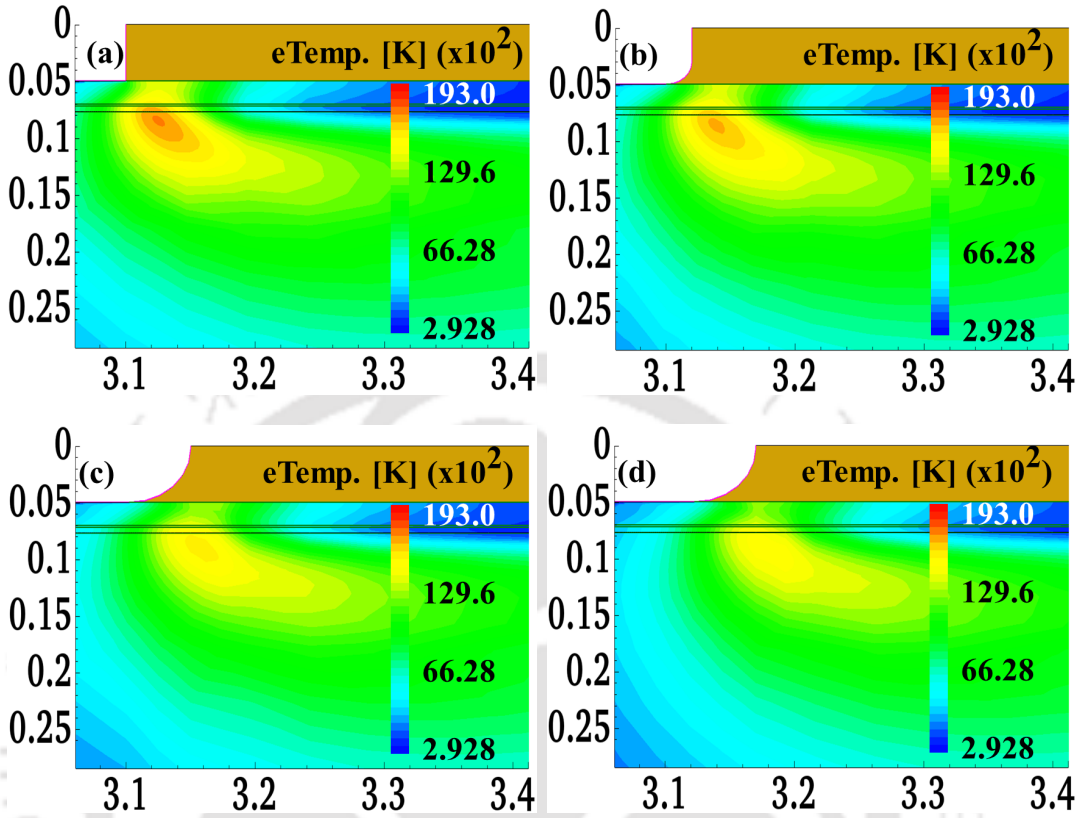

Figure 5.3: Variations in eTemperature for different gate structure at V_{GS} = 0 V and V_{DS} = 20 V (ON state). Figure (a) – (d) are arranged in terms of increasing fillet radius (dr0 to dr7). The cross sectional area as well as the leakage channel penetration in the AlGaN layer exhibits a diminishing trend with the increase in filleting radius resulting in reduced spillover effect, which leads to the lowering of gate leakage current.

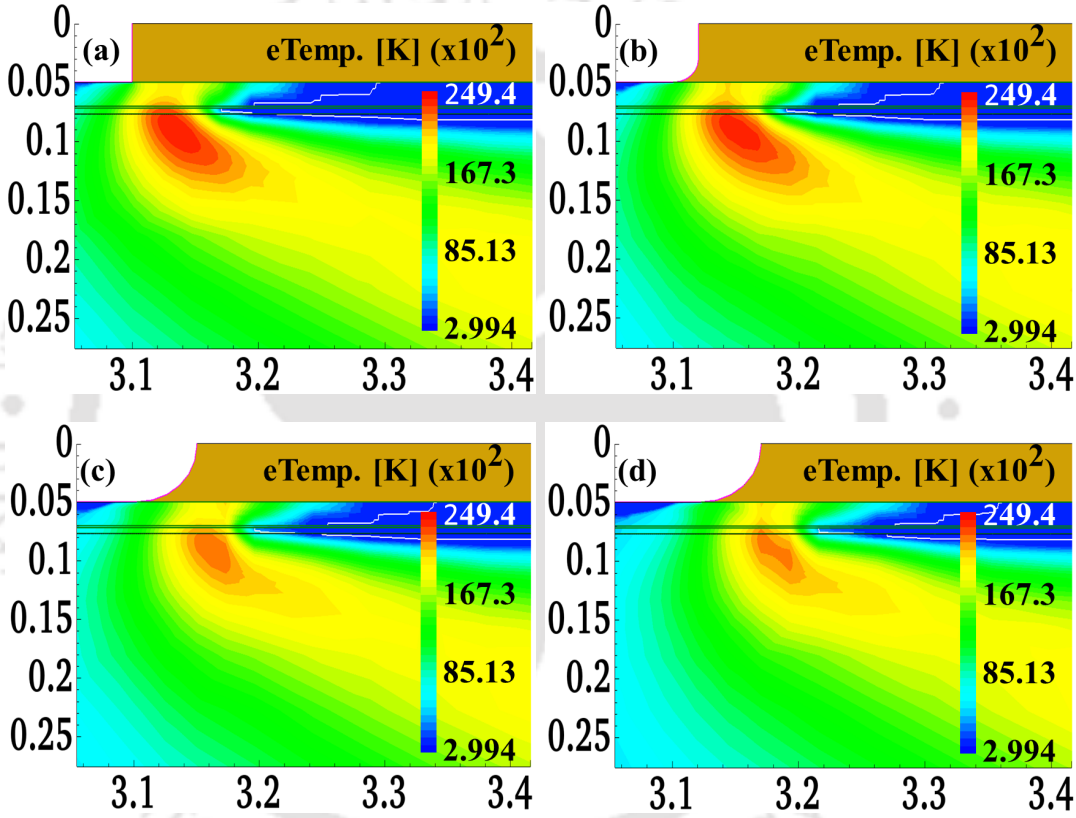

Figure 5.4: Higher cross sectional area as well as higher eTemperature values can be observed for devices biased in the OFF state (V_{GS} = – 6 V and V_{DS} = 20 V). There is a high electric field below the gate edge as compared to ON state. Figure (a) – (d) are arranged in terms of increasing fillet radius.

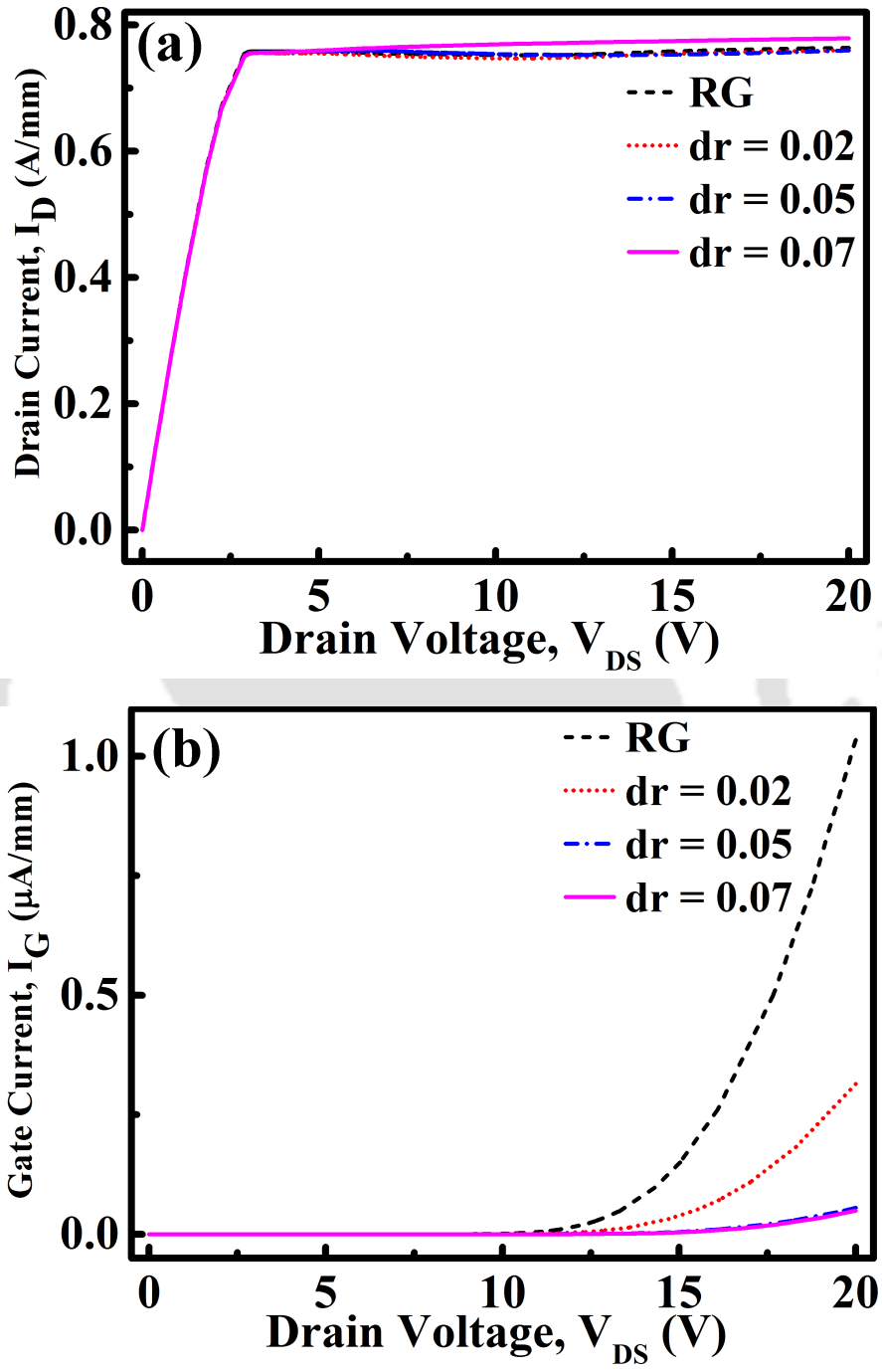

Figure 5.5: Electrical characteristic of various gate structures. Figure (a) shows the drain current characteristics for V_{GS} = 0 V and V_{DS} ramped till 20 V from which it can be inferred that the increase in filleting radius reduces spilling and channelling of electrons from 2DEG. Figure (b) illustrates gate leakage current of the HEMTs for the bias condition of V_{GS} = – 6 V and V_{DS} ramped till 20 V and it can be observed that for dr = 0.07 μm gate leakage current is low. The leakage current for $dr7$ is two orders of magnitude lower as compared to $dr0$ HEMT.

The gate leakage current is primarily due to tunnelling instead of thermionic emission because the observed leakage current is independent of temperature and there is no difference between leakage currents either at 100 K or at room temperature [85]. Incidentally, it has also been observed that the polarization field reduces the depletion region in AlGaN layer because of which gate leakage current increases. Thus, the gate tunnelling current can be decreased by increasing depletion region in AlGaN barrier layer [85]. The proposed structure in this thesis has a lower polarization. Hence, it does not reduce the depletion region width in the manner *RG* HEMT does. It can be observed from Table 5.1, that the space charge decreases in our

Table 5.1: Space charge in the AlGaN layer.

Parameter	***RG***	***dr2***	***dr5***	***dr7***
Space Charge (10^4 μm^{-1})	-1.1631	-1.1105	-1.0992	-1.0833

proposed structure, thus, implying a larger depletion width in the AlGaN layer and lowering the leakage current in filleted gate HEMT as compared to *RG* HEMT. Therefore, the filleted gate HEMT exhibits low gate leakage current (see Fig. 5.5 (b)). The leakage current for *dr*7 and *RG* HEMTs are 4.1 $\times 10^{-8}$A/mm and 1.03 $\times 10^{-6}$A/mm, respectively. Another mechanism that affects gate leakage is the Poole-Frenkel (PF) emission. It is dependent on the applied field and temperature of the device. The PF emission depends on the square root of applied field [94] and is lower in a structure which has a low electric field. Therefore, the proposed device has a lower gate leakage current due to various advantages explained above.

5.4 Summary

A hot electron is generally formed due to the presence of high electric field and the degradation mechanism caused by it is mostly very active in the semi ON state of the device. It has been found that filleting of the gate helps in controlling electric field by diffusing it at the gate edge. This approach has shown that its benefits are significant and the gate leakage reduces by two orders of magnitude. The electrons having high eTemperature also

decreases in the OFF state by adopting a filleted gate approach. As the density of hot electrons reduces, the number of trapping events as well as the leakage current decreases. This also lowers the rate of hot electron promoted degradation.

6

Limiting Self Heating in HEMTs

Contents

Self-heating arises in a semiconductor device due to Joule heating effect caused by the current flowing in it. In a MOS chip, the temperature rise is attributed to the high transistor density, whereas, in the power devices, it is primarily due to high current density. Owing to the high electron mobility, saturation currents in GaN-HEMTs can reach as high as 1.9 A/mm [95] and 2.3 A/mm [96]. At such high currents, there is a significant Joule heating effect in the transistor [97]. Power densities in an AlGaN/GaN HEMTs can be unusually high due to the simultaneous presence of high currents and high voltages. Thermal management is an important aspect, irrespective of the size of the transistor to enhance its life. The heat generated in a semiconductor can be classically expressed as,

$$Q_{gen} = J \cdot E \tag{6.1}$$

where, J and E are, respectively, the local current density and electric field. Gallium Nitride High Electron Mobility transistors have emerged as a promising alternative to Silicon based transistors in the past two decades, especially in the field of power [98] and RF electronics [99], because of its high saturation currents and high breakdown voltage [100]. As we know that with any new technology in its infancy, the HEMTs as well, suffers from critical problems such as current collapse [101, 102], self-heating [56, 57, 97, 103–105], failure due to CPE [17, 28, 46], etc. A device progresses into degradation, mainly because of temperature and the simultaneous presence of an electric field further accelerates the degradation mechanism. It is also reported that some of the degradation mechanism observed are unique to GaN [106]. Self-heating alters electric field near the gate edge on the drain side, and this accelerates electrons from the channel towards the surface states of the device [107]. Therefore, to understand and determine the reliability of a GaN-HEMT, channel temperature plays a crucial role [34]. These challenges are critical and need to be addressed so that GaN-HEMTs could revolutionize the power and RF electronics industry.

6.1 The Heating Effect

Joule heating occurs in a GaN-HEMT as a very high saturation current flows in its channel [97]. Although Gallium Nitride has a higher thermal stability as compared to Silicon [108], the heating causes mobility of the electrons in 2DEG to drop which results in the reduction of current [96, 109]. This hinders prolonged use of GaN-HEMTs. A detailed analysis of the heating effect reveals that the temperature rise is concentrated at the drain side of the gate edge where the formation of thermal hot-spot is found [3]. The self-heating contours portraying the temperature variations are illustrated in Fig. 6.1, where it can be observed that the temperature increases at the gate edge on the drain side and the maximum temperature, as high as 900 °C [74], can reach. The temperature rise in the device can be seen as a linear function of the drain source voltage, (V_{DS}) which decreases the current obtained from the negative slope of I-V curve.

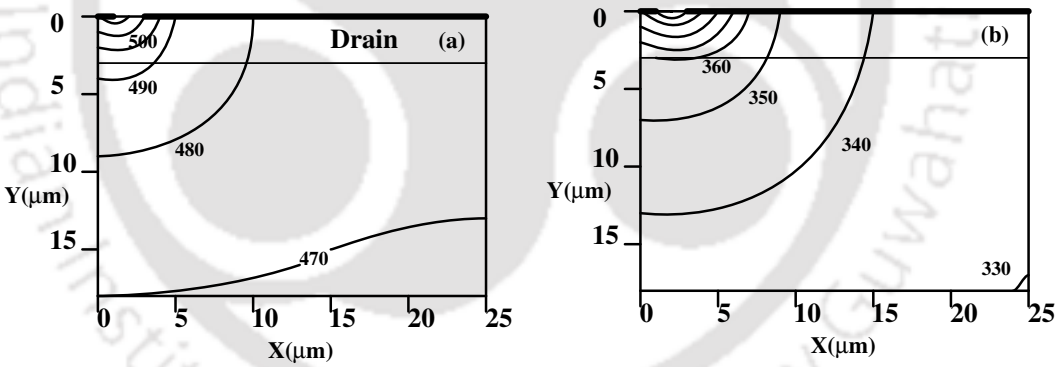

Figure 6.1: Contour diagram exhibiting distribution of temperature in Kelvin for GaN-HEMTs on Silicon Carbide for various substrate lengths: (a) for 50 μm and (b) for 3 mm. An isothermal boundary condition is maintained at the bottom of the substrate. The biasing conditions are V_{DS} = 50 V and V_G = 0 V [3].

6.1.1 Modelling Heat Flow and Carrier Transport

In any semiconductor TCAD simulator, a set of well-defined semiconductor equations are analyzed, which are Poisson, Current and Continuity equations. These equations are iteratively solved to obtain the desired device characteristics. The carrier transport in the

device is governed by current density equations [69] and is described by Eq. 6.2 and 6.3.

$$\nabla \cdot J_n = qR_{net,n} + q\frac{\partial n}{\partial t} \tag{6.2}$$

$$-\nabla \cdot J_p = qR_{net,p} + q\frac{\partial p}{\partial t} \tag{6.3}$$

where, J_n and J_p represent carrier current densities and, $R_{net,n}$ and $R_{net,p}$ represent carrier recombination rates. Depending on the model used, the method of computing J_n and J_p varies. In the standard drift-diffusion model, J_n and J_p are computed according to Eqs. 6.4 and 6.5.

$$J_n = \mu_n(n\nabla E_C - 1.5nkT\nabla \ln m_n) + D_n(\nabla n - n\nabla \ln \gamma_n) \tag{6.4}$$

$$J_p = \mu_p(p\nabla E_V + 1.5pkT\nabla \ln m_p) - D_p(\nabla p - p\nabla \ln \gamma_p) \tag{6.5}$$

The first term in the above equations include combined effect of contributions due to variation in the bandgap, electrostatic potential and electron affinity in the space. The rest of the terms describe contribution due to spatial variation of the effective masses (m_n, m_p) and the concentration gradient of carriers. The D_n and D_p are given by Einstein's relation for mobilities, where $D_n = kT\mu_n$, $D_p = kT\mu_p$, γ_n and γ_p for Fermi statistics are defined as,

$$\gamma_n = \frac{n}{N_C}\exp\left(\frac{E_C - E_{F,n}}{kT}\right) \tag{6.6}$$

$$\gamma_p = \frac{p}{N_V}\exp\left(\frac{E_{F,p} - E_V}{kT}\right) \tag{6.7}$$

where, k is the Boltzmann's constant; T is the temperature; E_C and E_V are conduction and valence band edge; N_C and N_V are the conduction and valence band effective density of states; $E_{F,n}$ and $E_{F,p}$ are quasi-Fermi energies for electrons and holes; n and p are the electron and hole concentrations, respectively. When Einstein's relation satisfies, the current equations (Eq. 6.4 and 6.5) can be reduced to Eqs. 6.8 and 6.9.

$$J_n = -nq\mu_n\nabla\Phi_n \tag{6.8}$$

$$J_p = -pq\mu_p\nabla\Phi_p \tag{6.9}$$

Here, Φ_n and Φ_p represent electron and hole quasi-fermi potentials, respectively. The drift-diffusion model is solved by assuming an isothermal condition, hence, it does not evaluate temperature distribution in the device.

6.1.2 Thermodynamic model

In the thermodynamic model of carrier transport [69], the current density equations are solved considering temperature gradient as expressed in Eqs. 6.10 and 6.11.

$$J_n = -nq\mu_n(\nabla\Phi_n + P_n\nabla T) \tag{6.10}$$

$$J_p = -pq\mu_p(\nabla\Phi_p + P_p\nabla T) \tag{6.11}$$

Here, P_n and P_p are absolute thermoelectric powers of the carriers and T represents lattice temperature. The temperature is estimated by using equations for lattice temperature which are expressed in Eq. 6.12.

$$\begin{aligned}\frac{\partial}{\partial t}(c_L T) - \nabla\cdot(k_t\nabla T) = &-\nabla\cdot[(P_nT+\Phi_n)J_n + (P_pT+\Phi_p)J_p] \\ &-\frac{1}{q}\left(E_C + \frac{3}{2}kT\right)(\nabla\cdot J_n - qR_{net,n}) \\ &-\frac{1}{q}\left(-E_V + \frac{3}{2}kT\right)(-\nabla\cdot J_p - qR_{net,p}) \\ &+\hbar\omega G^{opt}\end{aligned} \tag{6.12}$$

Here, k_t is the thermal conductivity; c_L is the lattice heat capacity; E_C and E_V are conduction and valence band energies, respectively, and G^{opt} is the optical generation rate due to photons. The RHS of Eq. 6.12 is equal to the total heat, H. If a stationary case is considered, the second and the third terms can be ignored, and Eq. 6.12 can be expressed as Eq. 6.13.

$$H = -\nabla\cdot[(P_nT+\Phi_n)J_n + (P_pT+\Phi_p)J_p] + \hbar\omega G^{opt} \tag{6.13}$$

The coupled solution of lattice temperature with current density equations manifests a more realistic lattice temperature distribution and a carrier transport model that incorporates device self-heating.

6.2 Self-Heating Related Degradation

The degradation mechanisms in AlGaN/GaN HEMTs are thermally initiated and accelerated [58]. At a high drain bias, due to high temperature and accumulation of heat, the electron wavefunction starts spreading into AlGaN barrier, which causes scattering [110]. Thermal stress arises in AlGaN and GaN layers as heat diffuses to other areas of HEMT from the hot-spot region [111]. The degradation mechanism is of diffusive nature as the generation and evolution of degradation follows a square law dependence with time [112]. It has been reported that devices which are subjected to a long duration high temperature operation test, exhibit degradation that is initiated by CPE and further accelerated by high temperature. The primary location of this degradation is at the gate edge on the drain side. This led to the reduction of drain current as well as transconductance because of the trapping in gate drain access region [113]. The degradation caused by trapping does not fade away on its own and detrapping does not happen even after months of inactivity, which implies that the degradation becomes permanent. However, in this case, the Schottky contacts exhibits an increase in barrier height [114]. As we know, the key test process for understanding degradation in an AlGaN/GaN HEMT is through DC stress test, which is conducted at high operational temperatures. The DC stress test at various temperature has a consistent drift behaviour (in device characteristics); that's why it facilitates easy determination of failure mechanism. It is reported by Singhal *et al.,* that those devices which operate at a higher temperature have a higher drift (reduction) in drain current for a fixed operational lifetime of 20 years and an exponential decrease in the mean time to failure. There is a degradation of an interfacial layer in the gate contact region resulting in an increase in Schottky barrier height, which leads to increase threshold voltage and decrease drain current [56]. It is worth noting that the self-heat has a major impact on the gate contact and leads to its permanent degradation. The Schottky gate in an AlGaN/GaN HEMT, is formed by using a metal stack of Ni/Au. At high temperatures, an interdiffusion of the metal stack has been reported [56, 57, 103–105]. It is observed that Gold tends to migrate to AlGaN surface

through gate edges having a stress voltage of V_{DS} = 50 V with wafer backside temperature held at 100 °C [57]. The outcome of this migration increases gate leakage current. An

Table 6.1: Properties of Nickel Silicides. The reaction consumption shows amounts of metal and Silicon employed to create a 100 nm thick layer of Silicide [7].

Silicide	Resistivity at 298 K (Ω-cm)	Reaction Consumption (nm)	
		Metal	Silicon
NiSi	15	49.8	91.0
$NiSi_2$	45	27.7	101.2

anomaly that needs to be pointed here is that, even though the work function of both Gold (5.1 eV) and Nickel (5.15 eV) are almost the same, there is still an increase in gate leakage current in the HEMT [57]. It has also been reported that the Ohmic contacts on the source and drain (Ti/Al/Ni/Au) are fairly stable, whereas, for the Schottky contact (Ni/Au) the barrier height increases due to the thermal storage at 400 °C for 48 hours [103]. In all the studies carried so far, Gold migration is held responsible for the degradation of gate's Schottky contacts. Another aspect of the degradation is the reaction between Silicon of SiN passivation and Nickel of the Schottky metal stack. The reaction of Silicon with metal forms a Silicide, and there are various phases of it. Some phases have been reported to have low contact resistance. Such reaction may increase the contact resistance, if a high resistivity phase is formed. It can be seen in Table 6.1 that Silicon reacts with Nickel to form Silicides having different resistivity, and there is a consumption of Silicon in the process. Table 6.1 represents data for reaction of Nickel with Silicon, but similar justification may be provided for SiN passivation layer as it contains Silicon. When a commercially available AlGaN/GaN HEMT on Si is subjected to 700 hours RF test at a channel temperature of 300 °C and V_{DS} = 45 V, Gold migration is observed leading to 6% drop in average drain current, decrease of 10% in the output power and an increment of 150% in the gate current [105]. To stop the reaction between Silicon of Nitride passivation and Nickel of gate stack, a Nickel Oxide (NiO) barrier layer is used on the sidewalls of Nitride layers [115].

6.3 Solutions to the Heating Problem

A number of effective solutions to tackle self-heating problem have been proposed in literature. Heat sink layers made up of good thermal conductors, such as nanocrystalline Diamond have been used effectively in the device to remove the heat [116]. An exterior heat sink over the entire chip is used in [117] to mitigate the channel temperature. A quilt like Garphene layer is deposited over an entire transistor [118] to control device temperature. Proper substrate selection for heat removal is the most reliable and long practiced approach. Substrate selection for GaN-HEMT is primarily based on the requirement to handle power and breakdown voltage. For low end low cost systems, Silicon can be an attractive choice, but devices using it as substrate suffer from early breakdown. For higher power dissipation, the substrate has to have higher thermal conductivity to enhance heat extraction, hence, incorporating higher thermal conductivity substrate becomes an indispensable requirement. The growth of the composite device heterostructure is a challenging task and the stack needs to be grown keeping in mind the lattice mismatch. Lattice mismatch creates additional strain at substrate-GaN interface even after using a stress relieving layer. Table 6.2 lists lattice mismatch, thermal conductivity and coefficient of linear thermal expansion of popular materials employed in the thermal management of GaN-HEMT. For device applications, nanocrystalline (NC) Diamond is used as heat spreaders. These NC Diamond are highly disordered and very defective along with having a large lattice mismatch with GaN. Diamond integration has been found to be challenging as large defect density is formed during the integration process, and in some cases amorphous regions have been found to exist at GaN/Diamond interface [8].

As a whole, even though Diamond offers a high thermal conductivity which is an essential requirement for high performance HEMTs, its fabrication is not straight forward. For the integration with Diamond, an additional adhesion layer is required, but this adhesion layer is highly disordered and introduces an additional thermal resistance. Two approaches to reduce self-heating are presented in this thesis: (i) gate filleting and (ii) elevated Silicon

Table 6.2: Lattice mismatch and thermal conductivity of popular substrates and materials [4–6, 8–11]

Substrate/ Material	Lattice Mismatch with GaN (%)	Thermal Conductivity ($Wm^{-1}K^{-1}$)	Coeff. of Linear Thermal Exp^n ($10^{-6}K^{-1}$)
Sapphire	13	50	7.5
Silicon	17	150	3.59
Silicon Carbide	3.4	490	4.2
Diamond	11	2000	0.8
Copper	-	391	16.76
Aluminium Nitride	1	200	4.2
Gallium Nitride	-	210	5.6

Carbide substrate pillar.

6.4 Gate Filleting for Self-Heating Reduction

The work done in this thesis employs a filleted gate to cut the intensity of electric field, thus, reducing self-heating at the gate edge. Heat concentrates towards the gate edge on the drain side due to the presence of a high electric field. It can be either lowered by reducing the conduction current or by tailoring the electric field so that the local heat generated around strategically important areas subside. Due to gate filleting, the electrons diffuse because of the electric field diffusion. This reduces peak electric field at the gate edge, and it is found that the peak electric field shifts from the gate edge towards the GaN bulk. A reduction of temperature at the gate edge as well as a decrease in the high temperature region are observed due to filleting. For the devices studied in this thesis, the self-heating contours exhibiting temperature variations are depicted in Fig. 6.2. The reduced temperature at gate/AlGaN interface enhances life of the Schottky gate. Table 6.3 exhibits decrease in temperature because of simple filleting.

The temperature has an impact on device longevity and, lowering of temperature increases

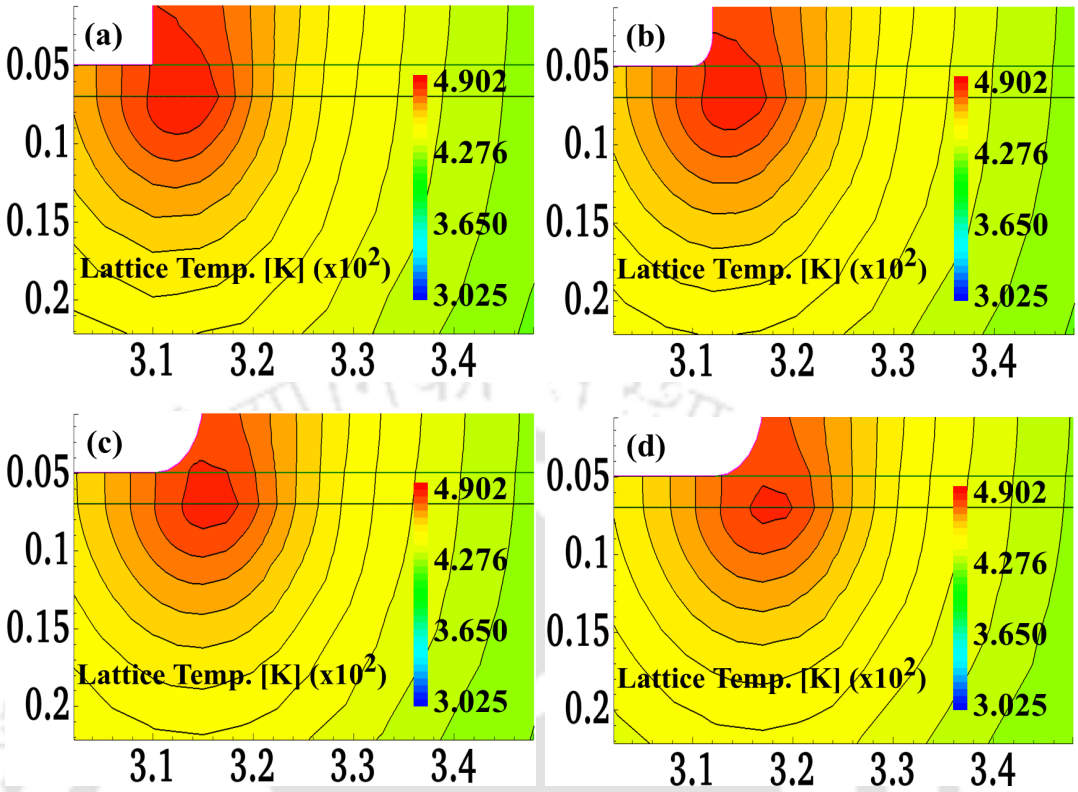

Figure 6.2: Figure illustrates variation of lattice temperature for various gate shapes. Due to diffusing effect of the filleted gate, cross sectional area of peak lattice temperature is reduced as well as is shifted from gate edge towards bulk. This further enhances thermal stability of the gate. Figure (a), (b), (c) and (d) corresponds to filleting radius of 0, 0.02, 0.05 and 0.07 μm, respectively. The measurement conditions are V_{GS} = 0 V and V_{DS} = 20 V (ON State of the device operation.)

Table 6.3: Peak lattice temperature obtained along the channel of different HEMT gate geometries.

Parameter	***RG***	***dr2***	***dr5***	***dr7***
Lattice Temp. (K)	487.15	486.41	485.18	483.1

its life exponentially [119]. Hence, even a slight reduction in operating temperature can enhance the life significantly. The proposed HEMT is expected to have a longer life as it operates at a ΔT of 4 K lower than *RG* HEMT, even though the same power is fed to all the devices. A plot of temperature variation along the channel is depicted in Fig 6.3 (a). The temperature rise in the device can be observed as a linear function of drain-source voltage and decrease in the drain current can be estimated using negative slope of I-V curve

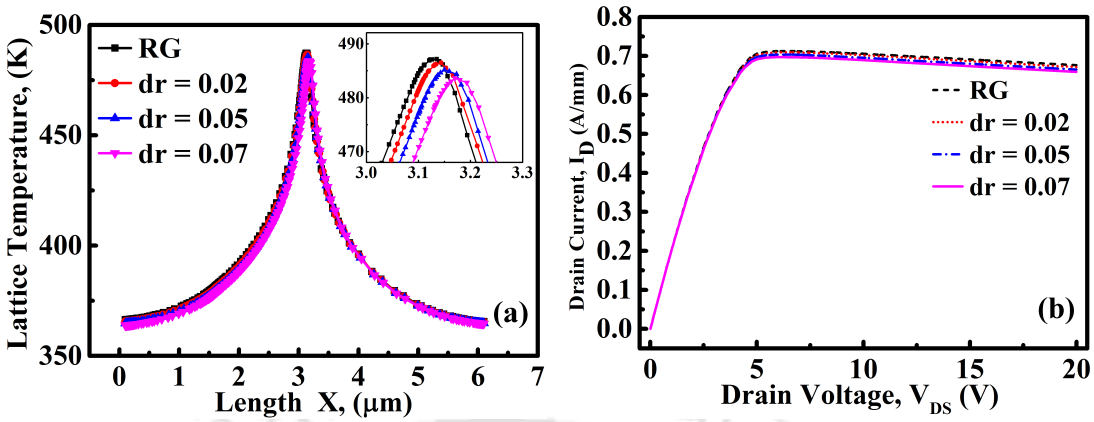

Figure 6.3: Plot of Figure (a) exhibits lattice temperature obtained from thermal simulation of various gate structures in the ON state obtained by Y-cut at a location of 2 nm below SiN/AlGaN interface in AlGaN and Figure (b) illustrates the ON state drain current reduction due to self-heating.

as shown in Fig. 6.3 (b). It is to mention that the electric field, device temperature and converse piezoelectric field, which are the degradation promoting parameters, are no longer high at the gate edge of the proposed filleted gate device.

6.5 Heat Extraction Through Elevated Substrate Pillar

Besides self-heating, current collapse is another critical phenomena plaguing AlGaN/GaN HEMTs. This happens mainly due to the formation of a virtual gate at the top of Nitride passivation layer [92, 120–124]. A thermally conductive layer above passivation layer may alter device electrostatics and promote current collapse by trapping charge at the interface of newly deposited material. Hence, the top surface of a HEMT is critical to obtain the desired device performance. Considering this, the work done in this thesis aims to extract heat from the bottom of the device, thus refraining from altering the electrostatics of the top layer. A preferable heat extraction path might be from the bottom of the device as Schottky gate of HEMT faces reliability issue due to excessive heating at the gate edge [56, 57, 103–105]. Therefore, this thesis explores the possibility of employing an extended substrate pillar to extract heat from the bottom side of the device. In the past, numerical modeling using Copper plug [62] and a device with a Copper plug [63] have been reported.

Metals have a high linear thermal expansion coefficient and, the volumetric expansion coefficient is approximately three times than that of linear expansion coefficient (refer Table 6.2). Additional stress may develop at higher temperatures in those devices which employs Copper plug for heat extraction and it may have a detrimental effect on the devices in a long run. Silicon Carbide has higher thermal conductivity as well as lower coefficient of thermal expansion as compared to Copper. Another advantage of SiC is that it has anisotropy in thermal conductivity (side walls have higher thermal conductivity as compared to top surface). The defect density in SiC is lower in the perpendicular plane (sidewalls) as compared to inplane [125]. The idea behind the proposed work is to use an elevated pillar like structure to tap hot phonons which are in large numbers in the active hot-spot region after their mean free path to avoid reflection at GaN/SiC interface. These phonons have a range of mean free path (MFP) as they do not obey gray approximation. It is also reported that the majority of heat is contained in the phonons having longer MFP [8, 126], whereas,

conventional flat SiC substrate does not utilize anisotropy in the heat flow.

6.5.1 Proposed Device Structure

A HEMT with an elevated SiC substrate pillar is shown in Fig. 6.4. Dimensions of the device structure, the associated materials and their thickness are illustrated in this figure as well. The substrate pillar length, L was fixed at 2 μm and the height, H was taken as 1.5 and 2 μm. A standard HEMT structure having the same dimensions, but with a planar substrate is employed for the comparison. Thermal simulations are performed on both the structures to observe the difference in channel temperatures.

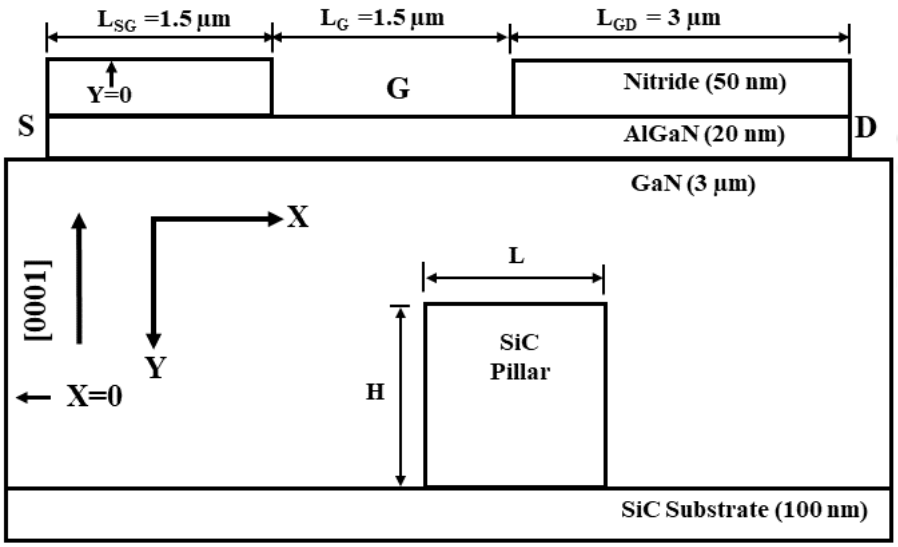

Figure 6.4: Schematic of an AlGaN/GaN HEMT structure, showing the elevated Silicon Carbide substrate pillar. The pillar is located midway below the gate edge towards the drain side.

6.5.2 Observations

Devices having an elevated substrate pillar has a lower channel temperature as compared to standard structure with planar substrate having same bias conditions. The simulation is performed by keeping gate voltage, (V_{GS}) constant at 0 V and the drain voltage (V_{DS}) is ramped from 0 V to 20 V. The self-heating map for the temperature variation is illustrated in Fig. 6.5. A cutline is taken in the middle of AlGaN layer (10 nm below AlGaN/gate interface) to observe the lattice temperature and it is found that there is a reduction in the temperature in HEMTs by using an elevated substrate pillar as presented in Table 6.4. It is originated that an increase in substrate pillar height increases lattice heat flux as shown in Fig. 6.6. The temperature rise in the device causes drain current to drop due to decrease in mobility because of self-heating which is illustrated in Fig. 6.7 (a). The same figure also exhibits that the device having lowest channel temperature has a marginally higher drain current. It can be observed that for a device having pillar dimensions of $L = 2\ \mu m$ and $H = 2\ \mu m$, the operational temperature is lowered by 19 K as compared to the planar substrate HEMT. Figure 6.7 (b) presents lattice heat flux obtained by taking an X-cut which passes through the substrate pillar. The device temperature is shown in 6.7 (c) and it is obtained by observing a Y-cut at 10 nm below AlGaN/gate interface. It can also be stated that the channel temperature reduces with an increase in the pillar height from 1.5 to 2 μm. To observe the temperature along the pillar, a X-cut is taken at the gate edge.

Table 6.4: A comparison of lattice temperature and heat flux for planar and elevated pillar substrates.

Substrate	**Lattice Temp. (K)**	**Lattice Heat Flux $\times 10^6 (W/cm^{-2})$**
Planar substrate HEMT	442	3.35
Elevated (L=2 μm, H=1.5 μm)	430	3.51
Elevated (L=2 μm, H=2 μm)	423	3.55

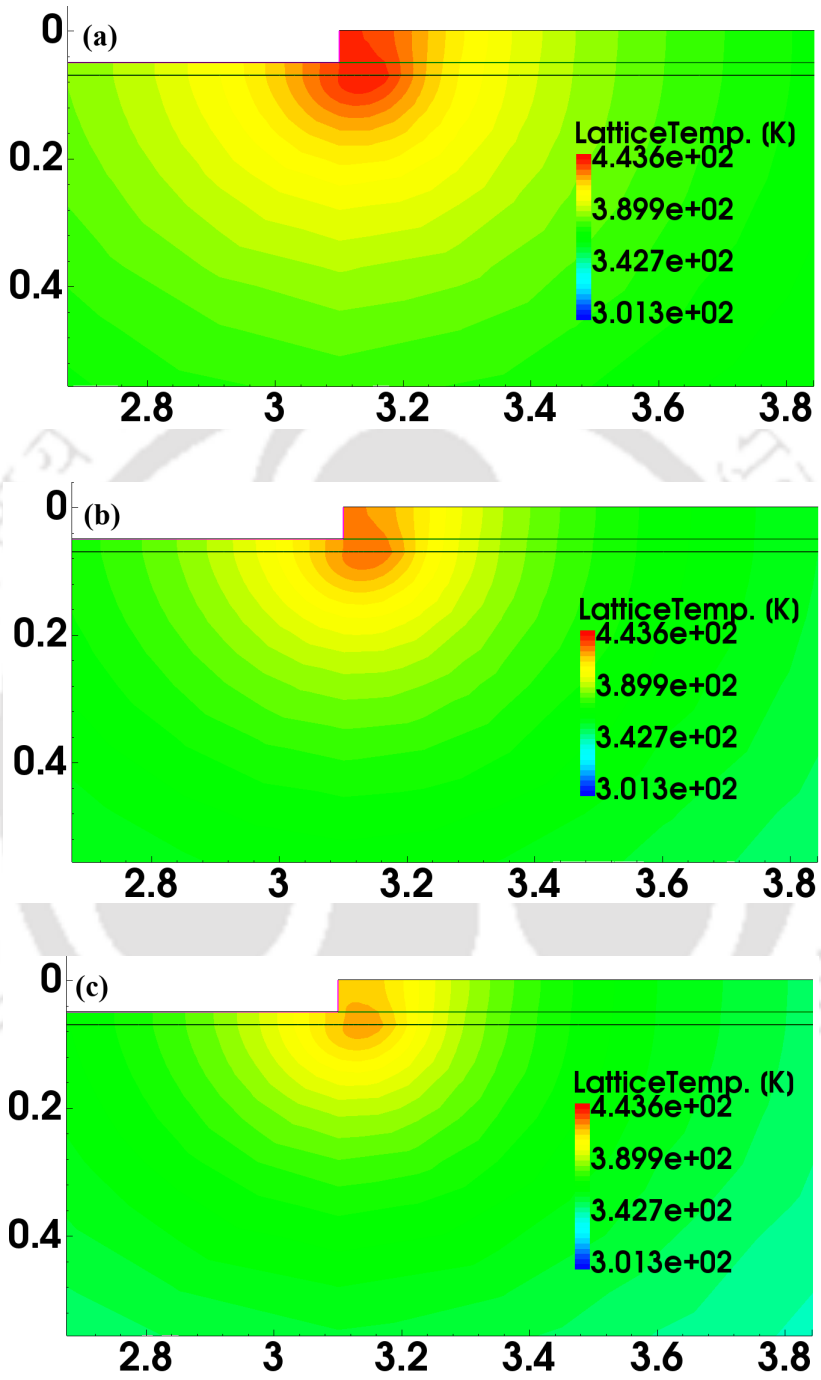

Figure 6.5: Variation of thermal map of the HEMT with an introduction of SiC substrate pillar. The plot of Figure (a) is a regular HEMT without substrate pillar. Figure (b) has a substrate pillar of W=2 μm, H=1.5 μm, whereas, Figure (c) has a pillar dimension of W=2 μm, H=2 μm. The bias conditions are V_{DS} = 20 V and V_{GS} = 0 V.

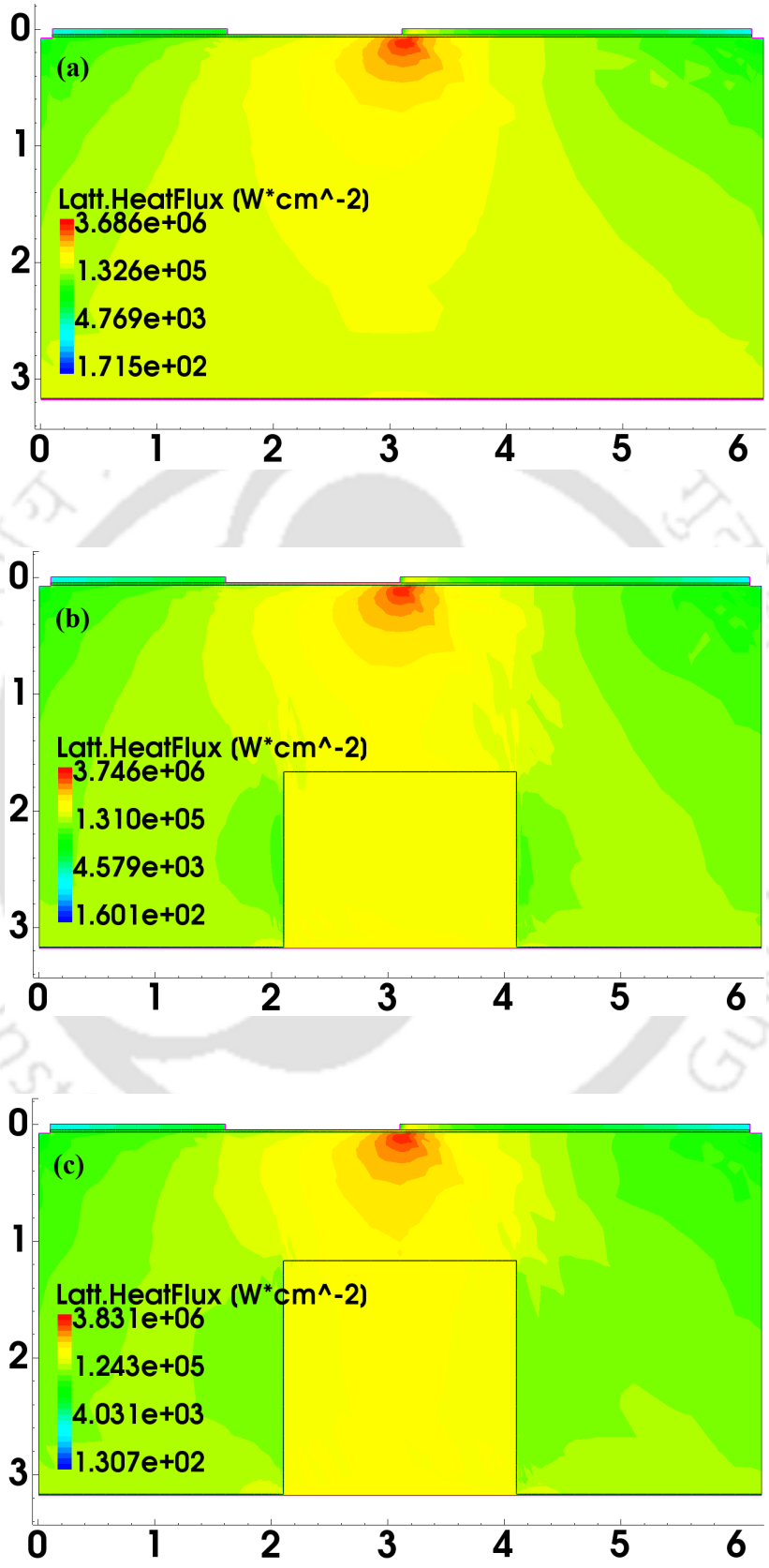

Figure 6.6: Lattice heat flux in various HEMT structures. In Figure (a), the substrate pillar is not employed, whereas, in Figure (b) and (c), introduction of substrate pillar enhances lattice heat flux resulting in reduction of lattice temperature at the gate edge. The bias conditions are V_{DS} = 20 V and V_{GS} = 0 V.

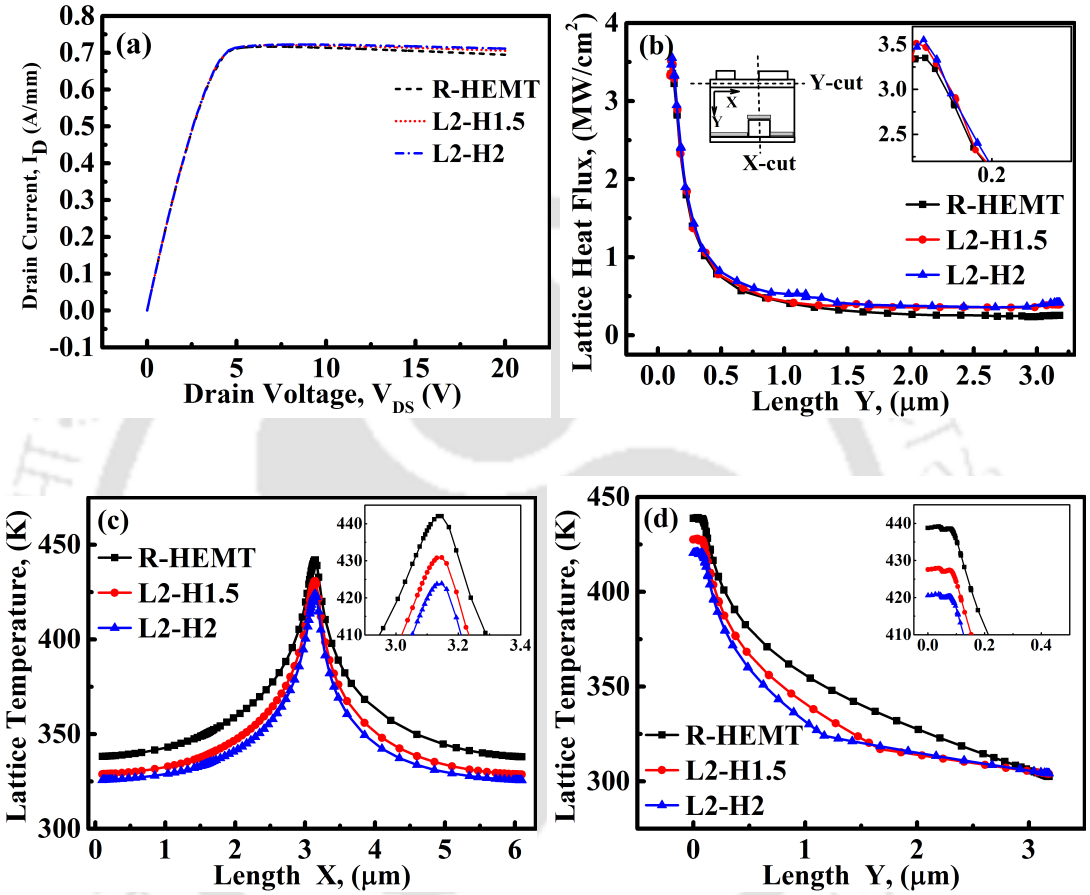

Figure 6.7: Electrical and various physical characteristics for the proposed (substrate pillar) and standard device structures showing, (a) Current Voltage characteristics, (b) X-cut (at the right gate edge) exhibiting lattice heat flux, (c) Y-cut (at middle of AlGaN layer) presenting lattice temperature due to self-heating along the channel and (d) X-cut at right gate edge depicting variations in lattice temperature from top to bottom of the device. The bias conditions are V_{DS} = 20 V and V_{GS} = 0 V.

It is found that increase in the pillar height decreases junction temperature as illustrated in Fig. 6.7 (d). Fall in device temperature has several benefits which have been described earlier.

There seems no direct way of getting such a pillar below the gate. Even etching SiC is a challenging task, and getting pillars of height 1.5 or 2 μm m is difficult. The growth of composite GaN layer above an etched SiC with pillars is also a tough task as non-planarities and other associated issues will creep in as the pillar height is significant. Sung *et al.* have demonstrated vertical etch into SiC wafer (of size 35 μm width and 98.2 μm) and beveled etch (of 70 degrees) in SiC using a mixture of gas plasma with an etch rate of 3050 Å/min using the gas ratio of $SF_6/(SF_6 + O_2) = 82$ % [127]. Even if such a pillar is created, deposition of GaN-HEMT composite layer would create non-planarities.

Device concept using Copper plugs for heat extraction have been demonstrated in the past [63]. Since, Copper has higher thermal expansion, at high temperature, its expansion may create strain in the vicinity of the Copper plug. Silicon Carbide has higher thermal conductivity as well as low thermal expansion as compared to Copper, hence, this work was targeted. Melting point of GaN is 2773 K [128], whereas that of SiC is 3103 K [129], even depositing SiC in the plug is impossible as GaN would melt by then. At this point there is no clear technology that can help in fabricating such a structure.

6.6 Summary

The high electric field at HEMT gate edge is known to introduce a significant self-heating in AlGaN barrier layer. During high power operation, there is a localized increase in the crystal temperature due to the dissipated Joule electric power. Self-heating creates a hot-spot which leads to the degradation of device performance. Many practical solutions, for example, an introduction of new materials to extract heat from hot-spots or innovative cooling techniques have been suggested. It has been shown in this thesis that the gate shaping and an elevated substrate pillar could reduce the temperature in GaN-HEMTs. Gate shaping

diffuses electric field, hence, the peak electric field at the gate edge decreases. The filleting reduces electron crowding at the gate edge, which aids in trimming self-heating. The peak temperature decreases with an increase in filleting radius and the proposed device operates at a temperature 4 K lower than the peak temperature of *RG* HEMT. Also, with the introduction of elevated substrate pillar, channel temperature falls. The height of the pillar plays a significant role in extracting heat from the channel by providing a high thermal conductivity path through Silicon Carbide substrate, and in this case, the temperature reduces by 19 K as compared to conventional Planar substrate HEMT. This reduction in temperature is healthy for Schottky contacts which has issues regarding its stability due to self-heating. This fall in temperature also discourages other degradation mechanism that work in tandem with self-heating related degradation. It is expected that, if all the issues associated with GaN-HEMTs are resolved, it is poised to dominate the power electronics sector.

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7

Summary and Conclusions

Contents

7.1 Summary of the Observations

We present a brief summary of the proposed research work and its future direction. As we know, the space is the next frontier and role of high power devices in this domain cannot be ignored any further. The summary presented below is an endeavour in that direction so that efficient high power devices could be developed and suitable materials could be explored to improvise efficiency of the power devices.

- One of the critical reliability issues in AlGaN/GaN HEMTs is the generation of CPE strain in AlGaN barrier layer, which is initiated by the strong electric field under the gate. The electric field is tailored by employing gate shaping, which is the key to reduce peak local electric field by diffusing it. However, when field plate is also added to *FG* HEMT, the electric field decreases further. Locally, electric field at the gate edge on the drain side for *FGdr*7 is about 44% lower as compared to *RG* HEMT and CPE reduces in the same proportion. The electric field in *FGdr*7 and *FGFPdr*7 is lowered by 30% and 38%, respectively as compared to *RGFP*. Incorporating FP in a *RG* HEMT reduces local peak electric field at the gate edge, however, the field is still higher as compared to *FGdr*7. The electric field for the FP HEMTs varies slowly over the FP length and peaks at the end of FP (secondary peak). However, for *FGdr*7 HEMT without FP, the peak local electric field at the gate edge is lower and the secondary peak is absent as well.

- The hot electrons contribute to the degradation of HEMTs and affect gate leakage current as well. Since the electric field could be moderated using gate filleting, the electron temperature is also controlled within the acceptable operating limits. The cross section area of high electron temperature region also decreases and this very region is also pushed towards GaN bulk. It causes reduction in siphoning of electrons to the gate, and lowering of the gate leakage current by two orders of magnitude in the proposed device structure than the conventional HEMT.

- The high electric field at HEMT gate edge is known to introduce a significant self-heating in AlGaN barrier layer. The application of gate shaping and an elevated substrate pillar is an attempt presented in this thesis, meant to mitigate self-heating issues in GaN-HEMTs. Filleting helps in the reduction of self-heating. We have achieved a lower temperature of 4 K in the filleted gate HEMT, which not only improves gate/AlGaN Schottky interface but also increases device lifetime. A SiC substrate pillar further improves heat extraction from an active junction region by enabling a high thermal conductivity path. In addition to that, low linear thermal expansion coefficient of SiC provides an advantage by generating no additional strain in GaN buffer with an increase in the operational temperature.It is found that the HEMT with substrate pillar functions at 19 K lower temperature than the standard HEMT with a planar substrate which increases drain current as well.

Therefore, it may be concluded that a GaN-HEMT with filleted gate and an elevated structure makes it a suitable candidate for high power industry. It is to mention that the further research in this area for increasing operations at high frequency would enable scientific community to improve efficiency of many essential high power applications manifolds.

7.2 Proposed Future Work

Having explored the filleted gate single finger device, it is anticipated that investigating effects of filleted gate on the performance of the multi-finger devices would be a promising direction of research and technology development. Use of alternate dielectric material to tailor the electric field can also be investigated. A similar approach of shaping source and drain contacts can also be explored.

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Bibliography

[1] O. Ambacher, B. Foutz, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, A. J. Sierakowski, W. J. Schaff, L. F. Eastman, R. Dimitrov, A. Mitchell, and M. Stutzmann, "Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped AlGaN/GaN heterostructures," *Journal of Applied Physics*, vol. 87, no. 1, pp. 334–344, 2000.

[2] J. F. Nye *et al.*, *Physical properties of crystals: their representation by tensors and matrices*. Oxford university press, 1985.

[3] V. O. Turin and A. A. Balandin, "Electrothermal simulation of the self-heating effects in GaN–based field–effect transistors," *Journal of Applied Physics*, vol. 100, no. 5, p. 054501, 2006.

[4] C. S. Suh, *Lateral GaN HEMT Structures*. Springer International Publishing, 2018, pp. 29–49. [Online]. Available: https://doi.org/10.1007/978-3-319-77994-2_2

[5] R. Quay, *Gallium Nitride Electronics*. Springer Science & Business Media, 2008, vol. 96.

[6] D. Ueda, *Properties and Advantages of Gallium Nitride*. Springer International Publishing, 2017, pp. 1–26.

[7] R. Tung, "Silicides for S/D Contacts," in *Encyclopedia of Materials: Science and Technology*, K.H. Jrgen Buschow and Robert W. Cahn and Merton C. Flemings and Bernhard Ilschner and Edward J. Kramer and Subhash Mahajan and Patrick Veyssire, Ed. Oxford: Elsevier, 2001, pp. 8479 – 8486.

[8] J. Cho, Z. Li, M. Asheghi, and K. E. Goodson, "Near-junction thermal management: Thermal conduction in gallium nitride composite substrates," *Annual Review of Heat Transfer*, vol. 18, 2015.

[9] K. Wang and R. R. Reeber, "Thermal Expansion of Copper," *High Temperature and Materials Science*, vol. 35, no. 2, 4 1996.

[10] Y.-C. Lei, W.-X. Yu, C.-H. Li, and X.-n. CHEnG, "Simulation on temperature field of tig welding of copper without preheating," *Transactions of Nonferrous Metals Society of China*, vol. 16, no. 4, pp. 838–842, 2006.

[11] P. Sohi, D. Martin, and N. Grandjean, "Critical thickness of GaN on AlN: impact of growth temperature and dislocation density," *Semiconductor Science and Technology*, vol. 32, no. 7, p. 075010, 2017.

[12] T. Mimura, S. Hiyamizu, T. Fujii, and K. Nanbu, "A New Field-Effect Transistor with Selectively Doped GaAs/n – $Al_xGa_{1-x}As$ Heterojunctions," *Japanese Journal of Applied Physics*, vol. 19, no. 5, pp. L225–L227, May 1980.

[13] D. W. Runton, B. Trabert, J. B. Shealy, and R. Vetury, "History of GaN: High-Power RF Gallium Nitride (GaN) from Infancy to Manufacturable Process and Beyond," *IEEE Microwave Magazine*, vol. 14, no. 3, pp. 82–93, 2013.

[14] G. Meneghesso, G. Verzellesi, F. Danesin, F. Rampazzo, F. Zanon, A. Tazzoli, M. Meneghini, and E. Zanoni, "Reliability of GaN High-Electron-Mobility Transistors: State of the Art and Perspectives," *IEEE Transactions on Device and Materials Reliability*, vol. 8, no. 2, pp. 332–343, June 2008.

[15] Y. F. Wu, A. Saxler, M. Moore, R. P. Smith, S. Sheppard, P. M. Chavarkar, T. Wisleder, U. K. Mishra, and P. Parikh, "30-W/mm GaN HEMTs by field plate optimization," *IEEE Electron Device Letters*, vol. 25, no. 3, pp. 117–119, March 2004.

[16] Y. f. Wu, M. Moore, A. Saxler, T. Wisleder, and P. Parikh, "40-W/mm Double Field-plated GaN HEMTs," in *2006 64th Device Research Conference*, June 2006, pp. 151–152.

[17] J. A. del Alamo and J. Joh, "GaN HEMT reliability," *Microelectronics reliability*, vol. 49, no. 9-11, pp. 1200–1206, 2009.

[18] R. J. Trew, D. S. Green, and J. B. Shealy, "AlGaN/GaN HFET reliability," *IEEE Microwave Magazine*, vol. 10, no. 4, pp. 116–127, June 2009.

[19] T. Ohki, T. Kikkawa, Y. Inoue, M. Kanamura, N. Okamoto, K. Makiyama, K. Imanishi, H. Shigematsu, K. Joshin, and N. Hara, "Reliability of GaN HEMTs: current status and future technology," in *2009 IEEE International Reliability Physics Symposium*, April 2009, pp. 61–70.

[20] G. Meneghesso, M. Meneghini, I. Rossetto, D. Bisi, S. Stoffels, M. V. Hove, S. Decoutere, and E. Zanoni, "Reliability and parasitic issues in GaN-based power HEMTs: A review," *Semiconductor Science and Technology*, vol. 31, no. 9, p. 093004, 2016.

[21] M. Meneghini, I. Rossetto, C. D. Santi, F. Rampazzo, A. Tajalli, A. Barbato, M. Ruzzarin, M. Borga, E. Canato, E. Zanoni, and G. Meneghesso, "Reliability and failure analysis in power GaN-HEMTs: An overview," in *2017 IEEE International Reliability Physics Symposium (IRPS)*, April 2017, pp. 3B–2.1–3B–2.8.

[22] P. B. Klein, S. C. Binari, K. Ikossi, A. E. Wickenden, D. D. Koleske, and R. L. Henry, "Effect of deep traps on sheet charge in AlGaN/GaN high electron mobility transistors," *Electronics Letters*, vol. 37, no. 25, pp. 1550–1551, Dec 2001.

[23] M. J. Uren, S. Karboyan, I. Chatterjee, A. Pooth, P. Moens, A. Banerjee, and M. Kuball, "Leaky Dielectric Model for the Suppression of Dynamic R_{ON} in Carbon-Doped AlGaN/GaN HEMTs," *IEEE Transactions on Electron Devices*, vol. 64, no. 7, pp. 2826–2834, July 2017.

[24] E. Zanoni, M. Meneghini, G. Meneghesso, D. Bisi, I. Rossetto, and A. Stocco, "Reliability and failure physics of GaN HEMT, MIS-HEMT and p-gate HEMTs for power switching applications: Parasitic effects and degradation due to deep level effects and time-dependent breakdown phenomena," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Nov 2015, pp. 75–80.

[25] A. Delias, A. Martin, P. Bouysse, J. M. Nebus, and R. Quere, "Low consumption and high frequency GaN–based gate driver circuit with integrated PWM," *Electronics Letters*, vol. 51, no. 18, pp. 1415–1416, 2015.

[26] N. Z. Yahaya, M. Begam *et al.*, "A review on design considerations & limitations of resonant gate drive circuit in VHF operations," *IAENG Engineering Letters*, vol. 17, no. 2, pp. 54–62, 2009.

[27] J. Joh, F. Gao, T. Palacios, and J. A. Del Alamo, "A model for the critical voltage for electrical degradation of GaN high electron mobility transistors," *Microelectronics reliability*, vol. 50, no. 6, pp. 767–773, 2010.

[28] J. Joh and J. A. del Alamo, "Critical Voltage for Electrical Degradation of GaN High-Electron Mobility Transistors," *IEEE Electron Device Letters*, vol. 29, no. 4, pp. 287–289, April 2008.

[29] V. Moroz, H. Y. Wong, M. Choi, N. Braga, R. Mickevicius, Y. Zhang, and T. Palacios, "The impact of defects on GaN device behavior: Modeling dislocations, traps, and pits," *ECS Journal of Solid State Science and Technology*, vol. 5, no. 4, pp. P3142–P3148, 2016.

[30] Jungwoo Joh and Feng Gao and Toms Palacios and Jess A. del Alamo, "A model for the critical voltage for electrical degradation of GaN high electron mobility transistors," *Microelectronics Reliability*, vol. 50, no. 6, pp. 767 – 773, 2010, 2009 Reliability of Compound Semiconductors (ROCS) Workshop).

[31] M. Ťapajna, N. Killat, V. Palankovski, D. Gregušová, K. Čičo, J.-F. Carlin, N. Grandjean, M. Kuball, and J. Kuzmik, "Hot-electron-related degradation in InAlN/GaN high-electron-mobility transistors," *IEEE Transactions on Electron Devices*, vol. 61, no. 8, pp. 2793–2801, 2014.

[32] N. Braga, R. Mickevicius, R. Gaska, X. Hu, M. S. Shur, M. A. Khan, G. Simin, and J. Yang, "Simulation of hot electron and quantum effects in AlGaN/GaN heterostructure field effect transistors," *Journal of Applied Physics*, vol. 95, no. 11, pp. 6409–6413, 2004.

[33] A. M. Darwish, A. J. Bayba, and H. A. Hung, "Thermal resistance calculation of AlGaN-GaN devices," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, no. 11, pp. 2611–2620, Nov 2004.

[34] J. Pomeroy, M. Uren, B. Lambert, and M. Kuball, "Operating channel temperature in GaN HEMTs: DC versus RF accelerated life testing," *Microelectronics Reliability*, vol. 55, no. 12, pp. 2505 – 2510, 2015.

[35] M. Asif Khan, J. N. Kuznia, A. R. Bhattarai, and D. T. Olson, "Metal semiconductor field effect transistor based on single crystal GaN," *Applied Physics Letters*, vol. 62, no. 15, pp. 1786–1787, 1993.

[36] "Gallium Nitride: The Material that Made the Difference," https://engineering.ucsb.edu/news/gallium-nitride-material-made-difference.

[37] N. Goyal, "Design and Modeling of High-Power Semiconductor Devices with Emphasis on AlGaN/GaN HEMTs," PhD dissertation, Norges teknisk-naturvitenskapelige universitet - NTNU, 2013.

[38] L. Liu and J. H. Edgar, "Substrates for Gallium Nitride Epitaxy," *Materials Science and Engineering: R: Reports*, vol. 37, no. 3, pp. 61–127, 2002.

[39] Y. Ando, Y. Okamoto, H. Miyamoto, N. Hayama, T. Nakayama, K. Kasahara, and M. Kuzuhara, "A 110-W AlGaN/GaN heterojunction FET on thinned sapphire substrate," in *International Electron Devices Meeting. Technical Digest (Cat. No. 01CH37224)*. IEEE, 2001, pp. 17–3.

[40] F. Bernardini and V. Fiorentini, "Nonlinear macroscopic polarization in III-V nitride alloys," *Phys. Rev. B*, vol. 64, p. 085207, Aug 2001.

[41] O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, L. F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, and J. Hilsenbeck, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures," *Journal of Applied Physics*, vol. 85, no. 6, pp. 3222–3233, 1999.

[42] J. P. Ibbetson, P. T. Fini, K. D. Ness, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors," *Applied Physics Letters*, vol. 77, no. 2, pp. 250–252, 2000.

[43] E. T. Yu, G. J. Sullivan, P. M. Asbeck, C. D. Wang, D. Qiao, and S. S. Lau, "Measurement of piezoelectrically induced charge in GaN/AlGaN heterostructure field-effect transistors," *Applied Physics Letters*, vol. 71, no. 19, pp. 2794–2796, 1997.

[44] B. Jogai, J. Albrecht, and E. Pan, "Effect of electromechanical coupling on the strain in AlGaN/GaN heterojunction field effect transistors," *journal of Applied physics*, vol. 94, no. 6, pp. 3984–3989, 2003.

[45] A. Sarua, H. Ji, M. Kuball, M. Uren, T. Martin, K. Nash, K. Hilton, and R. Balmer, "Piezoelectric strain in AlGaN/GaN heterostructure field-effect transistors under bias," *Applied physics letters*, vol. 88, no. 10, p. 103502, 2006.

[46] Ancona,M. G. and Binari,S. C. and Meyer,D. J. , "Fully coupled thermoelectromechanical analysis of GaN high electron mobility transistor degradation," *Journal of Applied Physics*, vol. 111, no. 7, p. 074504, 2012.

[47] C. Y. Zhu, M. Wu, C. Kayis, F. Zhang, X. Li, R. A. Ferreyra, A. Matulionis, V. Avrutin, U. Ozgur, and H. Morkoc, "Degradation and phase noise of inaln/aln/gan heterojunction field effect transistors: Implications for hot electron/phonon effects," *Applied Physics Letters*, vol. 101, no. 10, p. 103502, 2012.

[48] M. Meneghini, I. Rossetto, D. Bisi, A. Stocco, A. Chini, A. Pantellini, C. Lanzieri, A. Nanni, G. Meneghesso, and E. Zanoni, "Buffer traps in Fe-doped AlGaN/GaN HEMTs: Investigation of the physical properties based on pulsed and transient measurements," *IEEE Transactions on Electron Devices*, vol. 61, no. 12, pp. 4070–4077, 2014.

[49] M. Meneghini, M. Bertin, G. dal Santo, A. Stocco, A. Chini, D. Marcon, P. E. Malinowski, G. Mura, E. Musu, M. Vanzi, G. Meneghesso, and E. Zanoni, "A novel degradation mechanism of AlGaN/GaN/Silicon heterostructures related to the generation of interface traps," in *2012 International Electron Devices Meeting*, Dec 2012, pp. 13.3.1–13.3.4.

[50] M. Meneghini, D. Bisi, D. Marcon, S. Stoffels, M. Van Hove, T.-L. Wu, S. Decoutere, G. Meneghesso, and E. Zanoni, "Trapping in GaN-based metal-insulator-semiconductor transistors: Role of high drain bias and hot electrons," *Applied Physics Letters*, vol. 104, no. 14, p. 143505, 2014.

[51] E. Zanoni, M. Meneghini, A. Chini, D. Marcon, and G. Meneghesso, "AlGaN/GaN-Based HEMTs Failure Physics and Reliability: Mechanisms Affecting Gate Edge and Schottky Junction," *IEEE Transactions on Electron Devices*, vol. 60, no. 10, pp. 3119–3131, Oct 2013.

[52] S. C. Binari, P. B. Klein, and T. E. Kazior, "Trapping effects in GaN and SiC microwave FETs," *Proceedings of the IEEE*, vol. 90, no. 6, pp. 1048–1058, Jun 2002.

[53] A. Sarua, T. Batten, H. Ji, M. Uren, T. Martin, and M. Kuball, "Thermal and piezoelectric stress in operating AlGaN/GaN HFET devices and effect of the Fe doping in the GaN buffer layer," in *CS MANTECH Conference*, 2009, p. 127.

[54] M. Shur, "GaN based transistors for high power applications," *Solid-State Electronics*, vol. 42, no. 12, pp. 2131 – 2138, 1998.

[55] M. Hosch, J. Pomeroy, A. Sarua, M. Kuball, H. Jung, and H. Schumacher, "Field dependent self-heating effects in high-power AlGaN/GaN HEMTs," in *CS Mantech Conference*, 2009, pp. 18–21.

[56] S. Singhal, J. Roberts, P. Rajagopal, T. Li, A. Hanson, R. Therrien, J. Johnson, I. Kizilyalli, and K. Linthicum, "GaN-on-Si failure mechanisms and reliability improvements," in *2006 IEEE International Reliability Physics Symposium Proceedings.* IEEE, 2006, pp. 95–98.

[57] H. Jung, R. Behtash, J. R. Thorpe, K. Riepe, F. Bourgeois, H. Blanck, A. Chuvilin, and U. Kaiser, "Reliability behavior of GaN HEMTs related to Au diffusion at the Schottky interface," *physica status solidi c*, vol. 6, no. S2 2, pp. S976–S979, 2009.

[58] E. Zanoni, G. Meneghesso, M. Meneghini, A. Stocco, F. Rampazzo, R. Silvestri, I. Rossetto, and N. Ronchi, "Electric-field and thermally-activated failure mechanisms of AlGaN/GaN high electron mobility transistors," *ECS Transactions*, vol. 41, no. 8, p. 237, 2011.

[59] C. Hodges, J. Anaya Calvo, S. Stoffels, D. Marcon, and M. Kuball, "AlGaN/GaN field effect transistors for power electronics Effect of finite GaN layer thickness on thermal characteristics," *Applied Physics Letters*, vol. 103, no. 20, p. 202108, 2013.

[60] Y. Wu, W. Sasangka, and J. A. del Alamo, "Anomalous Source-Side Degradation of InAlN/GaN HEMTs Under High-Power Electrical Stress," *IEEE Transactions on Electron Devices*, vol. 64, no. 11, pp. 4435–4441, 2017.

[61] B. Chatterjee, J. Lundh, J. Dallas, H. Kim, and S. Choi, "Electro-thermal reliability study of GaN high electron mobility transistors," in *2017 16th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm).* IEEE, 2017, pp. 1247–1252.

[62] Y.-H. Hwang, T.-S. Kang, F. Ren, and S. J. Pearton, "Novel approach to improve heat dissipation of AlGaN/GaN high electron mobility transistors with a Cu filled via under device active area," *Journal of Vacuum Science & Technology B*, vol. 32, no. 6, p. 061202, 2014.

[63] S. K. Mohanty, Y.-Y. Chen, P.-H. Yeh, and R.-H. Horng, "Thermal Management of Gan-on-Si High electron Mobility transistor by copper filled Micro-trench Structure," *Scientific Reports*, vol. 9, no. 1, pp. 1–9, 2019.

[64] M. Pourfath, V. Sverdlov, and S. Selberherr, "Transport modeling for nanoscale semiconductor devices," in *Solid-State and Integrated Circuit Technology (ICSICT), 2010 10th IEEE International Conference on*, Nov 2010, pp. 1737–1740.

[65] Synopsys Inc., "Sentaurus," https://www.synopsys.com/silicon/tcad/device-simulation/sentaurus-device.html.

[66] *Sentaurus Workbench User Guide, Synopsys Inc.*, L-2016.03 ed., March 2016.

[67] *Sentaurus Structure Editor User Guide, Synopsys Inc.*, L-2016.03 ed., March 2016.

[68] *Sentaurus Mesh UserGuide, Synopsys Inc.*, L-2016.03 ed., March 2016.

[69] *Sentaurus Device User Guide, Synopsys Inc.*, L-2016.03 ed., March 2016.

[70] *Sentaurus Visual User Guide, Synopsys Inc.*, L-2016.03 ed., March 2016.

[71] A. Endoh, I. Watanabe, A. Kasamatsu, and T. Mimura, "Monte Carlo simulation of InAlAs/InGaAs HEMTs with various shape of buried gate," in *2014 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, Sep. 2014, pp. 261–264.

[72] S. Karmalkar and U. K. Mishra, "Enhancement of breakdown voltage in algan/gan high electron mobility transistors using a field plate," *IEEE Transactions on Electron Devices*, vol. 48, no. 8, pp. 1515–1521, 2001.

[73] A. Ray, G. Kumar, S. Bordoloi, D. K. Sinha, P. Agarwal, and G. Trivedi, "Fem based device simulator for high voltage devices," in *VLSI Design and Test*, B. K. Kaushik, S. Dasgupta, and V. Singh, Eds. Singapore: Springer Singapore, 2017, pp. 127–135.

[74] X. D. Wang, W. D. Hu, X. S. Chen, and W. Lu, "The Study of Self–Heating and Hot–Electron Effects for AlGaN/GaN Double–Channel HEMTs," *IEEE Transactions on Electron Devices*, vol. 59, no. 5, pp. 1393–1401, May 2012.

[75] A. Sarua, H. Ji, K. P. Hilton, D. J. Wallis, M. J. Uren, T. Martin, and M. Kuball, "Thermal Boundary Resistance Between GaN and Substrate in AlGaN/GaN Electronic Devices," *IEEE Transactions on Electron Devices*, vol. 54, no. 12, pp. 3152–3158, Dec 2007.

[76] S. Mukherjee, E. Patrick, and M. Law, "Simulation of Deep-Level Trap Distributions in AlGaN/GaN HEMTs and Its Influence on Transient Analysis of Drain Current," *ECS Journal of Solid State Science and Technology*, vol. 6, no. 11, pp. S3093–S3098, 2017.

[77] T. Tanaka, N. Ito, M. Akutsu, K. Chikamatsu, S. Takado, and K. Nakahara, "Extraction of net acceptor type trap density in semi-insulating GaN layers grown on Si substrate by DC I–V measurement," *physica status solidi (a)*, vol. 214, no. 8, p. 1600925, 2017.

[78] A. Y. Polyakov and I.-H. Lee, "Deep traps in GaN-based structures as affecting the performance of GaN devices," *Materials Science and Engineering: R: Reports*, vol. 94, pp. 1–56, 2015.

[79] L. Lew Yan Voon and M. Willatzen, "Electromechanical phenomena in semiconductor nanostructures," *Journal of Applied Physics*, vol. 109, no. 3, p. 3, 2011.

[80] D. C. E. A. Jones, F. F. Wang, "Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 707–719, Sep. 2016.

[81] B. Sarkar, P. Reddy, F. Kaess, B. Haidet, J. Tweedie, S. Mita, R. Kirste, E. Kohn, R. Collazo, and Z. Sitar, "Material Considerations for the Development of III-Nitride Power Devices," *ECS Transactions*, vol. 80, no. 7, p. 29, 2017.

[82] F. Bernardini, V. Fiorentini, and D. Vanderbilt, "Spontaneous polarization and piezoelectric constants of III-V nitrides," *Phys. Rev. B*, vol. 56, pp. R10 024–R10 027, Oct 1997.

[83] Anwar,A. F. M. and Webster,Richard T. and Smith,Kurt V. , "Bias induced strain in AlGaN/GaN heterojunction field effect transistors and its implications," *Applied Physics Letters*, vol. 88, no. 20, p. 203510, 2006.

[84] H. Huang, Y. C. Liang, G. S. Samudra, T.-F. Chang, and C.-F. Huang, "Effects of Gate Field Plates on the Surface State Related Current Collapse in AlGaN/GaN HEMTs," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2164–2173, May 2014.

[85] S. Mizuno, Y. Ohno, S. Kishimoto, K. Maezawa, and T. Mizutani, "Large Gate Leakage Current in AlGaN/GaN High Electron Mobility Transistors," *Japanese Journal of Applied Physics*, vol. 41, no. Part 1, No. 8, pp. 5125–5126, aug 2002.

[86] T. Grasser, T.-W. Tang, H. Kosina, and S. Selberherr, "A review of hydrodynamic and energy-transport models for semiconductor device simulation," *Proceedings of the IEEE*, vol. 91, no. 2, pp. 251–274, 2003.

[87] M. P. Vaughan, "Hot Electron Transport," in *Semiconductor Modeling Techniques*. Springer, 2012, pp. 71–113.

[88] B. Ridley, "Hot electrons in low-dimensional structures," *Reports on Progress in Physics*, vol. 54, no. 2, p. 169, 1991.

[89] N. Shigekawa, K. Shiojima, and T. Suemitsu, "Electroluminescence characterization of AlGaN/GaN high-electron-mobility transistors," *Applied Physics Letters*, vol. 79, no. 8, pp. 1196–1198, 2001.

[90] T. Nakao, Y. Ohno, M. Akita, S. Kishimoto, K. Maezawa, and T. Mizutani, "Electroluminescence in AlGaN/GaN high electron mobility transistors under high bias voltage," *Japanese journal of applied physics*, vol. 41, no. 4R, p. 1990, 2002.

[91] J. He, Y. Chen, Z. He, Y. En, C. Liu, Y. Huang, Z. Li, and M. Tang, "Effect of Hot Electron Stress on AlGaN/GaN HEMTs of Hydrogen Poisoning," *IEEE Journal of the Electron Devices Society*, vol. 7, pp. 76–81, 2018.

[92] W. Hu, X. Chen, F. Yin, J. Zhang, and W. Lu, "Two-dimensional transient simulations of drain lag and current collapse in GaN-based high-electron-mobility transistors," *Journal of Applied Physics*, vol. 105, no. 8, p. 084502, 2009.

[93] S. Vitusevich, S. Danylyuk, N. Klein, M. Petrychuk, A. Y. Avksentyev, V. Sokolov, V. Kochelap, A. Belyaev, V. Tilak, J. Smart *et al.*, "Separation of hot-electron and self-heating effects in two-dimensional AlGaN/GaN-based conducting channels," *Applied physics letters*, vol. 82, no. 5, pp. 748–750, 2003.

[94] O. Mitrofanov and M. Manfra, "Poole-Frenkel electron emission from the traps in AlGaN/GaN transistors," *Journal of Applied Physics*, vol. 95, no. 11, pp. 6414–6419, 2004.

[95] S. Wienecke, B. Romanczyk, M. Guidry, H. Li, E. Ahmadi, K. Hestroffer, X. Zheng, S. Keller, and U. K. Mishra, "N-Polar GaN Cap MISHEMT With Record Power Density Exceeding 6.5 W/mm at 94 GHz," *IEEE Electron Device Letters*, vol. 38, no. 3, pp. 359–362, March 2017.

[96] T. Zimmermann, D. Deen, Y. Cao, J. Simon, P. Fay, D. Jena, and H. G. Xing, "AlN/GaN Insulated–Gate HEMTs With 2.3 A/mm Output Current and 480 mS/mm Transconductance," *IEEE Electron Device Letters*, vol. 29, no. 7, pp. 661–664, July 2008.

[97] R. Gaska, A. Osinsky, J. W. Yang, and M. S. Shur, "Self–heating in high-power AlGaN–GaN HFETs," *IEEE Electron Device Letters*, vol. 19, no. 3, pp. 89–91, 1998.

[98] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, and I. Omura, "Recessed–gate structure approach toward normally off high–Voltage AlGaN/GaN HEMT for power electronics applications," *IEEE Transactions on Electron Devices*, vol. 53, no. 2, pp. 356–362, Feb 2006.

[99] N. Ikeda, Y. Niiyama, H. Kambayashi, Y. Sato, T. Nomura, S. Kato, and S. Yoshida, "GaN Power Transistors on Si Substrates for Switching Applications," *Proceedings of the IEEE*, vol. 98, no. 7, pp. 1151–1161, July 2010.

[100] Y. Dora, A. Chakraborty, L. Mccarthy, S. Keller, S. P. Denbaars, and U. K. Mishra, "High Breakdown Voltage Achieved on AlGaN/GaN HEMTs With Integrated Slant Field Plates," *IEEE Electron Device Letters*, vol. 27, no. 9, pp. 713–715, Sept 2006.

[101] P. B. Klein, S. C. Binari, K. Ikossi, A. E. Wickenden, D. D. Koleske, and R. L. Henry, "Effect of deep traps on sheet charge in AlGaN/GaN high electron mobility transistors," *Electronics Letters*, vol. 37, no. 25, pp. 1550–1551, Dec 2001.

[102] M. J. Uren, S. Karboyan, I. Chatterjee, A. Pooth, P. Moens, A. Banerjee, and M. Kuball, "Leaky Dielectric Model for the Suppression of Dynamic R_{ON} in Carbon-Doped AlGaN/GaN HEMTs," *IEEE Transactions on Electron Devices*, vol. 64, no. 7, pp. 2826–2834, July 2017.

[103] M. Zhao, X. Wang, X. Liu, J. Huang, Y. Zheng, and K. Wei, "Thermal storage of AlGaN/GaN high-electron-mobility transistors," *IEEE transactions on device and materials reliability*, vol. 10, no. 3, pp. 360–365, 2010.

[104] F. Vitobello and A. Barnes, "Long duration high temperature storage test on GaN HEMTs," in *2012 IEEE International Reliability Physics Symposium (IRPS)*. IEEE, 2012, pp. 2C–4.

[105] J.-B. Fonder, L. Chevalier, C. Genevois, O. Latry, C. Duperrier, F. Temcamani, and H. Maanane, "Physical analysis of Schottky contact on power AlGaN/GaN HEMT after pulsed-RF life test," *Microelectronics Reliability*, vol. 52, no. 9, pp. 2205 – 2209, 2012, special Issue 23rd European Symposium on the Reliability of Electron Devices, Failure Physics and Analysis.

[106] N. Killat and M. Kuball, "Following an Electrons Journey Through a GaN HEMT," *Compound Semiconductor Magazine*, vol. 19, no. 1, pp. 69 – 72, Jan/Feb 2013.

[107] B. Padmanabhan, D. Vasileska, and S. Goodnick, "Reliability concerns due to self-heating effects in GaN HEMTs," *Journal of Integrated Circuits and Systems*, vol. 8, no. 2, pp. 78–82, 9 2013.

[108] A. Aouf, F. Djeffal, and F. Douak, "Thermal stability investigation of power GaN HEMT including self–heating effects," in *2017 6th International Conference on Systems and Control (ICSC)*, May 2017, pp. 451–454.

[109] J. D. Albrecht, R. P. Wang, P. P. Ruden, M. Farahmand, and K. F. Brennan, "Electron transport characteristics of GaN for high temperature device modeling," *Journal of Applied Physics*, vol. 83, no. 9, pp. 4777–4781, 1998.

[110] P. Mukhopadhyay, A. Bag, U. Gomes, U. Banerjee, S. Ghosh, S. Kabi, E. Y. Chang, A. Dabiran, P. Chow, and D. Biswas, "Comparative DC characteristic analysis of AlGaN/GaN HEMTs grown on Si (111) and sapphire substrates by MBE," *Journal of electronic materials*, vol. 43, no. 4, pp. 1263–1270, 2014.

[111] T. Batten, J. W. Pomeroy, M. J. Uren, T. Martin, and M. Kuball, "Simultaneous measurement of temperature and thermal stress in AlGaN/GaN high electron mobility transistors using Raman scattering spectroscopy," *Journal of Applied Physics*, vol. 106, no. 9, p. 094509, 2009.

[112] M. Kuball, M. Ťapajna, R. J. Simms, M. Faqir, and U. K. Mishra, "AlGaN/GaN HEMT device reliability and degradation evolution: Importance of diffusion processes," *Microelectronics Reliability*, vol. 51, no. 2, pp. 195–200, 2011.

[113] J.-M. Lee, B.-G. Min, C.-W. Ju, H.-K. Ahn, J.-K. Mun, J.-W. Lim, and E. Nam, "Analysis of the degradation of AlGaN/GaN HEMTs by high-temperature operation tests," *Journal of the Korean Physical Society*, vol. 64, no. 10, pp. 1446–1450, 2014.

[114] A. Sozza, C. Dua, E. Morvan, S. Delage, F. Rampazzo, A. Tazzoli, F. Danesin, G. Meneghesso, E. Zanoni, A. Curutchet *et al.*, "Evidence of traps creation in GaN/AlGaN/GaN HEMTs after a 3000 hour on-state and off-state hot-electron stress," in *IEEE InternationalElectron Devices Meeting, 2005. IEDM Technical Digest.* IEEE, 2005, pp. 4–pp.

[115] T. Kikkawa, K. Makiyama, T. Ohki, M. Kanamura, K. Imanishi, N. Hara, and K. Joshin, "High performance and high reliability AlGaN/GaN HEMTs," *physica status solidi (a)*, vol. 206, no. 6, pp. 1135–1144, 2009.

[116] M. Dipalo, M. Alomari, J. F. Carlin, N. Grandjean, M. A. Diforte-Poisson, S. L. Delage, and E. Kohn, "Thick nano–crystalline diamond overgrowth on InAlN/GaN devices for thermal management," in *2009 Device Research Conference*, June 2009, pp. 103–104.

[117] Y. Han, B. L. Lau, X. Zhang, Y. C. Leong, and K. F. Choo, "Enhancement of Hotspot Cooling With Diamond Heat Spreader on Cu Microchannel Heat Sink for GaN–on–Si Device," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 4, no. 6, pp. 983–990, June 2014.

[118] Z. Yan, G. Liu, J. M. Khan, and A. A. Balandin, "Graphene quilts for thermal management of high-power GaN transistors," *Nature Communications*, vol. 3, pp. 827–834, May 2012.

[119] M. Rosker, C. Bozada, H. Dietrich, A. Hung, D. Via, S. Binari, E. Vivierios, E. Cohen, and J. Hodiak, "The DARPA wide band gap semiconductors for RF applications (WBGS-RF) program: Phase II results," *CS ManTech*, vol. 1, 2009.

[120] P. B. Klein, S. C. Binari, K. Ikossi-Anastasiou, A. E. Wickenden, D. D. Koleske, R. L. Henry, and D. S. Katzer, "Investigation of traps producing current collapse in AlGaN/GaN high electron mobility transistors," *Electronics Letters*, vol. 37, no. 10, pp. 661–662, May 2001.

[121] N. Braga, R. Mickevicius, M. Shur, R. Gaska, M. A. Khan, and G. Simin, "Simulation of gate lag and current collapse in GaN heterojunction field effect transistors," in *IEEE Compound Semiconductor Integrated Circuit Symposium, 2004.*, Oct 2004, pp. 287–290.

[122] W. D. Hu, X. S. Chen, and W. Lu, "Intrinsic Mechanism of Drain-Lag and Current Collapse in GaN-Based HEMTs," in *2009 IEEE Workshop on Microelectronics and Electron Devices*, April 2009, pp. 1–3.

[123] J. Joh, N. Tipirneni, S. Pendharkar, and S. Krishnan, "Current collapse in GaN heterojunction field effect transistors for high-voltage switching applications," in *2014 IEEE International Reliability Physics Symposium*, June 2014, pp. 6C.5.1–6C.5.4.

[124] M. Wang, D. Yan, C. Zhang, B. Xie, C. P. Wen, J. Wang, Y. Hao, W. Wu, and B. Shen, "Investigation of Surface and Buffer-Induced Current Collapse in GaN High-Electron Mobility Transistors Using a Soft Switched Pulsed (I-V) Measurement," *IEEE Electron Device Letters*, vol. 35, no. 11, pp. 1094–1096, Nov 2014.

[125] P. Wutimakun, H. Miyazaki, Y. Okamoto, J. Morimoto, T. Hayashi, and H. Shiomi, "Studies of Thermal Anisotropy in 4H-, 6H-SiC Bulk Single Crystal Wafers by Photopyroelectric (PPE) Method," in *Materials Science Forum*, vol. 600. Trans Tech Publ, 2009, pp. 521–524.

[126] J. P. Freedman, J. H. Leach, E. A. Preble, Z. Sitar, R. F. Davis, and J. A. Malen, "Universal phonon mean free path spectra in crystalline semiconductors at high temperature," *Scientific reports*, vol. 3, no. 1, pp. 1–6, 2013.

[127] H.-K. Sung, T. Qiang, Z. Yao, Y. Li, Q. Wu, H.-K. Lee, B.-D. Park, W.-S. Lim, K.-H. Park, and C. Wang, "Vertical and bevel-structured sic etching techniques incorporating different gas mixture plasmas for various microelectronic applications," *Scientific reports*, vol. 7, no. 1, pp. 1–9, 2017.

[128] http://www.ioffe.ru/SVA/NSM/Semicond/GaN/thermal.html#Lattice%20properties, 1988.

[129] http://www.ioffe.ru/SVA/NSM/Semicond/SiC/thermal.html, 1988.

List of Publications

Journals

1. **Ashok Ray**, Sushanta Bordoloi , Biplab Sarkar, Pratima Agarwal and Gaurav Trivedi, "*Numerical Simulation of Enhanced-Reliability Filleted-Gate AlGaN/GaN HEMT*" J. Electro. Mater., 2020, 49, (3), pp. 20182031

2. Sushanta Bordoloi, **Ashok Ray**, and Gaurav Trivedi "*Simulation Framework for GaN Devices with Special Mention to Reliability Concern*" VLSI and Post-CMOS Devices, Circuits and Modelling, IET book chapter

3. Sushanta Bordoloi, **Ashok Ray**, and Gaurav Trivedi; "*Introspection into Reliability Aspects in AlGaN/GaN HEMTs with Gate Geometry Modification*", IEEE Access (under review), May 2021

4. **Ashok Ray**, Sushanta Bordoloi, Pratima Agarwal, and Gaurav Trivedi; "*Heat Extraction from Gate Junction through elevated Silicon Carbide Substrate Pillar*", IEEE, Transactions on Electron Devices (to be communicated), June 2021

5. Sushanta Bordoloi, **Ashok Ray**, and Gaurav Trivedi; "*Access Region Stack Engineering for Mitigation of Degradation in AlGaN/GaN HEMTs with Field Plate*", IEEE Transactions On Device And Materials Reliability (under review), May 2021

Conferences

1. **Ashok Ray**, Sushanta Bordoloi, Pratima Agarwal and Gaurav Trivedi "*Investigation of electrical aspect in lateral and vertical SiC Diodes*" XXth International Workshop on the Physics of Semiconductor Devices (IWPSD2019), 17-20 December 2019, Kolkata.

2. Koushik Bharadwaj, **Ashok Ray**, Sushanta Bordoloi and Gaurav Trivedi "*Current Collapse reduction technique using N-doped buffer layer into the bulk region of a Gate Injection Transistor*" 32nd International Conference on VLSI Design

3. **Ashok Ray**, Gaurav Kumar, Sushanta Bordoloi, Dheeraj Kumar Sinha, Pratima Agarwal, and Gaurav Trivedi, "*FEM based Device Simulator for High Voltage Devices*" 21st International Symposium on VLSI Design and Test (VDAT 2017) IIT Roorkee, INDIA

Other Publications

1. Dheeraj Sinha, M Ansari, **Ashok Ray**, Gaurav Trivedi and Amitabh Chatterjee, "*Anomalous Switching Behavior and Selection of Trigger Transistor - A New Perspective for Marx-bank Circuit*" IEEE Transactions on Plasma Science vol. 46, no. 6, pp. 2064-2071, June 2018.

2. Gaurav Kumar, Mandeep Singh, **Ashok Ray**, Gaurav Trivedi, "*An FEM based Framework to Simulate Semiconductor Devices Using Streamline Upwind Petrov-Galerkin Stabilization Technique*" 27th international conference Radioelektronika 2017, Brno, Czech Republic.