Performance Improvement of Low Power LNA using Novel PVT Compensation Circuit and Current-Reuse Technique

A

Thesis submitted

for the award of the degree of

DOCTOR OF PHILOSOPHY

Under the supervision of

Prof. Roy Paily

and

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DECLARATION

*This is to certify that the thesis entitled "**Performance Improvement of Low Power LNA using Novel PVT Compensation Circuit and Current-Reuse Technique**", submitted by me to the Indian Institute of Technology Guwahati for the award of the degree of **Doctor of Philosophy** is a bonafide work carried out by me under the supervision of **Prof. Roy P Paily and Prof. Anil Mahanta**. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.*

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Certificate

This is to certify that the thesis entitled "**Performance Improvement of Low Power LNA using Novel PVT Compensation Circuit and Current-Reuse Technique**", submitted by **VINAYA M.M.** (10610213), a research scholar in the *Department of Electronics and Communication Engineering, Indian Institute of Technology Guwahati*, for the award of the degree of **Doctor of Philosophy**, is a record of an original research work carried out by him under our supervision and guidance. The thesis has fulfilled all requirements as per the regulations of the institute and in our opinion has reached the standard needed for submission. The results embodied in this thesis have not been submitted to any other University or Institute for the award of any degree or diploma.

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To

My dear Guruji

Sri Sri

&

My supervisors, family members and friends

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Abstract

In future communication systems, the requirement is not only for improving the quality of service but also towards finding an integrated solution for all the existing standards. Consequently, the coming generation RF system-on-chips (SOCs) must have the ability to cover a wide range of spectrum for different applications without much relaxation in their energy consumption. The transceiver SOCs may require multiple LNAs (low-noise amplifier), a key component of the receiver, where the LNA count increases almost proportionally with the number of supporting bands. Further, added diversity features incorporated in applications like LTE (Long Term Evolution) may use techniques such as massive MIMO (Multiple Input Multiple Output) that increase the hardware (the number of LNAs) requirement compared to earlier single input and single output (SISO) systems. Moreover, LNAs are one of the major power consuming blocks in a receiver. One must therefore design an LNA to operate at as low a power as possible while maintaining the minimum noise performance and acceptable linearity requirement. The scope of this research is motivated by the implementation challenges of low power, low noise amplifiers, particularly in sub-nanometer technology.

The LNA exhibits three key issues when it is designed for low power conditions in sub-nanometer technological nodes. Firstly, reliability becomes a major concern in sub nanometer technology nodes. The performance parameters undergo large deviations when circuits are subjected to unavoidable PVT (process-voltage-temperature) variations. These demand development of compensation circuits to improve the reliability of the amplifier. Secondly, the performance parameters such as gain and noise undergo degradation. Therefore, topological modifications to the conventional techniques are necessary to enhance the performances when they are operating under low power conditions. Thirdly, circuit integration along with passive elements becomes unrealizable through conventional implementations in advanced technology nodes (like 65nm or below), particularly for low noise

amplifiers.

To begin with, the initial approach to address these issues involved a thorough investigation of an MOS device performance in Strong, Moderate, and Weak inversion (SI, MI, WI) regions. It is explored in this thesis whether LNA devices operating in MI offer a better noise-power trade-off as compared to the conventional SI regions implementations. In addition, it is explored whether full system integration is always the viable option for low power circuit implementation. Further, the suitability of implementing sub-mW powered LNA is also investigated for applications like LTE by deducing the system level requirement from the specifications of the LTE standard.

Coming to the reliability issue, effective compensation circuits based on simple current comparison techniques are introduced to nullify the PVT variations and to improve the reliability of the amplifier. In addition to the realization of compensation mechanisms, a novel low voltage constant current reference (CCR) based on beta multiplier is introduced in this thesis. Finally, a gain enhancement technique based on the current-reuse topology is introduced to balance the degradation due to the low power operating conditions. Overall, this thesis has introduced circuit techniques along with an investigative study for improving the performance of low-power low-noise amplifiers.

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List of Acronyms

ADC	Analog-to-Digital Converters
AC	Alternating Current
BOM	Bill-of-Materials
B4G	Beyond 4G
BLE	Bluetooth Low Energy
BPF	Band pass Filter
CTAT	Complementary to Absolute Temperature
CCR	Constant Current Reference
CSF	Channel Selection Filter
CS	Common Source
CD	Common Drain
CG	Common Gate
CMOS	Complementary Metal-Oxide-Semiconductor
CBT	Conventional Biasing Technique
D2D	Device-to-Device
DC	Direct Current
DCR	Direct Conversion Receiver
DT	Discrete Time
DSP	Digital Signal Processing
DVB	Digital Video Broadcasting
Dup_{ISO}	Duplexer Isolation
FPFA	Field Programmable Filter Arrays
FN	Flicker Noise
FOM	Figure of Merit

FDD	Frequency Division Duplexing
FE_{loss}	Frontend Loss
GSM	Global System for Mobile Communications
HT	Hilbert Transform
IIP	Input Intercept Point
IF	Intermediate Frequency
IR	Image Rejection
IM	Intermodulation
IPN	Integrated Phase Noise
IoT	Internet of Things
KCL	Kirchhoff's Current law
KVL	Kirchhoff's Voltage law
LO	Local Oscillator
LTE	Long Term Evolution
LNA	Low Noise Amplifier
LPF	Low Pass Filter
LPLNA	Low Power LNA
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MIMO	Multiple Input Multiple Output
MI	Moderate Inversion
NF	Noise figure or Noise factor
NTT	Nippon Telegraph and Telephone
OFDM	Orthogonal Frequency Division Multiplexing
OTA	Operational Transconductance Amplifier
OOB	Out Of Band
PAR	Peak-to-Average Ratio
PSD	Power Spectral Density
PCSNIM	Power Constrained Simultaneous Noise and Impedance Matching
PA	Power Amplifier
PBT	Proposed Biasing Technique

PTAT	Proportional to Absolute Temperature
PVT	Process-Voltage-Temperature
RF	Radio Frequency
SAW	Surface Acoustic Wave
SDR	Software Defined Radio
SISO	Single Input Single Output
SNR	Signal-to-Noise Ratio
SIR	Signal-to-Interference Ratio
SI	Strong Inversion
SOC	System-On-Chip
TDD	Time Division Duplexing
VGA	Variable Gain Amplifier
VLC	Visible Light Communications
VCO	Voltage Controlled Oscillator
WI	Weak Inversion
WPAN	Wireless Personal Area Network
ZTC	Zero Temperature Coefficient

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1

Introduction

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1.1 Motivation

Compared to any other system of communication, mobile telephony has become the most dominant form of communication with more than 3.6 billion mobile subscribers around the globe [1]. The increasing popularity of cellular phones brings in a lot of commercial interests and this, in turn, creates wide opportunities for research in RF communications. Several wireless communication standards have been developed over the past few decades to address the growing and the varying needs of the users. To support the future trends, the cellular technology has transcended from person-to-person communication towards device-to-device communication.

The first generation (1G) cellular network was launched in Japan by NTT (Nippon Telegraph and Telephone) in 1979 [2]. Voice communication was the sole service in 1G cellular network system. Digital era in wireless communication began in the second generation with the introduction of GSM (Global System for Mobile Communications) where the data transmission was also included in addition to the voice service. The migration to the development of third-generation systems took place for the need of transmitting integrated voice, data, and multimedia information. Further enhancement of data rates and supporting additional services such as DVB (Digital Video Broadcasting) and Mobile TV are added for 4G as in LTE advanced systems. Beyond 4G (B4G) is a heterogeneous network, it envisages combining mm-wave communication, visible light communications (VLC), WiFi and features such as Internet of Things (IoTs) and device-to-device (D2D) communications [3, 4]. In addition, cognitive ability is also an important aspect for improving the spectrum efficiency [5]. The evolution of the wireless technology with supporting main features is summarized in Fig 1.1.

Further, the coming 5G technology will be capable not only of accommodating users for voice and data services, in addition it will be able to accommodate several devices for purpose of device-to-device communications and IoTs on its network. In this regard, it is estimated that around 50 billion devices will be connected on a cellular network platform worldwide by 2020 [6]. Integrating heterogeneous environment through internet cloud where everything is connected to a single node will become the leading technology in the coming years. The composite may start from health to infrastructure monitoring, measure the environmental conditions, and also would allow remote controlling of devices, for which data can be accessible and the controlling information can be sent from anywhere and at any time. In addition to the data exchange capability, achieving the connectivity through "Internet of Things (IoT)" has enormous challenges, possibilities, and applications.

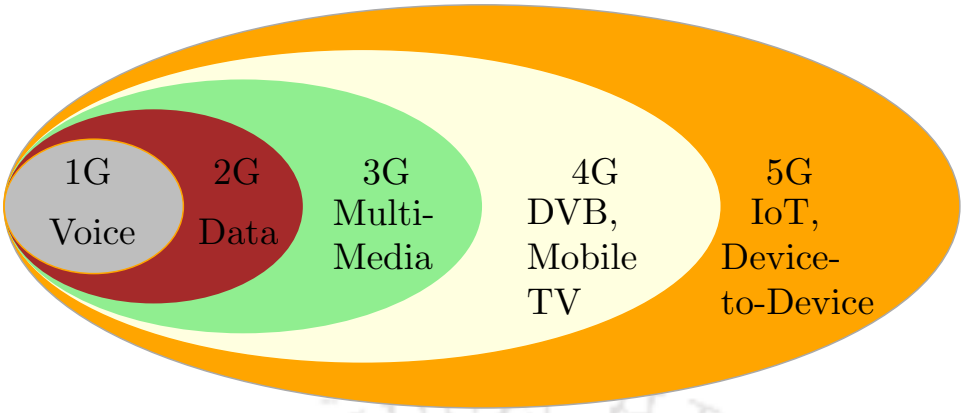

Figure 1.1: The evolution of cellular standards.

The deployment of such an advanced system seeks solutions for several challenges in which going green would become a major constraint. The development of energy efficient systems is highly desirable to curb large amount of carbon emissions which in turn help in protecting the environment [4]. Further, future applications will demand small sized systems [7] as connectivity and several functionalities are projected through multiple devices in the future. Hence, smart, small, self-sustainable and energy efficient devices or systems have to be developed with simultaneous improvement in their performances.

The trend of implementing several functionalities on-chip to yield SoCs (System-On-Chip) is critical in future as well. Only through SoCs, one can expect the development of energy efficient, miniature systems. In-order to support the roadmap mentioned above, the optimization and further development of SoCs in a multi-dimensional way are necessary. These have to be re-looked at various abstraction levels such as devices, circuits, and system architecture to find the solutions, in general, for the following issues.

- Tackling performance degradation issues due to low power operating conditions
- Issues related to increasing the manufacturing yield for advanced technology nodes
- Ways to increase the degree of integration on chip for reducing bill-of-materials (BOM)

For a wireless connectivity, RF SoCs play a significant role between air-to-system interfaces. In the up-coming wireless standards, the focus is not only on improving the quality of service but also towards finding the integrated solution for all the existing standards. In this regard, coming generation RF SOCs must have the ability to process multi-standard and multi-band signals without any relaxation in their energy consumption. Further, receivers, in particular, are needed to be highly sensitive as

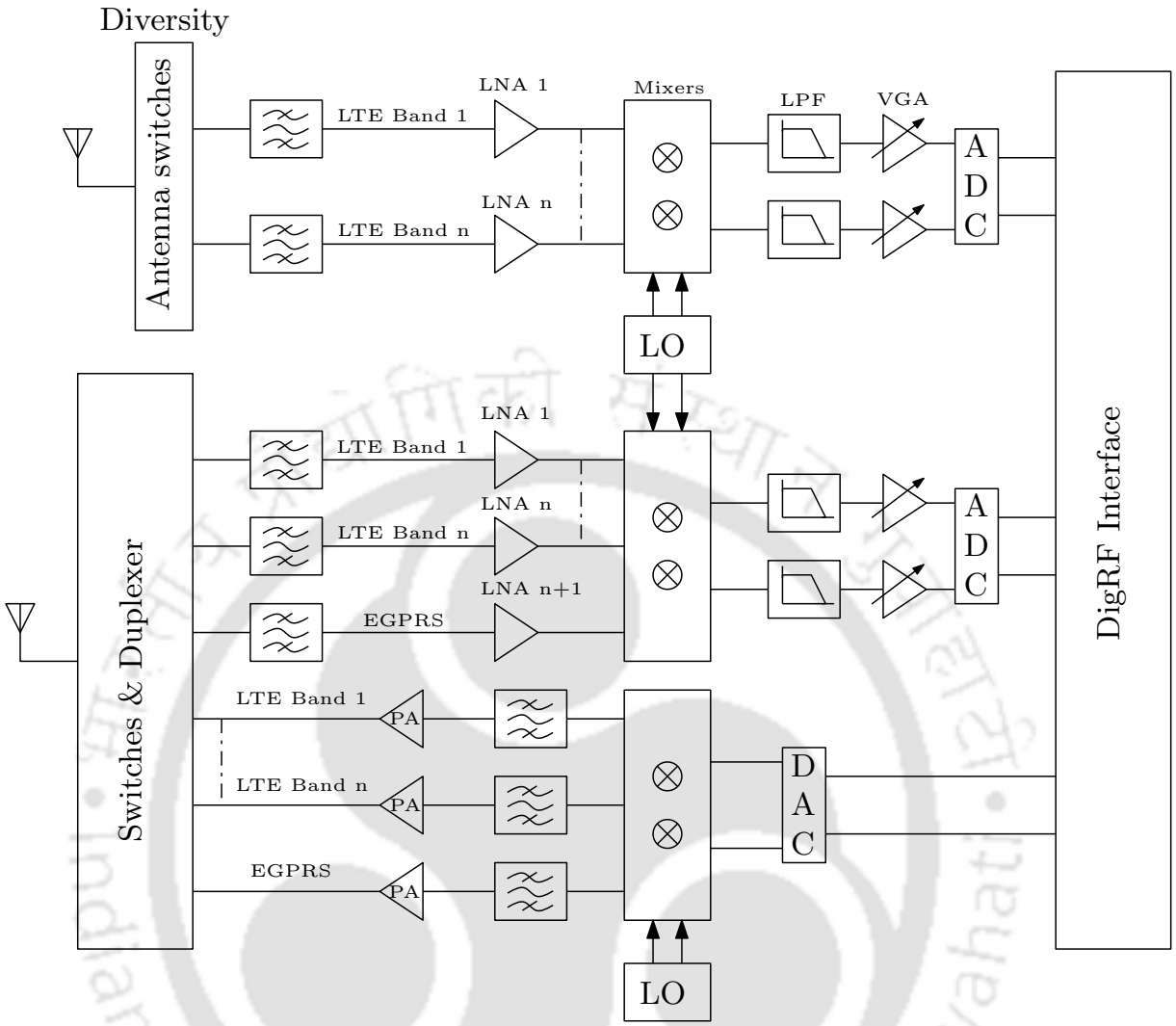

Figure 1.2: Multi-band transceivers.

D2D communication will be carried out in underlaying licensed cellular networks [8].

Transceivers are the vital components which are responsible for carrying the information between two nodes. The multi-band transceiver for LTE standard showcasing as a modern receiver is shown in Fig 1.2 [9] as an example. The RF front end of receiver consists of low noise amplifier (LNA), Mixers, filters and Analog-to-Digital Converters (ADC). The usage of MIMO (Multiple Input Multiple Output) technologies doubles the hardware requirement compared to SISO (Single Input Single Output) systems. It can be seen in Fig. 1.2 a separate diversity configuration is added in addition to the primary path. The prospective receiver will use massive MIMO that may consist of tens to hundreds of antennas [4] and consequently the number of diversity paths. Hence optimizing the performance of individual components by keeping the power consumption in prime focus is critical to build an overall

energy savvy system.

1.2 Problem definition

In the forthcoming receivers, usage of LNA is inevitable because of the necessity to implement highly sensitive receivers. Moreover, LNAs are one of the major power consumers in the receiver [10]. Transceiver SOCs may require multiple LNAs, a key component of the receiver, where the power consumption of individual amplifier is critical in order to prolong the battery life. Therefore, one must design an LNA to operate with as low a power as possible while maintaining an acceptable noise performance and linearity requirement. The current scope of this research is motivated by the implementation challenges of low power, low noise amplifiers. In this thesis, the performance degradation issues in low power LNAs are addressed along the following directions.

- Investigation of different MOS inversion regions to carry out better noise-power trade-off
- Improving the reliability of amplifier and the yield issues by introducing circuit accessories
- Investigation of the the suitability of low-power LNA for the current communication standard such as LTE
- A current-reuse topology is suggested for improving the gain performance of the low power amplifier

1.3 Organization of the Thesis

The thesis is organized into six chapters. The brief descriptions of these chapters are as follows.

Chapter 1 briefs about the motivation, problem definition, and the outline of the thesis.

Chapter 2 gives an introduction of RF front ends and the existing LNA topologies. Further, it gives a literature survey of the existing low power LNAs and highlights the trends of low power LNAs. Further, it discusses a method for deducing the performance requirement of the LNA from the specification of LTE standards. It briefs about the power level assignment to the LNA based on the system level budgeting of the LTE receiver. It details the procedure to carry out power optimization of LNA based on the LTE receiver requirement.

Chapter 3 discusses the analysis and the design challenges of sub-mW power LNAs. Further, it discusses implementation methodology for moderate inversion based LNAs. A unified noise figure

model is provided based on which noise can be estimated in any of the inversion regions. A microwatt LNA is implemented based on the given methodology and compared with other state of the art low power LNAs. Finally, it concludes by briefing the issues and challenges of low power LNAs, particularly for sub-nanometer technology implementations.

Chapter 4 gives a detailed work of the development of compensation circuits for near sub-threshold LNAs. In addition, it gives details about the implementation of low voltage constant current reference (CCR) which is used as one of the basic building blocks for implementing compensation mechanisms. This chapter showcases a compensated microwatt powered LNA which shows minimum deviations when it undergoes PVT variations. Further along with the PVT analysis, yield estimation is presented in this chapter to show the effectiveness of the suggested compensation techniques. Finally, depending on the deduced requirement from the LTE specification, a compensated microwatt powered LNA is implemented satisfying the sensitivity requirement of LTE receiver. It shows the feasibility of implementing a microwatt LNA for LTE receiver.

Chapter 5 gives a G_m enhancement technique based on current-reuse mechanisms. It discusses the implementation details and further gives the comparison between conventional and the suggested technique. The comparison with other state of the art current-reuse LNAs and other low power LNAs are also given at the end of the chapter.

Chapter 6 lists conclusions of the current research and outlines a few directions for future work based on the prospective receiver requirements.

1.4 Conclusion

A single transceiver system which has the provision to support a diverse range of applications is desirable in future communication scenarios. Besides this ability, it is expected to be reliable, cost-effective and compact while consuming as a low power as possible. In this regard, the performance of each individual unit of the transceivers must be optimized while keeping the lower power consumption as the primary focus. To begin with, an LNA, a key component of the receiver, is considered and issues such as reliability improvement and performance such as gain improvement are addressed in this thesis.

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2

Introduction to RF front ends and LNAs

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2.1 Introduction

The performance of RF systems depends on several factors. To meet the required specifications, several combinations of modulation and detection techniques are used depending on their noise immunity, the complexity, and the cost of implementation. In addition, an appropriate selection of multiple access techniques guarantees proper communication between multiple users. The selection of transceiver architecture also plays a major role in fulfilling the required performance.

A transceiver is a unit which contains a receiver and a transmitter for an effective two-way communication. Power, size, and cost are always the worrying factors and the degree of integration is of serious concern to reduce the number of external components required [11]. In addition, interoperability and robustness being the primary criteria for choosing particular transceiver architecture. Because of the noise and the interference rejection requirements, receiver implementation is more challenging compared to the transmitter. Hence, only the receiver architectures are considered here.

Receivers consist of multiple blocks where LNA is one of the important units situated at the front end. The spectrum range is broadly decided by the selection of particular LNA topology. Further, the total receiver sensitivity depends on the performance of this amplifier. Therefore, the choice of LNA topology is an important factor as it influences the overall performance of the receiver. In addition to the RF receiver front end, this chapter briefs about the available LNA topologies and further gives a comparison between their performances.

For future applications, batteryless systems are ideally expected and in such cases, it must scavenge the energy from ambient sources. Though it is not a reality in current applications such as radio communication, however, systems have to be progressively developed to gradually meet this roadmap. Power-centric designs that focus on lowering the power consumption towards reaching this requirement are essential. Therefore, power optimization is an important aspect and this chapter further gives an example to carry out power and performance trade-off for an LNA to a specific application like LTE.

2.2 Receiver architectures

The incoming RF signal cannot be fed directly to the ADC (Analog-to-Digital Converter) as it increases the requirement of the converter in-terms of bit resolution, input bandwidth and sampling frequencies which in turn increases the power requirement. Hence, the signal is pre-processed using blocks such as LNA, mixer, filter that situates at the front end of the RF receiver. Consequently,

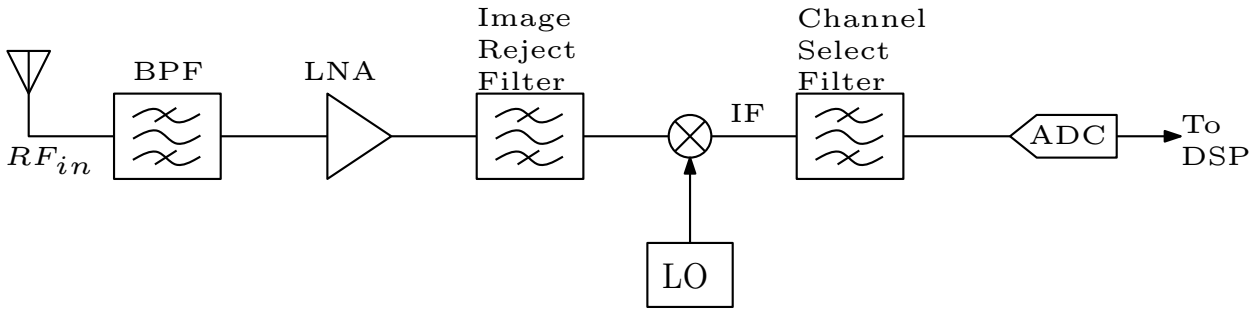

Figure 2.1: The architecture of Superheterodyne receiver.

a receiver chain consists of band-select filters, low-noise amplifiers, mixers, channel selection filters, ADCs and DSP blocks. In advanced receivers, the channel selection is done in the digital domain. Different types of architectures exist depending on the usage of distinct image rejection techniques and the way the IF (Intermediate Frequency) is being handled.

2.2.1 Superheterodyne receiver

The primary basic building blocks of this architecture is shown in Fig 2.1. The LNA amplifies an incoming signal from the antenna and then feeds it to a mixer for downconversion after passing through a filter called image rejection (IR) filter. The down-converted and filtered signal is then passed to the ADC for digitization. The channel selection may be carried out using channel selection filter (CSF) either at the front end or in the baseband processor. The IR filters are necessary to avoid signal corruption due to the presence of images.

In modern receivers the super-heterodyne architecture is less preferred because of the necessity of the IR filter. The IR filter is generally implemented by an off-chip, high-Q SAW filter which increases the bill of materials. Moreover, a trade-off is required between the image rejection and the channel selection requirements. The seperation between an RF signal and its image depends on the selection of the IF value in the receiver. The higher the value of the IF, the larger will be the spectral distance between these two signals. As a result, the image can be effectively suppressed by the given IR filter. However, a large IF imposes a restriction on realizing high-Q on-chip CSF. On the other hand, selection of low IF leads to poor image rejection but relaxes constraints on CSF implementation. Therefore, it may necessitate dual downconversion to relax this trade-off [12]. Dual conversion super-heterodynes are bulky and consume a large amount of power. Fortunately, there are recent advancements in building on-chip BPF using N-path filtering [13] with progressive filtering

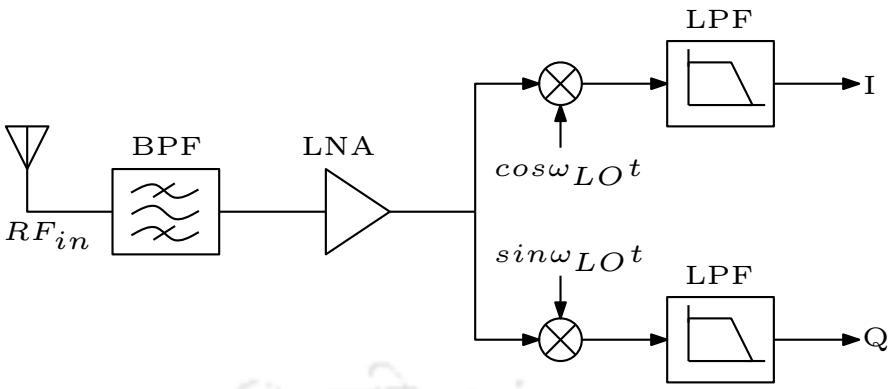

Figure 2.2: The architecture of Direct Conversion Receiver with a quadrature down-conversion.

technique [14] or Discrete Time (DT) Charge Sharing (CS) BPF [15] which may bring back the usage of superheterodyne architecture in modern receivers. The image problem is solved in Zero-IF receivers. Image reject receivers are also introduced for image rejection in low-IF receivers.

2.2.2 Zero-IF receiver

The integration issue in the super-heterodyne receiver is completely solved by downconverting the incoming signal to DC. The Zero-IF is also called as Direct Conversion Receiver (DCR) or homodyne receiver. As a DCR architecture does not leave any provision for images, there is no necessity for the inclusion of bulky off-chip IR filters. Therefore, the entire receiver can be implemented on-chip thereby improving the degree of integration. On the other hand, the input signal is required to be quadrature downconverted because the incoming asymmetric signal would lead to self-corruption after its frequency translation [12]. The DCR with quadrature downconversion is shown in Fig. 2.2.

The Zero-IF receiver despite avoiding the image problem, it suffers from issues such as signal corruption due to DC offsets, I/Q mismatch, LO leakage to the antenna, the effect of flicker noises and an even order distortion. These issues are as follows.

- DC offsets: The main cause of corruption due to DC offset is the leakage from LO (Local Oscillator) to the input of the LNA. This leads to self-mixing of the signal and due to that the resulting signal falls in the desired spectrum centered at DC. Another possibility is an appearance of any interference which may get down converted to near DC and thereby corrupting the desired signal [16]. The capacitive AC coupling can be used to avoid the offset corruption. However, there are three problems associated with it [17]. Firstly, the required R and C values are quite high as the desired frequency is low. Secondly, the response is slow to transient change in

offsets because of the increased time constant. Thirdly, the signal which is having energy at DC gets corrupted as these are blocked due to AC coupling. Hence, digitally assisted calibration techniques are normally employed to solve this issue [16–18].

- I/Q mismatch: Asymmetrically occurring signal undergoes self-corruption when the incoming signal is directly downconverted to Zero-IF spectrum. Hence, quadrature down-conversion is used which is done in two separate paths called I (In-phase) and Q (Quadrature phase) paths. These two paths are symmetrical and are processed together to correctly reconstruct the original signal. However, as there always exists some degree of imbalance among these two paths, this creates a signal corruption. In addition to the focus on creating symmetrical layouts, calibration techniques are used for nullifying I/Q mismatches [12].

- Even order distortion: The non-ideality in a mixer that causes it to pass a low-frequency component without any frequency translation is known as feed-through phenomenon. Because of these effects, the even order distorted components from an LNA appears in the desired spectrum at the output of the mixer which in turn results in corrupting the original information. In addition, asymmetries in the devices of the mixer also lead to the generation of even order distortion. In another possibility, the second harmonic of input RF signal mixes with the second harmonic of LO and causes baseband signal corruption. Further, the even order distortions are responsible for demodulating the varying envelope signals into the baseband spectrum [12, 17]. This is a severe problem in widely used modulation schemes such as OFDM (Orthogonal Frequency Division Multiplexing) which exhibits a large PAR (Peak-to-Average Ratio). Calibration techniques are used with direct conversion receivers to reduce even order distortions [11].

- LO leakage and flicker noises: A proper isolation is required for LO leakage otherwise it will lead to spurious emissions at the antenna terminals [16]. The usage of differential LO by maintaining symmetric path towards input pad would help in minimizing the LO leakage emissions at the antenna terminal [12]. As regards the flicker noise, the output of mixer tends to get affected by this noise because the downconverted signal is centered around the zero frequency. The device sizes in the circuit blocks followed by mixers have to be relatively increased in-order to minimize the flicker noise effects. In addition, periodic offset cancellation can also be used to suppress the effects [17].

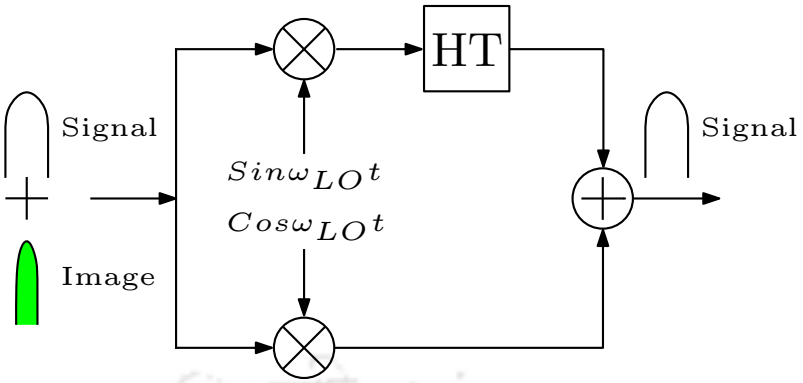

Figure 2.3: The block diagram of an Image Reject Receiver.

2.2.3 Image-Reject Receivers

The zero-IF receiver that evolved from the superheterodyne topology offers simplistic solutions for avoiding images in the desired spectrum. Despite being the widely preferred architecture, it is susceptible to other non-idealities mentioned above. As an alternative, images can be suppressed by using image canceling mechanisms which are carried out by Image-reject receivers.

The Image-Reject receivers process both signal and images in such a way that the ultimate residues will be free of any images. The conceptual diagram highlighting the techniques of image rejection is shown in Fig. 2.3. The block "HT" shown in the figure indicates the Hilbert Transform. Because of the Mixer and the HT, signals and images are processed differently and thereby it offers provision for image cancelation.

The resulting spectral components at each block for LO low-side injection is shown in Fig. 2.4. For a $Sin\omega_{LO}t$ LO, the signal below ω_{LO} undergoes in positive HT and the signal above ω_{LO} undergoes a negative HT. Mathematically, it is nothing but the multiplication of an actual signal by a signum function, $[-jsgn(\omega)]$. On the other hand, both the signal and the image fall in the same spectrum band after down-conversion with the $Cos\omega_{LO}t$ LO signal. For simplicity, amplitudes of both the signal and the image are assumed to be A. When these get processed by an image reject topology, images fall out of phase with each other and get canceled while keeping only the desired signal in the final outcome. This is as depicted in Fig. 2.4.

Image cancellation is accomplished by using Hartely or Weaver architectures. The shown conceptual diagram in Fig. 2.3 depicts the Hartely architecture. The Weaver architecture differs from the Hartley architecture by the way the Hilbert transform is carried out. In the latter topology, RC-CR

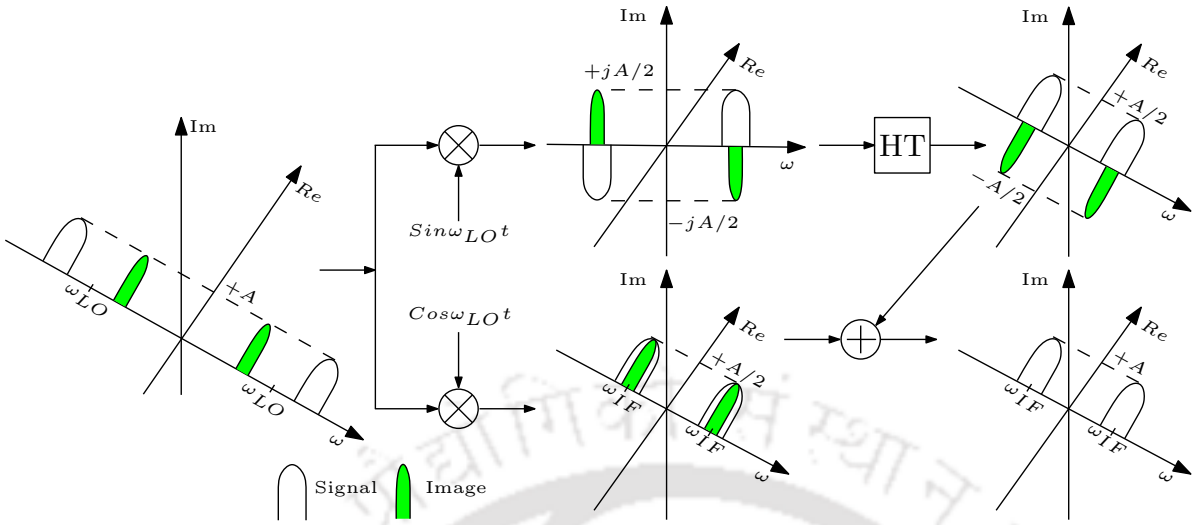

Figure 2.4: The spectral processing in an Image Reject Receiver for low-side LO injection.

network is used while in the former, two steps down-conversion is used to perform the Hilbert Transform. The usage of RC-CR results in a lower image rejection because of two reasons [12]. Firstly, R and C values in RC to CR network are never identical and the mismatch always exists in these two values. Secondly, the converging point for the gains of RC and CR networks exists only at a single point. Hence, the RC and the CR networks result in a different gain overall when the signal frequency deviates from the point of concurrence where the gain difference results in a limited image rejection. Moreover, both architectures yield a limited image rejection because of the gain and mismatch between two parallel paths. Hence, a calibration technique [19–21] has to be associated with these type of architectures to achieve image rejections above 40 dB [12].

2.2.4 Low-IF receivers

The integration issue in the superheterodyne receiver and the DC offsets and 1/f noise issues of the direct-conversion rceiver are solved in low-IF receivers. In these types of receivers, the IF is kept slightly above zero to avoid offset and 1/f noise issues and yet still maintaining a relatively low IF value so that it can be easily processed by on-chip filters and A-to-D converters. Low-IF receivers are suitable in the circumstances where desired signals are surrounded by weak interferences [22].

Since IF is not equal to zero like DCRs, there is a stringent requirement on the image rejection as compared to DCRs as image falls in the nearby desired channels [23]. It requires the usage of complex polyphase filters to get a higher image rejection ratio [12, 24]. Further, the phase and amplitude mismatches between I and Q branches put a serious limitation on the image rejection and this requires

a digital error correction mechanisms to achieve an effective higher IRR (Image Rejection Ratio) [25]. Moreover, it would increase the requirements on the ADC as compared to DCRs [26].

2.2.5 Architectures for Modern Radios

A reconfigurable RF front-end which has the ability to process any frequency signal and which in particular can be easily programmed by a software, will be the ultimate system in future. Cost reduction per radio while addressing the performance enhancement issues faces multiple implementation challenges. From introducing several circuit techniques at each block level to architectural modifications are carried out in the current state of the art receivers to realize efficient radios and are known as Software-Defined-Radios (SDRs). The multi-band and multi-standard approaches are investigated to find unique hardware solutions to cover a wide range of the spectrum.

The presence of SAW filters in superheterodyne technology assisted the system in removing powerful blockers thereby relaxing the linearity requirement of the overall RF front end. However, it adds to the cost, size and complexity for multi-standard or multi-band receivers [11, 15, 27]. Moreover, tunability and on-chip implementations become issues while inserting SAW filters [28–30]. On the other hand, removal of external filters such as SAW filters tightens the linearity requirement and demands for implementation of blocker removal techniques.

The majority of systems in the literature prefer to employ Zero/Low IF techniques because of the flexibility in integration. In some, multi-standard and multi-band systems have used either universally or separately zero or low IF topologies depending on the surrounding interference environment for the particular bands [11, 27]. Besides, there are implementations which switch to different schemes such as zero IF or low IF depending on the performance level requirement of the receiver [31]. As discussed above, zero/low IF always are accompanied by calibration techniques. Although zero-IF are widely accepted, the super-heterodynes are currently being investigated with the introduction of progressive filtering with the usage of on-chip filters [15].

Modern receivers are mostly wide band operative where these are associated with blocker removal techniques. N-path based filtering techniques are generally employed to nullify the strong blockers. These can be used at the mixers [28,30,32], or in a feedback translational loops with LNAs to improve the linearity of the receivers. However, wide-band receivers are still inferior in sensitivity and blocker suppression compared to narrow band systems [33]. Hence, separately optimized front ends are used for different bands [27, 31, 33, 34] to enhance these performances.

Coming to the duplexing schemes, these receivers use either the FDD (Frequency Division Duplexing) or the TDD (Time Division Duplexing) communication systems. The first technique uses two separate channels thus affecting the communication throughput while the latter technique increases the latency. Hence, in-band full duplex receiver is under investigation [35] which doubles the spectral efficiency. However, it suffers from self-interference issues. Consequently, in-band full duplex systems are associated with interference cancelation mechanisms [29, 36]. While attending to these issues, the future receivers would also have to incorporate services for D2D communication which will be assigned in the cellular networks. Therefore, a higher sensitivity requirement is expected and this can be achieved effectively by the narrow-band systems. Hence, future systems would require both wide band and as well as narrow band front ends to address the varying sensitivity demands.

2.3 LNA topologies

The first active component a signal reaches in the RF front end is the low noise amplifier. LNAs are required to amplify the received weak signal and to build highly sensitive receivers. Unlike general purpose amplifiers, there are two essential factors that need to be taken care of while realizing LNAs. The foremost is that it must provide an acceptable input impedance match to the path from the antenna and in general it must be matched to 50 Ω. Secondly, it must process the incoming weak signal only by adding as minimum a noise as possible an attribute commonly quantified as noise factor. The noise factor of a system can be given as

$$NF = \frac{SNR_{in}}{SNR_{out}} \tag{2.1}$$

where SNR_{in} and SNR_{out} are the Signal-to-Noise ratios at the input and output of the system respectively. The noise factor is termed as noise figure when (2.1) is used in the logarithmic scale as 10log(NF). In this thesis, the abbreviation "NF" is interchangeably used for both noise factor and noise figure.

Because of these two requirements, not any amplifier can be used as an LNA. There are several circuits based on the few basic topologies as shown in Fig. 2.5. The overall resulting performance and the necessary components to build an LNA depend on the incorporation of these basic topologies. Fig. 2.5 lists the basic topologies and their respective performance matrices are given in Table 2.1.

The Fig. 2.5(a) shows a simple technique of LNA realized with resistive termination. The input

impedance, Z_{in}, can be matched to R_{50} by equating the parallel resistance, R_p, to 50 Ω. The resulting noise factor of this circuit includes noise from the resistance R_P and from the transconductance (G_m) stage. The noise of the G_m stage can be minimized by increasing the total G_m of the amplifier. However, noise from R_p cannot be minimized by increasing the resistance value because it must be fixed to 50 Ω for an input match. Therefore, this type of structure leads to a minimum NF of 3 dB even after neglecting noise from the G_m stage. This can be observed from the first term of the noise factor equation, R_{50}/R_p, given in Table 2.1 where this term alone yields a value of unity.

An LNA with a resistive feedback technique is shown in Fig. 2.5(b). A resistor, R_F, is used in a shunt-shunt feedback technique through which the input impedance is lowered to a value of 50 Ω. In this type of configuration, any arbitrary value for G_m cannot be chosen because of its dependency on the input impedance. As a consequence, power is primarily decided by the input impedance requirement.

Further, as in the topology in Fig. 2.5(a), the NF yields a minimum value of 3 dB but not due to the limitation from R_F, instead the limitation comes from the excess noise coefficient γ. For long channel devices, γ is around 2/3, however, it increases to a value nearer to 2 for short channel MOSFETs. The noise effect from R_F can be minimized by increasing the R_F value but the effect of the G_m stage cannot be lowered.

In either of the first two topologies in Fig. 2.5, a resistor is required in the configuration to lower the input impedance to 50 Ω. Alternatively, one can make use of the lower input impedance of a common-gate (CG) amplifier that is as shown in Fig. 2.5(c). As in Fig. 2.5(b), the G_m of the device in CG stage too is used to match to R_{50} Ω. However, the Z_{in} differs from the value of $1/g_m$ due to channel length modulation in the advanced technological nodes and the actual value is given as [12]

$$Z_{in} = \frac{R_L + r_o}{1 + g_m r_o} \approx \frac{1}{g_m}\left(1 + \frac{R_L}{r_o}\right) \tag{2.2}$$

where r_o is the drain-source resistance describes the channel length modulation of the MOS. Due to the appearance of r_o, the value of g_m has to be further increased which in turn burn more power. A cascode MOS can be attached to the core transistor to reduce the influence of R_L on Z_{in} [12]. The corresponding NF equation in Table 2.1 suggests that this configuration also yields a minimum value of 3 dB. The advantage of the first three topologies is that these can be used for a broadband input match.

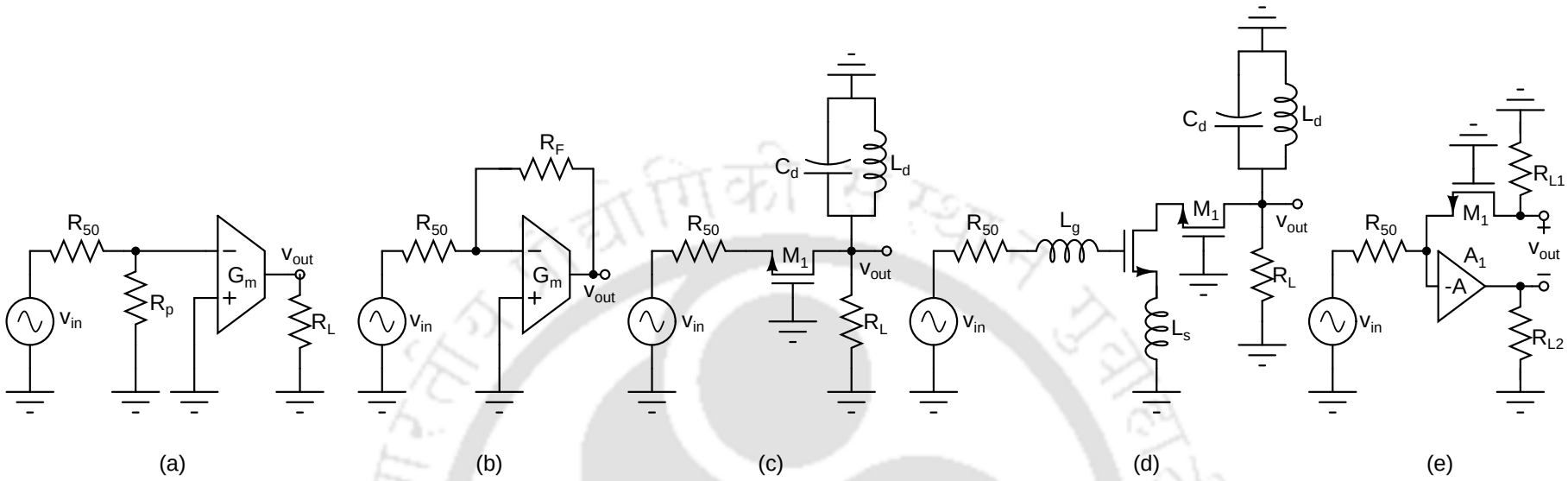

Figure 2.5: Various basic LNA topologies: (a) An LNA with resistive termination; (b) An LNA with shunt resistive feedback; (c)An LNA with CG configuration; (d) A CS LNA with an inductive degeneration; (e) A noise canceling LNA.

Table 2.1: Comparison of parameter matrices of different basic LNA topologies

LNA Topology	Resistive termination	Resistive feedback	CG	CS degenerative	Noise cancelling
Voltage gain (A_v)	$\frac{G_m R_L}{R_p}(R_p \| R_{50})$	$\frac{1}{2}(1-G_m R_F)$ $\approx -\frac{R_F}{2R_{50}}$	$\frac{g_{m1}R_L}{1+g_{m1}R_{50}}$	$Q_{in} g_m R_L$ *	$\frac{R_{L1}}{R_{50}}$ +
Input impedance ($\|Z_{in}\|$)	$R_p = R_{50}$	$1/G_m = R_{50}$	$1/g_m = R_{50}$	$\omega_t L_s = R_{50}$ *	$1/g_m = R_{50}$
Noise Factor ($NF-1$)	$\frac{R_{50}}{R_p} + \frac{\gamma R_{50}}{G_m (R_p \| R_{50})^2}$	$\frac{4R_{50}}{R_F}+$ $\gamma G_m R_{50}\left(\frac{R_{50}+R_F}{R_F}\right)^2$ $\approx \frac{4R_{50}}{R_F}+\gamma$ **	$\frac{4R_{50}}{R_L}+\frac{\gamma}{g_m R_{50}}$ $=\frac{4R_{50}}{R_L}+\gamma$	$\gamma g_{m1} R_{50}\left(\frac{\omega_o}{\omega_t}\right)^2$	$\frac{R_{50}}{R_{L1}} + \frac{R_{50}R_{L2}}{R_{L1}^2} + \frac{\gamma R_{L2}}{R_{L1}}$

* $Q_{in} = (2\omega_o C_{gs} R_{50})^{-1}$; $\omega_t = g_m C_{gs}^{-1}$; ** For $R_{50} \ll R_F$; + Factor is based on the condition, $R_{L1} = A R_{L2} R_{50}$, required for an exact noise cancelation.

Unlike the first three cases, the real input impedance can be created virtually with the usage of inductance as source degeneration in the CS (Common-Source) amplifier. The resulting CS degenerated LNA is shown in Fig. 2.5(d). Though it provides a narrowband match, nevertheless, it yields the best NF in comparison to all the cases. Further, the g_m here is ruled by the gain of the amplifier rather than the input impedance requirement of the LNA. Therefore, the power consumption of this topology can be made less compared to other configurations such as Fig. 2.5(b), (c) and (e).

These basic configurations can be used to build sophisticated amplifiers. The wideband advantage and the best noise performance of the CS configuration can be simultaneously achieved by incorporating noise cancelling mechanism to a CG or a resistive feedback configuration [37, 38]. In this mechanism, the incoming signal and the device noises are processed differently and finally the noise of the core device gets cancelled at the output. A noise cancellation technique based on [38] is shown in Fig. 2.5(e) where the intended amplifier, A_1 can be realized by a simple CS stage. The impedance match is provided by the g_m of M_1 and its corresponding noise is cancelled with the usage of an additional amplifier A_1. Again as g_m of M_1 is decided by the input impedance requirement, the power consumption of an LNA with a noise cancelling technique is higher compared to CS degenerative configuration. Therefore in this thesis, a CS degenerative configuration is selected for realizing sub-mW powered LNAs.

To get insight into the power trend, several receiver front end implementations that include LNAs in recent years [39–63]are considered and depicted in Fig 2.6. These implementations are diverse in nature; however, only those low power implementations that consume near micro watt or at most a few tens of mW are considered year wise starting from 2012. Not all the implementations have explicitly stated the performance of the LNA concerned; in such cases, the documented figures of the RF front end are considered merely to outline a draft trend. The power consumption and the noise figure of LNAs[1] for each case are considered and the average value among them in that respective year is computed. This is shown in Fig 2.6. The dashed red line highlights the value of the averaged power consumption in that corresponding year.

It is seen that LNAs in some cases consumed upto $30-40\%$ [42, 53] of the total power of the RF front end; in other cases the consumption has gone well above 70% [51, 54, 57, 61]. Applications targeted for short range communication such as Zigbee, BLE (Bluetooth Low Energy) and other WPAN

[1]The power consumption of the LNA is considered if such figures are reported for the concerned LNA; otherwise, power consumption of the RF front end itself is considered in the plot.

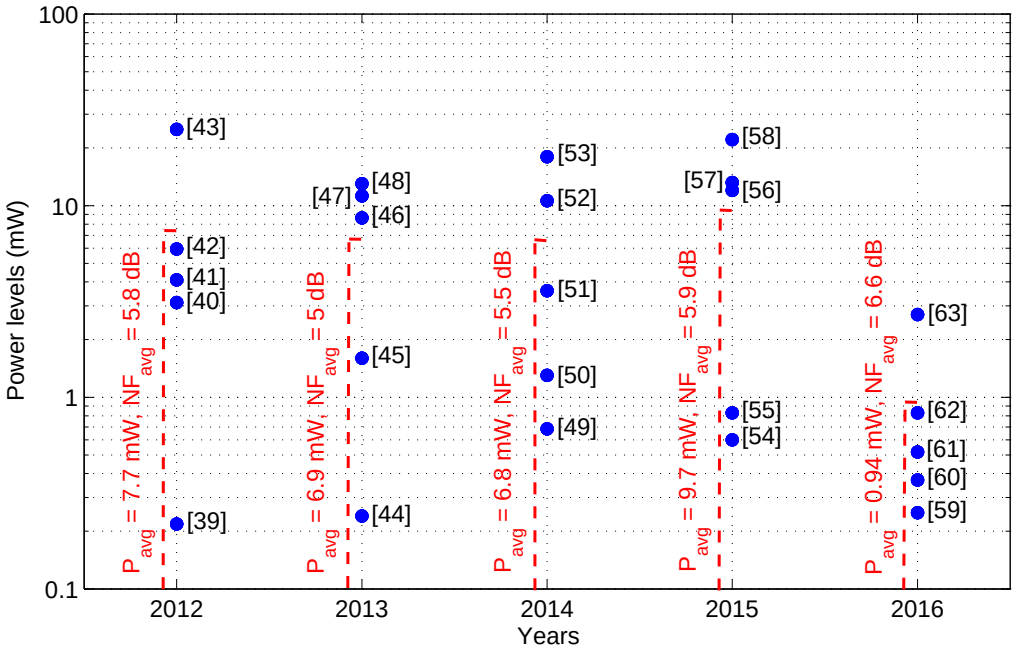

Figure 2.6: A power trend among implementation of low noise amplifiers.

(Wireless Personal Area Network) systems [39, 44, 49, 54, 55, 59–62] have successfully incorporated and implemented sub-mW LNAs. Among these, the majority of the implementations have used wide-band amplifiers. As a consequence, this has resulted in noise figures exceeding 4 dB. Systems for communications in medical applications [50, 60] too have tried to incorporate microwatt-power LNAs in order to extend the battery life. On the other hand, applications targeted for mobile communications and general radios like SDRs (Software Defined Radios) consume relatively more power due to the incorporation of additional features such as blocker filtering [43, 56] and harmonic rejection techniques [46, 58] with broadband capability. In addition, aspects of linearity improvement [47, 48, 53] are considered. The current-reuse techniques are becoming popular [39, 41, 50, 52, 55, 62]. Further implementations have tried to bring together complex blocks such as LNA, Mixers and VCOs [54, 63] to use the same bias current to achieve the power reduction of the overall system. As the years have progressed as shown in Fig. 2.6, the average power in each year is decreasing with the year 2015 being an exception. This is because the selected implementations in the year 2015 have embedded features such as blocker-tolerant and harmonic-rejection techniques that have consumed extra power. The average noise figure is almost uniform. However, the NF value is seen to increase slightly in 2016. This may be because most of the designs concentrated on the micro-watt power implementations. Low power techniques along with current-reuse mechanisms may be combined in future. This is expected to further bring

down the power and noise figure levels in the coming years.

2.4 Power optimization of LNA for LTE receiver

In general, most LNA designs are targeted only towards achieving a low noise performance, and the power consumption factor comes afterwards. As a result, more power is expended per amplifier to improve its noise performance which is more than what is necessarily be required. On the other hand, an arbitrary power selection to reduce the power consumption would lead to performance degradation and the final outcome may not satisfy the requirement of the receiver. Therefore, power level assignments to LNAs must be carried out by evaluating performance requirements from the LTE specifications.

2.4.1 Performance assessment of LTE receiver

The LTE standard consists of several operating bands defined throughout the world ranging from band 1 to band 40 [64]. For analysis, only band 1 is considered here; evaluation methods nevertheless holds good for other bands as well. The receiver sensitivity requirement at the antenna port associated with various bandwidths is given in Table 2.2. The band 1 is having a minimum channel bandwidth of 5 MHz and can reach up to 20 MHz. The sensitivity requirements are given for QPSK modulation schemes with a target coding rate of (1/3). These requirements are set with an expected signal-to-noise ratio (SNR) of -1 dB and an overall noise figure (NF) of 9 dB with a 2 dB implementation margin [65]. However, noise figure requirements must be altered to take several other receiver impairments.

Among several receiver architectures, direct conversion receivers (DCR) are widely used because the whole system can be easily implemented on-chip. As a result it reduces bill of materials (BOM) and hence the intended system can be made more compact. However, it is naturally associated with certain shortcomings such as problems of DC offsets, LO leakage, flicker noise etc [12]. Fig. 2.7 highlights the front end of the DCR. The topology is shown for FDD duplex mode where both the

Table 2.2: Sensitivity requirements of the LTE receiver

Band 1	UL[*]: 1920-1980 MHz; DL[*]: 2110-2170 MHz				
	BW^*(MHz)	5	10	15	20
	$P_{sens}{}^*$ (dBm)	-100	-97	-95.2	-94

[*] UL: Uplink; DL:Downlink; BW: Channel bandwidth; P_{sens}: Sensitivity

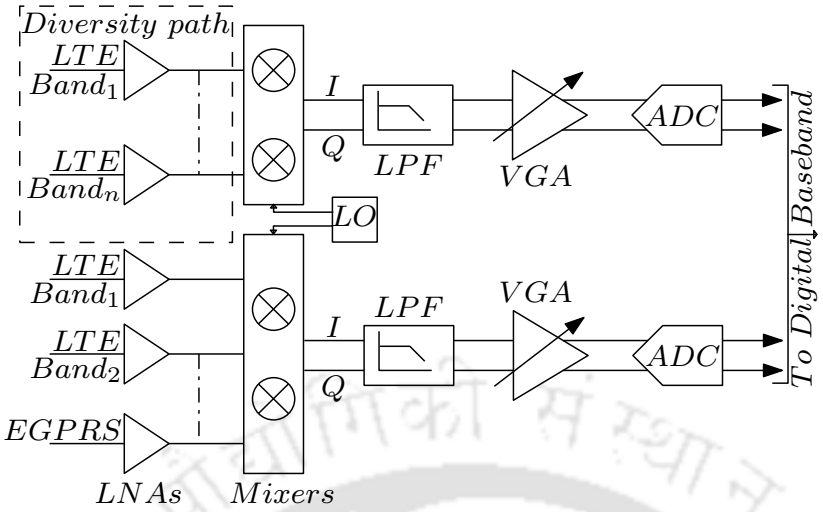

Figure 2.7: Typical front-end of the multi-band receiver using the direct conversion architecture.

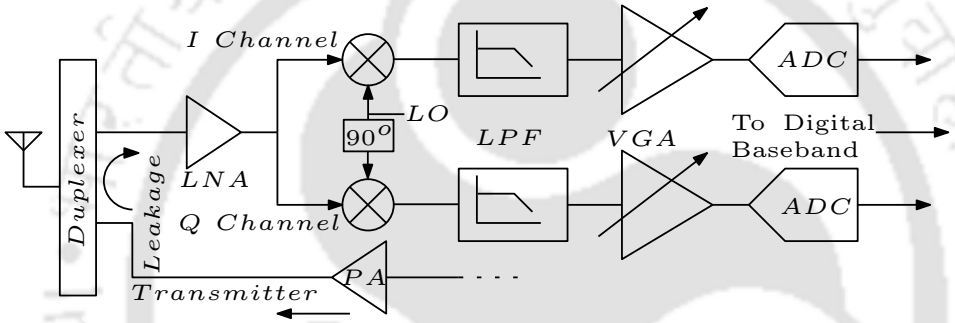

Figure 2.8: Transceiver depicting the leakage path from transmitter to receiver.

transmitter and the receiver operate concurrently but in different bands of frequency. The duplexer isolates the receiver from the transmitter, however, there is always a leakage path that exists from the transmitter to the receiver as shown in Fig. 2.8. The two paths, I-channel and Q-channel are used for handling asymmetrically modulated signal [12] there by to reduce signal corruption after down-conversion. Nevertheless, the IQ mismatch results in residue signals in the band of interest and they corrupt the wanted signal. These impairments constrain the dynamic range of the receiver by affecting through either noise or linearity performances.

For receiver budgeting, the noise and the linearity are the main performance matrices which are taken into account. Among these, only the noise parameter is considered here for power trade-off as there are well established linearity enhancement techniques which can achieve good linearity for any kind of power levels. Linearity is considered here only to estimate the noise contribution from intermodulation residues.

2.4.2 Linearity estimation

The linearity performance primarily depends on the largest value of the maximum input level allowable at the antenna input port, transmitter leakage to the receiver and other undesired signals present such as adjacent channels, in-band and out of band blockers. In addition, separately defined intermodulation criteria sets the rule for linearity. For linearity estimation, practically occurring losses such as front end loss (FE_{loss}) [66] is also taken into consideration. The equations and relevant assumptions required for analysis are considered from [66].

Maximum input level

For band 1, maximum input (P_{inmax}) at the antenna port is restricted to -25 dBm. By including a FE_{loss} of 3.8 dB to the maximum input signal, signal at the input of the LNA can be calculated as

$$P_{LNAmax1} = P_{inmax} - FE_{loss} + PAR \tag{2.3}$$

where PAR is the peak-to-average ratio that quantifies the amplitude variation with respect to its mean value for a pulse shaped modulated signal. LTE uses OFDM signals for downlink which exhibit a PAR value of 2lnN [12], with N being the number of sub-channels. For a bandwidth of 20 MHz with 200 sub-channels in it, PAR is around 10.6 dB. The resulting $P_{LNAmax1}$ is -18.2 dBm. Assuming this level as a 1-dB compression point, the required IIP3 for the receiver is around -8 dBm as the latter is near about 10 dB greater than the former one theoretically.

Transmitter leakage to receiver

For calculating the power of the leakage signal from the transmitter, duplexer profile from [66] is considered. LTE defines a power class 3 with a maximum output power (P_{max}) of 23 dBm being considered as the output of the power amplifier. The leakage signal at the LNA from the transmitter with a duplexer isolation (Dup_{ISO}) of 44 dB is thus given as

$$P_{LNAmax2} = P_{max} - FE_{loss} + Dup_{ISO} = +23 - 3.8 - 44 = -24.8\ dBm \tag{2.4}$$

The 1-dB compression point has to be greater than -24.8 dBm where linearity due to transmitter leakage case is a little relaxed compared to the earlier case. The resulted value -24.8 dBm is thus considered as a transmitter leakage in the following analyses.

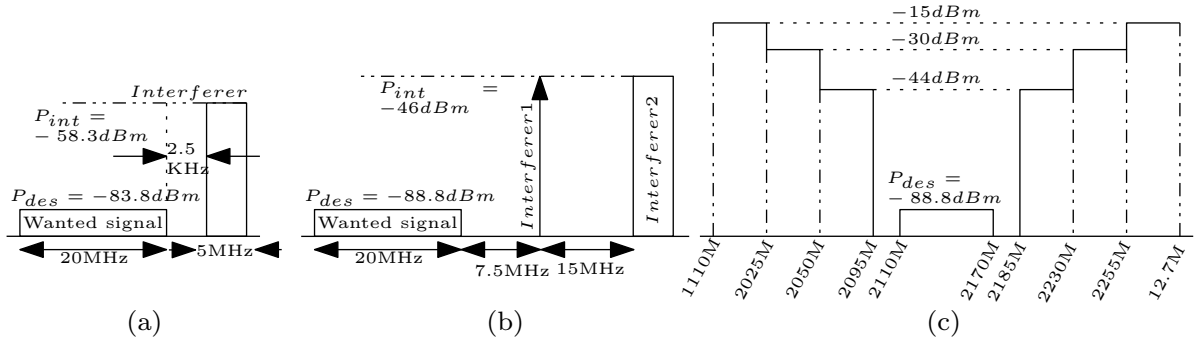

Figure 2.9: The band profile for testing of (a) adjacent channel selectivity (ACS) of case 1, (b) intermodulation, (c) Out of band blockers (OOB). Desired signal levels are kept 14 dB for case (a) and 9 dB each for case (b) and (c) above the minimum sensitivity level. Interference level is kept 39.5 dB above the minimum sensitivity level for case (a), it is fixed to -46 dBm for case (b), and (c) has got a varying profile with frequency as shown for 20 MHz channel bandwidth.

Adjacent channels and intermodulation

The band profile for adjacent channel test case 1 is shown in Fig. 2.9(a). The desired signal (P_{des}) is 14 dB higher than the minimum sensitivity level [64]. The lower edge of the adjacent channel (P_{int}) is at 2.5 KHz offset from the higher edge of the 20 MHz channel, where the P_{int} is having a bandwidth of 5 MHz. Considering the adjacent leakage in the desired spectrum to be 16 dB below the wanted signal [66], the IIP3 requirement can be estimated from [66, 67] as

$$IIP3 = \frac{1}{2}(-20.75 + 2P_{int} + 1.6PAR - P_{ACLR}) \tag{2.5}$$

(2.5) yields an IIP3 requirement of -10.3 dBm. The assumption for IIP3 is considered for calculating IIP2 value and that can be estimated as [66]

$$IIP2 = -P_{IIM2} + 2P_{int} - 3.87 = -20.67\ dBm \tag{2.6}$$

The requirement for intermodulation test are as shown in Fig. 2.9(b). The desired signal is 9 dB above the minimum sensitivity level for 20 MHz bandwidth signal. There are two interferers, one is the continuous wave (CW) situated at 7.5 MHz offset from the edge of the desired signal. The other interferer is a 5 MHz E-UTRA modulated signal situated 22.5 MHz away from the edge of the desired signal. With the assumption of residues 16 dB below the desired signal, IIP3 requirement due to intermodulation can be given as

$$IIP3 = 1.5P_{int} - 0.5P_{IIM3} = -16.6\ dBm. \tag{2.7}$$

Out of band (OOB) blockers

Compared to the above cases, OOB interferers put a stringent requirement on linearity performance of the receiver. The OOB profile is described in Fig. 2.9(c). The power level of the interferer can go as high as -15 dBm for a 85 MHz offset from the desired band. There are several combinations of frequencies for which interferer might fall in the desired band [66]. Out of several possibilities, one case is dominant for IIP3 requirement. This is due to the presence of blocker at $F_{rx} - 2\Delta f$, with F_{rx} as the receiver frequency and Δf as the separation between transmitter and receiver frequency. The IIP3 estimation due to the interferer at $F_{rx} - 2\Delta f$ is given as [66]

$$IIP3 = 0.5(P_{int} + 2P_{tx} - P_{IM3}) \tag{2.8}$$

where P_{int} is the interferer power level, P_{tx} is the transmitter leakage level at the receiver as given in (2.4), and P_{IM3} is the product of intermodulation due to interferer and the transmitter leakage. With an assumption that interference undergoes an attenuation of 38 dB yields a P_{int} of -53 dBm. The transmitter power is set 4 dB below the maximum allowable power [64] and by considering a 44 dB duplexer isolation and the front end losses, IIP3 in (2.8) yields a requirement of +1.1 dBm.

The second order intermodulation requirement results due to mixing of transmitter frequency (F_{tx}) with a blocker present at the frequency ($F_{rx} - F_{tx}$). It can be given as

$$IIP2 = P_{int} + P_{tx} - P_{IM2} \tag{2.9}$$

With a duplexer attenuation of 30 dB for the blocker [66], the P_{int} results in -45 dBm. With a transmitter leakage of -24.8 dBm and an IM power level of -104.8 dBm, the IIP2 requires a value of +35 dBm. From these analyses, it is observded that linearity requirements are mainly dictated by out of band blockers. These can be relaxed with the usage of BPF, however the noise performance has to be compromised [12].

2.4.3 Noise performance of receiver

The requirement of receiver given in Table 2.2 assumes that a receiver noise figure of 9 dB [65] would satisfy the minimum sensitivity performance. In general, only the prime contributors such as thermal noise and noise from other internal components are taken into account for estimating the overall noise figure. However, in reality, other receiver impairments also contribute to signal corruption which is

needed to be taken into account as well. These impairments include (a) leakage of power amplifier (PA) phase noise into receiver, (b) integrated phase noise (IPN) from frequency synthesizers, (c) image residues due to I/Q mismatch, (d) interferences due to second and third order intermodulation, and (e) ADC noise. As these affect the sensitivity of the receiver, noise figure has to be re-evaluated by considering all the imperfections in the receiver . In-order to quantify the overall noise effect, certain assumptions are made based on practically achievable conditions.

PA phase noise

From [66], phase noise profile shows a value of -140 dBm/Hz. With a duplexer isolation of 44 dB from transmitter to receiver, phase noise at the input of the front end can be given as

$$P_{PAnoise} = -140 + 10log(BW) - FE_{loss} - Dup_{ISO} = -114.7\ dBm \tag{2.10}$$

IPN

From a phase noise skirts of -101 dBc/Hz [12], IPN can be estimated to be -41 dBc for 1MHz offset. Hence, its noise power level comes to be -138.8 dBm.

IQ mismatch

If the receiver is mismatch calibrated, SIR (Signal-to-Interference ratio) can be maintained as high as 50 dB [68]. It results in a noise power level of -147.8 with the desired signal being at the minimum sensitivity level.

Intermodulation

The linearity analysis in the previous sub-section showed that IIP2 and IIP3 for an LTE receiver have to be greater than +35 dBm and +1.1 dBm respectively. Assuming that the receiver satisfies these requirements for second and third order linearity, power levels of the intermodulation (IM) products at the receiver input can be given as

$$P_{IIM2} = 2P_{int} - IIP2 - 3 = -128\ dBm \tag{2.11}$$

$$P_{IIM3} = 3P_{int} - 2IIP3 - 3 = -143\ dBm \tag{2.12}$$

The power level of interferer (P_{int}) is set to -46 dBm as given in intermodulation conditions for IM3. On the other hand, IM2 is set to -45 dBm from the OOB requirement. As there are two inter-modulated

signals, only 50% of the power is contributed by single IM component. Hence, the obtained value is corrected by adding -3 dB to the (2.11) and (2.12).

ADC noise

For a 1 V peak to peak amplitude and with a dynamic range (DR) of 60 dB, the available noise at the ADC input is -56 dBm. If the front-end gain of the receiver is 60 dB then the ADC noise reflected at the receiver input is -116 dBm.

Total Noise

With the consideration of all these above noise sources starting from PA phase noise to ADC noise and in addition assuming receivers' internal components exhibiting a noise with its value being equal to the minimum sensitivity of the receiver, the total noise at the receiver input can be calculated as

$$Noise_{total} = 10log\Big\{10^{-\frac{114}{10}} + 10^{-\frac{138}{10}} + 10^{-\frac{147}{10}} + 10^{-\frac{123}{10}} + 10^{-\frac{137}{10}} + 10^{-\frac{116}{10}} + 10^{-\frac{98}{10}}\Big\} = -97.8dBm \quad (2.13)$$

The total noise obtained is almost equal to the minimum sensitivity requirements. Hence, the earlier noise figure assumption of 9 dB can be considered to be an upper limit for designing LTE receiver front ends.

2.4.4 Noise-power trade-off of LNA

Reduction of the power consumption can be achieved by scaling down the supply voltage and by decreasing the biasing current that flows through it. The supply scaling is feasible if devices are biased in weak or moderate inversion region as devices require less voltage headroom across them. Further, this is an implementable solution only for advanced technological nodes because they offer ample amount of transition frequency in weak and moderate inversion regions. On the other hand, reduction in biasing current of the device has relatively strong proportional effect on gain and noise figure of the LNA. Hence the criteria for minimum biasing current can only be decided by the upper extremity of receiver's noise performance.

For deciding LNA power level analytically, noise figure of the LNA has to be correlated with the overall noise performance of the direct conversion receiver (DCR). The DCR front-end consisting of LNA, mixer, low pass filter (LPF) and variable gain amplifier (VGA) primarily decides the noise and

Table 2.3: Typical parameter values for different receiver components

Parameters	Mixer	LPF*	VGA*
NF (dB)	14	0.5	5
Gain or attenuation (dB)	15◇	0.5	30
IIP3	+15	+30	-20

* LPF: Low pass filter; VGA: Variable gain amplifier;
◇ Conversion gain

the linearity performance of the receiver. As linearity can always be improved for any power level using the distortion cancelation techniques, only the noise performance is considered here for selection of power levels.

Further, to quantify the resulting overall performance, a cascode LNA circuit is considered here with the assumptions of performances matrices for other components of the receiver given in Table 2.3. The Mixer and the VGA are assumed to have a conversion gain of 15 dB and a normal gain of 30 dB respectively and the LPF is assumed to have an attenuation of 0.5 dB. These values are shown to be practically achievable in the current state of the art. For the CS degenerated LNA, noise figure which is related to transconductance, total capacitances and resistances [69], is given as

$$NF = \frac{R}{R_s}\left(1 + \frac{\omega_0^2\gamma}{\alpha}\frac{C_{tot}^2}{g_m}R\chi\right) \tag{2.14}$$

where $\chi = \left(1-2C\frac{C_{gs1}}{C_{tot}}\sqrt{\frac{\delta\alpha^2}{5\gamma}}+\frac{C_{gs1}^2}{C_t^2}\frac{\delta\alpha^2}{5\gamma}(1+Q_{in}^2)\right)$ with the input network quality factor, $Q_{in} = \frac{1}{\omega_0 C_{tot} R}$, $R = R_s + R_g$, and $C_{tot} = C_{gs1} + C_{ext}$. Other parameter details can be seen in [69].

For cascaded systems like front-end of the DCR, the total noise figure can be given as

$$NF_{total} = NF_{LNA} + \frac{(NF_{Mixer} - 1)}{Ap_1} + \frac{(NF_{LPF} - 1)}{Ap_1 Ap_2} + \frac{(NF_{VGA} - 1)}{Ap_1 Ap_2 Ap_3} \tag{2.15}$$

where NF is the noise figure with subscripts referring to particular components. Ap_1 and Ap_2 are the available power gain for LNA and Mixer respectively. Ap_3 is the attenuation loss of the LPF.

The noise figure outcome for varying power levels of LNA can be calculated by (2.14). The obtained noise figure from (2.14) when used in (2.15), gives the overall noise figure of the receiver. The noise figure of LNA and the receiver for varying power from $35\mu W$ to 3.5 mW is given in Fig. 2.10. The response is plotted by assuming a supply voltage of 0.7 V. The analytical results obtained underestimate the noise contribution because noise contribution from the core device alone is considered.

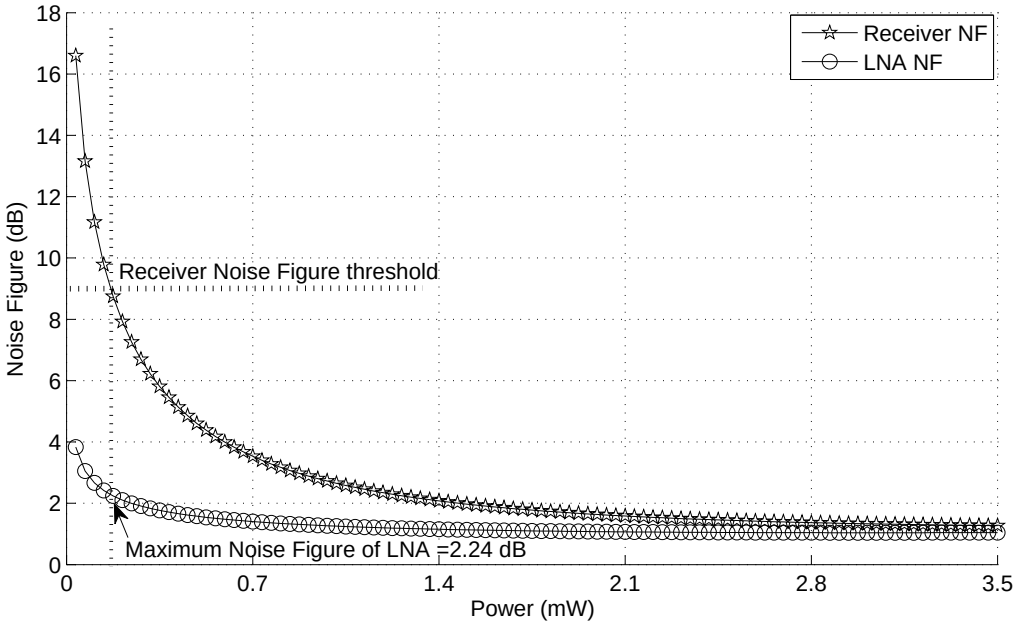

Figure 2.10: The analytical response of noise figure of LNA and the receiver with respect to LNA power levels. The supply voltage is assumed to be 0.7 V.

There are also noises from other elements that would further scale up the noise figure.

It is observed in Fig. 2.10 that noise figure increases drastically as one moves from 3.5 mW to $35\mu W$ of power. It can be seen that the overall receiver noise figure drastically increases for a power level below 1.4 mW. It is because of two reasons. Firstly, the reduction in noise figure of LNA itself contributes to degradation in the complete receiver. Secondly, LNA gain decreases with the reduction in its power. As a consequence of the latter case, mixer noise become dominant in overall receiver as it gets barely masked by LNA gain in low power conditions. However, noise figure of LNA can be compromised till 2.24 dB while still satisfying the overall receiver noise performance. Overall, it shows the feasibility of achieving a micro-watt range of power level per amplifier for the LTE receiver.

2.5 Conclusion

In this chapter, a brief introduction is given about available RF front ends and about basic LNA topologies. It is evident from the overall discussion that the performance of the receiver depends on the type of architecture. Currently, the zero-IF architecture is the widely used architecture, however, in future it may be replaced by the superheterodyne architecture because of the possibility of implementing high-Q, on-chip filters. Contrary to the conventional single architecture based system, modern receivers may combine multiple architectures with an objective to cover diverse applications.

As regards LNAs, noise cancelling and current-reuse amplifiers with wideband operability are becoming popular. These are one of the major power consumers in the RF front ends and the trend shows that attention is being paid to reduce the power consumption of these amplifiers in recent years. The recent implementations are focusing towards achieving sub-mW powered levels for LNAs. In future, few of the applications like D2D would still need narrow band LNAs because of the requirement of highly sensitive and low power receivers.

As discussed, the power consumption of individual amplifier is critical. Therefore, an LNA power is optimized based on the sensitivity requirement of the LTE receiver. The power level assignment is carried out with a near accurate estimation of the performance of the receiver. A noise figure limit for an LNA is deduced depending on the overall performance requirement of the LTE receiver.

3

Analysis of moderate inversion based sub-mW LNA

Contents

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3.1 Introduction

In the era of advanced wireless technology, the trend is towards developing energy efficient, smart technologies in-order to improve computational capability and connectivity. Consequently, RF receivers, ubiquitous in all wireless applications - from smartphones to health care units, are required to be operated with as low a power as possible in order to achieve long battery life. The requirement of low power imposes great design challenges involving compromises between several performance parameters.

LNAs, which are a key component of a receiver, however, suffer performance degradation when it is operated in low power conditions. In-order to meet the performance requirements, LNAs have to be designed carefully by exploring all possible design spaces. Fortunately, the advancement in CMOS technology and improvement in device transition frequency provide an opportunity to design sub-mW dissipation level low-noise amplifiers.

Conventionally, most LNAs are designed in strong inversion region in-order to keep the minimum noise figure low. However, design in this region invites critical challenges when these are, in particular, to be implemented in sub-nanometer technologies for micro-watt powered LNAs. The issues are as follows.

(i) When designed for low power, circuit demands a larger gate inductance, L_g, because of the presence of lower gate capacitances.

(ii) The necessary large gate inductance along with the value of gate capacitance lowers the requirement of source inductor, L_s, to parasitic inductance ranges.

(iii) It necessitates the increase of the gate capacitance to put L_g and L_s in a reasonable range. However, the power requirement is simultaneously increased which is in contrary to the requirement.

Hence, LNAs in strong inversion region requires large power and further, topologies like cascode require large voltage headroom which in turn requires a higher supply voltage. Therefore to achieve low power consumption with reasonable performance, sub-nanometer devices should be biased in lower inversion regions such as weak or moderate inversion regions. Further, it may provide a fully on-chip implementable solution as passive elements fall into reasonable values.

As per the definitions in [70], operating regions are categorized according to terminal gate-source voltage (or by effective gate overdrive voltage, $V_{eff} = V_{gs} - V_{th}$) as illustrated in Fig. 3.1, where WI,

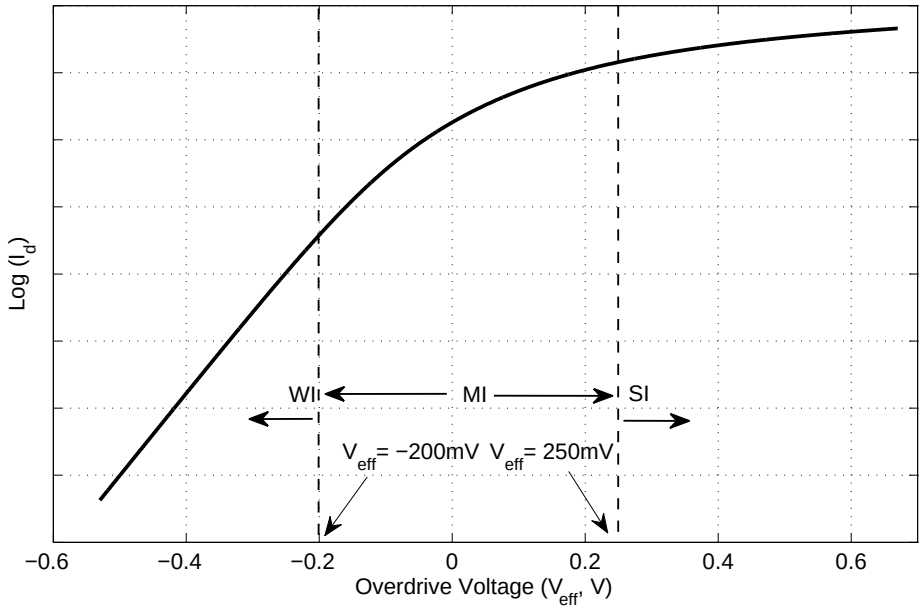


Figure 3.1: Logarithmic of I_d versus overdrive voltage (V_{eff}).

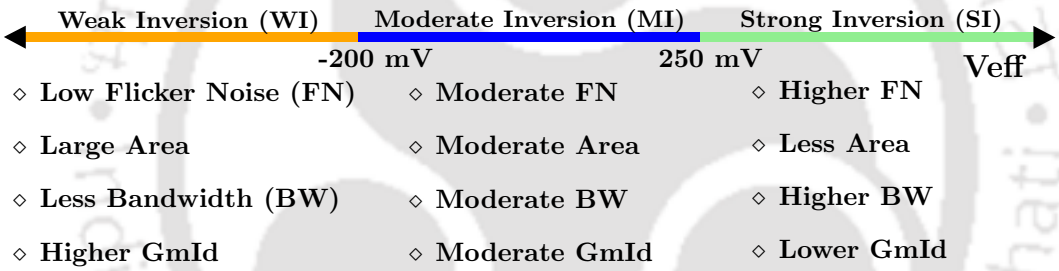


Figure 3.2: Performance summary of different region of inversions.

MI and SI respectively are the weak, the moderate and the strong inversion regions. The value of V_{th} is found to be 0.53 V. As expected, the logarithm of currents in the weak and the strong inversion regions hold a linear relationship with respect to the gate-source voltage. For a chosen technology and device, moderate inversion spans over a range from -200 mV to +250 mV.

Devices operating in each of these three regions result in different performance. Based on the discussions [71], these are summarized in Fig. 3.2. The bandwidth defined here is the intrinsic bandwidth, the highest frequency at which current gain (drain to gate) reaches unity. As regards noise, the MOS device also suffers from flicker noise (FN) in addition to thermal noise, whose spectral density varies inversely and hence it is also called as (1/f) noise. Another important parameter, g_m/I_d, is the trans-conductance efficiency that describes how effectively g_m is generated for a given value of current. For a given current, the gain and the required area are higher in weak inversion region compared

to strong inversion whereas one can achieve higher bandwidth in strong inversion region. As flicker noise is inversely proportional to area, one can expect lower value in weak inversion region for a given current.

Regarding thermal noise, both noise current and voltage show dependency on device transconductance - in which the thermal noise voltage is inversely proportional to g_m, whereas the noise current is directly proportional to g_m. Consequently, the resulting thermal noise voltage is higher in strong inversion region whereas the thermal noise current is higher in weak inversion region. On the contrary, moderate inversion region provides trade-off in the performances that are achievable in the other two regions. Thus, moderate inversion region would result in a reasonable gain, noise performance and area requirement.

Coming to the performance estimation of the LNA, the simplest form of analytical models can be readily used for SI based designs. However, performance analysis in other inversion regions is not simple - the analysis results in complex formulations and further it becomes inaccurate when sub-nanometer technologies are targeted. Designs, in general, are based on three types of models such as analytical, empirical and semi-empirical models [72]. Out of these, the semi-empirical model approach is the compromise between the other two and it is the most efficient in-terms of both design time and accuracy. In-order to carry out semi-empirical based designs, an extraction methodology has to be developed.

In this chapter, a conventional cascode LNA is analyzed and designed where all the devices are biased in the moderate inversion region. The design is carried out using the proposed semi-empirical based noise model and the implemented LNA is operated at a voltage of 0.7 V. In order to estimate the values of parameters, an extraction methodology is developed. Further, the existing analytical noise model of LNA is modified to support the parameter extraction based designs. It is observed that the modified noise factor model can be applied to different region of inversions for the noise estimation.

3.2 Analytical unified noise factor of LNA

Consider the cascode LNA shown in Fig. 3.3(a). M_0 is the core transistor while M_1 provides isolation between the input and the output. Further M_1 improves output impedance. L_g along with L_s provide the input impedance match at a particular frequency of interest. An extra capacitor, C_{gse}, is added in parallel with C_{gs} of M_0 for avoiding unnecessary widening of MOS width [73] and thereby

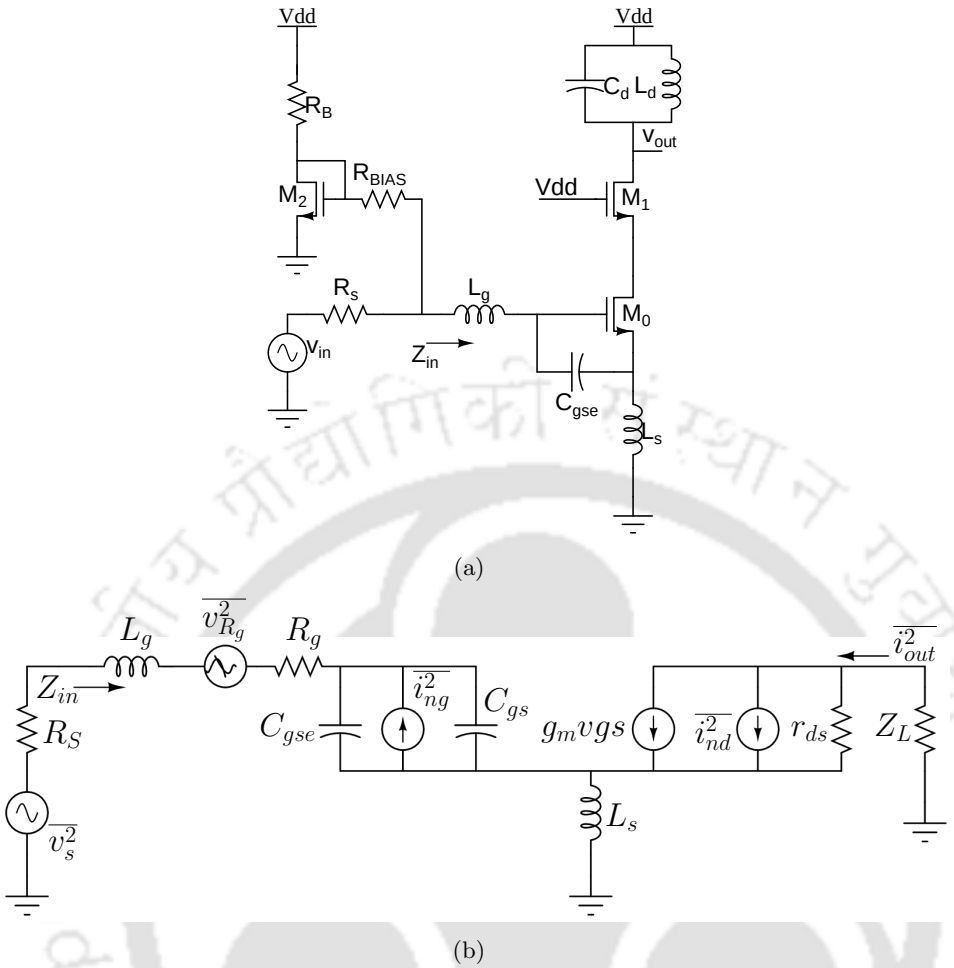


Figure 3.3: (a) Circuit diagram of the cascode LNA. (b) Small signal equivalent model with all noise sources and parasitic resistances from gate inductor, and MOS sheet resistance are taken into account.

saving the power consumption. M_2 along with R_B and R_{BIAS} provide biasing for the core transistor. Z_L is the impedance seen at the source terminal of M_1. The small signal equivalent of the cascode LNA [69] is shown in Fig. 3.3(b).

3.2.1 Unified noise figure model

There are a few widely accepted noise optimization techniques which take both drain and gate noises into account. Shaeffer and Lee [74] have formulated device width optimization technique for low-power LNA by taking induced gate noise into account. Nguyen et.al [73] have summarized different noise optimization techniques and introduced PCSNIM (Power Constrained Simultaneous Noise and Impedance Matching) technique which helps in achieving low power LNA. Belostotski et.al [69] improved Nguyn's work by taking into account the effects of gate inductors' parasitic resistance and

showed that the gate inductor which has lower Q (quality factor) affects the noise performance. Fiorelli et.al [75] have improved the accuracy of estimation by including parasitic effects from source and drain inductors.

The power consumption of the amplifier needs to be optimized in-order to prolong the battery life. As power is one of the major factors and on-chip inductors have low Qs, the method proposed in [69] offers a suitable optimization technique. However, Belostotski's noise analysis in [69] is based on velocity saturation current equation models which do not give valid results in moderate inversion region. Hence to get valid results, parameter extraction based estimation is performed for noise analysis.

Following sub-sections discuss the development of a unified noise factor based on which the LNA design is carried out.

Input Impedance

To find the input impedance, a test voltage is applied at the input terminal of L_g and the resulting current is measured. By referring to Fig. 3.3(b) and applying KCL to different nodes, the relation between v_{test}/i_{test} i.e. Z_{in} may be expressed as

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{tot}} + R_g + \frac{\omega_t L_s \left[r_{ds} - \frac{s^2 L_s^2}{\omega_t L_s} \right]}{r_{ds} + Z_L + sL_s} \tag{3.1}$$

where $\omega_t = \frac{g_m}{C_{tot}}$ with $C_{tot} = C_{gs} + C_{gse}$, R_g is the gate resistance which includes both the parasitic resistance of the gate inductance and the gate sheet resistance of MOS M_0 [69]. If one assumes the operating and transition frequency relation as $\omega_t = 10\ \omega_0$, which is generally considered in designs, then $\left[r_{ds} - \frac{s^2 L_s^2}{\omega_t L_s} \right]$ in (3.1) would lead to $\left[r_{ds} + 0.01(\omega_t L_s) \right]$. As $0.01\ \omega_t L_s$, with $\omega_t L_s$ being nearly equal to R_s[1], is much smaller than r_{ds}, the (3.1) can be approximated by (3.2) which can be further approximated as (3.3). The details of this approximation is given in Appendix A.1.

$$Z_{in} \approx s(L_g + L_s) + \frac{1}{sC_{tot}} + R_g + \frac{\omega_t L_s r_{ds}}{r_{ds} + Z_L + sL_s} \tag{3.2}$$

$$Z_{in} \approx s(L_g + L_s) + \frac{1}{sC_{tot}} + R_g + \omega_t L_s r \tag{3.3}$$

In (3.3), 'r' is the impedance ratio given as $r = \frac{r_{ds}}{r_{ds}+Z_L}$, Z_L is the impedance seen towards the source of M_1. If we consider the general case where $Z_L = \frac{1}{g_{m1}}$, g_{m1} is the transconductance of the MOS

[1]Generally, R_s is having a value of 50 Ω

M_1, and with a worst case value of $g_{m1}r_{ds} = 5$, the value of 'r' comes to be around 0.8. For power matching, the real part of Z_{in} and $\omega_t L_s$ are given as

$$Re\{Z_{in}\} = R_g + \omega_t L_s r = R_s = 50\ \Omega \tag{3.4}$$

$$\Rightarrow \omega_t L_s = 1.2(R_s - R_g) = 1.2\ R_n \tag{3.5}$$

where r = 0.8 and $R_n = (R_s - R_g)$.

Noise factor (NF)

The effects of the resistance of the inductance and the gate are also included in the analysis as these are among the main contributors of noise in LNA. The total gate inductor, L_g, at the gate of MOS M_0 constitutes bond-wire inductor, $L_{g,BW}$, and the necessary on-chip inductor $L_{g,ind}$ [69]. The gate resistance is shown in the Fig. 3.3(b) and can be expressed as [69]

$$R_g = R_{g,ind} + R_{g,BW} + R_{g,MOS} \tag{3.6}$$

where $R_{g,ind}$, $R_{g,BW}$ and $R_{g,MOS}$ are the respective resistances of the gate inductor, the bond wire, and the MOS gate. The $R_{g,ind}$, and $R_{g,BW}$ can be related to their inductances $L_{g,BW}$ and $L_{g,ind}$ through their respective quality factors called Q_{ind} and Q_{BW}. The impedance due to the inductance at the gate, L_g, can be given as

$$\omega_0 L_g = \omega_0 \left(L_{g,ind} + L_{g,BW}\right) = R_{g,ind}Q_{ind} + R_{g,BW}Q_{BW} \tag{3.7}$$

By subtracting and adding $R_{g,MOS}Q_{ind}$ and $R_{g,BW}Q_{ind}$ to (3.7), the following (3.8) can be written in terms of R_g as follows.

$$\omega_0 L_g = R_g Q_{ind} + R_{g,BW}\left(Q_{BW} - Q_{ind}\right) - R_{g,MOS}Q_{ind} \tag{3.8}$$

To calculate the NF, relation between R_s and R_g is to be obtained. At resonance, $\omega_o L_g$ can be given as

$$\omega_o L_g = \frac{1}{\omega_o C_t} - \omega_o L_s = Q_s R - \omega_o L_s \tag{3.9}$$

where $R = R_s + R_g$ and $Q_s = \frac{1}{\omega_o C_t R} = \frac{\omega_o(L_s+L_g)}{R}$

Considering the above equations for $\omega_o L_g$ for power constrained design, relation between R_g and

R_s in terms of R and R_s can be written as

$$\frac{R}{R_s} = \frac{Q_{ind} - \frac{2\omega_o}{\omega_t r} + \frac{R_{g,BW}}{R_s}(Q_{ind} - Q_{BW}) + \frac{R_{g,MOS}}{R_s}Q_{ind}}{Q_{ind} - Q_s - \frac{\omega_o}{\omega_t r}} \tag{3.10}$$

The derivation details for R/R_s are given in Appendix A.2. The MOS internal noise sources such as the mean square drain ($\overline{i_{nd}^2}$) and the gate ($\overline{i_{ng}^2}$) noise currents are given as [76]

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\triangle f \tag{3.11}$$

$$\overline{i_{ng}^2} = 4kT\delta g_g \triangle f \tag{3.12}$$

with $g_g = \frac{\omega_0^2 C_{gs}^2}{5g_{d0}}$, k is the Boltzmann constant, T is the absolute temperature, $\triangle f$ is the bandwidth. Further, it includes γ and δ that are the channel thermal and gate noise coefficients with the values 2/3 and 4/3 respectively for long channel devices. The gate induced noise and the channel thermal noise has a correlation, C, with an approximate value of j0.395 that can be given as [77]

$$C \equiv \frac{\overline{i_{ng} i_{nd}^*}}{\sqrt{\bar{i}_{ng}^2}\sqrt{\bar{i}_{nd}^2}} \tag{3.13}$$

By considering equations from (3.4)-(3.13), the overall noise factor can be expressed as

$$NF = \frac{R}{R_s}\left(1 + \frac{\omega_0^2\gamma}{\alpha}\frac{C_t^2}{g_m}\frac{R\chi}{\left(1 + \frac{\omega_0^2 L_s}{\omega_t r_{ds}}\right)^2}\right) \approx \frac{R}{R_s}\left(1 + \frac{\omega_0^2\gamma}{\alpha}\frac{C_t^2}{g_m}R\chi\right) \tag{3.14}$$

where $\chi = \left(1 - 2C\frac{C_{gs}}{C_t}\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{C_{gs}^2}{C_t^2}\frac{\delta\alpha^2}{5\gamma}\left(1+\beta^2\right)\right)$ with $Q_s = \frac{1}{\omega_0 C_t R}$. The derivation details of the NF is given in Appendix A.2.

The above equation for NF can be related to the width of the device either through a square law model or through a parameter extraction. If one uses a square law model then it becomes region dependent and it cannot be used for designing LNA in MI or in WI region. Hence to get a unified model that is suitable for all inversion regions, NF equation should be modified by introducing a few more parameters. The details are as follows: From the basic relations, width of the device can be

written as

$$(W/L) \propto \frac{I_d}{f\left(V_{gs} - V_{th}\right)} \tag{3.15}$$

The (3.15) can be evaluated based on the normalized current, i, which is given as

$$i = \frac{I_d}{W/L} \Rightarrow W = \frac{LI_d}{i} \tag{3.16}$$

where i is called the normalized current. Using (3.16), the gate-source capacitance is given as

$$C_{gs} \propto WLC_{ox} = NWLC_{ox} \tag{3.17}$$

$$\Rightarrow C_{gs} = \frac{NL^2C_{ox}I_d}{i} \tag{3.18}$$

where N is a constant of proportionality whose value depends on the region of inversion. The total capacitance, C_t, with a capacitance ratio $C_r = \frac{C_{ext}}{C_{gs}}$, is given as

$$C_t = C_{gs} + C_{ext} = C_{gs}\left(1 + C_r\right) \tag{3.19}$$

By considering inverse normalized current as a parameter and from equations (3.16)-(3.19), $\frac{R}{R_s}$ and NF can be re-written as

$$\frac{R}{R_s} = \frac{Q_{ind}R_s - \frac{2R_sN\omega_0L^2C_{ox}(1+C_r)}{i(g_m/I_d)r} + R_{g,BW}\left(Q_{ind} - Q_{BW}\right) + \frac{I_dQ_{ind}R_\square}{12n^2i}}{R_s\left(Q_{ind} - \frac{i}{N\omega_0I_dL^2C_{ox}(1+C_r)} - \frac{N\omega_0L^2C_{ox}(1+C_r)}{i(g_m/I_d)r}\right)} \tag{3.20}$$

$$NF = \frac{R}{R_s}\left(1 + \frac{\omega_0^2\gamma R_s}{\alpha}\frac{R}{R_s}\frac{\left(NL^2C_{ox}\right)^2}{i\left(g_m/I_d\right)}I_d\chi(1+C_r)^2\right) \tag{3.21}$$

where $\chi = \left(1 - \frac{2C}{1+C_r}\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{1}{(1+C_r)^2}\frac{\delta\alpha^2}{5\gamma}\left(1+\beta^2\right)\right)$, $R_\square$ is the polysilicon sheet resistance and n is the number of gate fingers.

Unlike the expression in [69] where the noise factor is related to overdrive voltages through a strong inversion based velocity saturation dependent model, the expression for NF in (3.21) remains the same irrespective of the region of inversions. The latter expression is related to the overdrive voltages through factors such as (g_m/I_d), N, and i which are independent of device sizes and can be easily extracted for different inversion regions. Hence, (3.21) may be referred to as a unified noise factor for a cascode LNA as it can be used to estimate noise in all the regions of inversions. Noise estimation can be carried out with the help of this unified model and it will be discussed in the

section 3.4.

As mentioned earlier, a semi-empirical model could provide an analytical solution for all the inversion regions. Before getting into the detailed analysis with such a noise model, one needs to know how these factors (g_m/I_d), N and i are extracted. The parameter extraction methodology is given in the following section.

3.3 Methodology for parameter extraction

Basically, the performance of a circuit depends on the selection of the overdrive voltage (or effective voltage, V_{eff}), the channel length (L) and the drain current (I_d) of individual MOS devices [71]. Although V_{eff} is the prime deciding factor as discussed in the earlier section, L and I_d also make a significant performance difference and hence should be considered for circuit design. However for parameter extraction, different values of L and I_d need not be considered. This is because the resulting performance can be easily scaled with different values of L and I_d while incurring only a minor error in the estimation. Hence, parameter extraction is carried out with different values of V_{eff} while maintaining L and I_d constant. However in reality, only the channel length can be maintained constant in the experiment for parameter extraction. It is because the device width (W) has to be varied with a change in V_{eff} value throughout the experiment or simulation to maintain a constant current. Nevertheless to record the data for a selected current value, firstly, the extraction is carried out for different values of 'W' and later a data set corresponding to the required drain current is separated from the entire set of recorded compilations.

As we know, not all current values are realizable in each region of inversion because the device dimensions are limited and are given as (W_{max}, W_{min}, L_{max} and L_{min}) by the foundry. We are interested in a specific single current value which is achievable in all the three regions of inversions in-order to create a parameters data set. The lower current values are limited by W_{min} in SI region and in contrast higher values of current are limited by W_{max} in WI region. Consequently, only the intermediate current values which fall within these limits are achievable in all the inversion regions. The current value corresponding to the condition (W_{min}, V_{effmax}) is considered here as it is most likely to be realizable in all the regions of inversion. Therefore, it may be noted that the current selection cannot be arbitrary; a specific current value is to be selected to guarantee that all the three inversion regions are covered for carrying out the parameter extraction.

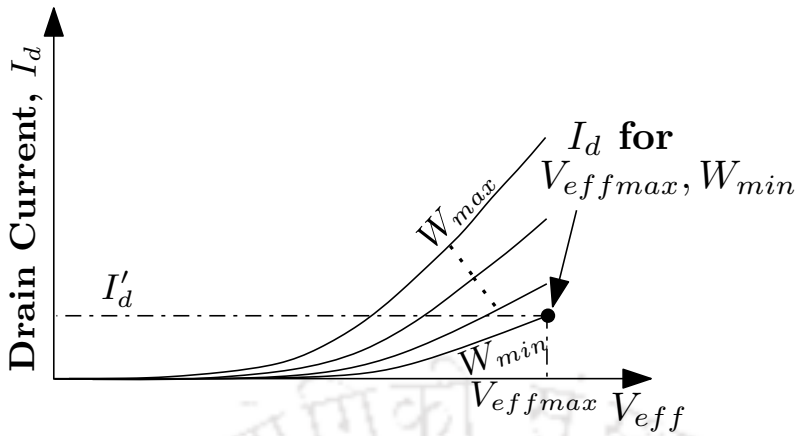


Figure 3.4: Selection of drain current, I_d, i.e. I'_d for parameter extraction.

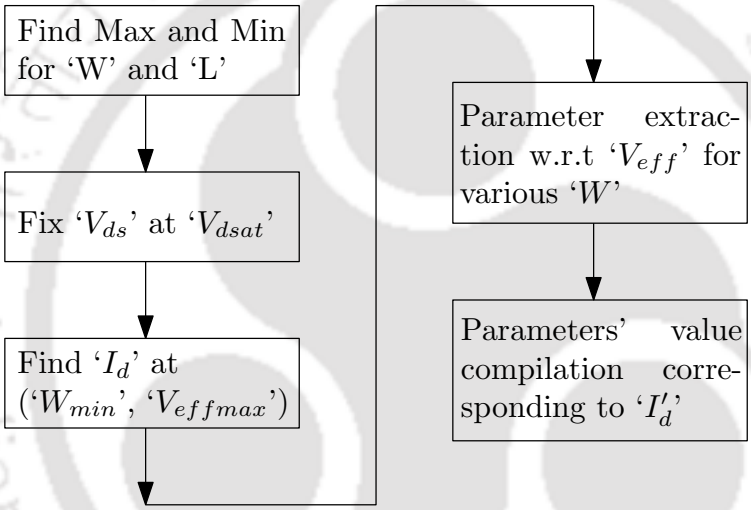


Figure 3.5: Parameter extraction methodology.

The drain current selection for parameter extraction is shown in Fig. 3.4. It shows that a suitable drain current I'_d, is found at V_{effmax} (the maximum value of V_{eff}). Hence, I'_d defines a criteria for the current selection. Although, any value of current above I'_d, unless limited by W_{max} in weak inversion, covers the full range of V_{eff}, the current value corresponding to V_{effmax} and W_{min} (minimum device width) condition is selected keeping in view the target of low power consumption.

The extraction methodology is given in Fig. 3.5. Firstly, the minimum width (W_{min}) and the minimum channel length (L_{min}) are found for a given device. The drain-source voltage (V_{ds}) is set to V_{dssat} to confirm that transistor works in saturation through all the inversion regions. The minimum

V_{ds} voltage is decided by the maximum gate-source voltage (V_{gs}) which may be given as

$$V_{DSSATmin} = \frac{V_{GSmax} - V_{th}}{n} \tag{3.22}$$

where V_{th} is the threshold voltage of the device and n is the substrate factor. Keeping the device in saturation, the current I'_d, corresponding to (W_{min}, V_{effmax}) is found and this current is to be used as a reference for all future extractions. Subsequently, all the required parameters are extracted with distinct values of device width, W, for a whole range of V_{eff}. Lastly, values corresponding to I'_d is compiled as a reference data for further analysis and design of low noise amplifier. Parameters such as (g_m/I_d), C_{gs}, i and the required W value to maintain a specific current are extracted. The required value of N is then derived from the known values of C_{gs} and W.

3.4 Analysis and design of low power LNA

An analytical model suitable for parameter extraction based design was developed in the earlier section 3.2.1. The R/R_s and NF equations are based on factors such as (g_m/I_d), N, and i and they are used for optimizing the design for low power. Similar to other parameters, the normalized current, i, is a function of only the MOS overdrive voltage and is independent of device sizes. Normalized current, i, is plotted for different values of device width 'W' and is shown in Fig. 3.6. From Fig. 3.6, it can be observed that drain current of the device shows negligible variation with respect to its width. It implies that the factor i can be easily extracted for any single value of width and can be used for any arbitrary device sizes while expecting negligible errors. This does not affect the accuracy of the design. Another parameter, N, a proportional constant shows a value of 0.1, 0.43, and 0.76 respectively in WI, MI and SI regions of inversions.

The sizing of core transistor depends on the analysis of (3.20) and (3.21). Every parameter in these equations is extracted for 65nm RF CMOS device and will further be used for designing a low-power LNA. For simplicity, the noise coefficients of a long channel transistor [78] are assumed for this analysis. Further, in this analysis, every element is considered on-chip and hence Q value for inductors is chosen to vary from 5 to 10 while C_{gse} is assumed to vary from 0.2 fF to 0.5 fF.

Noise figure analysis is carried out for different values of C_{gse} with different overdrive voltages (V_{eff}). The noise performance with respect to quality factor (Q_g) of the gate inductor for various overdrive voltages is shown in Fig. 3.7. It can be observed that higher Q factor of the gate inductor

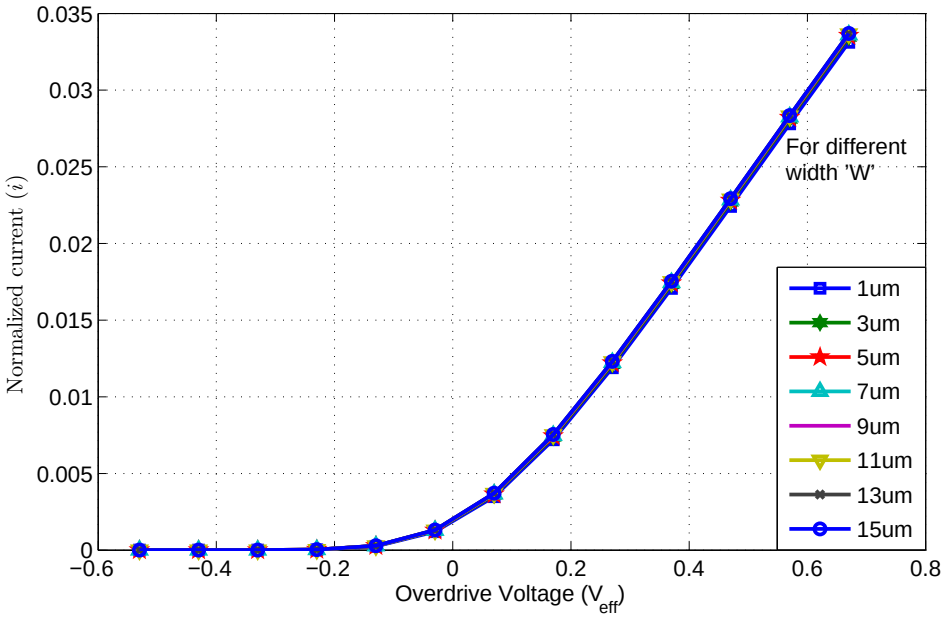


Figure 3.6: Normalized current with respect to overdrive voltage (Veff) for different values of 'W'.

improves the noise figure of the low-noise amplifier. However, it is difficult to achieve high Q for on-chip inductors.

The extra capacitance C_{gse} aids in improving the noise figure. From Fig. 3.7, a higher value of C_{gse} seems to be favorable; however, it is seen that a C_{gse} value greater than 0.4 pF does not show any significant improvement in noise figure. As a matter of fact, there is a serious problem associated with choosing a higher C_{gse} since it causes a reduction in both gain and input impedance.

In addition to its dependency on Q_g and C_{gse}, noise figure shows a greater dependency on device overdrive voltages. It can be observed from the Fig. 3.7 that larger V_{eff} degrades the noise performance. This is mainly because the required value of L_g becomes larger as V_{eff} increases and proportionally its noise contribution becomes higher. Therefore, one can choose lower V_{eff} to improve the noise performance. Lower V_{eff}, however, increases the required area for a given power. Finally, a V_{eff} of -94 mV is chosen for the core transistor with a C_{gse} of 0.3 pF. Typically, Q of the gate inductor that can be achieved is around 7. As shown in Fig. 3.7, with these values of V_{eff}, C_{gse} and Q_g, noise figure is expected to be around 3 dB. The resulting value is slightly large for CS degenerated LNA. The incorporation of the low-Q inductor at the gate and further operating the device in low-power condition has increased the noise figure of the CS degenerated LNA.

A few iterations are carried out to decide the final values of the components. The final values are

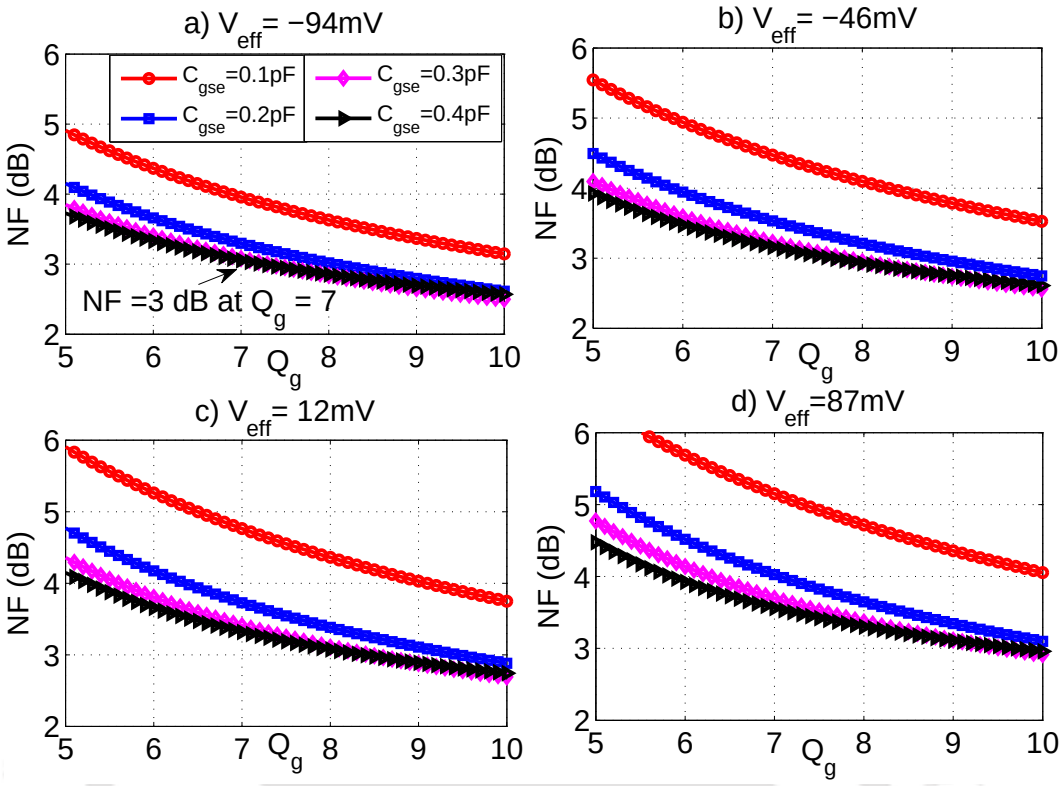


Figure 3.7: Noise performance estimation for different values of Q_g, C_{gse}, and V_{eff}.

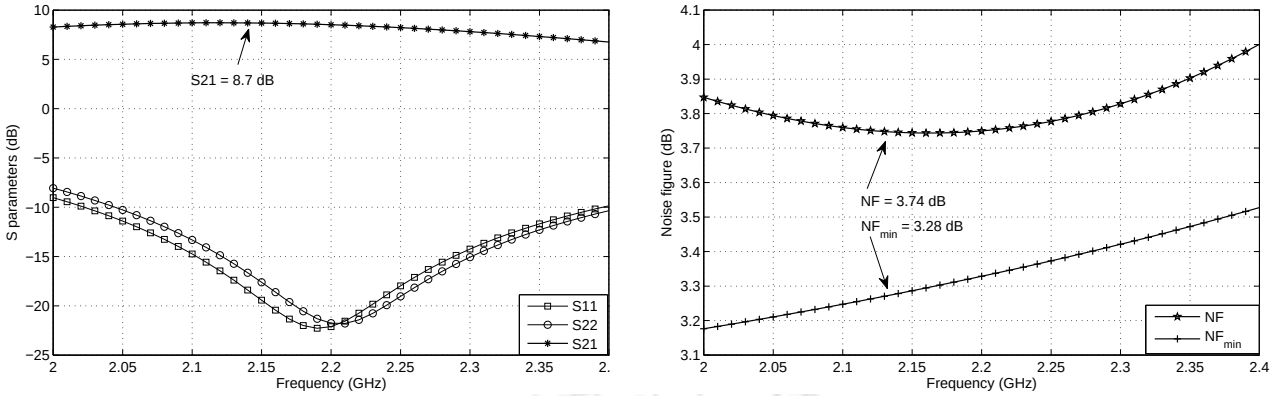
Table 3.1: Designed values for transistor sizes and passive components

$\frac{W_0(\mu m)}{L(nm)}$	$\frac{167}{60}$	$L_g(nH)$ 19.6	$R_B(\Omega)$ 6K
$\frac{W_1(\mu m)}{L(nm)}$	$\frac{16.4}{60}$	$L_s(nH)$ 2.3	$C_d(F)$ 130f
$\frac{W_2(\mu m)}{L(nm)}$	$\frac{9}{60}$	$L_d(nH)$ 18	$C_{gse}(F)$ 70f

shown in the Table 3.1. The value for C_{gse} is chosen to be lower than the designed value to avoid any degradation in gain due to a reduction in transition frequency of the device.

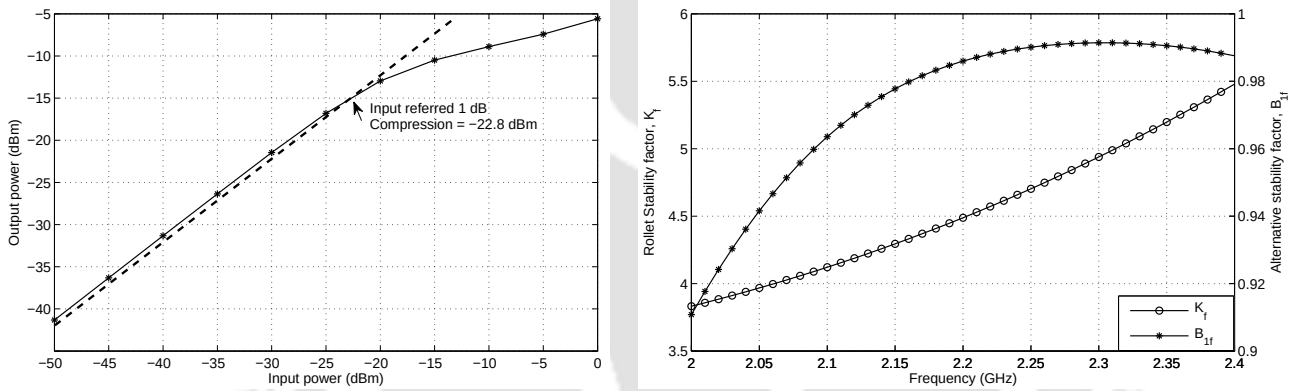
3.5 Results and discussions

A cascode LNA is designed and simulated using UMC's 65nm RF CMOS technology. Every component of the LNA is implemented on-chip. The LNA occupies a total core area of 680 μm X 650μm. The design is intended for the 2.14 GHz band. Post-layout simulations are carried out with RLCK parasitic extraction to verify the overall performance of the LNA. The simulated S-parameter values are shown in Fig. 3.8(a). S11 shows an excellent value of -22 dB that implies a good input match. $|Z11|$ achieved is around 46 Ω at 2.14-GHz.



(a) (b)

Figure 3.8: Response of the LNA after post-layout simulation with RLCK parasitic extraction. a) S-parameter analysis, b) Noise analysis.



(a) (b)

Figure 3.9: Linearity and stability analysis of the LNA after post-layout simulation with RLCK parasitic extraction.

The NF is around 3.74 dB which is a little higher than the estimated value in the earlier section. It is because the estimation has included effects only from the core device and the gate inductor. The resulting noise figure and the minimum achievable noise figure are shown in Fig. 3.8(b) that are close to each other in the band of interest.

Simulation results show a moderate power gain of 8.7 dB with DC power consumption of only 315 μW. The reduction in gain is mainly due to the lower Q value of L_d. With RC extraction and with every element on-chip, the gain is around 10.4 dB. However, the parasitic mutual inductances have affected the output impedance and thereby reducing the gain to 8.7 dB in the simulation with RCLK extraction.

Linearity and stability analysis are being carried out after RCLK extraction. This is shown in

Table 3.2: Performance comparison with other low-power LNAs

Specification	This work**	[80]*	[75]*	[81]*	[82]*	[83]	[84]	[44]	[85]
Technology(nm)	65	180	90	180	130	180	130	130	130
Frequency (GHz)	2.14	1	2.45	2.4	3	2.4	2.4	2.4	2.4
Power (μW)	315	260^{+}	684	945^{++}	400	1100	60^{+}	240	600
P_{1dB} (dBm)	-22.8	-13	-15	-15	-25	N/R	-19	-13.5	N/R
NF (dB)	3.74	4.6	4.36	5.2	4.7	5.2	5.3	4.54	3.8
Gain(dB)	8.7	13.6	9.7	21.4	9.1	20	13.1	18.2	25.2
FOM	28.5 #	47.4^{++}	30.6^{++}	22.9^{++}	28.4	21.3	43.4	44.1	29.9
Area (μm $\times$ μm)	680 $\times$650	890 $\times$780	1080 $\times$845	500 $\times$360	N/R	N/R	630 $\times$630	N/R	740 $\times$840

* Post-fabricated results;** Post-layout with RLCK extraction;$^{+}$ Extra buffer is used but power consumption of buffer is not mentioned;#IIP3 is considered to be 10 dB higher than P_{1dB};$^{++}$Values are considered from the inference as these are not specified explicitly in the literature;N/R:Not reported.

Fig. 3.9(a). The 1 dB compression point achieved is around -22.8 dBm. In order to check the stability, factors such as K_f (Rollet stability factor) and B_{1f} (Alternative stability factor) [79] are verified for the band of interest. This is shown in Fig. 3.9(b). According to [79], K_f and B_{1f} have to be greater than 1 and 0 respectively for satisfying the stability requirement. It can be inferred from the figure that the low-noise amplifier presented here is absolutely stable.

Finally, the performance of the designed LNA is compared with other narrow-band low-power LNAs. This is shown in Table 3.2. In comparison to most of the other LNAs, low noise amplifier presented here consumes relatively less power. Although the core transistor in [80,84] consumes lower power than the present design, their design additionally uses buffer stage whose DC power requirements are unknown. For an effective comparison, a figure of merit (FOM) [82], which takes into account all the significant parameters - gain, linearity, dc power, noise figure and operating frequency is considered and is given in (3.23).

$$FOM = 10\log\left(100\left(\frac{Gain\,[dB]}{(F-1)\,P_{dc}\,[mW]}\right)\left(\frac{IIP_3\,[mW]}{P_{dc}\,[mW]}\right)\right) + 10\log\frac{f_0}{1GHz} \tag{3.23}$$

The work [80] achieves the highest FOM mainly because of its lower power consumption and a better IIP3 compared to other contributions. However, the addition of the buffer power would lower the FOM for [80].The presented LNA achieves a moderate value of FOM because of its lower IIP3. However, this can be improved with the use of specific linearity enhancement techniques. Overall, the

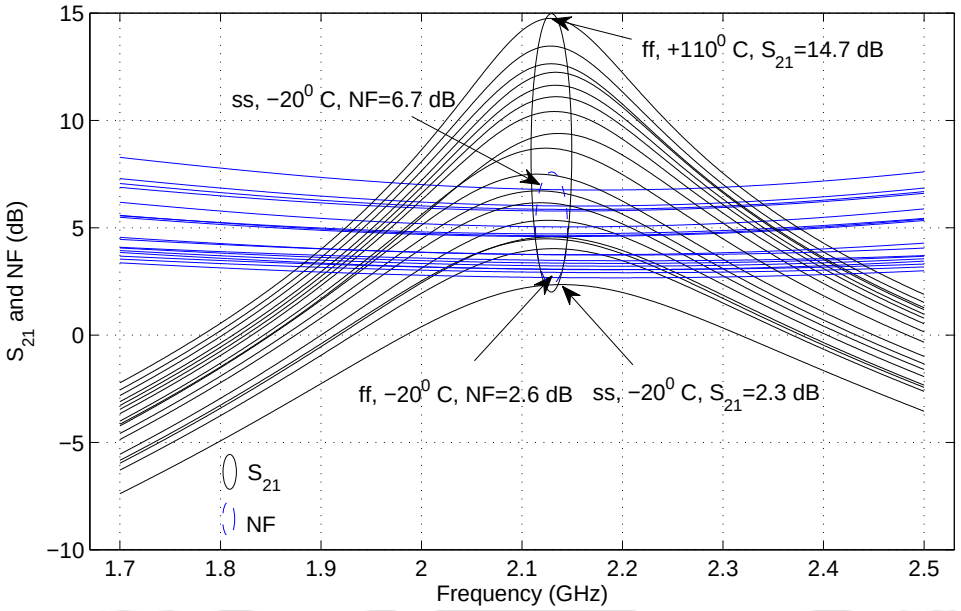


Figure 3.10: Performance deviations due to PVT variations.

proposed LNA offers the best noise figure that is minimum among all the other low-power LNAs given in Table 3.2.

Although low-power consumption is been achieved, the noise figure is high for common-source degenerated LNA. It is because of the reduction in gain due to the biasing for low current operation and also due to the usage of a low quality-factor, on-chip gate inductance. On the other hand, the given LNA with conventional biasing when implemented in sub-nanometer technologies becomes highly susceptible to PVT (Process-Voltage-Temperature) variations and it is more pronounced in moderate inversion based LNAs. Hence, appropriate PVT compensation circuits are required to nullify these effects. The performance of the circuit, when subjected to process and temperature variations, is given in Fig. 3.10. The analysis is carried out by taking all corners into account and by varying the temperature from -20^oC to $+110^oC$. It can be observed that S_{21} has undergone more than $\pm 70\%$ deviation from its nominal value of 8.7 dB and similarly NF exhibits more than 4 dB variation when the circuit is subjected to a temperature range from -20 to $+110^oC$ while taking all the corners into consideration. It severely affects the yield and the implemented amplifiers become highly unreliable.

3.6 Conclusion

A fully integrated, low power cascode LNA is analyzed and presented for 2.14 GHz band. The noise performance of the LNA is analyzed for the different regions of inversion using the developed unified noise factor model. It is found that moderate inversion biased LNAs offer an on-chip implementable solution for passive elements compared to strong inversion region when operated in low power conditions. The noise and power performance of the resulting circuit are better compared to other subthreshold LNAs in the literature, however it appears low for the CS degenerated LNA. The key observations and certain issues related to the low-power LNA are as follows.

- The circuits, when implemented in sub-nanometer technologies, cannot be used independently as it affects the yield and performance. Hence, it demands development of compensation circuits through which the degree of reliability can be enhanced.
- It seeks for implementation of additional techniques to improve performances such as gain and noise figure as these are degraded due to the constraints on the power consumption.
- It is imperative to use high-quality factor, off-chip inductor atleast at the gate in-order to avoid further noise performance degradation of low power LNA. The noise performance of LNAs are already affected by the low-power conditions, and the incorporation of on-chip lossy inductors to that only adds further degradation.

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4

Compensation circuit for LNAs

Contents

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4.1 Introduction

Compensation techniques are critical for circuits that are to be implemented in sub-nanometer technologies. As discussed in the earlier chapter, the performance of an LNA is expected to show relatively large deviations with respect to PVT (Process-Voltage-Temperature) variations when a device is operated in moderate or weak inversion regions [86]. These effects become more prominent in these inversion regions because of the exponential or pro-exponential dependency of the device-current on its overdrive voltage. Moreover in circuits like LNA, the corresponding performance deviation arises primarily because of the variation in the device trans-conductance, g_m. Therefore to stabilize g_m of the core device against PVT variations, compensation circuits are needed in an LNA. The compensation mechanisms can be realized through several techniques. These can be based either on conventional constant g_m techniques or on calibration techniques or based on variable gate-bias techniques.

There exist several constant g_m techniques for general-purpose circuits such as amplifiers (OTAs) and $g_m - C$ filters. One such technique [87,88] involves correcting the g_m variation by adjusting the tail current of the amplifier with the help of feedback mechanism. In [89,90], the concept of incorporating complementary techniques are used to stabilize the $g_m - C$ filter performance. In another approach, stable g_m is achieved with the help of variable conductance, 1/R, as a reference that is implemented using switched capacitor schemes [91]. These techniques, if used for LNA, require the core device of the amplifier to be part of the compensating mechanism, which in turn, affects the functionality and the performance of the low-noise amplifier. Furthermore, these topologies also limit the scaling of the supply voltage. Alternatively, the scheme presented in [92] can be employed for the LNA. However, it demands considerably higher amount of power if the core device width has to equal those in the constant g_m circuits in order to keep the divergence minimum. Further, as the bias for the LNA has to be generated within the constant g_m circuit, it would again restrict voltage scaling.

Another approach is to nullify g_m variations through the implementation of calibration techniques or with the help of built-in self-test mechanisms [93–96]. These techniques are targeted mainly for correcting the post-fabrication effects by employing extra circuits to improve the overall yield. These techniques, however, require complex accessories and are very power hungry. Further, the majority of calibration techniques involve time consuming multiple iterations.

As opposed to these two approaches, the constant g_m method based on variable bias voltage generation [97–100] promises to be an efficient technique for designing PVT-independent LNA. In [97],

which is also the basis for [98, 99], conventional g_m topologies are used in a cross-coupled manner to generate a gate bias such that it balances the core device's current against process or temperature variations. However, these become vulnerable to supply variations and also would severely suffer from process variations when implemented in sub-nanometer technologies. In addition, like [92], these mechanisms also limit possible low voltage designs. In a distinctive approach [100], the core device is split into two halves with one half driven by a compensating gate voltage while a constant drive is applied to the other half. As a result, when there are deviations in g_m, compensating voltage is generated which in turn maintains overall g_m constant. Though [100] shows better results in respect of process variations, it does not yield optimum results for temperature variations. Moreover, [97, 100] does not feature any kind of feedback path for tracking LNA core device current, hence it cannot be relied upon to work in all conditions.

It is clear from these discussions that there is a need for low power, low voltage LNA that requires an effective compensation technique to tackle its performance deviations due to PVT variations. For implementation, compensation technique must let the low voltage option feasible and must utilize feedback controlling technique without actually hampering the LNA performance.

In this chapter, we present a new compensation technique that minimizes the PVT variations of the performance of the near sub-threshold operated LNA. The controlling mechanism basically involves sensing the deviation of the core device current from its nominal expected value and accordingly an error signal is generated. This error is then used to correct the drifted value by applying a variable gate bias voltage to the core device of the LNA to keep the g_m constant. For implementation, the proposed technique requires an error generation circuit along with a constant current source that is used as a reference. Accordingly, a low voltage constant current reference is also realized based on a conventional PTAT current reference. However, the resulting currents are compensated with a new, simple compensating circuit technique. In addition to the benefit of minimum PVT variations with low voltage operability, the proposed scheme is a self-biased technique which does not require any additional inputs from external band-gap constant references.

4.2 Proposed compensation technique

The conventional current mirror biasing [76] is shown in Fig. 4.1. The required gate voltage is produced by adjusting the values of the resistor R_B and the aspect ratio of MOS M_2. Since this type of

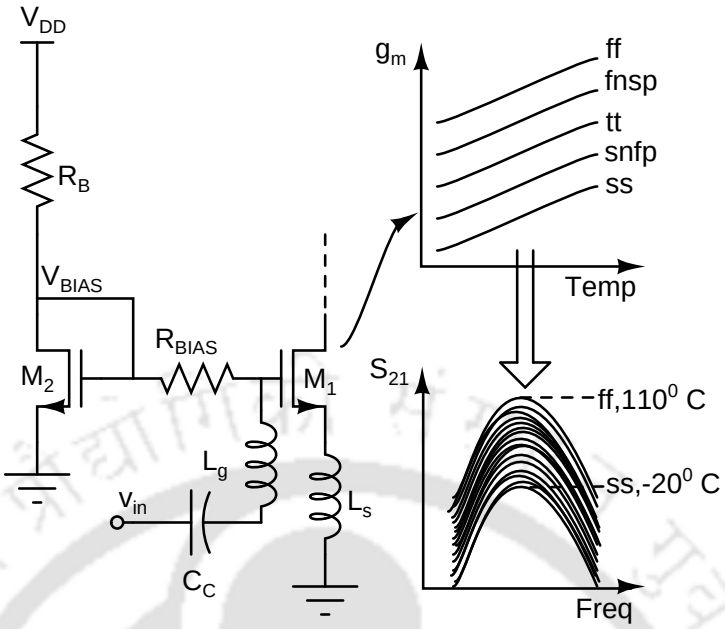

Figure 4.1: The conventional biasing mechanism of LNA depicting the change in S_{21} due to process and temperature variations.

biasing lacks any type of controllability, the performance undergoes drastic deviations when the circuit is subjected to process, temperature and supply variations. Fig. 4.1 highlights the variation in S_{21}, caused primarily due to the changes in g_m which is because of variations in process and temperature. Hence the LNA becomes unreliable when it is implemented with such biasing techniques. However, the same biasing concept can still be used for realizing a robust LNA if it is modified to incorporate PVT variation handling abilities. Importantly, g_m of the core device has to be maintained constant. If the constant R_B in Fig. 4.1 is replaced either by a variable resistance or in general a variable current source whose magnitude changes are completely mapped by LNA current variations then resulting amplifier's g_m can be stabilized.

The conceptual diagram of the proposed compensation technique is shown in Fig. 4.2. The pointers describe the feedback technique showing how the LNA current is stabilized with the help of generated intermediate voltages. It works on the principle of sensing the core device current and then correcting the current through a negative feedback mechanism. It consists of an error generator circuit that generates an error voltage by comparing a fraction of the LNA current (K.I_{LNA}), where K is the current scaling factor, with a constant current reference (I_{CCR}) source. Any increment or decrement in I_{LNA}, when it is compared with I_{CCR}, results in corresponding changes in the voltage across the node impedance, Z_{int} that comprises of the node capacitances. This in turn acts as an error voltage

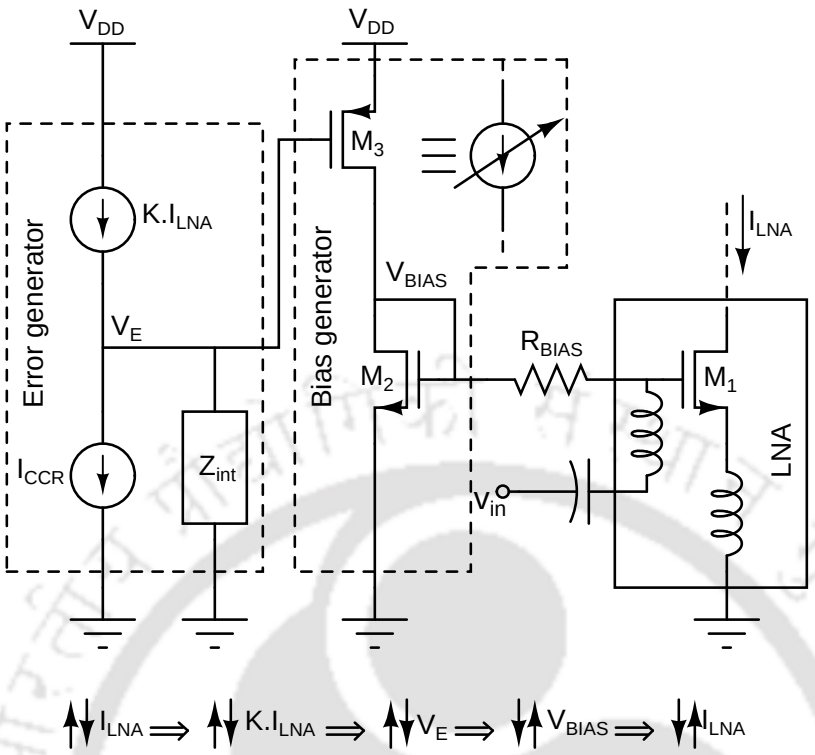

Figure 4.2: The conceptual diagram of the proposed technique for PVT compensation of the LNA.

for the bias generator. The generated error voltage drives the gate of a PMOS transistor, which passes current to the diode connected NMOS, M_2, and alters the current that needs to be sourced. As a result, the gate voltage to the core device is modified to the extent that brings the LNA current back to the expected value.

As I_{CCR} is a constant current source, the change in error voltage is directly proportional to the change in I_{LNA} and is given as

$$\Delta V_E \ \alpha \ \Delta I_{LNA} \tag{4.1}$$

Assuming that transistors M_2 and M_3 operate in weak inversion (WI) region, the current through these devices can be equated to find the effect on the resulting V_{BIAS} i.e. is V_{GS2}. From [101] for the current equation in WI, V_{BIAS} can be given as

$$V_{BIAS} = V_{GS2} = V_{thn} + n_n v_t \ln\left[\frac{I'_{0p}(\frac{W}{L})_3}{I'_{0n}(\frac{W}{L})_2}\exp\left(\frac{V_{DD} - V_E - V_{thp}}{n_p v_t}\right)\right] \tag{4.2}$$

where $I'_0 = \frac{I_0}{(\frac{W}{L})} = \mu\sqrt{\frac{q\epsilon_{si}NDEP}{2\phi_s}}v_t^2$, with V_{th}, n, and v_t respectively are the threshold voltage, the subthreshold swing of the device and the equivalent thermal voltage. Explanations of other parameters

can be found in [101]. The subscripts n and p represent NMOS and PMOS devices respectively. Assuming equal values of $I_0'(\frac{W}{L})$, n, V_{th} for both NMOS and PMOS devices, (4.2) can be written as

$$V_{BIAS} = V_{thn} + n_n v_t \frac{V_{DD} - V_E - |V_{thp}|}{n_p v_t} \approx V_{DD} - V_E \tag{4.3}$$

From (4.1) and (4.3), it can be shown that for a constant V_{DD} the following holds:

$$\Delta V_{BIAS} = -\Delta V_E \;\; \Rightarrow \;\; \Delta V_{BIAS} \;\; \alpha \;\; -\Delta I_{LNA} \tag{4.4}$$

Equation (4.4) highlights the core functionality of the proposed compensation technique. According to (4.4), if there are any changes in I_{LNA} correspondingly opposite changes take place in V_{BIAS} that counters the initial change in LNA current. As a result, the LNA current is maintained in equilibrium irrespective of any kind of perturbations that occurs due to PVT variations.

The proposed technique has three main advantages. Firstly, depending on the accuracy of I_{CCR}, it gives guaranteed control of the LNA bias current. Secondly, as M_3 is placed in the feedback path, it can have small drain-source drop across it. Hence it allows considerable amount of V_{BIAS} for the LNA that makes voltage scaling a feasible option. Thirdly, the compensation circuit along with I_{CCR} consume less power as only a fraction of the LNA current is used for error generation.

The advantages, however, come at the expense of two implementation challenges. Firstly, it demands for an accurate constant current reference that must necessarily operate at a voltage below the operating voltage of the main LNA. Secondly, tracking of the LNA current cannot be directly derived from the main LNA as it affects the LNA performance. Hence implementing a constant current reference and an error generation circuit that addresses these issues is a challenging task. These are addressed in Section 4.3 and 4.4 respectively.

4.3 Low voltage Constant Current Reference

As discussed in Section 4.2, the proposed compensation scheme is based on comparison of I_{LNA} with that of an ideal current source, I_{CCR}, that is independent of PVT variations. Ideal constant current source, however, is not realizable - it can only be approximated by a current source that exhibits minimum possible fluctuations when it undergoes unavoidable PVT variations. Furthermore, it must be able to operate at voltage that is below the operating voltage of the amplifier in order that implementation of a low voltage LNA is feasible.

In general, most constant current sources are based on the boot-strapping technique (or β multiplier) [102, 103] that are robust against supply variations. This basic structure is further improved to counter-balance temperature and process variations. Temperature compensation, in particular, can be accomplished through five broad categories of methods: (a) temperature insensitive current reference using BJT [104] or weak inversion biased MOS based curvature cancelation techniques [105], (b) selecting and biasing devices at ZTC (Zero Temperature Coefficient) point [106–109], (c) generating and combining proportional to/complementary to absolute temperature (PTAT, CTAT) currents [110–112], (d) harnessing process parameter and resistor temperature dependency [113, 114], or (e) through generating CTAT controlled gate voltage [115]. As regards process variations, the compensation techniques can be broadly classified into four categories: (a) post fabrication trimming based on resistor [116, 117] or with trimmable floating gate devices [106, 108], (b) provision for programmability options [110, 117], (c) correlating threshold voltage variation to the gate voltage [107, 118], or (d) making one of the current constituents to correlate negatively with the other in order to maintain the overall current constant [119]. With the exception of a few, all others have used some form of β multiplier.

Among these several contributions, not every performance is achieved best with a minimal cost. The BJT based compensation technique suffers severe process variations [120] that may require additional process steps such as trimming. The ZTC based designs cannot guarantee exact cancelation of temperature coefficients because it is difficult to keep the device exactly at the ZTC point and any deviations from those result in non-zero variations. The PTAT and CTAT combination becomes complex when process compensations are also required to be incorporated. Moreover, all the contributions discussed above are targeted for supply voltages higher than 1V and are implemented with technologies larger than 130 nm. Furthermore, direct implementation of these techniques in sub-nanometer technologies may suffer from supply variations. An exception to these, the circuit in [121] offers low voltage operability option. However, the circuit is vulnerable to supply variations and thus demands a separate band gap reference circuit. For the proposed compensation mechanism, a suitable constant current technique has to be devised. Though it may not give the best performance when compared to each of the above contributions, it nevertheless gives reasonable performance for all process-voltage-temperature variations.

The circuit-diagram of the proposed constant current reference (CCR) along with the newly sug-

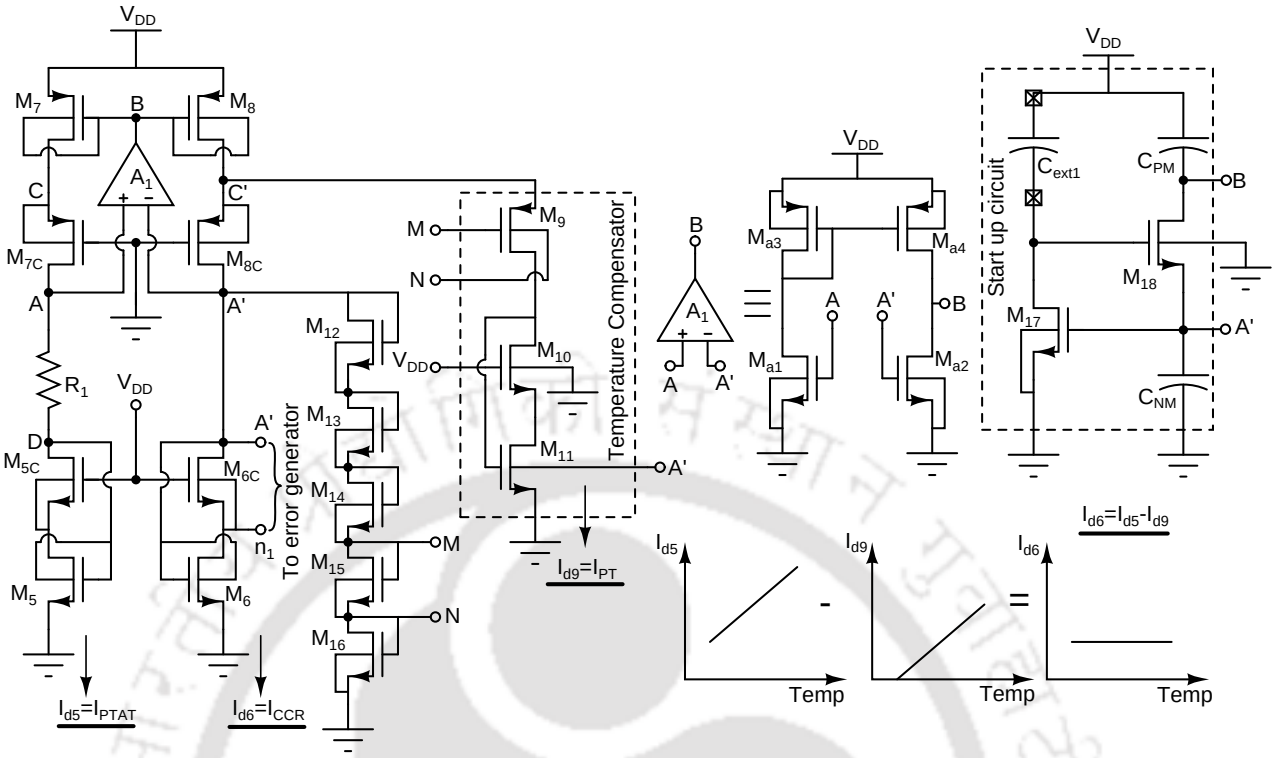

Figure 4.3: The complete diagram of the proposed self-biased low-voltage constant current reference (CCR).

gested temperature and process compensation technique is shown in Fig. 4.3. The basis for this circuit is the β multiplier [103] that can operate below 0.5 V of supply voltage and can be implemented in lower process technologies. The original beta multiplier is, however, is a PTAT reference which is further modified here to tackle all the PVT variations. The detail explanation is as follows.

The self-biased β multiplier consists of the core transistors M_{5-8} along with their respective cascodes M_{5C-8C}. The cascode devices $M_{7C,8C}$ together with a differential amplifier, A_1, are required to enhance the resistance to V_{DD} that otherwise gets degraded due to the short channel effects [70] in sub-nanometer technologies. One more pair of cascode devices, $M_{5C,6C}$, instead of a resistor [116], helps to match V_{ds} between MOS M_5 and M_6. All are intended to be biased in weak inversion region in order to consume minimum voltage headroom across it. To avoid the zero current state condition, a startup circuit [122] is also added as shown in the Fig. 4.3. The capacitances C_{NM} and C_{PM} in the circuit are realized by MOS devices; in addition to their assistance in the start-up circuit, these also help in maintaining the current reference's frequency stability [103]. The CCR uses triple well NMOS devices with their body being biased by few selective voltages that help in minimizing the process variations (this is discussed in following sub-section 4.3.2).

4.3.1 Temperature compensation

The idea behind the proposed temperature compensation technique is illustrated in Fig. 4.3 interms of current plots across different branches. The PTAT-current I_{PTAT} can be viewed as a composition of two constituents [105]: one is a constant current source that is referred to as I_{CCR} while the other is proportional to temperature and is denoted by I_{PT}. These currents are related as

$$I_{PTAT} = I_{CCR} + I_{PT} \tag{4.5}$$

As shown in Fig. 4.3, the right arm of the proposed CCR copies I_{PTAT} current from the left arm and, unlike in conventional implementations, the right arm is equipped with a provision called a "Temperature Compensator" to separate I_{CCR} and I_{PT} currents. The devices M_{9-11} constitute the temperature compensator that bypasses I_{PT} current. As a result, the remaining constant current I_{CCR} flows through M_6 and can be copied further to later stages.

The diode-connected devices, $M_{5,6}$, can be predicted to generate a negative temperature coefficient (NTC) gate voltage [123]. The resulting NTC voltage when applied to the gate of a PMOS device would induce a positive temperature coefficient (PTC) current through it. This concept is used in building a temperature compensator that uses a PMOS device M_9. However, as the source terminal of PMOS also has to be connected to intermediate node of the right arm of the current source for I_{PT} extraction, the final PMOS source-gate voltage results only in NTC. Fortunately, the threshold voltage (V_{th}) has a NTC [123] that helps in achieving a PTC current through it and the slope of $|V_{gs9}|$ can be reduced by feeding back a fraction of the voltage $V_{A'}$ (voltage across node A') to M_9 gate. The voltage division is accomplished through a series of diode connected transistors M_{12-16}. The devices $M_{9,11}$ are the core transistors of the temperature compensator while M_{10} is added to reduce the influence of M_{11} gate voltage to that of drain voltage. The temperature compensator consisting of M_{9-11} results in achieving an I_{PT} current whose temperature dependency slope can be varied by changing their aspect ratios. The body of $M_{9,11}$ controlled by intermediate voltages provide process compensation to a certain extent (this is discussed in the following sub-section).

The sub-threshold current from [101] can be generalized as

$$I_d(x) = Ka(x)exp(b(x))[1 - exp(c(x))] \tag{4.6}$$

where 'x' is the temperature variable and a, b, c relate the node voltages and the device parameters. In

general, c(x) that carries drain-source voltage dependency information is neglected since the condition, $V_{ds} >= 4v_t$ where v_t is the thermal voltage, is normally satisfied. However, if V_{ds} is made small so as to make it comparable with that of thermal voltage, v_t, then it can play a vital role in changing the characteristics of the curve: a(x) exp(b(x)). The reduction in $|V_{ds9}|$ is achieved by adding NMOS transistor M_{11}. In the CCR circuit of Fig. 4.3, M_9 would effectively extract the I_{PT} from I_{PTAT} current only if the slopes of both I_{PT} and I_{PTAT} are matched to each other. The device M_{11} when added, reduces V_{ds9} and different slopes of I_{PT} can be generated only by changing aspect ratios of these devices.

The complete development of an analytical model based on (4.6) becomes complex as the majority of variables exhibit both temperature-dependency and as-well-as inter-dependency. However, in order to observe how I_{PT} slopes change with aspect ratio, iterative solution is found for which node voltages are extracted from standard simulators and typical values of process parameters are considered from model files. The subthreshold current equation from [101] is used for calculation of M_9 current with $|V_{ds}| = |V_{C'} - V_{gs11}|$. The current in M_9 equals the current in M_{11}, and the generation of the voltage V_{gs11} is given as

$$V_{gs11} = V_{thn} + n_n v_t ln\Big[\frac{I_{d9}}{I'_{on}(W/L)_{11}}\Big] + V_{offn} \tag{4.7}$$

The details of the parameter can be found in (4.2) and in [101]. V_{ds11} is neglected as it is larger than v_t. Equation (4.7) with I_{d9} as the subthreshold current [101] has to be solved iteratively with the values of terminal and threshold voltages from the simulator to obtain the slope dependency on the device sizes. From simulation, the node voltages $|V_{gs9}|$, $|V_{sb9}|$, and $V_{A'}$ showed a temperature coefficient ranging from -0.6 to -0.8mV/C for the circuit of Fig. 4.3. In the following analysis, for simplicity, it is assumed that the nature of these voltage responses remain constant irrespective of M_{9-11} aspect ratios.

The final iterative solution for I_{d9} w.r.t temperature is shown in Fig. 4.4. For this analytical response, the aspect ratio of M_{11} device is kept at a moderate value of 10 as the minimum size does not yield a converging solution. Next, with this constant value of $(W/L)_{11}$, $(W/L)_9$ is varied from 1 to 40 to illustrate the temperature compensator's degree of freedom. The dashed and the solid lines in Fig. 4.4 respectively denote variation of I_{d9} in absence and in presence of M_{11}. It can be observed that M_9 along with M_{11} exhibits a more linearized response compared to a case which uses M_9 alone.

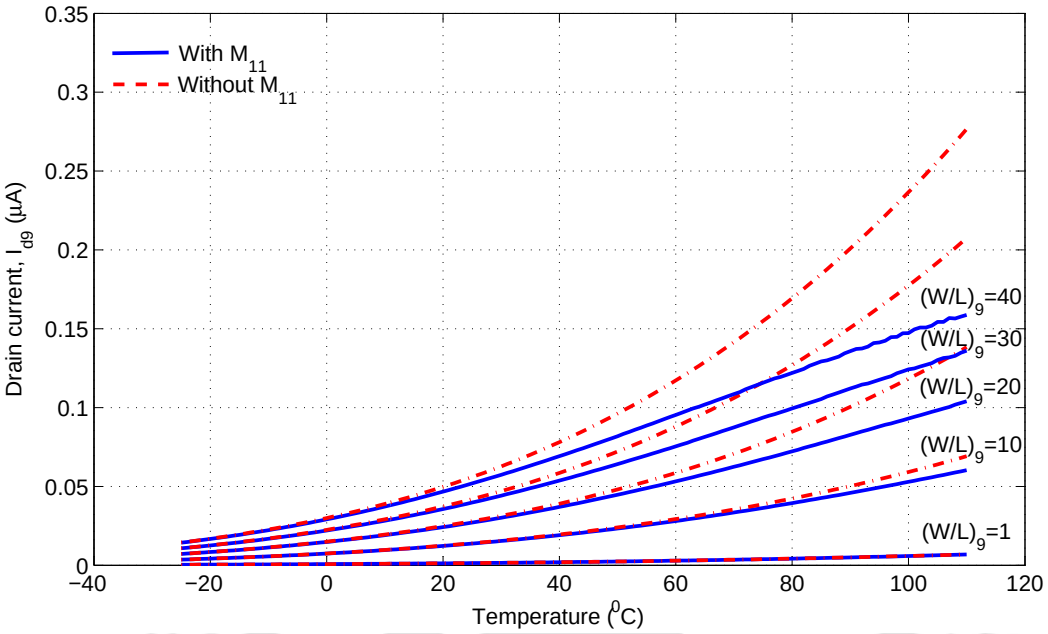

Figure 4.4: The analytical response of the temperature compensator for different size selection of M_9.

Further, it shows the possibility of obtaining different slopes (i.e. different temperature sensitivity) depending on particular selection of $M_{9,11}$ device sizes. Thus, it may be concluded from the Fig. 4.4 that M_{9-11} as a temperature compensator aids in extracting the undesired increments in the current which makes constant current generation possible with the addition of minimal circuits.

4.3.2 Process compensation

The performance deviations due to the process variations that include intra and inter-die variations [124] is a serious concern in sub-nanometer technologies. The effect of intra-die variations can be minimized by special layout techniques along with selection of large device sizes [125]. Alternative techniques such as adaptive body bias control [86, 126] can be used to minimize the latter variations. Unlike [118, 119], body bias control offers provision to minimize the process variation without being affected by supply variations.

Process variations are primarily due to the deviations in threshold voltage of the device and the process trans-conductance parameter, $\mu_{n,p}C_{0x}$ $(K_{n,p})$. For a diode connected transistor being sourced by a constant current, change in the gate-source voltage due to v_{th} and $K_{n,p}$ variations is given as

$$\Delta V_{gs} = \Delta V_{thn} + n_n v_t ln\Big[\frac{I_d}{\Delta I'_{on}(W/L)}\Big] \tag{4.8}$$

If one assumes I_d to be constant then it directly follows from equation 4.8 that a faster device tends

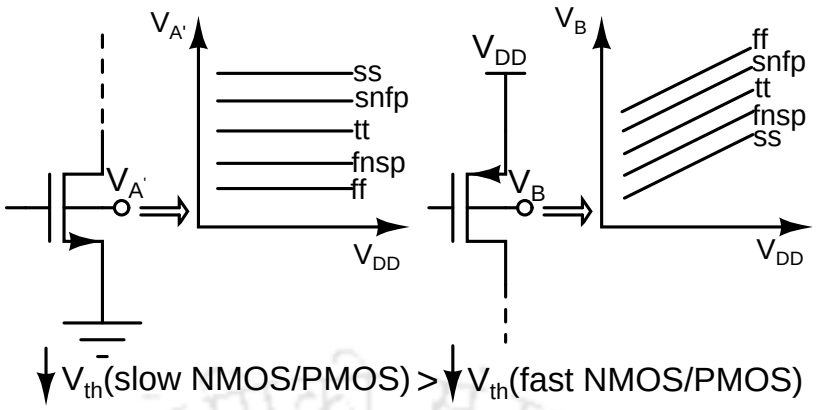

Figure 4.5: Illustration of process compensation for CCR.

to produce smaller V_{gs} compared to a slower one. Therefore in Fig. 4.3, $M_{5,6}$, the diode connected devices produce a gate voltage, V_D and $V_{A'}$, which are higher for slow NMOS compared to a faster one. Likewise, the diode connected PMOS, M_{a3}, in amplifier, A_1, induces a voltage, V_B, which is higher for fast PMOS compared to its slower counterpart. These induced voltages when further applied to the bulk of a transistor, correspondingly scales up or down the threshold voltage of the device (V_{th}). Thereby, it counter-balances the original shifts in the process parameters which in turn aids in minimizing the process variations.

For the circuit in Fig. 4.3, compensating voltages are mainly applied to the core transistors M_{5-8}. In addition to their process compensation relevancy, supply dependency of compensating voltages also need to be considered. For the devices, $M_{5,6}$, the compensating voltage applying to their bulk must be independent of supply variation as its source is connected to zero potential. On the contrary, as source of $M_{7,8}$ is connected to V_{DD}, the compensating voltage applying to the bulk of these PMOS devices must show correlation with the supply variation. Interestingly, V_D and $V_{A'}$ are independent of V_{DD} variation. However, V_B shows dependency towards the supply variation. As a result, V_D and $V_{A'}$ are more suited for the bulk of NMOS devices and V_B for the PMOS devices. Hence to minimize process variations, the bulk of the main devices M_5, M_6 and $M_{7,8}$ are fed by the intermediate node voltages V_D, $V_{A'}$ and V_B respectively. The process compensation technique which is used for CCR is illustrated in Fig. 4.5. Compared to other corner counterpart, slow NMOS (ss, snfp) and fast PMOS (ff, snfp) devices exhibit a higher $V_{A'}$ and V_B node voltages respectively. These when applied to respective bulks, the reduction of V_{th} in slow NMOS or PMOS device becomes higher relative to fast NMOS or PMOS device, thereby counter balancing the process variations. Similar body biasing technique using the intermediate voltages is utilized for lowering the process variations of the temperature compensator

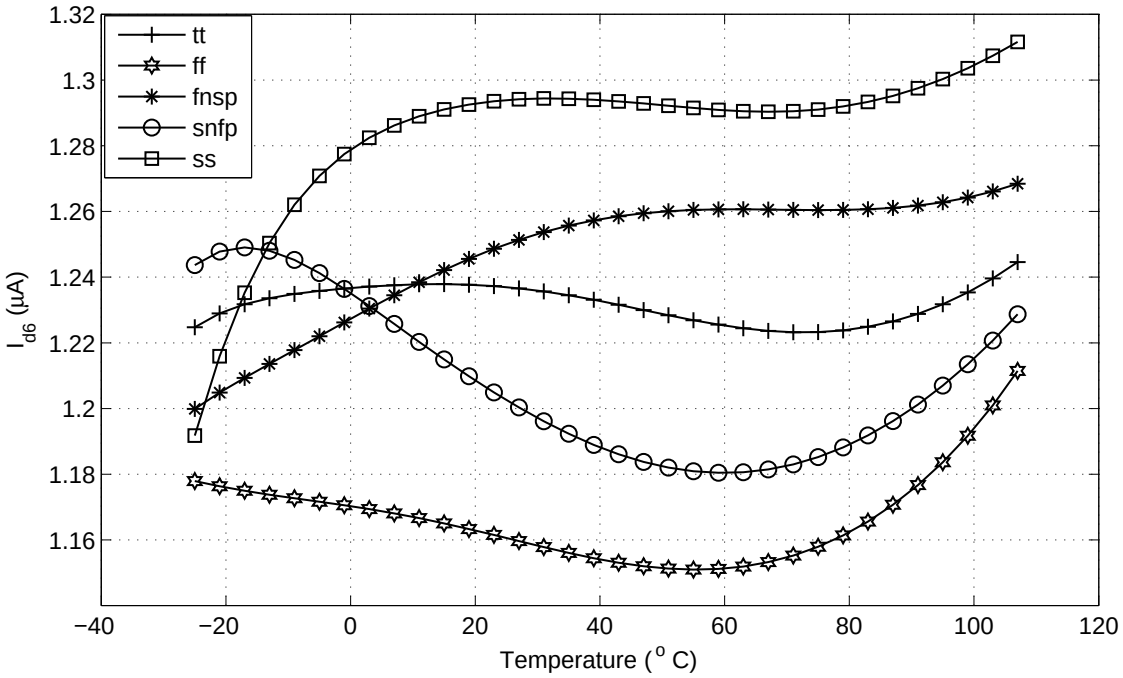

Figure 4.6: Post-layout simulation showing the response of I_{d6} with temperature for different process corners.

also shown in Fig. 4.3.

It may not be possible to minimize the process variations completely by using these intermediate voltages, as the generated voltage may not be the exact voltage to do so. Nevertheless, without requiring any external mechanism, the process variations can certainly be put within limits by using the suggested technique. The V_{th} change in device M_6 alone is investigated for two extreme corners i.e. ff and ss. It is observed that the threshold voltage reduction for ss corner is 20 mV higher compared to ff corner when body biasing compensation is used. Similar phenomenon can be expected from other devices, which are being sourced by body compensation. Further, the combined effects of all the devices M_{5-11} after body bias compensation, have suppressed the current variation by at least 15%.

4.3.3 Results of CCR

The proposed CCR circuit is implemented using UMC 65 nm RF CMOS technology. For resistor R_1, though an external component would be more appropriate to get minimum process variation, nevertheless, a high ρ on-chip resistor is considered here with a temperature coefficient of $-367ppm/^oC$. The current through M_6, I_{d6}, is the final PVT compensated current that is used as a reference for other blocks. The post-layout simulations are given in Fig. 4.6 and 4.7 showing the response for temperature and the supply variations respectively for different process corners. The tt (typical-typical) corner

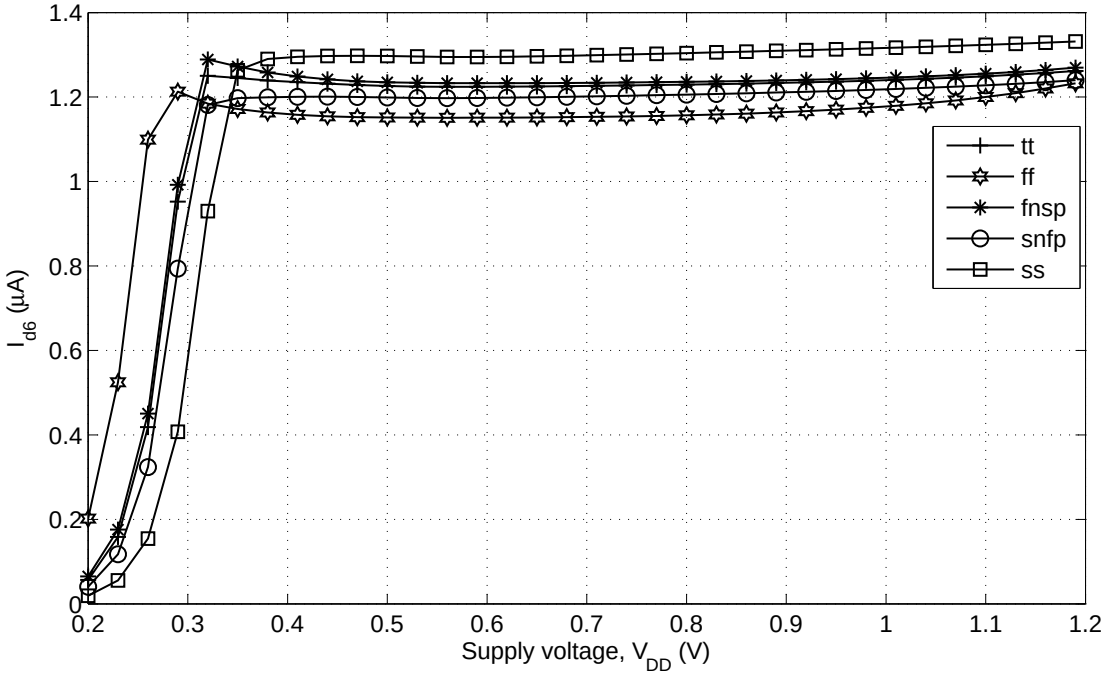

Figure 4.7: Post-layout simulation showing the response of I_{d6} with supply voltage variation for different process corners.

exhibits the minimum temperature variation compared to other corners with a maximum percentage deviation around $\pm 1\%$ from a lowest possible supply voltage of 0.4 V for the temperature range of -20^oC to $+110^oC$. With the same range of temperature and by considering all the five corners, the maximum percentage deviation is found to be around $\pm 6.4\%$. As regards supply variations, the tt corner case starts saturating from a voltage as low as 0.32 V and shows maximum percentage deviation of $\pm 1.6\%$ for a voltage range of 0.32 V to 1.2 V. When all the other corners are considered, it is observed that the ss corner starts saturating from a voltage of 0.37 V. Hence it may be concluded that the proposed CCR can be operated satisfactorily with a lowest possible voltage of around 0.4 V, which will be used as a basis for the error generator circuit which is discussed in Section 4.4.1. All the corners start deviating beyond the given temperature range.

The CCR results obtained are compared with the results from recent contributions and are shown in Table 4.1. Although the proposed CCR does not yield the best results against temperature and supply variations individually, nevertheless it achieves moderate performances with a V_{DD} as low as 0.4 V that is the minimum among all other contributions (Table 4.1). In addition, it shows robust performance against supply variations that is quite close to other results in spite of its implementation in an advanced technology node like 65 nm that seriously suffers from second order effects such as

Table 4.1: Performance comparison with other Constant Current References

	Tech. (nm)	Min.V_{DD} (V)	P_d@min. $V_{DD}(\mu W)$	Temp. range(^oC) From,To	TC ($ppm/^oC$)	Supply Var.(%/V)	Est. Area
This work	65	0.4	1	-20,110	118	±1.6	$0.012mm^2$
[109]*	350	1.8	1	0,80	520	0.2	$0.015mm^2$
[110]	180	1.2	0.6¶	-40,120	119	0.69	N/R
[111]*	180	1.8	18¶	-40,125	4.36	N/R	$0.008mm^2$
[112]	500	4.5	72¶	-45,125	13	±1.2	N/R
[114]	180	1.5	38.7	20,130	16.5	N/R	$130\mu m^2$
[115]*	180	1.2	23pW	0,80	780	0.58	$38.2K\mu m^2$

N/R: Not reported; P_d: Power dissipation; TC: Temperature Coefficient; * Measured results;¶Values are not explicitly given rather inferred from the given results.

channel length modulation. The area required is also quite moderate although all the devices are operated in weak inversion region.

4.4 PVT compensated LNA

The core topology is a conventional cascode LNA; however, the gate of the core device is driven by an error monitored voltage that facilitates maintaining a stable g_m of the amplifier. The stability of g_m is achieved by maintaining a constant LNA current. In-order to do so, the LNA current is sensed, the difference between I_{CCR} and I_{LNA} is evaluated, and the difference current is then used to correct the drifted value of I_{LNA}. The complete circuit of the proposed mechanism is shown in Fig. 4.8. The various components are explained as follows.

4.4.1 Error generator

The proposed compensation technique relies on sensing and comparing the LNA current with a constant-current reference. The LNA current can be traced either by sensing any intermediate node voltages along the cascode path of the LNA or by inserting an extra device at the top [127] for mirroring the amplifier current. Alternatively, to isolate the LNA completely, one can also use replica of the core device. However, the behavior of the currents in the core device and its replica must be guaranteed to be the same by using other accessories.

The error generator circuit with inputs from CCR and LNA is shown in Fig. 4.8. The transistors $M_{19,20}$ are used to mirror the CCR current while the device M_{21} acts as a replica of the LNA's core device M_1. The rest of the devices M_{23}, M_{24} and M_{23C}, M_{24C} help in couple LNA current to the CCR

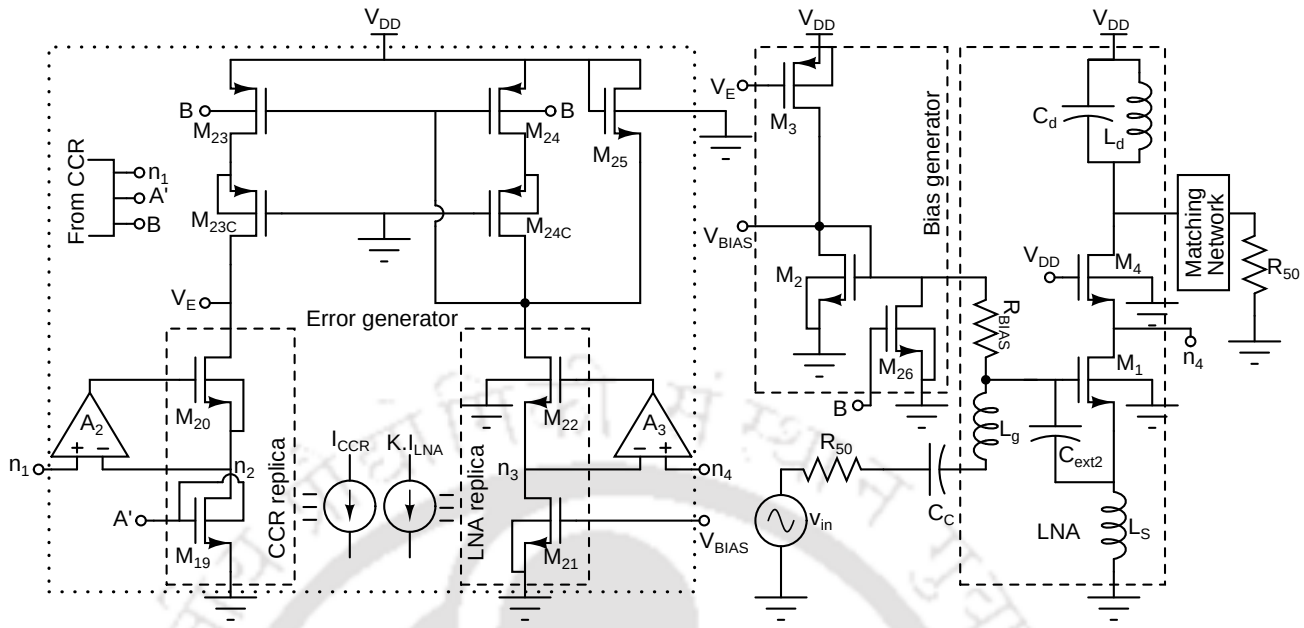

Figure 4.8: The complete circuit diagram of the compensated LNA showing its main constituents: error generator and bias generator.

current and produce the respective error voltage, V_E. Thus, the error generator consists not only of a replica of CCR but also that of the LNA core element. In-order to maintain the strong correlation between the original and its replica currents in both CCR and LNA, assisting devices M_{20} and M_{22} are used along with the additional amplifiers A_2 and A_3. The amplifiers A_2 and A_3 are similar to A_1: compare drain voltages of M_6, M_{19} and M_1, M_{21} and set respective gate voltages of M_{20} and M_{22} devices. As a result, in addition to the gate voltage, drain voltages are also made equal for the core and its replicas thereby maintaining similar current across both the circuits. The scaling factor K in (K.I_{LNA}) can be achieved in two steps with appropriate choice of the relative sizes of M_1 and M_{21}, and M_{23} and M_{24}. Thus the current required for comparison can be made very small and therefore compensation circuits do not unnecessarily dictate the power budget of the overall amplifier.

The error generation circuits which use replicas of the core device has the advantage that the LNA is almost completely isolated from the error and the bias generation circuits. Hence these circuits do not severely influence the LNA performance. Moreover, unlike [127], it does not constrain the output swing of the LNA. Recently, we have come across similar type of technique [128] which is however applied for stabilizing power amplifier. One may readily use this technique for stabilizing LNA also.

Table 4.2: Values of the core LNA elements

Elements	$L_g(nH)$	$L_s(nH)$	$L_d(nH)$	$C_{ext2}(fF)$
Values	17.4	1	8.7	165
Elements	$C_d(fF)$	$R_{BIAS}(K\Omega)$	$(\frac{W}{L})_1$	$(\frac{W}{L})_4$
Values	585	200	$\frac{40\mu m}{60nm}$	$\frac{128\mu m}{60nm}$

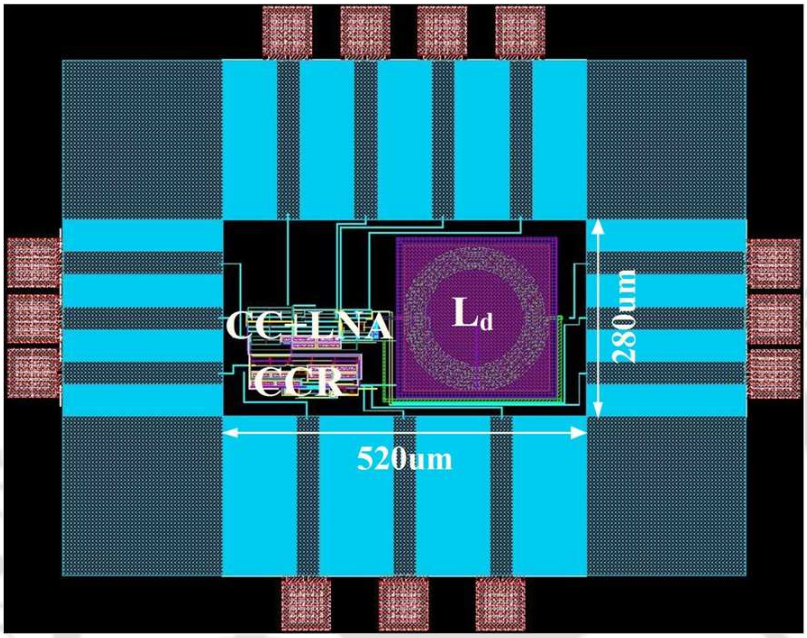

Figure 4.9: The layout prototype of the compensated LNA. The CC indicates the compensating circuits which include error and bias generators.

4.4.2 Bias generation

The error voltage generated, V_E, is next fed to a PMOS device M_3 which sources the diode connected NMOS, M_2, to produce the required bias voltage, V_{BIAS}. The feedback mechanism was illustrated in Fig. 4.2: any increment in I_{LNA} results in increasing the error voltage, V_E, which in turn, reduces the current through M_2. As a result V_{BIAS} is reduced thereby keeping I_{LNA} to its original value. A similar type of negative feedback phenomenon occurs whenever there is a reduction in LNA current due to PVT variations. The cascade connection of error and bias generator circuits along with a feedback appears as if it could introduce stability issues. However, the design is stable and the reason for stability and its analysis is given in Appendix B.

The error generation and the bias generation circuits, in turn, introduce their own errors which make the overall circuit little susceptible to supply variations. To nullify these effects, extra transistors M_{25} and M_{26} are used whose currents are directly dependent on supply voltage, V_{DD}. These transistors

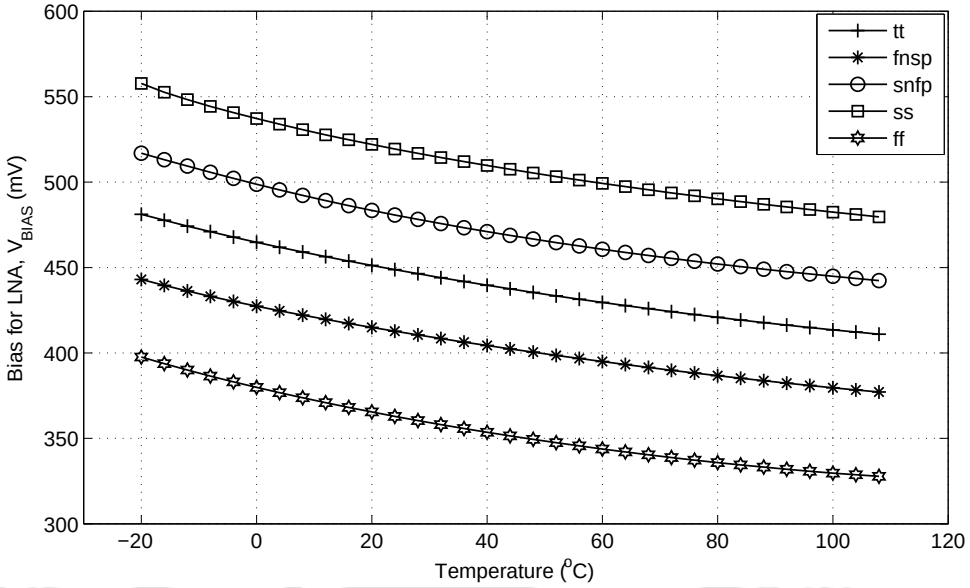

Figure 4.10: The generated V_{BIAS} for nullifying PVT variations of the LNA.

are sized such that they counter the errors introduced by the error generation and the bias generation circuits.

4.4.3 Design and results of the compensated LNA

The complete circuit shown in Fig. 4.8 with the CCR shown in Fig. 4.3 is implemented using UMC 65nm RF CMOS technology. The LNA has a conventional cascode topology with its core transistor M_1 using an extra capacitor [73], C_{ext2}, to reduce the power consumption. The source inductor, L_s, of value 1nH, is considered to be implemented by a bond-wire with a quality factor of 50. The gate inductor, L_g, with a required value of 17.4 nH, turns out to be large for implementing on-chip and therefore an external inductor is considered with a quality factor of 50. The load tank circuit uses on-chip elements for both capacitor and inductor. The capacitors C_{ext2} and C_d are realized by on-chip MOM capacitances from the UMC foundry while an external coupling capacitor is assumed for C_c. Assuming the core LNA g_m value to be around 10mS with a V_{gs} of around 0.45V, values of L_g and C_{ext2} can be related through equations 4.9 and 4.10 [73].

$$Z_{in} = s(L_g + L_s) + \frac{1}{s(C_{ext2} + C_{gs1})} + \frac{g_m L_s}{(C_{gs1} + C_{ext2})} \tag{4.9}$$

$$\omega_0 = \frac{1}{\sqrt{(L_s + L_g)(C_{ext2} + C_{gs1})}} \tag{4.10}$$

The final elemental values of the core LNA is given in Table. 4.2. With these values, an external

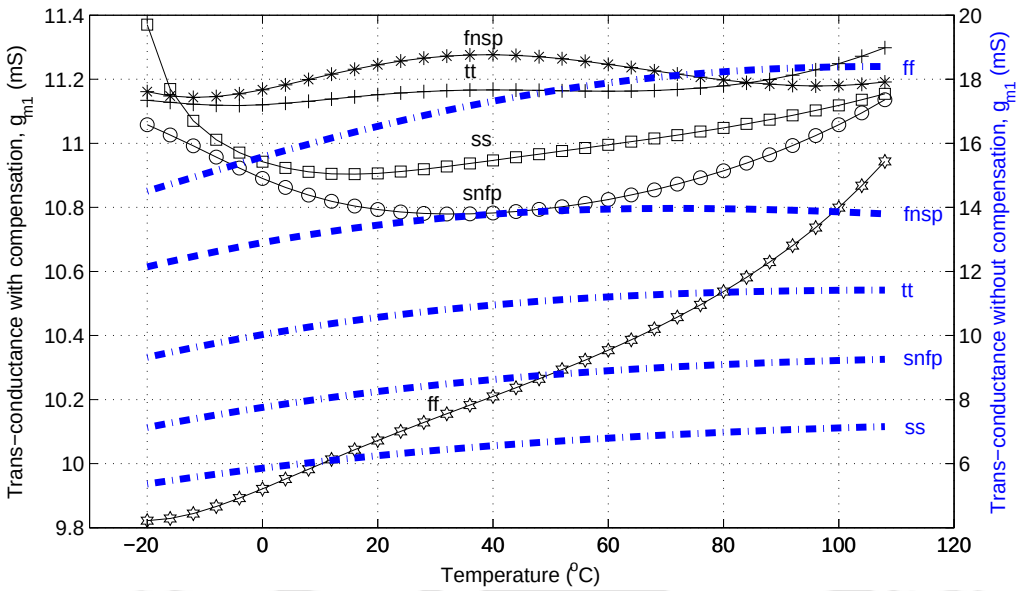

Figure 4.11: Transconductance response of the core LNA M_1 plotted w.r.t temperature variation for five different corners after post-layout simulation.

matching network is used to match the LNA output load to a 50 Ω load resistance R_{50}. In addition, an external resistor R_{BIAS} is used to avoid any noise coupling from the bias circuits. Quite a large device size is required for the devices M_{24}, M_{23C}, M_{24C} and M_3 in order that a small voltage is dropped across it. An optimization process is carried out in the simulator to determine the appropriate sizes for devices in the CCR and the error and the bias generation circuits. The complete layout of the overall PVT compensated LNA is given in Fig. 4.9. For analysis, process variability in RLC components is not considered with an assumption that these can be easily calibrated post-fabrication.

The post layout simulation with RLCK parasitic extraction is carried out to verify the functionality of the proposed technique for different process corners. The generated bias voltage, V_{BIAS}, for nullifying the PVT variation, is shown in Fig. 4.10. It is observed that the generated V_{BIAS} for slow NMOS is higher as compared to that for fast NMOS. This is true for any diode connected device like M_{20}; however, the exact desired voltages are generated only through the proposed scheme. The resulting V_{BIAS}, shown in Fig. 4.10, changes by over 230 mV between the two extreme operating conditions: from -20^oC, ss to $+110^oC$, ff. In contrast, conventional biasing scheme shown in Fig. 4.1 also uses diode connected NMOS for V_{BIAS} generation, only undergoes a change of 124 mV between these two extremes which is clearly inadequate to counteract the resulting variations.

The comparison between the g_m of the core LNA device, M_1, using the proposed and the con-

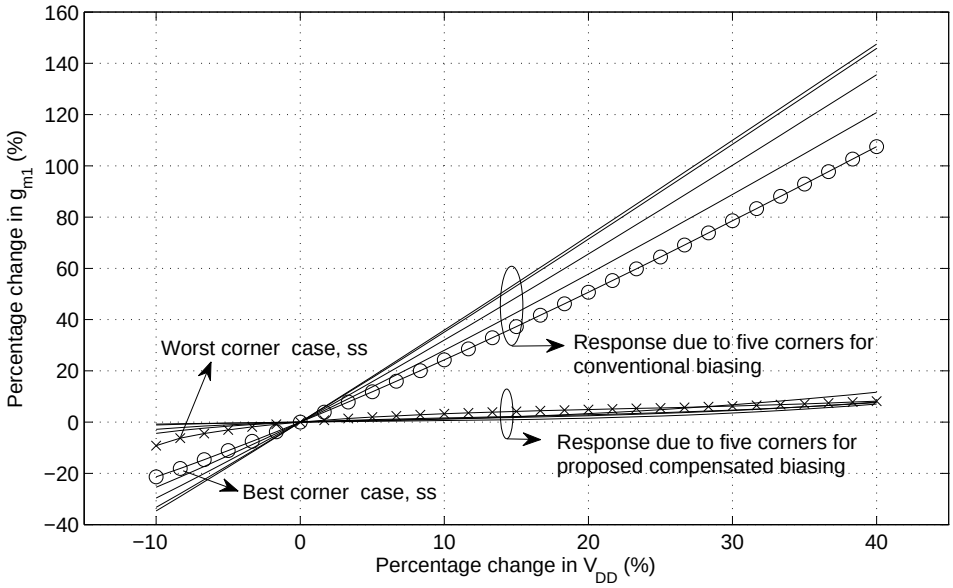

Figure 4.12: Transconductance response of the core LNA M_1 plotted w.r.t supply variation for five different corners after post-layout simulation.

ventional biasing schemes are shown in Fig. 4.11 for different process corners. The dashed blue lines indicate the response of the conventional LNA while the black markered lines show the response of the proposed technique. It is observed that for the conventional biasing technique the transconductance, g_{m1}, shows large variation ranging from 5.4 mS to 18.4 mS for conditions from -20^oC, ss to $+110^oC$, ff as shown in Fig. 4.11. However, with the proposed compensation, the g_{m1} coursed only from 9.8 mS to 11.37 mS for the same range. Thus the proposed technique shows a 8x improvement in-terms of the maximum percentage deviation as compared to the conventional scheme for the same set of conditions. Moreover, with the exception of the ff corner, the remaining four corners exhibit a maximum percentage change of only $\pm 2.6\%$ for conditions ranging from -20^oC, ss to $+110^oC$, snfp. The g_m reduction for the ff corner compared to other corners may be attributed to the inclusion of additional devices such as M_{25} and M_{26}. In addition, CCR itself produced lower current for the ff corner.

The change in g_{m1} due to supply variations for both the conventional and the proposed biasing techniques is given in Fig. 4.12. The response is plotted for a temperature of 27^oC with 0.6 V being the reference value. The results of five corners are normalized with respect to their trans-conductances at a supply voltage of 0.6 V and the deviations are measured with respect to that reference point. It can be observed that the proposed technique offers a good control with ss being the worst case corner giving the maximum variation of $\pm 6.15\%$ for $V_{DD} \pm 10\%$. On the other hand, the conventional

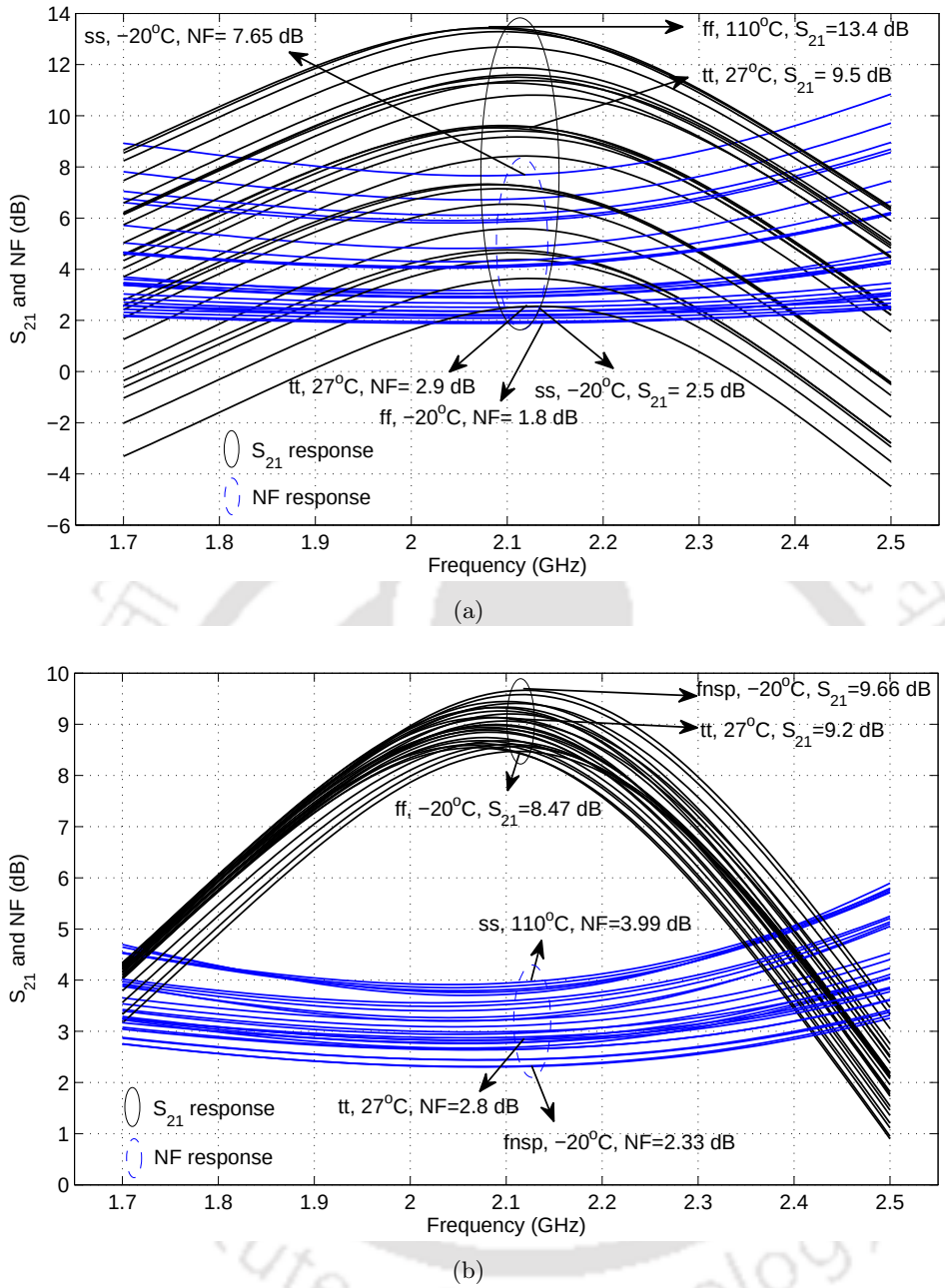

Figure 4.13: S-parameter analysis highlighting extreme values of S_{21} and NF (a) S_{21} and NF response due to conventional biasing. (b) S_{21} and NF response due to the proposed compensation technique.

technique of Fig. 4.1 shows a strong dependency on supply variation with ss being the best case with a minimum variation of $\pm 22.5\%$ for a supply variation of $V_{DD} \pm 10\%$. It is clear that in a conventional biasing scheme (Fig. 4.1) the supply variation has a strong influence on bias generation since the value of R_B remains constant irrespective of the variations in V_{DD}. On the other hand in the proposed case, g_{m1} is constant up to $V_{DD} + 40\%$ but starts increasing beyond this value due to the limitations

Table 4.3: Comparison between the S-parameter and NF responses of the conventional and proposed biasing schemes for corner and temperature variations.

LNA parameters	Maximum and minimum value for CBT*			Maximum and minimum value for PBT*		
	Corner,^oC,dB	nom$^+$(dB)	Δ^{**}(dB)	Corner,^oC,dB	nom (dB)$^+$	Δ^{**}(dB)
S_{21}	ff,110,13.4 ss,-20,2.54	9.5	+3.9 -6.9	fnsp,-20,9.66 ff,-20,8.47	9.26	+0.4 -0.79
S_{11}	ff,110,-18 snfp,10,-48	-28	+10 -20	ff,110,-23.5 ss,-20,-35.4	-26.8	+3.3 -8.6
S_{12}	ff,-20,-34.7 ss,-20,-40.7	-37.3	+2.6 -3.34	ff,-20,-34.3 ss,110,-37.3	-36	+1.7 -1.3
S_{22}	ss,-20,-28.3 snfp,110,-40.9	-31.8	+3.5 -9.1	ff,110,-25.3 ss,10,-36.8	-33	+7.7 -3.8
NF	ss,-20,7.6 ff,-20,1.88	2.9	+4.7 -1.02	ss,-20,3.94 fnsp,-20,2.3	2.82	+1.09 -0.52

* CBT and PBT indicates conventional and proposed biasing techniques respectively. $^{**}\Delta$ indicates a change, maximum or minimum value from nominal. $^+$nom indicates response of tt corner at 27^oC.

imposed by the error generation circuit.

The S-parameter analysis of the LNA is carried out for temperature ranging from -20 to 110^oC for all the five possible process corners. The performance comparison between the conventional and the proposed techniques vis-a-vis S_{21} and NF are shown in Fig. 4.13. The resulted extreme values due to respective operating conditions are highlighted in Fig. 4.13. The response of the conventional scheme (Fig. 4.13(a)) exhibits a drastic variation when the circuit undergoes process and temperature variations with S_{21} deviating from 2.54 dB to 13.4 dB when the conditions change from ss,-20^oC to ff,$+100^oC$. The resulting noise figure, NF, also shows a significant variation from 1.88 dB to 7.6 dB for the same set of conditions. In contrast, the response of LNA that uses the proposed compensation technique shown in Fig. 4.13(b) results in a maximum percentage change of only $\pm 6.5\%$ for S_{21} with a maximum of 1 dB noise figure deviation from its nominal value. Hence for S_{21}, the proposed scheme shows around 8x reduction in percentage deviation compared to conventional biasing scheme. The four S-parameters and the noise figure in these two techniques are compared in Table 4.3. Thus, it is evident from Fig. 4.13 and Table 4.3 that the proposed scheme effectively suppresses the consequences of PVT variations resulting in a more reliable LNA.

Finally, monte carlo simulations which include both process and mismatch statistical variables for 1000 samples are carried out with post-layout extracted parasitics. The distribution of S_{21}, one of the important parameters, is shown in Fig. 4.14 for both the conventional (Fig. 4.1) and the proposed

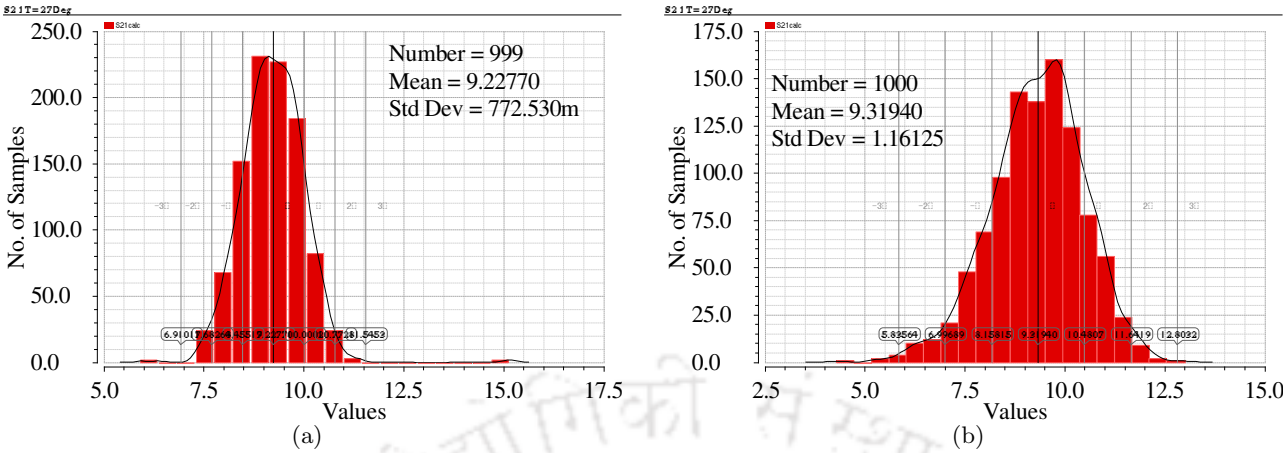

Figure 4.14: Monte carlo analysis for both process and mismatch statistical variables (a) S_{21} distribution of the compensated LNA (b) S_{21} distribution of the conventionally biased LNA.

technique (Fig. 4.8) at a room temperature of 27^oC. For the proposed technique, one sample which falls far away from the mean value is discarded for a fair estimation of the distribution for the other 999 samples. From Fig. 4.14(a), it is clear that the proposed biasing technique (henceforth referred to as "PBT") has a narrower spread with a standard deviation (σ) of 0.77 dB that is 34% smaller as compared to that in the conventional biasing technique (henceforth referred to as "CBT") shown in Fig. 4.14(b). As PBT gives the minimum σ for the two techniques, the maximum percentage change for $\pm 1\sigma$ of PBT may be considered as the yield for both the techniques in order to validate the performance comparison in monte carlo analysis. Approximately 71% of the total samples from PBT fall within $\pm 1\sigma$ of the mean value which is equivalent to a maximum percentage change of $\pm 8.3\%$ from its mean value. Overall, 95% of the total samples are within $\pm 2\sigma$ value. Conversely, only 51% of the total samples from CBT technique (Fig. 4.14(b)) are within a maximum percentage change of $\pm 8.3\%$ from its mean value. As a result, 20% increase in yield can be attributed to the effectiveness of the proposed compensation technique. The other important LNA parameter is the noise figure (not shown here) which also shows similar distributions.

Table 4.4: Performance summary and comparison

	Freq (GHz)	Techno -logy (nm)	V_{DD} (V)	P_d (mW)	Temp. range (^oC)	Area (mm^2)	S_{21} Max. deviation					
							nom. value (dB)	Temp. Max.Var. for tt corner (dB, $ppm/^oC$, %)	Five Corner Max.Var. @ 27^oC(dB, %)	Temp. + five Corners Max.Var. (dB, %)	σ/μ (%)	Yield improve-ment (%)
This work	2.14	65	0.6	0.402♠	-20 to 110	0.14	9.2	-0.35,415, ±2.6	-0.66, ±5	-0.79, ±6.4	8.34	20 for S_{21} ±8.3%
CBT	2.14	65	0.6	0.346	-20 to 110	0.08	9.5	-0.99,931, ±6	-5.5, ±47.2	-6.9, ±56.8	12.45	-
[97]	2.34	180	N/R	N/R	-40 to 80	N/R	4.5	0.14,N/R, +3¶	1.31, +28.9¶	1.9, +42¶	13.48¶	N/R
[100]	3.2	65	N/R	7.69	0 to 80¶	0.4	9.5	N/R,1554,* N/R	N/R, +4.5	N/R	2.19*	50 for Gain±5%
[127]	1.8	250	N/R				15	N/R				18 for Gain±20%
[129]	1.85	180	N/R			1.6	16.8	N/R				13 for¶ Gain±7.7%

♠ It includes power from compensating accessories and CCR. * Measured results. N/R:Not reported.
¶ Values are not explicitly given rather inferred from the given results.

In Table 4.4, the S_{21} results are compared with results from related works in recent literature. To demonstrate the efficacy of the proposed technique, results obtained using conventional biasing scheme (Fig. 4.1) are also shown in the same Table 4.4. The results suggest that the conventional biasing scheme is highly unreliable for implementing in sub-nanometer technologies. The deviations are minimized by almost 8 times with the help of the proposed technique when the circuit undergoes both process corner and temperature variations. The technique given in [97] shows poor performance for process variations and would degrade further if it is implemented in advanced technologies, say 65 nm. Further, the proposed work shows minimum 3 times improvement for both temperature and corner despite considering only upper bound for [97] due to lack of available data. The technique in [100] shows a greater control over process variations, however, the temperature variations achieved is inferior as compared to the proposed technique. In summary, the proposed method shows reasonably good performance when both process and temperature variations are considered as compared to all other contributions, and in addition, it gives the most robust performance among all in respect of temperature variations. The comparison with [100] in terms of σ/μ ratio and yield as given in Table. 4.4 does not truly reflect the effectiveness of proposed method because of the large difference in the consideration of number of samples. Moreover, it is interesting to note that the power consumption in [100] is approximately 19 times higher as compared to that of the proposed method including the power consumption in the biasing circuit. On the other hand, the noise performance achieved may not be optimum for some applications like LTE. Hence, a trade-off between power and noise figure is required depending on the system level requirements of the certain receiver.

4.5 LNA for LTE receiver

An LTE receiver can tolerate a maximum NF value of 2.2 dB for an LNA to satisfy the overall sensitivity requirement as deduced from the system level specifications in Section 2.4 of Chapter 2. Since the NF obtained in the above design exceeds the limit, the current of the core device must be scaled up to improve the noise performance of the amplifier and thereby to satisfy the LTE requirement. Hence these circuits are re-designed and simulations are carried out with post-layout extracted parasitics.

The prime parameters of the LNA, S21 and NF responses for different process corners are given in Fig. 4.15. The noise figure response highlights the LNA's suitability for an LTE receiver. The typical-

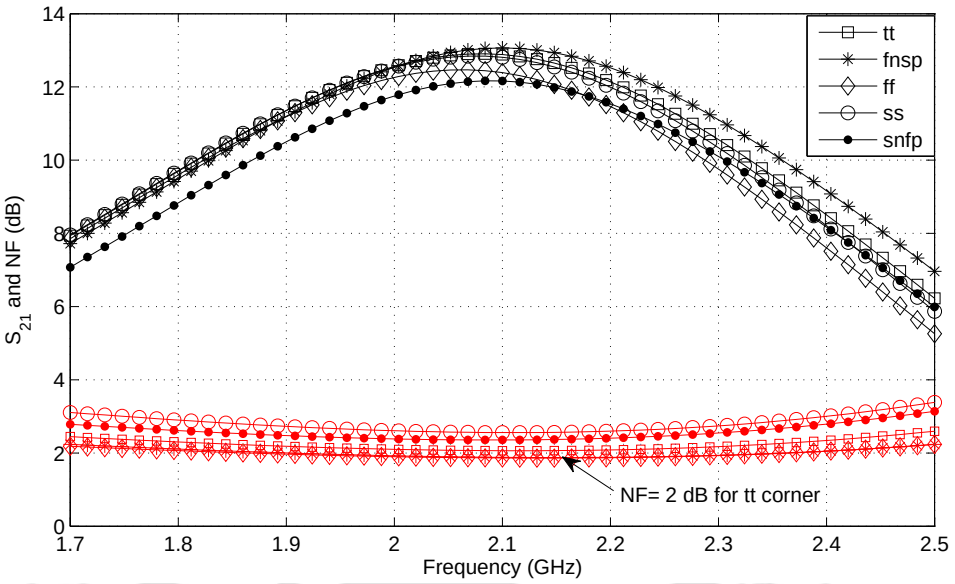

Figure 4.15: The S21 and NF post-layout simulation response of the low-power LNA for different process corners.

Table 4.5: Performance comparison with other low power LNAs

Specifications	This work**	[83]*	[130]*	[44]	[85]	[49]*	[81]*	[80]*	[131]*
Technology (nm)	65	180	130	130	130	90	180	180	130
Frequency (GHz)	2.14	2.4	2.4	2.4	2.4	2.4	2.4	1	3
Power (μW)	706	1100	60	240	600	684	945	260	400
S21 or Gain (dB)	12.4	20	13.1	18.2	25.2	9.7	21.4	13.6	9.1
NF (dB)	2	5.2	5.3	4.54	3.8	4.36	5.2	4.6	4.7
IIP3 (dBm)	-4.8$^{\diamond}$	-11	-12.2	-2	-10.8	-4	-11	+7.2	-11
FOM	34.7	21.3	43.4	44.1	29.9	30.6	22.9	47.4	28.4
Area (μmXμm)	476X 254	N/R	N/R	N/R	N/R	1080X 845	500X 360	890X 780	N/R

* Measured results.** Post-layout simulation results of tt corner.$^{\diamond}$IIP3 is assumed 10 dB higher than P_{1dB}. N/R:Not reported.

typical (tt) corner exhibits an NF of around 2 dB for frequencies from 2 to 2.2 GHz which is below the noise threshold deduced from the requirements of the complete receiver. The devices associated with slow NMOS corners (ss, snfp), however, little overshoot the 2.2 dB requirement. Out of five corners, three cases function within the acceptable NF levels. The tt corner consumes a total power of 706 μW which includes dissipation from both the core circuitry and the biasing elements. Due to the usage of compensation circuits, the maximum percentage deviation of S21 among different process corners

from its nominal value (tt case) is less than ±3.5% which corresponds to a NF change of 0.5 dB. The resulting performance is compared with other microwatt powered, narrow-band LNAs and the results are given in Table 4.5. The FOM (Figure of Merit) described in [131] is used for an effective comparison with other state of the art LNAs. The FOM of [131] takes into account performances such as gain, linearity, NF, and biasing power condition, in addition to the operating frequency and is described in Chapter 3. It can be observed that the presented amplifier offers the lowest noise figure among the microwatt operated low-noise amplifiers. On the other hand, the improved linearity performance in [80] resulted in the highest FOM. The lowest power in [130] has also achieved a greater value of FOM. Further, a moderately large gain along with a better linearity performance has fetched [44] a larger FOM. However, in spite of their larger figure of merit these are not appropriate for LTE receivers as they exhibit higher noise figure that certainly fails to meet the minimum sensitivity requirement. In comparison to all the contributions listed in Table 4.5, the presented LNA offers the best noise figure with a relatively moderate FOM.

4.6 Conclusion

This paper presents a new compensation technique to tackle PVT variations of near sub-threshold low voltage LNAs. The technique is based on a comparison of the current of LNA to that of a constant current source and paves the way for achieving low voltage reliable LNAs. It has also demonstrated a low voltage constant current reference that can work with a minimum voltage of 0.4 V. The compensated LNA operates with a voltage of 0.6 V. The overall circuit consumes a total power of $402\mu W$. The proposed technique can be extended to design low voltage constant g_m or constant current sources in circuits such as OTAs, filters etc. Interestingly, the approach does not necessitate insertion of sensing devices in the core circuitry and this makes voltage scaling a feasible option. In addition, the compensating circuits do not interfere in normal operation of the amplifier and hence do not hamper the overall performance. In the final implementation, the LNA current is scaled according to the performance requirement of the LTE receiver.

5

Gain enhancement of LNA using current-reuse technique

Contents

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5.1 Introduction

The common-source LNA with source degeneration offers the best noise performance in general. However as discussed in earlier chapters, direct current scaling to reduce the power consumption would lead to performance degradation. In particular, it lowers the effective transconductance (G_m) which in turn deteriorates the gain and may further deteriorate the noise performance of an amplifier. Moreover, insertion of an extra capacitor (C_{ext}) between gate-source capacitance of the core device aids in avoiding an additional power consumption [73]. However, that reduce the transition frequency (ω_t) due to which again gain of the amplifier gets reduced. The usage of an extra capacitor (C_{ext}) is necessary to bring both L_s and L_g in the possible implementation limit and become inevitable whenever the intended low-power LNA is implemented in an advanced CMOS technological node.

Alternatively, instead of the capacitor C_{ext} connected between gate and source of the core device, an L-match consists of an inductor (L_g) and capacitor (C_g) can be used for the input match as shown in Fig. 5.1a. Additional benefits can be obtained if fraction of C_g is replaced by an active device. Accordingly, an active device, NMOS, as a replacement to a fraction of C_g is shown in Fig. 5.1b.

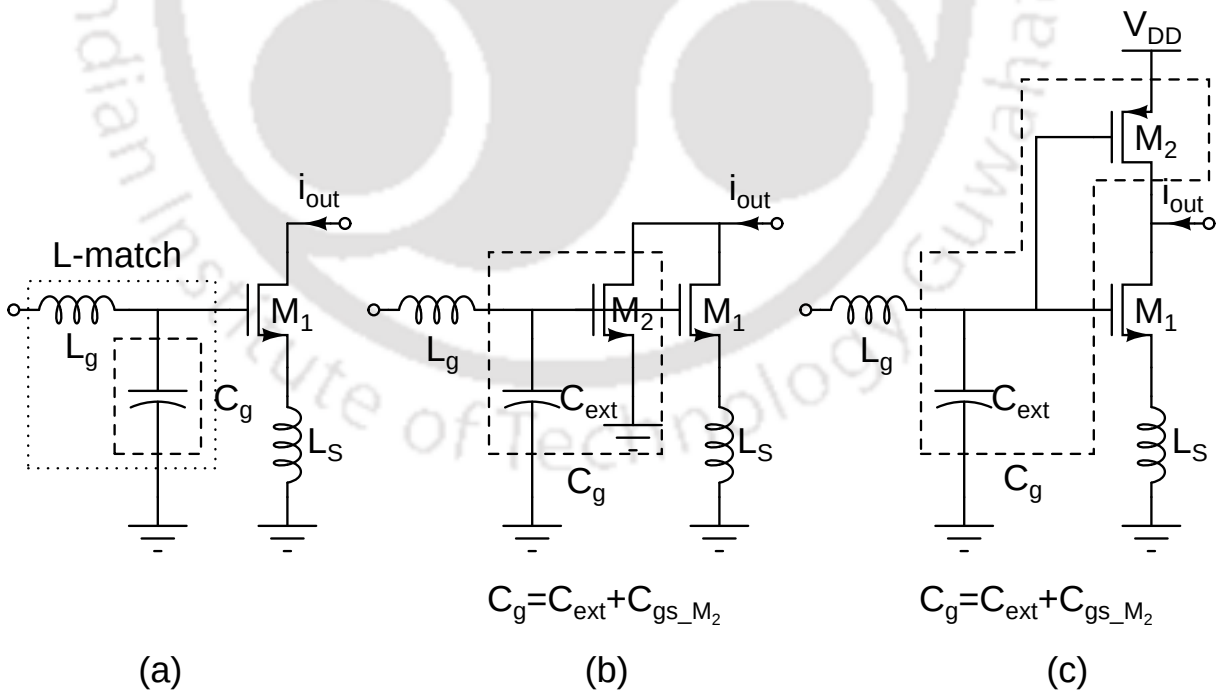

Figure 5.1: (a) Usage of L-match for the input match. (b) Partial value of C_g is realized by C_{gs} of NMOS M_2. (c) Devices are connected in current-reuse technique where partial value of C_g is realized by C_{gs} of PMOS M_2.

The output current, i_{out}, comprises currents from core transistor M_1 and also from the additional transistor M_2. The circuit in Fig. 5.1b implies that it needs an additional supply of current if part of C_g has to be realized by another NMOS transistor. However, the functionality of M_2 transistor can also be implemented by a PMOS device. Consequently, it results in the current-reuse technique if PMOS is used and this avoids any additional requirement of current.

Accordingly, a PMOS replacement to an NMOS device is shown in Fig. 5.1c. In addition to its contribution to input match, the PMOS device, M_2, provides extra g_m to the LNA. Hence, an enhanced G_m is expected for the latter circuit which not only would improve the gain but also would add a little improvement in noise performance of the amplifier.

There exist other current-reuse techniques for LNAs [132–135] similar to the one suggested in this chapter. The techniques in [132, 133] would require multiple inductors that in turn increases the cost and the area of an amplifier. On the other hand, the circuit in [134] would need twice the value of the inductance, L_s, at the source terminal compared to the value used in the suggested LNA. The technique in [135] consumes larger voltage headroom compared to the suggested LNA in Fig. 5.1c. Compared to these existing techniques, the suggested topology in Fig. 5.1c would result in a low-power, and low-cost LNA.

5.2 Current-reuse LNA

The complete circuit of a conventional CS degenerated cascode LNA (LNA-1) and the current-reuse LNA (LNA-2) with their equivalent circuits are shown in Fig. 5.2. Fig. 5.2c shows a simplified model for highlighting the input matching network for the circuits in Fig. 5.2a and b. As shown in Fig. 5.2c, at resonance, the current flowing out of the voltage source V_{in} is $I_{in} = V_{in}/(2R_s)$, where R_s is the source resistance. At matched condition, the impedance seen at the input of the transconductance stage should be equal to the complex conjugate of the impedance seen on the other side of the node X, which is equal to $R_s + j\omega_o L_g$. Therefore, the intermediate node voltage, V_x, can be computed as,

$$\begin{aligned} V_x &= I_{in}(R_s - j\omega_o L_g) \\ &= \frac{V_{in}}{2}(1 - j\frac{\omega_o L_g}{R_s}) \\ &= \frac{V_{in}}{2}(1 - jQ_g) \end{aligned} \tag{5.1}$$

where $Q_g = \omega_o L_g/R_s$ is the effective quality factor of the series inductor L_g at the resonance.

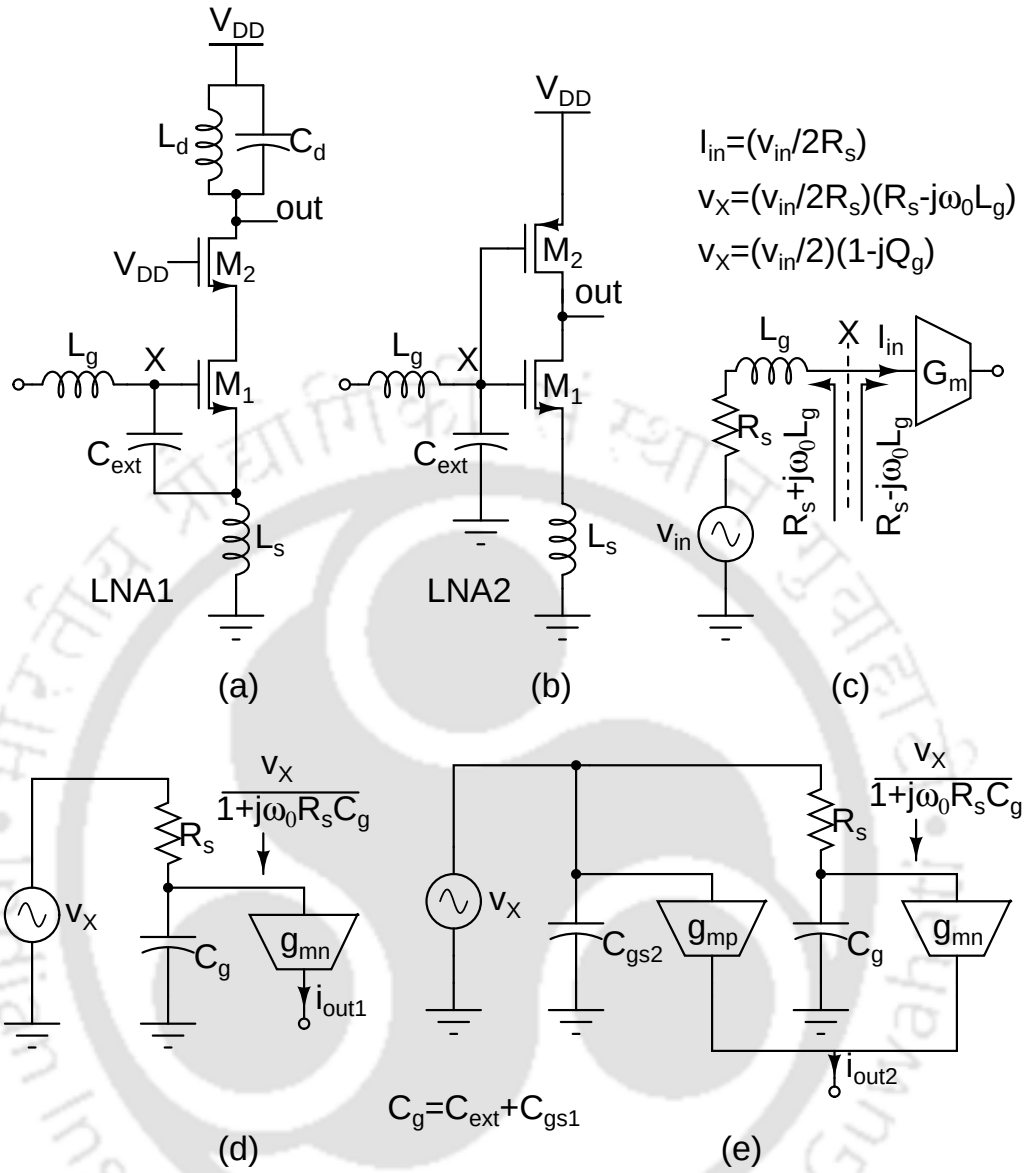

Figure 5.2: Schematics of the two topologies with their equivalent circuits. Equivalent circuits are shown with an assumption that L_s offers relatively negligible impedance in reference to C_{gs} of the MOS device. (a) LNA-1: Schematic of a conventional CS degenerated LNA. Its equivalent circuit is shown in (d). (b) LNA-2: A current-reuse topology with an L-match at the input. Its equivalent circuit is shown in (e). (c) A simplified model of the input matching network.

In Fig. 5.2d and e, the impedance, $\omega_o L_s$, is assumed to be much smaller than the impedance offered by gate-to-source capacitance. The capacitance, C_g, shown includes both C_{gs} of M_1 and the extra capacitance C_{ext}. From the Fig. 5.2d-e, output signal currents $I_{out1,2}$ for each LNA can be computed

as,

$$I_{out1} = \frac{V_x}{1 + j\omega_0 R_s C_g} g_{mn} \tag{5.2}$$

$$I_{out2} = V_x g_{mp} + \frac{V_x}{1 + j\omega_0 R_s C_g} g_{mn} \tag{5.3}$$

where g_{mp}, g_{mn} are the transconductances of the PMOS and the NMOS devices respectively. From (5.2)-(5.3), the effective transconductance ($G_m = \frac{I_{out}}{V_s}$) for the circuits in Fig. 5.2d-e can be written as follows.

$$2G_{m1} = \frac{1 - jQ_g}{1 + j\omega_0 R_s C_g} g_{mn} \tag{5.4}$$

$$2G_{m2} = (1 - jQ_g) g_{mp} + \frac{1 - jQ_g}{1 + j\omega_0 R_s C_g} g_{mn} \tag{5.5}$$

where G_{m1}, and G_{m2} are the effective transconductance of the circuits in Fig. 5.2a, and b respectively.

From (5.4) and (5.5), it can be observed that LNA-1 has the smallest transconductance, G_{m1}, as there is only one device (M_1) that is contributing to the total transconductance. However, a larger G_{meff} is expected for the circuit in Fig. 5.2b (LNA-2) because both the NMOS and the PMOS devices are contributing to the total transconductance. This shows that the suggested current-reuse LNA, shown in Fig. 5.2b, has a more effective transconductance (G_{meff}) compared to that of a conventional cascode CS-LNA.

As regards the noise performance, LNA-2 consists of two devices M_1 and M_2, contributes to the total noise as against a single device M_1 in case of LNA-1. However, noises are masked by a larger value of transconductance in LNA-2 as compared to LNA-1. Hence, a slight noise improvement is expected in case of LNA-2 compared to LNA-1.

5.3 Design and Results

The two LNAs, shown in Fig. 5.2a-b are designed in 65nm CMOS process. The complete circuit of the current-reuse LNA is shown in Fig. 5.3. Unlike in the conventional circuit, the input node in Fig. 5.2b is influenced by the output through an additional path from M_2. Therefore, to reduce the output influence on the input node, a buffer stage consisting of a unity-gain CS (common source) amplifier is added. The buffer stage is realized by the transistor M_3 shown in Fig. 5.3. A CD (common drain) topology can be used instead of a CS stage as a buffer, however, the former circuit requires more power to reduce the signal loss compared to the latter topology.

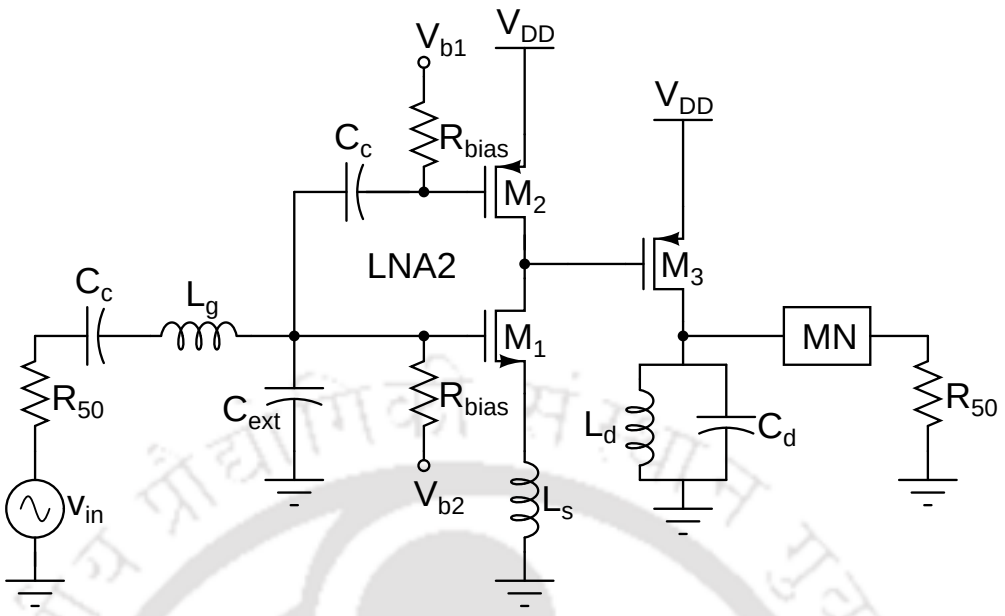

Figure 5.3: The complete circuit of the current-reuse LNA. MN is the matching network used to match the output node to 50 Ω load.

Table 5.1: Designed values for transistors and passive components

Topology	W_1 (μm)	W_{1c} (μm)	W_2 (μm)	W_3 (μm)	L_g (nH)	L_s (nH)	L_d (nH)	C_{ext} (fF)	C_d (pH)	I_{bias} (μA)	Power (μW)
LNA-1	44	64	-	-	16	2	2	260	2.5	571	514
LNA-2	32	-	16	20	16	2	2	200	2.5	423 +151*	516

* The First and second stage carries 423 μA and 151 μA respectively and the power is calculated for V_{DD}=0.9 V.

The designed values of the transistors and the passive elements are given in Table 5.1. The power consumption and the values of the passive elements are maintained same in both the LNA topologies in-order to obtain a fair performance comparison. The LNA-1 carries a current equal to the summation of both the stages in LNA-2. Consequently, LNA-1 and LNA-2 are maintained to operate at same power levels. A tuned tank at the load assumes a bond wire inductor, L_d, along with an on-chip MOM capacitor, C_d. In addition, an external element and a bond wire are assumed for gate (L_g) and source (L_s) inductors respectively both with a Q factor of 50. These are operated with a V_{DD} of 0.9 V and designed for a center frequency of 2.14 GHz.

High Q inductors are selected that are important factors for gate inductor and tank circuit. As discussed in earlier chapters, low Q on-chip inductors at the gate cannot be used for low power designs as the required large value of inductor may severely degrade the noise figure of the amplifier. Further,

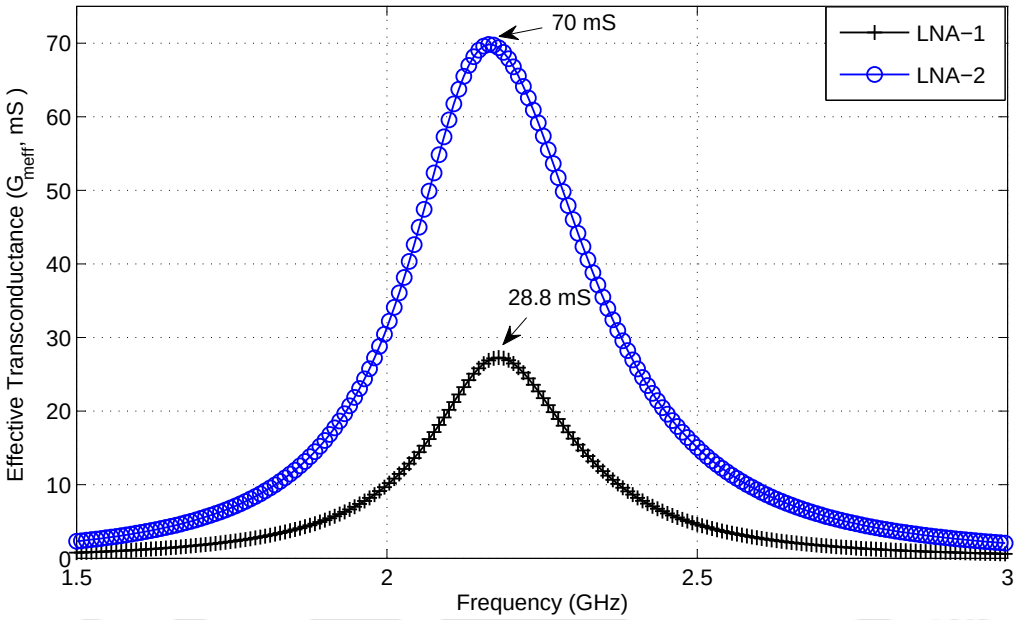

Figure 5.4: Effective transconductances of LNA-1 and LNA-2.

low Q on-chip at L_d would reduce the overall gain and increase the noise figure (NF) particularly in the case of LNA-1. On the other hand, LNA-2 has an advantage compared to LNA-1 that the usage of low Q on-chip for L_d would not affect the overall gain as the total gain is largely decided by the first stage. The required inductor, L_d, can be easily realized by bond-wires as these offers typical inductance per length ratio of 1nH/mm.

The effective transconductance, G_{meff}, for the two instances are shown in Fig. 5.4. It can be observed that LNA-2 achieves more than two times higher value compared to LNA-1. The LNA-2 has benefitted from the extra g_m of the second transistor, M_2. A schematic simulation depicting S_{21} and NF of both the LNAs are compared in Fig. 5.5. LNA-2 offers nearly 7 dB higher S_{21} compared to LNA-1. The gain differences are large because of the differences in their respective transconductances. However, the noise performance does not show a significant improvement even though LNA-2 exhibits larger gain. It is because there are two transistors that contribute to the noise in LNA-2 compared to LNA-1.

The post-layout simulation for LNA-2 is carried out after RCLK extraction and is given in Fig. 5.6. The S_{21} and the obtained NF are 15.8 dB and 1.3 dB respectively. A matching network is used at the output to match a load of 50 Ω for standalone measurement. The obtained S_{11} and S_{22} are -15 dB

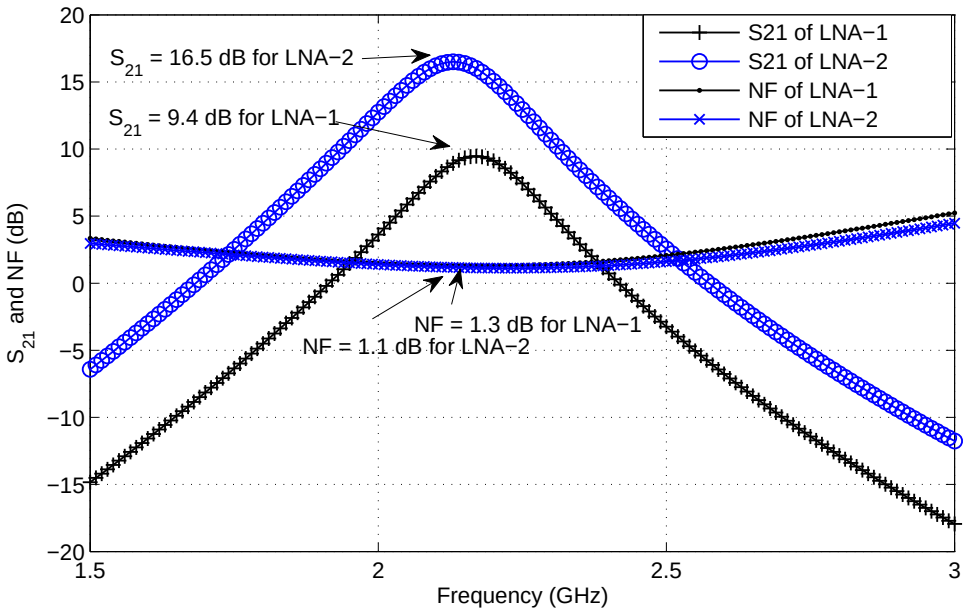

Figure 5.5: S21 and NF performance of the LNA-1 and LNA-2

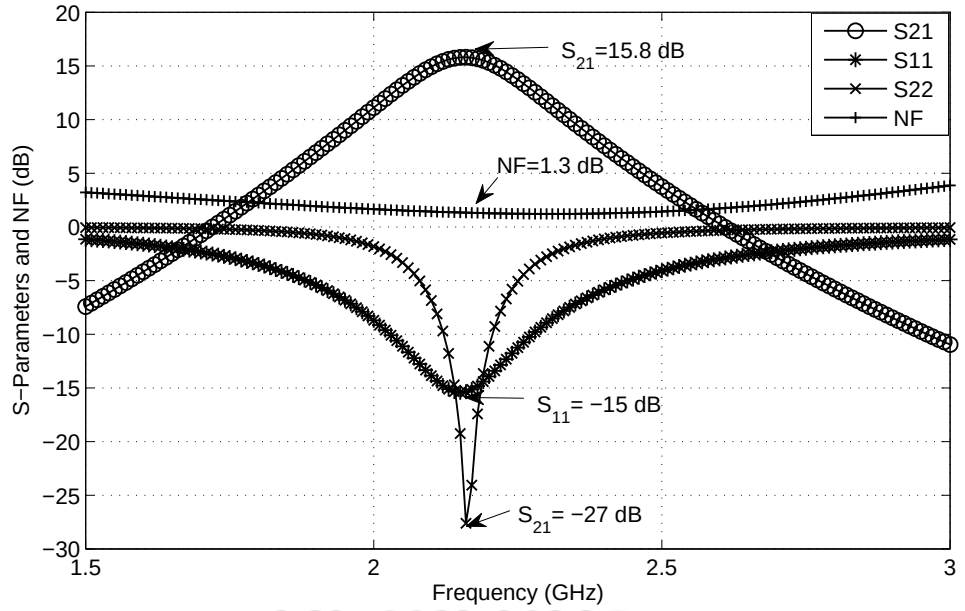

Figure 5.6: Post-layout simulation after RCLK extraction for LNA-2

and -27 dB respectively. Further, a two-tone test is also carried out with a carrier offset of 10 MHz and it resulted in an IIP3 value of -6 dBm.

The performances of the LNA-2 is compared with the state of art narrow band low-power current-reuse LNAs by using the figure of merit (FOM) which is mentioned in equation (3.23) of chapter 3. In addition, other low power LNAs which are having a higher FOM from Table 4.5 of chapter 4 are

Table 5.2: Comparison with other current reuse LNAs and other low power LNAs

Specification	This work**	[132]	[133]	[134]	[135]	[84]	[44]**	[75]	[80]
Technology(nm)	65	180	180	180	180	130	130	90	180
Frequency (GHz)	2.14	5	5.4	2	0.4	2.4	2.4	2.4	1
Power (μW)	380 +135#@	900	2.7 mW	3.8 mW	150	60 μW +1.4 mW&	240	684	260
P_{1dB} (dBm)	-22.8	-13	-15	-15	-25	N/R	-19	-13.5	N/R
Gain or S_{21}(dB)	15.8	9.2	21+	11	20.2	13.1	18.2	9.7	13.6
NF (dB)	1.3	4.5	2.7p	1.8	2.8	5.3	4.54	4.36	4.6
IIP3 (dBm)	-6	-16	-22p	0	-8.1	-12.2	-2	-4	+7.2
FOM	39.6	18.9	10.5	24.7	37.8	16#	44.1	30.6	47.4
Area (μm × μm)	51 ×73.6	860 ×1100	N/R	175 ×50	836 ×836	793 ×793	N/R	1080 ×845	890 ×780

** Post-layout simulation results. @Core and buffer consume 380 and 135 μW respectively. +Higher gain end is selected. p Values are not explicitly given rather inferred from the given results. &Core circuit consumed 60 μW and buffer consumed 1.4 mW. #both core and buffer power are considered for FOM calculation. $Buffer power is not included. N/R:Not reported

considered here. The comparison is given in Table 5.2.

The works [84, 132–135] use current-reuse topology while [44, 75, 80] are based on conventional source degenerative CS techniques. It can be observed that the suggested LNA achieves the highest FOM compared to other current-reuse techniques. If core power alone is included then the FOM of the presented technique reaches a value of 42. Further, the presented design offers the lowest noise figure among all the other LNAs considered in Table 5.2. The circuits for [44] and [80] achieve larger FOM mainly because of the improved linearity performances. However, their inferior noise performance is not suitable for applications like LTE standards. The suggested technique in this chapter offers the best noise figure. Its linearity performance, however, has to be improved to make it suitable for LTE applications. In addition, it undergoes PVT variations and hence has to be augmented with compensation techniques that are discussed in chapter 4. Addressing these two issues would make the implementation complete and these will be considered as future work.

5.4 Conclusion

An overall gain enhancement based on current-reuse technique is presented in this chapter. Unlike the conventional cascode LNA, the gain of the suggested technique does not rely on the Q-factor of the tank circuit at the output node. Hence, the gain dependency is effectively decoupled from the Q-factor of the tank circuits. Further, it gives a better noise-power performance and shows a feasible implementation of an effective micro-watt powered LNA for an application like LTE.

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6

Conclusion and Future directions

Contents

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6.1 Conclusion

Keeping in view of some of the requirements of the forthcoming communication technologies, current research has addressed issues related to the implementation of low power low noise amplifiers. The major contributions and the respective conclusions are as follows.

- The initial approach involves investigation of different MOS regions of inversion to achieve a better noise-power trade-offs.
  - Exploration of design spaces has led to a development of unified noise figure model that can estimate the noise in any of these regions.
  - Noise-power trade-off is carried out with the help of parameter extraction and accordingly a methodology is developed.
  - It is found that moderate inversion based design gives a better noise-power trade-off and furthermore it gives fully on-chip implementable solution for low-power LNA.
  - Usage of low Q factor on-chip inductor is not a viable option at-least at the gate terminal of a LNA as it severely degrades the overall noise performance of a low power amplifier. Hence, it is always better to use high Q off-chip inductors since the required inductor values are large especially in the case of low-power LNA.
- An arbitrary power scaling down would lead to performance degradation and as a consequence performance may not meet the requirements of applications of interest. Hence, power level assignment to an LNA is carried out using the system budgeting of the receiver.
  - The receiver performance assignment and estimations are carried out by including irregularities such as transmitter leakages, phase noise from frequency synthesizers, I/Q mismatch, the presence of interferences and blockers, and ADC noise.
- A new PVT compensation technique based on a simple current comparison is introduced for near sub-threshold LNA
  - PVT variations have a pronounced effect in sub-threshold based amplifiers especially when implemented in sub-nanometer technologies. Hence, these circuits have to be accompanied by compensation mechanisms.

- Compensation is achieved by stabilizing the core device trans-conductance (g_m). A current comparison technique is used to minimize the performance deviation.
- The proposed technique has three main advantages. Firstly, it gives a guaranteed control of the g_m deviation. Secondly, compensation circuits (CCs) do not limit the voltage scaling. Thirdly, CCs consume only a fraction of the total power and thereby do not unnecessarily dictate power budget of the receiver.
- Compensated LNA has shown considerable improvements against process, voltage and temperature variations. It has shown 20% yield improvement compared to conventionally biased LNAs.
- The proposed compensated LNA could operate from -20^o to $+110^o$C with a gain deviation of $\pm 1\%$ for typical device corner cases. The overall circuit is operated at 0.6 V of supply voltage with a total power consumption of 402 μW. The deviations due to PVT variations are firmly controlled in the proposed compensated LNA.
- To facilitate compensation mechanisms, a low voltage constant current reference (CCR) is introduced. CCR could operate with a voltage as low as 0.4 V which is the minimum among all other recent contributions reported in literature.
- The proposed CCR results in a TC (temperature coefficient) of $118 ppm/^oC$ and has shown a maximum percentage deviation of $\pm 1.6\%$ for a voltage range from 0.32 to 1.2 V for the typical-typical (tt) corner case. It has shown a maximum percentage deviation of $\pm 6.4\%$ when all the process corners are considered and it can operate with a power consumption of 1 μW.
- Depending on the deduced requirements from the LTE specification, a compensated microwatt-power LNA is implemented and is estimated to satisfy the sensitivity requirement of LTE receiver.

- G_m enhancement technique is implemented with the usage of current-reuse mechanisms.
  - The overall gain of the circuit is increased because of G_m elevation for a given power. Further, it resulted in an option of decoupling the gain dependency from the Q-factor of the tank circuit.

6.2 Future directions

The prospective work will be a combination of the current research and the forthcoming generation technological requirements. The future work is beamed through a model which can be defined as SIPP (System, Integration, Process, and Power). Future research scope is inspired by the following implementation challenges for the upcoming technological requirements.

- System: Architectural development and implementation of multi-mode receivers along with device-to-device (D2D) communication features would be an interesting problem. Significant improvement is required at the system architecture level to incorporate advanced features.
  - Cognitive radios seek incorporation of cognitive ability such as spectrum sensing, analysis and decision-making provisions [136].
  - Scalable RF receivers [137] are suitable architectures for dynamic spectrum allocation. Further, the incorporation of cognitive abilities to such receivers can be a scope for future research.
  - Usage of underlay spectrum sharing demands more sensitive receivers.
  - Deployment of heterogeneous network for cellular communication as such planned in 5G networks [138] would increase the interference level seen at the receiver ends. It would again demand for enhancements in current receivers' sensitivity.
  - Expected increase in interference level would also demand more linear receivers. Digitally assisted calibration techniques can be relooked at the system level to achieve the linearity demands.
- Integration: Challenges are involved in developing system-on-chips.
  - Tunable radios demand filters bank or Field Programmable Filter Arrays (FPFA) [139]. Incorporation of such features on a single chip would be a challenging task.
  - FPFA based on $G_m - C$ filters [140] a feasible option for SOCs, however, linearity and power dissipations are still a major concern.
  - Novel circuit topologies are required in receiver components which can deliberately avoid inclusion of passive elements. Not meeting such demands would increase the bill of materials for future multi-mode receivers.

  - On-chip implementable and reconfigurable circuit topologies are required for amplifiers and filters in-order to realize multi-mode transceivers.

- Process: Yield is going to be a major concern in advanced technological nodes.
  - Analog/RF circuits have to be accompanied with compensation circuits to stabilize against PVT (Process-Voltage-Temperature) variations [141]. Implementations of these circuits in sub-nanometer technologies would demand development of compensation circuits to improve the overall yield.
  - Novel circuit topologies are required to improve the performances which are naturally degraded by second-order effects in sub-nanometer technologies.
- Power: Lower the power, the longer will be the battery life.
  - Low power receivers [142] are always ideally expected to prolong the battery life.
  - Embedding multiple features onto a single radio increases requirement of energy consumption of the receivers. Novel low power design techniques and circuit topologies are further required in order to efficiently address energy requirements of the upcoming receivers.

To summarize, future radios invite challenges at different implementation levels starting from circuits to system level design issues and the power consumption would remain as the major focus in bringing the next generation receivers.

A

Input impedance and NF expression

Contents

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A.1 Input impedance approximation

The input impedance from equation (3.2) can be given as

$$Z_{in} = s\left(L_g + L_s\right) + \frac{1}{sC_t} + R_g + A(s) \tag{A.1}$$

where $A(s) = \frac{\omega_t L_s r_{ds}}{r_{ds}+Z_L+sL_s}$. Consider the A(s) alone by replacing s by $j\omega$. Further, multiply and divide $A(j\omega)$ by its denominator term $r_{ds} + Z_L + sL_s$ and is given as

$$A(j\omega) = \frac{\omega_t L_s r_{ds}}{r_{ds} + Z_L + j\omega_o L_s}\left(\frac{r_{ds} + Z_L - j\omega_o L_s}{r_{ds} + Z_L - j\omega_o L_s}\right) \tag{A.2}$$

$$\Rightarrow A(j\omega) = \frac{\omega_t L_s r_{ds}\left(r_{ds} + Z_L - j\omega_o L_s\right)}{\left(r_{ds} + Z_L\right)^2 + \left(\omega_o L_s\right)^2} \tag{A.3}$$

With a value of ω_o, $\omega_o = 0.1\omega_t$, and $\omega_t L_s \approx R_s = 50\ \Omega$, that are based on general design assumptions, the denominator of $A(j\omega)$ can be written as

$$\left(r_{ds} + Z_L\right)^2 + \left(\omega_o L_s\right)^2 = \left(r_{ds} + Z_L\right)^2 + \left(0.1\omega_t L_s\right)^2 \approx \left(r_{ds} + Z_L\right)^2 \tag{A.4}$$

The approximated denominator from (A.4) is used for $A(j\omega)$ in (A.3) and is given as

$$A(j\omega) = \frac{\omega_t L_s r_{ds}\left(r_{ds} + Z_L - j\omega_o L_s\right)}{\left(r_{ds} + Z_L\right)^2} = \frac{\omega_t L_s r_{ds}\left(r_{ds} + Z_L\right)}{\left(r_{ds} + Z_L\right)^2} - j\frac{\omega_t L_s r_{ds}\left(\omega_o L_s\right)}{\left(r_{ds} + Z_L\right)^2} \tag{A.5}$$

$$\Rightarrow A(j\omega) = \omega_t L_s \frac{r_{ds}}{r_{ds} + Z_L} - j\frac{\omega_t L_s r_{ds}\left(\omega_o L_s\right)}{\left(r_{ds} + Z_L\right)^2} = \omega_t L_s r - j\frac{\omega_t L_s r_{ds}\left(\omega_o L_s\right)}{\left(r_{ds} + Z_L\right)^2} \tag{A.6}$$

where $r = \frac{r_{ds}}{r_{ds}+Z_L}$. By considering the approximations from (A.6), Z_{in} from (A.1) can be written as,

$$Z_{in} = j\left[\omega_o\left(L_g + L_s\right) - \frac{1}{\omega_o C_t} - \frac{\omega_t L_s r_{ds}\left(\omega_o L_s\right)}{\left(r_{ds} + Z_L\right)^2}\right] + R_g + \omega_t L_s r \tag{A.7}$$

In the imaginary term of Z_{in}, the value of $\frac{\omega_t L_s r_{ds}(\omega_o L_s)}{\left(r_{ds}+Z_L\right)^2}$ is less compared to the value of $\frac{1}{\omega_o C_t}$. Hence, $\frac{\omega_t L_s r_{ds}(\omega_o L_s)}{\left(r_{ds}+Z_L\right)^2}$ can be neglected and the final Z_{in} can be written as

$$Z_{in} \approx s\left(L_g + L_s\right) + \frac{1}{sC_t} + R_g + \omega_t L_s r \tag{A.8}$$

A.2 NF expression

The noise factor of a CS degenerative topology can be given as

$$NF = \frac{\overline{i^2_{out\_R_s}}|G_m|^2 + \overline{i^2_{out\_R_g}}|G_m|^2 + \overline{i^2_{out\_tot}}}{\overline{i^2_{out\_R_s}}|G_m|^2} = \frac{R}{R_s} + \frac{\overline{i^2_{out\_tot}}}{\overline{i^2_{out\_R_s}}|G_m|^2} \tag{A.9}$$

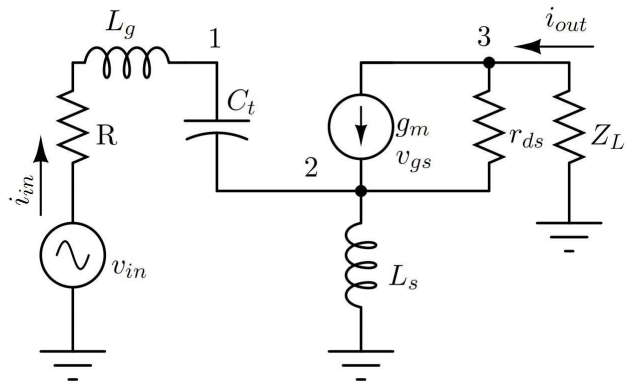

Figure A.1: A set up for deriving expression for G_m of a CS degenerated LNA.

where $\overline{i^2_{out\_R_s}} = 4kTR_s$, $\overline{i^2_{out\_R_g}} = 4kTR_g$, $R = R_s + R_g$ and $\overline{i^2_{out\_tot}}$ is the total output noise PSD (power spectral density) due to internal noise sources $\overline{i^2_{nd}}$ and $\overline{i^2_{ng}}$. To calculate the NF, the parameters G_m, R/R_s, and the output noise current $\overline{i_{out}}$ are derived individually and then substituted in the NF expression.

Effective transconductance, G_m:

To find an expression for G_m, eliminate both $\overline{i^2_{nd}}$ and $\overline{i^2_{ng}}$ in the Fig 3.3(b). An input voltage is applied at the terminal of R and the resulting output current i_{out} is found to calculate the overall G_m. The setup is as shown in Fig A.1. Apply KVL at the input node and correspondingly the input voltage can be given as

$$v_{in} = i_{in}\left[R + sL_g + \frac{1}{sC_t} + sL_s\right] + i_{out}\left(sL_s\right) \tag{A.10}$$

By applying KCL at the output node 3, the expression for i_{out} can be given as

$$i_{out} = g_m v_{gs} + \frac{(v_3 - v_2)}{r_{ds}} \tag{A.11}$$

where $v_2 = (i_{out} + i_{in})\, sL_s$ and $v_3 = -i_{out}Z_L$. By considering (A.10) and (A.11) with values of v_2 and v_3, G_m can be given as

$$G_m = \frac{i_{out}}{v_{in}} = \frac{g_m}{sC_tR}\frac{\left[1 + \frac{\omega_o^2 C_t L_s}{g_m r_{ds}}\right]}{\left[1 + \frac{Z_L}{r_{ds}} + \frac{g_m L_s}{C_t R} + \frac{\omega_o^2 L_s^2}{r_{ds} R} + j\frac{\omega_o L_s}{r_{ds}}\right]} \tag{A.12}$$

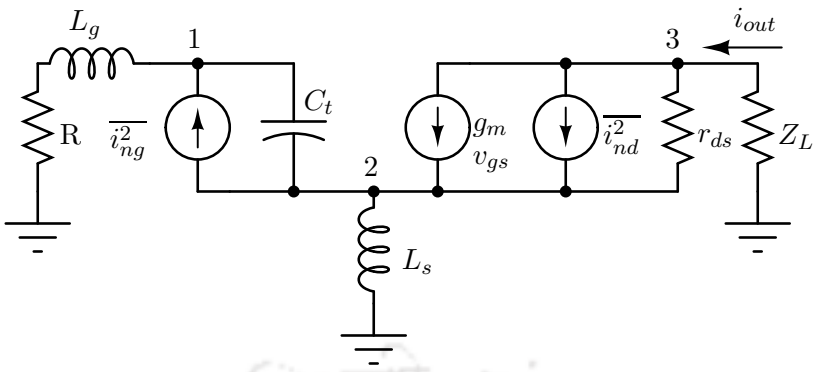

Figure A.2: Equivalent circuit of the source degenerated LNA including its internal noise sources $\overline{i_{nd}}$ and $\overline{i_{ng}}$.

R/R_s**:**

The expression of R contains R_g and R_s, where R_g can be related to $\omega_o L_g$ through the quality factor Q_{ind}. Therefore, R/R_s can be related to quality factors from the expressions of $\omega_o L_g$. $\omega_o L_g$ from (3.8) and (3.9) are equated and is given as

$$Q_s R - \omega_o L_s = R_g Q_{ind} + R_{g,BW}\left(Q_{BW} - Q_{ind}\right) - R_{g,MOS} Q_{ind} \tag{A.13}$$

However, $R = R_s + R_g$ and $L_s = \frac{(R_s - R_g)}{\omega_t r}$ from the power match condition. By taking these into account along with (A.13), R_g can be given as

$$R_g = \frac{R_s\left(Q_s - \frac{\omega_o}{\omega_t r}\right) + R_{g,BW}\left(Q_{BW} - Q_{ind}\right) - R_{g,MOS} Q_{ind}}{\left(Q_{ind} - Q_s - \frac{\omega_o}{\omega_t r}\right)} \tag{A.14}$$

Dividing by R_s and then adding +1 on both sides one can write,

$$1 + \frac{R_g}{R_s} = \frac{R_g + R_s}{R_s} = \frac{R}{R_s} \tag{A.15}$$

$$\Rightarrow \quad \frac{R}{R_s} = \frac{Q_{ind} - \frac{2\omega_o}{\omega_t r} + \frac{R_{g,BW}}{R_s}\left(Q_{ind} - Q_{BW}\right) + \frac{R_{g,MOS}}{R_s} Q_{ind}}{Q_{ind} - Q_s - \frac{\omega_o}{\omega_t r}} \tag{A.16}$$

Output noise current, $\overline{i_{out\_tot}}$ **and NF:**

The equivalent circuit for the CS degenerated LNA is shown in Fig. A.2. Let us consider v_1, v_2 and v_3 are the voltages at nodes 1, 2 and 3 respectively in the Fig. A.2. The current flowing through

R is given as

$$i_R = \overline{i_{ng}} - (v_1 - v_2)\, sC_t = \overline{i_{ng}} - (i_R\,(R + sL_g) - v_2)\, sC_t \tag{A.17}$$

$$\Rightarrow i_R = \frac{\frac{\overline{i_{ng}^2}}{sC_t} + v_2}{Z} = i_{out} - \frac{v_2}{sL_s} \tag{A.18}$$

where $Z = R + sL_g + \frac{1}{sC_t}$. From the above relation, node voltages v_1 and v_2 can be given as

$$v_1 = i_R\,(R + sL_g) = \left(i_{out} - \frac{v_2}{sL_s}\right)(R + sL_g) \tag{A.19}$$

$$v_2 = \frac{i_{out}\,(ZsL_s)}{(Z + sL_s)} - \frac{\overline{i_{ng}}\left(\frac{sL_s}{sC_t}\right)}{(Z + sL_s)} \tag{A.20}$$

From v_1 and v_2, v_{gs} can be given as

$$v_{gs} = v_1 - v_2 = \frac{1}{sC_t\,(Z + sL_s)}\left[-i_{out}sL_s + \overline{i_{ng}}\,(R + s\,(L_s + L_g))\right] \tag{A.21}$$

Applying KCL at the output node, 3, in Fig. A.2, the expression for output noise current $\overline{i_{out}}$ can be expressed as,

$$\overline{i_{out}} = \overline{i_{nd}} + g_m v_{gs} + \frac{(v_3 - v_2)}{r_{ds}} \tag{A.22}$$

where $v_3 = -i_{out}Z_L$. By substituting, v_{gs}, v_2, and v_3, $\overline{i_{out}}$ can be written as follows:

$$\overline{i_{out}}\left[1 + \frac{Z_L}{r_{ds}} + \frac{g_m sL_s}{sC_t\,(Z + sL_s)} + \frac{ZsL_s}{r_{ds}\,(Z + sL_s)}\right] = \overline{i_{nd}} + \overline{i_{ng}}\left[\frac{g_m\,(R + s\,(L_s + L_g))}{sC_t\,(Z + sL_s)} + \frac{sL_s}{sC_t r_{ds}\,(Z + sL_s)}\right] \tag{A.23}$$

At resonance, $Z + sL_s = R + sL_g + \frac{1}{sC_t} + sL_s = R = R_s + R_g$. The gate induced noise, $\overline{i_{ng}}$, consists of a correlated noise, $\overline{i_{ngc}}$ and an uncorrelated part, $\overline{i_{nguc}}$ and these are given as [69]

$$\overline{i_{ngc}} = -j|C|\overline{i_{nd}}\frac{\omega C_{gs}}{g_m}\sqrt{\frac{\delta\alpha^2}{5\gamma}} \tag{A.24}$$

$$\overline{i_{nguc}} = \frac{\omega C_{gs}}{g_m}\sqrt{4kT\gamma g_{do}}\sqrt{\frac{\delta\alpha^2}{5\gamma}\,(1 - |C|^2)} \tag{A.25}$$

where $\alpha = g_m/g_{do}$, with g_{do} as the drain-source conductance when $v_{ds} = 0\ V$, C is the correlation coefficient, and γ and δ are the noise parameters. Using (A.24) and (A.25) in (A.23), the resulting output noise current due to the correlated and the uncorrelated noise can be obtained as

$$\overline{i_{out\_c}} = \overline{i_{nd}} \frac{\left[\left(1 - |C|\frac{C_{gs}}{C_t}\sqrt{\frac{\delta\alpha^2}{5\gamma}}\right) - j|C|\frac{C_{gs}}{C_t}\sqrt{\frac{\delta\alpha^2}{5\gamma}}\left[Q_{in} + \frac{\omega_o L_s}{g_m r_{ds} R}\right]\right]}{\left[1 + \frac{Z_L}{r_{ds}} + \frac{g_m L_s}{C_t R} + \frac{\omega_o^2 L_s^2}{r_{ds} R} + j\frac{\omega_o L_s}{r_{ds}}\right]} \tag{A.26}$$

$$\overline{i_{out\_uc}} = \overline{i_{nd}} \frac{\frac{C_{gs}}{C_t}\sqrt{\frac{\delta\alpha^2}{5\gamma}\left(1 - |C|^2\right)}\left[Q_{in} + \frac{\omega_o L_s}{g_m r_{ds} R} - j\right]}{\left[1 + \frac{Z_L}{r_{ds}} + \frac{g_m L_s}{C_t R} + \frac{\omega_o^2 L_s^2}{r_{ds} R} + j\frac{\omega_o L_s}{r_{ds}}\right]} \tag{A.27}$$

where Q_{in} is the quality factor of the network with $Q_{in} = \frac{\omega_o(L_s+L_g)}{R}$. The total output noise current PSD can be given as

$$\overline{|i_{out\_tot}|^2} = \overline{|i_{out\_c}|^2} + \overline{|i_{out\_uc}|^2} \tag{A.28}$$

$$\Rightarrow \overline{i_{out\_tot}^2} = \overline{i_{nd}^2} \frac{\left[1 - 2\,|C|\,\frac{C_{gs}}{C_t}\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \left(\frac{C_{gs}}{C_t}\right)^2 \frac{\delta\alpha^2}{5\gamma}\left(1 + \beta^2\right)\right]}{\left[\left(1 + \frac{Z_L}{r_{ds}} + \frac{g_m L_s}{C_t R} + \frac{\omega_o^2 L_s^2}{r_{ds} R}\right)^2 + \left(\frac{\omega_o L_s}{r_{ds}}\right)^2\right]} \tag{A.29}$$

where $\beta = Q_{in} + \frac{\omega_o L_s}{g_m r_{ds} R}$. Finally, the expression of G_m (A.12) and $\overline{i_{out\_tot}}^2$ (A.29) are substituted in (A.9) to get the NF as

$$NF = \frac{R}{R_s}\left(1 + \frac{\omega_0^2 \gamma}{\alpha}\frac{C_t^2}{g_m}\frac{R\chi}{\left(1 + \frac{\omega_o^2 C_t L_s}{g_m r_{ds}}\right)^2}\right) \tag{A.30}$$

with $\chi = \left(1 - 2C\frac{C_{gs}}{C_t}\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{C_{gs}^2}{C_t^2}\frac{\delta\alpha^2}{5\gamma}\left(1 + \beta^2\right)\right)$.

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B

Stability of compensation circuits

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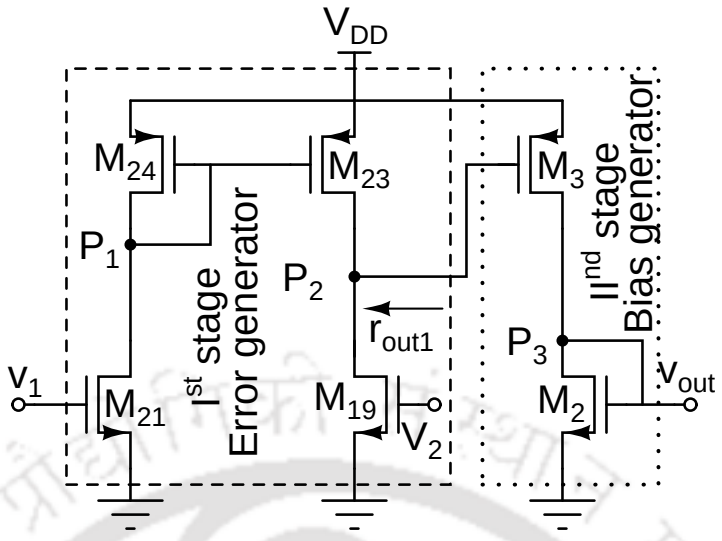

Figure B.1: Simplified equivalent of the compensating mechanism

Amplifiers may suffer from stability issues when it is comprised of two or more cascaded stages. The error and the bias generator in the compensation mechanism together form a topology similar to a cascaded amplifier and structurally it appears to pose a threat to stability. In this appendix we show that although the circuit looks similar to that of a cascaded amplifier, it does not impose stability problems because of the difference in functionality requirement in comparison to the conventional amplifiers.

Poles and zeros

To gain insight and to validate the reason for absolute stability, the compensation circuit from Chapter 4, Fig. 4.8, is simplified and is redrawn in Fig. B.1. The feedback connection is removed with the respective input and output voltages of the equivalent circuit denoted as V_1 and V_{out}. Further, the voltage input from the CCR to the compensation circuit, V_2, is assumed to be constant for the stability analysis. For simplicity, the respective cascodes in compensation circuits are not shown. In this configuration, there exist three poles (P_1, P_2, and P_3) and one zero. An approximate DC gain of the configuration shown in Fig. B.1 is given as

$$|A_v| = \frac{v_{out}}{v_1} = g_{m21} r_{out1} \tag{B.1}$$

By taking the cascode devices ($M_{20,23c}$ are not shown here) also into consideration, r_{out1} can be written as $r_{out1} \approx \frac{g_{m23} r_{ds23}^2}{2}$ for a case where r_{ds} and g_m values of devices $M_{19,20}$ and $M_{23,23c}$ are equal.

In addition, it is assumed that M_2 and M_3 have the same transconductance and as a consequence the second stage can be interpreted as an unity gain amplifier.

Poles and zero of this configuration can be given as

$$P_1 = \frac{g_{m24}}{C_{gs23} + C_{gs24}} \approx \frac{g_{m24}}{C_{gs24}} \tag{B.2}$$

$$P_2 \approx \frac{2}{g_{m23} r_{ds23}^2 C_{gs3}} \tag{B.3}$$

$$P_3 \approx \frac{g_{m2}}{C_{gs2}} \tag{B.4}$$

$$P_z \approx 2P_1 \tag{B.5}$$

P_1: The current is scaled down from M_{24} to M_{23}. In this design, the size of M_{23} is around 24 times small compared to M_{24}. Hence, the effective capacitance at the node of P_1 is largely dominated by C_{gs} of M_{24} transistor.

P_2: In this design, the size of M_3 is happened to be comparable with that of M_{24}. Therefore, M_3 contributes a larger capacitance compared to any other device at the node, P_2. Hence, the capacitance is approximated only with C_{gs3} for P_2.

P_3: The resistance, $1/g_{m2}$, and the capacitance, C_{gs2}, offered by M_2 is considered for P_3.

Stability

There are three poles and a left half plane zero which is situated at twice the frequency of the first pole, P_1. If these poles fall near to each other and before the UGF(Unity Gain Frequency) then the system will be subjected to stability issues. The P_3 cannot become the dominant pole because C_{gs2} is much smaller than other capacitances such as C_{gs3} and C_{gs24}. The pole dominance among P_1 and P_2 can be determined by making an assumption for the intrinsic gain as, $g_m r_{ds} = 10$, and replacing the variables by this typical value. As $C_{gs24} \approx C_{gs3}$, comparison has to be made between $P_1 \propto g_{m24}$ and $P_2 \propto \frac{1}{5 r_{ds23}}$. By using $g_m r_{ds} = 10$, it can be estimated that $P_1/P_2 = 50$. Hence P_2 is acting as a dominant pole primarily because of the larger resistance at node P_2 as compared to P_1. Consequently,

the unity gain frequency (UGF) can be given as

$$UGF \approx \frac{g_{m21}}{C_{gs3}} \tag{B.6}$$

A comparison between P_1 and UGF indicates that $P_1 \approx UGF$ for $g_{m21} = g_{m24}$. This tells that the dominant pole is situated far from the UGF while the second pole is placed near to UGF. Thus, the overall circuit behaves like a single pole system and therefore it is expected to be absolutely stable. In summary, the cascaded stage shown in Fig. B.1 is stable because of three reasons. Firstly, the unequal sizing between M_{23} (smaller) and M_{24}, makes P_1 to be non-dominant and as a consequence it stays far away from P_2. Secondly, the cacsode stage at the drains of M_{23} and M_{19} introduces larger resistance, which makes P_2 to be the dominant one. Thirdly, the diode connected device M_2 in the second stage pushed P_3 far away from P_2.

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Journal Publications

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1. MM. Vinaya, R. Paily and A. Mahanta,"Power Optimization of LNA for LTE Receiver", *2016 29th International Conference on VLSI Design and 2016 15th International Conference on Embedded Systems (VLSID)*, Kolkata, India, pp. 162-167, Jan. 2016.

2. MM. Vinaya, R. Paily and A. Mahanta,"A low-power subthreshold LNA for mobile applications", *VLSI Design and Test (VDAT), 2015 19th International Symposium on*, Ahmedabad, India, pp. 1-5, June 2015.

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