Modeling Ambipolar Behavior under High Current Injection Regimes in Layered Semiconductor Device Structures

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By

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Certificate

This is to certify that the thesis entitled "**Modeling Ambipolar Behavior under High Current Injection Regimes in Layered Semiconductor Device Structures**", submitted by **Dheeraj Kumar Sinha** (11610243), a research scholar in the *Department of Electronics and Electrical Engineering, Indian Institute of Technology Guwahati*, for the award of the degree of **Doctor of Philosophy**, is a record of an original research work carried out by him under my supervision and guidance. The thesis has fulfilled all requirements as per the regulations of the institute and in my opinion has reached the standard needed for submission. The results embodied in this thesis have not been submitted to any other University or Institute for the award of any degree or diploma.

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To

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for their guidance and inspiration

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for their blessings, love and support

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Abstract

This thesis develops novel insight towards understanding high current injection phenomenon in bipolar structures. High current injection mechanisms are ubiquitously connected to reliability issues both in advanced nano-scale as well as high power devices which are lifeline of the semiconductor industry. In absence of accurate high current breakdown models, an attempt has been made to develop physical insights into basic layered semiconductor structures that are present as parasitic elements in advanced high voltage semiconductor device structures such as: VDMOS, IGBT, cool MOS etc. Under this conditions, it is very difficult to model or derive the analytical solutions, hence numerical device simulations (TCAD) is an inevitable first step towards the physical understanding of these mechanisms. The goal of this thesis is to develop high current breakdown models that can be incorporated in the form of circuit level models to obtain reliable numerical simulation results prior to putting it into silicon wafer. In this work, the dynamic avalanche model is connected with the Base push-out effect or Kirk effect for the first time to explain anomalous or non-deterministic switching behavior of bipolar transistor at high current densities. Moreover, we first look into the 1D coupling of diode breakdown and bipolar turn-on and then extend it to 2D models. Subsequently, the dynamic avalanche is explained through an analytical model which leads to transit time behavior of carriers under high current conditions. The developed model will be essential to predict and understand the ambipolar high current injection behavior of complex high voltage device structures during dynamic avalanche phenomenon, at ultra-fast switching conditions and during an ESD event.

Initially, we establish a novel physics-based models to understand the anomalous or non-deterministic switching behavior of different configurations of bipolar structures such as: base-drive, base open, emitter open and base-emitter shorted, at high current injection conditions. Furthermore, the role of voltage trigger pulse with variable rise time when applied to the base terminal is investigated to model the underlying physics of anomalous

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switching behavior. In another experimental split, a variable ultra-fast high voltage pulses are applied to collector terminal of bipolar transistor whose base-emitter is externally shorted. The occurrence of two completely different breakdown mode (*i.e.*, no-snapback or snapback) is observed. The measurement results pertaining to different rise time of high voltage pulses, applied across different configurations of the bipolar transistor are discussed and analytically modeled. The double injection mechanisms under variable ultra-fast high-speed ramps are investigated through formation and propagation of self-reinforced ionizing wavefront, which results in either strong or weak injection of holes from the n^-/n^+ junction, as the avalanche injection of mobile carriers get coupled in the device structures. Moreover, different measurement observations are confirmed using commercially available (Sentaurus) $2-D$ TCAD device simulations, as we explain the generic behavior of filaments in different regions of the high voltage ramp speed. Finally, we revisited and analytically modeled the mobile carrier distribution and derived the condition for the triggering of moving ionization front in the depletion region by varying carrier drift velocities and impact-ionization coefficients, and discuss voltage collapse due to double injection of mobile carrier and subsequently model the non-deterministic snapback behavior of bipolar transistors.

Keywords: Avalanche breakdown, base push-out effect, bipolar transistors, bipolar turn-on, current mode secondary breakdown (CMSB), dynamic avalanche, filamentation, non-deterministic switching, instability.

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List of Acronyms

BCD	Bipolar, CMOS, and DMOS
BE	Base-emitter
BJT	Bipolar junction transistor
BiCMOS	Bipolar CMOS
BTE	Boltzmann transport equation
BV	Breakdown voltage
CAD	Computer Aided Design
CMOS	Complementary MOS
DC	Direct current
DD	Drift-diffusion
DoE	Design of Experiments
EPI	Epitaxial (layer)
ESD	Electrostatic Discharge
VDMOS	Vertical Double diffused MOS
DMOSFET	Double-diffused MOS transistor
FET	Field Effect Transistor
FOX	Field oxide
GTO	Gate turn-off thyristor
HBM	Human body model
HBT	Heterojunction Bipolar Transistor
HD	Hydrodynamic
HV	High-voltage
HVDC	High-voltage direct current
HVIC	High-voltage IC

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IC	Integrated circuit
IEEE	The Institute of Electrical and Electronics Engineering
IEGT	Injection-enhanced gate transistor
IGBT	Insulated gate bipolar transistor
II	Impact-Ionization
IV	Current voltage
JFET	Junction field-effect transistor
LDD	Lightly doped drain
VDMOSFET	Vertical double diffused MOS transistor
VIGBT	Vertical IGBT
LV	Low-voltage
MOS	Metal-oxide semiconductor
MOSFET	Metal-oxide semiconductor field-effect transistor
NMOS	n-channel MOS
ggNMOS	Gate-grounded n-channel MOS
PIC	Power IC
PMOS	p-channel MOS
RF	Radio frequency
SCR	Silicon controlled rectifier
SiC	Silicon carbide
Si	Silicon
SOA	Safe operating area
SOI	Silicon on insulator
SRH	Shockley-Read-Hall
TCAD	Technology computer aided design
TLP	Transmission line pulse
ULSI	Ultra large scale integration
UMOSFET	U-shape metal-oxide semiconductor field-effect transistor
VLSI	Very large scale integration

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List of Symbols

J	Current Density
V	Voltage
ϵ	Permittivity
ϵ_{si}	Permittivity of Silicon
L	Distance between a cathode and an anode
q	The charge of an electron
k	Boltzmanns constant
T	Temperature
β	Bipolar Gain
ϵ	Dielectric constant
μ	Mobility
σ	Conductivity
x	Position in a material
v	Average drift velocity
t	Transit time of a free electron
N_c	Density of states in the conduction band
N_v	Density of states in the valence band
C	Capacitance of a material
C_O	Capacitance of a parallel-plate capacitor
E_C	Conduction band energy level
E_V	Valence band energy level
E_F	Fermi-level at thermal equilibrium
n	Free electron concentration
n_0	Thermal equilibrium free electron concentration

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$\alpha_{n,p}$	Electron, hole impact ionization coefficient
α_0	Effective impact ionization coefficient
BV_{CEO}	Collector to emitter breakdown voltage with the base open
BV_{CBO}	Collector to base breakdown voltage with the emitter open
$C_{n,p}$	Auger coefficient
D, $D_{n,p}$	Diffusion coefficient
E	Electric field
E_c	Critical electric field
E_max	Maximum electric field
E_i	Intrinsic energy level
E_r	Recombination energy level
E_t	Trap energy level
$G_{n,p}$	Generation rates
N_epi	n-epi layer doping concentration
$N_\mathrm{D,A}$	Donor, acceptor doping concentration
N_D^+, N_A^-	Ionized donor, acceptor concentration
p	Hole concentration
n	Hole concentration
R, $R_{n,p}$	Recombination rate
R_Auger	Auger recombination rate
R_SRH	Shockley, Read, and Hall recombination rate
T	Temperature
T_0	Room temperature (300 K)
$T_{n,p,\mathrm{L}}$	Electron, hole, and lattice temperature
τ_HL	High level carrier lifetime
τ_LL	Low level carrier lifetime
$\tau_{n,p}$	Electron, hole minority carrier lifetime
$\tau_{n0,p0}$	Minority carrier lifetimes at low doping level
t_ox	Buried oxide thickness
v	Drift velocity

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v_{ns}	Electron drift velocity
v_{ps}	Hole drift velocity
V_{A}	Anode voltage
V_{BR}	Breakdown voltage
$V_{\mathrm{DS,GS,BS}}$	Drain to source, gate to source, bulk to source voltage
V_{PT}	Punchthrough voltage
V_{R}	Reverse voltage
V_{BE}	Base-emitter Voltage
W	Depletion region width
W	Base region width
W_{dep}	Depletion region width.

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1 Introduction

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In current scenario, electronic products and components have become an integral part for a numerous number of applications based on the semiconductor material devices [1–3]. The miniaturization and improvement in performance of integrated circuits (ICs) continuously paves new possibilities for academic and industrial research [1, 4]. On the other hand, the entire development is targeted to decrease the cost per transistor [5]. The important factor responsible for the cost reduction is a sudden increase of device density on the same silicon wafer area. The semiconductor manufacturing industry has shown many improvements as the feature size of Metal Oxide Semiconductor (MOS) devices shifted towards nanometer regime [4]. Due to the continuous scaling of the device, a huge number of MOS transistor could be accomadated on a single chip, a downside of this increased integration is an increase in leakage current [1]. The electric field and current density are also increasing rapidly which results in many types of breakdown mechanism in the device structures such as gate-oxide tunneling, avalanche breakdown etc [6]. Therefore, the knowledge of high current breakdown mechanism in high voltage device structure is also very important and useful for any researchers and scientist [7]. The complex geometry of the device structures in nanometer regimes shows higher bulk leakage current due to the presence of parasitic layered semiconductor structures or elements which become reliability issues in the CMOS technology, particularly under ultra high current injection conditions such as ESD phenomenon, dynamic avalanche breakdown conditions [8–11]. Reliability physics of high current phenomenon in commercially critical and emerging power devices integrated into state of art VLSI devices is intricately related to transient mechanisms of high current pulses across a parasitic bipolar structures [11, 12]. However, the microscopic understanding of transient behind the breakdown phenomenon under high current injection conditions in semiconductor devices has so far not been clearly understood [9, 11]. This is due to an absence of knowledge of high current injection theory and development of high current breakdown models concerning semiconductor devices, therefore reliability study of the complex device structures has become an area of the interest under high current conditions [8, 9]. An overview on the reliability of semiconductor device structure is followed by specific reliability concerns.

1.1 Reliability Issues in Semiconductor Devices

The reliability issue is still a major concern from the early stages of the industrialization of semiconductor ICs [13]. When we go back and look at history, it has taken roughly 60 years until the

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reliability issue of the incandescent light bulb has been high enough to make electronics lighting commercially interesting [14]. Researchers had put so much effort into finding suitable materials used for development of filament as well as for gas surrounding it. Furthermore, technological advancement was finally offered for high-performance vacuum pumps. Then finally it became successful when fabrication steps and design of incandescent bulbs were defined. This example shows the importance of reliability for any new products and the two key challenging issues for the development of robust and reliable products are technology and materials [15, 16].

As the manufacturing industry wants to incorporate more semiconductor devices on the same area of a chip without degrading the performance of the internal circuit [17]. To achieve this, devices need to be scaled in nanometer regimes, various complex device structures have been proposed by the industry. However, different kind of breakdown and short channel effects (SCEs) comes into the picture [7]. Therefore, reliability issues in the VLSI industry is a major concern due to hot-carrier and impact-ionization process. In high voltage device structures, it has been especially noticeable near the drain side of a channel region in power MOSFET device structure [18]. The cascaded avalanche breakdown mechanism leads to triggering avalanche-generated mobile carrier thus the net carrier concentrations and current densities increase rapidly. High voltage device structure has been designed to the specifications carefully to avoid avalanche breakdown under all the operating conditions. However, for some applications such as; power supply peaks or electrostatic discharge (ESD), avalanche breakdown can not be fully avoided. The electric field and current density also increases rapidly within the complex device structure as the semiconductor devices moved nanometer regime which results in higher bulk leakage current. Due to the presence of parasitic layered elements such as diode, bipolar transistor etc, leakage current becomes higher which becomes reliability issues in the current CMOS technologies. These intrinsic elements are operated under high current breakdown regimes [19, 20]. In order to understand high current injection behavior of layered semiconductor devices, ultra-fast high voltage or current pulses are applied across the contacts. Most of the high voltage as well as nano-scale device structure have intrinsic bipolar transistor such as IGBT, MOS, etc. The basic knowledge of ultra high current injection behavior of bipolar transistor is required to obtain higher robust reliability issues in advanced nanometer CMOS technologies and for other applications such as ultra-fast switching, ESD, etc. [9, 21]. It has been seen that, when an ultra-fast high voltage or current pulses are applied to the bipolar transistor, anomalous or non-deterministic switches behavior was observed [22]. In other

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words, the device shows erratic breakdown mode i.e., either snapback or no-snapback mode [23]. In the snapback mode or current mode secondary breakdown mode (CMSB), current sharply increases and voltage decreases and reaches to the same state where devices were clamped at the breakdown voltage and also shows negative differential conductivity region in current-voltage characteristics. However, in the case of no-snapback mode, the device shows slow switching or primary breakdown mode and current sharply increases but voltage fails to attain low voltage state which results in catastrophic failure of the device [24]. Although significant progress has been made to understand high current injection behavior of high voltage devices. However, the understanding is still incomplete about the understanding high current injection behavior when the ultra-fast high voltage or current ramps are applied across advanced high voltage devices.

1.2 High-Voltage and Power Device Structures

High-performance semiconductor device structures with high voltage and better current handling capability are required for different applications like computers, power electronics and automation [3, 25, 26]. From the invention of germanium point contact transistor in the beginning of 1948 to the current market scenario, there has been all around continuous progress in the area of science and technology of power devices [2, 27]. Several new devices have been designed and manufactured and old technologies device structures have been modified and optimized by introducing new wide band-gap materials, processes and designs to meet the continuous growing need for better and reliable current-voltage characteristics [28]. Besides, current ratings, higher voltage, and higher switching frequency are also needed for the compact and smaller design of integrated circuits [29, 30]. The high voltage diode and bipolar transistors have been in use for last three decade in such applications [31–33]. Now a days, for ultra-fast switching applications and high current handling capability, it is quite common to use the two different major types of device: MOSFET (Metal Oxide Semiconductor Field Effect Transistor) and SCR (Silicon Controlled Rectifier) [5]. Negative differential resistance region (NDR) can be observed in all high voltage device structures (discussed below). This NDR is observed due to impact ionization process and secondary breakdown (latching). During the NDR current filament formation is also observed at the junctions [34]. The current channel formation generally occurs when ultra-fast transient current and voltage pulses are applied, for example during high current avalanche injection conditions or dynamic avalanche breakdown of high voltage device structures [35–37]. To

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understand the insight of the device behavior during the stated conditions is of great importance to develop prevention techniques to avoid the device destruction [11, 21]. Some of the high voltage device structures and their study under high current conditions has been described in the following subsections.

1.2.1 High Voltage Diode

Power diodes are usually called as pin-diodes, because they have an intrinsic region with very low doping concentration in the order of $10^{10} cm^{-3}$ and it is enclosed with outer p^+ and n^+ semiconductor layers [38, 39]. In comparison to unipolar devices, high voltage diodes have the advantage that at high current injection level it's on-resistance gets reduced strongly in the intrinsic region of the diode, which is also called space charge conductivity modulation. Therefore, high voltage diode can be used for very high blocking voltages [32, 38]. In the case of pin diode, doping in the intrinsic region is the range of $< 10^{10} cm^{-3}$, however attaining very low doping by current technology is very difficult. Extreme low doping in the intrinsic region would result in disadvantages during the turn-off behavior. Therefore, power diodes are made-up of layered $p^+/n^-/n^+$ semiconductor structure (shown in Figure 1.1), where intrinsic layer becomes an n^- epi-layer which has doping concentration is the range of $< 10^{15} cm^{-3}$ depending on reverse-biased breakdown voltages [37, 40, 41].

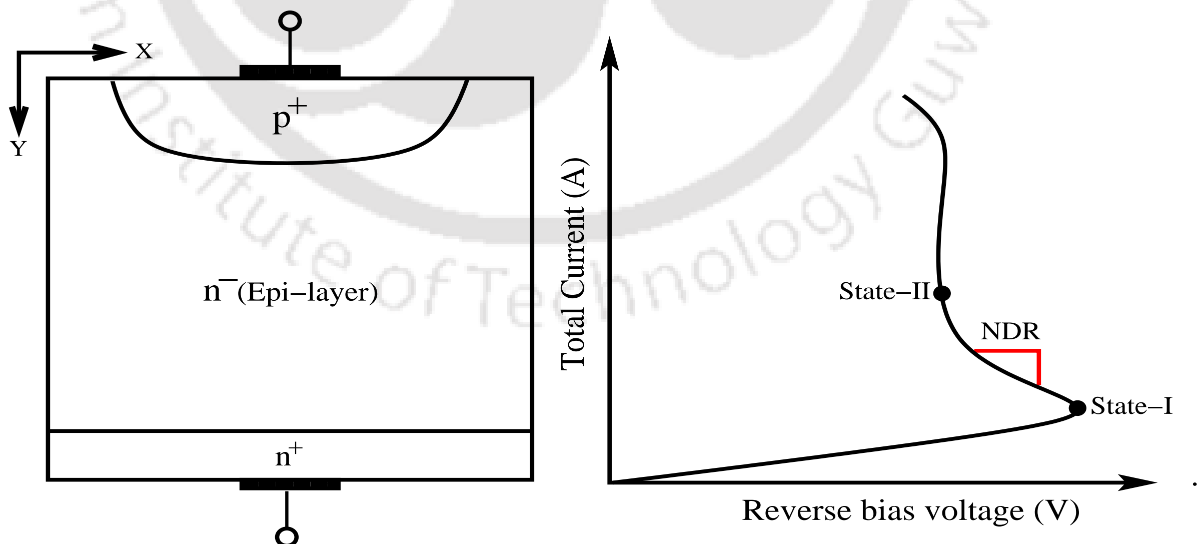

Figure 1.1: Cross-section of high voltage $p^+/n^-/n^+$ diodes and its reverse biased current-voltage characteristics under high current injection condition.

At very high reverse bias voltages, impact-ionization is triggered inside a semiconductor device, thus avalanche generated electrons and holes move towards anode and cathode respectively. The

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generation rate of avalanche generated mobile carriers depends on carrier velocities (v_{ns}, v_{ps}), ionization rates (α_n, α_p) and carrier densities of mobile carriers (n, p):

$$G(n,p,E) = \alpha_n.v_{ns}.n + \alpha_p.v_{ps}.p \tag{1.1}$$

The mobile carrier ionization rate increases rapidly with depleted electric field and mobile carrier drift velocities are dependent on breakdown electric field values which are necessary for initiation of avalanche breakdown process. For reverse biased characteristics of high voltage $p^+/n^-/n^+$ diode, impact ionization process creates electron and hole pairs (EHPs) and current density sharply increase, as shown in Figure 1.1. When the current density exceeds critical value of current density ($i.e.$, $J_{cr} = q.N_d.v_{ns}$), where N_d represents the depletion region background doping concentration in the n^- region, q is the electronic charge and v_{ns} is saturated drift velocity of electron, negative differential conductivity region in the reverse characteristic was observed, which is due to space charge limited (SCL) transport of the mobile carriers. It has been described by looking at the distribution of electric field in depletion region and space charge density at different states of the reverse $I-V$ characteristic of the high voltage diode structure, as shown in Figure 1.1.

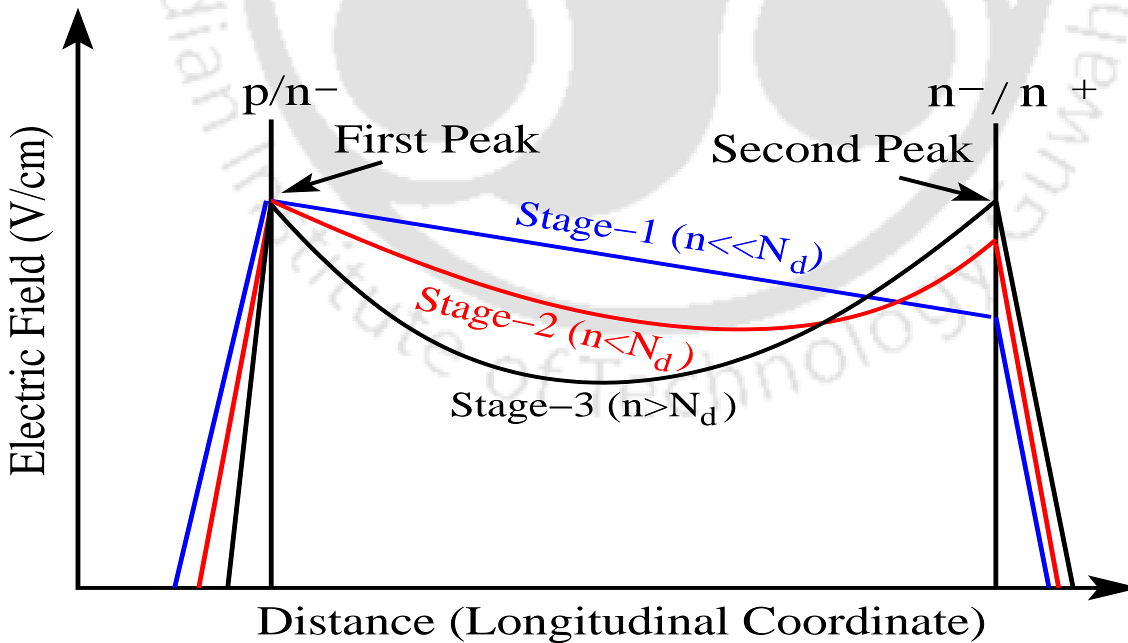

Figure 1.2: Absolute electric field distributions at different value of current densities during reverse recovery mode of high voltage diode.

Initially, the diode is reverse biased, thus it conducts very small current density at stage-1. The strength of electric field in the lightly doped (n^-) region is evaluated through the given value of

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doping density (N_d). However, the shape of electric field changes as the impact-ionization process is initiated at p/n^- junction. The avalanche-generated mobile carrier (*i.e.*, hole) move towards the anode terminal and lead to increase in the space-charge density at the p^+/n^- junction. Whereas, the avalanche-generated electrons start moving towards the cathode terminal, results in a decrease in space-charge density within lightly doped (n^-) region. When the electron carrier density (J_n) becomes higher, another electric field peak is observed at the n^-/n^+ junction. The decrease of electric field profile within the depletion region for increasing current densities, the snapback mode was observed. The formation of two peaks of electric field at both the junctions and decreased values of electric field within the depleted region is also known as an Egawa-type electric field, as shown in Figure 1.2 [38]. In order to prevent catastrophic failure caused by device entering into NDR-region, a precautionary measure is to shift the operating point of the device towards high reverse current densities [42].

1.2.2 IMPATT and TRAPATT Diodes

All the avalanche or tunneling transit-time diode rely on avalanche and tunneling breakdown mechanism across the reverse-biased p/n junction which produces a huge number of mobile carriers such as; electrons and holes. Ever since the evolution of basic semiconductor theory for high voltage devices, many scientists and researchers have thought that there are possibilities to design a two-terminal device structure which possesses negative differential resistance in the current-voltage characteristics. It has been observed that IMPATT and TRAPATT diode are suitable for such applications [43].

The theory and operation of IMPATT diode can be understood by reference in which the first avalanche diode was proposed in 1958 by Read and further experimental results have been presented by Lee et al. in 1965 [44–47]. The IMPATT diode is madeup of $n^+/p/i/p^+$ layered semiconductor structure (shown in Figure 1.3), where i refers to intrinsic region. It has two different regions; (i) a very thin p-region at which static avalanche breakdown occurs, this layer is also known as avalanche region or high field region. (ii) The other region is drift region or intrinsic region where the avalanche-generated mobile carriers must drift towards the p^+ contact. The width between the i/p^+ and n^+/p junctions is referred as the space charge region. This diode is generally operated under the reverse bias conditions so that impact ionization process gets initiated. It occurs in the heavily doped p-region and corresponding electric field across the p/n junction reaches avalanche breakdown field because the applied reverse-biased voltage appears across very narrow space charge region and creates a high potential gradient, therefore any generated mobile carriers gets accelerated across the junction. An

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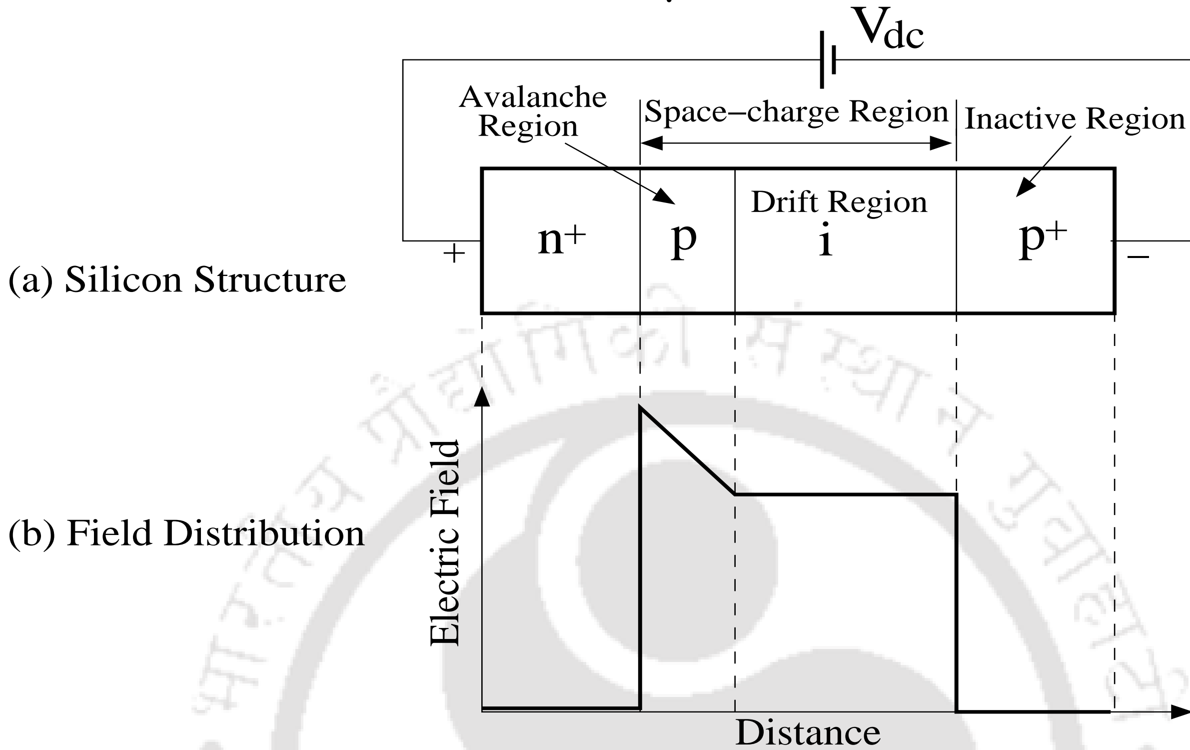

Figure 1.3: Cross-section of IMPATT diode and its electric field distribution across device structure.

avalanche generated mobile carriers start moving towards the high electric field region near the n^+/p junction achieve sufficient amount of energy to knock-out valence band electrons into the conduction band which generates a huge amount of electron and hole pairs (EHPs). An IMPATT has also shown relatively standard current-voltage characteristic, where it possesses negative differential resistance region (or snapback mode) [48, 49].

The TRAPATT mode stands for Trapped Plasma Avalanche Triggered Transit mode, which is based on the basic concept of IMPATT [31, 50]. The basic operation of semiconductor reverse-biased p/n junction diode where total current densities exceed well above those observed in normal avalanche operation of the diode. The structure of high power TRAPATT diode typically manufactured by layered silicon $p/n^-/n^+$ structure with an n-type depleted region where width is varied from $1\mu m$ to $10\mu m$. The doping of the depletion region are determined through the breakdown electric field well above saturated drift velocity level. A high current excitation across reverse-biased depletion region is required to operate the TRAPATT diode. This high current increases the electric field to critical value where impact-ionization process occurs. During this time, the electric field collapses locally in the depletion region due to generated plasma of mobile carriers. The separation of the holes and electrons are further driven by very much smaller electric field. It has been observed that some of the

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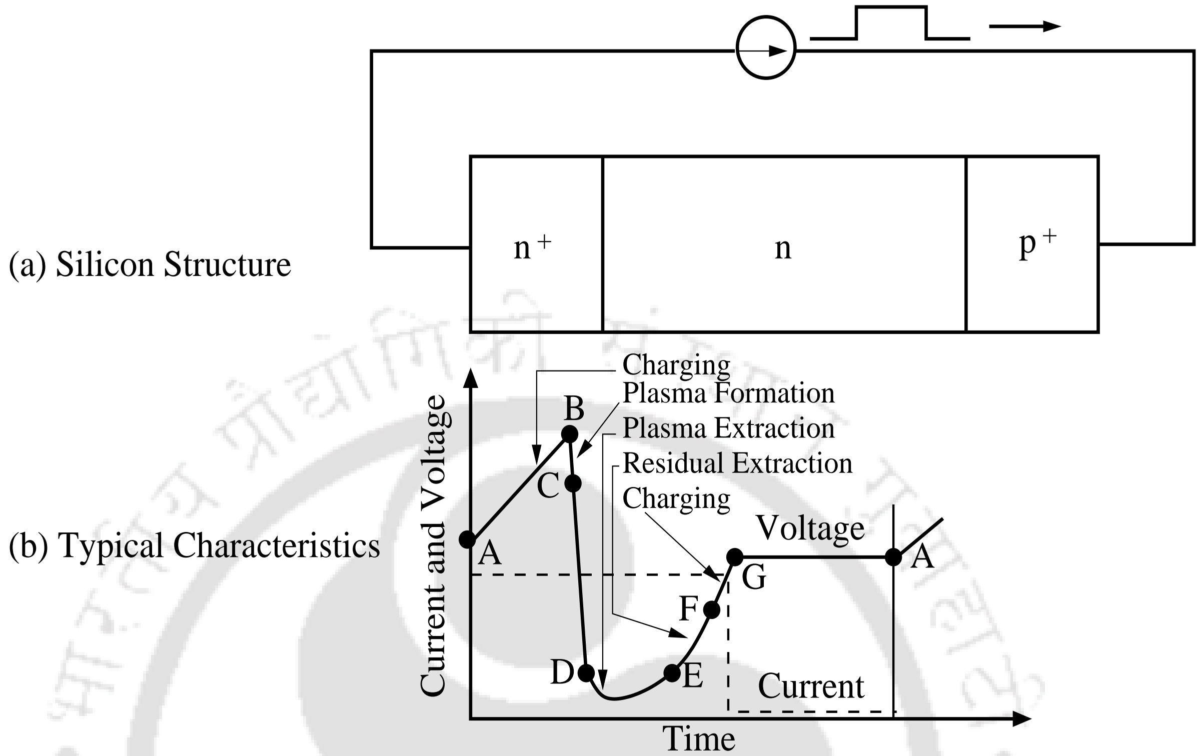

Figure 1.4: Cross-section of TRAPATT diode and its voltage-time characteristics at different points.

mobile carriers are 'trapped' behind with a velocity smaller than drift saturation velocity of carriers. As the plasma of carrier density spreads across the whole depletion region, electrons and holes start to drift to opposite terminals of the diode and then electric field further increases at the n^-/n^+ junction. The criterion for operation of TRAPATT diode is that the shock wave like wave-front propagates faster than the value of drift saturation velocity of mobile carriers.

An approximate analytical description of the TRAPATT mode in silicon layered $p^+/n/n^+$ diode structure have been proposed in 1960s by Deloach et al. and Clorfeine et al. It has been stated that an avalanche zone travels in the high field region of diode which first completely fills the depletion region with plasma of mobile carriers (i.e., electrons and holes). However, some of the mobile carriers are captured within low electric field region behind avalanche zone. The typical voltage-time characteristic of $p^+/n/n^+$ diode which was subjected to square-wave current pulse, as shown in Figure 1.4 [31]. The distribution of electric field is uniform in the entire depletion region and its value is high but less than avalanche breakdown at point A. The current density (J) in terms of electric field can be given as:

$$J = \epsilon_s \frac{dE}{dt} \tag{1.2}$$

where ϵ_s represents dielectric permittivity of the semiconductor material.

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At point A, the diode current starts to flow. Initially, very small charge carriers are present due to thermal generation in the diode, so it charges like a linear capacitor as the voltage is applied, which results in an increase in the depleted electric field to breakdown voltage. As sufficient amount of mobile carriers are generated through impact-ionization process, the displacement current far exceeds external circuit current and during this time the electric field also subsides within the depletion region, which results in collapse of load voltage (shown from point B to point C). During this time interval, the electric field at the p^+/n^- junction is sufficiently high which causes a huge amount of electron and hole pair generation, thus forms plasma of mobile carrier in the depletion region. As some of the electrons and hole move towards both the junctions, the electric field sharply decreases in the depletion region and traps remaining plasma of mobile carriers and the diode voltage decreases further from point C to D. As the time increases and reaches point E, plasma of charge carrier is removed which requires a long time compared to the charge per unit time in the external circuit. However, a residual hole charge is still present in one end of the depleted layer and residual charge of electrons at the other end of the layer. As the residual mobile charges are removed, the voltage across the device rises from point E to F. At point F, all the avalanche-generated mobile carrier internally has been completely removed. This remaining charge must be equal to or greater than that supplied to the external circuit. The TRAPATT diode charges again like a fixed capacitor and reaches from point F to point G. Finally, diode current further goes to zero as it reaches point G and the applied voltage remains constant at point A for half a period, until the current again come to the same point and so the cycle repeats. The electric field reduces according to the following equation:

$$E(x,t) = \frac{J.t}{\epsilon_s} - \frac{qN_A}{\epsilon_s}x + E_m \tag{1.3}$$

Where, $J = \epsilon_s \frac{dE}{dt}$, N_A represents doping concentration of the depletion region and E_m is the corresponding maximum electric field.

1.2.3 Avalanche Bipolar Junction Transistors (ABJTs)

The general theory of the principle and operation of high voltage bipolar transistors with negative differential resistance region at the base-collector junction has been proposed last four decade ago and the same theory is applicable to both bipolar transistors such as; $n-p-n$ and $p-n-p$ [6, 51–53]. The avalanche bipolar transistor switches from maximum collector-emitter voltage (V_{CBO}) for shorted configuration of base-emitter terminal and reaches minimum collector-emitter voltage (V_{CEO}) for

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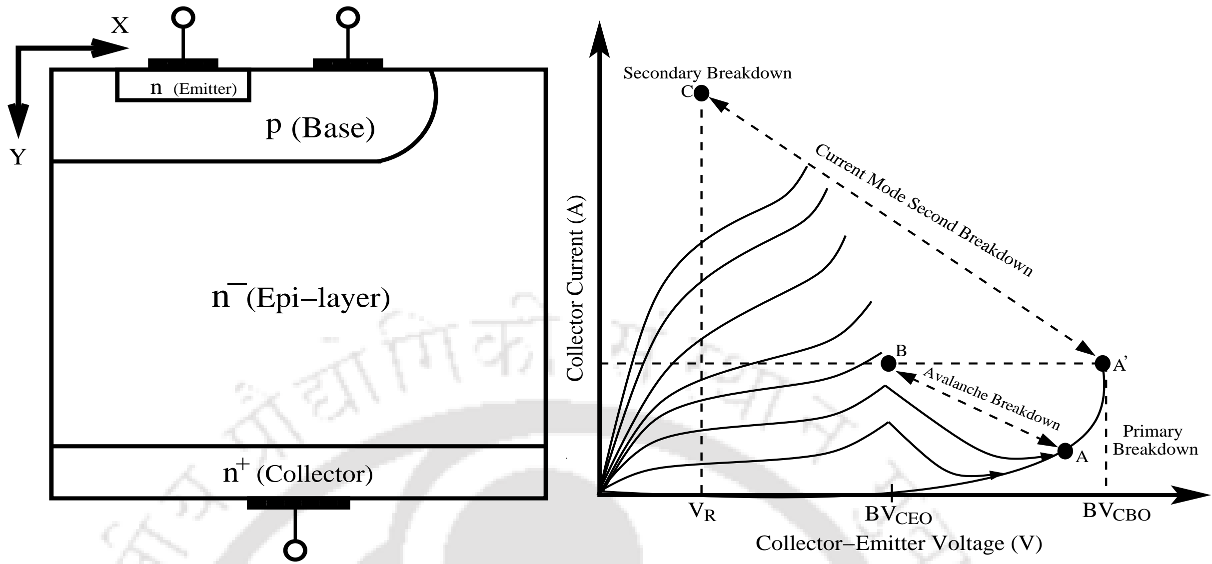

Figure 1.5: Schematic cross-section of the bipolar junction transistor and its design window under high current injection condition.

open base configuration [51]. V_{CBO} generally represents reverse biased breakdown voltage of the base-collector junction, whereas V_{CEO} has been associated with intrinsic positive feedback mechanism between weaker carrier multiplication in the depletion region of reverse biased base-collector junction and subsequently carrier injection from the emitter side. The depleted electric field has been evaluated using the value of doping concentrations of base and collector regions [54]. Accordingly, the value V_{CEO} refer to the minimum residual voltage, which can be achieved when the transistor is turned-on [55,56].

Figure 1.5 shows the standard current-voltage characteristics of commercial NPN BJTs. The load line of both avalanche and CMSB switching is completely different but begins from the same point-A (slightly below BV_{CBO}) [30,57]. In avalanche switching mode, load line roughly switches from BV_{CBO} to BV_{CEO} (i.e., from point-A to point-B) and residual collector voltage are of the order of tens of volts where collector currents are much less than $1-2A$ [58]. This mode is non-destructive and slow by nature when subjected to ultra-fast triggering pulse [59]. As the load line (point-B) is close to maximum power curve, the transistor is switches to current mode secondary breakdown region after some time delay. An application of trigger pulse to the base terminal results in shifting of operating point from A-A' to A'-C without entering the safe operating regime. In CMSB switching mode, the residual collector voltage of several hundred of volts and a current of more than $10A$ have been observed [30,51].

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1.2.4 Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs)

The basic principle of MOSFET is to control a surface current in a silicon semiconductor devices by application of an electric field [60]. In comparison to the BJT, the biggest advantages of CMOS (Complementary MOS) devices are its scalability and simpler processing along with lower power consumption [3]. As can be seen in Figure 1.6, a parasitic bipolar transistor is present in NMOS. This parasitic bipolar transistor is capable of handling high current. Hence, due to the presence of such a parasitic bipolar structure the NMOS can handle significant amount of discharging current in the snapback conduction mode [7, 21]. When high current pulses are applied to drain terminal of the ggNMOS wherein all terminals are grounded (except drain) as shown in Figure 1.6, this configuration of ggNMOS is capable to discharge large amount of current protecting other internal circuitry. Such an arrangement is widely used as a protecting elements against an ESD events [9, 18]. It exploits S-shaped current-voltage characteristic (snapback conduction mode) where it is characterized by high current and low voltage states when the protection device is subjected to high current pulse across drain terminal. The snapback mode shows the role of parasitic bipolar transistor action (Source=Emitter; Substrate=Base; Drain=Collector) which is present in the device structure, as shown in Figure 1.6. Under high current injection regimes, the device structure exhibits high impedance state when reverse-biased drain-substrate junction reaches avalanche breakdown electric field. Electron-hole pairs (EHPs) are generated at the drain-substrate junction due to the breakdown electric field, hence avalanche-generated holes are collected by grounded substrate contact while electrons are collected by the drain contact. As the avalanche injection of mobile carrier is initiated, the injection of holes from the drain-substrate ($i.e., n^-/n^+$) junction is coupled with source and substrate.

The injection of electrons from the source in the p-type substrate is related to barrier lowering, which is electro-statically coupled to injected holes. As the electron injection is initiated from the source side, the hole recombination process increases in the substrate, which results in the less potential build-up and less barrier lowering across the source and substrate junction. As electron injection is initiated from the source side and collected by the drain contact this results in the first snapback and subsequently bipolar turns on. The parasitic bipolar structure shows high forward gain by keeping the source-substrate junction forward biased. As intrinsic bipolar transistor turns on, the drain voltage reduces from the first snapback triggering point (V_{t1}, I_{t1}) to minimum value of (V_h) which results in filament formation at the n^-/n^+ junction. It has been noted in the $I - V$ characteristics that, the

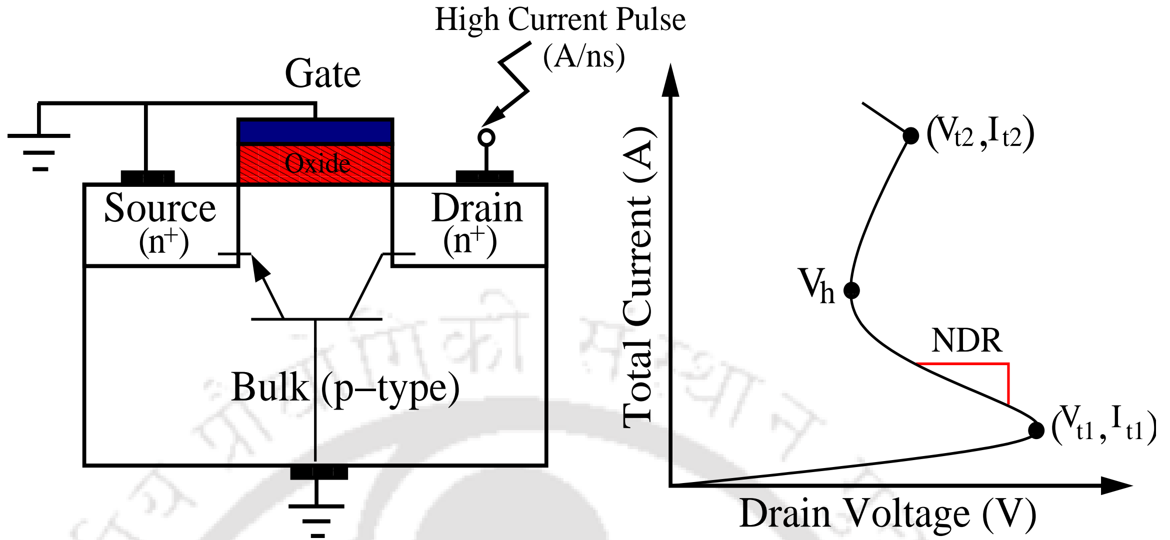

Figure 1.6: Schematic diagram of gg-NMOS in a CMOS process showing the parasitic $n-p-n$ transistor and its current-voltage characteristics when ESD pulse is applied across the drain contact.

transition from triggering voltage to holding voltage exhibits an unstable region where the devices can not be biased. This region is also known as negative differential resistivity (NDR) region which shows the switching from high impedance to low impedance state which has two stable biasing points. When holding voltage (V_h) or residual voltage is achieved, the total current is completely passed through the intrinsic parasitic bipolar transistor. Therefore, during the snapback breakdown mode, the efficient role of bipolar activity in the device structure under ultra high current injection conditions has been important to overcome the destruction of protection devices. Beyond this region, resistance again becomes positive which is also known as "on-resistance" of the protection devices. It determines shunting capabilities of the device structure, therefore less barrier lowering across the source and substrate junction are required to keep the intrinsic bipolar structure turned-on. As the total current further increases, localization of mobile carriers leads to trigger self-heating effects which increase the internal temperature of the device structure. A switching of impedance can take place again which leads to an irreversible snapback behavior thus it forces the device to enter into destruction mode, which is known as "second breakdown or thermal breakdown"and that second snapback point has been mentioned in Figure 1.6 by (V_{t2}, I_{t2}). The second breakdown of the device is generally described by the current filamentation due to an occurrence of negative resistance coefficient beyond melting temperature of silicon. This event has been observed when thermally generated mobile carrier concentrations is equal to background doping concentration of depletion region of the drain and substrate

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junction. The crucial importance of the ggNMOS transistor in current CMOS technology has shown basics of intensive studies. Most of the work on ESD protection design available in literature focuses only on optimizing the existing protection device structures to improve the ESD protection capability without concentrating on the phenomena responsible for such an event. The basic understanding of such a mechanism is very important in enhancing the reliability of ESD protection devices. The basic design approach of ESD protecting device does not change as the CMOS technology migrates from one technology node to another. The impact of process and design parameters of ggNMOS transistor is required to be clearly understood in order to obtain robust and high performance CMOS ICs. Therefore, the study of high current injection mechanism under ESD stress conditions will be useful to generate accurate and reliable compact models for circuit simulations.

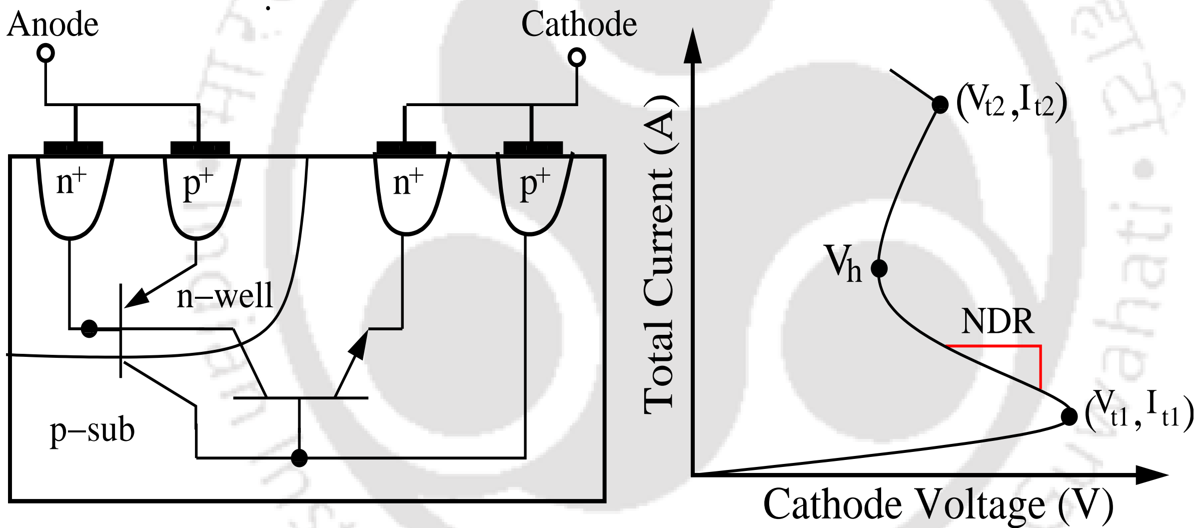

Figure 1.7: Schematic cross-section of SCR and the typical current-voltage characteristics and the design window under high current injection regimes.

1.2.5 Silicon Controlled Rectifiers (SCRs)

Silicon Controlled Rectifier (SCR) or thyristor is an active device that exploits S-shaped negative differential resistance region in current-voltage characteristics [61]. The schematic device structure of thyristor in standard complementary MOS technology (CMOS) which is made-up of silicon layered $p/n/p/n$ structure. The compact model of thyristor is generally represented by its intrinsic parasitic bipolar transistors, as shown in Figure 1.7 [61]. The p^+ diffusion in n-well region forms anode contact and n^+ diffusion in $p-sub$ region forms cathode contact of the device structure. The $p-sub$ contact is connected to the cathode terminal, however the $n-well$ contact is generally connected to an anode

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terminal. It acts as protection device of integrated circuits, when the anode terminal is connected to Input-Output (I/O) pad and cathode terminal is connected to ground level.

As the anode voltage increases further, the well-substrate junction enters in a higher reverse-biased condition until it reaches breakdown electric field. Among the two substrate parasitic bipolar transistors, one of them can abruptly turn-on depending upon the avalanche-generated current. As is obvious, the gain of $n/p/n$ bipolar transistor is higher by an order of magnitude than that of $p/n/p$ bipolar transistor, therefore $n/p/n$ bipolar transistor turns on more effectively than the later. When the intrinsic $n/p/n$ bipolar transistor turns on, the increased current leads to collapse in voltage across n-well and further turns on other parasitic $p/n/p$ bipolar transistor. The flow of current through $p/n/p$ bipolar transistor causes a voltage drop across the p-sub which helps to holds the $n/p/n$ bipolar transistor on. At this point, due to continuous current flow in parasitic $p/n/p$ bipolar transistor, there is no need for the anode terminal to provide bias of $n/p/n$ bipolar transistor. Therefore, the anode voltage is further reduced to holding voltage (V_h) which can be seen in the current-voltage characteristic of the thyristor, similar to that of gg-NMOS transistor.

1.3 Motivation for the Thesis Work

Due to aggressive scaling of the MOS transistors, ultra high current injection mechanism has shown great attention in the last one decade, typically concerning operating conditions of the semiconductor power devices and protection devices. High current avalanche injection behavior which is related to ESD stress condition, has been a well-established phenomenon in parasitic bipolar structure (i.e. $n/p/n^-/n^+$) of high voltage as well as protection devices. However, it somewhat impacts on the first snapback has not been clearly addressed in the literature. Whenever an ultra-fast variable current or voltage ramps are applied across the layered semiconductor device structure, one of the two different breakdown mode *(i.e. either snapback or non-snapback)* is observed. This non-deterministic snapback behavior of the intrinsic bipolar transistor has not been clearly addressed in the literature, even though these parasitic bipolar transistors in high voltage devices have shown an impact on snapback mechanism since last two decades. The analysis for non-deterministic snapback behavior presented in this thesis will be critical for modeling the high current injection phenomenon in state of art high voltage as well as low voltage devices. Therefore, this thesis establishes new physical insights towards understanding non-deterministic snapback behavior of different configurations of the basic parasitic

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bipolar structures which can be further used in nanometer regimes complex device structure under ultra high current injection conditions.

1.4 Organization of the Thesis

This thesis establishes detailed physical insights towards understanding anomalous or non-deterministic snapback behavior of different configurations of the bipolar transistors through intensive TCAD device simulations and developed analytical model can be further used in nanometer regimes complex device structure under ultra high current injection conditions such as; ESD stress and dynamic avalanche conditions. The organization of the thesis is as follows:

- In chapter 2, a general overview of high current injection mechanism in different layered semiconductor structure and that will be used throughout the entire dissertation to better understand the phenomenon which will be presented. First, different types of breakdown phenomenon and high current injection behavior will be discussed. The basic concepts of single and twin carrier injection will be described in detailed manner. Then, the am-bipolar transport equations will be presented to point-out the limitation of the analytical approach. Finally, the physical models used in our two-dimensional (2D) through device simulations will be outlined.

- In chapter 3, we model experimental observations related to anomalous switching behavior of the bipolar transistor at variable rise time and pulse width of the base-triggering voltage ramp and supply voltages. In this experiments, we have applied variable ultra fast triggering voltage pulses across base terminal of the bipolar transistor. A qualitative analyses and numerical simulation results presented in this work including internal dynamics and transient behavior of bipolar transistor under base-triggering condition. We have also analyzed the mobile carrier distribution and formation of ionizing waves in the depletion region. The role of base width, base-transit time and recombination physics in the base region has also been studied to model the anomalous switching behavior of the bipolar transistor.

- In chapter 4, we explore the indeterminacy during bipolar turn-on and model high current injection phenomenon. In this experiments, we apply variable ultra fast voltage pulses across a bipolar structure in several configurations and observe erratic behavior of the device at intermediate speeds of the voltage ramp. Moreover, different experimental observations are confirmed

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using 2D TCAD device simulations, as we explain the generic behavior of filaments in different regimes of the ramp speed. We next revisit and analyze mobile carrier distribution and formation of ionizing waves in the depletion region and study voltage collapse due to avalanche injection and subsequently model bipolar coupling. Two basic processes leading to the bipolar coupling mechanism are identified as bipolar structure turn on.

- In chapter 5, the numerical simulation result pertaining to an application of a variable speed ultra fast pulse across base-emitter externally shorted configuration of bipolar structure is discussed. Furthermore, we use the dynamic avalanche breakdown mode to describe the instability due to variation of saturated drift velocity (V_{sat}) and impact-ionization coefficient(α). The role of mobile carriers distributions and build-up of moving ionization front are analyzed and device simulations through 2D TCAD commercially available device simulator (Sentaurus) is performed by giving a similar ramp input to the bipolar structure. Finally, the process of filamentation has been associated with an ultra short time scale event when self-reinforced ionization front is triggered in the depletion region at low V_{sat} condition.

- Chapter 6 summarizes the work presented in this dissertation and also highlights the main contributions of the work and discusses future recommended research problems for generations of CMOS technologies.

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2

High Current Injection Mechanism in Layered Semiconductor Device Structures - A Review

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Objective

Due to continuous scaling of microelectronic devices a huge number of MOS transistors are being accommodated on a single chip [5]. This results in higher leakage current, which has been increasing rapidly due to scaling, and this increases the total power consumption of chip [1, 5]. The complex geometry of the device structures in nanometer regimes shows higher bulk leakage current due to presence of parasitics layered structures which creates reliability issues in the current CMOS technology, particularly under high current injection conditions such as: dynamic avalanche breakdown conditions, generation of ultra-fast high voltage pulses etc [47, 62]. Moreover, due to unawareness of high current injection theory and development of high current breakdown models for layered semiconductor devices, reliability study of the complex device structures has become area of interest under quasi-transient conditions [7, 63–65]. A basic concept and theory is used throughout the thesis to understand high current injection behavior of the bipolar transistors. We, first discuss the concepts of one-type of carrier injection (either electrons or holes) in semiconductor slab and then both type of carrier injections (two-type). Furthermore, physical models considered in our TCAD device simulations are discussed with particular emphasis on the avalanche breakdown dependencies. Without going much deep in theory, a phenomenological approach is presented here such that it can demonstrate a physical insight underlying the high current carrier injection problems. Therefore, we establish physical insights towards understanding breakdown phenomenon in different basic semiconductor layered structures under ultra high current injection conditions.

2.1 High Current Injection Mechanism

The understanding of high current injection theory is critical for the development of any high current breakdown models concerning layered semiconductor device structures [7, 22]. Avalanche injection has been defined in a situation where, *"the avalanche mechanism behaves as a copious source of mobile carriers which are injected into the materials"*. Under high current injection conditions, the concentration of avalanche generated mobile carriers starts to get modulated and it further exceeds the background doping concentration of reverse biased base-collector depletion region [33, 51, 66]. Mathematically, the value is correlated with critical current density:

$$J_{cr} = qN_d v_{ns} \tag{2.1}$$

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where, q represents the electron charge, N_d is background doping concentration of depletion region and v_{ns} represents drift saturated velocity of electron [7]. If total current density is less than or equal to critical current density (i.e., $J \leq J_{cr}$), it is called as low level current injection mechanism. The problem in this work is addressed to solve several degrees of complexities in a semiconductor like observing the dynamics of single carrier injection to twin type carrier injection.

2.1.1 One-type carrier injection

Figure 2.1 shows the specimen of "one-dimensional" silicon substrate of length (L) with two electrodes where anode and cathode is connected on either side of it [7]. The study of given specimen for one-type carrier injection is characterized through one electrode (*i.e.*, anode), which has the ability of mobile carrier (hole) injection in the semiconductor slab. It is assumed that contact is ohmic and infinite reservoir of mobile carrier (i.e., hole), is available for injection in the slab. In this case, our analysis is only focused on average values of all quantities involved such as: trap-free charge concentrations, mobile-carrier drift velocities and the electric field. These assumptions are valid because spatial change of these quantities are limited in the case of lateral flow of current, hence diffusion component of the current can be neglected. The following assumptions are made: (i) semiconductor slab is doped with either donor or acceptor impurities, and (ii) slab is trap free.

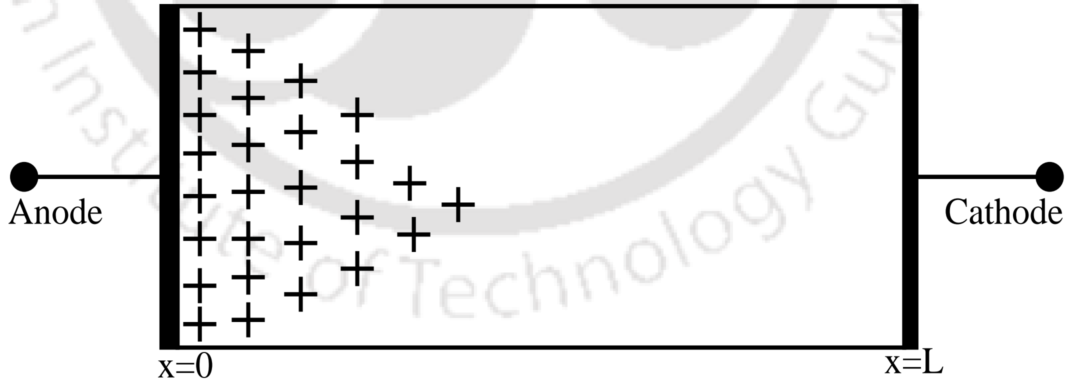

Figure 2.1: Schematic diagram of one-dimensional semiconductor slab under consideration for one-type carrier injection.

The total current density related to one-type carrier (electron) injection is given as:

$$J = \overline{\rho}.\overline{v_n} = \frac{Q}{t_{tr}} \tag{2.2}$$

where, $\overline{v_n}$ represents average drift velocity of mobile electron, $\overline{\rho}$ depicts average injected mobile carrier concentration, Q is total mobile charge carrier density and t_{tr} is transit time of free electron between

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cathode and anode having distance L. The relationships between the parameters introduced in above equation 2.2 can be expressed as:

$$t_{tr} = \frac{L}{v_n} \Rightarrow Q = \overline{\rho}.L \tag{2.3}$$

For a parallel plate capacitor we can write, $C_0 = \epsilon/L$, similarly an expression can be analogously written as $Q = C.V$, where it is assumed that the injected mobile charges were distributed uniformly between the two contacts and the average distance between electrodes would be $L/2$. Therefore, the capacitance would be doubled in comparison to parallel plate capacitance. However, some of the mobile charges were injected from the contacts (i.e., anode), non-uniform distribution of the injected charge is observed with the distance between L and $L/2$. Hence, it can be expressed as $C_0 < C < 2C_0$.

$$Q \cong C_0.V = \left(\frac{\epsilon}{L}\right) V \tag{2.4}$$

Combining equations 2.2 and 2.4,

$$J \cong C_0 \overline{v_n} \frac{V}{L} = \epsilon \overline{v_n} \frac{V}{L^2} \tag{2.5}$$

At low electric field, saturated drift velocity of electron is proportional to applied electric field:

$$\overline{v_n} = \mu_n E = \mu_n \left(\frac{V}{L}\right) \quad and \quad t_{tr} = \frac{L^2}{\mu_n V} \tag{2.6}$$

Therefore, equation 2.5 and 2.6 can be combined and written as:

$$J \cong \epsilon \mu_n \left(\frac{V^2}{L^3}\right) \tag{2.7}$$

In order to obtain exact solution, Poisson's and continuity equations are solved as given below:

$$\left\{ \begin{matrix} J = q\mu_n n(x) E(x) & Current \ \ relation \\ \epsilon \frac{dE}{dx} = qn(x) & Poisson \ \ equation \end{matrix} \right\} \tag{2.8}$$

After combining Poisson's and continuity equations, we have;

$$J = \epsilon \mu_n E(x) \frac{dE(x)}{dx} \tag{2.9}$$

Integrating equation 2.9 and applying boundary condition at $x = 0$ yields:

$$E(x) = \left(\frac{2J_x}{\mu_n \epsilon}\right)^{1/2} \tag{2.10}$$

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Again integrating equation 2.10 between the electrodes from 0 to L, we obtain:

$$J \cong \frac{9}{8}\epsilon\mu_n\left(\frac{V^2}{L^3}\right) \tag{2.11}$$

Equation 2.11 is found to conflict with equation 2.7 by a factor of 9/8. Although an idealized $1-D$ slab was under consideration, the obtained results are however very helpful. It can be shown that equation 2.11 is still useful at high electric fields, the drift velocity becomes independent of the E-field and the concept of mobility becomes useless. At low-fields, the mobility is independent of the electric field.

2.1.2 Twin-type carrier injection

When voltage of proper polarity is applied across the slab where one contact injects electron and other contact start injecting hole in the semiconductor slab which is under observation, a double injection of mobile carriers are obtained, as shown in Figure 2.2. Since both the injected mobile carriers neutralize each other in the material, this results in larger twin-carrier injection current than that of one-type carrier injection current in the same semiconductor slab. The injected holes and electrons recombine mutually before they are collected by their respective contacts. However, due to recombination of injected electron and holes with each other, increases the leakage current. In the case of silicon which is indirect gap material, wide range of injection level and phonon-assisted recombination are observed through SRH recombination (deep impurity levels). At high current injection conditions, direct recombination of hole and electrons are accompanied by the energy transfer to another mobile carriers hole/electrons. This is also known as Auger recombination. Under this condition, it has been observed in the past that the current is limited by space charge modulation [67]. Therefore, the Poisson's equation can be written as:

$$\epsilon\frac{dE}{dx} = \rho_{total} = \overline{\rho} + \rho_T \tag{2.12}$$

Above equation 2.12, shows that the total current density (J) is dependent on fixed applied voltage (V), thus finite build-up of electric field across space charge region in the bulk. Twin-carrier induced current is calculated based on the amount of injected plasma of mobile carriers in semiconductor material. The following assumptions are considered while defining the plasma:

- The average injected hole and electron concentrations are approximately equal but higher than background doping concentration of semiconductor slab.

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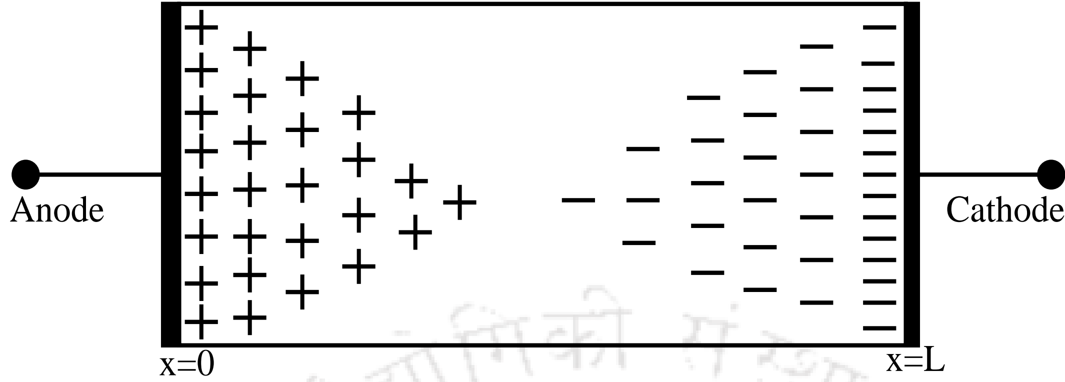

Figure 2.2: An illustrative cross-section of one-dimensional semiconductor slab under the consideration for twin-type carrier injection.

- The concentration of localized-defect states are considered small enough, hence any change in their occupancies may be neglected: this implies constant life-time of mobile carriers.

We consider that the plasma of mobile carrier are injected into slab of an n-type semiconductor ($p_0 < n_0$) having two electrodes, where injection of holes was facilitated through anode at $x = 0$ and electron was injected through cathode at $x = L$. Hence the following set of basic equations which describes injection of mobile carriers in semiconductor slab can be given as:

$$\begin{cases} J_n = qn\mu_n E \qquad J_p = qp\mu_p E \\ n - p = n_0 - p_0 \\ \frac{1}{q}\frac{\partial J_n}{\partial x} = \mu_n \frac{\partial}{\partial x}(nE) = \frac{n}{\tau} = r_n \\ -\frac{1}{q}\frac{\partial J_p}{\partial x} = \mu_p \frac{\partial}{\partial x}(pE) = \frac{p}{\tau} = r_p \\ n \approx >> n_0, p_0 \end{cases} \tag{2.13}$$

Replacing $b = \mu_n/\mu_p$, we can re-write equation2.13:

$$J = J_n + J_p = q(b+1)n\mu_p E \tag{2.14}$$

When all the above equations of 2.13 and 2.14 are solved then, we obtain:

$$E\left(\frac{dE}{dx}\right) = \frac{J}{[q(n_0 - p_0)\mu_p\mu_n\tau]} \tag{2.15}$$

Equation 2.15 is differential equation which is of first-order and similar to equation 2.9. Also the same boundary conditions are assumed, *i.e.*, $E(0) = 0$. Therefore, the solution is given below as:

$$J = \frac{9}{8}q(n_0 - p_0)\mu_p\mu_n\tau\left(\frac{V^2}{L^3}\right) \tag{2.16}$$

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It can be noted that the injection of plasma of mobile carriers in the semiconductor slab will have the same current-voltage characteristics as one-type carrier injection in the material without traps and thermal free carriers. However, twin-carrier injection in the semiconductor slab has shown various hidden effects such as: current limitation due to space charge limited transport, current channel formation at the contacts, etc.

2.2 Analytical Approach to High Current Injection in Semiconductor Device Structures

The coupling of a formidable set of semiconductor device equations such as; Poisson's and continuity equations for holes and electrons, solves analytically in few simplified cases [68]. However, it is preferable to derive analytical solutions because they physically describe phenomenon under a particular conditions [7]. Due to complexity of solutions, these equations are numerically solved through either finite-element method (FEM) or finite-difference method (FDM) [69]. In order to perform numerical simulations, physical models need to be incorporated under particular conditions but in many of the cases it is very difficult to assign proper consistent physical models. Therefore, many numerical simulations are performed generally by varying several device parameters. Under these circumstances it is very difficult to obtain a predictable results. In this section, we introduce a simple analytical approach to solve the mentioned set of Poisson's and continuity equations, under quasi-neutrality condition. It allows us to derive the analytical solutions by convoluted mechanism in layered device structures at low-level carrier injection as well as under high-level carrier injection condition. This approach is also known as am-bipolar transport, where this term has been first introduced by Roosbroek et al [70]. Here, the heat equation has not been included because it would increase an enormous analytical complexity, therefore self-heating effects are neglected in the following set of equations: Under the steady-state conditions, the continuity equations for holes and electrons are given as:

$$D_n \frac{\partial^2 n}{\partial x^2} + \mu_n E \frac{\partial n}{\partial x} + \mu_n n \frac{\partial E}{\partial x} - U = 0 \tag{2.17}$$

$$D_p \frac{\partial^2 p}{\partial x^2} - \mu_p E \frac{\partial p}{\partial x} - \mu_p p \frac{\partial E}{\partial x} - U = 0 \tag{2.18}$$

When equation 2.17 is multiplied by factor of $\mu_p.p$ and equation 2.18 is multiplied by factor of $\mu_n.n$, we get:

$$D_n \mu_p p \frac{\partial^2 n}{\partial x^2} + \mu_n \mu_p p E \frac{\partial n}{\partial x} + \mu_n \mu_p p n \frac{\partial E}{\partial x} - \mu_p p U = 0 \tag{2.19}$$

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$$D_p\mu_n n\frac{\partial^2 p}{\partial x^2} - \mu_p\mu_n nE\frac{\partial p}{\partial x} - \mu_p\mu_n np\frac{\partial E}{\partial x} - \mu_n nU = 0 \tag{2.20}$$

To establish the quasi-neutrality in the semiconductor slab, we have:

$$\begin{cases} p' = p - p_0 & excess\ \ of\ \ injected\ \ holes, \\ n' = n - n_0 & excess\ \ of\ \ injected\ \ electrons \\ \quad and & \\ \quad n' = p' & \end{cases} \tag{2.21}$$

The above condition shows that:

$$\frac{\partial n'}{\partial x} = \frac{\partial p'}{\partial x} = \frac{\partial n}{\partial x} = \frac{\partial p}{\partial x} \tag{2.22}$$

Adding equation 2.19 and 2.20, and putting the above quasi-neutrality condition in equation 2.21 and then dividing it by $[\mu_p p + \mu_n n]$, then we get:

$$\frac{\mu_p pD_n + \mu_n nD_p}{\mu_p p + \mu_n n}\frac{\partial^2 p}{\partial x^2} - \frac{\mu_p\mu_n(n-p)}{\mu_p p + \mu_n n}E\frac{\partial p}{\partial x} - U = 0 \tag{2.23}$$

Here we define:

$$D_A = \frac{\mu_p pD_n + \mu_n nD_p}{\mu_p p + \mu_n n} = \frac{\frac{D_p}{V_T}pD_n + \frac{D_n}{V_T}nD_p}{\frac{D_p}{V_T}p + \frac{D_n}{V_T}n} = \frac{D_nD_p(n+p)}{nD_n + pD_p} \equiv Am-bipolar\ \ diffusion\ \ coefficient$$

arranging above equation in terms of D_A, we have:

$$\frac{1}{D_A} = \frac{1}{D_p}\frac{n}{n+p} + \frac{1}{D_n}\frac{p}{n+p} \tag{2.24}$$

Analogously we define:

$$\mu_A = \frac{\mu_p\mu_n(n-p)}{\mu_p p + \mu_n n} \equiv Am - bipolar\ \ mobility \tag{2.25}$$

To obtain better physical insight on the am-bipolar mobility, above equation can be re-written as:

$$\frac{1}{\mu_A} = \frac{1}{\mu_p}\frac{n}{(n-p)} + \frac{1}{\mu_n}\frac{p}{(n-p)} = \frac{1}{\mu_p}\frac{n}{(n_0-p_0)} + \frac{1}{\mu_n}\frac{p}{(n_0-p_0)} \tag{2.26}$$

The above expression shows an average mobility with respect to net concentration of total charge. Therefore, we have considered an n-type silicon slab with spacing of L between anode and cathode, as shown in Figure 2.3.

Let us suppose that a plasma of mobile charges are injected over thickness $d << L$ of the cross-section of semiconductor slab. The average mobile carrier concentrations in plasma region are "p''" (for excess holes) and $n = p'' + n_0$ (for excess electrons, where n_0 represents initial concentration

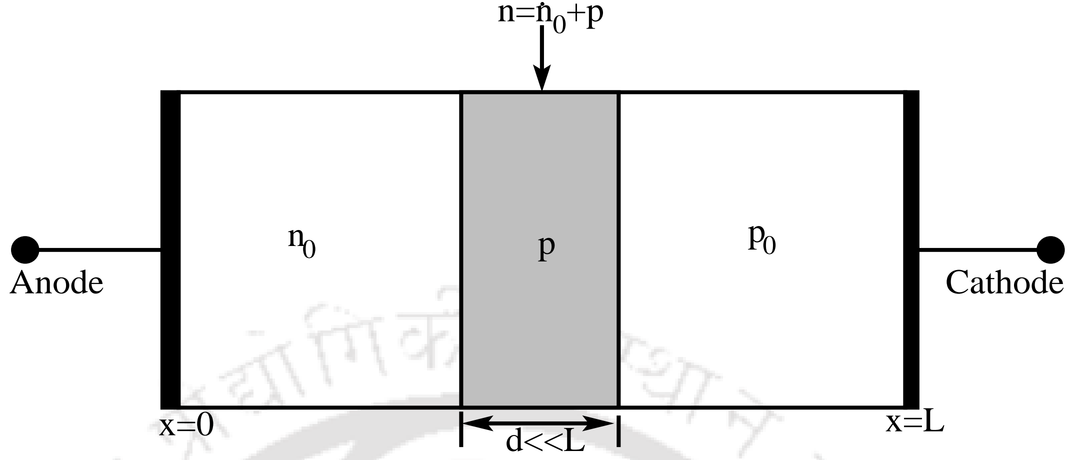

Figure 2.3: Cross-section of an n-type semiconductor slab where the plasma of mobile carriers are injected over thickness $d << L$.

in one-dimensional specimen). The electric field distribution inside the plasma region is E_P and the electric field strength is V/L elsewhere (because we assume $d << L$). The total currents outside and inside the plasma region under steady-state condition, must be equal i.e.,

$$J = q(n_0 + p)\mu_n E_p + qp\mu_p E_p = qn_0\mu_n \frac{V}{L} \tag{2.27}$$

Solving for E_P, we obtain:

$$E_p = \frac{\mu_n n_0}{\mu_n(p + n_0) + p\mu_p}\left(\frac{V}{L}\right) \tag{2.28}$$

The hole moves from left to right towards a region where space-charge is neutralized due to build-up of electric field in the plasma region, as shown in Figure 2.3. The speed and direction of the hole movement along with plasma region migration indicates that these moving particles travel with an am-bipolar drift velocity v_a which is same as the hole drift velocity v_p. Hence, we can write:

$$v_a = \mu_p E_p = \mu_a \left(\frac{V}{L}\right) \tag{2.29}$$

Now, we can obtain the am-bipolar drift mobility as:

$$\mu_a = \frac{\mu_n \mu_p n_0}{p\mu_p + \mu_n(p + n_0)} = \frac{n - p}{\frac{n}{\mu_p} + \frac{p}{\mu_n}} \tag{2.30}$$

Therefore, the am-bipolar mobility can be physically termed as group mobility for drift velocities of excess hole (p) and electron (n) under influence of depleted electric field (E_p). Using the derived expression of am-bipolar mobility and diffusion coefficient, the complete am-bipolar transport equation

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can be obtained as:

$$D_A \frac{\partial^2 p}{\partial x^2} - \mu_A E \frac{\partial p}{\partial x} - U = 0 \tag{2.31}$$

Now, we consider how the above equation 2.31 varies depending on the different injection levels of the carriers. It can be analyzed by imposing quasi-neutrality condition and by introducing the excess carrier concentration in the derived equations of the am-bipolar mobility, so we have:

$$\mu_A \equiv \frac{(n-p)\mu_p\mu_n}{\mu_p p + \mu_n n} = \frac{(n_0 + n' - p_0 - p')\mu_p\mu_n}{\mu_p p_0 + \mu_n n_0 + \mu_n n' + \mu_p p'} \cong \frac{n_0\mu_n\mu_p}{(\mu_n + \mu_p)p' + \mu_n n_0} \tag{2.32}$$

Analogously, we obtain am-bipolar diffusion coefficient as:

$$D_A = \frac{D_n D_p(n+p)}{D_n n + D_p p} = \frac{D_n D_p(n_0 + n' + p_0 + p')}{D_n n_0 + D_p p_0 + D_n n' + D_p p'} \cong \frac{D_n D_p(n_0 + 2p')}{p'(D_n + D_p) + n_0 D_n} \tag{2.33}$$

Similarly, we can derive an expression for net recombination rate. Silicon is an indirect band-gap material, so, U is given by SRH recombination equation, where low level injection is assumed. In case of high level injection of mobile carriers Auger recombination is observed. We can now write an expression for U as:

$$U = \frac{np - n_i^2}{\tau_{n_0}(p + p_1) + \tau_{p_0}(n + n_1)} \approx \frac{n_0 p' + p'^2}{\tau_\infty p' + \tau_{p_0} n_0)} \tag{2.34}$$

At two different injection levels, such as:

(i) Low-level carrier injection;

This condition is generally characterized by following equation:

$$\frac{p'}{n_0} \to 0 \tag{2.35}$$

Therefore the following terms μ_a, D_a and U can be reduced to:

$$\begin{cases} U \to \frac{p'}{\tau_{p0}} \\ \mu_A \to \mu_p \\ D_A \to D_p \end{cases} \tag{2.36}$$

Under the above stated conditions, the amplitude of applied electric field is very small. So, am-bipolar transport equation can be given as:

$$D_p \frac{\partial^2 p}{\partial x^2} = \frac{p'}{\tau_{p0}} \tag{2.37}$$

and then it can be solved further to obtain familiar minority carrier diffusion equation.

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(ii) High-level carrier injection;

In this case we have:

$$\frac{p'}{n_0} \to \infty \tag{2.38}$$

Therefore the following terms μ_a, D_a and U can be reduced to:

$$\begin{cases} U \to \frac{\partial p}{\tau_\infty} \\ D_A \to D_\infty = \frac{2D_nD_p}{D_n+D_p} \\ \mu_A \to 0 \end{cases} \tag{2.39}$$

Finally, the am-bipolar transport equation gets reduced to:

$$D_\infty \frac{\partial^2 p}{\partial x^2} = \frac{p'}{\tau_{p0} + \tau_{p0}} \tag{2.40}$$

The solution of am-bipolar transport equations allows to represent high current injection equations in terms of low-level carrier injection equations (where t_{p0} is replaced with τ_A and D_p is replaced with D_A) which provides meaningful physical interpretation. In this section, we have outlined the main concepts of injection theory in the semiconductor slab and particular focus has been laid on difference between single carrier injection and double carrier injection currents under quasi-neutrality condition. The am-bipolar transport equation in terms of drift-diffusion transport equations of both the carriers has been outlined to develop analytical solutions to high current injection problems.

2.3 Numerical Simulation and Parameter Modeling under High Current Injection Conditions

In this section, the main numerical simulation tool which will be used in the entire thesis are presented and the important physical models used in device simulator under high current conditions have been discussed, particularly in the context of basic drift-diffusion transport model. Additionally the basic equations of semiconductor device and a short discussion on modeling of the important parameters like carrier mobility, generation/recombination are also outlined. To define the behavior of a complete system which is subjected to external circuit setup, the basic set of semiconductor device equations are solved numerically. The situation becomes more challenging when dealing with nanometer scaled complex device structures, in which it is very difficult to extract an analytical solution under high current injection conditions. In order to obtain reliable simulation results, it is

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very important to distinguish as to which physical models should be implemented to obtain realistic behavior of complex device structure under high voltage and current conditions. In particular, when dealing with high current injection mechanism, particular care must be taken care in the device simulation setup [68, 71]. Therefore, we have reviewed the physical models which are implemented in the device simulator in the following sub-sections.

2.3.1 Basic Semiconductor Equations

To know the distribution of current density and potential inside any arbitrary semiconductor device under various operating conditions, the structure needs to be modeled numerically using the following equations.

2.3.1.1 Poisson's and Continuity Equation

Poisson's equation and the continuity equations is a basic set of semiconductor equation which have been derived from the Maxwell's equation.

(i) Poisson's equation is effectively Maxwell's third equation which is

$$div\left(\vec{D}\right) = \rho; \tag{2.41}$$

Where:

$\vec{D}$ - Displacement vector

ρ - Electric charge density

The relation between displacement vector and electric field $\vec{E}$ is given as:

$$\vec{D} = \epsilon.\vec{E} \tag{2.42}$$

If permittivity ϵ is homogeneous, then the relation between electric field $\vec{E}$ and electrostatic potential ψ can be given as:

$$\vec{E} = -grad\psi \tag{2.43}$$

Substituting equations 2.42 and 2.43 in equation 2.41 gives the well known form of Poisson's equation;

$$div\left(grad\psi\right) = -\frac{\rho}{\epsilon} \tag{2.44}$$

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Charge density ρ is given as:

$$\rho = q\,(C + p - n) \tag{2.45}$$

Where,

C = Immobile charge concentration

n = Negatively charged electron concentration

p = Positively charged hole concentration

q = Elementary electronic charge.

Substituting equation 2.45 in 2.44 gives final expression of the Poisson's equation as:

$$div\,(grad\psi) = -\frac{q\,(C + p - n)}{\epsilon} \tag{2.46}$$

(ii) Continuity equation can be derived in a straight forward approach from Maxwells first equation which can be given as:

$$curl\vec{H} = \vec{J} + \frac{\partial \vec{D}}{\partial t}; \tag{2.47}$$

$$div.curl\vec{H} = div.\vec{J} + \frac{\partial \rho}{\partial t} = 0; \tag{2.48}$$

in equation 2.48 current density $\vec{J}$ can be split into hole current density $\left(\vec{J_p}\right)$ and electron current density $\left(\vec{J_n}\right)$ and assuming static charges time invariant system $\frac{\partial C}{\partial t} = 0$, we can write:

$$div\left(\vec{J_p} + \vec{J_n}\right) + q.\frac{\partial\,(p - n)}{\partial t} = 0; \tag{2.49}$$

the above equation 2.49 can be re-written as:

$$div\left(\vec{J_n}\right) - q.\frac{\partial n}{\partial t} = q.R; \tag{2.50}$$

$$div\left(\vec{J_p}\right) + q.\frac{\partial p}{\partial t} = -q.R; \tag{2.51}$$

Where,

R = Net recombination rate of carriers

$\frac{\partial\ (n,p)}{\partial t}$ = Net build-up of mobile carriers.

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2.3.1.2 Carrier Transport Equations

The Boltzmann's transport equation (BTE) is an approximate semi-classical description of carrier transport in lattice. This transport equation represents evolution of the distribution function in all six-dimensional phase space (x, y, z, p_x, p_y, p_z) [70]. However, an analytical solutions can be obtained only for periodic and simple configurations of lattice. One simple approach to find the solution of BTE in any arbitrary semiconductor structures is the *Monte Carlo simulation*, which can provide highly accurate and reliable results. However, it is computationally very expensive due to statistical nature of the Monte Carlo simulation. Due to very good agreement with the experimental results, it is generally used as reference for the generation of simpler analytical models.

As the technology node moves towards nanometer regime, numerical device simulations require simpler as well as efficient transport equations, which solves complex differential equations of semiconductor within reasonable time and should be computationally inexpensive. One approach is to perform this simplification by considering only moments of distribution function. To derive the higher order of transport equations or Hydrodynamic and Thermodynamic transport models for nanoscale devices, higher number of moments are considered in the model. The well known drift-diffusion model is derived based on first two moment of distribution.

2.3.1.3 Drift-Diffusion Equation

In the starting of semiconductor technology Drift-Diffusion (DD) model for career transport was used to model the basic characteristics of the device. As size of the device started to reduce, many assumptions underlying the DD model became invalid and hence it was refined to take into consideration the effects like velocity saturation. Drift Diffusion Equation as the name suggests is the combination of carrier transport due to diffusion and drift inside the device which is given as follows:

$$\vec{J_n} = q.n.\mu_n.\vec{E} + q.D_n.grad\ n; \tag{2.52}$$

$$\vec{J_p} = q.p.\mu_p.\vec{E} - q.D_p.grad\ p; \tag{2.53}$$

Where,

$\vec{J_{n,p}}$ - Current density

$\mu_{n,p}$ - Field dependent mobility of carriers

$D_{n,p}$ - Diffusion coefficient

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By substituting the equations 2.52 and 2.53 in equations 2.50 and 2.51 and making the time dependent term equal to zero (as we need to consider quasi steady state analysis for plotting the current-voltage characteristics), we get the final form of continuity equations as given in 2.54 and 2.55, these two equations along with the Poisson's equation given in equation 2.46 forms the system of basic semiconductor equations that need to be solved are.

$$div\,(D_n.grad\;n - \mu_n.n.grad\;\psi) = R\,(\psi, n, p) \tag{2.54}$$

$$div\,(D_p.grad\;p + \mu_p.p.grad\;\psi) = R\,(\psi, n, p) \tag{2.55}$$

2.3.2 Device Parameter Modeling

The semiconductor equations discussed in the above subsections show basic relationships between the electrostatic potential and carrier distribution. The mobility and recombination rate are two different physical parameters which needs appropriate modeling to describe the occurrence of physical mechanism in device structures. These parameters will be discussed in details in the following subsections.

2.3.2.1 Empirical mobility models of carriers

The derivation of empirical model for mobility originates from relaxation time of mobile carrier in the lattice. Therefore, it is influenced by scattering mechanism in lattice due to thermal vibrations, interface charges and traps, energy of the carriers, impurity atoms, surfaces and interfaces and other effects such as lattice defects [72]. Various mobility models are used during the numerical simulation to capture these effects in continuous system [73–75]. The empirical approaches are generally used to derive exact solutions. Some of scattering effects used in the mobility model will be presented in the following section.

(i) Lattice scattering:

The basic means by which carriers get scattered is thermally generated vibrations of atoms called as lattice scattering. Sah et al. have reported an empirical model [76] to predict the mobility values of silicon accurately in the temperature range of [4,2,600]K given as:

$$\mu_n^L = \frac{1}{\frac{1}{4195.\frac{cm^2}{V.s}.\left(\frac{T}{300K}\right)^{-1.5}} + \frac{1}{2153.\frac{cm^2}{V.s}.\left(\frac{T}{300K}\right)^{-3.13}}} \tag{2.56}$$

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$$\mu_p^L = \frac{1}{\frac{1}{2502.\frac{cm^2}{V.s}.\left(\frac{T}{300K}\right)^{-1.5}} + \frac{1}{591.\frac{cm^2}{V.s}.\left(\frac{T}{300K}\right)^{-3.25}}} \tag{2.57}$$

(ii) Ionized impurity scattering:

An approach for modeling the combined effects of lattice and ionized impurity scattering has been proposed by Caughey and Thomas [77] using experimental data as:

$$\mu_{n,p}^{LI} = \mu_{n,p}^{min} + \frac{\mu_{n,p}^{L} - \mu_{n,p}^{min}}{1 + \left(\frac{CI}{C_{n,p}^{ref}}\right)^{\alpha_{n,p}}} \tag{2.58}$$

Above equation also considers the saturation effect and mobility degradation due to high impurity concentration level.

(iii) Carrier-Carrier scattering:

In power devices operating in on-state, carrier-carrier scattering can become more pronounced as the free carrier concentration may become far more than the doping concentration. Adler et al. [78] suggested a model where carrier-carrier scattering can be accounted by adding an additional term in the Caughey and Thomas equation:

$$\mu_{n,p}^{LIC} = \mu_{n,p}^{min} + \frac{\mu_{n,p}^{L} - \mu_{n,p}^{min}}{1 + \left(\frac{CI}{C_{n,p}^{ref}}\right)^{\alpha_{n,p}} + \left(\frac{\sqrt{n.p}}{14.C_{n,p}^{ref}}\right)^{\alpha_{n,p}}} \tag{2.59}$$

Neutral impurity scattering mechanism becomes significant at low temperature (nearly 77K) and can be safely neglected for room temperature hence it is not being taken into consideration.

(iv) Velocity saturation:

The effect of saturation velocity of carriers at higher electric fields can be taken into account using the expression;

$$\mu_{n,p}^{LICE} = \frac{\mu_{n,p}{}^{LICE}}{\left(1 + \left(\frac{\mu_{n,p}^{LIC}.E_{n,p}}{\nu_{n,p}^{sat}}\right)^{\beta_{n,p}}\right)^{\frac{1}{\beta_{n,p}}}} \tag{2.60}$$

The values of constants used in the mobility models stated above are summarized in the Table 2.1.

2.3.2.2 Models for Generation-Recombination of carriers

From a physical point of view, the term recombination rate, R was introduced to include generation and recombination of electron-hole pairs in standard drift-diffusion transport equations (2.50 and 2.51)

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Constants	Units	Value for electrons	Value for holes
μ^{min}	$\frac{cm^2}{V.s}$	65	47.7
α	no units	0.72	0.76
β	no units	2	1
C^{ref}	cm^{-3}	$8.5 * 10^{16}$	$6.3 * 10^{16}$
ν^{sat}	$\frac{cm}{s}$	$1.1 * 10^{7}$	$9.5 * 10^{6}$

Table 2.1: Constants used in mobility modeling equations.

by separating the continuity equation into two different parts for holes and electrons. When the lattice is in thermal equilibrium, mobile carrier recombination and generation are balanced, thus carrier concentration values are calculated by their equilibrium values n_0 and p_0 ($n_0 p_0 = n_i^2$). It is observed that, a low carrier concentration results in increased generation, but excess number of mobile carriers leads to an increased recombination. The generation as well as recombination processes contribute to calculate total net generation rate effectively based on different physical effects which are modeled independently of each other. The separately evaluated models add up to total net recombination rate and resulting rate is considered in the continuity equations.

(i) Phonon transition or SRH generation recombination:

A theory about phonon transition was published by Shockley and Read [79] and [80] and therefore this effect is also called as SRH recombination generation rate. The phonon transition is a two step process with a trap in between conduction band and valence band. It is divided into four partial process namely;

- Electron capture: a free electron from the conduction band may be trapped due to an unoccupied defect which now turn into occupied.
- Hole capture: an electron may be released from occupied trap due to thermal vibrations and moves to the valence band and neutralizes a hole which results in unoccupied trap.
- Hole emission: it occurs when free electron from the valance band gets trapped due to some defect in lattice thus leaving a hole and an occupied trap.
- Electron emission: it occurs when free electron from occupied trap moves to the conduction band leaving the trap unoccupied.

The net phonon recombination rate $\left(R^{SRH}\right)$ is

$$R^{SRH} = \frac{n.p - n_i^2}{\tau_p \left(n + n_1\right) + \tau_n \left(p + p_1\right)} \tag{2.61}$$

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Where,

$n_1 = n_0.\frac{1-f_{t0}}{f_{t0}}$

$p_1 = p_0.\frac{f_{t0}}{1-f_{t0}}$

$\tau_{n,p} = \frac{\tau_{n,p0}}{1+\frac{N_D+N_A}{N_{n,p}^{ref}}}$

f_{t0} - Fraction of traps occupied under equilibrium

$\tau_{n,p0}$ - Carrier life time under equilibrium.

(ii) Photon transition:

Photon transition takes place in a one step process (*i.e.*, it is a direct generation recombination process) and is important in narrow band gap semiconductors and semiconductors which allows direct transitions like $GaAs$. In silicon band to band transition is insignificant and can be neglected for all possible practical purposes [68].

(iii) Auger or Three particle transition:

Auger recombination can be divided into four partial process and in every partial process three carriers are involved hence the name three particle transition [81]. As a matter of fact the partial process involved in this generation/recombination are still under investigation and are understood more or less qualitatively. The four partial process are

- Electron capture: when free electron from the conduction band reaches valence band and recombines with hole. During this process, it transmits excess amount of energy to an electron present in the conduction band.
- Hole capture: when free electron from the conduction band reaches valence band which further recombines with the hole present. In this process, excess energy is transmitted in hole present in valence band which moves out from the valence band.
- Hole emission: when an electron present in the valence band reaches conduction band by consuming energy of high energetic hole in the valence band and moves out from the valence band.
- Electron emission: when an electron in the valence band reaches conduction band by consuming energy of a high energetic electron in the conduction band and a hole is left in valence band.

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From the above explanations, it can be observed that the emission rate of carriers is directly proportional to the concentration of carriers and auger emission coefficient and is independent of the current flow *i.e.*, even with negligible amount of current flow and high concentration of carriers there can be auger generation of carriers.

The net auger recombination rate $\left(R^{AU}\right)$ is;

$$R^{AU} = \left(C^{AU}_{cn}.n + C^{AU}_{cp}.p\right).\left(n.p - n_i^2\right) \tag{2.62}$$

Where

$C^{AU}_{c\ n,p}$ - Capture rate of electron and hole in auger recombination

(iv) Impact ionization:

Impact ionization is a pure generation process and there is no recombination in this process but for reasons stated before the generation rate is expressed as net recombination rate [82]. Impact ionization can be divided into two partial process as;

- Hole emission: when an electron in valence band reaches conduction band by consuming energy of a high energetic hole in the valence band and the hole is left in valence band edge.
- Electron emission: when an electron in the valence band reaches conduction band by consuming energy of a high energetic electron in the conduction band and hole is left in valence band.

The net generation rate of carriers is given as:

$$G^{II}_{n,p} = \alpha_{n,p}.\frac{\left|\vec{J_{n,p}}\right|}{q} \tag{2.63}$$

Where,

$\alpha_{n,p}$ - Ionization rate for carriers

Ionization rate is defined as the electron hole pairs generated per unit length of travel per carrier. From equation 2.63 it can be seen that a significant amount of current is necessary for impact ionization.When seen at microscopic level the Impact ionization is same as Auger generation.The net Impact Ionization recombination rate $\left(R^{II}\right)$ is;

$$R^{II} = -G^{II}_n - G^{II}_p \tag{2.64}$$

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An accurate approximation to calculate the ionization rate of carrier was given by Sutherland [83] as:

$$\alpha.\lambda = exp\left(C_0\left(r\right) + C_1\left(r\right).x + C_2\left(r\right).x^2 + C_3\left(r\right).x^3\right) \tag{2.65}$$

With

$$\begin{aligned} C_0\left(r\right) &= -\left(7.238 * 10^{-2}\right) - 51.5r + 239.6r^2 + 3357r^3 \\ C_1\left(r\right) &= -0.4844 + 12.45r + 363r^2 - 5836r^3 \\ C_2\left(r\right) &= \left(2.981 * 10^{-2}\right) - \left(7.571r * 10^{-2}\right) - 148.1r^2 + 1627r^3 \\ C_3\left(r\right) &= -\left(1.841 * 10^{-5}\right) - 0.1851r + 10.41r^2 - 95.65r^3 \end{aligned} \tag{2.66}$$

Where

$r = \frac{E_r}{E_i}$

$x = \frac{E_i}{q.\lambda.E}$

E_r - Average loss of energy per collision

E_i - Ionization Energy The effective net recombination rate is obtained by summing up all the net recombination models discussed above in equations 2.61,2.62,2.64 and is given as:

$$R = R^{II} + R^{AU} + R^{SRH} \tag{2.67}$$

The values of various constants used in the recombination models discussed above are stated in table 2.2.

Constant	units	Value for electrons	Value for holes
$\tau_{n,p0}$	s	10^{-5}	10^{-5}
$N_{n,p}^{ref}$	cm^{-3}	$3 * 10^{17}$	$3 * 10^{17}$
C_{cn}^{AU}	$cm^6.s^{-1}$	$2.8 * 10^{-31}$	$9.9 * 10^{-32}$

Table 2.2: Constants used in net recombination equations.

2.3.3 Discretization of basic semiconductor equations

We need to discretized the basic semiconductor equations to solve them numerically. Though there are many ways to discretize a the Partial differential equations like finite element method (FEM), finite volume method (FVM) and finite difference method (FDM). However, we choose to discretized using five point Finite Difference Method owing to its simplicity and good accuracy. FDM Discretized basic semiconductor equations are [69];

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- Poisson's equation:

$$\frac{n_d}{m_d}\psi(x+1,y)+\frac{n_d}{m_d}\psi(x-1,y)-2\left(\frac{n_d}{m_d}+\frac{m_d}{n_d}\right)+\frac{m_d}{n_d}\psi(x,y+1)+\frac{m_d}{n_d}\psi(x,y-1)= m_d.n_d\frac{q}{\epsilon}(n-p-C) \tag{2.68}$$

- Continuity equation for electrons:

$$n(x+1,y)\left[\frac{n_d}{m_d}-\frac{n_d}{2v_t}E_x\right]+n(x-1,y)\left[\frac{n_d}{m_d}+\frac{n_d}{2v_t}E_x\right]+n(x,y+1)\left[\frac{m_d}{n_d}-\frac{m_d}{2v_t}E_y\right]+ n(x,y-1)\left[\frac{m_d}{n_d}-\frac{m_d}{2v_t}E_y\right]-n(x,y)\left[2\left(\frac{m_d}{n_d}+\frac{n_d}{m_d}\right)+temp\right]= m_dn_d\left(\frac{R(\psi,n,p)}{D_n}+\frac{1}{D_n}\frac{\partial n}{\partial t}\right) \tag{2.69}$$

- Continuity equation for holes:

$$p(x+1,y)\left[\frac{n_d}{m_d}+\frac{n_d}{2v_t}E_x\right]+p(x-1,y)\left[\frac{n_d}{m_d}-\frac{n_d}{2v_t}E_x\right]+p(x,y+1)\left[\frac{m_d}{n_d}+\frac{m_d}{2v_t}E_y\right]+ p(x,y-1)\left[\frac{m_d}{n_d}-\frac{m_d}{2v_t}E_y\right]-p(x,y)\left[2\left(\frac{m_d}{n_d}+\frac{n_d}{m_d}\right)-temp\right]= m_dn_d\left(\frac{R(\psi,n,p)}{D_p}+\frac{1}{D_p}\frac{\partial p}{\partial t}\right) \tag{2.70}$$

Where,

$$E_x=\frac{\partial\psi}{\partial x};\ dE_x=\frac{\partial^2\psi}{\partial x^2};\ \text{and}\ E_y=\frac{\partial\psi}{\partial y};\ dE_y=\frac{\partial^2\psi}{\partial y^2};$$

m_d/n_d = horizontal/vertical differential length and E_x, dE_x, E_y and dE_y in the continuity equation can be calculated using the central difference and five point discretization method.

2.3.4 Boundary conditions for observing NDC region

Boundaries of a semiconductor device can be classified into two types such as: Physical Boundaries and Artificial Boundaries. Physical boundaries include the boundaries which physically exist like contacts and interface to the insulating material while artificial boundaries are the ones which is introduced for the purpose of simulation or calculations so that it can separate one device from the neighboring devices. Boundary conditions are mathematical conditions which are specified at the boundaries to solve the partial differential equations. In general the boundary conditions are decided by the type of contacts which is dependent on the type of the input given to the device. Broadly boundary conditions are divided as:

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- Dirichlet boundary: In Dirichlet boundary condition, as solution (potential) is initially assumed and a set of discretized partial differential equations are then solved at the boundaries. We further solve the Poissons equation with potential as the parameter and stating Dirichlet boundary condition at the boundaries which means we are fixing the value of the potential at the boundaries which is equivalent to connecting the device to a voltage source. To plot the I-V characteristics of a device with Dirichlet boundary conditions is physically equivalent to connecting the device to a variable voltage source and checking the current flowing through the device.

- Neumann boundary: Neumann boundary condition states that the derivative of solution parameter on the boundary of domain must be satisfied by the solution of partial differential equation. Physically Neumann boundary condition is applied when we have to connect the device to a current source.

2.4 High Current Injection Behavior in Different Layered Semiconductor Structures

Ultra high current avalanche injection behavior in parasitic layered device structures is a well established phenomenon [8]. It has been experimentally observed that, when an ultra-fast voltage pulse is applied across the device structures, one of two entirely different modes of breakdown phenomena (i.e., snapback or no snapback) has been observed, with the occurrence of the two modes being erratic [22,66,84]. Based on high current injection mechanisms, all these device structures (transit time diodes, power diodes, resistors and bipolar transistors) have been associated with negative differential resistance [9, 31, 40, 85], as tabulated in Table 2.3.

2.4.1 Transit-time Diodes (p/n)

In transit time diodes, the collapse of voltage across a reverse-biased p/n junction and its dependence on displacement current has been explained by the Trapped Plasma Avalanche Triggered Transit (TRAPATT) mode of operation [31, 86], involving the dynamic avalanche breakdown model. An application of a voltage pulses across a silicon layered $p/n^-/n^+$ structure with sufficient time rate of change of voltage (dv/dt) can produce plasma of electron-hole that causes the breakdown electric field to fall significantly which causes trapping of the plasma in the depletion region. Such an ionization wave front is typical of $p/n^-/n^+$ structures, where the n^- region is very lightly doped to order of

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Structure	Devices	Authors
p/n	TRAPATT IMPATT Pulse Sharpening Diode	B. Deloach et.al. [31] Y. Mizushima et. al. [46] I. V. Grekhov et. al. [29]
n^-/n^+	High Voltage Resistor	P. Hower et.al. [8]
$p^+/n^-/n^+$	Power Diode	J. Lutz et.al. [40] M. Domeij et.al. [32] H. Egawa et.al. [38]
$n/p/n^-/n^+$	Bipolar Transistor Field-Effect Transistor	P. Hower et.al. [8] M. Shrivastava et.al. [18] A. Chatterjee et.al. [9]

Table 2.3: Various layered semiconductor structure and their associated devices.

$N_D > 10^{15} cm^{-3}$ and the time of the propagation are of the order of a few hundreds of picoseconds [66]. The large displacement current has been shown to cause propagation of shock wave like pattern in the electric field across reverse-biased junction. The role of displacement current in the 2D structures have been incorporated through transient simulation using variable load resistors, which accounts for the role of increased current density for faster ramps [22]. The increased current densities leading to a double avalanche injection mechanism has not been considered during the propagation of the above phenomenon. Steady-state breakdown current results when transients involving the propagation of shock wave phenomenon had settled down for a given breakdown voltage across the device and high level of current densities causes a double injection mechanisms in $p/n^-/n^+$ structures [40, 85].

2.4.2 High Voltage Resistor ($n^+/n^-/n^+$)

A similar behavior underlying the mechanism of avalanche injection observed in silicon layered $n^+/n^-/n^+$ high voltage structure at high current injection conditions. It has been explained by saturation of mobile carrier drift velocities at breakdown electric field and charge storage in the neutral region that causes the electric field to peak at the n^-/n^+ junction [8]. It impacts the resistor as the mechanism of avalanche injection is initiated at the n^-/n^+ junction. It has been reported that, once the avalanche injection is triggered inside the device structure, a significant change has been observed in the mobile carrier distribution and electric field. However, microscopic view of injection of the carrier and the role of dynamic avalanche has not been considered.

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2.4.3 High Voltage Diodes ($p^+/n^-/n^+$)

At high current densities in the layered $p^+/n^-/n^+$ device structures, snapback mechanism has been associated with high current injection from the ohmic contact [38, 87, 88]. When the avalanche generated mobile concentration is less than the intrinsic background concentration (i.e., $n << n_i$), the maximum electric field is present at the p^+/n^- junction. Consequently, most of the charges are generated at this junction and swept toward the n^-/n^+ junction, which decreases the space charge density in the intrinsic (n^- region). Then the distribution of the absolute electric field is flatter, and as the current density increases, avalanche multiplication process is initiated in the i region. However, when $n >> n_i$, the net space charge density of the mobile carriers are induced by multiplication process, especially at both the junctions, and peak of electric fields are induced on both sides. The avalanche multiplication has been concentrated at both the junctions, thus the electric field in the n^- region decreases rapidly. As the peak in electric field is observed at the n^-/n^+ junction, the device goes to thermal breakdown mode or catastrophic failure of the device. As a consequence, the current-voltage characteristics from the avalanche injection exhibits a positive differential resistance for small currents and a negative differential resistance for higher currents. However, the role of dynamic avalanche of the carrier and their sustained injection on the redistribution of the electric field and net space charge density of mobile carriers have not been clearly understood [89, 90].

2.4.4 Bipolar Transistors ($n/p/n^-/n^+$)

In bipolar junction transistors (BJTs), high current injection mechanism occurs during transients at turn-on and turn-off when lateral flow of base current causes voltage drop across the base-emitter junction that leads to bipolar turn-on mechanism which is also known as *"base push-out effect"*. The occurrence of base push-out effect has been observed at high current densities which results in dramatic increase in carrier transit-time of the bipolar transistor. The negative differential resistance observed in bipolar structure due to transit-time effects have been studied extensively under steady-state condition by Kirk et al. and demonstrated many applications in the microwave devices [33, 91]. This effect occurs due to carrier density associated with electron current crosses through the depletion region of base-collector junction. Once the carrier density exceeds background carrier density of the depleted region, this region ceases to exist. However, there will be build-up of majority carriers from the base in the reverse biased base-collector depletion region. In this process, dipole is formed by

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positively and negatively ionized charge acceptors and donors is pushed towards the collector contact *(n^+ region)* and further replaced by positive ionized charge donors and negative electron charged accumulation layer, which is defined as base-push out effect. Moreover, the effective width of base region becomes equal to actual width of the base region and collector region, which substantially increases the transit time of the bipolar junction transistor [33, 91, 92]. Snapback mechanism has also been observed in absence of base drive of avalanche BJTs, in which high current injection from the base-emitter junction leads to re-distribution of the breakdown electric field across the depletion region of base-collector region [91, 93, 94].

2.5 Comparison of Studies under High Current Injection Conditions

Snapback in high voltage device structures has been primarily related to two basic mechanisms - the first has been explained through the base push-out/Kirk effect and second through dynamic avalanche processes. The first mechanism of base push-out effect, has also been used to explain snapback behavior in parasitic bipolar structures at the device level [33]. The second mechanism involves dynamic avalanche breakdown models that include a non-linear processes, which helps to explain the instability and avalanche to streamer transition resulting from the field-enhanced ionization of deep level centers [95, 96]. Moreover, the dynamic avalanche breakdown in silicon layered semiconductor and gas structures have been associated with different shapes of shock wave phenomena manifested as plane waves, concentric waves, finger shaped streamers, etc. [97, 98]. In all these semiconductor device structures, current injection from the base-emitter junction leads to re-distribution of the electric field profile across the depleted region of the collector junction [8, 22, 40], a phenomenon resembling the base push-out effect. So far these phenomena have not been collectively studied to understand the non-deterministic snapback behavior of high voltage device structures.

Table 2.4 shows the comparison between our study and observation by other authors for different layered structures under high current injection conditions. The analyses in the literature concerning an ultra-fast switching behavior of high voltage bipolar transistors in current mode secondary breakdown (CMSB) have been physically described by the shrinkage of depleted electric field at very high current densities [8, 33, 38, 99–101], as shown in Figure 2.4. However, the role of avalanche injection due to triggering of the ionization front across collector junction and base-transit time of mobile carriers has not been considered at high current densities [6, 46, 102]. Switching mechanism of reverse-biased

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Author	Work Done	Mechanisms				Comments
		Shockwave/Soliton		High Current Injection		
		Unipolar	Bipolar	p/n^-	n^-/n^+	
Vainshtein et.al. P.Rodin et.al. M. Domeij et.al. Deloach et.al.	Dynamic Avalanche	√	×	√	×	1. Generalized Concept of shock-wave without looking front profile. 2. Am-bipolar characteristics introduces a lot of interesting features is overlooked.
Kirk. et.al. Shrivastava et.al. K. Esmark et.al.	Bipolar Turn-on/ Kirk Effect	×	√	×	√	1.Essentially 1D phenomenon in steady state. 2.Multiple path of current injection overlooked. 3.Transient analysis of bipolar turn-on is missing. 4.Propagating ionization front is not modeled.
Our Studies	Coupled Bipolar Effect	√	√	√	√	1. Complete am-bipolar transient mechanism is described to understand the experimental work.

Table 2.4: Comparison between our study and other authors studies for different layered structures under high current injection conditions.

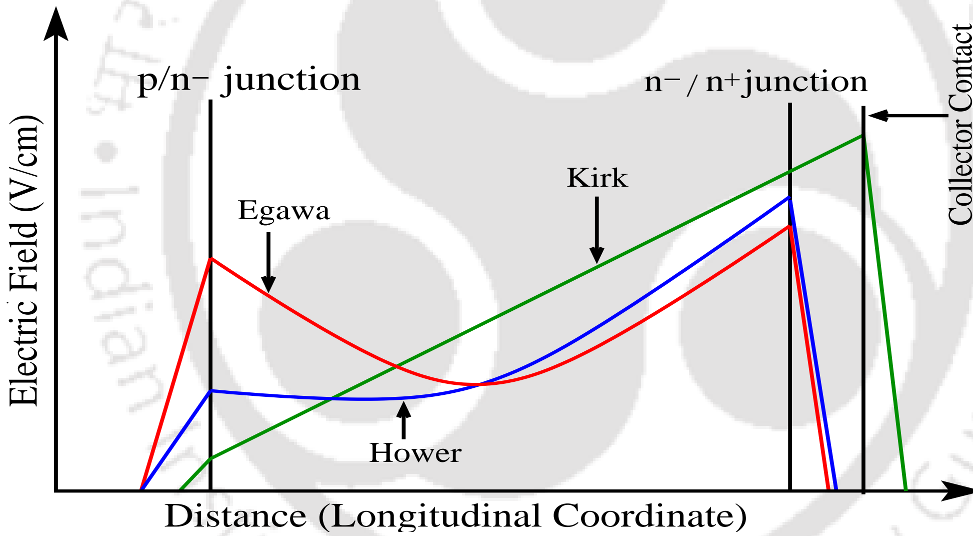

Figure 2.4: The schematic Distribution of electric field and related studies by different authors.

diodes has been described by Trapped Plasma Avalanche Triggered Transit (TRAPATT) mode of operation "*Shock wave*" like avalanche breakdown electric field traverses entire collector junction, which results in collapse of voltage across the reverse biased p/n junction and its dependence on displacement current has been discussed [22, 31, 44, 96]. However, the switching behavior of diodes due to ultra short time injection phenomenon across the contact has so far largely been overlooked and the impact of the boundary conditions on the moving charges have not been clearly addressed, leading to a hazy picture of how the electric field builds up across the contact [32, 39, 40]. Therefore, to the best of our knowledge, the analysis presented in this thesis work including internal dynamics and transient behavior of bipolar transistor having different configurations under different condition

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will be critical for reliability issues and modeling the high current phenomenon in high voltage device structures. Also, the role of base width, base-transit time, hole injection from the depletion region and its recombination physics has been discussed in this thesis work.

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3

Fast Ionization-front Induced Ultra-fast Anamolous Switching Mechanism in Bipolar Transistors Under Base-triggering Conditions

Contents

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Objective

Based on the analyses in the literature concerning an ultra-fast anomalous switching behavior of bipolar transistors under ordinary conditions have been physically described by the shrinkage of depleted avalanche breakdown electric field at very high current densities. However, the role of avalanche injection due to triggering of the ionization front across collector junction and base-transit time of mobile carriers has not been discussed in the detailed manner. Therefore, we establish novel physics based models to understand the anomalous switching behavior in bipolar structures at high current injection conditions. The role of voltage trigger pulse with variable rise time when applied to the base terminal is investigated to model the underlying physics of anomalous switching behavior. Experimental observations related to ultra fast anomalous switching mechanisms *i.e.*, either primary breakdown (PB) or current mode secondary breakdown (CMSB), for faster and slower base drives were presented respectively. Furthermore, we have captured the importance of dynamic avalanche model and reverse saturation current on the switching mechanism, under high speed base-trigger ramps for different avalanche BJTs from various manufacturers and different lots. We have also analyzed the mobile carrier distribution and formation of ionizing waves in the depletion region. The agreement between two dimensional $(2-D)$ TCAD device simulation results and the experimental observations discussed in this work shows validity of the proposed theory when the base width and mobile carrier recombination rate are used as parameters in the device simulation setup.

3.1 Motivation for Modeling Anomalous Switching Behavior in Bipolar Structures

This chapter focuses on understanding the anomalous switching behavior of bipolar transistor under base-triggering condition. The realization of ultra-fast switches under base-triggering conditions considering both practical and physical aspects are very interesting [66, 84, 103–105]. The avalanche bipolar transistor has been triggered through the base-drive voltage ramp, as shown in Figure 3.2. In this experiments, anomalous switching behavior has been observed in the avalanche bipolar transistor whose base-collector is reverse biased and variable voltage pulses with different rise times are applied across the base electrode [22, 24, 84]. Surprisingly, the switching transient of such avalanche bipolar transistors under base drive conditions has not yet been analyzed, even though these transistors where in use for last four decade. Moreover, the anomalous switching behavior of bipolar transistor under

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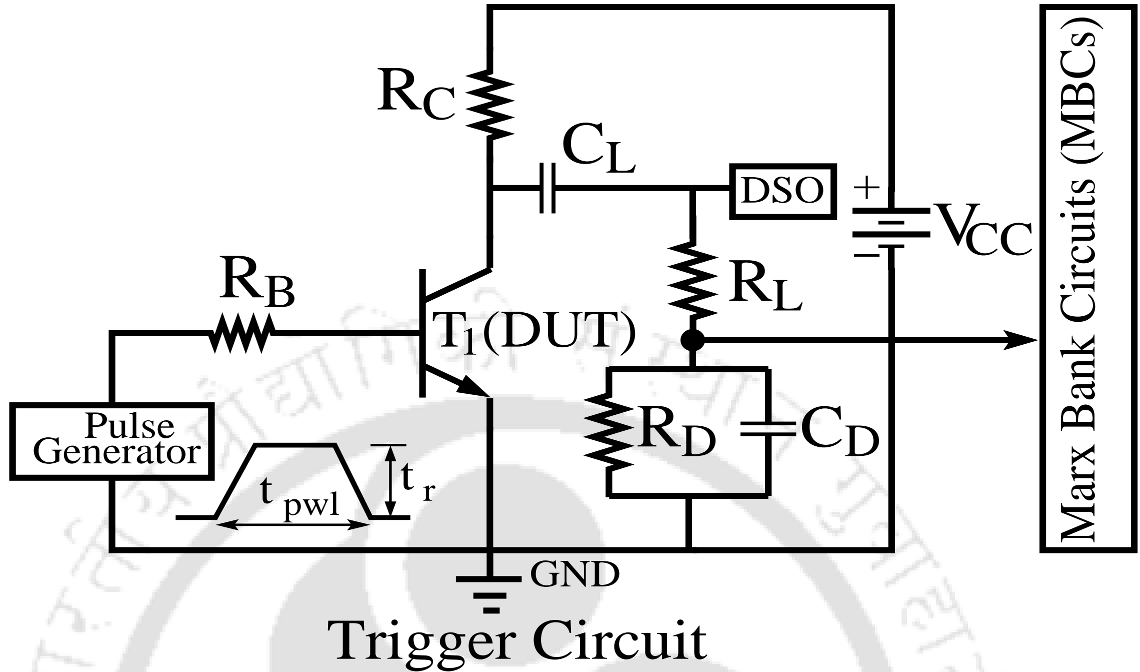

Figure 3.1: External circuit diagram of experimental setup comprising two stage circuits. First stage circuit has avalanche bipolar transistor which further triggers the remaining bipolar transistors of the MBCs.

ordinary condition remains unresolved in literature and the involved physical processes in device structure is quite complicated [106–109].

Therefore, the qualitative analyses and numerical simulation results presented in this chapter including internal dynamics and transient behavior of avalanche transistor under base-triggering condition will be critical for optimal design of ultra-fast switches and modeling the high current phenomenon in high voltage devices. In the experiments, we have applied variable ultra fast triggering voltage pulses across base terminal of the bipolar transistor. We have observed the anomalous behavior of the device at intermediate speeds of the voltage ramp and supply voltage. We have also analyzed the mobile carrier distribution and formation of ionizing waves in the depletion region. The role of base width, base-transit time and recombination physics in the base region has also been studied to model the anomalous switching behavior of the BJT.

3.2 Experimental and Simulation Set-up Details

3.2.1 Experimental set-up

The experimental setup of Marx bank circuits (MBCs) is shown in Figure 3.2, however complete transistorized MBCs can be seen in Ref. [30, 84] The pulses were applied across the base terminal of

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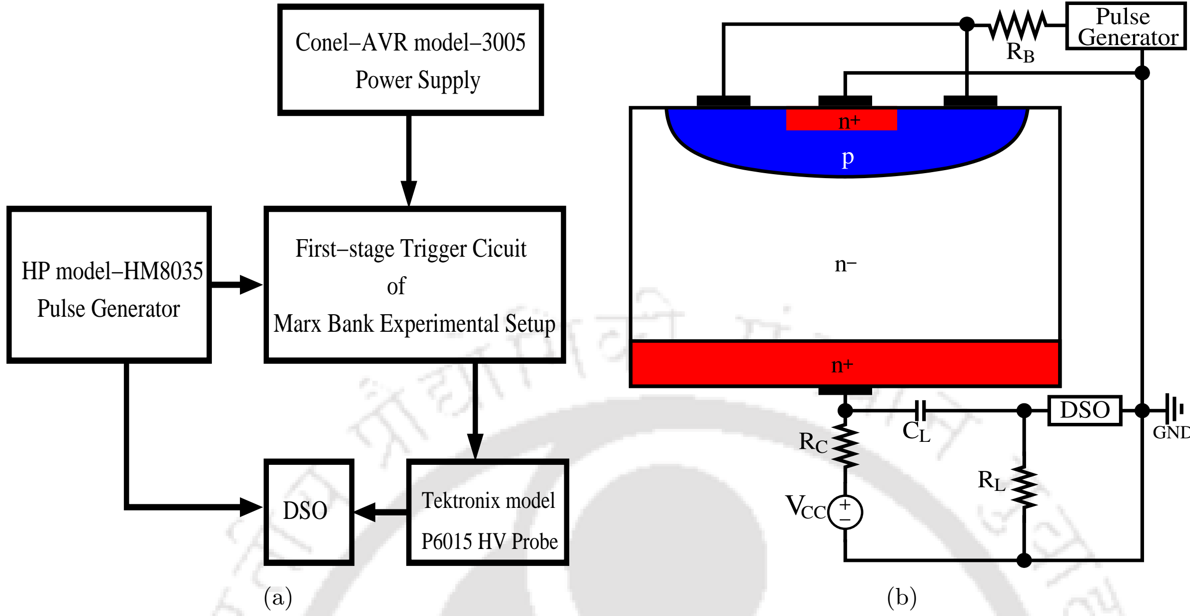

Figure 3.2: (a) Block diagram of the experimental systems and (b) external experimental setup of first stage Marx-bank circuit showing cross-section of silicon planar bulk $n/p/n^{-}/n^{+}$ bipolar transistor. Circuit element values are $R_B = 50\Omega$, $R_L = 1K\Omega$, $C_L = 10nF$, $R_C = 10K\Omega$ and BJT structure of $2N5551$ whose base-collector junction reverse biased was used for device simulation purpose. The doping of bipolar structure are $N_d = 10^{19}cm^{-3}$, $N_a = 10^{17}cm^{-3}$, $N_{d^-} = 1 \times 10^{15}cm^{-3}$ and $N_{d^+} = 10^{19}cm^{-3}$.

commercial bipolar junction transistor as suggested in Ref. [66, 84]. The experiments were repeated with $n/p/n$ transistors ($2N5551$ and $2N2221$) having different switching frequency (f_T) from various manufacturers and different lots. The devices were clamped to different supply voltage of $120V$ to $250V$, and voltage pulses of $2V$ in the range of nanosecond (ns) to microsecond (μs) were applied across the base terminal whose base-collector junction is reverse biased. A controlled power supply *(Conel-AVR model-3005)* was used for DC biasing. The MBC circuit was triggered with variable base voltage ramp using a pulse generator *(HP model-HM8035)* capable of producing 0 to $+5V$ rectangular pulses of variable rise time ranging from ns to $100ns$ typically at $20Hz - 2KHz$ repetition rate. The voltage transient waveform was measured across a load resistance, $R_L = 10K\Omega$ using digital storage oscilloscope having a bandwidth of $8GHz$ *(Keysight Infiniium S-Series model-DSOS804A)*, equipped with a high voltage probe *(Tektronix model-P6015)* having bandwidth of $75MHz$ and nominal attenuation factor of 1000.

3.2.2 TCAD Device Simulation set-up under Dynamic Avalanche Conditions

Detailed information related to the device structure and the associated external experimental circuit setup is required for a proper comparison between measured experimental and TCAD device

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simulation results. We chose Fairchild's high voltage NPN silicon BJT ($2N5551$) and ($2N2221$) device structures. The cross-section of the planar device structure as shown in Figure 3.2 was used for numerical device simulation. Device structure was optimized to match $BV_{CBO} = 180V$ & $BV_{CEO} = 160V$ and a cut-off frequency (f_T) $= 100MHz$ for $2N5551$ and $BV_{CBO} = 80V$ & $BV_{CEO} = 60V$ and cut-off frequency (f_T) $= 250MHz$ for $2N2221$ of the experimental device under test for simulation purpose. The epi-region doping of 1×10^{15} and 3×10^{15} were considered for $2N5551$ and $2N2221$ respectively. We have performed transient isothermal mixed-mode numerical device simulation (circuit being same as experimental setup) to characterize voltage-time characteristics under high current avalanche injection conditions through commercially available Sentaurus TCAD device simulator. We used drift-diffusion transport and high electric field models such as electric field dependent mobility, Auger recombination, Shockley-Read-Hall (SRH) recombination, band-gap narrowing and Selberherr impact ionization models. All of these physical models were calibrated with the experiments [71].

3.2.3 Calibration of device structure from measurements and calculations

Device structure was built to match $BV_{CBO} = 180V$, $BV_{CEO} = 160V$, $f_T = 100MHz$ and maximum current is $0.6A$ of the experimental device under test, and also assumed that the n-epitaxial layer was fully depleted under breakdown conditions. For the simulation purpose, we have considered depletion width of $W_{dep} = 8 \times 10^{-4}cm$, and total area ($A$) $= 1.5 \times 10^{-6}cm^2$. We have calculated current density of $J = 4 \times 10^5 A/cm^2$, breakdown electric field (E_{br}) and base width (W_B) calculation by following data-sheet of $2N5551$.

- Given $BV_{CBO} = 180V$ and $W_{dep} = 8\mu m$.

$$E_{br} = \frac{BV_{CBO}}{W_{dep}} = \frac{180V}{8\mu m} = 2.25 \times 10^5 V/cm. \tag{3.1}$$

- Given $f_T = 100MHz = \frac{1}{2\pi\tau_B}$, where τ_B is base-transit time.

$$\tau_B = \frac{1}{2\pi f_T} = \frac{1}{2\pi.100 \times 10^6} \approx 1.6 \times 10^{-9} sec \tag{3.2}$$

$$W_B^2 = \tau_B \times 2D_n = \tau_B \times 2 \times \frac{KT}{q}\mu_n = 1.6 \times 10^{-9} \times 2 \times 0.0259 \times 700 \approx 5.4 \times 10^{-8} cm^2$$

$$W_B \approx 2.3\mu m \tag{3.3}$$

Moreover, the depletion region doping concentration (N_d) calculation from C-V Measurement through B1500A Semiconductor Device Analyzer.

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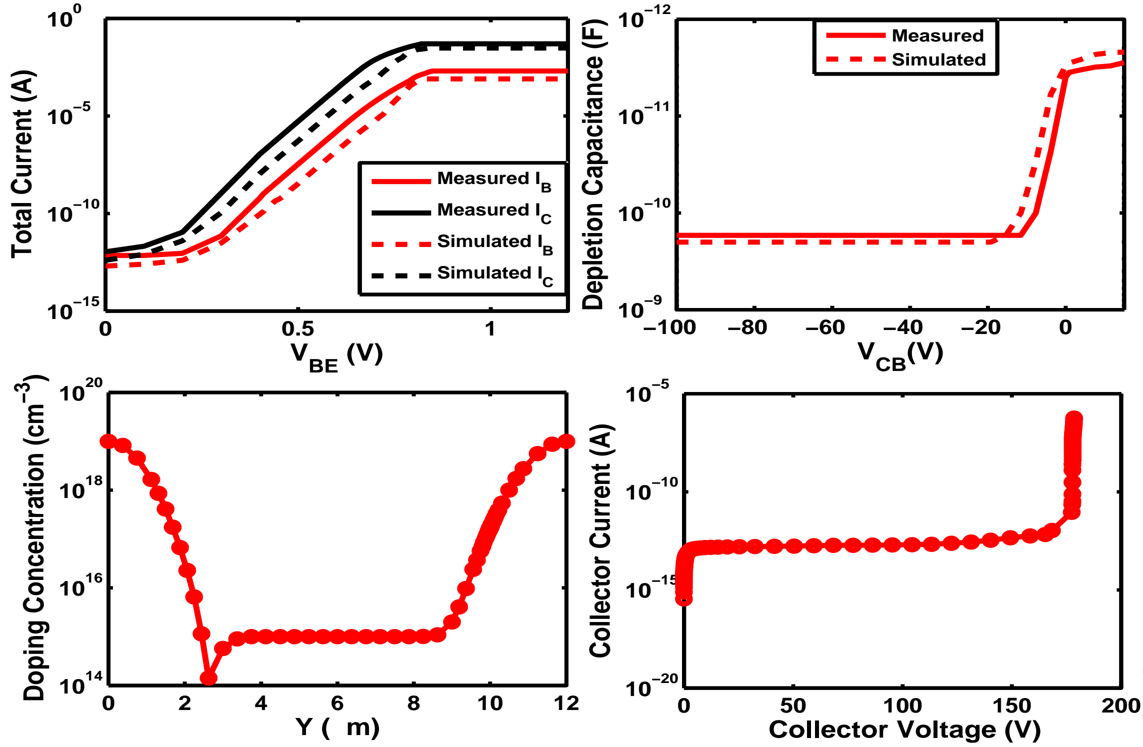

Figure 3.3: A very good agreement is observed between measured and simulated Gummel and C-V plot which has been carried through B1500A Semiconductor Device Analyzer and TCAD device simulator respectively. Profile of doping concentration of the calibrated bipolar junction transistor after calculating all the values of device parameter and quasi-stationary current-voltage characteristics shows approximately $V_{CBO} = 180V$.

- Given $C_{dep} = 1.68 \times 10^{-12}F$ at $V_{CBO} = 180V$ through C-V Measurement and $Area = 25 \times 10^{-4}cm^2$ provided by BEL, India.

$$C_{dep} = \frac{Area}{2}\left[\frac{2q\epsilon}{V_{CBO}}N_d\right]^{\frac{1}{2}}$$

$$N_d = \frac{2V_{CBO}}{q.\epsilon}\left(\frac{C_{dep}}{Area}\right)^2 \tag{3.4}$$

$$N_d = \frac{2 \times 180V}{1.6 \times 10^{-19}C \times 11.8 \times 8.85 \times 10^{-14}F/cm}\left(\frac{1.68 \times 10^{-12}F}{25 \times 10^{-4}cm^2}\right)^2$$

$$N_d \approx 1 \times 10^{15}cm^{-3} \tag{3.5}$$

Finally, we have calculated base region doping concentration (N_B) calculation from Gummel-plot measurement through B1500A Semiconductor Device Analyzer.

- Given $I_{sat} \approx 1 \times 10^{-13}A$ from Gummel-plot Measurement and $Area = 25 \times 10^{-4}cm^2$ provided by BEL, India.

$$I_{sat} = \frac{qAn_i^2}{Gummel\ \ Number} = \frac{qAn_i^2}{G_B} \tag{3.6}$$

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$$G_B = \frac{qAn_i^2}{I_{sat}} = \frac{1.6 \times 10^{-19}C \times 25 \times 10^{-4}cm^2 \times 2.25 \times 10^{20}cm^{-6}}{1 \times 10^{-13}}$$

$$G_B \approx 9 \times 10^{11}cm^{-4} - s \tag{3.7}$$

$$G_B = \frac{N_B}{D_n} \times W_B \tag{3.8}$$

$$N_B = \frac{G_B \times D_n}{W_B} = \frac{9 \times 10^{11} \times 0.026 \times 700}{2.3 \times 10^{-4}} = 0.8 \times 10^{16}cm^{-3}$$

$$N_B \approx 1 \times 10^{17}cm^{-3} \tag{3.9}$$

After all the calculations and measurements, we have calibrated the device structure through the TCAD device simulation. A very good agreement is observed between simulation and measurement results, as shown in Figure 3.3.

3.3 Comparison of the Experimental and TCAD Device Simulation Results

A comparison between the experimental observations and TCAD simulation results of voltage-time characteristics across the resistive load is shown in Figure 3.4. In order to understand the mechanisms responsible for the anomalous switching mechanism of the avalanche bipolar transistors under high current conditions, a large number of experiments were performed with different $n/p/n$ devices ($2N5551$ and $2N2221$) from a random lot. The bias voltage is first set at $V_{CC} = 120V$ as indicated in Figure 3.2 and results are shown in Figure 3.4. The bipolar structure is subjected to variable voltage pulse with different rise time from $5ns$ to $50ns$ across the base electrode. Furthermore, the supply voltage was varied from *120V to 250V*, but rise time of base triggering voltage pulse was kept constant at $5ns$.

Initially, when we applied voltage ramp of $2V$ with rise times of $5ns$ and $10ns$, the device demonstrated avalanche mode *(i.e., PB or slow switching, where the device exhibits no collapse in voltage)*. This experimental observation was also verified using numerical simulation in Sentaurus, however a difference of $10V$ in amplitude of collapsing load voltage is observed between simulation and practical results (shown in Figure 3.4 (a)). When the rise time of ramp speed is increased to $50ns$, device goes into CMSB mode *(i.e., device exhibits fast collapse in voltage)*, as shown in Figure 3.4 (a). Thus, the bipolar structure exhibits two completely different modes for variable base-drive voltage ramp speed ("*avalanche mode*" or "*CMSB mode*"), at constant value of supply voltage, which can be seen in the

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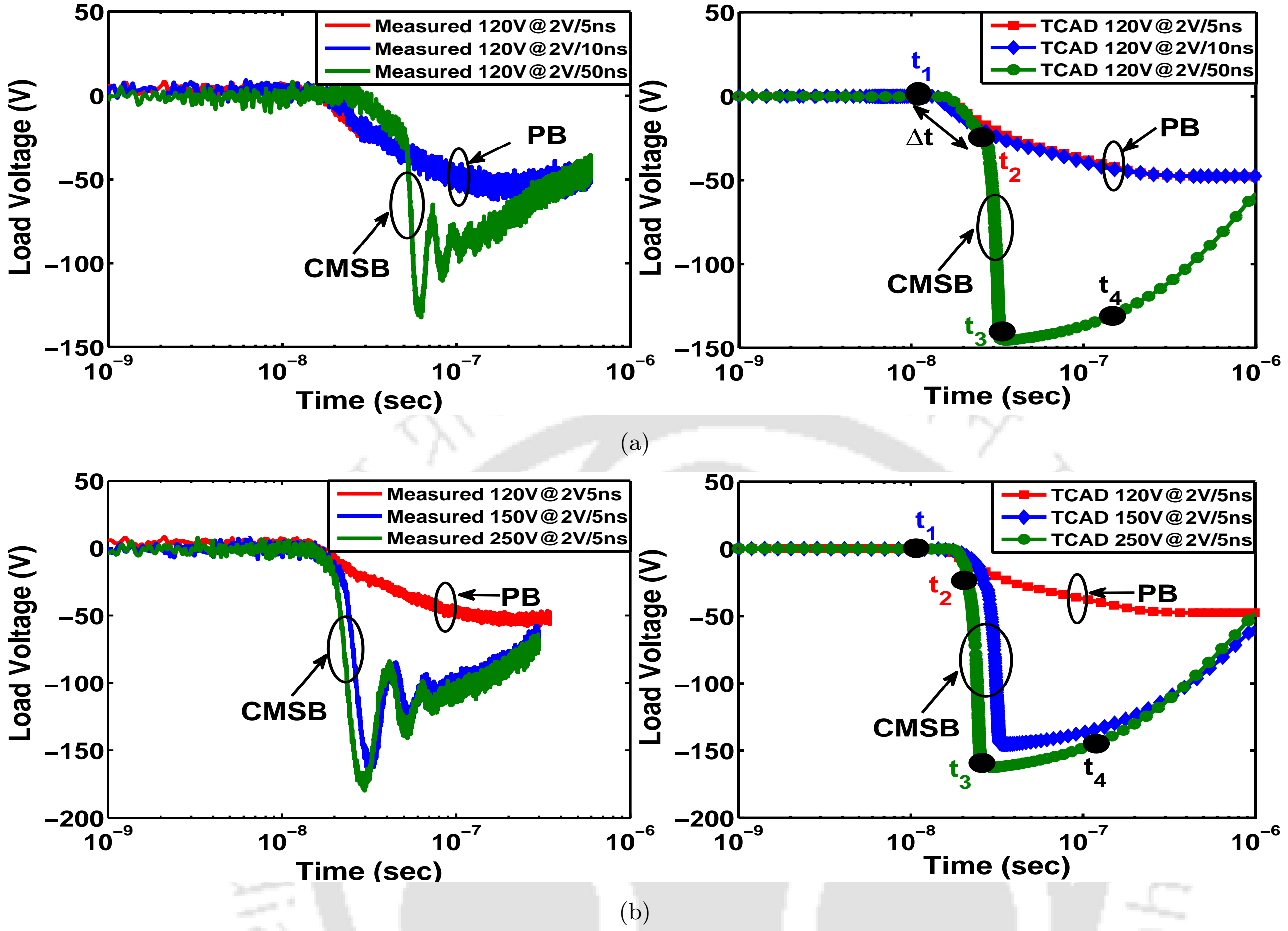

Figure 3.4: Measured output anomalous voltage-time characteristics of the device under test ($2N5551$, BJT under ordinary conditions). (a) Variable rise times of base-triggering voltage pulses at fixed supply voltage of $120V$ were applied. (b) Different value of supply voltages with fixed base-triggering voltage ramp of $2V/5ns$ were applied. Δt represents avalanche build-up time which changes with bias voltage and applied base-triggering voltage pulse.

load voltage-time characteristics of the external circuit. Hence, the junction exhibits indeterminacy in choosing either of the possible breakdown states, which results in jittery behavior for different base rise times of voltage pulse. It is noteworthy that as the rise time of base-triggering voltage pulse is increased from $10ns$ to $50ns$, devices show avalanche build-up time ($i.e.$, $\Delta t \approx (t_2 - t_1)$), then it switches to secondary breakdown mode which results in fast collapse of load voltage. However, an application of faster rise time of base triggering pulse across the device do not exhibit avalanche build-up time and fast collapse of voltage is not observed, as shown in Figure 3.4 (a). Moreover, it was observed that the devices did not exhibit the overvolting phenomenon in all the above cases as they remained clamped to a fixed bias voltage.

The same pulsing configurations of the bipolar structure is operated at different value of supply

voltages ranging from *120V to 250V* with fixed triggering voltage pulse of $2V/5ns$ applied across the base electrode. When the MBCs were subjected to a supply voltage of $120V$ in the experimental circuit, the device exhibited slow switching in the load voltage *(i.e., avalanche mode)* however, for supply voltage of either $150V$ or $250V$ with same base triggering voltage ramp (*i.e.*, $2V/5ns$), the device progressed into CMSB mode and bipolar structure exhibited fast collapse in load voltage even when Δt was very small, as shown in Figure 3.4 (b).

The dependence of device behavior on the voltage ramp speed is similar to the displacement current in bipolar transistors with the base-emitter externally shorted. In these devices, the large displacement current density causes propagation of a wave-front like pattern in the depleted base-collector junction [24, 31]. We also observed this in our experimental and simulation results, where the increase in rise time of the base-triggering voltage pulse from *5ns to 50ns* resulted in anomalous switching behavior. This shows that the phenomenon may not be explained purely by the rise time of the triggering voltage ramp across the base terminal. In order to understand the anomalous behavior of the switching mechanism of avalanche bipolar transistor under base triggering conditions, we need to model the internal dynamics of the device. The load voltage at different times is discussed in the next section to analyze the physical processes and validate the numerical simulation results with experimental observations.

3.4 Modeling Transient Behavior of Switching Mechanism Under Base-triggering Conditions

3.4.1 Results and Discussion

The load-voltage transient and its corresponding mobile carrier density and electric field distributions for different base triggering voltage ramps at a supply voltage of $120V$ is shown in Figure 3.5. As the supply voltage increases, the device is clamped to a fixed voltage and the base-collector depletion region reaches the breakdown electric field at t_1. The slope of the breakdown electric field in the depletion region is determined from (i.e., $dE/dy = qN_d/\epsilon_{si}$), where E represents electric field, N_d is background doping concentration in the depletion region and ϵ_{si} is the permittivity of silicon.

The initial build-up of the electric field triggers impact ionization process at the p/n^- junction. These avalanche-generated holes move towards the p/n^- junction, but the avalanche-generated electrons move towards the n^-/n^+ junction [40]. The generated electrons and holes increase and then separate, modulating the electric field in the depletion region, as shown in Figure 3.5. The electric

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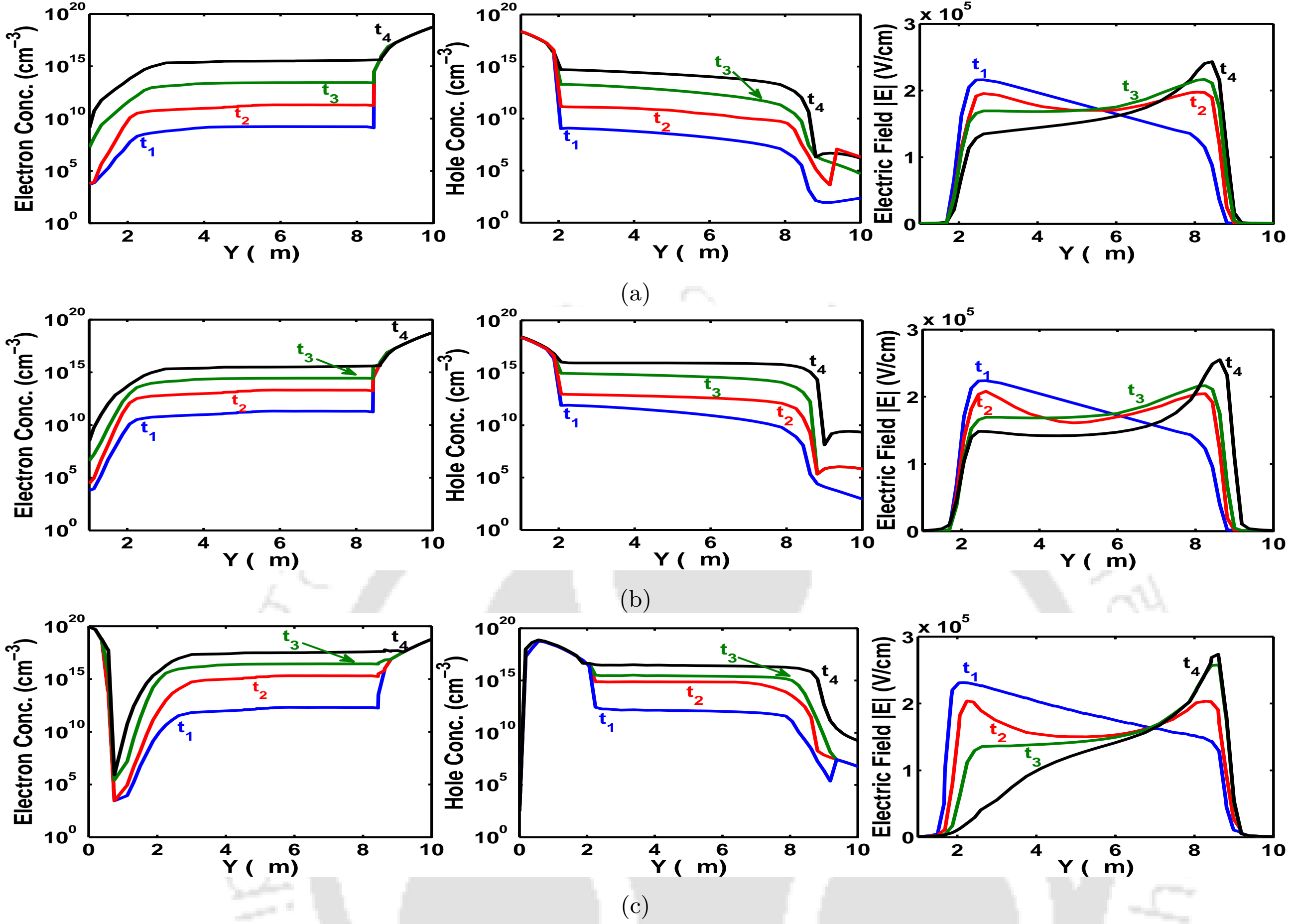

(a)

(b)

(c)

Figure 3.5: The spatial distributions of electron concentration $n(y,t)$, hole concentration $p(y,t)$ and absolute electric field $|E(y,t)|$ within the depleted base-collector junction, obtained by performing longitudinal cut-line at $x = 15.5\mu m$ and plotted at different time instances such as; (1) $t_1 = 10.262ns$, (2) $t_2 = 28.276ns$, (3) $t_3 = 31.290ns$ and (4) $t_4 = 190.304ns$. (a) When faster base-triggering voltage ramp speed of *2V with rise time of 5ns* is applied, (b) When intermediate base-triggering voltage ramp speed of *2V with rise time of 10ns* is applied, (c) when an slower voltage ramp of *2V with rise time of 50ns* is applied across the base.

field decreases within the depletion region in each of the cases at t_2, but the shape of the electric field profile depends on the amount of avalanche-generated mobile carriers and the avalanche build-up time (*i.e.*, Δt). For base-triggering voltage pulses with rise times of *5ns or 10ns*, the electric field decreases slightly in the depletion region and rises slowly at the n^-/n^+ junction, as shown in Figure 3.5 (a) and (b). Due to injection of electrons from the base-emitter junction, the time available for avalanching to build-up is relatively small, so a sufficient density of mobile carriers is not generated. When the bipolar ramp speed is slower, however, with rise time of $50ns$ the electric field in the depletion region decreases but there is a sharp increase in electric field compared to the earlier cases. This results in triggering a moving ionization front towards the n^-/n^+ junction at times t_3 & t_4, as shown in Figure 3.5 (c). In this case, a sufficient number of mobile carriers is generated in the depletion region

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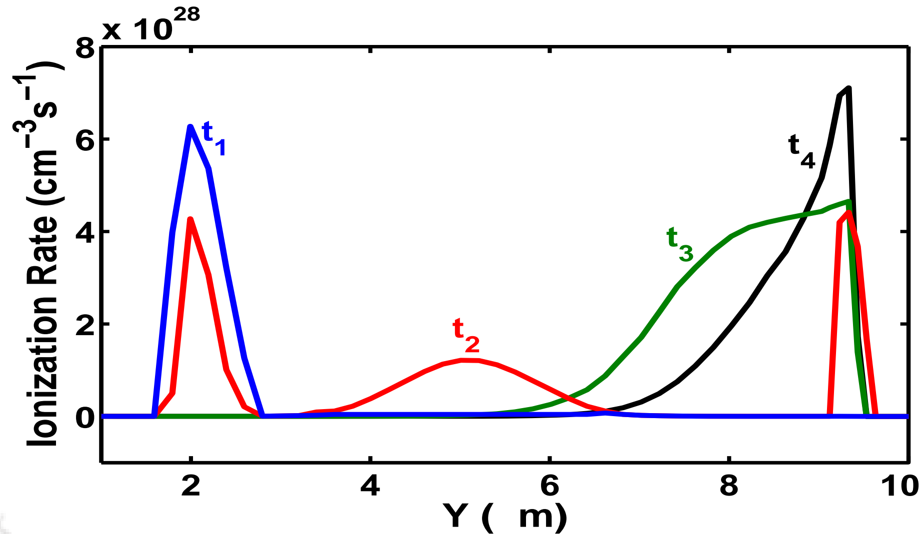

Figure 3.6: The distribution of self-reinforced moving ionization front at different time instances, it is triggered at time (t_2) within the base-collector depletion region due to separation of electron and hole concentrations. The moving ionization front also sharpens as it progresses towards the n^-/n^+ junction and front movement is restricted at time t_4.

due to the delay in injection of electrons from the base-emitter junction. The physics of triggering of the self-reinforced moving ionization front can be understood by looking at the electron and hole concentrations during the impact ionization process. It is noted in numerical simulations that, when a faster triggering voltage ramp is applied to the base terminal, the mobile carriers are more evenly distributed in comparison to slower voltage ramps. During the separation of electrons and holes, the concentrations in the depletion region are approximately equal to the background donor doping concentration ($i.e., n - p \approx N_d$). The resulting shock wave and self-reinforced moving ionization front are observed for faster and slower base-triggering voltage ramp speeds respectively at t_2, which moves towards the n^-/n^+ junction [24]. The wave-front (shown in Figure 3.6) results in accumulation of electrons which increases the electric field at the n^-/n^+ junction for slower base-triggering voltage ramp. The ionization front sharpens and electric field also increases rapidly as the front travels towards the n^-/n^+ junction at different time instances t_3 and t_4.

When the ionization front reaches the n^-/n^+ junction at t_4 and at the same instance if the front movement is restricted across the base-collector junction, then it results in regenerative process. Also, double injection of the mobile carriers are observed, which depends on the base width (W_B) and reverse saturation current I_{sat}. This determines the anomalous switching behavior *(i.e., PB or CMSB)* of the bipolar structure under base-triggering conditions. Therefore, the roles of base width and recombination of injected electrons in the base region are important. However, when faster base

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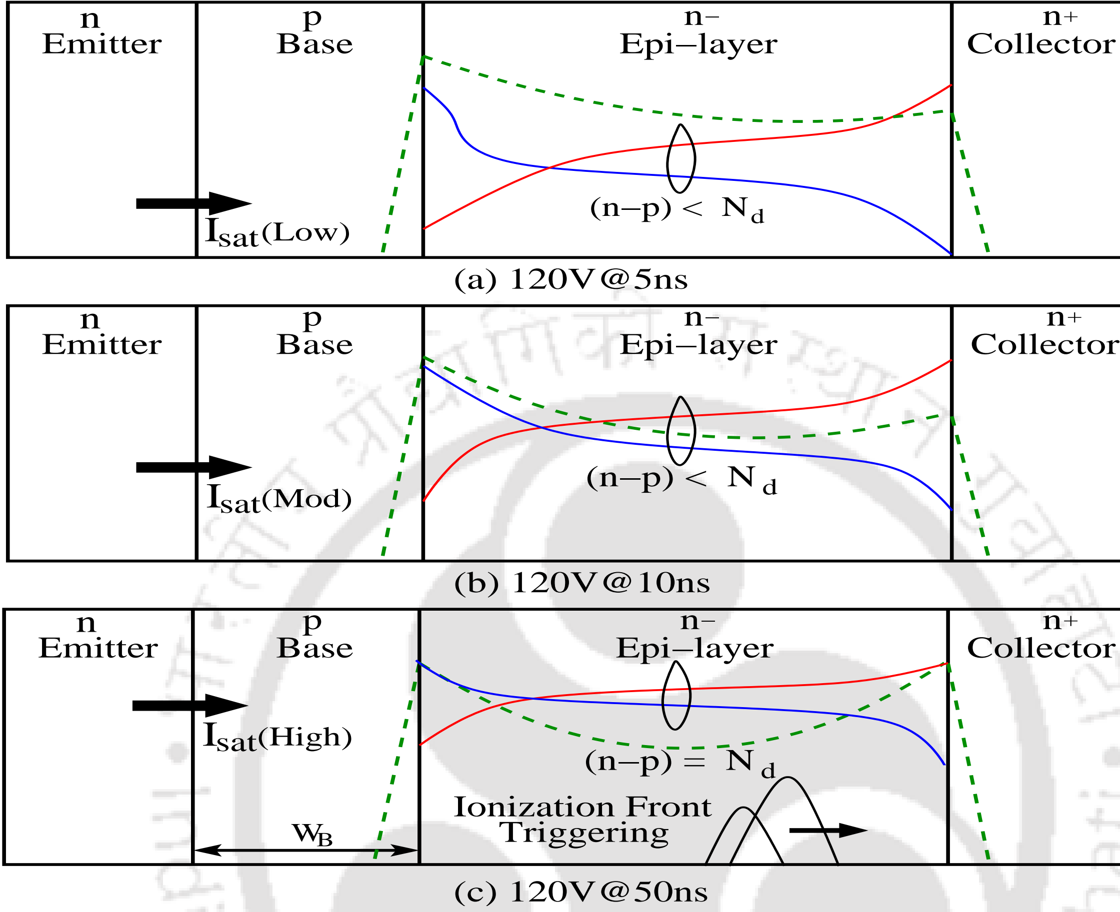

Figure 3.7: Schematic representation of the mobile carriers and electric field distributions at different base-triggering voltage ramp. The triggering of the self-reinforced ionization front in the case of slower rise time, that traverses towards the depleted base-collector junction and also sharpens as it progresses towards the n^-/n^+ junction. As the injection of electron is delayed due to slower rise time from the base-emitter junction, stronger reverse saturation current and increase in plasma of mobile carriers is observed.

drive signals are applied, the condition for triggering the moving ionization front does not occur because the mobile carriers are more evenly distributed at the same supply voltage. Therefore, in order to understand the anomalous switching behavior, we need to have appropriate boundary conditions at both junctions *(i.e., p/n^- and n^-/n^+ junctions)* [40].

Moreover, it has been observed that the delay in injection of electrons from the base-emitter junction causes a sufficient amount of generation of mobile carriers in the depletion region, which triggers the moving ionization front. Injection of electrons is related to barrier lowering of the base-emitter junction, which is related to the reverse saturation current (I_{sat}). Some of the injected electrons recombine and the remaining electrons are swept across the reverse bias of the base-collector depletion region. Therefore, in order to obtain ultra-fast switching or CMSB mode, sufficient avalanche build-up time is required. Figure 3.7 shows the schematic distribution of the electron and hole concentration

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and electric field profile at different base triggering conditions. As the rise time of the base-triggering voltage pulse increases at fixed bias voltage of $120V$, it shows delay in electron injection from the emitter, which results in stronger I_{sat} and an increase in the plasma of mobile carriers in the depletion region. When the slower base voltage ramp is applied, the condition for moving ionization front is obtained and the device show CMSB mode. However in the case of faster base triggering voltage ramp, moving ionization front is not triggered thus it shows PB mode. It is seen that there are two independent processes (i) recombination of injected electrons with holes in the base region and (ii) condition for the triggering of ionization front. The coupling of above two independent processes determines anomalous switching mechanism.

3.5 Role of Base Width and Recombination rate on Switching Mechanism under High Current Conditions

The triggering of the moving ionization front depends on the mobile carrier distributions, however injection of electrons from the base-emitter junction (dictated by reverse saturation current (I_{sat})) affects the profiles of mobile carrier, as discussed in last section. A few injected electrons recombine with holes in the base region but majority of electrons passes through the base region to base-collector depletion region and these collected electrons are a function of base width and recombination rate of mobile carriers. Therefore, the role of base width (W_B) and recombination of injected electrons from emitter with holes in the base region are described in this section. In order to verify our results, similar experiments were performed with different $n/p/n$ devices from different lots and different manufacturers with switching frequency (f_T) of $250MHz$ and $100MHz$ respectively, but other than value of the base-collector breakdown voltage (V_{CBO}), the anomalous switching behavior of the breakdown mode was observed to be generic in all the device structures. Table-3.1 summarizes behavior of these devices with different rise times of base-triggering voltage ramp at different bias voltages i.e., $V_{CC} = 120V$ or $V_{CC} = 150V$, such that a breakdown current flows across the reverse biased base-collector junction of the transistor for a considerable time. It shows anomalous switching behavior of the base-triggering pulsing configuration of both the bipolar transistors such as: $2N2221$ and $2N5551$. These low breakdown-voltage devices like $2N2221$, though exhibiting this erratic switching behavior, have a much sharper transition region. The transition between the two modes of breakdown in these devices caused by change in the ramp speed is very abrupt as compared to $2N5551$. Since f_T of different transistors are taken from their respective data-sheet, thus the width of DUT can be calculated

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DUT	Parameter	Supply Voltages (V_{CC})					
		120V			150V		
		$2V/5ns$	$2V/10ns$	$2V/50ns$	$2V/5ns$	$2V/10ns$	$2V/50ns$
2N2221	$f_T = 250MHz$, $W_B = 1.6\mu m$	×	√	√	√	√	√
2N5551	$f_T = 100MHz$, $W_B = 2.3\mu m$	×	×	√	√	√	√

Table 3.1: Experimental observations related to anomalous switching behavior of the base-triggering pulsing configuration of $n/p/n$ bipolar transistors of different switching frequency (f_T) at two different supply voltages with variable rise times. Where √ represents triggering of secondary breakdown mode and × shows primary breakdown mode.

Device Width (W_B)	Recombination Rate (sec)	Supply Voltages (V_{CC})					
		120V			150V		
		$2V/5ns$	$2V/10ns$	$2V/50ns$	$2V/5ns$	$2V/10ns$	$2V/50ns$
$W_B = 1.6\mu m$	3×10^{-4}	×	×	√	×	×	√
	3×10^{-6}	×	√	√	√	√	√
	3×10^{-8}	√	√	√	√	√	√
$W_B = 2.3\mu m$	3×10^{-4}	×	×	×	×	×	√
	3×10^{-6}	×	×	√	√	√	√
	3×10^{-8}	×	×	√	√	√	√

Table 3.2: TCAD device simulation observations related to anomalous switching behavior (√ represents triggering of secondary breakdown mode and × dictates primary breakdown mode) of bipolar structures when we parametrize base width and recombination of mobile carrier at different base-triggering rise times and supply voltages.

using formula $f_T = \frac{W_B^2}{2D_n}$, where D_n represents electron diffusion coefficient. Now, $2-D$ TCAD device simulation were performed to understand the physical insight behavior of the device structure, when the base-width and recombination rate are parametrized in the simulation setup.

In the numerical simulation and experimental observations, it is seen that devices with base width of either $1.6\mu m$ or $2.3\mu m$ shows erratic switching behavior in the voltage-time characteristics, when the rise time of base triggering pulse is varied from $5ns$ to $50ns$ at different bias voltages, as summarized in Table 3.1 and 3.2. The reasonable agreement between the measured and simulated behavior was achieved. In the process, it is observed that deterministic front triggering and the recombination of injected electron with holes in the base region shows an chaotic behavior of different device structures. Figure 3.7 shows the complete schematic representation of switching mechanism of bipolar transistor, where deterministic front triggering is obtained at particular condition. The condition for the triggering of self-reinforced moving ionization front is observed when the separation of mobile carrier is equal to background doping concentration ($i.e.$, $(n-p) \approx N_D$, as discussed in the last section). The

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coupling of electron injection from forward biased base-emitter junction and the moving ionization front triggering condition are determined by the recombination rate of mobile carriers, as summarized in Table 3.2. Initially the device width is kept constant at $1.6\mu m$ and base triggering voltage ramp of $2V/10ns$ is applied at $V_{CC} = 120V$, lesser recombination of holes with strong injection of electrons from emitter. In this case, most of the electron crosses the base region without recombination and thus CMSB mode is observed, whereas devices having width of $2.3\mu m$ shows complete recombination of holes with electrons in the base region, thus very less electron is collected by the collector contact which results in PB mode. In order to understand the role of recombination physics in the base region, we have varied recombination rate of mobile carrier from 3×10^{-4} to 3×10^{-8} with fixed supply voltage of either $120V$ and $150V$ at different rise time of base-triggering voltage pulse. The bipolar transistors having higher base width of $2.3\mu m$ shows PB mode for higher recombination rate of 3×10^{-4}, but CMSB mode is observed in the bipolar structure which has lower device width of $1.8\mu m$. Therefore, as the recombination rate of mobile carrier is decreased from 3×10^{-4} to 3×10^{-8} CMSB mode is seen in both the bipolar transistors however lesser recombination of mobile carriers are required in the base region, thus stronger I_{sat} is observed. The complete understanding of ultra-fast switching mechanism of avalanche bipolar transistor and the optimal design of switching transistor for UWB application requires deep insight towards the role of recombination physics and base width of the device as discussed in this section.

3.6 Conclusion

In this chapter, we have modeled the anomalous switching behavior of first stage trigger avalanche bipolar transistors of MBCs under base-triggering conditions. We have performed fast-switching experiments on various avalanche BJTs under the same conditions and also verified our results through numerical simulations. A very good agreement has been observed between measurement and $2-D$ TCAD device simulation results. The nonlinear phenomena involving propagation of self-reinforced impact ionization wave front caused by accumulation of avalanche-generated mobile carriers has been analyzed through numerical simulation. The triggering of the moving ionization front phenomenon leads to CMSB mode, which results from the regenerative process, as it travels towards the n^-/n^+ junction. Thus, the anomalous switching behavior of the bipolar structure can be summarized through the following observations;

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- The faster base-triggering voltage ramp with rise time of either $5ns$ or $10ns$ results in early injection of electrons from emitter or lower I_{sat} which affects avalanche process in the depletion region thus it is not able to trigger moving ionization front, hence primary breakdown has been observed.

- The slower ramp speed of $2V/50ns$ triggers deterministic moving ionization front which results from plasma of generated mobile carriers in depletion region due to sufficient avalanche build-up time and stronger I_{sat}, hence CMSB mode has been seen.

- It has been observed that the triggering delay of MBCs depends upon the switching behavior of first stage trigger transistor.

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4

Erratic Switching Mechanism due to High Current Filamentation in Bipolar Structures whose Base-emitter Externally Shorted under Dynamic Avalanche Conditions

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Objective

In this chapter, we model the indeterminacy that occurs during formation of breakdown current channels in a bipolar structure whose base-emitter is externally shorted, when subjected to an ultra-fast high voltage pulse. The experimental results pertaining to different regimes of the voltage ramp speed, applied across the bipolar structure are modeled. The avalanche injection mechanisms under variable high speed ramps are studied through formation and propagation of ionizing waves, which lead to either weak or strong injection of mobile carriers, as the high current injection paths get coupled. Furthermore, the role of emitter injection is related to the indeterminacy associated with the snapback phenomenon and systematically related to the experimental observations. we explore the indeterminacy during bipolar turn-on and model the high current injection phenomenon.

4.1 Motivation for Modeling Non-deterministic Switching Behavior in Bipolar Structures

High current avalanche injection behavior is well established phenomenon in a BJT (Bipolar Junction Transistor) [8]. However, its impact on the first snapback is somewhat less understood [6]. It has been experimentally observed that, when an ultra-fast pulse is applied across the BJT with base-emitter shorted, one of the two breakdown mode (i.e avalanche breakdown or second breakdown) is observed [8], [22]. During the dynamic avalanche breakdown, build-up of electric field at the ohmic contact is associated with high current injection mechanisms [22], [66]. The microscopic understanding of transient behind the breakdown phenomenon, under high current injection in semiconductor devices has so far not been clearly understood [67]. However, the reliability physics of high current phenomenon in commercially critical and emerging power devices integrated into state of art VLSI devices is intricately related to transient mechanisms of high current pulses across a parasitic $n/p/n^-/n^+$ structures [22], [55]. The analysis presented in this work will be critical for modeling the high current phenomenon in state of art high voltage as well as low voltage devices [67], [110].

In the course of this chapter, we explore the indeterminacy during bipolar turn-on and model the high current injection phenomenon. In this experiments, we apply variable ultra fast voltage pulses across a bipolar structure in several configurations and observe erratic (indeterminate) behavior of the device at intermediate speeds of the voltage ramp. Moreover, different experimental observations are confirmed using 2D TCAD device simulations, as we explain the generic behavior of filaments

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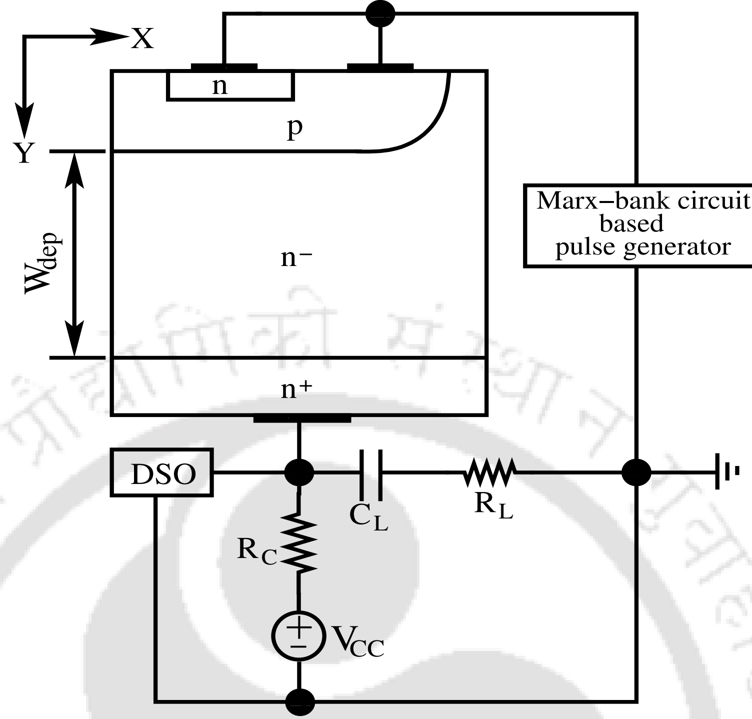

Figure 4.1: The experimental external circuit setup and cross section of an $n/p/n^-/n^+$ transistor, where W_{dep} is the depletion region width. Circuit elements are $R_L = 1M\Omega$, $C_L = 2nF$, $R_C = 5.6M\Omega$, and supply voltage (V_{CC}) = $300V$ or $400V$. In the experiments, BJT structure is used with different configurations for simulation purpose. The doping in different regions of bipolar structure are $N_E = 10^{19}cm^{-3}$, $N_B = 10^{17}cm^{-3}$, $N_{Epi} = 10^{15}cm^{-3}$ and $N_C = 10^{19}cm^{-3}$.

in different regimes of the ramp speed. We next revisit and analyze mobile carrier distribution and formation of ionizing waves in the depletion region and study voltage collapse due to avalanche injection and subsequently model bipolar coupling. Two basic processes leading to the bipolar coupling mechanism are identified as the bipolar structure turns on.

4.2 Summary of Experimental Study and Observations

A commercial 2N5551 (Fairchild), an NPN bipolar junction transistor was considered for the experimental study and observation. We have analyzed different configurations of the BJT, such as: (i) base-emitter shorted, (ii) base open and (iii) emitter open, where a variable ultra-fast voltage ramp of *250V to 400V* with different rise times of nanosecond (ns) to microsecond (μs) was applied to the devices by maintaining pulse width (t_{pwl}) constant at $100ns$. The external experimental circuit setup consists of Marx-bank circuit based pulse generation and an ultra-fast voltage pulse across the device under test (DUT), as shown in Figure 4.1 [66, 84]. The supply voltage is set at two different biases, i.e., either $V_{CC} = 300V$ *or* $V_{CC} = 400V$, such that a breakdown current flows across the reverse biased

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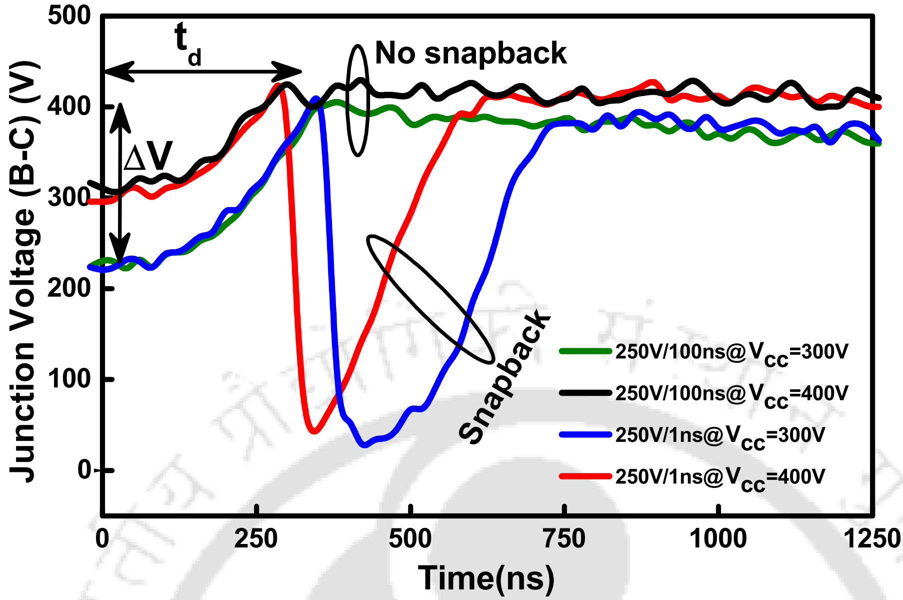

Figure 4.2: Measured base-collector junction voltage-time characteristics of base-emitter shorted configuration of BJT when subjected to variable ultra-fast high voltage pulses, given the circuit parameters shown in Figure 4.1. Erratic (snapback or no snapback) behavior for intermediate ramp speeds is observed. ΔV and t_d are avalanche build-up voltage and build-up time respectively, related to triggering delay of ionization front (discussed in next section).

base-collector junction of the transistor for a considerable time, after which variable ultra-fast pulses are applied. Table 4.1 summarizes device behavior for various rise times.

Initially, the behavior of a BJT structure with base-emitter externally shorted is analyzed. For pulses having a rise time of a few μs, the collector voltage shows oscillation with amplitude of *2V-20V*, as shown in Figure 4.2. If the rise time of the voltage ramp is $100ns$, the device shows erratic behavior, i.e., either no snapback mode, where the device exhibits no collapse in collector voltage and current continues to increase, or snapback mode where the device enters a low voltage and high current state. Therefore, the device shows erratic behavior ("*Snapback*" or "*No snapback*") for high applied voltages, at variable ramp speed ranging from *500ns to 10ns.* Thus, the device exhibits indeterminacy in choosing either of the possible breakdown states, which results in jittery behavior for intermediate ramp speeds. For extremely fast pulses *(e.g., 250V in 1ns)*, the device is guaranteed to go into snapback mode as shown in Figure 4.2. In each of the cases, the device under test exhibits an overvoltage phenomenon (ΔV, shown in Figure 4.2) each time the ultra-fast pulses are applied. After going into the different states, the device recovers to the same voltage that appears across the device in the avalanche (no snapback) mode of breakdown.

For the bipolar device structure with emitter open, each time high voltage pulses with rise time

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<table>
<tr><th rowspan="2">Case</th><th rowspan="2">Ramp rise time</th><th colspan="3">Configuration</th></tr>
<tr><td>Base-Emitter Shorted</td><td>Base Open</td><td>Emitter Open</td></tr>
<tr><td>(a)</td><td>$1\mu s$-$500ns$</td><td>Oscillation</td><td rowspan="2">Erratic Behavior or No Overvolting</td><td>Failure</td></tr>
<tr><td>(b)</td><td>$500ns$-$10ns$</td><td>Erratic Behavior</td><td>Failure</td></tr>
<tr><td>(c)</td><td>$10ns$-$1ns$</td><td>Snapback</td><td>Snapback</td><td>Failure</td></tr>
</table>

Table 4.1: Behavior of different configurations of BJT device structure for various rise times.

ranging from $1ns$ to a few μs are applied across the reverse biased base-collector junction, the device always exhibited thermal secondary breakdown mode (see Table 4.1). Catastrophic failure of the device occurs as it fails to reach the high current and low residual voltage (during snapback) state. For devices with the base-emitter junction shorted, at a particular intermediate ramp speed, after an initial oscillatory behavior, the device reaches a stable state (i.e., high current and low voltage) [84]. The above two different pulsing configurations indicate the role of emitter injection as bipolar turn-on avoids catastrophic failure of the device and results in entering a low voltage state.

Finally, a bipolar structure operated with base open is analyzed, for voltage pulses having a rise time ranging from ns to μs, device did not exhibit overvolting phenomenon and shows erratic behavior (see Table 4.1). For extremely fast voltage pulses with $1ns$ rise time, the device shows snapback behavior, however the device is clamped to a voltage, which is nearly the collector-emitter breakdown voltage (V_{CEO}).

4.3 Two Dimensional TCAD Device Simulation Results and Discussion

The erratic occurrence of the different breakdown modes was analyzed through 2D isothermal physics-based transient mixed-mode device simulations (external circuit is the same as that used for the experiments [84], [66]) using the device simulator Sentaurus (2D TCAD simulator). Electric field dependent mobility, Auger recombination, Shockley-Read-Hall (SRH) recombination, band-gap narrowing and Selberherr impact ionization models are considered in a bipolar structure (shown in Figure 4.1) for various ramp speeds. The device structure exhibits $BV_{CBO} = 180V$, $BV_{CEO} = 160V$ and $f_T = 100MHz$, matching the experimental device. The width of the device, W is $500\mu m$ and an n-epitaxial layer which is fully depleted under breakdown conditions. The depletion width is

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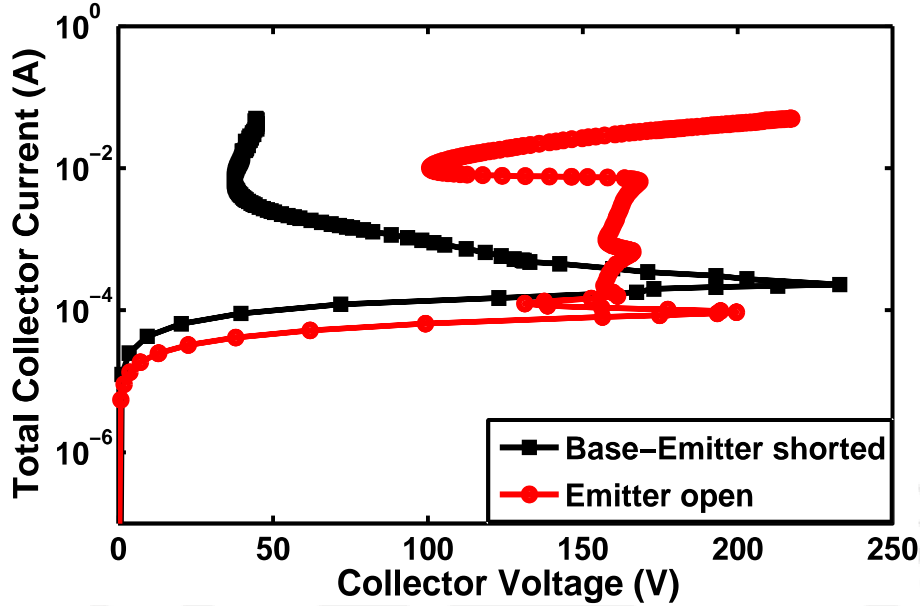

Figure 4.3: TCAD simulated current-voltage characteristics of BJT (DUT) with different configurations such as: (i) base-emitter shorted and (ii) emitter open (i.e., resembling a diode), when voltage ramp of $250V/ns$ is applied across the reverse biased base-collector junction.

$W_{dep} = 8\mu m$, and breakdown electric field of $E_{br} = 2.25 \times 10^5 V/cm$ evaluated from the collector-base breakdown voltage. The donor concentration in the depletion region $(N_d) \approx 1 \times 10^{15} cm^{-3}$ was calculated from capacitance-voltage $(C - V)$ measurements.

4.3.1 Results and Discussion

Figure 4.3 shows the current-voltage $(I-V)$ characteristics, when the base-emitter (BE) is shorted and a voltage ramp of *250V* with rise time of *1ns* is applied, resulting in snapback. However, when the emitter terminal is opened in the layered structure (i.e., resembling a diode), we observe an oscillation when the same voltage ramp is applied, but snapback is not observed. The simulation results agree well with the experimentally observed bipolar turn-on process as the failure to turn on the bipolar structure explains the permanent damage in the device. Thus, the bipolar structure with base-emitter shorted can provide deep insight towards the instability observed in the device.

Figure 4.4 shows the transient behavior of e-current density in the bipolar structure with BE shorted (shown in Figure 4.4), which has been ramped by forcing a current input at the collector terminal. As the device is ramped with a voltage pulse of *250V in 100 ns*, "*filaments*" start to build-up in the structure at t_1 (shown in Figure 4.4 (a)) and the p/n^- junction reaches the breakdown electric field and triggers diode action in the bipolar structure, shown by path-1. At t_2, due to a

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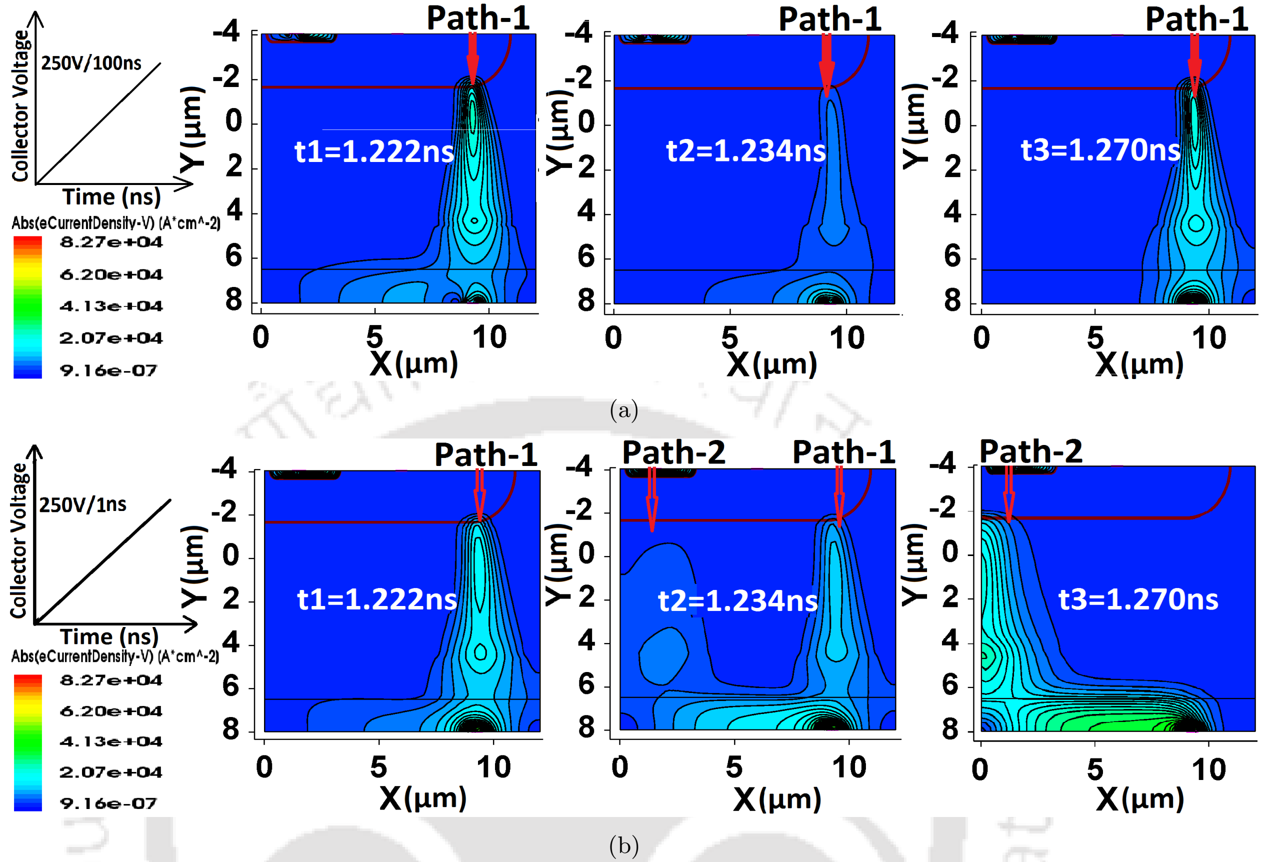

Figure 4.4: Cross section of e-current density (A/cm^2) profile (hyperbolic scale is considered so that clear filaments can be shown), where breakdown current channels are formed. (a) When slower ramp speed (*250V in 100ns*) is applied, filaments dynamically appear at $t_1 = 1.222ns$, but disappear at $t_2 = 1.234ns$ and reappears again at $t_3 = 1.270ns$ and (b) when faster ramp (*250V in 1ns*) is applied, filaments appear at t_1, but it start to take different path at t_2 and then filament, completely shifted from path-1 to path-2 at t_3.

decrease in the electric field and the generation rate, mobile carriers from the filament core disappear, which results in voltage oscillation across the device, as determined by the plasma life-time (mobile carrier lifetime), and a filament again appears at t_3. When a voltage pulse of *250V* is ramped in *1ns* across the same structure, a filament starts to build-up at the p/n^- junction at t_1 and follows path-1 (shown in Figure 4.4 (b)). Eventually another filament starts to build-up across path-2 (where the transport factor is maximum), which is triggered due to strong hole injection in the base at t_2. Moreover, as the injection becomes stronger, the filament shifts from path-1 to path-2, as shown in Figure 4.4 (b) at t_3. To summarize, we see that path-1 (diode action) is triggered in sub *1ns*, while path-2 (bipolar action) is triggered a few *ps* later to complete the process. The above simulations show the physics of coupling of two paths through strong electron injection from the emitter and paths followed by the holes injected into the base region. The bipolar turn-on mechanism depends on

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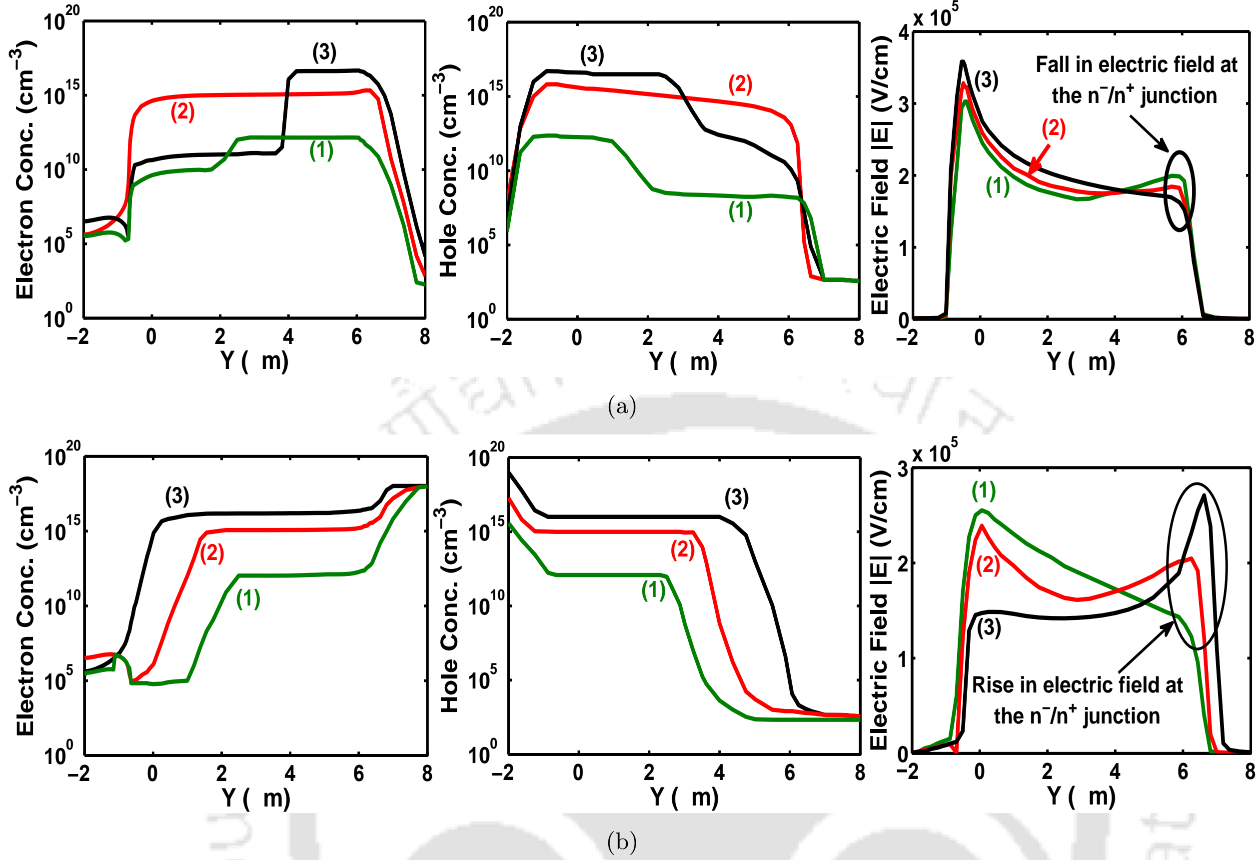

Figure 4.5: The spatial profiles of hole concentration $p(y,t)$, electron concentration $n(y,t)$ and electric field $|E(y,t)|$ in the depletion region, extracted by performing cut-line at $x = 9.5\mu m$ and observed at different time instances; (1) $t_1 = 1.222ns$, (2) $t_2 = 1.234ns$ and (3) $t_3 = 1.270ns$. (a) When slower voltage ramp speed of *250V with rise time of 100ns* is applied, and (b) when faster voltage ramp speed of *250V with rise time of 1ns* is applied.

base thickness, amount of hole injection in the base, base transit time, and rise time of the voltage pulse.

Figures. 4.5 (a) and (b) show the mobile carrier concentration and electric field profile at different times when voltage ramps of *250V/100ns and 250V/ns* are applied to the device for a cut-line at $x = 9.5\mu m$. When a slower voltage ramp is applied, the mobile carriers are more evenly distributed in comparison to the faster voltage ramp. During the separation of the electron and hole concentration profiles in the depletion region, a distributed impact-ionization front (shock wave) and a single self-reinforced moving ionization front (solitary wave like pattern) are observed for the slower and faster voltage ramps, respectively [44], as described in the next sub-section. The profile of electric field changes for both cases in the depletion region with space and time, however, the faster voltage pulse leads to a decrease in electric field within the depletion region and its increase at the n^-/n^+ junction

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as time progresses [38, 40], which results in strong sustained hole injection. However, the slower ramp shows an increase in electric field within the depletion region which decreases towards the n^-/n^+ junction as time progresses, which leads to weak sustained hole injection in the base region. This dependence on ramp speed leads to comparison with the TRAPATT mode of operation. In TRAPATT mode, it has also been observed that large displacement current results in propagation of a shock-wave like pattern in the depleted reverse biased n^-/n^+ junction. Moreover, erratic behavior of the device is observed when an ultra-fast high voltage ramp is applied, which shows that behavior can not be described only by the ramp speed [31]. Therefore, in order to understand the formation of the ionization front and the erratic behavior of the device under strong avalanche injection, appropriate boundary condition at the n^-/n^+ junction (*i.e.*, $J_n = J$ & $J_p = 0$), where J is current density, are required [32].

4.3.2 Formation of moving ionization front in the depletion region

The physics of formation of the ionization front can be understood by looking at the distribution of mobile carriers during the process of impact ionization. The initial build-up of the electric field triggers avalanche breakdown at the p/n^- junction, as electron and hole pairs (EHP) are generated. As the avalanche-generated electrons move towards the n^-/n^+ junction, similarly the avalanche-generated holes move towards the p/n^- junction [40]. Thus, the distribution of generated electrons and holes first peak and as they separate, they modulate the electric field across the junction, as shown in Figure 4.5. Now, separation of the mobile carriers also causes the electric field to decrease within the depletion region, which triggers a moving ionization front (i.e., a single wave) or a shock wave-like pattern at $t_2 = 1.234ns$, which moves towards the n^-/n^+ junction. Separation of the mobile carriers can lead to many possible distributions of the impact ionization front, however triggering of the ionization front is observed at a particular condition, which can be described by following equation:

$$\frac{N_d}{\alpha_0} \leq \left[\frac{W_{dep}(v_{ns}.n(y) - v_{ps}.p(y))}{V_{sat}}\right] \tag{4.1}$$

This above condition shows that the self-reinforced moving ionization front (a single wave) triggering is related to velocity saturation and also the distribution of avalanche-generated carriers in the depletion region. The process is non-deterministic; as ramp speed becomes faster, the relative distribution shows less variation and a moving ionization front is triggered more predictably.

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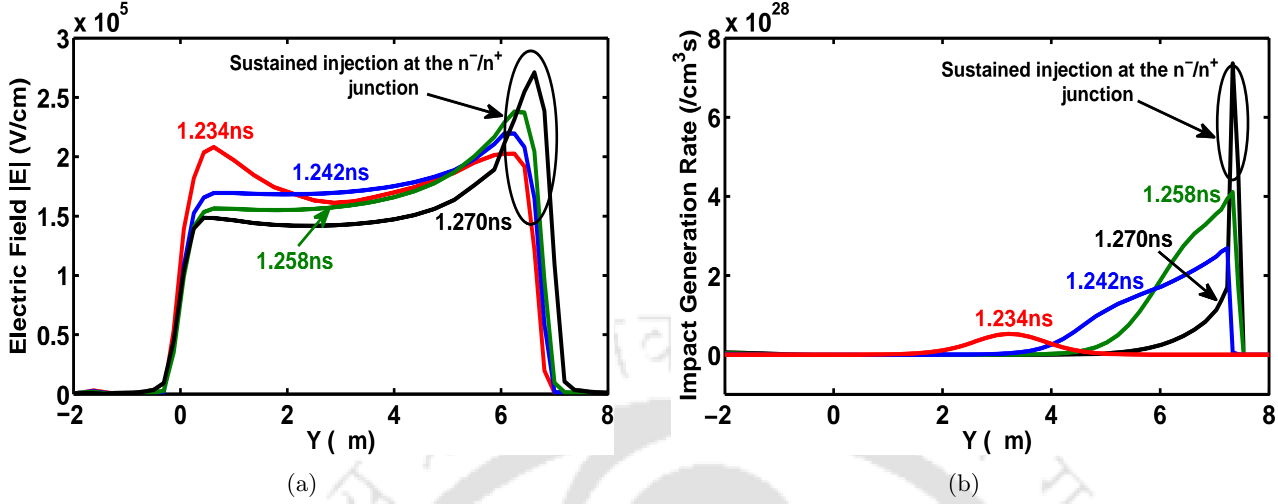

Figure 4.6: The distributions of (a) electric field and (b) moving ionization front in the depletion region at different time instances, wave front is triggered and sustained injection of holes are initiated at time ($t_2 = 1.234ns$) (condition derived in eqn. (1)). The electric field increases and ionization front also sharpens at times *1.246ns and 1.258ns* as it moves towards the n^-/n^+ junction. At time ($t_3 = 1.270ns$), front movement is restricted across the n^-/n^+ region, which leads to strong sustained injection of holes in the base. t_2 and t_3 are related to the time instances shown in Figs. 4 and 5.

4.3.3 Physics of traveling ionization front

The ionization front moves like a single wave (shown in Figure 4.6 (b)), leading to accumulation of electrons at the n^-/n^+ junction for an ultra-fast voltage ramp. Similarly the hole build-up at the diode junction is also formed due to a shock wave like pattern, when subjected to a slower voltage ramp, as shown in Figures 4.5 (a) and (b). The electric field increases and the ionization front of mobile carriers also sharpens as the front progresses towards the n^-/n^+ junction at time instances *1.246ns and 1.258ns*, as shown in Figures 4.6 (a) and (b). When the wave front reaches the n^-/n^+ junction at $t_3 = 1.270ns$, the front movement is restricted across the n^-/n^+ region, which leads to regenerative and strong sustainable back injection of holes in the base region, which explains the erratic behavior (snapback or no snapback) of the device, as shown in Figure 4.7 and described in next section.

4.4 Modeling the instability in device structures

After the voltage ramp is applied, the device exhibits inherent delay (t_d, avalanche build-up time, as shown in Figure 4.2) in the avalanche breakdown process, which leads to an excess breakdown field at the p/n^- junction and also results in excess voltage build-up (ΔV). The excessive multiplication of carriers occurs in the depleted region and their net generation far exceeds charge removed from the boundary. Thus, the changing electric field leads to displacement current at the boundary, wherein the

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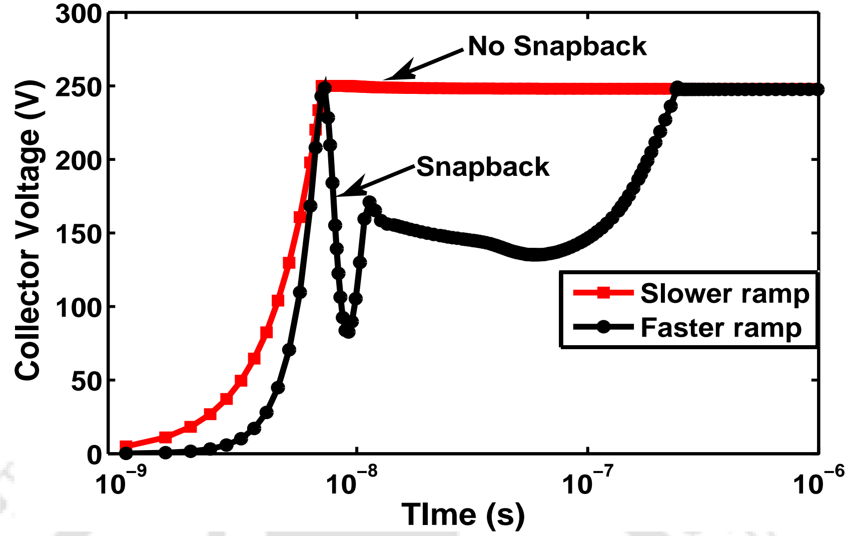

Figure 4.7: TCAD simulated collector voltage-time characteristics of BE shorted configuration of BJT. When voltage ramp of $250V/100ns$ is applied across reverse biased base-collector junction, no impact ionization front formation is observed which results in no snapback behavior. However, when voltage ramp of $250V/ns$ is applied across the reverse biased base-collector junction, moving ionization front is observed, which leads to snapback behavior.

current density far exceeds the initial uniform current density at the contact terminal as the electric field is enhanced across the junctions, shown in Figure 4.5 (b). Therefore, at the n^-/n^+ junction, polarization of mobile charges lead to

$$\frac{\epsilon \partial E(x,t)}{\partial t} > \frac{I_{Total}}{A} \tag{4.2}$$

where A is the area of the depletion region.

Once the ionization front is triggered, displacement current at the contact edge is determined by the moving ionization front. The simulation results show that the moving mobile carriers also modulate electrostatic conditions at the boundary, while forming a filament as shown in Figures 4.4 (a) and (b).

4.4.1 Non-deterministic snapback & bipolar turn-on due to sustained avalanche injection

The sustained back injection of holes from the n^-/n^+ junction can be strong or weak, which depends on unpredictable triggering of the ionization front. The faster ramp should predictably lead to strong hole injection, whereas the slower ramp is not able to trigger the moving ionization front, which leads to weaker hole injection in the base region. The injected holes in the base determine the erratic behavior of the device, which can be understood by the coupling mechanism of the two paths,

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as discussed in the next sub-section. The build-up of potential (BV_{EB}) is needed to establish the flow of holes, which also are electro-statically coupled to the emitter and base regions. The amount of holes required to turn-on the bipolar structure is;

$$p_E = \frac{n_i^2}{N_a} exp\left(\frac{q\eta V_{EB}}{KT}\right) \approx \frac{p_{inj}}{1+\gamma} \tag{4.3}$$

where,

p_E = Injected hole concentration in emitter

n_i = Intrinsic carrier concentration

N_a = Acceptor impurity concentration

q = Electronic charge

η = Ideality factor, ranges from *1 to 2*

V_{EB} = Emitter-base voltage

K = Boltzmann constant

T = Temperature

p_{inj} = Injected hole concentration from base-collector junction

γ = Coupling factor $=\frac{p_B}{p_E}$

p_B = Non-equilibrium hole concentration in the base.

4.4.2 Role of Bipolar Gain & Physics of Coupling

The discussion in the previous sections indicates that in addition to two paths, there are two independent processes (i.e., injection of holes and injection of electrons), which need to be aligned. It has been experimentally observed that snapback features in a bipolar device vary for different manufacturers and different lots [84]. Moreover, it has also been observed that when the rise time of the voltage pulse is faster than one-tenth the maximum transit time (t_r) of the device (i.e., $t_r \approx 1/f_T$), the hole injection from the base-collector junction becomes stronger and couples the two paths, as shown in Figure 4.8 (b). The coupling is primarily determined by hole injection in the base region from the base-collector junction, which can be visualized in a 2D device structure with ref. to Figure 4.4. This coupling is also related to the bipolar gain which is defined by the ratio between total current (i.e., sum of impact ionization current and excess hole injection current, across path-1 and path-2

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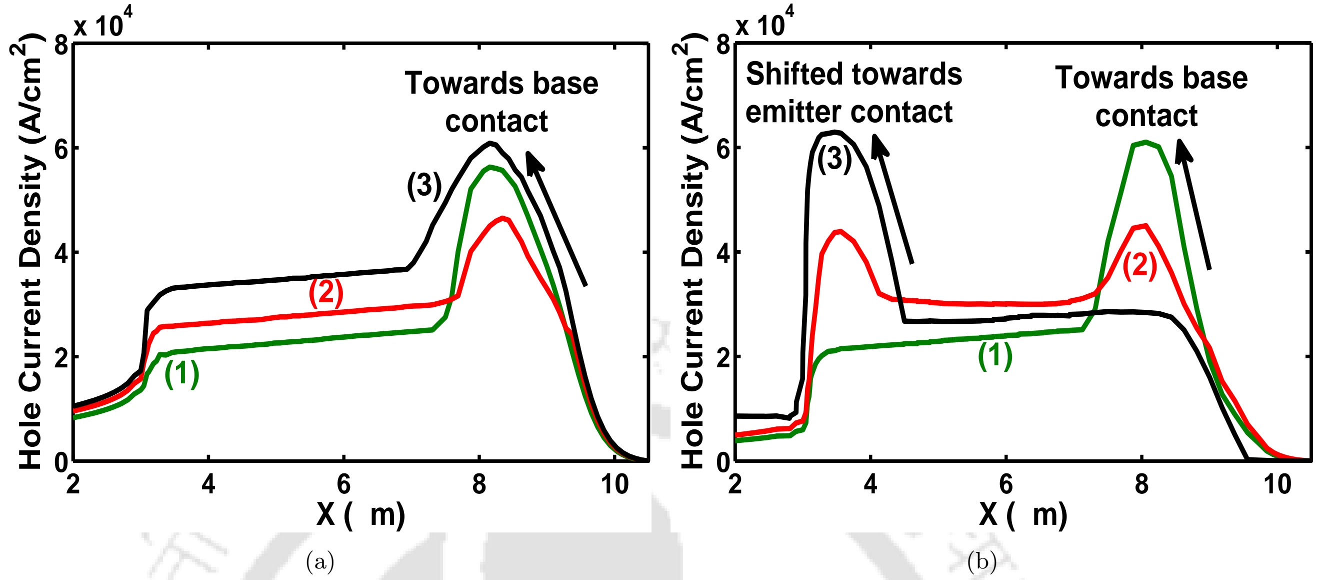

Figure 4.8: The hole current density profile is extracted from cross section of the device structure using a lateral cut-line along the base region at $3\mu m$ below the emitter contact. The sustained injection of holes and its coupling in the base region for (a) slower voltage ramp and (b) faster voltage ramp at different time instance; (1) $t_1 = 1.222ns$, (2) $t_2 = 1.234ns$ and (3) $t_3 = 1.270ns$.

respectively) and the net recombination current in the base region. Therefore, it can be written as;

$$\beta = \frac{(M.I_{co} + I_{hole})\tau_B}{qAW_B p_E(1+\gamma)} \tag{4.4}$$

where,

M = Multiplication factor

I_{co} = Reverse saturation current

$M.I_{co}$ = Avalanche generated current across path-1

I_{hole} = Hole current injected across path-2

τ_B = Base transit time

W_B = Base width.

Figures 4.8 and 4.9 show two paths, where path-1 shows holes collected by the base contact (drift dominated), but as electron injection from the emitter gets stronger, the hole current is dominated by the recombination process in path-2. Injection of electrons in the base is related to barrier lowering, which is electro-statically coupled to injected holes. As the electron injection is initiated, the hole recombination process increases, which leads to less potential build-up and less barrier lowering across the BE junction. The salient features of bipolar coupling can be summarized through the following observations:

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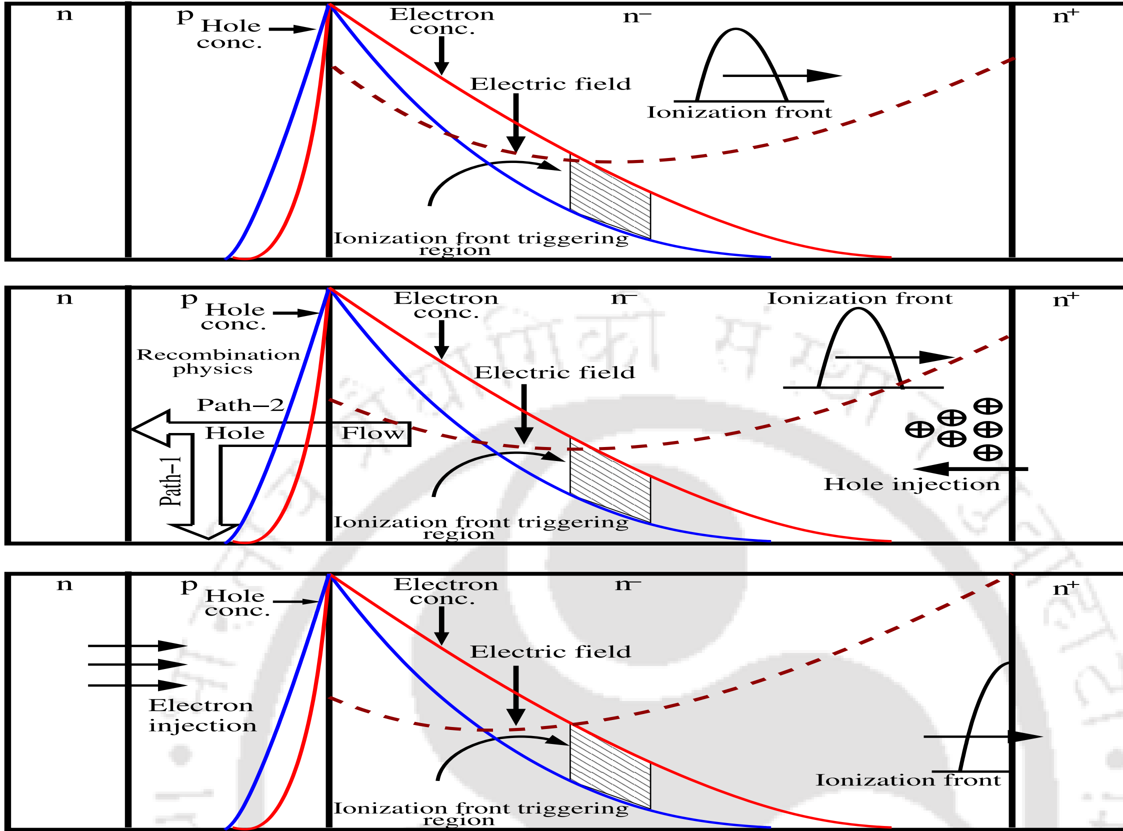

Figure 4.9: Schematic distribution of the mobile carriers which leads to triggering of ionization front, that moves towards the base-collector junction and results in sustained injection of holes from the n^-/n^+ junction, which follows two different paths (i.e., path-1 & path-2). Path-1 shows holes collected by the base contact and path-2 shows electron injection from the emitter and their recombination with injected holes in the base region.

(i) The slower ramp speed not only results in less hole injection, but also in the recombination of injected electrons, which prevents efficient build up. Hence mobile carriers follow path-1, as shown in Figure 4.8 (a).

(ii) The faster ramp speed increases the amount of hole injection, as it establishes more hole build-up. Hence path-2 shows very strong injection of electrons, as shown in Figure 4.8 (b).

(iii) The bipolar structure is unable to turn-on until the coupling occurs in both paths and oscillation takes place till the bipolar structure is unable to turn-on for slower ramp speed. As the ramp speed increases to an intermediate range *(500ns-10ns)*, the device goes into one of the two possible states (i.e., snapback or no snapback).

(iv) Therefore, we conclude that the ramp speed under these conditions should be an order of magnitude less than the transit time corresponding to the maximum switching frequency of the device, where injected electrons efficiently recombine with avalanche-injected holes and do not

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allow the bipolar structure to turn-on regeneratively. As the ramp speed approaches to the time corresponding to switching frequency, holes start to accumulate more efficiently. It triggers a strong bipolar turn-on, and greater coupling of path-1 and path-2 takes place with a strong positive feedback. Thus, when a ramp speed of $10ns$ (i.e., $t_r \approx 1/f_T$) is applied across the device, a strong snapback behavior is guaranteed, which is triggered by back-injection of holes with complete flow of current along path-2.

4.5 Conclusion

In summary, the propagation of an impact ionization wave front caused by accumulation of avalanche-generated carriers is analyzed using 2D simulations. Application of an ultra fast voltage pulse causes the carriers to trigger an ionizing front, which travels in a single wave pattern towards the depleted n^-/n^+ junction. This phenomenon leads to non-deterministic snapback caused by strong or weak sustained avalanche injection of holes from the n^-/n^+ junction to the base region, which results from the regenerative process, as the moving ionization front travels to the contact (i.e., the n^-/n^+ junction). Thus, two basic processes leading to bipolar coupling mechanism are identified as the bipolar structure turns-on: (i) formation of an impact ionization front (single wave) and (ii) the resulting hole injection by avalanche generation at the n^-/n^+ junction, which must be sufficiently high.

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5

Instability due to Triggering of Ionization Front in Base-emitter Externally Shorted Bipolar Structures under High Current Injection Conditions

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Objective

Based on the earlier chapter discussions, we employ a simple analytical model of the instability due to triggering of self-reinforced ionization front in a generic $n/p/n^-/n^+$ bipolar structure whose base-emitter is externally shorted, when subjected to an ultra-fast high voltage pulse. This developed model allows to understand the instability in the semiconductor device structure with different material properties like saturation velocity V_{sat}, impact-ionization coefficient (α), etc. These stated material properties are related to the distribution of mobile carrier and formation of the moving impact ionization front in the reverse-biased base-collector depletion region. Furthermore, the condition for the triggering of self-reinforced ionization front are analytically derived and as it further travels, the avalanche injection mechanisms at the n^-/n^+ junction under high speed current ramp are modeled. It can lead to prominent double injection of avalanche generated holes and electrons from the ohmic contacts, as the high current injection paths get coupled which results in current channel formation and irreversible damage in the device structure.

5.1 Motivation for Analytical Modeling of Bipolar Structure under High Current Injection Conditions

The microscopic understanding of transient behind the breakdown phenomenon under high current injection in the bipolar transistors has been discussed in the earlier chapters [24, 67]. High current injection from the base-emitter junction leads to re-distribution of electric field profile across the depleted region of the collector junction [22], [31]. *Self-reinforced ionization wave-front*" like avalanche breakdown electric field traverses entire depletion region, which results in the collapse of a voltage across the reverse biased base-collector junction and its dependence on displacement current has been discussed in our earlier work [22]. The shape of the moving impact ionization front transverse towards the direction of the front propagation depends on the outer boundaries, the voltage, etc. The moving ionization fronts of various structures-finger-shaped streamers, plane fronts, concentric fronts, etc- have been observed in layered semiconductor device structures. The dynamic avalanche models involving nonlinear processes has been presented to explain the instability and avalanche to streamer transition, which results from the field-enhanced ionization of deep level centres [95], [97]. However, the atomistic model overlooks the underlying electrostatics under the double injection mechanisms from the n^-/n^+ junction, which leads to its snapback has not been discussed in the literature [65], [111].

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Also, the high current injection from n^-/n^+ structure has been extensively studied, wherein the reverse injection under high current condition during this dynamic avalanche process is somewhat less clearly addressed [85]. Therefore, we revisit and analyze the role of moving ionization-front and study the voltage collapse due to avalanche injection at the n^-/n^+ junction for the first time. We further explore the role of emitter injection to understand indeterminacy associated with the current channel formation and snapback mechanisms, where-in the state of breakdown is determined through several competing processes.

In the course of this chapter, the value of V_{sat} and α are varied in the high voltage bipolar structure whose base-emitter is externally shorted and an ultra-fast high voltage ramp pulse is applied across reverse biased collector junction, one of the two entirely different modes of breakdown is observed. The numerical simulations were performed through 2D TCAD commercial device simulator under the same condition by giving a similar ramp input to the bipolar structure. The formation of ionization front and its propagation has been revisited and the role of distribution of mobile carriers was discussed and analytically modeled. Furthermore, the role of emitter injection and build-up of the electric field across the n^-/n^+ junction due to triggering of the moving ionization-front are discussed, which dictates the formation of breakdown current channel at the n^-/n^+ junction.

5.2 Two Dimensional TCAD Device Simulation Results and Discussion

Generic nature of the above experimentally observed instability was analyzed through 2D isothermal physics-based transient mixed-mode device simulations (external circuit is given in Figure 5.1) using the device simulator Sentaurus (2D TCAD simulator), wherein the electric field dependent mobility model, Auger recombination, Shockley-Read-Hall (SRH) recombination, band-gap narrowing and Selberherr impact ionization are used for simulation purpose in a bipolar structure (shown in Figure. 5.1) with base-emitter shorted for various values of V_{sat} and α. Device structure was built to match $BV_{CBO} = 180V$, $BV_{CEO} = 160V$, $f_T = 100MHz$ and maximum current is $0.6A$ of the experimental device under test, and also assumed that the n-epitaxial layer was fully depleted under breakdown conditions. For the simulation purpose we have considered depletion width of $W_{dep} = 8 \times 10^{-4} cm$, and total area $(A) = 25 \times 10^{-4} cm^2$. We calculated current density of $J = 4 \times 10^4 A/cm^2$ and breakdown electric field of $E_{br} = 2.25 \times 10^5 V/cm$ from the given maximum current and collector-base breakdown voltage respectively (see chapter-3). Moreover, depletion donor concentration $(N_d) \approx 10^{15} cm^{-3}$ and

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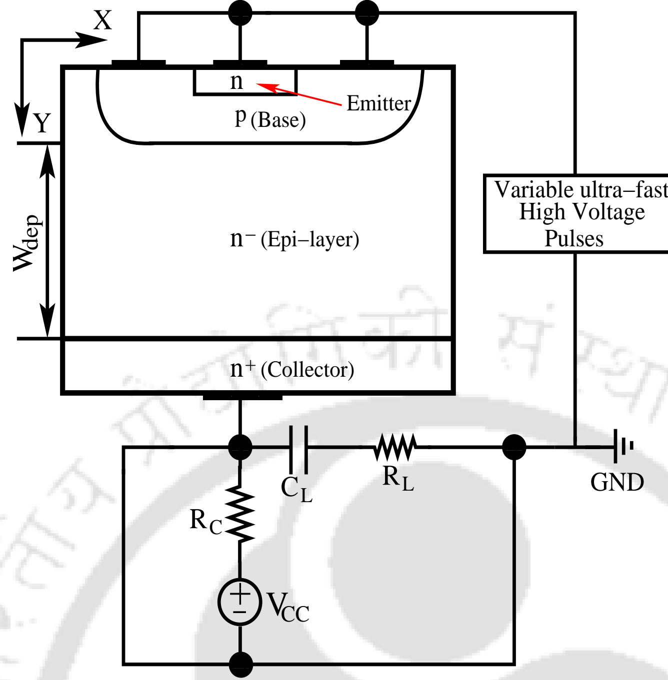

Figure 5.1: The mixed-mode circuit simulation setup and schematic cross-section of bipolar junction transistor, where W_{dep} represents the depletion width. External circuit components values are $R_L = 1M\Omega$, $C_L = 2nF$, $R_C = 5.6M\Omega$, and supply voltage is initially biased at $(V_{CC}) = 300V$. The base-emitter shorted configuration of bipolar structure was used for simulation purpose. The doping values of bipolar transistor in different regions are $N_E = 10^{19}cm^{-3}$, $N_B = 10^{17}cm^{-3}$, $N_{Epi} = 10^{15}cm^{-3}$ and $N_C = 10^{19}cm^{-3}$.

critical current density $J_{crit} = q.N_d.V_{sat} \approx 2 \times 10^4 A/cm^2$ were calculated from given device breakdown voltage, as we have done in chapter-3. In this simulation setup, surface traps were also accounted near the boundary, because these bugs or traps are always present in a real device.

5.2.1 Numerical Consideration

The accuracy of the solution is determined by specifying proper boundary conditions in the numerical solver. However, specifying both Dirichlet and Neumann boundary conditions leave the system over-determined. The numerical analysis of the bipolar phenomenon in these 2D bulk structure, primarily involves Neumann boundary conditions across the collector contact and all side of the device structure, however Dirichlet boundary condition is used as base and emitter contacts (since both are grounded), which can approximate the physical model under high current injection condition. Neumann boundary condition states that the derivative of solution parameter (ψ) on the boundary of the domain must be satisfied by the partial differential equation, when a current source is connected to the contacts. Therefore, we consider total current and $\frac{\delta\psi}{\delta n} = E_{br}$ as boundary condition (since it is assumed that at $t = 0$, depletion region is formed), across the 2D device structure, for solving

Poisson's equation and current continuity equation. The boundary condition for both the junctions (i.e., p/n^- & n^-/n^+) are specified as:

$$\text{at } p/n^- \quad J_p(p/n^-) = J_{p0} \quad J_n(p/n^-) = 0 \quad \text{and}$$

$$\text{at } n^-/n^+ \quad J_n(n^-/n^+) = J_{n0} \quad J_p(n^-/n^+) = 0$$

Where J_{p0} and J_{n0} are the hole and electron current densities. An application of these above boundary conditions show the relation between total current (I) and applied potential (V). Moreover, self-organization behavior of the mobile carriers across both the junctions have been observed, as discussed in next subsection. Therefore, it is obvious that for different ramp speed, it will provide the unique solution and accurate relation between current and voltage.

5.2.2 Results and Discussion

Numerical simulation was performed through variations of saturated drift velocity (V_{sat}) and impact-ionization coefficient (α), and by giving a ultra-fast voltage ramp input of $250V$ with a rise time of $1ns$ to the reverse biased base-collector junction of the bipolar transistor whose base-emitter is shorted. Therefore, the dependence of device behavior on the voltage ramp speed shows a similarity to displacement current in base-emitter externally shorted configuration of the bipolar transistor. In these devices, it has been observed that large displacement current density causes propagation of a wave-front like pattern in the depleted base-collector junction [24, 31]. We had also made similar observations in our simulation results, wherein increase in the order of V_{sat} and α resulted in erratic snapback behavior, as shown in Figure 5.2. This shows that the phenomenon may not be explained purely by only the ultra-fast high voltage ramp rise time. For a higher value of saturated drift velocity ($V_{sat}(electron) = 1.07 \times 10^8 cm/s$, $V_{sat}(hole) = 8.37 \times 10^7 cm/s$), prominent self-reinforced ionization front is not observed (within the time scale between each sampled data point), thus snapback mode is not observed in the current-voltage ($I-V$) characteristics (shown in Figure 5.2 (a)). Whereas for a lower value of V_{sat} ($i.e., V_{sat}(electron) = 1.07 \times 10^6 cm/s$, $V_{sat}(hole) = 8.37 \times 10^5 cm/s$), the moving ionization front is triggered deterministically in the depletion region. However, under lower V_{sat} conditions, the response time for avalanche generation is prolonged, as it takes much longer for it to equal the background doping concentration (due to higher transit time). Under this condition, stronger growth of avalanche wave-front due to prominent injection at the n^-/n^+ contact, which results in the stronger snapback. The role of avalanche injection phenomenon at the junctions causing snapback

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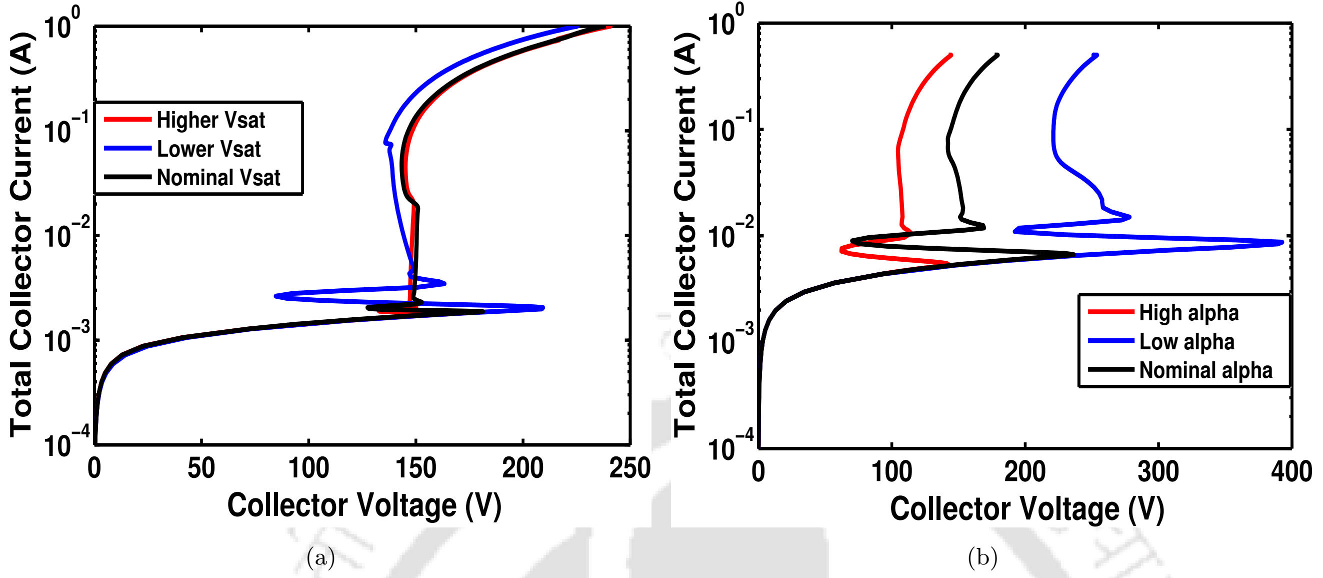

Figure 5.2: TCAD simulated current-Voltage characteristics of base-emitter shorted configuration of BJT when subjected to ultra-fast high voltage pulse of $250V/ns$, non-deterministic snapback behavior is observed at (a) different values of carrier saturation velocity (V_{sat}), and (b) different value of impact-ionization coefficient (α).

can be observed in the $I - V$ curve, shown in Figure 5.2 (a). For lower (V_{sat}) condition shows an excess build-up voltage of $75V$ across the device for the similar voltage ramp, and this causes a strong snapback and highly localized filamentation as compared to partial snapback for a nominal value of V_{sat} $(i.e., V_{sat}(electron) = 1.07 \times 10^7 cm/s$, $V_{sat}(hole) = 8.37 \times 10^6 cm/s$, as shown in Figure 5.2 (a).

Whereas, when an impact ionization coefficient (α) is varied (an order of magnitude higher or lower), snapback mode is observed in all the cases, as shown in Figure 5.2 (b). As the value of α changes from lower to higher, it shows an excess build-up of voltage across the device structure for the similar voltage ramp of $250V$ with rising time of $1ns$, which results in strong snapback in the case of higher α $(i.e., \alpha_n = 7.03 \times 10^6 cm^{-1}$, $\alpha_p = 1.582 \times 10^7 cm^{-1})$ and highly localized filamentation as compared to partial snapback for nominal value of α $(i.e., \alpha_n = 7.03 \times 10^5 cm^{-1}$, $\alpha_p = 1.582 \times 10^6 cm^{-1})$, as shown in Figure 5.2 (b). In order to understand the non-deterministic snapback behavior of bipolar transistor under both the conditions, internal carrier dynamics of the device structure is analytically modeled in this chapter. The transient of current-voltage characteristics at different time instances is discussed here to analyze physical processes in the bipolar structure and validation of numerical simulation observations.

Figure 5.3 shows the dynamic avalanche transient numerical simulation results and describe the occurrence of physical processes in the device structure towards understanding the switching behavior

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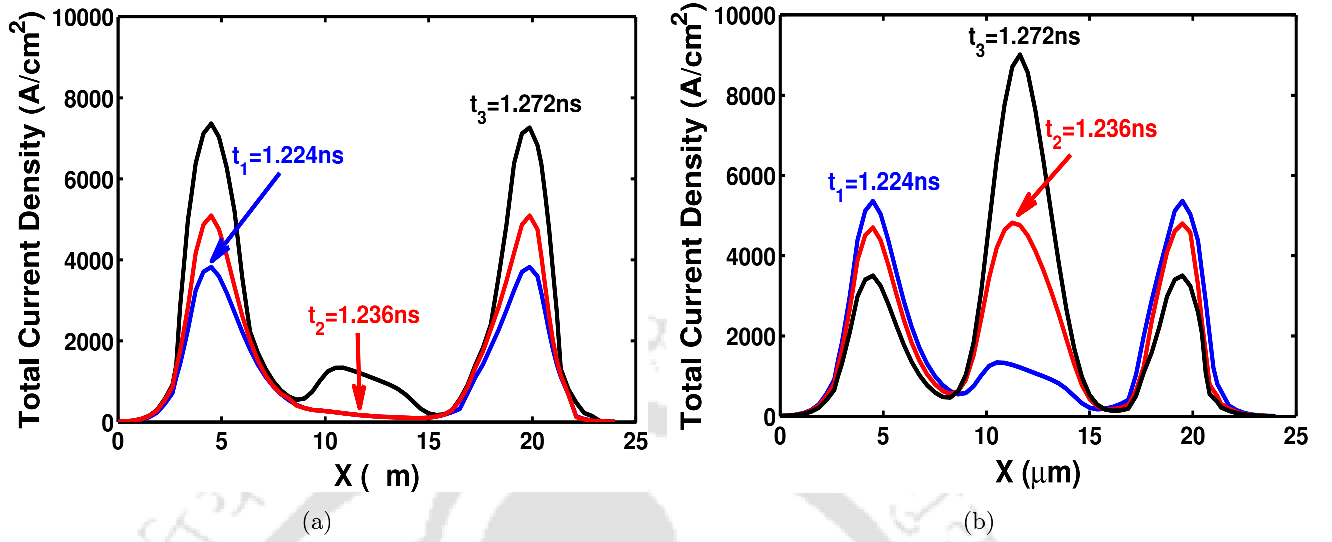

(a) (b)

Figure 5.3: The total current density profile is observed through a lateral cut-line along the base region at 3.5μm across the cross-section of the bipolar transistor, when ultra-fast voltage ramp of (*250V in* 1*ns*) is applied. (a) For higher V_{sat} and (b) For lower V_{sat}.

of total current density profile when performed lateral cut-line across the bipolar transistor whose base-emitter is externally shorted, and ramped by applying a current input at the reverse biased base-collector terminal. As the voltage across the bipolar transistor is ramped with *250V in* 1*ns* for higher V_{sat} conditions, at t_1 "*mobile carriers*" start to move towards the base contact, as the p/n^- junction reaches the breakdown electric field and triggers the diode action in the structure, called as path-1. At t_2 and t_3, as the breakdown electric field increases and hence generation rate, the more number of mobile carriers start moving towards the base contact and amplitude of current density increases across path-1, as shown in Figure 5.3 (b). Whereas, for lower V_{sat}, a current density starts to build-up at the p/n^- junction at t_1 and follows path-1. Eventually, current density starts to build-up across path-2 (where transport factor is maximum or towards emitter contact), which is triggered due to strong sustained injection of holes in the base region at t_2. Moreover, as the injection of holes becomes stronger, the current density profile shifts from path-1 to path-2, as shown in Figure 5.3(b) at t_3. However, we see that path-1 (diode action) is triggered in sub *1ns*, while path-2 (bipolar action) is triggered in only some few *ps* to complete the process. Furthermore, shifting of paths has not been seen as the thickness of base increases. Above, simulations show the physics of coupling through a strong base injection of electrons and the paths followed by holes injected into the base region. Thus, the bipolar turn-on mechanism is dependent on the base thickness, the amount of hole injection in the base (determined by dynamic avalanche model), its transit time, and the rise time of the voltage

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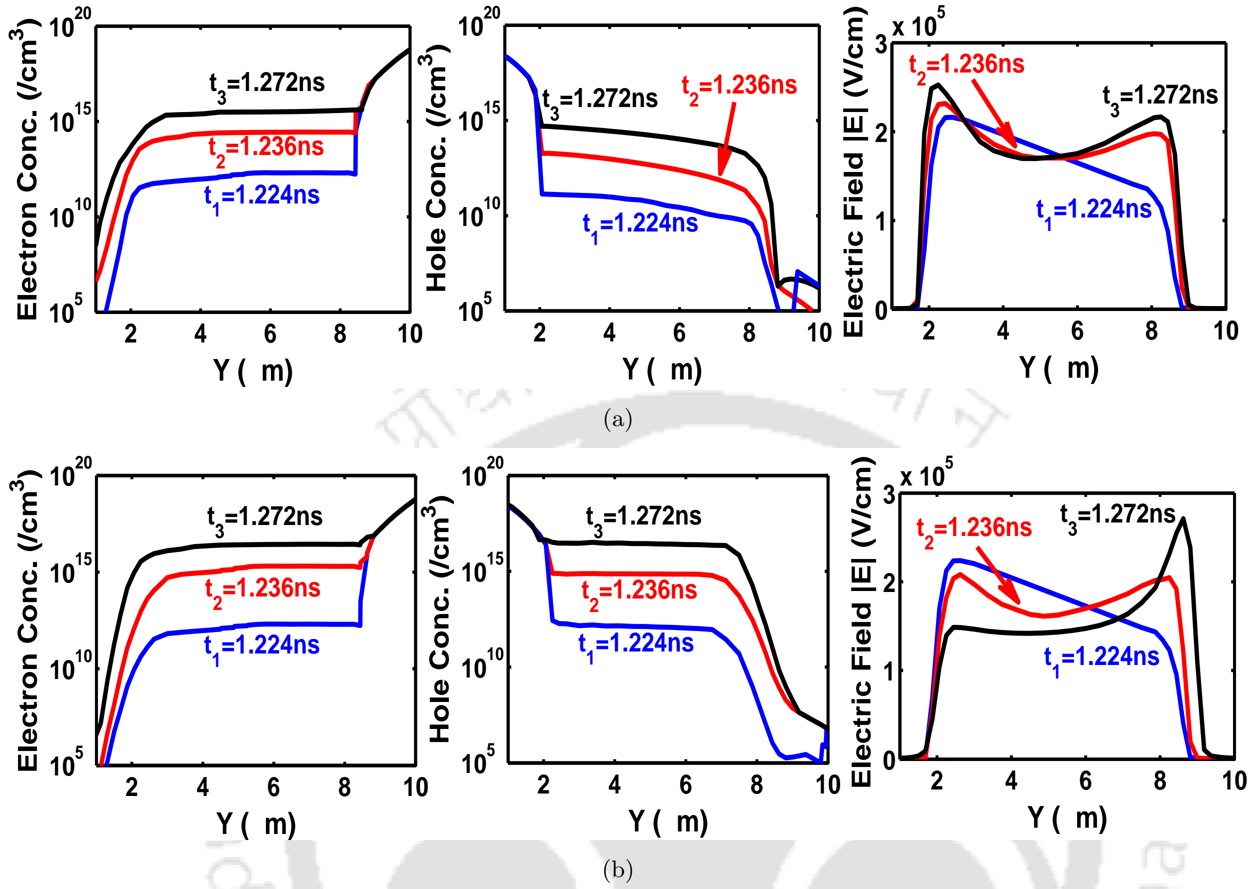

Figure 5.4: The spatial profiles of hole concentration $p(y,t)$, electron concentration $n(y,t)$ and electric field $|E(y,t)|$ in the depletion region, extracted by performing cut-line at $x = 12\mu m$ and observed at different time instances; (1) $t_1 = 1.224ns$, (2) $t_2 = 1.236ns$ and (3) $t_3 = 1.272ns$. (a) For higher V_{sat} and (b) For lower V_{sat}.

pulse.

Figures 5.4 (a) and (b) show the electric field and carrier concentration profile at different time instances for higher and lower V_{sat} conditions respectively, which is obtained by performing longitudinal cut-line at $x = 12\mu m$. It is observed that, for higher V_{sat} condition, the mobile carriers are more evenly distributed in comparison to lower V_{sat} conditions. During the separation of electron and hole concentration profile in the depletion region, two different kinds of non-linear impact ionization fronts: either distributed or single wave-like pattern (self-reinforcing moving ionization front) are observed for higher and lower V_{sat} conditions respectively, as described in next section. Moreover, the electric field dips in both the cases however for lower V_{sat} condition leads to fast rise in the electric field at the n^-/n^+ junction which results in strong sustained hole injection, however for higher V_{sat} condition shows slow rise in the electric field profile and weak sustained hole injection at n^-/n^+ junction are observed. Therefore, in order to understand the formation of moving ionization front

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and non-deterministic snapback behavior of the device structure under strong avalanche injection mechanism needs appropriate boundary conditions at both the junctions.

5.3 Modeling Propagating Ionization Front under Strong Avalanche Injection

In this section, we describe the phenomenology of triggering of ionization front and its propagation through uniformly doped epi-layer (n^-) under high current injection conditions. An analytical condition for the triggering of self-reinforced ionization front is derived when voltage ramp of $250V/1ns$ is applied to the bipolar transistor. Furthermore, the profile of moving ionization front are modeled through dynamic drift-diffusion, Poisson's and continuity equation of mobile carriers. The profile of moving impact ionization front and electric field are obtained at different time instances through the numerical simulations and as the front moves towards the junctions leads to weak or strong injection of mobile carriers has been discussed.

5.3.1 Phenomenology of self-reinforced ionization front triggering

The physics of formation of the moving ionization front in the reverse-biased base-collector junction can be understood by looking at the mobile carrier distribution when an ultra-fast voltage ramp is applied across the base-emitter shorted configuration of the bipolar transistor. The initial build-up of the electric field (shown in Figure 5.4 (b)) triggers avalanche breakdown at the p/n^- junction which results in the generation of the electron and hole pairs (EHPs). As the avalanche-generated electron start moving towards the n^-/n^+ junction, while the avalanche-generated holes move towards the p/n^- junction. However, some of the mobile carriers seed a region of higher electron and hole concentration in the depletion region. The distribution of generated electrons and holes first peaks and as it separates modulates the electric field at both the junctions, which can be seen in Figure. 5.4 (b). The separation of mobile carriers also causes the electric field to dip within the depletion region, triggers a self-reinforced ionization front (i.e., a single wave) and a shock wave-like pattern which moves towards the n^-/n^+ junction. To understand this mechanism and approximate analytical model of electron and hole concentration is needed to find the condition for the formation of moving ionization front.

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5.3.2 Condition for the triggering of moving ionization front

Let us consider a differential element between y and $y + dy$, as shown in Figure 5.5. dp holes and dn electrons cross this (dy) distance per unit time. In crossing the differential distance, $\alpha_p p(y) v_{ps}$ holes and $\alpha_n n(y) v_{ns}$ electrons are generated, where α_p and α_n are the hole initiated rate and electron initiated rate respectively. The electron and hole saturated drift velocities are v_{ns} and v_{ps} respectively. Thus, the hole and electron generation rates are given by:

$$\frac{dp}{dt} = \alpha_p.v_{ps}.p(y) \quad and \quad \frac{dn}{dt} = \alpha_n.v_{ns}.n(y) \tag{5.1}$$

Solving the above equation and integrating both sides we get,

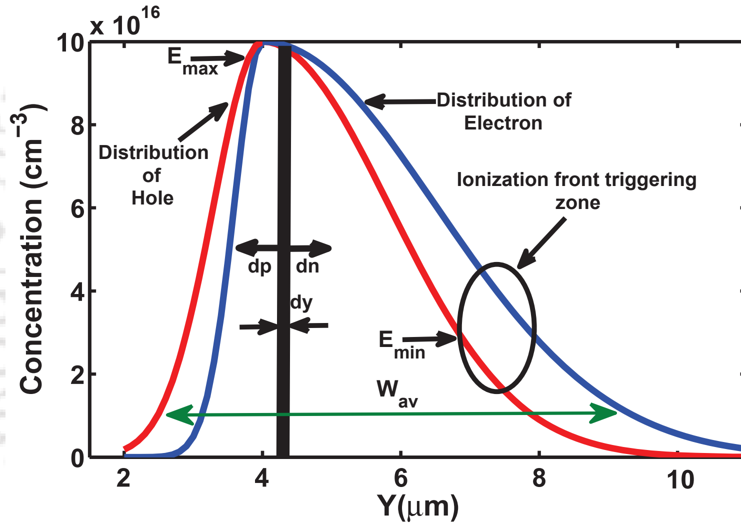

Figure 5.5: Schematic distribution of electron and hole concentrations, obtained by impact ionization process and seeding of carriers in the depletion region, where recombination of carriers are neglected. W_{av} ($i.e., W_{av} < W_{dep}$) represents avalanche zone width.

$$p(x,t) = p_0(t).exp\left[\alpha_p.v_{ps}\int_0^{W_{av}} exp\left(\frac{E_{br}}{E_{max}}\right).dx\right] \tag{5.2}$$

$$n(x,t) = n_0(t).exp\left[\alpha_n.v_{ns}\int_0^{W_{av}} exp\left(\frac{E_{br}}{E_{max}}\right).dx\right] \tag{5.3}$$

where, E_0 and E_{max} is initial build-up of electric field and maximum electric field respectively. The dynamics of charge carriers and electric field distribution can be approximated by Poisson's equation:

$$\frac{dE(y,t)}{dy} = -\frac{q}{\epsilon_{si}}\left[n(y,t) - p(y,t) - N_d\right] \tag{5.4}$$

Where ϵ_{si} represents permittivity of silicon. The separation of the mobile carriers cause the electric field to decrease within the depletion region (discussed earlier). Therefore, the distribution of electric

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Figure 5.6: Schematic distribution of the (a) electric field and (b) net charge distribution (i.e., $N_d - n + p$) in the depletion region. Red and blue arrows show centroid of negative and positive charges respectively. Under the conditions of minima observed in the electric field, one observes that negative mobile charges are imaged by fixed positive charge across the N_{d+} contact.

field reshapes its profile w.r.t. time, as shown in Figure 5.4. Thus, it can be written as:

$$\frac{dE}{dy} = -\frac{q}{\epsilon_{si}}\left[(n_0 + dn) - (p_0 + dp) - N_d\right] \tag{5.5}$$

$$\frac{dE}{dy} = -\frac{q}{\epsilon_{si}}\left[(n_0 - p_0 - N_d) + \int_0^{t_d}\left(\frac{dn}{dt} - \frac{dp}{dt}\right)dt\right] \tag{5.6}$$

Putting equation 5.1 in the above equation 5.6, then we have

$$\frac{dE}{dy} = \frac{dE_0}{dy} - \frac{q}{\epsilon_{si}}\int_0^{t_d}\left[\alpha_n.v_{ns}.n(y) - \alpha_p.v_{ps}.p(y)\right]dt \tag{5.7}$$

The separation of avalanche generated electron and hole pairs, constituting the plasma triggers the ionization front. The avalanche zone width (W_{av}) over which this plasma is spread, has two distinct distributions of electron and hole concentrations, as shown in Figure 5.5. Each of the distribution is convoluted as it evolves over time and space, as avalanche zone width increases. Now, we can get an approximate solution for condition of triggering ionization front by looking at the derivatives of field and the potential, even without an accurate analytical model for mobile carriers.

Now, if we assume $\alpha_n = \alpha_p = \alpha_0$, $t_d \approx \int_0^{W_{av}} \frac{1}{v(y)}dy = \frac{W_{av}}{V_{sat}}$ (assuming that the mobile carrier concentration increases both with avalanche multiplication and transit of carriers, however the width of avalanche zone ($i.e., W_{av} < W_{dep}$) is principally due to transit and much less due to multiplication),

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$V_{sat} = \frac{v_{ns}+v_{ps}}{2}$ and $\frac{dE_0}{dy} \approx \frac{qN_d}{\epsilon_{si}}$ (assuming complete ionization in the depletion region under depletion approximation, (i.e., $N_d >> (n_0 - p_0)$, where n_0 and p_0 are intrinsic electron and hole concentrations respectively), then we get

$$\frac{dE}{dy} = \frac{qN_d}{\epsilon_{si}} - \frac{q.\alpha_0.W_{av}}{V_{sat}.\epsilon_{si}} [v_{ns}.n(y) - v_{ps}.p(y)] \tag{5.8}$$

Under dynamic avalanche conditions, the first peak of electric field (i.e., maxima) is observed at the interface of the p/n^- junction. Therefore, the generation rate of mobile carriers is highest at the interface. As the concentration of mobile carriers increases in the depletion region, it may lead to triggering of the ionizing front as they separate. Even if region-I has the highest concentration of mobile carriers, the difference of $(n - p)$ will be much less than N_d, showing that the electrostatics of this region is primarily influenced by the background donor charges (i.e., N_d). The ionization front is triggered at the interface of region-II and region-III, where the net am-bipolar charge (i.e, $(n - p)$) modulates the electric field.

As shown in Figure 5.6, another extrema (i.e., minima) of electric field distribution is observed at y_1, by setting equation 5.8 to zero. In order to prove that y_1 corresponds to minima, second order differentiation of the electric field is evaluated for step h (i.e., very small change of y):

$$\left.\frac{d^2E}{dy^2}\right|_{y_1} = \frac{\left.\frac{dE}{dy}\right|_{y_1+h} - \left.\frac{dE}{dy}\right|_{y_1-h}}{2h} = -\frac{\frac{q}{\epsilon_{si}}[N_d - n + p]}{h} < 0 \tag{5.9}$$

As per the evaluation in equation 5.9, a maxima should be observed at y_1. Instead a minima is seen because the absolute value of electric field distribution is considered in all simulations.

Thus a self-reinforced moving ionization front is triggered once the condition of minima of electric field distribution within the depletion region sets at time $t_2 = 1.234ns$ and the wave front sharpens as it progresses towards the n^-/n^+ junction, as shown in Figure 5.4. After solving equation 5.9 by substituting $\frac{dE}{dy} = 0$, the condition for the front triggering can be given as:

$$\frac{N_d}{\alpha_0} \leq \left[\frac{W_{dep}(v_{ns}.n(y) - v_{ps}.p(y))}{V_{sat}}\right] \tag{5.10}$$

The condition derived in equation 5.10 indicates that once the amount of mobile carriers in the avalanche zone width (W_{av}) exceeds N_d, it will be imaged by depleted N_{d+} ions at the n^-/n^+ junction, as shown in Figure 5.6. This physical insight self-consistently defines the critical condition for establishing an ionizing front as it triggers sustained injection from the n^-/n^+ junction.

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5.3.3 Modeling the dynamic ionization wave-front

The standard set of equations under dynamic avalanche injection is given by continuity, transport and Poisson's equation:

$$\frac{\partial n(x,t)}{\partial t} = D_n \frac{\partial^2 n(x,t)}{\partial x^2} + \frac{\partial n(x,t)}{\partial x} v_{ns} + G(n,p,E) \tag{5.11}$$

$$\frac{\partial p(x,t)}{\partial (t)} = D_p \frac{\partial^2 p(x,t)}{\partial x^2} - \frac{\partial p(x,t)}{\partial x} v_{ps} + G(n,p,E) \tag{5.12}$$

where *n(x, t)* and *p(x,t)* are electron and hole concentration, v_{ns} and v_{ps} are saturated drift velocities of electron and hole, and N_d is the constant background doping concentration of the depletion region.

The impact ionization rate is given by:

$$G(n,p,E) = n\alpha_n v_{ns} + p\alpha_p V_{ps} \tag{5.13}$$

where α_n and α_p are electron and hole initiated impact ionization coefficients. The dynamic avalanche can be modeled by coupling the rate equation for hole and electron avalanche generation, which describes the spatial and temporal behavior of generation mechanisms. Here, recombination in the sub ns time-scale is neglected and the diffusion term is neglected because drift component is more dominant compared to diffusion component. Now, if we assume $D_n = D_p = D_A$, $v_{ns} = v_{ps} = V_{sat}$ and $\alpha_n = \alpha_p = \alpha_0$, then equation reduces to:

$$\frac{\partial n(x,t)}{\partial t} = D_A \frac{\partial^2 n(x,t)}{\partial x^2} + \frac{\partial n(x,t)}{\partial x} V_{sat} + G(n,p,E) \tag{5.14}$$

$$\frac{\partial p(x,t)}{\partial (t)} = D_A \frac{\partial^2 p(x,t)}{\partial x^2} - \frac{\partial p(x,t)}{\partial x} V_{sat} + G(n,p,E) \tag{5.15}$$

$$G(n,p,E) = \alpha_0 V_{sat}(n+p) \tag{5.16}$$

The condition for triggering of moving ionization front across the depletion region was derived as:

$$\frac{N_d}{\alpha_0} \leq \left[\frac{W_{dep}(v_{ns}.n(y) - v_{ps}.p(y))}{V_{sat}}\right] \tag{5.17}$$

Putting all the above assumption in equation 5.16 and 5.17, then we have

$$(n+p) = \frac{G(n,p,E)}{\alpha_0 V_{sat}} \tag{5.18}$$

$$(n-p) = \frac{N_d.V_{sat}}{\alpha_0.W_{dep}} \tag{5.19}$$

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By adding equations 5.14 and 5.15, we get

$$\frac{\partial(n+p)}{\partial t} = V_{sat}\frac{\partial(n-p)}{\partial x} + D_A\frac{\partial^2(n+p)}{\partial x^2} + 2G(n,p,E) \tag{5.20}$$

$$G(x,t) = G(x - V_{sat}t) \tag{5.21}$$

Putting equations 5.18, 5.19 and 5.21 in equation 5.20 and solving this equations, we get:

$$\frac{\partial G}{\partial t} + \frac{2G}{\alpha_0(n+p)}\frac{\partial G}{\partial x} + \frac{\partial^3 G}{\partial x^3} = 0 \tag{5.22}$$

Substituting the trial solution 5.21 into 5.22, then it leads to the Ordinary Differential Equation:

$$-V_{sat}\frac{\partial G}{\partial x} + \frac{2G}{\alpha_0(n+p)}\frac{\partial G}{\partial x} + \frac{\partial^3 G}{\partial x^3} = 0 \tag{5.23}$$

Integration of above equation 5.23 can be done directly since it is a form of a total derivative. We get;

$$-V_{sat}G + \frac{G^2}{\alpha_0(n+p)} + \frac{\partial^2 G}{\partial x^2} = c_1 \tag{5.24}$$

where c_1 represents the constant of integration. In order to obtain a first order equation for G, multiplication with $\frac{\partial G}{\partial x}$ can be done;

$$-V_{sat}.G\frac{\partial G}{\partial x} + \frac{G^2}{\alpha_0(n+p)}.\frac{\partial G}{\partial x} + \frac{\partial^2 G}{\partial x^2}.\frac{\partial G}{\partial x} = c_1.\frac{\partial G}{\partial x}$$

$$-V_{sat}.G\partial G + \frac{G^2}{\alpha_0(n+p)}\partial G + \frac{\partial^2 G}{\partial x^2}\partial G = c_1\partial G$$

Integration on both sides (with c_2 as the constant of integration) leads to;

$$-\frac{V_{sat}}{2}G^2 + \frac{G^3}{3\alpha_0(n+p)} + \frac{1}{2}\left(\frac{\partial G}{\partial x}\right)^2 = c_1 G + c_2 \tag{5.25}$$

Now it is required that in case $x \to \infty$, we should have $G \to 0$, $\frac{\partial G}{\partial x} \to 0$ and $\frac{\partial^2 G}{\partial x^2} \to 0$. From these requirements it follows $c_1 = c_2 = 0$.

With $c_1 = c_2 = 0$, equation 5.25 can be written as;

$$\left(\frac{\partial G}{\partial x}\right)^2 = G^2\left(V_{sat} - \frac{2G}{3\alpha_0(n+p)}\right) \tag{5.26}$$

By seperation of variables we may write;

$$\int_0^G \frac{dG}{G\sqrt{\left(V_{sat} - \frac{2G}{3\alpha_0(n+p)}\right)}} = \int_0^L dx \tag{5.27}$$

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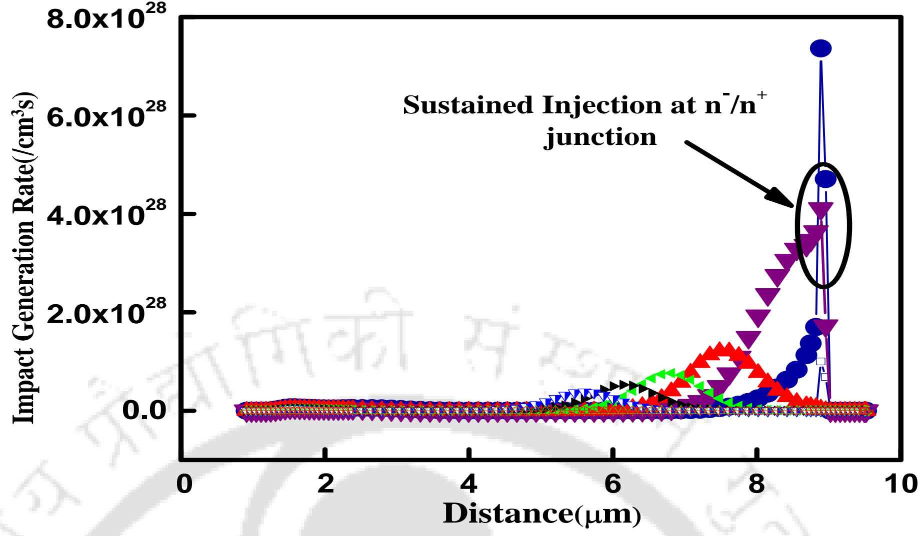

Figure 5.7: Analytical model of traveling ionization front in the depletion region and showing sustained injection of mobile carrier as it moves towards the n^-/n^+ junction.

The choice of 0 for the lower integration limits does not bring any loss of generality since the starting point can be transformed linearily. The integration of the left hand side of equation 5.27 can be done by using a transformation.

$$G = \frac{3\alpha_0(n+p)}{2} V_{sat} sech^2 w \tag{5.28}$$

Then we can write as:

$$\left(V_{sat} - \frac{2G}{3\alpha_0(n+p)}\right) = V_{sat}(1 - sech^2 w) = V_{sat} tanh^2 w \tag{5.29}$$

$$\frac{dG}{dw} = -3V_{sat}\frac{sinhw}{cosh^3 w}, \qquad w = sech^{-1}\sqrt{\frac{2G}{3\alpha_0(n+p)V_{sat}}} \tag{5.30}$$

By substituting equation 5.28, 5.29, 5.30 and solving equation 5.27, transforming back to G, then moving impact ionization wave front can be given by:

$$G(x,t) = G_0.sech^2\left[\sqrt{\frac{3\alpha_0(n+p)V_{sat}}{2G_0}}(x - V_{sat}t)\right] \tag{5.31}$$

where,

$G_0 = \frac{3\alpha_0(n_0+p_0)}{2}.V_{sat}$=Initial generation rate.

In order to have a real solution the quantity must be a positive number. As it is easily seen from equation 5.29 for $V_{sat} > 0$ the solitary wave moves to the right. The second point is that the amplitude is proportional to the speed which is indicated by the value of V_{sat}. Thus larger amplitude solitary

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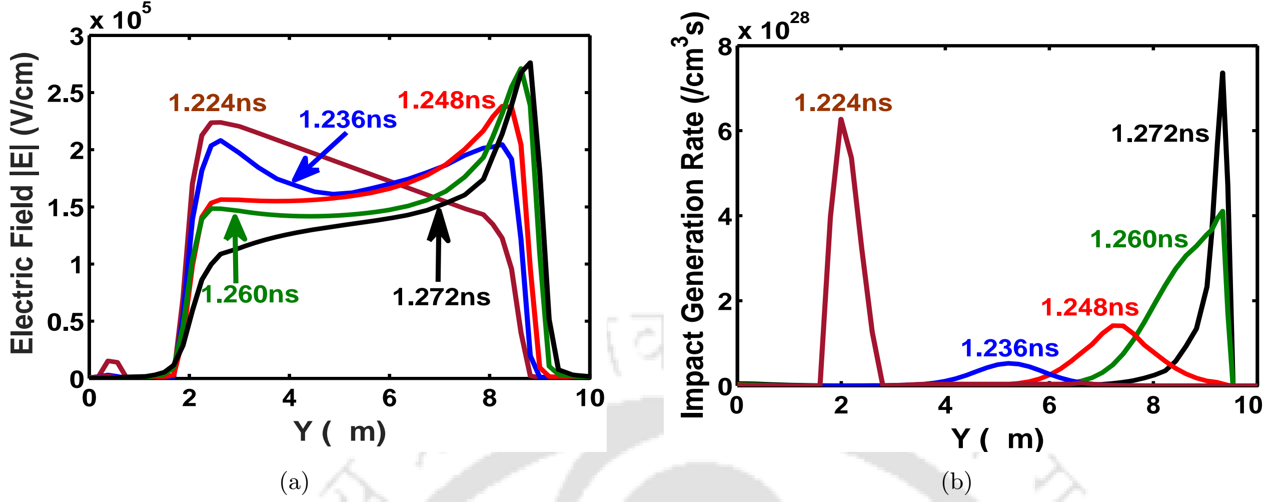

(a)

(b)

Figure 5.8: The profile of (a) electric field and (b) self-reinforced ionization front in the depletion region at different time instances, wave front is triggered and sustained injection of holes are initiated at time ($t_2 = 1.236ns$) (condition derived in equation 5.10). The electric field increases and ionization front also sharpens at times *1.248ns, 1.260ns and 1.272ns* as it moves towards the n^-/n^+ junction. At time ($t_3 = 1.272ns$), front movement is restricted across the n^-/n^+ region, which leads to strong sustained injection of holes in the base region.

waves move with a higher speed than smaller amplitude waves. The resulting ionization front and its propagation are shown in Figure 5.7, which is given at different time instances.

5.3.4 Physics of moving ionization front

The self-reinforced ionization front moves like a soliton, resulting from the accumulation of electrons at the n^-/n^+ junction, and similarly, holes accumulating at the diode, (i.e., the p/n^-) junction at an ultra-fast voltage ramp of $250V/1ns$ under low V_{sat} conditions. The amplitude of the traveling ionization front is partially determined by coupling of mobile carriers and electric field at the junctions, which can also be related to the accumulation of space charge during the movement of the ionization front. The ionization front of mobile carriers is sharpened as the front progress towards the n^-/n^+ junction, which is caused by electron accumulation creating a net space charge of $1 \times 10^{15} cm^{-3}$ (when the wave-front reaches, $y = 8.3\mu m$). We have also observed the profile of the impact ionization front, where growth in the front is exponential and is maximum when the electric field increases to its maximum value. Please refer to Figures 5.8 (a) and (b), where we see the distributions of the electric field and impact ionization front at five-time instances which are shown in colored representation in both the figures. At time $t_2 = 1.236ns$, the self-reinforced ionization front is triggered under low V_{sat} conditions within the depletion region and sustained injection of holes is initiated from the n^-/n^+

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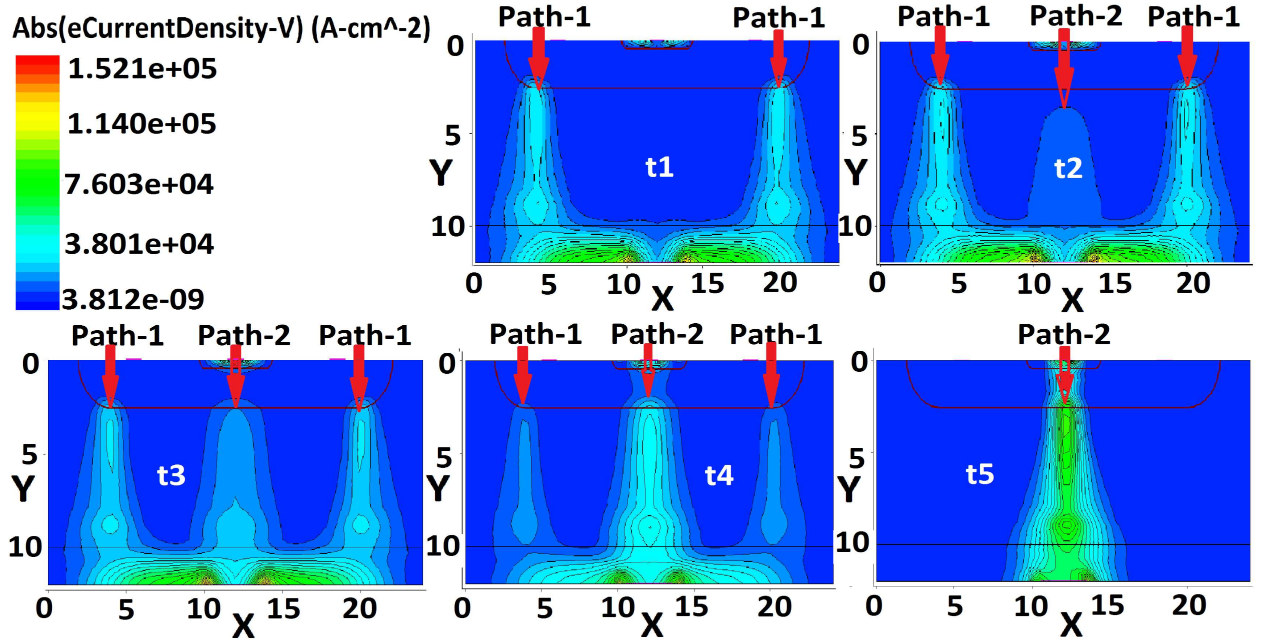

Figure 5.9: Cross-Section of e-Current Density (A/cm^2) profile where filaments are formed across the junctions, when ultra-fast voltage ramp of (*250V in 1ns*) is applied across the reverse biased base-collector junctions. Filaments dynamically appear at $t_1 = 1.224ns$ at diode junction, and becomes stronger as the time progresses but it start to take different path at t_2 and then filament completely shifted from path-1 to path-2 at $t_3 = 1.272ns$.

junction (with ref. to Figure 5.3 (b)). However, the amplitude of the wave-front is small and also the electric field is minimum within the depletion region in the space domain. Further, the electric field increases with time at the n^-/n^+ junction and its decrease within the depletion region and similarly the wave-front of mobile carriers sharpens (amplitude increases) as the front progress towards the n^-/n^+ junction at times *1.248ns, 1.260ns and 1.272ns*. When the wave front reaches the n^-/n^+ junction at $t_3 = 1.272ns$, the front movement is restricted across the n^-/n^+ region, which leads to regenerative and strong sustainable back injection of holes in the base region, thus snapback mode is observed. However, the hole build-up at the diode junction is not formed at low V_{sat} condition (see Figure 5.4 (b)). Whereas, hole build-up are seen at the p/n^- junction by accumulated holes but electron build-up is not observed at the n^-/n^+ junction at high V_{sat} condition, as shown in Figure 5.4 (a). However, under high V_{sat} condition (discussed earlier), the wave front is not observed, which causes weak sustainable back avalanche injection of holes in the base region, thus snapback mode is not observed.

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5.4 Filament Formation at the Junctions

Avalanche injection mechanisms in device lead to current constriction phenomenon as a result the positive feedback mechanisms is triggered at the n^-/n^+ junction (discussed in the last section). The transient current growth in the external circuit and the modulation of the electric field under the influence of the drifting mobile charges due to triggering of the self-reinforced ionization front can be intricately related to physics of filamentation during the avalanche injection phenomenon. The breakdown field across the depleted junction continues to rise until the nonlinear discrete event is triggered, which is also consistent with the experimentally observed phenomenon, wherein the depleted junction can withstand much higher breakdown field for ultra-fast voltage ramps.

Figure 5.9 shows the e-current density (hyperbolic profile is shown so that filaments can be seen clearly) in the bipolar transistor whose base-emitter is externally shorted and ultra-fast voltage ramp of $250V/1ns$ is applied by forcing a current input at the reverse biased base-collector terminal. As the voltage across the device is ramped at low V_{sat} condition, at t_1 "*current channel*" start to build in the structure, as the p/n^- junction reaches the breakdown electric field and triggers the diode action in the structure, shown by path-1. At t_2, due to a increase in the breakdown electric field and hence generation rate, eventually a filament starts to build-up across path-2 (bipolar action), which is triggered due to formation of the self-reinforced ionization front resulting in the sustained hole injection in the base region, as it travels to the n^-/n^+ junction. Moreover, as the injection of the mobile carrier from the n^-/n^+ junction becomes stronger, the filament starts shifting from path-1 to path-2 (*i.e.*, 1-D coupling of diode breakdown and bipolar turn-on), as shown in Figure 5.9 at t_5. It is observed that, as diode breakdown is triggered in *1ns*, while it took only a few *ps* to turn-on the bipolar structure and the injection of electron from emitter is initiated. This process leads to filamentation and results irreversible damage in the device. Above, simulation results show the physics of coupling through a strong injection of electrons from the emitter and the paths followed by holes injected from the n^-/n^+ junction into the base region of the transistor. The sustained back injection of holes from the n^-/n^+ junction can be strong or weak, which depends on non-deterministic triggering of the moving ionization front. The coupling of both the path is primarily determined by hole injection in the base region from the base-collector junction, which can only be visualized in a 2D device structure, as shown in Figure 5.9. Under low V_{sat} condition, the n^-/n^+ junction should predictably lead to strong hole injection, whereas at high V_{sat} condition the triggering condition of moving ionization front is

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not observed, which leads to weaker hole injection in the base region. The injected holes in the base determine non-deterministic snapback behavior of the device structure, which can be understood by the coupling mechanism of the two paths, as discussed in section-3. It indicates that in addition to two paths there are two independent processes (i.e., injection of holes and injection of electrons), which need to be aligned.

5.5 Conclusion

In this chapter, we have developed an analytical model of the instability due to propagation of the impact ionization wave-front caused due to the accumulation of avalanche-generated mobile carriers, which has been analyzed through 2D numerical simulation. This developed model has shown deeper insight towards understanding the instability which occurs in the bipolar structure when different material properties like saturation velocity V_{sat}, impact-ionization coefficient (α), have been varied. Through the device model, it has been shown that the ultra-fast voltage pulse causes the mobile carrier to get accumulated under low V_{sat} condition, which causes an ionizing front to travel across the depletion region which moves towards the n^-/n^+ junction. Furthermore, we have derived the condition for the triggering of self-reinforced ionization front and modeled the dynamic behavior of propagating ionization front as it travels towards the n^-/n^+ junction. The faster ramps cause prominent accumulation of avalanche generated carrier at low V_{sat} condition, which can then travel to the n^+/n^- junction to trigger a prominent snapback phenomenon due to regenerative avalanche injection at the junctions. Finally, the process of filamentation has been associated with an ultra short time scale event when self-reinforced ionization front is triggered in the depletion region at low V_{sat} condition.

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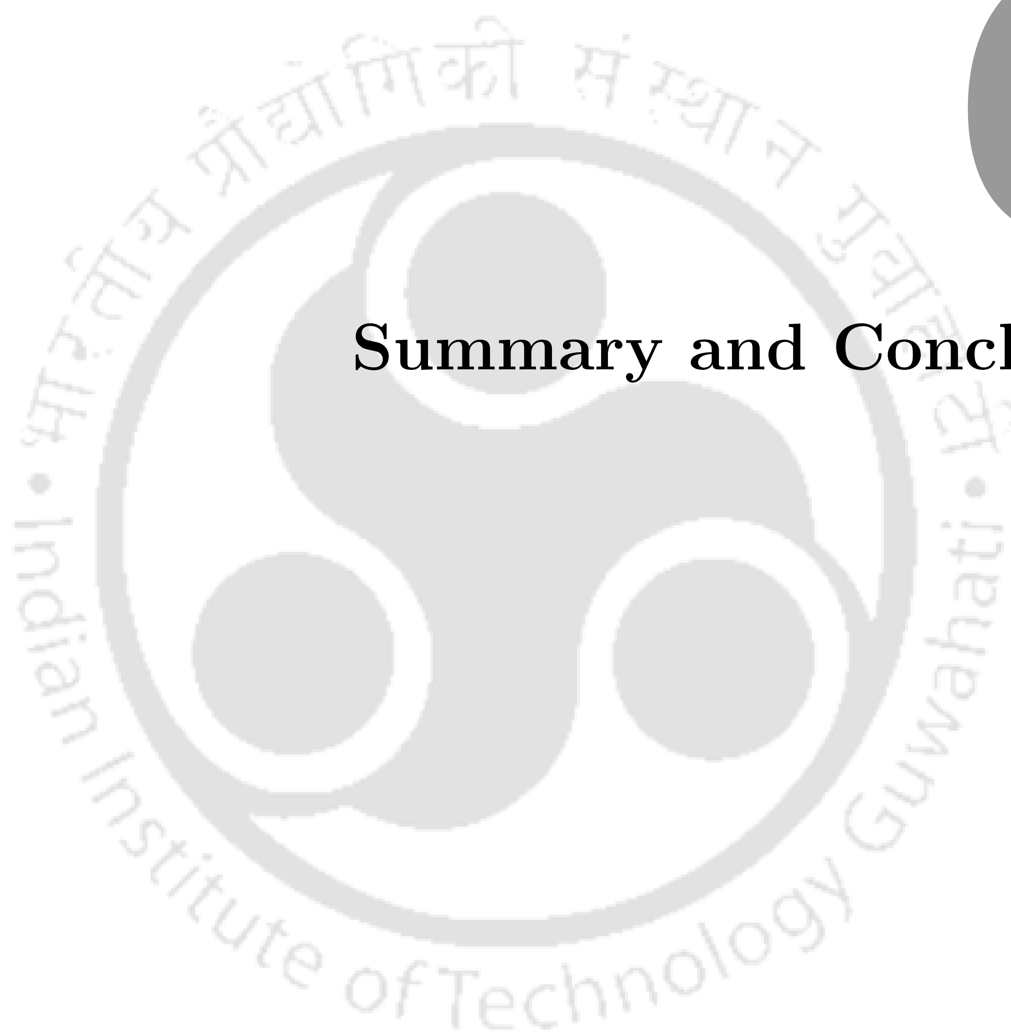
6 Summary and Conclusions



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6.1 Summary

This thesis has proposed the new physical insight towards understanding high current injection behavior of semiconductor bipolar structure when operated at different conditions. Ultra high current injection mechanism problems have shown great attention in the semiconductor manufacturing industry, therefore it has become area of interest as the size of the channel of MOS devices has been scaled towards nanometer regimes. In absence of high current breakdown models in the literature, this proposed thesis has provided some physical insights into layered semiconductor bipolar structures that are present as parasitic elements in high voltage as well as high power devices. A phenomenological approach has been presented to understand anomalous or non-deterministic switching behavior of bipolar transistor without going much deep in theory and an attempt has been made to connect dynamic avalanche model with the Kirk effect for the first time at high current densities.

In this thesis work, we have developed physics based TCAD modeling to comprehend the anomalous and non-deterministic switching behavior of different configurations of bipolar transistor such as: base drive, base-emitter shorted, base open and emitter open. We have first modeled the anomalous switching behavior of avalanche bipolar transistors under base-triggering conditions. Fast-switching experiments have been performed on various bipolar transistors from different manufacturers under the same conditions and also verified our results through numerical simulations. The nonlinear phenomena involving triggering and propagation of moving impact ionization wave front due to accumulation of avalanche-generated mobile carriers has been analyzed through TCAD device simulation. The triggering of the moving ionization front phenomenon leads to CMSB mode, as it travels towards the n^-/n^+ junction. A very good agreement has been observed between measurement and 2D TCAD device simulation results when the base width and carrier recombination rate are used as parameters in the simulation setup.

Furthermore, in another experimental split, ultra-fast variable high voltage pulses were applied to the collector terminal of base-emitter externally shorted configuration of bipolar transistor under high current injection conditions. Experimental results pertaining to different regimes of ramp speed has been modeled and 2D TCAD device simulation has been performed to explain the non-deterministic snapback behavior of the bipolar structure. We further explore, the role of emitter injection to understand indeterminacy associated with the snapback mechanisms, where in the state of breakdown is determined through several competing processes and linked to dynamical system. The phenomenon

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has been extensively studied to investigate two basic processes in multiple path leading to bipolar coupling mechanism as the bipolar structure turns-on.

Finally, we have developed a simple analytical model of the instability due to triggering of the moving ionization front in base-emitter shorted configuration of bipolar transistor with different material properties like saturation velocity V_{sat} and impact ionization coefficient (α), when an ultra-fast variable high voltage ramp pulse is applied across the reverse biased base-collector junction. The avalanche injection mechanisms with different velocity saturation and variable ionization coefficient are studied through formation of ionization front, that leads to either weak or strong injection of mobile carriers, as the high current injection paths get coupled. The role of distribution of mobile carriers has been discussed and phenomenology of triggering of the moving ionization front and its propagation have been revisited and analytically modeled. Furthermore, build-up of the electric field across the n^-/n^+ junction due to triggering of the moving ionization-front and role of emitter injection are clearly addressed, which dictates the the process of filamentation at the n^-/n^+ junction.

6.2 Contributions

The major contributions of the research work reported in this thesis includes,

- The physics-based TCAD modeling has been developed to comprehend the anomalous or non-deterministic switching mechanisms in bipolar transistor under high current injection conditions.
- Experimental observations and analysis related to ultra-fast anomalous switching behavior of the bipolar transistor for voltage pulse (base drive) having variable rise time is investigated.
- This work models the instability, that occurs during filament formation in a bipolar transistor whose base-emitter is externally shorted, when subjected to an ultra-fast high voltage pulse across reverse biased base-collector junction.
- Role of dynamic avalanche model and reverse saturation current on the anomalous switching mechanism, under high speed base-trigger ramps for different commercial BJTs have been discussed.
- The avalanche injection mechanisms under variable high speed ramps has been studied through formation and propagation of ionizing waves, that leads to either weak or strong injection of mobile carriers, as the high current injection paths get coupled.

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- This thesis work conceptualizes the turn-on mechanism of parasitic bipolar and bipolar coupling in 2D device structure, which is triggered by a propagating ionization front in a depleted field. Moreover, the electrostatic coupling of holes and electrons under high current injection and sustained injection of mobile carriers turn-on the device structure, which is corroborated by experiments and models.

- We have developed a simple analytical model of the instability due to triggering of self-reinforced ionization front in a generic $n/p/n^{-}/n^{+}$ bipolar structure whose base-emitter is externally shorted, when subjected to an ultra-fast high current pulse.

- This developed model allows to understand the instability in the semiconductor device structure with different material properties like saturation velocity V_{sat}, impact-ionization coefficient (α).

- The jittery nature related to trigger delay (Δt) and avalanche build-up voltage (ΔV) have been associated with the excess voltage required to trigger the plasma of mobile carriers in the depletion region and triggering of moving ionization front.

- Nuances leading to turn on mechanism of the bipolar structure and its eventual coupling and the rate dependence of the hole accumulation and its recombination dependent transport has been described.

- High current phenomenon like dynamic avalanche and base push out-effect is clearly linked in this work to elucidate the novelty of models established.

- This work addresses several areas of other high current breakdown mechanisms rather than focusing on novel device structures.

6.3 Directions for future work

Based on the outcome of this thesis work, this section provides some of the possible future directions for research.

(i) The knowledge of the high current injection mechanisms during dynamic avalanche breakdown model, ultra-fast switching mechanisms and ESD event are also essential to predict and understand the insight behavior of more complex device structures.

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(ii) The reliability physics of high current phenomenon in commercially critical and emerging power devices integrated into state of art VLSI devices is intricately related to transient mechanisms of high current pulses across a parasitic $n/p/n^-/n^+$ structures.

(iii) The analysis presented in this work will be critical for modeling the high current phenomenon in state of art high voltage as well as low voltage devices. Its worth mentioning that snapback physics plays an important role in ESD protection devices and overall reliability of high current devices and several other areas.

(iv) We believe that, the novel dynamic avalanche injection from the contact builds foundation of bipolar turn-on and it can be related to basic understanding of filamentation mechanism. The physics of injection is not purely related to injection from base (as required for base push out effect) but related to triggering dynamics of avalanche and strong reverse injection of holes.

(v) The knowledge of the high current injection phenomenon taking place during an ESD event in single protection devices is fundamental to understand and predict the behavior of more complex protection ESD protection devices.

(vi) A qualitative analyses and numerical simulation results presented in this thesis work including internal dynamics and transient behavior of trigger transistor under base-drive condition will be critical for optimal design of ultra-fast switches and modeling high current phenomenon in high voltage devices.

(vii) A complete analysis of all stages of Marx-bank circuits (MBCs) can be done through numerical device simulation to describe the operation of transistorized MBCs for development of ultra-fast generation of high voltage pulses.

(viii) The development of high current breakdown models based on the theory presented in this work can be implemented in the form of circuit level simulators to provide reliable simulation results prior to silicon manufacturing.

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List of Publications

Journal Publications

- Published Papers:

  1. **Dheeraj Kumar Sinha**, Amitabh Chatterjee and Ronald D. Schrimpf, *"Modeling Erratic Behavior Due to High Current Filamentation in Bipolar Structures under Dynamic Avalanche Conditions"*, **IEEE Transactions on Electron Devices**, Vol. 63, pp. 3185-3192, 2016, DOI:10.1109/TED.2016.2584102.

- Manuscripts under review

  1. **Dheeraj Kumar Sinha**, M. S. Ansari, Ashok Ray, Gaurav Trivedi, Amitabh Chatterjee and Ronald D. Schrimpf, *"Fast Ionization-front Induced Anomalous Switching Behavior in Trigger Bipolar Transistors of Marx-bank Circuits Under Base-drive Conditions"*, **IEEE Transactions on Plasma Science**, under review.
  2. **Dheeraj Kumar Sinha**, M. S. Ansari, Ashok Ray, Gaurav Trivedi and Amitabh Chatterjee, *"Anomalous Switching Behavior and Selection of Trigger Transistor - A New Perspective for Marx-bank Circuit Design"*, **Review of Scientific Instruments**, under major revision.

Conference and Workshop Publications

1. **Dheeraj Kumar Sinha**, Amitabh Chatterjee and Gaurav Trivedi, *"Two Dimensional Numerical Simulator for Modeling NDC Region in SNDC Devices"*, **Journal of Physics Conference Series**, vol. 759(1), pp. 012099, 2016, DOI:10.1088/1742-6596/759/1/012099.

2. **Dheeraj Kumar Sinha**, Vishnuram Abhinav, Amitabh Chatterjee and Forrest Brewer, *"A Novel Capacitorless DRAM Cell Design Using Band-Gap Engineered Junctionless Double-Gate FET"*, 29th IEEE International Conference on VLSI Design, pp. 312-317, Kolkata, 2016.

3. Vishnuram Abhinav, **Dheeraj Kumar Sinha**, Amitabh Chatterjee and Forrest Brewer, *"A Novel Co-design Methodology for optimizing ESD Protection Device Using Layout Level Approach"*, 29th IEEE International Conference on VLSI Design, pp. 282-287, Kolkata, 2016.

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4. **Dheeraj Kumar Sinha**, Amitabh Chatterjee and Forrest Brewer, *"Design of Band-gap Engineered Silicon-Germanium Junctionless Double-gate FET for ZRAM application"*, 6th International Conference on Computers and Devices for Communication, Kolkata, 2015.

5. **Dheeraj Kumar Sinha**, Amitabh Chatterjee, Gaurav Trivedi and Victor Koldyaev, *"Analysis and Design of ZRAM Cell for Low Voltage Operations"*, 18th International Workshop on Physics of Semiconductor Devices, Bangalore, 2015.

6. Vishnuram Abhinav, Amitabh Chatterjee, **Dheeraj Kumar Sinha**, and Rajan Singh, *"Methodology for optimizing ESD protection for high speed LVDS based I/Os"*, 19th International Symposium on VLSI Design and Test (VDAT), pp. 1-5, Ahmedabad, 2015.

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