DESIGN AND IMPLEMENTATION OF NEW EXTENDED-BOOST QUASI Z-SOURCE INVERTERS FOR HIGH-BOOST DC-AC POWER CONVERSION

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by

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To my loving parents

For their life lessons

Certificate

This is to certify that the thesis entitled **"Design and Implementation of New Extended-Boost Quasi Z-Source Inverters for High-Boost DC-AC Power Conversion"**, submitted by **Abhishek Paikray** (146102020), a research scholar in the Department of Electronics and Electrical Engineering, Indian Institute of Technology Guwahati, for the award of the degree of Doctor of Philosophy, has been carried out by him under my supervision and guidance. The thesis has fulfilled all requirements as per the regulations of the institute and in my opinion has reached the standard needed for submission. The results embodied in this thesis have not been submitted to any other university or institute for the award of any degree or diploma.

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Abstract

Power electronics has undergone rapid growth in recent years, and this growth has increased the demand for inverter systems that are flexible, efficient, and compact. Many applications now require inverters that can operate across wide voltage ranges while maintaining superior performance and reliability. Traditional voltage-source and current-source inverters have inherent limitations, including an inability to boost voltage and poor immunity to electromagnetic interference (EMI) and shoot-through faults. To address these challenges, impedance source inverters (ISIs) have been introduced as a viable alternative. ISIs place an impedance network between the power source and the inverter bridge. This network enables the inverter to both buck and boost voltage in a single stage, thereby improving overall system efficiency. The first and most well-known ISI is the Z-Source Inverter (ZSI). Its impedance network usually consists of two inductors placed in series with the DC source and two capacitors connected between the inverter legs in an X-shaped pattern. A unidirectional diode is also placed between the DC source and the impedance network to ensure proper current flow and protect the circuit.

The ZSI features a diode at its input to block reverse current and prevent shoot-through states in the inverter. While this diode is essential for the proper operation of the ZSI, it also causes the input current to become discontinuous. During shoot-through intervals, the diode blocks the source, and the input current falls to zero. Such discontinuous current is not suitable for photovoltaic (PV) panels and fuel cells, as these sources operate most efficiently under a continuous current profile. Discontinuous current can introduce voltage ripple, reduce energy-harvesting efficiency, and, in some cases, cause long-term degradation of the source. As a result, the traditional ZSI is not an ideal choice for PV and fuel cell systems unless additional circuitry is introduced to smooth the input current.

The quasi-Z-source inverter (qZSI) with an asymmetrical impedance network addresses the need for continuous input current, a key requirement for renewable sources such as photovoltaic (PV) arrays and fuel cells. However, its voltage boost potential remained inherently limited due to its single-stage LC network. Further developments in ISIs include

cascaded, embedded, and extended impedance-network topologies. The trans-ZSI introduced transformer coupling to achieve higher boost factors and galvanic isolation. At the same time, switched-inductor and switched-capacitor ZSIs utilized momentary energy storage and transfer paths to extend boost capability without increasing shoot-through duty cycle.

Subsequent innovations led to the switched-inductor and switched-capacitor ZSIs, which employed resonant and non-resonant configurations of additional passive elements and diodes to momentarily store and transfer energy, thereby significantly increasing the boost factor without increasing the shoot-through duty cycle. While effective in voltage boosting, these topologies sometimes suffer from increased complexity and transient response issues. The enhanced boost-qZSI and its improved variants have gained considerable attention in the pursuit of an optimal trade-off between a high boost factor and system simplicity. These designs reshape the impedance network by adding extra inductors and capacitors, which may be coupled or non-coupled. This layout enables the circuit to utilize the shoot-through period more effectively, thereby enhancing the voltage gain.

Over the past two decades, several ISI topologies have been introduced, each aimed at improving the boost factor, reducing the size of passive components, enhancing power density, and minimizing total harmonic distortion (THD). Despite significant progress, achieving a consistently high voltage gain with reduced passive elements and minimal stress on switching devices remains a primary challenge.

The primary objective of this research is to design, analyze, and validate novel ISI topologies that achieve significantly higher voltage gain while operating with a reduced shoot-through duty ratio, thereby improving modulation capability and reducing stress on switching devices. To this end, the thesis proposes three innovative inverter configurations: the Diode-Assisted Switched-Inductor Extended-Boost Quasi Z-Source Inverter, the Capacitor-Assisted Switched-Inductor Extended-Boost Quasi Z-Source Inverter, and the Improved Extended-Boost Quasi Z-Source Inverter (Improved-EBqZSI).

The research methodology encompasses a comprehensive operational analysis of these proposed topologies under shoot-through and non-shoot-through states. Mathematical mod-

eling is carried out to derive expressions for the boost factor, capacitor voltages, inductor currents, and device stresses. The impedance networks are designed using linearized small-ripple approximations, and the network parameters are calculated by solving the simultaneous equations that emerge from steady-state operation. The theoretical results are checked through detailed PSCAD simulations and confirmed using laboratory-built prototypes. The tests show that the proposed inverters reach much higher voltage boost than existing qZSI and enhanced-boost ZSI designs, even while using lower shoot-through duty cycles.

The thesis also includes an illustrated design approach of the impedance network of the qZSI. The operation of the qZSI in shoot-through, non-shoot-through, and active states is discussed. The thesis also explains three static states that can appear in the circuit. The impedance network must be appropriately designed to prevent these states from occurring. The ripple is considered small for the linear approximation of capacitor voltages and inductor currents. The values of impedance network inductors and capacitors are obtained by solving the simultaneous equations derived in the design analysis. The design parameters are verified with simulation and experiments.

In conclusion, this thesis presents three high-performance ISI topologies that effectively address long-standing challenges related to voltage boosting, device stress, and network design complexity. The proposed inverters offer a practical and efficient solution for integrating renewable energy, electric drives, and other power-electronic applications that require high voltage gain and robust operation. The analytical, simulation, and experimental validations collectively establish the superiority and applicability of these novel topologies in modern power-electronic systems.

List of Acronyms

AC	Alternating Current
CA-EBqZSI	Capacitor-Assisted Extended-Boost Quasi Z-Source Inverter
CA-SLEBqZSI	Capacitor-Assisted Switched- Inductor Extended-Boost qZSI
CBC	Constant Boost Control
DA-EBqZSI	Diode-Assisted Extended-Boost Quasi Z-Source Inverter
DA-SLEBqZSI	Diode-Assisted Switched- Inductor Extended-Boost qZSI
DC	Direct Current
DG	Distributed Generation
EMI	Electromagnetic Interference
EV	Electric Vehicle
HESS	Hybrid Energy Storage System
IGBT	Insulated Gate Bipolar Transistor
Imp-EBqZSI	Improved Extended-Boost Quasi Z-Source Inverter
ISIs	Impedance Source Inverters
LCCT	Inductor-Capacitor-Capacitor-Transformer
MBC	Maximum Boost Control
MOSFET	Metal–Oxide Semiconductor Field-Effect Transistor
MPC	Model Predictive Control
MPPT	Maximum Power Point Tracking

PCB	Printed Circuit Board
PSCAD	Power Systems Computer Aided Design
PSMS	Permanent Magnet Synchronous Motor
PV	Photovoltaic
PWM	Pulse Width Modulation
qSBI	Quasi Switched-Boost Inverter
qZSI	Quasi Z-Source Inverter
RES	Renewable Energy Source
SBC	Simple Boost Control
SBI	Switched-Boost Inverter
SL-qZSI	Switched-Inductor Quasi Z-Source Inverter
SL-ZSI	Switched-Inductor Z-Source Inverter
SPWM	Sinusoidal Pulse Width Modulation
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
Trans-ZSI	Trans-Z-Source Inverter
UPS	Uninterruptible Power Supply
VSI	Voltage Source Inverter
ZSI	Z-Source Inverter

List of Symbols

B	Boost factor.
C_{1-5}	Impedance network capacitors.
C_f	Filter capacitor.
D	Shoot-through duty ratio.
D_{1-7}	Impedance network diodes.
f	Fundamental frequency of $\widehat{v}_m$ and $\widehat{i}_m$.
f_o	Operating frequency.
f_s	Switching frequency.
G	AC gain of the inverter.
I_0	DC current drawn by the load.
$I_{C_{1-5}}$	Average current through capacitors.
I_{in}	DC current drwan from the source.
$i_{L_{1-5}}$	Instantaneous current through inductors.
$I_{L_{1-5}}$	Average current through inductors.
$\widehat{i}_m$	Peak phase AC current through load.
I_{PN}	DC-link current.
k_i	Ripple factor of inductor current.
k_v	Ripple factor of capacitor voltage.
L_{1-5}	Impedance network inductors.

L_f	Filter inductor.
M	Modulation index.
R	Load Resistor.
S_{1-6}	Switches of the three-phase inverter.
t_A	Active state duration.
t_S	Shoot-through state duration.
T	Time duration of a switching cycle.
$v_{C_{1-5}}$	Instantaneous voltage across capacitors.
$V_{C_{1-5}}$	Average voltage across capacitors.
V_{in}	Input voltage.
$V_{L_{1-5}}$	Average voltage across inductors.
$\widehat{v}_m$	Peak phase AC voltage across load.
V_{PN}	DC-link voltage.
$\Delta i_{L_{1-5}}$	Ripple of inductor curretnts.
$\Delta V_{C_{1-5}}$	Ripple of capacitor voltages.
ϕ	Phase angle between the voltage and current.

CHAPTER 1

Introduction

1.1 Introduction

Three-phase inverters are fundamental components in modern power electronics systems. Their role is critical in converting direct current (DC) into three-phase alternating current (AC) [1, 2], essential for various industrial, commercial, and residential applications. These inverters are typically built using six power switches (e.g., IGBTs or MOSFETs) arranged in a bridge configuration, as shown in the figure. The output is generally in the form of pulse-width modulated (PWM) signals that approximate sinusoidal waveforms [3]. One of the most significant applications of three-phase inverters is integrating renewable energy sources (RES), such as solar photovoltaic (PV) and wind power, into the electrical grid [4]. In grid-tied PV systems, inverters convert the DC power generated by solar panels into AC power suitable for grid usage. Three-phase inverters are preferred in large-scale installations due to their ability to handle high power levels and provide a balanced three-phase output, which enhances grid stability.

Three-phase inverters are widely used in motor drive applications, particularly for controlling three-phase induction motors, synchronous motors, and permanent magnet synchronous motors (PMSMs) [5]. In industrial automation and robotics, variable frequency drives (VFDs) use three-phase inverters to adjust the frequency and amplitude of the output voltage, thereby controlling motor speed and torque.

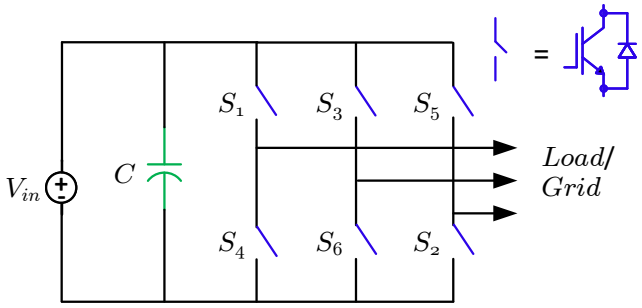


Fig. 1.1. Voltage source inverter (VSI) [1].

In electric vehicles, three-phase inverters are employed to drive the traction motors [6]. The onboard inverter converts the DC voltage from the battery into three-phase AC to power the vehicle's motor. Modern EVs often use PMSMs due to their high efficiency and power density. The inverter also plays a critical role in regenerative braking, acting as a rectifier and converting excess kinetic energy into electrical energy to recharge the battery .

Three-phase inverters are integral to uninterruptible power supply (UPS) systems [7], which provide backup power during grid outages. Three-phase UPS systems ensure continuous and high-quality power delivery in data centers, hospitals, and other critical infrastructure. The inverter section of a UPS converts stored DC energy from batteries into stable AC power.

With the advent of smart grids and microgrids, the role of three-phase inverters have expanded significantly. These inverters enable bidirectional power flow, facilitating grid-support functionalities such as reactive power compensation, voltage regulation, and harmonic compensation. In distributed generation systems, inverters ensure that power from local generation sources (like rooftop solar) can be efficiently synchronized and integrated into the grid. Advanced grid-forming and grid-following inverters also support microgrid operation in both grid-connected and islanded modes [8].

In a conventional voltage source inverter (VSI), the upper and lower switches of each phase leg must never be turned on simultaneously, whether intentionally or due to electromagnetic interference (EMI). If this occurs, it causes a short circuit across the inverter leg, a condition known as shoot-through, which can severely damage the switches. Shoot-through events are typically caused by unintended switching due to EMI noise and are a significant threat to the reliability and lifespan of the VSI [11]. To mitigate shoot-through, a dead-time, a short delay is introduced between the switching of the upper and lower devices in each phase leg. While this helps prevent simultaneous conduction, implementing dead time adds complexity to the control circuitry and can lead to waveform distortion and other operational challenges [12, 13].

Another inherent limitation of the VSI is that its peak AC output voltage cannot exceed the input DC-link voltage. This becomes problematic in renewable energy applications such

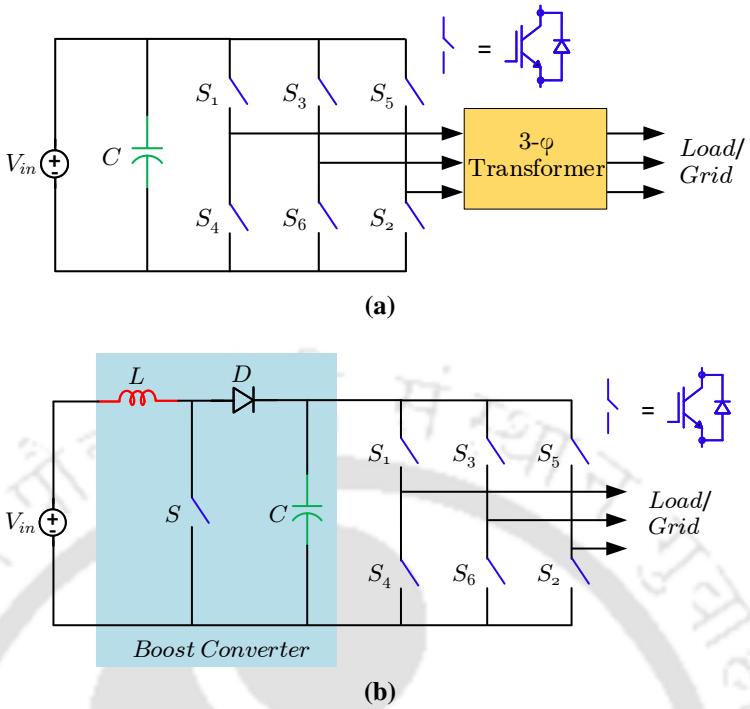


Fig. 1.2. Examples of two-stage system: (a) the combination of a VSI and a step-up transformer; (b) the combination of a boost converter and a VSI [9, 10].

as solar or wind where the input DC voltage is often relatively low. To overcome this, either a step-up transformer is added at the inverter output, or a boost converter is used at the input to raise the voltage level [9] as shown in Fig. 1.2. However, both approaches introduce drawbacks.

(a) Step-up transformers require a high turns ratio to achieve significant voltage gain, which makes them bulky, noisy, and costly. Their size and magnetic losses also reduce the overall system efficiency [10].

(b) Also, the DC-DC boost converters provide an alternative as shown in Fig. 1.2. (b), but achieving high voltage gain requires operating at a duty ratio "D" close to unity. This results in very short conduction times for the diode and output capacitor while still handling high currents [14]. Such narrow pulse widths intensify the reverse-recovery problem of the diode, increasing conduction losses and generating EMI. The issue becomes more severe at high switching frequencies. Moreover, traditional boost

converters are typically limited to a voltage gain of 4 to 5 times, making them unsuitable for high-gain applications [15].

1.2 Overview of impedance-source inverter topologies

Impedance-source inverters (ISIs) are a class of power inverters that use an impedance network to convert DC to AC, offering advantages like voltage buck-boost capability, improved reliability, and elimination of dead time. When classifying ISI topologies based on the presence or absence of transformers/coupled-inductors, we can divide them into two main categories. The summary of different ISI topologies is listed in the Table 1.1.

(a) **Non-transformer-based ISI topologies** These topologies rely purely on passive and active elements (inductors, capacitors, diodes, and switches) without any magnetic coupling. They are typically simpler, cheaper, compact, and non-isolated, with moderate voltage gain.

(b) **Transformer-based ISI topologies** These topologies incorporate magnetic coupling via a transformer or coupled inductors along with inductors, capacitors, diodes, and switches to achieve higher voltage gain, galvanic isolation. These are often used in high-gain or isolated applications.

Table 1.1. Summary of different ISI topologies [16, 17]

Topology Type	Galvanic Isolation	Voltage Gain	Complexity	Example Topologies
Non-transformer-based	No	Medium–High	Lower	ZSI, qZSI etc
Transformer-based	Yes (usually)	High	Higher	Trans-ZSI

The following section presents a detailed discussion of the first ISI proposed by Fang Zheng Peng [18]. This original Z-source inverter (ZSI) introduced the concept of an impedance network that enables controlled shoot-through operation, forming the fundamental basis for all subsequent ISI topologies. An in-depth understanding of this pioneering configuration is crucial for appreciating the evolution and enhancement of ISIs addressed in the later chapters of this thesis.

1.3 Z-source inverter

The ZSI was first proposed in 2002 by Fang Zheng Peng as shown in Fig. 1.3, marking a significant advancement in inverter technology. The key idea behind the ZSI was to intentionally utilize the shoot-through state of an inverter bridge, which had traditionally been considered a destructive fault condition. By inserting a properly designed impedance network between the DC source and the inverter bridge, the shoot-through state could be safely exploited to boost the DC-link voltage. This invention eliminated the need for an additional DC–DC boost converter, thereby reducing system complexity, component count, and conversion losses.

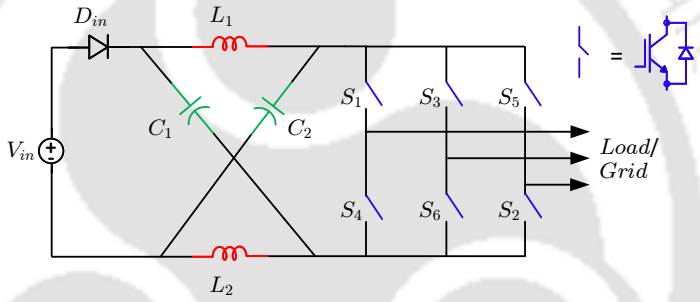


Fig. 1.3. Z-source inverter (ZSI) [18].

The classcical ZSI topology consists of three main sections:

(a) **DC input source:** The input source may be a battery, photovoltaic array, fuel cell, or rectified AC supply.

(b) **Impedance network (Z-network):** The impedance network is composed of two inductors, two capacitors and one diode. These components are arranged in a symmetrical X-shaped configuration. The inductors are connected in series with the DC source, while the capacitors are cross-connected between the inductors and the inverter bridge.

(c) **Inverter bridge:** A conventional three-phase inverter bridge comprising six power semiconductor switches (IGBTs or MOSFETs) with antiparallel diodes. The Z-network acts as an energy storage and transfer stage, enabling voltage boost without requiring an isolated transformer or additional active switches.

1.3.1 Operating principle of the ZSI

The operation of the ZSI can be clearly understood by examining two distinct modes that occur within each switching cycle: the non-shoot-through (NST) state and the shoot-through (ST) state as shown in Fig. 1.4 and Fig. 1.5 respectively. These two modes work together to enable the unique buck–boost capability of the ZSI without requiring an additional DC–DC converter.

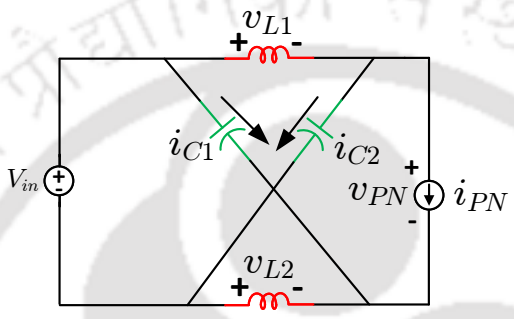


Fig. 1.4. Equivalent circuit of ZSI in non-shoot-through state [18].

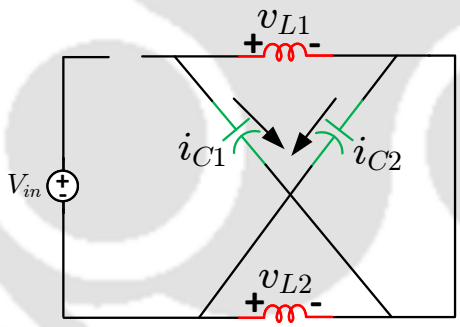


Fig. 1.5. Equivalent circuit of ZSI in shoot-through state [18].

A) ***Non-shoot-through state***

During the non-shoot-through state, the inverter operates similarly to a conventional VSI, where the inverter bridge generates the required active and zero voltage vectors based on the selected PWM strategy. In this mode, the DC source delivers power to the load through the impedance network, while the inductors release their stored energy to support the inverter bridge. Simultaneously, the capacitors maintain the DC-link voltage at a stable and elevated level, ensuring effective and continuous power transfer from the DC source to the AC load under normal operating conditions.

B) ***Shoot-through state***

The shoot-through state is the defining operating mode of the ZSI, in which both switches of one or more inverter legs are intentionally turned ON simultaneously, resulting in a controlled short-circuit of the inverter bridge while the DC source is isolated by the impedance network. During this interval, the capacitors discharge their stored energy into the inductors, causing the inductor currents to rise and magnetic energy to be accumulated. As a result, the voltage across the impedance network is boosted. By appropriately controlling the duration and placement of the shoot-through intervals within the switching cycle, the ZSI can achieve effective voltage boosting without compromising the safe operation of the inverter switches.

1.3.2 Mathematical analysis

Let the shoot-through duty ratio be denoted by D. Assuming a symmetrical impedance network:

$$L_1 = L_2 = L; \quad C_1 = C_2 = C$$

Applying the volt–second balance principle to the inductors over one switching period:

$$v_L^{(ST)} \cdot D + v_L^{(NST)} \cdot (1 - D) = 0$$

Solving the above equation yields the capacitor voltage:

$$V_C = \frac{V_{in}}{(1 - D)}$$

The effective DC-link voltage applied to the inverter bridge is given by:

$$V_{dc} = 2V_C - V_{in}$$

The voltage boost factor B can therefore be expressed as:

$$B = \frac{1}{(1 - 2D)}$$

The peak phase voltage of the inverter output is:

$$\widehat{v}_m = M \cdot B \cdot \frac{V_{in}}{2}$$

where M is the modulation index. This expression demonstrates that the ZSI inherently supports both buck and boost operation within a single conversion stage.

Pulse Width Modulation (PWM) plays a crucial role in the operation of the ZSI, as it not only controls the output AC voltage and frequency but also governs the shoot-through state. This key feature enables voltage boosting. Unlike conventional VSIs, where shoot-through is strictly avoided, the ZSI intentionally introduces shoot-through intervals through specially designed PWM strategies. The ZSI concept enables the inverter bridge to be safely short-circuited because the impedance network absorbs and redistributes energy during these intervals. Therefore, PWM in ZSI must simultaneously satisfy two objectives:

1. Generation of high-quality AC output voltage
2. Regulation of the shoot-through duty ratio for the voltage boost

Simple boost control (SBC) is the most basic and widely used PWM method for ZSI. In this technique:

1. Shoot-through states are inserted only during the traditional zero states of the inverter.
2. Active states remain unchanged, ensuring sinusoidal output voltage.

The advantage of SBC is its simplicity and ease of implementation using conventional carrier-based PWM.

1.3.3 Advantages of ZSI

1. Single-stage buck–boost operation.
2. Elimination of dead-time issues.
3. Improved reliability against shoot-through faults.
4. Reduced component count compared to two-stage converters.
5. High immunity to EMI.
6. Wide input voltage operating range.

These advantages make the ZSI particularly attractive for renewable energy systems where input voltage varies widely.

1.3.4 Limitations and Challenges

Despite its benefits, the ZSI has some drawbacks:

1. High voltage stress on capacitors.
2. Inrush current during startup.
3. Larger passive component size.
4. Discontinuous input current.
5. Limited boost capability at low shoot-through ratios.

The ZSI has been extensively studied in various applications, including distributed generation [19], electric vehicles [20], fuel-cell converters [21–23], motor drives [24], PV generation [25–28] and UPS [29]. A comparison of ZSI with VSI and CSI is listed in the Table 1.2.

Table 1.2. Comparison with conventional inverters [18]

Feature	VSI	CSI	ZSI
Buck/Boost	Buck only	Boost only	Buck-Boost
Shoot-through tolerance	No	Limited	Yes
DC-DC stage required	Yes	Yes	No
Reliability	Moderate	Moderate	High
Dead-time operation	Yes	Yes	No

1.4 Summary

This chapter introduced the fundamental role of three-phase inverters in modern power electronics, highlighting their widespread applications in renewable energy systems, motor drives, electric vehicles, UPS systems, and smart grids. The limitations of the conventional VSI, including susceptibility to shoot-through faults, the requirement for dead time, and the inability to provide voltage boost beyond the DC-link voltage, were discussed in detail. Conventional solutions employing two-stage configurations with transformers or DC–DC boost converters have been shown to increase system complexity, cost, size, and losses. To overcome these challenges, ISI topologies were introduced, offering single-stage buck–boost operation, improved reliability, and enhanced flexibility. The chapter provided an overview of ISI classifications into non-transformer-based and transformer-based topologies. A detailed discussion of the pioneering ZSI was presented, including its operating principle, mathematical analysis, PWM control, advantages, and limitations.

The inherent limitations of the conventional ZSI, particularly in terms of limited boost capability, component stress, and restricted modulation range, have driven extensive research toward the development of advanced ISI topologies. To address these challenges, several non-transformer-based ISI configurations have been proposed, focusing on improved voltage gain, reduced shoot-through duty ratio, and enhanced utilization of passive components without increasing circuit complexity. In parallel, transformer-based ISI topologies have been introduced to achieve higher boost factors and galvanic isolation through magnetic coupling. A comprehensive review of both non-transformer-based and transformer-based ISI topologies is therefore presented in the next chapter, highlighting their advantages, and limitations.

CHAPTER 2

Literature Review

2.1 Introduction

The ISIs represent a distinct class of power inverters that utilize an impedance network between the DC source and the inverter bridge to enable DC–AC power conversion. Unlike conventional voltage-source and current-source inverters, ISIs inherently provide both voltage buck and boost capabilities within a single power conversion stage. This feature eliminates the need for additional DC–DC converters and dead-time insertion, thereby improving system reliability, reducing component count, and enhancing overall efficiency.

Over the past few decades, ISI topologies have undergone significant development to address limitations such as limited voltage gain, high component stress, and control complexity. As a result, numerous ISI configurations have been proposed, each differing in the arrangement and type of impedance network components. Consequently, a systematic classification of ISI topologies is essential to understand their operating principles, performance characteristics, and suitability for applications. One widely adopted approach for classification is based on the presence or absence of transformers or coupled inductors within the impedance network. Based on this criterion, ISI topologies can be broadly categorized into non-transformer-based ISIs and transformer-based ISIs. The former typically offer simpler structures and lower cost, while the latter provide higher voltage gain, galvanic isolation, and improved flexibility in voltage regulation. A detailed study of the ISI topologies available in the literature is discussed in the following section.

2.2 Non-transformer-based ISI topologies

Since its inception, Z-source inverter (ZSI) [18] has gained popularity for single-stage power conversion. It has an impedance network, typically consisting of two inductors in series with the DC source and two capacitors between the inverter legs connected in an X-shaped

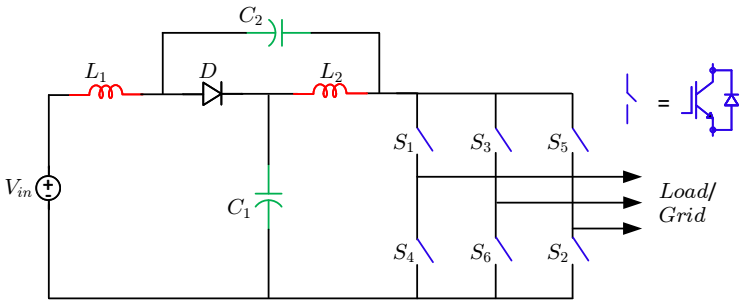


Fig. 2.1. Quasi Z-source inverter (qZSI) [30].

configuration, and a unidirectional diode from the source to the network is placed between the DC power source and the inverter bridge. The primary function of this network is to allow both voltage buck and boost capabilities within a single-stage power conversion system.

However, ZSI has some inherent drawbacks that need to be addressed. One of the primary concerns is the discontinuous input current due to the diode at the input end. Additionally, the ZSI experiences high voltage stress on the capacitors, which can lead to reliability issues and reduced system lifespan. These drawbacks have been addressed with the quasi Z-source inverter (qZSI) [30] as shown in Fig. 2.1. Similar to the ZSI, the qZSI operates in three distinct states. These states include the conventional zero, active, and the crucial shoot-through state. Among these states, the shoot-through state is pivotal for enabling voltage boosting in any impedance source inverter topology. The boost factor for both ZSI and qZSI is defined below:

$$B = \frac{\widehat{V}_{PN}}{V_{in}} = \frac{1}{1-2D}$$

where B denotes the boost factor, the peak dc-link voltage across the inverter is represented by $\widehat{V}_{PN}$, the input DC voltage is denoted as V_{in}, and the shoot-through duty ratio is represented by $D = T_s/T$. The shoot-through time duration is T_s, and T denotes duration of one switching cycle.

The voltage-boost capability of ZSI/qZSI can be significantly enhanced by integrating additional inductors, capacitors and diodes into the impedance network. This extension is particularly beneficial for applications that demand very high voltage gain. A family of extended-boost qZSI [31] topologies, including diode-assisted (DA) extended-boost qZSI

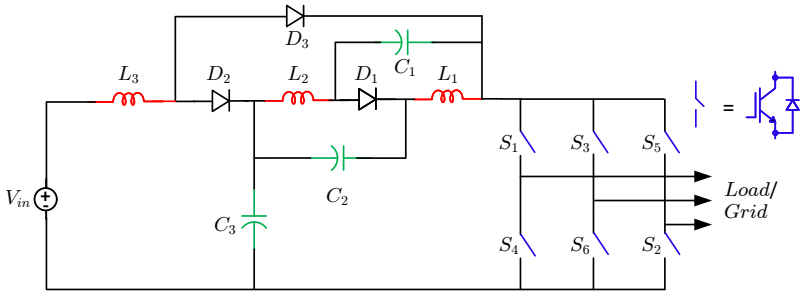


Fig. 2.2. Diode-assisted extended-boost qZSI [31].

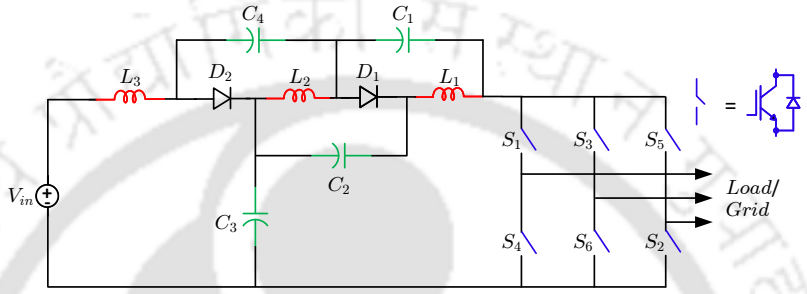


Fig. 2.3. Capacitor-assisted extended-boost qZSI [31].

and capacitor-assisted (CA) extended-boost qZSI, have been proposed as shown in Fig. 2.2. and Fig. 2.3. respectively. The boost factors for these topologies, denoted as B_{DA} and B_{CA} respectively, can be expressed as:

$$B_{DA} = \frac{1}{(1-D)(1-2D)}; \quad B_{CA} = \frac{1}{1-3D}$$

The switched-inductor ZSIs [32] add auxiliary inductors and diodes to the impedance network to increase voltage gain. A common approach is to replace each series inductor of the classic

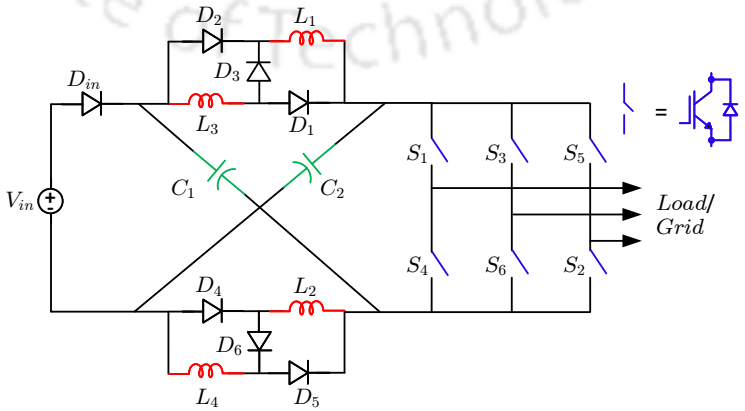


Fig. 2.4. Switched-inductor ZSI [32].

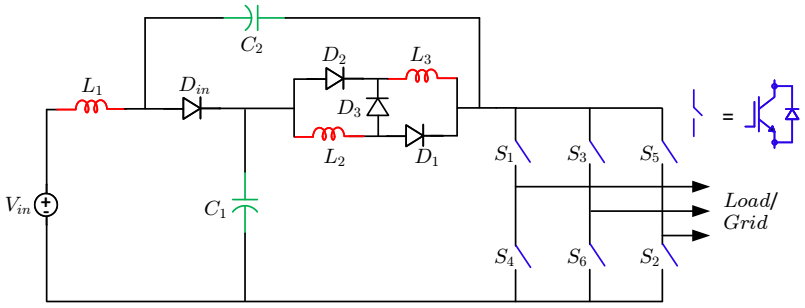


Fig. 2.5. Switched-inductor qZSI [33].

network with a switched network. The switched-inductor (SL) cells comprise three diodes and two inductors, as shown in Fig. 2.4. The top inductor of the ZSI is replaced with a SL cell consisting of (L_1–D_1–L_3–D_2–D_3), and the bottom inductor of the ZSI is replaced with a SL cell consisting of (L_2–D_4–L_4–D_5–D_6). During shoot-through, these additional inductors are connected in series, effectively multiplying the total inductance and boosting the energy pumped into the capacitors. In the following active state, the capacitors thus gain a much higher voltage boost. The boost factor of the SL-ZSI can be expressed as:

$$B = \frac{1+D}{1-3D}$$

However, it exhibits the drawback of discontinuous input current. This discontinuity is primarily attributed to the presence of a diode at the input end. A switched-inductor quasi ZSI (SL-qZSI) [33] topology is introduced to overcome this drawback as shown in Fig. 2.5. In this topology, the inductor L_2 of the qZSI is replaced with SL cells consisting of three diodes and two inductors (L_2–D_1–L_3–D_2–D_3). The presence of inductor L_1 ensures continuous input current. The boost factor of the SL-qZSI can be expressed as follows:

$$B = \frac{1+D}{1-2D-D^2}$$

Two additional topologies have been reported in literature, enhanced boost ZSI [34] and enhanced boost qZSI [35] are shown in Fig. 2.6. and Fig. 2.7. respectively. These novel topologies offer further improvements in the boost factor of inverters. These configurations

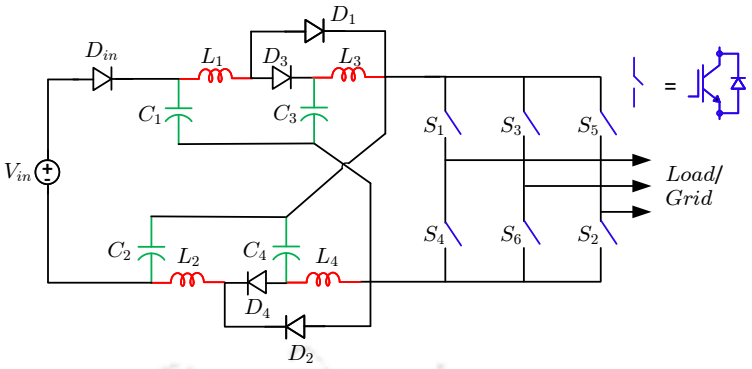


Fig. 2.6. Enhanced-boost ZSI [34].

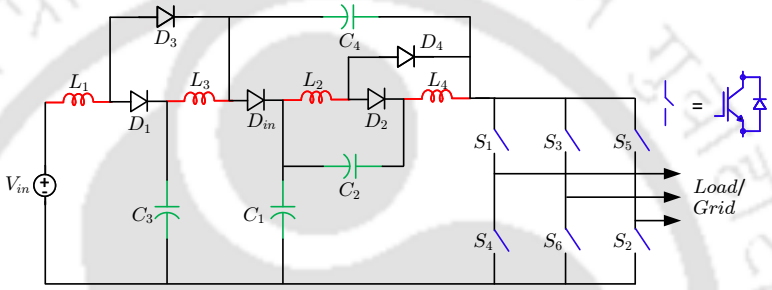


Fig. 2.7. Enhanced-boost qZSI [35].

incorporate four inductors, four capacitors, and five diodes in their impedance networks. The boost factor of these topologies is given below:

$$B = \frac{1}{1 - 4D + 2D^2}$$

In a parallel embedded ZSI [36], two DC sources are connected in series with the inductors of the classical ZSI. Furthermore, an embedded enhanced-boost ZSI [37] with a higher boost factor has been proposed. The above-mentioned topologies use only inductors, capacitors, and diodes in the impedance network and don't use any switches. Several ISI variants incorporating active switches within their impedance networks have been introduced in the literature. One such topology is the switched boost inverter (SBI) [38], depicted in Fig. 2.8. The SBI is developed as a simplified alternative to the traditional ZSI, aiming to reduce the number of passive components by replacing the conventional impedance network with a more compact arrangement. Compared to the original ZSI, the SBI introduces an additional active

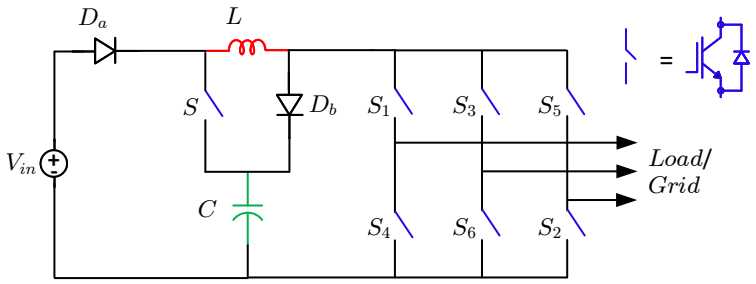


Fig. 2.8. Switched boost inverter [38].

switch while requiring fewer inductors and capacitors, reducing component size and cost. However, one of its limitations is that the voltage gain of the SBI is reduced than that of the ZSI and qZSI. This makes the SBI unsuitable for applications demanding high voltage boost. Additionally, like the original ZSI, the SBI suffers from a discontinuous input current due to the presence of the input diode (D_a), which makes it unsuitable for applications involving renewable energy sources. The boost factor of SBI is given below:

$$B = \frac{1-D}{1-2D}$$

Fig. 2.9. (a) and (b) illustrate the embedded-type quasi switched boost inverter (qSBI) topologies, classified as Type-1 and Type-2, respectively. These configurations employ the same basic components as the conventional SBI topologies. A key characteristic of these embedded designs is that the DC source is connected in series with the inductor. Compared to the basic SBI topology shown in Fig. 2.8., the embedded qSBI topologies offer continuous input current drawn from the DC source. However, a limitation remains, the voltage stress across the capacitor is still equal to the DC-link voltage, similar to the basic SBI. The embedded Type-2 qSBI topology, shown in Fig. 2.9. (b) and introduced in [39], features a common ground between the input source and the inverter bridge. In contrast, the embedded Type-1 qSBI topology, depicted in Fig. 2.9. (a), does not share a common ground between the input and the inverter leg. The boost factor of these topologies are given below:

$$B_1 = \frac{1}{1-2D} \quad and \quad B_2 = \frac{1-D}{1-2D}$$

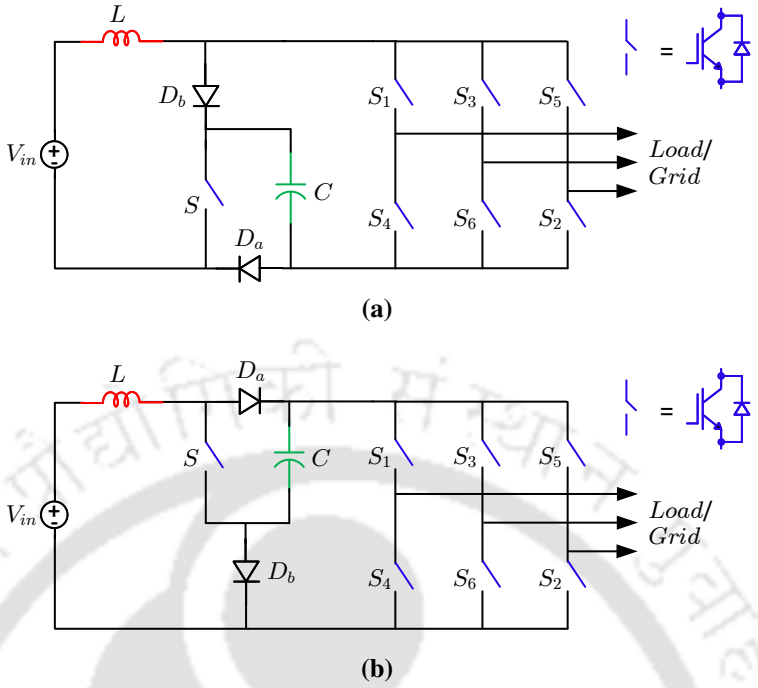


Fig. 2.9. Embedded type qSBI (a) Type-1 and (b) Type-2 [39].

Researchers have discussed several additional similar topologies in the literature with higher boost factors [40–53]. Incorporating switches into the impedance network adds complexity to the ISI topology. The switches enable higher voltage gain capabilities of ISI; their use in the impedance network also introduces several disadvantages related to the complexity of the PWM technique, switching losses, reliability, voltage/current stress, switching frequency limitations, and electromagnetic interference.

2.3 Transformer-based ISI topologies

In the case of non-transformer-based ISIs, achieving very high boost ratios in practice puts enormous stress on the semiconductor switches and components. To overcome this, transformer-based ISI variants have been developed. In these topologies, inductors are replaced with magnetically coupled inductors or transformers to enhance voltage gain, lower device stress, and provide galvanic isolation. The Trans-Z-source inverter (trans-ZSI) [54] modifies the conventional ZSI by using a transformer (or coupled inductor) in the impedance network. In the original trans-ZSI, two versions are proposed, a voltage-fed and a current-fed

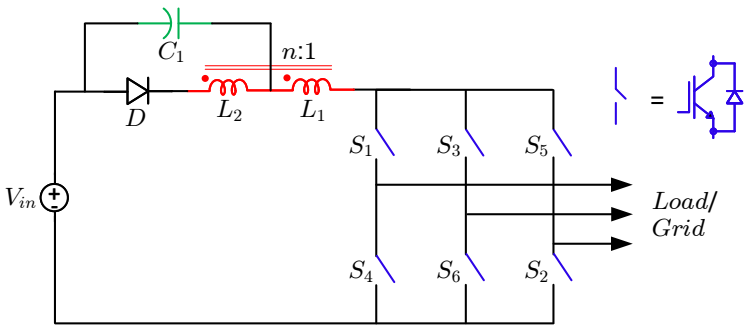


Fig. 2.10. Trans-Z-source inverter [54].

variant. Both replace one of the ZSI inductor with a single transformer (or a tightly coupled inductor) and retain a single capacitor in the network. By adjusting the transformer turns ratio, the trans-ZSI can achieve a higher boost factor than the classic ZSI, with a lower equivalent duty cycle. Its operation is otherwise similar, in the shoot-through state, the transformer stores energy, and in the active state, this energy is released to boost the output. It can operate down to much lower DC input levels and achieves a wider output range. However, the added transformer makes the circuit larger and more costly. Fig. 2.10. illustrates a generic trans-ZSI layout with one transformer and one capacitor. The boost factor is given by:

$$B = \frac{1}{1-(1+n)D}$$

The Y-source inverter [55] extends the trans-ZSI concept by using a three-winding coupled inductor (essentially a three-winding transformer) in the impedance network. The three windings (often called Y1, Y2, Y3) provide additional flexibility, there are three voltage

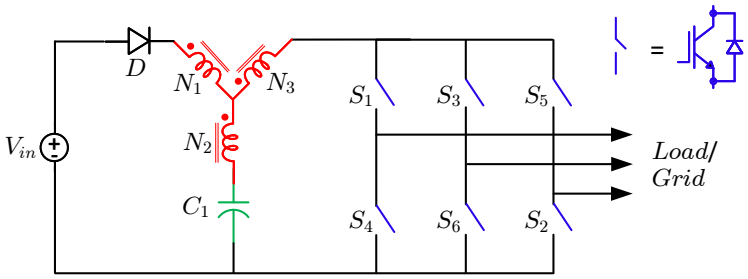


Fig. 2.11. Y-source inverter [55].

levels, two independent turn ratios to choose from, and the shoot-through duty. The Y-source inverter can realize very high voltage gain and high modulation index simultaneously with relatively small shoot-through duty. It has been shown to reduce output current ripple and THD compared to trans-ZSI due to its ability to shape the waveform over the extra winding. In practice, the coupled inductors in this topology can lead to discontinuous input current, and the leakage inductances may cause voltage overshoots during switching. Still, the Y-source topology has been explored for high-gain renewable and motor-drive applications, benefiting from its high step-up capability. The boost factor is given by:

$$B = \frac{1}{1 - \left(\frac{N_3 + N_1}{N_3 - N_2}\right) D}$$

The Γ-Z-source inverter (Gamma-source) [56] is another magnetically-coupled variant derived from the trans-ZSI. It uses two inductors shaped like the Greek letter Γ, with their end windings magnetically coupled to form effectively a single transformer with taps. The coupling and transformer turn ratio can be adjusted to raise the boost gain using fewer components in this network. The Γ-ZSI's gain increases when the turn ratio decreases, unlike most other Z-network topologies. This allows for achieving high voltage boosts with a lower magnetic turns ratio. The Γ-ZSI typically has better spectral performance (lower harmonic distortion) because of its continuous input current, and it achieve a higher modulation index than other impedance-source variants. However, like the Y-source, the Γ-ZSI suffers from leakage inductance effects. The leakage in the coupled inductors introduce extra voltage and current stress on the semiconductors during switching transients. Despite this, due to its high gain and relatively simple layout, the Γ-ZSI is considered well-suited to renewable-energy power converters. The boost factor is given by:

$$B = \frac{1}{1 - \left(1 + \frac{N_1}{N_2}\right) D}$$

The LCCT-Z-source inverter [57] integrates a transformer into a quasi ZSI topology. Specifically, its network is arranged as an Inductor-Capacitor-Capacitor-Transformer (LCCT) chain. It can be viewed as a conventional high-frequency transformer followed by a quasi ZSI network. During the shoot-through state, only one inductor (or one winding) stores energy, and in normal operation, the transformer transfers energy while the capacitors filter the waveform. This lowers the high-frequency ripple on the input and output currents and allows higher voltage gain and modulation index. The LCCT topology has been applied to fuel cells and renewable generation, where continuous input current and high gain are desired. The trade-off is the added complexity of designing a transformer that withstands the switching conditions; however, the two capacitors help keep the core unsaturated. The boost factor is given by:

$$B = \frac{1}{1 - \left(1 + \frac{N_1}{N_2}\right) D}$$

Table 2.1. Comparison of different ISI topologies [16]

Topologies	Boost Factor	Inductors	Capacitors	Diodes	Switches
ZSI [18]	$\frac{1}{1-2D}$	2	2	1	-
qZSI [30]	$\frac{1}{1-2D}$	2	2	1	-
DA-EBqZSI [31]	$\frac{1}{(1-D)(1-2D)}$	3	3	3	-
CA-EBqZSI [31]	$\frac{1}{1-3D}$	3	4	2	-
SL-ZSI [32]	$\frac{1+D}{1-3D}$	4	2	7	-
SL-qZSI [33]	$\frac{1+D}{1-2D-D^2}$	3	2	4	-
Enhanced Boost-ZSI [34]	$\frac{1}{1-4D+2D^2}$	4	4	5	-
Enhanced Boost-qZSI [35]	$\frac{1}{1-4D+2D^2}$	4	4	5	-
SBI [38]	$\frac{1-D}{1-2D}$	1	1	2	1
Embedded qSBI-I [39]	$\frac{1}{1-D}$	1	1	2	1
Embedded qSBI-II [39]	$\frac{1-D}{1-2D}$	1	1	2	1
Trans-ZSI [54]	$\frac{1}{1-(1+n)D}$	1(Coupled)	1	1	-
YSI [55]	$\frac{1}{1-\left(\frac{N_3+N_1}{N_3-N_2}\right)D}$	1 (3-winding)	1	1	-
Γ-ZSI [56]	$\frac{1}{1-\left(1+\frac{N_1}{N_2}\right)D}$	1+1 (Coupled)	2	1	-
LCCT-ZSI [57]	$\frac{1}{1-\left(1+\frac{N_1}{N_2}\right)D}$	1+1 (Coupled)	2	1	-

In summary, transformer-coupled ISIs build on the original ZSI concept to deliver even greater functionality. They offer very high voltage gain and flexible current profiles, making them suitable for challenging power conversion tasks (e.g. renewables, EVs, HESS). The trade-offs are primarily in magnetics design complexity and cost. As wide-bandgap devices and digital control techniques advance and specialized winding technologies (planar/magnetic integration) mature, transformer-based ISIs are poised to become more practical. Several other impedance network topologies [17, 58–62] have recently been introduced to achieve high gain. These topologies involve the addition of diodes, switches, inductors, and capacitors to the impedance network, resulting in a higher DC-link voltage.

2.4 Pulse width modulation of ISIs

The classic sine–triangle PWM (SPWM), known as carrier-based PWM, compares a sinusoidal reference with a high-frequency triangular carrier as shown in Fig. 2.12. (a). This SPWM method is very popular in industry because it provides good fundamental output quality and is relatively easy to implement on analog comparators or digital controllers. For a three-phase VSI, the SPWM scheme generates switching signals by comparing a low-frequency three-phase sinusoidal modulating wave with a high-frequency triangular carrier wave. Whenever the instantaneous reference sine exceeds the triangular carrier, the comparator output goes high, turning on the upper switch of that leg, otherwise, the lower switch conducts. The ISIs utilize the impedance network to allow deliberate shoot-through states as listed in Table 2.2, giving single-stage buck-boost conversion. In a conventional VSI, simultaneously gating both phase leg switches is forbidden; the ISI intentionally uses shoot-through to boost the DC-link, enabling output voltages above the DC input. This fundamental change means that standard PWM schemes must be modified. The challenge is to insert shoot-through intervals without distorting the desired AC waveform while optimizing the voltage boost factor, device stress, and waveform quality. In practice, PWM strategies for ISIs schedule shoot-through states during the traditional zero-voltage intervals so that the AC output remains sinusoidal while the DC voltage is boosted.

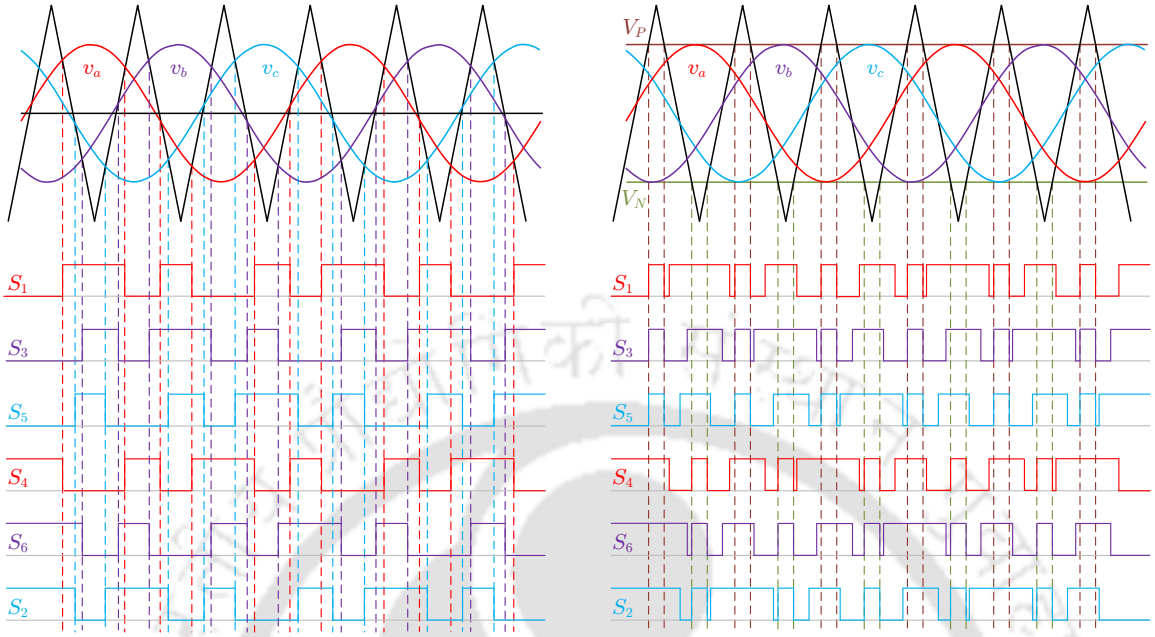


Fig. 2.12. Generation of gate signals (a) sine-triangle PWM and (b) SBC-PWM. [17]

Table 2.2. Switching states of ZSIs [17]

State (Output Voltage)	S_1	S_4	S_3	S_6	S_5	S_2
Active 100 (Finite)	1	0	0	1	0	1
Active 110 (Finite)	1	0	1	0	0	1
Active 010 (Finite)	0	1	1	0	0	1
Active 011 (Finite)	0	1	1	0	1	0
Active 001 (Finite)	0	1	0	1	1	0
Active 101 (Finite)	1	0	0	1	1	0
Zero 000 (0V)	0	1	0	1	0	1
Zero 111 (0V)	1	0	1	0	1	0
Shooth-through E1 (0V)	1	1	S_3	$\overline{S_3}$	S_5	$\overline{S_5}$
Shooth-through E2 (0V)	S_1	$\overline{S_1}$	1	1	S_5	$\overline{S_5}$
Shooth-through E3 (0V)	S_1	$\overline{S_1}$	S_3	$\overline{S_3}$	1	1
Shooth-through E4 (0V)	1	1	1	1	S_5	$\overline{S_5}$
Shooth-through E5 (0V)	1	1	S_3	$\overline{S_3}$	1	1
Shooth-through E6 (0V)	S_1	$\overline{S_1}$	1	1	1	1
Shooth-through E7 (0V)	1	1	1	1	1	1

Several fundamental PWM methods have been proposed for conventional ISIs. The most common are simple boost control [63], maximum boost control [64], and maximum constant boost control [65]. These modify a carrier-based PWM by adding shoot-through

intervals under certain conditions. Table 2.4 lists the advantages and disadvantages of different carrier-based PWM techniques.

A) Simple boost control

The simple boost control (SBC) PWM overlays two straight reference thresholds around the sinusoidal modulation signal as shown in Fig. 2.12. (b). The inverter is forced into shoot-through when the triangular carrier exceeds the upper threshold or falls below the lower threshold. In effect, small shoot-through windows occur at fixed positions in each half-carrier cycle. This method is straightforward and easy to implement using conventional SPWM hardware. However, its boost capability is limited. As the modulation index M increases, the shoot-through intervals rapidly shrink and vanish at $M = 1$. In fact, in the SBC, the maximum shoot-through duty (and thus maximum boost) occurs at low M, and no boosting is available at full modulation. The result is a modest boost factor (typically B in the linear range) and relatively high device voltage stress (some zero-voltage states of a normal VSI are unused).

B) Maximum boost control

To achieve higher gains, maximum boost control (MBC) PWM always converts all traditional zero-voltage vectors into shoot-through. In other words, whenever a zero-vector occurs, the inverter gates both switches on to enter shoot-through. This maximizes the shoot-through duty in each cycle, yielding the greatest possible DC boost for a given modulation command. In practice, one typically combines this with the normal active-state timing of

Table 2.3. Comparison of different PWM techniques [17]

Parameters	**Simple Boost**	**Maximum Boost**	**Constant Boost**
D	1-M	$\frac{(2\pi - 3\sqrt{3}M)}{2\pi}$	1-$\frac{\sqrt{3}}{2}M$
Boost Factor (B)	$\frac{1}{2M-1}$	$\frac{\pi}{3\sqrt{3}M-\pi}$	$\frac{1}{\sqrt{3}M-1}$
Voltage Gain (G)	$\frac{M}{2M-1}$	$\frac{\pi M}{3\sqrt{3}M-\pi}$	$\frac{M}{\sqrt{3}M-1}$
Maximum (M)	1	1	1

SPWM (keeping the six non-zero vectors intact). By using every available zero interval, maximum boost control minimizes device voltage stress for a given output (since the effective DC-link voltage is higher). Its drawback is that every zero interval is now used for boosting, so the inductor currents and capacitor voltages carry a low-frequency ripple tied to the AC output frequency. This ripple can be significant at low output frequencies (e.g., slowly varying loads), requiring bulky inductors or capacitors to filter. Thus, maximum boost is ideal when the AC output frequency is fixed or relatively high; the Z-network currents become more choppy at low frequencies.

C) Constant boost control

The existing PWM technique is modified to maintain a constant shoot-through duty ratio throughout the fundamental cycle while achieving high voltage boost. By injecting a third-harmonic (zero-sequence) component into the sinusoidal references, one can keep the available zero-space constant length and fix the shoot-through duty, regardless of instantaneous M. This constant-boost strategy yields the maximum voltage gain for any desired M without introducing low-frequency ripple. In effect, the DC-link experiences a steady boost in each half-cycle. In practice, the third-harmonic injection is limited to about 16% of the fundamental, extending the linear modulation range from 0–50% (standard SPWM) to about 0–115%. In summary, constant-boost control (CBC) achieves the highest possible gain per modulation index and eliminates the ripple issue at the cost of extra complexity. It requires careful generation of the third-harmonic injection and fixed shoot-through timing. Importantly, maintaining a constant shoot-through duty also helps to minimize the device voltage stress

Table 2.4. Summary of different PWM techniques [17]

PWM Techniques	Advantages	Disadvantages
Simple Boost Control	Very simple to implement	Shoot-through window shrinks to zero as $M \rightarrow 1$ Device voltage stress is relatively high
Maximum Boost Control	Highest attainable boost for a given M	Low output-frequency operation not suitable Large passive components required
Constant-Boost Control	Maintains fixed shoot-through duty	Requires 3rd-harmonic injection The modulation becomes more complex.

and Z-network size. A detailed comparison of different PWM techniques for ZSIs is listed in Table 2.4.

D) Space-vector modulation

Space-vector modulation (SVM) can also be adapted for ZSI [66]. The SVM for VSI inherently has two zero vectors (000 and 111). Modified SVM inserts shoot-through pulses only during the zero-vector intervals, leaving the six active vectors and their timing unchanged. This preserves the classical SVM advantages of lower carrier harmonics and higher linear modulation range while providing a voltage boost. By evenly assigning shoot-through to each phase, these schemes avoid introducing imbalance. In practice, a modified SVM algorithm reduces each zero-vector time, and routes that interval into shoot-through. More detailed analysis of PWM techniques for impedance source inverters is described in [67–71].

2.5 Research motivation

The rapid advancement of power electronics and the growing demand for efficient and reliable energy conversion systems have spurred intensive research into novel inverter topologies. Among these, the ISI and its various modified topologies have emerged as promising alternatives to conventional VSIs and CSIs. The fundamental innovation of ISI lies in its unique impedance network, which allows for both buck and boost operations within a single-stage conversion, offering significant advantages in terms of circuit simplicity, fault tolerance, and cost-effectiveness. However, as the technology evolves, so do the expectations for performance, efficiency, and adaptability to different applications. The primary objectives of this research work are to address specific limitations of existing ISI-based systems and to expand the practical applications of their implementation. The primary objective is to develop an ISI topology that can operate at a lower shoot-through duty ratio, attaining a higher boost factor, so that the operating modulation index is close to unity. Additionally, the design principle of the impedance network inductors and capacitors plays a crucial role in operating the inverter smoothly and efficiently, with lower ripple in inductor currents and capacitor voltages.

(a) **Extending the voltage gain range of ISIs**

One of the central motivations for the ongoing development of ISI topologies is to enhance the voltage gain capability of the inverter. In ISIs, the voltage gain is determined by the shoot-through duty cycle and the configuration of the impedance network. While this configuration allows for boost operation, the achievable gain is limited by component ratings and practical constraints on shoot-through duty. Extending the voltage gain range is crucial for applications where the input voltage is significantly lower than the required output voltage, such as renewable energy systems (e.g., photovoltaic and fuel cell systems), electric vehicles, and specific industrial applications. Several design strategies have been proposed to achieve this objective. One approach involves modifying the impedance network to include additional active/passive components, such as extra inductors, capacitors, diodes, and switches- to increase the boost factor without substantially increasing the stress on individual components. Other approaches include transformer-based Z-source networks, where coupled inductors or isolation transformers are used to achieve higher gains through magnetic coupling.

(b) **Optimizing the PWM technique to reduce switching losses and stress**

PWM plays a crucial role in the operation of ISIs. The inclusion of shoot-through states, which are necessary for boosting, introduces additional switching events that, if not properly managed, can lead to increased switching losses and thermal stress on the power electronic switches and passive components. Therefore, optimizing the PWM technique is also required to minimize these losses while maintaining or improving the overall performance of the inverter. This involves the development of advanced modulation strategies that intelligently control the shoot-through states to reduce switching frequency or distribute switching occurrences in a way that lowers the thermal stress on individual components [72–74]. For example, SVM techniques and hybrid modulation strategies can be employed to achieve better voltage utilization, reduced harmonic distortion, and improved efficiency. An optimized PWM strategy not only

enhances system efficiency but also extends the operational life of the inverter, making it more suitable for long-term deployment in critical infrastructure and renewable energy systems.

(c) **Reducing component count and rating** Another critical objective in the development of new ISI topologies is the reduction of component count and rating. A lower component count directly translates to reduced system complexity, lower cost, and improved reliability. Similarly, using components with lower voltage and current ratings allows for smaller, lighter, and less expensive parts, which are especially important in applications with strict size and weight constraints, such as portable or embedded systems. Designing networks where voltage and current ripples are balanced across multiple components makes it possible to use components with lower ratings without sacrificing performance. This also improves the thermal performance of the inverter and enhances overall system longevity. Traditional ISI configurations, while effective, often require relatively large inductors and capacitors to achieve the desirable boost characteristics. These components occupy considerable space and contribute to overall energy losses through resistive heating and magnetic core losses. To address this, researchers have focused on optimizing the design of the impedance network.

(d) **Application-oriented optimization and improvement** One of the primary objectives is to design ISIs to meet the specific demands of target applications. For instance, a solar inverter used in a residential setting may prioritize high efficiency and low noise. In contrast, an inverter for an electric vehicle may prioritize compactness and faster transient response. Application-oriented optimization involves both hardware and software enhancements. On the hardware side, this could be designing topologies better suited for integrating specific power sources (e.g., a qZSI with maximum power point tracking for solar applications [75]) or developing configurations that can be easily scaled or modularized for larger systems. Adaptive algorithms that can respond to varying load and input conditions are essential on the control side. These algorithms

can adjust operating parameters in real-time to maintain optimal performance. For instance, model predictive control (MPC) and artificial intelligence-based controllers have been explored to manage inverter operations for better efficiency and dynamic response [76–79].

In addition, thermal management, fault tolerance, and protection mechanisms are essential for application-specific improvements. For example, in industrial environments where power quality is crucial, the ISI designs must be robust to input voltage variations and capable of filtering out harmonics effectively. There is growing interest in integrating ISI topologies with energy storage systems, such as batteries and supercapacitors. These applications benefit from the bi-directional power flow capabilities of specific ISI variants, enabling them to serve both as inverters and chargers. This dual functionality is particularly valuable in smart grid and microgrid environments where flexibility and efficiency are paramount.

2.6 Objectives of the thesis

Based on the above research motivations, the primary objective of this thesis is to develop and analyze advanced ZSI topologies with enhanced voltage-boosting capability and improved overall performance for low-voltage DC applications such as PV and DG systems. To achieve this overarching goal, the following specific objectives are pursued:

(1) To achieve a high voltage boost at a lower shoot-through duty ratio, thereby reducing stress on the inverter-leg switches and improving overall system reliability. A lower shoot-through duty ratio enables operations at a modulation index close to unity, which improves the quality of the output AC voltage, reduces harmonic distortion, and enhances utilization of the inverter switches.

(2) To design an efficient impedance network, with appropriately sized inductors and capacitors that ensure stable energy transfer during both shoot-through and non-shoot-through states, thus minimizing ripple in inductor currents and capacitor voltages,

thereby reducing conduction losses, electromagnetic interference, and thermal stress on passive components.

2.7 Contributions of the thesis

Based on the objectives listed in Section 2.6, the contributions of the thesis are listed below:

(1) To propose novel switched-inductor extended-boost qZSI topologies, including the diode-assisted (DA-SLEBqZSI) and capacitor-assisted (CA-SLEBqZSI) configurations, and to analyze their steady-state in both shoot-through and non-shoot-through states.

(2) To develop an improved extended-boost qZSI topology (improved-EBqZSI) with superior voltage gain at lower shoot-through duty ratios, supporting higher modulation indices and reducing stress on inverter switches.

(3) To perform mathematical modeling and derive expressions for boost factors, voltage gain, and component stress across the above proposed topologies to guide the selection and sizing of impedance network components.

(4) To validate the proposed topologies and design methods through comprehensive simulation studies using PSCAD and experimental verification using hardware prototypes.

(5) To present a systematic design methodology for selecting impedance network parameters that ensure continuous energy transfer, minimize ripple, and prevent undesirable static states during inverter operation.

(6) To evaluate and compare the performance of the proposed inverter topologies with existing designs in terms of voltage boost capability, component stress, switching losses, and overall efficiency, thereby demonstrating their suitability for next-generation power electronics applications.

2.8 Organization of the thesis

This thesis is organized into six chapters. **Chapter 1** provides the background of the thesis and a brief review of the ISI topologies. The chapter also presents a classification of ISI topologies based on the presence or absence of transformers or coupled inductors. A detailed explanation of the ZSI operation is then provided, covering both the NST and ST states. The mathematical modeling and analysis of the ZSI are presented to derive the boost factor. Furthermore, the advantages and inherent limitations of the ZSI are discussed. Finally, the chapter highlights the major application areas of the ZSI.

Chapter 2 provides a critical review of ISI topologies and their associated PWM techniques. A detailed discussion is presented on the classification of ISI topologies based on the presence or absence of transformers or coupled inductors. The boost factors of these topologies are systematically analyzed. Furthermore, the PWM strategies employed for ISIs are discussed in detail, including SBC, MBC, CBC, and SVM. Based on the insights gained from the literature survey, the research gaps in existing ISI topologies are identified, which form the basis for the research motivation. Subsequently, a set of research objectives is formulated. The chapter concludes with the overall organization of the thesis.

In **Chapter 3**, a family of switched-inductor extended-boost quasi Z-source inverter topologies has been presented. These include the diode-assisted switched-inductor extended-boost quasi Z-source inverter and the capacitor-assisted switched-inductor extended-boost quasi Z-source inverter. A comprehensive analysis of the inverter operation is carried out for both shoot-through and non-shoot-through modes. Mathematical derivations are provided to calculate the boost factor and guidelines for the design of the impedance network components. The theoretical findings are validated through detailed simulations carried out and corroborated by experimental results obtained from laboratory-built prototypes. These results demonstrate the high-gain performance of the proposed inverters. Furthermore, an in-depth evaluation of capacitor voltages, diode stress, and switch stress is provided for the new topologies. The performance metrics are compared against existing inverter designs reported in the literature, highlighting the advantages and superior characteristics of these proposed inverters.

An improved extended-boost quasi Z-source inverter topology is presented in **Chapter 4**. This inverter topology offers enhanced voltage-boosting capability compared to the switched-inductor extended-boost quasi Z-source inverter topologies while operating with a reduced shoot-through duty cycle. As a result, they support higher modulation indices, leading to improved output voltage performance and reduced electrical stress on the inverter switches. A detailed analysis of the proposed inverter topology covers both shoot-through and non-shoot-through operational modes. Mathematical derivations are presented to determine the boost factor, along with selecting appropriate impedance network components to keep the ripple in inductor currents and capacitor voltages as per the design specification. In addition, a comprehensive assessment of capacitor voltages, diode stress, and switch stress is provided for this topology. The performance of the proposed topologies is compared with inverter topologies documented in the literature, clearly demonstrating its advantages in terms of voltage gain and component stress reduction.

Chapter 5 presents a detailed and illustrated design methodology for the impedance network of the qZSI. The operation of the qZSI is thoroughly investigated across shoot-through, non-shoot-through, and active states. In addition to these desired dynamic states, it identifies and discusses three potential static states that may arise under certain conditions. To ensure reliable operation and avoid these undesirable static states, the impedance network must be carefully designed. For the purpose of analysis, a linear approximation is adopted by assuming a small ripple in the capacitor voltages and inductor currents. The values of the inductors and capacitors in the impedance network are determined by solving a set of simultaneous equations derived during the design process. These calculated design parameters are subsequently validated through simulation and experimental results, confirming the accuracy and effectiveness of the proposed design approach.

In **Chapter 6**, the concluding remarks of the thesis are outlined. Based on these conclusions, potential directions for future works are proposed.

2.9 Summary

This chapter discusses the design trade-offs across different ZSI topologies. Transformer-based ISIs provide high voltage gain, making them suitable for RES, EVs, and HESS applications. However, they come with increased complexity in magnetic design and higher costs. Incorporating active switches into the impedance network enhances control flexibility and facilitates the development of new topologies, but also adds hardware and control complexity, increases losses, generates EMI, and reduces system reliability. On the other hand, ZSIs that utilize only passive components, diodes, inductors, and capacitors offer a simpler design, greater reliability, and lower costs due to reduced control and thermal management requirements. The next chapter introduces two novel switched-inductor extended-boost qZSI topologies that enhance the boost factor while maintaining a passive-only impedance network.

CHAPTER 3

Switched-Inductor Extended-Boost Quasi Z-Source Inverter

3.1 Introduction

As discussed in the previous chapter, rearrangement in the impedance network can be done to enhance the gain of ISIs. Transformer-based ISIs provide enhanced gain by incorporating a transformer/coupled inductor into the impedance network; these topologies achieve very high voltage gain, making them well-suited for demanding power conversion applications such as RES, EVs, and HESS. However, this improved performance comes with trade-offs, particularly in increased magnetic design complexity and higher cost due to the transformer.

Also, introducing active switches into the impedance network of a ISI can enhance control flexibility and enable new topologies. Adding switches requires additional gate drivers, control logic, and coordination with the inverter switching sequence. This makes the system more complex in terms of both hardware design and control software. Every additional switch introduces switching and conduction losses, which reduce overall efficiency. This also adds to the thermal management burden, requiring larger heatsinks or active cooling systems in compact designs. Additional switching events in the impedance network can increase EMI, potentially affecting nearby control circuits or communication. It also reduces system reliability, as more components are subject to wear and aging.

ISI topologies that use only diodes, inductors, and capacitors, without any additional active switches in the impedance network, offer several important advantages, particularly in terms of reliability and cost-effectiveness. One of the primary benefits is the simplicity of the circuit. The impedance network becomes easier to design, control, and implement without extra switches. This reduces the complexity of the gate-driving circuitry and avoids synchronization issues between multiple switches. The absence of active components in the impedance path also enhances system reliability, as passive components like inductors and capacitors typically have longer lifespans and lower failure rates than active devices.

This chapter introduces two novel switched-inductor extended-boost qZSI topologies: Diode-assisted switched-inductor extended-boost qZSI (DA-SLEBqZSI) and capacitor-assisted switched-inductor extended-boost qZSI (CA-SLEBqZSI). These topologies are derived from SL-qZSI and continuous current configuration of the CA-EBqZSI. Section 3.2 and Section 3.3 present a detailed theoretical analysis of the DA-SLEBqZSI and CA-SLEBqZSI, covering both steady-state and dynamic behavior. The operational modes of the inverter are examined, and the fundamental equations governing its operation are derived. Key performance parameters such as voltage gain, boost factor, and component stresses are analytically expressed. Section 3.4 details the design methodology for the passive components, with a particular focus on the inductors and capacitors used in the impedance network. The sizing of these components is based on the analytical expressions developed in the preceding sections. It considers critical design factors, including current and voltage ripple limits, voltage ratings, and the chosen switching frequency. The selected component values are aligned with standard commercial specifications to ensure practicality and robust performance under expected load conditions. A detailed design example are presented in Section 3.5 to illustrate the practical implementation of the proposed inverter topologies. Section 3.6 presents simulation and experimental results to validate the theoretical analysis. Simulations performed to illustrate the inverter operating across various operating conditions. These results are corroborated by experimental data obtained from a laboratory prototype, demonstrating the practical feasibility and high boost performance of the SLEBqZSIs, especially at low input voltages. Finally, Section 3.7 offers a comparative evaluation of the SLEBqZSIs against several existing impedance-source inverter topologies documented in the literature. The comparison focuses on critical metrics such as component count, voltage gain, boost factor, component stress, and efficiency, thereby highlighting the distinctive advantages of the proposed topology over conventional designs.

3.2 Diode-assisted switched-inductor extended-boost qZSI

The circuit diagram of the proposed DA-SLEBqZSI topology is shown in Fig. 3.1. This inverter topology is designed for a single-stage DC-AC power conversion with a voltage boost functionality. This impedance network replaces the inductor L_3 in the CA-EBqZSI with a switched-inductor cell consisting of two inductors and three diodes. The impedance network is placed between the DC source (V_{in}) and the three-phase inverter legs. The impedance network of the DA-SLEBqZSI comprises four inductors L_{1-4}, four capacitors C_{1-4}, and five diodes D_{1-5}. The three-phase inverter bridge consists of six switches S_{1-6}, each equipped with an anti-parallel diodes D_{1-6}, responsible for converting the DC-link voltage (V_{PN}) to an AC output. The switches and the anti-parallel diode are arranged as $S_1 - S_3 - S_5$ are top switches, and $S_4 - S_6 - S_2$ are bottom switches. The main advantage of the DA-SLEBqZSI is its ability to achieve a higher boost factor by incorporating the switched-inductor network, which enhances the voltage boost capability compared to traditional ZSI topologies. The impedance network in the DA-SLEBqZSI enables additional shoot-through switching states, allowing the short-circuiting of the inverter bridge and enabling the system to boost the input voltage. The AC output voltage can be widely varied by adjusting the duration of the shoot-through state. The shoot-through duty ratio D is defined as $D = t_S/T$, where t_S is the shoot-through duration, and T is the duration of a switching cycle.

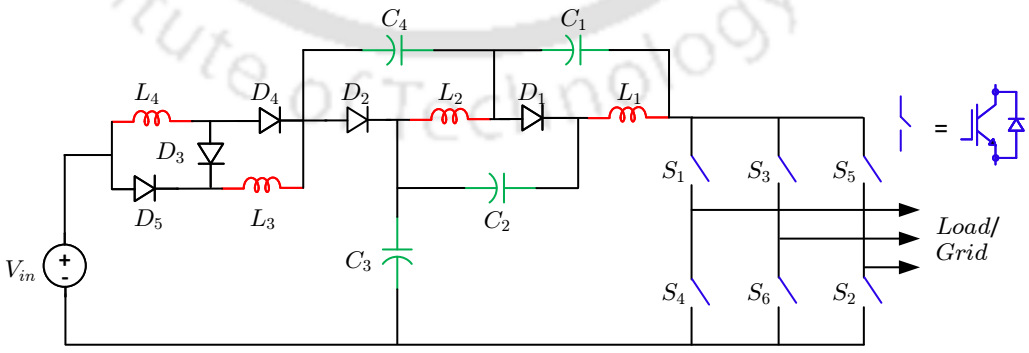


Fig. 3.1. Circuit diagram of DA-SLEBqZSI.

3.2.1 Operating principle of the DA-SLEBqZSI

Like any ZSI, the DA-SLEBqZSI operates in three states: shoot-through and non-shoot-through (active and zero) state. No power is transferred in zero states, therefore, the operation of the DA-SLEBqZSI in the shoot-through and non-shoot-through (active) states will be discussed in this work. For the analysis of the DA-SLEBqZSI during both shoot-through and non-shoot-through intervals, the following assumptions are made:

- All circuit elements are ideal (no losses or non-linearities).
- The inverter operates in continuous conduction mode (CCM), meaning inductor current does not drop to zero.
- The fundamental output frequency f is much lower than the inverter switching frequency f_s.
- During shoot-through intervals, switches are turned ON simultaneously without dead-time delays.

The steady-state voltages across inductors L_1, L_2, L_3, and L_4 are V_{L_1}, V_{L_2}, V_{L_3}, and V_{L_4} respectively, and V_{C_1}, V_{C_2}, V_{C_3}, and V_{C_4} are the steady-state voltages across capacitors C_1, C_2, C_3, and C_4 respectively. The steady-state currents flowing through the inductors in the proposed DA-SLEBqZSI are I_{L_1}, I_{L_2}, I_{L_3}, and I_{L_4} and those flowing through the capacitors are I_{C_1}, I_{C_2}, I_{C_3}, and I_{C_4} respectively. The equivalent circuits of the proposed DA-SLEBqZSI topology, in shoot-through and non-shoot-through states are shown in Fig. 3.2. and Fig. 3.3. respectively.

A) Shoot-through state

During the shoot-through interval DT, the upper and lower switches of one or more legs are turned on simultaneously, thereby creating a short circuit across the DC-link voltage. The inductors are charged, and energy is transmitted from the source or capacitors to the inductor while the capacitors are discharged in this state. This led to a voltage boost. Diodes

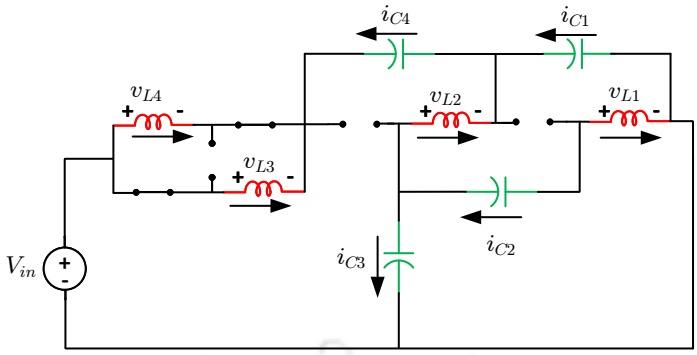


Fig. 3.2. Equivalent circuit of DA-SLEBqZSI in shoot-through state.

D_4 and D_5 are forward biased and will be equivalent to a short circuit, and diodes D_1, D_2, and D_3 will have a reversed bias, therefore, these three diodes are open-circuited. Thus, the mathematical equations of the inductor voltages in the shoot-through interval can be written as:

$$\begin{aligned} v_{L_1}(t) &= v_{C_2}(t) + v_{C_3}(t) \\ v_{L_2}(t) &= v_{C_1}(t) + v_{C_3}(t) \\ v_{L_3}(t) = v_{L_4}(t) &= V_{in} + v_{C_1}(t) + v_{C_4}(t) \end{aligned} \tag{3.1}$$

Similarly, the mathematical equations of the capacitor currents in the shoot-through interval can be written as:

$$\begin{aligned} i_{C_1}(t) &= -(i_{L_2}(t) + i_{L_3}(t) + i_{L_4}(t)) \\ i_{C_2}(t) &= -i_{L_1}(t) \\ i_{C_3}(t) &= -(i_{L_1}(t) + i_{L_2}(t)) \\ i_{C_4}(t) &= -(i_{L_3}(t) + i_{L_4}(t)) \end{aligned} \tag{3.2}$$

The small ripple approximation assumes that the ripples in inductor current and capacitor voltage over a switching period are small compared to their average values. Under this assumption, the instantaneous capacitor voltage $v_C(t)$ and inductor current $i_L(t)$ can be expressed as the sum of their average (DC) components and small time-varying (AC) perturbations, as shown below:

$$v_C(t) = V_C + \tilde{v}_C(t)$$
$$i_L(t) = I_L + \tilde{i}_L(t)$$

where V_C and I_L are the average values of the capacitor voltage and inductor current, respectively, and $\tilde{v}_C(t)$ and $\tilde{i}_L(t)$ represent the small ripple components.

Using small ripple approximation, (3.1) and (3.2) can be rewritten as

$$\begin{aligned} v_{L_1}(t) &= V_{C_2} + V_{C_3} \\ v_{L_2}(t) &= V_{C_1} + V_{C_3} \\ v_{L_3}(t) = v_{L_4}(t) &= V_{in} + V_{C_1} + V_{C_4} \end{aligned} \tag{3.3}$$

$$\begin{aligned} i_{C_1}(t) &= -(I_{L_2} + I_{L_3} + I_{L_4}) \\ i_{C_2}(t) &= -I_{L_1} \\ i_{C_3}(t) &= -(I_{L_1} + I_{L_2}) \\ i_{C_4}(t) &= -(I_{L_3} + I_{L_4}) \end{aligned} \tag{3.4}$$

B) Non-shoot-through state

During the non-shoot-through interval $(1-D)T$, the inverter operates in one of six possible active states, delivering a constant current I_{PN} to the load. In the non-shoot-through state the inductors discharged when the capacitors are charged. Diodes D_4 and D_5 will be reverse biased and are equivalent to an open circuit, and diodes D_1, D_2, and D_3 are forward biased, so these three diodes are short-circuited. Thus, the mathematical equations of the inductor voltages and capacitor currents in the non-shoot-through interval can be written as:

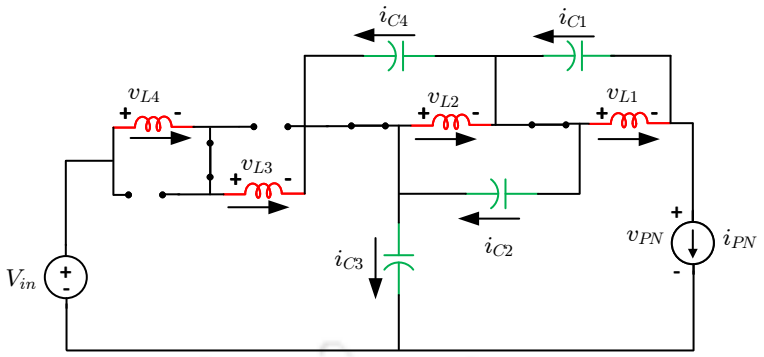


Fig. 3.3. Equivalent circuit of DA-SLEBqZSI in non-shoot-through state.

$$\begin{aligned} v_{L_1}(t) &= -v_{C_1}(t) \\ v_{L_2}(t) &= -v_{C_2}(t) = -v_{C_4}(t) \\ v_{L_3}(t) &= v_{L_4}(t) = \frac{(V_{in} - v_{C_3}(t))}{2} \\ v_{PN}(t) &= v_{C_1}(t) + v_{C_2}(t) + v_{C_3}(t) \end{aligned} \tag{3.5}$$

$$\begin{aligned} i_{C_1}(t) &= i_{L_1}(t) - i_{PN}(t) \\ i_{C_3}(t) &= i_{L_3}(t) - i_{PN}(t) \\ i_{C_2}(t) + i_{C_4}(t) &= i_{L_2}(t) - i_{PN}(t) \end{aligned} \tag{3.6}$$

Using small ripple approximation, (3.5) and (3.6) can be rewritten as

$$\begin{aligned} v_{L_1}(t) &= -V_{C_1} \\ v_{L_2}(t) &= -V_{C_2} = -V_{C4} \\ v_{L_3}(t) &= v_{L_4} = \frac{(V_{in} - V_{C_3})}{2} \\ v_{PN}(t) &= V_{C_1} + V_{C_2} + V_{C_3} \end{aligned} \tag{3.7}$$

$$\begin{aligned} i_{C_1}(t) &= I_{L_1} - I_{PN} \\ i_{C_3}(t) &= I_{L_3} - I_{PN} \\ i_{C_2}(t) + i_{C_4}(t) &= I_{L_2} - I_{PN} \end{aligned} \tag{3.8}$$

3.2.2 Steady state analysis of the DA-SLEBqZSI

This steady-state analysis offers critical insights into the voltage and current behavior of the proposed improved-EBqZSI topology, facilitating a deeper understanding of its operational performance and effectiveness in achieving a voltage boost. In steady-state conditions, the average voltage across an inductor over a complete switching cycle must be zero by the inductor volt-second balance principle. This principle is foundational in analyzing switching converters and ensures that the magnetic flux within the inductors does not continuously increase or decrease over time. Let "D" represent the shoot-through duty ratio, defined as the ratio of the shoot-through duration to the total switching period, applying inductor volt-sec balance to inductors L_1, L_2, L_3, L_4, and L_5 using (3.3) and (3.7) we obtain expand this

$$\langle v_L(t)\rangle_T = \begin{cases} D\cdot(V_{C_2}+V_{C_3})+(1-D)\cdot(-V_{C_1})=0 \\ D\cdot(V_{C_1}+V_{C_3})+(1-D)\cdot(-V_{C_2})=0 \\ D\cdot(V_{C_1}+V_{C_3})+(1-D)\cdot(-V_{C_4})=0 \\ D\cdot(V_{in}+V_{C_1}+V_{C_4})+(1-D)\cdot\dfrac{(V_{in}-V_{C_3})}{2}=0 \end{cases} \tag{3.9}$$

By solving the above equations and simplifying the expressions, the resulting equation can be expressed as follows:

$$\begin{aligned} V_{C_1} &= \frac{D}{(1-D)}\cdot(V_{C_2}+V_{C_3}) \\ V_{C_2} &= \frac{D}{(1-D)}\cdot(V_{C_1}+V_{C_3}) \\ V_{C_4} &= \frac{D}{(1-D)}\cdot(V_{C_1}+V_{C_3}) \end{aligned} \tag{3.10}$$

The set of equations given in (3.10) can be rewritten with respect to V_{C_3} is as below:

$$V_{C_1}=V_{C_2}=V_{C_4}=\frac{D}{(1-2D)}\cdot V_{C_3} \tag{3.11}$$

Substituting (3.11) into (3.10) yields the following expression:

$$V_{C_3} = \frac{(1-2D)\cdot(1+D)}{(1-3D-2D^2)} \cdot V_{in} \tag{3.12}$$

By applying (3.12) to (3.11), we obtain:

$$V_{C_1} = V_{C_2} = V_{C_4} = \frac{D\cdot(1+D)}{(1-3D-2D^2)} \cdot V_{in} \tag{3.13}$$

Based on (3.7), (3.12), and (3.13), the peak DC-link voltage across the inverter legs can be derived as follows:

$$\widehat{V}_{PN} = \frac{1+D}{(1-3D-2D^2)} \cdot V_{in} \tag{3.14}$$

Thus the boost factor for the proposed DA-SLEBqZSI is derived as:

$$B = \frac{\widehat{V}_{PN}}{V_{in}} = \frac{1+D}{(1-3D-2D^2)} \tag{3.15}$$

The peak phase AC output voltage of the DA-SLEBqZSI is determined using the modulation index and boost factor as follows:

$$\widehat{v}_m = M \cdot \frac{\widehat{V}_{PN}}{2} = M \cdot B \cdot \frac{V_{in}}{2} = G \cdot \frac{V_{in}}{2} \tag{3.16}$$

For simple boost control $M = (1-D)$, the peak AC voltage gain can be expressed in terms of the modulation index (M) and boost factor (B) as follows:

$$G = M \cdot B = \frac{M\cdot(M-2)}{(2M^2-7M+4)} \tag{3.17}$$

In steady state, the net charge gained or lost by a capacitor over one complete switching period is zero. This implies that the average capacitor current over a switching cycle is zero.

Using capacitor amp-second balance, we obtain

$$\langle i_C(t)\rangle_T = \begin{cases} -D\cdot(I_{L_2}+I_{L_3}+I_{L_4})+(1-D)\cdot(I_{L_1}-I_{PN})=0 \\ -D\cdot(I_{L_1}+I_{L_2})+(1-D)\cdot(I_{L_3}-I_{PN})=0 \\ -D\cdot(I_{L_1}+I_{L_3}+I_{L_4})+(1-D)\cdot(I_{L_2}-I_{PN})=0 \end{cases} \tag{3.18}$$

Solving the above equations simultaneouslt we get

$$\begin{aligned} I_{L_1} = I_{L_2} &= \frac{1-D^2}{(1-3D-2D^2)}\cdot I_{PN} \\ I_{L_3} = I_{L_4} &= \frac{1-D}{(1-3D-2D^2)}\cdot I_{PN} \end{aligned} \tag{3.19}$$

(3.19) represents the average inductor currents in the impedance network inductors of the DA-SLEBqZSI.

3.3 Capacitor-assisted switched-inductor extended-boost qZSI

The proposed capacitor-assisted switched-inductor extended-boost quasi Z-source inverter (CA-SLEBqZSI) topology is shown in Fig. 3.4. This topology is derived from the DA-SLEBqZSI topology by replacing diode D_5 with capacitor C_5 connected to common ground. Consequently, the proposed CA-SLEBqZSI topology incorporates four inductors, five capacitors, and four diodes in its impedance network, aiming to improve the boost factor.

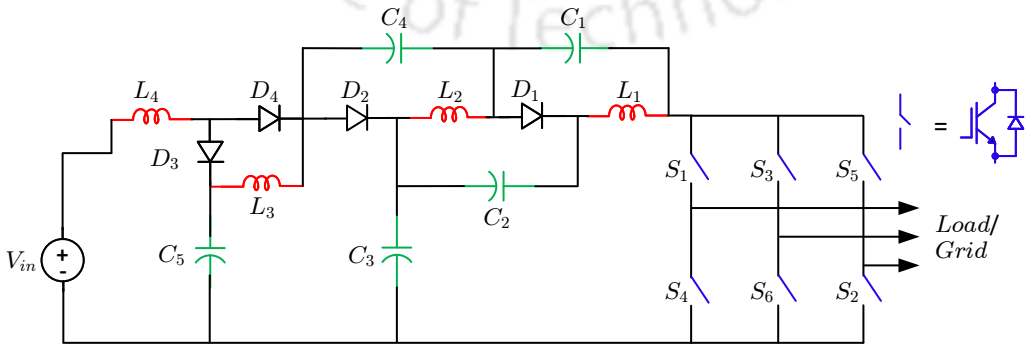


Fig. 3.4. Circuit diagram of CA-SLEBqZSI.

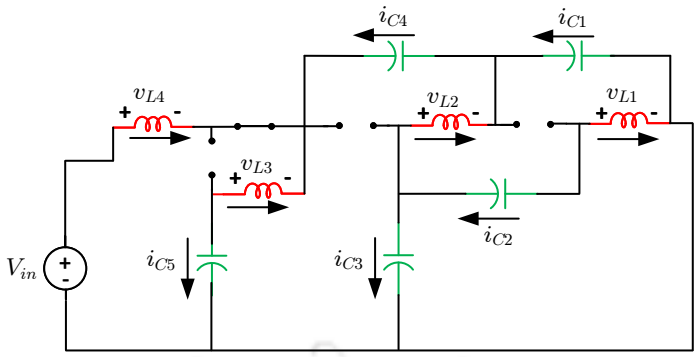


Fig. 3.5. Equivalent circuit of CA-SLEBqZSI in shoot-through state.

3.3.1 Operating principle of the CA-SLEBqZSI

The operating principle of CA-SLEBqZSI is the same as that of DA-SLEBqZSI. The steady-state voltages across inductors (V_{L_1}, V_{L_2}, V_{L_3}, and V_{L_4}) and the steady-state voltages across capacitors (V_{C_1}, V_{C_2}, V_{C_3}, V_{C_4}, and V_{C_5}) are determined during the steady-state operation of the CA-SLEBqZSI. Additionally, the steady-state currents flowing through inductors (I_{L_1}, I_{L_2}, I_{L_3}, and I_{L_4}) and the steady-state currents flowing through capacitors (I_{C_1}, I_{C_2}, I_{C_3}, I_{C_4}, and I_{C_5}) are considered. The equivalent circuits of the proposed CA-SLEBqZSI topology, in shoot-through and non-shoot-through states are shown in Fig. 3.5. and Fig. 3.6. respectively.

A) Shoot-through state

During the shoot-through interval DT, the simultaneous conduction of upper and lower switches in a leg creates a short circuit across the DC-link. In this condition, the inductors begin to charge, drawing energy from either the input source or the capacitors, while the capacitors discharge to support the energy transfer. This energy storage in the inductors during the shoot-through phase is the primary mechanism that enables voltage boosting in the inverter. In the shoot-through state, diode D_4 is forward biased and acts as a short circuit, whereas diodes D_1, D_2, and D_3 are reverse biased and behave as open circuits. Thus, the mathematical equations of the inductor voltages and capacitor currents in the shoot-through

interval can be written as:

$$\begin{aligned} v_{L_1}(t) &= v_{C_2}(t) + v_{C_3}(t) \\ v_{L_2}(t) &= v_{C_1}(t) + v_{C_3}(t) \\ v_{L_3}(t) &= v_{C_1}(t) + v_{C_4}(t) + v_{C_5}(t) \\ v_{L_4}(t) &= V_{in} + v_{C_1}(t) + v_{C_4}(t) \end{aligned} \tag{3.20}$$

$$\begin{aligned} i_{C_1}(t) &= -(i_{L_2}(t) + i_{L_3}(t) + i_{L_4}(t)) \\ i_{C_2}(t) &= -i_{L_1}(t) \\ i_{C_3}(t) &= -(i_{L_1}(t) + i_{L_2}(t)) \\ i_{C_4}(t) &= -(i_{L_3}(t) + i_{L_4}(t)) \end{aligned} \tag{3.21}$$

Using small ripple approximation, (3.20) and (3.21) can be rewritten as

$$\begin{aligned} v_{L_1}(t) &= V_{C_2} + V_{C_3} \\ v_{L_2}(t) &= V_{C_1} + V_{C_3} \\ v_{L_3}(t) &= V_{C_1} + V_{C_4} + V_{C_5} \\ v_{L_4}(t) &= V_{in} + V_{C_1} + V_{C_4} \end{aligned} \tag{3.22}$$

$$\begin{aligned} i_{C_1}(t) &= -(I_{L_2} + I_{L_3} + I_{L_4}) \\ i_{C_2}(t) &= -I_{L_1} \\ i_{C_3}(t) &= -(I_{L_1} + I_{L_2}) \\ i_{C_4}(t) &= -(I_{L_3} + I_{L_4}) \end{aligned} \tag{3.23}$$

B) Non-shoot-through state

During the non-shoot-through interval $(1-D)T$, the inverter operates in one of six possible active states, delivering a constant current I_{PN} to the load. In this interval, the inductors discharge, transferring stored energy to the load, while the capacitors are recharged. This phase ensures continuous power delivery and energy balance within the system. In this state,

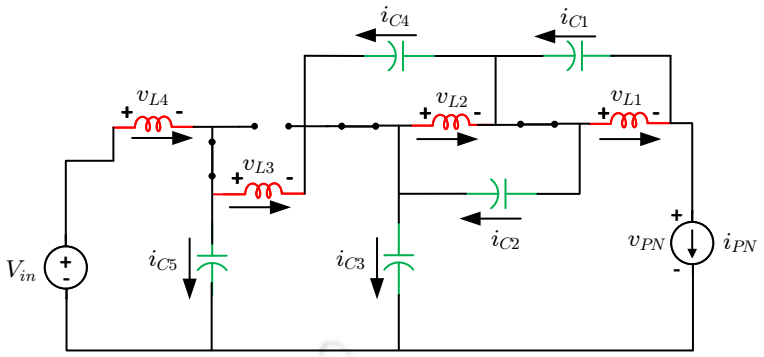


Fig. 3.6. Equivalent circuit of CA-SLEBqZSI in non-shoot-through state.

diode diode D_4 becomes reverse biased, effectively behaving as open circuits and blocking current flow. On the other hand, diodes D_1, D_2, and D_3 are forward biased, acting as short circuits, and allow current to flow freely through their respective paths. Thus, the mathematical equations of the inductor voltages and capacitor currents in the non-shoot-through interval can be written as:

$$\begin{aligned} v_{L_1}(t) &= -v_{C_1}(t) \\ v_{L_2}(t) &= -v_{C_2}(t) = -v_{C_4}(t) \\ v_{L_3}(t) &= v_{C_5}(t) - v_{C_3}(t) \\ v_{L_4}(t) &= V_{in} - v_{C_5}(t) \\ v_{PN}(t) &= v_{C_1}(t) + v_{C_2}(t) + v_{C_3}(t) \end{aligned} \tag{3.24}$$

$$\begin{aligned} i_{C_1}(t) &= i_{L_1}(t) - i_{PN}(t) \\ i_{C_3}(t) &= i_{L_3}(t) - i_{PN}(t) \\ i_{C_5}(t) &= i_{L_4}(t) - i_{L_3}(t) \\ i_{C_2}(t) + i_{C_4}(t) &= i_{L_2}(t) - i_{PN}(t) \end{aligned} \tag{3.25}$$

Using small ripple approximation, (3.24) and (3.25) can be rewritten as

$$\begin{aligned} v_{L_1}(t) &= -V_{C_1} \\ v_{L_2}(t) &= -V_{C_2} = -V_{C_4} \\ v_{L_3}(t) &= V_{C_5} - V_{C_3} \\ v_{L_4}(t) &= V_{in} - V_{C_5} \\ V_{PN}(t) &= V_{C_1} + V_{C_2} + V_{C_3} \end{aligned} \tag{3.26}$$

$$\begin{aligned} i_{C_1}(t) &= I_{L_1} - I_{PN} \\ i_{C_3}(t) &= I_{L_3} - I_{PN} \\ i_{C_5}(t) &= I_{L_4} - I_{L_3} \\ i_{C_2}(t) + i_{C_4}(t) &= I_{L_2} - I_{PN} \end{aligned} \tag{3.27}$$

3.3.2 Steady state analysis of the CA-SLEBqZSI

The steady-state analysis offers crucial insights into the voltage and current behavior of the proposed CA-SLEBqZSI topology, facilitating a deeper understanding of its voltage-boosting capability and overall performance. In steady-state operation, the average voltage across each inductor over a complete switching cycle is assumed to be zero, in accordance with the principle of inductor volt-second balance. Let "D" denotes as the shoot-through duty ratio, applying inductor volt-sec balance to inductors L_1, L_2, L_3, and L_4 using (3.22) and (3.26) we obtain

$$\langle v_L(t)\rangle_T = \begin{cases} D\cdot(V_{C_2}+V_{C_3}) + (1-D)\cdot(-V_{C_1}) = 0 \\ D\cdot(V_{C_1}+V_{C_3}) + (1-D)\cdot(-V_{C_2}) = 0 \\ D\cdot(V_{C_1}+V_{C_3}) + (1-D)\cdot(-V_{C_4}) = 0 \\ D\cdot(V_{C_1}+V_{C_4}+V_{C_5}) + (1-D)\cdot(V_{C_5}-V_{C_3}) = 0 \\ D\cdot(V_{in}+V_{C_1}+V_{C_4}) + (1-D)\cdot(V_{in}-V_{C_5}) = 0 \end{cases} \tag{3.28}$$

By solving the above equations simultaneously, the following expressions are obtained:

$$\begin{aligned} V_{C_1} = V_{C_2} = V_{C_4} &= \frac{D}{(1-4D+D^2)} \cdot V_{in} \\ V_{C_3} &= \frac{1-2D}{(1-4D+D^2)} \cdot V_{in} \\ V_{C_5} &= \frac{1-3D}{(1-4D+D^2)} \cdot V_{in} \end{aligned} \tag{3.29}$$

From (3.26) and (3.29) the peak DC-link voltage across the inverter legs is obtained as follows:

$$\widehat{V}_{PN} = \frac{1}{(1-4D+D^2)} \cdot V_{in} \tag{3.30}$$

Thus the boost factor for the proposed CA-SLEBqZSI is derived as:

$$B = \frac{\widehat{V}_{PN}}{V_{in}} = \frac{1}{(1-4D+D^2)} \tag{3.31}$$

The peak phase AC output voltage of the CA-SLEBqZSI is expressed as

$$\widehat{v}_m = M \cdot \frac{\widehat{V}_{PN}}{2} = M \cdot B \cdot \frac{V_{in}}{2} = G \cdot \frac{V_{in}}{2} \tag{3.32}$$

For simple boost control $M = (1-D)$, the ac peak gain can be written in terms of the modulation index (M) and boost factor (B)

$$G = M \cdot B = \frac{M}{(M^2+2M-2)} \tag{3.33}$$

In steady-state operation, the total charge exchanged by the capacitors during one complete switching period is zero. This results in a zero average capacitor current over the switching cycle.

Applying the capacitor amp-second balance, we derive:

$$\langle i_C(t)\rangle_T = \begin{cases} -D\cdot(I_{L_2}+I_{L_3}+I_{L_4})+(1-D)\cdot(I_{L_1}-I_{PN})=0 \\ -D\cdot(I_{L_1}+I_{L_2})+(1-D)\cdot(I_{L_3}-I_{PN})=0 \\ -D\cdot(I_{L_1}+I_{L_3}+I_{L_4})+(1-D)\cdot(I_{L_2}-I_{PN})=0 \\ -D\cdot I_{L_3}+(1-D)\cdot(I_{L_4}-I_{L_3})=0 \end{cases} \tag{3.34}$$

Simultaneous solution of the above equations yields:

$$\begin{aligned} I_{L_1}=I_{L_2}=I_{L_4}&=\frac{1-D}{(1-3D-2D^2)}\cdot I_{PN} \\ I_{L_3}&=\frac{(1-D)^2}{(1-3D-2D^2)}\cdot I_{PN} \end{aligned} \tag{3.35}$$

3.4 Design of inductors and capacitors

To ensure the effective functioning of the inverter, it is crucial to appropriately design inductors and capacitors to limit the ripple in inductor currents and capacitor voltages to the desired level. The design methodology is based on the assumption that both the capacitor voltages and inductor currents exhibit linearity. This assumption holds when the variations in these variables, represented by ripples, are significantly smaller in magnitude than their mean values.

$$k_i=\frac{\Delta I_L}{I_L} \quad and \quad k_v=\frac{\Delta V_C}{V_C} \tag{3.36}$$

where k_i is defined as the ratio of the peak-to-peak inductor current ripple to the average current of the inductor and the factor k_v is defined as the ratio of the peak-to-peak capacitor voltage ripple to the average voltage of capacitor. These factors quantify the extent of the variation or fluctuations in the respective waveforms. By assuming linear behavior of the waveforms, the changes in inductor current (ΔI_L) and capacitor voltage (ΔV_C) can be

expressed as functions of these ripple factors.

$$\Delta I_L = \frac{V_L \cdot \Delta t}{L} \quad and \quad \Delta V_C = \frac{I_C \cdot \Delta t}{C} \tag{3.37}$$

During shoot-through state, using (3.36) in (3.37)

$$L = \frac{V_L \cdot (D \cdot T)}{k_i \cdot I_L} \quad C = \frac{I_C \cdot (D \cdot T)}{k_v \cdot V_C} \tag{3.38}$$

3.4.1 Design of L & C for the proposed DA-SLEBqZSI

In the shoot-through state, inductor currents increase linearly as the capacitors charge the inductors. The voltages across the inductors in the shoot-through state for the proposed DA-SLEBqZSI are expressed as follows:

$$\begin{aligned} V_{L_1} = V_{L_2} &= \frac{(1-D^2)}{(1-3D-2D^2)} \cdot V_{in} \\ V_{L_3} = V_{L_4} &= \frac{(1-D)}{(1-3D-2D^2)} \cdot V_{in} \end{aligned} \tag{3.39}$$

The relationship between the input current (I_{in}) and constant DC-link current (I_{PN}) in the non-shoot-through state for DA-SLEBqZSI is defined as follows:

$$I_{PN} = \frac{I_{in}}{G} = \frac{(1-3D-D^2)}{1-D^2} \cdot I_{in} \tag{3.40}$$

The inductors in the impedance network of the proposed DA-SLEBqZSI can be designed by using (3.38). For inductor L_1

$$L_1 = \frac{V_{L_1} \cdot (D \cdot T)}{k_i \cdot I_{L_1}} \tag{3.41}$$

Replacing the values of V_{L_1} and I_{L_1} from (3.39) and (3.19) in the above equation we get

$$L_1 = \frac{D \cdot V_{in}}{k_i \cdot f_o \cdot I_{PN}} \tag{3.42}$$

Replacing the value of I_{PN} from (3.40) we get

$$L_1 = \frac{D \cdot (1 - D^2) \cdot V_{in}}{k_i \cdot f_o \cdot I_{in} \cdot (1 - 3D - 2D^2)} = K_L \cdot \frac{D \cdot (1 - D^2)}{(1 - 3D - 2D^2)} \tag{3.43}$$

where $K_L = V_{in}/k_i \cdot f_o \cdot I_{in}$, where f_o is the operating frequency, which is twice the switching frequency f_s.

Similarly the inductors L_2, L_3, and L_4 can be calculated as follows

$$L_2 = L_3 = L_4 = K_L \cdot \frac{D \cdot (1 - D^2)}{(1 - 3D - 2D^2)} \tag{3.44}$$

The current through the capacitors in the shoot-through state for the proposed DA-SLEBqZSI are expressed as follows:

$$\begin{aligned} I_{C_1} &= \frac{(3 - 2D - D^2)}{(1 - 3D - 2D^2)} \cdot I_{PN} \\ I_{C_2} &= \frac{(1 - D^2)}{(1 - 3D - 2D^2)} \cdot I_{PN} \\ I_{C_3} &= \frac{2(1 - D^2)}{(1 - 3D - 2D^2)} \cdot I_{PN} \\ I_{C_4} &= \frac{2(1 - D)}{(1 - 3D - 2D^2)} \cdot I_{PN} \end{aligned} \tag{3.45}$$

The capacitors in the impedance network of the proposed DA-SLEBqZSI can be designed by using (3.38).

For capacitor C_1

$$C_1 = \frac{I_{C_1} \cdot (D \cdot T)}{k_v \cdot V_{C_1}} \tag{3.46}$$

Replacing the values of I_{C_1} and V_{C_1} from (3.45) and (3.11) in the above equation we get

$$C_1 = \frac{I_{PN}}{k_v \cdot f_o \cdot V_{in}} \cdot \frac{(3 - 2D - D^2)}{(1 + D)} = K_C \cdot \frac{(3 - 2D - D^2)}{(1 + D)} \tag{3.47}$$

where $K_C = I_{PN}/k_v \cdot f_0 \cdot V_{in}$, where f_0 is the operating frequency, which is twice the switching frequency f_s.

Similarly the capacitors C_2, C_3, and C_4 can be calculated as follows

$$\begin{aligned} C_2 &= K_C \cdot (1-D) \\ C_3 &= K_C \cdot \frac{2D \cdot (1-D)}{(1-2D)} \\ C_4 &= K_C \cdot \frac{2 \cdot (1-D)}{(1+D)} \end{aligned} \tag{3.48}$$

3.4.2 Design of L & C for the proposed CA-SLEBqZSI

The voltages across the inductors in the shoot-through state for the proposed CA-SLEBqZSI are expressed as follows:

$$\begin{aligned} V_{L_1} = V_{L_2} = V_{L_3} &= \frac{(1-D)}{(1-4D+D^2)} \cdot V_{in} \\ V_{L_4} &= \frac{(1-D)^2}{(1-4D+D^2)} \cdot V_{in} \end{aligned} \tag{3.49}$$

The relationship between the input current (I_{in}) and constant DC-link current (I_{PN}) in the non-shoot-through state for DA-SLEBqZSI is defined as follows:

$$I_{PN} = \frac{I_{in}}{G} = \frac{(1-4D+D^2)}{(1-D)} \cdot I_{in} \tag{3.50}$$

The inductors in the impedance network of the proposed CA-SLEBqZSI can be designed by using (3.38).

For inductor L_1

$$L_1 = \frac{V_{L_1} \cdot (D \cdot T)}{k_i \cdot I_{L_1}} \tag{3.51}$$

Replacing the values of V_{L_1} and I_{L_1} from (3.49) and (3.35) in (3.51) we get

$$L_1 = \frac{D \cdot V_{in}}{k_i \cdot f_o \cdot I_{PN}} \tag{3.52}$$

Replacing the value of I_{PN} from (3.50) we get

$$L_1 = \frac{D \cdot (1-D) \cdot V_{in}}{k_i \cdot f_o \cdot I_{in} \cdot (1-4D+D^2)} = K_L \cdot \frac{D \cdot (1-D)}{(1-4D+D^2)} \tag{3.53}$$

where $K_L = V_{in}/k_i \cdot f_o \cdot I_{in}$, where f_o is the operating frequency, which is twice the switching frequency f_s.

Similarly the inductors L_2, L_3, and L_4 can be calculated as follows

$$\begin{aligned} L_2 &= K_L \cdot \frac{D \cdot (1-D)}{(1-4D+D^2)} \\ L_3 &= K_L \cdot \frac{D}{(1-4D+D^2)} \\ L_4 &= K_L \cdot \frac{D \cdot (1-D)^2}{(1-4D+D^2)} \end{aligned} \tag{3.54}$$

The current through the capacitors in the shoot-through state for the proposed CA-SLEBqZSI are expressed as follows:

$$\begin{aligned} I_{C_1} &= \frac{(3-2D-D^2)}{(1-4D+D^2)} \cdot I_{PN} \\ I_{C_2} &= \frac{(1-D)}{(1-4D+D^2)} \cdot I_{PN} \\ I_{C_3} &= \frac{2(1-D)}{(1-4D+D^2)} \cdot I_{PN} \\ I_{C_4} &= \frac{(2-2D-D^2)}{(1-4D+D^2)} \cdot I_{PN} \\ I_{C_5} &= \frac{(1-D^2)}{(1-4D+D^2)} \cdot I_{PN} \end{aligned} \tag{3.55}$$

The capacitors in the impedance network of the proposed DA-SLEBqZSI can be designed by using (3.38). For capacitor C_1

$$C_1 = \frac{I_{C_1} \cdot (D \cdot T)}{k_v \cdot V_{C_1}} \tag{3.56}$$

Replacing the values of I_{C_1} and V_{C_1} from (3.55) and (3.29) in the above (3.56) we get

$$C_1 = \frac{I_{PN}}{k_v \cdot f_o \cdot V_{in}} \cdot (3 - 2D - D^2) = K_C \cdot (3 - 2D - D^2) \tag{3.57}$$

where $K_C = I_{PN}/k_v \cdot f_0 \cdot V_{in}$, where f_0 is the operating frequency, which is twice the switching frequency f_s.

Similarly the capacitors C_2, C_3, C_4, C_5 can be calculated as follows

$$\begin{aligned} C_2 &= K_C \cdot (1 - D) \\ C_3 &= K_C \cdot \frac{2D \cdot (1 - D)}{(1 - 2D)} \\ C_4 &= K_C \cdot (2 - D - D^2) \\ C_5 &= K_C \cdot \frac{D \cdot (1 - D^2)}{(1 - 3D)} \end{aligned} \tag{3.58}$$

3.5 Design examples

To illustrate the design methodology of the proposed SLEBqZSI topologies, consider a power conversion system intended to step up a 60 V DC input to deliver a higher AC output. The unique architecture of the SLEBqZSI allows for single-stage power conversion, effectively combining voltage boosting and DC-AC inversion into one compact and efficient

Table 3.1. Parameters and component values for simulation and experiment of SLEBqZSIs

Parameters	**Values**
Input voltage	V_{in} = 60 V
Shoot-through duty ratio	D = 0.20
Modulation index	M = 0.75
Fundamental frequency	f = 50 Hz
Switching frequency	f_s = 9 kHz
Filter inductor	L_f = 2 mH
Filter capacitor	C_f = 30 μF
Resistive load	R = 20/25 Ω
Inductor current ripple	k_i = 0.20
Capacitor voltage ripple	k_v = 0.05

Table 3.2. Imdedance network inductors and capacitors values for simulation and experiment of SLEBqZSIs

Parameters	**DA-SLEBqZSI**		**CA-SLEBqZSI**	
	Value	ESR	Value	ESR
L_1	1 mH	0.094 Ω	1.5 mH	0.130 Ω
L_2	1 mH	0.094 Ω	1.5 mH	0.130 Ω
L_3	1 mH	0.094 Ω	1 mH	0.094 Ω
L_4	1 mH	0.094 Ω	1 mH	0.094 Ω
C_1	150 μF	0.015 Ω	150 μF	0.015 Ω
C_2	56 μF	0.039 Ω	56 μF	0.039 Ω
C_3	56 μF	0.039 Ω	56 μF	0.039 Ω
C_4	100 μF	0.022 Ω	100 μF	0.022 Ω
C_5	NA	NA	56 μF	0.039 Ω

system. In this design example, both DA-SLEBqZSI and CA-SLEBqZSI configurations operate at a shoot-through duty ratio of 0.2, which provides a substantial boost while ensuring safe operation within the design limits of the components. The detailed specifications of the system, including control parameters and component ratings, are provided in Table 3.1. These parameters serve as the foundation for selecting the appropriate inductors and capacitors used in the impedance networks of each topology. The sizing of passive components is guided by analytical expressions derived from the steady-state and dynamic analysis of the topologies, considering the desired voltage boost, shoot-through duty ratio, and switching frequency. The theoretical component values obtained through these calculations are rounded to the nearest higher standard commercial values, ensuring that the selected components are readily available in the market. This step also accounts for design tolerances, parasitic losses, and operational safety margins under real-world conditions. By adopting commercially available values with sufficient voltage and current ratings, the system ensures both practical viability and reliability in hardware implementation. These finalized values are consistently used across simulation models and experimental setups, ensuring coherence between theoretical design and real-world performance validation. The finalized inductance and capacitance values used for each SLEBqZSI configuration are comprehensively listed in Table 3.2. These component values form the foundation for the experimental verification and simulation studies, which demonstrate the ability of the proposed topologies to deliver high-voltage AC output from a low-voltage DC source with minimal component count and improved conversion efficiency.

3.6 Simulation and experimental results

To validate the theoretical analysis and the mathematical modeling of the proposed SLEBqZSI topologies, comprehensive computer simulations are conducted using the PSCAD simulation environment. These simulations provided a platform to analyze the dynamic and steady-state performance of the proposed inverters under idealized operating conditions. Specifically, the simulations assumed ideal components, neglecting all forms of parasitic resistance associated with the impedance network inductors, capacitors, and filter elements. However, in order to maintain a realistic approximation of the switching behavior, conduction losses due to the on-state voltage drops of the semiconductor devices, including switches and diodes are included in the simulation model.

To further substantiate the simulation results, hardware prototypes of both the DA-SLEBqZSI and CA-SLEBqZSI topologies are fabricated. The detailed view of the experimental setup is presented in Fig. 3.11. while the printed circuit board (PCB) of these prototypes is illustrated in Fig. 3.10. The experimental implementation utilized high-performance switching devices. Each inverter leg employed STMicroelectronics STGWA40S120DF3 IGBTs, known for their high voltage and current handling capability. The impedance networks are equipped with onsemi RURG8060 ultrafast recovery diodes, characterized by a maximum forward voltage drop of V_F = 1.6 V. These diodes are selected to support fast switching and reduce power losses in the high-frequency impedance network paths.

A TMS320F28335 digital signal processor (DSP) experiment kit [80] is employed for pulse generation [81] using simple-boost control technique. This digital signal processor provided the required flexibility and precision in generating PWM signals, including the shoot-through switching logic necessary to operate SLEBqZSIs. This integrated approach, combining simulation, hardware prototyping, and empirical tuning, provides a strong foundation for assessing the effectiveness of the proposed SLEBqZSI topologies in achieving enhanced voltage-boosting performance and operational reliability under both ideal and practical constraints.

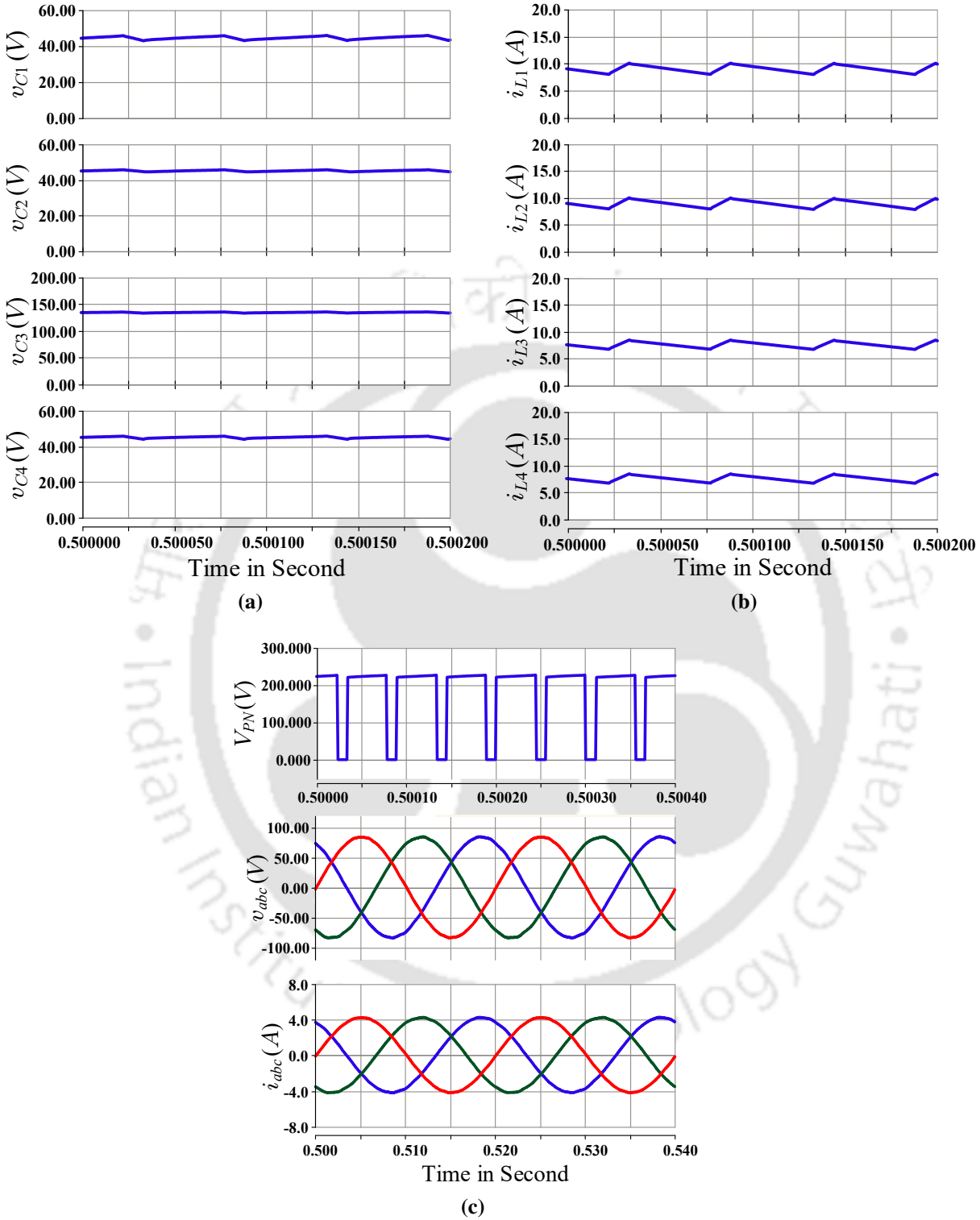


Fig. 3.7. Simulation results of the DA-SLEBqZSI (a) capacitor voltages, (b) inductor currents, and (c) three phase voltages, currents, and DC-link voltage.

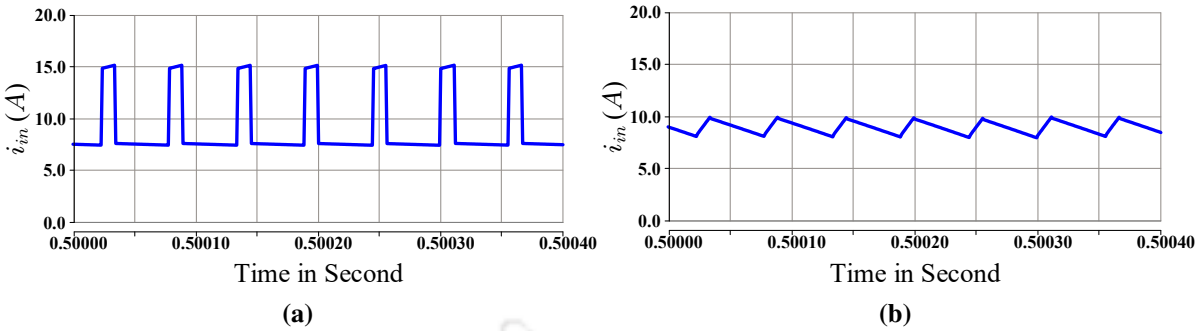


Fig. 3.8. Simulation results of the input current (a) DA-SLEBqZSI and (b) CA-SLEBqZSI.

3.6.1 Simulation results of DA-SLEBqZSI

Analytical calculations and detailed computer simulations are conducted to validate the performance of the proposed DA-SLEBqZSI. The system is fed with an input DC voltage of 60 V. The shoot-through duty ratio D is 0.2, and a modulation index M of 0.75 is used for inverter control. Based on these values, the boost factor B is calculated using (3.15) as 3.75, indicating that the voltage at the inverter bridge could be significantly amplified compared to the input. Subsequently, the voltage gain G, which defines the ratio of peak AC output voltage to input DC voltage, is determined as 2.8125 using (3.17). Using (3.14), the peak DC-link voltage $\widehat{V}_{PN}$, i.e., the voltage appearing across the inverter legs is calculated as 225 V. This value ensures a sufficiently high ac output voltage when processed through the modulation strategy. The steady-state voltages across the impedance network capacitors are also analytically derived using (3.12) and (3.13). The calculated capacitor voltages are V_{C_1} = 45 V, V_{C_2} = 45 V, V_{C_3} = 135 V, and V_{C_4} = 45 V, consistent with the expected distribution of voltages across the capacitive elements in the proposed DA-SLEBqZSI topology. The peak phase AC voltage $\widehat{v}_m$, derived based on the calculated DC-link voltage and modulation index, is 84.375 V. For a purely resistive load of 20 Ω, the corresponding peak phase AC current $\widehat{i}_m$ is calculated as 4.219 A.

A subsequent simulation of the DA-SLEBqZSI model is performed in Power Systems Computer Aided Design (PSCAD) software to observe practical behavior under idealized conditions. The simulation results exhibited slight deviations from the calculated values due

to modeling simplifications and switching dynamics. The average capacitor voltages obtained through simulation are V_{C_1} = 44.5 V, V_{C_2} = 44.5 V, V_{C_3} = 134.0 V, and V_{C_4} = 44.5 V shown in Fig. 3.7. (a). These results closely match theoretical predictions, confirming the consistency of the design. The inductor current waveforms, illustrated in Fig. 3.7. (b), revealed average currents $I_{L_1} = I_{L_2}$ = 9.0 A and $I_{L_3} = I_{L_4}$ = 7.5 A. Further, simulation results shown in Fig. 3.7. (c) indicated a peak DC-link voltage $\widehat{V}_{PN}$ = 223 V, a peak AC voltage $\widehat{v}_m$ = 83.6 V , and a peak AC current $\widehat{i}_m$ = 4.15 A. These values align well with the analytical predictions and confirm the effectiveness of the inverter control strategy. The input current waveform is shown in Fig. 3.8. (a), which demonstrates stable and continuous current behavior, further verifying the proper operation of the switched inductor network in energy transfer and voltage boosting.

3.6.2 Simulation results of CA-SLEBqZSI

To further validate the performance and operational characteristics of the CA-SLEBqZSI, simulations are conducted using the same input parameters as in the DA-SLEBqZSI case. The theoretical performance metrics are first derived using relevant expressions with an input DC voltage of 60 V, a shoot-through duty ratio of D = 0.2, and a modulation index M = 0.75. Based on (3.31), the boost factor B for CA-SLEBqZSI is calculated to be 4.1667, indicating a significant enhancement in the effective voltage across the inverter bridge compared to the source input. Using (3.33), the voltage gain G, defined as the ratio of peak ac output voltage to the input DC voltage, is computed to be 3.125, higher than that of the DA-SLEBqZSI for the same operating point. From (3.30), the corresponding peak DC-link voltage $\widehat{V}_{PN}$ is estimated to be 250 V. The steady-state voltages across the capacitors in the impedance network are evaluated using (3.29). The calculated values are V_{C_1} = 50 V, V_{C_2} = 50 V, V_{C_3} = 150 V, V_{C_4} = 50 V, and V_{C_5} = 100 V. These values indicate a well-distributed voltage profile within the impedance network, contributing to efficient voltage boosting and power flow continuity. From these values, the peak AC phase voltage $\widehat{v}_m$ is calculated as 93.75 V, and for a purely resistive load of 25 Ω, the resulting peak AC $\widehat{i}_m$ is computed to be 3.75 A.

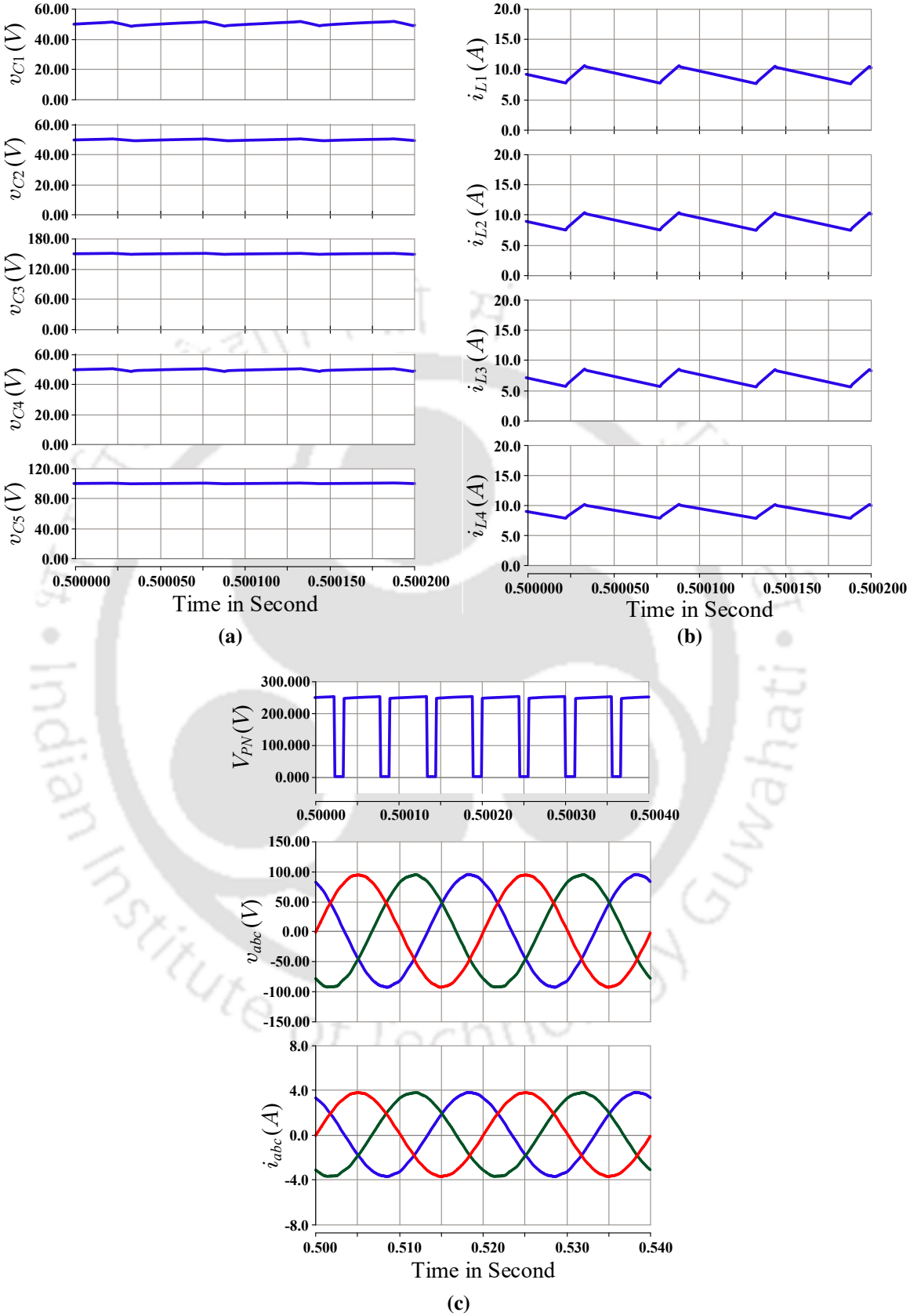


Fig. 3.9. Simulation results of the CA-SLEBqZSI (a) capacitor voltages, (b) inductor currents, and (c) three phase voltages, currents, and DC-link voltage.

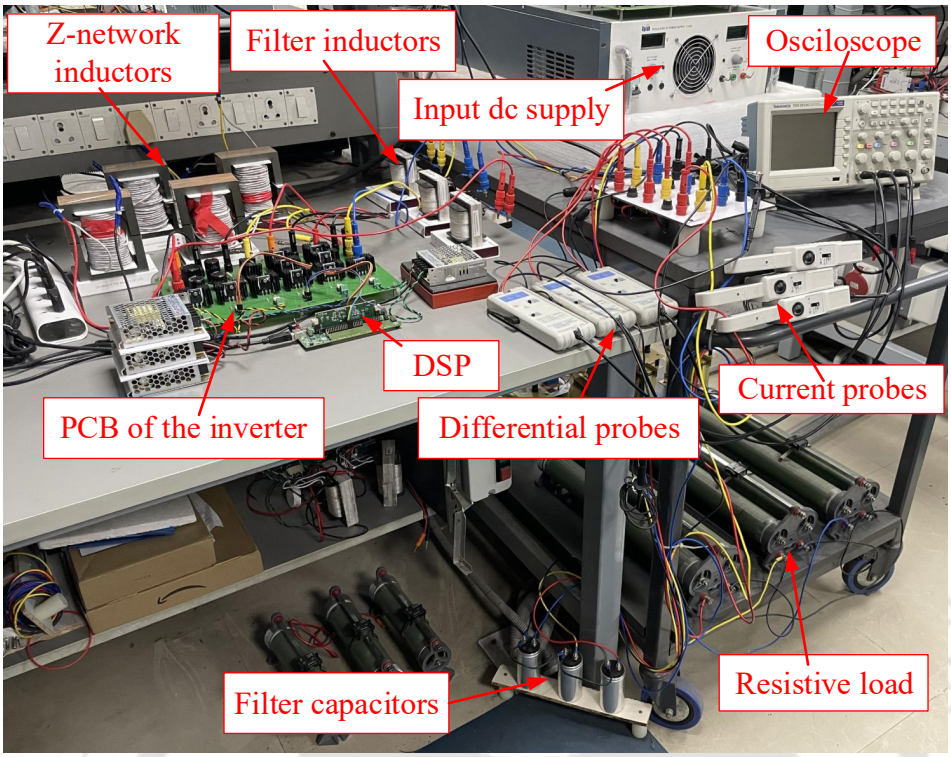


Fig. 3.10. The experimental setup of SLEBqZSIs.

Computer simulations of the CA-SLEBqZSI are carried out under idealized conditions to compare theoretical predictions with practical behavior. The simulated capacitor voltages showed slight deviations from analytical results due to dynamic effects and numerical ap-

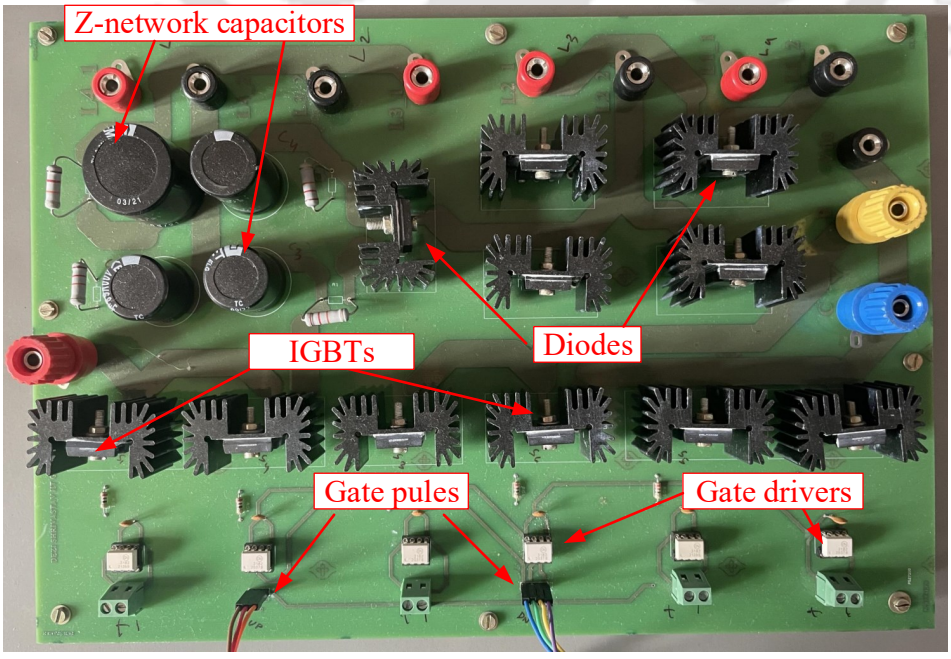
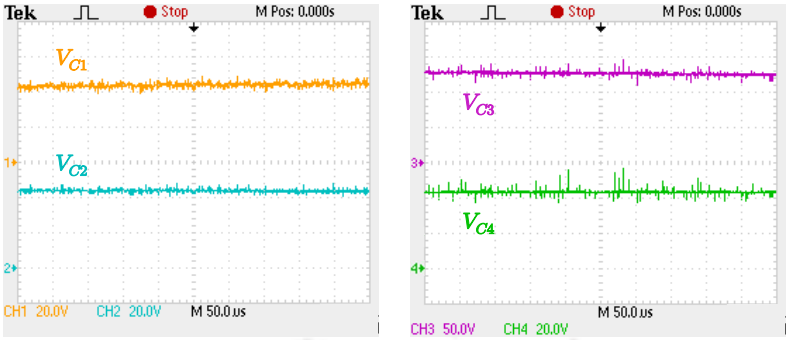


Fig. 3.11. The printed circuit board of SLEBqZSIs.

proximations in the model. As depicted in Fig. 3.9. (a), the average capacitor voltages are: V_{C_1} = 49.4 V, V_{C_2} = 49.4 V, V_{C_3} = 149.2 V, V_{C_4} = 49.4 V, and V_{C_5} = 99.3 V. These variations are within expected limits and validate the robustness of the analytical derivation. The inductor current profiles, shown in Fig. 3.9. (b), revealed that the average inductor currents are: $I_{L1} = I_{L_2}$ = 9.0 A, I_{L_3} = 7.0 A, and I_{L_4} = 9.0 A. The DC-link voltage and three-phase output AC waveforms from the simulation are presented in Fig. 3.9. (c). The peak simulated values observed are $\widehat{V}_{PN}$ = 248 V, $\widehat{v}_m$ = 92.9 V, and $\widehat{i}_m$ = 3.7 A. These values closely match the theoretical predictions, further confirming the accuracy of the analytical model and the effectiveness of the CA-SLEBqZSI design. Finally, the input current waveform is captured and is illustrated in Fig. 3.8. (b), demonstrating stable input behavior and continuous energy intake from the DC source under the switching pattern and load conditions. This validates the robost design of the impedance network in maintaining consistent power transfer.

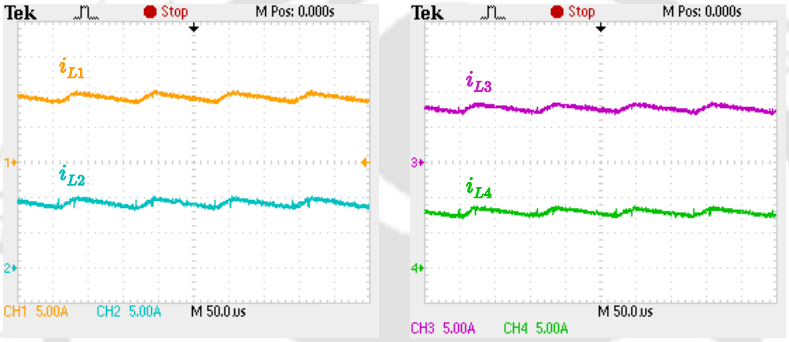
3.6.3 Experimental results of DA-SLEBqZSI

The experimental results for both the DA-SLEBqZSI and CA-SLEBqZSI are acquired using the laboratory prototype depicted in Fig. 3.11. The specifications for the impedance network inductors, capacitors, switches, and diodes, as well as the operating parameters for the system are listed in Table 3.1 and Table 3.2. These experimental tests are designed to validate the theoretical predictions and verify the performance of both topologies under practical operating conditions. For the DA-SLEBqZSI, the experimental results demonstrated slightly lower capacitor voltages than the theoretical values, which is typical due to parasitic effects, switches non-idealities, and practical component tolerances. The measured capacitor voltages are: V_{C_1} = 42.5 V, V_{C_2} = 42.5 V, V_{C_3} = 127.4 V, and V_{C_4} = 42.5 V. These values, shown in Fig. 3.12., illustrate a reasonable match with the theoretical predictions, confirming the ability of the impedance network to maintain desired voltage levels during the switching process. The experimental results for the inductor currents, which are crucial in ensuring proper energy storage and transfer, are $I_{L_1} = I_{L_2}$ = 8.85 A, $I_{L_3} = I_{L_4}$ = 7.40 A. These values, depicted in Fig. 3.13., represent a relatively small deviation from the expected current values, likely due



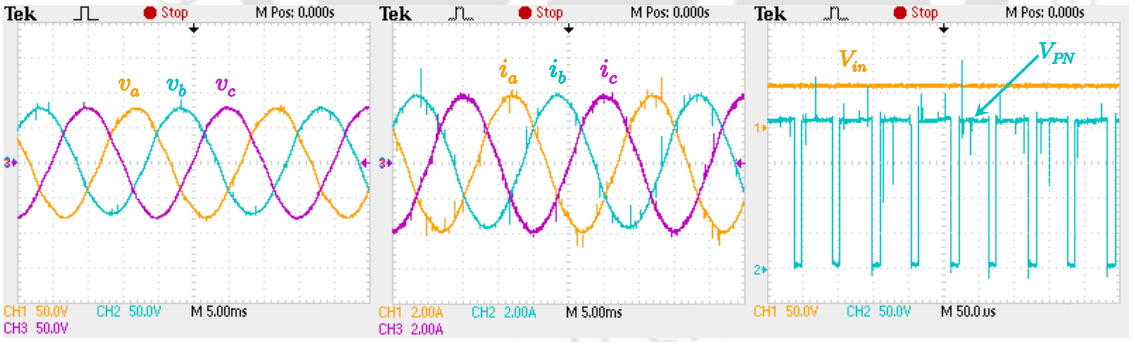
(a) **(b)**

Fig. 3.12. Measured voltages across capacitors (a) C_1 (V_{C_1}) and C_2 (V_{C_2}), (b) C_3 (V_{C_3}), and C_4 (V_{C_4}) of DA-SLEBqZSI.



(a) **(b)**

Fig. 3.13. Measured currents through inductors (a) L_1 (I_{L_1}) and L_2 (I_{L_2}), (b) L_3 (I_{L_3}), and L_4 (I_{L_4}) of DA-SLEBqZSI.

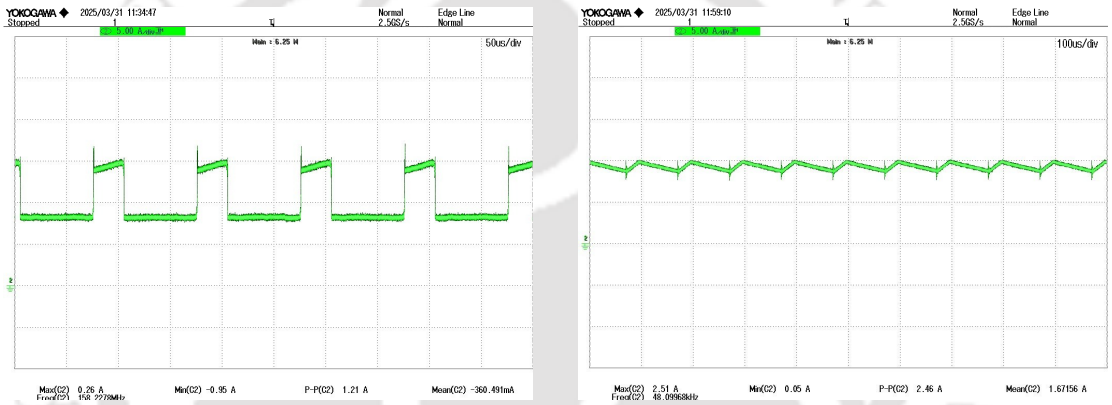


(a) **(b)** **(c)**

Fig. 3.14. Experimental results of the DA-SLEBqZSI (a) three phase voltages, (b) three phase currents, and (c) input voltage and DC-link voltage.

to the parasitic resistance. The DC-link voltage, three-phase AC voltages and currents are measured to assess the overall inverter performance. The measured peak values are $\widehat{V}_{PN}$ = 212.4 V, $\widehat{v}_m$ = 79.6 V, and $\widehat{i}_m$ = 4.0 A. These values, presented in Fig. 3.14., align closely with the theoretical expectations and demonstrate the system's ability to deliver consistent

output under specified load condition. Furthermore, the output AC power is measured at 477.6 W, confirming the system's power conversion capabilities. The inverter efficiency is calculated as 89.46 %, which highlights the effective operation of the DA-SLEBqZSI prototype, particularly in terms of power conversion and minimal losses, ensuring that a substantial portion of the input power is delivered to the load. These experimental results substantiate the theoretical predictions made during the design phase and demonstrate the practical viability of the DA-SLEBqZSI in a laboratory environment, showing its potential for real-world applications.

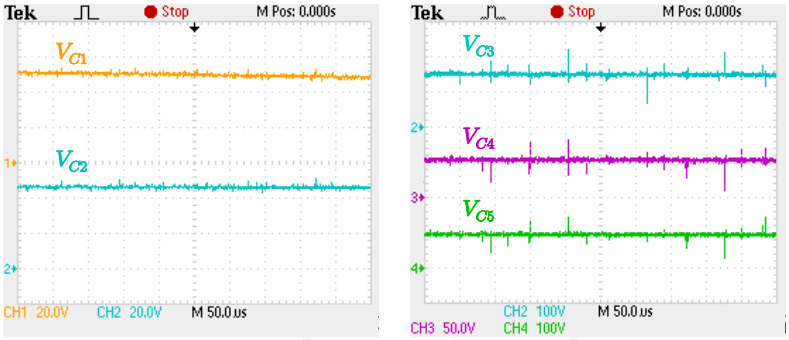


(a) **(b)**

Fig. 3.15. Measured input current (a) DA-SLEBqZSI and (b) CA-SLEBqZSI.

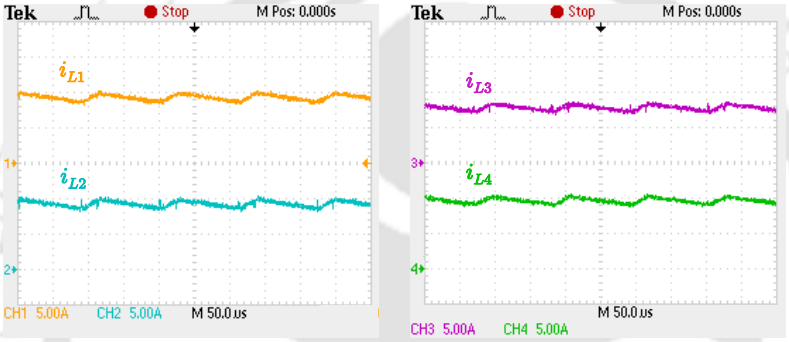
3.6.4 Experimental results of CA-SLEBqZSI

Similarly, for the CA-SLEBqZSI, the experimental results showed capacitor voltages that are slightly different from the theoretical estimates due to practical limitations and parasitic effects, as expected. The measured capacitor voltages are V_{C_1} = 47.5 V, V_{C_2} = 47.5 V, V_{C_3} = 142.5 V, V_{C_4} = 47.5 V, and V_{C_5} = 97.0 V as shown in Fig. 3.16. The experimental results for the inductor currents are depicted in Fig. 3.17. The recorded inductor currents are I_{L_1} = I_{L_2} = 8.7 A, I_{L_3} = 6.87 A, and I_{L_4} = 8.7 A. These measured values are close to the predicted values, showing minor discrepancies likely caused by non-idealities in the inductors. The DC-link voltage, three-phase AC voltages, and currents showed the following peak values $\widehat{V}_{PN}$ = 237.5 V, $\widehat{v}_m$ = 89.0 V, and $\widehat{i}_m$ = 3.56 A. These values, shown in Fig. 3.18., are consistent



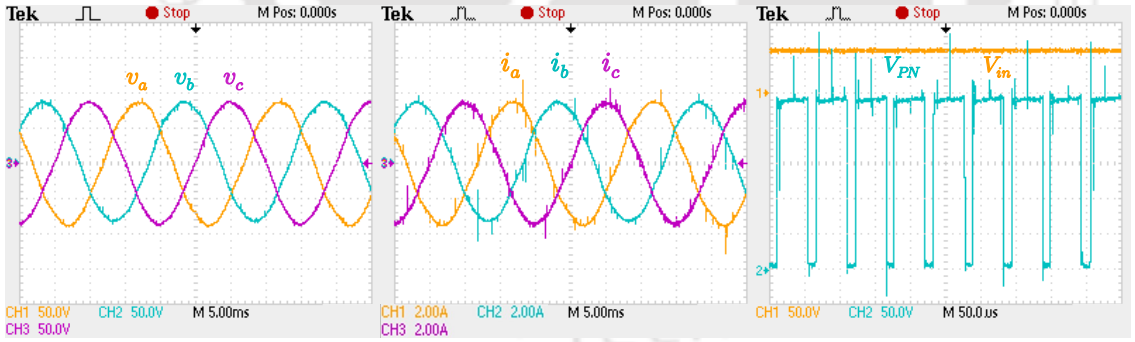
(a) **(b)**

Fig. 3.16. Measured voltages across capacitors (a) C_1 (V_{C_1}) and C_2 (V_{C_2}), (b) C_3 (V_{C_3}), C_4 (V_{C_4}), and C_5 (V_{C_5}) of CA-SLEBqZSI.



(a) **(b)**

Fig. 3.17. Measured currents through inductors (a) L_1 (I_{L_1}) and L_2 (I_{L_2}), (b) L_3 (I_{L_3}) and L_4 (I_{L_4}) of CA-SLEBqZSI.



(a) **(b)** **(c)**

Fig. 3.18. Experimental results of the CA-SLEBqZSI (a) three phase voltages, (b) three phase currents, and (c) input voltage and DC-link voltage.

with the expected performance of the system, demonstrating the effective voltage and current regulation by the inverter. The output AC power generated is 475.26 W, and the inverter efficiency is calculated to be 90.12 %. This high efficiency indicates that the system operates with minimal losses, ensuring that most of the input power is efficiently converted to usable

output power. In comparing the DA-SLEBqZSI and CA-SLEBqZSI, it is observed that the CA-SLEBqZSI exhibited a higher boost factor, as expected, due to its impedance network configuration. Fig. 3.19. presents a comparative analysis of the efficiency of the SLEBqZSIs at

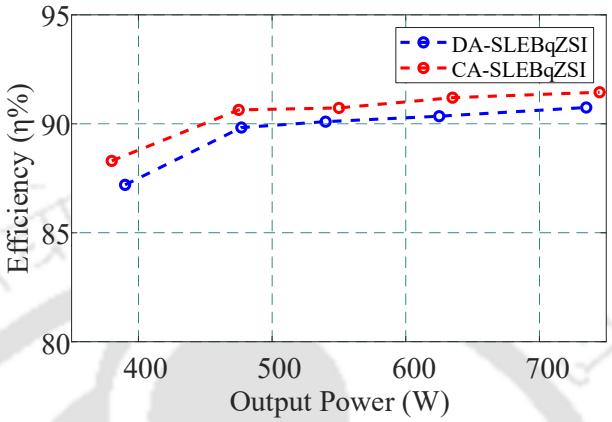


Fig. 3.19. Output power versus efficiency of the proposed SLEBqZSI topologies.

various output power levels. Efficiency is a critical metric in power electronics that represents how effectively input power is converted to useful output power, with higher percentages indicating less energy loss. As the output power increases, the efficiency remains relatively high, confirming the robustness and effectiveness of the system under different operating conditions. However, CA-SLEBqZSI consistently outperforms DA-SLEBqZSI across the entire range of output power. This suggests that the CA-SLEBqZSI topology is more effective in minimizing losses and maintaining energy conversion performance at various load levels. The superior efficiency of DA-SLEBqZSI implies that it is better suited for applications demanding higher performance and lower energy loss, especially in medium to high power conditions. Also, the %THD of the output voltages is well within the desired limits set by the IEEE 519-2022 standard, demonstrating that the system produces high quality power with minimal harmonic distortion. This is a significant achievement, as maintaining low THD is critical for ensuring the reliable operation of power electronics systems in sensitive applications.

3.7 Comparison with different topologies

Table 3.3 presents a comprehensive comparison of the active (switches and diodes) and passive (inductors and capacitors) components used in the proposed DA-SLEBqZSI and CA-SLEBqZSI with other prominent ZSI topologies reported in the literature. This comparative analysis shows that the DA-SLEBqZSI utilizes the same number of components as the enhanced-boost qZSI, highlighting its design efficiency without additional complexity. In contrast, the CA-SLEBqZSI achieves further optimization by reducing the diode count by one while introducing an additional capacitor. This minimal design alteration results in improved performance metrics, demonstrating the advantage of the CA-SLEBqZSI topology.

The evaluation includes critical design and performance parameters such as steady-state capacitor voltage stress, voltage and current stresses on diodes and switches, boost factor, and overall voltage gain. These parameters are benchmarked against several established

Table 3.3. Comparison of the active and passive components of the proposed inverter with the existing inverter topologies.

	Extended-Boost qZSI [31]		SL-ZSI [32]	SL-qZSI [33]	Enhanced-Boost	Proposed SL-EBqZSI	
No. of	DA-EBqZSI	CA-EBqZSI			ZSI/qZSI[34, 35]	DA-SLEBqZSI	CA-SLEBqZSI
Inductors	3	3	4	3	4	4	4
Capacitors	3	4	2	2	4	4	5
Diodes	3	2	7	4	5	5	4
Switches	6	6	6	6	6	6	6

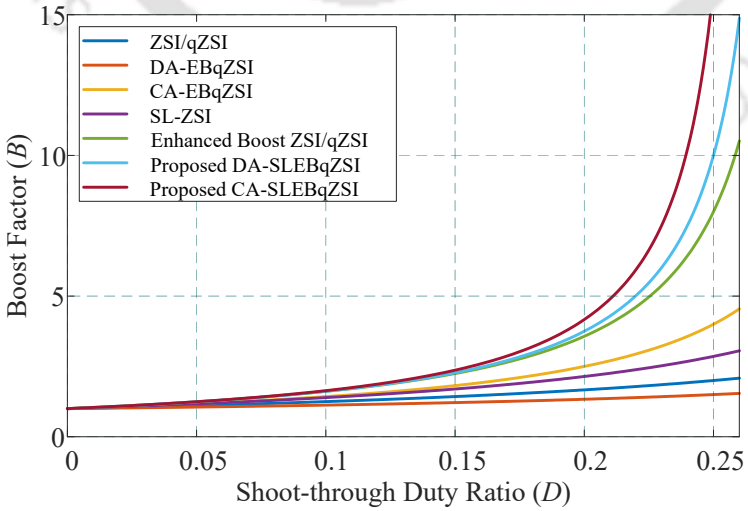


Fig. 3.20. Assessment of the boost factor among various impedance network inverter topologies with the newly proposed topologies.

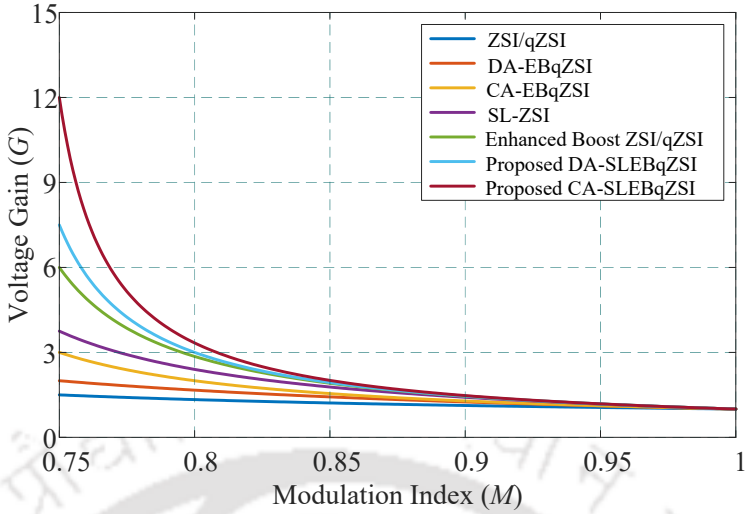


Fig. 3.21. Comparative evaluation of the voltage gain of different impedance network inverter topologies with the newly proposed topologies.

inverter topologies, including extended-boost qZSI, SL-ZSI, SL-qZSI, enhanced-boost ZSI, and enhanced-boost qZSI. A detail of this comparison is presented in Table 3.4.

Several figures are referenced to interpret the performance trends visually. Fig. 3.20. plots the shoot-through duty ratio against the boost factor for various inverter topologies. This plot shows that both proposed SLEBqZSIs achieve higher boost factors for a given duty ratio compared to other impedance-source inverters. Fig. 3.21. illustrates the modulation index versus voltage gain, where the proposed topologies again show superior gain capabilities,

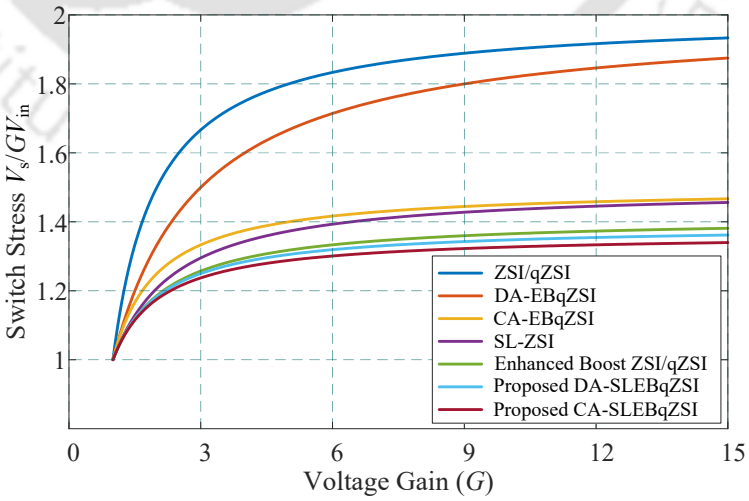


Fig. 3.22. Comparison of switch stress of various impedance network inverter topologies with the newly proposed topology.

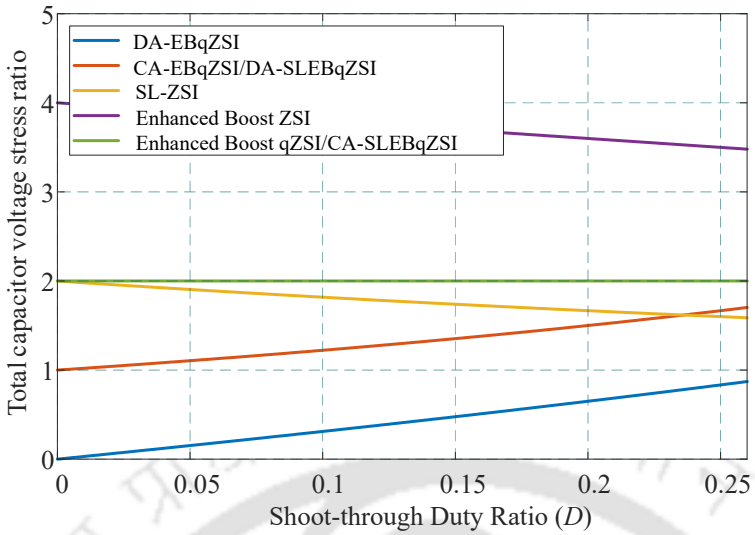


Fig. 3.23. Performance comparison of the total capacitor voltage stress of different impedance network inverter topologies with the newly proposed topologies.

particularly for the CA-SLEBqZSI, which offers the highest voltage gain among all compared designs. Fig. 3.22. compares the semiconductor switch voltage stress across different inverter topologies. A key observation from this figure is that the proposed DA and CA variants of the SLEBqZSI significantly reduce the voltage stress on the switches compared to traditional designs like ZSI, DA/CA-qZSI, SL-ZSI, and enhanced-boost ZSI/qZSI. This reduction in stress improves system reliability and extends the lifetime of the switching devices. The total capacitor voltage stress, defined by the ratio $\Sigma V_c/(B \cdot V_{in})$, is plotted in Fig. 3.23. This

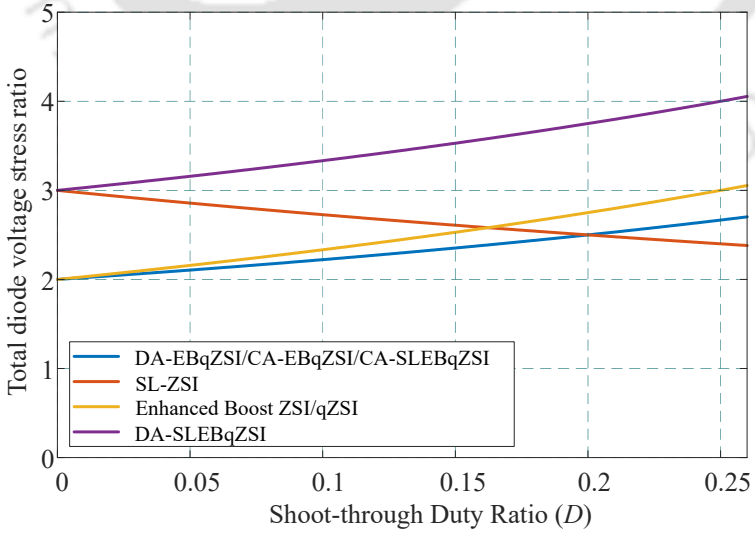


Fig. 3.24. Performance comparison of the total diode voltage stress of different impedance network inverter topologies with the newly proposed topologies.

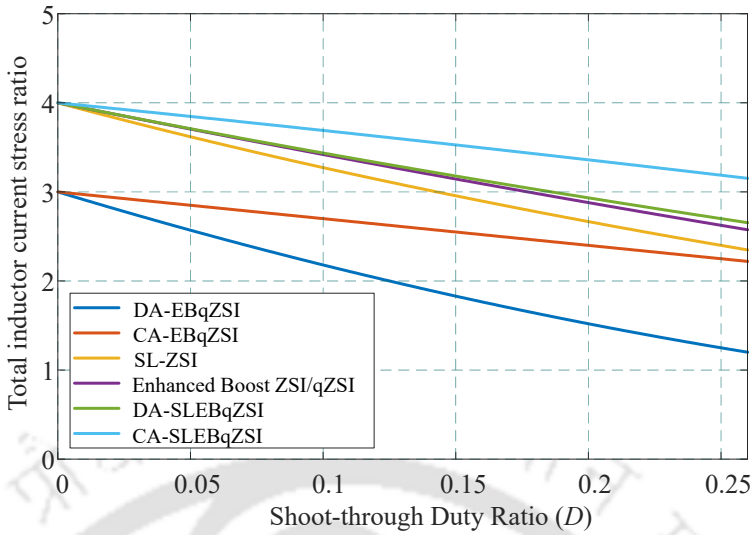


Fig. 3.25. Performance comparison of the total inductor current stress of different impedance network inverter topologies with the newly proposed topologies.

metric is crucial for evaluating the energy handling and voltage balancing requirements of the capacitors in the network. Both proposed topologies demonstrate lower total capacitor voltage stress than the enhanced-boost ZSI, indicating reduced voltage ratings for capacitors and potentially lowering the cost and size of passive components. Similarly, Fig. 3.24. plots the total diode voltage stress versus the shoot-through duty ratio, using the ratio $\Sigma V_d/(B \cdot V_{in})$. This analysis reveals that the CA-SLEBqZSI has significantly lower diode voltage stress at higher shoot-through duty ratios compared to other designs, making it more robust and efficient in high-duty applications. The inductor current stress is another critical factor, and its variation with shoot-through duty ratio is depicted in Fig. 3.25. The total inductor current stress is quantified by the ratio $\Sigma I_L/(B \cdot I_{PN})$. The results indicate that the current stress for all ZSI topologies generally decreases with an increase in the shoot-through duty ratio. Among them, the DA-SLEBqZSI shows a balanced current stress level while maintaining the same number of components as the enhanced-boost ZSI/qZSI, yet delivering a higher boost factor under equivalent conditions. The comparative study highlights the DA-SLEBqZSI and CA-SLEBqZSI as highly efficient, compact, and high-performance alternatives to conventional ZSI topologies. The CA-SLEBqZSI, in particular, stands out for achieving the highest boost factor and voltage gain among all compared inverters while requiring only a minor modification.

Table 3.4. Comparison of capacitor voltages, diode stress, switch stress, boost factor, voltage gain of the proposed inverter with the existing inverter topologies.

Parameters	**SL-ZSI [32]**	**SL-qZSI [33]**	**Enhanced-Boost ZSI [34]**	**Enhanced-Boost qZSI [35]**	**Proposed SL-EBqZSI**	
					DA-SLEBqZSI	**CA-SLEBqZSI**
C_1	$\frac{1-D}{1-3D}V_{in}$	$\frac{1-D}{1-2D-D^2}V_{in}$	$\frac{(1-D)^2}{1-4D+2D^2}V_{in}$	$\frac{(1-D)^2}{1-4D+2D^2}V_{in}$	$\frac{D(1+D)}{(1-3D-2D^2)}V_{in}$	$\frac{1-2D}{1-4D+D^2}V_{in}$
C_2	$\frac{1-D}{1-3D}V_{in}$	$\frac{2D}{1-2D-D^2}V_{in}$	$\frac{(1-D)^2}{1-4D+2D^2}V_{in}$	$\frac{D-D^2}{1-4D+2D^2}V_{in}$	$\frac{D(1+D)}{(1-3D-2D^2)}V_{in}$	$\frac{D}{1-4D+D^2}V_{in}$
C_3	NA	NA	$\frac{(1-D)}{1-4D+2D^2}V_{in}$	$\frac{1-3D+D^2}{1-4D+2D^2}V_{in}$	$\frac{(1-2D)(1+D)}{(1-3D-2D^2)}V_{in}$	$\frac{D}{1-4D+D^2}V_{in}$
C_4	NA	NA	$\frac{(1-D)}{1-4D+2D^2}V_{in}$	$\frac{2D-D^2}{1-4D+2D^2}V_{in}$	$\frac{D(1+D)}{(1-3D-2D^2)}V_{in}$	$\frac{D}{1-4D+D^2}V_{in}$
C_5	NA	NA	NA	NA	NA	$\frac{1-3D}{1-4D+D^2}V_{in}$
D_1/D_2	$\frac{D}{1-3D}V_{in}$	$\frac{D}{1-2D-D^2}V_{in}$	$\frac{(1-D)}{1-4D+2D^2}V_{in}$	$\frac{(1-D)}{1-4D+2D^2}V_{in}$	$\frac{(1+D)}{(1-3D-2D^2)}V_{in}$	$\frac{D}{1-4D+D^2}V_{in}$
D_3/D_6	$\frac{1-D}{1-3D}V_{in}$	$\frac{2(1-D)}{1-2D-D^2}V_{in}$	$\frac{D}{1-4D+2D^2}V_{in}$	$\frac{D}{1-4D+2D^2}V_{in}$	$\frac{(1-D)}{(1-3D-2D^2)}V_{in}$	$\frac{1-D}{1-4D+D^2}V_{in}$
D_4/D_5	$\frac{D}{1-3D}V_{in}$	$\frac{1-3D}{1-2D-D^2}V_{in}$	$\frac{D}{1-4D+2D^2}V_{in}$	$\frac{D}{1-4D+2D^2}V_{in}$	$\frac{D}{(1-3D-2D^2)}V_{in}$	$\frac{1-D}{1-4D+D^2}V_{in}$
Boost Factor	$\frac{1+D}{1-3D}$	$\frac{1+D}{1-2D-D^2}$	$\frac{1}{1-4D+2D^2}$	$\frac{1}{1-4D+2D^2}$	$\frac{1+D}{(1-3D-2D^2)}$	$\frac{1}{1-4D+D^2}$
Voltage Gain	$\frac{M(2-M)}{3M-2}$	$\frac{M(M-2)}{M^2-4M+2}$	$\frac{M}{2M^2-1}$	$\frac{M}{2M^2-1}$	$\frac{M(M-2)}{(2M^2-7M+4)}$	$\frac{M}{(M^2+2M-2)}$
D_{in}/Switch/ DC-link voltage	$\frac{1+D}{1-3D}V_{in}$	$\frac{1+D}{1-2D-D^2}V_{in}$	$\frac{1}{1-4D+2D^2}V_{in}$	$\frac{1}{1-4D+2D^2}V_{in}$	$\frac{1+D}{(1-3D-2D^2)}V_{in}$	$\frac{1}{1-4D+D^2}V_{in}$
Input Current, I_{in}	$2i_{L1}$ - i_{PN}	i_{L3}	$2i_{L3}$ - i_{PN}	i_{L1}	$2i_{L3}$ - i_{PN}	i_{L3}

3.8 Summary

This chapter presents two novel inverter topologies, DA-SLEBqZSI and CA-SLEBqZSI, developed by strategically modifying the impedance network configuration. One of the primary advantages of the proposed DA-SLEBqZSI and CA-SLEBqZSI configurations is their enhanced voltage boost capability, which is achieved even at relatively low shoot-through duty ratios. This characteristic makes them particularly well-suited for applications involving low-input voltage sources, such as PV panels and DG systems, where boosting low voltages is critical. Additionally, the higher boost factor achieved by these inverters allows for operation at a higher modulation index. This results in lower voltage stress across the inverter switches, improving reliability, minimizing switching losses, and allowing low-rated (potentially more cost-effective) semiconductor devices.

The performances of these inverters are evaluated using theoretical analysis, which derives expressions for the boost factor, voltage gain, component stress, and steady-state behavior. Simulation studies are carried out using the PSCAD platform to validate analytical predictions. Experimental validations are done using a hardware prototype to confirm real-world feasibility and performance metrics. The theoretical analysis assumes ideal conditions, i.e., neglecting parasitic resistances, switching losses, and nonlinearities in inductors and capacitors. Nevertheless, these assumptions serve as a solid baseline to derive key performance metrics and design expressions. Among the two proposed topologies, CA-SLEBqZSI exhibits superior performance, offering the highest boost factor and voltage gain among the compared impedance-source inverters. These advantages are achieved with a minimal increase in component count, as the CA-SLEBqZSI requires only one additional capacitor while replacing a diode. This design trade-off results in significantly improved performance without excessive complexity or cost. Their superior boosting performance reduced stress on active components, and high efficiency make them promising candidates for next-generation power electronics interfaces.

This chapter introduces two novel switched-inductor extended-boost qZSI topologies that enhance the boost factor using only passive elements, diodes, inductors, and capacitors

in their impedance networks. Building on this foundation, the next chapter presents an improved extended-boost qZSI topology that further increases the boost factor through additional impedance network modifications. Like the proposed SLEBqZSI configurations, the improved-EBqZSI maintains the advantages of a passive-only design, including compactness, reduced complexity, lower EMI, and improved reliability. The design aims to achieve higher voltage gain without significantly increasing the shoot-through duty cycle, thereby minimizing component stress and preserving system efficiency.

Note: This work, "Switched-Inductor Extended-Boost Quasi-Z-Source Inverter," in *IEEE Access*, DOI: 10.1109/ACCESS.2025.3569076

CHAPTER 4

Improved Extended-Boost Quasi Z-Source Inverter

4.1 Introduction

As discussed in the previous chapter, the gain of ZSIs can be significantly improved by strategically modifying the impedance network. Chapter 2 introduces two novel SLEBqZSI topologies: DA-SLEBqZSI and CA-SLEBqZSI. These topologies are derived from the SL-qZSI and the continuous current configuration of the CA-EBqZSI. These configurations can deliver exceptionally high voltage gains, making them well-suited for power conversion applications with low input voltage. Significant potential remains for enhancing the voltage gain of ZSIs through further modification and optimization of the impedance network. By carefully redesigning the arrangement or topology of the passive components, inductors, capacitors, and diodes, it is possible to achieve higher voltage conversion ratios without increasing the shoot-through duty ratio excessively, which would otherwise lead to greater component stress and reduced efficiency. In particular, novel passive-only networks, which avoid using additional active switches or transformers, are highly interesting due to their compact size, simpler control requirements, lower EMI generation, and increased reliability. By exploring new ways to arrange and interconnect passive components within the impedance network, further improvements in gain can be achieved, making ZSIs more suitable for low-voltage renewable energy sources such as photovoltaics, fuel cells, and battery systems. This chapter introduces a novel improved extended-boost quasi Z-source inverter (imp-EBqZSI) derived from enhanced-boost qZSI. It uses two additional diodes, one inductor, and one capacitor in the impedance network compared to the enhanced-boost qZSI.

The structure of this chapter is organized to provide a comprehensive understanding of the proposed imp-EBqZSI and its performance evaluation. Section 4.2 presents the detailed theoretical analysis of the imp-EBqZSI topology, including its steady-state and dynamic behavior. The governing equations are derived based on the operating modes of the inverter, and expressions for voltage gain, boost factor, and component stresses are established.

Section 4.3 focuses on the design methodology for the passive components, particularly the inductors and capacitors used in the impedance network. The component sizing is carried out using the analytical equations derived in earlier sections, considering key design constraints such as ripple limits, voltage ratings, and switching frequency. The final values are chosen to ensure compatibility with commercially available components and to guarantee robust operation under the desired load conditions. A comprehensive design example is provided in Section 4.4 to demonstrate the practical implementation of the proposed inverter topology. Section 4.6 presents simulation and experimental results, validating the theoretical findings. The simulation results, obtained using PSCAD, highlight the performance of the imp-EBqZSI under various operating conditions. These are followed by experimental results derived from a laboratory prototype, demonstrating the real-world feasibility of the topology and its capability to deliver a high boost at low input voltages. Finally, Section 4.6 provides a comparative analysis of the proposed topology against several existing impedance-source inverter configurations reported in the literature. Key performance metrics such as component count, voltage gain, boost factor, component stress, and efficiency are discussed to highlight the advantages of the imp-EBqZSI.

4.2 Improved extended-boost quasi Z-source inverter

The circuit diagram of the proposed imp-EBqZSI is illustrated in Fig. 4.1. This inverter topology is designed for a single-stage DC-AC power conversion with integrated voltage-boosting capability. The impedance network is positioned between the input DC source (V_{in}) and the three-phase inverter legs. The impedance network of the imp-EBqZSI comprises five inductors L_{1-5}, five capacitors C_{1-5}, and seven diodes D_{1-7}. The three-phase inverter bridge is composed of six switches S_{1-6}, each paired with an anti-parallel diodes D_{1-6}, which together facilitate the inversion of the DC-link voltage to an AC output. The switches and the anti-parallel diode are arranged as $S_1 - S_3 - S_5$ are top switches, and $S_4 - S_6 - S_2$ are bottom stitches. The proposed imp-EBqZSI, similar to the classical ZSI, operates in a shoot-through

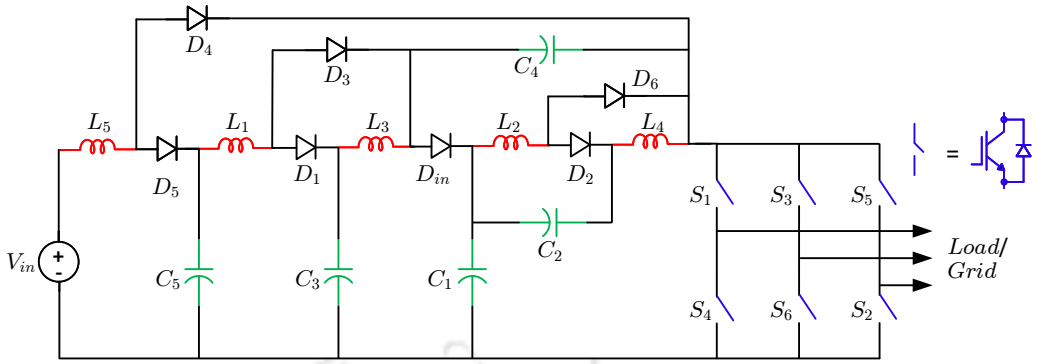


Fig. 4.1. Circuit diagram of imp-EBqZSI.

state, as well as in six active and two zero states. A detailed analysis of the imp-EBqZSI is given in the following sections.

4.2.1 Operating principle of the imp-EBqZSI

Like other ZSIs, the proposed imp-EBqZSI operates in three distinct switching states: shoot-through, active (non-shoot-through), and zero state. Since no power is transferred during the zero state, this study focuses on analyzing the operation of the imp-EBqZSI during the shoot-through and non-shoot-through intervals. For steady-state analysis, the following assumptions are made:

- All components in the circuit are considered ideal, implying no parasitic resistances, non-linearities, or losses.
- The inverter operates in CCM, ensuring that the inductor currents never fall to zero during operation.
- The fundamental output frequency f is significantly lower than the inverter switching frequency f_s.
- During shoot-through intervals, the designated inverter switches are turned ON simultaneously, with no dead-time delays between transitions.

The steady-state voltages across inductors L_1, L_2, L_3, L_4, and L_5 are V_{L_1}, V_{L_2}, V_{L_3}, V_{L_4}, and V_{L_5} respectively, and V_{C_1}, V_{C_2}, V_{C_3}, V_{C_4}, and V_{C_5} are the steady-state voltages across

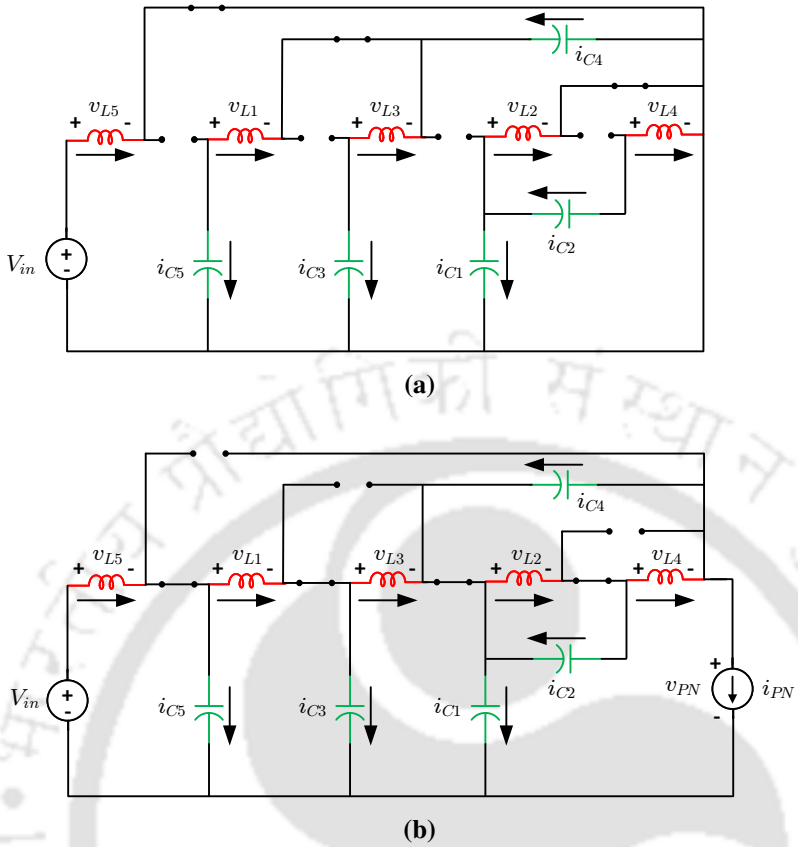


Fig. 4.2. Equivalent circuit of the imp-EBqZSI in (a) shoot-through state and (b) non-shoot-through state.

capacitors C_1, C_2, C_3, C_4, and C_5 respectively. The steady-state currents flowing through the inductors in the proposed imp-EBqZSI are I_{L_1}, I_{L_2}, I_{L_3}, I_{L_4}, and I_{L_5} and those flowing through the capacitors are I_{C_1}, I_{C_2}, I_{C_3}, I_{C_4}, and I_{C_5} respectively. The equivalent circuits of the proposed imp-EBqZSI topology, in shoot-through and non-shoot-through states, are shown in Fig. 4.2. (a) and (b) respectively. These equivalent circuits are fundamental to deriving the operating principles, voltage relationships, and boost characteristics of the proposed topology.

A) Shoot-through state

During the shoot-through interval of duration DT, the simultaneous conduction of the upper and lower switches in one or more inverter legs results in a short circuit across the DC-link. Under this state, the inductors in the impedance network are charged, drawing energy either from the input DC source or the capacitors. Concurrently, the capacitors

discharge, contributing to the energy transfer process and maintaining current continuity. This controlled short-circuit condition is fundamental to the boosting capability of the imp-EBqZSI. The stored energy is released when the inverter transitions out of the shoot-through state, contributing to an elevated DC-link voltage. In the shoot-through state, the diodes D_1, D_2, D_5, and D_{in} are reverse biased and behave as open circuits, preventing current flow through their respective paths, whereas D_3, D_4, and D_6 are forward biased effectively acting as a short circuit. Based on these operating conditions, the voltage across the inductors and the currents through the capacitors during the shoot-through interval can be mathematically expressed as:

$$\begin{aligned} v_{L_1}(t) &= v_{C_4}(t) + v_{C_5}(t) & v_{L_2}(t) &= v_{C_1}(t) \\ v_{L_3}(t) &= v_{C_3}(t) + v_{C_4}(t) & v_{L_4}(t) &= v_{C_1}(t) + v_{C_2}(t) \\ & & v_{L_5}(t) &= V_{in} \end{aligned} \tag{4.1}$$

$$\begin{aligned} i_{C_1}(t) &= -(i_{L_2}(t) + i_{L_4}(t)) & i_{C_2}(t) &= -i_{L_4}(t) \\ i_{C_3}(t) &= -i_{L_3}(t) & i_{C_4}(t) &= -(i_{L_1}(t) + i_{L_3}(t)) \\ & & i_{C_5}(t) &= -i_{L_1}(t) \end{aligned} \tag{4.2}$$

Applying small ripple approximation, the governing equations originally given in (4.1) and (4.2) can be reformulated to simplify the analysis by linearizing the system around the average operating point. The updated expressions become:

$$\begin{aligned} v_{L_1}(t) &= V_{C_4} + V_{C_5} & v_{L_2}(t) &= V_{C_1} \\ v_{L_3}(t) &= V_{C_3} + V_{C_4} & v_{L_4}(t) &= V_{C_1} + V_{C_2} \\ & & v_{L_5}(t) &= V_{in} \end{aligned} \tag{4.3}$$

$$\begin{aligned} i_{C_1}(t) &= -(I_{L_2} + I_{L_4}) & i_{C_2}(t) &= -I_{L_4} \\ i_{C_3}(t) &= -I_{L_3} & i_{C_4}(t) &= -(I_{L_1} + I_{L_3}) \\ & & i_{C_5}(t) &= -I_{L_1} \end{aligned} \tag{4.4}$$

B) Non-shoot-through state

During the non-shoot-through interval, which spans $(1-D)T$, the inverter operates in one of its six possible active states, delivering a constant current I_{PN} to the load. In this phase, the inductors discharge, releasing the energy stored during the shoot-through interval to the load, while the capacitors are recharged to restore their voltage levels. This interval ensures continuous power delivery and maintains the energy balance within the system. The diodes D_1, D_2, D_5, and D_{in} are forward biased, acting as short circuits and permitting current to flow through the corresponding components of the impedance network, and D_3, D_4, and D_6 are reverse biased effectively acting as an open circuit and blocking current flow through its path. Thus, the mathematical equations of the inductor voltages and capacitor currents in the non-shoot-through interval can be written as:

$$\begin{aligned} v_{L_1}(t) &= v_{C_5}(t) - v_{C_3}(t) & v_{L_2}(t) &= -v_{C_2}(t) \\ v_{L_3}(t) &= v_{C_3}(t) - v_{C_1}(t) & v_{L_4}(t) &= v_{C_2}(t) - v_{C_4}(t) \\ v_{L_5}(t) &= V_{in} - v_{C_5}(t) & v_{PN}(t) &= v_{C_1}(t) + v_{C_4}(t) \end{aligned} \tag{4.5}$$

$$\begin{aligned} i_{C_1}(t) &= i_{L_3}(t) - i_{PN}(t) & i_{C_2}(t) &= i_{L_2}(t) - i_{L_4}(t) \\ i_{C_3}(t) &= i_{L_1}(t) - i_{L_3}(t) & i_{C_4}(t) &= i_{L_4}(t) - i_{PN}(t) \\ & & i_{C_5}(t) &= i_{L_5}(t) - i_{L_1}(t) \end{aligned} \tag{4.6}$$

Applying small ripple approximation, the governing equations originally given in (4.5) and (4.6) can be reformulated to simplify the analysis by linearizing the system around the average operating point. The updated expressions become:

$$\begin{aligned} v_{L_1}(t) &= V_{C_5} - V_{C_3} & v_{L_2}(t) &= -V_{C_2} \\ v_{L_3}(t) &= V_{C_3} - V_{C_1} & v_{L_4}(t) &= V_{C_2} - V_{C_4} \\ v_{L_5}(t) &= V_{in} - V_{C_5} & v_{PN}(t) &= V_{C_1} + V_{C_4} \end{aligned} \tag{4.7}$$

$$\begin{aligned} i_{C1}(t) &= I_{L3} - I_{PN} & i_{C2}(t) &= I_{L2} - I_{L4} \\ i_{C3}(t) &= I_{L1} - I_{L3} & i_{C4}(t) &= I_{L4} - I_{PN} \\ & & i_{C5}(t) &= I_{L5} - I_{L1} \end{aligned} \tag{4.8}$$

4.2.2 Steady-state analysis of the imp-EBqZSI

This steady-state analysis offers critical insights into the voltage and current behavior of the proposed imp-EBqZSI topology, facilitating a deeper understanding of its operational performance and effectiveness in achieving a voltage boost. In steady-state conditions, the average voltage across an inductor over a complete switching cycle must be zero by the inductor volt-second balance principle. This principle is foundational in analyzing switching converters and ensures that the magnetic flux within the inductors does not continuously increase or decrease over time. Let "D" represent the shoot-through duty ratio, defined as the ratio of the shoot-through duration to the total switching period, applying inductor volt-sec balance to inductors L_{1-5} using (4.3) and (4.7) we obtain:

$$\langle v_L(t)\rangle_T = \begin{cases} D\cdot(V_{C_4}+V_{C_5})+(1-D)\cdot(V_{C_5}-V_{C_3})=0 \\ D\cdot(V_{C_1})+(1-D)\cdot(-V_{C_2})=0 \\ D\cdot(V_{C_3}+V_{C_4})+(1-D)\cdot(V_{C_3}-V_{C_1})=0 \\ D\cdot(V_{C_1}+V_{C_2})+(1-D)\cdot(V_{C_2}-V_{C_4})=0 \\ D\cdot(V_{in})+(1-D)\cdot(V_{in}-V_{C_5})=0 \end{cases} \tag{4.9}$$

Solving the set of equations in (4.9) simultaneously we obtain:

$$\begin{aligned} V_{C_1} &= \frac{(1-D)}{(1-4D+2D^2)}\cdot V_{in} \\ V_{C_2} &= \frac{D}{(1-D)}\cdot V_{C_1} \\ V_{C_3} &= \frac{(1-3D+D^2)}{(1-D)^2}\cdot V_{C_1} \\ V_{C_4} &= \frac{(2D-D^2)}{(1-D)^2}\cdot V_{C_1} \\ V_{C_5} &= \frac{V_{in}}{(1-D)} \end{aligned} \tag{4.10}$$

By solving equations (4.10) simultaneously, the capacitor voltages can be expressed in terms of the input voltage as follows:

$$\begin{aligned} V_{C_1} &= \frac{(1-D)}{(1-4D+2D^2)} \cdot V_{in} \\ V_{C_2} &= \frac{D}{(1-4D+2D^2)} \cdot V_{in} \\ V_{C_3} &= \frac{(1-3D+D^2)}{(1-4D+2D^2)} \cdot \frac{V_{in}}{(1-D)} \\ V_{C_4} &= \frac{(2D-D^2)}{(1-4D+2D^2)} \cdot \frac{V_{in}}{(1-D)} \\ V_{C_5} &= \frac{V_{in}}{(1-D)} \end{aligned} \tag{4.11}$$

The peak value of DC-link voltage is given by

$$\widehat{V}_{PN} = V_{C_1} + V_{C_4} = \frac{V_{in}}{(1-D)\cdot(1-4D+2D^2)} \tag{4.12}$$

The boost factor of imp-EBqZSI is given by

$$B = \frac{\widehat{V}_{PN}}{V_{in}} = \frac{1}{(1-D)\cdot(1-4D+2D^2)} \tag{4.13}$$

The peak phase AC voltage of the imp-EBqZSI is expressed as

$$\widehat{v}_m = M.\frac{\widehat{V}_{PN}}{2} = M.B.\frac{V_{in}}{2} = G.\frac{V_{in}}{2} \tag{4.14}$$

$$G = \frac{1}{2M^2-1} \tag{4.15}$$

where G is the AC gain of the inverter.

Under steady-state conditions, the net charge exchanged by each capacitor over a complete switching cycle is zero. Consequently, the average current through each capacitor over one period is zero.

Applying the capacitor amp-second balance principle to C_{1-5} using (4.4) and (4.8) we obtain:

$$\langle i_C(t)\rangle_T = \begin{cases} -D\cdot(I_{L_2}+I_{L_4})+(1-D)\cdot(I_{L_3}-I_{PN})=0 \\ -D\cdot I_{L_4}+(1-D)\cdot(I_{L_2}-I_{L_4})=0 \\ -D\cdot I_{L_3}+(1-D)\cdot(I_{L_1}-I_{L_3})=0 \\ -D\cdot(I_{L_1}+I_{L_3})+(1-D)\cdot(I_{L_4}-I_{PN})=0 \\ -D\cdot I_{L_1}+(1-D)\cdot(I_{L_5}-I_{PN})=0 \end{cases} \tag{4.16}$$

Solving (4.16) simultaneously, the derived expressions for inductor currents are as follows:

$$\begin{aligned} I_{L_1} = I_{L_2} &= \frac{(1-D)}{(1-4D+2D^2)}\cdot I_{PN} \\ I_{L_3} = I_{L_4} &= \frac{(1-D)^2}{(1-4D+2D^2)}\cdot I_{PN} \\ I_{L_5} &= \frac{1}{(1-4D+2D^2)}\cdot I_{PN} \end{aligned} \tag{4.17}$$

4.3 Design of inductors and capacitors

Proper design of the inductors and capacitors in the impedance network is essential to ensure stable operation and to limit the ripples in inductor currents and capacitor voltages within acceptable bounds. Excessive ripple can lead to increased EMI, reduced component lifespan, and degraded inverter performance. The ripple components must be carefully constrained during the design phase to mitigate these issues. The design method is based on the assumption that the inductor currents and capacitor voltages vary linearly within a switching period, which is a valid approximation under the condition that their ripple magnitudes are small compared to their average values. This assumption simplifies the analysis and leads to straightforward sizing formulas for the passive components. The ripple

factors for the inductor current and capacitor voltage are defined as:

$$k_i = \frac{\Delta I_L}{I_L} \quad and \quad k_v = \frac{\Delta V_C}{V_C} \tag{4.18}$$

where k_i and k_v are the ripple factor of inductor currents and capacitor voltages, respectively. Assuming linear waveforms over a switching period, the ripple magnitudes ΔI_L and ΔV_C can be calculated using the following relationships:

$$\Delta I_L = \frac{V_L \cdot \Delta t}{L} \quad and \quad \Delta V_C = \frac{I_C \cdot \Delta t}{C} \tag{4.19}$$

During the shoot-through state, the inductor currents in the proposed imp-EBqZSI topology increase linearly as energy is transferred from the capacitors to the inductors. The voltages across the inductors during this interval can be mathematically expressed as follows:

$$\begin{aligned} V_{L_1} = V_{C_4} + V_{C_5} &= \frac{(1-D)}{(1-4D+2D^2)} \cdot V_{in} \\ V_{L_2} = V_{C_1} &= \frac{(1-D)}{(1-4D+2D^2)} \cdot V_{in} \\ V_{L_3} = V_{C_3} + V_{C_4} &= \frac{1}{(1-4D+2D^2)} \cdot V_{in} \\ V_{L_4} = V_{C1} + V_{C_2} &= \frac{1}{(1-4D+2D^2)} \cdot V_{in} \\ V_{L_5} &= V_{in} \end{aligned} \tag{4.20}$$

The relationship between the input current (I_{in}) and the constant DC-link current (I_{PN}) during the non-shoot-through interval is given by the following expression:

$$I_{PN} = \frac{I_{in}}{G} = (1 - 4D + 2D^2) \cdot I_{in} \tag{4.21}$$

The inductors in the impedance network of the proposed imp-EBqZSI can be designed by using (4.19).

For inductor L_1

$$L_1 = \frac{V_{L_1} \cdot (D \cdot T)}{k_i \cdot I_{L_1}} \tag{4.22}$$

Replacing the values of V_{L_1} and I_{L_1} from (4.20) and (4.17) in the above equation we get

$$L_1 = \frac{D \cdot V_{in}}{k_i \cdot f_o \cdot I_{PN}} \tag{4.23}$$

Replacing the value of I_{PN} from (4.21) we get

$$L_1 = K_L \cdot \frac{D}{(1 - 4D + D^2)} \tag{4.24}$$

where $K_L = V_{in}/k_i \cdot f_o \cdot I_{in}$, where f_o is the operating frequency, which is twice the switching frequency f_s. Similarly the inductors L_2, L_3, and L_4 can be calculated as follows

$$\begin{aligned} L_2 &= K_L \cdot \frac{D}{(1 - 4D + D^2)} \\ L_3 = L_4 &= K_L \cdot \frac{D}{(1-D)^2 \cdot (1 - 4D + D^2)} \\ L_5 &= K_L \cdot D \end{aligned} \tag{4.25}$$

The current through the capacitors in the shoot-through state for the proposed imp-EBqZSI are expressed as follows:

$$\begin{aligned} I_{C_1} &= -(I_{L_2} + I_{L_4}) = -\frac{(1-D) \cdot (2-D)}{(1 - 4D + 2D^2)} \cdot I_{PN} \\ I_{C_2} &= -I_{L_4} = -\frac{(1-D)^2}{(1 - 4D + 2D^2)} \cdot I_{PN} \\ I_{C_3} &= -I_{L_3} = -\frac{(1-D)^2}{(1 - 4D + 2D^2)} \cdot I_{PN} \\ I_{C_4} &= -(I_{L_1} + I_{L_3}) = -\frac{(1-D) \cdot (2-D)}{(1 - 4D + 2D^2)} \cdot I_{PN} \\ I_{C_5} &= -I_{L_1} = -\frac{(1-D)}{(1 - 4D + 2D^2)} \cdot I_{PN} \end{aligned} \tag{4.26}$$

The capacitors in the impedance network of the proposed imp-EBqZSI can be designed by using (4.19).

For capacitor C_1

$$C_1 = \frac{I_{C_1} \cdot (D \cdot T)}{k_v \cdot V_{C_1}} \tag{4.27}$$

Replacing the values of I_{C_1} and V_{C_1} from (4.26) and (4.10) in the above equation we get

$$C_1 = \frac{I_{PN}}{k_v \cdot f_o \cdot V_{in}} \cdot D \cdot (2 - D) = K_C \cdot D \cdot (2 - D) \tag{4.28}$$

where $K_C = I_{PN}/k_v \cdot f_0 \cdot V_{in}$, where f_0 is the operating frequency, which is twice the switching frequency f_s.

Similarly the capacitors C_2, C_3, C_4, C_5 can be calculated as follows

$$\begin{aligned} C_2 = C_4 &= K_C \cdot (1 - D)^2 \\ C_3 &= K_C \cdot \frac{D \cdot (1 - D)^3}{(1 - 3D + D^2)} \\ C_5 &= K_C \cdot D \cdot (1 - D^2) \end{aligned} \tag{4.29}$$

4.4 Design example

The design strategy to accurately determine the inductor and capacitor values required for the impedance network of the imp-EBqZSI. The peak-to-peak ripple in the inductor currents is limited to 20% of their nominal values, while the capacitor voltage ripple is constrained to within 1% of the steady-state voltage. These conservative ripple limits ensure low EMI, reduced stress on power components, and improved system reliability over long-term operation. The design calculations are performed using the analytical expressions derived earlier, specifically equations (4.24)-(4.25) and (4.28)-(4.29), which relate the inductor and capacitor values to the input voltage, switching frequency, shoot-through duty ratio, and permissible ripple magnitudes. The fundamental system parameters, including input voltage,

Table 4.1. Parameters and component values for simulation and experiment of imp-EBqZSI

Parameters	**Values**
Input voltage	V_{in} = 56 V
Shoot-through duty ratio	D = 0.20
Modulation index	M = 0.75
Fundamental frequency	f = 50 Hz
Switching frequency	f_s = 9 kHz
Filter inductor	L_f = 2 mH
Filter capacitor	C_f = 30 μF
Resistive load	R = 25 Ω
Inductor current ripple	k_i = 0.20
Capacitor voltage ripple	k_v = 0.01

output power, switching frequency, and shoot-through duty cycle, are drawn from Table 4.1 and used to estimate the passive components. The computed values for the inductors and capacitors are then adjusted to the nearest higher commercially available standard values. This rounding ensures ease of procurement and practical implementation and introduces an added safety margin that accounts for component tolerances, aging effects, and temperature variations during operation. The finalized values are summarized in Table 4.2. Importantly, the selected inductor and capacitor values are consistent with the ripple constraints initially defined and are validated for both simulation and experimental setups. Adhering to these design principles ensures minimal ripple, optimized energy transfer, and stable inverter operation under varying load and input conditions. These carefully selected component values

Table 4.2. Imdedance network inductors and capacitors values for simulation and experiment of imp-EBqZSI

Parameters	**Theoretical**	**Simulation/Experiment**
L_1	1.0 mH	1.0 mH
L_2	1.0 mH	1.0 mH
L_3	1.6 mH	2.0 mH
L_4	1.6 mH	2.0 mH
L_5	290.37 μH	0.5 mH
C_1	107.14 μF	120 μF
C_2	190.48 μF	220 μF
C_3	69.26 μF	100 μF
C_4	190.48 μF	220 μF
C_5	136.05 μF	150 μF

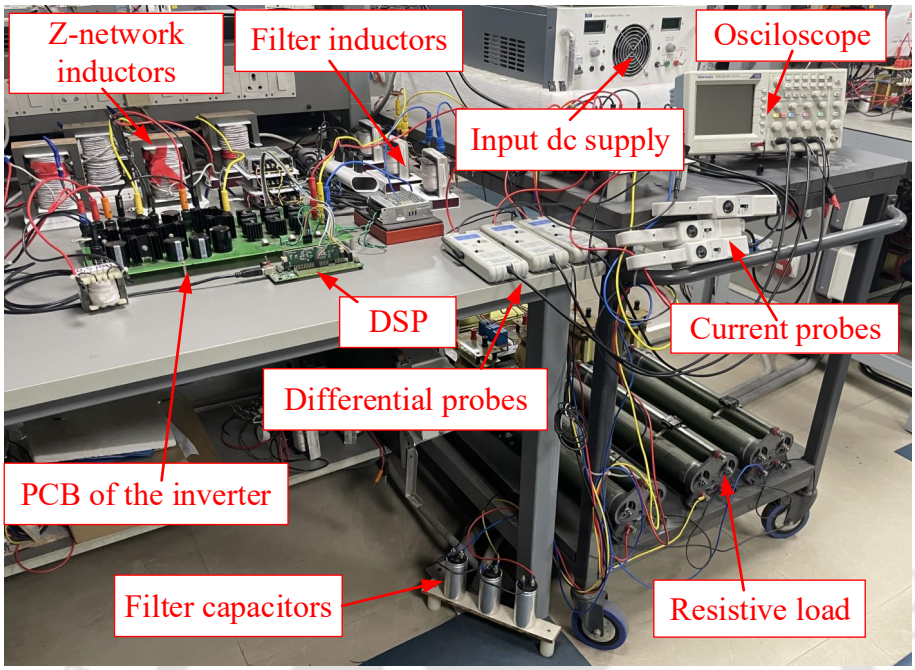


Fig. 4.3. The experimental setup of imp-EBqZSI.

form the foundation for subsequent performance verification through PSCAD simulations and laboratory experiments.

4.5 Simulation and experimental results

To validate the theoretical analysis and mathematical modeling of the proposed imp-EBqZSI topology, comprehensive simulations are performed using the PSCAD simulation platform. These simulations enabled an in-depth evaluation of the dynamic and steady-state

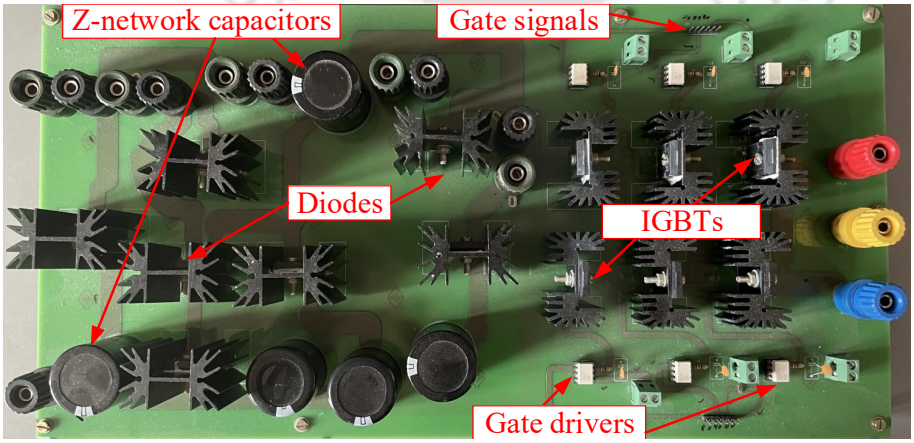


Fig. 4.4. The printed circuit board of imp-EBqZSI.

behavior of the imp-EBqZSI topology under controlled idealized conditions. The simulation environment modeled the power electronic system using ideal passive components, with all parasitic resistances of the inductors, capacitors, and filter elements deliberately ignored to isolate the core functional characteristics of the topologies. However, to maintain a degree of realism and ensure that switching dynamics are accurately captured, conduction losses from semiconductor devices, namely the on-state voltage drops of switches and diodes, are incorporated into the simulation model.

To reinforce the credibility of the simulation results, an experimental hardware prototype of imp-EBqZSI topology is constructed. The complete view of the experimental test bench is depicted in Fig. 4.3., while the physical layout of the fabricated PCB is shown in Fig. 4.4. Each inverter leg employed STMicroelectronics STGWA40S120DF3 IGBT modules for the power stage, which offer high voltage and current ratings suited for rigorous power conversion applications. The impedance networks incorporated RURG8060 ultrafast recovery diodes from onsemi, selected for their rapid switching capabilities and robust thermal characteristics. These diodes exhibit a forward voltage drop of approximately $V_F = 1.6$ V, contributing to reduced switching losses in high-frequency operation scenarios. A TMS320F28335 DSP development board is used for simple-boost control and pulse-width modulation (PWM) generation. This high-performance digital signal processor enabled precise control over shoot-through states, ensuring that the timing and coordination of PWM pulses are consistent. The combination of simulation studies, hardware implementation, and real-time DSP-based control establishes a rigorous validation framework. This multi-faceted approach confirms the viability and high performance of the proposed imp-EBqZSI topology in delivering enhanced voltage boosting and reliable power conversion under ideal and real-world operating conditions.

4.5.1 Simulation results of the imp-EBqZSI

To demonstrate the validity of the analytical design and steady-state performance of the imp-EBqZSI, a detailed case study is presented with an input DC voltage of 56 V. With

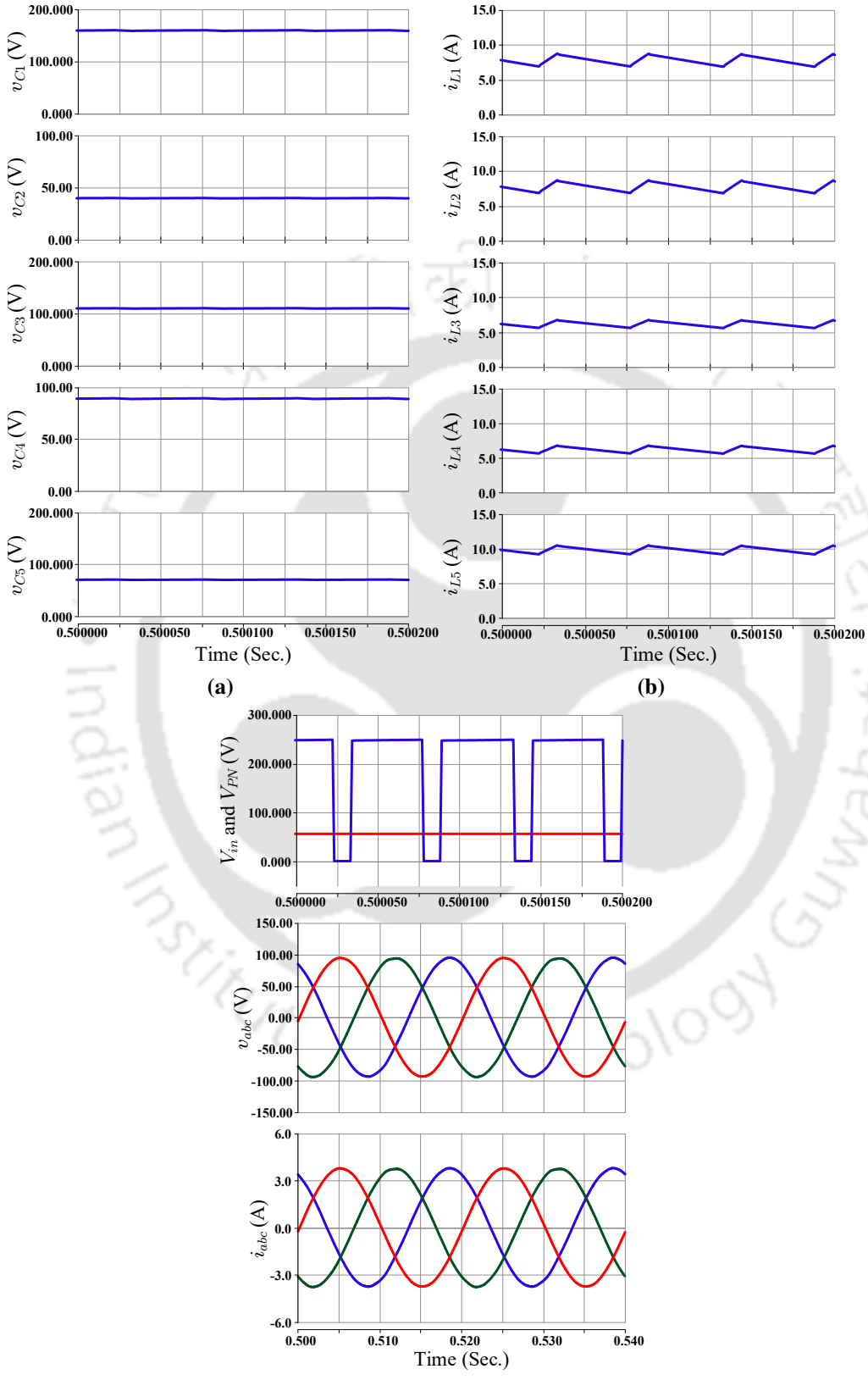


Fig. 4.5. Simulation results of the imp-EBqZSI (a) capacitor voltages and (b) inductor currents. (c) three phase voltages, currents, input voltage, and DC-link voltage.

simple-boost control technique, the inverter operates with a shoot-through duty ratio D = 0.2 and a modulation index M = 0.75. Using the theoretical expressions defined in (4.13), the boost factor B is calculated as 4.4643, indicating a significant voltage boost capability. Correspondingly, the voltage gain G is determined to be 3.5715 from (4.15), reflecting the combined effect of the boost network and modulation strategy. From (4.12), the peak DC-link voltage $\widehat{V}_{PN}$ is computed to be 250 V, which serves as the reference voltage for the modulation process. Applying the capacitor voltage expressions derived in (4.11), the calculated steady-state capacitor voltages are as follows: V_{C_1} = 160 V, V_{C_2} = 40 V, V_{C_3} = 110 V, V_{C_4} = 90 V, and V_{C_5} = 70 V. The average inductor currents are estimated from (4.17) as I_{L_1} = I_{L_2} = 8.03 A, I_{L_3} = I_{L_4} = 6.43 A, and I_{L_5} = 10.04 A. Additionally, the peak phase AC voltage $\widehat{v}_m$ at the inverter output is calculated to be 93.75 V. Given a purely resistive load of 25 Ω, the corresponding peak phase AC current $\widehat{i}_m$ is computed as 3.75 A.

Computer simulations are carried out in PSCAD to verify these theoretical results. The simulation results for capacitor voltages closely match the analytical predictions, with slight reductions due to parasitic and dynamic effects modeled in the system. The capacitor voltages are simulated as V_{C_1} = 159.0 V, V_{C_2} = 39.4 V, V_{C_3} = 109.2 V, and V_{C_4} = 89.0 V, V_{C_5} = 69.8 V. These results are illustrated in Fig. 4.5. (a), confirming the correct charge-sharing dynamics within the impedance network. Fig. 4.5. (b) shows the waveforms of the inductor currents, which exhibit average values of I_{L_1} = I_{L_2} = 7.8 A, I_{L_3} = I_{L_4} = 6.2 A, and I_{L_5} = 9.8 A. These currents indicate the adequate energy storage and transfer occurring within the imp-EBqZSI impedance network during the switching cycle. Fig. 4.5. (c) presents the simulation waveforms for the DC-link voltage, three-phase AC voltages, and output currents. The peak values observed in the simulation are $\widehat{V}_{PN}$ = 248 V, $\widehat{v}_m$ = 93.0 V, and $\widehat{i}_m$ = 3.7 A as depicted in Fig. 4.5. (c). These values align with theoretical calculations, with minimal deviations attributed to modeled losses and dynamic responses in the simulation environment.

4.5.2 Experimental results of imp-EBqZSI

The experimental validation of the imp-EBqZSI is conducted using a laboratory prototype, as illustrated in Fig.4.3. Table 4.2 reflect the analytically determined values and the final selections based on standard commercial availability. The capacitor voltage waveforms,

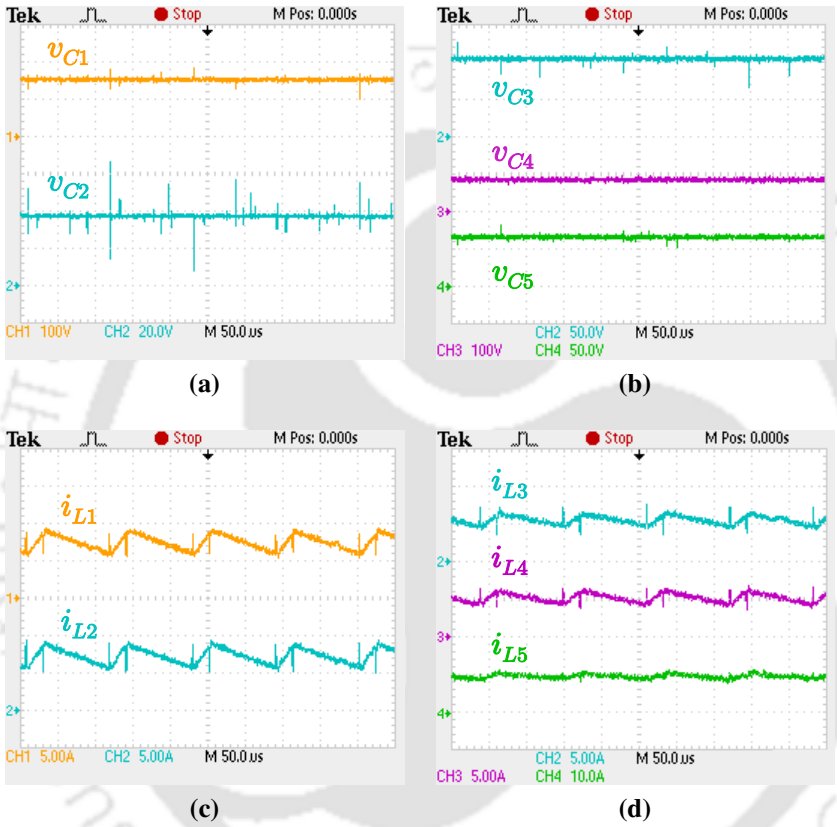


Fig. 4.6. Measured voltage across capacitors (a) C_1 (V_{C_1}) and C_2 (V_{C_2}), (b) C_3 (V_{C_3}), C_4 (V_{C_4}), and C_5 (V_{C_5}) of the imp-EBqZSI. The measured current through inductors (c) L_1 (I_{L_1}) and L_2 (I_{L_2}), (d) L_3 (I_{L_3}), L_4 (I_{L_4}), and L_5 (I_{L_5}) of the imp-EBqZSI.

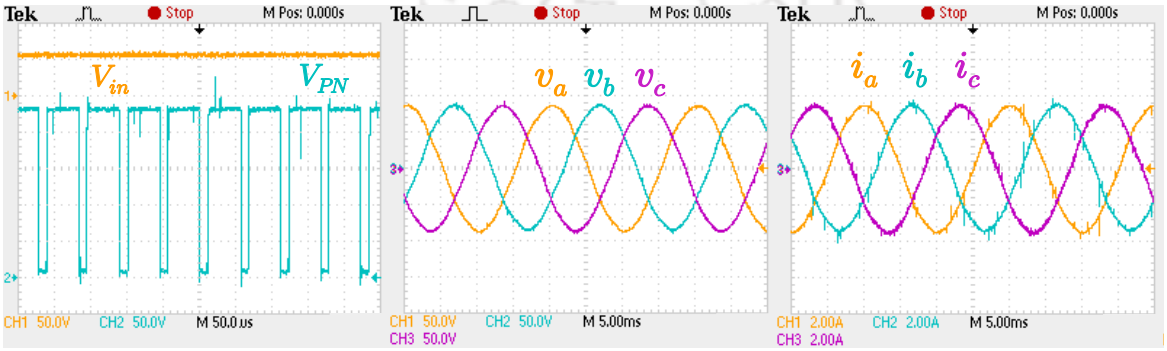


Fig. 4.7. Experimental results of the imp-EBqZSI (a) input voltage and DC-link voltage (b) three phase voltages, and (c) three phase currents.

Table 4.3. Comparison of the active and passive components of the proposed inverter with the existing inverter topologies.

	Extended-Boost qZSI [31]		SL-ZSI [32]	SL-qZSI [33]	Enhanced-Boost	Proposed
	DA-qZSI	CA-qZSI			ZSI/qZSI [34, 35]	imp-EBqZSI
No. of Inductors	3	3	4	3	4	5
No. of Capacitors	3	4	2	2	4	5
No. of Diodes	3	2	7	4	5	7
No. of Switches	6	6	6	6	6	6

captured during steady-state operation, are presented in Figs. 4.6. (a) and (b). The measured voltages across the capacitors are V_{C_1} = 152.0 V, V_{C_2} = 38.4 V, V_{C_3} = 103.8 V, V_{C_4} = 84.0 V, and V_{C_5} = 67.2 V. These values closely align with the simulated and theoretical predictions, albeit with minor deviations. These discrepancies are primarily attributed to non-idealities such as parasitic resistances in inductors and capacitors and voltage drops across switching devices, which are inherent in real hardware but typically idealized in simulation environments. Similarly, the inductor currents measured experimentally are shown in Figs. 4.6. (c) and (d), with average values recorded as $I_{L_1} = I_{L_2}$ = 7.2 A, $I_{L_3} = I_{L_4}$ = 5.8 A, and I_{L_5} = 9.2 A. These currents are consistent with simulated waveforms, validating the current-sharing and energy-storage characteristics of the inductors. The DC-link voltage and three-phase AC output voltages and currents are also experimentally measured and are shown in Fig. 4.7. The observed peak values are $\widehat{V}_{PN}$ = 236.0 V, $\widehat{v}_m$ = 88.0 V, and $\widehat{i}_m$ = 3.52 A. The output AC power delivered to the load is measured to be P_{out} = 464.6 W. Despite the slight reduction in voltage and current magnitudes compared to the simulation attributable to losses, including switching losses, on-state voltage drops, and copper losses in inductors and capacitors, the experimental results strongly support the theoretical analysis and validate the simulation model. The performance consistency across all three domains (theory, simulation, and hardware) demonstrates the practical viability, robustness, and efficiency of the imp-EBqZSI topology under real operating conditions.

4.6 Comparison with different topologies

The comprehensive performance analysis of the proposed imp-EBqZSI encloses several critical parameters, including semiconductor stress on switches, boost factor, and voltage gain. These performance indicators are quantitatively compared with various state-of-the-art ZSI topologies documented in the literature, such as the extended-boost qZSI, SL-ZSI, SL-qZSI, enhanced-boost ZSI, and enhanced-boost qZSI. Table 4.3 presents a detailed breakdown of the active (switches and diodes) and passive (inductors and capacitors) components used across the different topologies. Comparison results are summarized in Table 4.4. To further illustrate the structural and functional distinctions, notably, the imp-EBqZSI achieves a boost factor of 4.4643 with a shoot-through duty ratio of only 0.2. At the same time, the enhanced-boost qZSI requires a higher duty ratio of 0.2177 to attain the same boost level. This demonstrates the greater boost in efficiency of the proposed topology. Moreover, when operating at a shoot-through duty ratio of 0.25, the imp-EBqZSI achieves a 33.33% higher boost factor than the enhanced-boost qZSI, highlighting its superior voltage boosting capability. Fig. 4.8. shows the variation of the boost factor as a function of the shoot-through duty ratio for all compared inverter configurations. Similarly, Fig. 4.9. presents the relationship between modulation index and voltage gain across different ZSIs, further emphasizing the performance advantage

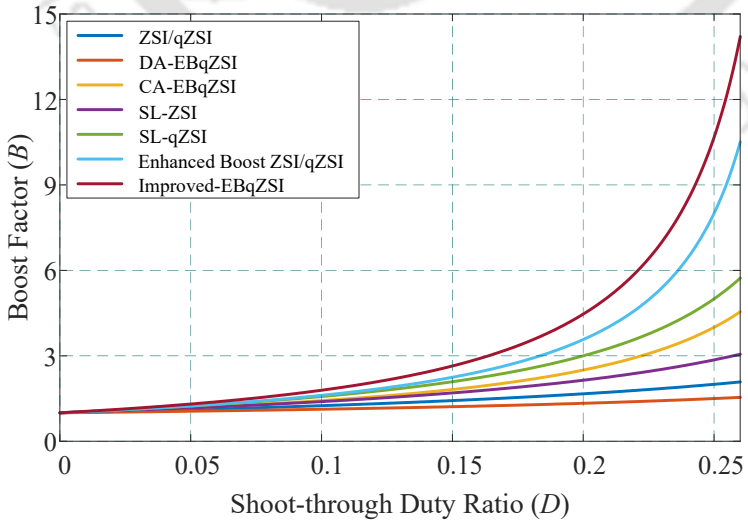


Fig. 4.8. Assessment of the boost factor among various impedance network inverter topologies with the newly proposed topology.

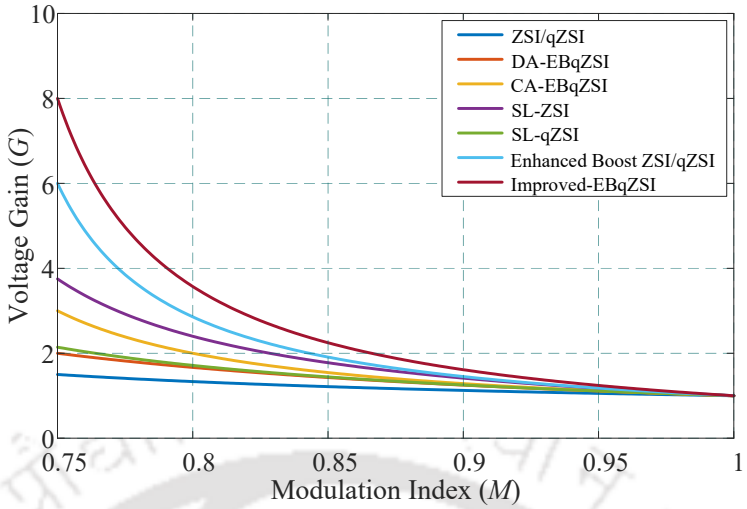


Fig. 4.9. Comparative evaluation of the voltage gain of different impedance network inverter topologies with the newly proposed topology.

of the imp-EBqZSI. A critical metric for inverter reliability is the voltage stress across the inverter-leg switches, defined as the ratio of the peak DC-link voltage (V_{PN}) to the GV_{in}. This stress metric serves as an indicator of the voltage withstand requirement of the semiconductor devices. Fig. 4.10. illustrates the switch stress distribution for the proposed inverter and all other comparator topologies. The proposed imp-EBqZSI exhibits reduced voltage stress on its switches, outperforming traditional ZSI, DA/CA-qZSI, SL-ZSI, and enhanced-boost ZSI and enhanced-boost qZSI topologies.

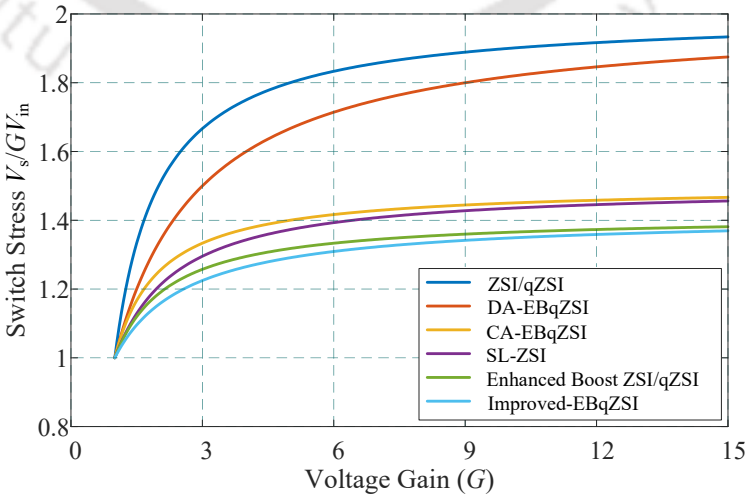


Fig. 4.10. Comparison of switch stress of various impedance network inverter topologies with the newly proposed topology.

Table 4.4. Comparison of capacitor voltages, diode stress, switch stress, boost factor, voltage gain, and DC-link voltage of the proposed inverter with the existing inverter topologies.

	Parameters	Extended-Boost qZSI [31] DA-qZSI	Extended-Boost qZSI [31] CA-qZSI	SL-ZSI [32]	SL-qZSI [33]	Enhanced-Boost ZSI [34]	Enhanced-Boost qZSI [35]	Proposed imp-EBqZSI
CAPACITOR STRESSES	C_1	$\frac{D}{(1-D)(1-2D)}V_{in}$	$\frac{D}{1-3D}V_{in}$	$\frac{1-D}{1-3D}V_{in}$	$\frac{1-D}{1-2D-D^2}V_{in}$	$\frac{(1-D)^2}{1-4D+2D^2}V_{in}$	$\frac{(1-D)^2}{1-4D+2D^2}V_{in}$	$\frac{1-D}{1-4D+2D^2}V_{in}$
	C_2	$\frac{D}{(1-D)(1-2D)}V_{in}$	$\frac{D}{1-3D}V_{in}$	$\frac{1-D}{1-3D}V_{in}$	$\frac{2D}{1-2D-D^2}V_{in}$	$\frac{(1-D)^2}{1-4D+2D^2}V_{in}$	$\frac{D-D^2}{1-4D+2D^2}V_{in}$	$\frac{D}{1-4D+2D^2}V_{in}$
	C_3	$\frac{D}{1-D}V_{in}$	$\frac{1-2D}{1-3D}V_{in}$	NA	NA	$\frac{(1-D)}{1-4D+2D^2}V_{in}$	$\frac{1-3D+D^2}{1-4D+2D^2}V_{in}$	$\frac{1-3D+D^2}{1-4D+2D^2}V_{in}$
	C_4	NA	$\frac{D}{1-3D}V_{in}$	NA	NA	$\frac{(1-D)}{1-4D+2D^2}V_{in}$	$\frac{2D-D^2}{1-4D+2D^2}V_{in}$	$\frac{2D-D^2}{1-4D+2D^2}V_{in}$
	C_5	NA	NA	NA	NA	NA	NA	$\frac{V_{in}}{1-D}$
DIODE STRESSES	D_1/D_2	$\frac{1}{1-2D}V_{in}$	$\frac{1}{1-3D}V_{in}$	$\frac{D}{1-3D}V_{in}$	$\frac{D}{1-2D-D^2}V_{in}$	$\frac{(1-D)}{1-4D+2D^2}V_{in}$	$\frac{(1-D)}{1-4D+2D^2}V_{in}$	$\frac{1}{1-4D+2D^2}V_{in}$
	D_3/D_6	$\frac{2D}{(1-D)(1-2D)}V_{in}$	NA	$\frac{1-D}{1-3D}V_{in}$	$\frac{2(1-D)}{1-2D-D^2}V_{in}$	$\frac{D}{1-4D+2D^2}V_{in}$	$\frac{D}{1-4D+2D^2}V_{in}$	$\frac{D}{(1-D)\cdot(1-4D+2D^2)}V_{in}$
	D_4/D_5	NA	NA	$\frac{D}{1-3D}V_{in}$	$\frac{1-3D}{1-2D-D^2}V_{in}$	$\frac{D}{1-4D+2D^2}V_{in}$	$\frac{D}{1-4D+2D^2}V_{in}$	$V_{D4} = \frac{V_{in}}{1-D}\cdot\left(\frac{1}{1-4D+2D^2}-1\right)$, $V_{D5} = \frac{V_{in}}{1-D}$
	Boost Factor	$\frac{1}{(1-D)(1-2D)}$	$\frac{1}{1-3D}$	$\frac{1+D}{1-3D}$	$\frac{1+D}{1-2D-D^2}$	$\frac{1}{1-4D+2D^2}$	$\frac{1}{1-4D+2D^2}$	$\frac{1}{(1-D)\cdot(1-4D+2D^2)}$
	Voltage Gain	$\frac{1}{(2M-1)}$	$\frac{M}{3M-2}$	$\frac{M(2-M)}{3M-2}$	$\frac{M(M-2)}{M^2-4M+2}$	$\frac{M}{2M^2-1}$	$\frac{M}{2M^2-1}$	$\frac{1}{2M^2-1}$
	D_{in}/Switch/ DC-link voltage	$\frac{1}{(1-D)(1-2D)}V_{in}$	$\frac{1}{1-3D}V_{in}$	$\frac{1+D}{1-3D}V_{in}$	$\frac{1+D}{1-2D-D^2}V_{in}$	$\frac{1}{1-4D+2D^2}V_{in}$	$\frac{1}{1-4D+2D^2}V_{in}$	$\frac{1}{(1-D)\cdot(1-4D+2D^2)}V_{in}$
	Input Current, I_{in}	i_{L3}	i_{L3}	$2i_{L1}$ - i_{PN}	i_{L3}	$2i_{L3}$ - i_{PN}	i_{L1}	i_{L5}
	Inductor Currents	$i_{L1,L2} = \frac{1-D}{1-2D}I_{PN}$, $i_{L3} = \frac{1-D}{1-3D}I_{PN}$	$i_{L1,L2,L3} = \frac{1-D}{1-3D}I_{PN}$	$i_{L1,L2,L3,L4} = \frac{1-D}{1-3D}I_{PN}$	$i_{L1} = \frac{1-D}{1-2D+2D^2}I_{PN}$, $i_{L2} = \frac{1-3D+2D^2}{1-2D+2D^2}I_{PN}$	$i_{L1,L2} = \frac{(1-D)}{1-4D+2D^2}I_{PN}$, $i_{L3,L4} = \frac{(1-D)^2}{1-4D+2D^2}I_{PN}$	$i_{L1,L2} = \frac{(1-D)}{1-4D+2D^2}I_{PN}$, $i_{L3,L4} = \frac{(1-D)^2}{1-4D+2D^2}I_{PN}$	$i_{L1,L2} = \frac{(1-D)}{1-4D+2D^2}I_{PN}$, $i_{L3,L4} = \frac{(1-D)^2}{1-4D+2D^2}I_{PN}$, $i_{L5} = \frac{1}{1-4D+2D^2}I_{PN}$
	Avg DC-link Current, I_{PN}	$(1-D)\frac{\widehat{V}_{PN}}{R}$	$(1-D)\frac{\widehat{V}_{PN}}{R}$	$(1-D)\frac{\widehat{V}_{PN}}{R}$	$(1-D)\frac{\widehat{V}_{PN}}{R}$	$(1-D)\frac{\widehat{V}_{PN}}{R}$	$(1-D)\frac{\widehat{V}_{PN}}{R}$	$(1-D)\frac{\widehat{V}_{PN}}{R}$

From a structural perspective, the proposed imp-EBqZSI introduces only minimal component overhead, specifically, two additional diodes, one extra inductor, and one capacitor compared to the enhanced-boost qZSI. However, this modest increase in components yields a significant performance improvement, particularly in terms of voltage gain and boost factor, while also lowering the electrical stress on critical switching elements. Furthermore, when the same voltage gain is targeted across all topologies, the proposed inverter demonstrates superior characteristics by maintaining lower stress levels on the semiconductor switches. This is a key advantage for thermal management, long-term reliability, and component derating in practical implementations. In conclusion, the imp-EBqZSI offers a well-balanced trade-off between complexity and performance, delivering the highest boost factor and voltage gain among the compared topologies, ensuring better operating margins for power semiconductor devices.

4.7 Summary

This chapter presents a novel inverter topology, imp-EBqZSI, developed by strategically modifying the traditional impedance network. The performance of the proposed inverter is rigorously evaluated through a combination of theoretical analysis, detailed simulation studies, and experimental validation. The imp-EBqZSI demonstrates superior operational characteristics to existing ZSI topologies, particularly its enhanced voltage boost capability at a reduced shoot-through duty ratio. This characteristic makes it especially well-suited for applications involving low-voltage DC sources, such as PV systems and distributed generation, where high step-up ratios are necessary to meet grid-level voltage requirements. One of the key advantages of the proposed topology lies in its ability to achieve higher voltage gain with lower stress on the semiconductor switches, enabling the inverter to operate at higher modulation indices. This not only improves the overall efficiency of the system but also facilitates the use of lower-rated and more cost-effective switching devices, thereby contributing to both thermal performance and cost-efficiency in practical implementations. The theoretical analysis assumes idealized conditions, neglecting losses due to parasitic resistances and the non-ideal behavior of switches, diodes, inductors, and capacitors. This foundational analysis

establishes a benchmark for performance under optimal conditions. To validate these theoretical predictions, extensive simulations are performed using PSCAD, modeling the dynamic and steady-state behavior of the inverter. These simulations incorporate non-ideal characteristics such as semiconductor conduction losses, offering a more realistic representation of actual inverter behavior. Further validation is achieved by developing a laboratory-scale hardware prototype, which experimentally confirms the simulation results. Key performance metrics, including DC-link voltage levels, capacitor voltage profiles, inductor currents, and output AC waveforms, are closely aligned with theoretical expectations, demonstrating the robustness and reliability of the proposed design across different testing environments.

Chapters 3 and 4 introduced high-gain inverter topologies, DA-SLEBqZSI, CA-SLEBqZSI, and imp-EBqZSI, which demonstrate the advantages of passive-only impedance networks, including reduced EMI, enhanced reliability, and suitability for low-voltage renewable energy applications such as photovoltaic and fuel cell systems. However, the increased complexity of these impedance networks makes analyzing undesirable operating modes more challenging. The following chapter addresses this by presenting a practical and analytical design methodology for sizing the impedance network components of the qZSI. It emphasizes the importance of maintaining continuous input current and provides a systematic procedure for calculating the minimum inductance and capacitance values necessary to avoid static or unstable operating states.

Note: This work, "Improved Enhanced-Boost Quasi-Z-Source Inverter," *2022 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Jaipur, India, 2022, pp. 1-6, DOI: 10.1109/PEDES56012.2022.10080512.

"Impedance Network Design of the Improved Enhanced-Boost Quasi-Z-Source Inverter," *2023 IEEE 3rd International Conference on Smart Technologies for Power, Energy and Control (STPEC)*, held in Bhubaneswar, India, Dec. 2023, pp. 1-6, DOI: 10.1109/STPEC59253.2023.10431290.

CHAPTER 5

Impedance Network Design of the Quasi Z-Source Inverter

5.1 Introduction

As outlined in the previous chapters, the voltage gain of ISIs can be significantly enhanced by strategically modifying the structure of the impedance network. Chapter 2 introduced two innovative SLEBqZSI topologies, namely DA-SLEBqZSI and CA-SLEBqZSI. Chapter 3 proposed a new imp-EBqZSI, which further extends the gain of the inverter. The inverters with passive-only impedance networks that eliminate the need for additional active switches or magnetic components, such as a transformer and coupled inductor, are an exciting research area. Such configurations offer several advantages, including reduced control complexity, minimized EMI, improved reliability, and compact hardware implementation. By systematically exploring new ways to interconnect passive components, further gains in voltage boost capability can be achieved, thereby expanding the suitability of ISIs for low-voltage renewable energy sources such as photovoltaic systems, fuel cells, and battery storage.

In designing the impedance network of these ISIs, a systematic method is used to calculate the critical threshold values of inductance and capacitance below which undesirable or unstable modes may occur. The proposed topologies, DA-SLEBqZSI, CA-SLEBqZSI, and imp-EBqZSI, have a complex impedance network compared to ZSI/qZSI. It would be more complicated to analyse the undesirable operating modes for these topologies. A detailed analysis of ZSI operating in these modes is presented in [82, 83]. Unlike the traditional ZSI, which uses an X-shaped impedance network, the qZSI adopts a more compact and efficient configuration that ensures a continuous input current, one of the most significant advantages of the qZSI over conventional ZSI. The continuous input current is suitable for photovoltaic panels or fuel cells. These sources typically require a stable and smooth current profile for optimal performance and longevity. The primary objective of this chapter is to present a practical and analytical design guideline for appropriately sizing the components of the impedance network of qZSI. This impedance network design of the qZSI is a primitive step

towards understanding the application-oriented optimization, considering all the desirable and undesirable states.

The organization of this chapter is structured to provide a comprehensive understanding of the qZSI and the proposed design methodology. Section 5.2 presents a detailed steady-state analysis of the qZSI, focusing on the operating principles, key circuit behavior, and the various possible operating modes. This analysis forms the theoretical foundation for the subsequent design procedures. In Section 5.3, design guidelines are developed to aid in properly selecting and sizing the impedance network components, namely the inductors and capacitors, ensuring stable operation of the inverter within the desired modes and avoiding undesirable states. These guidelines are based on the nonlinear steady-state equations derived in the previous section. Section 5.4 validates the proposed design methodology through simulation and experimental results. Comparative performance evaluations are provided to demonstrate the effectiveness, reliability, and practical applicability of the designed impedance network under various operating conditions. Finally, Section 5.5 concludes the chapter with a summary of key findings.

5.2 Steady-state analysis of qZSI

The qZSI is a single-stage power conversion topology that integrates voltage buck and boost capabilities through a uniquely structured impedance network. The impedance network of the qZSI consists of two inductors and two capacitors arranged in a split-branch manner, along with a single diode. Each inductor is connected in series with the DC source, and each capacitor is connected in parallel with its corresponding inductor, forming two symmetrical branches. These branches converge through the diode into the DC-link, which is then connected to the inverter bridge. The inverter bridge, typically a standard three-phase full-bridge configuration, converts the boosted DC voltage into AC for the load.

The qZSI operates by alternating between the shoot-through, active state, and zero state. The possible operating states of the impedance network in a qZSI are fundamentally determined by the switching state of the diode within the network, specifically whether the diode

Table 5.1. Possible impedance network operating states

VSI	**Open**		**Active**		**Shoot-through**	
Diode	ON	OFF	ON	OFF	OFF	ON
Impedance Network	Open-I	Open-II	Active-I	Active-II	ST-I	ST-II

is in the ON (conducting) or OFF (blocking) state. Table 5.1 outlines the possible operating states based on the diode status (ON/OFF). This classification is critical for analyzing and predicting the inverter performance, designing control strategies, and properly sizing the impedance network components to avoid undesirable operating modes that could compromise system stability or efficiency.

In the open state, the inverter applies zero switching vectors such as [0,0,0] or [1,1,1], meaning that all the upper or all the lower switches of the three-phase bridge are either ON or OFF simultaneously. This configuration effectively disconnects the inverter from the impedance network, resulting in no power transfer to the load. In circuit terms, the VSI appears as an open circuit during this interval, and no current flows through the DC-link.

In contrast, during the active state, the inverter applies one of the six non-zero switching vectors corresponding to the normal operation of the VSI. In this mode, the inverter is represented by a constant current source, denoted as I_{PN}, which reflects the current drawn by the load. The value of I_{PN} is determined solely by the load connected to the inverter and is considered constant over short time intervals. While the inverter is in the active state, power is transferred from the impedance network to the load. During this interval, the inductors discharge and transfer energy to the capacitors and the inverter, while the capacitors are simultaneously charged, storing energy for the next shoot-through period.

In the shoot-through state, one or more inverter legs are short-circuited by simultaneously turning on both the top and bottom switches of that leg. Unlike in a traditional VSI, where shoot-through causes a short circuit, the qZSI is designed to utilize the shoot-through state. In this mode, the input terminal of the VSI is shorted, and no power is delivered to the load. Instead, this period is used to store energy in the impedance network. Specifically, the capacitors discharge and transfer their energy into the inductors, which are being charged.

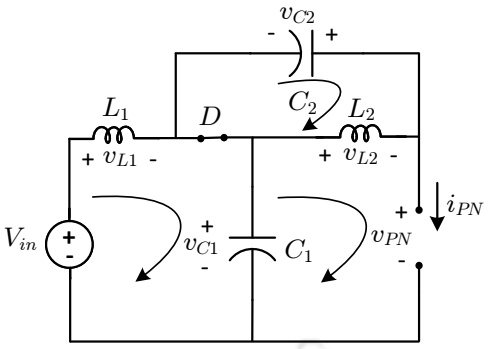


Fig. 5.1. Equivalent circuit of qZSI in open state.

This energy exchange is essential for boosting the output voltage of the inverter. The general steady-state equations that describe the voltage-current variation of the impedance network is expressed as:

$$\begin{aligned} v_{L1} &= L_1 \frac{di_{L_1}}{dt}; \qquad v_{L2} = L_2 \frac{di_{L_2}}{dt} \\ i_{C1} &= C_1 \frac{dv_{C_1}}{dt}; \qquad i_{C2} = C_2 \frac{dv_{C_2}}{dt} \end{aligned} \tag{5.1}$$

$$\begin{aligned} V_{in} &= v_{L_1} + v_{C_1}; \qquad I_{in} = i_{L_1} \\ v_{PN} &= v_{C_1} - v_{L_2}; \qquad i_{PN} = i_{L_2} - i_{C_2} \end{aligned} \tag{5.2}$$

where v_{L_1}, v_{L_2} and i_{L_1}, i_{L_2} are voltage across and current through the inductors L_1 and L_2, v_{C_1}, v_{C_2} and i_{C_1}, i_{C_2} are voltage across and current through the capacitors C_1 and C_2. V_{in}, and I_{in} are source voltage and current, and v_{PN}, and i_{PN} are the voltage and current at the input of terminal of VSI.

Open-I state

During the open-I state, the DC bus current is zero, as illustrated in Fig. 5.1.

$$i_{PN} = 0. \tag{5.3}$$

By substituting (5.3) into (5.1) and (5.2), we obtain the following expressions:

$$\frac{d^2 v_{C_1}}{dt^2} + \frac{v_{C_1}}{L_1 C_1} = \frac{V_{in}}{L_1 C_1} \tag{5.4}$$

Solving the above equation yields the expressions for the voltage across capacitor C_1 and the current flowing through it, which can be written as follows:

$$\begin{aligned} v_{C_1} &= V_{in} + X_{O_1} \cdot \sin(\omega_1 t + \Phi_{O_1}) \\ i_{C_1} = C_1 \cdot \frac{dv_{C_1}}{dt} &= \omega_1 C_1 \cdot X_{O_1} \cdot \cos(\omega_1 t + \Phi_{O_1}) \end{aligned} \tag{5.5}$$

where

$$\begin{aligned} \omega_1 &= 1/\sqrt{L_1 C_1} \\ X_{O_1} &= \sqrt{(v_{C_{1iO}} - V_{in})^2 + [i_{L_{1iO}}/\omega_1 C_1]^2} \\ \Phi_{O_1} &= \tan^{-1}[\omega_1 C_1 \cdot (v_{C_{1iO}} - V_{in})/i_{L_{1iO}}] \end{aligned} \tag{5.6}$$

Similarly for capacitor C_2 the equations can be written as:

$$\begin{aligned} v_{C_2} &= X_{O_2} \cdot \sin(\omega_2 t + \Phi_{O_2}) \\ i_{C_2} = C_2 \cdot \frac{dv_{C_2}}{dt} &= \omega_2 C_2 \cdot X_{O_2} \cdot \cos(\omega_2 t + \Phi_{O_2}) \end{aligned} \tag{5.7}$$

where

$$\begin{aligned} \omega_2 &= 1/\sqrt{L_2 C_2} \\ X_{O_2} &= \sqrt{(v_{C_{2iO}})^2 + [i_{L_{2iO}}/\omega_2 C_2]^2} \\ \Phi_{O_2} &= \tan^{-1}[\omega_2 C_2 \cdot v_{C_{2iO}}/i_{L_{2iO}}] \end{aligned} \tag{5.8}$$

In the above set of equations, $v_{C_{1iO}}$, $v_{C_{2iO}}$, and $i_{L_{1iO}}$, $i_{L_{2iO}}$ represent the initial values of the capacitor voltages and inductor currents, respectively, during the open-I state. When the phase angles Φ_{O1}, Φ_{O2} are less than $\pi/2$, these initial values are positive. Under this condition, the voltages across the capacitors increase sinusoidally over time, reaching their peak values when Φ_{O1}, Φ_{O2} = $\pi/2$. Concurrently, the inductor currents gradually decrease and eventually reach zero. At this point, the diode becomes reverse-biased and turns off, prompting the qZSI to transition from the open-I state to the open-II state.

The expressions for the inductor currents during the open-I state are given by:

$$\begin{aligned} i_{L_1} &= i_{C_1} \\ i_{L_2} &= i_{C_2} \end{aligned} \tag{5.9}$$

Open-II state

In this state, the diode remains off and the VSI is still in the open circuited.

$$\begin{aligned} I_{in} &= 0 \\ i_{PN} &= 0 \end{aligned} \tag{5.10}$$

During this stage, all system variables remain constant because the impedance network is disconnected from both the input source and the load, effectively isolating it from the rest of the circuit. The following condition must be satisfied to ensure the inverter avoids entering this inactive and undesirable state.

$$\begin{aligned} i_{L_{1fO}} &> 0 \\ i_{L_{2fO}} &> 0 \end{aligned} \tag{5.11}$$

Active-I state

In the active-I state, as illustrated in Fig. 5.2., the diode remains ON, allowing current to flow, and the capacitors are being charged. During this interval, energy is transferred from the input source to the VSI. The corresponding state equations that describe the behavior of the circuit during this mode are given as follows:

$$\begin{aligned} i_{PN} &= I_0 \\ i_{L_1} - i_{L_2} &= i_{C_1} - i_{C_2} \end{aligned} \tag{5.12}$$

By substituting (5.12) into (5.1) and (5.2), the expressions for the voltage across capacitor C_1

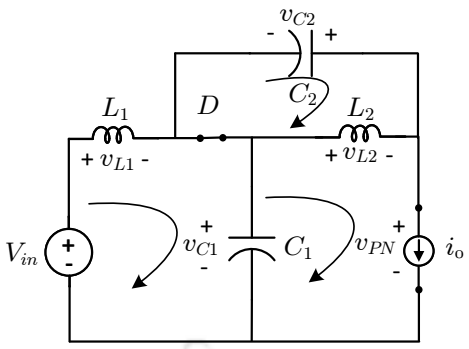


Fig. 5.2. Equivalent circuit of qZSI in active state.

and the current flowing through it can be derived and are given as follows:

$$\begin{aligned} v_{C_1} &= V_{in} + X_{A_1} \cdot \sin(\omega_1 t + \Phi_{A_1}) \\ i_{C_1} = C_1 \cdot \frac{dv_{C_1}}{dt} &= \omega_1 C_1 \cdot X_{A_1} \cdot \cos(\omega_1 t + \Phi_{A_1}) \end{aligned} \tag{5.13}$$

where

$$\begin{aligned} X_{A_1} &= \sqrt{(v_{C_{1iA}} - V_{in})^2 + [(i_{L_{1iA}} - I_0)/\omega_1 C_1]^2} \\ \Phi_{A_1} &= \tan^{-1}[\omega_1 C_1 \cdot (v_{C_{1iA}} - V_{in})/(i_{L_{1iA}} - I_0)] \end{aligned} \tag{5.14}$$

Similarly for capacitor C_2 the equations can be written as:

$$\begin{aligned} v_{C_2} &= X_{A_2} \cdot \sin(\omega_2 t + \Phi_{A_2}) \\ i_{C_2} = C_2 \cdot \frac{dv_{C_2}}{dt} &= \omega_2 C_2 \cdot X_{A_2} \cdot \cos(\omega_2 t + \Phi_{A_2}) \end{aligned} \tag{5.15}$$

where

$$\begin{aligned} X_{A_2} &= \sqrt{(v_{C_{2iA}})^2 + [(i_{L_{2iA}} - I_0)/\omega_2 C_2]^2} \\ \Phi_{A_2} &= \tan^{-1}[\omega_2 C_2 \cdot v_{C_{2iA}}/(i_{L_{2iA}} - I_0)] \end{aligned} \tag{5.16}$$

In the equations above, $v_{C_{1iA}}$, $v_{C_{2iA}}$, and $i_{L_{1iA}}$, $i_{L_{2iA}}$ represent the initial values of the capacitor voltages and inductor currents during active-I state.

The expressions for the inductor currents are given by:

$$\begin{aligned} i_{L_1} = i_{C_1} + I_0; \quad i_{L_2} = i_{C_2} + I_0 \\ i_{PN} = i_{L_1} + i_{L_2} - i_D; \quad i_{L_1} = i_{L_2} = i_L \end{aligned} \tag{5.17}$$

If the duration of active-I state is t_A, the equations (5.13) and (5.15) can be expressed as follows:

$$\begin{aligned} v_{C_{1fA}} &= V_{in} + X_{A_1} \cdot \sin(\omega_1 t_A + \Phi_{A_1}) \\ v_{C_{2fA}} &= X_{A_2} \cdot \sin(\omega_2 t_A + \Phi_{A_2}) \\ i_{L_{1fA}} &= I_0 + \omega_1 C_1 \cdot X_{A_1} \cdot \cos(w_1 t_A + \Phi_{A_1}) \\ i_{L_{2fA}} &= I_0 + \omega_2 C_2 \cdot X_{A_2} \cdot \cos(w_2 t_A + \Phi_{A_2}) \end{aligned} \tag{5.18}$$

Active-II state

In active-II state, the capacitor is forced to discharge through the load, causing its voltage to drop to zero. This condition adversely affects the boosting operation of the qZSI and should be avoided. To prevent the inverter from entering this inactive and undesirable state, the following condition must be satisfied.

$$\begin{aligned} i_{L_{1fA}} &> 0 \\ i_{L_{2fA}} &> 0 \end{aligned} \tag{5.19}$$

Shoot-through-I state

In the shoot-through state, as illustrated in Fig. 5.3., one or more inverter legs are short-circuited by simultaneously turning on both the upper and lower switches of the same leg. During this mode, the input terminals of the VSI are shorted, and no power is supplied to the

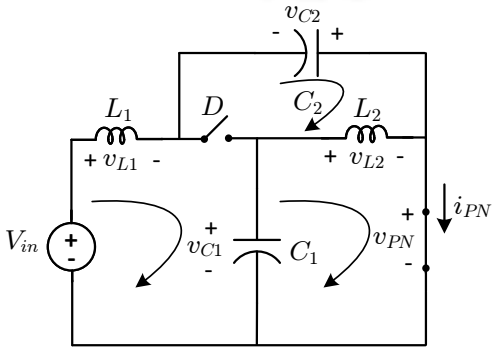


Fig. 5.3. Equivalent circuit of qZSI in shoot-through state.

load. The state equation for shoot-through-I state is expressed as:

$$\begin{aligned} i_{C_1} &= i_{L_2} \quad i_{C_2} = i_{L_1} \\ v_{C_1} &= v_{L_2} \quad v_{C_2} = v_{L_1} - V_{in} \end{aligned} \tag{5.20}$$

By substituting (5.20) into (5.1) and (5.2), the following expressions are obtained:

$$\begin{aligned} v_{C_1} &= X_{S_1} \cdot \sin(\omega_3 t + \Phi_{S_1}) \\ i_{C_1} &= C_1 \frac{dv_{C_1}}{dt} = \omega_3 C_1 \cdot X_{S_1} \cdot \cos(w_3 t + \Phi_{S_1}) \end{aligned} \tag{5.21}$$

where

$$\begin{aligned} \omega_3 &= 1/\sqrt{L_2 C_1} \\ X_{S_1} &= \sqrt{(v_{C_{1iS}})^2 + [-i_{L_{1iS}}/\omega_3 C_1]^2} \\ \Phi_{S_1} &= \tan^{-1}\left[-\omega_3 C_1 \cdot v_{C_{1iS}}/i_{L_{1iS}}\right] \end{aligned} \tag{5.22}$$

Similarly for capacitor C_2 the equations can be written as:

$$\begin{aligned} v_{C_2} &= V_{in} + X_{S_2} \cdot \sin(\omega_4 t + \Phi_{S_2}) \\ i_{C_2} &= C_2 \frac{dv_{C_2}}{dt} = \omega_4 C_2 \cdot X_{S_2} \cdot \cos(w_4 t + \Phi_{S_2}) \end{aligned} \tag{5.23}$$

where

$$\begin{aligned} \omega_4 &= 1/\sqrt{L_1 C_2} \\ X_{S_2} &= \sqrt{(v_{C_{2iS}} - V_{in})^2 + [-i_{L_{2iS}}/\omega_4 C_2]^2} \\ \Phi_{S_2} &= \tan^{-1}\left[-\omega_4 C_2 \cdot (v_{C_{2iS}} - V_{in})/i_{L_{2iS}}\right] \end{aligned} \tag{5.24}$$

In the above set of equations, $v_{C_{1iS}}$, $v_{C_{2iS}}$, and $i_{L_{1iS}}$, $i_{L_{2iS}}$ represent the initial values of the capacitor voltages and inductor currents during shoot-through-I State.

If the duration of this state is t_S, the equations (5.21) and (5.23) can be rewritten as follows:

$$\begin{aligned} v_{C_{1fS}} &= X_{S_1} \cdot \sin(\omega_3 t_S + \Phi_{S_1}) \\ v_{C_{2fS}} &= V_{in} + X_{S_2} \cdot \sin(\omega_4 t_S + \Phi_{S_2}) \\ i_{L_{1fS}} &= \omega_3 C_1 \cdot X_{S_1} \cdot \cos(w_3 t_S + \Phi_{S_1}) \\ i_{L_{2fS}} &= \omega_4 C_2 \cdot X_{S_2} \cdot \cos(w_4 t_S + \Phi_{S_2}) \end{aligned} \tag{5.25}$$

Shoot-through-II state

The diode is turned on, and the current through the diode increases linearly. This state must be avoided as the diode current may reach a very high value, damaging it. The following condition should be met to make the diode reverse-biased all the time in the shoot-through state.

$$v_{C_1} > V_{in} - v_{L_1} \tag{5.26}$$

5.3 Designing of impedance network

The preceding analysis shows that the open-II, active-II, and shoot-through-II states do not contribute to the desired power conversion process and should be avoided. These states never support energy transfer to the load. They are considered non-functional in effective inverter operation and are referred to as static states. In contrast, practical qZSI operation typically involves only two or three states: active-I, and shoot-through-I. These states directly contribute to energy conversion and voltage boosting, forming the core of the inverter operating principle. Accordingly, they are termed dynamic states. The occurrence of static states is generally associated with large fluctuations in capacitor voltages and inductor currents, which can result in violations of critical operating conditions defined in equations (5.11), (5.19), and (5.26). To prevent this, limiting the ripple magnitudes of the capacitor voltages and inductor currents is essential. This can be effectively achieved by appropriately increasing the capacitance and inductance values in the circuit design. Therefore, after completing the design of the qZSI circuit, it is recommended that compliance with the three key conditions mentioned above be

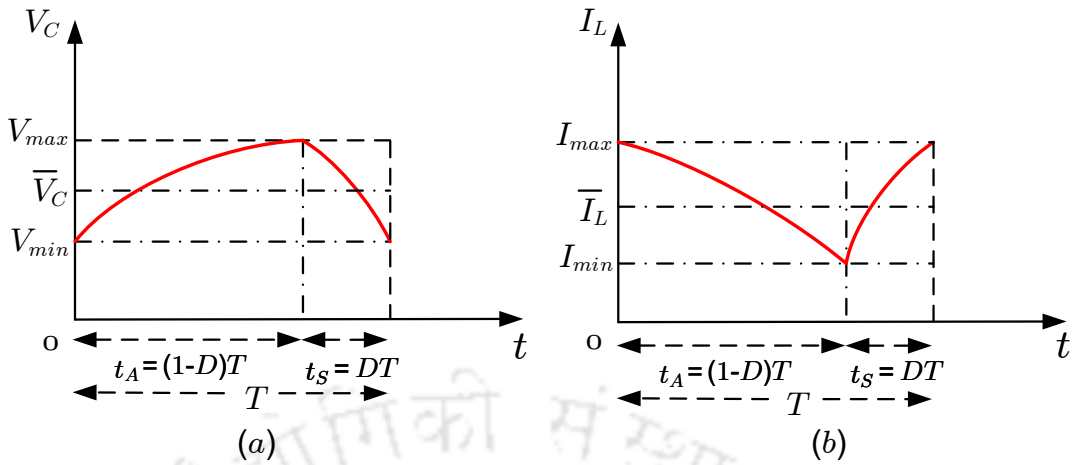


Fig. 5.4. Steady state waveforms of (a) capacitor voltage and (b) inductor current.

verified. Ensuring these conditions are satisfied confirms that the operation is only confined to the dynamic states, thereby avoiding unwanted and inefficient static states and ensuring optimal inverter performance.

5.3.1 Sinusoidal waveforms based design

When the qZSI operates in dynamic states, avoiding static and zero states where no power conversion occurs, it functions in active-I and shoot-through-I states. The boundary condition is defined by assuming that the final value of a variable in one state corresponds to the initial value of the same variable in the other state. The steady-state values of these variables are expressed as follow:

$$\begin{aligned} v_{C_{1iA}} &= v_{C_{1fS}} = V_{1_{min}} \\ v_{C_{2iA}} &= v_{C_{2fS}} = V_{2_{min}} \\ v_{C_{1iS}} &= v_{C_{1fA}} = V_{1_{max}} \\ v_{C_{2iS}} &= v_{C_{2fA}} = V_{2_{max}} \end{aligned} \tag{5.27}$$

$$\begin{aligned} i_{L_{1iA}} &= i_{L_{1fS}} = I_{1_{max}} \\ i_{L_{2iA}} &= i_{L_{2fS}} = I_{2_{max}} \\ i_{L_{1iS}} &= i_{L_{1fA}} = I_{1_{min}} \\ i_{L_{2iS}} &= i_{L_{2fA}} = I_{2_{min}} \end{aligned} \tag{5.28}$$

where $V_{1_{min}}$ and $V_{2_{min}}$ represent the minimum values, and $V_{1_{max}}$ and $V_{2_{max}}$ represent the maximum values of the capacitor voltages. In comparison, $I_{1_{min}}$ and $I_{2_{min}}$ are the minimum values, and $I_{1_{max}}$ and $I_{2_{max}}$ are the maximum values of the inductor currents, respectively. Furthermore, considering T as the period of one switching cycle, it can be divided into the active-I state and the shoot-through-I state. The duration of the shoot-through-I state and the active-I state are defined as $T = D \cdot T$ and $t_A = (1 - D) \cdot T$, respectively. The capacitor voltage and inductor current waveforms are shown in Fig. 5.4. (a) and (b), respectively.

By substituting (5.27) and (5.28) in (5.14), (5.16), (5.22) and (5.24) the following expression are obtained.

$$\begin{aligned} X_{A_1} &= \sqrt{(V_{1_{min}} - V_{in})^2 + \left[\frac{(I_{1_{max}} - I_0)}{\omega_1 C_1}\right]^2} \\ \Phi_{A_1} &= \tan^{-1}\left[\frac{\omega_1 C_1 \cdot (V_{1_{min}} - V_{in})}{(I_{1_{max}} - I_0)}\right] \\ X_{A_2} &= \sqrt{(V_{2_{min}})^2 + \left[\frac{(I_{2_{max}} - I_0)}{\omega_2 C_2}\right]^2} \\ \Phi_{A_2} &= \tan^{-1}\left[\frac{\omega_2 C_2 \cdot V_{2_{min}}}{(I_{2_{max}} - I_0)}\right] \end{aligned} \tag{5.29}$$

$$\begin{aligned} X_{S_1} &= \sqrt{(V_{1_{max}})^2 + \left[\frac{-I_{2_{min}}}{\omega_3 C_1}\right]^2} \\ \Phi_{S_1} &= \tan^{-1}\left[\frac{\omega_3 C_1 \cdot V_{1_{max}}}{-I_{2_{min}}}\right] \\ X_{S_2} &= \sqrt{(V_{2_{max}} - V_{in})^2 + \left[\frac{-I_{1_{min}}}{\omega_4 C_2}\right]^2} \\ \Phi_{S_2} &= \tan^{-1}\left[\frac{\omega_4 C_2 \cdot (V_{2_{max}} - V_{in})}{-I_{1_{min}}}\right] \end{aligned} \tag{5.30}$$

Similarly by substituting (5.27) and (5.28) in (5.18) and (5.25) we get

$$\begin{aligned}
F(1) &= -V_{1_{max}} + V_{in} + X_{A_1} \cdot \sin(\omega_1 t_A + \Phi_{A_1}) = 0 \\
F(2) &= -I_{1_{min}} + I_0 + \omega_1 C_1 \cdot X_{A_1} \cdot \cos(w_1 t_A + \Phi_{A_1}) = 0 \\
F(3) &= -V_{2_{max}} + X_{A_2} \cdot \sin(\omega_2 t_A + \Phi_{A_2}) = 0 \\
F(4) &= -I_{2_{min}} + I_0 + \omega_2 C_2 \cdot X_{A_2} \cdot \cos(w_2 t_A + \Phi_{A_2}) = 0 \\
F(5) &= -V_{1_{min}} + X_{S_1} \cdot \sin(\omega_3 t_S + \Phi_{S_1}) = 0 \\
F(6) &= -I_{1_{max}} + \omega_3 C_1 \cdot X_{S_1} \cdot \cos(w_3 t_S + \Phi_{S_1}) = 0 \\
F(7) &= -V_{2_{min}} + V_{in} + X_{S_2} \cdot \sin(\omega_4 t_S + \Phi_{S_2}) = 0 \\
F(8) &= -I_{2_{max}} + \omega_4 C_2 \cdot X_{S_2} \cdot \cos(w_4 t_S + \Phi_{S_2}) = 0
\end{aligned} \tag{5.31}$$

The equivalent DC-link voltage applied to the VSI corresponds to the average value of v_{PN} during the active-1 state, and is expressed as $\overline{V}_{PN}$

$$\overline{V}_{PN} = \frac{1}{t_A} \int_0^{t_A} v_{PN} \cdot dt = V_{in} + \frac{1}{(1-D) \cdot T} \frac{(I_{1_{max}} - I_{1_{min}})}{(\omega_1^2 C_1)} + \frac{(I_{1_{max}} - I_{2min})}{(\omega_2^2 C_2)} \tag{5.32}$$

For a three-phase VSI operated with sinusoidal PWM, the peak value of the fundamental line-to-neutral output voltage $\widehat{v}_m$ is given by $M \cdot \overline{V}_{PN}/2$, where M is the modulation index. Substituting $\overline{V}_{PN}$ in equation (5.32), $\widehat{v}_m$ can thus be expressed as:

$$F(9) = \frac{-2 \cdot \widehat{v}_m}{M} + V_{in} + \frac{1}{(1-D) \cdot T} \frac{(I_{1_{max}} - I_{1_{min}})}{(\omega_1^2 C_1)} + \frac{(I_{1_{max}} - I_{2min})}{(\omega_2^2 C_2)} = 0 \tag{5.33}$$

Neglecting inverter power losses and the impact of harmonics on the AC side, the average power transferred from the DC-link can be equated to the power delivered to the AC load over one cycle

$$\overline{V}_{PN} \cdot I_0 \cdot (1-D) = \frac{3}{2} \cdot \widehat{v}_m \cdot \widehat{i}_m \cdot \cos\phi \tag{5.34}$$

$\widehat{i}_m$ represents the peak phase current on the AC side, and ϕ denotes the power factor angle of the AC load connected to the inverter.

By substituting $\overline{V}_{PN} = (2 \cdot \widehat{v}_m/M)$ in (5.34) we get,

$$F(10) = -I_0 + \frac{3}{4} \cdot M \cdot \widehat{i}_m \cdot \frac{\cos\phi}{(1-D)} \tag{5.35}$$

5.3.2 Solution process

To obtain the impedance network inductors and capacitors, the functions F(1) - F(10) mentioned in (5.31), (5.33), and (5.35). A total of thirty-one variables are involved in these equations. These variables are categorized as follows to facilitate the solution of the equations discussed above.

1. input parameters: V_{in}, $\widehat{v}_m$, $\widehat{i}_m$, ϕ, and T;
2. output variables: L_1, L_2, C_1, C_2, D, I_0, $V_{1_{max}}$, $V_{2_{max}}$, $I_{1_{max}}$, and $I_{2_{max}}$;
3. design parameters: $V_{1_{min}}$, $V_{2_{min}}$, $I_{1_{min}}$, and $I_{2_{min}}$;
4. internal variables: X_{A_1}, X_{A_2}, Φ_{A_1}, Φ_{A_2}, X_{S_1}, X_{S_2}, Φ_{S_1}, Φ_{S_2}, ω_1, ω_2, ω_3, ω_4 and M.

To determine the values of the ten unknown variables mention as output variables, it is essential to solve a system of ten nonlinear equations, labeled as F(1) through F(10), which correspond to equations (5.31), (5.33), and (5.35). These equations are inherently nonlinear due to the complex relationships among voltages, currents, and duty ratios in the circuit. Solving them analytically is impractical; hence, a numerical iterative approach, such as MATLAB's fsolve function, is employed to find a consistent solution that satisfies all the equations simultaneously. In addition to the ten output variables, thirteen internal variables are involved in formulating these nonlinear equations. These internal variables are explicitly defined through algebraic equations based on other system parameters and variables. Although it is mathematically feasible to eliminate the internal variables by substituting their expressions directly into the nonlinear equations, this leads to complex and less readable formulations. Consequently, retaining these internal variables within the iterative loop is preferable, as this approach improves the clarity of the equations and makes the numerical implementation more straightforward.

A critical requirement for iterative numerical solvers like fsolve is the specification of initial guesses for each unknown variable. The convergence and accuracy of the solution are highly dependent on the quality of these initial values. Poorly chosen starting points may lead to slow convergence, divergence, or convergence to non-physical solutions. An approximate design approach is proposed in the subsequent section to address this. This method relies on a simplified analysis using linearized waveforms, which provides reasonably accurate estimations of the unknown variables. These estimations serve as effective initial conditions for the nonlinear solver, significantly enhancing the robustness and efficiency of the numerical solution process.

5.3.3 Initial values

The design approach presented here is based on the assumption that the capacitor voltage and inductor current vary linearly over time. This assumption holds well when the ripple components of these variables are small relative to their average values. Excessive ripple increases the voltage and current stresses on ZSI components and degrades the quality of the AC output waveform by introducing harmonics. For this reason, practical qZSI design typically employ relatively large inductors and capacitors to minimize ripple. Consequently, the following method provides a suitable approximation for sizing components in most practical applications. Fig. 5.5. illustrates the assumed linear waveforms of the capacitor voltage and inductor current over a single switching cycle of the DC-link. Denoting the ripple and average values of capacitor voltages and inductor currents in steady-state as ΔV_{C_1}, ΔV_{C_2}, ΔI_{L_1}, ΔI_{L_2}, $\overline{V}_{C_1}$, $\overline{V}_{C_2}$, $\overline{I}_{L_1}$, and $\overline{I}_{L_2}$, respectively are written below.

$$\begin{aligned} V_{1_{min}} &= \overline{V}_{C_1} - \Delta V_{C_1} = (1 - k_v)\overline{V}_{C_1} \\ V_{2_{min}} &= \overline{V}_{C_2} - \Delta V_{C_2} = (1 - k_v)\overline{V}_{C_2} \\ V_{1_{max}} &= \overline{V}_{C_1} + \Delta V_{C_1} = (1 + k_v)\overline{V}_{C_1} \\ V_{2_{max}} &= \overline{V}_{C_2} + \Delta V_{C_2} = (1 + k_v)\overline{V}_{C_2} \end{aligned} \tag{5.36}$$

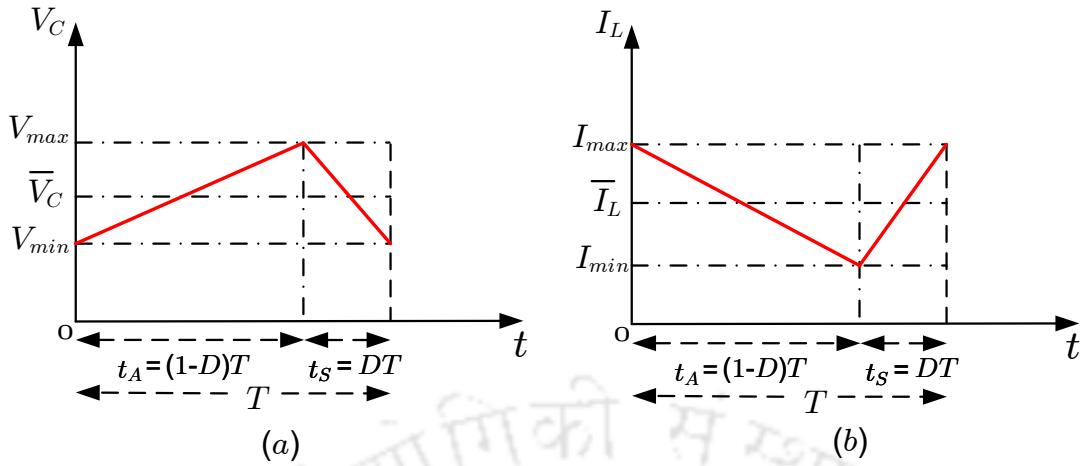


Fig. 5.5. Linear approximation of (a) capacitor voltage and (b) inductor current for small ripple.

$$\begin{aligned} I_{1_{min}} &= \overline{I}_{L_1} - \Delta I_{L_1} = (1 - k_i)\overline{I}_{L_1} \\ I_{2_{min}} &= \overline{I}_{L_2} - \Delta I_{L_2} = (1 - k_i)\overline{I}_{L_2} \\ I_{1_{max}} &= \overline{I}_{L_1} + \Delta I_{L_1} = (1 + k_i)\overline{I}_{L_1} \\ I_{2_{max}} &= \overline{I}_{L_2} + \Delta I_{L_2} = (1 + k_i)\overline{I}_{L_2} \end{aligned} \tag{5.37}$$

where k_v and k_i are the ripple factor of capacitor voltages and inductor currents respectively, given by $k_v = \Delta V_{C_1}/\overline{V}_{C_1} = \Delta V_{C_2}/\overline{V}_{C_2}$ and $k_i = \Delta I_{L_1}/\overline{I}_{L_1} = \Delta I_{L_2}/\overline{I}_{L_2}$.

With linear variation of waveforms ΔV_{C_1}, ΔV_{C_2}, ΔI_{L_1}, and ΔI_{L_2} can be expressed as

$$\begin{aligned} \Delta V_{C_1} &= \frac{\overline{I}_{C_1} \cdot \Delta t}{C_1}; \qquad \Delta V_{C_2} = \frac{\overline{I}_{C_2} \cdot \Delta t}{C_2} \\ \Delta I_{L_1} &= \frac{\overline{V}_{L_1} \cdot \Delta t}{L_1}; \qquad \Delta I_{L_2} = \frac{\overline{V}_{L_2} \cdot \Delta t}{L_2} \end{aligned} \tag{5.38}$$

Considering shoot-through-I period

$$\begin{aligned} C_1 &= \frac{DT \cdot \overline{I}_{L_2}}{2 \cdot \Delta V_{C_1}}; \qquad C_2 = \frac{DT \cdot \overline{I}_{L_1}}{2 \cdot \Delta V_{C_2}} \\ L_1 &= \frac{DT \cdot (\overline{V}_{C_2} + V_{in})}{2 \cdot \Delta I_{L_1}}; \qquad L_2 = \frac{DT \cdot \overline{V}_{C_1}}{2 \cdot \Delta I_{L_2}} \end{aligned} \tag{5.39}$$

For qZSI the relationship between capacitor voltages and input voltages given below are

$$\frac{\overline{V}_{C_1}}{V_{in}} = K; \quad \frac{\overline{V}_{C_2}}{V_{in}} = K - 1; \quad \frac{\overline{I}_{L_1}}{I_0} = \frac{\overline{I}_{L_2}}{I_0} = K \tag{5.40}$$

where

$$K = \frac{1-D}{1-2D}$$

combining (5.39) and (5.40) the inductors and capacitors values are obtained as given below

$$C_1 = \frac{DT \cdot I_0}{2 \cdot k_v \cdot V_{in}}; \qquad C_2 = \frac{(1-D)T \cdot I_0}{2 \cdot k_v \cdot V_{in}}$$
$$L_1 = L_2 = \frac{DT \cdot V_{in}}{2 \cdot k_i \cdot I_0} \tag{5.41}$$

The peak value of the AC phase voltage is given by

$$\widehat{v}_m = M \cdot B \cdot \frac{V_{in}}{2} \tag{5.42}$$

where M is modulation index and B is the boost factor. For simple boost control the modulation index is defined as

$$M = (1-D) \tag{5.43}$$

5.4 Design example

The qZSI is powered by a 36 V DC input and employs the simple boost control (SBC) strategy for modulation. The switching frequency is fixed at 10 kHz to ensure effective high-frequency operation while maintaining manageable switching losses. The inverter is specifically configured to supply a balanced three-phase resistive load operating at unity power factor, facilitating straightforward analysis and emphasizing real power transfer. The detailed circuit parameters used in the design are summarized in Table 5.2. To ensure stable and efficient operation, careful attention is given to the design of the impedance network, which plays a crucial role in energy buffering and voltage boosting. A key design objective is minimizing both voltage and current ripples to reduce stress on passive components and improve overall reliability. Accordingly, the capacitor voltage ripple is limited to 2% of its average steady-state value, while the inductor current ripple is constrained to 5%. These ripple constraints are chosen to strike a balance between physical component size,

Table 5.2. Parameters and component values for simulation and experiment

Parameters	**Values**
Input Voltage	V_{in} = 36 V
Impedance network inductors	L_1 = 3 mH, L_2 = 3 mH
Impedance network capacitors	C_1 = 56 μF, C_2 = 56 μF
Capacitor voltage ripple	k_v = 0.02
Inductor current ripple	k_i = 0.05
Fundamental frequency	f_r = 50 Hz
Switching frequency	f_s = 10 kHz
Shoot-through duty ratio	D = 0.351
Modulation index	M = 0.62
Resistive Load	R = 14 Ω
Filter inductor	L_f = 5 mH
Filter capacitor	C_f = 10 μF

cost, and performance, ensuring that the passive elements operate well within their thermal and electrical ratings. The initial design estimates for the impedance network elements, including the inductance and capacitance values, are calculated using a set of analytical expressions (5.36), (5.37), (5.39), (5.41), and (5.42). These equations are derived based on linear approximations of the steady-state waveforms and are constrained by the specified ripple limits. The final values of the output variables obtained after convergence of the nonlinear solver are summarized in Table 5.3.

Table 5.3. Output variables obtained in solution process

L_1 = 3.0050 mH	L_2 = 2.9972 mH
C_1 = 26.5175 μ F	C_2 = 49.0296 μ F
D = 0.315	I_0 = 2.12 A
$V_{1_{max}}$ = 79.87 V	$V_{2_{max}}$ = 43.19 V
$I_{1_{max}}$ = 4.85 A	$I_{2_{max}}$ = 4.85 A

5.4.1 Simulation results of qZSI

An extensive time-domain simulation study has been conducted for the qZSI using MATLAB/Simulink to validate the analytical design and assess the dynamic performance of the inverter. The simulation employs the component values determined via the numerical

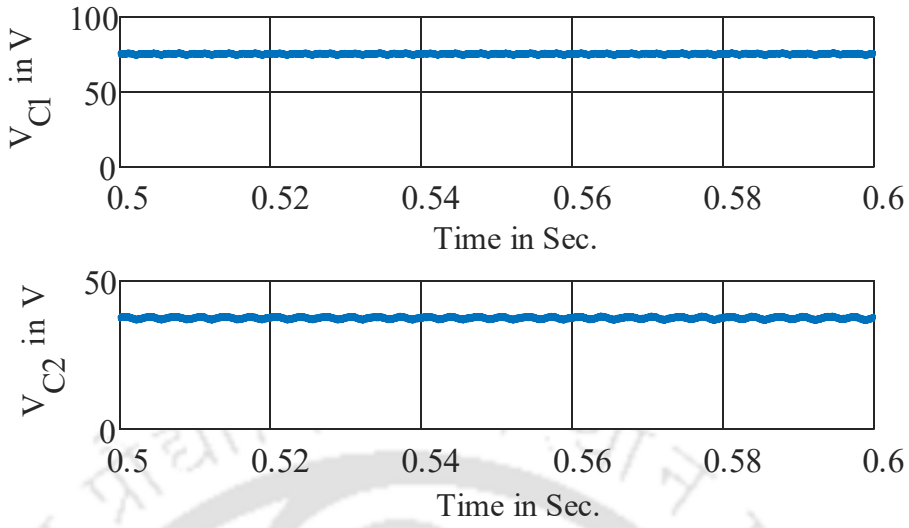


Fig. 5.6. Simulation results of capacitor voltages of the qZSI.

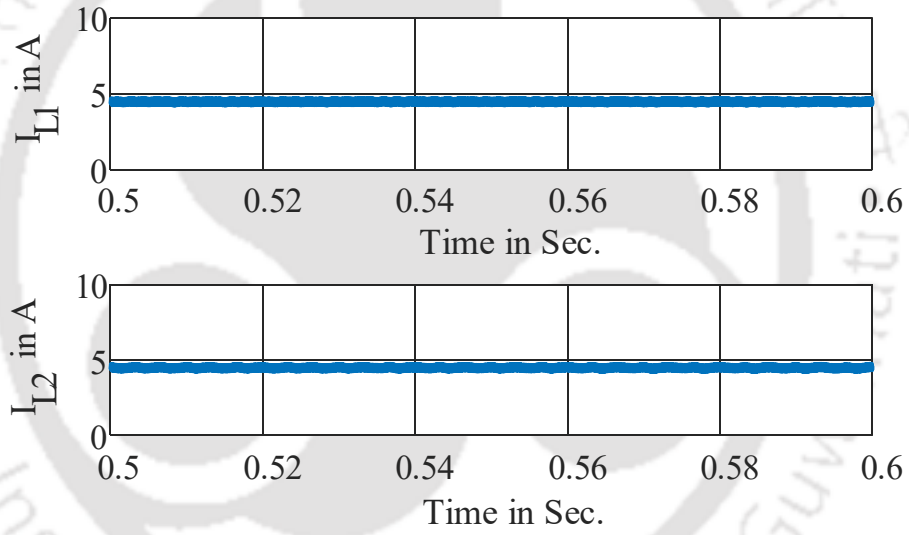


Fig. 5.7. Simulation results of inductor currents of the qZSI.

solution of the system of nonlinear equations using the fsolve function in MATLAB, ensuring that the impedance network parameters meet all specified operating constraints. Based on the refined results from the analytical calculations, the impedance network is realized using identical capacitors and inductors; $C_1 = C_2 = 56$ μF and $L_1 = L_2 = 3$ mH. The inverter is powered by a constant input DC voltage of $V_{\text{in}} = 36$ V. Under the control of the simple boost strategy, the qZSI effectively boosts the input voltage to a peak DC-link voltage of $\widehat{V}_{PN} = 118.40$ V. This significant voltage amplification demonstrates the efficacy of inherent boost functionality and validates the voltage gain predicted by the analytical design model of the

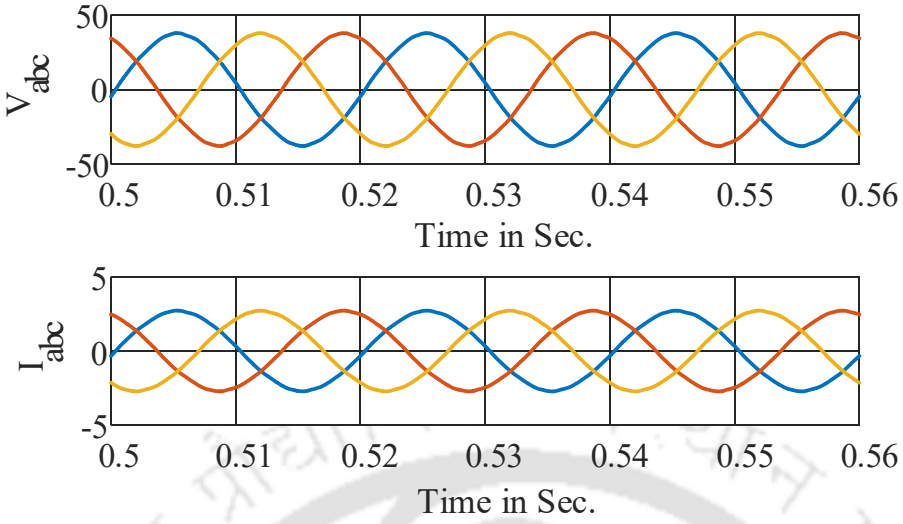


Fig. 5.8. Simulation results of three phase voltages and currents of the qZSI.

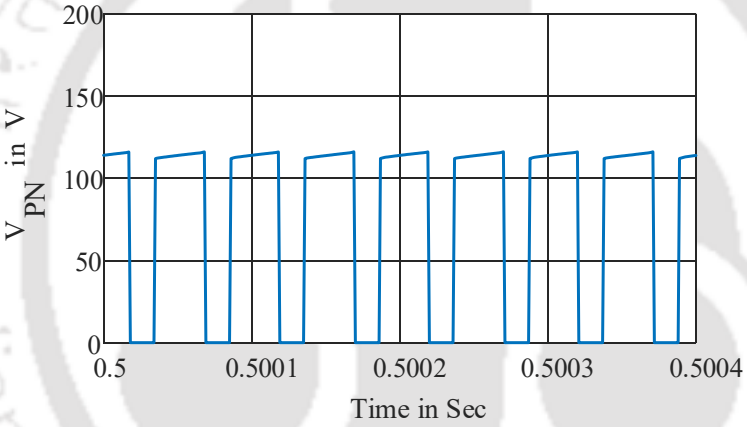


Fig. 5.9. Simulation results of dc-link voltage of the qZSI.

qZSI. During the simulation, the average voltage across the impedance network capacitors was recorded as $\overline{V}_{C_1}$ = 76.90 V and $\overline{V}_{C_2}$ = 41.50 V. These values confirm the proper charge distribution across the capacitors and are consistent with the expected steady-state voltages derived from the waveform analysis. The average inductor currents are observed to be $\overline{I}_{L_1}$ = $\overline{I}_{L_2}$ = 4.50 A, indicating a balanced and stable operation of the energy storage elements within the impedance network. The symmetry in current sharing also implies that the design supports thermal and electrical stress balancing across the inductive components. A modulation index of M = 0.62 is applied to the inverter during the simulation. This value optimizes the boosted DC-link voltage while maintaining linear modulation. As a result, the inverter generated a peak phase voltage of $\widehat{v}_m$ = 36.60 V and a peak phase current of $\widehat{i}_m$ = 2.60 A at the output.

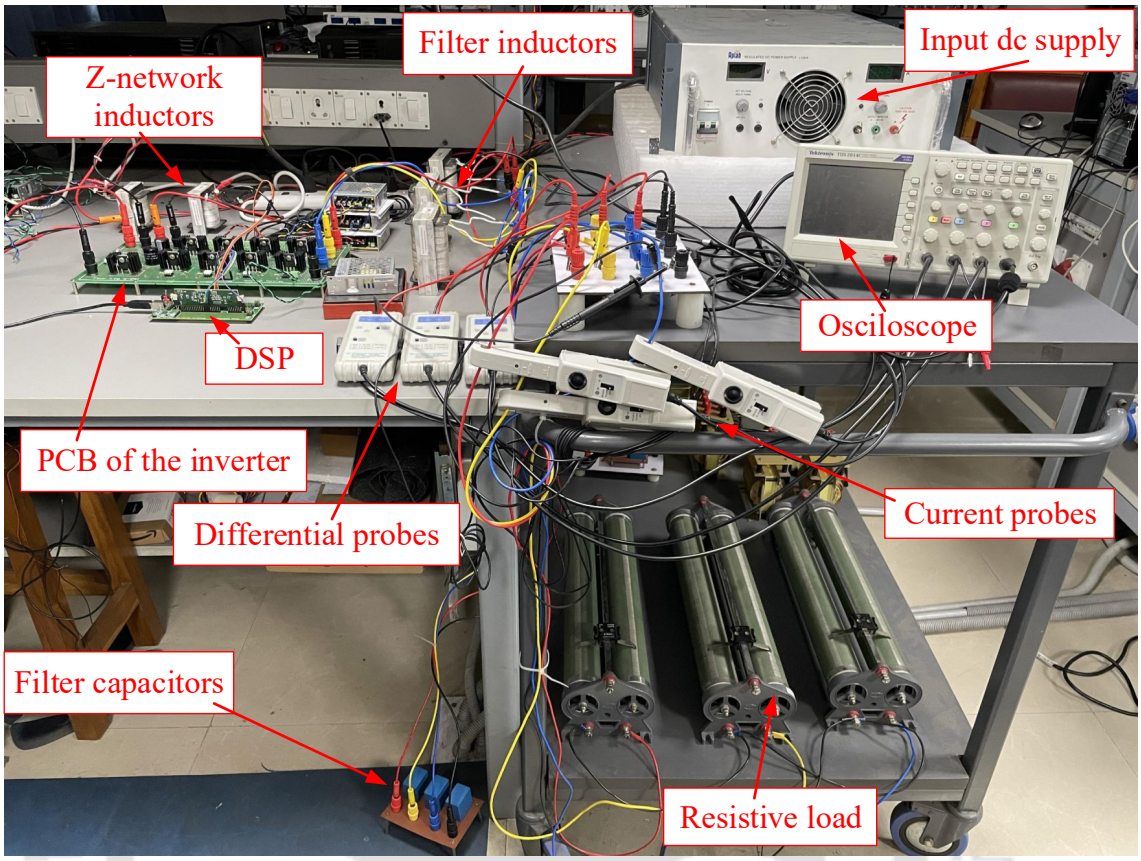
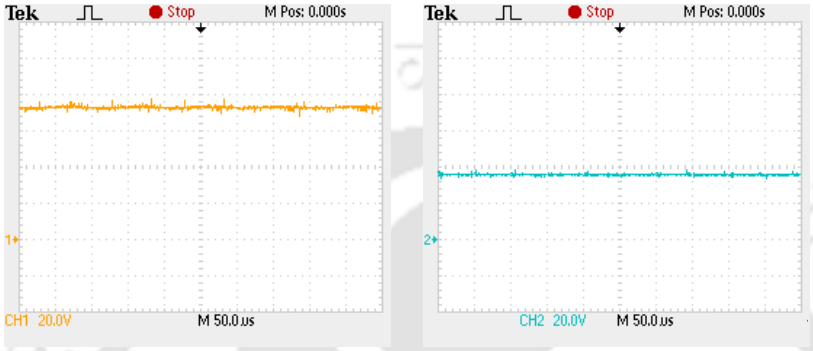


Fig. 5.10. Experimental setup of the qZSI.

These values are in close agreement with theoretical expectations for a purely resistive load operating at unity power factor, further confirming the accuracy of output voltage control of the inverter and its capability to deliver sinusoidal, in-phase voltage and current waveforms to the load. The ripple factors of capacitor voltages and inductor currents of the simulated waveforms are given in Table 5.4. The detailed simulation waveforms provide further insights into the system performance. The inductor currents and capacitor voltages waveforms are depicted in Fig. 5.6. and 5.7. respectively. Fig. 5.8. shows the phase voltages and currents of the inverter. The DC-link voltage waveform is shown in Fig. 5.9. The simulation outcomes closely match the values predicted by the analytical design approach, thereby validating the effectiveness and accuracy of the proposed method for component sizing and performance prediction of qZSI system.

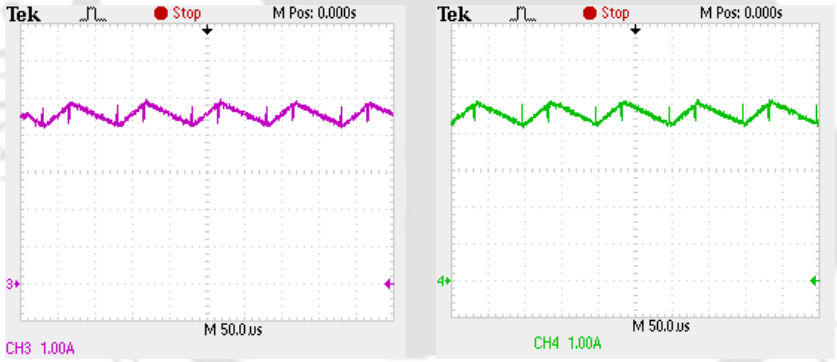
5.4.2 Experiment results of qZSI

A laboratory prototype is developed and tested to experimentally validate the theoretical analysis and simulation results of the qZSI. The experimental setup, shown in Fig. 5.10., replicates the parameters and operating conditions used in the analytical and simulation



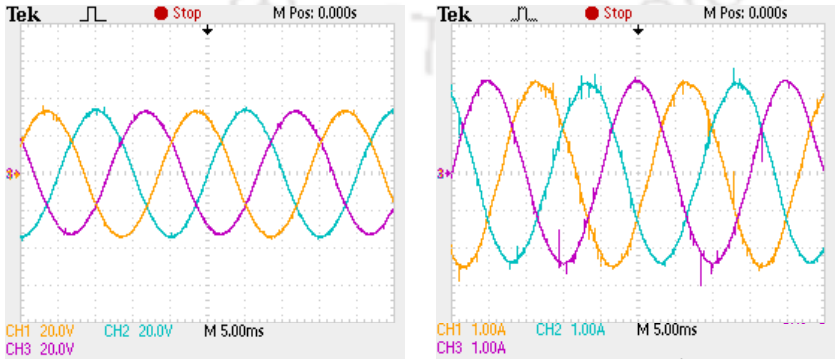
(a) **(b)**

Fig. 5.11. The measured voltage across capacitors of qZSI (a) C_1 (V_{C_1}), and (b) C_2 (V_{C_2}).



(a) **(b)**

Fig. 5.12. The measured current through inductors of qZSI (a) L_1 (I_{L_1}), and (b) L_2 (I_{L_2}).



(a) **(b)**

Fig. 5.13. Experimental results of the qZSI (a) three phase AC voltage, and (b) three phase AC current.

studies. This allows for a direct and meaningful comparison of results across all three domains. During the experimental evaluation, the inverter is powered with a DC input voltage of V_{in}= 36 V. Under these conditions and with the application of simple boost control, the capacitor voltages are measured to be $\overline{V}_{C_1}$ = 76.40 V and $\overline{V}_{C_2}$ = 38.40 V, which are in close agreement with the corresponding simulation and theoretical values. Similarly, the average inductor currents are recorded as $\overline{I}_{L_1} = \overline{I}_{L_2}$ = 4.45 A, indicating stable and symmetric current sharing in the impedance network, and thereby validating the proper sizing and balancing of the inductive components. A modulation index of M = 0.62 is applied during the experimental tests, consistent with the value used in simulation. As a result, the inverter generated a peak phase AC voltage of $\widehat{v}_m$ = 35.60 V and a peak phase AC current of $\widehat{i}_m$ = 2.55 A across the three-phase resistive load. The dynamic behavior of the system is further illustrated through the experimental waveforms. The capacitor voltage waveforms are depicted in Fig. 5.11. Fig. 5.12. shows the corresponding inductor current profiles. The ripple factors of the capacitor voltages and inductor currents, as obtained from the experimental waveforms, are presented in Table 5.4. Both sets of waveforms confirm the low-ripple operation of the system, which is a direct result of the impedance network design guided by the 2% capacitor voltage ripple and 5% inductor current ripple constraints. The inverter output phase voltages and currents, captured in Fig. 5.13., display clean sinusoidal waveforms with minimal distortion, highlighting the effectiveness of the chosen modulation strategy and the integrity of the control implementation.

Table 5.4. Comparison between theoretical, simulation, and experimental results

Parameters	**Theoretical**	**Simulation**	**Experiment**
$\Delta V_{C_1}/\overline{V}_{C_1}$	0.02	0.012	0.015
$\Delta V_{C_2}/\overline{V}_{C_2}$	0.02	0.017	0.019
$\Delta I_{L_1}/\overline{I}_{L_1}$	0.05	0.047	0.049
$\Delta I_{L_2}/\overline{I}_{L_2}$	0.05	0.047	0.049

5.5 Summary

The dynamic and static operating states of qZSI have been thoroughly analyzed, with the corresponding steady-state equations derived for each mode of operation. In practical implementations, the undesirable static states where current or voltage may momentarily stagnate can be effectively mitigated or completely avoided by carefully designing the impedance network parameters. Proper selection of inductor and capacitor values ensures continuous energy transfer and maintains the desired switching dynamics. Small-signal ripple assumptions are employed in the analytical modeling and design process to justify the linear approximation of capacitor voltage and inductor current waveforms. This simplification is valid when the ripple magnitudes are sufficiently small relative to the average values, a condition that can be ensured by choosing appropriately large inductors and capacitors. Using this approximation, a set of nonlinear and algebraic equations is formulated, from which the component values of the impedance network are determined by solving the system of simultaneous equations. The designed parameters were subsequently validated through simulation and experimental testing, confirming the accuracy and effectiveness of the proposed design method. The results showed strong agreement between theoretical predictions and practical outcomes, further demonstrating the reliability of the linearized approach for initial design. However, parasitic resistances in the practical implementation of inductors and capacitors introduce non-idealities in the system. These parasitics cause power losses within the impedance network, reducing the voltage gain of the qZSI compared to the ideal case. While relatively small, this gain drop must be considered during the design phase to ensure that the inverter meets its voltage boosting requirements under real operating conditions.

Note: This work,"Impedance Network Design of the Quasi-Z-Source Inverter," *2022 22nd National Power Systems Conference (NPSC)*, New Delhi, India, 2022, pp. 172-177, DOI: 10.1109/NPSC57038.2022.10069748.

CHAPTER 6

Concluding remarks and future scope of research

6.1 Concluding remarks

This thesis introduces three novel ZSI topologies, DA-SLEBqZSI, CA-SLEBqZSI, and improved-EBqZSI, developed through strategic modifications of the impedance network configuration. A comprehensive steady-state analysis is conducted for both shoot-through and non-shoot-through states. Mathematical expressions for the boost factor are derived for each proposed topology, accompanied by a design methodology to determine the appropriate impedance network parameters. Detailed simulations are carried out using PSCAD software to validate the performance of the proposed topologies. The simulation outcomes are further verified through experimental waveforms, demonstrating real-time operational viability.

Additionally, the thesis presents an in-depth design framework for the impedance network of qZSI. It includes a thorough analysis of both static and dynamic operating states. The conditions required to prevent static state operation in qZSI are identified and discussed. A practical design example is provided and validated through both simulation and experimental results.

The detailed conclusions drawn from the individual chapters are given below.

Chapter 2, introduces two novel inverter topologies, DA-SLEBqZSI and CA-SLEBqZSI, developed through strategic modifications of the impedance network configuration. A key advantage of both configurations is their enhanced voltage boost capability, achieved even at relatively low shoot-through duty ratios. The higher boost factors offered by these topologies also support operation at increased modulation indices, which reduces voltage stress across inverter switches. This enhances system reliability, lowers switching losses, and enables low-rated, potentially more cost-effective semiconductor devices. The performance of the proposed inverters is thoroughly evaluated through theoretical analysis, which includes the derivation of expressions for boost factor, voltage gain, component stress, and steady-state behavior. These analytical findings are validated through detailed simulations using the

PSCAD platform and further corroborated by experimental testing on a hardware prototype. The CA-SLEBqZSI topology demonstrates superior performance, achieving the highest boost factor and voltage gain among comparable impedance-source inverter designs. This is accomplished with minimal added complexity, requiring only one additional capacitor while substituting a diode.

Chapter 3, introduces a novel inverter topology, improved-EBqZSI, developed through strategic modifications to the conventional impedance network. The performance of this proposed topology is rigorously assessed through a combination of theoretical analysis, comprehensive simulation studies, and experimental validation. The improved-EBqZSI exhibits superior operational characteristics to existing ZSI variants, notably its enhanced voltage boosting capability at reduced shoot-through duty ratios. A key advantage of the improved-EBqZSI lies in its ability to achieve higher voltage gain while imposing lower voltage stress on the semiconductor switches. This allows operation at higher modulation indices, improving overall system efficiency. Additionally, it enables the use of lower-rated, cost-effective switching devices, contributing to better thermal performance and overall cost-efficiency in practical applications. Simulation results are validated through experimental testing on a laboratory-scale hardware prototype. The experimental results show strong agreement with both theoretical predictions and simulation outcomes. Key performance indicators, including DC-link voltage levels, capacitor voltage profiles, inductor currents, and output AC waveforms, closely match expected values, affirming the robustness, efficiency, and real-world viability of the improved-EBqZSI design.

In **Chapter 4**, dynamic and static operating states of the qZSI have been comprehensively analyzed, with steady-state equations derived for each mode of operation. In practical implementations, undesirable static states where voltage or current may temporarily stagnate can be effectively mitigated or avoided through careful impedance network design. Small-signal ripple assumptions are employed to facilitate analytical modeling and simplify the design process. These assumptions allow linear approximations of the capacitor voltage and inductor current waveforms, valid when the ripple magnitudes are small relative to

their average values. The derived design parameters are validated through simulation and experimental testing, demonstrating strong alignment between theoretical predictions and actual performance. This confirms the accuracy and practicality of the linearized design approach, particularly for initial design iterations.

6.2 Future scope of research

The work presented in this thesis can be further extended in the future. Some of the future scopes of research that can be further explored from this thesis are given as follows:

(1) While the thesis focuses primarily on topology and impedance network design, integrating advanced control strategies such as MPC or adaptive proportional-integral (PI) controllers could further optimize the performance of the proposed inverters under dynamic operating conditions. These techniques enhance system responsiveness, efficiency, and fault tolerance in real-time applications.

(2) The proposed topologies can be further evaluated for grid-connected applications, including compliance with grid codes (e.g., IEEE 1547 or EN 50549) and performance under grid disturbances such as voltage sags, frequency fluctuations, and harmonics.

(3) Future work can explore the implementation of the proposed topologies using wide-bandgap semiconductor devices such as silicon carbide (SiC) and gallium nitride (GaN), which support higher switching frequencies, reduced losses, and more compact designs. This could further reduce passive component size and overall system volume. Also, it aims to minimize the cost per watt while maximizing efficiency, particularly in applications like residential PV systems and electric vehicle drives.

List of Publications

Journal

1. **A. Paikray**, D. Srivastava and S. K. Nayak, "Switched-Inductor Extended-Boost Quasi-Z-Source Inverter," in ***IEEE Access***, DOI: 10.1109/ACCESS.2025.3569076.

Under Review

1. **A. Paikray**, S. Prudhvi and S. K. Nayak, "Improved Enhanced-Boost Quasi-Z-Source Inverter," in ***IEEE Transactions on Circuits and Systems II: Express Briefs***.

Conferences

1. **A. Paikray**, S. Prudhvi and S. K. Nayak, "Impedance Network Design of the Improved Enhanced-Boost Quasi-Z-Source Inverter," *2023 IEEE 3rd International Conference on Smart Technologies for Power, Energy and Control (STPEC)*, held in Bhubaneswar, India, Dec. 2023, pp. 1-6, DOI: 10.1109/STPEC59253.2023.10431290.
2. **A. Paikray**, S. Prudhvi and S. K. Nayak, "Impedance Network Design of the Quasi-Z-Source Inverter," *2022 22nd National Power Systems Conference (NPSC)*, New Delhi, India, 2022, pp. 172-177, DOI: 10.1109/NPSC57038.2022.10069748.
3. **A. Paikray**, S. Prudhvi and S. K. Nayak, "Improved Enhanced-Boost Quasi-Z-Source Inverter," *2022 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Jaipur, India, 2022, pp. 1-6, DOI: 10.1109/PEDES56012.2022.10080512.

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