INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI
SHORT ABSTRACT OF THESIS

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Enhancement of SBST Techniques for Detection of Processor Faults

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SHORT ABSTRACT

At-speed testing of processors is extremely difficult with any external testing technique, therefore, Software-based self-testing (SBST) is introduced for efficient at-speed testing of processors. Evolutionary approaches are used for the automated synthesis of SBST codes. However, SBST development has been exceedingly difficult due to the sophisticated circuits of the modern processor hardware. In addition, the momentary nature of faults necessitates a careful and extensive test application. This thesis comprises four major contributions which address the challenges in SBST code synthesis, application, and optimization phases.

In the first contribution, we present a greedy cover-based strategy for automated SBST code synthesis, where the instruction sequences that detect the freshly identified faults are preserved throughout the evolutionary process to identify the hard-to-test faults of the processor. This preservation of test programs that detect hard-to-test faults in the evolutionary process increases the fault coverage. Also, a selection probability is estimated from the testability properties of the processor components and assigned to every instruction to accelerate the test synthesis. In addition, we have used high-level behavioral fault models for modeling processor hardware faults without using gate-level details of the processor. In this contribution, we synthesize high-quality SBST programs with 96.32% fault coverage for a MIPS processor and 95.8% fault coverage for a Leon3 processor with the detection of 40% of the hard faults.

However, the test synthesis time required for automated SBST synthesis is high for the existing evolutionary approaches. So, an advanced SBST technique, termed as Rapid SBST (RSBST), is proposed in the second contribution that reduces the overall test synthesis time by reusing the simulation responses of existing test programs of identical observability. The fault diagnostic characteristics of test programs are reused for the test quality evaluation if these test programs produce similar values in the observable locationsof the processor. We exploit this reusability to enhance the speed of the test synthesis process. In a nutshell, this contribution develops a faster technique for synthesizing high-quality SBST programs. This strategy develops test solutions with 96.1% fault coverage for the MIPS processor in 90 hours and test solutions with

95.5% coverage for the Leon3 processor in 98 hours. To achieve this, we have exploited the reusability of 82.1% of test solutions for the MIPS processor and the reusability of 80.8% of test solutions for the Leon3 processor during the evolutionary test synthesis.

In the third contribution, the test codes are optimized with the help of enhanced assembly code compaction techniques. The tradeoff between test compaction and computational effort required for the test compaction is dealt with two compression stages. In the first stage, the test program is preprocessed using a novel instruction removal technique that makes use of data dependence graphs to identify and eliminate independent and redundant instruction groups. In the second stage, an instruction restoration technique delivers a high compaction rate with the help of low-cost, high-level logic simulations for test quality evaluation. In this contribution, SBST programs are efficiently compacted after test synthesis phase by identifying and removing 19% of the redundant instructions of the SBST program consuming 72.24% of the computational cost of instruction-by-instruction redundancy check.

In the online test application mode, SBST schemes provide high fault coverage but incur long detection latencies in case of intermittent faults, due to large size and longer execution time of the test codes. In the last contribution, a fragmented SBST method is developed which develops a reliable set of SBST code fragments of minimal fault detection latency to detect the intermittent faults and enhance the reliability of the system. Also, these code fragments suffer inconsiderable overall fault coverage drop, compared to the coverage of the complete SBST test code. In this contribution, test programs with a better trade-off between execution time and fault coverage are selected during the test synthesis phase and are applied for the online testing of the processor. In our experiment, a group of 20 smaller test programs of 80% fault coverage and adequate overall coverage of 96% is observed to have maximum reliability to replace the optimal test program with 96.3% for the online testing of MIPS processor for our input data set.