AVERAGE MODELING AND DC-LINK CAPACITOR VOLTAGE REGULATION OF SRF-DQ CONTROLLED SINGLE-PHASE ANPCI FOR SOLAR AND WIND POWER APPLICATIONS

Jagath Vallabhai Missula

AVERAGE MODELING AND DC-LINK CAPACITOR VOLTAGE REGULATION OF SRF-DQ CONTROLLED SINGLE-PHASE ANPCI FOR SOLAR AND WIND POWER APPLICATIONS

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By

JAGATH VALLABHAI MISSULA

Department of Electronics and Electrical Engineering,

Indian Institute of Technology Guwahati,

Guwahati, Assam, INDIA, 781039

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Dedicated

to

my beloved parents,

Smt. Missula Kamala Kumari,

and

Sri. Missula Suryanarayana

CERTIFICATE

This is to certify that the thesis entitled "**Average Modeling and DC-Link Capacitor Voltage Regulation of SRF-dq Controlled Single-Phase ANPCI for Solar and Wind Power Applications**", submitted by **Jagath Vallabhai Missula** (146102011), a Research Scholar in the *Department of Electronics and Electrical Engineering, Indian Institute of Technology Guwahati*, for the award of the degree of **Doctor of Philosophy**, has been carried out by him under my supervision and guidance. The thesis has fulfilled all requirements as per the regulations of the institute and in my opinion has reached the standard needed for submission. The results embodied in this thesis have not been submitted to any other University or Institute for the award of any degree or diploma.

Date:

Guwahati.

Dr. Ravindranath Adda,
Assistant Professor,
Dept. of Electronics and Electrical Engineering,
Indian Institute of Technology Guwahati,
Guwahati, Assam, INDIA, 781039.

Date:

Guwahati.

Dr. Praveen Tripathy,
Associate Professor,
Dept. of Electronics and Electrical Engineering,
Indian Institute of Technology Guwahati,
Guwahati, Assam, INDIA, 781039.

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ABSTRACT

A Voltage Source Inverter (VSI) converts DC voltage to ac voltage with adjustable magnitude and frequency. VSIs have numerous industrial applications, such as, uninterrupted power supplies, adjustable speed drives, High Voltage DC (HVDC) transmission, Flexible AC Transmission Systems (FACTS), renewable power generation, etc. Based on the number of output voltage levels, the VSIs can be classified as two-level inverters and Multi-Level Inverters (MLIs). Due to the high voltage and large power handling capability and reduced Total Harmonic Distortion (THD) in the output voltage, MLIs are preferred to two-level inverters, mostly in the medium and high-power applications. Neutral Point Clamped (NPC) MLI, Flying Capacitor (FC) MLI and cascaded H-bridge MLI are the most popular topologies among the various MLIs available in the literature.

An Active Neutral Point Clamped (ANPC) Inverter is a combination of two basic MLI topologies, viz., NPC-MLI and FC-MLI. Hence it combines the features of both these MLI topologies. Unlike NPC-MLI, the ANPC Inverter (ANPCI) has redundant switching states to balance the capacitor voltages. Due to the increased number of switching states in ANPCI, a loss-balancing control can be implemented for equal distribution of power losses and junction temperature among its switches. Therefore, the power-handling capability of ANPCI can be increased further compared with the NPC-MLI. Owing to its advantages, the ANPCI has been proposed as an alternative to the NPC-MLI in medium voltage drives and renewable energy applications. Also, it is worth noting that the five-level active-neutral-point-clamped converter is the only commercially available five-level multilevel converter, which does not require multiple isolated DC sources.

Due to the advantages and increasing applications of the ANPCI, this thesis presents the detailed analysis, modeling and control techniques of single-phase ANPCI. Detailed operation and steady-state analysis of single-phase ANPCI in different switching states is given in this thesis. Also, the thesis describes different Pulse-Width-Modulation (PWM) strategies

for the ANPCI and it is shown that the Phase Disposition and Shifting (PDS) PWM technique results in low THD output voltage. Different Capacitor Voltage Balancing Strategies (CVBS) are described and customized for an eight-switch, five-level ANPCI. For the closed-loop operation of the ANPCI, a Synchronous Reference Frame (SRF) dq domain controller has been presented.

Further, a Dynamic Average Circuit Model (DACM) has been developed for the single-phase ANPCI in this thesis. Unlike the Analytical Average Value Model (AAVM) and Parametric Average Value Model (PAVM), the DACM developed in this thesis does not have complex mathematical equations. Also, the model can be directly simulated using any standard circuit simulation software. The model is also modular in nature and valid for all the operating conditions of the converter. The model significantly reduces the computational resources and execution times while analyzing or designing power electronic systems involving ANPCI. Extensive experimental and simulation results are given in the thesis to validate the operation, capacitor voltage balancing strategy and DACM of the ANPCI. The results demonstrate the advantages and the strength of the DACM developed for ANPCI.

In this thesis, it is also proposed to integrate an external chopper circuit to the DC-link of ANPCI, to regulate the ripple in DC-link capacitor voltages. Various suitable control techniques are also presented for the chopper circuit to reduce the DC-link capacitor voltage ripple while limiting the current flowing through various elements of chopper circuit. The external chopper circuit augments the CVBS in regulating the DC-link capacitor voltages of ANPCI. Employing an external circuit for voltage ripple reduction also helps in reduction of the DC-link capacitor values and in increasing the power density and reliability. The operation of chopper integrated ANPCI and its control techniques are verified using simulation and experiment considering various test cases.

Further in this thesis, the chopper integrated ANPCI has been proposed as a power electronic interface in solar and wind power generation systems. The operation of these systems is described in detail and the performance is validated using PSCAD simulation.

CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

A Voltage Source Inverter (VSI) converts DC input voltage to an ac output voltage with adjustable magnitude and frequency. The VSIs are widely used in uninterruptible power supplies, adjustable speed drives, High Voltage DC (HVDC) transmission, Flexible AC Transmission Systems (FACTS), custom power devices, renewable power generation, etc., [1–4]. The circuit diagram of a single-phase VSI consists of power semiconductor switches arranged as either half-bridge or full-bridge configuration, as shown in Fig. 1.1. The choice of the switching device depends on the power level and application of the converter. In general, an Insulated-Gate Bipolar Transistor (IGBT) with an antiparallel diode is used as the switching device for small and medium power applications. The antiparallel diodes enable four-quadrant operation of the converter which is essential for operation at any power factor. The switching signals for the switches are generated using Pulse-Width-Modulation (PWM) techniques to provide a sinusoidal output voltage with low Total Harmonic Distortion (THD).

Based on the number of output voltage levels, the VSIs can be classified as two-level inverters and multilevel inverters (MLIs) [5–8]. For the two-level inverter, shown in Fig. 1.1, the output voltage of each leg (i.e., v_{an} and v_{bn}) can be either $+\frac{V_{DC}}{2}$ or $-\frac{V_{DC}}{2}$. The number of voltage levels in the output voltage waveform of an MLI depends on the number of switches in the phase-leg. Fig. 1.2(a) shows one phase-leg of a three-level inverter, which can generate three output voltage levels, viz., $+\frac{V_{DC}}{2}$, 0 and $-\frac{V_{DC}}{2}$. Similarly, the five-level inverter shown in Fig. 1.2(b) can generate five voltage levels, viz., $+\frac{V_{DC}}{2}$, $+\frac{V_{DC}}{4}$, 0, $-\frac{V_{DC}}{2}$ and $-\frac{V_{DC}}{4}$. As the number of levels in the output voltage increases, the quality of output voltage will improve. Thus, the advantage of MLIs is that they can reduce the

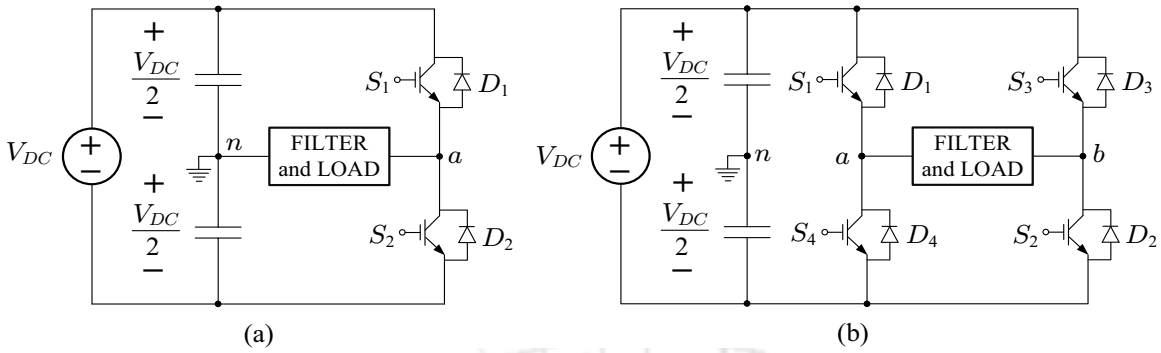


Fig. 1.1. Circuit diagram of (a) Half-bridge VSI, and (b) Full-bridge VSI.

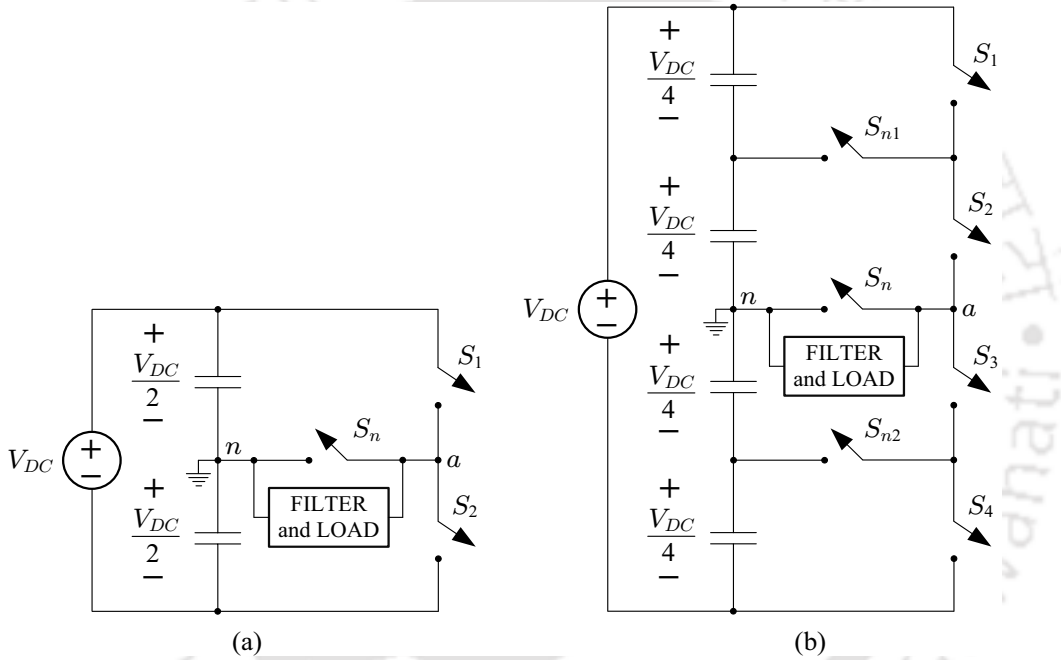


Fig. 1.2. Basic representation of a (a) three-level VSI, and (b) five-level VSI.

harmonic content in the ac output voltage of the inverter compared to the two-level VSIs [5,9]. Therefore, the size of passive filter on the ac-side will also reduce. Another advantage is that the MLIs can reduce the voltage ratings of the power semiconductor devices and also the switching loss [10, 11]. The main features of MLIs can be summarized as below:

1) MLIs generate output voltage with multiple smaller voltage steps. Due to this the output voltage waveform is closer to a sinusoidal signal compared to that of a two-level VSI. Thus, the harmonic content in the output voltage decreases and the ac side filter size also reduces. This also results in lower $\frac{dv}{dt}$ and low common-mode voltages

[11–13].

2) Due to the ability to generate multi-step output voltage, the MLIs switching frequency can be reduced compared to that of a two-level VSI. This leads to low switching loss and higher efficiency [11].

3) Unlike two-level VSI, the voltage stress of each switch in the MLI is less than the input DC-link voltage. Hence with low voltage rating switches, MLIs can be operated at fairly high voltages, which makes them suitable for medium- and high-power applications [14].

4) The MLIs input current has low harmonic content compared to that of a two-level VSI [11].

Ever since the concept of multilevel power conversion is introduced, researchers have introduced several MLI topologies, some of which are listed in Fig. 1.3. However, only few of these topologies are found to be suitable for industrial applications. The three topologies which are widely used in commercial applications are: 1) Neutral Point Clamped (NPC) MLI, 2) Flying Capacitor (FC) MLI and 3) Cascaded H-Bridge (CHB) MLI. These converters are often considered as classical or traditional MLIs.

By combining the features of two classical MLIs, viz., NPC-MLI and FC-MLI, an Active Neutral Point Clamped Inverter (ANPCI) has been developed. The ANPCI combines the important features of NPC-MLI and FC-MLI. Also, the power-handling capability of ANPCI is higher compared to both of these MLIs. Owing to its advantages, the ANPCI has been proposed as an alternative to the NPC-MLI in medium voltage drives and renewable energy applications. Due to the advantages and suitability for wide commercialization, this thesis presents a detailed analysis and average modeling of a single-phase five-level ANPCI. Also, an auxiliary circuit-based techniques are presented to regulate the DC-link capacitor voltages of ANPCI. Further, the operation of ANPCI based solar and wind power generation systems is described in this thesis.

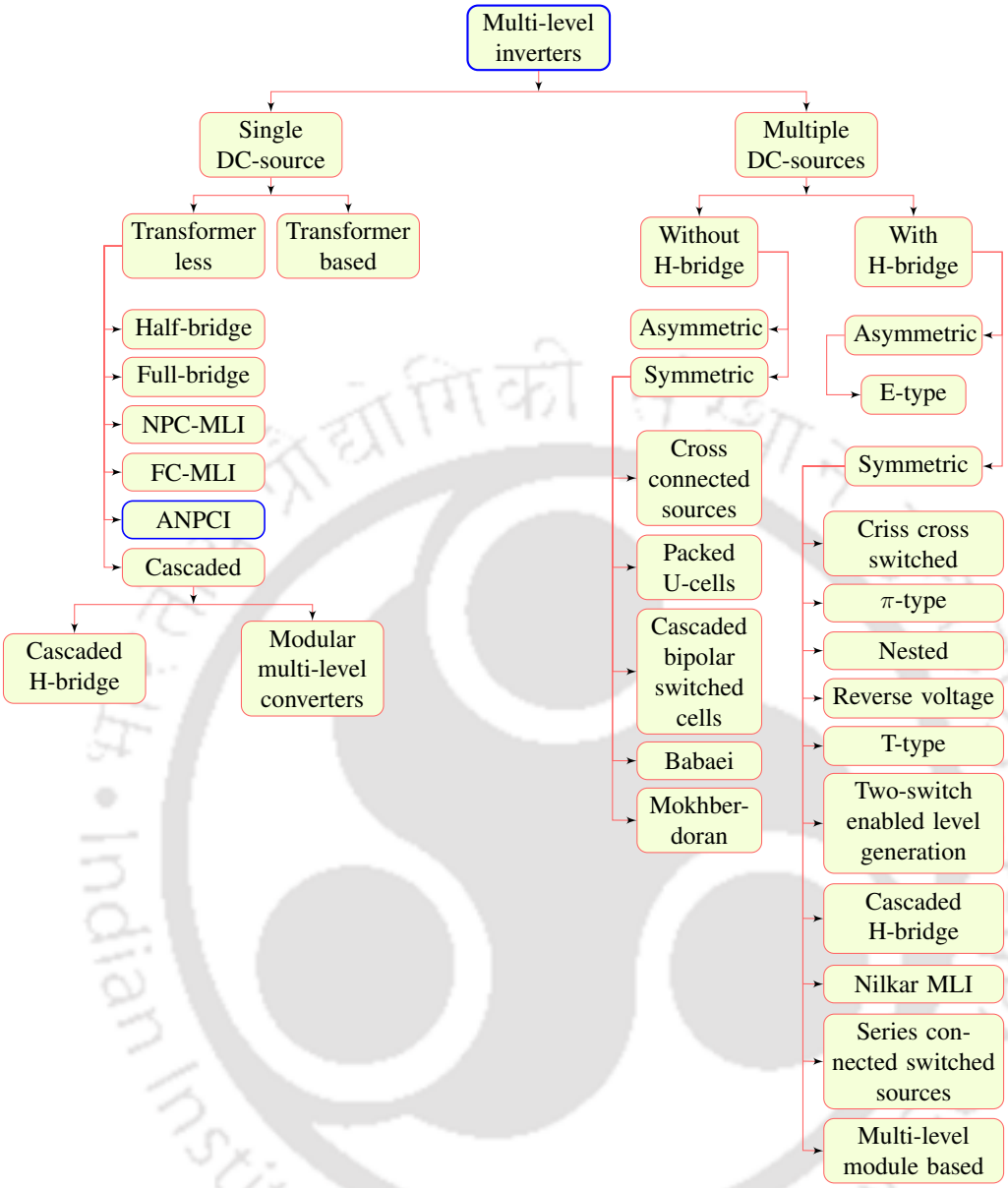


Fig. 1.3. Some of the MLI topologies from the literature.

The following section, i.e., Section 1.2 presents a review of three classical MLIs, viz., NPC-MLI, FC-MLI and CHB-MLI. Section 1.3 introduces the ANPCI topology and the existing contributions related to this converter. Research motivation and objectives of the thesis are presented in Section 1.4. Section 1.5 describes the organization of the thesis and Section 1.6 provides the concluding remarks for this chapter.

1.2 REVIEW OF CLASSICAL MLIS

As mentioned in Section 1.1 and Fig. 1.3, there are several multilevel inverter topologies proposed by the researchers in the last few decades. Each of these topologies have their own set of advantages and drawbacks. However, the three topologies, viz., NPC-MLI, FC-MLI and CHB-MLI are widely researched from many operational and design aspects of power electronic converters. Also, these topologies are widely accepted ones for commercialization by many manufacturers working in the field [6, 15]. The circuit diagram and operation of most of the MLI topologies in the literature can be directly or indirectly related to the basic principles of NPC-MLI, FC-MLI and CHB-MLI. Hence these converters are generally considered as classical MLI topologies in the literature.

The following three sub-sections describe the circuit diagrams, switching states and important features of these three classical MLIs.

1.2.1 Neutral Point Clamped Multi-Level Inverter (NPC-MLI)

The circuit diagram of a three-level neutral point clamped inverter is shown in Fig. 1.4, where a series combination of two capacitors C_1 and C_2 is connected across the DC voltage source, V_{DC}. The voltage across each of these DC-link capacitors is equal to $\frac{V_{DC}}{2}$. This converter consists of four switches S_1 to S_4 each with an antiparallel diode. In addition, there are two clamping diodes D_{t1} and D_{t2}. In the circuit of Fig. 1.4, the midpoint of the DC-link capacitors, 'n' is considered as the neutral point and the terminal 'a' is considered

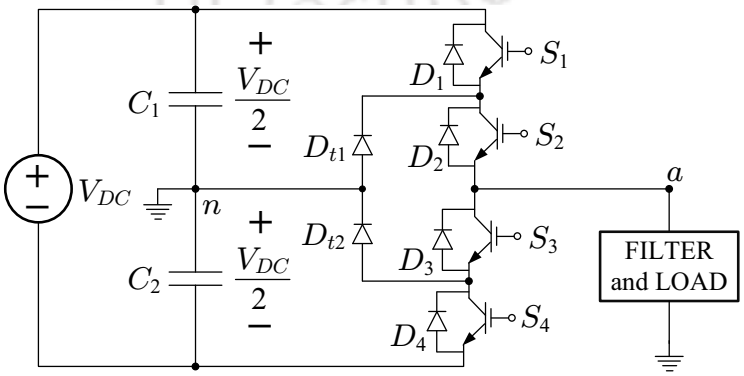


Fig. 1.4. Circuit diagram of single-phase three-level NPC-MLI.

as the output terminal. The clamping diodes help to limit the voltage stress of each switch to half of the DC-link voltage, i.e., $\frac{V_{DC}}{2}$. The switches S_1 and S_4 are the main switches which are controlled independently using a PWM technique. The switches S_2 and S_3 are the auxiliary switches, which always operate complimentary to the main switches S_4 and S_1, respectively. When both the main switches are OFF, the auxiliary switches are turned ON to clamp the potential of output terminal 'a' to the neutral point 'n' with the help of clamping diodes D_{t1} and D_{t2}.

Table 1.1 lists the possible switching combinations of the converter and the corresponding output terminal voltage with respect to the neutral point, i.e., v_{an}, to obtain a three-level waveform. Fig. 1.5 shows the output voltage waveform of three-level NPC inverter along with the switching signals. It can be seen that the output voltage (v_{an}) is a three-level waveform. There are different switching schemes in the literature to further reduce the harmonic content in the output voltage [15, 16].

The concept of NPC-MLI can be extended to any number of levels, by increasing the number of DC-link capacitors, switches and clamping diodes. For an N-level output voltage, the NPC-MLI requires $(N-1)$ capacitors, $2{\cdot}(N-1)$ switches and $(N-1)\cdot(N-2)$ clamping diodes.

Fig. 1.6 shows the circuit diagram of a five-level NPC-MLI consisting of four DC-link capacitors C_1 to C_4, eight switches S_1 to S_8 and 12 clamping diodes, D_{t1} to D_{t12}. Here,

Table 1.1. POSSIBLE SWITCHING STATES FOR THE THREE-LEVEL NPC-MLI OF FIG. 1.4

Voltage level	Switch positions			
v_{an}	S_1	S_2	S_3	S_4
$+\frac{V_{DC}}{2}$	1	1	0	0
0	0	1	1	0
$-\frac{V_{DC}}{2}$	0	0	1	1

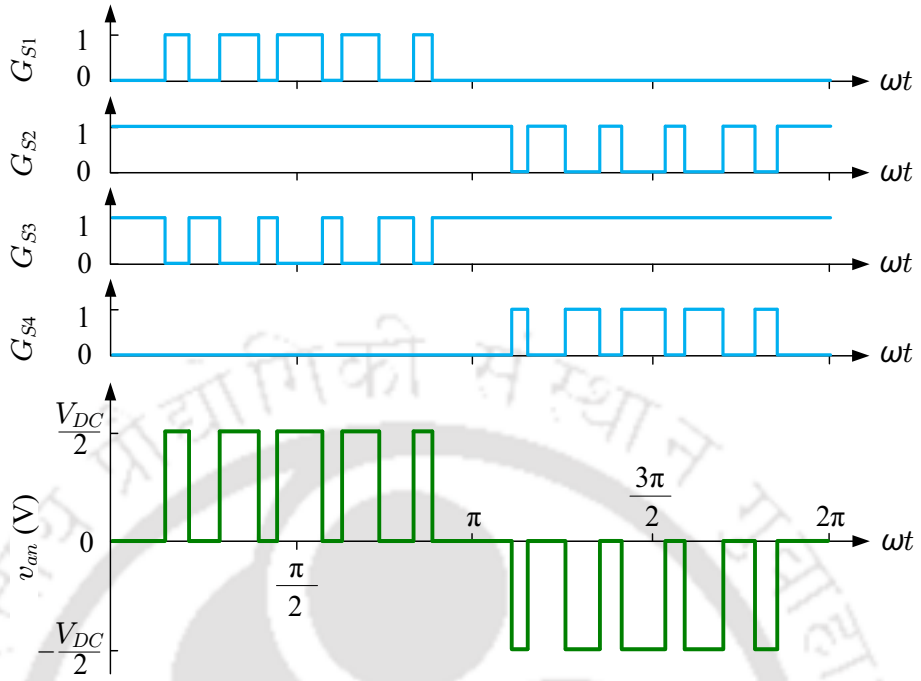


Fig. 1.5. Switching signals and PWM voltage waveform generation for three-level NPC-MLI.

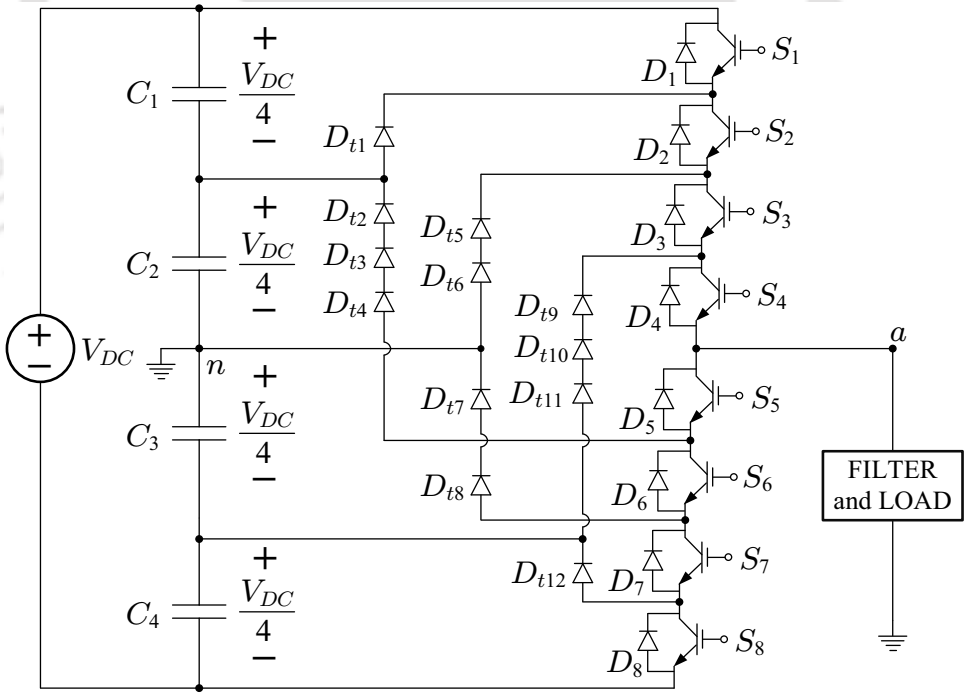


Fig. 1.6. Circuit diagram of single-phase five-level NPC-MLI.

the voltage across each capacitor is equal to $+\frac{V_{DC}}{4}$ and the voltage stress of each switch is limited to $+\frac{V_{DC}}{4}$ through clamping diodes. Also, the number of clamping diodes is chosen

such that the maximum voltage stress across each diode is $\frac{V_{DC}}{4}$. Similar to three-level NPC inverter, the midpoint of the DC-link capacitors is the neutral point 'n' and the midpoint of the switches is the output terminal 'a'. The possible switching states of the five-level NPC inverter are listed in Table 1.2. Fig. 1.7 shows the switching signals and the five-level output voltage waveform. Since the number of levels is increased, the output voltage of five-level NPC inverter will have less harmonic content compared to that of a three-level inverter.

The NPC-MLI offers a simple solution to extend the voltage and power level of the inverter with existing semiconductor switches [16]. Also, in a three-phase NPC-MLI, all the phase legs share a common DC-link. Hence, it can be connected in back-to-back configuration to achieve regenerative braking of drives [15]. However, the commercialization of NPC-MLI is generally limited to its three-level version only. To increase the number of levels, one has to use more DC-link capacitors and clamping diodes, which increases the cost of implementation. Also, due to the absence of redundant switching states, the NPC-MLIs with more than three-levels require complicated circuits for balancing the DC-link capacitor voltages. Also, the clamping diodes introduce additional losses and their reverse recovery currents further increase the switching losses in the converter. One more drawback of the NPC-MLI including its three-level version is uneven distribution of losses among its

Table 1.2. POSSIBLE SWITCHING STATES FOR THE FIVE-LEVEL NPC-MLI OF FIG. 1.6

Voltage level	Switch positions							
v_{an}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$+\frac{V_{DC}}{2}$	1	1	1	1	0	0	0	0
$+\frac{V_{DC}}{4}$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-\frac{V_{DC}}{4}$	0	0	0	1	1	1	1	0
$-\frac{V_{DC}}{2}$	0	0	0	0	1	1	1	1

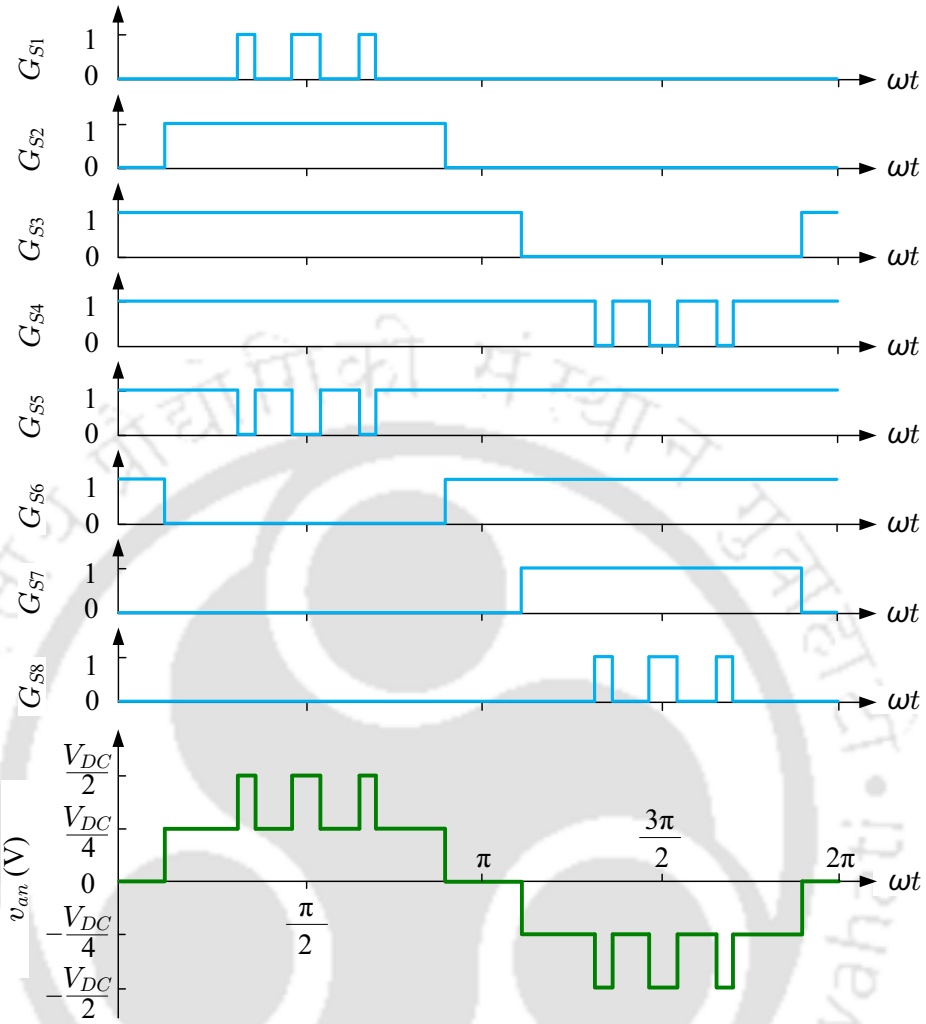


Fig. 1.7. Switching signals and PWM voltage waveform generation for five-level NPC-MLI.

semiconductor devices, which causes unequal junction temperature and limits the switching frequency of the converter.

1.2.2 Flying Capacitor Multi-Level Inverter (FC-MLI)

Fig. 1.8 shows the circuit diagram of the three-level FC inverter topology, where a capacitor C_{t1} is used to clamp the voltage stress of each switch to half of the DC input voltage, $+\frac{V_{DC}}{2}$. The converter can synthesize a three-level waveform of output voltage (v_{an}) using the switching combinations shown in Table 1.3. It can be seen that, unlike NPC-MLI, FC-MLI has two switching combinations to generate zero voltage level. In one of the switching states, the clamping capacitor is charged, while in other switching state, the clamping capacitor is discharged. In order to generate a three-level output voltage, it is

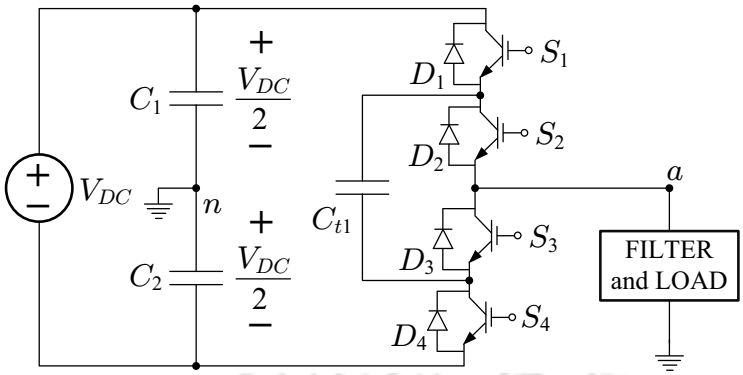


Fig. 1.8. Circuit diagram of single-phase three-level FC-MLI.

Table 1.3. POSSIBLE SWITCHING STATES FOR THE THREE-LEVEL FC-MLI OF FIG. 1.8

Voltage level	Switch positions			
v_{an}	S_1	S_2	S_3	S_4
$+\frac{V_{DC}}{2}$	1	1	0	0
0	1	0	1	0
	0	1	0	1
$-\frac{V_{DC}}{2}$	0	0	1	1

necessary to maintain the clamping capacitor voltage to $+\frac{V_{DC}}{2}$ by proper selection of zero voltage level switching state.

The concept of FC-MLI can be extended to any number of levels, by increasing the number of DC-link capacitors, switches and clamping capacitors. For an N-level output voltage, the FC-MLI requires $(N-1)$ DC-link capacitors, $2{\cdot}(N-1)$ switches and $\frac{(N-1)\cdot(N-2)}{2}$ clamping capacitors.

Fig. 1.9 shows the circuit diagram of a five-level flying capacitor inverter using four DC-link capacitors and multiple clamping capacitors. Here, the voltage stress across each switching device is maintained at $+\frac{V_{DC}}{4}$. The possible switching combinations of this converter to generate a five-level output voltage waveform are listed in Table 1.4. It can be

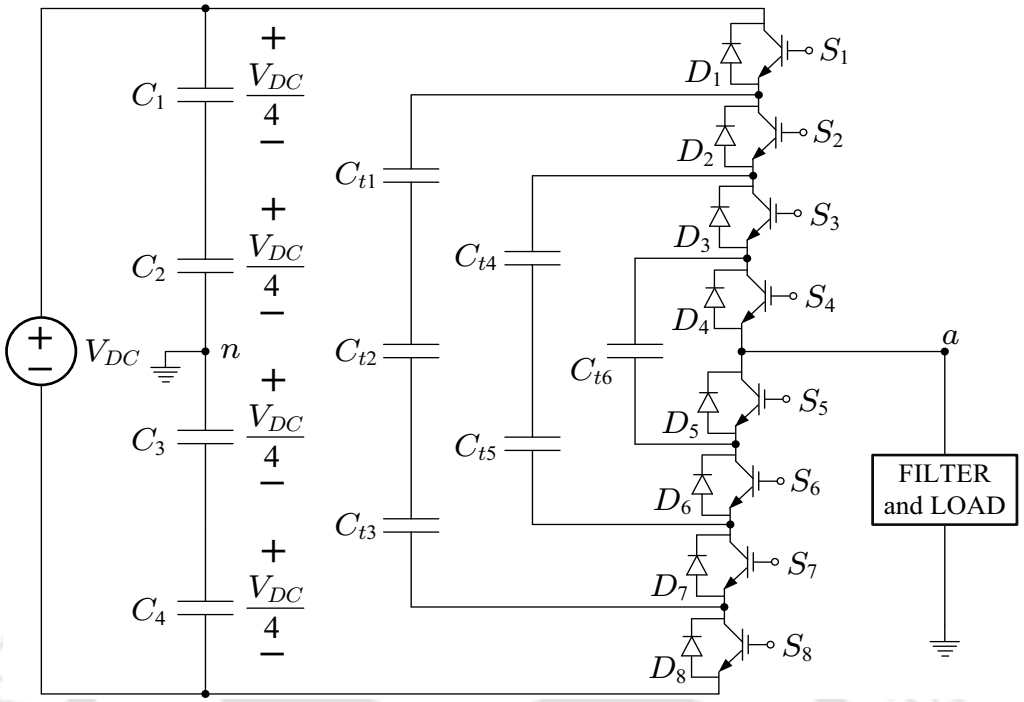


Fig. 1.9. Circuit diagram of single-phase five-level FC-MLI.

seen that, unlike five-level NPC-MLI, the five-level FC-MLI has many redundant switching combinations to synthesize the voltage levels: $+\frac{V_{DC}}{4}$, 0 and $-\frac{V_{DC}}{4}$, with each switching combination having different effect on the clamping capacitor voltages. By proper selection of the switching state, the voltage across each clamping capacitor is always maintained at $+\frac{V_{DC}}{4}$.

The main advantage of FC-MLI is the availability of redundant switching states to balance the capacitor voltages. Also, the switching loss is more evenly distributed in this converter compared to the NPC-MLI [15]. Due to the presence of energy storage capacitors, this converter provides better ride through capability during power interruptions compared to other topologies. However, the flying capacitors need to be pre-charged at the starting for this converter. Also, the switching frequency of the converter has to be high enough to keep the capacitor voltages within the desired limits. With increase in number of levels, the number of flying capacitors also increases and the makes capacitor voltage balancing more complex. In addition, the presence of so many capacitors in the FC-MLI increases the cost of implementation.

Table 1.4. POSSIBLE SWITCHING STATES FOR THE FIVE-LEVEL FC-MLI OF FIG. 1.9

Voltage level	Switch positions							
v_{an}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$+\frac{V_{DC}}{2}$	1	1	1	1	0	0	0	0
$+\frac{V_{DC}}{4}$	1	1	1	0	1	0	0	0
	0	1	1	1	0	0	0	1
	1	0	1	1	0	0	1	0
0	1	1	0	0	1	1	0	0
	0	0	1	1	0	0	1	1
	1	0	1	0	1	0	1	0
	1	0	0	1	0	1	1	0
	0	1	0	1	0	1	0	1
	0	1	1	0	1	0	0	1
$-\frac{V_{DC}}{4}$	1	0	0	0	1	1	1	0
	0	0	0	1	0	1	1	1
	0	0	1	0	1	0	1	1
$-\frac{V_{DC}}{2}$	0	0	0	0	1	1	1	1

1.2.3 Cascaded H-Bridge Multi-Level Inverter (CHB-MLI)

Fig. 1.10 shows the circuit diagram of a cascaded H-bridge MLI, where two single-phase H-bridge inverters are connected in series to synthesize a five-level output voltage. Each H-bridge is supplied from a separate voltage source $+\frac{V_{DC}}{2}$, which can be generated using a transformer and a diode bridge rectifier. The output voltage of each H-bridge can have three values: $+\frac{V_{DC}}{2}$, 0 and $-\frac{V_{DC}}{2}$. Thus, the cascaded connection will result in a five-

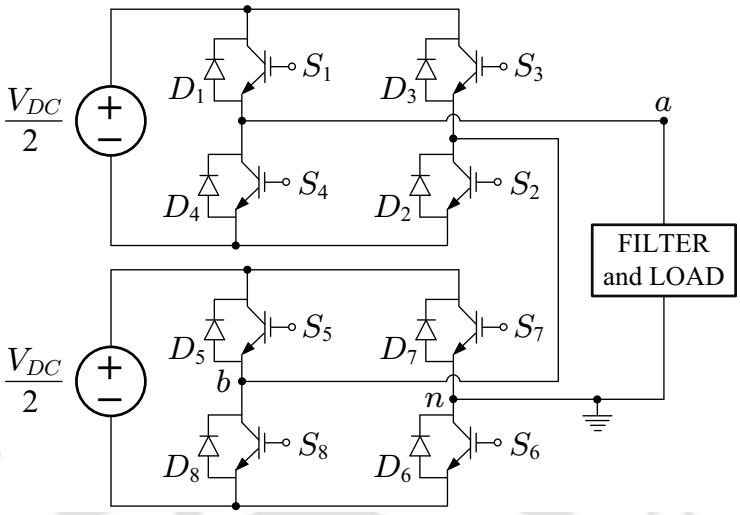


Fig. 1.10. Circuit diagram of single-phase five-level CHB-MLI.

level output voltage waveform. The possible switching combinations of the converter are listed in Table 1.5, from which it can be seen that the CHB-MLI offers higher number of redundant switching combinations compared to the FC-MLI. In addition, since separate DC-sources are used for each H-bridge, there is no need of flying capacitors or clamping diodes in this circuit.

The concept of CHB-MLI can be extended to any number of levels, by connecting more H-bridges in cascade. For an N-level output, $\frac{(N-1)}{2}$ number of H-bridges is required. Hence an N-level CHB-MLI requires $\frac{(N-1)}{2}$ DC sources and $2{\cdot}(N-1)$ switches.

The main advantage of CHB-MLI is its modular structure. There is no requirement of clamping diodes to limit the voltage stress of switches. Also, there is need for capacitor voltage balancing, since each H-bridge is supplied from a DC voltage source. The main drawback of the converter is requirement of isolated DC sources, which are generally realized using phase shifted transformers and rectifiers. These transformers are generally more expensive and increases the size of the converter. Due to the absence of common DC-link, it is difficult to realize the back-to-back configuration using this converter [15, 17].

Table 1.5. POSSIBLE SWITCHING STATES FOR THE FIVE-LEVEL CHB-MLI OF FIG. 1.10

Voltage level	Switch positions							
v_{an}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$+V_{DC}$	1	1	0	0	1	1	0	0
$+\frac{V_{DC}}{2}$	0	1	0	1	1	1	0	0
	1	0	1	0	1	1	0	0
	1	1	0	0	1	0	1	0
	1	1	0	0	0	1	0	1
0	0	1	0	1	0	1	0	1
	0	0	1	1	1	1	0	0
	1	0	1	0	1	0	1	0
	1	1	0	0	0	0	1	1
	0	1	0	1	1	0	1	0
	1	0	1	0	0	1	0	1
$-\frac{V_{DC}}{2}$	0	1	0	1	0	0	1	1
	0	0	1	1	0	1	0	1
	0	0	1	1	1	0	1	0
	1	0	1	0	0	0	1	1
$-V_{DC}$	0	0	1	1	0	0	1	1

1.3 ACTIVE NEUTRAL POINT CLAMPED INVERTER (ANPCI)

The circuit diagram of a three-level inverter topology proposed in [16,18], is shown in Fig. 1.11. Here, two additional active switches, S_{t1} and S_{t2}, are connected in antiparallel to the clamping diodes, D_{t1} and D_{t2}, respectively, of a three-level NPC-MLI as shown in Fig. 1.11. This new topology is named as three-level active neutral point clamped inverter. Table 1.6 lists the possible switching combinations of this converter to generate a three-level

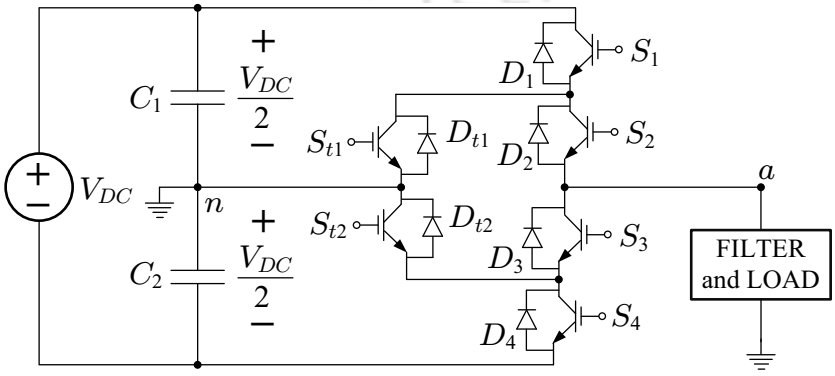


Fig. 1.11. Circuit diagram of single-phase three-level ANPCI.

Table 1.6. POSSIBLE SWITCHING STATES FOR THE THREE-LEVEL ANPCI OF FIG. 1.11

Voltage level	Switch positions					
v_{an}	S_1	S_2	S_3	S_4	S_{t1}	S_{t2}
$+\frac{V_{DC}}{2}$	1	1	0	0	0	1
0	0	1	0	0	1	0
	0	1	0	1	1	0
	1	0	1	0	0	1
	0	0	1	0	0	1
$-\frac{V_{DC}}{2}$	0	0	1	1	1	0

output voltage. Unlike the three-level NPC-MLI, this converter has two switching combinations to generate zero-level output voltage, which can be attributed to the addition of the active switches, S_{t1} and S_{t2}. The increased number of switching states also helps to distribute the power losses more evenly among different semiconductor devices, thereby significantly enhancing the power handling capability when compared to the three-level NPC-MLI.

The concept of three-level ANPCI is extended in [19, 20] to five-level ANPCI by introducing two additional switches (S_7 and S_8) with antiparallel diodes (D_7 and D_8) and then by strategically connecting a flying capacitor FC as shown in Fig. 1.12. The five-level ANPCI has been considered as a hybrid topology that combines the operational features and advantages of both NPC-MLI and FC-MLI topologies [11, 21]. The ANPCI circuit is also modular in nature, i.e., the number of output voltage levels can be easily increased by connecting additional flying capacitors and switches as shown in Fig. 1.13. For an N-level output, the ANPCI requires two DC-link capacitors, $\frac{(N-3)}{2}$ flying capacitors and $(N+3)$ switches with antiparallel diodes. The detailed steady-state operation and control strategies of five-level ANPCI will be discussed in Chapter 2.

Table 1.7 gives the comparison of number of DC-link capacitors, flying capacitors,

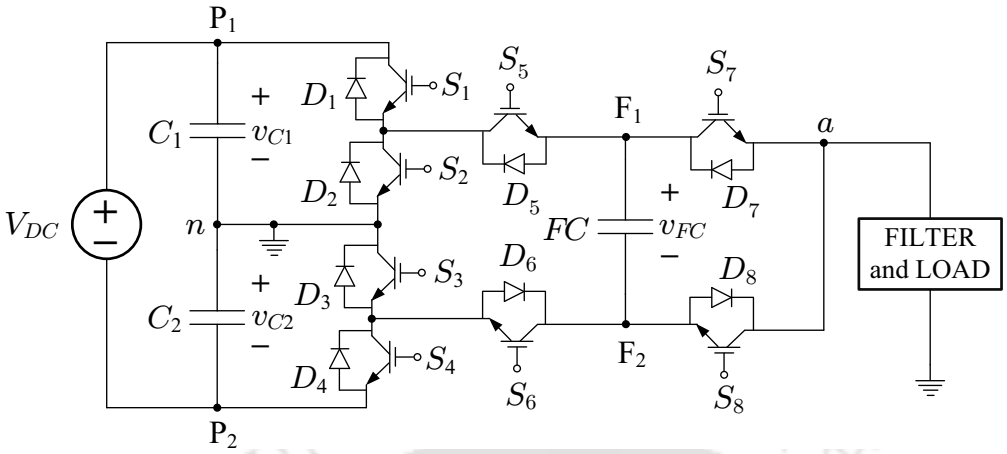


Fig. 1.12. Circuit diagram of single-phase five-level ANPCI.

clamping diodes and active switches with anti-parallel diodes in an ANPCI and in the three classical MLI topologies for an N-level output voltage. Unlike the five-level NPC-MLI and FC-MLI, the ANPCI has only two DC-link capacitors for any number of levels. Also, it does not require any clamping diodes as in NPC-MLI. In addition, it doesn't require separate DC sources as in the case of CHB-MLI. Thus, the ANPCI offers several additional advantages compared to the classical MLIs and several other MLI topologies available in the literature.

Due to the aforementioned features, the three-level and five-level ANPCIs are widely accepted for industrial applications as an alternative to the classical MLI topologies. The five-level ANPCI is proposed for use in low power medium voltage drives by the Allmänna Svenska Elektriska Aktiebolaget Brown Boveri (ABB) Ltd. [20] and now it has become a widely accepted and matured technology [21]. In addition to variable speed drives, the three-level or five-level ANPCI is also proposed for many other industrial applications, such as, grid connected solar PV [22], wind power generation [23], nanogrids [24], aircraft propulsion system [25], etc.

Note that the increase in number of levels of ANPCI is achieved by adding more flying capacitors and active switches as shown in Fig. 1.13. This will help in increasing quality of output voltage waveform. However, as in classical MLIs, the power and voltage rating of ANPCI cannot be increased by increasing the voltage levels. Its power handling capability and voltage rating are always limited by the rating of switches S_1 to S_4, which

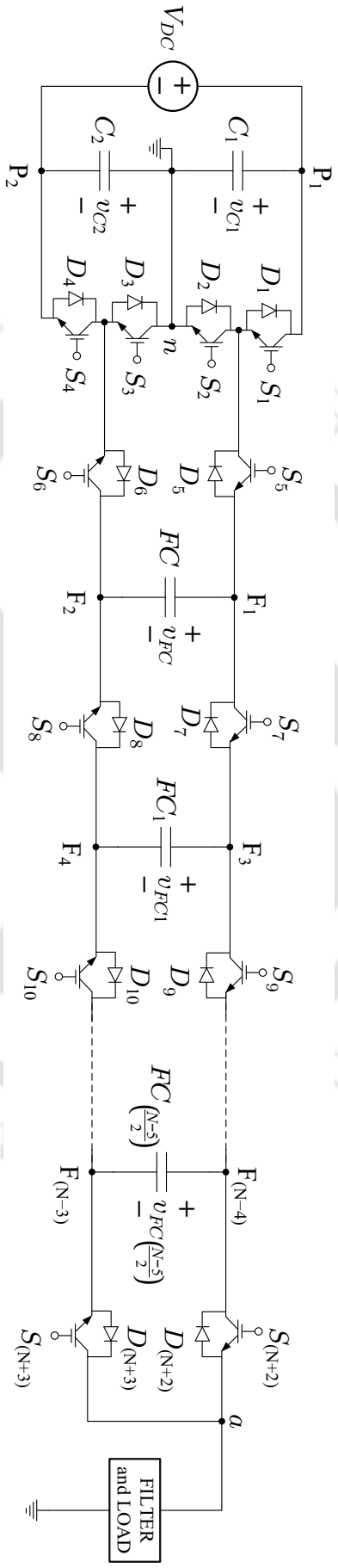


Fig. 1.13. Circuit diagram of single-phase N-level ANPCI.

Table 1.7. COMPARISON OF NUMBER OF COMPONENTS IN THREE CLASSICAL MLIS WITH ANPCI CONSIDERING N-LEVEL OUTPUT VOLTAGE

Parameter	NPC-MLI	FC-MLI	CHB-MLI	ANPCI
Switches with anti parallel diodes	$2\cdot(N-1)$	$2\cdot(N-1)$	$2\cdot(N-1)$	$(N+3)$
Clamping diodes	$(N-1)\cdot(N-2)$	0	0	0
DC-link capacitors	$(N-1)$	$(N-1)$	0	2
Flying capacitors	0	$\frac{(N-1)\cdot(N-2)}{2}$	0	$\frac{(N-3)}{2}$
DC-voltage sources	1	1	$\frac{(N-1)}{2}$	1

need to withstand a half the DC-link voltage, irrespective of number of levels [6]. This is one of the main drawbacks of ANPCI.

1.4 RESEARCH MOTIVATION AND OBJECTIVES OF THE THESIS

A review of classical MLIs along with their advantages and drawbacks has been presented in Section 1.2. Section 1.3 has introduced the basic features and advantages of the three-level and five-level Active Neutral Point Clamped inverters when compared to the NPC-MLI, FC-MLI and CHB-MLI topologies. Due to its advantages, the ANPCI topology can be considered as dc-to-ac converter interface in several industrial applications such as renewable energy systems, variable speed drives, electric vehicle propulsion systems, etc. The three-phase five-level ANPCI in back-to-back configuration has already been commercialized by the ABB Ltd. for its low power medium voltage four-quadrant drive system, ACS2000 [20, 26]. In [23], the performance of a hybrid five-level ANPCI is investigated for a 6 MVA wind power system. Here a three-level ANPCI is also used to interface the wind turbine generator to the DC-link of five-level ANPCI. A single-phase full-bridge five-level ANPCI is proposed as a power conditioning unit for solar PV system in [22]. The converter is also studied for application in aircraft propulsion system [24] and nanogrids [24].

In order to design and analyze the suitability of ANPCI for any of the applications

mentioned above, the researchers need to perform extensive modeling and computer-based simulations of the system under study. For these system-level studies, one can use the switching circuit model of the ANPCI shown in Fig. 1.12, which generally requires more time and extensive computational resources. On the other hand, if an average model of ANPCI is used for these system-level studies, the time and computational resources needed for the modeling and simulation studies can be significantly reduced. Hence this thesis aims to develop an average model of the ANPCI which can accurately predicts the steady-state and dynamic waveforms of the converter in both open-loop and closed-loop operation with significantly less computational time and resources.

Also, when ANPCI is used in single-phase applications, DC-link experiences double line frequency ripple due to pulsating output power, which effects transient operation of the system and deteriorate the output voltage causing lower order harmonics [27, 28]. The voltages of DC-link capacitors and FC of single-phase ANPCI can be balanced using various voltage balancing methods given in [28–32]. Even though voltage balancing is possible, voltage ripple in DC-link capacitors cannot be reduced using any of these methods. This significant voltage ripple present in the DC-link capacitors results in increased voltage stress on the switching devices. Further, lower order harmonics are introduced in the output of the ANPCI. Hence this thesis proposes to reduce the DC-link capacitor voltage ripple of single-phase ANPCI by integrating an external chopper circuit. This also helps in size reduction of DC-link capacitors and FC.

Further this thesis investigates the strength of the averaged model and the operation of chopper integrated ANPCI in single-phase grid-connected solar PV and wind power generation systems.

From the above discussion, the main objectives of this thesis can be listed as below.

1) To perform a detailed study on the circuit diagram and operation of the single-phase five-level ANPCI and to perform a detailed analysis of the converter in all the possible switching states.

2) To implement various multi-carrier pulse width modulated strategies for the ANPCI and compare their performance in terms of harmonic content in the output voltage.

3) To implement various capacitor voltage balancing strategies for the single-phase five-level ANPCI and compare their performance in terms of response time, peak-to-peak ripple in the DC-link capacitor voltages and flying capacitor voltage.

4) To develop a dynamic average circuit model of ANPCI with and without including the non-idealities and to demonstrate its advantages in both open-loop and closed-loop operations of the converter.

5) To reduce the DC-link capacitor voltage ripple in single-phase ANPCI by integrating an external chopper circuit and to develop control methods for the chopper switches.

6) To implement single-phase grid connected solar PV and wind power generation systems using ANPCI as the power conditioning unit and to verify the operation of chopper integrated ANPCI for application in these systems.

1.5 ORGANIZATION OF THE THESIS

The thesis is organized into six chapters. The present chapter, i.e., Chapter 1 has presented the background of the thesis and a brief review of the three classical MLIs. The ANPCI topology has been introduced. This chapter also presents the objectives and organization of the thesis.

In the next chapter, i.e., Chapter 2, the circuit diagram of single-phase five-level ANPCI and its steady-state operate are described. Also, the analysis of the converter in all the possible switching state is given. This chapter also presents the multi-carrier PWM techniques for the converter and their performance comparison. A description of four different capacitor voltage balancing strategies is also given in Chapter 2. Also, a closed-loop controller is also presented for the single-phase ANPCI. The simulation and experimental results to validate the theory are also given in Chapter 2.

In Chapter 3, a dynamic average circuit model for the ANPCI is developed. The chapter also discusses how to include the non-idealities of ANPCI in the average model. The modular nature of the developed average mode is also discussed in this chapter. The chapter also presents the required simulation and experimental results to verify the effectiveness of the averaged model. Further in this chapter, the strength of the model is also demonstrated using a simple standalone PV system with ANPCI as the power conversion stage.

In Chapter 4, it is proposed to integrate an external chopper circuit to the DC-link of single-phase ANPCI, which helps to reduce its DC-link capacitor voltage ripple. The circuit diagram and operation of chopper integrated ANPCI are described. Also, this chapter presents different control techniques to regulate the chopper switches so that the DC-link capacitor voltage ripple of ANPCI is reduced. Finally, this chapter also verifies the operation of ANPCI with and without chopper using simulation and experiment considering various test cases.

Chapter 5 presents implementation of single-phase grid connected solar and wind power generation systems using ANPCI as the main power conditioning unit. This chapter also verifies the operation of chopper integrated ANPCI applied to solar PV and wind power generation systems.

Finally, the concluding remarks of the thesis are presented in Chapter 6. This chapter also presents some issues identified for future research work.

1.6 CONCLUDING REMARKS

This chapter has presented the background of the thesis and a brief review of the three classical MLIs, viz., NPC-MLI, FC-MLI and CHB-MLI. The switching table and main features of these three topologies have been discussed. The ANPCI topology and its advantages have been introduced. This chapter has also presented the objectives and organization of the thesis.

CHAPTER 2

SINGLE-PHASE ANPCI: DETAILED OPERATION AND CONTROL

2.1 INTRODUCTION

In Chapter 1, a brief review of the three classical MLIs, viz., NPC-MLI, FC-MLI, and CHB-MLI, is discussed. The NPC-MLI offers a simple solution to extend the voltage and power level of the inverter with existing semiconductor switches [16]. Also, in a three-phase NPC-MLI, all the phase legs share a common DC-link. Hence, it can be connected in back-to-back configuration to achieve regenerative braking of drives [15]. However, the commercialization of NPC-MLI is generally limited to its three-level version only. To increase the number of levels, one has to use more DC-link capacitors and clamping diodes, which increases the cost of implementation. Also, due to the absence of redundant switching states, the NPC-MLIs with more than three-levels require complicated circuits for balancing the DC-link capacitor voltages. Also, the clamping diodes introduce additional losses and their reverse recovery currents further increase the switching losses in the converter. One more drawback of the NPC-MLI including its three-level version is uneven distribution of losses among its semiconductor devices, which causes unequal junction temperature and limits the switching frequency of the converter.

The second topology introduced is FC-MLI. The main advantage of FC-MLI is the availability of redundant switching states to balance the capacitor voltages. Also, the switching loss is more evenly distributed in this converter compared to the NPC-MLI [15]. Due to the presence of energy storage capacitors, this converter provides better ride through capability during power interruptions compared to other topologies. However, the flying capacitors need to be pre-charged at the starting for this converter. Also, the switching frequency of the

converter has to be high enough to keep the capacitor voltages within the desired limits. With increase in number of levels, the number of flying capacitors also increases and the makes capacitor voltage balancing more complex. In addition, the presence of so many capacitors in the FC-MLI increases the cost of implementation.

The third topology is the CHB-MLI. The main advantage of CHB-MLI is its modular structure. There is no requirement of clamping diodes to limit the voltage stress of switches. Also, there is need for capacitor voltage balancing, since each H-bridge is supplied from a DC voltage source. The main drawback of the converter is requirement of isolated DC sources, which are generally realized using phase shifted transformers and rectifiers. These transformers are generally more expensive and increases the size of the converter. Due to the absence of common DC-link, it is difficult to realize the back-to-back configuration using this converter [15, 17].

Further in previous chapter, ANPCI is also introduced by combining the features of the two classical MLIs, viz., NPC-MLI and FC-MLI. Due to its features, the three-level and five-level ANPCIs are widely accepted for industrial applications as an alternative to the classical MLI topologies. The five-level ANPCI is proposed for use in low power medium voltage drives by ABB [20] and now it has become a widely accepted and matured technology [21]. In addition to variable speed drives, the three-level or five-level ANPCI is also proposed for many other industrial applications, such as, grid connected solar PV [22], wind power generation [23], nanogrids [24], aircraft propulsion system [25], etc.

Due to the advantages and the suitability, this thesis performs a detailed study on the circuit diagram and operation of the single-phase five-level ANPCI. Also, different PWM strategies and capacitor voltage balancing strategies are implemented for single-phase five-level ANPCI and their performance is compared. A dynamic average circuit model of the ANPCI is also presented in this thesis. Also, a chopper integrated ANPCI is proposed to reduce ripple in the DC-link capacitor voltages. This thesis also verifies the operation of chopper integrated ANPCI in solar and wind power generation systems.

In this chapter, the circuit diagram, switching states and steady-state operation of

single-phase five-level ANPCI are explained in detail. In each switching state of the converter, the relation between charging/discharging conditions of the capacitors and the inductor current are determined. The Phase Disposition and Shifting (PDS) PWM technique is applied for gate signal generation of ANPCI, because it generates lower THD compared to conventional PWM techniques of MLIs. Based on the charging/discharging conditions of the capacitors in each switching state of ANPCI, a capacitor voltage balancing algorithm is developed and explained in detail. The algorithm is successful in regulating the capacitor voltages of ANPCI to their respective reference values. The performance of proposed capacitor voltage balancing strategy is compared with the Capacitor Voltage Balancing Strategies (CVBS) given in the literature for the five-level ANPCI. A closed-loop Synchronous Reference Frame (SRF)-dq controller is developed and implemented for the single-phase ANPCI to regulate its load voltage. Experimental results are presented to validate the operation, PDS-PWM technique, proposed capacitor voltage balancing strategy and closed-loop SRF-dq controller.

This chapter is organized as follows. In Section 2.2, circuit diagram and steady-state operation are given. Comparison of Phase Disposition (PD), Phase Opposition Disposition (POD), Alternative Phase Opposition Disposition (APOD) and PDS-PWM techniques is given in Section 2.3. Various CVBS are described and their performance comparison is given in Section 2.4. The operation of ANPCI with closed-loop SRF-dq controller is given in Section 2.5. The experimental results of the ANPCI for open-loop and closed-loop operations are presented in Section 2.6. Finally, summary of this chapter is given in Section 2.7.

2.2 CIRCUIT DIAGRAM AND STEADY-STATE OPERATION

Fig. 2.1 shows the circuit diagram of single-phase five-level active neutral point clamped inverter (ANPCI) consisting of two DC-link capacitors C_1 and C_2, one flying capacitor FC and eight switches S_1 to S_8, each with an antiparallel diode. The average voltage across each of the capacitors C_1 and C_2 is maintained at 50% of the input voltage, V_{DC},

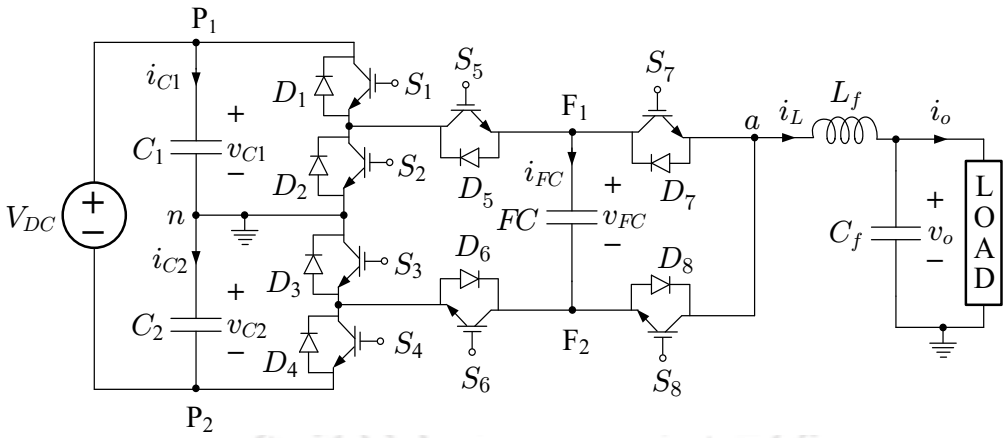


Fig. 2.1. Circuit diagram of single-phase five-level ANPCI.

while the average voltage across FC is maintained at 25% of V_{DC}. At any instant of time, the PWM output voltage v_{an} can be equal to any one of the five-voltage levels: $+\frac{V_{DC}}{2}$, $+\frac{V_{DC}}{4}$, 0, $-\frac{V_{DC}}{4}$, $-\frac{V_{DC}}{2}$. The LC filter, consisting of L_f and C_f, filters out the switching frequency components in five-level PWM voltage v_{an} so that the load voltage v_o is pure sinusoidal waveform.

Table 2.1 lists eight possible switching states of ANPCI and the corresponding voltage level, v_{an}. Fig. 2.2 shows the equivalent circuits of the ANPCI for each of the switching state given in Table 2.1. Although ANPCI has eight switches, there are only three independent switching signals: S_1, S_5 and S_7. Other five switching signals can be obtained as: $S_2 = S_4 = S_1'$, $S_3 = S_1$, $S_6 = S_5'$ and $S_8 = S_7'$; where S_1', S_5' and S_7' are the logical complements of S_1, S_5 and S_7, respectively. In Table 2.1, redundant switching states are available for voltage levels, $+\frac{V_{DC}}{4}$, 0 and $-\frac{V_{DC}}{4}$.

Fig. 2.2(a) shows the equivalent circuit of ANPCI in State I, in which the switches S_1, S_3, S_5, S_7 are ON and S_2, S_4, S_6, S_8 are OFF. The PWM voltage v_{an} is equal to v_{C1} as capacitor C_1 is directly connected between nodes 'a' and 'n'. To determine the effect of i_L on capacitor voltages v_{C1} and v_{C2}, one can write from Fig. 2.2(a),

$$i_L = -i_{C1} + i_{C2} \tag{2.1}$$

$$V_{DC} = v_{C1} + v_{C2} \tag{2.2}$$

Table 2.1. POSSIBLE SWITCHING STATES FOR THE ANPCI OF FIG. 2.1

State	Voltage level	Switch positions								$i_L > 0$			$i_L < 0$		
	v_{an}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	v_{C1}	v_{C2}	v_{FC}	v_{C1}	v_{C2}	v_{FC}
I	$+\frac{V_{DC}}{2}$	1	0	1	0	1	0	1	0	↓	↑	N.E.	↑	↓	N.E.
II	$+\frac{V_{DC}}{4}$	1	0	1	0	1	0	0	1	↓	↑	↑	↑	↓	↓
III	$+\frac{V_{DC}}{4}$	1	0	1	0	0	1	1	0	N.E.	N.E.	↓	N.E.	N.E.	↑
IV	0	1	0	1	0	0	1	0	1	N.E.	N.E.	N.E.	N.E.	N.E.	N.E.
V	0	0	1	0	1	1	0	1	0	N.E.	N.E.	N.E.	N.E.	N.E.	N.E.
VI	$-\frac{V_{DC}}{4}$	0	1	0	1	1	0	0	1	N.E.	N.E.	↑	N.E.	N.E.	↓
VII	$-\frac{V_{DC}}{4}$	0	1	0	1	0	1	1	0	↓	↑	↓	↑	↓	↑
VIII	$-\frac{V_{DC}}{2}$	0	1	0	1	0	1	0	1	↓	↑	N.E.	↑	↓	N.E.

Note: Upward arrow (↑), Downward arrow (↓), and N.E. indicate increase, decrease, and no effect in capacitor voltages, respectively.

Differentiating (2.2) on both sides and noting that V_{DC} is constant, we get

$$\frac{\mathrm{d}v_{C1}}{\mathrm{d}t} = -\frac{\mathrm{d}v_{C2}}{\mathrm{d}t} \tag{2.3}$$

Also, the capacitor currents, i_{C1} and i_{C2} can be expressed as

$$i_{C1} = C_1\frac{\mathrm{d}v_{C1}}{\mathrm{d}t} \quad \text{and} \quad i_{C2} = C_2\frac{\mathrm{d}v_{C2}}{\mathrm{d}t} \tag{2.4}$$

Assuming $C_1 = C_2$; using (2.1), (2.3) and (2.4), it can be shown that

$$i_{C1} = -i_{C2} = -\frac{i_L}{2} \tag{2.5}$$

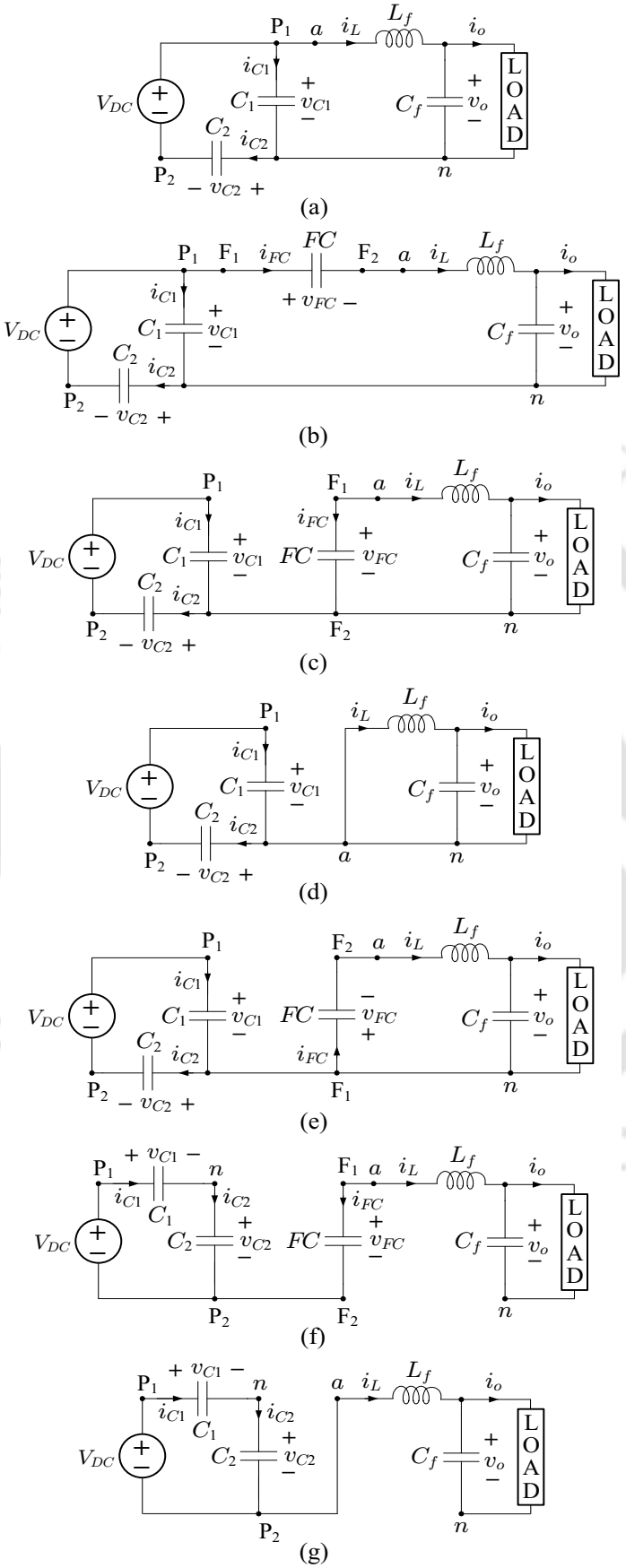


Fig. 2.2. Equivalent circuit of ANPCI in (a) State-I, (b) State-II, (c) State-III, (d) States-IV and V, (e) State-VI, (f) State-VII, and (g) State-VIII.

From (2.4) and (2.5), it can be concluded that if i_L is positive, v_{C1} decreases and v_{C2} increases as mentioned in Table 2.1. Similarly if i_L is negative, v_{C1} increases and v_{C2} decreases. Note that in State I, FC is not connected in the circuit and hence v_{FC} is unaffected in this state.

Fig. 2.2(b) shows the equivalent circuit of ANPCI in State II, in which the switches S_1, S_3, S_5, S_8 are ON and S_2, S_4, S_6, S_7 are OFF. The PWM voltage v_{an} is equal to $(v_{C1} - v_{FC})$ in this state. Here FC is connected in series with L_f and hence,

$$i_{FC} = (FC)\frac{\mathrm{d}v_{FC}}{\mathrm{d}t} = i_L \tag{2.6}$$

Therefore, if i_L is positive, v_{FC} increases and if i_L is negative, v_{FC} decreases. Note that (2.1)−(2.5) are valid in this state also, because $i_{FC} = i_L$. Thus, the effect of i_L on v_{C1} and v_{C2} is same as that determined in State I.

Using similar analysis, the effect of i_L on v_{C1}, v_{C2} and v_{FC} is determined in other switching states and listed in Table 2.1.

2.3 PWM TECHNIQUES AND THEIR PERFORMANCE COMPARISON

To operate a power electronic inverter, a suitable PWM technique is required. To operate the MLIs various PWM techniques are implemented in the literature of which some are shown in Fig. 2.3. The PWM techniques are mainly classified as carrier based PWM and carrier-less PWM techniques. The carrier based strategies require a modulation signal and a single/multiple carrier signals. The modulation signals are classified as continuous modulation and discontinuous modulation [30, 33–79]. An MLI in general requires multiple carrier signals based on its number of levels.

Among the various carrier based techniques, PD, POD and APOD techniques are widely known PWM techniques for generating switching signals for NPC-MLI [48, 51, 80–84]. A detailed analysis of these three PWM techniques is carried out in [49] for NPC-MLI. THD comparison for output PWM voltage of three-phase NPC-MLI using PD and APOD-PWM techniques is given in [80]. In [51], an apparent switching frequency doubling based

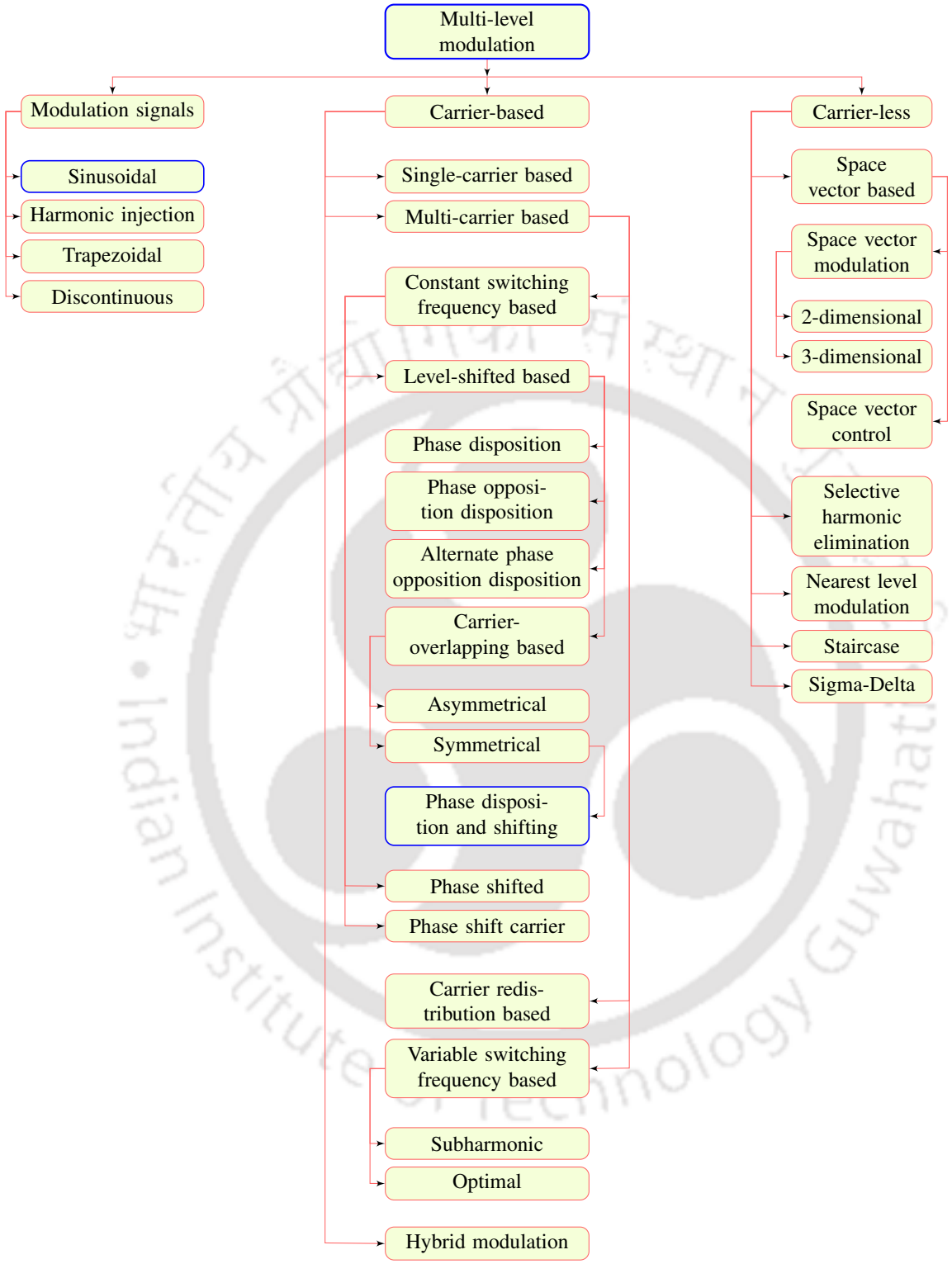


Fig. 2.3. Classification of the modulation strategies for the MLIs.

Phase Disposition and Shifting (PDS) PWM technique is proposed. In [83], the PDS-PWM technique is compared with APOD-PWM technique for ANPCI. The PD, POD, APOD and

PDS-PWM techniques can be easily extended for generating switching signals of ANPCI. Hence, these four PWM techniques are implemented and compared for five-level ANPCI in below subsections.

2.3.1 PD-PWM Technique

Fig. 2.4 shows the modulation and triangular carrier signals and the PWM voltage for PD-PWM technique [82]. In PD-PWM technique, none of the four carrier signals: v_{t1}, v_{t2}, v_{t3} and v_{t4}, overlap and each carrier has a magnitude of 0.5. This technique involves comparison of a sinusoidal modulation signal, $m_a = M \cdot \sin(\omega_o t)$, with all the carrier signals. The carrier signals v_{t1} to v_{t4} varies as: v_{t1} from 0.5 to 1, v_{t2} from 0 to 0.5, v_{t3} from -0.5 to 0 and v_{t4} from -1 to -0.5. The signals v_{t1}, v_{t2}, v_{t3} and v_{t4} are all in-phase. The peak of m_a is called the modulation index, M. Based on the instantaneous value of m_a, four different regions are defined in Fig. 2.4. In each of these four regions, the PWM voltage level (v_{an}) shown in Fig. 2.4 is determined depending on the relative values of modulation and carrier signals, as given below in (2.7a)$-$(2.7d).

Region 1: $0.5 < m_a < 1$**:**

$$v_{an} = +\frac{V_{DC}}{2} \quad \text{if} \quad m_a > v_{t1} \ \text{and} \ m_a < 1.0$$

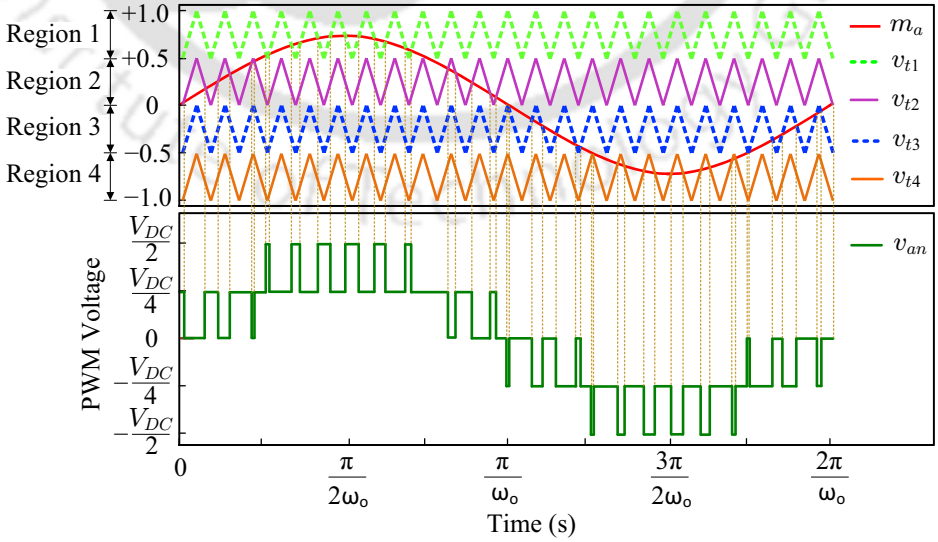


Fig. 2.4. Generation of PWM voltage (v_{an}) using PD-PWM technique by comparison of the modulation signal (m_a) with the carrier signals (v_{t1}, v_{t2}, v_{t3}, and v_{t4}).

$$v_{an} = +\frac{V_{DC}}{4} \quad \text{if} \quad m_a < v_{t1} \ \text{and} \ m_a > 0.5 \tag{2.7a}$$

Region 2: $0 < m_a < 0.5$**:**

$$\begin{aligned} v_{an} &= +\frac{V_{DC}}{4} \quad \text{if} \quad m_a > v_{t2} \ \text{and} \ m_a < 0.5 \\ v_{an} &= \quad 0 \quad\ \ \text{if} \quad m_a < v_{t2} \ \text{and} \ m_a > 0 \end{aligned} \tag{2.7b}$$

Region 3: $-0.5 < m_a < 0$**:**

$$\begin{aligned} v_{an} &= \quad 0 \quad\ \ \text{if} \quad m_a > v_{t3} \ \text{and} \ m_a < 0 \\ v_{an} &= -\frac{V_{DC}}{4} \quad \text{if} \quad m_a < v_{t3} \ \text{and} \ m_a > -0.5 \end{aligned} \tag{2.7c}$$

Region 4: $-1 < m_a < -0.5$**:**

$$\begin{aligned} v_{an} &= -\frac{V_{DC}}{4} \quad \text{if} \quad m_a > v_{t4} \ \text{and} \ m_a < -0.5 \\ v_{an} &= -\frac{V_{DC}}{2} \quad \text{if} \quad m_a < v_{t4} \ \text{and} \ m_a > -1.0 \end{aligned} \tag{2.7d}$$

Once the desired value of v_{an} is determined using (2.7), the switching state to be applied can be found from Table 2.1. Note that if $v_{an} = +\frac{V_{DC}}{2}$ or $-\frac{V_{DC}}{2}$, there is only one possible switching state that can be applied. However, if $v_{an} = \pm\frac{V_{DC}}{4}$ or 0, redundant switching combinations are available in Table 2.1.

Fig. 2.5 shows the PSCAD/EMTDC simulation waveforms of DC input voltage (V_{DC}), DC-link capacitor voltages (v_{C1} and v_{C2}), flying capacitor voltage (v_{FC}), PWM voltage (v_{an}) and load voltage (v_o) for 5L-ANPCI with PD-PWM technique. The DC input voltage is 1 kV. The DC sources of voltages 500 V, 500 V and 250 V are considered in place of C_1, C_2 and FC capacitors, hence their corresponding voltages measured are pure DC. The filter values L_f and C_f are 2 mH and 40 μF, respectively. The load considered is 16 Ω. It can be observed that the PWM voltage obtained is of three-level when $0 < M < 0.5$, i.e.,

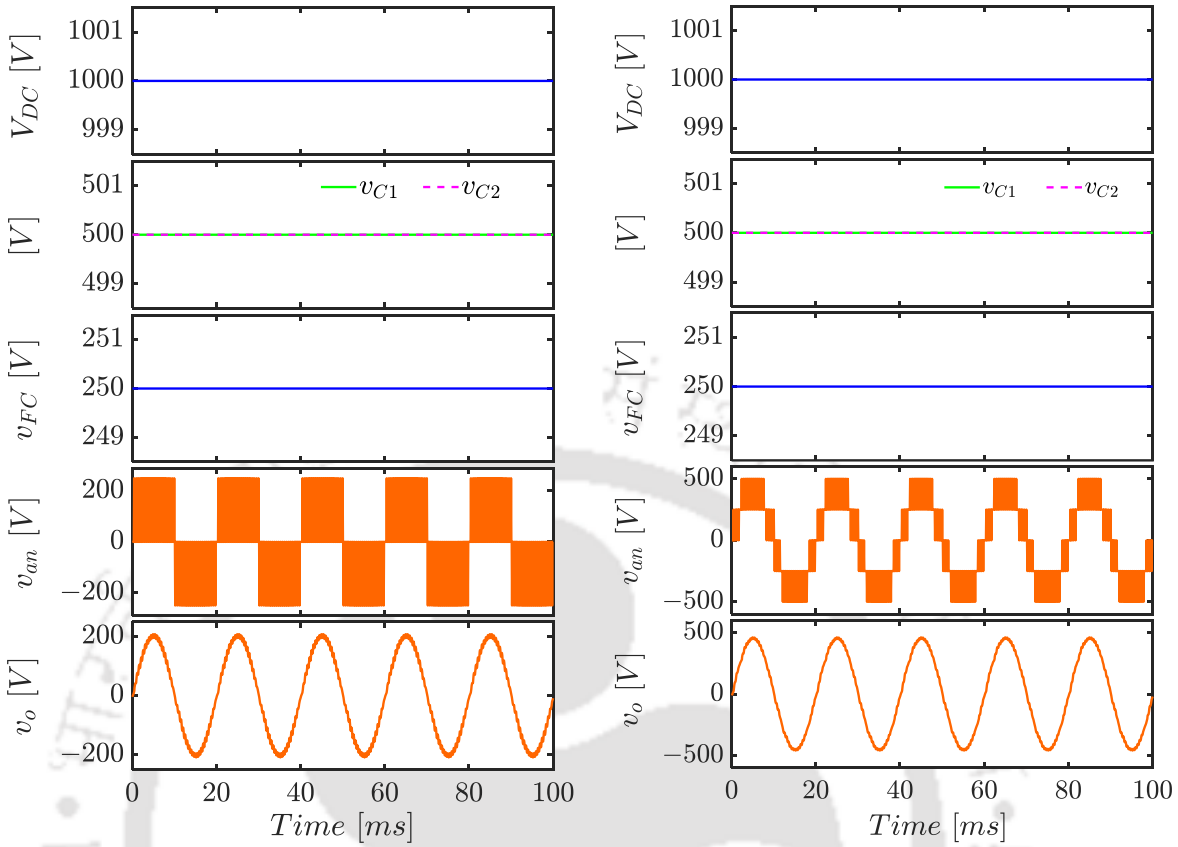


Fig. 2.5. Simulation results obtained for 5L-ANPCI using PD-PWM technique considering fundamental frequency (f_o) as 50 Hz, switching frequency (f_{s1}) as 2.1 kHz with M as (a) 0.4, and (b) 0.9.

in Fig. 2.5(a), whereas it is of five-level when $0.5 < M < 1.0$, i.e., in Fig. 2.5(b).

2.3.2 POD-PWM Technique

Fig. 2.6 shows the modulation and triangular carrier signals and the PWM voltage for POD-PWM technique [82]. In POD-PWM technique, none of the four carrier signals: v_{t1}, v_{t2}, v_{t3} and v_{t4}, overlap and each carrier has a magnitude of 0.5. This technique involves comparison of a sinusoidal modulation signal, $m_a = M \cdot \sin(\omega_o t)$, with all the carrier signals. The carrier signals v_{t1} to v_{t4} varies as: v_{t1} from 0.5 to 1, v_{t2} from 0 to 0.5, v_{t3} from -0.5 to 0 and v_{t4} from -1 to -0.5. The signals v_{t1} and v_{t2} are in-phase as well as v_{t3} and v_{t4} are in-phase, where as v_{t1} and v_{t2} are 180° phase shifted from v_{t3} and v_{t4}. Based on the instantaneous value of m_a, four different regions are defined in Fig. 2.6. In each of these four regions, the PWM voltage level (v_{an}) shown in Fig. 2.6 is determined depending on the relative values of modulation and carrier signals, as given in (2.7a)−(2.7d).

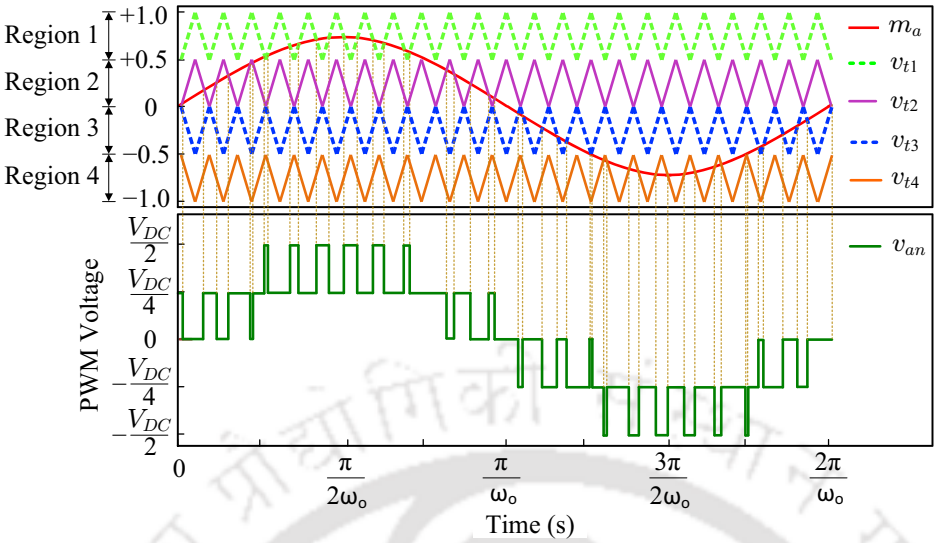


Fig. 2.6. Generation of PWM voltage (v_{an}) using POD-PWM technique by comparison of the modulation signal (m_a) with the carrier signals (v_{t1}, v_{t2}, v_{t3}, and v_{t4}).

Once the desired value of v_{an} is determined using (2.7), the switching state to be applied can be found from Table 2.1. Note that if $v_{an} = +\frac{V_{DC}}{2}$ or $-\frac{V_{DC}}{2}$, there is only one possible switching state that can be applied. However, if $v_{an} = \pm\frac{V_{DC}}{4}$ or 0, redundant switching combinations are available in Table 2.1.

Fig. 2.7 shows the PSCAD/EMTDC simulation waveforms of V_{DC}, v_{C1}, v_{C2}, v_{FC}), v_{an} and v_o for 5L-ANPCI with POD-PWM technique. Here also, the DC sources of voltages 500 V, 500 V and 250 V are considered in place of C_1, C_2 and FC capacitors, hence their corresponding voltages measured are pure DC. The filter values L_f and C_f are 2 mH and 40 μF, respectively. The load considered is 16 Ω. It can be observed that the PWM voltage obtained is of three-level when $0 < M < 0.5$, i.e., in Fig. 2.7(a), whereas it is of five-level when $0.5 < M < 1.0$, i.e., in Fig. 2.7(b).

2.3.3 APOD-PWM Technique

Fig. 2.8 shows the modulation and triangular carrier signals and the PWM voltage for APOD-PWM technique [82]. In APOD-PWM technique, none of the four carrier signals: v_{t1}, v_{t2}, v_{t3} and v_{t4}, overlap and each carrier has a magnitude of 0.5. This technique involves comparison of a sinusoidal modulation signal, $m_a = M \cdot \sin(\omega_o t)$, with all the carrier signals. The carrier signals v_{t1} to v_{t4} varies as: v_{t1} from 0.5 to 1, v_{t2} from 0 to 0.5, v_{t3} from -0.5 to

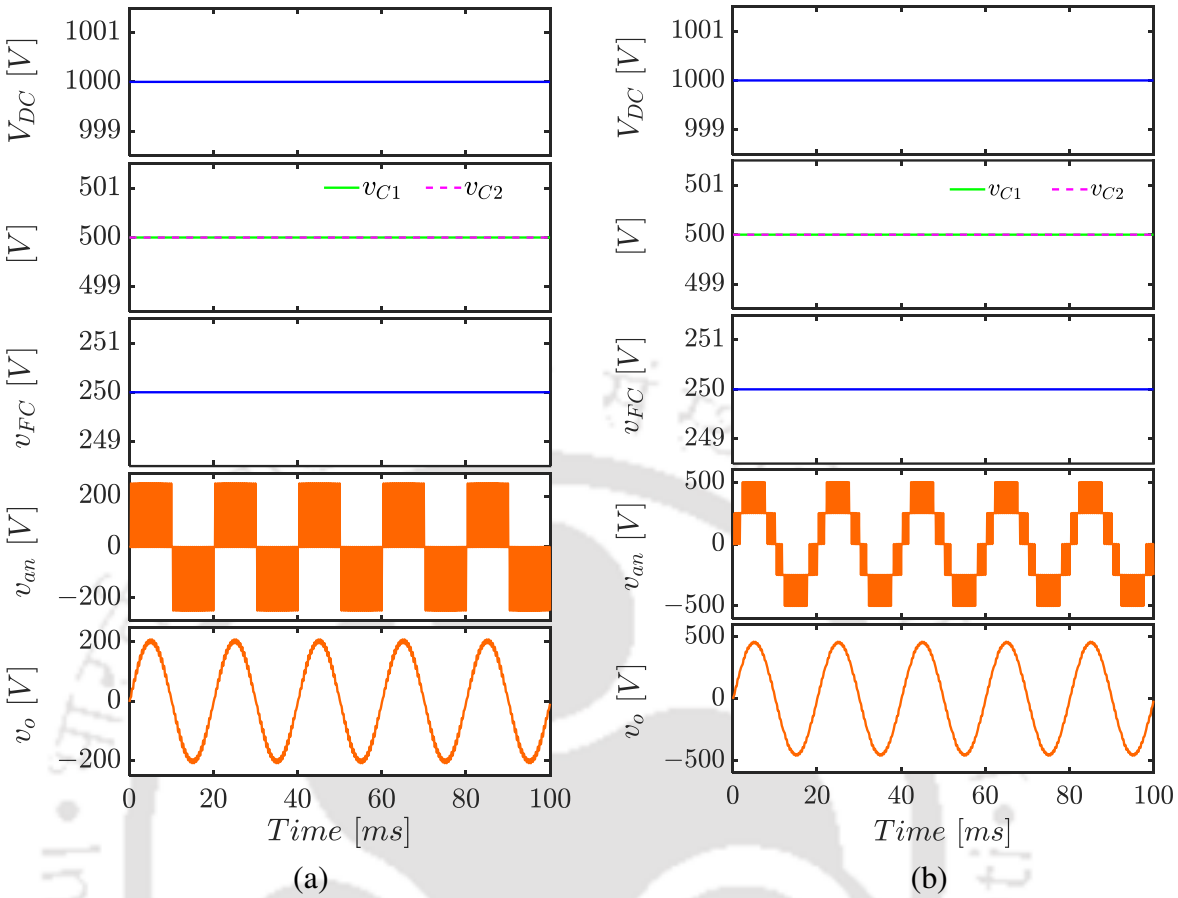


Fig. 2.7. Simulation results obtained for 5L-ANPCI using POD-PWM technique considering fundamental frequency (f_o) as 50 Hz, switching frequency (f_{s1}) as 2.1 kHz with M as (a) 0.4, and (b) 0.9.

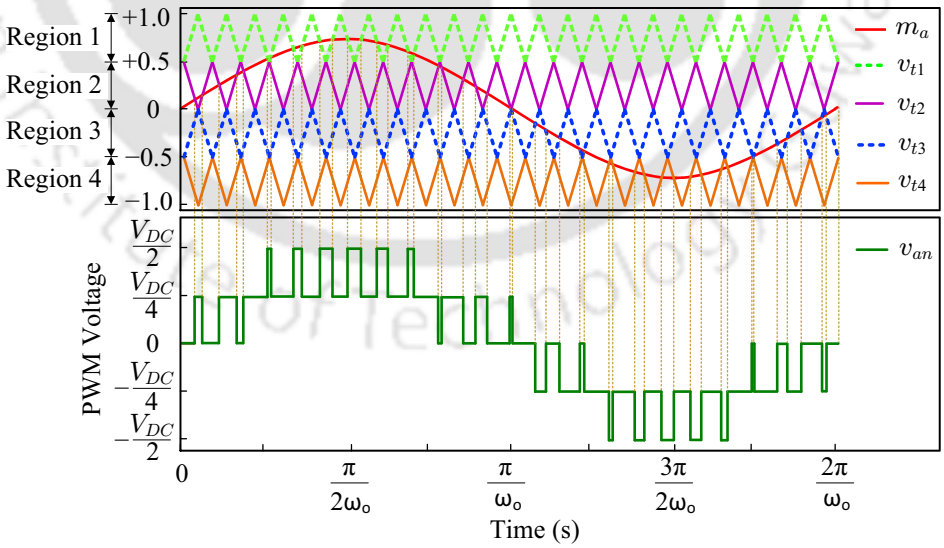


Fig. 2.8. Generation of PWM voltage (v_{an}) using APOD-PWM technique by comparison of the modulation signal (m_a) with the carrier signals (v_{t1}, v_{t2}, v_{t3}, and v_{t4}).

0 and v_{t4} from -1 to -0.5. Also, the signals v_{t1} and v_{t3} are 180° phase shifted from v_{t2} and v_{t4}, respectively. Based on the instantaneous value of m_a, four different regions are defined

in Fig. 2.8. In each of these four regions, the PWM voltage level (v_{an}) shown in Fig. 2.8 is determined depending on the relative values of modulation and carrier signals, as given in (2.7a)−(2.7d).

Once the desired value of v_{an} is determined using (2.7), the switching state to be applied can be found from Table 2.1. Note that if $v_{an} = +\frac{V_{DC}}{2}$ or $-\frac{V_{DC}}{2}$, there is only one possible switching state that can be applied. However, if $v_{an} = \pm\frac{V_{DC}}{4}$ or 0, redundant switching combinations are available in Table 2.1.

Fig. 2.9 shows the PSCAD/EMTDC simulation waveforms of V_{DC}, v_{C1}, v_{C2}, v_{FC}), v_{an} and v_o for 5L-ANPCI with APOD-PWM technique. The DC sources of voltages 500 V, 500 V and 250 V are considered in place of C_1, C_2 and FC capacitors, hence the voltages V_{DC}, v_{C1}, v_{C2} and v_{FC} measured are pure DC. The filter values L_f and C_f are 2 mH and 40 μF, respectively. The load considered is 16 Ω. It can be observed that the

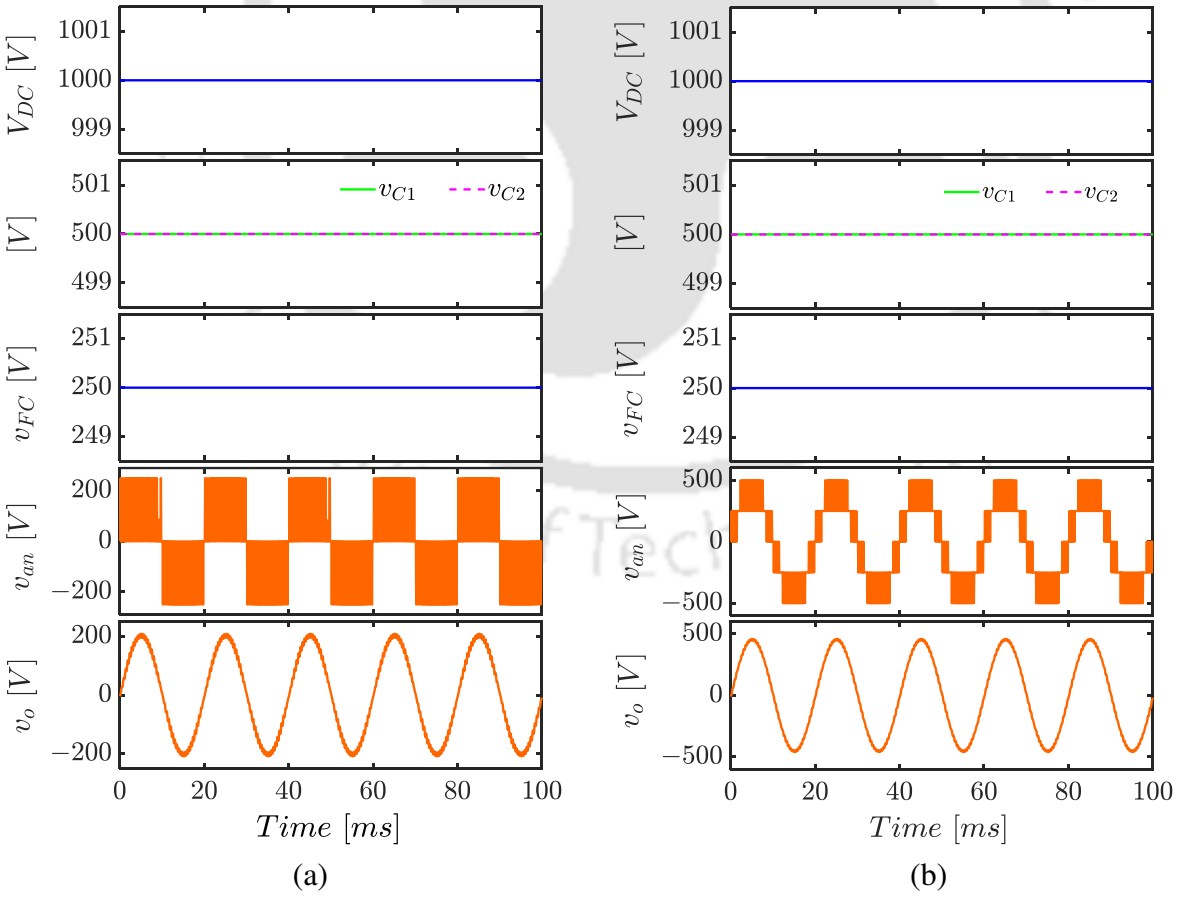


Fig. 2.9. Simulation results obtained for 5L-ANPCI using APOD-PWM technique considering fundamental frequency (f_o) as 50 Hz, switching frequency (f_{s1}) as 2.1 kHz with M as (a) 0.4, and (b) 0.9.

PWM voltage obtained is of three-level when $0 < M < 0.5$, i.e., in Fig. 2.9(a), whereas it is of five-level when $0.5 < M < 1.0$, i.e., in Fig. 2.9(b).

2.3.4 PDS-PWM Technique

Fig. 2.10 shows the modulation and triangular carrier signals and the PWM voltage for PDS-PWM technique [51]. In PDS-PWM technique, carriers v_{t1} and v_{t2} overlap with each other; similarly, carriers v_{t3} and v_{t4} also overlap with each other and the magnitude of each carrier is 1.0. This technique involves comparison of a sinusoidal modulation signal, $m_a = M \cdot \sin(\omega_o t)$, with all the carrier signals. The carrier signals, v_{t1} and v_{t2} vary from 0 to 1, while v_{t3} and v_{t4} vary from 0 to -1. Also, the signals v_{t2} and v_{t4} are 180° phase shifted from v_{t1} and v_{t3}, respectively. Based on the instantaneous value of m_a, four different regions are defined in Fig. 2.10. The PWM voltage level, v_{an} in each of these four regions is determined depending on the relative values of modulation and carrier signals, as given below in (2.8a)−(2.8d).

Region 1: $0.5 < m_a < 1$**:**

$$\begin{aligned} v_{an} &= +\frac{V_{DC}}{2} \quad \text{if} \quad m_a > v_{t1} \ \text{and} \ m_a > v_{t2} \\ v_{an} &= +\frac{V_{DC}}{4} \quad \text{if} \quad m_a < v_{t1} \ \text{or} \ m_a < v_{t2} \end{aligned} \tag{2.8a}$$

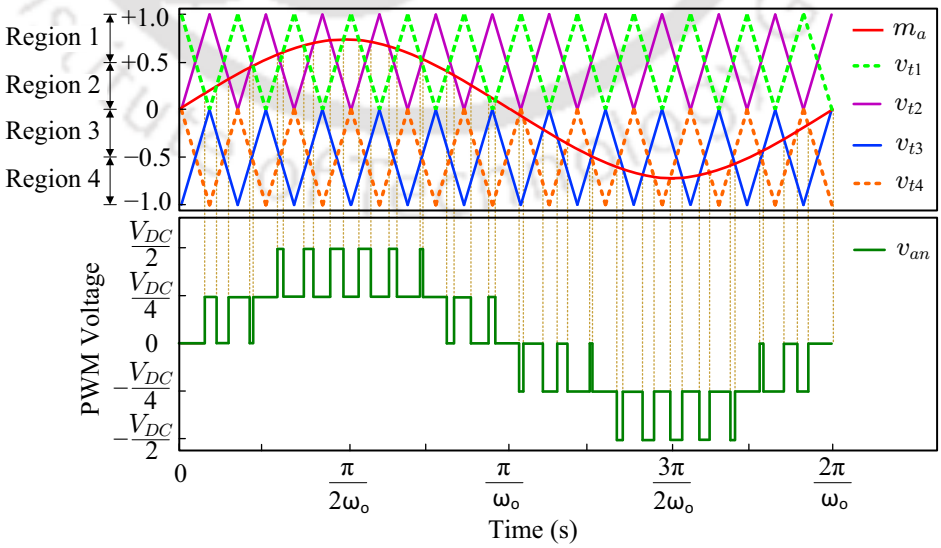


Fig. 2.10. Generation of PWM voltage (v_{an}) using PDS-PWM technique by comparison of the modulation signal (m_a) with the carrier signals (v_{t1}, v_{t2}, v_{t3}, and v_{t4}).

Region 2: $0 < m_a < 0.5$**:**

$$v_{an} = +\frac{V_{DC}}{4} \quad \text{if} \quad m_a > v_{t1} \ \text{ or } \ m_a > v_{t2}$$
$$v_{an} = 0 \quad \text{if} \quad m_a < v_{t1} \ \text{ and } \ m_a < v_{t2} \tag{2.8b}$$

Region 3: $-0.5 < m_a < 0$**:**

$$v_{an} = 0 \quad \text{if} \quad m_a > v_{t3} \ \text{ and } \ m_a > v_{t4}$$
$$v_{an} = -\frac{V_{DC}}{4} \quad \text{if} \quad m_a < v_{t3} \ \text{ or } \ m_a < v_{t4} \tag{2.8c}$$

Region 4: $-1 < m_a < -0.5$**:**

$$v_{an} = -\frac{V_{DC}}{4} \quad \text{if} \quad m_a > v_{t3} \ \text{ or } \ m_a > v_{t4}$$
$$v_{an} = -\frac{V_{DC}}{2} \quad \text{if} \quad m_a < v_{t3} \ \text{ and } \ m_a < v_{t4} \tag{2.8d}$$

Once the desired value of v_{an} is determined using (2.8), the switching state to be applied can be found from Table 2.1. Note that if $v_{an} = +\frac{V_{DC}}{2}$ or $-\frac{V_{DC}}{2}$, there is only one possible switching state that can be applied. However, if $v_{an} = \pm\frac{V_{DC}}{4}$ or 0, redundant switching combinations are available in Table 2.1. The choice between these redundant switching states is made by the capacitor voltage balancing strategy, which is incorporated in the PDS-PWM technique. The capacitor voltage balancing strategy will be explained in the next section. The objective of capacitor voltage balancing strategy is to maintain the FC voltage to be within the range $\frac{V_{DC}}{4} \pm \epsilon$ and DC-link capacitor voltages to be within the range $\frac{V_{DC}}{2} \pm \epsilon$. Here ϵ is a predefined tolerance for the capacitor voltages based on their allowable deviations from the respective nominal values.

Fig. 2.11 shows the PSCAD/EMTDC simulation waveforms of V_{DC}, v_{C1}, v_{C2}, v_{FC}), v_{an} and v_o for 5L-ANPCI with PDS-PWM technique. The DC sources of voltages 500 V, 500 V and 250 V are considered in place of C_1, C_2 and FC capacitors, hence the

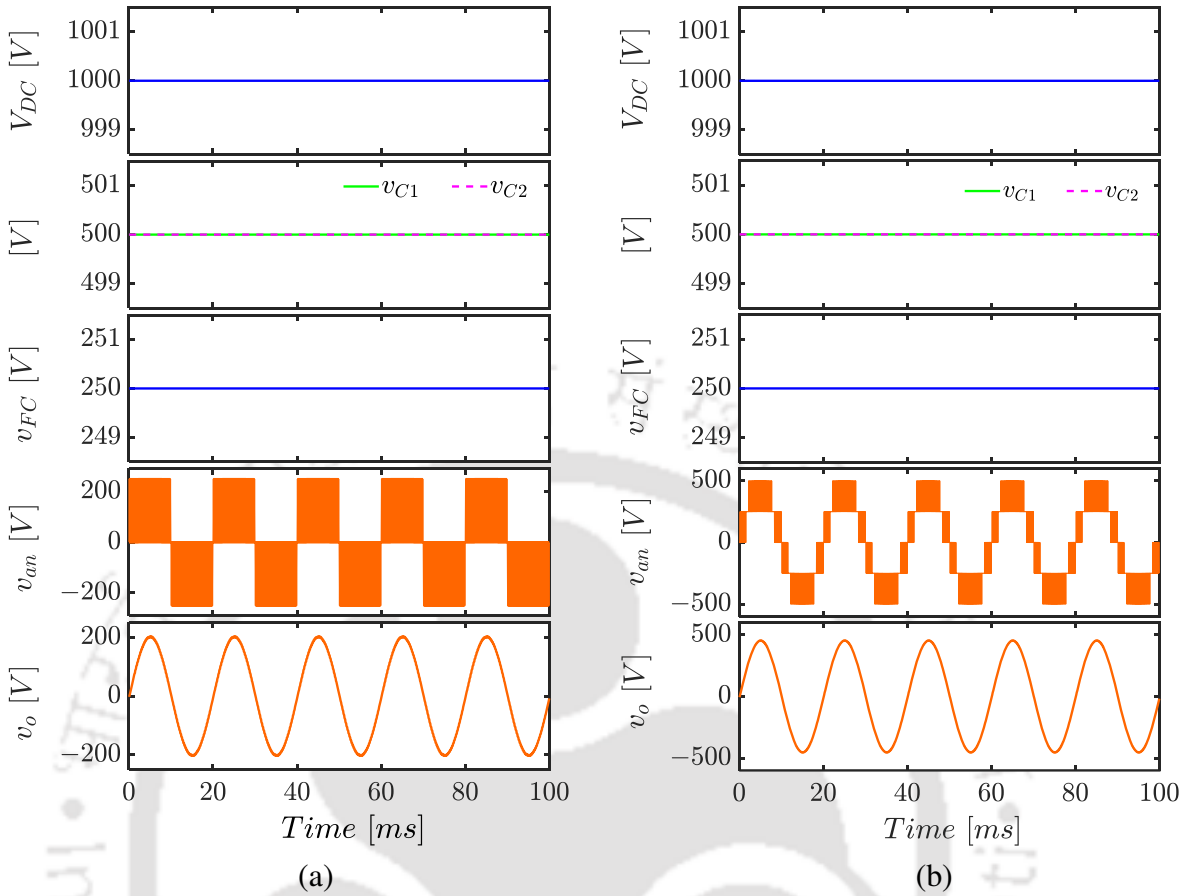


Fig. 2.11. Simulation results obtained for 5L-ANPCI using PDS-PWM technique considering fundamental frequency (f_o) as 50 Hz, switching frequency (f_{s1}) as 2.1 kHz with M as (a) 0.4, and (b) 0.9.

voltages V_{DC}, v_{C1}, v_{C2} and v_{FC} measured are pure DC. The filter values L_f and C_f are 2 mH and 40 μF, respectively. The load considered is 16 Ω. It can be observed that the PWM voltage obtained is of three-level when $0 < M < 0.5$, i.e., in Fig. 2.11(a), whereas it is of five-level when $0.5 < M < 1.0$, i.e., in Fig. 2.11(b).

2.3.5 Performance Comparison of the PWM Techniques

Figs. 2.12−2.15 show the normalized harmonic spectrum of v_{an} for 5L-ANPCI using PD, POD, APOD and PDS-PWM techniques considering M as 0.4 and the capacitors in Fig. 2.1 are replaced by DC-voltage sources. Similarly Figs. 2.16−2.19 show the normalized harmonic spectrum of v_{an} considering M as 0.9. In Figs. 2.12−2.19, the maximum harmonic order considered is 255. The harmonics in v_{an} waveform of 5L-ANPCI using PD-PWM technique appear at $jm_f \pm k$. Here, j and k are positive integers; if j is an even number, then k is an odd number and vice versa. The harmonics in v_{an} waveform of 5L-ANPCI using POD-

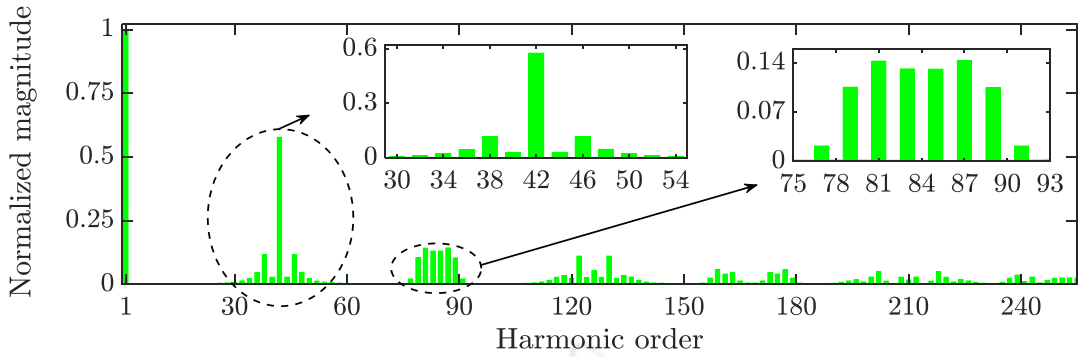


Fig. 2.12. Normalized harmonic spectrum of v_{an} for 5L-ANPCI using PD-PWM technique with $M = 0.4$, frequency modulation ratio $(m_f) = 42$, switching frequency $(f_{s1}) = 2.1$ kHz, and base voltage of 200 V.

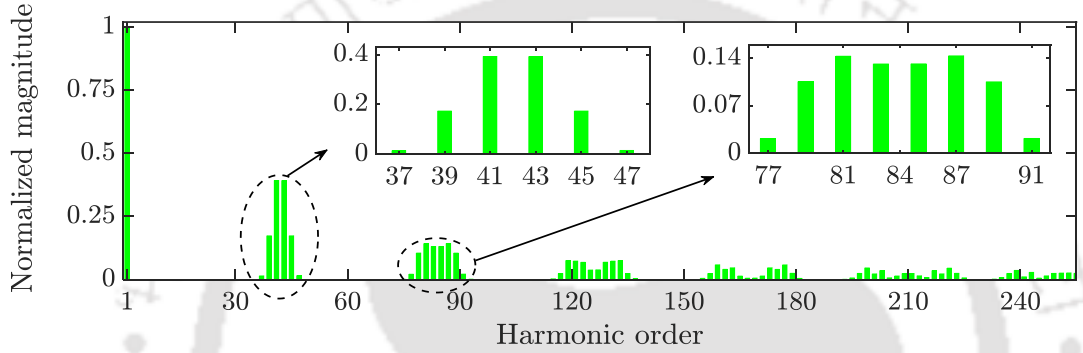


Fig. 2.13. Normalized harmonic spectrum of v_{an} for 5L-ANPCI using POD-PWM technique with $M = 0.4$, frequency modulation ratio $(m_f) = 42$, switching frequency $(f_{s1}) = 2.1$ kHz, and base voltage of 200 V.

PWM and APOD-PWM techniques appear at $jm_f \pm k$. Here, j is a positive integer and k is a positive odd integer [80]. The harmonics in v_{an} waveform of 5L-ANPCI using PDS-PWM technique appear at $j(2m_f) \pm k$. Here, j is a positive integer and k is a positive odd integer. The harmonics spread with PD, POD and APOD-PWM techniques are around the integral multiples of switching frequency, whereas the harmonics spread with PDS-PWM technique are around twice the integral multiples of switching frequency. From Figs. 2.12– 2.15, it is observed that the maximum amplitude of dominant harmonics is more with PD-PWM technique compared to remaining three PWM techniques. From Figs. 2.16– 2.19, it is observed that the maximum amplitude of dominant harmonics obtained is more with PD-PWM and then reduces with POD-PWM and then reduces to nearly constant value with remaining two PWM techniques. It is also noted that all these spectrums are independent of the modulation index.

The simulations for 5L-ANPCI are also performed with various values of modu-

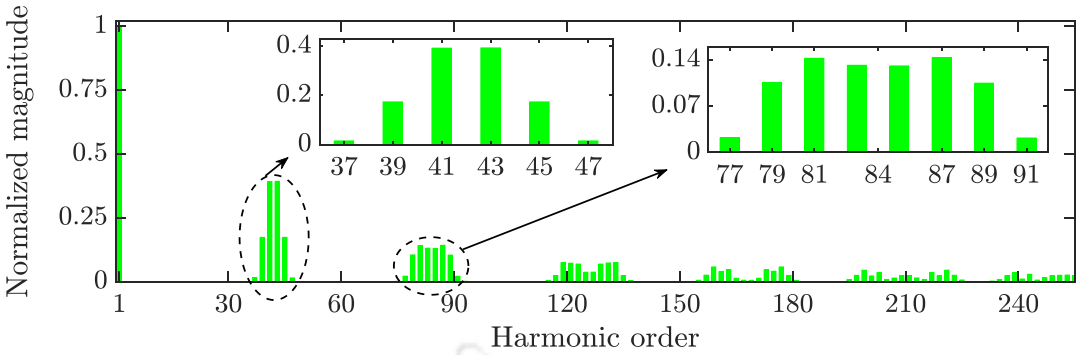


Fig. 2.14. Normalized harmonic spectrum of v_{an} for 5L-ANPCI using APOD-PWM technique with $M = 0.4$, frequency modulation ratio $(m_f) = 42$, switching frequency $(f_{s1}) = 2.1$ kHz, and base voltage of 200 V.

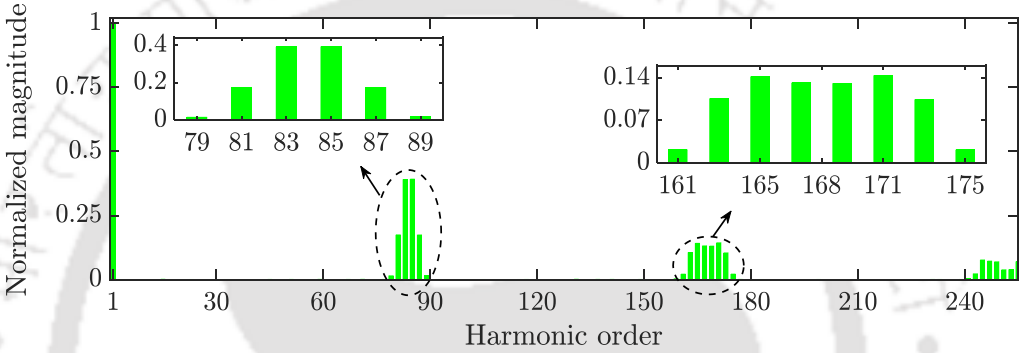


Fig. 2.15. Normalized harmonic spectrum of v_{an} for 5L-ANPCI using PDS-PWM technique with $M = 0.4$, frequency modulation ratio $(m_f) = 42$, switching frequency $(f_{s1}) = 2.1$ kHz, and base voltage of 200 V.

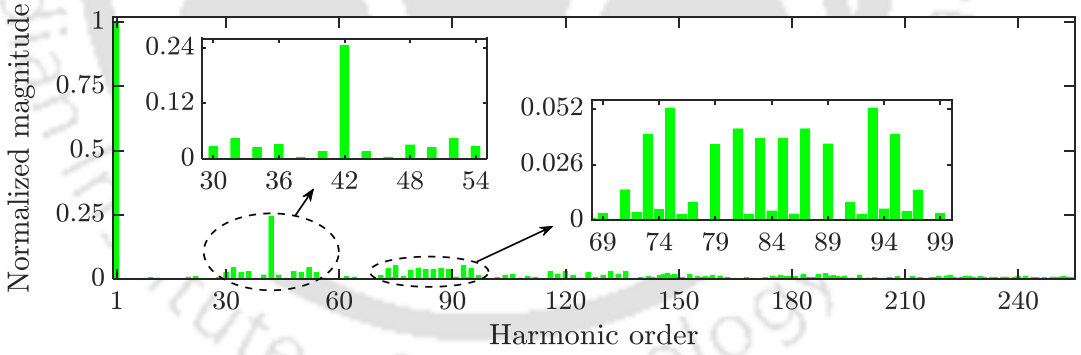


Fig. 2.16. Normalized harmonic spectrum of v_{an} for 5L-ANPCI using PD-PWM technique with $M = 0.9$, frequency modulation ratio $(m_f) = 42$, switching frequency $(f_{s1}) = 2.1$ kHz, and base voltage of 450 V.

lation index (M). Table 2.2 lists the THD values obtained with respect to the modulation index (M) varied from 0.1 to 1, considering maximum harmonic order as 255 for all the PWM techniques. Plot of THD vs. M is shown in Fig. 2.20. Considering entire range of the modulation index, the results show that the PD, POD and APOD-PWM techniques are producing nearly same THD for v_{an}, whereas PDS-PWM technique produces low THD compared to the remaining three PWM techniques. Because the effective switching frequency

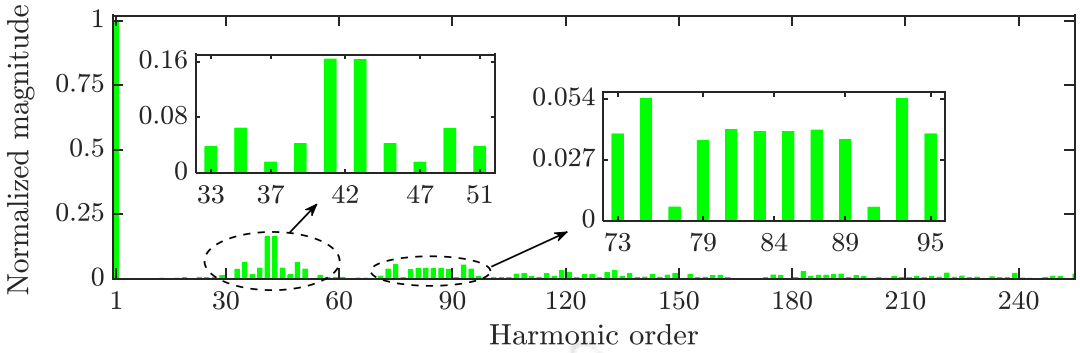


Fig. 2.17. Normalized harmonic spectrum of v_{an} for 5L-ANPCI using POD-PWM technique with $M = 0.9$, frequency modulation ratio $(m_f) = 42$, switching frequency $(f_{s1}) = 2.1$ kHz, and base voltage of 450 V.

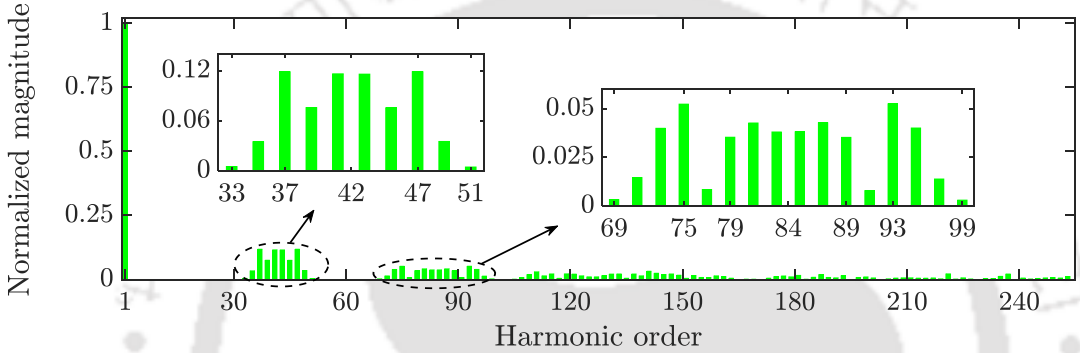


Fig. 2.18. Normalized harmonic spectrum of v_{an} for 5L-ANPCI using APOD-PWM technique with $M = 0.9$, frequency modulation ratio $(m_f) = 42$, switching frequency $(f_{s1}) = 2.1$ kHz, and base voltage of 450 V.

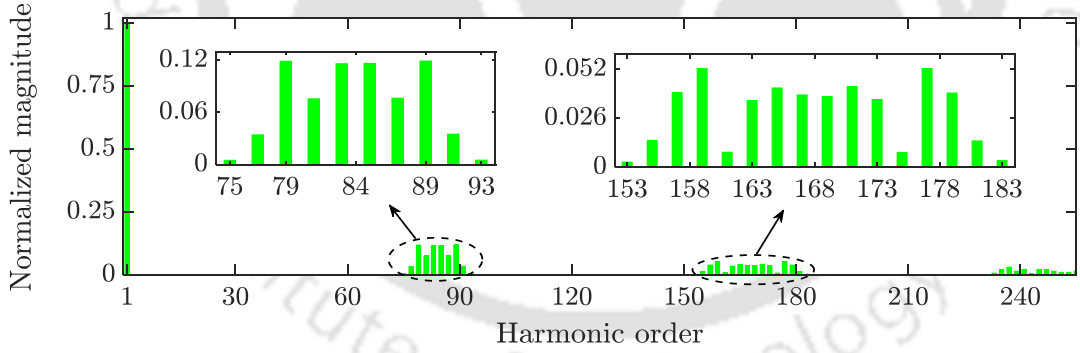


Fig. 2.19. Normalized harmonic spectrum of v_{an} for 5L-ANPCI using PDS-PWM technique with $M = 0.9$, frequency modulation ratio $(m_f) = 42$, switching frequency $(f_{s1}) = 2.1$ kHz, and base voltage of 450 V.

of ANPCI with PDS-PWM technique is two times the carrier frequency due to which the dominant harmonics in v_{an} appear at twice the integral multiples of carrier frequency. As the dominant harmonics are shifted to twice the integral multiples of carrier frequency, the filter requirement is reduced for 5L-ANPCI with PDS-PWM technique. When M is 0.1, the minimum THD in the PWM output voltage of 5L-ANPCI is obtained with PDS-PWM technique as 198.66%, whereas maximum THD is obtained with APOD-PWM technique as

Table 2.2. THD VALUES OBTAINED FOR v_{an} WITH RESPECT TO M CONSIDERING PD, POD, APOD, AND PDS-PWM TECHNIQUES

Modulation index (M)	Total harmonic distortion (%)			
	PD-PWM	POD-PWM	APOD-PWM	PDS-PWM
0.1	213.938	213.786	214.034	198.66
0.2	140.867	140.879	140.851	134.438
0.3	101.827	101.787	101.8505	97.86
0.4	73.587	73.559	73.598	70.88
0.5	49.247	49.159	49.338	46.61
0.6	41.947	41.734	42.08	39.567
0.7	39.844	39.838	39.98	37.843
0.8	36.709	36.489	37.032	35.09
0.9	31.95	31.78	31.8738	30.558
1.0	25.473	25.28	25.842	23.986

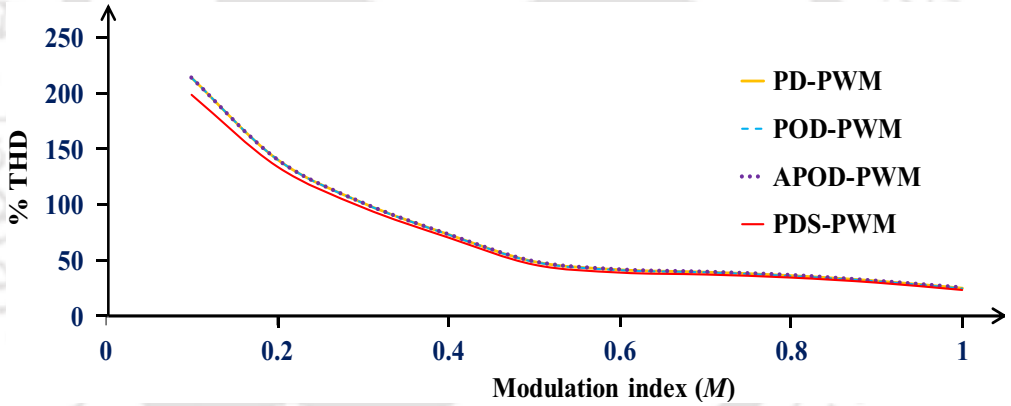


Fig. 2.20. Plot of THD vs. M for v_{an} considering PD, POD, APOD, and PDS-PWM techniques.

214.03%. When M is 1.0, the minimum THD in the PWM output voltage of 5L-ANPCI is obtained with PDS-PWM technique as 23.98%, whereas the maximum THD is obtained with APOD-PWM technique as 25.842%. Hence for the rest of the thesis, the PDS-PWM technique is chosen.

2.4 CAPACITOR VOLTAGE BALANCING STRATEGIES

The DC-link capacitor voltages unbalancing causes balancing problem of Neutral Point Potential (NPP). To achieve DC-link capacitor voltage balancing and FC voltage regulation in ANPCI, many modulation strategies have been presented [85], such as Phase-

Shifted PWM (PS-PWM) [84], Selective-Harmonic-Elimination (SHE) PWM [86] and Zero-Sequence voltage injection [87]. However, these methods are suitable for three-phase applications only. The DC-link voltage imbalance problem for the three-phase ANPCI is solved by modifying the converter switching pattern according to a control strategy [88]. Considering the DC-link capacitor voltages are balanced, the FC voltage of a three-phase five-level ANPCI is regulated in [84] by adding optimum zero-sequence voltage.

In single-phase systems, the inverter's DC-link experiences double line frequency ripple and regulating NPP during dynamic conditions may not be possible using modified control strategies [28]. In single-phase applications, the DC-link of the ANPCI may also experience voltage variation and it is important to keep the DC-link neutral point voltage balanced using a suitable method. In single-phase ANPCI, redundant switching states allow full regulation of FC voltage and partial regulation of DC-link capacitor voltages. The voltages of DC-link capacitors and FC of single-phase ANPCI can be balanced using various voltage balancing methods given in [28–32, 89]. In [89], optimized switching pulse patterns for single-phase five-level ANPCI are obtained based on SHE and iterative method. The basic objective is to maintain THD and individual harmonic magnitudes below the acceptable range. If there are multiple pulse patterns meeting these objectives, then the solution with minimum FC voltage deviation is chosen which helps in FC voltage regulation. But no information is given in [89] about DC-link capacitor voltage balancing. A PWM modulator is proposed in [28] regulates the FC voltage to follow half of upper/lower DC-link capacitor's voltage depending on the sign of reference output voltage. This strategy reduces THD in the load voltage, however because in each half-cycle only one DC-link capacitor is providing the energy, it will have a line-frequency voltage disturbance, resulting in the line frequency voltage ripple in FC. Additionally, after each zero-crossing point of output current, the FC voltage will change suddenly because its reference voltage is changed. So, the complexity of modulation is increased to reduce THD in the output current. Alternate redundant switching states are applied in [30, 31] to balance the FC voltage in each switching cycle resulting in arbitrary FC voltage. A duty cycle adjustment strategy is implemented in [32] to balance

the DC-link capacitor voltages. In this strategy also alternate redundant switching states are utilized to balance the FC voltage in each switching cycle resulting in arbitrary FC voltage. In [90], a simplified single carrier PWM method for single-phase five-level ANPCI with capacitor voltage self-balancing is presented. By employing the sensor-less switching method, the FC is equally charged and discharged in each PWM period which causes sensor-less voltage balancing of FC. A strategy based on tolerance levels defined for DC-link capacitor voltages and FC voltage is proposed in [29] to maintain near constant FC voltage and balance NPP under any load power factor. Some of these strategies are named as Strategy-I−Strategy-IV. The Strategy-I [28] and Strategy-IV [29] are implemented for eight-switch five-level ANPCI (8S-5L-ANPCI), while the Strategy-II [30, 31] and Strategy-III [32] are implemented for seven-switch five-level ANPCI (7S-5L-ANPCI).

In this section, all these four strategies are customized for 8S-5L-ANPCI and their performance is compared. To compare the performance of four capacitor voltage balancing strategies, the single-phase five-level ANPCI is simulated with all the four strategies in PSCAD/EMTDC platform and the results are presented.

2.4.1 Strategy-I

The capacitor voltage balancing strategy proposed in [28] is shown in Fig. 2.21, where the reference value for the fundamental component of v_{an} is represented as v^*_{an1}, which is given by,

$$v^*_{an1} = M \cdot \sin(\omega_o t) \cdot \frac{V_{DC}}{2} = m_a \cdot \frac{V_{DC}}{2} \tag{2.9}$$

Here M is the modulation index and m_a is the sinusoidal modulation signal. As shown in Fig. 2.21, the first step is to select the three voltage levels of the ANPCI nearest to v^*_{an1}. Out of these three voltage levels, two voltage levels, $(V_L,\ V_U)$ are finally chosen such that the FC voltage v_{FC} follows its reference value, v^*_{FC}, given by [28],

$$v^*_{FC} = \frac{v_{C1}}{2} \quad \text{if} \quad v^*_{an1} > 0$$

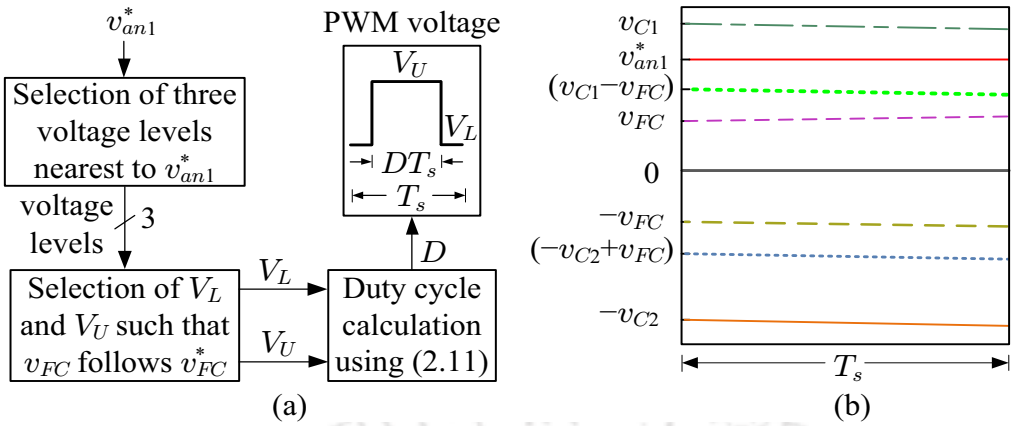


Fig. 2.21. Capacitor voltage balancing strategy-I: (a) block diagram (b) voltage levels.

$$v^*_{FC} = \frac{v_{C2}}{2} \quad \text{if} \quad v^*_{an1} < 0 \tag{2.10}$$

For example, in a particular switching cycle shown in Fig. 2.21(b), the three nearest voltage levels to v^*_{an1} are v_{C1}, $(v_{C1} - v_{FC})$ and v_{FC}, among which v_{C1} is chosen as the upper voltage level V_U. The lower voltage level V_L depends on whether FC has to be charged or discharged to follow v^*_{FC}. This selection is made based on polarity of i_L and the data given in Table 2.1. Once the voltage levels V_L and V_U are decided, the duty cycle D is calculated using switching cycle averaging as

$$D = \frac{(v^*_{an1} - V_L)}{(V_U - V_L)} \tag{2.11}$$

The final PWM voltage generated using this method is shown in Fig. 2.21(a). It is equal to V_U for $D \cdot T_s$ interval and V_L for $(1-D) \cdot T_s$ interval.

To verify the Strategy-I, the simulation is performed using the parameters listed in Table 2.3 and the results are presented in Fig. 2.22. Note that there is a step change in the load resistance at time $t = t_o$, as shown in this figure. Fig. 2.22(b) shows the zoomed waveforms of Fig. 2.22(a) around the load step instant, t_o. From Fig. 2.22, it can be observed that the average values of v_{C1}, v_{C2} and v_{FC} are maintained at $\frac{V_{DC}}{2}$, $\frac{V_{DC}}{2}$ and $\frac{V_{DC}}{4}$, respectively, before the load step change. However, the capacitor voltages are diverged from their reference values after the load step change, which means that the Strategy-I works only for

Table 2.3. SIMULATION PARAMETERS

Electrical parameters⋆	V_{DC}	f_o	f_{s1}	M
Attributes	800 V	50 Hz	10 kHz	0.9
Component parameters	L_f	C_1 & C_2	FC	C_f
Attributes	2 mH	1 mF	0.53 mF	20 μF

⋆ $f_o = \frac{\omega_o}{2\pi}$ is the fundamental frequency and f_{s1} is the switching frequency of ANPCI.

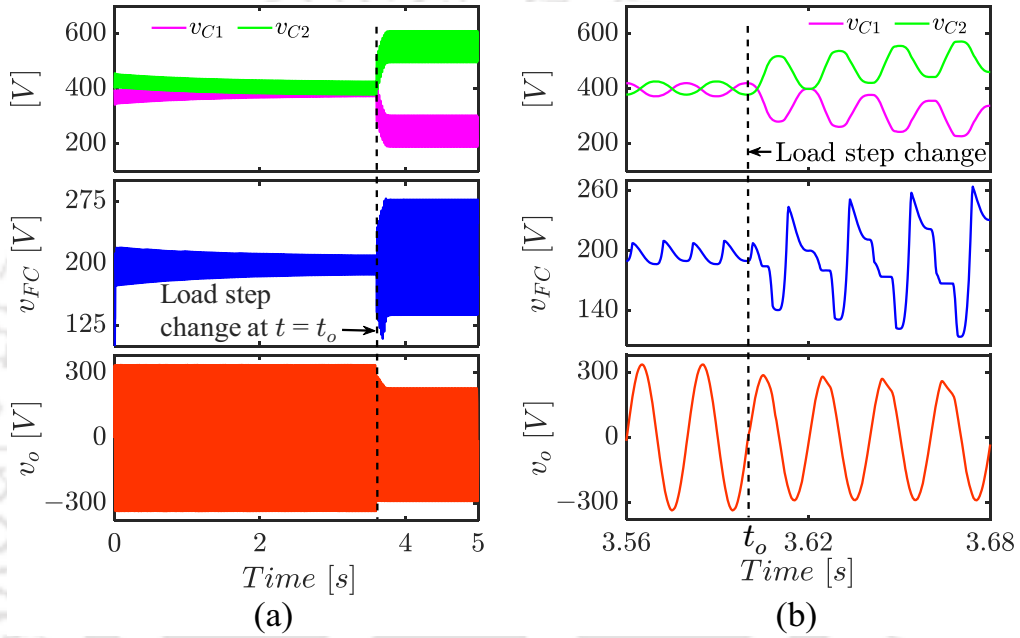


Fig. 2.22. Simulation waveforms obtained for 8S-5L-ANPCI with (a) Strategy-I (b) zoomed waveforms of Strategy-I near $t = t_o$.

a particular range of load current. Further, as mentioned in Table 2.6, the load THD during $t < t_o$ is maintained very low despite of the large peak-to-peak ripple in v_{C1} and v_{FC}, which is the main advantage of Strategy-I.

2.4.2 Strategy-II

In this strategy [30, 31], the desired PWM voltage levels in each switching cycle are obtained by comparing sinusoidal modulation signal m_a with triangular carrier signals v_{t1} and v_{t2} as shown in Fig. 2.23. Once the desired v_{an} is obtained, alternate redundant switching states are applied in the switching cycle when $v_{an} = \pm\frac{V_{DC}}{4}$. In this way, in one switching cycle, the energy supplied to the FC will be equal to the energy drawn from FC,

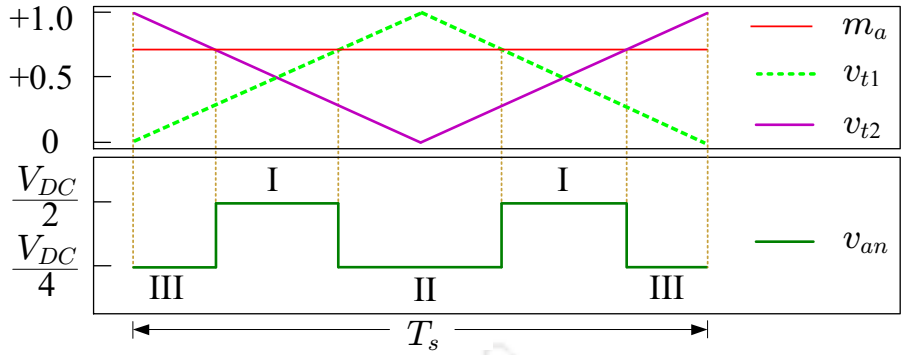


Fig. 2.23. Selection of PWM voltage levels and corresponding states using capacitor voltage balancing strategy-II.

which causes the switching cycle averaged voltage of FC to be constant.

To verify the Strategy-II, the simulation is performed using the parameters listed in Table 2.3 and the results are presented in Fig. 2.24. Note that there is a step change in the load resistance at time $t = t_o$, as shown in this figure. Fig. 2.24(b) shows the zoomed waveforms of Fig. 2.24(a) around the load step instant, t_o. As shown in Fig. 2.24, the average values of both v_{C1} and v_{C2} are maintained at $\frac{V_{DC}}{2}$, before and after the load step change. However, the voltage v_{FC} is settled at an arbitrary value other than $\frac{V_{DC}}{4}$. Also, as listed in Table 2.6, the settling time of v_{FC} using this strategy is quite high compared to other three strategies.

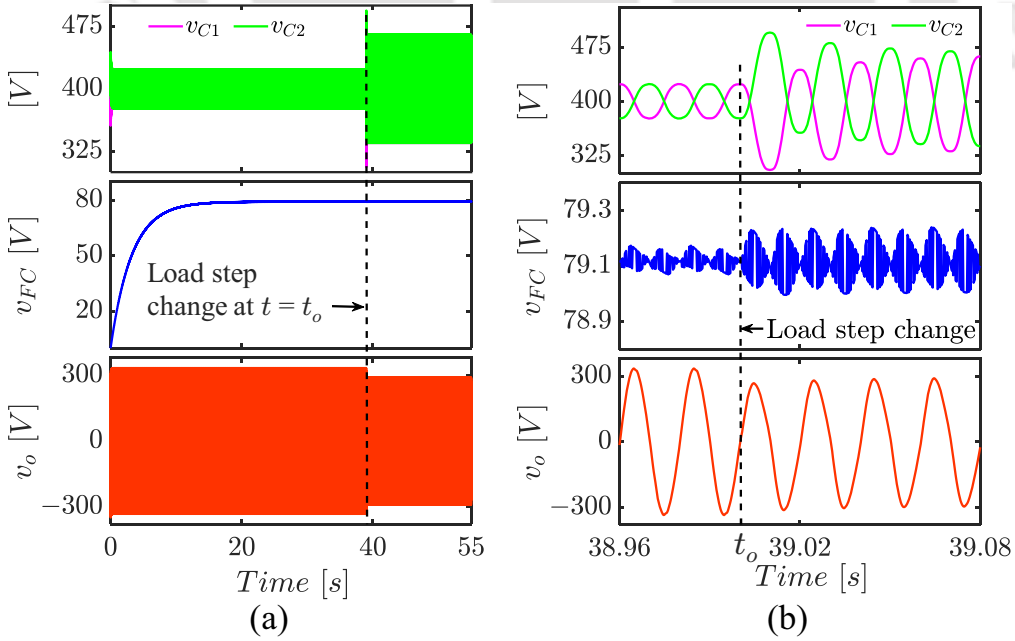


Fig. 2.24. Simulation waveforms obtained for 8S-5L-ANPCI with (a) Strategy-II using PDS-PWM technique (b) zoomed waveforms of Strategy-II near $t = t_o$.

2.4.3 Strategy-III

In [32], the authors have proposed an improvement to Strategy-II by incorporating regulation of DC-link capacitor voltage v_{C1} of ANPCI, using 1-level state duty cycle adjustment. Fig. 2.25 shows the block diagram for implementation of Strategy-III. Here, a small duty cycle shift ($\triangle d$) is introduced in the switching signals generated using Strategy-II, as shown in Fig. 2.26. The value of $\triangle d$ is calculated by a PI controller so that the voltage v_{C1} follows its reference value, $+\frac{V_{DC}}{2}$. Thus both the DC-link capacitor voltage and switching cycle averaged FC voltage can be balanced using this strategy.

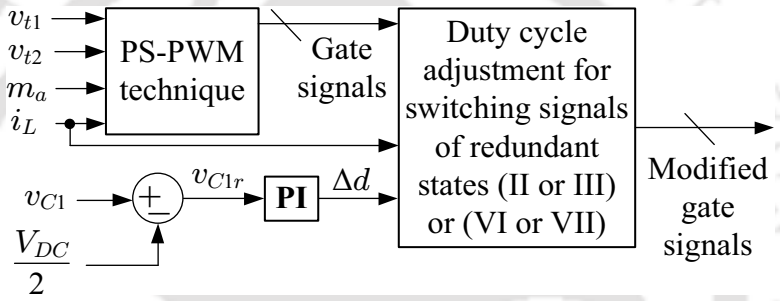


Fig. 2.25. Capacitor voltage balancing strategy-III.

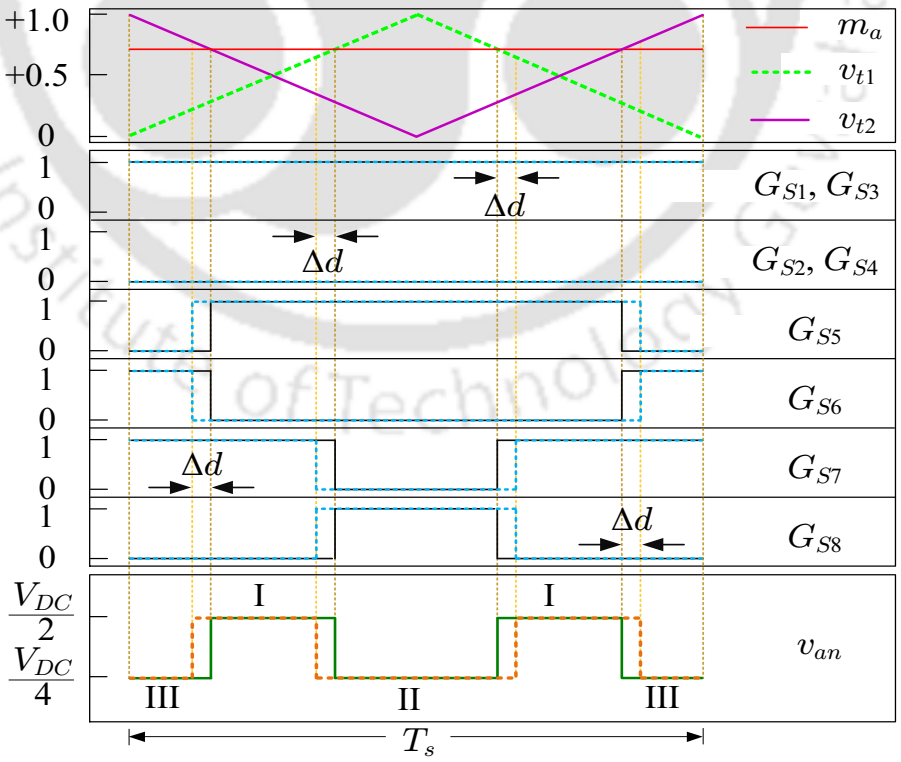


Fig. 2.26. Switching pulses generation using Strategy-III.

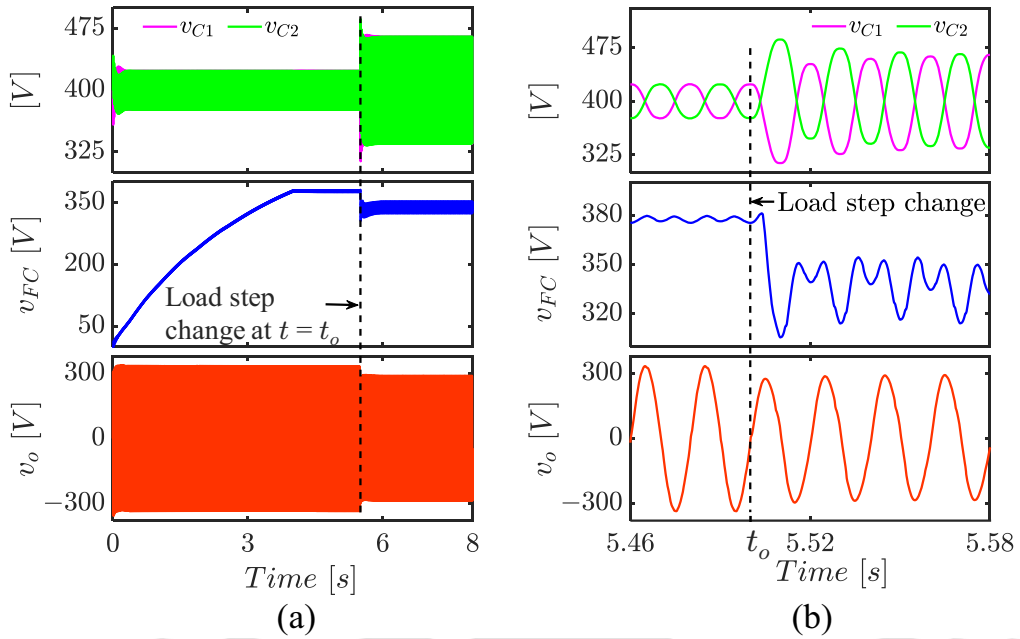


Fig. 2.27. Simulation waveforms obtained for 8S-5L-ANPCI with (a) Strategy-III using PDS-PWM technique (b) zoomed waveforms of Strategy-III near $t = t_o$.

To verify the Strategy-III, the simulation is performed using the parameters listed in Table 2.3. Fig. 2.27 shows the simulation results of ANPCI with Strategy-III, which is an upgraded version of Strategy-II. Note that there is a step change in the load resistance at time $t = t_o$, as shown in this figure. Fig. 2.27(b) shows the zoomed waveforms of Fig. 2.27(a) around the load step instant, t_o. The average values of v_{C1} and v_{C2} are maintained at $\frac{V_{DC}}{2}$, before and after the load step change using Strategy-III. However, v_{FC} settles to an arbitrary value depending on the load resistance. Note that the settling time of v_{FC} is much lower compared to that in Strategy-II.

2.4.4 Strategy-IV

A capacitor voltage balancing strategy is presented in [29], which maintains the FC voltage, v_{FC} and DC-link capacitor voltage, v_{C1}, within $v_{FC} \pm \epsilon$ and $v_{C1} \pm \epsilon$, respectively. The capacitor voltage balancing strategy proposed in [29] can be explained using the flowchart given in Fig. 2.28 and Tables 2.4 and 2.5. Here, v_{C1}^* and v_{FC}^* are set to $+\frac{V_{DC}}{2}$ and $+\frac{V_{DC}}{4}$, respectively. As shown in the flowchart, in each switching cycle, the voltage level v_{an} is found using (2.8). Then the algorithm checks whether the redundant switching states are available in Table 2.1 or not. Since redundant states are not available for voltage level

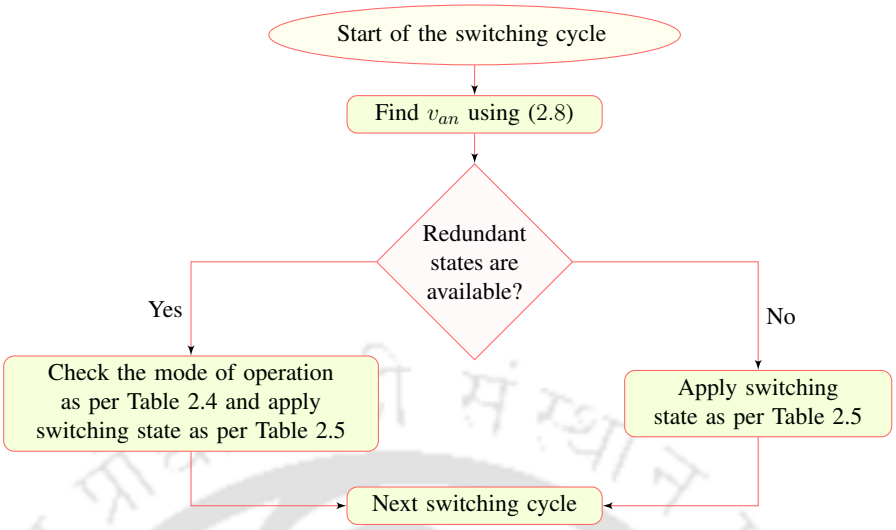


Fig. 2.28. Flowchart for implementation of capacitor voltage balancing strategy-IV.

$+\frac{V_{DC}}{2}$, switching state I is directly applied without checking any other conditions, as given in Table 2.5. In case the redundant switching states are available, the algorithm checks for the deviations of v_{FC}, v_{C1} and polarity of i_L before determining the switching state to be applied. For example, if the desired voltage level is $+\frac{V_{DC}}{4}$, there are two possible switching states. So, as shown in Tables 2.4 and 2.5, the algorithm checks whether the v_{FC} is within allowable range or not. If the value of v_{FC} is less than the tolerance range (Mode M1 in Table 2.4), the FC needs to be charged. Now if the inductor current i_L is positive, switching state II will be applied to the ANPCI and if i_L is negative, switching state III will be applied.

Table 2.4. OPERATING MODES DEFINED BASED ON THE DEVIATION OF THE CAPACITOR VOLTAGES FOR ANPCI

Condition for capacitor voltages		Mode of
v_{FC}	v_{C1}	operation
$v_{FC} < (v^*_{FC} - \epsilon)$	—	M1
$v_{FC} > (v^*_{FC} + \epsilon)$	—	M2
$(v^*_{FC} - \epsilon) < v_{FC} < (v^*_{FC} + \epsilon)$	$v_{C1} < (v^*_{C1} - \epsilon)$	M3
	$v_{C1} > (v^*_{C1} + \epsilon)$	M4
	$(v^*_{C1} - \epsilon) < v_{C1} < (v^*_{C1} + \epsilon)$	M5

Table 2.5. SELECTION OF SWITCHING STATES FOR THE ANPCI BASED ON CAPACITOR VOLTAGE BALANCING STRATEGY

Voltage level	Redundant states	Mode as per	State to be applied	
v_{an}	are available?	Table 2.4	$i_L > 0$	$i_L < 0$
$+\frac{V_{DC}}{2}$	No	Not checked	I	I
$+\frac{V_{DC}}{4}$	Yes	M1 or M4	II	III
		M2 or M3	III	II
		M5	III	III
0	Yes	Not checked	IV	V
$-\frac{V_{DC}}{4}$	Yes	M1 or M3	VI	VII
		M2 or M4	VII	VI
		M5	VI	VI
$-\frac{V_{DC}}{2}$	No	Not checked	VIII	VIII

If v_{FC} is already within the acceptable range, then the algorithm checks the value of v_{C1}. If v_{C1} is below the tolerance range (Mode M3), then it has to be charged. Now if i_L is negative, State II is applied so that v_{C1} is increased. However, if i_L is positive, there is no switching state to charge C_1. In this case, State III will be chosen to avoid further decrease in v_{C1}. If the algorithm detects that both v_{FC} and v_{C1} are within allowable range (Mode M5), then State III will be applied, irrespective of the polarity of i_L. Similarly, the algorithm chooses between other redundant switching states as given in Fig. 2.28 and Tables 2.4 and 2.5. Note that, if v_{C1} is maintained within the acceptable range, then the value of v_{C2} will be regulated automatically, so that (2.2) is satisfied.

To verify the Strategy-IV, the simulation is performed using the parameters listed in Table 2.3 and the results are presented in Fig. 2.29. Note that there is a step change in the load

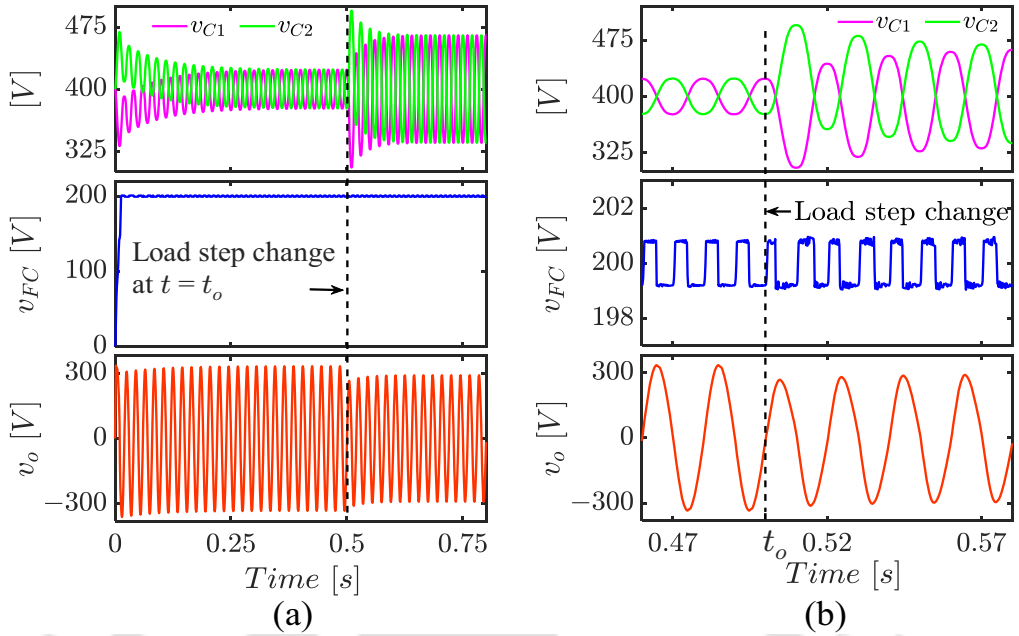


Fig. 2.29. Simulation waveforms obtained for 8S-5L-ANPCI with (a) Strategy-IV using PDS-PWM technique (b) zoomed waveforms of Strategy-IV near $t = t_o$.

resistance at time $t = t_o$, as shown in this figure. Fig. 2.29(b) shows the zoomed waveforms of Fig. 2.29(a) around the load step instant, t_o. As shown in Fig. 2.29, the average values of v_{C1}, v_{C2} and v_{FC} are maintained at $\frac{V_{DC}}{2}$, $\frac{V_{DC}}{2}$ and $\frac{V_{DC}}{4}$, respectively, both before and after the load step change. Also, the settling time of the capacitor voltages is significantly lower compared to the above three strategies. In addition, this strategy is successful in tightly regulating the average value of v_{FC} to $\frac{V_{DC}}{4}$ with negligible peak-to-peak ripple, which was not possible in previous three strategies.

Table 2.6 lists the peak-to-peak ripple in DC-link capacitor voltage, FC voltage and percentage total harmonic distortion (%THD) in output voltage, v_o of the ANPCI, obtained from waveforms of all the four strategies given in Figs. 2.22, 2.24, 2.27 and 2.29. From the simulation results of Figs. 2.22, 2.24, 2.27 and 2.29, and Table 2.6, it can be concluded that the performance of Strategy-IV is better compared to other three strategies, in terms of regulation of capacitor voltages to their reference values, minimizing the peak-to-peak ripple and settling time of FC voltage. Hence in the rest of the thesis, Strategy-IV is employed for ANPCI.

Table 2.6. P-P RIPPLE IN v_{C1} AND v_{C2} (ΔV_C), P-P RIPPLE IN v_{FC} (ΔV_{FC}), SETTLING TIME OF FC (t_s), %THD IN v_o OBTAINED FROM FIGS. 2.22, 2.24, 2.27, AND 2.29.

Strategy	Before step change				After step change				Remarks
	t_o (s)	ΔV_C (V)	ΔV_{FC} (V)	t_s (s)	THD (%)	ΔV_C (V)	ΔV_{FC} (V)	t_s (s)	THD (%)	
I	3.6	53.67	23.2	3.11	0.26	—	—	—	—	System is unstable for $R_L < 16\ \Omega$ as v_{C1} and v_{C2} are diverged
II	39	47.1	0.11	20	2	130.1	0.22	4.5	5.2	v_{FC} is arbitrarily settled with very large settling time
III	5.5	47.22	4.27	4	1.95	130	28.98	0.01	4.75	v_{FC} is arbitrarily settled with very large settling time
IV	0.5	47.03	1.6	0.01	1.92	130.1	1.91	—	5.01	v_{FC} is quickly settled and its reference value is maintained

2.5 CLOSED-LOOP SRF-DQ CONTROL OF ANPCI

The operation of single-phase five-level ANPCI presented in Section 2.2 has been verified in both open-loop and closed-loop modes of the converter. For closed-loop operation, an SRF-dq controller [91] has been developed for the ANPCI to regulate its load voltage v_o to a reference v_o^*. The block diagram of the closed-loop controller is shown in Fig. 2.30, which uses a second-order generalized integrator (SOGI) [92] as shown in Fig. 2.31. The SOGI shown in Fig. 2.31(a) considers the input quantity i_L and generates its orthogonal

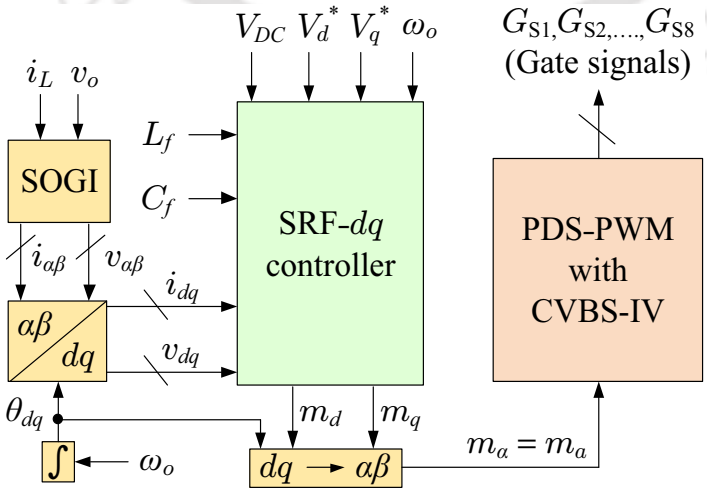


Fig. 2.30. Block diagram of closed-loop controller for ANPCI.

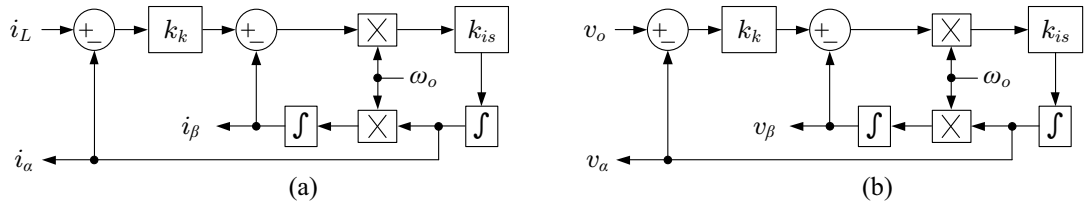


Fig. 2.31. Detailed diagram of SOGI.

quantities i_α and i_β in $\alpha\beta$ frame. Similarly, SOGI shown in Fig. 2.31(b) considers the input quantity v_o and generates its orthogonal quantities v_α and v_β in $\alpha\beta$ frame. Here, k_{is} is the integral gain; and k_k is the constant. These $\alpha\beta$-domain signals are then transformed into dq-domain using the transformation given by,

$$T_{\alpha\beta\to dq} = \begin{bmatrix} \sin\left(\theta_{dq}\right) & -\cos\left(\theta_{dq}\right) \\ \cos\left(\theta_{dq}\right) & \sin\left(\theta_{dq}\right) \end{bmatrix} \tag{2.12}$$

The SRF-dq controller block takes the dq-domain quantities $(i_d,\ i_q)$, $(v_d,\ v_q)$ and the reference voltage $\left(V_d^*,\ V_q^*\right)$ as inputs. The SRF-dq controller has a cascaded control structure with an inner current controller and an outer voltage controller, which are depicted in the block diagram of Fig. 2.32. It can be seen that PI controllers are used to regulate both d-axis and q-axis currents and voltages. To design these PI controllers, the circuit diagram of ANPCI is modeled as,

$$\frac{\mathrm{d}v_o}{\mathrm{d}t} = \left(\frac{i_L}{C_f}\right) - \left(\frac{v_o}{R_L C_f}\right) \tag{2.13}$$

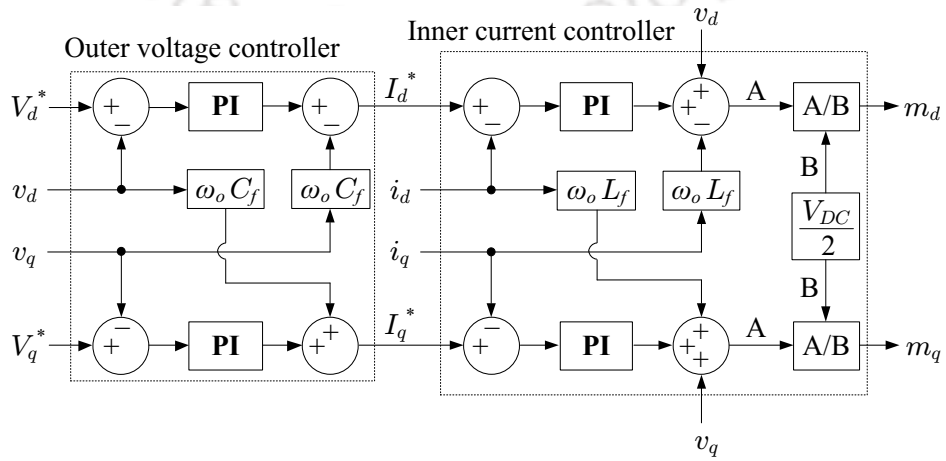


Fig. 2.32. Detailed diagram of SRF-dq controller for ANPCI.

Table 2.7. PI CONTROLLER PARAMETERS

Parameters	Current control loop	Voltage control loop
Proportional constant (k_p)	0.8	6.5
Integral constant (k_i)	45	10

$$\frac{\mathrm{d}i_L}{\mathrm{d}t} = \frac{(v_{an} - v_o - i_L r_L)}{L_f} \tag{2.14}$$

where R_L is the load resistance and r_L is the ESR of L_f. This model is then transformed to dq-domain using the transformation given in (2.12). The mathematical model of ANPCI in dq-domain is given by,

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} -\frac{1}{R_L C_f} & \omega_o \\ -\omega_o & -\frac{1}{R_L C_f} \end{bmatrix} \cdot \begin{bmatrix} v_d \\ v_q \end{bmatrix} + \frac{1}{C_f} \cdot \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{2.15}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -\frac{r_L}{L_f} & \omega_o \\ -\omega_o & -\frac{r_L}{L_f} \end{bmatrix} \cdot \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{1}{L_f} \cdot \begin{bmatrix} v_{and} - v_d \\ v_{anq} - v_q \end{bmatrix} \tag{2.16}$$

The time domain model is then transformed into s-domain, which is given by the transfer functions,

$$\frac{v_d(s)}{i_d(s) + \omega_o C_f v_q(s)} = \frac{R_L}{1 + sR_L C_f} \tag{2.17}$$

$$\frac{v_q(s)}{i_q(s) - \omega_o C_f v_d(s)} = \frac{R_L}{1 + sR_L C_f} \tag{2.18}$$

$$\frac{i_d(s)}{v_{and}(s) - v_d(s) + \omega_o L_f i_q(s)} = \frac{1}{sL_f + r_L} \tag{2.19}$$

$$\frac{i_q(s)}{v_{anq}(s) - v_q(s) - \omega_o L_f i_d(s)} = \frac{1}{sL_f + r_L} \tag{2.20}$$

These transfer functions are used to determine the PI controller parameters and they are listed in Table 2.7. The outer voltage controller generates the dq-domain reference currents, $\left(I_d^*,\ I_q^*\right)$, which are given as inputs to the inner current controller. The current controller block generates the modulation signal $(m_d,\ m_q)$ in SRF, which is again transformed back

Table 2.8. EXPERIMENTAL PARAMETERS

Parameters	Attributes
C_1 and C_2	3.3 mF
FC	2 mF
L_f	2 mH
C_f	20 μF
Fundamental frequency $\left(f_o = \frac{\omega_o}{2\pi}\right)$	50 Hz
Switching frequency (f_{s1})	10 kHz
V_{DC}	128 V
Output power	300 W

into stationary reference frame and then used to generate the gate signals for ANPCI as shown in Fig. 2.30.

2.6 RESULTS AND DISCUSSION

The experimental setup of single-phase ANPCI is developed to validate the analysis. Table 2.8 gives the parameters used for validation and Fig. 2.33 shows the photograph of experimental set-up. The switching signals for the ANPCI are generated using PDS-PWM technique, which is implemented in Texas Instruments TMS320F28335 Digital Signal Controller (DSC) kit. The capacitor voltage balancing strategy and SRF-dq controller are also implemented using the same DSC. The source voltage, V_{DC}, capacitor voltages, v_{C1}, v_{FC} and the load voltage, v_o, are measured using the LEM voltage sensors LV-25P and the inductor current, i_L, is measured using the LEM current sensor LA-55P.

In this section, the results are presented for open-loop and closed-loop operation of the ANPCI.

2.6.1 Validation of PWM Technique and Capacitor Voltage Balancing Strategy

Fig. 2.34 shows the experimental results of ANPCI during open-loop operation. Fig. 2.34(a) shows the steady-state waveforms of DC-link capacitor voltage (v_{C1}), flying capacitor voltage (v_{FC}), load voltage (v_o) and the load current (i_o) with the modulation index, $M = 0.9$. It is observed that the mean value of v_{C1} is half the DC-link voltage, i.e.,

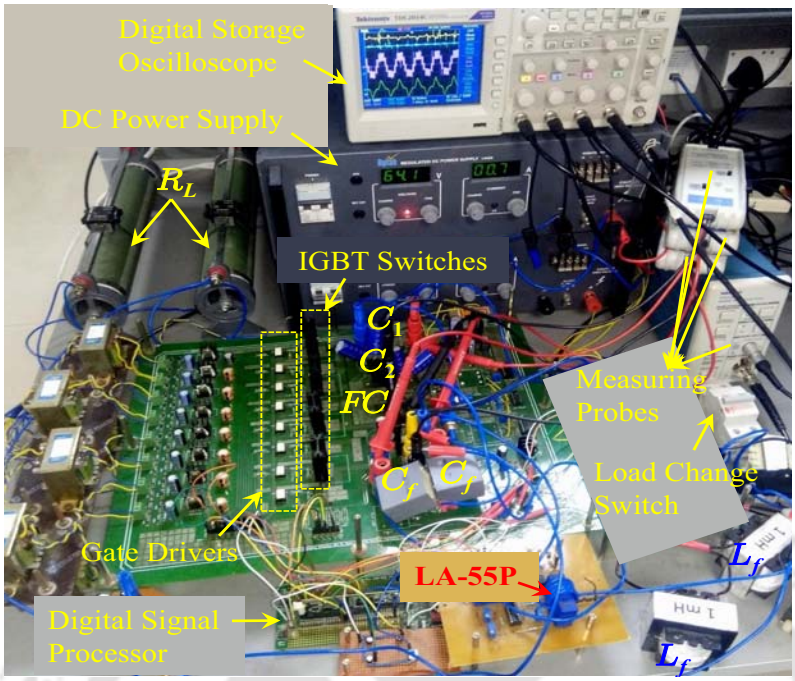


Fig. 2.33. Photograph of the experimental setup.

64 V, with a peak-to-peak (P-P) ripple of 8 V and the mean flying capacitor voltage is 31.9 V with a P-P ripple of 0.8 V. Load voltage and current are sinusoidal and their RMS values are observed as 33.85 V and 6.44 A, respectively. The THD in v_o and i_o are 4.53% and 4.6%, respectively. Fig. 2.34(b) shows the results when modulation index is suddenly changed from 0.9 to 0.4, while the load resistance, R_L, is 5 Ω. It can be observed that, when M becomes below 0.5, a three-level PWM voltage waveform is obtained with a P-P value of 64 V and the RMS value of i_o is reduced to 3.11 A from 6.5 A. Note that the average values of the v_{C1} and v_{FC} are obtained as 62.8 V and 32 V, respectively. Further, the P-P ripple in v_{C1} is reduced to 2.5 V due to reduction in the load current. Fig. 2.34(c) shows the results when the load step change is given from 5 Ω to 10 Ω with $M = 0.9$. The reduction in RMS load current from 6.5 A to 3.39 A can be observed from Fig. 2.34(c). Moreover, the v_{C1} and v_{FC} are maintained at their respective reference values.

2.6.2 Validation of SRF-dq based Closed-Loop Controller

Fig. 2.35 shows the experimental results of ANPCI during closed-loop operation. Fig. 2.35(a) shows the steady-state waveforms using SRF-dq controller for the v_{C1}, v_{FC}, v_o and i_o. The reference load voltages in the dq frame, V_d^* and V_q^*, are set to 46 V and 0 V,

respectively, which corresponds to 32.6 V RMS and 0 V RMS, respectively. In Fig. 2.35(a), the RMS values of the sinusoidal waveforms, v_o and i_o, are obtained as 32.6 V and 6.37 A, respectively, with 5 Ω load resistance. The calculated THD in v_o and i_o are 3.86% and 3.04%, respectively. Also, the mean of v_{C1} and v_{FC} are observed as 63.3 V and 32.1 V, respectively. Fig. 2.35(b) shows the results when the load is suddenly changed from 10 Ω to 5 Ω, with 46 V constant peak reference load voltage. It is observed that the ripple in v_{C1} is increased due to the rise of RMS load current from 3.39 A to 6.36 A. In spite of increase in the RMS load current, the positive peak of v_o tracks its reference value, V_d^*, because of the

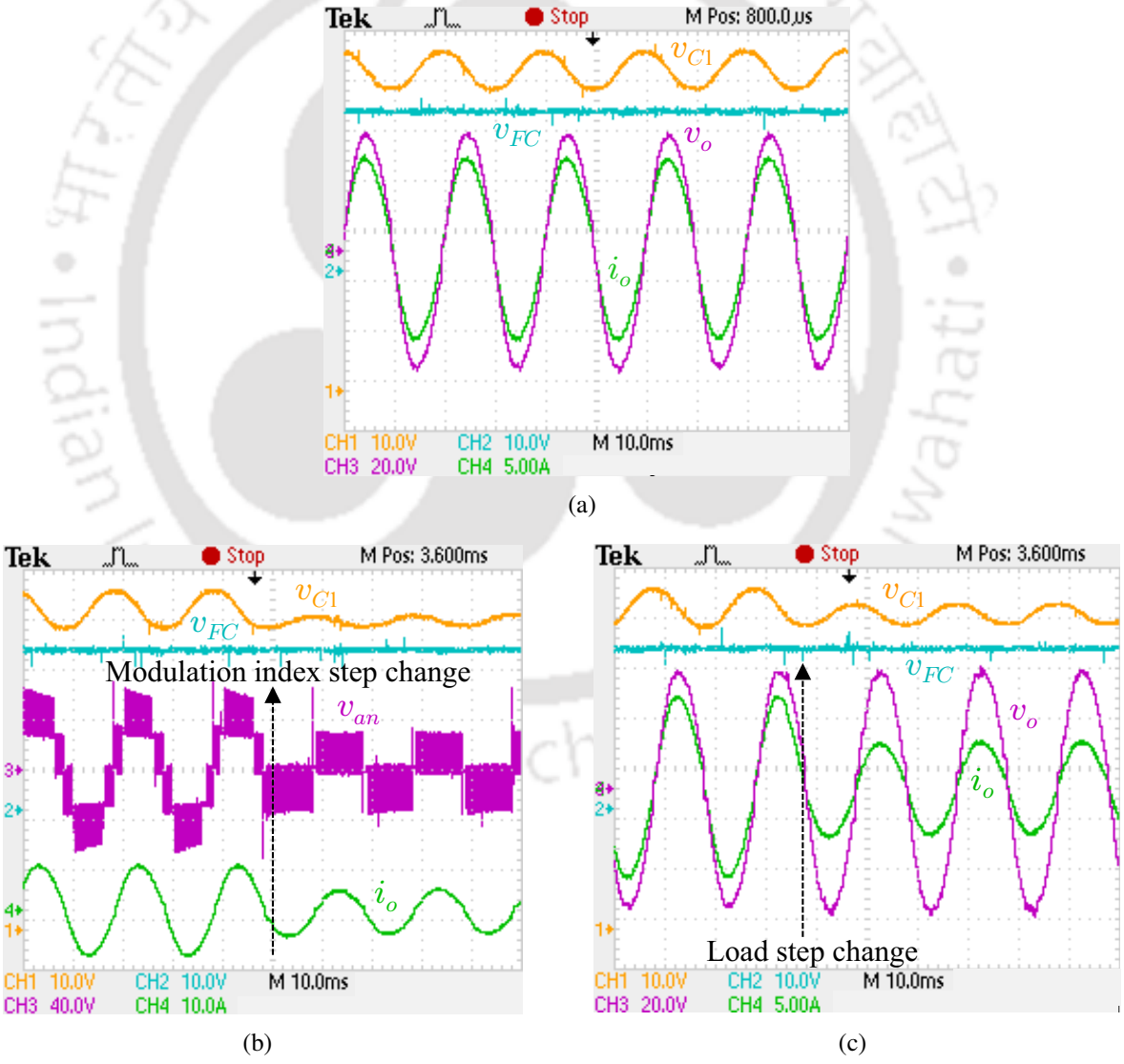


Fig. 2.34. Experimental results in open-loop for (a) steady-state operation (b) step change in the Modulation index from 0.9 to 0.4 (c) step change in the load from 5 Ω to 10 Ω.

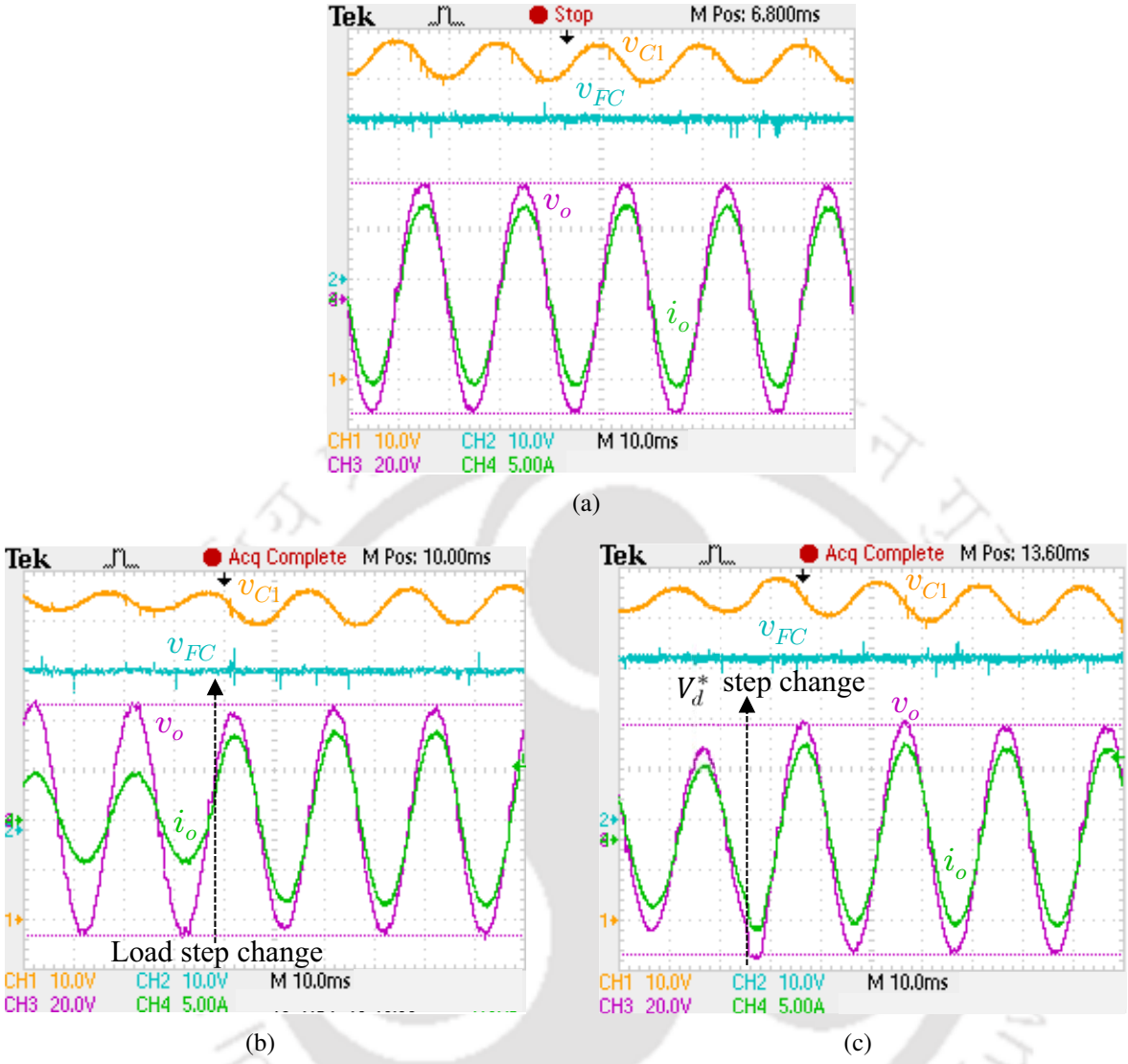


Fig. 2.35. Experimental results in closed-loop for (a) steady-state operation (b) step change in the load from 10 Ω to 5 Ω (c) step change in the reference peak voltage from 36 V to 46 V.

closed-loop controller. Fig. 2.35(c) shows the results when step change in the V_d^* is given from 36 V to 46 V with $R_L = 5\ \Omega$. The RMS load current is 5 A before the step change and 6.53 A after the step change. Note that the load voltage is tracking its reference with in two fundamental cycles.

The closed-loop results shown in Fig. 2.35 confirm the effectiveness of SRF-dq controller in maintaining the load voltage at its reference value during steady-state and transient operations. The results in Figs. 2.34 and 2.35 also confirm the effectiveness of capacitor voltage balancing strategy in both open-loop and closed-loop operation of ANPCI. As small

variation in the v_{FC} causes significant distortion in the v_o, high priority is set to maintain low ripple in the FC voltage rather than the DC-link capacitor voltages in the capacitor voltage balancing strategy. Thus, the FC voltage in Figs. 2.34 and 2.35 is flat with negligible P-P ripple.

2.7 SUMMARY

In this chapter, detailed operation and various capacitor voltage balancing strategies for single-phase five-level ANPCI are presented. The performance of the PD, POD, APOD and PDS-PWM techniques is compared for five-level ANPCI. This chapter has also described four different capacitor voltage balancing strategies for the ANPCI. It is shown that the Strategy-IV performs better than remaining three strategies in maintaining the average value of DC-link capacitor and flying capacitor voltages with minimum settling time. Also, it is shown that remarkable voltage ripple remains in the DC-link capacitor voltages irrespective of the capacitor voltage balancing strategy. An SRF-dq controller is presented and implemented for the single-phase ANPCI. The experiments are conducted in open-loop as well as in closed-loop using SRF-dq controller. Various CVBS and the SRF-dq controller operation are verified using the demonstrated results.

CHAPTER 3

AVERAGED MODELING OF SINGLE-PHASE ANPCI

3.1 INTRODUCTION

In Chapter 1, a brief review of the three classical MLIs, viz., NPC-MLI, FC-MLI, and CHB-MLI as well as ANPCI is discussed. In Chapter 2, detailed operation and steady-state analysis of single-phase five-level ANPCI are presented. The performance of four different PWM techniques is compared for five-level ANPCI. Also, in this chapter four different capacitor voltage balancing strategies (CVBS) are discussed and their performance is compared for the ANPCI. Further, an SRF-dq controller is presented and implemented for the single-phase ANPCI. Finally, various CVBS and the SRF-dq controller operation are verified using the demonstrated results.

In the present chapter, i.e., Chapter 3, a Dynamic Average Circuit Model (DACM) of ANPCI is developed and presented. Also, the DACM is verified using the switching circuit and experimental results. In addition, the effectiveness of the model is also demonstrated using a simple stand-alone PV system with ANPCI as the power conversion stage.

This chapter is organized as follows. In Section 3.2, motivation for the average modeling of the power electronic converters is presented. In Section 3.3, the DACM of the five-level ANPCI is presented without considering non-idealities. The DACM of five-level ANPCI considering the non-idealities is presented in Section 3.4. Moreover, considering N-levels, the DACM of ANPCI is presented in Section 3.5. Further Section 3.6 presents results for validation of the dynamic average circuit model in open-loop and closed-loop operation of ANPCI. Section 3.7 describes the operation of a stand-alone PV system with SRF-dq controlled ANPCI as power converter interface. Section 3.7 also presents the results

to demonstrate strength of the average circuit model developed in this thesis. Finally, this chapter is summarized in Section 3.8.

3.2 MOTIVATION FOR AVERAGE MODELING

Modeling and computer-based simulations are the essential steps for design and analysis of power-electronic-based systems such as microgrids, industrial drives, solar and wind energy conversion systems, etc., [93–100]. For these system-level studies, the power electronic converters can be modeled and simulated by using either detailed switching circuit or averaged model. The Switching Circuit Model (SCM) based approach simulates every switching instant of the power semiconductor devices and it is used for capturing the switching frequency components in the converter waveforms. Here, the simulation time-step should be much less than the switching time period of the converter. Hence the switching circuit model based simulations require extensive computational resources while performing system-level studies, involving large number of power electronic converters. On the other hand, the averaged models of power electronic converters are developed by approximating the converter waveforms after omitting the switching-frequency components. Using the averaged model based approach, the averaged steady-state and dynamic waveforms of the converters can be accurately predicted with fairly large simulation time-steps. For system-level studies, the average model based approach will significantly reduce the time and computational resources required for the study. Although the converter switching frequency components cannot be evaluated using averaged models, they are generally of less interest while analyzing large-scale electrical systems.

In literature, various average modeling approaches are presented for power electronic converters. Early works on average modeling are mainly focused on dc-to-dc converters and diode/thyristor-based rectifiers. The synthesis of equivalent averaged circuit models for different dc-to-dc converters using state-space averaging and in-place or direct-circuit averaging has been described in [96, 101]. In [97, 98, 102], dynamic average value models are presented for line commutated converter-synchronous machine system using analytical

average value modeling (AAVM) approach. Here, the ac side variables of the system in each sub-interval of a particular switching interval are transformed into dq-reference frame and then their averaged values are determined analytically. These averaged values in each sub-interval are carefully integrated to obtain the averaged value model for a given operating mode. In [99, 100], Parametric Average Value Models (PAVM) are developed for the machine-rectifier systems. In this approach, the average-value relationship among the variables is established using different parametric functions, which are generally determined by simulating the detailed system model. Unlike AAVM, the PAVM is easier to develop and it can be used to simulate the converter in wide range of operating conditions.

The averaged models of pulse width modulated (PWM) two-level and multilevel inverters (MLIs) are presented in [103–108]. In [103], state-space averaging approach is used to obtain two separate models for positive and negative half-cycle of the filter inductor current, resulting in a discontinuous converter model. In [104], a comprehensive dynamic model of three-phase four-level diode clamped inverter is derived based on the generalized state-space averaging method. The authors have used line-cycle averaging to remove the discontinuity in the converter model. However, line-cycle averaging limits the validity of the model to half the fundamental frequency. In [105], differential equations based modeling is used based on state space form. The switches are considered as ideal and unity power factor operation is assumed. Averaged model of a three-level neutral-point clamped (NPC) multilevel inverter (MLI) using switching-cycle averaging is presented in [106], which is valid up to half the switching frequency. In [107], two stage inverter is modeled by splitting the inverter in to two buck converters and then dc-to-dc averaged modeling approach is applied for the averaged circuit model. In [108], generalized average models for PWM inverters are proposed based on a quasi-Fourier series representation of the switching functions that includes fundamental and switching frequency components as well as sideband components of the switching frequency. These generalized average models are suitable for simulation applications in which both fundamental and switching behavior have to be predicted accurately with fast run times. These models run faster than the detailed model and slower than

the state-space averaged model in simulation.

In this chapter, dynamic average circuit model with capacitor voltage balancing has been developed for ANPCI without non-idealities using step-by-step procedure. Further, the model is developed by considering non-idealities also. Unlike AAVM and PAVM, the model do not have complex mathematical equations. Also, the model can be directly simulated using any standard circuit simulation software. The model is also modular in nature and valid for all the operating conditions of the converter. The model significantly reduces the computational resources and execution times while analyzing or designing power electronic systems involving ANPCI. To demonstrate the strength of the DACM, the SRF-dq based closed-loop controller is also implemented for a stand-alone PV system using ANPCI. Extensive experimental and simulation results are presented to validate the DACM of the ANPCI. The results presented demonstrate the advantages and strength of the DACM developed for ANPCI.

3.3 AVERAGE MODEL OF ANPCI

The switching circuit diagram of the single-phase five-level ANPCI is shown in Fig. 3.1. The average circuit model of ANPCI is obtained such that the average capacitor voltages and inductor current of the converter during steady-state and transients are accurately predicted with less computational time and resources. To achieve this, the switch network of ANPCI is replaced with a network of dependent voltage and current sources,

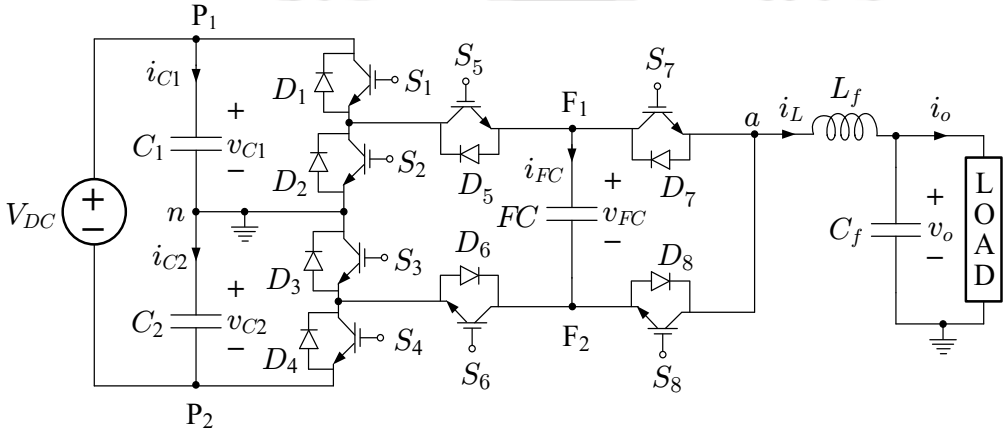


Fig. 3.1. Circuit diagram of single-phase five-level ANPCI.

whose control variables are chosen such that the following conditions are satisfied: (1) The voltage v_{an} of the average circuit model is equal to the fundamental component of PWM voltage expressed as a function of m_a, v_{C1}, v_{C2} and v_{FC}, (2) The average capacitor currents are obtained as a function of m_a and i_L, (3) Instantaneous power balance is maintained in the average circuit, (4) The capacitor voltages are maintained with in the acceptable tolerance range around their respective nominal values.

To develop the average model of ANPCI as mentioned above, one fundamental cycle of m_a is divided into four different regions as shown in Fig. 3.2. Then, the average circuit model in each of these four regions and the control variables of dependent sources are determined. As the switching states used by the ANPCI are different in each of these four regions, the average circuit model has to be obtained separately for each region. However, it is important to note that the averaging in each region is actually performed over one switching (or PWM) cycle only. Once the average circuit models are developed in each of the four regions, all these individual circuits are carefully combined to obtain the average circuit model which is valid for entire fundamental cycle. The detailed description of these steps is given below.

Region 1: $0.5 < m_a < 1$**:** In this region, the PWM voltage, v_{an} of switching circuit can be either v_{C1} or $(v_{C1} - v_{FC})$ or v_{FC}. Thus, the average value of v_{an} is a function of v_{C1},

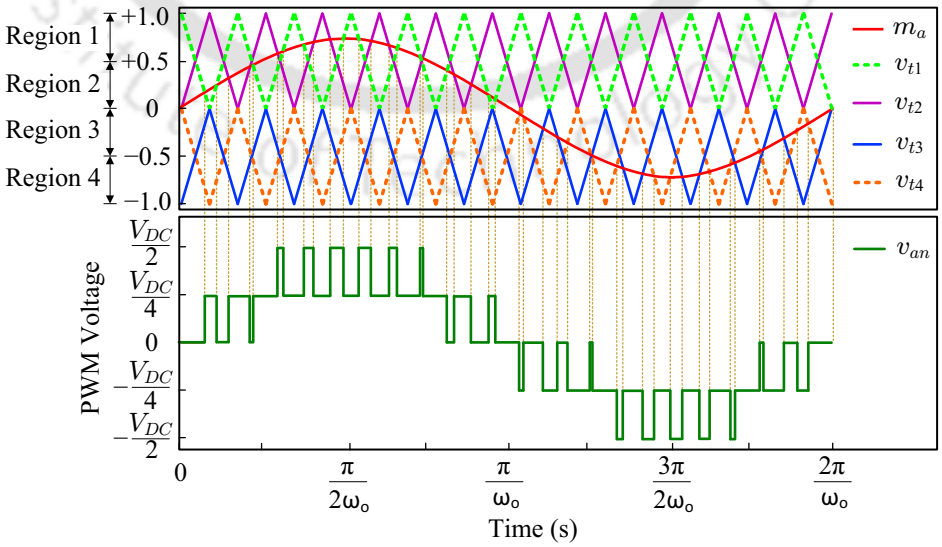


Fig. 3.2. Generation of PWM voltage (v_{an}) using PDS-PWM technique by comparison of modulation (m_a) and carrier signals (v_{t1}, v_{t2}, v_{t3} and v_{t4}).

v_{FC} and m_a. However, for simplification in the average circuit model, it is assumed that the v_{FC} is constant in this region and C_1 is responsible for supplying power to the load due to the following reasons: (1) In this region, average value of v_{an} is always greater than $+\frac{V_{DC}}{4}$ and hence most of the time, the voltage level v_{C1} has to be applied, (2) The tolerance level of v_{FC} is much smaller compared to that of v_{C1}, (3) Even if there is an energy exchange between FC and output terminals, the energy supplied by FC obtains from C_1 and C_2 only. With this approximation, the average model of ANPCI in 'Region 1' can be obtained as shown in Fig. 3.3(a). The control variable, v_{aD} for the dependent voltage source in Fig. 3.3(a) is given by:

$$\begin{aligned} v_{aD} &= m_a \overline{v}_{C1} \quad \text{for} \quad 0.5 < m_a < 1 \\ \text{or} \quad v_{aD} &= d_P \overline{v}_{C1} \end{aligned} \tag{3.1}$$

where d_P is a multiplying factor defined such that,

$$d_P = \begin{cases} m_a & \text{if} \quad 0.5 < m_a < 1, \\ 0 & \text{otherwise} \end{cases}$$

The expression for d_P and other multiplying factors used in the average modeling are given in Table 3.1. Similarly, i_{D1} and i_{D5} are given by,

$$i_{D1} = i_{D5} = d_P \bar{i}_L \tag{3.2}$$

Region 2: $0 < m_a < 0.5$**:** In this region, the voltage v_{an} of switching circuit can be either $(v_{C1} - v_{FC})$ or v_{FC} or 0. Thus, the average value of v_{an} is a function of v_{C1}, v_{FC} and m_a. Unlike 'Region 1', here FC is connected to the output terminals for most of the time, hence v_{FC} cannot be considered as constant. In the switching circuit, the choice between the states $(v_{C1} - v_{FC})$ and v_{FC} is made based on the capacitor voltage balancing strategy.

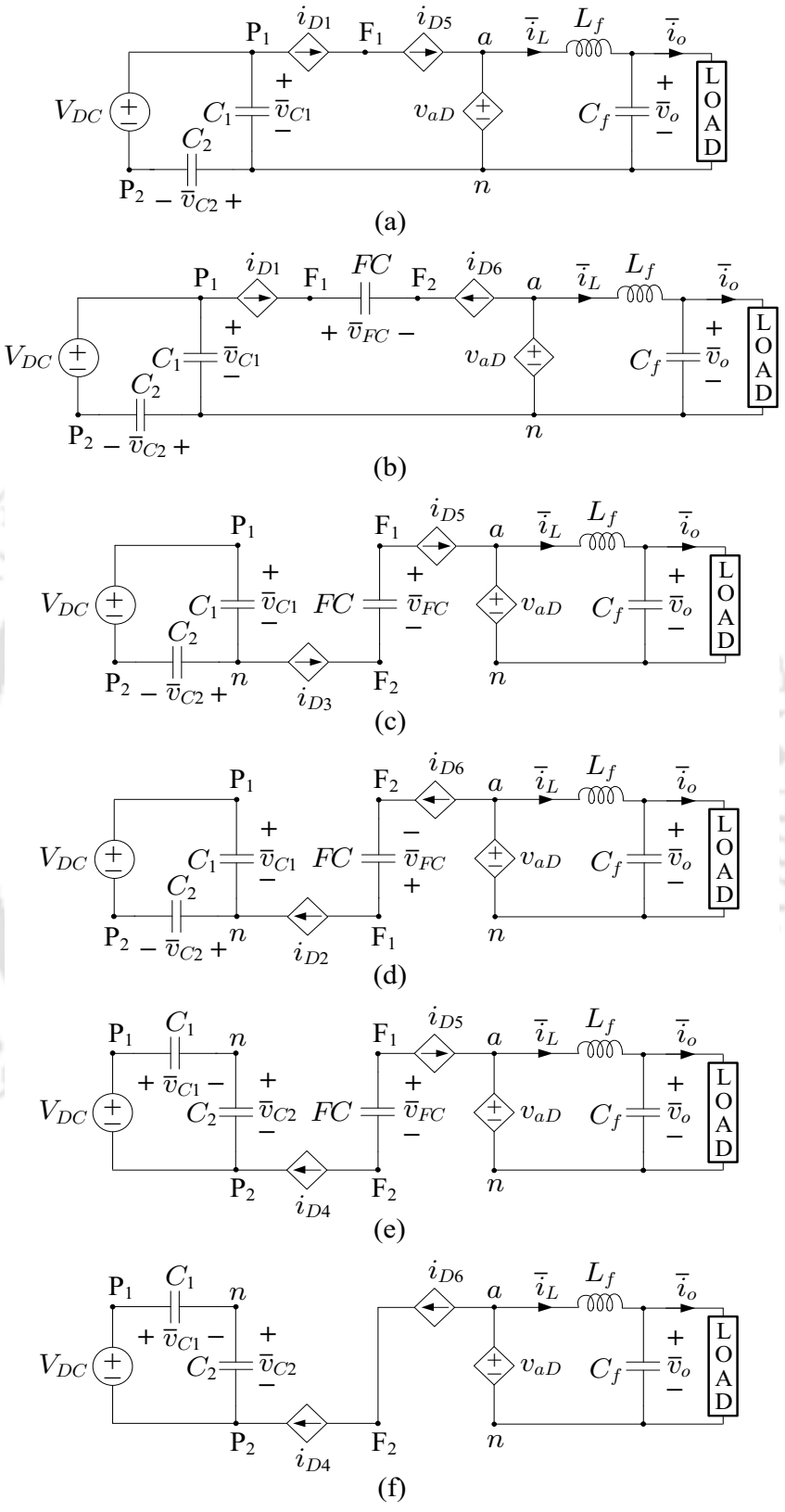


Fig. 3.3. Average models of ANPCI in (a) Region 1, (b) Region 2 for Modes M1 and M4, (c) Region 2 for Modes M2 and M3, (d) Region 3 for Modes M1 and M3, (e) Region 3 for Modes M2 and M4, and (f) Region 4.

Table 3.1. MULTIPLYING FACTORS USED IN THE AVERAGE MODEL OF ANPCI

Variable	Expression	Variable	Expression
d_P	$(1/2)\,(1+\text{sgn}(m_a-0.5))\,m_a$	α_1	$\gamma_1\gamma_9$
d_{PH}	$[1+(\text{sgn}(m_a)\ \text{sgn}(0.5-m_a))]\,m_a$	α_2	$\gamma_2\gamma_9$
d_{NH}	$[(\text{sgn}(m_a)\ \text{sgn}(0.5+m_a))-1]\,m_a$	α_3	$\gamma_2\gamma_{10}$
d_N	$(1/2)\,(\text{sgn}(m_a+0.5)-1)\,m_a$	α_4	$\gamma_1\gamma_{10}$
γ_1	$(1/2)\,(1+\text{sgn}(v^*_{FC}-\epsilon-\overline{v}_{FC}))$	α_5	$\gamma_3\gamma_4\gamma_6\gamma_9$
γ_2	$(1/2)\,(1-\text{sgn}(v^*_{FC}+\epsilon-\overline{v}_{FC}))$	α_6	$\gamma_3\gamma_4\gamma_6\gamma_{10}$
γ_3	$(1/2)\,(1+\text{sgn}(v^*_{FC}+\epsilon-\overline{v}_{FC}))$	α_7	$\gamma_3\gamma_4\gamma_5\gamma_9$
γ_4	$(1/2)\,(1-\text{sgn}(v^*_{FC}-\epsilon-\overline{v}_{FC}))$	α_8	$\gamma_3\gamma_4\gamma_5\gamma_{10}$
γ_5	$(1/2)\,(1+\text{sgn}(v^*_{C1}-\epsilon-\overline{v}_{C1}))$	α_9	$\gamma_3\gamma_4\gamma_7\gamma_8$
γ_6	$(1/2)\,(1-\text{sgn}(v^*_{C1}+\epsilon-\overline{v}_{C1}))$		
γ_7	$(1/2)\,(1+\text{sgn}(v^*_{C1}+\epsilon-\overline{v}_{C1}))$	β_1	$\sum_{i=1,3,5,8}\alpha_i$
γ_8	$(1/2)\,(1-\text{sgn}(v^*_{C1}-\epsilon-\overline{v}_{C1}))$	β_2	$\sum_{i=2,4,5,8}\alpha_i$
γ_9	$(1/2)\,(1+\text{sgn}(\overline{i}_L))$	β_3	$\sum_{i=1,3,6,7,9}\alpha_i$
γ_{10}	$(1/2)\,(1-\text{sgn}(\overline{i}_L))$	β_4	$\sum_{i=2,4,6,7,9}\alpha_i$

Hence there are two possible average circuit models as shown in Fig. 3.3(b) and (c). The choice between these two circuits is made based on the sign of $\overline{i}_L$ and deviation of $\overline{v}_{C1}$, $\overline{v}_{FC}$ from their respective nominal values. The average circuit of ANPCI becomes Fig. 3.3(b), if v_{an} depends on both v_{C1} and v_{FC}, e.g., when $i_L > 0$ and FC has to be charged. The control variables of sources in Fig. 3.3(b) can be written as,

$$\begin{aligned} v_{aD} &= (\alpha_1+\alpha_3+\alpha_5+\alpha_8)\,d_{PH}\,(\overline{v}_{C1}-\overline{v}_{FC}) \\ &= \beta_1 d_{PH}\,(\overline{v}_{C1}-\overline{v}_{FC}) \end{aligned} \tag{3.3}$$

$$i_{D1} = -i_{D6} = \beta_1 d_{PH}\overline{i}_L \tag{3.4}$$

where α_i $(i=1,2,...,9)$ and β_j $(j=1,2,3,4)$ are the multiplying factors defined in Table 3.1. Similarly, the average circuit of ANPCI becomes Fig. 3.3(c), if v_{an} depends only on v_{FC}, e.g., when $i_L < 0$ and FC has to be charged. The control variables of sources in Fig. 3.3(c)

can be written as

$$v_{aD} = \beta_4 d_{PH} \overline{v}_{FC} \tag{3.5}$$

$$i_{D3} = i_{D5} = \beta_4 d_{PH} \bar{i}_L \tag{3.6}$$

Region 3: $-0.5 < m_a < 0$**:** In this region, the voltage v_{an} of switching circuit can be either $-v_{FC}$ or $(v_{FC} - v_{C2})$ or 0. Thus, the average v_{an} is a function of v_{C2}, v_{FC} and m_a. Similar to 'Region 2', here FC is connected to the output terminals for most of the time. In the switching circuit, the choice between the states $-v_{FC}$ and $(v_{FC} - v_{C2})$ is made based on the capacitor voltage balancing strategy. Hence there are two possible average circuit models as shown in Fig. 3.3(d) and (e). The choice between these two circuits is made based on the sign of $\bar{i}_L$ and deviation of $\bar{v}_{C2}$, $\bar{v}_{FC}$ from their respective nominal values. The average circuit of ANPCI becomes Fig. 3.3(d), if v_{an} depends only on v_{FC}, e.g., when $i_L > 0$ and FC has to be charged. The control variables of sources in Fig. 3.3(d) can be written as

$$v_{aD} = -\beta_3 d_{NH} \overline{v}_{FC} \tag{3.7}$$

$$i_{D2} = i_{D6} = -\beta_3 d_{NH} \bar{i}_L \tag{3.8}$$

Similarly, the average circuit of ANPCI becomes Fig. 3.3(e), if v_{an} depends on both v_{C2} and v_{FC}, e.g., when $i_L < 0$ and FC has to be charged. The control variables of sources in Fig. 3.3(e) can be written as

$$v_{aD} = \beta_2 d_{NH} \left(\overline{v}_{FC} - \overline{v}_{C2}\right) \tag{3.9}$$

$$i_{D4} = -i_{D5} = -\beta_2 d_{NH} \bar{i}_L \tag{3.10}$$

Region 4: $-1 < m_a < -0.5$**:** In this region, the voltage v_{an} of switching circuit can be either $-v_{C2}$ or $(v_{FC} - v_{C2})$ or $-v_{FC}$. Thus, the average v_{an} is a function of v_{C2}, v_{FC} and m_a. However, similar to 'Region 1', for simplification in the average circuit model, it is assumed that the v_{FC} is constant in this region and only C_2 is responsible for supplying

power to the load. With this approximation, the average model of ANPCI in this region can be obtained as shown in Fig. 3.3(f). The control variables for the dependent sources in Fig. 3.3(f) are given by:

$$v_{aD} = -d_N \overline{v}_{C2} \tag{3.11}$$

$$i_{D4} = i_{D6} = -d_N \bar{i}_L \tag{3.12}$$

By carefully combining the circuits given in Figs. 3.3(a)−3.3(f) and equations (3.1)−(3.12), the final DACM of ANPCI is obtained as shown in Fig. 3.4. The control variables of dependent sources in Fig. 3.4 are given by:

$$\begin{aligned} v_{aD} &= d_P \overline{v}_{C1} - d_N \overline{v}_{C2} + \beta_1 d_{PH}(\overline{v}_{C1} - \overline{v}_{FC}) \\ &\quad + \beta_2 d_{NH}(\overline{v}_{FC} - \overline{v}_{C2}) - (\beta_3 d_{NH} - \beta_4 d_{PH})\overline{v}_{FC} \\ &= \left(\frac{V_{DC}}{2}\right) m_a \end{aligned} \tag{3.13}$$

$$i_{D1} = (d_P + \beta_1 d_{PH})\bar{i}_L \tag{3.14}$$

$$i_{D2} = -\beta_3 d_{NH} \bar{i}_L \tag{3.15}$$

$$i_{D3} = \beta_4 d_{PH} \bar{i}_L \tag{3.16}$$

$$i_{D4} = -(d_N + \beta_2 d_{NH})\bar{i}_L \tag{3.17}$$

$$i_{D5} = (d_P + \beta_2 d_{NH} + \beta_4 d_{PH})\bar{i}_L \tag{3.18}$$

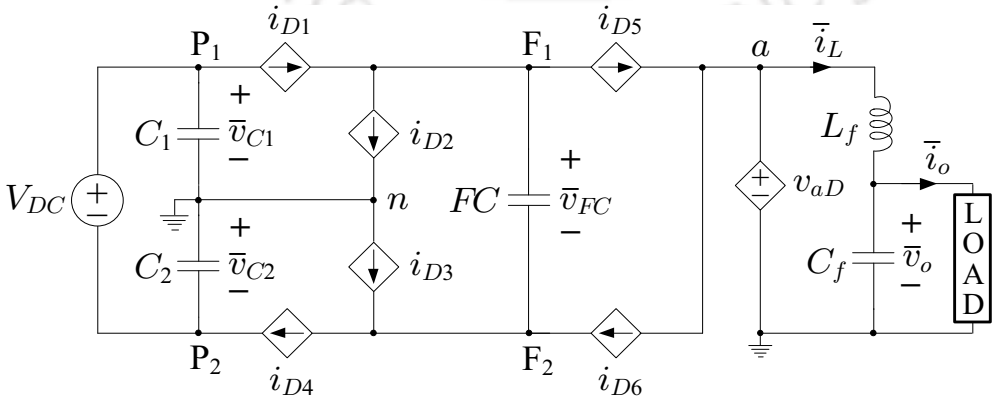


Fig. 3.4. Combined dynamic average circuit model of the ANPCI.

$$i_{D6} = -\left(d_N + \beta_1 d_{PH} + \beta_3 d_{NH}\right)\bar{i}_L \tag{3.19}$$

3.4 INCLUSION OF NON-IDEALITIES IN THE DYNAMIC AVERAGE CIRCUIT MODEL

Fig. 3.5 shows the circuit diagram of ANPCI considering non-idealities such as: (i) ON-state resistance of each switch, r_S; (ii) Equivalent series resistance (ESR) of each DC-link capacitor, r_C; (iii) ESR of the FC, r_{FC}; (iv) ESR of the filter capacitor, r_{Cf}; and (v) ESR of the filter inductor, r_L.

Table 3.2 lists various switches in the ON-state and conducting switches carrying the current i_L for each state of the ANPCI. From Table 3.2, it can be seen that only four switches are turned ON in each switching state, out of which only three switches are conducting at any time. Also these three switches will be connected in series with the filter inductor L_f and hence all of them carry the current i_L. For instance, in State I, the switches S_1, S_3, S_5 and S_7 are turned ON, however the conducting switches are only S_1, S_5 and S_7. The switch S_3 do not conduct in this state and it is turned ON only to balance the voltage

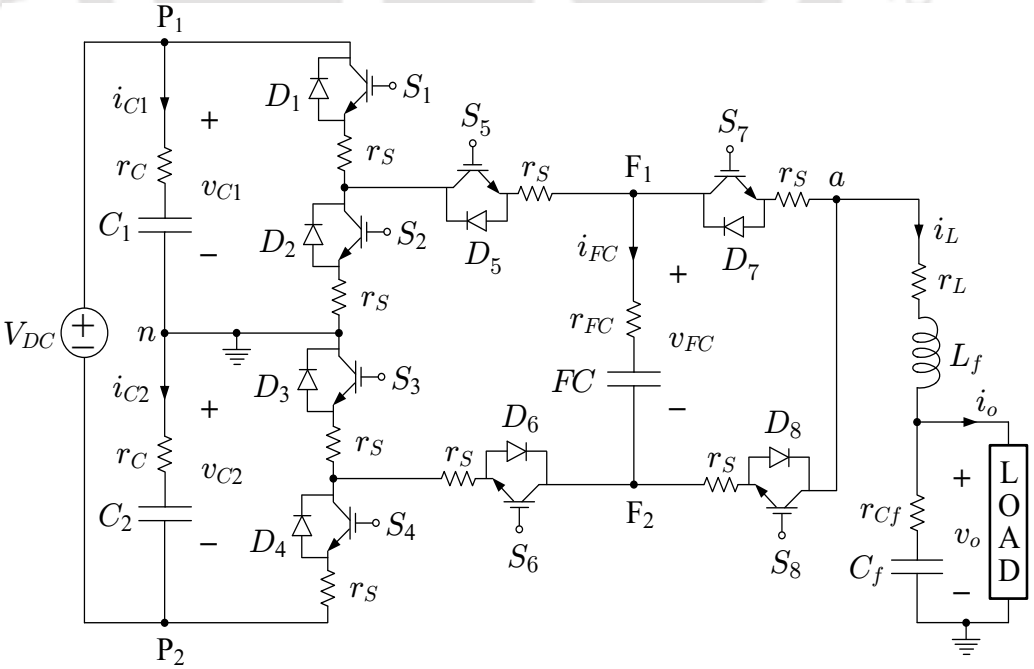


Fig. 3.5. SCM of the ANPCI with non-idealities: switch ON-state resistance (r_S) shown separately for each switch.

Table 3.2. SWITCHES IN THE ON-STATE AND SWITCHES IN THE CONDUCTION MODE CARRYING THE INDUCTOR CURRENT, (i_L) FOR EACH SWITCHING STATE OF THE ANPCI OF FIG. 2.1

State	Switches in ON-state	Switches in the conduction mode carrying the inductor current, (i_L)$^\sharp$
I	S_1, S_3, S_5, S_7	S_1, S_5, S_7
II	S_1, S_3, S_5, S_8	S_1, S_5, S_8
III	S_1, S_3, S_6, S_7	S_3, S_6, S_7
IV	S_1, S_3, S_6, S_8	S_3, S_6, S_8
V	S_2, S_4, S_5, S_7	S_2, S_5, S_7
VI	S_2, S_4, S_5, S_8	S_2, S_5, S_8
VII	S_2, S_4, S_6, S_7	S_4, S_6, S_7
VIII	S_2, S_4, S_6, S_8	S_4, S_6, S_8

$^\sharp$ when a switch is said to be in conducting mode, the conducting device can be either the IGBT or its anti-parallel diode, depending on the polarity of i_L.

stress among the switches. Note that when a switch is said to be in conducting mode, the conducting device can be either the IGBT or its anti-parallel diode, depending on the polarity of i_L.

Therefore, the combined effect of the switch ON-state resistance on the ANPCI output voltage can be represented as a single resistance, $3{\cdot}r_S$, connected in series with the filter inductor L_f, as shown in Fig. 3.6. Fig. 3.7 shows the DACM of ANPCI considering the non-idealities listed above. Note that, as the position of all the passive components is not changed in the average circuit model, there is no need to re-derive the equations for the dependent sources in the average model. This is the main advantage of the DACM presented in this thesis.

3.5 N-LEVEL MODEL OF SINGLE-PHASE ANPCI

The circuit diagram of ANPCI is modular, i.e., for increment of every two levels of PWM voltage, two switches and one flying capacitor have to be integrated to the five-level ANPCI shown in Fig. 3.1 [21]. Fig. 3.8 shows the circuit diagram of N-level ANPCI, where $N \geq 5$ is an odd integer. It can be observed that for N-level output voltage waveform, the required number of switches and flying capacitors are $(N+3)$ and $\left(\frac{N-3}{2}\right)$, respectively.

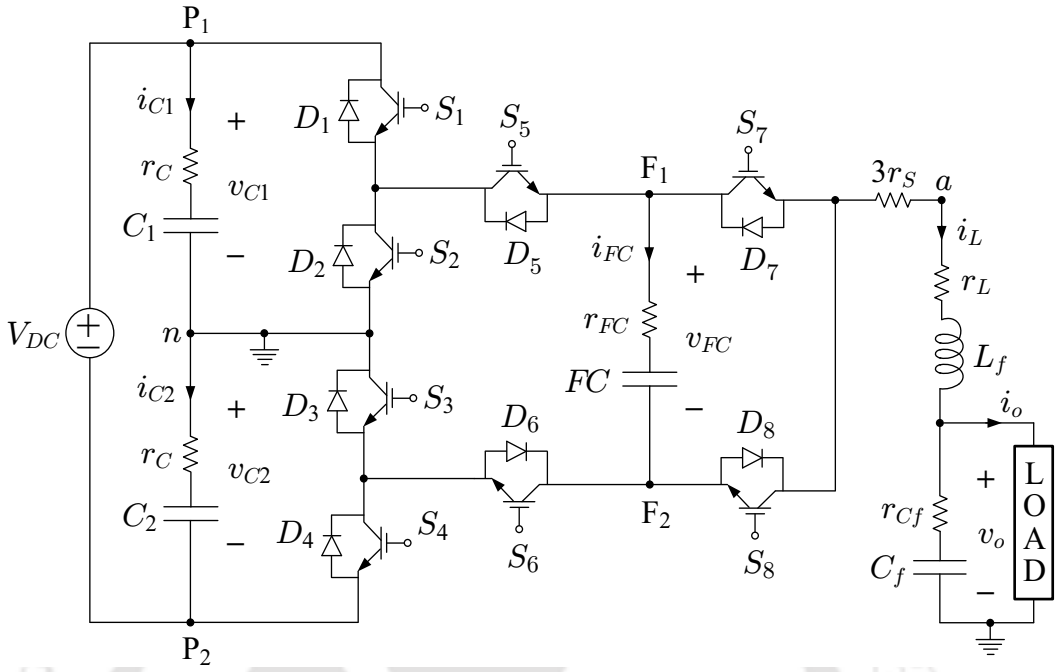


Fig. 3.6. SCM of the ANPCI with non-idealities: ON-state resistance of three conducting switches is combined and placed in series ($3{\cdot}r_S$) with the filter inductor L_f.

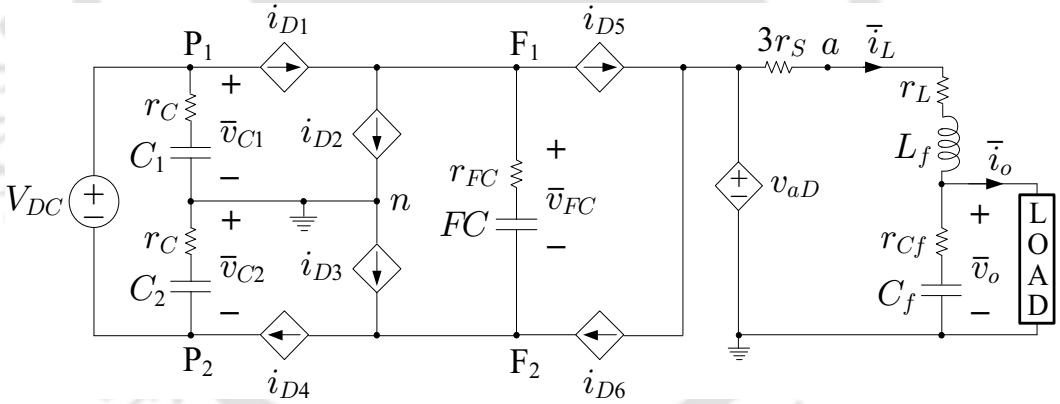


Fig. 3.7. DACM of the ANPCI with non-idealities, i.e., for the SCM shown in Fig. 3.6.

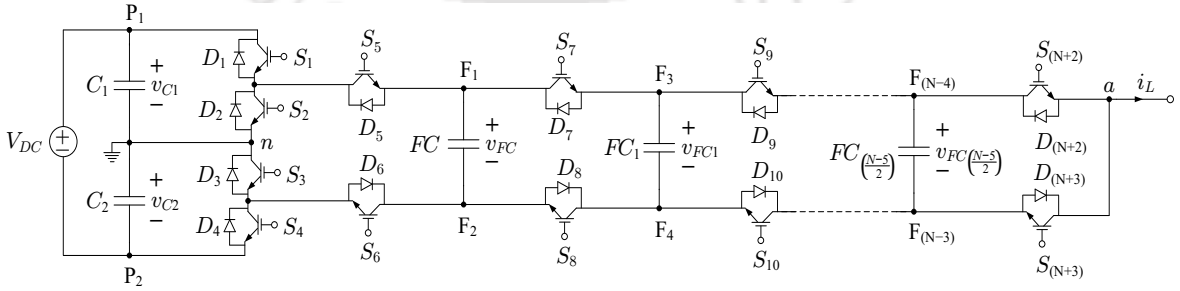


Fig. 3.8. Circuit diagram of single-phase N-level ANPCI.

The averaged modeling concept presented in this thesis can also be extended for the N-level ANPCI by adding two dependent current sources and one flying capacitor to

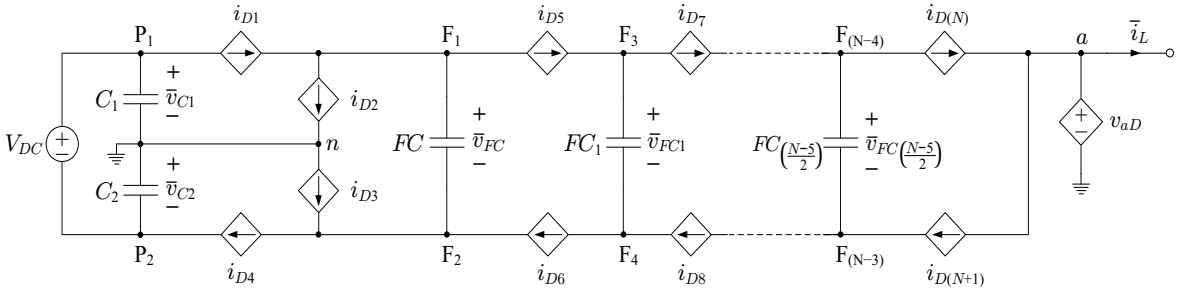


Fig. 3.9. Dynamic average circuit model of the single-phase N-level ANPCI.

the circuit of Fig. 3.4 for increment of every two output voltage levels. The average circuit model obtained for an N-level ANPCI is shown in Fig. 3.9. The number of dependent current sources required in the average circuit model of N-level ANPCI is $(N+1)$. However, only one dependent voltage source is required irrespective of the number of output voltage levels.

3.6 RESULTS AND DISCUSSION

Results to validate the average circuit model are also presented in this section. The results for strength demonstration of the average circuit model are given in Section 3.7. Note that all the simulation results presented in Sections 3.6 and 3.7 are obtained using PSCAD/EMTDC software on a desktop computer with Intel® Core™ i5-3470 CPU @ 3.2 GHz processor, 8 GB RAM and Windows 10 64-bit operating system.

3.6.1 Validation of the Dynamic Average Circuit Model

To validate the DACM of the ANPCI developed in this thesis, the waveforms obtained from DACM simulation are compared with the switching circuit model (SCM) simulation waveforms and the experimental waveforms for various test cases. These simulations also consider the non-idealities present in the switches and passive components used in hardware prototype. However, the EMI and the dead band effects are ignored. The time instants of step changes given in the simulation waveforms of the SCM and DACM are the same as given in the experimental waveforms for each test case. The simulation time-step (T_{st}) considered is 1 μs and the simulation plot step (T_p) is 40 μs for the SCM. In Figs. 3.10 and 3.11, $Avg40$ and $Avg160$ represent the DACM waveforms obtained with the simulation time-steps of 40 μs and 160 μs, respectively. The parameters considered for experimental

and simulation results are given in Table 3.3.

Fig. 3.10 shows the comparison of open-loop waveforms obtained from simulation of DACM and SCM, and experiment. The steady-state waveforms of v_{C1}, v_{FC}, v_o and i_o are shown in Fig. 3.10(a). The modulation index step change is given from 0.9 to 0.4 at $t = 50.92$ ms with the constant load resistance of 5 Ω and the corresponding waveforms are shown in Fig. 3.10(b). In Fig. 3.10(c), the load resistance is suddenly increased from 5 Ω

Table 3.3. SIMULATION AND EXPERIMENTAL PARAMETERS

Parameters	Attributes
C_1 and C_2	3.3 mF
FC	2 mF
L_f	2 mH
C_f	20 μF
Fundamental frequency $\left(f_o = \frac{\omega_o}{2\pi}\right)$	50 Hz
Switching frequency (f_{s1})	10 kHz
V_{DC}	128 V
Output power	300 W

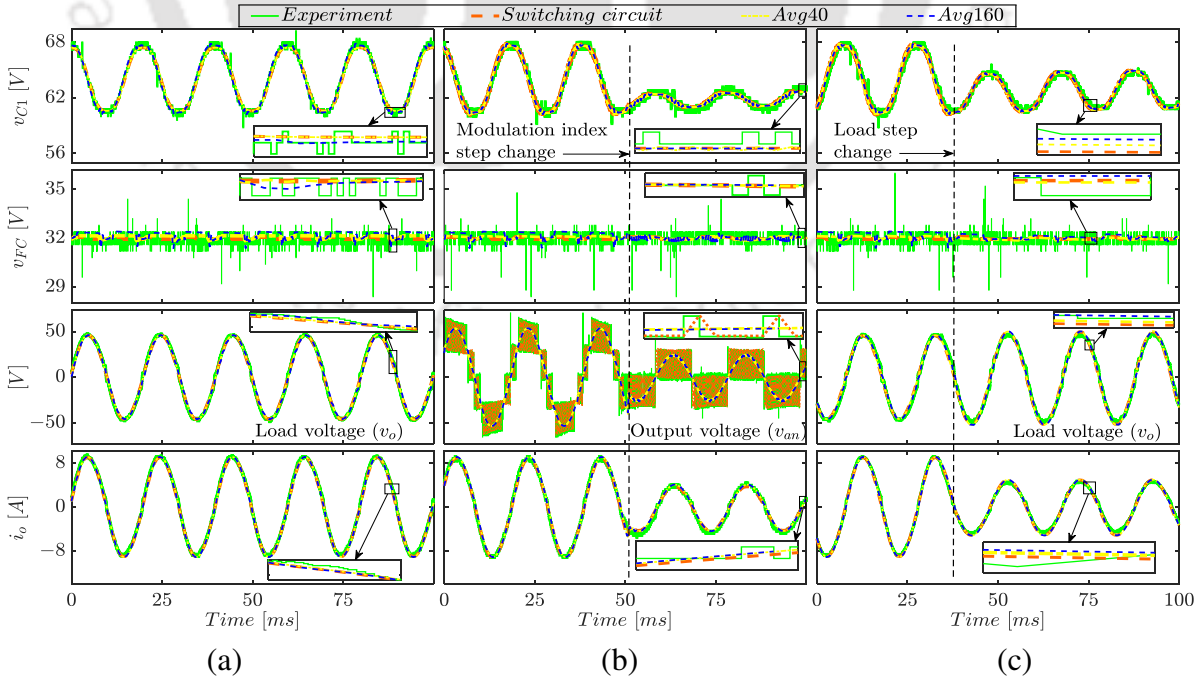


Fig. 3.10. Comparison of waveforms obtained from simulation of DACM, simulation of SCM and experimental prototype of ANPCI in open-loop for (a) steady-state (b) step-down change in modulation index (M), and (c) step-down change in load.

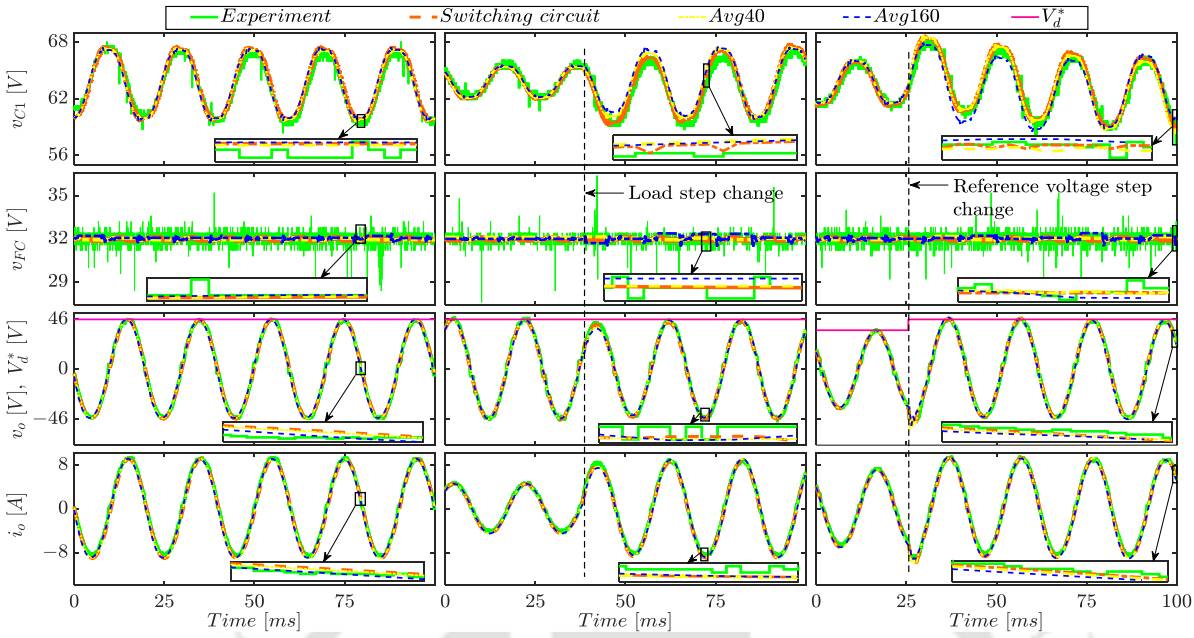


Fig. 3.11. Comparison of waveforms obtained from simulation of DACM, simulation of SCM and experimental prototype of ANPCI in closed-loop for (a) steady-state (b) step-up change in load, and (c) step-up change in reference load voltage (V_d^*).

to 10 Ω at $t = 37.6$ ms. Fig. 3.11 shows the comparison of closed-loop waveforms obtained from simulation of DACM and SCM, and experiment. Fig. 3.11(a) shows the steady-state waveforms for the reference peak load voltage (V_d^*) of 46 V and 5 Ω load. Figs. 3.11(b) and 3.11(c) show the waveforms with step change in load resistance given at $t = 38.01$ ms and step change in the reference load voltage given at $t = 25.55$ ms, respectively. From Figs. 3.10 and 3.11, it is confirmed that the average circuit model accurately predicts the waveforms of ANPCI in both steady-state and transient conditions. Note that the average model requires very less computational time compared to the switching circuit simulation. The results to support this are presented in Section 3.7.

In addition to comparison of waveforms, the effectiveness of DACM is also validated using Root Mean Square Error (RMSE) for various test cases listed in Table 3.4. The RMS errors for all these test cases with three different simulation time-steps (T_{st}), viz., 40 μs, 80 μs and 160 μs are listed in Table 3.5. It can be seen that the RMS errors for all the test cases considered are in acceptable range for both simulation and experiment. Note that, in all the results presented in this thesis, the units of RMS errors are same as the units of the

signals under consideration.

Table 3.4. PARAMETERS FOR VALIDATION OF AVERAGE MODEL CONSIDERING VARIOUS CASES

Variables	Open-loop cases			Variables	Closed-loop cases			
	C-1	C-2	C-3		C-4	C-5	C-6	C-7
M	0.9	0.4	0.9	V_d^*	46 V	46 V	46 V	36 V
R_L	5 Ω	5 Ω	10 Ω	R_L	5 Ω	8.4 Ω	10 Ω	5 Ω

Table 3.5. RMS ERRORS FOR THE CASES LISTED IN TABLE 3.4 WITH DIFFERENT SIMULATION TIME-STEPS OF THE AVERAGE MODEL (DACM)

Case	T_{st}	RMS errors							
		DACM Simulation and SCM Simulation				DACM Simulation and Experiment			
		v_{C1}	v_{FC}	v_o	i_o	v_{C1}	v_{FC}	v_o	i_o
C-1	40 μs	0.28	0.10	0.49	0.09	0.38	0.35	2.41	0.36
	80 μs	0.27	0.07	0.53	0.1	0.38	0.34	2.36	0.36
	160 μs	0.31	0.32	1.49	0.26	0.38	0.46	2.82	0.36
C-2	40 μs	0.17	0.03	—	0.22	0.34	0.25	—	0.37
	80 μs	0.17	0.06	—	0.26	0.33	0.25	—	0.4
	160 μs	0.17	0.11	—	0.24	0.33	0.26	—	0.36
C-3	40 μs	0.15	0.03	0.53	0.05	0.33	0.27	2.71	0.4
	80 μs	0.15	0.04	0.54	0.05	0.33	0.29	2.75	0.4
	160 μs	0.2	0.15	2.35	0.23	0.27	0.36	2.47	0.41
C-4	40 μs	0.26	0.07	0.53	0.1	0.56	0.47	1.74	0.52
	80 μs	0.28	0.08	1.1	0.14	0.61	0.48	1.99	0.55
	160 μs	0.28	0.16	2.18	0.35	0.61	0.46	2.7	0.61
C-5	40 μs	0.17	0.07	0.59	0.06	0.35	0.37	2.59	0.27
	80 μs	0.22	0.08	0.68	0.08	0.37	0.4	2.52	0.26
	160 μs	0.19	0.17	1.69	0.2	0.36	0.44	1.92	0.19
C-6	40 μs	0.16	0.11	0.68	0.06	0.34	0.37	1.91	0.27
	80 μs	0.18	0.08	0.78	0.06	0.33	0.41	1.94	0.27
	160 μs	0.21	0.06	1.08	0.09	0.28	0.51	1.94	0.29
C-7	40 μs	0.29	0.05	0.43	0.08	0.43	0.42	1.55	0.36
	80 μs	0.27	0.08	0.52	0.05	0.44	0.37	1.61	0.37
	160 μs	0.31	0.12	0.74	0.09	0.44	0.38	1.76	0.39

3.7 STRENGTH DEMONSTRATION OF THE DYNAMIC AVERAGE CIRCUIT MODEL

To demonstrate the strength of the dynamic average circuit model of the ANPCI and to compare the computational time required for switching circuit based simulation and average model based simulation, SRF-dq controlled ANPCI based stand-alone PV system is considered as shown in Fig. 3.12. The PV array in Fig. 3.12 consists of four series connected KC200GT PV panels, each with open circuit voltage, V_{OC} = 32.9 V and short circuit current, I_{SC} = 8.21 A [109]. In Fig. 3.12, C_{PV} is 6 mF and the parameters of the ANPCI are same as given in Table 3.3. However, the V_{DC} $(= V_{PV})$ will depend on the connected load and the operating point on the PV curve. The characteristics of the combined PV array are shown in Fig. 3.13 for various irradiation (G) and temperature (T) conditions. Also, Table 3.6 gives the maximum power point and V_{OC} values of these curves.

To simulate the system shown in Fig. 3.12, the PV array model given in [109] is utilized. The load voltage in Fig. 3.12 is maintained to be constant in all the operating conditions, whereas the terminal voltage of the PV array, V_{PV}, depends on the operating point. The proposed test system is run for 100 s with step changes in solar irradiation, temperature and the load. Fig. 3.14 shows the comparison of waveforms obtained from switching circuit based simulation and average model based simulation. In this figure, $Avg40$ and $Avg160$ represent the DACM waveforms obtained with the simulation time-steps of

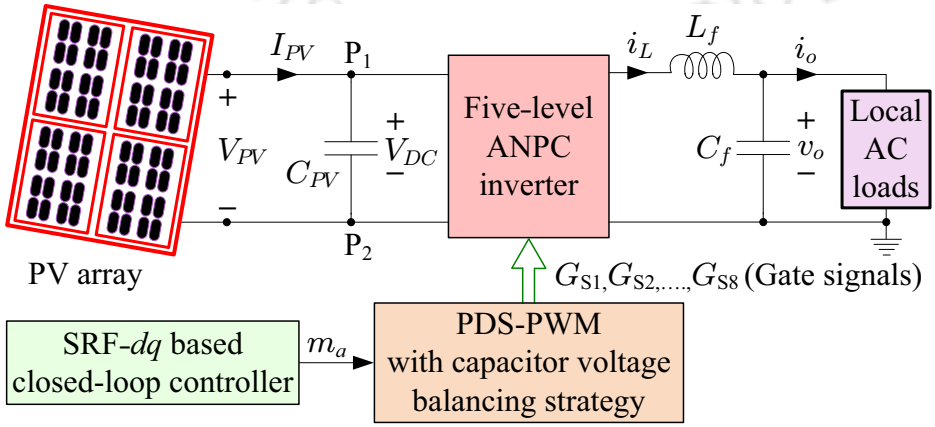


Fig. 3.12. Block diagram of ANPCI based stand-alone PV system.

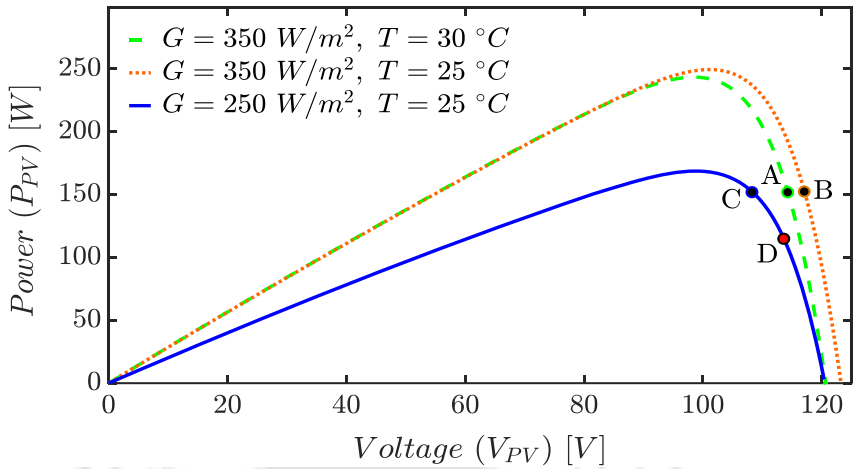


Fig. 3.13. Power vs. voltage characteristics of the PV array.

40 μs and 160 μs, respectively. Fig. 3.14(a) shows results with the initial parameters, $G =$ 350 $\frac{\text{W}}{\text{m}^2}$, $T = 30$ °C, $V_d^* = 46$ V, $Z_L = (5{+}j3.14)\ \Omega$, so that the system operates at point 'A' on the PV curve shown in Fig. 3.13. At $t = 20$ s, the temperature is changed to 25 °C and the operating point has changed to 'B'. Later, in Fig. 3.14(b), a step change is given in the irradiation at $t = 40$ s, from 350 $\frac{\text{W}}{\text{m}^2}$ to 250 $\frac{\text{W}}{\text{m}^2}$, due to which the operating point becomes 'C'. Fig. 3.14(c) shows the results with step change in the ac load (Z_L) from $(5{+}j3.14)\ \Omega$ to $(8{+}j3.14)\ \Omega$ at $t = 80$ s and the system operates at point 'D' on the PV curve. Table 3.7 lists the steady-state operating points of the ANPCI based PV system obtained from SCM and DACM for various time-steps. From the results of Fig. 3.14 and Table 3.7, it can be observed that waveforms obtained from average model based simulation are closely following the waveforms obtained from switching circuit based simulation during both steady-state and transients. Table 3.8 gives the RMS errors of the average circuit model with respect to the switching circuit model for various system parameters and simulation time-steps. It can be

Table 3.6. V_{OC} AND MAXIMUM POWER POINT (MPP) OF THE PV-CURVES SHOWN IN FIG. 3.13

Parameters	V_{OC}	Maximum power point	
		V_{MPP}	P_{MPP}
$G = 350\ \frac{\text{W}}{\text{m}^2}$ and $T = 30$ °C	120.66 V	98.53 V	243.51 W
$G = 350\ \frac{\text{W}}{\text{m}^2}$ and $T = 25$ °C	123.24 V	101.13 V	249.54 W
$G = 250\ \frac{\text{W}}{\text{m}^2}$ and $T = 25$ °C	120.38 V	98.88 V	168.70 W

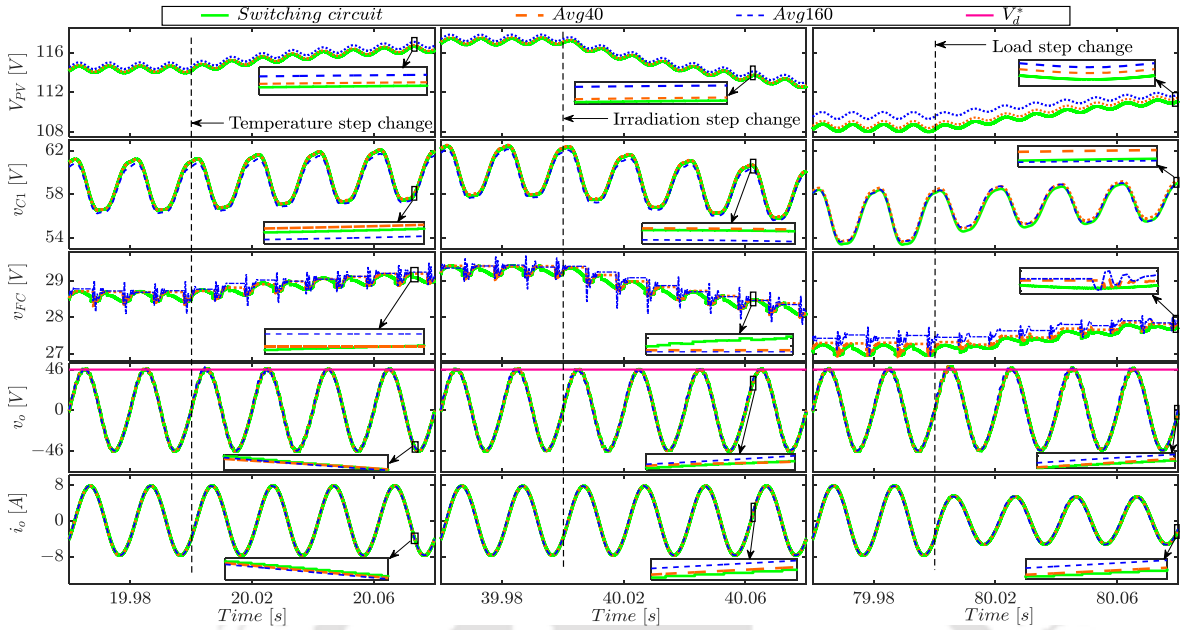


Fig. 3.14. Comparison of waveforms obtained from DACM and SCM simulations of ANPCI integrated PV array in closed-loop for step-down change in (a) temperature (b) irradiation, and (c) load.

Table 3.7. STEADY-STATE OPERATING POINTS ON PV CURVES FOR CLOSED-LOOP OPERATION OF ANPCI BASED PV SYSTEM

Point	SCM	DACM		
	$T_{st} = 1\ \mu$s	$T_{st} = 40\ \mu$s	$T_{st} = 80\ \mu$s	$T_{st} = 160\ \mu$s
A	(114.3,151.75)	(114.35,150.3)	(114.45,148.75)	(114.7,145.7)
B	(117.1,152.3)	(117.2,150.3)	(117.32,148.7)	(117.5,145.7)
C	(108.3,151.8)	(108.75,150.3)	(109.1,148.7)	(109.65,145.7)
D	(113.65,114.7)	(113.75,113.9)	(113.77,113.3)	(113.9,111.85)

observed that the RMS errors for the PV system simulation are also in acceptable range.

Further, note that the execution time required for simulating the ANPCI based PV system will significantly reduce if DACM of the ANPCI is used for simulation. This is because the DACM based simulations can use larger simulation time-steps (T_{st}) compared to those used for SCM based simulations. To verify this, the execution times (T_e) required to simulate the PV system of Fig. 3.12 for 100 s runtime are compared in Table 3.9 for six different cases: Case-I to Case-VI. In each case, different values of simulation time-step (T_{st}), plot step (T_p) are considered for SCM and DACM, as listed in Table 3.9. The simulation is run for a duration of 100 s while keeping all other system parameters same

Table 3.8. RMS ERRORS FOR SIMULATION OF ANPCI INTEGRATED PV ARRAY USING AVERAGE MODEL (DACM) AND SWITCHING CIRCUIT (SCM)

Parameters	T_{st}	RMS Errors DACM and SCM				
		V_{PV}	v_{C1}	v_{FC}	v_o	i_o
$G = 350\ \frac{\text{W}}{\text{m}^2}$,	40 μs	0.01	0.03	0.11	0.92	0.09
$T = 30\ ^\circ$C, $V_d^* = 46$ V,	80 μs	0.17	0.09	0.12	0.98	0.11
and $Z_L = 5 + j3.14\ \Omega$	160 μs	0.38	0.37	0.17	1.51	0.17
$G = 350\ \frac{\text{W}}{\text{m}^2}$,	40 μs	0.1	0.1	0.11	1.0	0.09
$T = 25\ ^\circ$C, $V_d^* = 46$ V,	80 μs	0.19	0.2	0.13	0.86	0.1
and $Z_L = 5 + j3.14\ \Omega$	160 μs	0.36	0.32	0.16	2.83	0.43
$G = 250\ \frac{\text{W}}{\text{m}^2}$,	40 μs	0.36	0.25	0.16	0.65	0.08
$T = 25\ ^\circ$C, $V_d^* = 46$ V,	80 μs	0.7	0.49	0.23	0.69	0.04
and $Z_L = 5 + j3.14\ \Omega$	160 μs	1.27	0.17	0.36	2.4	0.36
$G = 250\ \frac{\text{W}}{\text{m}^2}$,	40 μs	0.07	0.12	0.08	0.56	0.06
$T = 25\ ^\circ$C, $V_d^* = 46$ V,	80 μs	0.14	0.22	0.1	1.06	0.12
and $Z_L = 8 + j3.14\ \Omega$	160 μs	0.28	0.45	0.15	2.23	0.25

as those considered for Fig. 3.14. Note that, as mentioned in Section V, these execution times are obtained by simulating the system using PSCAD/EMTDC software on a desktop computer with Intel® Core™ i5-3470 CPU @ 3.2 GHz processor, 8 GB RAM and Windows 10 64-bit operating system.

As listed in Table 3.9, for Case-I to Case-III, the simulation time-step (T_{st}) is considered as 1 μs for both SCM and DACM based simulations, whereas the plot step (T_p) is varied from 40 μs to 160 μs. It can be seen that for the same simulation time-step, the DACM based simulation runs approximately three times faster than the SCM based simulation. Further it is also observed that the value of plot step has negligible or no effect on the total execution time. In Case-IV, the simulation time-steps for the DACM based simulations is considered as 40 μs, which is 40 times higher than that considered for SCM based simulation. It can be seen that the execution time of DACM based simulation is very less (approximately 50 times) compared to the SCM based simulation. This clearly demonstrates the strength of DACM in reducing the simulation times required for system level studies.

Further, in Case-V and Case-VI, the switching frequency of the SCM is changed

Table 3.9. EXECUTION TIMES (T_e) FOR 100 S RUN TIME OF PV ARRAY INTEGRATED ANPCI USING SWITCHING CIRCUIT MODEL (SCM) AND AVERAGE MODEL (DACM)

Case	Simulation parameters⋆					Execution time	
	SCM			DACM		SCM	DACM
	T_{st}	T_p	f_{s1}	T_{st}	T_p	T_e	T_e
I	1 μs	40 μs	10 kHz	1 μs	40 μs	4688 s	1732 s
II	1 μs	80 μs	10 kHz	1 μs	80 μs	4588 s	1692 s
III	1 μs	160 μs	10 kHz	1 μs	160 μs	4555 s	1680 s
IV	1 μs	50 μs	10 kHz	40 μs	40 μs	4622 s	96 s
V	2 μs	50 μs	5 kHz	80 μs	80 μs	2367 s	48 s
VI	5 μs	50 μs	2 kHz	160 μs	160 μs	991 s	24 s

⋆ All other system parameters are same as those considered for Fig. 3.14.

to 5 kHz and 2 kHz, respectively, which helps to increase the simulation time-step for SCM based simulations. Even for these two cases, the DACM based simulation has significantly smaller execution times compared to the SCM based simulations.

3.8 SUMMARY

In this chapter, a DACM of ANPCI is developed. The DACM can include the non-idealities in the converter components and the CVBS. The model is also modular in nature and hence it can be extended for an N-level ANPCI. The waveforms obtained from PSCAD/EMTDC simulations of switching circuit, experiments, and average model, and the corresponding RMS errors confirm that the averaged model presented can accurately predict the steady-state and dynamic waveforms of ANPCI in both open-loop and SRF-dq controller based closed-loop operation. In addition, the effectiveness of the model is also demonstrated using a simple stand-alone PV system with ANPCI as the power conversion stage. From the results presented, it is confirmed that the dynamic average circuit model requires significantly less computation time compared to the detailed switching circuit model. Thus, the average model can be recommended for system-level studies with ANPCI as power converter interface to save the computational time and resources required.

CHAPTER 4

SINGLE-PHASE CHOPPER INTEGRATED ANPCI

4.1 INTRODUCTION

In Chapter 1, a brief review of the three classical MLIs, viz., NPC-MLI, FC-MLI, and CHB-MLI as well as ANPCI is discussed. In Chapter 2, detailed operation and steady-state analysis of single-phase five-level ANPCI are presented. The performance of four different PWM techniques is compared for five-level ANPCI. Also, in this chapter four different Capacitor Voltage Balancing Strategies (CVBS) are discussed and their performance is compared for the ANPCI. Further, an SRF-dq controller is presented and implemented for the single-phase ANPCI. Finally, various CVBS and the SRF-dq controller operation are verified using the demonstrated results. Chapter 3 has presented a dynamic average circuit model of the ANPCI.

As discussed in the previous chapters, for effective operation of the ANPCI, its DC-link capacitor voltages and FC voltage must be maintained at specific voltages. In Chapter 2, four different capacitor voltage balancing strategies are presented to regulate the DC-link capacitor voltages and FC voltage of ANPCI. However, it is shown that these four strategies are not successful in reducing the peak-to-peak ripple in DC-link capacitor voltages. In the Strategy-IV presented in Chapter 2, the FC voltage was maintained almost constant with negligible ripple due to the availability of sufficient number of redundant switching states. However, as sufficient number of redundant switching states are not available in the single-phase ANPCI, the ripple in DC-link capacitor voltages could not be reduced below a pre-defined limit. In single-phase systems, the inverter's DC-link experiences double line frequency ripple due to pulsating output power, which effects transient operation of the sys-

tem and deteriorate the output voltage causing lower order harmonics [27, 28]. Due to high ripple in the DC-link capacitor voltages, the voltage stress of switching devices in ANPCI will increase. These voltage ripples also introduce more harmonics in the output voltage of the converter. Although it is possible to reduce the voltage ripple by employing high value of DC-link capacitors, it will significantly reduce the power density of the converter. Further, very high DC-link capacitors cannot completely solve the issues related to low-frequency ripple and also any transients in the capacitor voltages can produce unexpected transients on the output voltage (v_{an}) and the system behavior [28]. Hence, an auxiliary circuit is necessary to minimize ripple in the DC-link capacitor voltages to a smaller value.

In literature [88, 110–114], there are different methods to regulate the DC-link capacitor voltages using external or auxiliary circuits for MLIs. In [110, 111], the existing power supply is used to generate two separate voltage sources which are connected across each of the DC-link capacitors. An external chopper circuit with single DC-source can be used to balance the DC-link capacitor voltages using different control strategies [114, 115]. In [113, 116, 117], a method based on resonant switched capacitors is proposed and implemented with and without feedback control. However, these methods are generally applied to NPC-MLIs or FC-MLIs. In [114], the chopper-based configuration along with the single-pulse based and the multi-pulse based discontinuous chopper current control schemes are proposed for the five-level NPC-MLI with reduced component count.

In this chapter, the CVBS-IV is used to regulate the average values of FC and DC-link capacitor voltages to their respective nominal values. Further, it is proposed to integrate an external chopper-based voltage balancing circuit for ANPCI to reduce the voltage ripples in the DC-link capacitors. Various chopper switch control schemes, namely, single-pulse based chopper current control scheme, multi-pulse based discontinuous chopper current control scheme, multi-pulse based continuous chopper current control scheme, hysteresis voltage control method, Continuous Conduction Mode (CCM) based hysteresis current control method and CCM based average current control with constant switching frequency are implemented to regulate the ripple in DC-link capacitor voltages of the chop-

per integrated ANPCI. In this chapter, out of these six techniques, all the techniques except single-pulse based chopper current control scheme and multi-pulse based discontinuous chopper current control scheme, are proposed. Note that the switching signals for the ANPCI are generated using the PDS-PWM technique. All these chopper control schemes are implemented in PSCAD/EMTDC based simulation. The chopper integrated ANPCI with all the chopper control schemes, except the single-pulse based chopper current control scheme, is implemented on the hardware using the Texas Instruments TMS320F28335 Digital Signal Controller (DSC) kit. The experimental waveforms obtained for the ANPCI and the chopper integrated ANPCI are analyzed and their performance comparison is presented.

This chapter is organized into five sections. Section 4.2 describes the circuit diagram and operation of the chopper integrated ANPCI. In Section 4.3, the control methods for the chopper circuit are explained in detail. Simulation and experimental results are presented in Section 4.4. Finally, Section 4.5 summarizes this chapter.

4.2 CHOPPER INTEGRATED SINGLE-PHASE FIVE-LEVEL ANPCI

Even though voltage balancing is possible, from the results compared in Section 2.4, it can be concluded that none of the capacitor voltage balancing strategies are successful in reducing the peak-to-peak ripple in DC-link capacitor voltages. An external chopper-based voltage balancing circuit is added to the DC-link of single-phase ANPCI. Employing an external circuit for ripple reduction helps in size reduction of the DC-link capacitors and FC without imposing any operational constraint on the converter. Hence, the power density increases and enhances the reliability of the ANPCI. Six suitable control techniques are also presented for the chopper circuit to reduce ripple in the DC-link capacitor voltages, among them five techniques can limit the current flowing through various elements of chopper circuit. Note that the external chopper circuit augments the CVBS-IV in regulating the DC-link capacitor voltages of ANPCI. Employing an external circuit for voltage ripple reduction also helps in size reduction of the DC-link capacitors and increasing the power density and reliability.

Fig. 4.1 shows the circuit diagram of a single-phase five-level chopper integrated ANPCI, in which two switches (S_9, S_{10}), and an inductor (L_{ch}) are connected at the DC-link of the ANPCI. Note that both the chopper switches have bidirectional current carrying capability due to the anti-parallel diodes. Fig. 4.2 shows the equivalent circuits of the chopper for various operating modes. By using switch S_9 and diode D_{10}, energy stored in C_1 can be transferred to C_2 through the chopper inductor L_{ch}. Similarly, the energy stored in C_2 can be transferred to C_1 by using switch S_{10} and diode D_9. At any instant of time, the switches S_9 and S_{10} are either operated in complementary mode or turned OFF.

The switching states of the ANPCI are listed in Table 4.1. From this table, it can be seen that the voltage v_{C1} decreases and v_{C2} increases in the positive half cycle of inductor current i_L, due to which the ripple content in v_{C2}, i.e., v_{C2r} also increases, where

$$v_{C2r} = v_{C2} - \frac{V_{DC}}{2} \tag{4.1}$$

If v_{C2r} exceeds a predefined tolerance ϵ, the chopper circuit transfers the excessive energy in C_2 to C_1 by operating S_{10} and D_9. To achieve this, initially switch S_{10} is turned ON for a specific time-interval, t_1, so that C_2 is connected in parallel to L_{ch} as shown in Fig. 4.2(a). Thus, C_2 transfers energy to L_{ch} and the chopper inductor current i_{ch} increases. After the interval t_1, the switch S_{10} is turned OFF and L_{ch} gets connected in parallel to C_1 by the diode D_9 as shown in Fig. 4.2(b). In this interval the energy stored in L_{ch} will be transferred to C_1

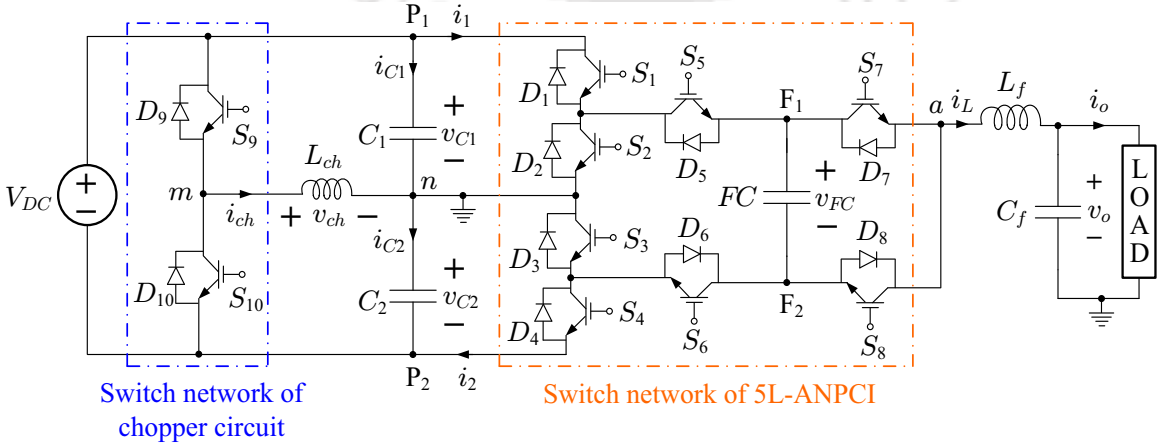


Fig. 4.1. Circuit diagram of chopper integrated single-phase five-level ANPCI.

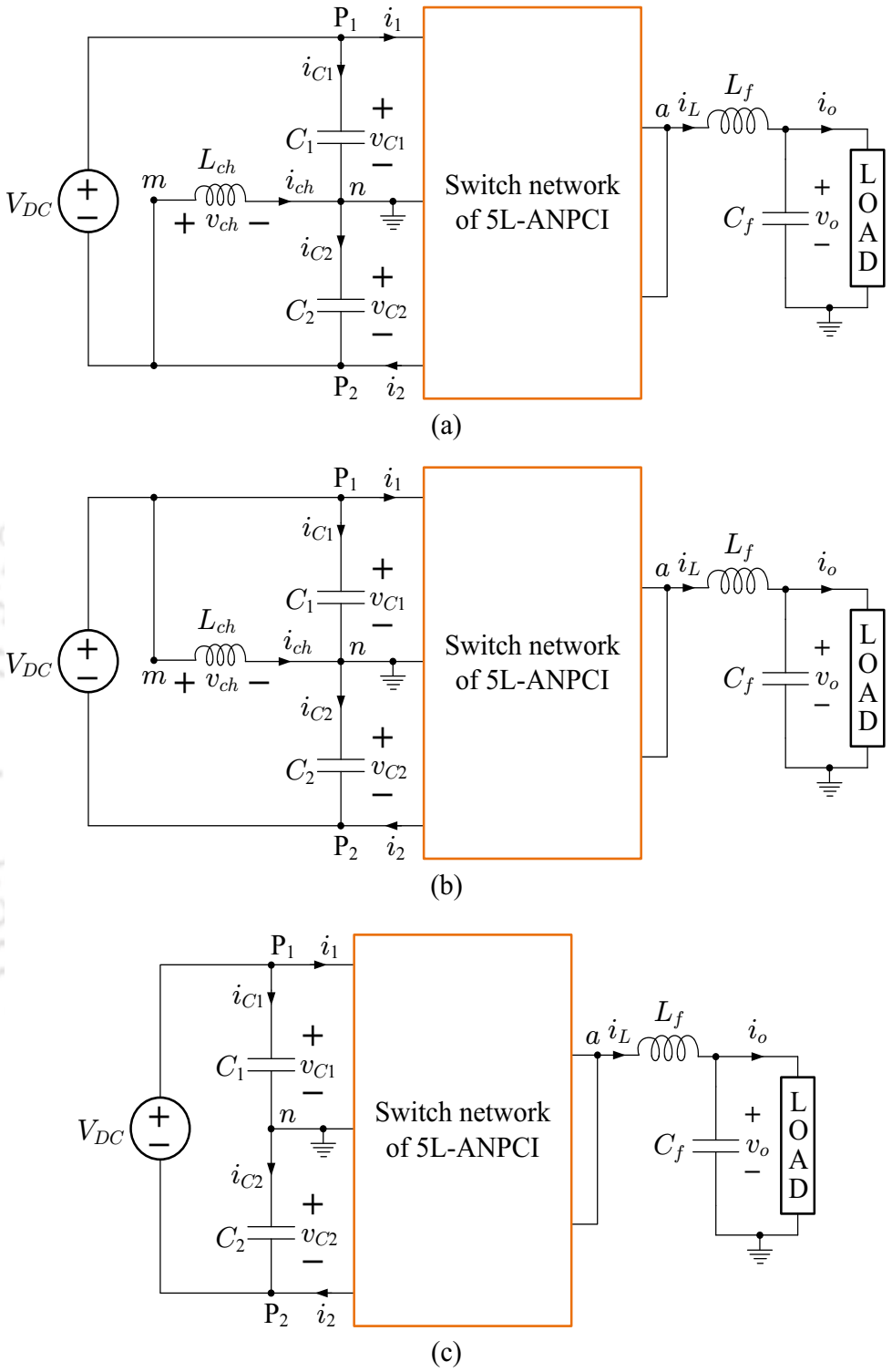


Fig. 4.2. Equivalent circuits of the chopper integrated ANPCI with (a) S_{10} or D_{10} is conducting, (b) S_9 or D_9 is conducting, and (c) none of S_9, D_9, S_{10}, and D_{10} is conducting.

for a duration of t_2. The time-intervals t_1 and t_2 depend on the chopper control strategy, the instantaneous voltage ripple v_{C2r} and the tolerance value ϵ. At any given time, the control strategy should ensure that the chopper inductor current does not exceed safe operating value

Table 4.1. POSSIBLE SWITCHING STATES FOR THE ANPCI OF FIG. 2.1

State	Voltage level	Switch positions								$i_L > 0$			$i_L < 0$		
	v_{an}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	v_{C1}	v_{C2}	v_{FC}	v_{C1}	v_{C2}	v_{FC}
I	$+\frac{V_{DC}}{2}$	1	0	1	0	1	0	1	0	↓	↑	N.E.	↑	↓	N.E.
II	$+\frac{V_{DC}}{4}$	1	0	1	0	1	0	0	1	↓	↑	↑	↑	↓	↓
III	$+\frac{V_{DC}}{4}$	1	0	1	0	0	1	1	0	N.E.	N.E.	↓	N.E.	N.E.	↑
IV	0	1	0	1	0	0	1	0	1	N.E.	N.E.	N.E.	N.E.	N.E.	N.E.
V	0	0	1	0	1	1	0	1	0	N.E.	N.E.	N.E.	N.E.	N.E.	N.E.
VI	$-\frac{V_{DC}}{4}$	0	1	0	1	1	0	0	1	N.E.	N.E.	↑	N.E.	N.E.	↓
VII	$-\frac{V_{DC}}{4}$	0	1	0	1	0	1	1	0	↓	↑	↓	↑	↓	↑
VIII	$-\frac{V_{DC}}{2}$	0	1	0	1	0	1	0	1	↓	↑	N.E.	↑	↓	N.E.

Note: Upward arrow (↑), Downward arrow (↓), and N.E. indicate increase, decrease, and no effect in capacitor voltages, respectively.

of the devices.

Similarly, in the negative half cycle of i_L, the voltage v_{C2} decreases and v_{C1} increases, due to which the ripple content in v_{C1}, i.e., v_{C1r} also increases, where

$$v_{C1r} = v_{C1} - \frac{V_{DC}}{2} \tag{4.2}$$

If v_{C1r} exceeds the tolerance value ϵ, the chopper circuit transfers the excessive energy in capacitor C_1 to C_2 by operating S_9 and D_{10}, using the similar steps explained above. If S_9 is turned ON, the voltage across L_{ch} is v_{C1} and the voltage stress on S_{10} is V_{DC}. If S_9 is turned OFF, diode D_{10} will carry the chopper current. In this state, the voltage across L_{ch} is $-v_{C2}$ and the voltage stress on S_9 is V_{DC}. This will result in reduction of the stored energy

in the overcharged capacitor C_1 , and hence v_{C1r} gets reduced. If both the capacitor voltage ripples are within the tolerance limit, all the chopper switches are kept in OFF condition. The equivalent circuit for this mode of operation is shown in Fig. 4.2(c). Therefore, according to the above given analysis, and from Table 4.1, S_{10} is controlled for $i_L > 0$, and S_9 is controlled for $i_L < 0$.

Note that when both the chopper switches are turned off and $i_{ch} = 0$, then the chopper based single-phase five-level ANPCI (see Fig. 4.1) operates as ANPCI, which is shown in Fig. 2.1. The method to generate the gate signals for the switches, S_1 to S_8, of the chopper based single-phase five-level ANPCI is the same as gate signals generation using Strategy-IV for the ANPCI described in Section 2.4. The capacitor voltage balancing strategy and the current control schemes for chopper based single-phase five-level ANPCI are independently operated.

In Section 4.3, operations of the single-pulse current based, multi-pulse current based, hysteresis based and continuous current based chopper control schemes are described, and their performance is compared for the chopper integrated ANPCI.

4.3 CHOPPER CONTROL SCHEMES

A control scheme is required to reduce ripple in the DC-link capacitor voltages of the chopper integrated ANPCI by operating the switches S_9 and S_{10}. In this chapter, the single-pulse current based, multi-pulse current based, hysteresis voltage based and CCM based chopper control schemes are implemented for the chopper integrated ANPCI [114, 115, 118–120]. The multi-pulse based chopper current control schemes are categorized into multi-pulse based discontinuous chopper current control scheme and multi-pulse based continuous chopper current control scheme, in which the latter is proposed in this thesis. Also, the hysteresis voltage based and CCM based chopper control schemes are proposed in this thesis. The hysteresis voltage based chopper control scheme does not control the chopper inductor current, but monitors this current to limit the range. The CCM based chopper control schemes are categorized into hysteresis current control method and average current

control with constant switching frequency. All the current control schemes except the single-pulse current control scheme require additional current transducer to measure the inductor current of the chopper, i_{ch}. The operation of all the three current control schemes is given in the following sub-sections when $v_{C1r} > \epsilon$. In similar to this, the operation for $v_{C2r} > \epsilon$ can be interpreted.

4.3.1 Single-Pulse based Chopper Current Control Scheme

The waveforms of single-pulse based chopper current control scheme are shown in Fig. 4.3. Here, G_{S9} and G_{S10} are the gate signals of the switches, S_9 and S_{10}, respectively. In this current control scheme, when $v_{C1r} > \epsilon$, then S_9 is turned ON and i_{ch} continuously rises in the chopper inductor for the period of time (t_{on}), which is calculated by considering L_{ch} to achieve $v_{C1r} < \epsilon$. The maximum current of i_{ch} obtains at t_{on}, which is given by I_{ch}^{Max}. After this time period (t_{on}) lapses, the switch S_9 is turned OFF. Then, the chopper inductor current starts decaying to zero. The time period when i_{ch} reaches to zero is called total time, t_t. When this time period lapses, the chopper cycle completes. The ripple in the capacitor voltages, v_{C1} and v_{C2}, is estimated to be zero at the end of the chopper cycle.

When $v_{C1r} > \epsilon$, considering the ideal DC-voltage source the ripple energy transferred from C_1 and C_2 to L_{ch} to mitigate the voltage ripple, V_{C1r}, can be expressed as

$$\frac{L_{ch}\left(I_{ch}^{Max}\right)^2}{2} = \frac{(C_1+C_2)}{2}\left[\left(\frac{V_{DC}}{2}+V_{C1r}\right)^2 - \left(\frac{V_{DC}}{2}\right)^2\right] \tag{4.3}$$

where V_{C1r} is the sampled value of the v_{C1r} at the starting of the chopper cycle, i.e., at $t = 0$. Hence, the peak $\left(I_{ch}^{Max}\right)$ of the single-pulse current as shown in Fig. 4.3 is

$$I_{ch}^{Max} = \sqrt{\frac{2C_1V_{C1r}\left(V_{DC}+V_{C1r}\right)}{L_{ch}}} \tag{4.4}$$

The voltage across the chopper inductor, v_{ch} $\left(\simeq \frac{V_{DC}}{2}\right)$ with period, t_{on}, is approximated as

$$\frac{V_{DC}}{2} \simeq \frac{L_{ch}I_{ch}^{Max}}{t_{on}} \tag{4.5}$$

The period, t_{on}, calculated using (4.4) and (4.5) is given as

$$t_{on} = \frac{2\sqrt{2L_{ch}C_1V_{C1r}\left(V_{DC}+V_{C1r}\right)}}{V_{DC}} \tag{4.6}$$

4.3.2 Multi-Pulse based Discontinuous Chopper Current Control Scheme

The waveforms of multi-pulse based discontinuous chopper current control scheme are shown in Fig. 4.4. In this current control scheme, when $v_{C1r} > \epsilon$, then S_9 is turned ON and i_{ch} continuously rises in the chopper inductor till i_{ch} reaches to a predefined value, I_{ch}^{Max}. The time period when i_{ch} reaches to I_{ch}^{Max} in the first current pulse is t_{on}. At this time instant, the switch S_9 is turned OFF until $i_{ch} = 0$. The time period when i_{ch} reaches to zero at the end of the first current pulse is called total time, t_t. When $i_{ch} = 0$, S_9 is again turned ON and this process continues until $v_{C1r} < \epsilon$. If $v_{C1r} < \epsilon$, then the switch S_9 will be in OFF position. At this condition when i_{ch} reaches to zero, i.e., at the end of the final current pulse, the chopper cycle completes. The time lapsed till this time instant is defined as final time,

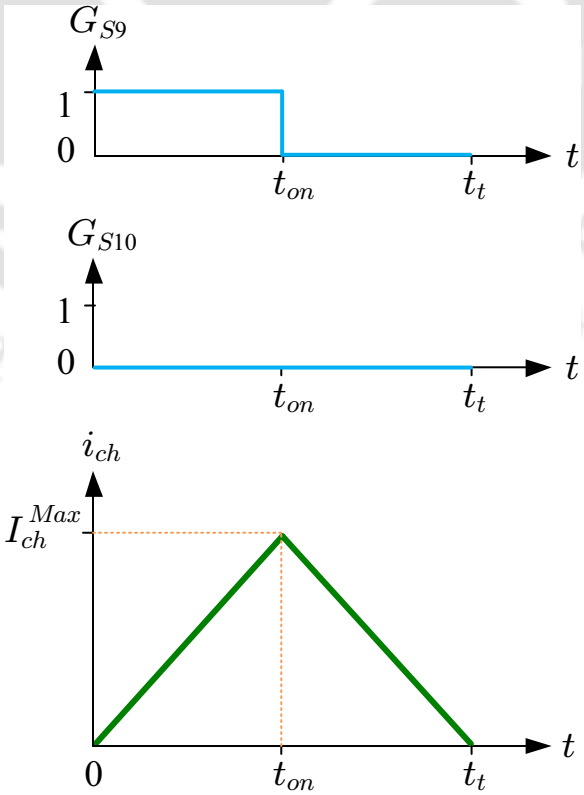


Fig. 4.3. Waveforms of single-pulse based chopper current control scheme.

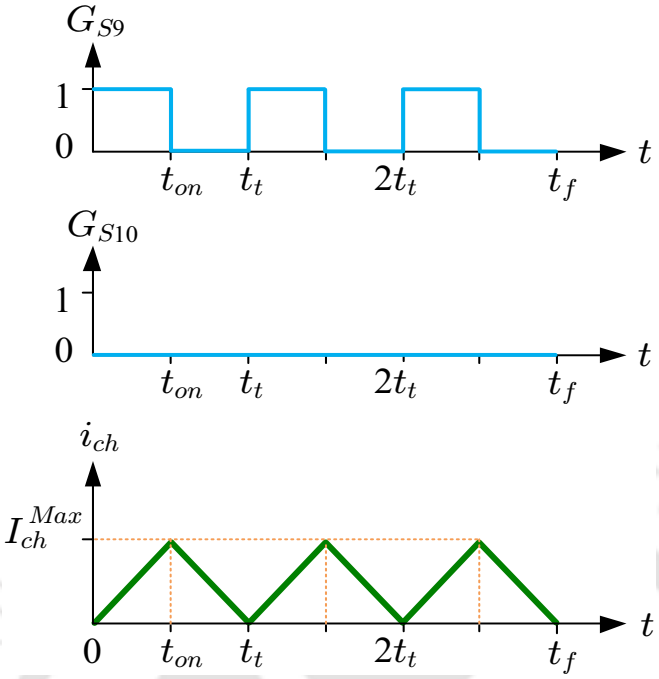


Fig. 4.4. Waveforms of multi-pulse based discontinuous chopper current control scheme.

given by t_f. It means, the discontinuous current pulses occur continuously until ripple in the capacitor voltages, v_{C1} and v_{C2}, reduces to the desired range.

4.3.3 Multi-Pulse based Continuous Chopper Current Control Scheme

The waveforms of multi-pulse based continuous chopper current control scheme are shown in Fig. 4.5. This current control scheme is proposed with the combined features of single-pulse based chopper current control scheme and multi-pulse based discontinuous chopper current control scheme, viz., maintaining low voltage ripple and low current rating of the chopper inductor. When $v_{C1r} > \epsilon$, then S_9 is turned ON and i_{ch} steeply rises in the chopper inductor until i_{ch} reaches to a predefined value, I_{ch}^{Max}. Unlike multi-pulse based discontinuous chopper current control scheme, i_{ch} is continuous and maintained near I_{ch}^{Max}. The time period when i_{ch} reaches to I_{ch}^{Max} in the first current pulse is t_{on}. At this time instant, the switch S_9 is turned OFF until i_{ch} reaches to I_{ch}^{Min}, which is given by

$$I_{ch}^{Min} = I_{ch}^{Max} - \epsilon_i \tag{4.7}$$

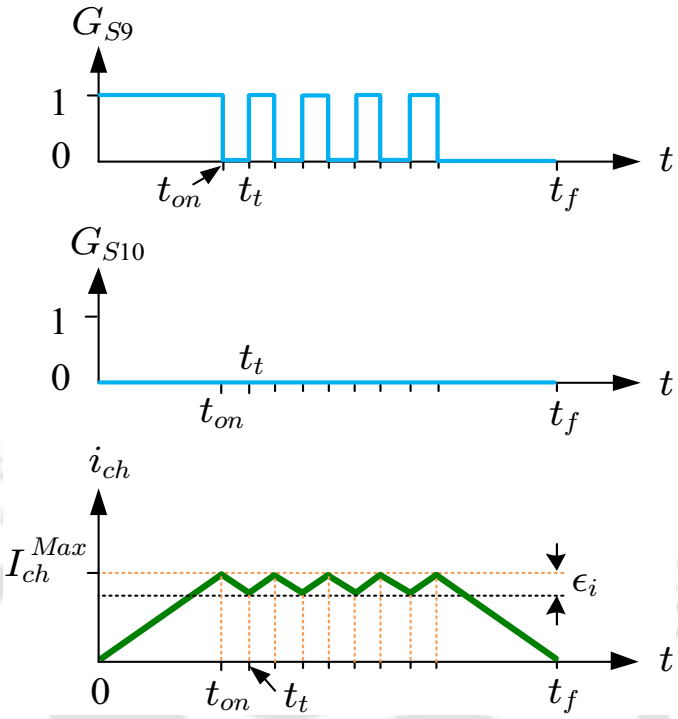


Fig. 4.5. Waveforms of multi-pulse based continuous chopper current control scheme.

where $\epsilon_i > 0$ is a predefined current tolerance. The time period when i_{ch} reaches to I_{ch}^{Min} at the end of the first current pulse is called total time, t_t. As i_{ch} is decreasing, when i_{ch} crosses I_{ch}^{Min}, i.e., $i_{ch} \leqslant I_{ch}^{Min}$, S_9 is again turned on till $i_{ch} = I_{ch}^{Max}$ and this process continues until $v_{C1r} < \epsilon$. If $v_{C1r} < \epsilon$, then the switch S_9 will be in OFF position. At this condition when i_{ch} reaches to zero, i.e., at the end of the final current pulse, the chopper cycle completes. The time lapsed till this time instant is the final time, given by t_f. It means, the continuous current pulses occur continuously until ripple in the capacitor voltages, v_{C1} and v_{C2}, reduces to the desired range. While i_{ch} is traversing to zero, if v_{C1r} rises and $v_{C1r} > \epsilon$, then S_9 is turned ON, thereby i_{ch} increases. It indicates that the chopper cycle is again started.

4.3.4 Hysteresis Voltage Control Method

In this control method, the chopper switches are controlled based on voltage ripple only but not according to the chopper current reference. However the chopper current is continuously monitored and if its magnitude exceeds, I_{ch}^{Max}, both the switches S_9 and S_{10} are turned OFF to protect the chopper circuit. As shown in Fig. 4.6, when $v_{C1r} > \epsilon$, S_{10} is turned OFF and S_9 is turned ON; so the inductor L_{ch} will be connected in parallel with

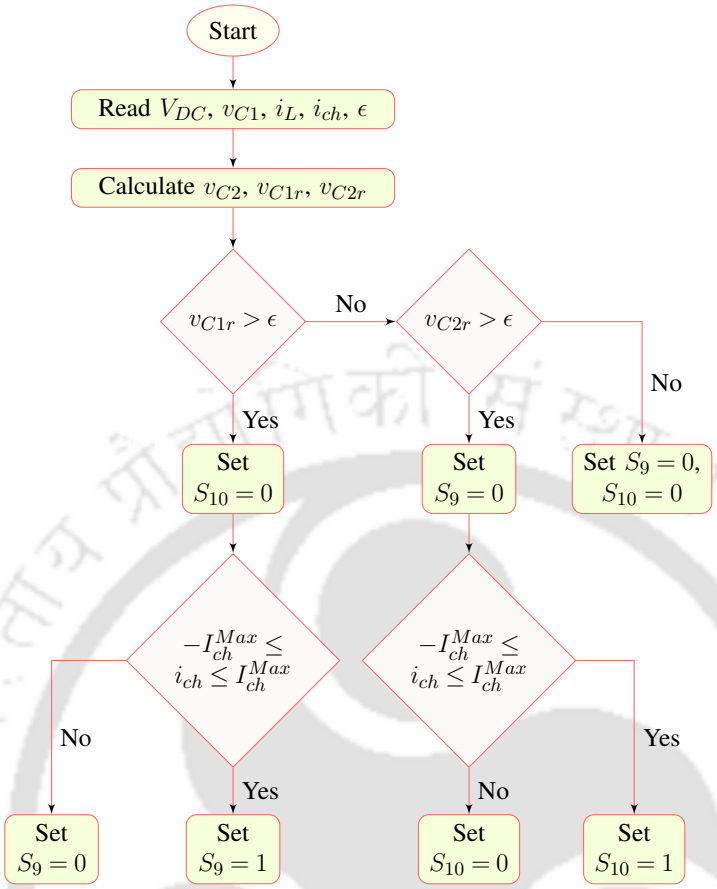


Fig. 4.6. Flowchart representing the hysteresis voltage control method to control the chopper circuit switches in chopper integrated ANPCI.

C_1. Therefore the energy is transferred from C_1 to L_{ch}. As i_{ch} increases, energy stored in L_{ch} increases. If i_{ch} exceeds maximum value I_{ch}^{Max}, then S_9 is also turned OFF. Similarly, when $v_{C2r} > \epsilon$, S_9 is turned OFF and S_{10} is turned ON; so L_{ch} will be connected in parallel with C_2. Therefore the energy is transferred from C_2 to L_{ch}. Hence, the magnitude of i_{ch} increases and energy stored in L_{ch} also increases. If the magnitude of i_{ch} exceeds maximum value I_{ch}^{Max}, then S_9 is also turned OFF.

4.3.5 CCM based Hysteresis Current Control Method

The flowchart for the CCM-based hysteresis current control method is shown in Fig. 4.7. The current control algorithm continuously monitors whether the magnitude of i_{ch} is less than the rated value of chopper inductor current, I_{ch}^{Max} or not. If the condition $-I_{ch}^{Max} < i_{ch} < I_{ch}^{Max}$ is not met, both the chopper switches S_9 and S_{10} are turned OFF

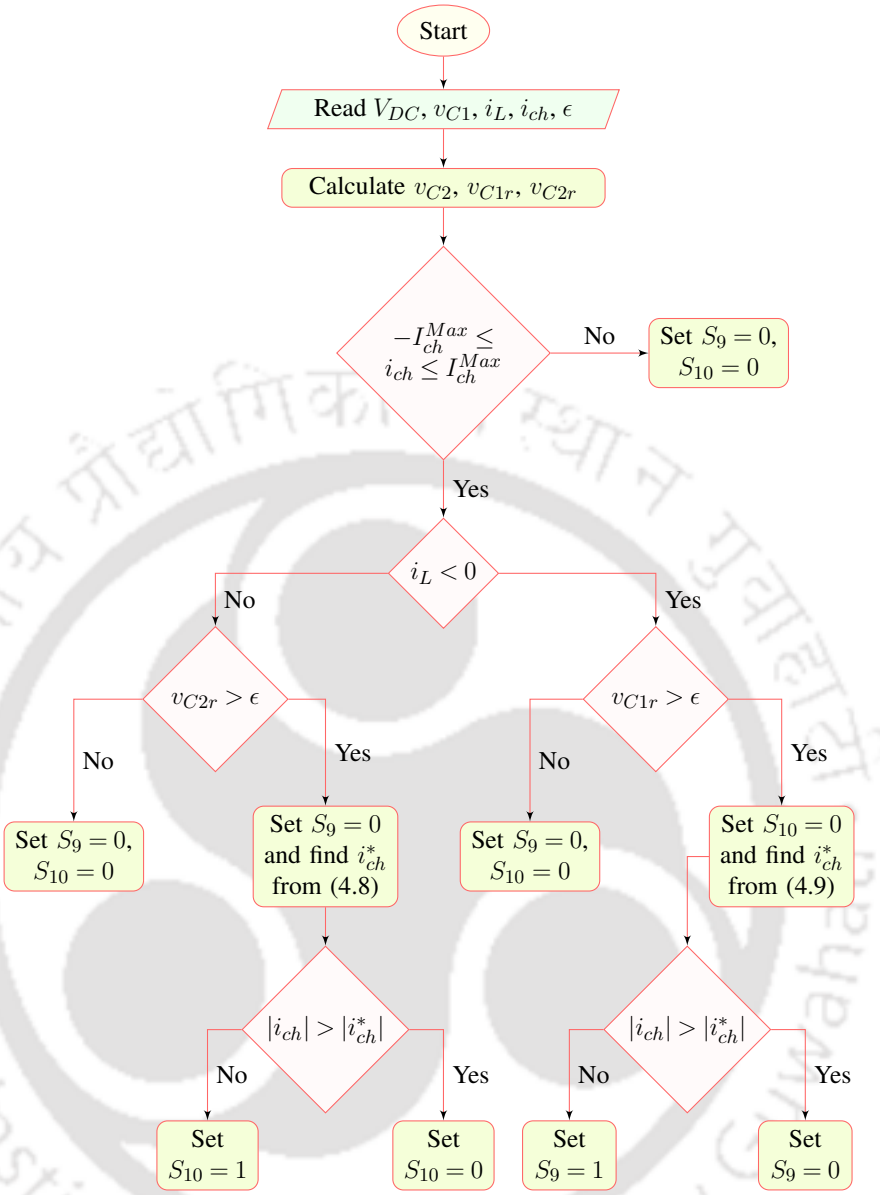


Fig. 4.7. Flowchart representing the hysteresis current control method to control the chopper circuit switches in chopper integrated ANPCI.

for protection of the chopper circuit. If the condition $-I_{ch}^{Max} < i_{ch} < I_{ch}^{Max}$ is true, then the control algorithm inspects the polarity of i_L. From Table 4.1, it can be seen that if the polarity of i_L is positive, then the ripple in one of the DC-link capacitor voltages, v_{C2}, increases. If the ripple in v_{C2}, i.e., v_{C2r} is greater than predefined tolerance, ϵ, then the chopper circuit must be operated to decrease v_{C2}. In this case, the switch S_9 is always turned OFF and i_{ch} is regulated using the switch S_{10} and diode D_9 such that it tracks the reference current, i_{ch}^*, which is generated using the equation,

$$i_{ch}^{*} = -k_p^h i_L - \frac{(v_{C2r} - \epsilon)}{r_e} \tag{4.8}$$

where k_p^h and r_e are the constants. It can be seen that i_{ch}^{*} contains a term proportional to i_L, which is responsible for ripple in DC-link capacitor voltages. After calculating i_{ch}^{*} from (4.8), switch S_{10} is controlled such that i_{ch} tracks i_{ch}^{*}. If $|i_{ch}|$ is less than $|i_{ch}^{*}|$, then S_{10} is turned ON, magnitude of i_{ch} increases and energy stored in the C_2 is transferred to the L_{ch}. If $|i_{ch}|$ is greater than $|i_{ch}^{*}|$, S_{10} is turned OFF, hence the energy in L_{ch} is transferred to C_1 through the diode D_9.

Similarly, if the polarity of i_L is negative, then the voltage ripple in the capacitor, C_1, increases. If the voltage ripple of C_1, i.e., v_{C1r} is greater than ϵ, then the chopper circuit must be operated to decrease v_{C1}. In this case, the switch S_{10} is always turned OFF and i_{ch} is regulated using the switch S_9 and diode D_{10} such that it tracks the reference current, i_{ch}^{*}, which is generated using the equation

$$i_{ch}^{*} = -k_p^h i_L + \frac{(v_{C1r} - \epsilon)}{r_e} \tag{4.9}$$

After calculating i_{ch}^{*} from (4.9), switch S_9 is controlled such that i_{ch} tracks i_{ch}^{*}. If $|i_{ch}|$ is less than $|i_{ch}^{*}|$, then S_9 is turned ON, $|i_{ch}|$ increases and energy stored in C_1 is transferred to L_{ch}. If $|i_{ch}|$ is greater than $|i_{ch}^{*}|$, then S_9 is turned OFF, hence the energy in L_{ch} is transferred to C_2 through the diode D_{10}.

4.3.6 CCM based Average Current Control with Constant Switching Frequency

Although the hysteresis band current control is a continuous conduction mode (CCM)-based technique, the chopper switching frequency is relatively high and continuously varies. Hence this subsection proposes a CCM-based average current control with

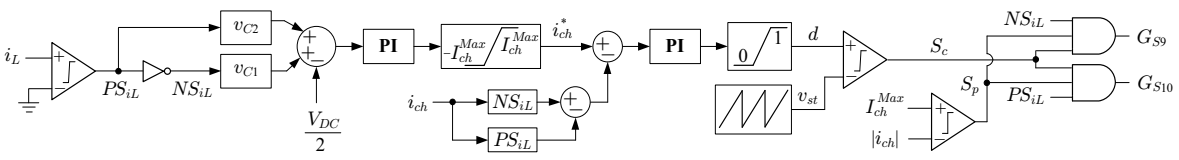


Fig. 4.8. Block diagram of the CCM based average current controller for chopper integrated ANPCI.

constant switching frequency for generating the gate pulses of chopper switches.

The block diagram of the proposed current control technique is shown in Fig. 4.8. Here, the variables, PS_{iL} and NS_{iL} indicate the polarity of current i_L. For $i_L > 0$, $PS_{iL} = 1$ and $NS_{iL} = 0$; for $i_L < 0$, $PS_{iL} = 0$ and $NS_{iL} = 1$. Thus, based on the polarity of i_L, either v_{C1} or v_{C2} is compared with $\frac{V_{DC}}{2}$. The resulting error signal will be fed through a PI controller to generate the reference chopper inductor current, i^*_{ch}. Note that the hard-limiter will limit the value of i^*_{ch} below the safe operating value of chopper devices. The reference current i^*_{ch} is then compared with actual current i_{ch} and the resulting error will be fed through another PI controller to generate the required duty ratio, d, as shown in Fig. 4.8. Then the chopper control signal S_c is generated by comparing the duty ratio d with a saw-tooth waveform v_{st}. Finally, the gate signals G_{S9} and G_{S10} for the switches S_9 and S_{10}, respectively, are generated using the logic gates as shown in Fig. 4.8. The logical expressions of G_{S9} and G_{S10} are given by

$$G_{S9} = S_p \cdot S_c \cdot NS_{iL} \quad \text{and} \quad G_{S10} = S_p \cdot S_c \cdot PS_{iL} \tag{4.10}$$

Here S_p is a chopper switch protection signal, which is generated by comparing the chopper current (i_{ch}) with maximum allowable chopper current, I^{Max}_{ch}, as shown in Fig. 4.8.

4.4 RESULTS AND DISCUSSION

To verify the effectiveness of chopper circuit in reducing the DC-link capacitor voltage ripple and the performance of all the chopper control schemes discussed in Section 4.3, the chopper integrated ANPCI of Fig. 4.1 has been simulated using various chopper control schemes. Note that the external chopper circuit augments the capacitor voltage balancing strategy-IV in regulating the DC-link capacitor voltages of ANPCI. The simulation results of all the chopper control schemes are presented and their performance is compared. Also, the experimental results are presented for all the control schemes except single-pulse current control scheme. Because, single-pulse current control scheme causes very high current rise and the chopper circuit damages.

4.4.1 Simulation Results

The simulation results are shown in Fig. 4.9 using the three chopper current control schemes based on single-pulse current and multi-pulse current, with the parameters given in Table 4.2 along with $C_1 = C_2 = 3$ mF and $FC = 1.6$ mF.

Fig. 4.9(a) depicts the PSCAD/EMTDC simulation results using the single-pulse based chopper current control scheme for the ANPCI without chopper till $t = 16$ ms and with chopper from $t = 16$ ms to $t = 50$ ms. As shown in Fig. 4.9(a), when the chopper is turned ON, the peak current drawn is very high and the ripple in the DC-link capacitor voltages increases. Eventually, the switches may get damaged due to the steep and large chopper current. Therefore, this current control scheme is not safe to implement in the hardware.

Fig. 4.9(b) depicts the PSCAD/EMTDC simulation results using the multi-pulse based discontinuous chopper current control scheme for the ANPCI without chopper till $t = 16$ ms and with chopper from $t = 16$ ms to $t = 50$ ms. Here, the predefined I_{ch}^{Max} is insufficient to reduce the voltage ripple to the desired range. Hence, I_{ch}^{Max} need to be increased further to limit the voltage ripple to the desired value. Depending on the value of L_{ch}, I_{ch}^{Max} can be selected. As shown in Fig. 4.9(b), i_{ch} is safely limited to I_{ch}^{Max} after the chopper is turned ON, i.e., for the circuit operation when $t \geqslant 16$ ms.

Fig. 4.9(c) depicts the PSCAD/EMTDC simulation results using the multi-pulse

Table 4.2. PARAMETERS OF CHOPPER INTEGRATED ANPCI WITH PULSE BASED TECHNIQUES

Parameters	Attributes
V_{DC}	64 V
I_{ch}^{Max}	7 A
I_{ch}^{Min}	6.8 A
Fundamental frequency (f_o)	50 Hz
Switching frequency of ANPCI (f_{s1})	10 kHz
Switching frequency of chopper circuit (f_{s2})	20 kHz
Tolerance (ϵ)	2% of the reference value
L_f and L_{ch}	2 mH
C_f	20 μF

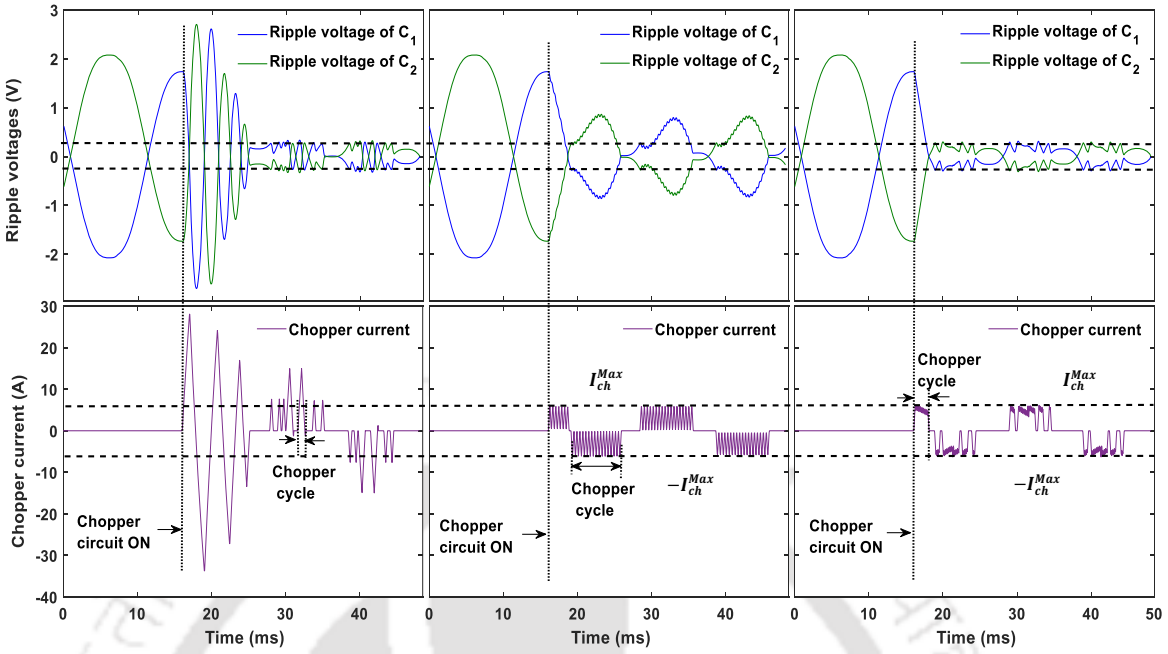


Fig. 4.9. PSCAD/EMTDC simulation results for the chopper based five-level ANPCI shown in Fig. 4.1 with the chopper circuit turned ON from the OFF state at $t = 16$ ms using (a) single-pulse based chopper current control scheme (b) multi-pulse based discontinuous chopper current control scheme, and (c) multi-pulse based continuous chopper current control scheme.

based continuous chopper current control scheme for the ANPCI without chopper till $t = 16$ ms and with chopper from $t = 16$ ms to $t = 50$ ms. As shown in Fig. 4.9(c), i_{ch} is safely limited to I_{ch}^{Max} after the chopper is turned ON, i.e., for the circuit operation when $t \geqslant 16$ ms. The chopper current is zero for large time in the multi-pulse based continuous chopper current control scheme compared to the multi-pulse based discontinuous chopper current control scheme. Hence, the current rating of the L_{ch}, i.e., I_{ch}^{Max} can be further reduced in the multi-pulse based continuous chopper current control scheme. Also, the ripple reduction is more in this control scheme compared to the multi-pulse based discontinuous chopper current control scheme.

The simulation results are shown in Fig. 4.10 using hysteresis current control scheme and hysteresis voltage control scheme for the chopper control, with the parameters given in Table 4.3.

Fig. 4.10(a) depicts the PSCAD/EMTDC simulation results using the hysteresis current control scheme for the ANPCI without chopper till $t = 0.3$ s and with chopper from

Table 4.3. PARAMETERS OF CHOPPER INTEGRATED ANPCI WITH HYSTERESIS VOLTAGE CONTROL AND HYSTERESIS CURRENT CONTROL SCHEMES

Parameters	Attributes
V_{DC}	1 kV
Fundamental frequency (f_o)	50 Hz
Switching frequency of ANPCI (f_{s1})	10 kHz
Switching frequency of chopper circuit (f_{s2})	20 kHz
$\|I_{ch}^{Max}\|$	50 A
Tolerance (ϵ)	2% of the reference value
Modulation index (M)	0.9
Load resistance (R_L)	10 Ω
L_{ch}	3 mH
C_1 and C_2	0.47 mF
FC	0.22 mF
L_f	2 mH
C_f	20 μF

$t = 0.3$ s to $t = 0.45$ s. For $t < 0.3$ s, both the chopper switches are turned OFF and hence the ANPCI operates without chopper. It can be seen from Fig. 4.10 that the peak-to-peak ripple in capacitor voltages is 190.26 V, which causes distortion in PWM voltage, v_{an}. As shown in Fig. 4.10(a), the chopper is turned ON at $t = 0.3$ s and its switches are operated using hysteresis current control method. It can be seen that the peak-to-peak ripple in capacitor voltages slowly reduces to 42.3 V in approximately 244 ms. The chopper current i_{ch} is sinusoidal and it follows the reference current, i_{ch}^*. As shown in Fig. 4.10(b), the chopper is turned ON at $t = 0.3$ s and its switches are operated using hysteresis voltage control method. It can be seen that the peak-to-peak ripple in DC-link capacitor voltages quickly reduces to 11.66 V in approximately 2.6 ms. It can be observed that the peak-to-peak capacitor voltage ripple is lower and response time is faster for hysteresis voltage control method compared to hysteresis current control method. The peak-to-peak ripple in FC voltage is also less in case of hysteresis voltage control method. However, large distortion in the chopper inductor current is noted as it it not controlled.

The simulation results are shown in Fig. 4.11 using hysteresis current control

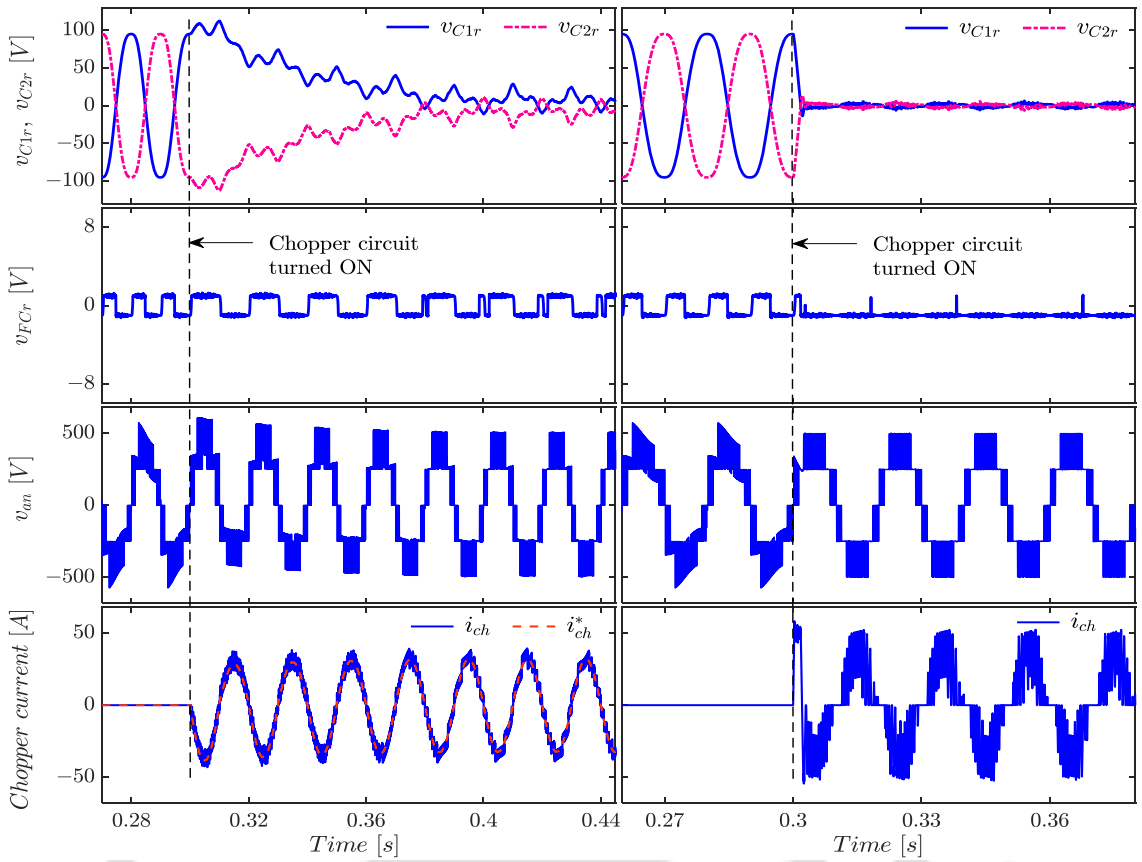


Fig. 4.10. PSCAD/EMTDC simulation results for chopper integrated ANPCI with the chopper circuit turned ON at $t = 0.3$ s using (a) hysteresis current control method, and (b) hysteresis voltage control method.

scheme and average current control scheme for the chopper control, with the parameters given in Table 4.4.

Fig. 4.11(a) and (b) depicts the PSCAD/EMTDC simulation results using hysteresis current controller (HCC) and average current controller (ACC), respectively, for the chopper integrated ANPCI. Here a step change in the load is given from 16 to 5 Ω, at $t_o = 0.5$ s. The peak-to-peak ripple in v_{C1}, v_{C2} and v_{FC} of ANPCI with and without chopper circuit are compared in Table 4.5.

From Fig. 4.11 and Table 4.5, it can be seen that the ripple in v_{C1} and v_{C2} are significantly reduced with the integration of the chopper circuit. For example, with $R_L = 5$ Ω, ΔV_C is 130.1 V for ANPCI without chopper circuit. After integrating the chopper circuit, ΔV_C is reduced to 22.31 V with HCC and 5.76 V with ACC. Also, both HCC and ACC techniques are successful in regulating the chopper current i_{ch} to its reference signal i^*_{ch}.

Table 4.4. PARAMETERS OF CHOPPER INTEGRATED ANPCI WITH HCC AND ACC

Parameters	Attributes
V_{DC}	800 V
Fundamental frequency (f_o)	50 Hz
Switching frequency of ANPCI (f_{s1})	10 kHz
Switching frequency of chopper circuit (f_{s2})	20 kHz
Tolerance (ϵ)	2% of the reference value
Modulation index (M)	0.9
L_f & L_{ch}	2 mH
C_1 & C_2	1 mF
FC	0.53 mF
C_f	20 μF

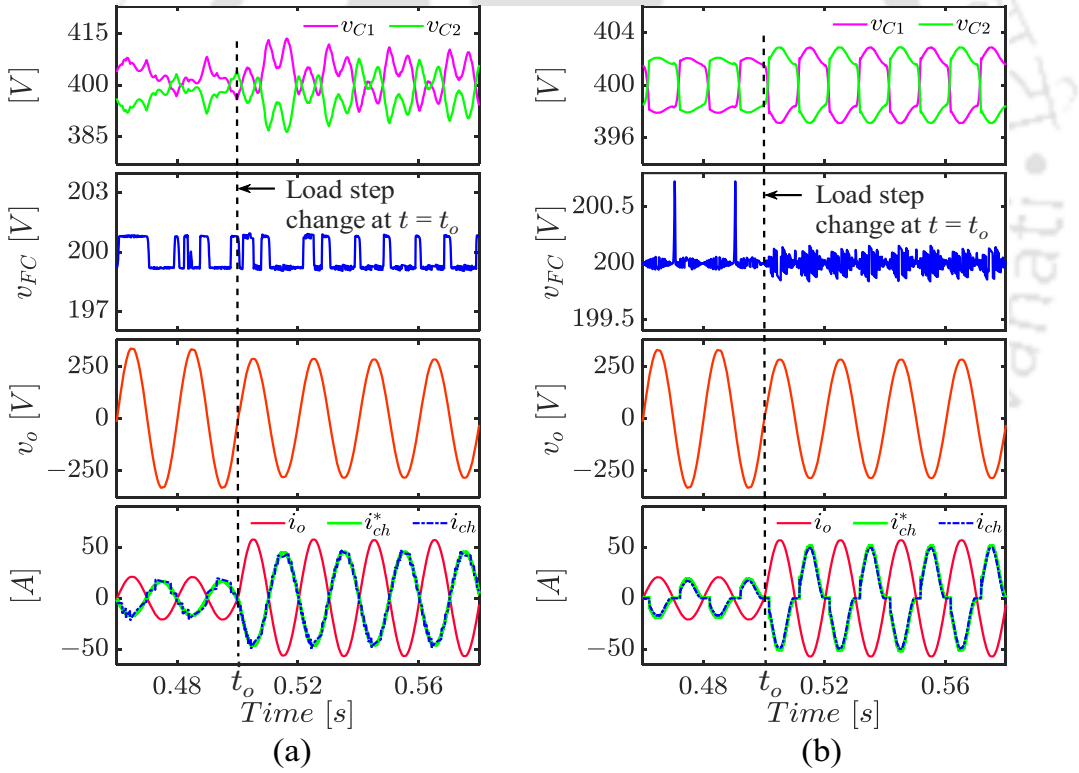


Fig. 4.11. PSCAD/EMTDC simulation results for chopper integrated ANPCI using (a) HCC, and (b) ACC.

However, from the simulation results, it can be noted that the ACC is performing better than HCC in reducing the ripple content.

Table 4.5. P-P RIPPLE IN v_{C1} AND v_{C2} (ΔV_C), P-P RIPPLE IN v_{FC} (ΔV_{FC}) FOR ANPCI WITH/WITHOUT CHOPPER INTEGRATION

P-P	$R_L = 16\ \Omega$			$R_L = 5\ \Omega$		
voltage	Fig.	Fig.	Fig.	Fig.	Fig.	Fig.
ripple	2.29(b)	4.11(a)	4.11(b)	2.29(b)	4.11(a)	4.11(b)
ΔV_C	47.03 V (11.75%)	13.75 V (3.44%)	4.16 V (1.04%)	130.1 V (32.52%)	22.31 V (5.57%)	5.76 V (1.44%)
ΔV_{FC}	1.6 V (0.8%)	1.71 V (0.85%)	0.78 V (0.39%)	1.91 V (0.95%)	1.92 V (0.96%)	0.32 V (0.16%)

4.4.2 Experimental Results

A hardware prototype of the chopper integrated ANPCI is built with the parameters listed in Table 4.2 to verify working and analysis of the chopper integrated ANPCI and control schemes. Fig. 4.12 shows the photograph of the experimental set-up. The control schemes, PWM technique, and the gate signal generation are implemented using TMS320F28335 Digital Signal Controller (DSC) kit. Also the DSC kit is used to implement the capacitor voltage balancing strategy along with all the chopper control schemes except single-pulse current control scheme described in Section 4.3. The experimental results of the

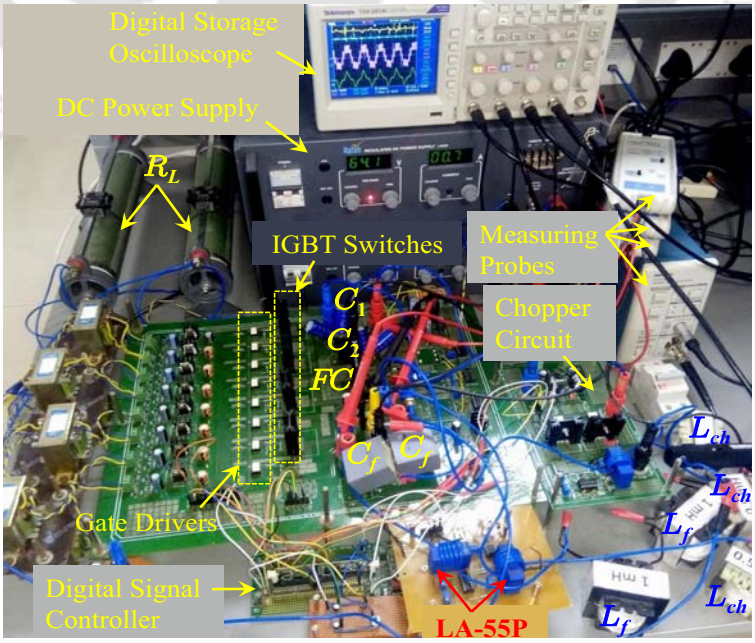


Fig. 4.12. Photograph for the hardware prototype of the chopper integrated ANPCI.

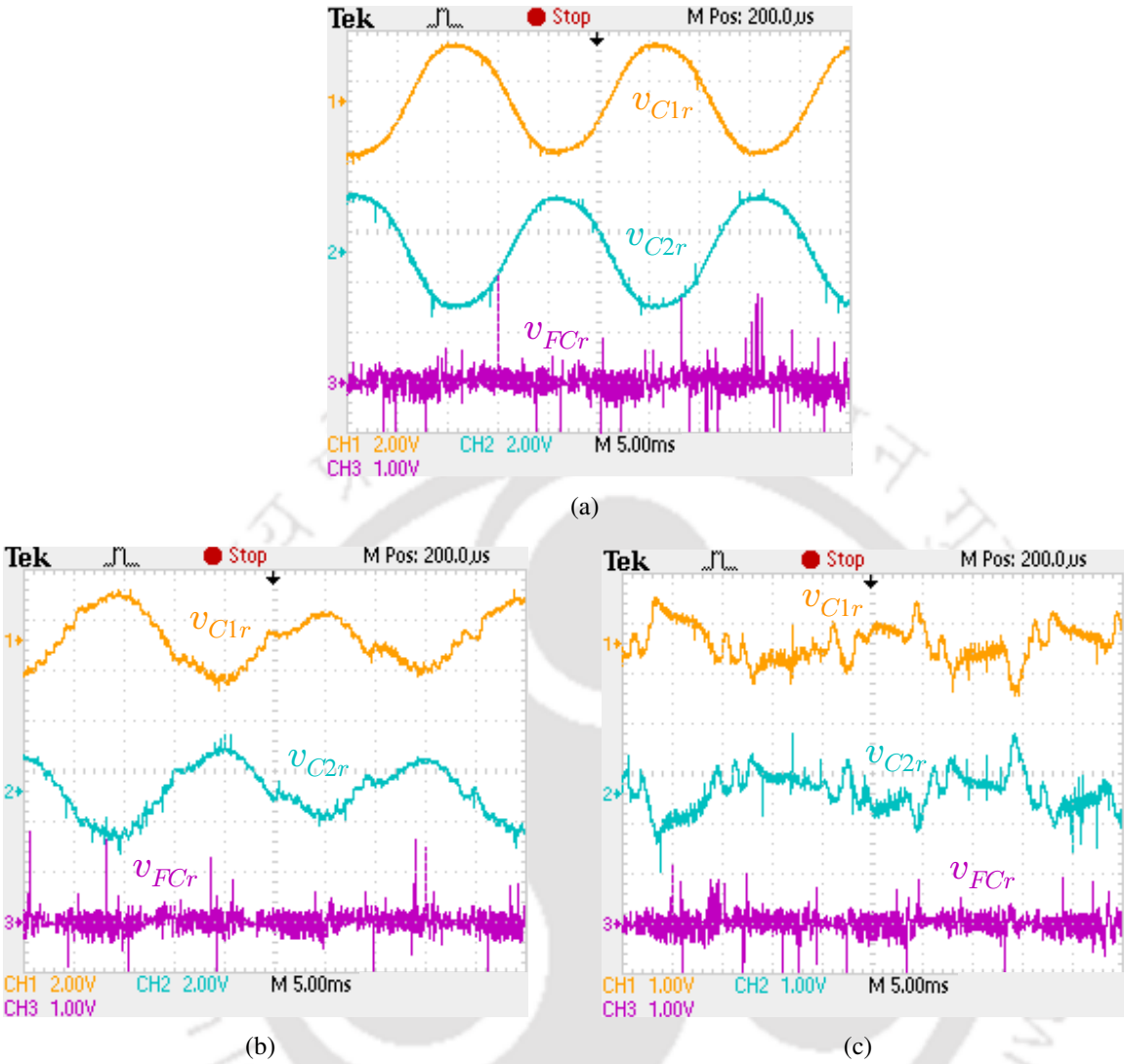


Fig. 4.13. The steady-state experimental waveforms for ripple in voltages of C_1, C_2, and FC with parameters given in Case M-1, $M = 0.9$ and 3.8 Ω load: (a) ANPCI without chopper (b) chopper integrated ANPCI with multi-pulse based discontinuous chopper current control scheme (c) chopper integrated ANPCI with multi-pulse based continuous chopper current control scheme.

chopper integrated ANPCI with and without load voltage control are presented. Here, rest of the parameters are considered with high and low capacitor values as two cases, viz., Case M-1: $C_1 = C_2 = 3$ mF and $FC = 1.6$ mF; Case M-2: $C_1 = C_2 = 1$ mF and $FC = 0.53$ mF. The voltages V_{DC}, v_{C1} and v_{FC} are measured using the LEM voltage sensors LV-25P, the currents flowing in the chopper and the filter inductors are measured using the LEM current sensors, LA-55P.

As mentioned in Case M-1, the parameters are considered for the waveforms shown in Fig. 4.13 and for the results shown in Fig. 4.14, the parameters are given in Case

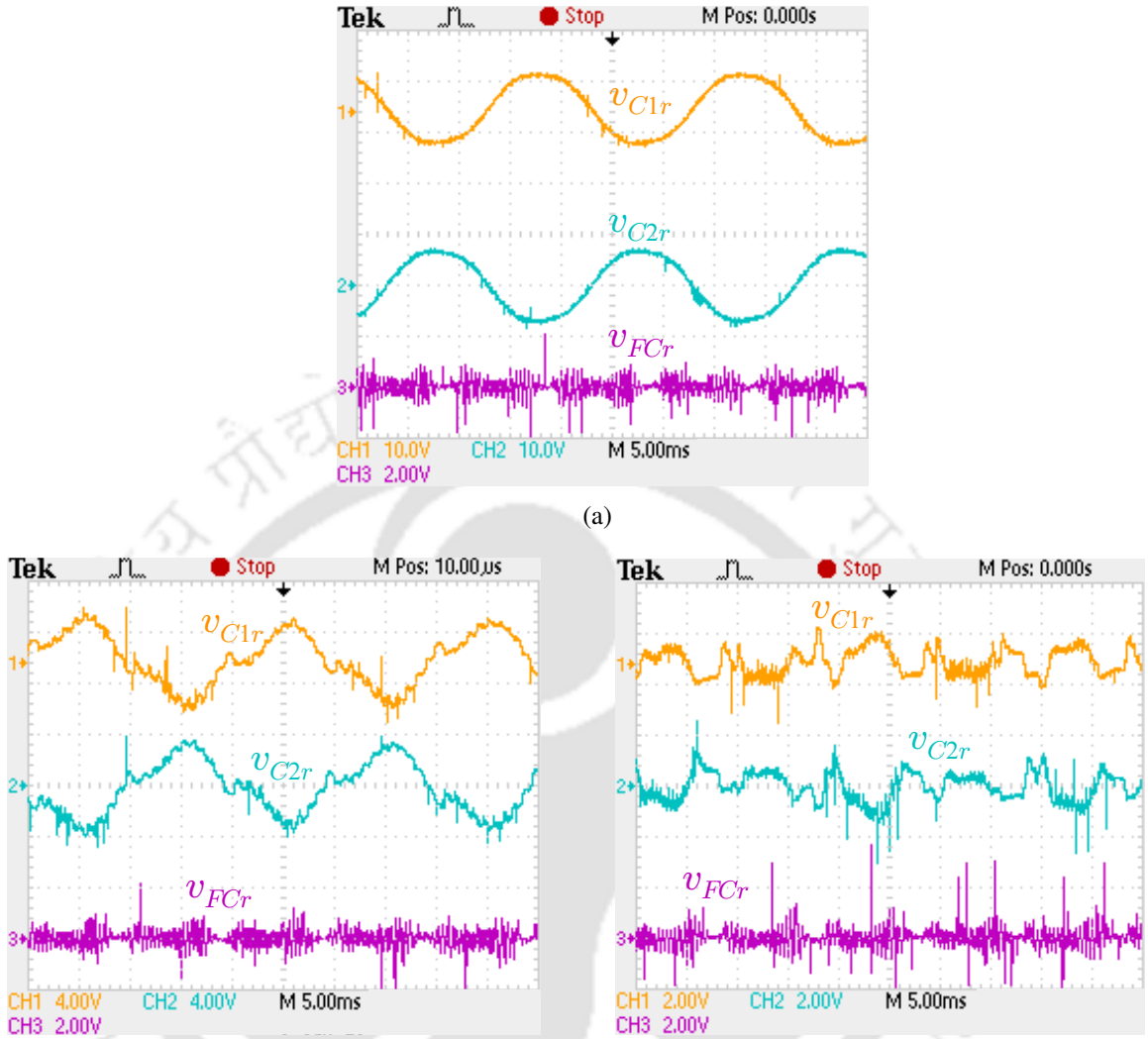


Fig. 4.14. The steady-state experimental waveforms for ripple in voltages of C_1, C_2, and FC with parameters given in Case M-2, $M = 0.9$ and 3.8 Ω load: (a) ANPCI without chopper (b) chopper integrated ANPCI with multi-pulse based discontinuous chopper current control scheme (c) chopper integrated ANPCI with multi-pulse based continuous chopper current control scheme.

M-2. Figs. 4.13 and 4.14 depict the experimental waveforms for the voltage ripple in the DC-link capacitors and FC. Figs. 4.13(a) and 4.14(a) show the waveforms for ANPCI without chopper. For the chopper integrated ANPCI, Figs. 4.13(b) and 4.14(b) show the waveforms using multi-pulse based discontinuous chopper current control scheme, whereas, Figs. 4.13(c) and 4.14(c) show the waveforms using the multi-pulse based continuous chopper current control scheme. The peak-to-peak voltage ripple for the waveforms shown in Figs. 4.13 and 4.14 are listed in Table 4.6. Here, ΔV_C and ΔV_{FC} are the peak-to-peak val-

Table 4.6. EXPERIMENTAL RESULTS FOR ANPCI AND CHOPPER INTEGRATED ANPCI WITH P-P RIPPLE IN v_{C1} AND v_{FC}

P-P voltage ripple	Case M-1			Case M-2		
	Fig. 4.13(a)	Fig. 4.13(b)	Fig. 4.13(c)	Fig. 4.14(a)	Fig. 4.14(b)	Fig. 4.14(c)
ΔV_C	4.8 V (15%)	3.6 V (11.25%)	1.8 V (5.63%)	14 V (43.75%)	8 V (25%)	2.8 V (8.75%)
ΔV_{FC}	0.8 V (5%)	0.8 V (5%)	0.8 V (5%)	0.8 V (5%)	0.8 V (5%)	0.8 V (5%)

ues of v_{C1r} and v_{FCr}, respectively. From the results given in this table, it can be noted that with the low values of capacitors, the peak-to-peak ripple in v_{C1} is reduced to 2.8 V by the use of chopper circuit with multi-pulse based continuous chopper current control scheme, where as this peak-to-peak ripple is 14 V and 4.8 V for the ANPCI (no chopper operation) with low values and high values of the DC-link capacitors, respectively.

In Fig. 4.15(a), the waveforms of v_{C1}, v_{FC}, v_{an} and i_o are shown for ANPCI (without chopper), the PWM voltage is skewed at the peaks and i_o is a distorted sinusoidal waveform. Fig. 4.15(b) shows the waveforms with chopper using multi-pulse based discontinuous chopper current control scheme, in which the extreme levels of PWM voltage are improved. The PWM voltage levels become flat using multi-pulse based continuous chopper current control scheme as shown in Fig. 4.15(c). Figs. 4.15(b) and 4.15(c), also show the FC voltage and variation of the i_{ch} with respect to the v_{C1}. It can be seen that the i_{ch} is continuously switching between 0 and $|I_{ch}^{Max}|$ using multi-pulse based discontinuous chopper current control scheme and sometimes it is continuously zero using multi-pulse based continuous chopper current control scheme. Fig. 4.16 shows the waveforms for chopper integrated ANPCI. Fig. 4.16(a) shows the load step change using multi-pulse based continuous chopper current control scheme. Here, the distortion less load voltages and currents are obtained. The DC-link capacitor voltages due to variation of the i_{ch} with respect to ON/OFF condition of switch S_9 are shown in Figs. 4.16(b) and 4.16(c) using multi-pulse based discontinuous chopper current control scheme and multi-pulse based continuous chopper current

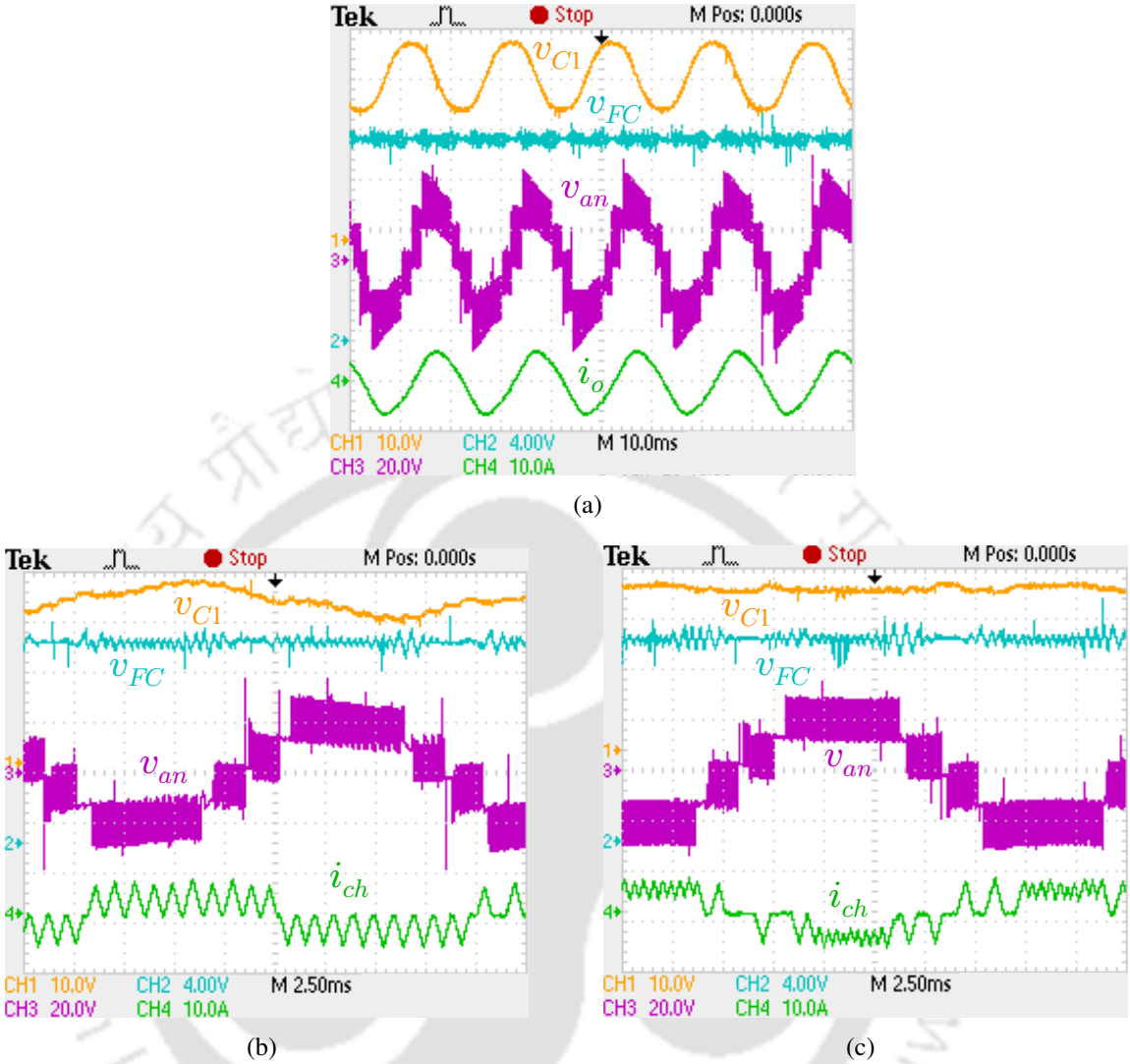


Fig. 4.15. The experimental waveforms with 3.8 Ω load and the parameters given in Case M-2: (a) ANPCI without chopper (b) chopper integrated ANPCI using multi-pulse based discontinuous chopper current control scheme (c) chopper integrated ANPCI using multi-pulse based continuous chopper current control scheme.

control scheme, respectively.

To verify operation of the hysteresis current control and hysteresis voltage control schemes for chopper integrated ANPCI, the parameters $M = 0.9$ and load resistance $R_L = 3.8\ \Omega$ are considered in addition to the parameters mentioned in Table 4.2 and Case M-2.

The ripples in voltages of C_1, C_2 and FC for the chopper integrated ANPCI are shown in Fig. 4.17(a) and (b) using hysteresis current control scheme and hysteresis voltage control scheme, respectively. The peak-to-peak ripple of v_{C1} and v_{C2} are observed as 3.6 V and 2 V using hysteresis current control method and hysteresis voltage control scheme,

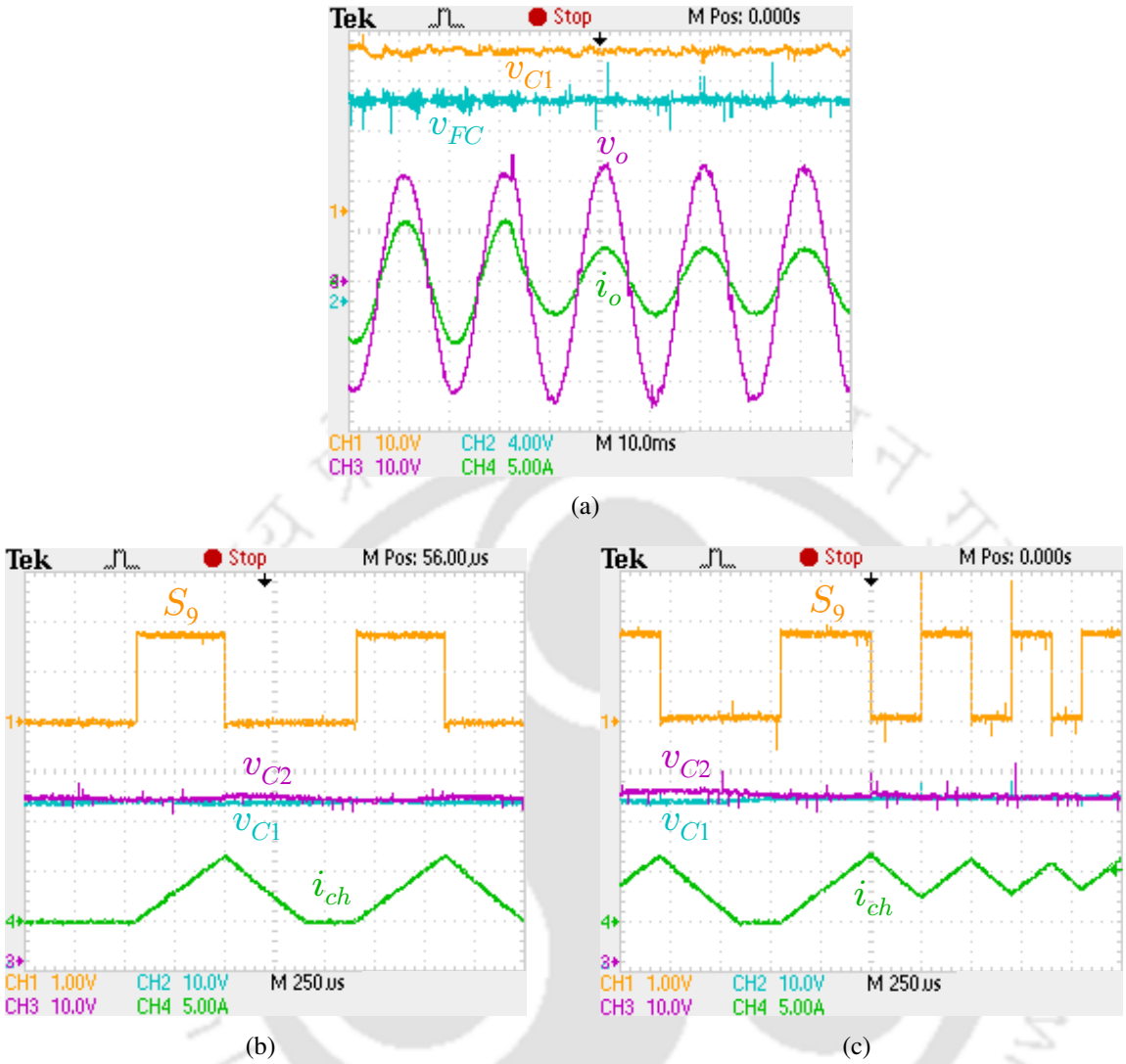


Fig. 4.16. The experimental waveforms with parameters given in Case M-2 for chopper integrated ANPCI using (a) multi-pulse based continuous chopper current control scheme with load step change from 3.8 Ω to 7.5 Ω (b) multi-pulse based discontinuous chopper current control scheme and (c) multi-pulse based continuous chopper current control scheme.

respectively.

Fig. 4.18(a), (b) and (c) shows the experimental results for the chopper integrated ANPCI using hysteresis voltage control scheme. Fig. 4.18(a) shows variation of the chopper current with respect to gate signal (G_{S10}) of the switch, S_{10}. It can be observed that the DC-link capacitor voltages are becoming equal as the chopper is operating. Fig. 4.18(b) shows the waveforms of v_{C1}, v_{FC}, v_{an} and i_{ch}. It can be seen that the chopper current is highly distorted. Fig. 4.18(c) shows the waveforms of v_{C1}, v_{FC}, v_{an} and i_o, in which a step-up change is given in M from 0.9 to 0.4 with $R_L = 3.8\ \Omega$. After the step change in M, the

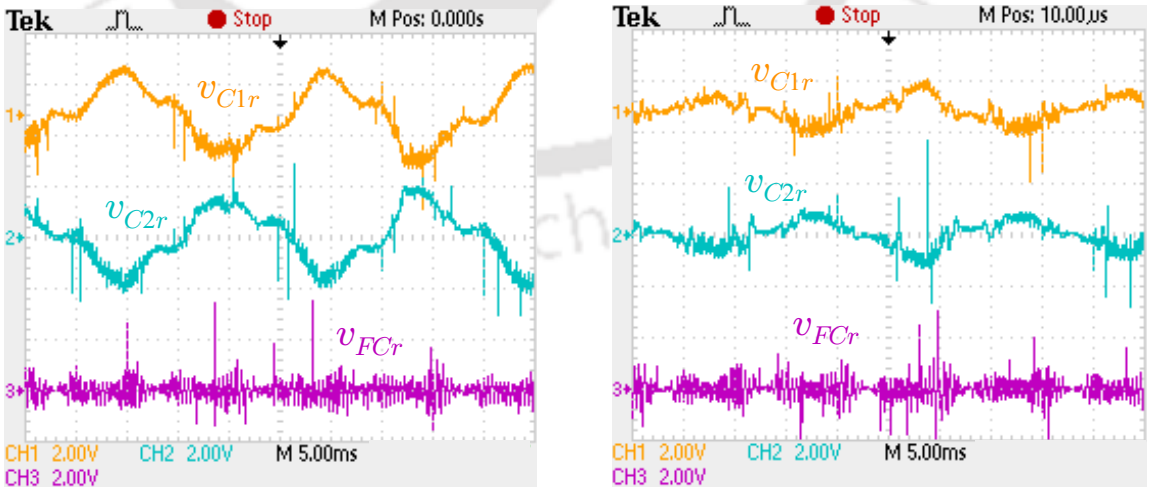
Table 4.7. DIFFERENT CASES CONSIDERED FOR THE EXPERIMENTAL VERIFICATION

Case	Is chopper integrated to ANPCI?	Chopper control scheme	SRF-dq-based load voltage controller is implemented?	Parameters♯		
				M	V_d^* (V)	R_L (Ω)
N-1	No	—	No	0.9	—	3.8
N-2	Yes	HCC	No	0.9	—	3.8
N-3	Yes	HCC	No	0.9	—	7.5
N-4	Yes	ACC	No	0.9	—	3.8
N-5	Yes	ACC	No	0.9	—	7.5
N-6	Yes	ACC	Yes	—	23	3.8
N-7	Yes	ACC	Yes	—	23	7.5

♯ All other parameters considered are listed in Table 4.2 and Case M-2 is considered; V_d^* is the peak of the reference load voltage (v_o^*).

waveform of v_{an} becomes a three-level waveform and load current i_o is reduced.

Table 4.7 lists various test cases: Case N-1 to Case N-7, considered along with the parameters mentioned in Case M-2 and Table 4.2 for the experimental verification of chopper integrated ANPCI using HCC and ACC schemes. The data obtained from the experiments are summarized in Table 4.8. The steady-state waveforms of ANPCI after integrating chopper circuit are shown in Fig. 4.19(a) with HCC (Case N-2) and in Fig. 4.19(b) with ACC



(a) (b)

Fig. 4.17. Steady-state experimental waveforms for ripple in voltages of C_1, C_2 and FC, with 3.8 Ω load: (a) chopper integrated ANPCI using hysteresis current control scheme (b) chopper integrated ANPCI using hysteresis voltage control scheme.

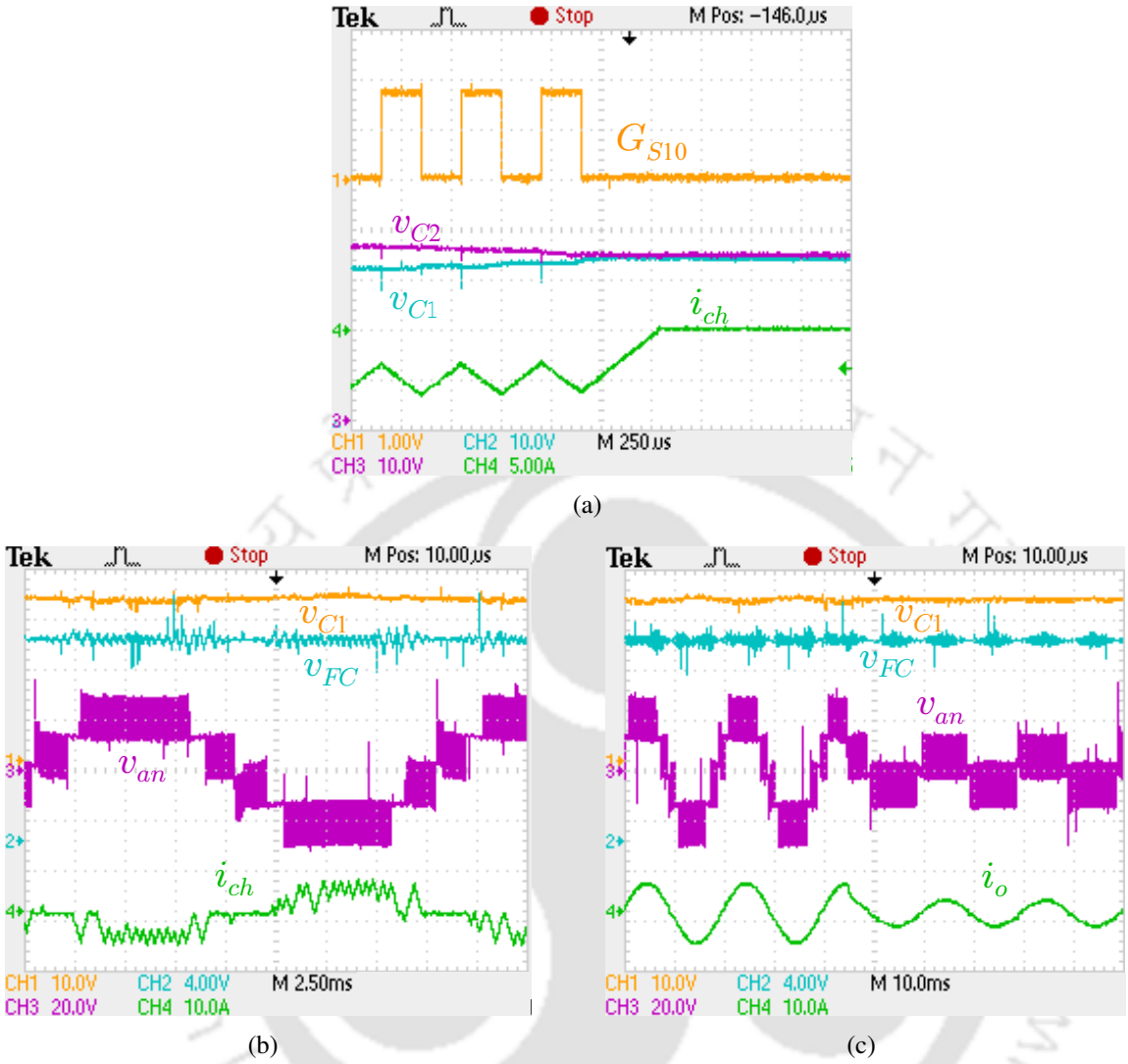


Fig. 4.18. The experimental waveforms of chopper integrated ANPCI using hysteresis voltage control scheme: (a) variation of chopper inductor current with respect to the gate pulse (G_{S10}) of switch S_{10} for 3.8 Ω load (b) steady-state waveforms for 3.8 Ω load and (c) step change in the modulation index from 0.9 to 0.4 with 3.8 Ω load.

(Case N-4).

The performance of chopper integrated ANPCI with load step change from 7.5 Ω to 3.8 Ω is shown in Fig. 4.20(a) using HCC (Cases N-2 and N-3) and Fig. 4.20(b) using ACC (Cases N-4 and N-5). It can be observed from Figs. 4.19 and 4.20, and Table 4.8 that the ripple in v_{C1} is reduced to 3.6 V with HCC and 2 V with ACC. This also results in better PWM voltage of ANPCI compared to the case of ANPCI without chopper circuit presented in Fig. 4.15(a). Thus, it can be seen that the proposed integration of external chopper circuit is successful in reducing the DC-link capacitor voltage ripples of ANPCI.

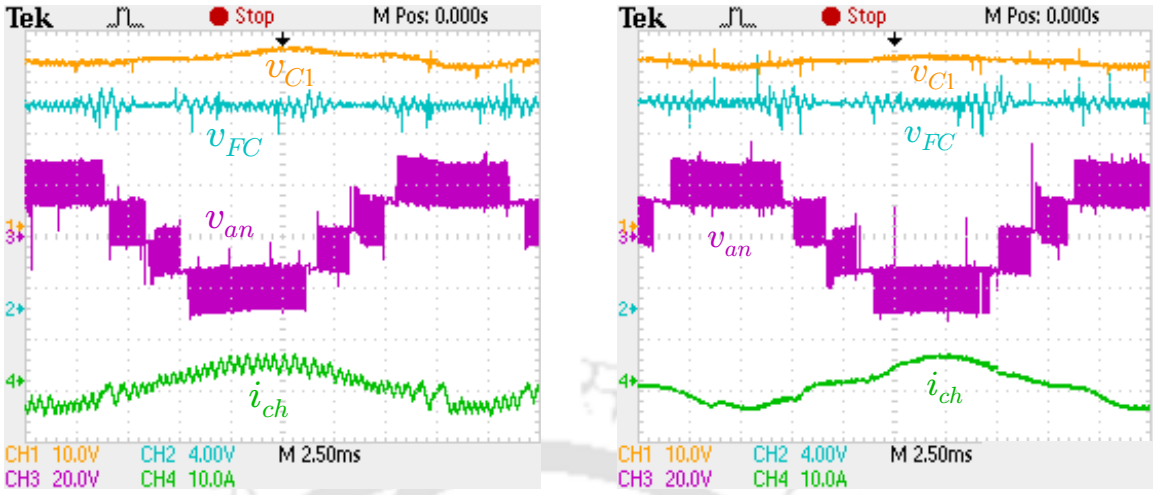


Fig. 4.19. Steady-state waveforms for (a) ANPCI with chopper integration using HCC (Case N-2) (b) ANPCI with chopper integration using ACC (Case N-4).

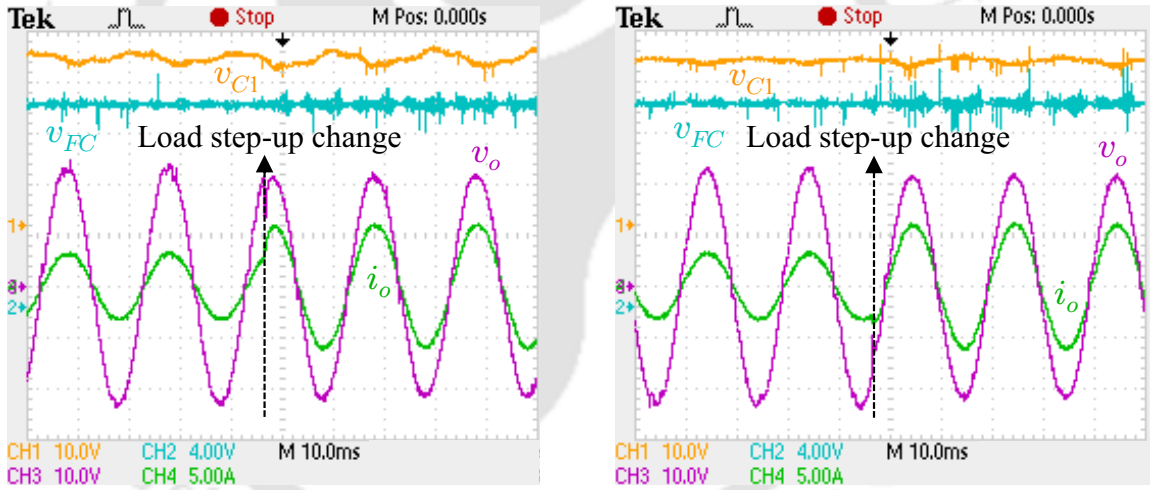
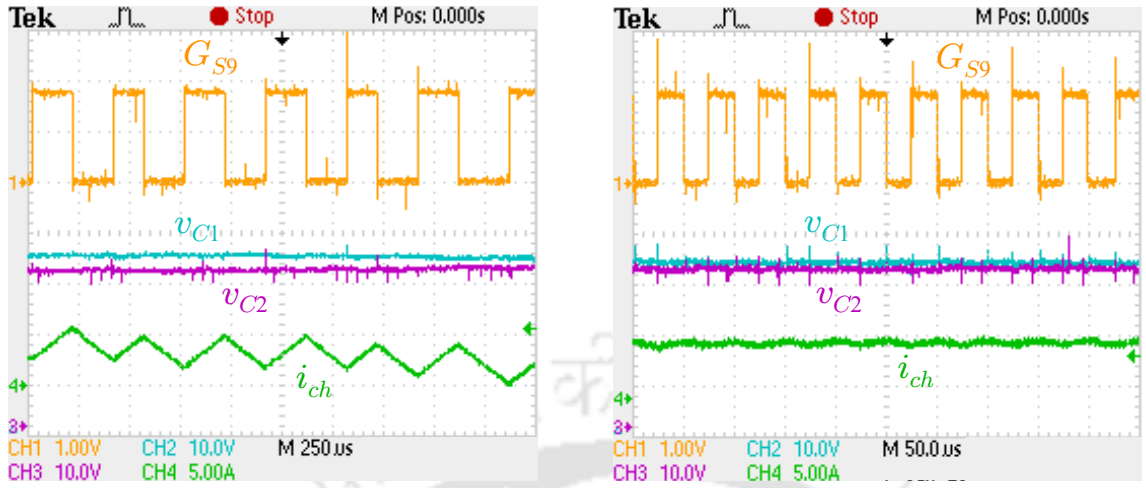


Fig. 4.20. Performance of chopper integrated ANPCI with step change in the load from 7.5 Ω to 3.8 Ω: (a) HCC (Cases N-2 and N-3) (b) ACC (Cases N-4 and N-5).

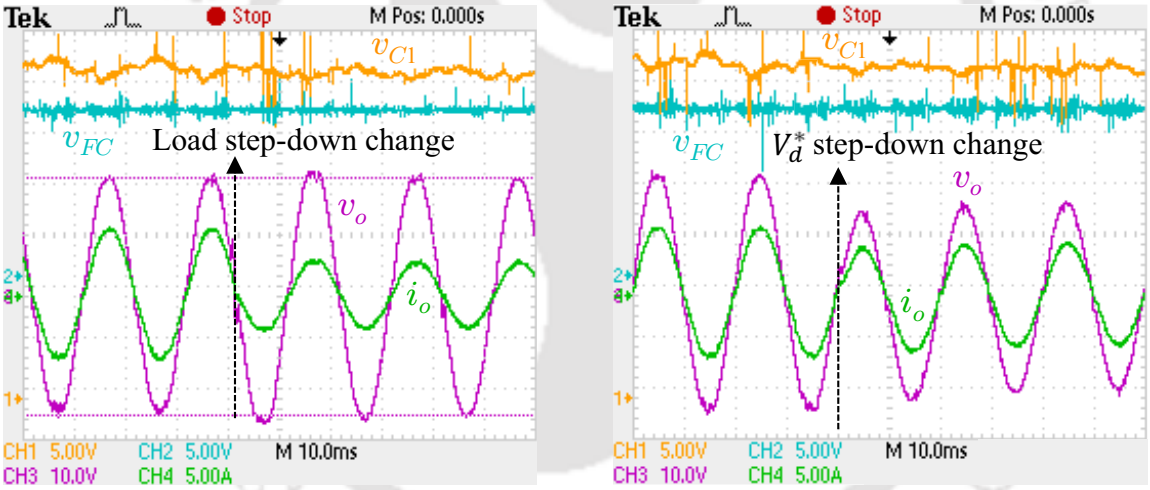
Fig. 4.21(a) and (b) shows the gate signal G_{S9} of the chopper circuit generated using HCC and ACC, respectively. It can be observed that with HCC, the switching frequency of the chopper switches continuously varies, while it is constant with ACC. Also, the ripple reduction with ACC based chopper circuit is more than the ripple reduction achieved with the HCC based chopper circuit.

To regulate the load voltage of chopper integrated ANPCI, SRF-dq-based load voltage controller [29] is developed and the corresponding results are presented in Fig. 4.22



(a) (b)

Fig. 4.21. Steady-state waveforms for variation of chopper current and DC-link capacitor voltages with respect to gate signal of S_9, i.e., G_{S9} (a) HCC (Case N-2) (b) ACC (Case N-4).



(a) (b)

Fig. 4.22. Waveforms of chopper integrated ANPCI with SRF-dq-based load voltage controller: (a) step change in R_L from 3.8 Ω (Case N-6) to 7.5 Ω (Case N-7) (b) step change in V_d^* from 23 to 18 V.

(Case N-6 and Case N-7). Only ACC based chopper circuit is considered here due to its superior performance compared to HCC. From Fig. 4.22(a), it can be seen that the output voltage is accurately tracking the reference voltage, v_o^*, which is $V_d^* \cdot \sin(\omega_o t)$, against the step-change in the load resistance from 3.8 to 7.5 Ω. Also, the peak output voltage, v_d, is following the step-change in V_d^* from 23 to 18 V as shown in Fig. 4.22(b). Even with load voltage control, the chopper circuit is maintaining significantly less ripple in v_{C1}, which can be seen from Fig. 4.22 and Table 4.8. These results confirm the effectiveness of SRF-dq-

Table 4.8. VOLTAGE RIPPLES, AND PEAK VALUES OBTAINED FROM THE EXPERIMENT

Case	Figure	ΔV_C		ΔV_{FC}		$\hat{v}_{an}$	v_d	$\hat{i}_o$
		(V)	(%)	(V)	(%)	(V)	(V)	(A)
N-1	Fig. 4.15(a)	14	43.75	1.6	10	23.33	22.27	6.19
N-2	Fig. 4.20(a)	3.6	11.25	1.6	10	23.27	21.96	6.06
N-3	Fig. 4.20(a)	3	9.37	0.8	5	24.36	23.38	3.21
N-4	Fig. 4.20(b)	2	6.25	1.6	10	23.23	21.82	6.05
N-5	Fig. 4.20(b)	1	3.12	0.8	5	23.77	23.25	3.2
N-6	Fig. 4.22(a)	2	6.25	1.6	10	24.15	22.98	6.31
N-7	Fig. 4.22(a)	1.6	5	0.8	5	23.07	23.03	3.13

Note: $\hat{v}_{an}$, v_d, and $\hat{i}_o$ are the peak values of the fundamental component of v_{an}, v_o, and i_o, respectively.

based load voltage controller and the external chopper circuit presented in this thesis.

4.5 SUMMARY

This chapter has discussed integration of external chopper circuit to the DC-link of five-level ANPCI for reduction of ripple in the DC-link capacitor voltages. A capacitor voltage balancing strategy is implemented and it could maintain the constant FC voltage for the ANPCI. The control and operation of single-phase chopper based five-level ANPCI are presented to reduce the ripple of DC-link capacitor voltages. The ripple in DC-link capacitor voltages is reduced by implementing six chopper control methods. These chopper control techniques are described and implemented using the PSCAD/EMTDC simulation. Due to the large starting current of the chopper inductor, single-pulse based chopper current control scheme is not recommended for hardware implementation. All the control schemes except single-pulse control scheme are implemented on the hardware using TMS320F28335 DSC kit, and their performance is compared. For the test case considered in the simulation, the DC-link capacitor voltage ripple has reduced from 130.1 V for ANPCI without chopper to 5.76 V for ANPCI with chopper circuit. Also, for the test case considered in the experiment, the DC-link capacitor voltage ripple has reduced from 14 V for ANPCI without chopper to 2 V for ANPCI with chopper circuit. The performance of the chopper integrated AN-

PCI is also verified with SRF-dq-based load voltage control. The results confirm that the proposed integration of chopper circuit and the controllers are successful in regulating the DC-link capacitor voltages and the load voltage of ANPCI. From the analysis presented and the experimental results obtained, it can be concluded that the proposed chopper circuit along with the CCM based average current control technique is effective in reducing ripple in the DC-link capacitor voltages. This further improves the quality of output voltage and current waveforms of the converter and also helps in reducing the values of DC-link capacitors, thereby increasing the power density of the single-phase, five-level ANPCI.

CHAPTER 5

APPLICATION OF ANPCI IN SOLAR AND WIND POWER GENERATION SYSTEMS

5.1 INTRODUCTION

In Chapter 1, a brief review of the three classical MLIs, viz., NPC-MLI, FC-MLI, and CHB-MLI as well as ANPCI is discussed. In Chapter 2, detailed operation and steady-state analysis of single-phase five-level ANPCI are presented. The performance of four different PWM techniques and four different Capacitor Voltage Balancing Strategies (CVBS) is compared for five-level ANPCI. Further, an SRF-dq controller is presented and implemented for the single-phase ANPCI. Finally, various CVBS and the SRF-dq controller operation are verified using the demonstrated results. Chapter 3 has presented a dynamic average circuit model of the ANPCI. Chapter 4 has discussed integration of external chopper circuit to the DC-link of five-level ANPCI for reduction of ripple in the DC-link capacitor voltages using various chopper control methods. Finally, the performance of all the chopper control schemes and SRF-dq-based load voltage controller is verified for the chopper integrated ANPCI.

In this chapter, the operation of chopper integrated ANPCI as a dc-to-ac converter interface in a Solar Power Generation System (SPGS) and Wind Power Generation System (WPGS) is presented. Both SPGS and WPGS are operated in grid connected mode. Both the active and reactive powers injected into the grid are controlled using a Second Order Generalized Integrator- Phase Locked Loop (SOGI-PLL) and an SRF-dq current controller. Further Maximum Power Point Tracking (MPPT) algorithm is implemented for both SPGS

and WPGS. Also the performance of both the systems is compared with and without integration of chopper circuit to the ANPCI.

This chapter is organized into four sections. Section 5.2 operation and control of SPGS using chopper integrated ANPCI as dc-to-ac converter interface are discussed. The PSCAD/EMTDC simulation results are also presented with and without chopper circuit integration to ANPCI in the SPGS. Section 5.3 operation and control of WPGS using chopper integrated ANPCI as dc-to-ac converter interface are discussed. The simulation results are presented with and without chopper circuit integration to ANPCI in the WPGS. Finally, Section 5.4 summarizes this chapter.

5.2 OPERATION AND CONTROL OF SPGS USING CHOPPER INTEGRATED ANPCI

5.2.1 Description of the System

Fig. 5.1 shows the block diagram of a SPGS connected to a single-phase distribution grid. This system consists of a solar PV array connected to the distribution grid through a boost converter, a dc-to-ac converter and a step-up transformer. The solar PV array consists

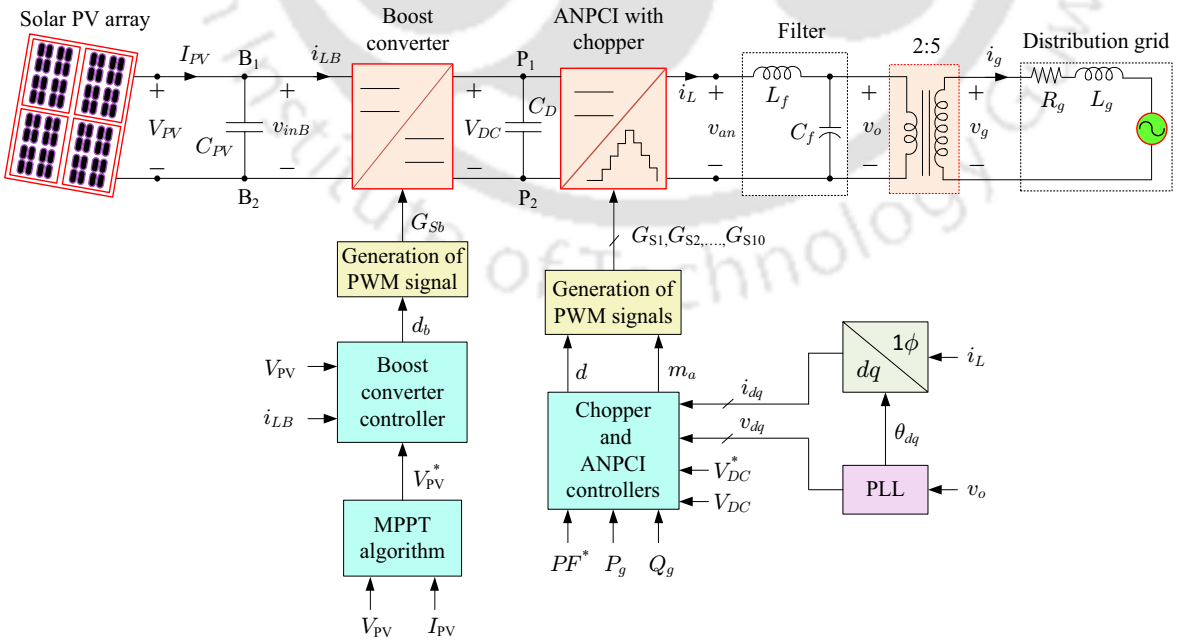


Fig. 5.1. Block diagram of SPGS with single-phase weak distribution grid connected ANPCI.

of several individual panels connected in series and parallel combinations. The output power of the solar PV array depends on the weather conditions, i.e., solar irradiation and temperature. The boost converter is used to operate the solar PV array at its maximum power point for any weather condition using an MPPT algorithm. The output of the boost converter is the DC-link voltage, V_{DC}, which is maintained as constant by the dc-to-ac converter. The real and reactive powers injected into the grid are also controlled by the dc-to-ac converter using an SRF-dq current controller.

In literature, different dc-to-ac converter topologies are used to interface the SPGS to the utility grid [121–125]. The dc-to-ac converter topology can be a two-level inverter or a multi-level inverter. In [121], a three-level T-type NPC inverter is used as a dc-to-ac interface in the SPGS, whereas in [122, 123], a cascaded H-bridge multilevel inverter is used. In [124], a five-level Current Source Inverter (CSI) is used for high power inversion with inherent voltage boosting, and thus, avoids the usage of transformer. In [125], a four leg CSI is used. Multi-level VSIs are familiar for their features such as reduced voltage stress, more efficiency, low THD, low filter requirement and high power transfer capability [11]. In this chapter, the five-level chopper integrated ANPCI is proposed as a dc-to-ac converter interface due to the advantages mentioned in the previous chapters. Due to the integration of the chopper circuit in ANPCI, the ripple in DC-link capacitor voltages is reduced, hence the quality of the grid injected current improves. An LC filter is used at the output of the ANPCI to filter the harmonics in the grid injected current. The grid considered here is a weak distribution grid with a Short Circuit Ratio (SCR) of 6.68 [126, 127].

The detailed description of different blocks in the SPGS of Fig. 5.1 is given below.

A) Solar PV array with MPPT

A solar PV array converts available solar energy on its surface into the electrical energy using photovoltaic effect. The terminal voltage and current of the PV array vary when its surface is affected by fluctuation in the weather conditions such as solar irradiation and temperature. Hence, to operate the solar PV array in wide voltage range, the dc-to-dc boost converter is used that converts the generated power into usable form [109,128]. The solar PV

array shown in Fig. 5.1 consists of four parallel connected strings with each string having eight series connected KC200GT solar PV panels. Each solar PV panel has open circuit voltage (V_{OC}) of 32.9 V and short circuit current (I_{SC}) of 8.21 A [109]. The circuit model of the solar PV panel used to simulate the system is shown in Fig. 5.2. The corresponding mathematical model of the PV panel is given by (5.1)−(5.4).

$$I_{PV} = I_{PVC} - I_o \left[\exp\left(\frac{V_{PV} + R_{se} I_{PV}}{a_d V_t}\right) - 1\right] - \left(\frac{V_{PV} + R_{se} I_{PV}}{R_p}\right) \tag{5.1}$$

$$I_{PVC} = \left(I_{PVC,n} + K_I \Delta_T\right) \frac{G}{G_n} \tag{5.2}$$

where I_{PVC} and I_o are the photovoltaic and saturation currents, respectively, of the solar PV array. $I_{PVC,n}$ is the nominal light generated current and V_t is the thermal voltage of the solar PV array with n_s cells connected in series. The expression for V_t is given by

$$V_t = \frac{n_s k_b T_K}{q} \tag{5.3}$$

where T_K is the temperature in Kelvin. The expression for I_o is given by

$$I_o = \frac{I_{SC,n} + K_I \Delta_T}{\exp\left(\frac{V_{OC,n} + K_V \Delta_T}{a_d V_t}\right) - 1} \tag{5.4}$$

Also, Δ_T is given by

$$\Delta_T = T - T_n \tag{5.5}$$

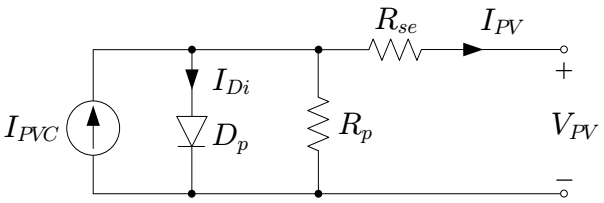


Fig. 5.2. Circuit model of the PV array.

Table 5.1. PARAMETERS OF KC200GT SOLAR PV PANEL AT NOMINAL IRRADIATION AND TEMPERATURE

Parameters	Attributes
Boltzmann constant (k_b)	1.3806503×10^{-23} $\frac{\text{J}}{\text{K}}$
Electron charge (q)	1.60217646×10^{-19} C
Current coefficient (K_I)	0.0032 $\frac{\text{A}}{\text{K}}$
Voltage coefficient (K_V)	-0.123 $\frac{\text{V}}{\text{K}}$
Series connected cells (n_s)	54
Series resistance (R_{se})	0.221 Ω
Parallel resistance (R_p)	415.405 Ω
Degree of ideality of the diode (a_d)	1.3
Nominal light generated current ($I_{PVC,n}$)	8.214 A
Nominal diode saturation current ($I_{o,n}$)	98.25 nA
Nominal irradiation (G_n)	1000 $\frac{\text{W}}{\text{m}^2}$
Nominal temperature (T_n)	25 °C
Open circuit voltage of PV panel ($V_{OC,n}$)	32.9 V
Short circuit current of PV panel ($I_{SC,n}$)	8.21 A
PV panel output voltage at MPP (V_{MPP})	26.3 V
PV panel output current at MPP (I_{MPP})	7.61 A
PV panel output power at MPP (P_{MPP})	200.14 W

where T and T_n are the actual and nominal temperatures in °C. The parameters used in Fig. 5.2 and (5.1)−(5.4) are defined in Table 5.1.

Figs. 5.3 and 5.4 show the I_{PV} vs. V_{PV} and P_{PV} vs. V_{PV} characteristics of the combined solar PV array for change in irradiation (G) with constant temperature (T). From the characteristics of Fig. 5.3, it is observed that with increase in the irradiation, V_{OC} slightly increases whereas I_{SC} significantly increases. From the characteristics of Fig. 5.4, it is observed that with increase in the irradiation, V_{MPP} slightly increases whereas I_{MPP} and P_{MPP} significantly increases. Figs. 5.5 and 5.6 show the I_{PV} vs. V_{PV} and P_{PV} vs. V_{PV} characteristics of the combined solar PV array for change in temperature with constant irradiation. From the characteristics of Fig. 5.5, it is observed that with increase in the temperature, V_{OC} significantly decreases whereas I_{SC} slightly increases. From the characteristics of Fig. 5.6, it is observed that with increase in the temperature, V_{MPP} significantly

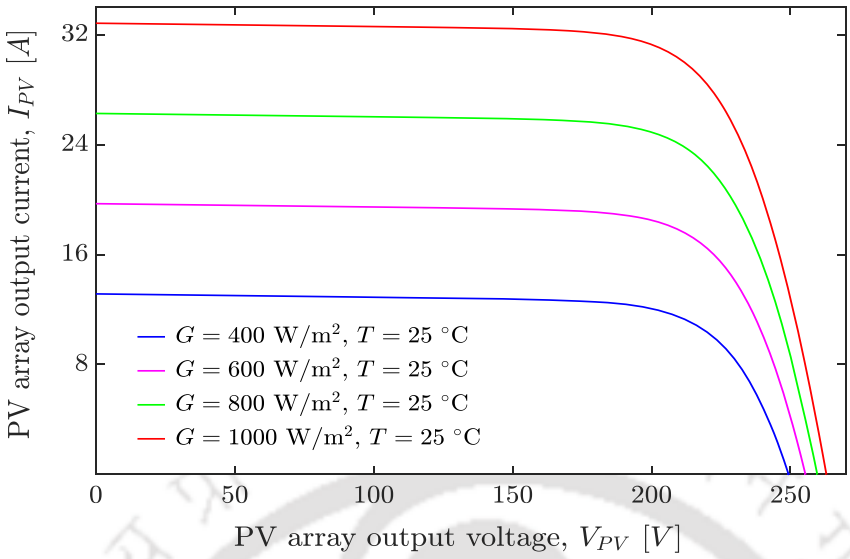


Fig. 5.3. I_{PV} vs. V_{PV} characteristics of the solar array with constant temperature and change in irradiation.

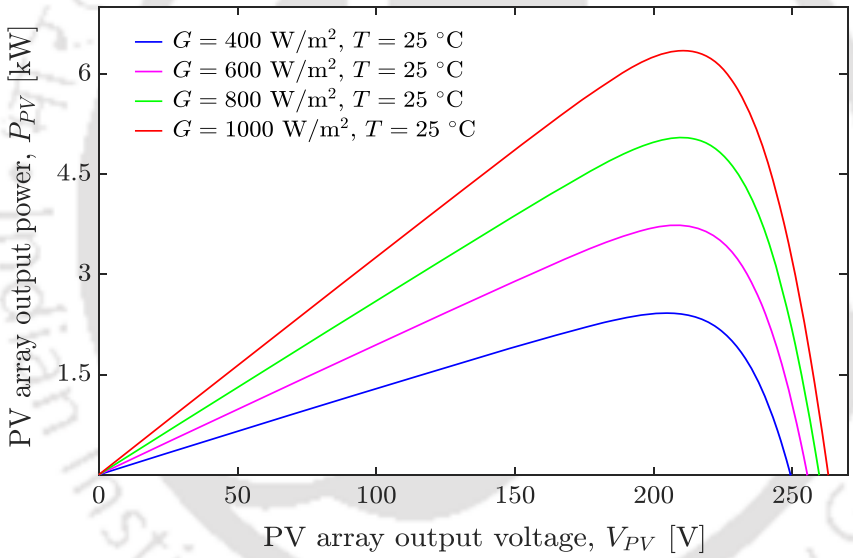


Fig. 5.4. P_{PV} vs. V_{PV} characteristics of the solar array with constant temperature and change in irradiation.

decreases, I_{MPP} slightly decreases and P_{MPP} significantly decreases. In Table 5.2, the maximum power point $(V_{MPP}, I_{MPP}, P_{MPP})$, open circuit voltage (V_{OC}) and short circuit current (I_{SC}) values obtained from these curves are also mentioned.

From the characteristics shown in Figs. 5.3−5.6 and the results given in Table 5.2, it can be observed that the power supplied by the PV array depends on the weather conditions. To extract the maximum available power from the PV array, an MPPT algorithm is required. In this work, Perturbation and Observation (P&O) based MPPT algorithm is utilized for the maximum power extraction from the PV array. The flowchart of an MPPT algorithm is

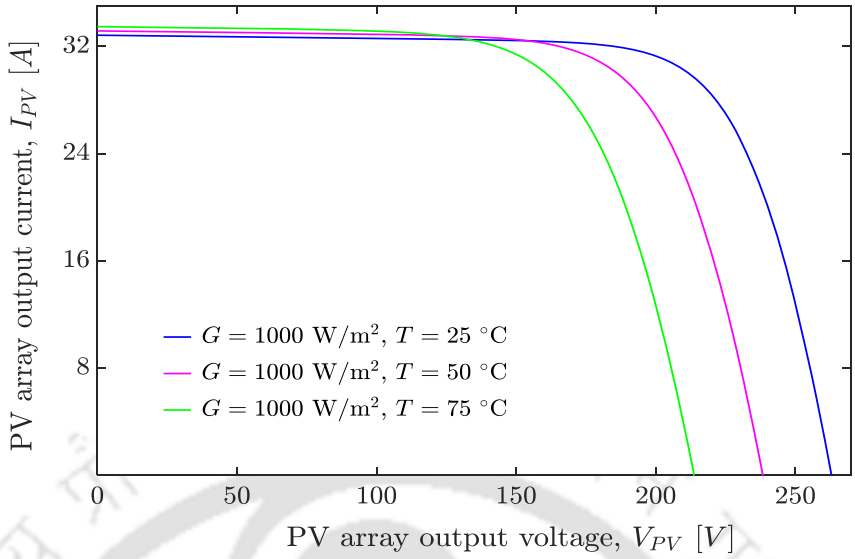


Fig. 5.5. I_{PV} vs. V_{PV} characteristics of the solar array with constant irradiation and change in temperature.

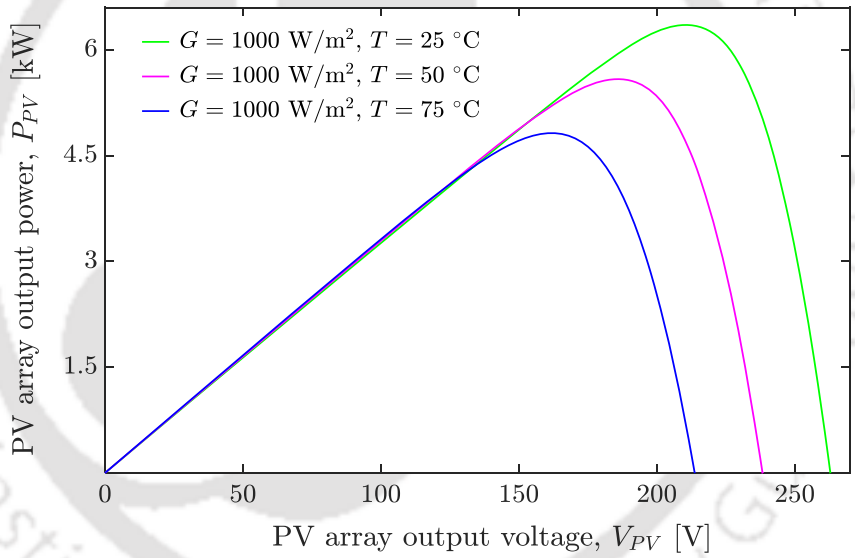


Fig. 5.6. P_{PV} vs. V_{PV} characteristics of the solar array with constant irradiation and change in temperature.

shown in Fig. 5.7 [129]. In this figure, $V_{PV}(k)$ and $I_{PV}(k)$ represent the PV array output voltage and current, respectively, at k^{th} sampling instant. Also, $P_{PV}(k)$, $\triangle P_{PV}$, $\triangle V_{PV}$ are given by

$$P_{PV}(k) = V_{PV}(k) I_{PV}(k) \tag{5.6}$$

$$\triangle P_{PV} = P_{PV}(k) - P_{PV}(k-1) \tag{5.7}$$

$$\triangle V_{PV} = V_{PV}(k) - V_{PV}(k-1) \tag{5.8}$$

Table 5.2. MAXIMUM POWER POINT (MPP), V_{OC}, AND I_{SC} OF THE PV-CURVES SHOWN IN FIGS. 5.3–5.6

Parameters	V_{OC}	I_{SC}	Maximum power points		
			V_{MPP}	I_{MPP}	P_{MPP}
$G = 400 \frac{\text{W}}{\text{m}^2}$ and $T = 25$ °C	249.31 V	13.13 A	204.74 V	11.82 A	2.42 kW
$G = 600 \frac{\text{W}}{\text{m}^2}$ and $T = 25$ °C	255.38 V	19.7 A	208.13 V	17.95 A	3.74 kW
$G = 800 \frac{\text{W}}{\text{m}^2}$ and $T = 25$ °C	259.64 V	26.27 A	209.81 V	24.07 A	5.05 kW
$G = 1000 \frac{\text{W}}{\text{m}^2}$ and $T = 25$ °C	262.92 V	32.84 A	210.74 V	30.15 A	6.35 kW
$G = 1000 \frac{\text{W}}{\text{m}^2}$ and $T = 50$ °C	238.33 V	33.16 A	185.92 V	30.06 A	5.59 kW
$G = 1000 \frac{\text{W}}{\text{m}^2}$ and $T = 75$ °C	213.75 V	33.47 A	161.8 V	29.79 A	4.82 kW

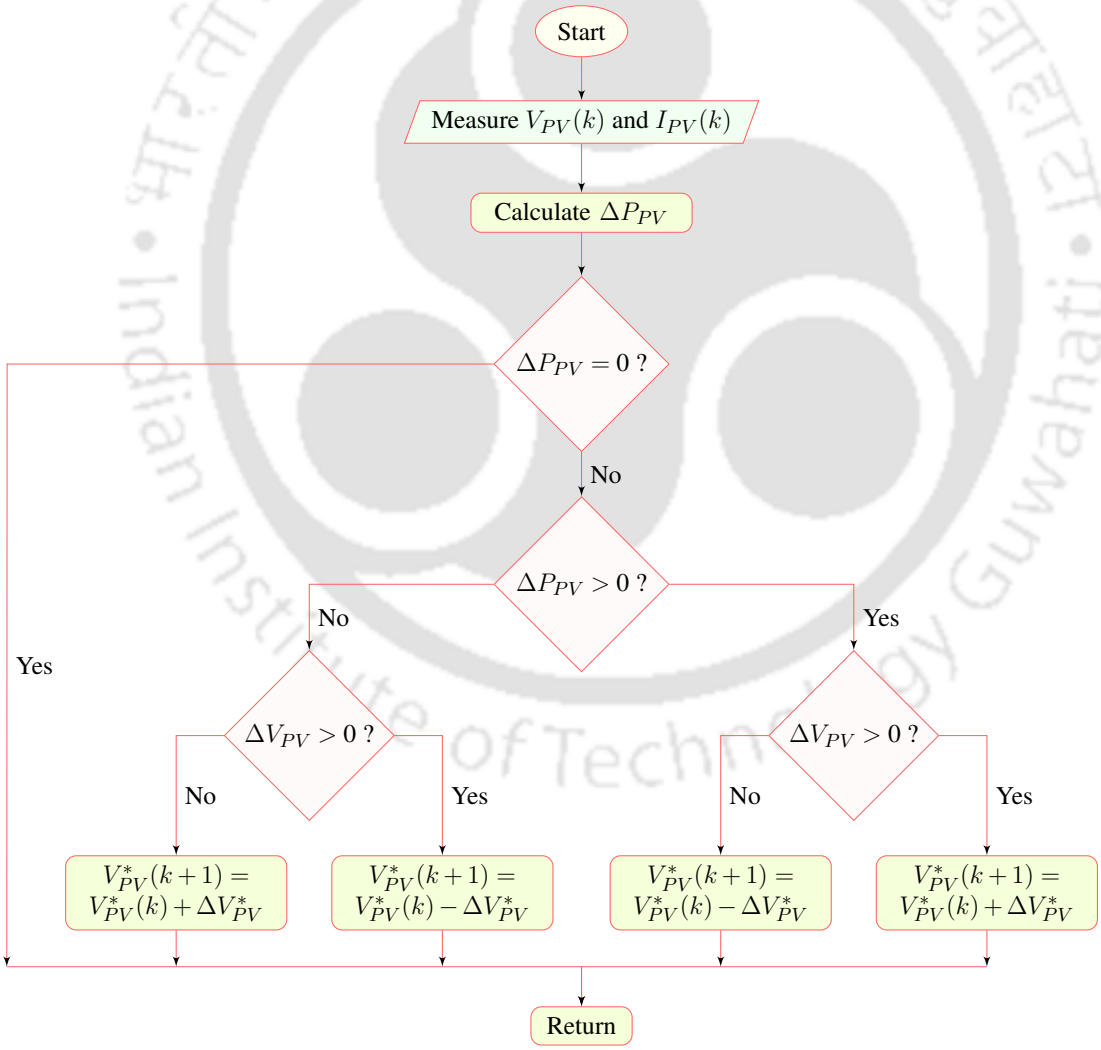


Fig. 5.7. Flowchart representing the MPPT algorithm for solar PV array.

The MPPT algorithm decides the reference PV terminal voltage for the next sampling instant $V^*_{PV}(k+1)$, which will be given as input to the boost converter controller. Note that $\triangle V^*_{PV}$ is the change in V^*_{PV} from k^{th} sampling instant to the $(k+1)^{\text{th}}$ sampling instant.

B) Boost Converter and its Control

Once the reference terminal voltage (V^*_{PV}) is obtained from the MPPT algorithm, the terminal voltage of PV array (V_{PV}) is regulated to V^*_{PV} using a boost converter shown in Fig. 5.8 and its closed-loop control algorithm described in Fig. 5.9. The boost converter also steps-up the PV output voltage, V_{PV} to the DC-link voltage V_{DC}. The relation between V_{PV} and V_{DC} is given by

$$\frac{V_{DC}}{V_{PV}} = \frac{1}{1-d_b} \tag{5.9}$$

The control block diagram shown in Fig. 5.9 calculates the error between V^*_{PV} and V_{PV}. This error is then fed to a PI controller to generate current reference i^*_{LB} for the inductor current, i_{LB}. The error between i^*_{LB} and i_{LB} is calculated and fed to another PI controller to generate the duty signal, d_b. Further this duty signal is compared with the sawtooth signal to generate the gate signal, G_{Sb}, which controls the switch S_b of the boost converter.

C) Chopper Integrated ANPCI

Fig. 5.10 shows the detailed circuit diagram of chopper integrated ANPCI. In SPGS, the chopper integrated ANPCI is proposed as a dc-to-ac converter interface between

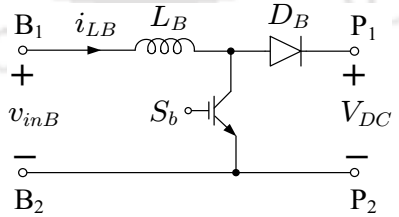


Fig. 5.8. Circuit diagram of the boost converter.

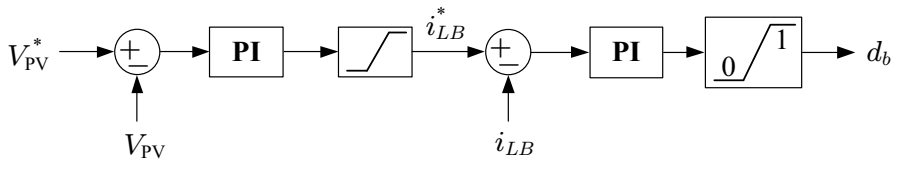


Fig. 5.9. Block diagram to control terminal voltage of the PV array.

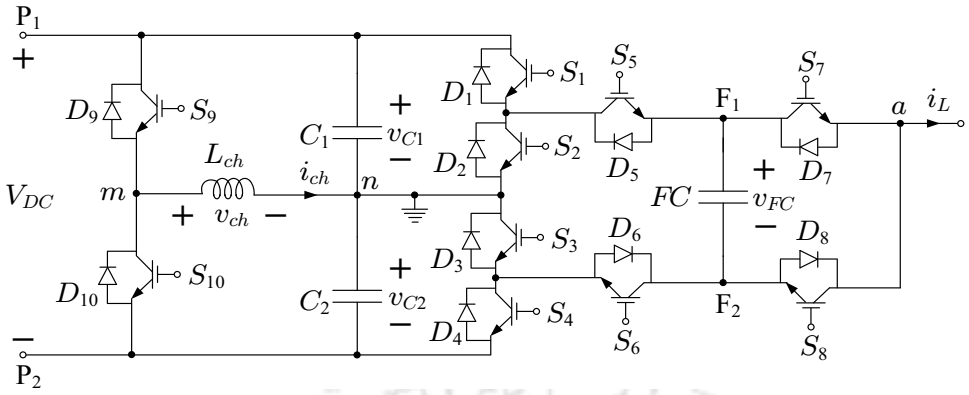


Fig. 5.10. Circuit diagram of the chopper integrated ANPCI.

the dc-to-dc boost converter and the weak distribution grid. Hence the input voltage of the chopper integrated ANPCI is V_{DC} and its output voltage is the five-level PWM waveform, v_{an}. The relation between the fundamental component of v_{an} and V_{DC} is given by

$$v_{an1} = m_a \cdot \frac{V_{DC}}{2} = M \cdot \sin\left(\omega_o^E t\right) \cdot \frac{V_{DC}}{2} \tag{5.10}$$

where ω_o^E is the grid frequency calculated by the PLL block. An LC filter is used at the output of the ANPCI to suppress the switching frequency components in v_{an}. A step-up transformer with turns ratio 2:5 is used to step-up the ANPCI voltage to the grid voltage. The main objective of chopper integrated ANPCI in SPGS is to regulate the real and reactive powers transferred to the grid using the control scheme, which will be explained in the subsequent paragraphs. In addition, the DC-link voltage is also regulated to V_{DC}^* by the chopper integrated ANPCI. The detailed explanation for operation and control of the stand-alone ANPCI and with its chopper integration is given in Chapters 2 and 4. As discussed in Chapter 4, ripple in the DC-link capacitor voltages of the ANPCI affects its output voltage adversely by introducing lower-order harmonics. Even though LC filter is connected after ANPCI, it can only suppress the high frequency harmonics. In SPGS, the chopper circuit integration to ANPCI can reduce the ripple in the DC-link capacitor voltages thereby THD in the current injected into the grid reduces. Further, it facilitates reduction of the DC-link capacitor values there by power density and reliability of the SPGS increases. The operation and control of

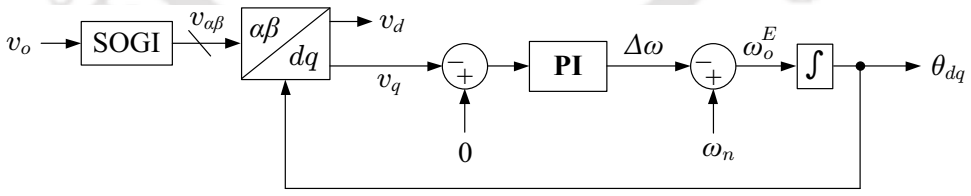
chopper integrated to ANPCI is same as described in Section 4.2.

D) SOGI-PLL

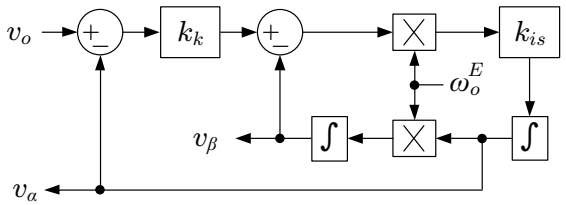
The main objective of the SOGI-PLL is to calculate the phase angle, θ_{dq} of the grid voltage and to calculate its dq domain components v_d and v_q. Note that for the control purpose, the transformer here is assumed as ideal and the waveform of v_o is used as the grid voltage. The block diagram of the SOGI-PLL is shown in Fig. 5.11 in which Fig. 5.11(a) shows the PLL and Fig. 5.11(b) shows voltage SOGI. The SOGI-PLL is used in SPGS to calculate the grid frequency as ω_o^E (rad/s). In Fig. 5.11(b), k_k is the constant and k_{is} is the gain of integrator. The voltage SOGI produces in-phase and quadrature components of v_o, i.e., v_α and v_β, respectively. As shown in Fig. 5.11(a), these $\alpha\beta$-domain signals are then transformed into dq reference frame using the transformation given by,

$$T_{\alpha\beta\rightarrow dq} = \begin{bmatrix} \sin\left(\theta_{dq}\right) & -\cos\left(\theta_{dq}\right) \\ \cos\left(\theta_{dq}\right) & \sin\left(\theta_{dq}\right) \end{bmatrix} \tag{5.11}$$

After obtaining the quadrature component, v_q, it is compared with zero and sent to the PI controller to generate the error, $\Delta\omega$. Further the grid frequency, ω_o^E, is calculated as the difference of $\Delta\omega$ and the nominal grid frequency (100π rad/s), and then integrated to generate θ_{dq}.



(a)



(b)

Fig. 5.11. Block diagram of (a) PLL, and (b) voltage SOGI.

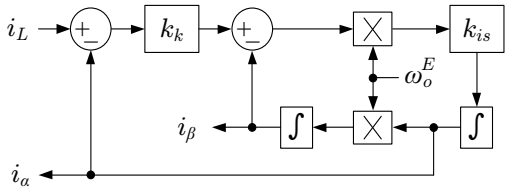


Fig. 5.12. Block diagram of current SOGI to transform from i_L to $i_{\alpha\beta}$.

E) Single-phase to dq ***Transformation***

The 1ϕ to dq transformation block of Fig. 5.1 generates the dq domain components, i_{dq} of the filter inductor current i_L. This block consists of two stages, namely, single-phase to $\alpha\beta$ transformation and then from $\alpha\beta$ to dq transformation. The single-phase to $\alpha\beta$ transformation for i_L is performed using the SOGI shown Fig. 5.12. Further, $i_{\alpha\beta}$ is transformed to synchronous reference frame using transformation matrix given in (5.11).

F) Chopper and ANPCI Controllers

To generate the gate signals for chopper switches of Fig. 5.10, different chopper current control techniques are explained in Section 4.3 of Chapter 4. As observed from the simulation and experimental results, and the advantages mentioned in Chapter 4, the Average Current Control (ACC) technique is utilized in this chapter to regulate the chopper current and control the chopper switches.

To generate the modulation signal m_a for the chopper intergraded ANPCI of Fig. 5.10, an SRF-dq based current controller is utilized. The main objective here is to regulate the DC-link voltage V_{DC} to V_{DC}^* and to regulate the grid power factor PF to PF^*. The detailed block diagram of the SRF-dq current controller is shown in Fig. 5.13. The inputs of the SRF-dq based controller are DC-link voltage (V_{DC}), grid active power (P_g), grid reactive power (Q_g) and dq-domain quantities of i_L and v_o, i.e., (i_d, i_q) and (v_d, v_q), respectively. The reference quantities given as inputs are reference power factor (PF^*) and reference DC-link voltage (V_{DC}^*). This controller has only one output, modulation signal (m_a). The reference power factor PF^* generates Q_g^* based on P_g using the equation given by

$$Q_g^* = \frac{P_g}{PF^*}\sqrt{1-(PF^*)^2} \tag{5.12}$$

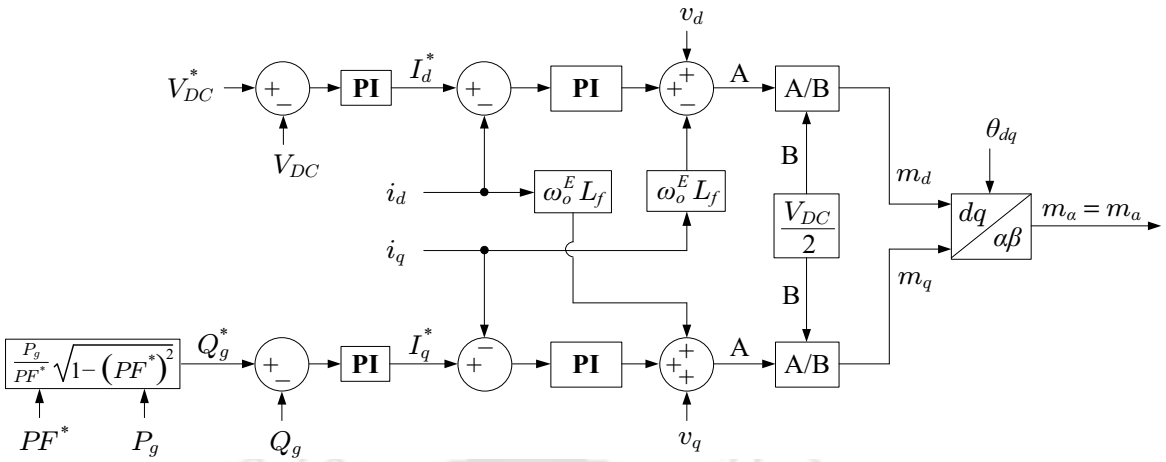


Fig. 5.13. Detailed block diagram of closed-loop controller for ANPCI.

The reference dq-axes currents I_d^* and I_q^* are generated using the PI controllers to regulate V_{DC} and Q_g, respectively. The quantities, i_d and i_q are obtained from 1ϕ to dq transformation of i_L. It can be seen that PI controllers are used to regulate i_d and i_q. To design these PI controllers, the circuit diagram of ANPCI is modeled as

$$\frac{\mathrm{d}i_L}{\mathrm{d}t} = \frac{(v_{an} - v_o - i_L r_L)}{L_f} \tag{5.13}$$

where r_L is the ESR of L_f. This model is then transformed to dq-domain using the transformation given in (5.11). The mathematical model of ANPCI in dq-domain is given by

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -\frac{r_L}{L_f} & \omega_o^E \\ -\omega_o^E & -\frac{r_L}{L_f} \end{bmatrix} \cdot \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{1}{L_f} \cdot \begin{bmatrix} v_{and} - v_d \\ v_{anq} - v_q \end{bmatrix} \tag{5.14}$$

The time domain model is then transformed into s-domain, which is given by the transfer functions

$$\frac{i_d(s)}{v_{and}(s) - v_d(s) + \omega_o^E L_f i_q(s)} = \frac{1}{sL_f + r_L} \tag{5.15}$$

$$\frac{i_q(s)}{v_{anq}(s) - v_q(s) - \omega_o^E L_f i_d(s)} = \frac{1}{sL_f + r_L} \tag{5.16}$$

These transfer functions are used to determine the PI controller parameters. The current controller block generates the modulation signal $(m_d,\ m_q)$ in SRF-dq domain, which is again

transformed back into stationary reference frame to obtain m_a using the equation given by

$$m_\alpha = m_a = m_d \cdot \sin\left(\theta_{dq}\right) + m_q \cdot \cos\left(\theta_{dq}\right) \tag{5.17}$$

Further, m_a is given as input to the PDS-PWM technique to generate the gate signals for ANPCI. The detailed explanation for generation of the gate signals using PDS-PWM technique is given in Chapter 2.

5.2.2 Simulation Results

The SPGS shown in the block diagram of Fig. 5.1 is simulated using PSCAD/EMTDC with the simulation parameters listed in Tables 5.3 and 5.4. The performance of SPGS is compared with and without chopper integration to the ANCPI and the corresponding simulation results are shown in Figs. 5.14−5.16.

Fig. 5.14 shows the simulation results of 5 kW rated SPGS with various operating

Table 5.3. SIMULATION PARAMETERS OF SPGS

Parameters	Attributes
Solar irradiation (G)	1000 $\frac{\text{W}}{\text{m}^2}$
Temperature (T)	25 °C
Switching frequency of the boost converter (f_b)	5 kHz
Switching frequency of the ANPCI (f_{s1})	5 kHz
Switching frequency of the chopper circuit (f_{s2})	5 kHz
Reference DC-link voltage (V^*_{DC})	500 V
C_{PV}	500 μF
L_B	10 mH
C_D	4.4 mF
C_1 and C_2	1.0 mF
FC	0.53 mF
L_f	2.5 mH
C_f	40 μF
L_{ch}	0.6 mH
Resistance of L_B	0.2 Ω
Resistance of L_f and switches of ANPCI	0.2 Ω

Table 5.4. PARAMETERS OF THE GRID

Parameters	Attributes
Nominal grid voltage	230 V RMS
Nominal grid frequency, $f_n \left(= \frac{\omega_n}{2\pi}\right)$	50 Hz
R_g	0.2 Ω
L_g	5 mH

Table 5.5. OPERATING CONDITIONS CONSIDERED FOR SIMULATION OF SPGS

Simulation time	Is chopper circuit turned ON ?	Grid power factor	MPPT
0 to 5 s	No	1.0	No
5 to 8 s	Yes	1.0	No
8 to 15 s	Yes	0.9 Lead	No
15 to 45 s	Yes	0.9 Lead	Yes

conditions listed in Table 5.5. From $t = 0$ to 5 s, the chopper circuit is turned OFF and the system is operated at unity power factor and without MPPT. The zoomed waveforms for this operating conditions are shown in Fig. 5.15. It can be observed that the reactive power injected into the grid Q_g is zero VAR and the real power injected into the grid P_g is 5.0 kW. Also, it can be observed from the results that without chopper integration to the ANPCI, the DC-link capacitor voltage ripple is very high (115.8 V, P-P), i.e., 46.32% which causes distortion in the grid injected current and ripple in active and reactive powers. Moreover, the THD of grid current is obtained as 6%.

At $t = 5$ s, the chopper circuit is turned ON and at $t = 8$ s, the grid power factor reference (PF^*) is set to 0.9 Lead. The zoomed waveforms for this operating conditions are shown in Fig. 5.16. It can be observed that the reactive power absorbed from the grid Q_g, is 2.25 kVAR and the real power injected into the grid, P_g is 4.66 kW. Also, it can be observed from the results that with chopper integration to the ANPCI, the DC-link capacitor voltage ripple is significantly reduced to 31.73 V, i.e., 12.69%. Moreover, the THD of grid current is reduced to 1.6%. Due to the reduced voltage ripples and THD, the grid injected active and

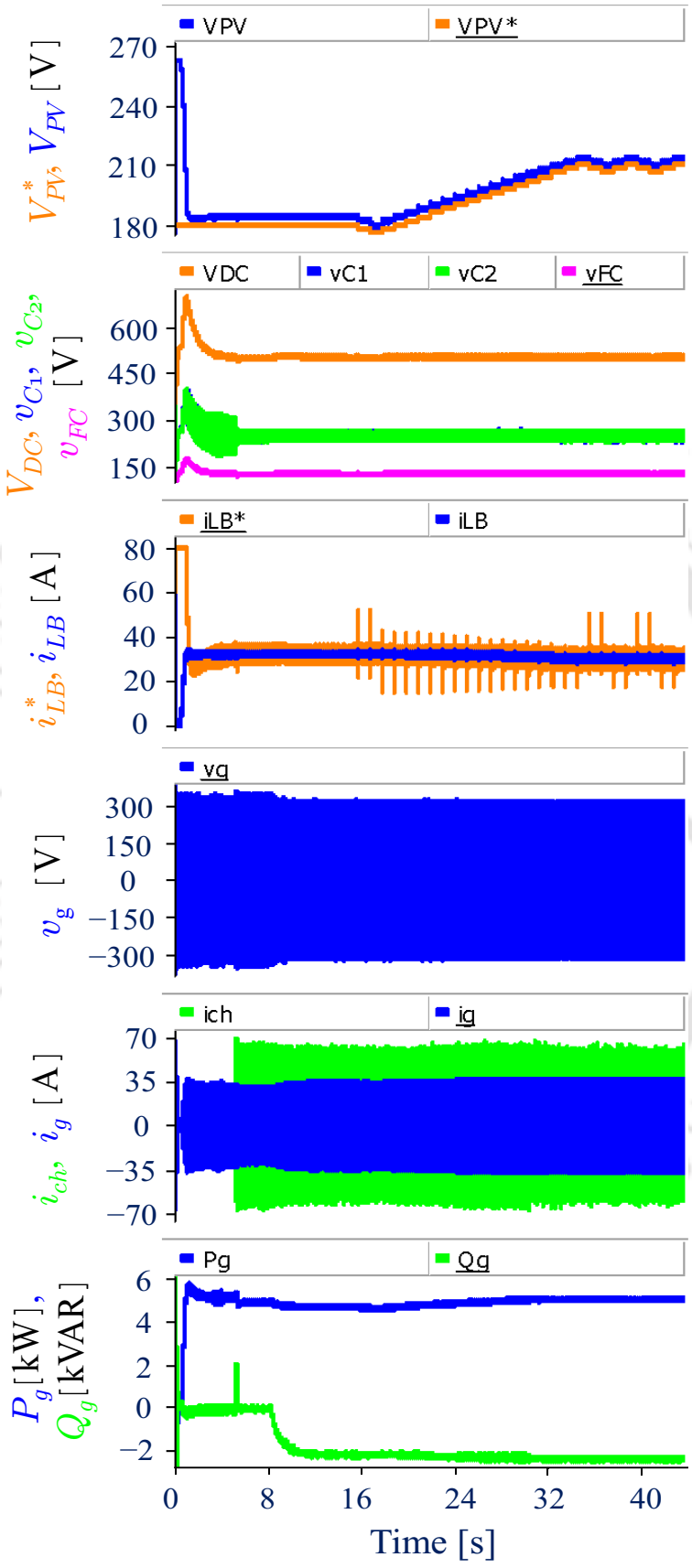


Fig. 5.14. Waveforms for SPGS with and without chopper integration.

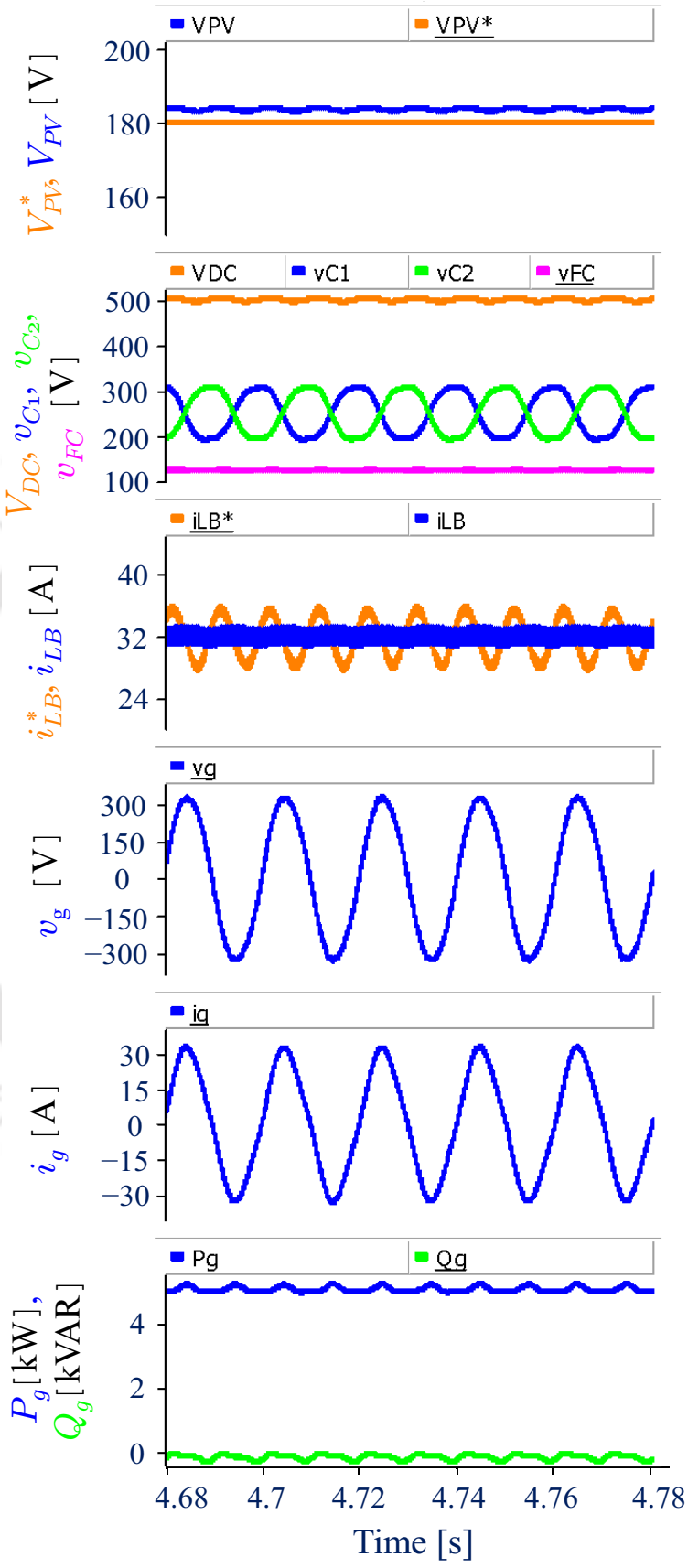


Fig. 5.15. Waveforms for SPGS without chopper integration (Zoomed waveforms of Fig. 5.14).

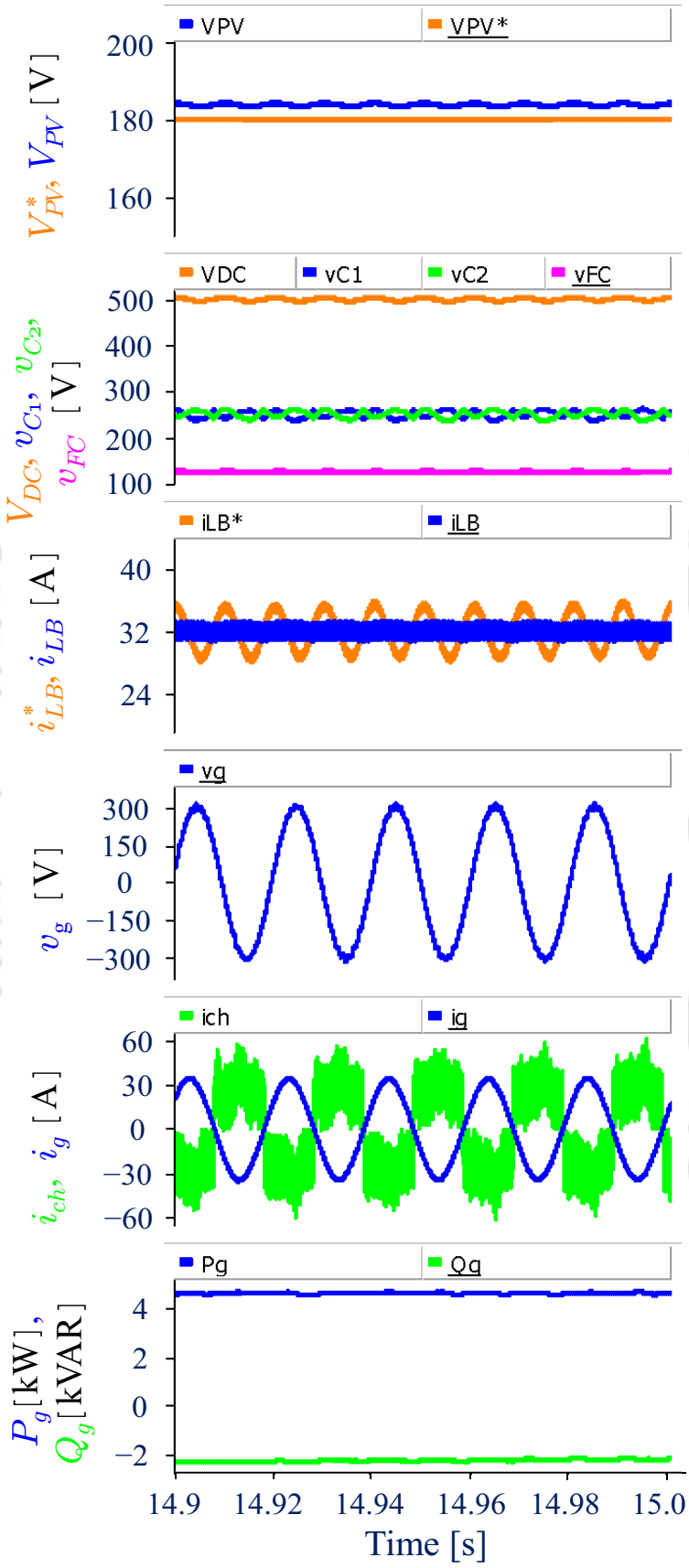


Fig. 5.16. Waveforms for SPGS with chopper integration (Zoomed waveforms of Fig. 5.14).

reactive powers are almost ripple free, which means the quality of grid injected powers is improved.

At $t = 15$ s, MPPT algorithm is initiated and the system tries to capture maximum available energy from the solar PV array. Nearly at $t = 34.4$ s, the MPPT algorithm settles and the system operates in steady-state. It can be observed that the reactive power absorbed from the grid, Q_g is 2.43 kVAR and the real power injected into the grid P_g is 5 kW.

5.3 OPERATION AND CONTROL OF WPGS USING CHOPPER INTEGRATED ANPCI

5.3.1 Description of the System

Fig. 5.17 shows the block diagram of a WPGS connected to a single-phase distribution grid. This system consists of a wind turbine connected to the distribution grid through a Permanent Magnet Synchronous Generator (PMSG), a Diode Bridge Rectifier (DBR), a boost converter, a dc-to-ac converter and a step-up transformer. The output power of the wind turbine depends on the wind speed. The boost converter is used to operate the wind turbine at its maximum power point for any weather condition using an MPPT algorithm. The output of the boost converter is the DC-link voltage, V_{DC}, which is maintained as constant by the dc-to-ac converter. The real and reactive powers injected into the grid are also

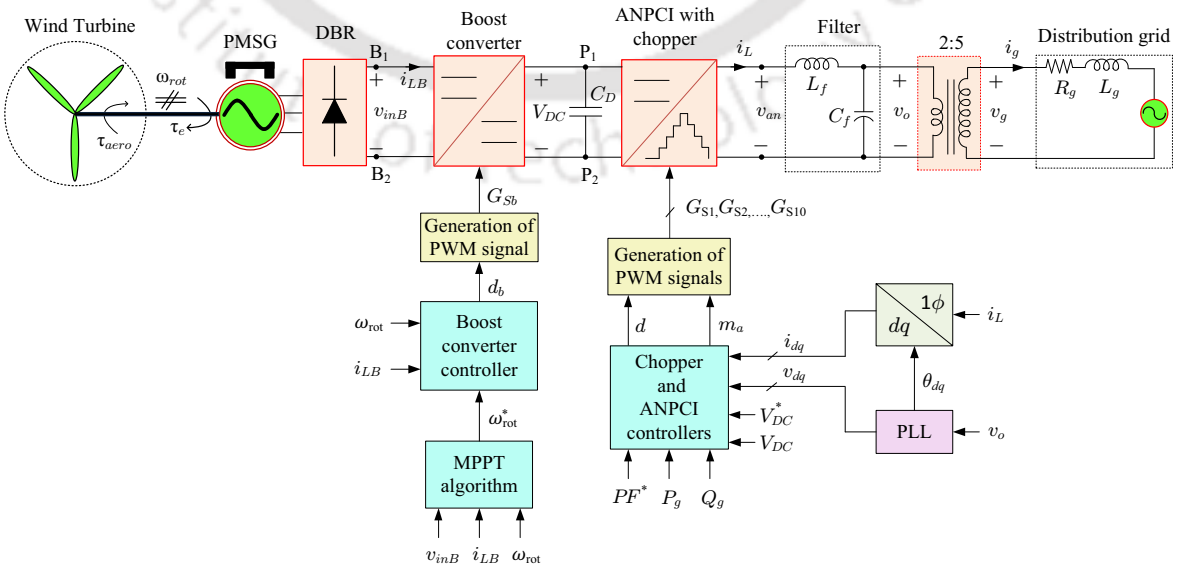


Fig. 5.17. Block diagram of WPGS with single-phase weak distribution grid connected ANPCI.

controlled by the dc-to-ac converter using an SRF-dq current controller.

In literature, different VSI topologies are available as dc-to-ac converter interface in the WPGS [130–135]. The dc-to-ac converter topology can be a two-level VSI or a multi-level VSI. In [130], a single-phase MOSFET inverter is used in stand-alone mode. In [131, 132], a single-phase two-level inverter is used, whereas in [133], a dual-buck inverter is used. In [134], a three-phase two-level inverter and in [135], a three-phase three-level NPC inverter are used. Multi-level VSIs are familiar for their features such as reduced voltage stress, more efficiency, low THD, low filter requirement and high power transfer capability [11]. In this chapter, the five-level chopper integrated ANPCI is proposed as a dc-to-ac converter interface due to the advantages mentioned in the previous chapters. Due to the integration of the chopper circuit in ANPCI, the ripple in DC-link capacitor voltages is reduced, hence the quality of the grid injected current improves. An LC filter is used at the output of the ANPCI to filter the harmonics in the grid injected current. The grid considered here is a weak distribution grid with Short Circuit Ratio (SCR) of 3.34 [126, 127].

The detailed description of wind turbine coupled with PMSG, diode bridge rectifier, boost converter and control blocks in the WPGS of Fig. 5.17 is given below. The description of remaining blocks is same as given for SPGS in Section 5.2.1.

A) Wind Turbine Coupled with PMSG and its Control

A wind turbine converts wind energy available at its blades to the mechanical energy which can be used to drive an electrical generator. The generated mechanical and electrical powers by the wind turbine and generator system, respectively, fluctuates due to variation in the wind speed (v_w). Hence, to operate the wind turbine in a wide speed range, a speed control mechanism is required. This is achieved by controlling the PMSG rotor speed using the dc-to-dc boost converter. The mechanical power, P_m (kW), drawn from the wind turbine depends on its power-coefficient or performance-coefficient (C_p) [136]. The expression for P_m is given as [136]

$$P_m = C_p \cdot P_w \tag{5.18}$$

where the wind power (P_w) in kilo-watt is given by

$$P_w = \frac{1}{2} \cdot \rho \cdot A \cdot v_w^3 \cdot 10^{-3} \tag{5.19}$$

To extract maximum available power from the wind turbine, C_p must be adjusted to its maximum value, C_p^{max} by changing the tip-speed ratio (λ) according to the varying wind speed. The characteristic equation of the wind turbine expressed using $C_p - \lambda$ relation is given by

$$C_p = x_1 \cdot \left(\frac{x_2}{\lambda_i} - x_3\right) \cdot \exp\left(-\frac{x_4}{\lambda_i}\right) \tag{5.20}$$

where λ_i is given by

$$\frac{1}{\lambda_i} = \frac{1}{\lambda} - 0.035 \tag{5.21}$$

The tip-speed ratio (λ) is calculated as

$$\lambda = \frac{(\omega_{rot} \cdot R_{rot})}{v_w} \tag{5.22}$$

Aerodynamic torque, τ_{aero} (N-m), developed in the rotor is

$$\tau_{aero} = \frac{P_m}{\omega_{rot}} \tag{5.23}$$

The parameters used in (5.19), (5.20) and (5.22) and the other parameters of the wind turbine shown in Fig. 5.17 are listed in Table 5.6. The coefficient of power vs. tip speed ratio characteristic of the wind turbine is shown in Fig. 5.18. The maximum power coefficient (C_p^{max}) is obtained at the tip-speed ratio, which is known as optimal tip-speed ratio (λ_{opt}) [136]. For various wind speed conditions, the mechanical power vs. rotor speed characteristics of the wind turbine are shown in Fig. 5.19. Also, Table 5.7 gives the maximum power point (ω_{MPP}, P_{MPP}) values obtained from these curves.

Table 5.6. PARAMETERS OF THE WIND TURBINE

Parameters	Attributes
Air density (ρ)	1.225 kg/m^3
Rated wind speed (v_w^r)	10.8 m/s
Maximum power co-efficient (C_p^{max})	0.4382
Optimal tip-speed ratio (λ_{opt})	6.3
Rotor radius (R_{rot})	3.1 m
Inertia (J)	59.61 kg-m^2
Area swept by the blades ($A = \pi R_{rot}^2$)	30.19 m^2
Rated rotor speed (ω_{rot}^r)	21.95 rad/s
Rated power (P_m^r)	10 kW
Coefficient (x_1)	0.22
Coefficient (x_2)	116
Coefficient (x_3)	5
Coefficient (x_4)	12.5

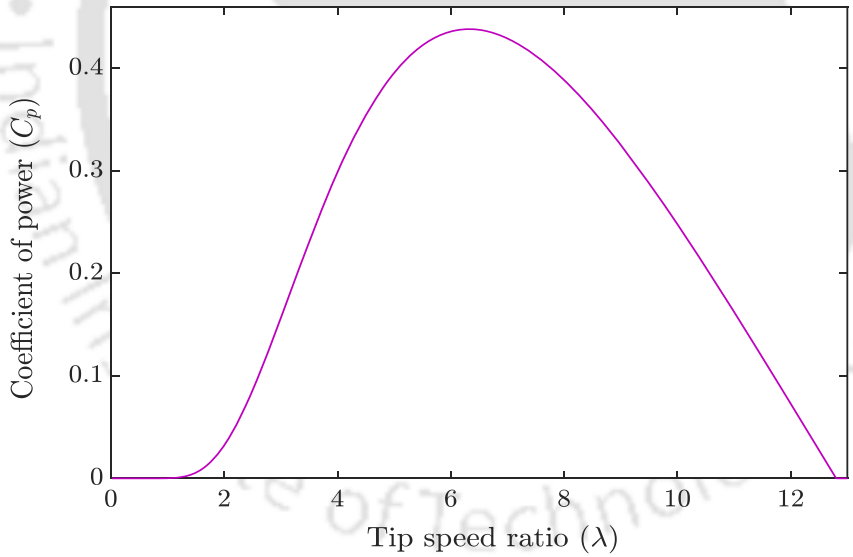


Fig. 5.18. C_p vs. λ characteristic of the wind turbine.

As shown in Fig. 5.19 and Table 5.7, it can be observed that the power generated by the wind turbine depends on the weather condition. As the wind speed increases, the power output of the wind turbine increases above a certain rotor speed. Also, when wind speed increases, the maximum power point is obtained for increased rotor speeds. To extract the maximum available power from the wind turbine, an MPPT algorithm is required. In

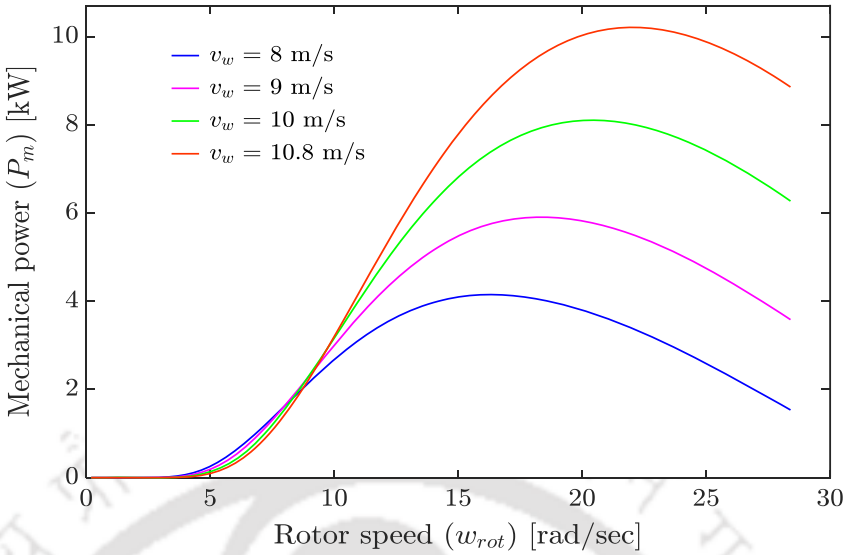


Fig. 5.19. P_m vs. ω_{rot} characteristics of the wind turbine for various wind speeds.

Table 5.7. MAXIMUM POWER POINT (MPP) OF THE WIND TURBINE CURVES SHOWN IN FIG. 5.19

Parameter	Maximum power point	
	ω_{MPP}	P_{MPP}
$v_w = 8$ m/s	16.4 rad/s	4.15 kW
$v_w = 9$ m/s	18.4 rad/s	5.91 kW
$v_w = 10$ m/s	20.4 rad/s	8.1 kW
$v_w = 10.8$ m/s	21.8 rad/s	10.21 kW

this work, Perturbation and Observation (P&O) based MPPT algorithm is utilized for the maximum power extraction from the wind turbine. The flowchart of an MPPT algorithm is shown in Fig. 5.20 [129]. In this figure, $\omega_{rot}(k)$, $v_{inB}(k)$ and $i_{LB}(k)$ represent the rotor speed, boost converter's input voltage and current, respectively, at k^{th} sampling instant. Also, $P_W(k)$, $\triangle P_W$, $\triangle\omega_{rot}$ are given by

$$P_W(k) = V_{inB}(k) I_{inB}(k) \tag{5.24}$$

$$\triangle P_W = P_W(k) - P_W(k-1) \tag{5.25}$$

$$\triangle\omega_{rot} = \omega_{rot}(k) - \omega_{rot}(k-1) \tag{5.26}$$

where $V_{inB}(k)$ and $I_{inB}(k)$ are the DC components extracted from $v_{inB}(k)$ and $i_{inB}(k)$,

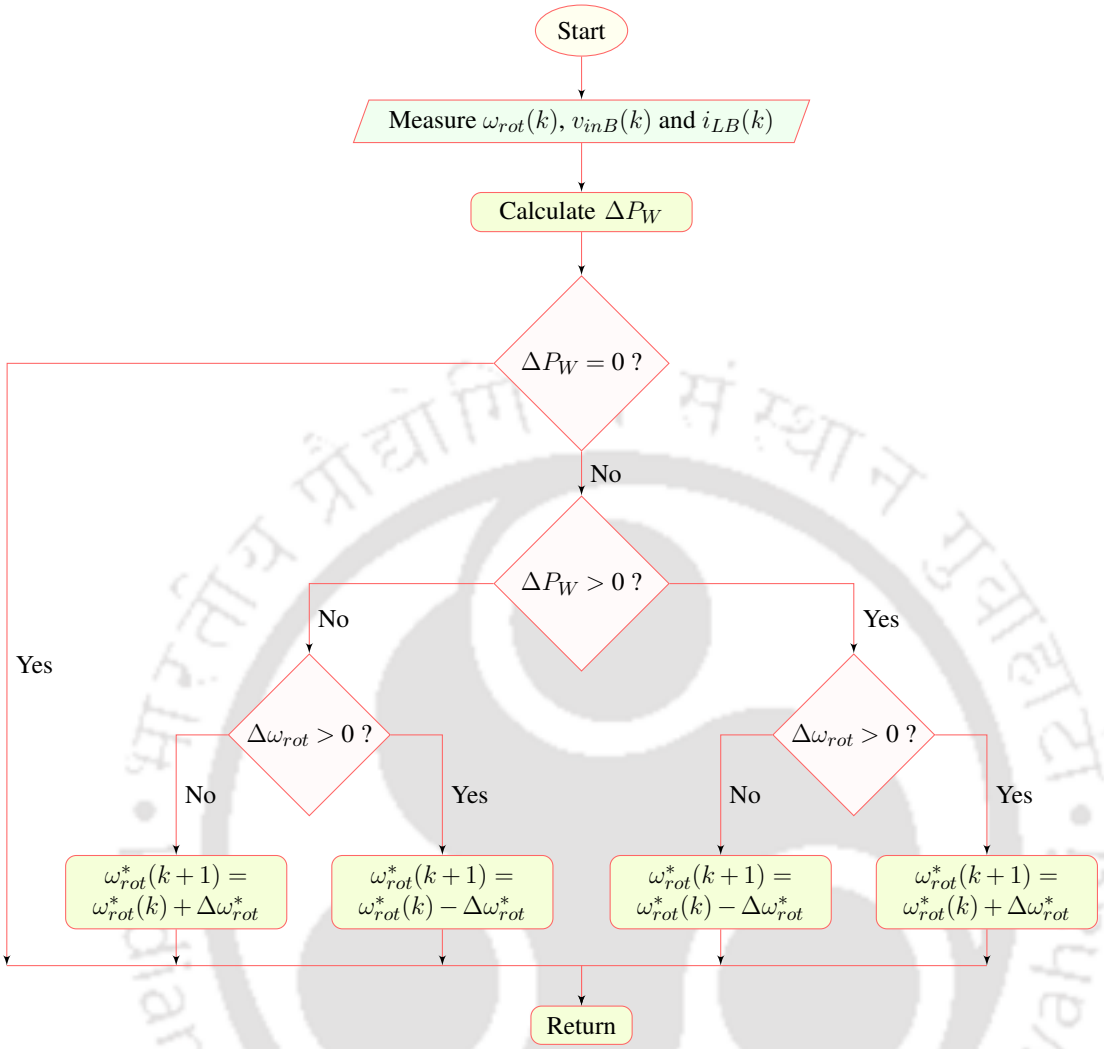


Fig. 5.20. Flowchart representing the MPPT algorithm for wind turbine.

respectively. The MPPT algorithm decides the reference rotor speed for the next sampling instant $\omega^*_{rot}(k+1)$, which will be given as input to the boost converter controller. Note that $\triangle\omega^*_{rot}$ is the change in ω^*_{rot} from k^{th} sampling instant to the $(k+1)^{\text{th}}$ sampling instant.

Depending on the generator and power converter configuration, WPGS can be generally of four types, viz., Type-I, II, III and IV [137–139]. Due to the advantages of Type-III and Type-IV WPGS over other two types, these configurations are widely used nowadays. Either an induction generator or a permanent-magnet synchronous-generator (PMSG) can be employed as the electrical generator in Type-IV WPGS [137]. When compared to an induction generator, the PMSG offers low maintenance cost, greater flexibility due to variable

speed operation, higher efficiency and reduced power conversion stages due to permanent magnets. The PMSG is an electro-mechanical device which converts the mechanical output power of the wind to electrical energy. It can be manufactured with higher number of poles to obtain low rated rotor speed, thus it directly couples to the wind turbine without a gear box [140, 141]. As the rotor of the PMSG is coupled to the wind turbine, the rotor speed of the wind turbine and the PMSG remains same. The parameters of the PMSG are given in Table 5.8 [138, 139]. A single mass model representing the coupled shaft dynamics of the wind turbine and PMSG is given as

$$\tau_{aero} - \tau_e = J \cdot \frac{\mathrm{d}}{\mathrm{d}t}(\omega_{rot}) \tag{5.27}$$

where τ_e (N-m) is the electromagnetic torque developed by PMSG and acts opposite to τ_{aero}. In steady-state, ω_{rot} reaches to a constant value such that τ_e equals to τ_{aero}. Per phase Emf induced in the stator of PMSG is calculated as

$$E_{rms} = \sqrt{2} \cdot \pi \cdot f_p \cdot \psi_s \tag{5.28}$$

Table 5.8. PARAMETERS OF THE PMSG

Parameters	Attributes
Stator resistance (R_S)	0.017 p.u.
Stator leakage reactance (X_{ls})	0.064 p.u.
d-axis unsaturated reactance (X_d)	0.55 p.u.
q-axis unsaturated reactance (X_q)	1.11 p.u.
d-axis damper winding resistance (R_{kd})	0.183 p.u.
d-axis damper winding reactance (X_{kd})	0.62 p.u.
q-axis damper winding resistance (R_{kq})	1.11 p.u.
q-axis damper winding reactance (X_{kq})	1.175 p.u.
Magnetic strength	1.0 p.u.
Rated voltage	250 V RMS (L-N)
Rated frequency	50 Hz
Rated power	10 kVA

where f_p (Hz) represents the electrical frequency of PMSG generated output voltage and ψ_s (wb-turns) is the stator flux linkages. Note that f_p is directly proportional to the ω_{rot} and hence, from (5.28), E_{rms} is also directly proportional to ω_{rot}. The flux linkages of the permanent magnet mounted on the rotor is ψ_r.

B) Diode Bridge Rectifier

As shown in Fig. 5.17, the stator terminals of PMSG are connected to the input of the Diode Bridge Rectifier (DBR) to convert the sinusoidal output voltage to unipolar voltage v_{inB}. The output voltage of the DBR [2] is given by,

$$v_{inB} = \left(\frac{3}{\pi}\right) v_{abm} \tag{5.29}$$

where v_{abm} is the maximum value of line-to-line voltage at the PMSG's stator terminals.

C) Boost Converter and its Control

Once the reference rotor speed (ω^*_{rot}) is obtained from the MPPT algorithm, the rotor speed of the wind turbine (ω_{rot}) is regulated to ω^*_{rot} using a boost converter shown in Fig. 5.8 and its closed-loop control algorithm described in Fig. 5.21. The boost converter also steps-up the output voltage of the diode bridge rectifier, v_{inB} to the DC-link voltage V_{DC}. The relation between v_{inB} and V_{DC} is given by

$$\frac{V_{DC}}{v_{inB}} = \frac{1}{1-d_b} \tag{5.30}$$

The control block diagram shown in Fig. 5.21 calculates the error between ω^*_{rot} and ω_{rot}. This error is then fed to a PI controller to generate current reference i^*_{LB} for the inductor current, i_{LB}. The error between i^*_{LB} and i_{LB} is calculated and fed to another PI controller to generate the duty signal, d_b. Further this duty signal is compared with the sawtooth signal to

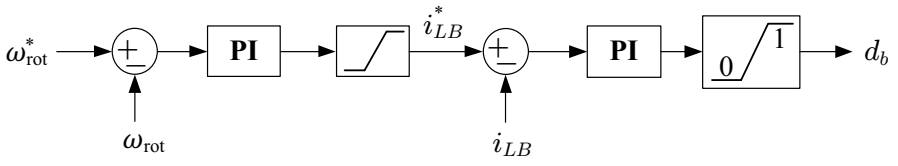


Fig. 5.21. Block diagram to control rotor speed of the wind turbine.

generate the gate signal, G_{Sb}, which controls the switch S_b of the boost converter.

5.3.2 Simulation Results

The WPGS shown in the block diagram of Fig. 5.17 is simulated using PSCAD/EMTDC with the simulation parameters listed in Tables 5.9 and 5.4. The performance of WPGS is compared with and without chopper integration to the ANCPI and the corresponding simulation results are shown in Figs. 5.22−5.24.

Fig. 5.22 shows the simulation results of 10 kW rated WPGS with various operating conditions listed in Table 5.10. From $t = 10$ to 15 s, the chopper circuit is turned OFF and the system is operated at unity power factor and without MPPT. The zoomed waveforms for this operating conditions are shown in Fig. 5.23. It can be observed that the reactive power injected into the grid Q_g is zero VAR and the real power injected into the grid P_g is 6.5 kW. Also, it can be observed from the results that without chopper integration to the ANPCI, the DC-link capacitor voltage ripple is very high (183 V, P-P), i.e., 73.2% which causes distortion in the grid injected current and ripple in active and reactive powers. Moreover, the

Table 5.9. SIMULATION PARAMETERS OF WPGS

Parameters	Attributes
Operating wind speed (v_w)	10.8 m/s
Switching frequency of the boost converter (f_b)	5 kHz
Switching frequency of the ANPCI (f_{s1})	5 kHz
Switching frequency of the chopper circuit (f_{s2})	5 kHz
V^*_{DC}	500 V
L_B	10 mH
C_D	4.4 mF
C_1 and C_2	1.0 mF
FC	0.53 mF
L_f	2.5 mH
C_f	40 μF
L_{ch}	2.5 mH
Resistance of L_B	0.2 Ω
Resistance of L_f and switches of ANPCI	0.2 Ω

Table 5.10. OPERATING CONDITIONS CONSIDERED FOR SIMULATION OF WPGS

Simulation time	Is chopper circuit turned ON ?	Grid power factor	MPPT
10 to 15 s	No	1.0	No
15 to 18.5 s	Yes	1.0	No
18.5 to 20 s	Yes	0.9 Lag	No
20 to 50 s	Yes	0.9 Lag	Yes

THD of grid current is obtained as 8%.

At $t = 15$ s, the chopper circuit is turned ON and at $t = 18.5$ s, the grid power factor reference (PF^*) is set to 0.9 Lag. The zoomed waveforms for this operating conditions are shown in Fig. 5.24. It can be observed that the reactive power injected into the grid Q_g is 3 kVAR and the real power injected into the grid P_g is 6.2 kW. Also, it can be observed from the results that with chopper integration to the ANPCI, the DC-link capacitor voltage ripple is significantly reduced to 21.64 V, i.e., 8.65%. Moreover, the THD of grid current is reduced to 2%. Due to the reduced voltage ripples and THD, the grid injected active and reactive powers are almost ripple free, which means the quality of grid injected powers is improved.

At $t = 20$ s, MPPT algorithm is initiated and the system tries to capture maximum available energy from the wind turbine. Nearly at $t = 38$ s, the MPPT algorithm settles and the system operates in steady-state. It can be observed that the reactive power injected into the grid Q_g is 3.5 kVAR and the real power injected into the grid P_g is 7.4 kW.

5.4 SUMMARY

In this chapter, the operation of chopper integrated ANPCI as a dc-to-ac converter interface in a 5 kW SPGS and 10 kW WPGS is presented. Both SPGS and WPGS are operated in grid connected mode. Both the active and reactive powers injected into the grid are controlled using an SOGI-PLL and an SRF-dq current controller. Further P&O MPPT algorithm is implemented for both SPGS and WPGS. Also the performance of both the systems is compared using PSCAD/EMTDC simulation with and without integration of chopper circuit

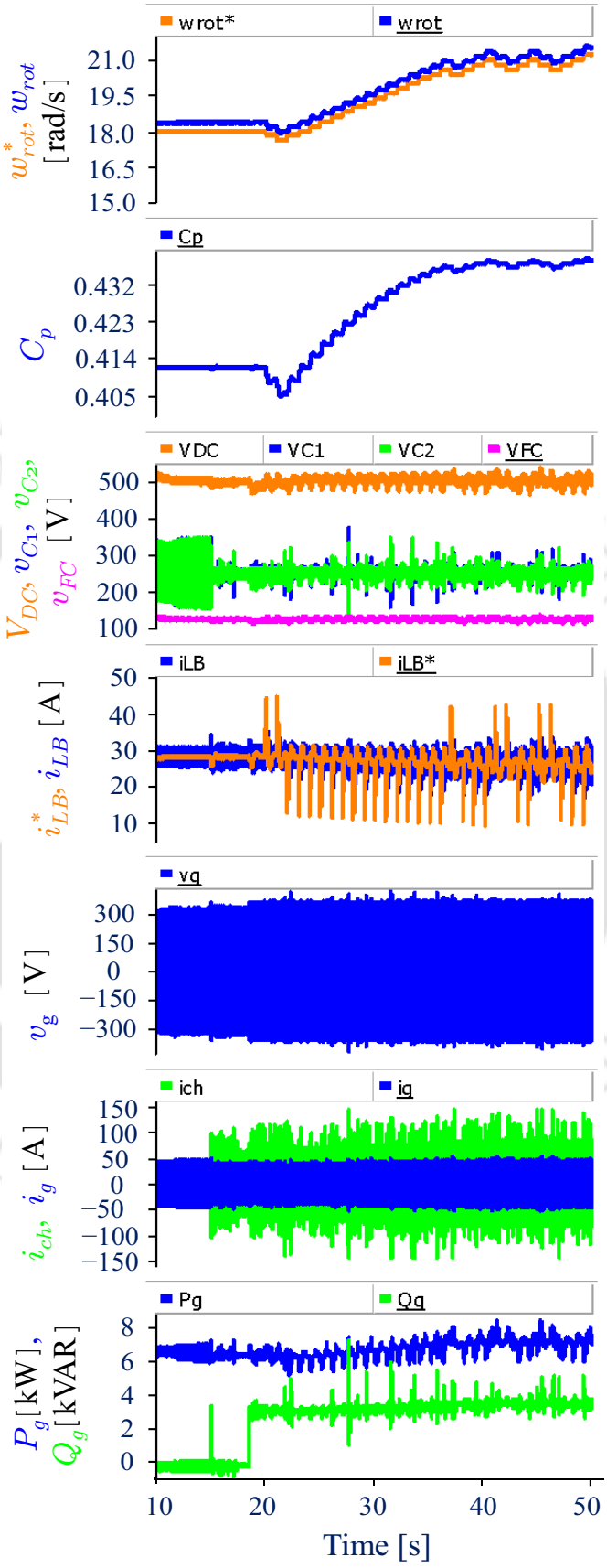


Fig. 5.22. Waveforms for WPGS with and without chopper integration.

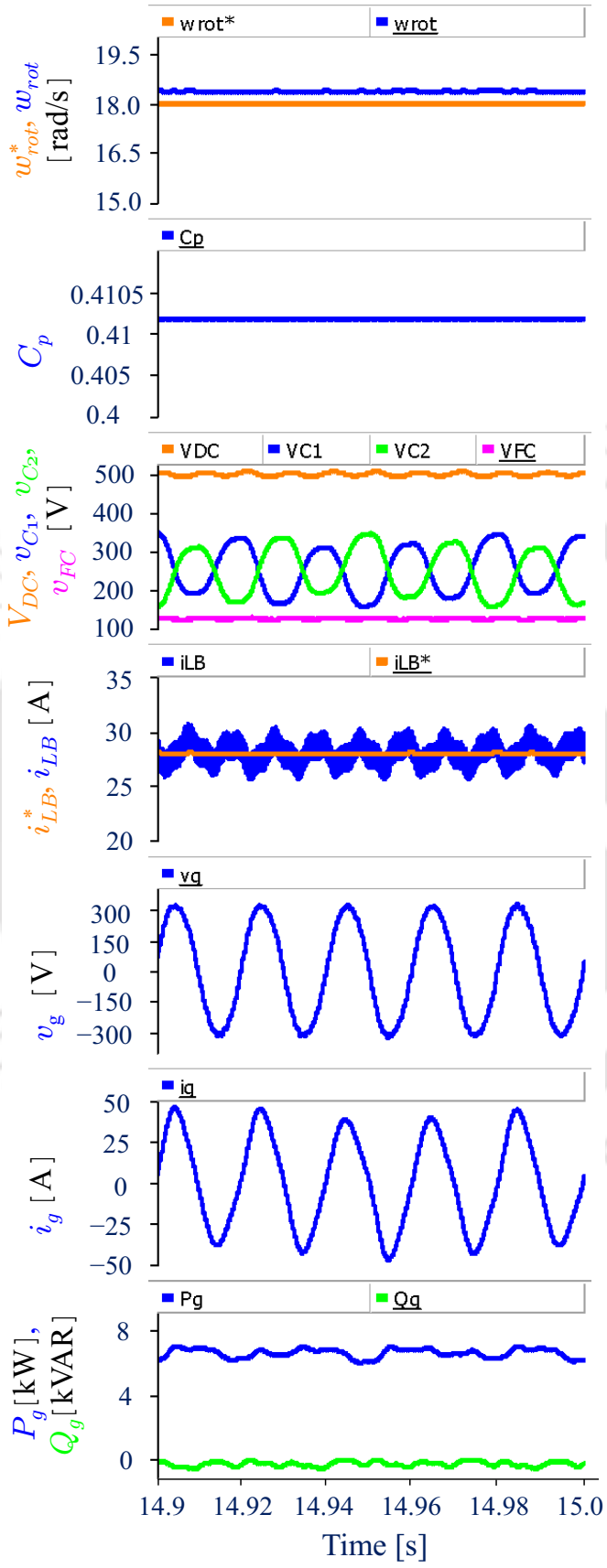


Fig. 5.23. Waveforms for WPGS without chopper integration (Zoomed waveforms of Fig. 5.22).

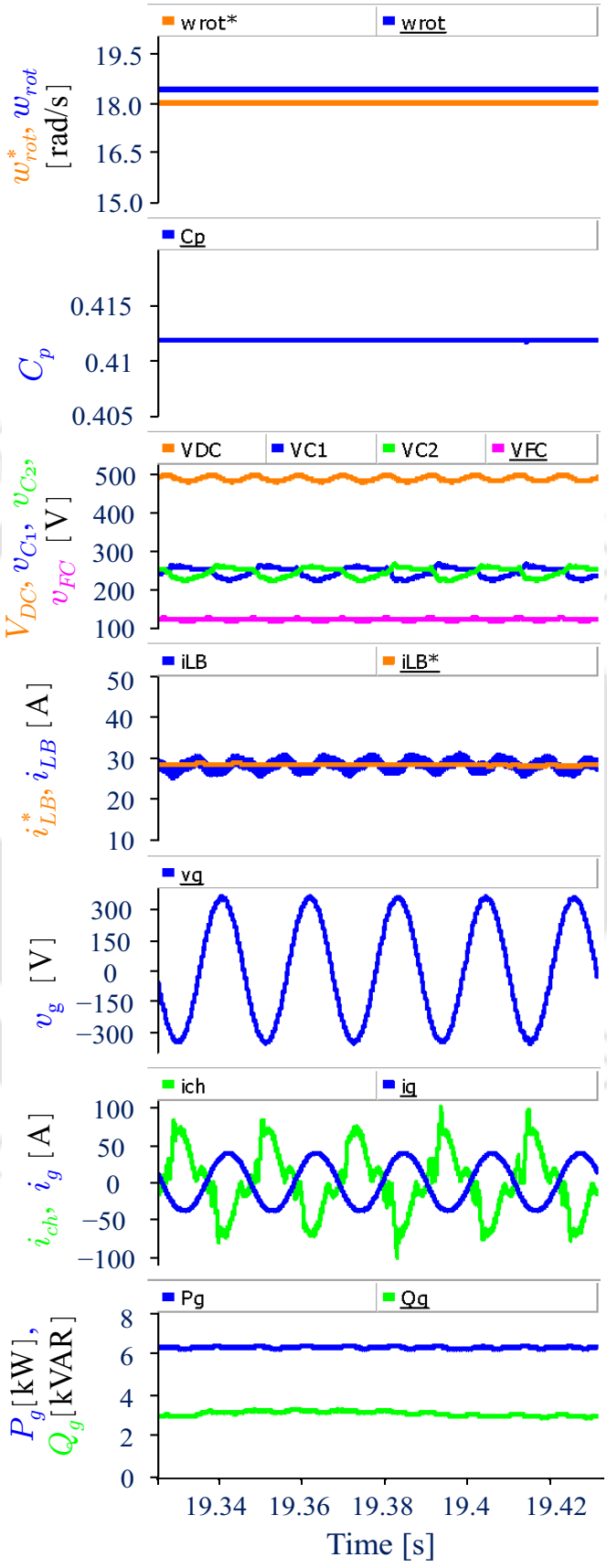


Fig. 5.24. Waveforms for WPGS with chopper integration (Zoomed waveforms of Fig. 5.22).

to the ANPCI. In both the SPGS and WPGS, the chopper circuit significantly reduced ripple in the DC-link capacitor voltages. The ripple reduction in the DC-link capacitor voltages is achieved from 46.32% to 12.69% for SPGS and from 73.2% to 8.65% for WPGS. The grid power factor is regulated to 0.9 lead/lag by the five-level ANPCI using the SRF-dq based controller. The proposed system has reduced the ripple in the powers, which are injected into the grid, there by power quality also increased.

The proposed SPGS and WPGS can regulate both real and reactive powers injected into the grid. Hence, there is no necessity of installing additional reactive power compensating devices in the proposed SPGS and WPGS.

CHAPTER 6

CONCLUSIONS AND FUTURE SCOPE OF THE RESEARCH

6.1 CONCLUSIONS

In this thesis, detailed analysis, modeling and control techniques of single-phase active neutral point clamped inverter are presented. Different pulse-width-modulation (PWM) strategies for the ANPCI are described and from their comparison, it is shown that phase disposition and shifting (PDS) PWM technique resulted in low THD output voltage. Different capacitor voltage balancing strategies are customized and compared for an eight-switch, five-level ANPCI. For the closed-loop operation of the ANPCI, a synchronous reference frame (SRF) dq domain controller has been implemented. Moreover, a dynamic average circuit model (DACM) has been developed and implemented for the single-phase ANPCI. The modularity of the DACM is also discussed. Using extensive simulations and experiments, it is shown that the DACM developed in this thesis results in significant reduction of computational resources and execution times while analyzing or designing power electronic systems involving ANPCI. The results for stand-alone PV system involving ANPCI demonstrated the strength of the DACM developed for ANPCI. Further, integration of the external chopper circuit to the DC-link of ANPCI, facilitated reduction of the DC-link capacitor values and regulation of ripple in the DC-link capacitor voltages. This helps in increasing the power density and reliability. For chopper circuit operation, various control techniques are presented and from their performance comparison, it is found that the CCM based average current control strategy is effective in reducing the voltage ripples. Further in this thesis, the performance of chopper integrated ANPCI as a power electronic interface (PEI) in solar and wind power generation systems is demonstrated.

The detailed conclusions drawn from the individual chapters are given below.

In Chapter 2, detailed operation and various capacitor voltage balancing strategies for single-phase five-level ANPCI are presented. The performance of four different PWM techniques and four different capacitor voltage balancing strategies is compared for five-level ANPCI. It is shown that the PDS-PWM technique is performing better than remaining PWM techniques and Strategy-IV is performing better than the remaining capacitor voltage balancing strategies in maintaining the average value of DC-link capacitor and flying capacitor voltages with minimum settling time. Also, it is shown that remarkable voltage ripple remains in the DC-link capacitor voltages irrespective of the capacitor voltage balancing strategy. The SRF-dq controller is presented and implemented for the single-phase ANPCI. The experimental results in open-loop as well as in closed-loop verified the CVBS-IV and SRF-dq controller operation.

In Chapter 3, a DACM of ANPCI is developed. The DACM can include the non-idealities in the converter components and the CVBS. The model is also modular in nature and hence it is extended for an N-level ANPCI. The waveforms obtained from PSCAD/EMTDC simulations of switching circuit, experiments, and average model, and the corresponding RMS errors confirmed that the averaged model presented could accurately predict the steady-state and dynamic waveforms of ANPCI in both open-loop and SRF-dq controller based closed-loop operation. In addition, the effectiveness of the model is also demonstrated using a simple stand-alone PV system with ANPCI as the power conversion stage. From the results presented, it is confirmed that the dynamic average circuit model requires significantly less computation time compared to the detailed switching circuit model. Thus, the average model is recommended for system-level studies with ANPCI as power converter interface to save the computational time and resources required.

Chapter 4 has discussed integration of external chopper circuit to the DC-link of five-level ANPCI augmenting capacitor voltage balancing strategy for reduction of ripple in the DC-link capacitor voltages. The control and operation of single-phase chopper based five-level ANPCI are presented. Six different chopper control techniques are described and

implemented using the PSCAD/EMTDC simulation. Due to the large starting current of the chopper inductor, single-pulse based chopper current control scheme is not recommended for hardware implementation. All the control schemes except single-pulse control scheme are implemented on the hardware, and their performance is compared. The performance of the chopper integrated ANPCI is also verified with SRF-dq-based load voltage control. The results confirm that the proposed integration of chopper circuit and the controllers are successful in regulating the DC-link capacitor voltages and the load voltage of ANPCI. From the analysis presented and the experimental results obtained, it can be concluded that the proposed chopper circuit along with the CCM based average current control technique is effective in reducing ripples in the DC-link capacitor voltages. This further improves the quality of output voltage and current waveforms of the converter and also helps in reducing the size of DC-link capacitors, thereby increasing the power density of the single-phase, five-level ANPCI.

In Chapter 5, the chopper integrated ANPCI is proposed as the dc-to-ac power converter interface in a Solar Power Generation System (SPGS) and Wind Power Generation System (WPGS) connected to a single-phase weak distribution grid. Both the SPGS and WPGS are described in detail and the performance of the ANPCI with and without chopper is compared using the simulation results. From the results, it can be concluded that the chopper circuit significantly reduces the ripple in DC-link capacitor voltages which will also help in reduction of THD in the grid current. The grid power factor is also regulated to lead/lag using the five-level ANPCI, which is controlled by the SRF-dq based controller.

6.2 FUTURE SCOPE OF THE RESEARCH

- The performance of the PDS-PWM technique can be compared with other pulse-width-modulation techniques available in the literature for five-level active neutral point clamped inverter. Further, a better performing pulse-width-modulation technique and the proposed capacitor voltage balancing strategy, i.e., CVBS-IV, can be applied to the seven-switch, five-level active neutral point clamped inverter for improving the

efficiency of the system.

- The strength of the dynamic average circuit model can be demonstrated for other applications of ANPCI, such as wind power generation system, adjustable speed drives, etc.
- The control parameters of the dependent sources in the DACM of N-level ANPCI can be derived so that a generalized DACM of the ANPCI is obtained.
- The performance of other advanced current controllers can be explored for the chopper integrated active neutral point clamped inverter.
- The ANPCI based solar and wind power generation systems can be integrated as a microgrid. The performance can be evaluated using simulation and experiments.

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LIST OF RESEARCH ARTICLES

Journal Publication

1. **Jagath Vallabhai Missula**, Ravindranath Adda, Praveen Tripathy, "**Averaged Modeling and SRF Based Closed-loop Control of Single-phase ANPC Inverter**," in *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 13839−13854, Dec. 2021. doi: 10.1109/TPEL.2021.3083279

Conference Publications

1. **Jagath Vallabhai Missula**, Ravindranath Adda, Praveen Tripathy, "**Performance Comparison of Capacitor Voltage Balancing Strategies for Eight-Switch Five-Level ANPC Inverter**," in *Proc. 10^{th} National Power Electronics Conf. (NPEC)*, Bhubaneswar, India, Dec. 2021, pp. 1−6. doi: 10.1109/NPEC52100.2021.9672461

2. **Jagath Vallabhai Missula**, Ravindranath Adda, Praveen Tripathy, "**Reduction of Voltage Ripple for Single-phase Chopper Integrated ANPCI based on Hysteresis Voltage and Chopper Current Control Methods**," in *Proc. IEEE Int. Conf. Power Electronics, Drives and Energy Systems (PEDES)*, Jaipur, India, Dec. 2020, pp. 1-6. doi: 10.1109/PEDES49360.2020.9379352

3. **Jagath Vallabhai Missula**, Ravindranath Adda, Praveen Tripathy, "**Ripple Reduction in the DC-link Capacitor Voltages of Single-phase ANPC Inverter using External Chopper Circuit**," in *Proc. 46^{th} Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Marina Bay Sands, Singapore, Oct. 2020, pp. 2436-2441. doi: 10.1109/IECON43393.2020.9254595.

4. **Jagath Vallabhai Missula**, Ravindranath Adda, Praveen Tripathy, "**A CCM based Average Current Control Technique for Chopper Integrated Single-phase ANPC**

Inverter to Minimize Voltage Ripple," in *Proc. 12th IEEE Energy Convers. Congr. Expo. (ECCE)*, Detroit, MI, USA, Oct. 2020, pp. 2633-2640.
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5. **Jagath Vallabhai Missula**, Ravindranath Adda, Praveen Tripathy, "**Average modeling of active neutral point clamped inverter**," in *Proc. 11th IEEE Energy Convers. Congr. Expo. (ECCE)*, Baltimore, MD, USA, Sep.-Oct. 2019, pp. 3689-3696.
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6. **Jagath Vallabhai Missula**, Ravindranath Adda, Praveen Tripathy, "**Pulse Width Modulation and SRF Based Closed-Loop Control of Stand-alone Single-phase 5L-ANPC Inverter**," in *Proc. IEEE Int. Conf. Power Electronics, Drives and Energy Systems (PEDES)*, Chennai, India, Dec. 2018, pp. 1-6.
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7. **Jagath Vallabhai Missula**, Ravindranath Adda, Praveen Tripathy, "**Five-Level ANPC Converter for PMSG Based Wind Power System with Grid Power Factor Regulation**," in *Proc. 20th National Power Systems Conf. (NPSC)*, Tiruchirappalli, India, pp. 1-6, Dec.2018.
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Journal Under Review

1. **Jagath Vallabhai Missula**, Ravindranath Adda, Praveen Tripathy, "**DC-Link Capacitor Voltage Balancing and Ripple Reduction in SRF-dq Controlled Single-Phase ANPCI by Employing External Chopper Circuit**," in *IEEE Trans. Power Electron.*

Journal Under Preparation

1. **Jagath Vallabhai Missula**, Ravindranath Adda, Praveen Tripathy, "**Solar and wind power generating system using chopper integrated ANPCI to control grid power factor**".