

**MODELLING AND SIMULATION
OF SHORT CHANNEL JUNCTIONLESS TRANSISTOR
FROM AN ANALOG DESIGN PERSPECTIVE**

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Department of Electronics & Electrical Engineering
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by

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at the



**INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI
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Declaration

This is to certify that the thesis entitled “**Modelling and Simulation of Short Channel Junctionless Transistor from an Analog Design Perspective**”, submitted by me to the Indian Institute of Technology Guwahati for the award of the degree of **Doctor of Philosophy** is a confide work carried out by me under the supervision of **Prof. Roy P. Paily** . The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Dedicated to my Beloved Parents



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Abstract

Conventional planar CMOS transistors on bulk silicon substrate have been a key component in ultra-large-scale integration technology for the past four decades, but are approaching the fundamental physical limits imposed by short-channel-effects (SCEs) and gate oxide tunnelling. Fully depleted multiple-gate-field-effect-transistors (Mug-FETs) have been proposed as an alternative to planar devices mainly because of their robust electrostatic control. However, Mug-FETs too face technological challenges in super-steep doping profile requirement and high thermal budget for sub-20 nm channel length era along with excessive short channel effects. Junctionless transistors (JLT), which do not have any pn junction in the source-channel-drain path can be scaled to lower channel lengths because of lower SCEs and easy fabrication steps. It has homogeneous and uniform doping throughout the source-channel-drain region unlike a junction based (JB) inversion mode (IM) transistor. A JLT demands high channel doping concentration ($\sim 10^{19} \text{ cm}^{-3}$) in the channel region to achieve an acceptable threshold voltage. Despite its high doping concentration, JLT has comparable drain current as JB devices. Therefore, JLT can be a prospective candidate for replacement to conventional Mug-FETs in ultra short channel length regime. In this work, the performances of a JLT for digital and analog applications are analysed; the impact of process variations on electrical performances are studied; the impact of fringing fields due to high-k gate dielectrics on JLT performances are studied; and different techniques namely spacer technology is studied for improvement of SCEs and dual-metal gate, gate-stack technology, and alternate substrate material are employed for better device performances and to improve the lower transconductance, which is a major drawback of a JLT.

We have investigated the analog circuit performance parameters for short-channel n-type double-gate junctionless transistor (DGJLT) with the help of extensive device simulations and compared them with conventional inversion mode counterpart i.e., double gate MOSFET (DGMOS). Among the two devices, DGJLT is more suitable for low frequency, high gain applications while DGMOS is more suitable for high speed applications. Analog performance parameters of an n-type bulk planar junctionless transistor (BPJLT) are investigated and compared with single-gate silicon-on-insulator (SOI) JLT. DGJLT is also investigated for possible low voltage applications. The impact of process induced variations and temperature on the electrical characteristics of an n-type junctionless symmetric double-gate transistor (DGJLT) is reported. Electrical parameters of DGJLT are more immune to channel length variations, while DGMOS are immune to silicon and gate oxide thickness variations. JLT offers better overall performance trends with respect to temperature variations, compared to a junction based (JB) transistor.

The analog and circuit performance parameters of a DGJLT as a function of gate dielectric

permittivity (k) are studied and the results are compared with a DGMOS of same dimensions. When the k value is increased, the performances of the JLT device are degraded like its JB counterpart. The effects of spacer dielectric material and spacer width with respect to the digital and analog device performance parameters of a short channel length (L) n-type DGJLT are studied. It is concluded that, as far as I_{ON}/I_{OFF} ratio is concerned, low- k gate oxide combined with high- k spacer dielectrics offers the best performance. As a solution to SCEs because of high- k gate dielectrics, hetero dielectric DGJLT with inclusion of spacers is suggested to improve the overall analog circuit performance. We also studied the effects of fringing field of high- k gate insulator and spacer dielectrics on the device performance parameters of a short channel length (L) p-DGJLT. Both n and p-channel DGJLT show similar performance trends in presence of high- k gate dielectrics and spacer dielectrics unlike a tunnel FET (TFET) where the trends are reported to be opposing.

We suggest a high- k spacer incorporated in a dual-material gate symmetric double-gate junctionless transistor (DGJLT) architecture, forming DMG-SP DGJLT. However, from fabrication point of view, it is somewhat challenging to realize. DMG-SP offers superior transconductance, early voltage and intrinsic gain compared to dual-material gate (DMG) and single-material gate (SMG) DGJLT. An electrostatic potential model for shorter-channel length dual-material gate DGJLT valid in subthreshold region is developed to support our simulation results. The model is in good agreement with the TCAD results. Combining the advantages of dual material gate along with double-layer gate-oxide stack, we propose a junctionless architecture called DM-DGS DGJLT. DM-DGS also offered marginally better transconductance, early voltage and intrinsic gain compared to DMG and SMG DGJLT.

Channel potential and a drain current model for shorter-channel length symmetric double-gate junctionless transistor are developed. Subthreshold slope and drain induced barrier lowering are extracted from this model. Assessment of the model with TCAD simulations confirms its validity for all regions of operation i.e., from subthreshold to accumulation region. Finally, simple fabrication steps are suggested for DGJLT using Genius device simulator from Cogenda TCAD vendor.

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Nomenclature

BJT	Bipolar junction transistor
BPJLT	Bulk planar junctionless transistor
BTBT	Band to band tunnelling
CLM	Channel length modulation
CMOS	Complementary metal oxide semiconductor
DIBL	Drain induced barrier lowering
DGJLT	Double-gate junctionless transistor
DGS	Double-layer gate stack
DGMOS	Double-gate metal-oxide-semiconductor
DM	Dual material
DMG	Dual-material gate
DRAM	Dynamic read only memory
EOT	Effective oxide thickness
GAA	Gate all around
Ge/Si	Germanium/Silicon
GIDL	Gate induced drain leakage
HG JLT	Hetero-gate-dielectric double-gate junctionless transistor
IM	Inversion mode
ITRS	International roadmap for semiconductors
JB	Junction based
JLT	Junctionless transistor
LPCVD	Low pressure chemical vapor deposition
MOSFET	Metal-oxide-semiconductor field-effect transistor
Mug-FET	Multiple-gate field-effect transistor
PVD	Physical vapour deposition
RF	Radio frequency
RIE	Reactive ion etching
SCE	Short channel effects
SEM	Scanning electron microscope
SOI	Silicon on insulator
SS	Subthreshold swing
SP	Spacer
TCAD	Technology computer aided design
TEM	Transmission electron microscope
TFET	Tunnel field-effect transistor

Chapter 1

Introduction

Over the past two decades, the computing and communication technologies have played as driving forces in the world economy. About more than 10% of the world economy is built on electronics market and this percentage is continuously growing. This revolution in semiconductor industry started from the invention of the first solid-state device, a bipolar point-contact transistor on Germanium (Ge) substrate, invented by Bardeen, Brattain, and Shockley at Bell labs in 1947. Complementary metal-oxide-semiconductor (CMOS) field-effect-transistor has almost replaced bipolar transistor because the former offers lower power and technology advantages. In 1965, Gordon Moore predicted that the number of transistor per chip would double every 18 months with improved characteristics [1]. As shown in Fig. 1.1, interestingly, this rule has been by now proved over 5 decades by semiconductor manufacturing industry. However, with the continuous miniaturization of the transistor dimensions, to achieve more dynamic read only memory (DRAM) chip density and more microprocessor speed, the conventional single gate MOSFETs are finding it difficult to cope up with the desired performance due to short channel effects and gate leakage currents. The challenges of scaling the device below 22 nm technology node can broadly be categorized into five groups, which are gate control, current output, capacitance, power/performance ratio, and variation/reliability. The gate control challenges consist of “short-channel effects” (SCEs) (SCE includes subthreshold slope degradation, drain induced barrier lowering, gate induces drain leakage), source to drain direct tunnelling and gate oxide tunnelling etc., which lead to an unacceptable leakage and subthreshold characteristics. In order to boost the device performance for every technology generation, the current delivered through the channel has to be increased. Mobility enhancement through strained silicon, different channel orientations or even alternate channel materials, such as III-V and germanium are some methods introduced by industry. To switch the transistors faster, the capacitance elements namely, under-lap capacitance, channel capacitance, junction capacitances (both gated edge and area) and the inner and outer fringe capacitances have to be minimized; which is again a challenging task at reduced dimensions. Below 65 nm technology regime itself, power density contribution from passive network is becoming very significant and cannot be neglected in comparison to the active power density where most modern applications demand low power consumption. Also, ultra short channel length, thin device layer and highly doped substrate devices do face giant device variability and reliability issues.

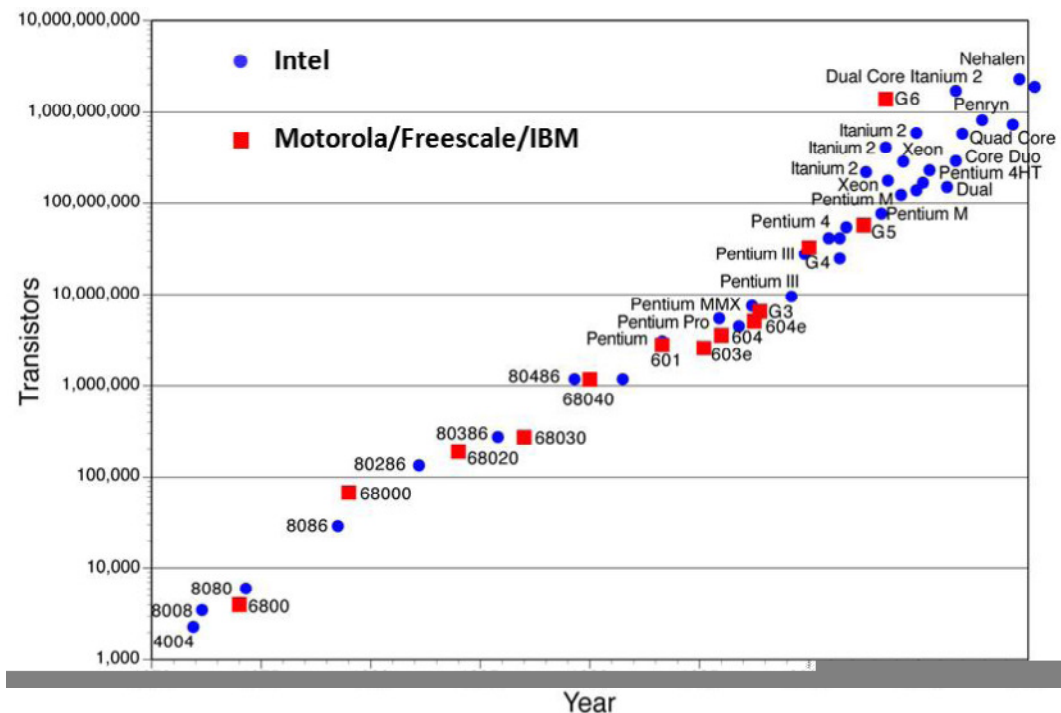


Figure 1.1: Illustration of Moore's law: transistor counts (number) against dates of introduction. The curve shows counts doubling every two years [2].

Fully depleted (FD) silicon on insulator (SOI) MOSFETs are very promising candidates for sub 100 nm ultra large scale integration (ULSI) because it is suitable for low power and high performance applications. However, it demands (1) ultra-thin semiconductor films (2) elevated source and drain, to reduce series resistance and (3) mid-gap gate, to balance the lowering of threshold voltage. Also, another lapse of the FD-SOI is the field penetration beneath the channel from source and drain through buried oxide (BOX) and substrate, at higher drain voltages. Multigate silicon-on-insulator (SOI) MOSFETs (Mug-FETs) have come into picture for further downscaling of MOSFETs, as these devices have more control on the electrostatics of the channel region because of the more number of gates. Fig. 1.2 shows the schematic view of the bulk, planar SOI MOSFET, and the multi-gate FETs (MuGFET) such as FinFET, tri-gate, pi-gate, omega-gate and gate-all-around SOI (GAA) devices along with “effective” number of gates for each device [3-8]. Also, Mug-FETs which do not need high channel doping concentration, improve SCEs, increase the carrier mobility and reduce the device variability coming from random dopant fluctuations. Also, Mug-FETs improve SCEs by scaling the thickness of the channel rather than scaling the oxide dielectric. Therefore, gate tunneling current can also be reduced. Because of the above advantages, Mug-FETs are predicted as a successor of planar transistors by the International Roadmap for Semiconductors (ITRS) since 2001 [3]. Unfortunately, in sub-20 nm era, the channel region is not only controlled by the gate but rather by the undesired source and drain regions. Thus, even though SCEs are reduced to some extent, it is not nullified even in with Mug-FET. Very abrupt source and drain junctions requirement of these ultra-short length devices put

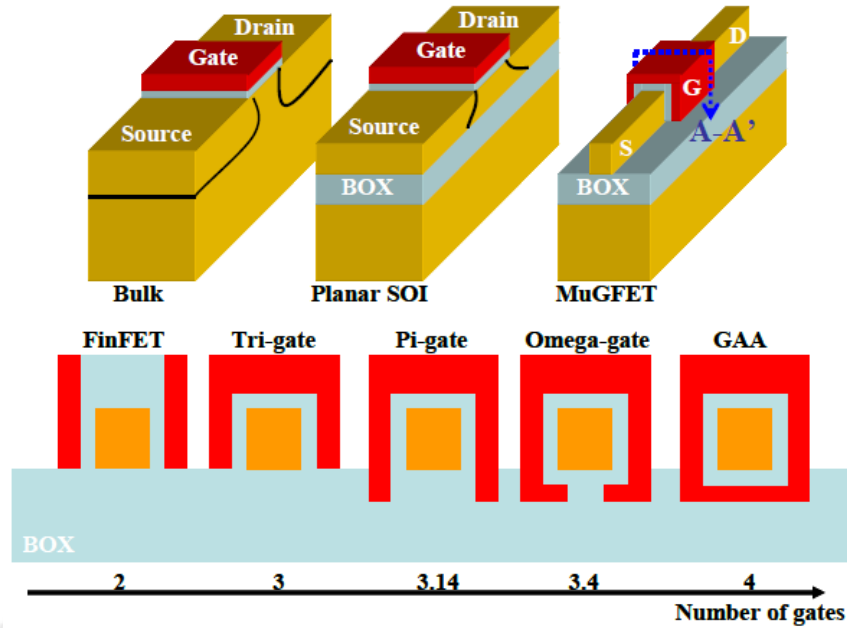


Figure 1.2: Schematic of bulk, SOI and MuGFET with cross-section of MuGFET and corresponding “effective” number of gates. This Fig. is adapted from [9].

challenges in doping profile techniques. For example, a typical n-channel MOSFET has doping concentration of 10^{20} cm^{-3} in the source/drain region and 10^{15} cm^{-3} - 10^{16} cm^{-3} in the channel region. Now, to form a junction within a nanometer or fraction of a nanometer or so (theoretically abruptly), with few orders of concentration gradient, is extremely tedious and needs technology breakthrough because of the restrictions in laws of diffusion and statistical nature of the distribution of the doping atoms. Also, very high thermal budget is involved with this process. Flash annealing techniques are now used for heating silicon for a very short duration to minimize diffusion. However, even in total absence of diffusion, ion implantation and other doping techniques cannot achieve perfectly abrupt junctions with many orders of concentration gradient [10]. Thus, even with Mug-FETs, the material and/or device properties have reached fundamental limits in deca-nanometer era [11-13]. Also, SCEs make transistors slower by lowering the maximum switching speed. Tunnel FET (TFET) is studied extensively because it offers ultra-small SCEs; however it has low ON-state current [14-15]. Single-electron transistor [16] and carbon nanotube [17-18] have been extensively studied as an alternative to conventional transistors in sub-20 nm regime. However, with present available technology, they are rather complicated to fabricate cost effectively for commercial use.

1.1 Conventional MOSFETs

A conventional MOSFET has four terminals namely, source, drain, gate and substrate and is composed of five regions namely, source, drain, gate, substrate and oxide region (Fig. 1.3). For an n-

type MOSFET, substrate is doped with p-type impurity and source/drain region is doped with n-type impurity. For p-type MOSFET doping impurity is just reversed. Generally, the workfunction of substrate region is similar to source/drain region. N^+ / P^+ polysilicon is used as a gate material for n-type/ p-type MOSFET respectively. In general, source is connected to zero or lowest potential. The most common gate oxide material is SiO_2 , which forms an excellent interface with silicon material. However, to prevent gate leakage current, high-k (k is gate dielectric constant) gate dielectrics (e.g. HfO_2 , ZrO_2 etc) are used. When gate to source voltage (V_{GS}) is negative (taking $V_{DS} = 0$ V); holes, which are majority carrier in substrate region, are accumulated in the Si- SiO_2 interface. This is called accumulation of holes in the surface of substrate region. When V_{GS} approaches toward zero potential, the holes start disappearing; and at a particular V_{GS} , all holes disappear from the surface. We call the band as “flat band region” and the particular V_{GS} as “flat band voltage”. Now, if we increase the V_{GS} towards positive voltage, holes are repelled from surface leaving immobile negative charges. With increase in V_{GS} , if the potential created by the immobile negative charges is such that it is equal to the potential in the source-channel pn junction barrier potential, electrons can now flow from source to silicon surface. As the number of electron flowing is less at this stage, the current is also of smaller amount. Rather, we say the channel is “weakly inverted”. With increase in V_{GS} , the electron flow is higher and higher (with $V_{DS} > 0$ V). Successively, we call channel to be “moderately inverted” and “strongly inverted” and adequate current flows from drain to source region [17-23].

1.2 Short Channel Effects in Conventional MOSFETs

It is understood that drain current (I_D) in a MOSFET increases with decrease in channel length (L). Also, intrinsic capacitance decreases with lower L, which makes it easier to switch. However, when L decreases, some unavoidable effects namely, short channel effects, channel length modulation, drain induced barrier lowering, mobility degradation with vertical field, velocity saturation etc. come into play. We will discuss them qualitatively as below. Researchers have tried to reduce them through different techniques like gate engineering, channel engineering, implementing different architectures with different working physics etc. Though they are able to reduce it to some extent, it is extremely difficult to nullify these effects in ultra short channel lengths with a single gate control on the silicon region [19].

1.2.1 Short Channel Effect (SCE)

The short channel effect (SCE) is the decrease of threshold voltage of a MOSFET as the channel length reduces. It is prominent when drain bias is equal to the power supply voltage. The important difference of long and short channel MOSFET is that, in a long channel MOSFET, the electrostatics

of the channel region is controlled by the gate; however, for short channel MOSFET, besides gate, source and drain regions also try to control the channel electrostatics. Therefore, it is now a 2D problem instead of 1D that is valid for a long channel MOSFET. The charge sharing from source and drain regions decreases the threshold voltage of the device [19].

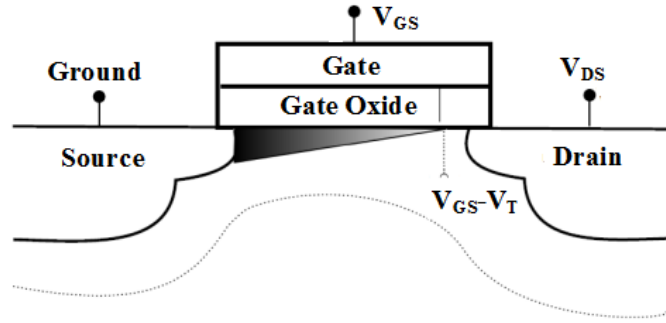


Figure 1.3: Schematic illustrating the channel length modulation affects. It can be seen here that when the drain voltage applied is above $V_{GS} - V_T$, the drain side of the channel is pinched-off resulting in channel length modulation.

1.2.2 Channel Length Modulation (CLM)

When drain to source voltage, $V_{DS} > V_{GS} - V_T$, I_D is relatively constant and we say the device operates in saturation region. The local density of inversion layer charge ($Q_d(x)$) is proportional to $V_{GS} - V(x) - V_T$, where $V(x)$ is the channel potential at x (x is along the channel direction). Thus, if $V(x)$ approaches $V_{GS} - V_T$, then $Q_d(x)$ drops to zero. This implies that if V_{DS} is slightly greater than $V_{GS} - V_T$, the inversion layer stops at $x \leq L$ and we say the channel is “pinched off”. If V_{DS} is increased further, the point at which Q_d is equal to zero approaches towards source (say, new position of Q_d is L'). Therefore, at some point along the channel, the local potential difference between the gate and the oxide-silicon interface is not sufficient to support an inverted channel (Fig. 1.3). That is, the actual length of the inverted channel gradually decreases as the potential difference between gate and drain increases. In other words, L' is a function of V_{DS} . This effect is called channel length modulation. This phenomenon results in a nonzero slope in the saturation region of I_D/V_{DS} characteristic [19-25].

1.2.3 Drain Induced Barrier Lowering (DIBL)

This phenomenon happens when gate voltage is lesser than the threshold voltage of the device. When drain and source voltages are equal, the depletion region beneath the source and drain are equal as they are equally doped. Now, with increase in V_{DS} , the depletion region below the drain region is more to compensate with the extra potential connected to drain. For short channel length devices, the electrostatics is not only controlled by the gate but also by the source and drain regions. The charges

in the drain region contribute to the depletion potential and the barrier between source and channel region decreases. As a result, threshold voltage decreases. This phenomenon is called drain induced barrier lowering. It is determined as the threshold voltage difference when V_{DS} changes from 50 mV to 1 V [19-25].

1.2.4 Velocity Saturation

The mobility of the carriers depends on the lateral electric field as well. It begins to drop as the field reaches a value of 1 V/ μm . Thus, the carrier velocity, $v (= \mu E)$ reaches a saturated value ($\sim 10^7$ cm/s) for sufficiently high fields along the channel at some point. The parameters, μ and E are the carrier mobility and low electric field respectively. The current thus produced linearly proportional to overdrive voltage and does not depend on length [19-25].

1.2.5 Hot Carrier Effects

With high drain to source voltage, short-channel MOSFETs may experience a high lateral electric field. Even though, average velocity of carriers saturates at high fields, the instantaneous velocity and therefore the kinetic energy of carriers continue to increase especially when they accelerate towards drain [19-25].

1.2.6 Gate Oxide Leakage

SiO_2 is a very popular gate insulator used in MOSFET because of its excellent interfacing capability with silicon material. However, because of dimension scaling for improved device performances, gate oxide thickness has already reached ~ 1 nm or below. When the gate oxide thickness is below 2-3 nm, tunneling probability increases, which results in an increase of oxide leakage current. High- k dielectric materials are used to reduce the direct tunneling leakage current [19-25].

1.2.7 Gate Induced Drain Leakage (GIDL)

With a high drain bias and a low gate voltage, the electric field in the gate/drain overlap region is high. Therefore, in the overlap region, there exists a band overlap between the valence band of the drain to the conduction band of the drain which activates band-to-band tunneling probability between the valence band and conduction band of the drain. The electron and hole pairs thus generated due to band to band tunneling may sweep to the drain and substrate regions. This phenomenon is called gate induced drain leakage [21-22].

1.2.8 Surface Scattering

As the channel length becomes smaller, due to lateral extension of the depletion layer into the channel region, the longitudinal electric field increases and the surface mobility becomes field-dependent. In the saturated or strong inversion region, the carriers are confined within the narrow inversion layer in a MOSFET. The carriers experience collisions suffered by the electrons that are accelerated toward the interface and drain by vertical electric field. This is called surface scattering which causes reduction of the mobility and this in turn affects both the drain current and transconductance [19-22].

1.2.9 Impact Ionization

The high velocity of electrons in presence of high longitudinal fields that can generate electron-hole pairs by impact ionization, that is, by impacting on silicon atoms and ionizing them. The situation can be even worst if some electrons generated due to high fields escape the drain field to travel into the substrate, thereby affecting other devices on a chip [19].

1.3 Junctionless Transistor (JLT)

The existing metal-oxide-semiconductor field-effect transistors are composed of pn junctions in the source-channel-drain path. The pn junctions allow or block current through it according to the applied bias on the gate. Junctionless transistor (JLT), which does not have pn junction in the source-channel-drain path (Fig. 1.4), has recently been reported by Colinge's group at Tyndall National Institute, University College Cork, Ireland [26] following the idea of the first transistor by Julius Edgar Lilienfeld in 1925 [27-28]. Lilienfeld patented his work under the title "Device for controlling the

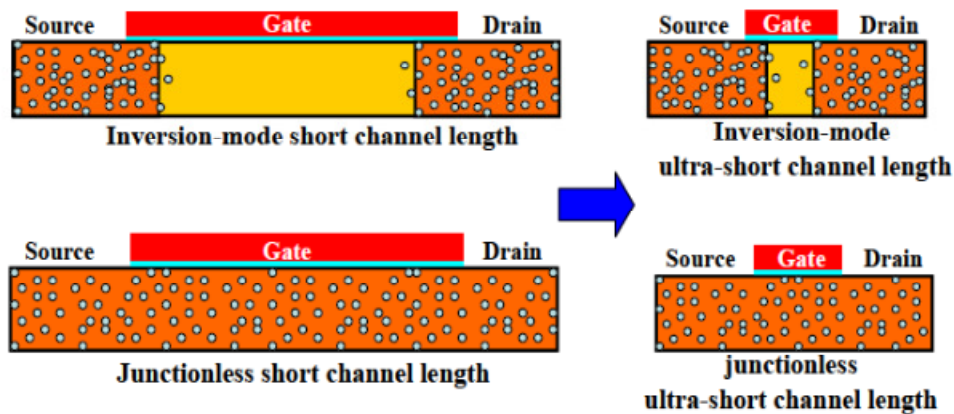


Figure 1.4: Source and drain doping of inversion-mode and junctionless transistor with short channel and ultra-short channel. This Fig. is taken from [9].

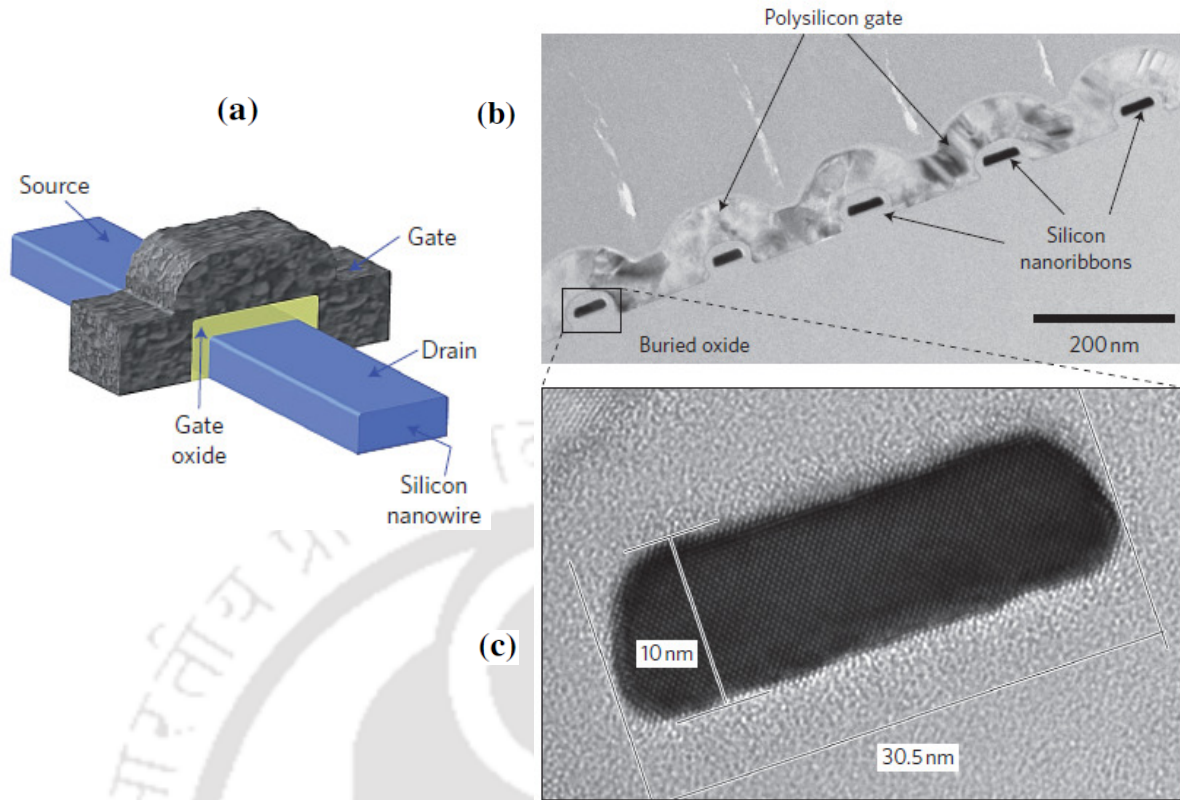


Figure 1.5: (a) Schematic of an n-channel nanowire transistor (Trigate structure). Buried oxide is not shown. (b) transmission electron micrograph (TEM) of silicon gated resistor nanoribbons of five parallel devices with a common polysilicon gate electrode (c) Magnification of a single nanoribbon device [26].

electric current”. It consists of a thin semiconductor film deposited in a thin insulator layer, itself deposited in a metal electrode (gate). Thus, it does not have a junction; rather it is a simple “resistor”. It is also called “gated trans-resistor”. In principle, current flows in the resistor in the same way that drain current flows from drain to source in a MOSFET. Junctionless transistor is basically an accumulation mode device with a very thin silicon thickness ($\sim 5\text{--}10\text{ nm}$). The requirement of thin semiconductor layer is to have full depletion of carriers when the device is turned off. Therefore, JLT offers good subthreshold characteristics. However, a typical accumulation mode device is made in relatively thick silicon films (typically higher than 20 nm or so) and hence it exhibits worst short channel performances. However, one advantage of accumulation mode transistor is, drain current varies less with channel doping concentration. The other major difference of JLT with accumulation mode transistor is that in the former, accumulation of carriers happens at a higher threshold voltage than the later device. The junctionless transistor which is also called “gated resistor” or “nanowire pinch-off FET” is highly doped (typically $\sim 8 \times 10^{18}\text{ cm}^{-3}$ to $8 \times 10^{19}\text{ cm}^{-3}$) to have an acceptable drain current. Commonly, a junctionless transistor has same doping concentration at source, channel and

drain regions. Thus, the structure of a JLT is $N^+ - N^+ - N^+$ for n-channel and $P^+ - P^+ - P^+$ for p-channel in the source-channel-drain region. P^+ and N^+ polysilicon gates are used for n and p channel JLT respectively (N^+/P^+ denote highly doped with N/P-type dopants respectively). However, non-uniform doping in JLT has also been reported; to obtain superior ON-state to OFF-state current ratio (I_{ON}/I_{OFF}) compared to uniformly doped JLT [29].

JLTs have many advantages over conventional MOSFETs such as – better SCE performance (reduced drain induced barrier lowering (DIBL) and subthreshold slope (SS) degradation) resulting better scalability, lesser sensitive to doping fluctuations and negative bias thermal instability, greatly simplified process flow and low thermal budgets after gate formation resulting in flexibility in the choice of materials for gate dielectric and gate metal etc. [26, 30-32]. Because of uniform and homogeneous doping in the channel region, a JLT eliminates the subsequent annealing process and the device can be fabricated with shorter channel lengths. In addition, JLTs offer low standby power operation and low gate induced drain leakage [30, 33-34]. Also, lesser fabrication steps reduce process cost significantly compared to junction based devices of similar dimension [35]. JLTs exhibit lesser random telegraph-noise [36] and $1/f$ noise [37]. JLT has fully CMOS compatibility. With constant device dimensions scaling, the effective gate oxide thickness decreases. This increases vertical electric field according to Takagi et al.'s relation $\mu \approx E^{-0.3}$ [38-39]. The inversion carrier mobility in a conventional MOSFET is reduced because of vertical electric field. For example when technology node changes from 0.8 μm to 0.13 μm , mobility decreases from 400 to 130 cm^2/V . The vertical electric field in a JLT is much lower compared to junction based MOSFET and accumulation mode devices as discussed below. Therefore, mobility in a JLT is not reduced much because of vertical electric field [40]. The conventional junction based device is normally an OFF device, as the drain junction is reverse biased. It prevents current flowing through the device. To turn the device on, an inverted channel is created by applying a gate bias. However, a JLT is normally an ON-device. The workfunction difference between the gate electrode and silicon nanowire (~ 1.1 eV) shift the flatband voltage and turns the threshold voltage into a positive value. In the ON-state, the device is in flatband condition. Therefore, there is zero vertical electric field perpendicular to the current flow. Unlike in a junction based transistor where conduction mechanism is surface based; in a JLT, current basically flows through bulk conduction mechanism. The threshold voltage depends on doping, equivalent oxide thickness as well as on the width and thickness of the nanowires [41]. In a JLT, the OFF-state current is determined solely by the electrostatic control of the gate and not by the leakage current as is the case for junction based device. This makes JLT lesser sensitive to contamination [30]. Junctionless transistor is studied theoretically with single, double, triple and gate-all-around architectures; and fabricated with triple and gate-all-around architectures. Fig. 1.4 (a) shows the schematic of first fabricated nanowire transistor (Trigate structure) along with (b) transmission electron micrograph (TEM) of silicon gated resistor nanoribbons of five parallel devices with a

common polysilicon gate electrode [26].

However, along with the many advantages that JLT offers as aforementioned, it has some disadvantages as well. One of the most important drawback of JLT is it suffer from lesser ON-state current (I_D) and hence transconductance (G_m) compared to IM MOSFETs due to its inferior mobility (due to high doping concentration (N_D) in channel region) [42]. Also, to have a highly doped uniform channel with such small thickness ($\sim 5\text{--}10\text{ nm}$) is extremely challenging and expensive for non planer kind of structure. The higher channel doping concentration to accomplish higher ON-state current makes threshold voltage variation with doping concentration as well as nanowire width [43-44].

1.4 Review of Junctionless Transistor

Many reports on junctionless transistors are available in literature [10, 28-37, 40-95, 130-141]. Colinge et al. have fabricated the junctionless nanowire gated registor successfully [26]. Choi et al. have demonstrated the gate-all-around architecture experimentally [41]. Su et al. have fabricated the gate-all-around junctionless transistor with heavily doped polysilicon nanowire channels [45]. Other JLT architectures reported include trigate nanowire architectures with bulk substrate [10], double-gate architecture [46-48] and bulk planar architecture [49]. JLTs show larger threshold voltage variation with temperature than classical MOSFETs though JLT MugFET devices present excellent properties for high temperature applications [42]. Also, JLTs suffer from threshold voltage variation with random dopant fluctuations than inversion mode (IM) counterpart [44]. Choi et al. reported the sensitivity of threshold voltage to nanowire width variation for gate-all-around junctionless transistor (GAA JLT) [41]. They found that V_T variation with silicon thickness (T_{si}) is more in GAA JLT than IM counterpart. Also, SOI based ultra-small nanowire JLTs require aggressive scaling of the film thickness ($\sim 10\text{ nm}$) and channel width ($\sim 5\text{ nm}$); which is technologically so challenging to be cost effective. Also, nanowire JLT is a nonplaner structure. Gundapaneni et al. [49] reported a bulk planer JLT (BPJLT) which does not have pn junction in the source-channel-drain path; however it has a junction in the vertical direction for isolation purposes. It has better scalability and controllability for tuning the device performance compared to SOI device of same dimension and material properties. Though such a structure is fully compatible with standard planer CMOS process flow, with a single gate device it is somewhat difficult to fully deplete the channel in the OFF-state. Also, the ON-state current achieved from a single-gate MOSFET cannot reach ITRS guideline. Rios et al. fabricated the trigate nanowire JLT with gate length down to 26 nm and compared with junction based transistor of same dimension [50]. Ghosh et al. reported a hetero-gate-dielectric double-gate junctionless transistor (HG JLT), with high-k gate insulator at the source-side and a low-k gate insulator at the drain side. This reduces the effects of band-to-band tunneling in subthreshold region [51]. The authors also proposed a HG tunnel FET, which enhances the ON-state current and I_{ON}/I_{OFF} ratio and suppresses

ambipolar behavior. Gundapaneni et al. estimated the OFF-state leakage current in a hetero-gate-dielectric JLT and proposed a design guideline for reducing band-to-band tunneling [52]. Lou et al. reported that a junctionless transistor with a dual material gate which enhances I_{ON} -state current, I_{ON}/I_{OFF} ratio, transconductance, unity gain frequency and reduced drain induced barrier lowering [53]. Koukab et al. proposed a design trade-off between speed and switching power performances in regard of the JLT parameters [54]. Gnani et al. reported that the global amount of electronic charge within a depletion device is less than that within a fully depleted nanowire of same geometry [55]. Also, impurity scattering affect the carrier mobility. Both factors affect the ON-state current of a JLT. Doria et al. reported that JLT has improved early voltage and intrinsic gain compared to inversion mode counterpart of same dimension [33]. Ansari et al. did the atomic level design factors such as dopant positioning and concentration for a 3 nm gate length junctionless nanowire transistor [56]. Yan et al. realized a diode with a junctionless transistor and they found that the characteristics of the diode are identical to the normal pn junction diode [57]. Singh et al. found that irrespective of doping concentration level in the channel, gate-all-around JLT is found to have almost 5 orders of magnitude lower spectral noise [58]. Also, low frequency noise is less sensitive to gate bias voltage and to the frequency than IM device. Colinge et al. reported that JLT can have a significantly lower Miller capacitance, which might be of great interest for RF applications [59]. Han et al. compared the performances of bulk FinFET and SOI JLT with the help of 3D quantum device simulations. Bulk FinFETs showed higher I_{ON}/I_{OFF} current ratio, better SCEs compared to SOI JLT [60]. There are many reports on analytical modeling of JLT as well [46, 48, 61-71], mostly are for long channel JLT [46, 48, 61-68]. The proposed models for short-channel JLT mainly address the subthreshold region only [69-71]. There are a very few reports on the modeling of short channel double/multigate JLT.

1.5 Motivation and Problem Statement

Out of different architectures reported for JLT; namely, bulk planar, single-gate, double-gate, triple-gate and gate-all-around JLT, we have chosen double-gate architecture in this thesis as it is fully depleted in the OFF-state and it offers good gate control in the channel region. Motivated by the fact that majority of the works reported for junctionless transistor are towards digital applications, in this thesis; more emphasis is given for analog applications of the device. Analog circuit performance parameters of short-channel double-gate junctionless transistor (DGJLT) and bulk planar junctionless transistor (BPJLT) are derived with the help of extensive device simulations [72] and are compared with conventional IM counterparts. Though there are reports of process induced variations on the electrical characteristics of a trigate JLT, the same is not reported for DGJLT yet and we present a systematic investigation of the same. Temperature dependence of the analog performance parameters of a DGJLT is not reported yet and therefore we have made a study of the same.

It is understood that though JLT offers many advantages compared to junction-based devices as mentioned above, its transconductance is inferior to the later. Therefore, one of our major focuses is on the improvement of transconductance of DGJLT. Different techniques, such as dual-material gate technology, choice of substrate material and gate stack geometry are investigated for the improvement of transconductance and other analog performance parameters. Further, addition of spacers on both sides of gate oxides gives better electrostatics control.

High-k gate dielectrics are used to prevent leakage currents through the extremely thin gate oxides in today's technology. The effect of fringing fields coming out of high-k gate dielectrics on the analog circuit performances of the device is studied. To reduce the affect of fringing fields on device performace, hetero-gate-dielectric technique (different gate dielectric at source and drain side) is utilized. There are no analytical models for dual-material DGJLT yet. An analytical potential model of the device valid at subthreshold region for short-channel DGJLT is developed. Though there are many analytical models available on JLT, only few are reported for a shorter-channel device. Analytical models valid from subthreshold-to-accumulation regions for shorter-channel DGJLT are rare. Models for the channel potential and the drain current of a shorter-channel length DGJLT are derived, and the threshold voltage and drain induced barrier lowering values are extracted. Possible fabrication steps for DGJLT are suggested using Genius TCAD simulator [73].

1.6 Summary of Contributions and Results

A brief description of major contributions is as follows.

- **Analog/Digital Performance of Different short-channel JLT Architectures**

Analog circuit performance parameters of a shorter-channel n-channel double-gate junctionless transistor are investigated here with the help of extensive device simulations and compared with conventional inversion mode counterpart, i.e., double-gate MOSFET. The analog performance parameters of an n-channel bulk planer junctionless transistor is also studied and compared with single-gate silicon-on-insulator JLT.

- **Estimation of Process-Induced Variations in DGJLT**

The impact of process induced variations on the electrical characteristics of an n-channel junctionless symmetric double-gate transistor is reported. The process parameters considered here are gate length (L), thickness of silicon film (T_{si}) and gate oxide thickness (T_{ox}). The impact of these process parameters on the electrical parameters viz., ON-state current (I_{ON}), threshold voltage (V_T) and subthreshold slope (SS) are systematically investigated with the

help of extensive device simulations. Temperature dependence of the electrical characteristics of an n-channel DGJLT is also investigated.

- **Impact of Fringing Fields on the Device and Circuit Performances of a JLT and High-k Spacer as a Solution**

The immunity of device and circuit performance parameters of a DGJLT as a function of high-k gate dielectric permittivity was studied and compared with a DGMOS of same dimensions. To reduce the affect of fringing fields because of high-k gate dielectrics and to improve the overall analog circuit performance, hetero-gate-dielectric DGJLT (HG-DGJLT) is suggested.

- **Impact of High-k Spacers on Device Performance of n and p-channel DGJLT**

High-k spacers are added on both sides of the gate oxides of the DGJLT to have better improved SCEs and other device performances. The effect of spacer width on device performance has also been studied. The effects of fringing field of high-k gate insulator and spacer dielectric on the device performance parameters of a p-channel DGJLT is investigated and trends are compared to n-channel device.

- **To Improve the Transconductance and other Device Performances of a DGJLT**

High-k spacer is incorporated in a dual-material gate symmetric double-gate junctionless transistor architecture forming DMG-SP DGJLT for improved transconductance. The results are compared with dual-material gate (without spacer) and single-material gate (without spacer) DGJLT. An electrostatic potential model for dual-material gate DGJLT valid in subthreshold region is derived to validate our demonstration taking vacuum as spacer material. Combining the advantages of dual material (DM) gate along with double-layer gate-oxide stack (DGS), we propose a junctionless architecture called DM-DGS DGJLT to improve the transconductance and analog performance. Germanium is studied as a substrate material in place of silicon for BPJLT architectures to improve the mobility and hence transconductance of the device.

- **Channel Potential and Drain Current models for shorter-channel length DGJLT**

Despite some similarities with conventional MOSFETs, the charge-potential relationship is quite different in a junctionless transistor, due to its different operational principle. A

channel potential and drain current model is formulated for shorter-channel length symmetric double-gate junctionless transistor (DGJLT) from two dimensional Poisson's equation using "Variable separation technique". The developed model captures the physics in all regions of device operation i.e., depletion to accumulation region without any fitting parameter. Threshold voltage and drain-induced barrier lowering values are extracted from the potential model. A drain current model is also derived using surface potential approach. Both potential and drain current model is in good agreement with professional TCAD simulation results.

- **Suggested Fabrication steps for DGJLT**

We have suggested the possible fabrication steps for n-type double-gate junctionless transistor following the fabrication steps used by Colinge's group [26]. We have performed the required process simulation for obtaining DGJLT structure and its electrical characteristic in VisualFab, Gds2Mesh, VirtualTCAD and 3D Genius device simulator from Cogenda [73]. Cogenda is an established vendor of Technology Computer Aided Design (TCAD) software both in process and device simulation in different parts of the world accepted by leading researchers.

1.7 Organization of the Thesis

The works presented in this thesis has been organized as follows.

- In chapter 1, we have presented introduction and motivations of our research work. Additionally, an overview of thesis contributions is presented in this chapter.
- Chapter 2 includes the simulation of analog and digital performance of different JLT architecture (double-gate and bulk planer JLT) and their comparison with respective conventional junction based transistors counterpart.
- Chapter 3 presents the effects of process induced variations and temperature on the DGJLT performances.
- The impact of fringing field on device and circuit performances is explained in chapter 4.
- High-k spacers are studied for improved SCEs and analog performances of n and p-channel DGJLT in chapter 5.
- High-k spacer is incorporated in a dual-material gate symmetric double-gate junctionless transistor architecture forming DMG-SP DGJLT to improve transconductance in Chapter 6. This chapter also includes a dual material double-layer gate stack junctionless transistor and use of germanium-substrate for enhanced analog performance.

- In chapter 7, the semi-analytical model for potential and drain current of shorter-channel length DGJLT is developed.
- Possible fabrication steps are suggested for a DGJLT in chapter 8.
- Finally, conclusion and future direction of research work are included in chapter 9.



Chapter 2

Estimation of Analog, Digital and Low Power Performances of Junctionless Transistor (JLT)

2.1 Introduction

Metal-oxide-semiconductor field-effect transistor (MOSFET) has been the unavoidable component in modern day electronic equipments for more than four decades now, without which we cannot think of a modern day life. From laptops or iPhone, medical equipment or modern satellites, almost everywhere these semiconductor devices have been used. The silicon-based CMOS technology has played a dominant role over other transistor technologies, e.g. bipolar, BiCMOS device technologies, because of the simple fabrication process steps, low power consumption, and high layout density offered by the CMOS technology. Junctionless transistor (JLT), which is compatible with CMOS process technology, has recently been explored as a promising candidate in sub-20 nm era due to its junction free nature of the source-channel-drain path and easy fabrication process steps. There are many reports on the advantages of it compared to its inversion mode counterpart in regard of digital applications along with other performances. However, there are fewer reports on analog performances of a JLT [33-34, 47]. Therefore, we are interested in estimation of analog performances of a shorter-channel length double-gate JLT (DGJLT). The analog performance parameters namely drain current (I_D), transconductance (G_m), transconductance/drain current ratio (G_m/I_D), early voltage (V_{EA}), drain output conductance (G_D), output resistance (R_O), intrinsic gain ($G_m R_O$), gate to source capacitance (C_{GS}), gate to drain capacitance (C_{GD}) and unity gain cut-off frequency (f_T) of a DGJLT are systematically investigated for n-type DGJLT with the help of extensive device simulations and compared with conventional inversion mode counterpart i.e., double-gate MOSFET (DGMOS) of similar dimension.

Bulk planar junctionless transistor (BPJLT) is claimed to have better SCE performance, more scalability and easy fabrication process compared to single-gate SOI JLT by Gundapaneni et al. [49] as mentioned in chapter 1. They claimed performance of BPJLT is better than single-gate SOI JLT in

regards to digital performances. Here, the circuit performance parameters of BPJLT are studied and compared with SOI JLT.

We are in an era where customers of electronic gadgets, always look for low power consumption of the product. So, it is of high concern to operate the device at lower supply voltage. However, there are rare reports on low power operation of JLT. Recently, Ghosh et al. have reported the ultra low-power analog/RF applications of JLT [47]. They found that JLT has much higher performance compared to inversion mode counterpart in regard of analog/RF applications. However, there are no reports on low power operation of JLT for digital applications yet, to best of our knowledge. Here, we report a systematic study for digital performance parameters of a shorter-channel DGJLT at lower supply voltage and performed its comparison with inversion mode counterpart.

2.2 Double-Gate JLT (DGJLT) for Analog Applications

2.2.1 Device Structure and Operation of DGJLT

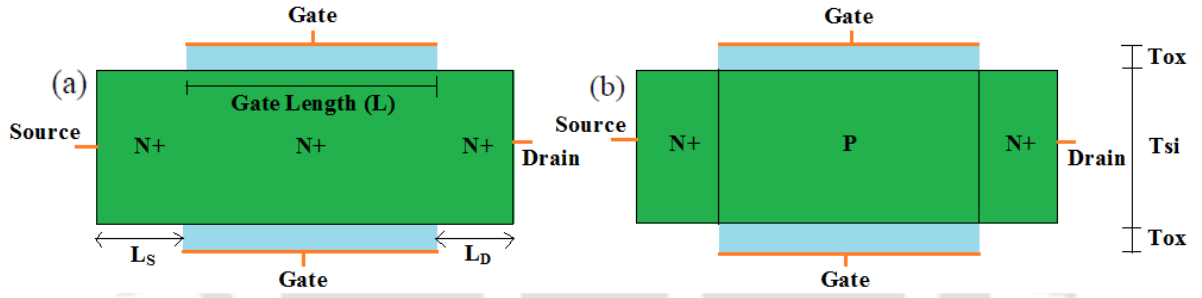


Figure 2.1: Cross-sectional view of n-channel (a) junctionless (DGJLT) (b) conventional inversion mode symmetric double-gate transistor (DGMOS).

Fig. 2.1 (a) and (b) show the device structures for DGJLT and DGMOS respectively. A DGMOS transistor has two pn junctions i.e., source-substrate and drain-substrate in source-channel-drain path and an n-type DGMOS has $N^+ - P - N^+$ structure where current conduction is due to the inverted carriers in the channel region. N^+ means channel is highly doped with boron atoms. A DGJLT has same structure as DGMOS transistor with the exception that there is no pn junction in the source-channel-drain path i.e., an n-channel device has $N^+ - N^+ - N^+$ structure and p-channel device has $P^+ - P^+ - P^+$ structure. It has uniform doping throughout the source-channel-drain region, where only majority carriers carry the current. Unlike a conventional DGMOS, where the channel is lightly doped or undoped, the channel region of a JLT is highly doped ($\sim 8 \times 10^{18} - 8 \times 10^{19} \text{ cm}^{-3}$) to attain an appreciable drain current. A JLT uses P^+ polysilicon as gate material for n-channel device and N^+ polysilicon for p-channel device respectively. Metal gate can also be used as a gate material. For a JLT, the workfunction difference between silicon layer (n-channel region) and metal gate (Φ_{MS}) is given by

$$\Phi_{MS} = \Phi_M - \left(\chi + \frac{E_g}{2} - kT \ln \left(\frac{N_D}{n_i} \right) \right) \quad (2.1)$$

Interface charges are neglected. Where, χ is the electron affinity and E_g is the band-gap energy of silicon, k is Boltzman's constant and T is temperature. N_D and n_i are the channel doping concentration and intrinsic doping concentration respectively. For example, with $N_D = 1 \times 10^{19} \text{ cm}^{-3}$, the workfunction difference, $\Phi_{MS} \sim 1.12 \text{ eV}$. Therefore, even without any gate bias, the channel region of JLT is fully depleted because of this workfunction difference. For this to happen the channel region of JLT is kept thin. Therefore, current conduction mechanism in JLT is different than inversion-mode and accumulation-mode transistor. In an inversion-mode transistor, with applied gate voltage, the channel is weakly inverted followed by strong inversion of carriers. In accumulation-mode transistor, with applied bias the channel region is depleted followed by accumulation of carriers at the surface. However, for JLT, compared to accumulation-mode transistor, accumulation of carriers at the

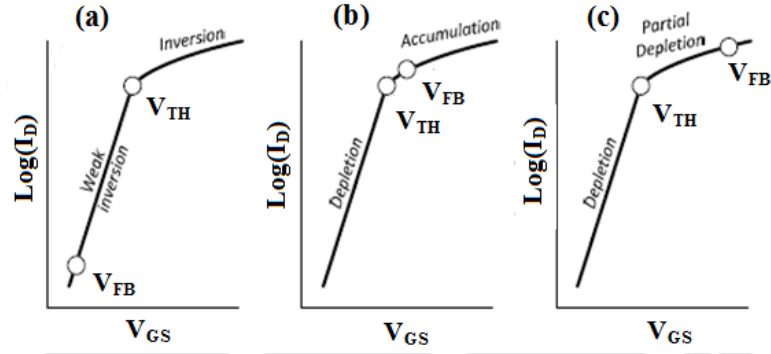


Figure 2.2: Current conduction mechanisms in (a) inversion-mode (b) accumulation-mode and (c) junctionless FETs [10].

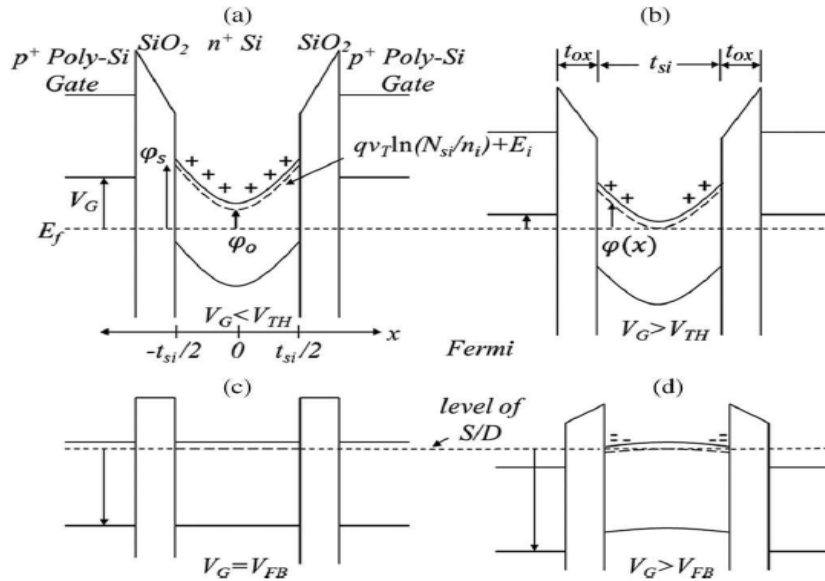


Figure 2.3: Band diagram of symmetric DGJLT showing a) fully depleted b) partially depleted c) flat band and d) accumulation regions [64].

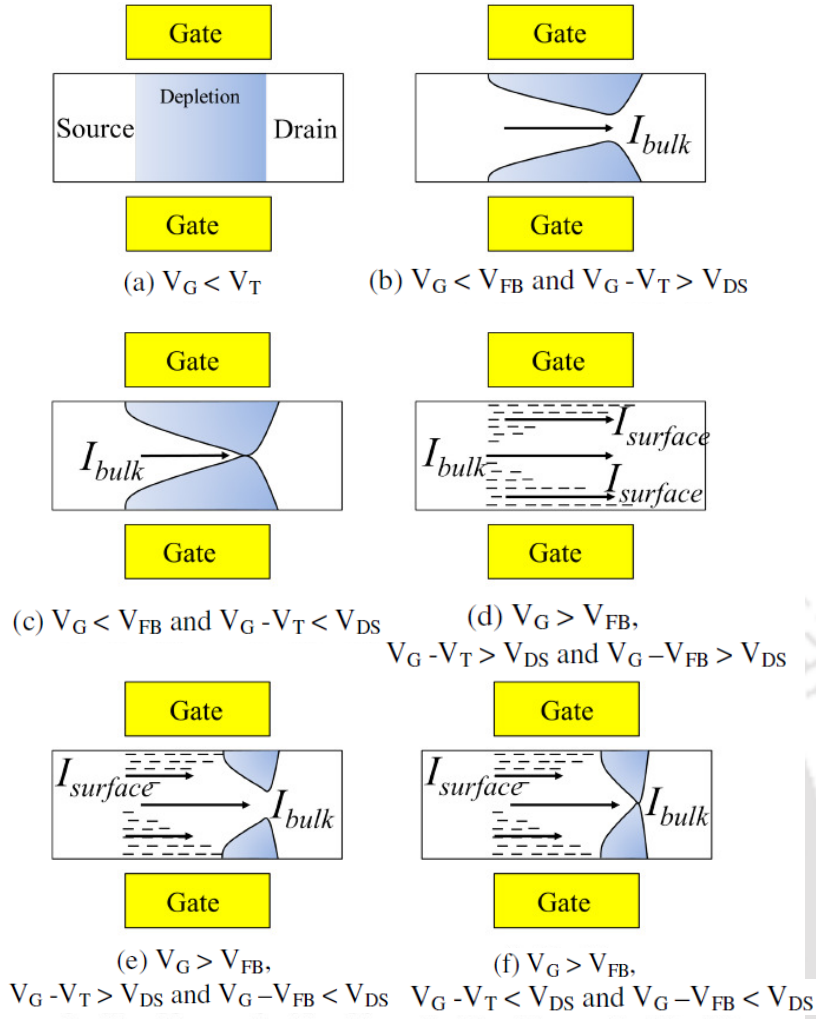


Figure 2.4: Current conditions depending on gate and drain biases for a symmetric double-gate junctionless transistor: (a) subthreshold fully-depleted, (b) linear partially-depleted, (c) saturation partially-depleted, (d) linear accumulated, (e) linear accumulated & partially-depleted, and (f) saturation accumulated & partially-depleted. This Fig. is adapted from [74].

surface happens at a much higher threshold voltage as shown Fig. 2.2.

In the subthreshold region ($V_{GS} < V_T$), the channel of a DGJLT is fully depleted. For a gate voltage, $V_{GS} > V_T$, the channel is partially depleted. When the gate voltage is equal to the flat band voltage, a completely neutral channel is created and current flows through the centre of the channel by the bulk conduction mechanism. On further increasing the gate voltage, majority carriers are accumulated in the bulk of the channel region, unlike conventional inversion DGMOS transistor, where inverted layer of carriers are formed at the semiconductor–insulator interface [46] Fig. 2.3 shows the band diagram for the DGJLT from fully depleted to accumulation region. The current conditions depending on different gate and drain voltages for a symmetric DGJLT for (a) subthreshold fully-depleted, (b) linear partially-depleted, (c) saturation partially-depleted, (d) linear accumulated, (e) linear accumulated & partially-depleted, and (f) saturation accumulated & partially-

depleted are also shown in Fig. 2.4 qualitatively.

In this work 2D numerical device simulations are performed for the devices shown in Fig. 2.1, using Atlas device simulator [72]. The simulations are carried out using two carriers Fermi-Dirac model without impact ionization to account for highly doped channel. Band-gap narrowing (BGN) and Schottky–Read–Hall (SRH) recombination models are included in simulations. As high-k gate dielectric materials are used, quantum models are not incorporated for gate leakage purpose. The mobility model includes both doping and transverse-field dependence. The technology parameters and the supply voltages used for the device simulations are according to the International Technology Roadmap for Semiconductors (ITRS) guidelines [2]. Uniform n-type channel doping having concentration $N_D = 1.5 \times 10^{19} \text{ cm}^{-3}$ for DGJLT and $N_D = 2 \times 10^{15} \text{ cm}^{-3}$ for DGMOS are used in this study. Typical value of doping concentration of $1 \times 10^{20} \text{ cm}^{-3}$ is used for source/drain extensions of DGMOS. Hafnium oxide (HfO_2 , $k = 22$) is used as a gate oxide material having equivalent oxide thickness (EOT) of 1 nm. For a fair comparison of both the devices, threshold voltage is fixed at 0.25 V corresponding to drain current value of 10^{-7} A at $V_{DS} = 50 \text{ mV}$ by adjusting the gate workfunction, which are 5.36 eV and 4.8 eV for DGJLT and DGMOS respectively. The drain and source extensions are taken as 20 nm for all simulations. The source and drain extensions (L_S and L_D) are typically assumed to be shorter compared to channel length in order to avoid parasitic resistance effects. But, we have taken such a value of L_S and L_D in order to predict the worse case situation.

2.2.2 Simulation Results and Discussion

Fig. 2.5 shows the electric field distribution of the devices along the channel direction close to the silicon-oxide interface. The electric field distribution is symmetrical in source and drain sides for both the devices at $V_{DS} = 50 \text{ mV}$. DGMOS has higher electric field compared to DGJLT in the channel region. When the drain voltage is increased to 1 V, the electric field on the drain side is increased for the devices thereby resulting in an asymmetrical distribution on both sides of the gate as obvious. Compared to DGJLT, the DGMOS has retained higher electric field in the channel region for $V_{DS} = 1 \text{ V}$.

Fig. 2.6 shows drain current (I_D) versus gate voltage at $V_{DS} = 50 \text{ mV}$ and 1 V. DGJLT has lesser leakage current and hence can be scaled to shorter channel lengths compared to DGMOS. Carrier mobility of junctionless transistors is not reduced much due to its lesser scattering. Also, JLT has lower vertical electric field compared to inversion mode transistors in the ON-state [40]. In addition, for a DGJLT, the bulk current drives almost the total current [26] in the saturation region, however in an inversion mode DGMOS, the current is dominated by the surface current component. Therefore, ON-state current of DGJLT is lesser compared to DGMOS although the values are comparable. ON-state to OFF-state current ratio (I_{ON}/I_{OFF}) and subthreshold slope (SS) of a nanowire kind of device also depends on dimension effects as well. It is reported that nanowires with low diameter and oxide

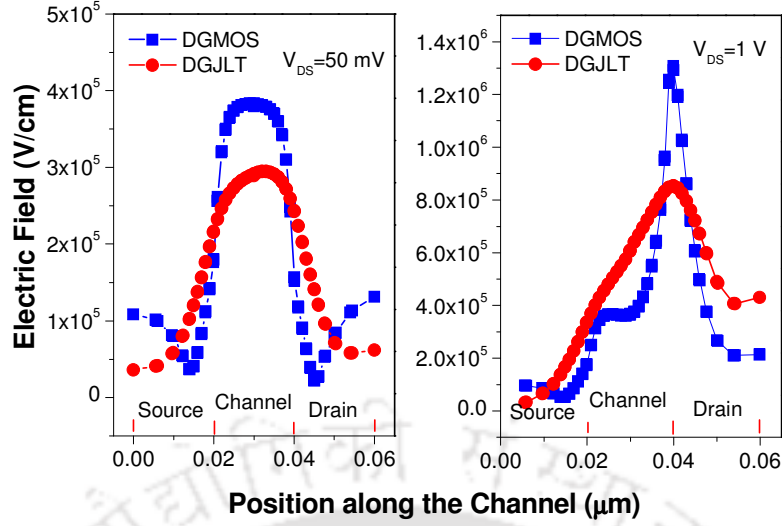


Figure 2.5: Electric field (E) along the channel length at $V_{DS}=50$ mV (left Fig.) and 1 V (right Fig.). $L = 20$ nm, $T_{si} = 10$ nm, $EOT = 1$ nm, $N_D=1.5 \times 10^{19} \text{ cm}^{-3}$ for DGJLT and $2 \times 10^{15} \text{ cm}^{-3}$ for DGMOS.

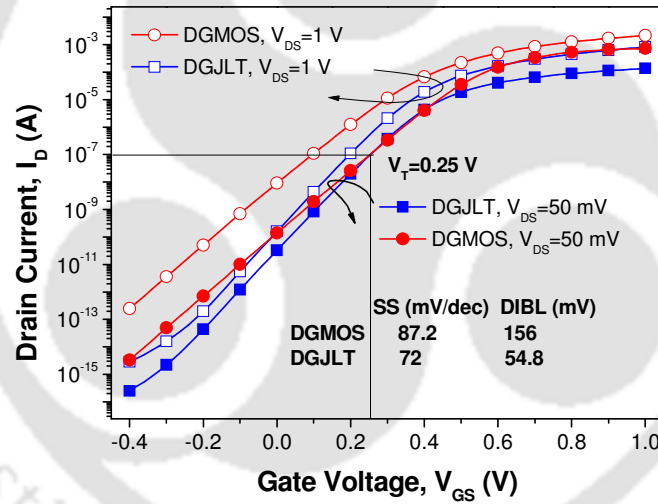
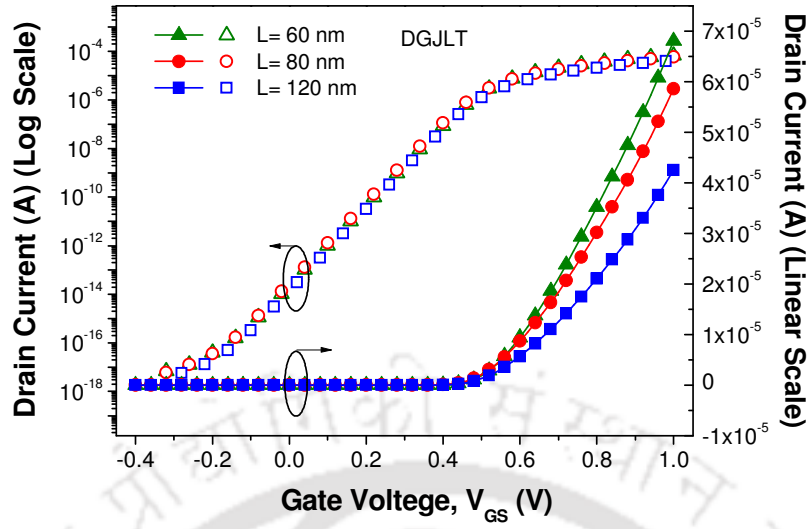


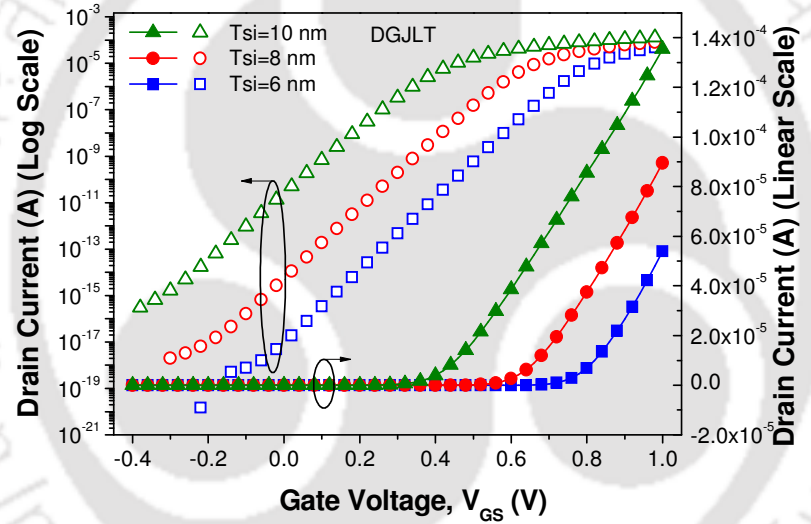
Figure 2.6: Drain current vs. gate voltage at $V_{DS} = 50$ mV (closed symbols) and 1 V (open symbols). $L = 20$ nm, $T_{si} = 10$ nm, $EOT = 1$ nm, $N_D=1.5 \times 10^{19} \text{ cm}^{-3}$ for DGJLT and $2 \times 10^{15} \text{ cm}^{-3}$ for DGMOS.

thickness tend to have the best transistor characteristics [75]. The value of SS for DGJLT and DGMOS are 72 mV/dec and 87.2 mV/dec respectively for channel length of 20 nm. SS is defined as the gate voltage shift for one decade change in drain current in subthreshold region. The drain induced barrier lowering (DIBL) value for DGJLT and DGMOS are 54.8 mV and 156 mV respectively for channel length of 20 nm. DIBL is defined as the difference in threshold voltage when the gate voltage is increased from 50 mV to 1 V ($DIBL = V_T(V_{DS} = 50 \text{ mV}) - V_T(V_{DS} = 1 \text{ V})$). The lower value of SS and DIBL makes the digital performance better for DGJLT than DGMOS transistor.

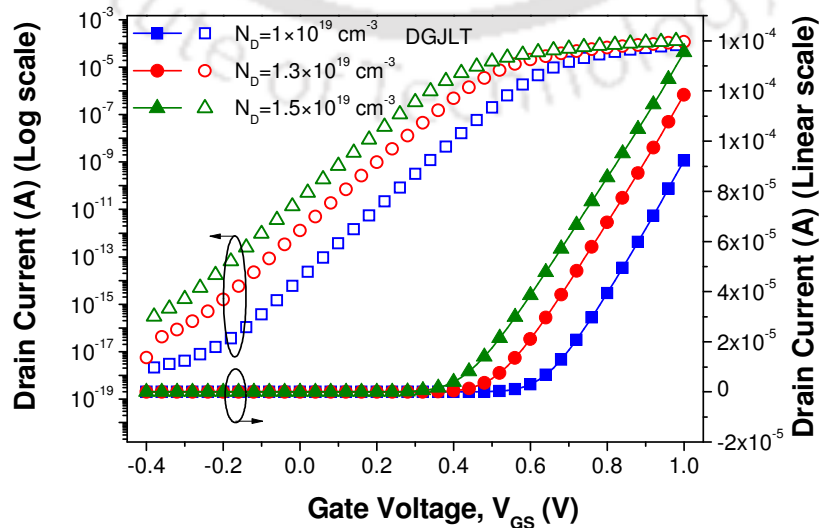
The drain current dependency on channel length, silicon thickness, channel doping concentration



(a)



(b)



(c)

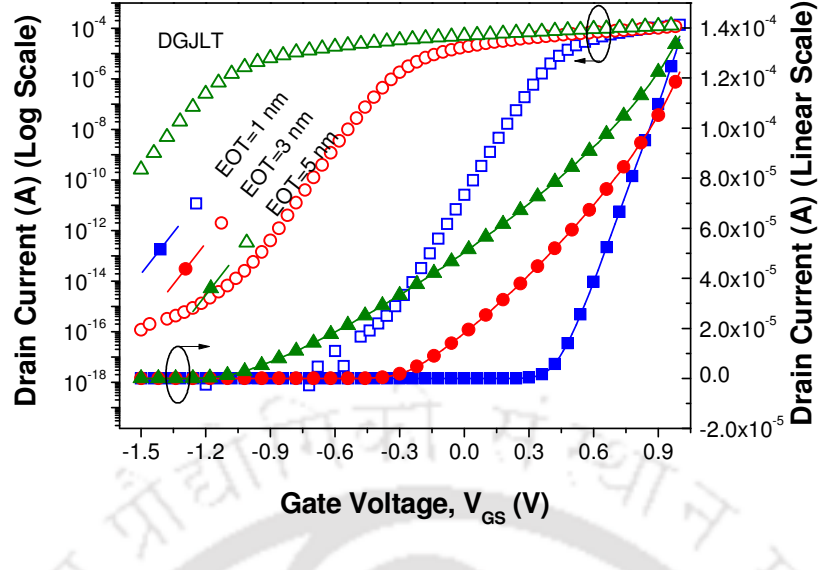


Figure 2.7: Drain current vs. gate voltage of the DGJLT at $V_{DS} = 50$ mV for (a) different channel lengths, $L = 60$ nm, 80 nm and 120 nm, while T_{si} , EOT and N_D are kept constant at 10 nm, 1 nm and $1.5 \times 10^{19} \text{ cm}^{-3}$ respectively, (b) different channel thicknesses, $T_{si} = 6$ nm, 8 nm and 10 nm, while EOT, L and N_D are kept constant at 1 nm, 20 nm and $1.5 \times 10^{19} \text{ cm}^{-3}$ respectively. Both linear (closed symbols, right y-axis) and log scales (open symbols, left y-axis) are plotted, (c) different channel doping concentrations, $N_D = 1 \times 10^{19} \text{ cm}^{-3}$, $1.3 \times 10^{19} \text{ cm}^{-3}$ and $1.5 \times 10^{19} \text{ cm}^{-3}$, while at T_{si} , L and EOT are kept constant at 10 nm, 20 nm and 1 nm respectively and (d) different oxide thicknesses at $EOT = 1$ nm, 3 nm and 5 nm, while T_{si} , L and N_D are kept constant at 10 nm, 20 nm and $1.5 \times 10^{19} \text{ cm}^{-3}$ respectively. Both linear (closed symbols, right y-axis) and log scales (open symbols, left y-axis) are plotted.

and oxide thickness is investigated for a DGJLT. Fig. 2.7 (a) shows the drain current versus gate voltage characteristics of DGJLT for different channel lengths, $L = 60$ nm, 80 nm and 120 nm respectively. As expected, drain current is higher for lower channel lengths when all other parameters are kept constant. Fig. 2.7 (b) shows the drain current versus gate voltage characteristics of DGJLT for different silicon thickness, $T_{si} = 6$ nm, 8 nm and 10 nm respectively. The number of bulk carriers and hence the drain current depends appreciably on the silicon thickness and its value is highest for $T_{si} = 10$ nm. Fig. 2.7 (c) shows the drain current versus gate voltage characteristics of DGJLT for different channel doping concentrations, $N_D = 1 \times 10^{19} \text{ cm}^{-3}$, $1.3 \times 10^{19} \text{ cm}^{-3}$ and $1.5 \times 10^{19} \text{ cm}^{-3}$ respectively. Drain current is highest for $N_D = 1.5 \times 10^{19} \text{ cm}^{-3}$. Fig. 2.7 (d) shows the drain current versus gate voltage characteristics of DGJLT for different oxide thickness, $EOT = 1$ nm, 3 nm and 5 nm. The drain current depends significantly on the oxide thickness and its value is highest for $EOT = 1$ nm. Similar study for DGMOS is already reported and therefore not discussed here. However, from the characteristics of both devices, it was observed that the threshold voltage of DGMOS is less

sensitive to silicon thickness and oxide thickness variations compared to DGJLT. Nevertheless, the threshold voltage of DGMOS is more sensitive to channel length variation compared to DGJLT.

The transconductance $G_m (= \partial I_D / \partial V_{GS})$ is a figure of merit which indicates how well a device converts a voltage to a current. Though the G_m values are closer for both the devices, at lower gate voltages ($V_{GS} < \sim 0.2$ V), DGMOS has higher value in the superthreshold region as shown in Fig. 2.8. The values of G_m for DGMOS and DGJLT are 4.5 mS and 1.9 mS respectively at $V_{GS} = 1$ V. An important figure of merit for analog performance of a device namely, transconductance/drain current ratio (G_m/I_D), also called transconductance generation factor is also plotted with respect to gate voltage, V_{GS} in Fig. 2.8 for a drain voltage, V_{DS} of 1 V. The G_m/I_D parameter represents the efficiency of a transistor to convert dc power into ac frequency and gain performance [76]. The values of G_m/I_D

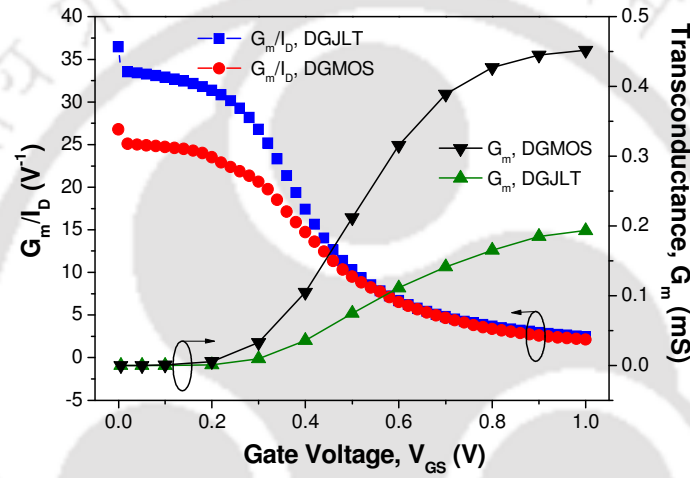


Figure 2.8: Transconductance/drain current ratio (G_m/I_D) and Transconductance (G_m) vs. gate voltage at $V_{DS} = 1$ V, $L = 20$ nm, $T_{si} = 10$ nm, $EOT = 1$ nm, $N_D = 1.5 \times 10^{19} \text{ cm}^{-3}$ for DGJLT and $2 \times 10^{15} \text{ cm}^{-3}$ for DGMOS.

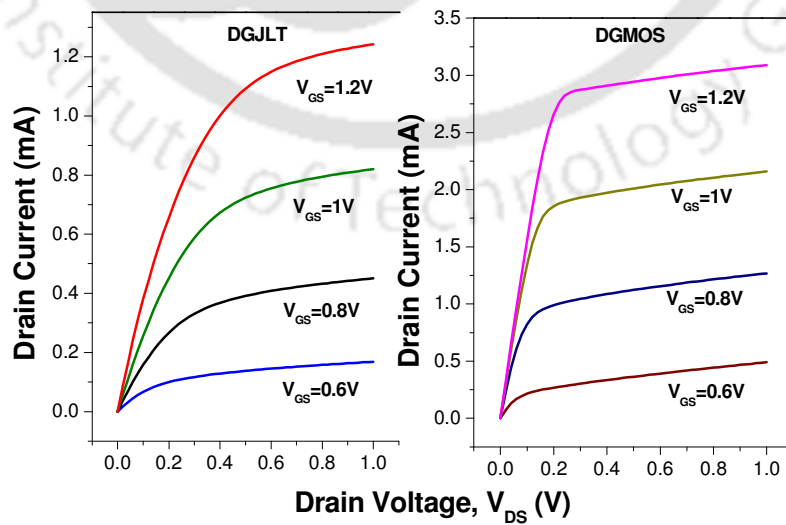


Figure 2.9: Drain current with respect to drain voltage for DGJLT and DGMOS at $V_{DS} = 1$ V at room temperature. $L = 20$ nm, $T_{si} = 10$ nm, $EOT = 1$ nm, $N_D = 1.5 \times 10^{19} \text{ cm}^{-3}$ (DGJLT), $2 \times 10^{15} \text{ cm}^{-3}$ (DGMOS).

for DGJLT and DGMOS are 31.3 V^{-1} and 23.3 V^{-1} respectively at $V_{GS} = 0.2 \text{ V}$. A smaller value of SS for DGJLT implies higher G_m/I_D than DGMOS in the subthreshold region. G_m/I_D is mainly controlled by body factor of the devices in weak inversion regime; however its value decreases in moderate/strong inversion regime due to the mobility degradation because of scattering etc. [33]. I_D - V_{DS} characteristic for different values of V_{GS} are plotted for both DGJLT and compared with DGMOS transistor as shown in Fig. 2.9. As obvious, junctionless transistor has inferior drain current with respect to drain voltage compared to DGMOS because of its lower mobility than the later device. Fig. 2.10 (a) presents the drain current and drain output conductance $G_D (= \partial I_D / \partial V_{DS})$ variation with drain voltage, V_{DS} for a fixed value of $V_{GS} = 1 \text{ V}$. The DGMOS carries higher current and hence output conductance than DGJLT due to its higher electric field at $V_{DS} = 1 \text{ V}$ [refer Fig. 2.2]. The value of G_D for DGMOS and DGJLT are $14.7 (\text{k}\Omega)^{-1}$ and $2.7 (\text{k}\Omega)^{-1}$ respectively at $V_{GS} = 0.02 \text{ V}$. Fig. 2.10 (b)

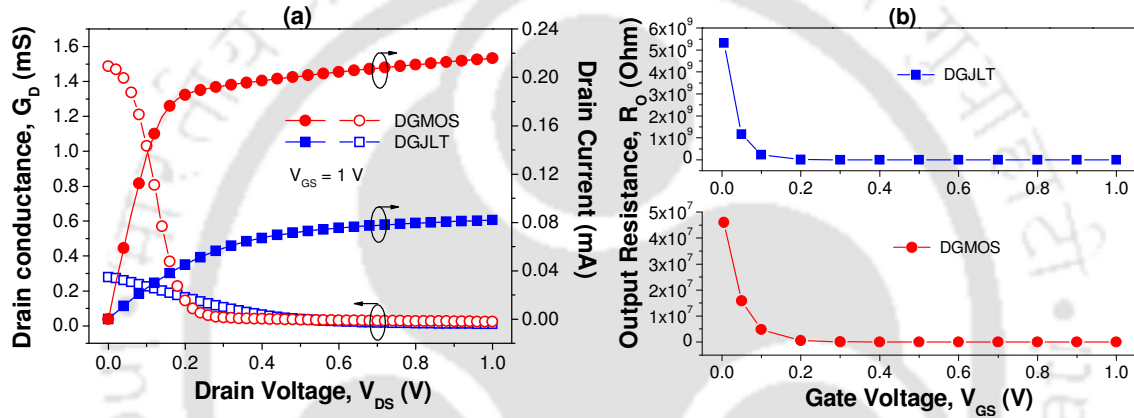


Figure 2.10: (a) Drain output conductance and drain current vs. drain voltage at $V_{GS} = 1 \text{ V}$ (Left side) (b) Output resistance (R_O) vs. gate voltage at $V_{DS} = 1 \text{ V}$. $L = 20 \text{ nm}$, $T_{si} = 10 \text{ nm}$, $EOT = 1 \text{ nm}$ (right side), $N_D = 1.5 \times 10^{19} \text{ cm}^{-3}$ for DGJLT and $2 \times 10^{15} \text{ cm}^{-3}$ for DGMOS.

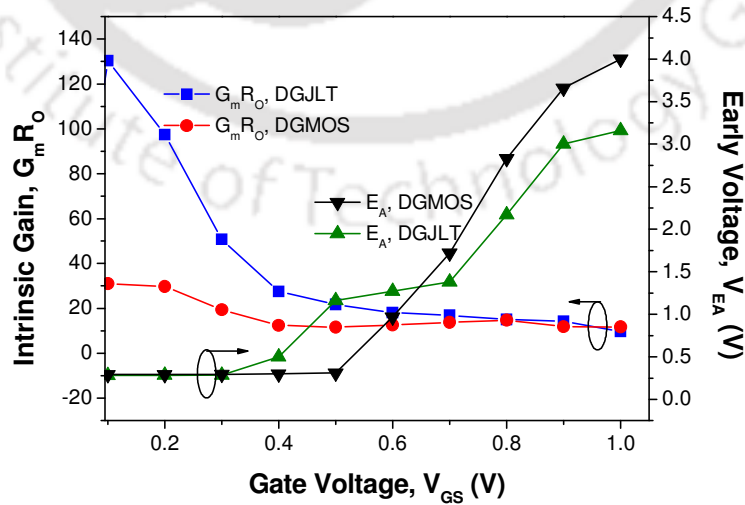


Figure 2.11: Intrinsic gain ($G_m R_O$) and Early voltage (V_{EA}) with gate voltage at $V_{DS} = 1 \text{ V}$. $L = 20 \text{ nm}$, $T_{si} = 10 \text{ nm}$, $EOT = 1 \text{ nm}$, $N_D = 1.5 \times 10^{19} \text{ cm}^{-3}$ for DGJLT and $2 \times 10^{15} \text{ cm}^{-3}$ for DGMOS.

presents the output resistance (R_O) with respect to V_{GS} . DGJLT offers much higher value of R_O due to smaller slope in I_D - V_{DS} characteristics as compared to DGMOS. The values of R_O for DGJLT and DGMOS are $5.3 \times 10^9 \Omega$ and $4.6 \times 10^7 \Omega$ respectively at $V_{GS}=0.005$ V. Early voltage, V_{EA} with respect to V_{GS} is also shown in Fig. 2.11. V_{EA} is higher at larger gate voltages as expected from the slope of I_D - V_{DS} characteristics [refer Fig. 2.9]. Early voltage can be derived from output resistance and vice versa as

$$V_{EA} = R_O I_{D(sat)} \quad (2.1)$$

Where, $I_{D(sat)}$ is the saturation current. The intrinsic gain $A_v (= G_m R_O)$ with respect to V_{GS} is also plotted in Fig. 2.11. The intrinsic gain of a device can be written as

$$G_m R_O = \frac{V_{EA} G_m}{I_{D(sat)}} \quad (2.2)$$

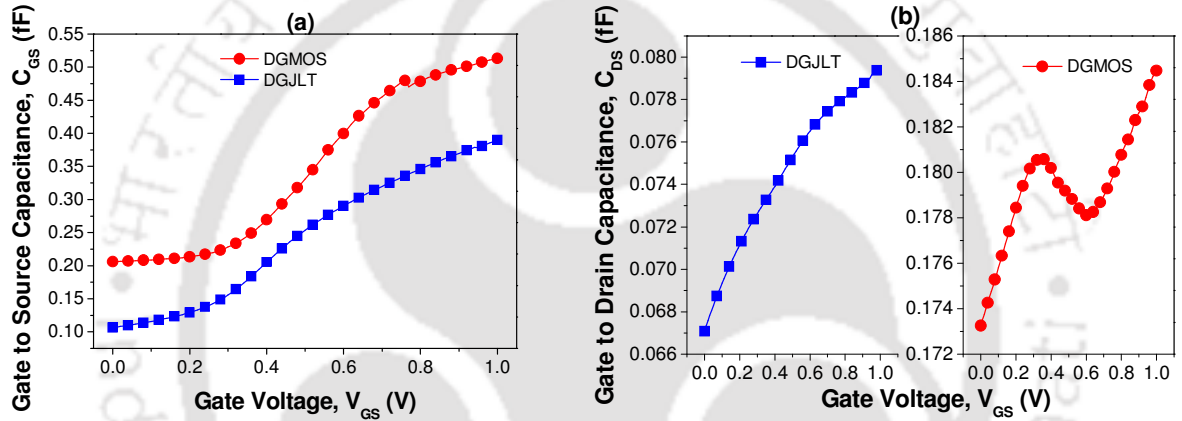


Figure 2.12: (a) Gate to source capacitance (C_{GS}) and (b) Gate to drain capacitance (C_{GD}) vs. gate voltage at $V_{DS}=1$ V. $L = 20$ nm, $T_{si} = 10$ nm, $EOT = 1$ nm, $N_D=1.5 \times 10^{19} \text{ cm}^{-3}$ for DGJLT and $2 \times 10^{15} \text{ cm}^{-3}$ for DGMOS.

The gain values for DGJLT and DGMOS at $V_{GS} = 0.2$ V are 97.4 and 29.7 respectively.

The parasitic capacitance of a device mainly consists of two parts namely oxide generated and junction generated components. As there are no pn junctions in a junctionless transistor in source-channel-drain path, junction related capacitances are not considered in this study. The intrinsic capacitances depend on the operating region of the device. Fig. 2.12 (a) and Fig. 2.12 (b) shows the gate-to-source (C_{GS}) and gate-to-drain (C_{GD}) capacitances as a function of V_{GS} for $V_{DS} = 1$ V. All the capacitances are extracted from the small-signal ac device simulations at a frequency of 1 MHz. DGMOS has the higher value C_{GS} and C_{GD} both in the subthreshold and superthreshold region as compared to DGJLT. The gate-to-bulk (C_{GB}) capacitance value for the devices is much lesser than C_{GS} and C_{GD} . DGJLT has higher C_{GB} value as compared to DGMOS (not shown). Higher value of C_{GS} and C_{GD} is due to higher electron concentration in the source and drain side respectively. The unity-gain cut-off frequency (f_T) is another useful figure-of-merit for analog applications. It is given by

$$f_T = \frac{G_m}{2\pi(C_{GS} + C_{GD} + C_{GB})} \quad (2.3)$$

Fig. 2.13 (a) shows the variation of f_T with V_{GS} for $V_{DS} = 1V$. At lower V_{GS} , f_T is almost same for all the devices due to almost same values of transconductance. The DGJLT has higher value f_T than DGMOS for $V_{GS} > \sim 0.45V$. f_T depends on C_{GS} , C_{GD} and G_m . As the G_m value is higher for DGMOS compared to DGJLT especially at higher V_{GS} , f_T is higher for DGMOS compared to DGJLT. With such f_T values, both the devices can meet ITRS guidelines for the specified voltages and dimensions. Unity gain cut-off frequency with respect to drain current is also shown in Fig. 2.13 (b) for the devices. Our simulations for DGJLT are calibrated with [46] for channel length $L = 1\mu m$, EOT = 7 nm, channel doping concentration $N_D = 1 \times 10^{19} cm^{-3}$, source/drain extension = 10 nm and device layer thickness of 10 nm at $V_{DS} = 50 mV$. As shown in Fig. 2.13 (c), both the results are closely matched.

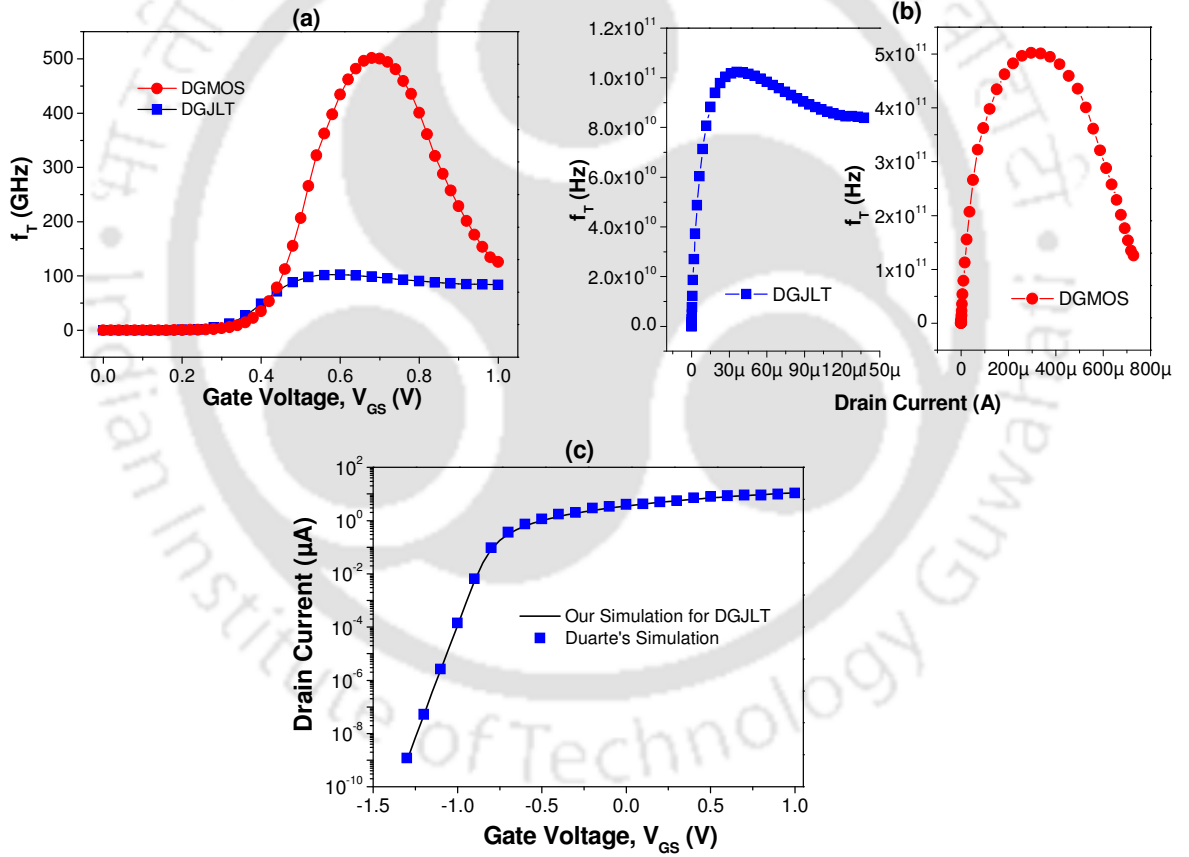


Figure 2.13: (a) Unity gain cut-off frequency (f_T) vs. gate voltage at $V_{DS} = 1V$. $L = 20 nm$, $T_{si} = 10 nm$, EOT = 1 nm, $N_D = 1.5 \times 10^{19} cm^{-3}$ for DGJLT and $2 \times 10^{15} cm^{-3}$ for DGMOS (b) Unity gain cut-off frequency with respect to drain current for DGJLT and DGMOS at $V_{DS} = 1V$ at room temperature. $L = 20 nm$, $T_{si} = 10 nm$, EOT = 1 nm, $N_D = 1.5 \times 10^{19} cm^{-3}$ (DGJLT), $2 \times 10^{15} cm^{-3}$ (DGMOS) (c) Calibration of our simulated I_D - V_{GS} characteristic for DGJLT with [37] at $V_{DS} = 50 mV$ for $L = 1\mu m$, $T_{si} = 10 nm$, EOT = 7 nm, $N_D = 1 \times 10^{19} cm^{-3}$, $L_S/L_D = 10 nm$.

2.2.3 Small-signal Equivalent Circuit Models of DGJLT

Large-signal models for DGJLT are presented in chapter 7. Non-quasi-static (NQS) small-signal equivalent circuit of DGJLT operating in strong inversion region is presented in Fig. 2.14. The equivalent circuit of a DGJLT in OFF-state is as represented in Fig. 2.15.

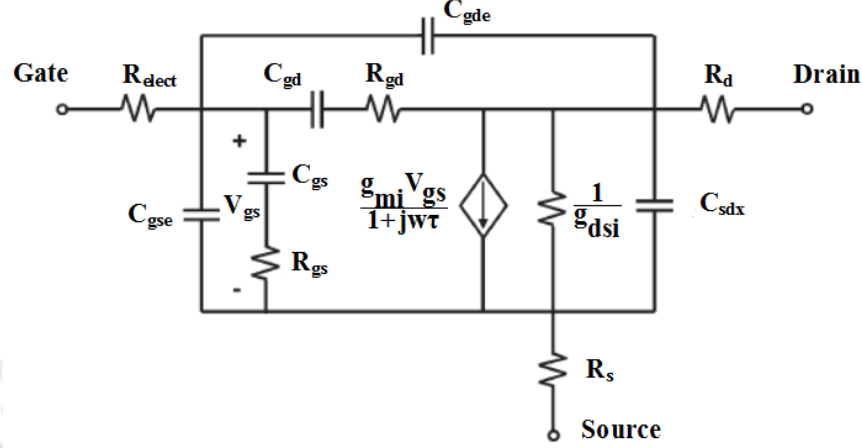


Figure 2.14: Non-quasi-static (NQS) small-signal equivalent circuit of DGJLT operating in strong inversion region.

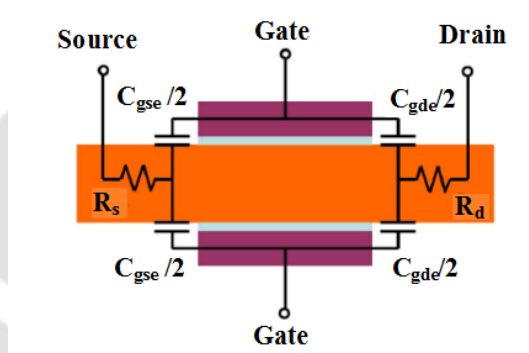


Figure 2.15: Equivalent circuit of a DGJLT in OFF-state (The intrinsic components are negligible).

R_s and R_d are the source and drain resistances, respectively. C_{gde} and C_{gse} are extrinsic gate-to-drain and gate-to-source capacitances respectively. g_{dsi} and g_{mi} are intrinsic source–drain conductance and transconductance. R_{gs} and R_{gd} are distributed channel resistances. C_{gd} and C_{gs} are intrinsic gate-to-drain and gate-to-source capacitances, respectively. By combining the RC-multiplications of $R_{gs}C_{gs}$, $R_{gd}C_{gd}$, and time constant τ , the charging and transport delay effects in the NQS model can be formulated. C_{sdx} is the source-to-drain capacitance. C_{sdx} reflects charge variation due to the DIBL effect in the short-channel MOSFETs. R_{elect} is the gate electrode resistance. The effect of R_{elect} is small enough to be neglected in the simulation works. The equivalent circuit shown in Fig. 2.14 can be analyzed in terms of Y -parameters as follows [35]:

$$Y_{11}^{int} \cong w^2 \left(R_{gs} C_{gs}^2 + R_{gd} C_{gd}^2 \right) + jw \left(C_{gs} + C_{gd} \right)$$

$$\begin{aligned}
Y_{12}^{\text{int}} &\cong -w^2 R_{gd} C_{gd}^2 - jw C_{gd} \\
Y_{21}^{\text{int}} &\cong g_{mi} - w^2 R_{gd} C_{gd}^2 - jw C_{gd} + \tau g_{mi} \\
Y_{22}^{\text{int}} &\cong g_{dsi} + w^2 R_{gd} C_{gd}^2 + jw (C_{sdx} + C_{gd})
\end{aligned} \tag{2.4}$$

Where Y^{int} means the internal Y -parameters of the device. The parameters C_{gd} , C_{gs} , R_{gd} , R_{gs} , τ , g_{mi} , C_{sdx} are provided as follows:

$$\begin{aligned}
C_{gd} &= -\frac{\text{Im}(Y_{12}^{\text{int}})}{w}, \quad C_{gs} = \frac{\text{Im}(Y_{11}^{\text{int}}) + \text{Im}(Y_{12}^{\text{int}})}{w} \\
R_{gd} &= -\frac{\text{Re}(Y_{12}^{\text{int}})}{w^2 C_{gd}^2}, \quad R_{gs} = \frac{1}{C_{gs}^2} \left(\frac{\text{Re}(Y_{11}^{\text{int}})}{w^2} - R_{gd} C_{gd}^2 \right), \quad \tau = -\frac{\text{Im}(Y_{21}^{\text{int}})/w + C_{gd}}{g_{mi}} \\
g_{mi} &= \text{Re}(Y_{21}^{\text{int}}) \Big|_{w^2=0}, \quad g_{dsi} = \text{Re}(Y_{22}^{\text{int}}) \Big|_{w^2=0}, \quad C_{sdx} = \frac{\text{Im}(Y_{22}^{\text{int}})}{w} - C_{gd}
\end{aligned} \tag{2.5}$$

Table 2.1:

Values of the parameters extracted in the saturation region ($V_{GS}=V_{DS}=1V$) for a DGJLT for $L=20$ nm, $T_{si}=10$ nm, $T_{ox}=2$ nm using TCAD.

	Bias Condition
Parameter	$V_{GS}=V_{DS}=1V$
C_{gs}	0.389 fF
C_{gd}	0.079 fF
R_{gs}	0.471 k Ω
R_{gd}	9.2 k Ω
τ	0.145 psec
g_{mi}	1.93 mS
g_{dsi}	0.1 mS
R_s, R_d	0.4 k Ω
C_{sdx}	0.156 fF

2.3 Analog Performance of Bulk Planar Junctionless Transistor (BPJLT)

In general, junctionless transistors require a silicon-on insulator (SOI) wafer and a uniform ultrathin channel to turn the device off, making them technologically difficult and expensive to produce. Recently, junctionless FinFET structures has been realised on bulk substrate forming bulk FinFET [60]. The advantages of the proposed transistor as they claim are as follows. First, the absence of an SOI wafer lowers the cost and improves scalability. Second, it has full compatibility with the industry standard bulk FinFET CMOS process flow. Third, an additional design parameter, i.e., substrate doping concentration, helps tune the device performance. The comparison of the simulated DIBL and

SS reveals that the JL bulk devices outperform the SOI devices for channel thickness $W = 10$ nm.

The electrons are more concentrated on the top of the channel in JL bulk FinFET [Fig. 2.16]. The reason is as follows. When zero voltage is applied to the gate of bulk FinFET, there is depletion from both top (because of workfunction difference between channel and gate) and bottom (because of workfunction difference between n-type channel and p-type substrate). The section of the physical device layer that is depleted by the gate at zero bias is the “effective device layer.” Thus, in the OFF-state, the device layers are depleted in both SOI and bulk FinFET. In the ON-state, the SOI-JLT device layer is uniform in flatband; whereas for the bulk FinFET, a fraction of the device layer at the top—corresponding to the effective device layer—is in flatband, and the rest of it still remains depleted. Thus, a continuous conduction channel is formed in the ON-state in both devices, of which thickness is equal to the physical (effective) device layer thickness for the SOI-JLT (bulk FinFET). The thinner effective device layer in the case of the bulk FinFET suggests that it would exhibit better electrostatic integrity than the SOI-JLT. Also, it exhibits better I_{ON}/I_{OFF} than SOI-JLT. The reduction in the effective channel thickness by the channel/substrate junction helps to reduce the SCE and the OFF-state current, and the sensitivity to the physical thickness of the channel. With respect to device design, the JL bulk FinFET offers an additional design parameter, i.e., the substrate doping concentration, for controlling device performance [60].

Traditionally, SOI technology is believed to be superior in many respects than bulk technology. To believe completely that bulk FinFET outperforms SOI counterpart, the device variability, reliability, oxide separations issues between devices must be looked into thoroughly.

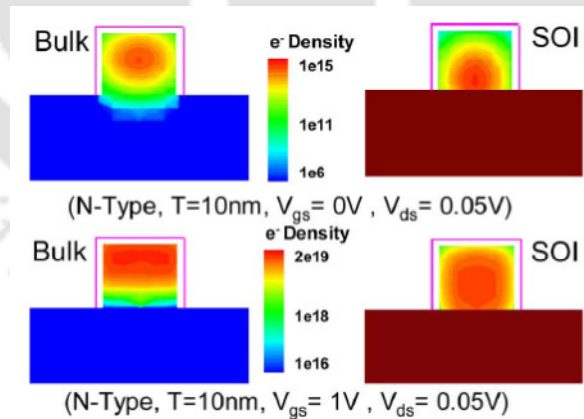


Figure 2.16: Electron density distributions in the middle of the channel at OFF-state ($V_{gs} = 0$ V) and ON-state ($V_{gs} = 1$ V) for $L_g = 15$ nm, $T = 10$ nm and $EOT = 1$ nm. (Courtesy, [60])

Recently, bulk planer junctionless transistor (BPJLT) structure has been reported by Gundapaneni et al. at IIT Bombay, India. The device structure and operation is described below. They studied the digital performance parameters of the structure. Here, we are interested for the possible analog applicability of the device.

2.3.1 Device Structure and Operation

Fig. 2.17 (a) shows the BPJLT device architecture for n-channel operation. A thin n-type device layer is formed on p-type silicon. A junction with a junction depth of X_j is formed. In n-type SOI-JLT, there is a buried-oxide layer (BOX) between device layer and bulk silicon as shown in Fig. 2.17 (b). In BPJLT, application of zero voltage at the gate makes the device layer depleted. On increasing the gate voltage, current starts flowing from source to drain. Similarly, when zero bias is applied to the gate of the SOI-JLT, the n-doped silicon will be depleted of carriers. As a positive bias is applied to the gate, a neutral region is created in thin SOI device layer and results in a conducting channel between the source and the drain [49].

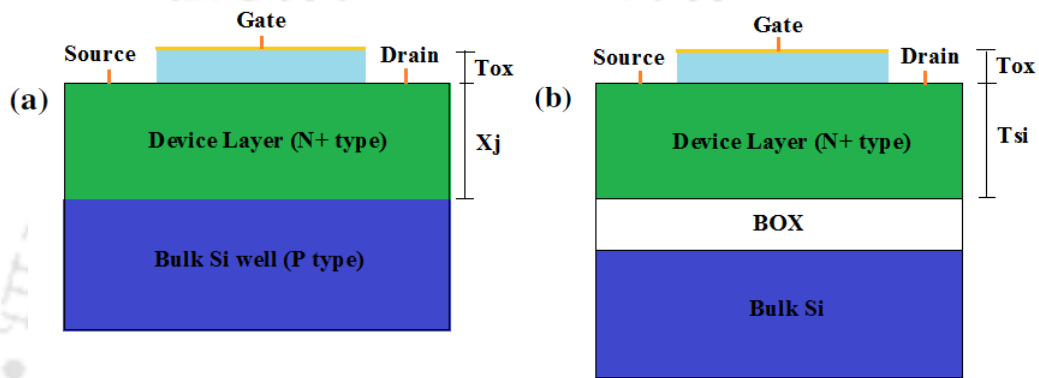


Figure 2.17: Crosssectional view of (a) bulk planar junctionless transistor (BPJLT) (b) SOI Junctionless transistor (SOI-JLT) [39].

Both the devices have uniform n-type body doping, i.e., the source, drain, and the channel have identical doping having concentration, N_D of $1.5 \times 10^{19} \text{ cm}^{-3}$. The gates of both the devices are a metal with p-type work function, separated from the channel by a thin SiO_2 gate dielectric of thickness 1 nm (EOT). Well is doped with p-type material having doping concentration (N_W) of $5 \times 10^{18} \text{ cm}^{-3}$. For both the devices, threshold voltage V_T is fixed at 0.25 V corresponding to drain current of 10^{-7} A at $V_{DS} = 50 \text{ mV}$ by adjusting the gate workfunction, which are 5 eV and 5.7 eV for BPJLT and SOI JLT respectively. Though gate workfunction value of 5.7 eV looks higher, this is for theoretical study only and can be adjusted by choosing channel doping concentration and threshold voltage. The simulations are carried out using two carriers Fermi-Dirac model, to account for highly doped channel, without impact ionization. Band-gap narrowing and Schottky-Read-Hall recombination models are included in simulations. Bohm quantum potential (BQP) model is also considered to simulate the effects of quantum mechanical confinement. The mobility model includes both doping and transverse-field dependence. Our simulation results are calibrated with [49].

2.3.2 Simulation Results and Discussion

The variations of the drain current and transconductance ($G_m = \partial I_D / \partial V_{GS}$), with gate to source voltage

(V_{GS}) are shown in Fig. 2.18 for BPJLT and SOI JLT at a drain voltage (V_{DS}) of 1V. BPJLT has better I_{ON}/I_{OFF} ratio as compared to SOI JLT, which makes BPJLT scalable to shortest channel lengths with affordable SCE performances. Also, BPJLT has lower subthreshold slope (SS), and drain induced barrier lowering (DIBL) as compared to SOI JLT. BPJLT shows superior transconductance value than SOI JLT for $V_{GS} > 0.4$ V. The values of transconductance at drain voltage of 1 V are 0.022 S and 0.011 S for BPJLT and SOI JLT respectively.

Fig. 2.19 presents the drain current and drain output conductance, $G_D (= \partial I_D / \partial V_{DS})$ change with respect to drain to source voltage, V_{DS} at a gate voltage of 1 V. BPJLT offers more current than SOI JLT both in subthreshold as well as super threshold region. The value of G_D for BPJLT and SOI JLT are 0.024 ohm^{-1} and 0.012 ohm^{-1} respectively at $V_{GS} = 0.02$ V. The variations of G_m/I_D with V_{GS} for

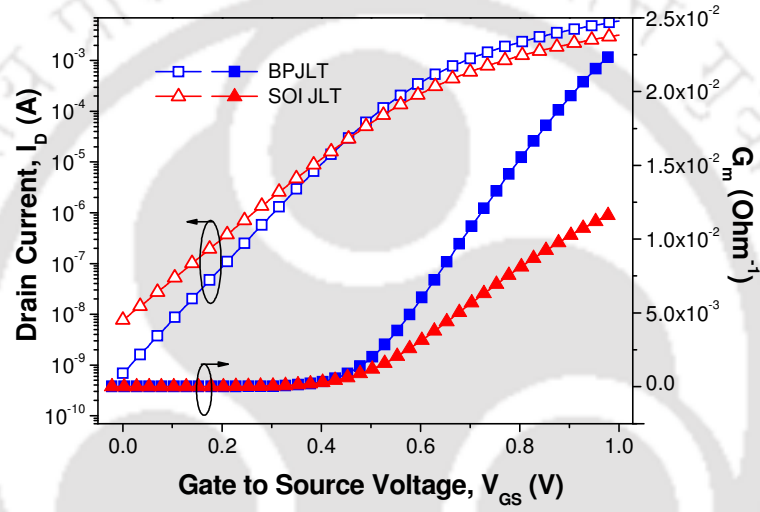


Figure 2.18: Variation of Drain current and transconductance with V_{GS} at $V_{DS} = 1$ V. $L = 20$ nm, $T_{si} = 10$ nm, $EOT = 1$ nm, $N_D = 1.5 \times 10^{19} \text{ cm}^{-3}$.

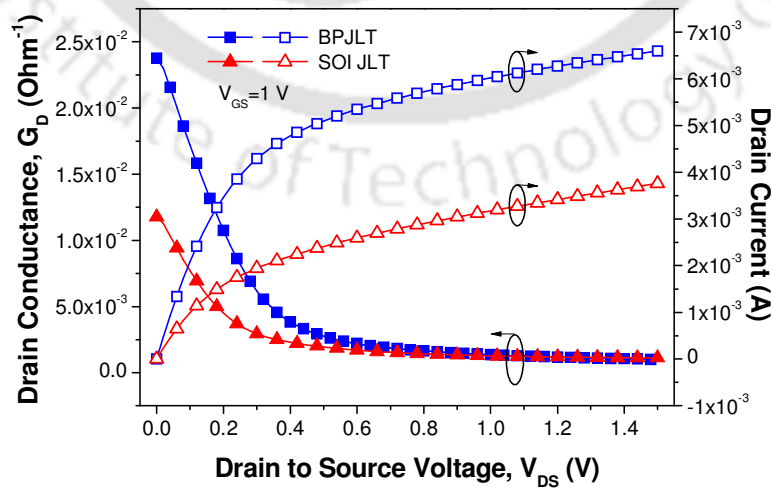


Figure 2.19: Variation of drain output conductance and drain current with V_{DS} at $V_{GS} = 1$ V. $L = 20$ nm, $T_{si} = 10$ nm, $EOT = 1$ nm, $N_D = 1.5 \times 10^{19} \text{ cm}^{-3}$.

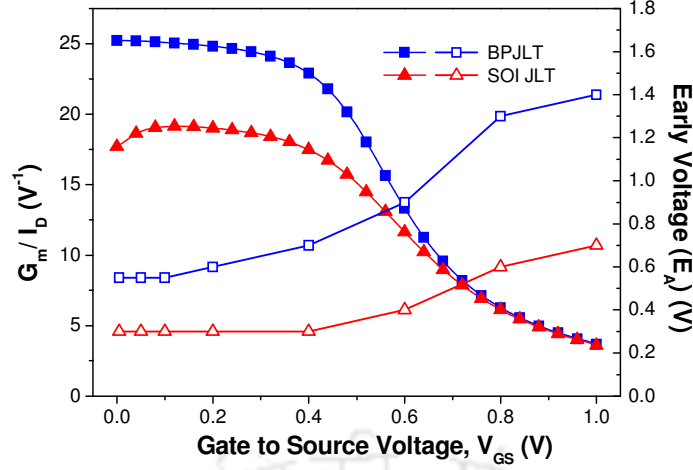


Figure 2.20 Variation of transconductance/drain current ratio (G_m/I_D) with V_{GS} at $V_{DS} = 1$ V. $L = 20$ nm, $T_{si} = 10$ nm, $EOT = 1$ nm, $N_D = 1.5 \times 10^{19} \text{ cm}^{-3}$.

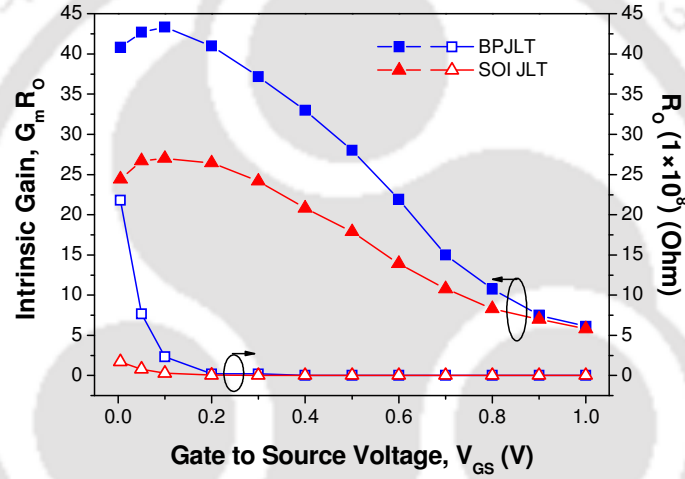


Figure 2.21: Variation of intrinsic gain ($G_m R_O$) and output resistance (R_O) with V_{GS} at $V_{DS} = 1$ V. $L = 20$ nm, $T_{si} = 10$ nm, $EOT = 1$ nm, $N_D = 1.5 \times 10^{19} \text{ cm}^{-3}$.

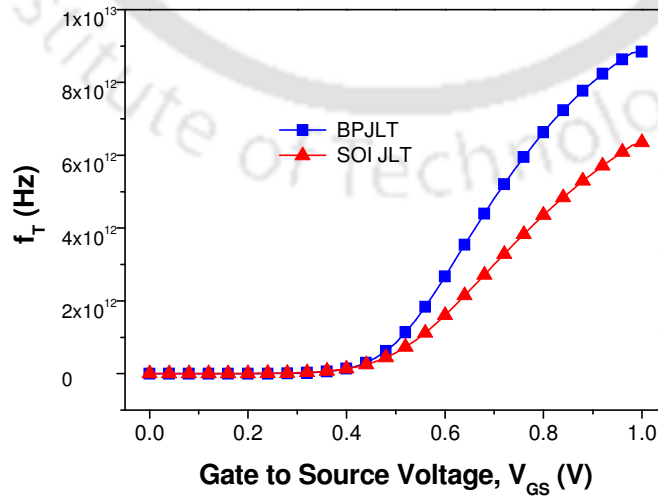


Figure 2.22: Variation of unity gain frequency (f_T) with V_{GS} at $V_{DS} = 1$ V. $L = 20$ nm, $T_{si} = 10$ nm, $EOT = 1$ nm, $N_D = 1.5 \times 10^{19} \text{ cm}^{-3}$.

the devices are shown in Fig. 2.20 at $V_{DS} = 1$ V. The values of G_m/I_D for BPJLT and SOI-JLT at $V_{GS} = 0.02$ V are 26 V^{-1} and 17.5 V^{-1} respectively at $V_{DS} = 1$ V. In the weak inversion regime, G_m/I_D is almost constant. In strong inversion, G_m/I_D decreases due to reduced mobility as electric field increases. The variation of early voltage (V_A) with gate voltage is also shown in Fig. 2.20. V_A is more both in weak and strong inversion region for BPJLT. The improvement in the V_A , and hence in the output resistance (R_O) is due to the reduction of short channel effects in the BPJLT devices. Therefore, the intrinsic gain ($G_m R_O$) of the BPJLT devices is improved significantly, as can be seen from Fig. 2.21. $G_m R_O$ is higher for BPJLT in all regions of operation of the device. The highest value of intrinsic gain occurs at $V_{GS} = 0.1$, which are 44 and 27.5 for BPJLT and SOI JLT respectively. All the capacitances are extracted from the small-signal ac device simulations at a frequency of 1 MHz. In weak inversion regime, SOI JLT has higher value C_{GS} than BPJLT; however, in strong inversion regime the trend is opposite. SOI JLT has higher value C_{GD} than BPJLT. BPJLT has higher value of f_T ($f_T = G_m / 2\pi (C_{GS} + C_{GD} + C_{GB})$) than SOI JLT (Fig. 2.22) making it more suitable for RF circuits.

2.4 Double-Gate JLT for Low Power Digital Applications

2.4.1 Simulation Results and Discussion

A channel doping concentration of $1 \times 10^{19} \text{ cm}^{-3}$ and $1 \times 10^{16} \text{ cm}^{-3}$ are considered for DGJLT and DGMOS respectively for all simulations. For DGJLT, this makes the work function difference of approximately E_G , i.e., 1.1 eV according to the relation $E_G/2 + qV_{TH} \times \ln(N_D/n_i)$, where E_G is the band gap of silicon, V_{TH} is the thermal voltage (kT/q), N_D is the doping concentration of the channel, and n_i is the intrinsic carrier density. The source/drain doping concentration for DGMOS is taken as $1 \times 10^{20} \text{ cm}^{-3}$. Threshold voltages of the devices are fixed at 0.25 V which corresponds to drain current of 10^{-7} A at $V_{DS} = 50$ mV by adjusting gate workfunctions (WF) which are 5.11 eV and 4.805 eV for DGJLT and DGMOS respectively. The channel thickness (T_{si}) is 10 nm. HfO_2 is used as gate oxide having oxide thickness (EOT) of 1 nm. Drain to source voltage is 0.5 V, unless otherwise specified. The drain and source extensions are taken as 20 nm for all simulations. The simulations were carried out using two carriers, the drift-diffusion model without impact ionization, doping concentration-dependent carrier mobility and electric field-dependent carrier model. Shockley-Read-Hall (SRH) recombination/ generation were included in the simulation to account for leakage currents. Quantum models are not included in this study.

The I_{ON}/I_{OFF} ratio, as shown in Fig. 2.23 (a), is better for DGJLT as compared to DGMOS; which makes junctionless DGMOS, i.e., DGJLT transistors scalable to shortest channel lengths with affordable SCE performances. Fig. 2.23 (b) shows the drain induced barrier lowering (DIBL) and threshold voltage (V_T) variation with physical gate length, $L = 20$ nm to 50 nm. The variation of threshold voltage change with physical length is lesser for DGJLT as compared to DGMOS. DIBL is

defined as the difference in threshold voltage when the gate voltage is increased from 50 mV to 1 V (i.e., $\text{DIBL} = V_T(V_{DS} = 50 \text{ mV}) - V_T(V_{DS} = 1 \text{ V})$). The drain induced barrier lowering for DGJLT and DGMOS transistor are 45 mV and 187 mV respectively for $L = 20 \text{ nm}$. Fig. 2.24 (a) shows the subthreshold slope for physical channel lengths of 20 nm to 50 nm. DGJLT and DGMOS exhibits a SS of 70.2 mV/dec and 89.7 mV/dec respectively for $L = 20 \text{ nm}$. The lesser value of SS for DGJLT will make the switching time lesser as compared to DGMOS transistor. Fig. 2.24 (b) shows the variation of threshold voltage with effective channel length which varies from 18 nm to 24 nm. Effective channel length is defined as the junction length between source and drain. It is seen that

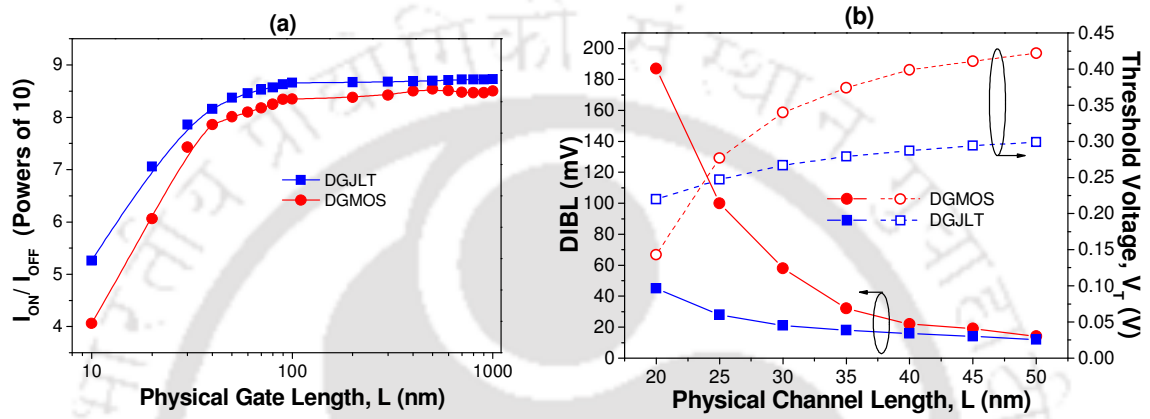


Figure 2.23: (a). Variation of I_{ON}/I_{OFF} ratio (b) DIBL and threshold voltage with physical channel length (L) at $V_{DS} = 0.5 \text{ V}$ at $T_{si} = 10 \text{ nm}$, $EOT = 1 \text{ nm}$, $N_D = 1 \times 10^{19} \text{ cm}^{-3}$ and $1 \times 10^{16} \text{ cm}^{-3}$ for DGJLT and DGMOS respectively.

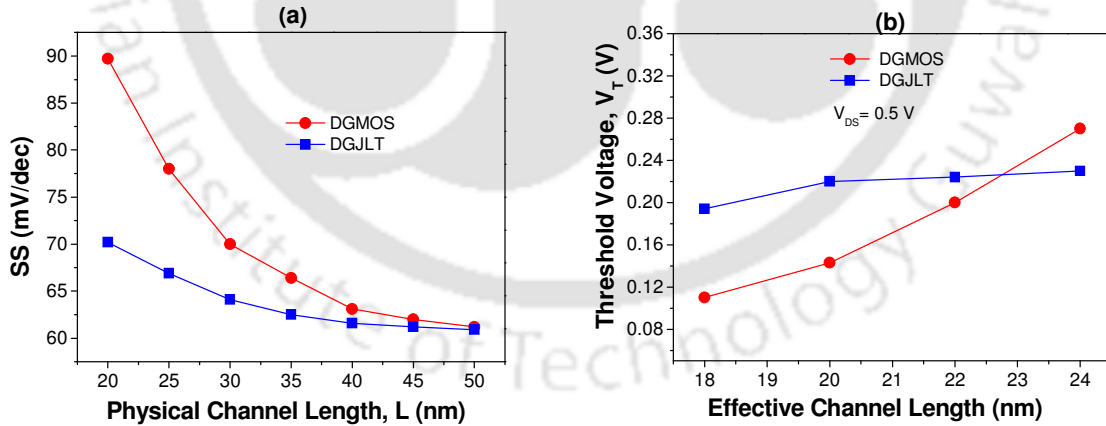


Figure 2.24: (a). Variation of SS and with physical channel length (L) (b) threshold voltage with effective channel length at $V_{DS} = 0.5 \text{ V}$ for $T_{si} = 10 \text{ nm}$, $EOT = 1 \text{ nm}$. $WF = 5.11 \text{ eV}$ for DGJLT and 4.805 eV for DGMOS.

threshold voltage change with effective channel length is lesser for DGJLT as compared to DGMOS due to the resistance of the gate overlap/underlap of the later [77]. However, V_T of JLT is more sensitive to silicon and gate oxide thickness variation compared to IM MOSFETs (not shown).

2.5 Summary

DGJLT offered 1.3 times higher transconductance to drain current ratio at $V_{GS} = 0.2$ V, 2.9 times higher output resistance at $V_{GS} = 0.9$ V and 3.3 times higher intrinsic gain at $V_{GS} = 0.2$ V when compared to a similar DGMOS device. However, in DGMOS, drain current with respect to drain voltage was 2.8 times higher at $V_{GS} = 0.9$ V and unity gain cut-off frequency was 2.7 times higher at $V_{GS} = 0.9$ V compared to DGJLT. Among the two devices, DGJLT is more suitable for low frequency, high gain applications while DGMOS is more suitable for high speed applications.

BPJLT is found to have better drain current (I_D), transconductance (G_m), transconductance/drain current (G_m/I_d), output conductance (G_D), output resistance (R_O), early voltage (E_A), intrinsic gain ($G_m R_O$), unity gain frequency (f_T) as compared to SOI JLT. Thus, BPJLT is superior to SOI JLT in regard of analog performance. DGJLT presents superior digital performance when compared with the conventional inversion mode DGMOS transistor at low drain voltage also.

For consideration of BPJLT to be superior to SOI JLT, the device variability, reliability, oxide separations between devices and other fabrication related issues must be looked into thoroughly. Traditionally, SOI technology is believed to be superior in many respects than bulk technology.

Chapter 3

Estimation of Process-Induced Variations and Effect of Temperature in DGJLT

3.1 Introduction

Though junctionless transistors are reported to offer many advantages as mentioned in chapter 1, it has some disadvantages also in regard of process variations as described below. Unlike, a conventional MOSFET where channel is either undoped (doping concentration, $N_D \sim 1.5 \times 10^{10} \text{ cm}^{-3}$) or lightly doped ($N_D \sim 10^{15} - 10^{16} \text{ cm}^{-3}$), the channel doping concentration of a JLT is much higher ($N_D \sim 8 \times 10^{18} - 8 \times 10^{19} \text{ cm}^{-3}$) as mentioned in previous chapter. This high doping concentration in JLT is required to ensure a comparable ON-state current as that of JB counterpart device while maintaining flat band condition at the ON-state to enhance the carrier mobility as a result of reduced surface roughness scattering (though its value is lesser). For JB device, reduction of channel width (W_{si}) means the channel region is more controlled by the gate. That is, SCE decreases with decrease in W_{si} and hence threshold voltage decreases with undoped or lightly doped channel. However, for JLT because of highly doped channel, threshold voltage is more sensitive to W_{si} . Although Colinge et al. predicted that random dopant fluctuation in junctionless transistors would become small due to its junction free nature [40], comprehensive analysis of threshold voltage fluctuation caused by random fluctuation and W_{si} variation is still necessary.

Choi et al. reported the sensitivity of threshold voltage to nanowire width variation for gate-all-around junctionless transistor (GAA JLT) [41]. They found that V_T variation with silicon thickness is more in GAA JLT than IM counterpart. A JLT suffers from more threshold voltage (V_T) variation with random dopant fluctuations than inversion mode (IM) counterpart [43-44]. A systematic investigation of the other process parameters on electrical performance of JLT is still lacking in literature. In this work, the impact of process induced variations on the electrical characteristics of an n-type junctionless symmetric double-gate transistor (DGJLT) is reported. The process parameters considered here are gate length (L), thickness of silicon film (T_{si}) and gate oxide thickness (T_{ox}). The impact of these process parameters on the electrical parameters viz., ON current, threshold voltage

(V_T) and subthreshold slope (SS) are systematically investigated with the help of extensive device simulations.

At high temperature (T), inversion mode (IM) devices usually would not succeed because of increased subthreshold swing, threshold voltage shift and increased leakage current. However, as the operational principle of JLT is different from IM devices, temperature dependence on the electrical characteristics are expected to be different in JLTs. A JLT has high electric field in the subthreshold region and zero electric field in the ON-state, converse to an IM device. Park et al. reported that JLTs show more marked conductance oscillations at high temperature compared to IM devices [78]. Doria et al. had reported that early voltage and gain are improved with temperature for JLTs unlike conventional MOSFETs. Junctionless transistors show larger threshold voltage variation with temperature than classical MOSFETs though JLT MugFET devices present excellent properties for high temperature applications [33]. Temperature dependence on the digital and analog performance parameters of a DGJLT is systematically investigated with the help of extensive simulations and compared with DGMOS of similar dimensions.

3.2 Process-Induced Variations in the Performance of a DGJLT

3.2.1 Device Structure and Simulation Setup

The device structure for an n-type symmetric DGJLT and DGMOS are shown in Fig. 2.1. Here, threshold voltages of the device having gate length $L = 20$ nm is fixed at 0.2 V at drain voltage $V_{DS} = 1$ V which corresponds to drain current of 10^{-7} A by adjusting gate workfunctions which are 5.3 eV for DGJLT and 4.8 eV for DGMOS respectively. The channel doping concentration of DGJLT is considered as $1.5 \times 10^{19} \text{ cm}^{-3}$. For DGMOS, channel and source/drain doping concentration are $2 \times 10^{15} \text{ cm}^{-3}$ and $1 \times 10^{20} \text{ cm}^{-3}$ respectively. The source and drain extensions (L_S and L_D) are taken as 20 nm. The simulations were carried out using two carriers, the Fermi-Dirac model without impact ionization, doping concentration-dependent carrier mobility and electric field-dependent carrier model. Band gap narrowing model was included. Shockley-Read-Hall (SRH) recombination/ generation were included in the simulation to account for leakage currents.

3.2.2 Simulation Results and Discussion

Fig. 3.1 (a) shows the ON-state current of the devices at channel lengths $L = 20$ nm to 100 nm at $T_{ox} = 1$ nm and $T_{si} = 10$ nm. In all simulations, ON-state current is extracted at a drain voltage of 1 V. The ON-state current for the devices with respect to L follow similar trend. Fig. 3.1 (b) presents the V_T change and SS variation with respect to L at $T_{ox} = 1$ nm and $T_{si} = 10$ nm. SS is extracted as the change

in the gate voltage for one decade change in the drain current in the subthreshold region at a drain voltage of 50 mV. Both V_T and SS with respect to L are lower and less fluctuating for JLT than IM transistor as SCEs are improved in such devices due to its junction free nature.

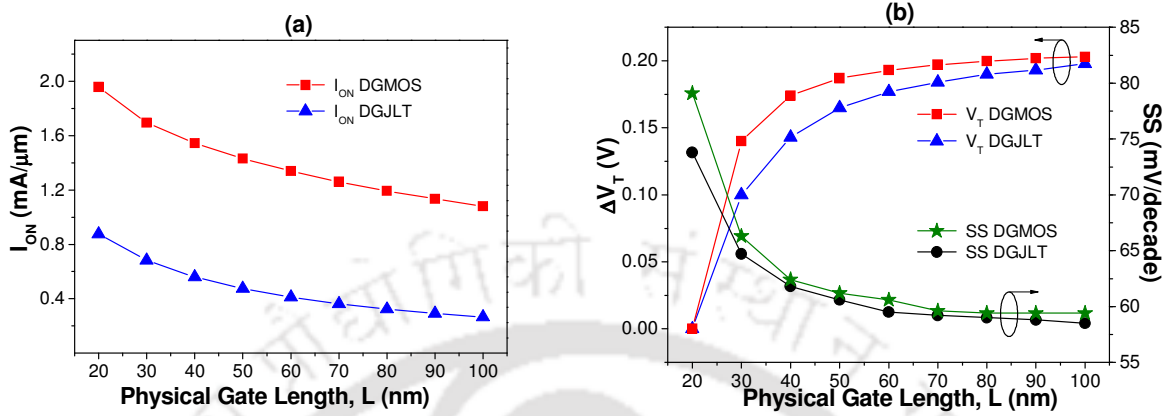


Figure 3.1: (a) I_{ON} and (b) threshold voltage and subthreshold slope variation with physical gate length at $T_{ox}=1$ nm and $T_{si}=10$ nm, channel doping concentration, $N_D=1.5 \times 10^{19} \text{ cm}^{-3}$ for DGJLT and $2 \times 10^{15} \text{ cm}^{-3}$ for DGMOS.

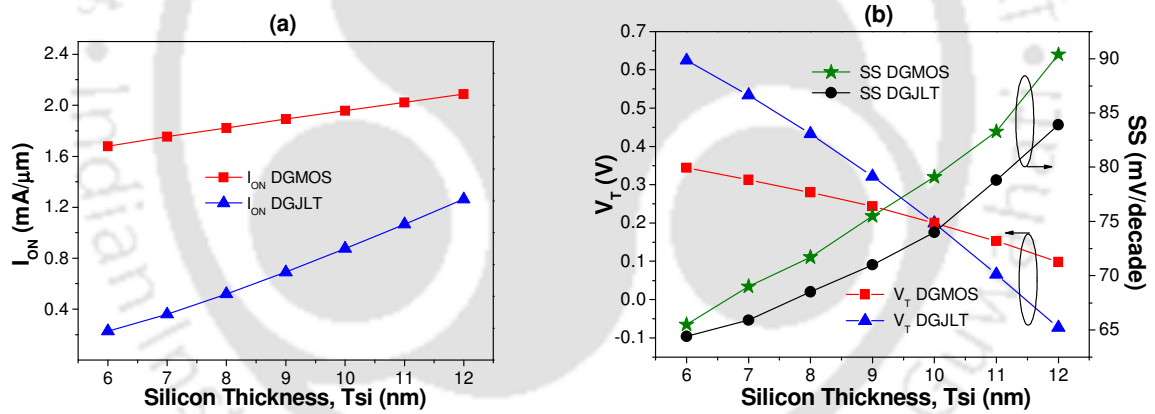


Figure 3.2: (a) I_{ON} and (b) threshold voltage and subthreshold slope variation with silicon thickness for $L = 20$ nm, $T_{ox} = 1$ nm, channel doping concentration, $N_D=1.5 \times 10^{19} \text{ cm}^{-3}$ for DGJLT and $2 \times 10^{15} \text{ cm}^{-3}$ for DGMOS.

Fig. 3.2 (a) shows the ON-state current of the devices for silicon thickness $T_{si} = 6$ nm to 12 nm at $L = 20$ nm and $T_{ox} = 1$ nm. DGJLT suffers from slightly more ON-state current variation with respect to silicon thickness compared to DGMOS. This is because, there is more V_T variation with respect to silicon thickness for DGJLT as compared to DGMOS as will be explained in next figure. V_T and SS variation with T_{si} are plotted in Fig. 3.2 (b) at $T_{ox} = 1$ nm and $L = 20$ nm. There is significant threshold voltage variation with respect to silicon thickness for DGJLT than DGMOS. Both the devices follow the almost similar variation of SS with respect to T_{si} . For inversion mode transistors

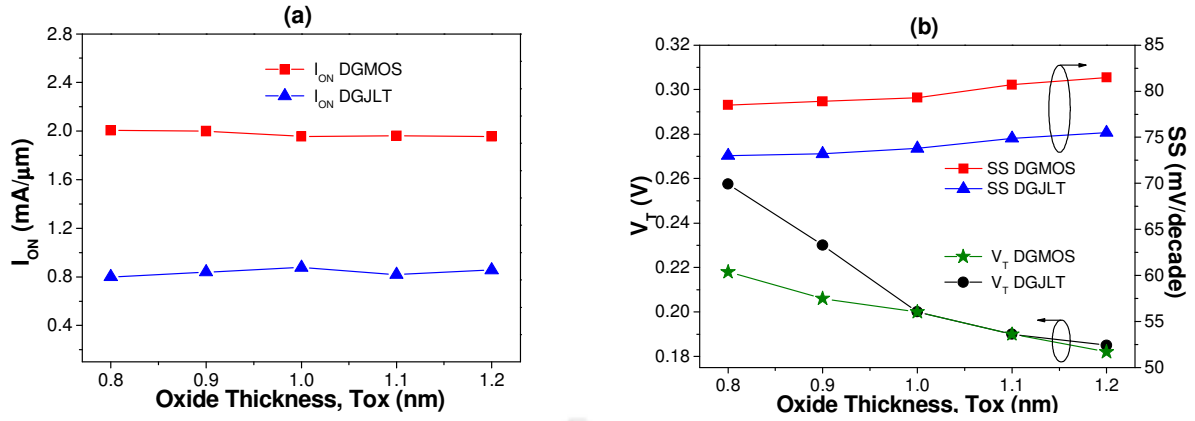


Figure 3.3: (a) I_{ON} and (b) threshold voltage and subthreshold slope variation with gate oxide thickness at $L = 20$ nm, $T_{si} = 10$ nm, channel doping concentration, $N_D = 1.5 \times 10^{19} \text{ cm}^{-3}$ for DGJLT and $2 \times 10^{15} \text{ cm}^{-3}$ for DGMOS.

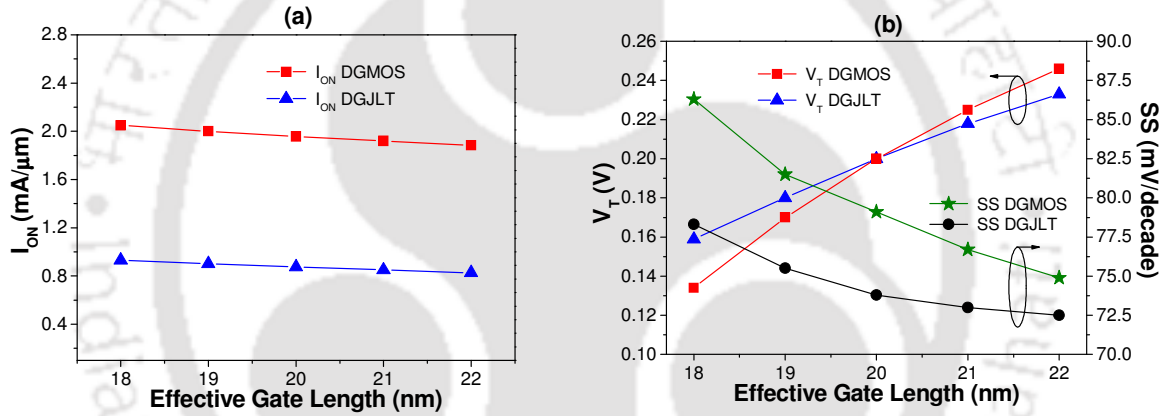


Figure 3.4: (a) I_{ON} and (b) threshold voltage and subthreshold slope with effective gate length at $T_{si} = 10$ nm, $T_{ox} = 1$ nm, channel doping concentration, $N_D = 1.5 \times 10^{19} \text{ cm}^{-3}$ for DGJLT and $2 \times 10^{15} \text{ cm}^{-3}$ for DGMOS.

there are two trends in the characteristics of V_T versus T_{si} . One, for low channel doping concentration (10^{15} cm^{-3} to 10^{16} cm^{-3}), SS decreases with increasing T_{si} and hence V_T decreases. In contrast, with channel doping concentrations greater than 10^{19} cm^{-3} threshold voltage increases with thickness (not shown) [41]. On the other hand, JLT needs a heavily doped channel to ensure a high ON-state current while keeping flat band condition at the ON-state [26, 30]. More sensitivity of V_T in DGJLT may be attributed to the random dopants in highly doped channel in JLT.

Variation of ON-state current with gate oxide thickness is plotted in Fig. 3.3 (a) for $T_{ox} = 0.8$ nm-1.2 nm at $T_{si} = 10$ nm and $L = 20$ nm. For inversion mode transistor, ON-state current decreases very marginally as oxide thickness increases. Because, as T_{ox} increases, gate to source/drain capacitance decreases (C is inversely proportional to T_{ox}) and hence ON-state current increases. However, the

trend is dissimilar for DGJLT. ON-state current marginally increases from $T_{ox} = 0.8$ nm to 1 nm, after which it decreases slowly. V_T and SS variation with T_{si} are shown in Fig. 3.3 (b) at $T_{si} = 10$ nm and $L = 20$ nm. SS variation with gate oxide is almost same for DGJLT and DGMOS. Threshold voltage variation with gate oxide is more for DGJLT than DGMOS especially below T_{ox} of 1 nm. When oxide thickness is very thin, gate has more impact on the channel. At higher gate voltage ($V_{GS} = 1$ V), the random dopant fluctuation is more, which shifts the threshold voltage considering at very lower oxide thickness. The ON-state current variation with effective gate length (L_{eff}) is plotted in Fig. 3.4 (a) for $L_{eff} = 18$ nm–22 nm at $T_{si} = 10$ nm and $T_{ox} = 1$ nm. The variation is almost equal for the devices. V_T and SS variation with L_{eff} are plotted in Fig. 3.4 (b) at $T_{si} = 10$ nm and $T_{ox} = 1$ nm. The variation in V_T and SS with channel length is larger for inversion mode device due to the resistance of the gate overlap/underlap region [77].

3.3 High-Temperature Effects on Device Performance of DGJLT

3.3.1 Device Structure and Simulation Setup

The device structure for an n-type symmetric DGJLT and DGMOS are shown in Fig. 2.1. Threshold voltage of the device is fixed at 0.25 V which corresponds to drain current of 10^{-7} A at drain voltage, $V_{DS} = 50$ mV at room temperature. The corresponding gate workfunction at this V_T are 5.35 eV for DGJLT and 4.8 eV for DGMOS respectively. The source-channel-drain region has uniform n-type doping concentration (N_D) of value $1.5 \times 10^{19} \text{ cm}^{-3}$ for all simulations. HfO_2 is used as gate oxide material having equivalent oxide thickness (EOT) of 1 nm (T_{ox}). The silicon thickness (T_{si}) is taken as 10 nm. The source/drain extensions (L_S/L_D) are taken as 20 nm. Drain voltage is taken as 1 V. The simulations are carried out using two carriers Fermi-Dirac model without impact ionization to account for highly doped channel, band-gap narrowing (BGN) and Schottky–Read–Hall (SRH) recombination models are included in simulations. As high-k gate dielectric materials are used, quantum models are not incorporated for gate leakage purpose. The mobility model includes both doping and transverse-field dependence.

3.3.2 Simulation Results and Discussion

Fig. 3.5 (a) and 3.5 (b) shows the I_D - V_{GS} characteristics of the devices at $V_{DS} = 1$ V in both linear and log scale. With increase in temperature (T), the threshold voltage decreases and hence the drain current increases for both the devices. In inversion mode (IM) devices, though V_T reduction increases I_D , mobility reduction due to phonon scattering eventually decreases the drain current [79, 80]. At a particular gate voltage of ~ 0.8 V, both these effects compensate each other and it is called the “zero

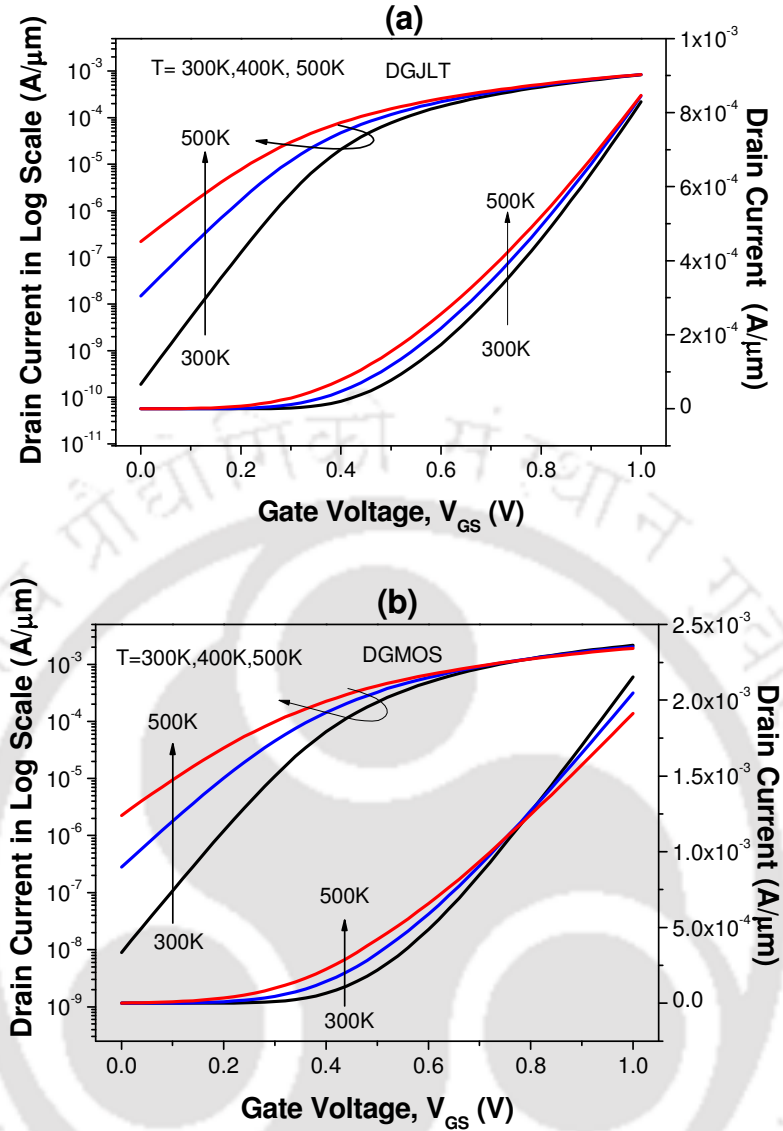


Figure 3.5: I_D - V_{GS} characteristics at various temperatures of $T_{si} = 10$ nm, $T_{ox} = 1$ nm, $L = 20$ nm at $V_{DS} = 1$ V for (a) DGJLT (b) DGMOS. Channel doping concentration, $N_D = 1.5 \times 10^{19} \text{ cm}^{-3}$ for DGJLT and $2 \times 10^{15} \text{ cm}^{-3}$ for DGMOS.

temperature coefficient" (ZTC) point. However, in JLTs, reduction in mobility with temperature is much lower than other type of transistors and hence current increases monotonously and there is no ZTC point [42].

Fig. 3.6 shows the ON-state and OFF-state current for the devices at different temperatures at a drain voltage of 1 V. I_{ON} and I_{OFF} are extracted at gate voltage of 1 V and 0 V respectively. I_{ON} is higher for IM devices as compared to JLT due to higher mobility in the former. The ON-state current of DGJLT increases very marginally with increase in temperature till 400 K, after which I_{ON} is almost independent of temperature. Mobility in a highly doped JLT is governed by impurity scattering which varies by $T^{3/2}$ and phonon scattering which varies by $T^{-3/2}$ [81]. Both the effects compensate with each

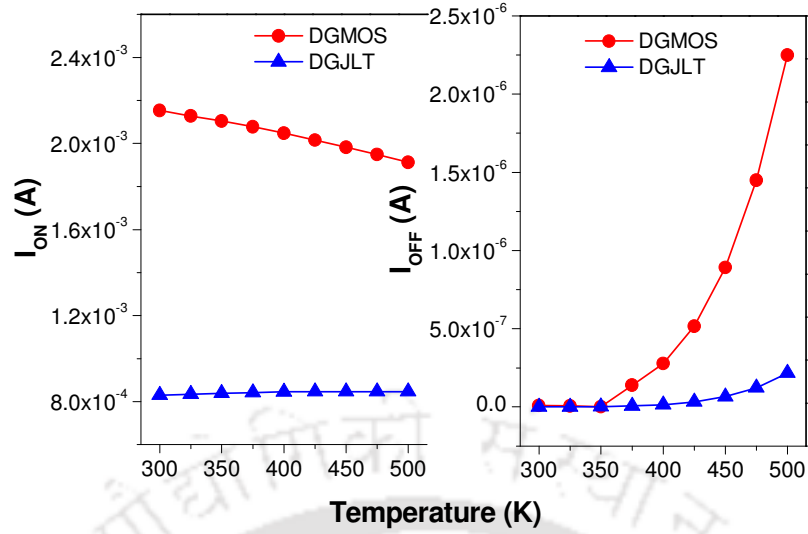


Figure 3.6: I_{ON} and I_{OFF} variation with Temperature of $T_{si} = 10$ nm, $T_{ox} = 1$ nm, $L = 20$ nm at $V_{DS}=1$ V. Channel doping concentration, $N_D=1.5 \times 10^{19} \text{ cm}^{-3}$ for DGJLT and $2 \times 10^{15} \text{ cm}^{-3}$ for DGMOS.

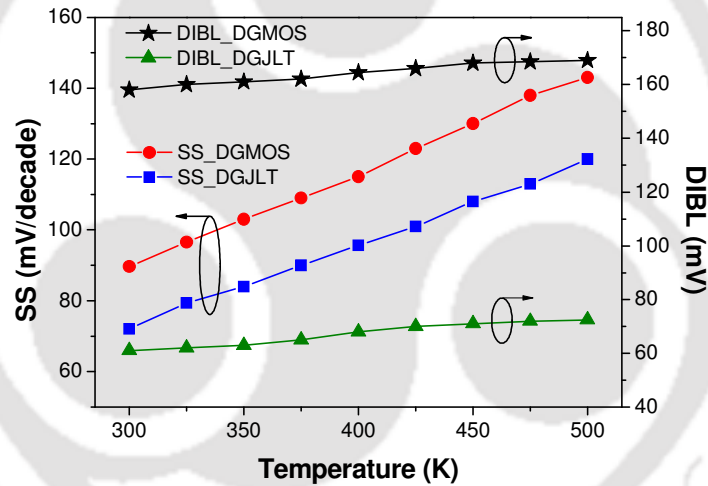


Figure 3.7: Subthreshold slope and drain-induced barrier lowering variation with temperature of $T_{si} = 10$ nm, $T_{ox} = 1$ nm, $L = 20$ nm. Channel doping concentration, $N_D=1.5 \times 10^{19} \text{ cm}^{-3}$ for DGJLT and $2 \times 10^{15} \text{ cm}^{-3}$ for DGMOS.

other and mobility is almost independent of temperature. As expected, ON-state current of DGMOS decreases with increase in temperature due to reduction of surface mobility by phonon scattering. The OFF-state current increases with increase in temperature due to increase in intrinsic carrier concentration n_i . The leakage current increases rapidly with increase in temperature for DGMOS after 350 K. However, for DGJLT, leakage current increases very slowly till temperature of 400 K after which it increases faster. Fig. 3.7 presents SS and DIBL variation as a function of V_{GS} at different temperatures. SS represents the OFF-to-ON switching capability of a device. Due to junction free nature, JLT offers better SCEs making SS and DIBL lower as compared to inversion mode

counterpart as mentioned in previous chapter. As DIBL predicts I_{ON}/I_{OFF} ratio, it is a key parameter for low-voltage CMOS [82]. SS and DIBL increases monotonously with increase in temperature for both the devices. Both SS as well as DIBL variations with temperature are almost similar for the devices.

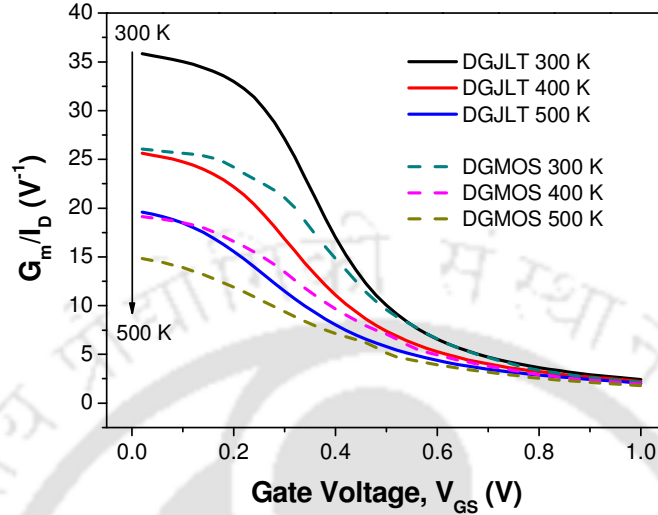


Figure 3.8: G_m/I_D variation with temperature of $T_{si} = 10$ nm, $T_{ox} = 1$ nm, $L = 20$ nm at $V_{DS} = 1$ V. Channel doping concentration, $N_D = 1.5 \times 10^{19} \text{ cm}^{-3}$ for DGJLT and $2 \times 10^{15} \text{ cm}^{-3}$ for DGMOS.

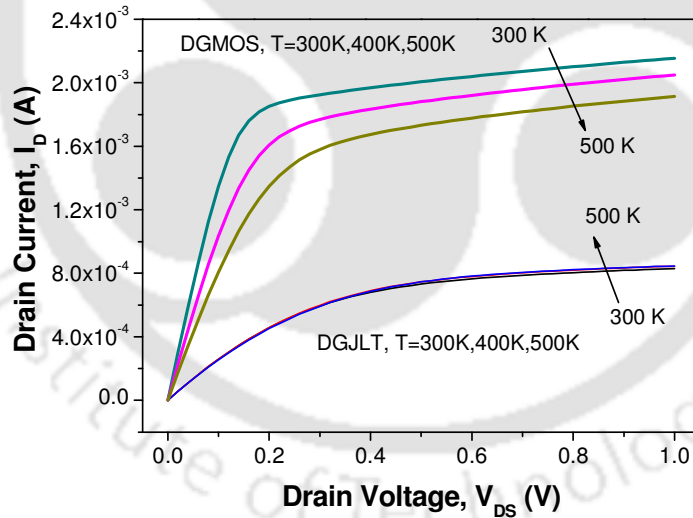


Figure 3.9: Drain current variation with respect to drain voltage at different temperatures of $T_{si} = 10$ nm, $T_{ox} = 1$ nm, $L = 20$ nm at $V_{GS} = 1$ V. Channel doping concentration, $N_D = 1.5 \times 10^{19} \text{ cm}^{-3}$ for DGJLT and $2 \times 10^{15} \text{ cm}^{-3}$ for DGMOS.

Fig. 3.8 presents G_m/I_D variation with temperature at $V_{DS} = 1$ V. In the subthreshold region, G_m/I_D is higher for DGJLT as compared to DGMOS for all temperature ranges because of lower subthreshold current of the former. G_m/I_D decreases with increase in temperature for both the devices in the subthreshold region. Both show almost similar behaviour because of their similar body factor. When

operated at ON-state gate voltage ($V_{GS} = 1$ V), G_m/I_D of both the devices are independent of temperature. Fig. 3.9 shows the drain current variation with respect to drain voltage at different temperatures for a gate voltage of 1 V. Due to reduction of mobility with increase in temperature, drain current with respect to drain voltage decreases with an increase in temperature for DGMOS.

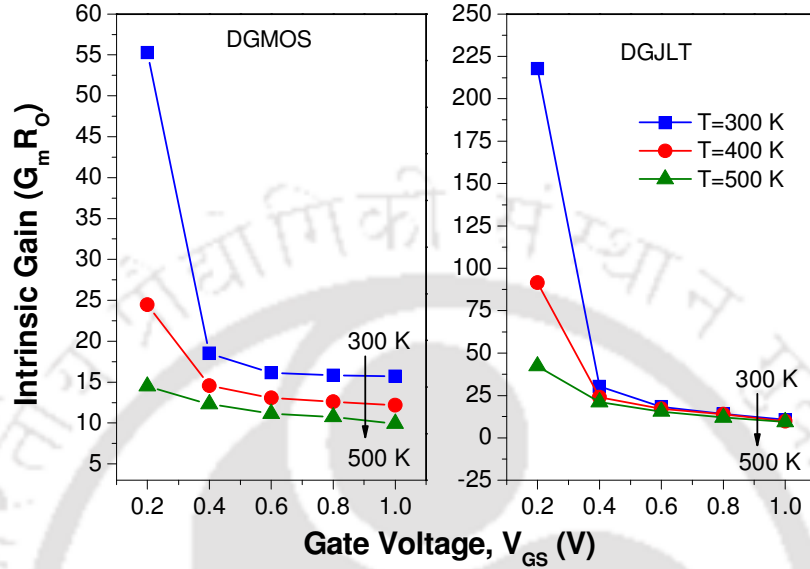


Figure 3.10: Intrinsic gain ($G_m R_O$) variation with respect to gate voltage at different temperatures of $T_{si} = 10$ nm, $T_{ox} = 1$ nm, $L = 20$ nm at $V_{DS} = 1$ V. Channel doping concentration, $N_D = 1.5 \times 10^{19} \text{ cm}^{-3}$ for DGJLT and $2 \times 10^{15} \text{ cm}^{-3}$ for DGMOS.

However, as aforementioned, in JLTs, the mobility is less sensitive to temperature. Therefore, current increases only marginally with increase in temperature. Fig. 3.10 shows the intrinsic gain ($G_m R_O$) of the devices as a function of gate voltage at a drain voltage of 1 V. $G_m R_O$ decreases with increase in temperature for both the devices; though the change is more for DGMOS compared to DGJLT. As seen from the figure, at a gate voltage greater than ~ 0.7 V where the device will be actually biased for high frequency operations, the intrinsic gain of DGJLT is almost independent of temperature. This is again due to lesser mobility change in DGJLT as compared to DGMOS. An input sinusoidal small signal with 1 MHz frequency coupled with DC bias is applied to the gate electrode for ac simulations. The gate capacitance $C_{GG} (= C_{GS} + C_{GD})$ is shown in Fig. 3.11. The gate capacitance is lower in JLT as compared to IM devices. In IM devices, the channel is exactly under the gate oxide and gate capacitance is given by $W \times L \times C_{ox}$ for low V_{DS} . Where C_{ox} is the oxide capacitance and W is the width. However, for a DGJLT, channel is buried in the centre of the silicon layer. Gate capacitance is series combination of C_{ox} and C_{depl} , where C_{depl} is the capacitance of the depletion region between Si-HfO₂ interface and the channel [59]. So, the minimum gate capacitance ($C_{GG \min}$) can be expressed as

$$C_{GG \min} = \frac{C_{ox} \cdot C_{depl}}{C_{ox} + C_{depl}} \quad (3.1)$$

Lower value of gate capacitance helps in lowering the intrinsic delay of the device. Fig. 3.12 shows the unity gain cut-off frequency ($f_T = G_m / \{2\pi(C_{GS} + C_{GD} + C_{GB})\}$) as a function of gate voltage for different temperatures for both the devices.

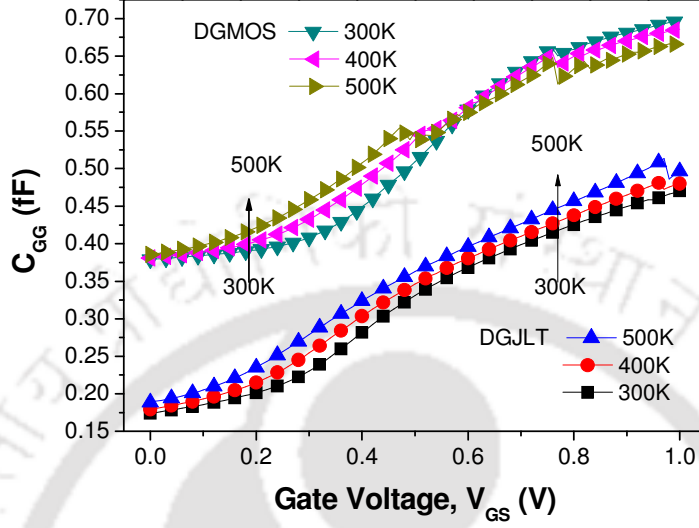


Figure 3.11: Gate capacitance (C_{GG}) as a function of gate voltage at different temperatures of $T_{si} = 10$ nm, $T_{ox} = 1$ nm, $L = 20$ nm at $V_{DS} = 1$ V. Channel doping concentration, $N_D = 1.5 \times 10^{19} \text{ cm}^{-3}$ for DGJLT and $2 \times 10^{15} \text{ cm}^{-3}$ for DGMOS.

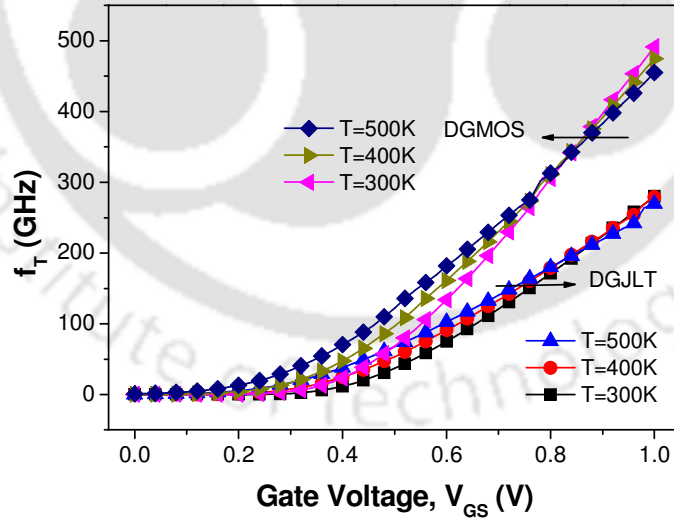


Figure 3.12: Unity gain cutoff frequency (f_T) as a function of gate voltage at different temperatures of $T_{si} = 10$ nm, $T_{ox} = 1$ nm, $L = 20$ nm at $V_{DS} = 1$ V. Channel doping concentration, $N_D = 1.5 \times 10^{19} \text{ cm}^{-3}$ for DGJLT and $2 \times 10^{15} \text{ cm}^{-3}$ for DGMOS.

f_T is higher for DGMOS as compared to DGJLT because of higher G_m in the former. f_T is higher for higher temperature for both the devices till gate voltage of ~ 0.85 V after which the case is reversed in

accordance with aforementioned ZTC point. The temperature dependence of current source CMOS inverter is shown below. The Q-point shifts towards left with an increase in temperature. The gain decreases with increase in temperature as shown in the Fig. 3.13. Though junctionless transistors show better temperature performance than JB counterpart, silicon carbide (SiC) is still more preferred at very high temperature; because at such temperature, I_{OFF} increases for JLT than SiC device.

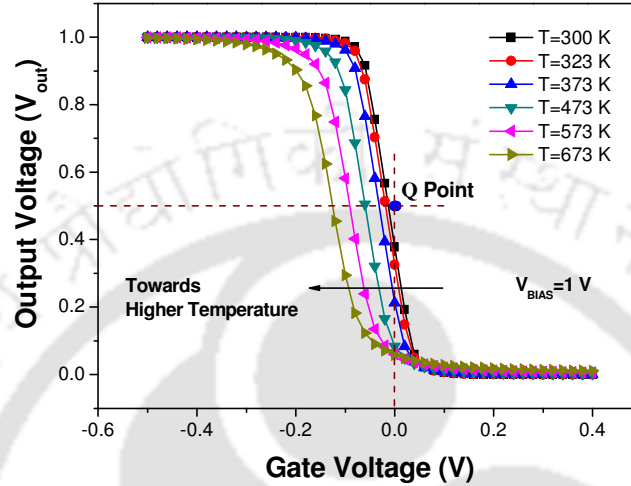


Figure 3.13: Temperature dependence of current source CMOS inverter. $T=27^{\circ}\text{C}-400^{\circ}\text{C}$. $V_{\text{bias}}=1\text{ V}$, $L=20\text{ nm}$, $T_{\text{si}}=10\text{ nm}$, $\text{EOT}=1\text{ nm}$.

3.4 Summary

The effects of variations in process parameters on the electrical characteristics of a junctionless symmetric double-gate transistor (DGJLT) were explored and compared with inversion mode counterpart with the help of extensive device simulations. ON current variation with respect to T_{si} was higher for DGJLT compared to DGMOS. V_T variation with respect to silicon thickness and oxide thickness is greater for DGJLT compared to DGMOS. The variation of V_T with respect to physical channel length is comparatively lesser in DGJLT than DGMOS. The SS variation with respect to L , T_{si} and T_{ox} were almost similar for both devices. In summary, DGJLT electrical parameters were more immune to channel length variations, while DGMOS were immune to T_{si} and T_{ox} variations.

Temperature dependence of the electrical characteristics of an n-type DGJLT is investigated. I_{ON} increases negligibly with increase in temperature for DGJLT; in contrast it follows the opposite trend in DGMOS. Drain current with respect to drain voltage increases with increase in increase in temperature, following the opposite trend in DGMOS. Intrinsic gain decreases with respect to T for DGMOS; however, for DGJLT, it is almost independent of temperature after a gate voltage of $\sim 0.6\text{ V}$. The trend of f_T change with temperature is same for both the devices.

Chapter 4

The Effect of High-k Gate Dielectrics on Device and Circuit Performances of a JLT and its Solution

4.1 Introduction

According to International Technology Roadmap for Semiconductors (ITRS), the recent CMOS technologies demand an oxide thickness of 1 nm or even less for sufficient current drive capability, which corresponds to approximately two to three layers of silicon dioxide atoms. This leads to an increase in the direct tunneling of carriers from gate to channel region leading to an exponential increase in the gate leakage current. The leakage current increases the power dissipation and deteriorates the device performance and circuit stability. Also, the parasitic capacitances due to aggressive device dimension reduction, critically affect the propagation delay of digital circuits and gain-bandwidth product for analog circuits. Therefore, conventional gate dielectric material, SiO_2 may be replaced by high-k gate dielectrics such as Al_2O_3 ($k=9.3$), HfO_2 ($k=22$) and TiO_2 ($k=50$) etc., in order to reduce the gate tunnelling current. However, in a conventional MOSFET, high-k gate dielectric results in fringing induced barrier lowering (FIBL), which degrades the short channel performance of the device [83-84]. There are many reports on the affect of high-k gate dielectric on device performance of tunnel FETs [85-86] as well. For junctionless transistor (JLT) also, high-k gate dielectric worsens the SCE due to band-to-band tunneling [51-52, 87-89]. It is reported that using high-k spacers on both sides of the gate dielectrics the device performance can be improved [90]. There are reports that junctionless transistors have great potential towards circuit applications [91]. A junctionless transistor can be a prospective candidate for future technology nodes because it offers extremely low power in subthreshold region circuit performances [92]-[93]. However, there is no report on the effect of high-k gate dielectric on analog and circuit performances of a JLT. In this work, we have studied the drain induced barrier lowering (DIBL), transconductance (G_m), intrinsic gain ($G_m R_O$), gate capacitance (C_{GG}) and unity gain cut-off frequency for a DGJLT with respect to gate dielectric permittivity (k) and compared the results with conventional DG MOSFET. The gain of

CMOS single stage amplifier and delay of single stage inverter are also studied. As a solution to severe SCEs due to high fringing fields arising out of high-k gate dielectrics, a hetero-gate-dielectric transistor is implemented in two different device architectures i.e., tunnel field-effect-transistor and junctionless transistor. The investigation of analog circuit performance parameters of a hetero-gate-dielectric junctionless transistor are still lacking in literature and the same is investigated in this chapter.

4.2 Device Structure and Simulation Setup

The device structure for an n-type symmetric DGJLT and DGMOS are shown in Fig. 2.1. The silicon thickness, equivalent oxide thickness (EOT) of the gate-dielectrics and source and drain extensions (L_S and L_D) of the devices are taken as 10 nm, 1 nm and 10 nm, respectively, for all simulations. Such a small value of source/drain length is taken to avoid the parasitic resistance effects. We understand the fabrication difficulties for incorporating such a small dimensions, but we are keen on the theoretical investigation as of now. The gate workfunction values of both DGJLT and DGMOS are tailored to obtain a threshold voltage (V_T) of 0.25 V corresponding to $I_D=10^{-7}$ A at $V_{DS}=50$ mV. The channel doping concentration (N_D) is $1 \times 10^{19} \text{ cm}^{-3}$ for DGJLT. For DGMOS, source and drain doping concentrations are $1 \times 10^{20} \text{ cm}^{-3}$ and for channel it is $2 \times 10^{15} \text{ cm}^{-3}$. The corresponding gate workfunctions at this V_T are 5.159 eV, 4.307 eV for n/p DGJLT and 4.772 eV, 4.687 eV for n/p DGMOS, respectively. Electrical characteristics for the devices are simulated using 2D ATLAS device simulator with default Silvaco parameters. Lombardi mobility model is employed, accounting for the dependence on the impurity concentrations as well as the transverse and longitudinal electric field values. Shockley-Read-Hall (SRH) recombination model is included in the simulation to account for leakage currents. Because of high channel doping concentration, Fermi-Dirac carrier statistics without impact ionization is utilized in the simulations. Band gap narrowing model (BGN) is also incorporated to take care of the band gap narrowing effect which may arise due to highly doped channel regions. The density gradient model was utilized to account for quantum mechanical effects.

4.3 Simulation Results and Discussion

High-k gate dielectrics are used in CMOS technology to attain a lower equivalent oxide thickness (EOT) with higher physical thickness. EOT scaling with the help of high-k/metal gate is crucially important to suppress not only gate leakage current but also to severe short-channel effect and random threshold voltage variation. Even though high-k gate dielectric with same EOT does not change the gate capacitance, it affects the electric fields along the parallel and perpendicular directions of the oxide interface. For a constant EOT, gate dielectrics with higher k value have more fringing fields to

source/drain region, which further induce electric fields to channel region, and weakens the gate control and can affect the device performance. Fig. 4.1 shows the drain current with respect to gate voltage of the DGJLT at a drain voltage of 1 V. As can be seen from the figure, DGJLT has almost same ON-state current for different values of k . This is because; JLT has near zero vertical electric field in the ON-state, i.e., it is in flatband region. Thus, any increase in the electric field due to high- k

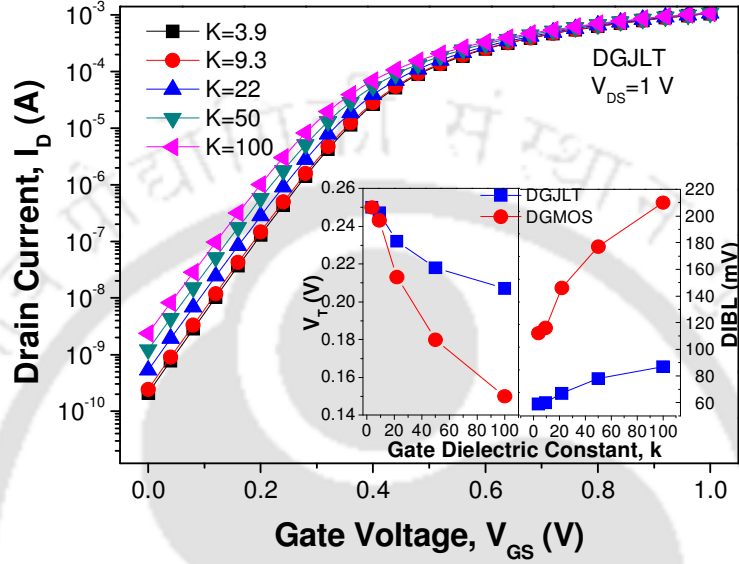


Figure 4.1: Drain current (I_D) versus gate voltage (V_{GS}) for n-DGJLT at $V_{DS} = 1$ V. In inset threshold voltage (V_T) at $V_{DS} = 50$ mV and DIBL for both DGJLT and DGMOS are shown. $T_{si} = 10$ nm, $T_{ox} = 1$ nm, $L = 20$ nm.

gate dielectric does not affect the ON-state current much. The OFF-state current increases with increase in gate dielectric permittivity. This results in decrease in I_{ON}/I_{OFF} with increase in k . There is a V_T decrease with increase in k for both the devices. However, the V_T shifts are higher for DGMOS with increase in k as shown in inset of Fig. 4.1. A junctionless transistor has higher threshold voltage when the channel region is fully depleted [52]. With increased fringing fields with high- k gate dielectric, the channel region is no longer fully depleted and hence the threshold voltage is decreased and thereby the OFF-state current increases. Due to higher fringing electric fields, the electric field towards the drain increases which degrades the drain induced barrier lowering (DIBL) (inset of Fig. 4.1). DIBL is defined as the shift in threshold voltage when drain-to-source voltage, V_{DS} changes from 50 mV to 1V. Fig. 4.2 (a) and 4.2 (b) show the transconductance (G_m) and intrinsic gain ($G_m R_O$) at $V_{GS} = V_{DS} = 1$ V. As can be seen from the figure, G_m and $G_m R_O$ decreases with increase in k for both the devices. However, DGMOS has more decrease in $G_m R_O$ with increase in k compared to DGJLT which is explain below. When the drain current of junctionless and inversion mode (IM) transistors of similar dimensions is compared at the same $V_{GT} (= V_{GS} - V_T)$, a higher drain current is observed in the

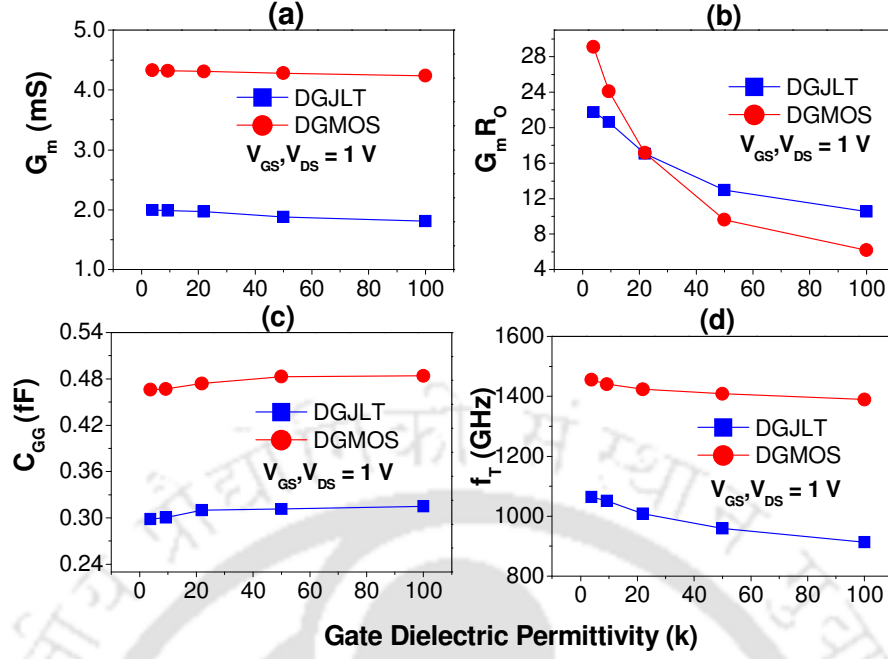


Figure 4.2: (a) Transconductance (G_m), (b) intrinsic gain ($G_m R_o$), (c) gate capacitance (C_{GG}) and (d) unity gain cut-off frequency (f_r) at $V_{GS} = V_{DS} = 1$ V. $T_{si} = 10$ nm, $T_{ox} = 1$ nm, $L = 20$ nm.

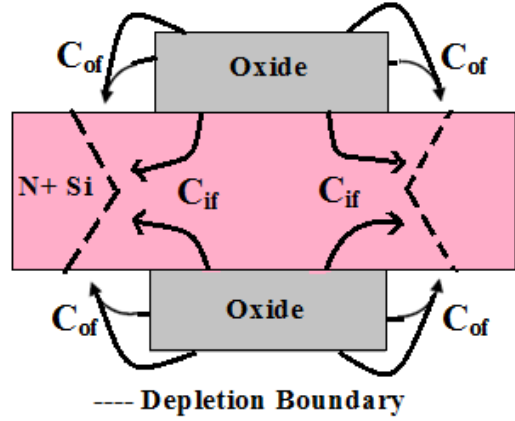


Figure 4.3: Inner (C_{if}) and outer (C_{of}) fringing capacitance of DGJLT. Dashed line shows depletion boundary.

IM device. This behaviour is attributed to the smaller low-field mobility of carriers in junctionless devices due to a higher doping concentration in the channel region [42] as mentioned. Therefore, transconductance of junctionless transistor is inferior to corresponding IM counterpart. In spite of reduced mobility, the I_{ON}/I_{OFF} characteristics of JL transistors can fulfil the requirements expected by the International Technology Roadmap for Semiconductors [2]. As mentioned above, JLT operates nearby the flatband region in accumulation region and therefore G_m is not affected much with increase in k . With increase in gate dielectric constants, fringing fields on both sides of the gate oxide are enlarged resulting in the higher gate-to-drain coupling and as a consequence, a high electric field is

created at the drain side. This results in high V_{DS} dependency on the drain currents and therefore, deteriorates the output impedance (R_O). Thereby the gain ($= G_m R_O$) decreases with increase in k . The effect of k on R_O is higher for IM transistor. So, gain of DGMOS is affected much more compared to DGJLT. Fig. 4.2 (c) and 4.2 (d) shows the gate capacitance (C_{GG}) and unity gain cut-off frequency ($f_T = G_m / 2\pi \times (C_{GS} + C_{GD})$) with respect to k . As expected, C_{GG} increases with k for both the devices. The decrease in f_T with k for the devices has a similar trend. C_{GS} and C_{GD} are gate to source and gate to drain capacitance respectively. All the capacitances are extracted from the small-signal ac device simulations at a frequency of 1 MHz. Fig. 4.3 shows the inner (C_{if}) and outer (C_{of}) fringing capacitances in a DGJLT. An increase in fringing field results in higher values of parasitic capacitance. The dominant contribution to the reduction in the capacitance is due to the inner fringing which is governed by the extension of the depletion width beyond the gate edge [94].

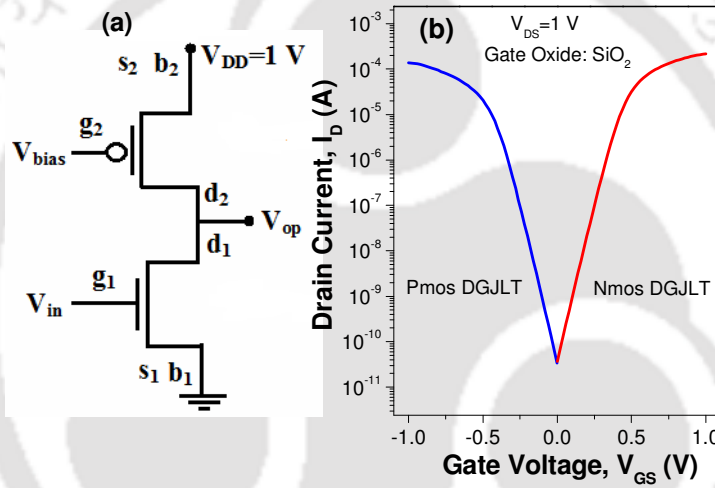


Figure 4.4: (a) Current source CMOS inverter amplifier with the n-channel device as a driver and the p-channel device as source (b) Drain current of n and p-DGJLT with SiO_2 as gate oxide at $V_{DS}=50\text{mV}$ for $T_{si}=10\text{ nm}$, $T_{ox}=1\text{nm}$, $L=20\text{ nm}$.

As shown in Fig. 4.4 (a), the current source CMOS inverter amplifier with the n-type device as a driver and the p-type device as source, biased by a dc voltage V_{bias} , as an active load is used to investigate the analog performance of the junctionless device. The gain formula ($A_v = G_m R_D$) of a single stage common source amplifier, suggests that the load impedance (R_D) may be increased to obtain high gain. However, increase in R_D limits the output voltage swing. Therefore, resistor in CS amplifier is replaced by current source load and the gain of the amplifier is

$$A_v = -G_{m1} (r_{o1} \parallel r_{o2}) \quad (4.1)$$

Where, r_{o1} and r_{o2} are the output resistances of NMOS and PMOS transistors (Fig. 4.4 (a)). Mixed-mode capability of the device simulator ATLAS of SILVACO-TCAD is used to simulate the

performance of this circuit. The width and workfunction of the n/p-type MOS devices are adjusted to make the current same for both the devices as shown in Fig. 4.4 (b).

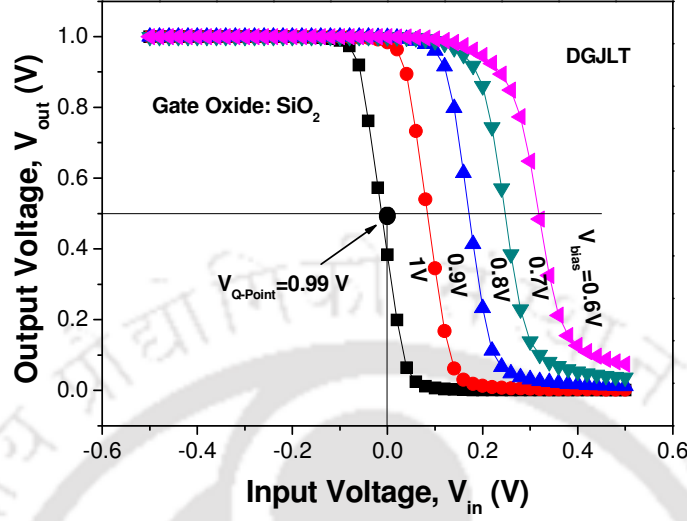


Figure 4.5: Voltage Transfer Curves (VTC) of the amplifier for different values of V_{bias} at $N_D = 1 \times 10^{19} \text{ cm}^{-3}$ for $T_{si} = 10 \text{ nm}$, $T_{ox} = 1 \text{ nm}$, $L = 20 \text{ nm}$.

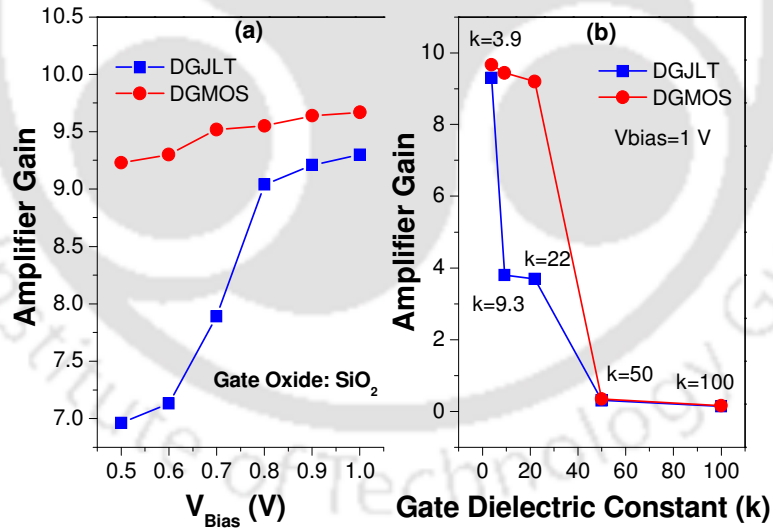


Figure 4.6: (a) Amplifier gain with respect to V_{bias} with SiO_2 as gate oxide (b) Amplifier gain with respect to gate dielectric constant for $V_{bias} = 1 \text{ V}$. $T_{si} = 10 \text{ nm}$, $T_{ox} = 1 \text{ nm}$, $L = 20 \text{ nm}$.

Fig. 4.5 shows the voltage transfer characteristics (VTC) of the CMOS amplifier (with n and p-type DGJLT) for different values of V_{bias} . The slope of this transition region is a measure of quality-steep slope which yield precise switching. As the V_T of the n and p-type devices are set at $+0.25\text{V}$ and -0.25V respectively for a channel doping concentration of $N_D = 1 \times 10^{19} \text{ cm}^{-3}$; the amplifier with a supply voltage of 1 V should be in subthreshold regime for a $V_{bias} > 0.75\text{V}$. The VTC corresponding to

$V_{bias} = 0.99$ V (named $V_{Q-point}$) meets 0 in the V_{in} curve and 0.5V in V_{out} curve. The amplifier gain with respect to V_{bias} for the devices is shown in Fig. 4.6 (a). As obvious, gain increases with V_{bias} for the devices. Gain is extracted from VTC as $\Delta V_{out}/\Delta V_{in}$ in the transition region. Fig. 4.6 (b) presents the amplifier gain variation with k . Output impedance of the amplifier decreases significantly with increase in k . This behaviour is due to the degradation of the slope of VTC (proportional to $1/R_O$) because of increased fringing field and decreased V_T . Therefore, gain decreases with increase in k . Similar trend of gain degradation with increase of k is observed for differential amplifier as well.

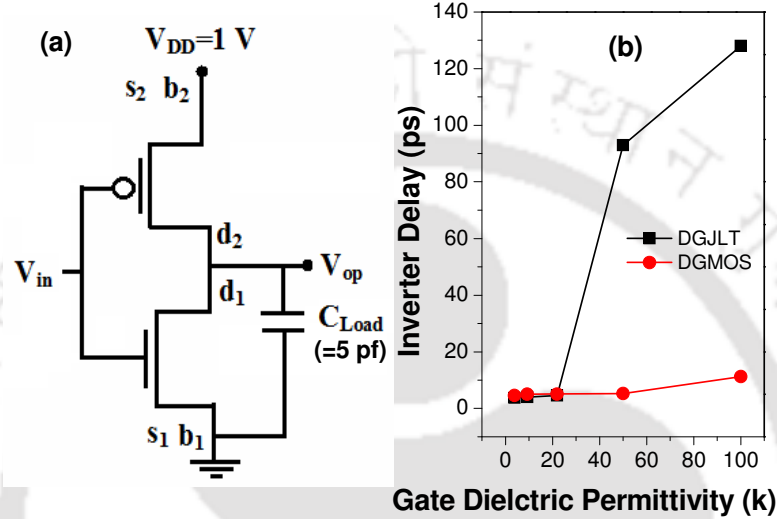


Figure 4.7: (a) CMOS inverter ($C_{Load} = 5\text{pf}$) (b) Inverter delay with respect to gate dielectric permittivity k at $V_{DD} = 1$ V. $T_{si} = 10$ nm, $T_{ox} = 1$ nm, $L = 20$ nm.

To study the impact of high- k gate dielectrics on digital circuits, a CMOS inverter (Fig. 4.7 (a)) is taken, which is the universally accepted, most basic Boolean operation on a single input variable. The outputs of the PMOS and NMOS transistors are complementary such that when the input is low, the output is high, and when the input is high, the output is low. Because of this behaviour of input and output, the CMOS circuits' output is the inverse of the input. The inverter delay or propagation delay defines how quickly output is affected by input. The propagation delay is usually defined at the 50% level, but sometimes the propagation delay can be defined at other voltage levels as well. The t_{pLH} defines delay for output going from low to high, t_{pHL} defines delay for output going from high to low and overall delay, t_p is defined as the average of t_{pLH} and t_{pHL} . The non-zero propagation delay is due to the capacitive load at the output node and the limited current driving capability of the logic gate. Inverter gate delay, $\tau (= CV/I$, C is the gate capacitance, V is the supply voltage, I is the ON state current) which represents the frequency limit of the transistor operation is shown in Fig. 4.7 (b). Till $k = 22$, inverter delay is not much affected by fringing fields. For a junctionless transistor, the number of fringing field lines are more due to increase in k , and the inverter delay increases because of its increased capacitance of fringing fields at high- k . Gate delay is lesser for IM devices because of its

higher ON-state current compared to a JLT. However, though gate-delay is larger in JLT compared to IM devices, since the switching energy is smaller in JLTs, energy delay product is almost identical for both the devices [95].

4.4 Hetero-Gate-Dielectric DGJLT as a Solution of High-k gate dielectrics and Enhanced Analog Performance

To reduce the short channel effects arising from high-k gate dielectrics, recently, a hetero-gate-dielectric transistor have been studied extensively [51, 87-89]. Choi et al. reported that tunneling field-effect-transistors with hetero-gate-dielectric (HG-TFET) architecture enhances ON-state current, suppresses ambipolar behaviour and make abrupt ON-OFF transition [87]. Lee et al. demonstrated that HG-TFET offers improved subthreshold slope with an increase in channel thickness or with a decrease in the number of gate fingers, unlike a conventional TFET [88]. Ghosh et al. showed that hetero-gate-dielectric junctionless transistor reduces the band-to-band tunnelling in the subthreshold region [51]. Though subthreshold performance is reported to be improved, there is hardly any detailed literature on analog performance capabilities of hetero-gate dielectric JLT yet. We have investigated the analog circuit performance parameters of a hetero-gate-dielectric double gate JLT here and compared the results with low-k only and high-k gate only dielectric architectures of similar device dimensions.

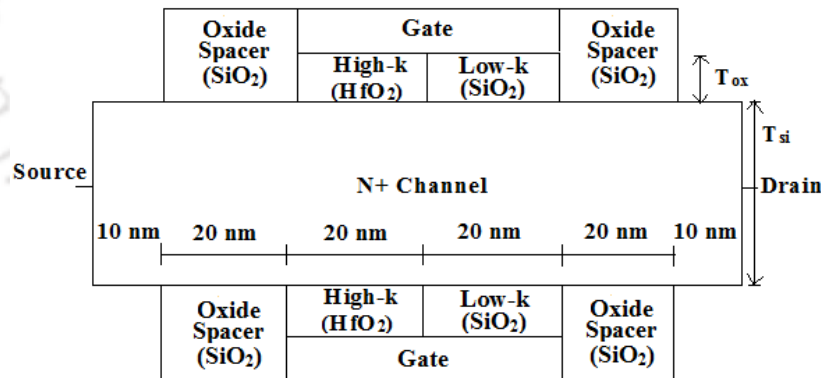


Figure 4.8: Crosssectional view of n-channel hetero-gate-dielectric symmetric double-gate junctionless transistor (HD-DGJLT).

A hetero-gate-dielectric DGJLT has two gate-oxide materials with different oxide permittivity (k) [Fig. 4.8]. The high-k oxide is placed near the source and low-k oxide is placed near the drain. HfO₂ and SiO₂ are used as high-k and low-k oxides. As explained in [87], HG-DGJLT can be fabricated by isotropic etching of SiO₂ followed by HfO₂ deposition. It is assumed that HfO₂-SiO₂ interface is abrupt as was taken in [51, 87-88] and the diffusion length of HfO₂ in SiO₂ was considered to be ~

0.035 nm in the annealing of the device at 1000° C for 5 seconds [96]. Oxide spacers (SiO_2) are placed on both sides of the gate oxide. The use of spacers on both side of the gate enhances the gate-channel fringing electric field through the spacer and confines it in the channel region resulting in extension of depletion layers beyond the gate edges [90] as mentioned. It reduces the peak of the electric fields in channel and thus subthreshold performance is improved. The length of high-k and low-k gate-dielectrics is taken as 20 nm each. The length of spacers is 20 nm each. Silicon thickness is taken as 10 nm. The equivalent oxide thickness (EOT) of the gate-dielectrics is 1 nm. The gate workfunction values of all three devices namely, HG-DGJLT, SiO_2 -only and HfO_2 -only are tailored to obtain a threshold voltage (V_T) of 0.3 V at $V_{DS} = 50$ mV. The channel doping concentration (N_D) is $1.1 \times 10^{19} \text{ cm}^{-3}$. The source and drain regions (L_S and L_D) are taken as 10 nm. In addition to the models used in earlier section, a nonlocal band-to-band tunneling model is added here to study band-to-band tunneling effects of hetero-gate-dielectric DGJLT.

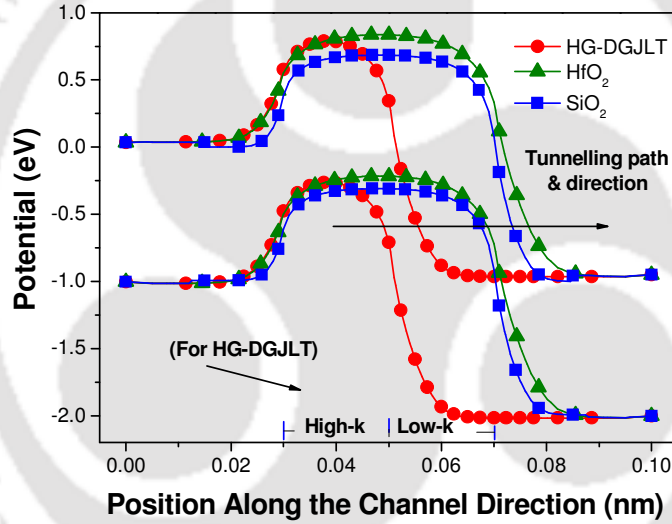


Figure 4.9: Energy band diagram for HG-DGJLT, HfO_2 -only and SiO_2 -only devices along the channel direction at 1 nm below the oxide-channel interface in OFF-state ($V_{GS}=0$ V and $V_{DD}=1$ V). $T_{Si}=10$ nm, $EOT=1$ nm, $L=40$ nm and $N_D=1.1 \times 10^{19} \text{ cm}^{-3}$.

For a junctionless transistor, OFF-state current is maintained by depletion of carriers choosing appropriate workfunction difference between gate and channel region. However, with a drain bias, because of overlapping of conduction band of drain to valance band of channel, electron tunnels from valance band of channel to conduction band of drain as shown in Fig. 4.9. While doing so, electrons leave behind holes in the channel region. The thus accumulated holes in the channel region form an npn parasitic bipolar junction (BJT) transistor with source as emitter, channel as base and drain as collector [51]. The increased potential of channel region due to accumulation of holes, switch on the BJT and by forward biasing the base-emitter junction results in huge collector current. This cost a

huge standby power dissipation. To overcome this problem, instead of using uniform gate oxide material, gate oxide with lower-k at drain side and with high-k towards source side (named HG-DGJLT) is used by many researchers as mentioned above. Therefore, in the OFF-state, the high electric field at the drain side which easily triggers electrons from valance band of channel to conduction band of drain is now reduced. The gate to channel coupling strength from source to drain

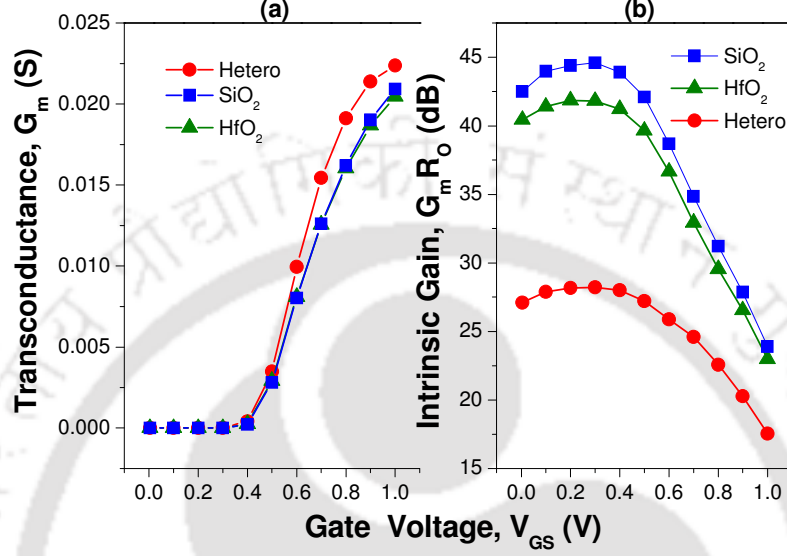


Figure 4.10: (a) Transconductance (G_m) and (b) Intrinsic Gain ($G_m R_o$) with respect to gate voltage for the devices at $V_{DS} = 1$ V. $T_{Si}=10$ nm, $EOT=1$ nm, $L=40$ nm and $N_D=1.1 \times 10^{19} \text{ cm}^{-3}$.

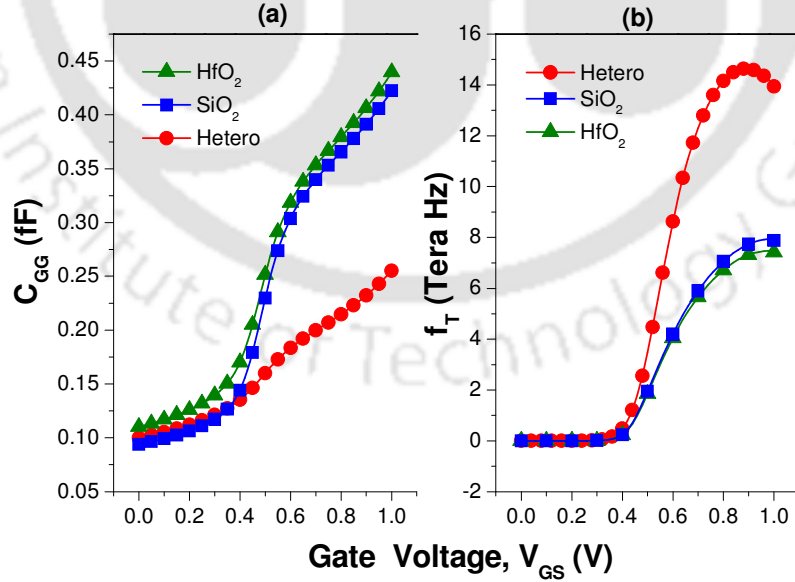


Figure 4.11: (a) Gate Capacitance (C_{GG}) and (b) Unity gain cut-off frequency (f_T) with respect to gate voltage for the devices at $V_{DS} = 1$ V. $T_{Si}=10$ nm, $EOT=1$ nm, $L=40$ nm and $N_D=1.1 \times 10^{19} \text{ cm}^{-3}$.

is non-uniform for HG-DGJLT, contrary to uniform values in SiO₂-only and HfO₂-only DGJLTs. That is, for a HG-DGJLT, because of high-k gate dielectric towards source side, there is more gate-channel

coupling towards source side producing a huge potential barrier between the source and the channel for electrons. Also, the lesser gate-channel coupling towards drain side (low-k oxide) weakens the gate to channel coupling at drain side reducing the electric field and results in a decrease of tunnelling probability of electron from valence band of channel to conduction band of drain compared to other two devices. As in heterogeneous gate dielectric DGJLT, ON-state current is determined at the source-to-channel region overlapped by the high-k material, it is higher than SiO₂-only and HfO₂-only DGJLTs. Also, as the OFF-state current is determined by the drain-to-channel region overlapped by low-k gate dielectric (SiO₂ here); HG-DGJLT is expected to offer better subthreshold characteristics. Also, HG-DGJLT reduces the formation of parasitic BJT by suppressing band-to-band tunnelling. Below a gate voltage of $V_{GS} \sim 0.4$ V, all three devices have almost similar value of G_m . Beyond $V_{GS} = 0.5$ V, HG-DGJLT has highest G_m followed by SiO₂-only and HfO₂-only DGJLT as shown in Fig. 4.10 (a). Because of higher I_{ON} for HG-DGJLT due to high-k gate oxide overlapped with source-channel region, its G_m is higher at higher gate voltage compared to other two devices. A_v with respect to V_{GS} is plotted in Fig. 4.10 (b). HG-DGJLT has the much lower value of gain compared to other two devices due to lower value of output resistance (not shown), though it has comparatively higher value of G_m . The gain values for HG-DGJLT, SiO₂-only and HfO₂-only DGJLT are 50.1 dB, 51.8 dB, 39.5 dB at $V_{GS}=0.2$ V; and 35.5 dB, 31.5 dB and 27.2 dB at $V_{GS}=1$ V respectively. Fig 4.11 (a) presents the gate capacitance ($C_{GG}=C_{GS}+C_{GD}$) for the devices at $V_{DS}=1$ V. As expected, HG-DGJLT has lowest C_{GG} followed by SiO₂-only and HfO₂-only DGJLT. For a HfO₂-only DGJLT, gate-to-channel coupling strength is stronger compared with SiO₂-only DGJLT, resulting very high electric field at the drain side and eventually very high band-to-band tunnelling current occurs for the former. In the DG-DGJLT, however, the strong gate-to-channel coupling strength is observed at the source side because of the use of high-k dielectric and the weak gate-to-channel coupling strength is observed at the drain side because of the use of low-k gate dielectric [51]. Therefore, the gate capacitance is lowest for DG-DGJLT followed by SiO₂-only only HfO₂-only DGJLT. Unity gain cut-off frequency ($f_T = G_m/2\pi \times C_{GG}$), another figure-of-merit useful for analog applications is also plotted in Fig. 4.11 (b) with respect to V_{GS} at $V_{DS}=1$ V. At lower V_{GS} (till 0.4 V), f_T is almost same for all the devices due to almost similar values of transconductance. However, HG-DGJLT offers almost double value of f_T compared to other two devices at $V_{GS}=0.8$ V because of lower value of gate capacitance as aforementioned. The simulated I_D - V_{GS} characteristic of the n-DGJLT is calibrated with [46].

4.5 Summary

The immunity of analog and circuit performance parameters of a DGJLT as a function of high-k gate dielectric permittivity were studied and compared with a DGMOS of same dimension. When the k value was increased, the V_T , G_m , $G_m R_O$ and f_T were decreased; and DIBL and C_{GG} were increased, for both DGJLT and DGMOS. However, the effects in V_T , DIBL and $G_m R_O$, with respect to k, were more

prominent for DGMOS compared to DGJLT. The percentage decrease in V_T , increase in DIBL and decrease in $G_m R_O$ for DGJLT, when gate dielectric constant changes from 3.9 to 22 are 7.2%, 13.6% and 21.6% respectively and the corresponding values for DGMOS are 14.8%, 30.4% and 41.1% respectively for gate and drain voltages of 1 V. The degradation is much worse for $k > 22$. In conclusion, DGJLT is more immune to SCEs and gain degradation with respect to high-k gate dielectrics compared to inversion mode counterpart. The gain of CMOS single stage amplifier was decreased and the delay of inverter was increased with respect to k . The decrease in amplifier gain for DGJLT and DGMOS, when k changes from 3.9 to 22 is 60.2% and 4.86% respectively at a gate bias of 1 V. The increase in inverter delay when k changes from 3.9 to 22 are 22.3% for DGJLT and 12.33% for DGMOS respectively. The affect is even higher for $k > 22$. In conclusion, the performance trends obtained for the device and circuit performance were similar to a conventional and a junctionless double-gate transistor. HG-DGJLT offered improved transconductance and unity gain cut-off frequency; and degraded gain compared to SiO_2 -only and HfO_2 -only DGJLTs.

Chapter 5

Impact of High-k Spacers on Device Performance of n and p-channel DGJLT

5.1 Introduction

The fringing field occurring due to high-k gate dielectric material bring in fringing induced barrier lowering, which degrades the device performance in conventional MOSFET and FinFET, whereas it improves the ON-state current of a tunnel FET (TFET) as aforementioned. With high-k spacer, the device performance degradation occurs for a TFET [85]. However, for a DG TFET, low-k spacer and a high-k gate dielectric improves I_{ON} by a factor of 3.8 compared with a high-k spacer and a high-k gate dielectric [97]. Thus it can be concluded that, the impact of using a low-k/high-k dielectric as a gate oxide combined with low-k/high-k spacer dielectric and vice versa are different for different architectures because of difference in operational principle. It will be interesting to see the affects of spacer dielectric on JLT.

It is reported that there is enhanced electrostatic integrity on single gate SOI JLT using high-k spacer dielectric as aforementioned [90]. As the double-gate or multigate transistor is a more promising candidate for the replacement of conventional MOSFETs in sub 20-nm technology node due to their better electrostatic control on the channel region, one would be interested to understand the behaviour of the device in presence of spacers. The impact of spacer width, which is one of the major performance parameter of the device using spacer dielectric, has not been studied for JLT. Moreover, the impact of spacer dielectric on analog performance of a JLT is not reported yet to best of our knowledge. In this chapter, we present the effects of spacer dielectrics and spacer width in the digital and analog device performance parameters of a 20-nm gate length (L) n-type symmetric double-gate junctionless transistor (DGJLT) with the help of extensive device simulations.

Mallik et al. reported that the impact of fringing field on p-channel TFET is converse to that of n-channel counterpart of similar dimension in many respects [98]. Therefore, in this work we investigate whether the device performance of p-DGJLT in presence of fringing field is similar to n-DGJLT of similar dimension or not. We present the effects of fringing field of high-k gate insulator and spacer

dielectrics on the device performance parameters of a short channel p-DGJLT.

The cross-sectional view of a T-FET is shown in Fig. 5.1 along with its band diagram and transfer characteristic. The brief description on operation of a T-FET is presented here. Fig. 5.1(a) shows the schematic cross-section of p-type tunnel FET (TFET). Fig. 5.1(b) shows the schematic energy band profile for the off state (dashed blue lines) and the on state (red lines). In the off state, no empty states are available in the channel for tunnelling from the source, so the off current is very low. With decrease in V_G , the valence band energy (E_V) of the channel moves above the conduction band energy (E_C) of the source so that inter-band tunnelling can occur. This makes the device to be in the on state, in which electrons in the energy window, $\Delta\Phi$ (green shading), can tunnel from the source conduction band into the channel valence band. Electrons in the tail of the Fermi distribution cannot tunnel because no empty states are available in the channel at their energy (dotted black line), so a slope of less than $60 \text{ mV decade}^{-1}$ can be achieved. This is indicated in the schematic transfer characteristics shown in fig 5.1(c). Because the tunnel current depends on the transmission probability through the barrier, as well as on the number of available states determined by the source and channel Fermi functions, the resultant slope is not linear on a logarithmic scale, which it is for a conventional MOSFET. λ , screening tunnelling length; a.u., arbitrary units; E_F , Fermi energy [14]. Thus, tunnel field-effect transistors (TFETs) have extremely low leakage current, exhibit excellent subthreshold swing, and are less susceptible to short-channel effects. However, TFETs do face certain special challenges, particularly with respect to the process-induced variations in the following: 1) the channel length and 2) the thickness of the silicon thin film and gate oxide.

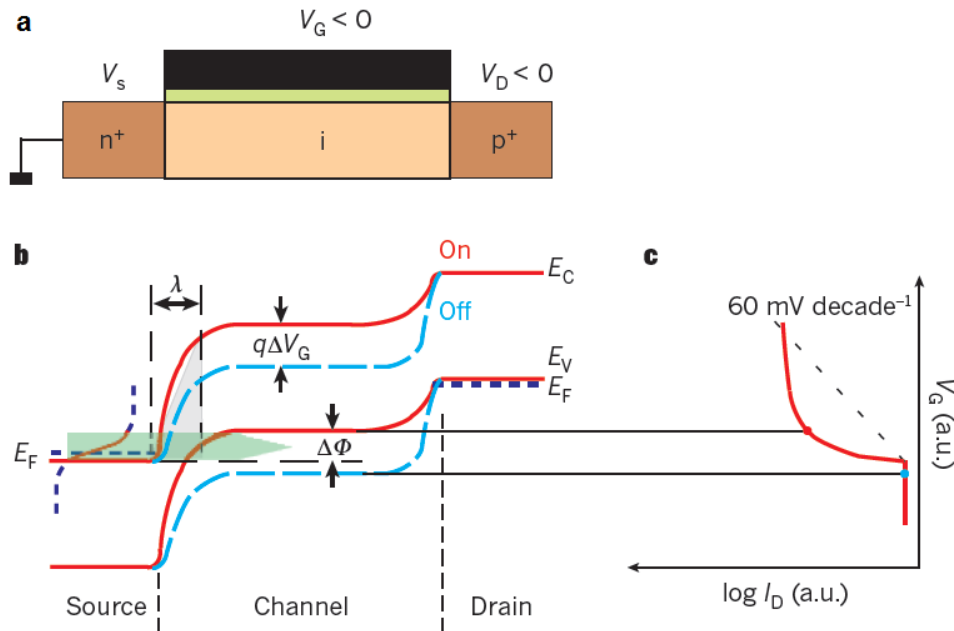


Figure 5.1: a) Cross-sectional view of p-type T-FET b) energy band diagram of a T-FET c) transfer characteristic of the device.

5.2 Impact of High-k Spacers on Device Performance of n-Channel DGJLT

5.2.1 Device Structure and Simulation

The crosssectional view of symmetric double-gate junctionless transistor (DGJLT) with spacer is shown in Fig. 5.2. SiO_2 , Al_2O_3 and HfO_2 are used as gate oxide material having equivalent oxide thickness (EOT) of 1 nm. Threshold voltage (V_T) of the device is fixed at 0.25 V which corresponds to drain current of 10^{-7} A at $V_{DS} = 50$ mV without the spacers for all three gate oxides namely SiO_2 , Al_2O_3 and HfO_2 . The corresponding gate workfunctions at this V_T are 5.356 eV, 5.36 eV and 5.38 eV for SiO_2 , Al_2O_3 and HfO_2 gate oxides respectively. The source-channel-drain region has uniform n-type doping concentration (N_D) of value $1.5 \times 10^{19} \text{ cm}^{-3}$. The spacer dielectric materials used are Air, Al_2O_3 and HfO_2 which have dielectric constants 1, 9.3 and 22 respectively. The silicon thickness (T_{Si}) is taken as 10 nm. The source/drain extensions (L_S/L_D) are taken as 20 nm. The simulations are carried out using two carriers Fermi-Dirac model without impact ionization to account for highly doped channel, band-gap narrowing (BGN) and Schottky–Read–Hall (SRH) recombination models are included in simulations. The mobility model includes both doping and transverse-field dependence.

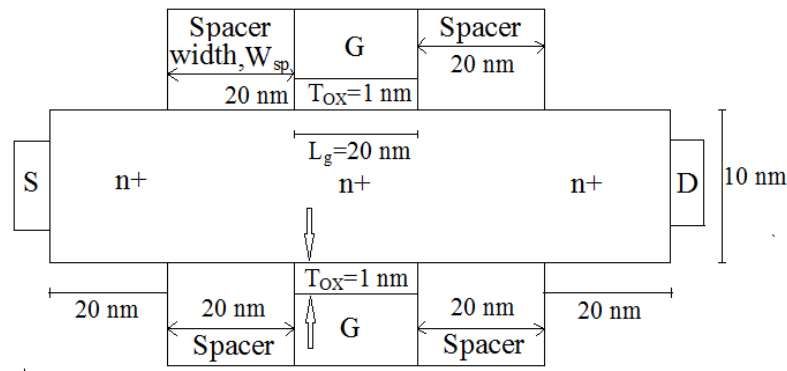


Figure 5.2: Crosssectional view of symmetric double-gate junctionless transistor (DGJLT) with spacer.

5.2.2 Simulation Results and Discussion

Fig. 5.3 shows the I_D - V_{GS} characteristics of the device for different spacer dielectrics taking HfO_2 as gate oxide at drain voltage, $V_{DS} = 1$ V. It is seen that OFF-state current decreases with increase in the spacer dielectric constant and it shows that devices having spacer with highest k_{sp} value can be scaled to lowest channel length. With the reduction of subthreshold current, electrostatic integrity of the device is improved. JLTs have high vertical electric field due to volume inversion in the OFF-state.

JLT exhibits zero electric field in the ON-state due to flat band region. Thus, the ON-state current

should be almost unaffected because of the zero electric field as mentioned previously [40]. The ON-state current is slightly lower for high- k_{sp} spacer at a gate voltage of 1 V because of the increase in threshold voltage with increase in spacer dielectric constant. As can be understood from Fig. 5.2, the threshold voltage increase with increasing spacer dielectric constant is obvious in JLT. This is due to the fact that the enhanced fringing electric fields through the spacer deplete the silicon beyond the gate edges for high- k spacer in the subthreshold region. Also, shown in the inset of Fig. 5.2 is the I_{ON}/I_{OFF} ratio variation with respect to spacer dielectric constant for different gate oxides namely, SiO_2 , Al_2O_3 and HfO_2 . I_{ON} and I_{OFF} are extracted as the current at gate voltages 1 V and 0 V respectively for drain voltage of 1 V. I_{ON}/I_{OFF} ratio increases with increasing spacer dielectric constant value for all gate oxides. The I_{ON}/I_{OFF} ratio is highest for SiO_2 gate oxide followed by Al_2O_3 and HfO_2 . Higher I_{ON}/I_{OFF} signifies better switching capability. Thus, low- k gate dielectric combined with high- k spacer dielectric DGJLT is more suitable to high speed applications compared to other combinations of gate/spacer dielectrics.

Fig. 5.4 presents subthreshold slope (SS) and drain induced barrier lowering (DIBL) variation with respect to spacer dielectric constant for different gate oxides at $V_{DS} = 1$ V. SS represents the OFF-to-ON switching capability of a device and is defined as the gate voltage which could cause one decade change in drain current in the subthreshold region. SS and DIBL decreases with increasing spacer dielectric constant k_{sp} for all three gate oxides for reasons as already explained. SiO_2 gate oxide has the lowest value of SS and DIBL for all spacer dielectrics considered. Fig. 5.4 shows the transconductance to drain current ratio (G_m/I_D) with respect to gate voltage for different spacer dielectrics. G_m/I_D is higher for higher k_{sp} in the subthreshold region. The transconductance and drain

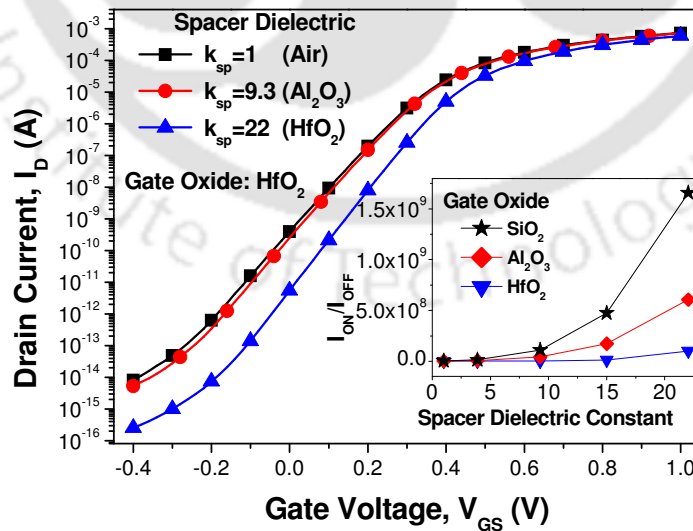


Figure 5.3: I_D - V_{GS} characteristics for different spacer dielectrics with HfO_2 gate dielectric material. In inset of Fig. 2, I_{ON}/I_{OFF} variation with spacer dielectric constant for different gate oxides. Drain voltage, $V_{DS} = 1$ V. $L=20$ nm, $T_{si}=10$ nm, $EOT=1$ nm, $N_D=1.5 \times 10^{19} \text{ cm}^{-3}$.

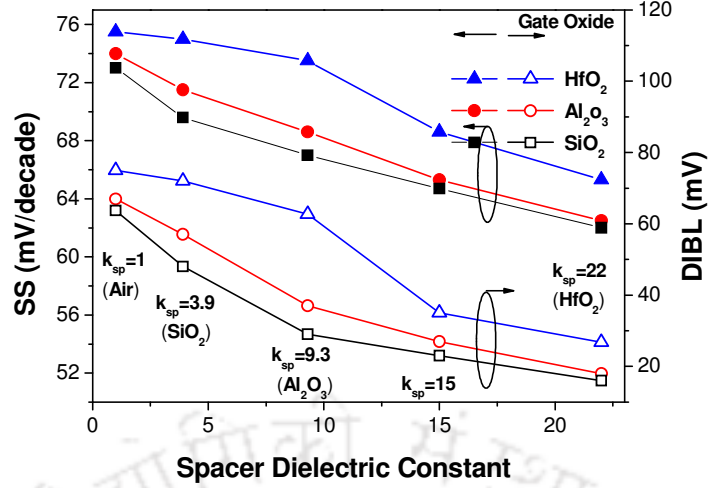


Figure 5.4: SS and DIBL variation with respect to spacer dielectric constant for different gate oxides at $V_{DS} = 1$ V, $L=20$ nm, $T_{si}=10$ nm, $EOT=1$ nm, $N_D=1.5 \times 10^{19} \text{ cm}^{-3}$.

currents for Air, Al_2O_3 and HfO_2 spacer dielectrics are $6.08 \mu\text{S}$, $4.77 \mu\text{S}$, $0.306 \mu\text{S}$ and $0.196 \mu\text{A}$, $0.148 \mu\text{A}$, $7.94 \times 10^{-3} \mu\text{A}$ respectively at a gate voltage of 0.2 V and a drain voltage of 1 V. Though G_m is lower for higher k_{sp} , but because of the lower drain current in the subthreshold region, high-k spacers offer higher G_m/I_D . In the ON-state, G_m/I_D has almost alike value for all spacer dielectrics because of their analogous value of G_m and I_D .

The intrinsic gain ($G_m R_O$) and output conductance ($G_D = \partial I_D / \partial V_{DS}$) as a function of gate voltage are presented in Fig. 5.6 for three spacer dielectrics considered in this study namely, Air, Al_2O_3 and HfO_2 with HfO_2 as gate oxide. The output conductance, G_D of a junctionless transistor is determined not only by mobility but by density of carriers and electric field [33], given by the expression

$$G_D = \mu q \left[N(x) \frac{\partial E(x)}{\partial V_{DS}} + E(x) \frac{\partial N(x)}{\partial V_{DS}} \right] \quad (5.1)$$

Where, μ is the mobility of electron. $N(x)$ is the density of carriers n , integrated in the cross-sectional area S of the device, x being the position perpendicular to the current flow. $E(x)$ is the Electric field. The 2nd term in the parenthesis is much smaller compared to 1st term and neglected. G_D ($= \partial I_D / \partial V_{DS}$) is slightly higher for low-k spacer. For example, the G_D value for Air, Al_2O_3 and HfO_2 spacer dielectrics are $1.44 \text{ m}\Omega$, $1.41 \text{ m}\Omega$, $1.19 \text{ m}\Omega$ respectively at a gate voltage of 0.2 V and $0.123 \text{ m}\Omega$, $0.109 \text{ m}\Omega$, $0.049 \text{ m}\Omega$ at a gate voltage of 1 V and a drain voltage of 1 V. The transconductance is lower for high-k spacer compared to low-k spacer in the subthreshold region as mentioned above. However, the early voltage and hence output resistance ($R_O = 1/G_D$) is better for high-k spacer due to lesser short-channel effects. Subsequently, a higher $G_m R_O$ is obtained for higher k_{sp} in the subthreshold region as indicated in Fig. 5.6. At gate voltage of 1 V, $G_m R_O$ is almost independent of k_{sp} , because for

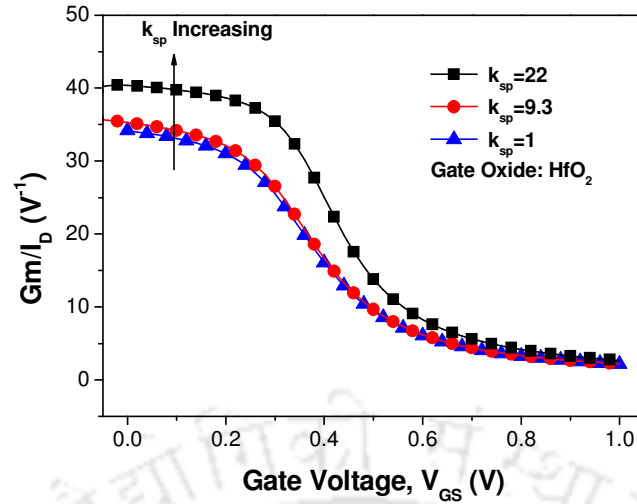


Figure 5.5: Transconductance to drain current ratio (G_m/I_D) with respect to gate voltage for different spacer dielectric material with HfO_2 gate oxide at $V_{DS} = 1$ V. $L=20$ nm, $T_{si}=10$ nm, $EOT= 1$ nm, $N_D=1.5 \times 10^{19} \text{ cm}^{-3}$.

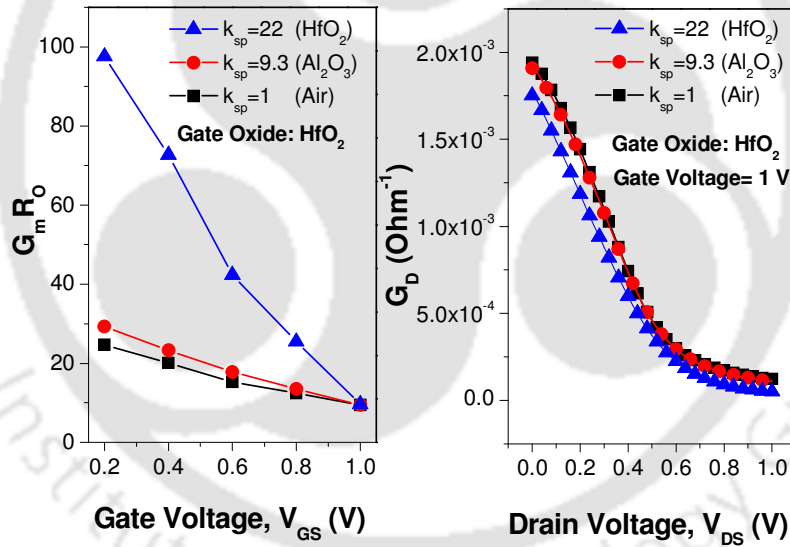


Figure 5.6: Intrinsic gain ($G_m R_O$) and output conductance (G_D) with respect to gate voltage for different spacer dielectrics with HfO_2 as gate oxide at $V_{DS} = 1$ V. $L=20$ nm, $T_{si}=10$ nm, $EOT= 1$ nm, $N_D=1.5 \times 10^{19} \text{ cm}^{-3}$.

all spacers considered, G_m and R_O values are more or less similar.

All the capacitances are extracted from the small-signal ac device simulations at a frequency of 1 MHz and drain voltage, $V_{DS} = 1$ V. The gate-to-bulk (C_{GB}) capacitance value for the device is much lesser than C_{GS} and C_{GD} and not considered. Fig. 5.7 shows the unity gain cut-off frequency (f_T) with respect to gate voltage for different spacer dielectrics. f_T is defined as the frequency when current gain becomes unity and expressed as $f_T = G_m / \{2\pi(C_{GS} + C_{GD})\}$, Where, C_{GS} and C_{GD} are gate to source

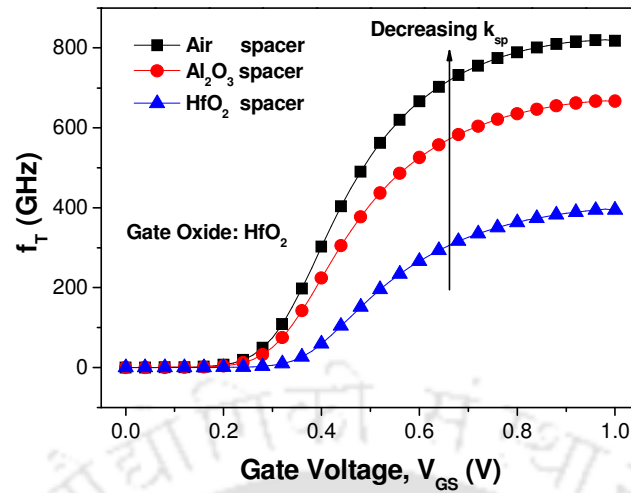


Figure 5.7: Unity gain frequency (f_T) with respect to gate voltage for different spacer dielectric material with HfO_2 gate oxide at $V_{DS} = 1$ V. $L=20$ nm, $T_{si}=10$ nm, $EOT= 1$ nm, $N_D= 1.5 \times 10^{19} \text{ cm}^{-3}$.

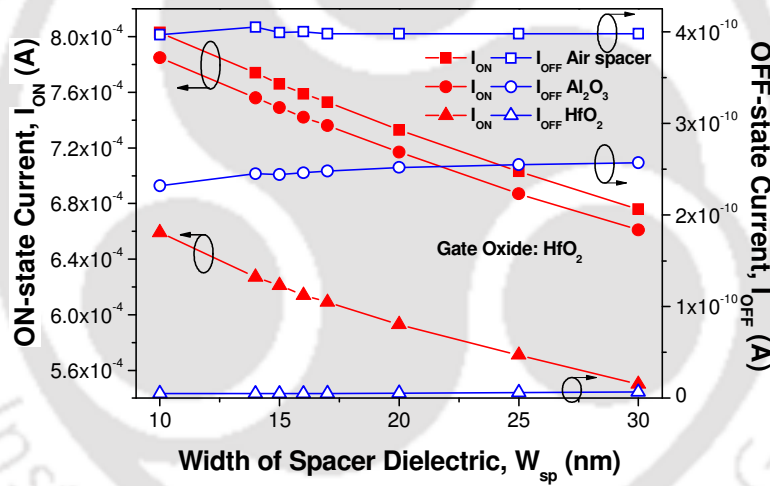


Figure 5.8: ON-state, OFF-state current variation with respect to spacer width at $V_{DS}=1$ V. HfO_2 is taken as gate oxide. $L=20$ nm, $T_{si}=10$ nm, $EOT= 1$ nm, $N_D= 1.5 \times 10^{19} \text{ cm}^{-3}$.

and drain capacitances respectively. f_T increases with decreasing k_{sp} . G_m is almost alike for all spacers considered at $V_{DS}=1$ V due to almost same ON-current. The higher value of f_T at ON-state for low- k spacer is due to lower gate capacitance ($C_{GS}+C_{GD}$) because of lower fringing field lines. For example, the gate capacitance for Air, Al_2O_3 and HfO_2 spacer dielectrics are 0.3 fF, 0.37 fF, 0.63 fF respectively at a gate and a drain voltage of 1 V. Fig. 5.8 shows the ON-state and OFF-state current variation with respect to spacer width, W_{sp} for HfO_2 as gate oxide material. With increasing W_{sp} , the coupling between gate metal and source through the spacer increases, resulting in device performance degradation similar to tunnel FET devices [86]. With positive voltage on the gate metal, the energy band is lowered in the channel region with increasing W_{sp} .

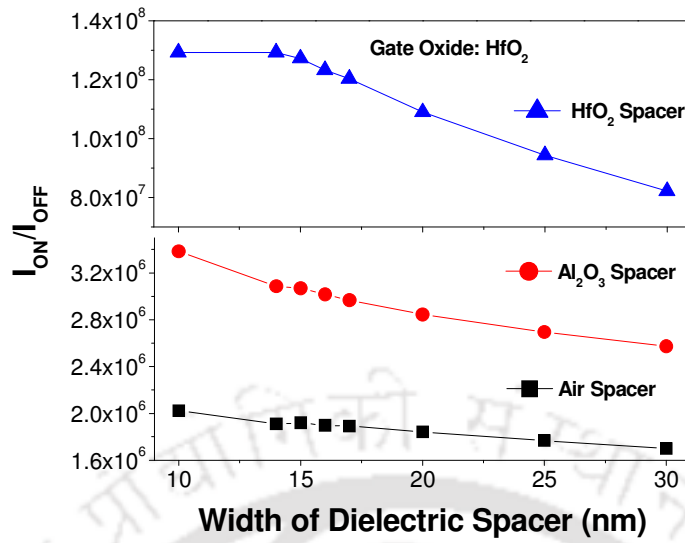


Figure 5.9: I_{ON}/I_{OFF} ratio variation with respect to spacer width at $V_{DS} = 1$ V. HfO_2 is taken as gate oxide. $L=20$ nm, $T_{Si}=10$ nm, $EOT=1$ nm, $N_D=1.5 \times 10^{19} \text{ cm}^{-3}$.

Therefore, there is a decrease in potential in the channel region with increase in spacer width. Hence, ON-state current decreases slightly with increase in spacer width. The OFF-state current marginally increases with respect to W_{sp} till a certain value, after which dependence becomes very weak. I_{ON} is highest in Air spacer and I_{OFF} is lowest in HfO_2 spacer dielectric material. The variation of I_{ON}/I_{OFF} ratio with respect to W_{sp} is shown in Fig. 5.9. Device with HfO_2 spacer has higher I_{ON}/I_{OFF} ratio followed by Al_2O_3 and Air spacer. For HfO_2 spacer, I_{ON}/I_{OFF} ratio is maximum till $W_{sp} \sim 15$ nm, after which it decreases with respect to W_{sp} . However, for Al_2O_3 and Air, I_{ON}/I_{OFF} ratio decreases with increasing W_{sp} . Therefore, while designing the device, proper dimension has to be taken for optimum performance.

5.3 Impact of Fringing Fields in a p-Channel DGJLT

5.3.1 Device Structure and Simulation Setup

The device structure of a p-channel symmetric double-gate junctionless transistor with spacer dielectrics is shown in Fig. 5.10. The working physics of n or p-channel DGJLT are same except for the polarities and are explained in section 2.1.2. A channel doping concentration (N_A) of $1 \times 10^{19} \text{ cm}^{-3}$ is considered. For simulations without spacers, a gate work-function (WF) of 4.22 eV is used. To study the impact of spacers on p-channel DGJLT (sections III.B), three different gate oxides namely, SiO_2 ($k=3.9$), Al_2O_3 ($k=9.3$) and HfO_2 ($k=22$) are considered. For a JLT, V_T can be fixed considering suitable values of metal WF and N_A for a specific set of device dimension parameters like channel

length (L), channel thickness (T_{si}), source/drain extension etc. Here, gate work-function of the device are tuned to obtain the same threshold voltage ($= -0.34$ V) at a drain voltage of -50 mV for all the three gate oxides with vacuum as spacers. The corresponding gate work-functions at this V_T are 4.220 V, 4.221 eV and 4.208 eV for SiO_2 , Al_2O_3 and HfO_2 gate oxides respectively. The equivalent oxide thickness of the gate oxide is considered to be 1 nm for all simulations. A channel thickness (T_{si}) of 10 nm and source/drain extensions of 10 nm is kept for all simulations. The simulations are carried out using with Fermi-Dirac model without impact ionization, doping concentration-dependent carrier mobility, electric field-dependent carrier model, band gap narrowing model, Shockley-Read-Hall (SRH) recombination/ generation to account for leakage currents and density gradient model to account for quantum mechanical effects.

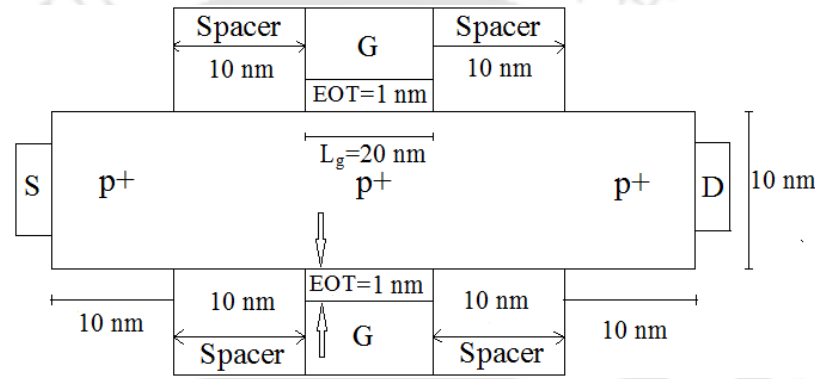


Figure 5.10: Cross-sectional view of a p-channel symmetric double-gate junctionless transistor (p-DGJLT).

5.3.2 Simulation results and discussion

(a) Effects of fringing field on I_D , V_T , SS and DIBL: Impact of k at constant EOT (without spacers)

The impact of fringing field (without spacers) on drain current of p-DGJLT is studied in Fig. 5.11 at a drain voltage V_{DS} of -1 V for different gate dielectric constant (k) of 3.9 , 9.3 , 22 , 50 and 100 for same EOT of 1 nm. Though dielectric constant value of 50 and 100 look higher for a gate oxide material, at present we are interested in the theoretical aspects of what fringing field will do to the characteristics of the device. It is well known that Si-SiO₂ substrate-gate oxide material form a very good interface. High- k gate oxide forms a poor interface and low barrier, producing high leakage current. Therefore, normally a stack of SiO₂/high- k material is used, lowering the effective k value. In this work, we are more interested in the intrinsic effect of fringing fields on the device characteristics at the same EOT. The ON-state and OFF-state currents are extracted at $V_{GS}-V_T$, where $V_{GS} = -1$ V and 0 V for ON and OFF-state currents respectively. The ON-state current decreases very marginally;

however, OFF-state current increases with an increase in k similar to an n-channel DGJLT. For example, when k changes from 3.9 to 100, the OFF-state currents obtained are 8.5×10^{-16} A and 9×10^{-14} A respectively. The increase of the OFF-state current with respect to an increase in gate oxide dielectric constant is explained below. A junctionless transistor has higher threshold voltage when the channel region is fully depleted. With the additional increased fringing fields for high- k gate dielectri-

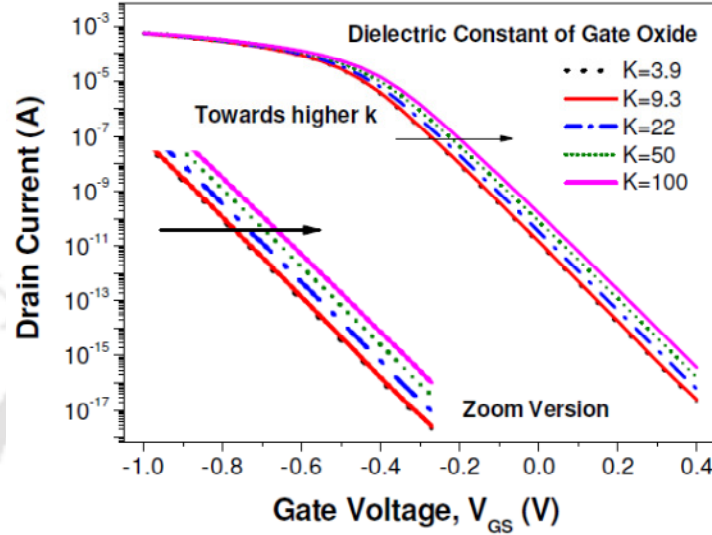


Figure 5.11: Drain current with respect to gate voltage for different gate insulator materials (without spacers) at $V_{DS} = -1$ V. $EOT = 1$ nm, $L = 20$ nm, $WF = 4.22$ eV, $N_A = 1 \times 10^{19} \text{ cm}^{-3}$ and $T_{Si} = 10$ nm.

cs, the channel region is no longer fully depleted and hence threshold voltage decreases. Also, with increase in k value, drain induced barrier lowering (DIBL) increases (Fig. 5.12 (a)) and hence threshold voltage decreases (Fig. 5.12 (b)) and OFF-state current increases (Fig. 5.12 (d)). Because of high electric field near the drain side, the subthreshold performance degrades for a high- k gate dielectric material. In the ON-state, the vertical electric field of JLT is already lower and the fringing lines due to higher k value of gate oxide do not make much effect the ON-state current (Fig. 5.12 (c)) as aforementioned. The n or p-type DGJLT device performances are compared for same device dimension and same value of gate biasing (signs reversed). Also, threshold voltage of the n/p-type DGJLT are kept same at $V_{DS} = -50$ mV for gate oxide with lowest dielectric constant considered here i.e., SiO_2 . The decrease of threshold voltage with increase in k is similar to n-DGJLT for reasons mentioned above. This is because increase in k means number of electric lines are contributing to the depletion region, which decreases the V_T . Since the gate has more capacitive coupling for higher k values, the SS performance is degraded as shown in figure 5.12 (e). This is similar to the behaviour of an n-channel DGJLT [99].

It was reported that for a p-channel TFET, the V_T and ON-state current degrades till $k = 100$, after which it improves [98]. Also, for n-channel TFET, device performance is improved with increase in dielectric constant except when k is relatively low [85]. Again, it was stated that the device behaviour

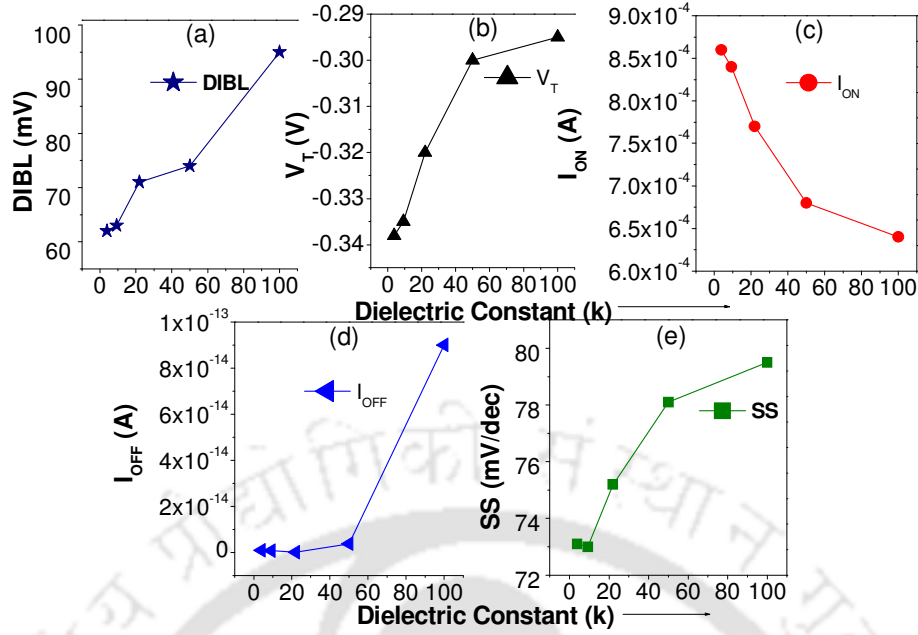


Figure 5.12: (a) DIBL, (b) threshold voltage (V_T) (at $V_{DS} = -50$ mV), (c) ON-state current (I_{ON}) and (d) OFF-state current (I_{OFF}) at $V_{GS} - V_T$ and (e) subthreshold slope (SS) with respect to gate dielectric constant k without spacers. EOT = 1 nm, $L = 20$ nm, $WF = 4.22$ eV, $N_A = 1 \times 10^{19} \text{ cm}^{-3}$ and $T_{si} = 10$ nm.

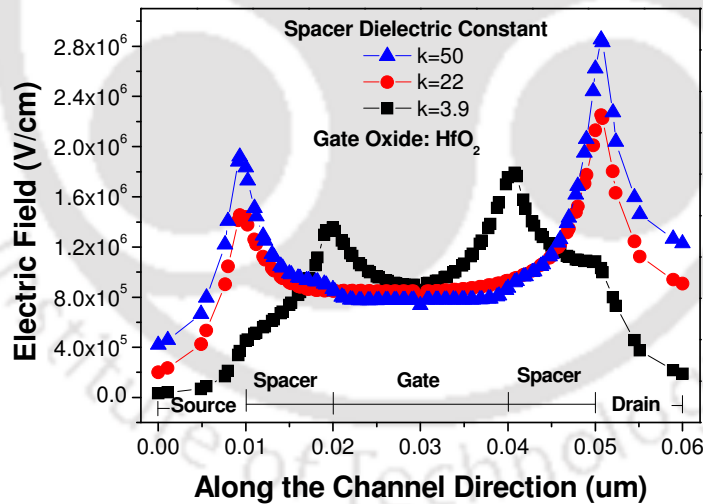


Figure 5.13: Electric field along the lateral direction of channel near the silicon-oxide interface at $V_{DS} = -1$ V. Gate oxide is HfO_2 . Spacer dielectric constant $k = 3.9, 22, 50$. $L = 20$ nm, EOT = 1 nm, $WF = 4.208$ eV, $N_A = 1 \times 10^{19} \text{ cm}^{-3}$ and $T_{si} = 10$ nm.

of a p-channel TFET in presence of fringing fields is contrast to n-channel counterpart [98]. However, for a DGJLT the device performances trends are similar for n and p-channel counterpart with increase in k . Thus it can be concluded that impact of fringing field is different for different device

architectures and channel doping profile.

(b) Impact of Spacer Materials

Dielectric spacers are placed on both sides of the gate oxide as shown in Fig. 5.10. Three different gate oxides namely, SiO_2 , Al_2O_3 and HfO_2 are studied as spacer materials. The spacer width is taken as 10 nm. The effect of spacer materials on electric field are shown in Fig. 5.13 with HfO_2 as gate oxide. The electric field is higher for higher k values of the spacer. Near the drain, electric field is lower for lower k spacers; which indicates that short channel effects (SCEs) like DIBL and hot carrier effect is reduced for low k values. In other words, for a particular gate oxide, using low- k spacer materials electric fields can be confined within the channel thereby minimizing the short channel performance degradation. With an increase in spacer dielectric constant, the carrier transport efficiency increases leading to higher transconductance. The transfer characteristics for different spacer dielectrics are shown in Fig. 5.14 for a case in which HfO_2 is used as gate oxide.

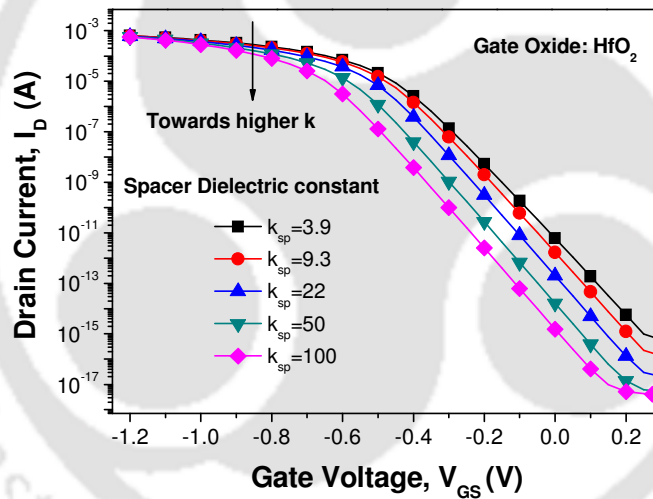


Figure 5.14: Drain current (at $V_{DS} = -1$ V) with respect to gate voltage for different spacer dielectric constants. $EOT = 1$ nm, $L = 20$ nm, $WF = 4.208$ eV, $N_A = 1 \times 10^{19} \text{ cm}^{-3}$ and $T_{si} = 10$ nm.

Fig. 5.15 shows the variation of I_{ON} and threshold voltage with respect to spacer dielectric constant for three different gate oxides namely, SiO_2 , Al_2O_3 and HfO_2 having EOT of 1 nm. ON-state current decreases with increase in spacer dielectric constant value for all the gate oxide materials considered. The I_{ON} is highest for HfO_2 gate oxide followed by Al_2O_3 and SiO_2 . Thus, high- k gate dielectrics combined with low- k spacer dielectrics DGJLT has higher I_{ON} . Threshold voltage increases with increase in spacer dielectric constant for all three gate oxides considered. In the OFF-state, with the introduction of the spacers, the depletion region extends on both sides of the channel region (i.e., below the spacer region) because of the higher fringing fields. This enhanced depletion causes higher barrier at source-channel interface and hence threshold voltage increases. Thus, effective gate length

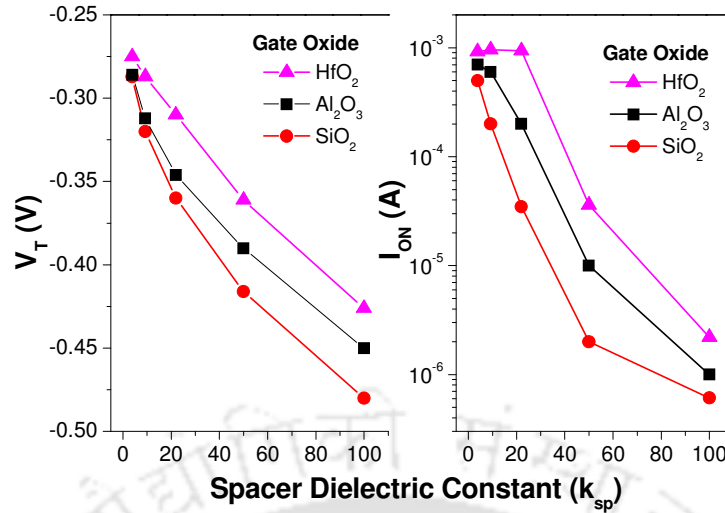


Figure 5.15: Threshold voltage (V_T) (at $V_{DS} = -1$ V) and I_{ON} variation with respect to spacer dielectric constant k for different gate oxide. $EOT = 1$ nm, $L = 20$ nm, $N_A = 1 \times 10^{19} \text{ cm}^{-3}$ and $T_{si} = 10$ nm.

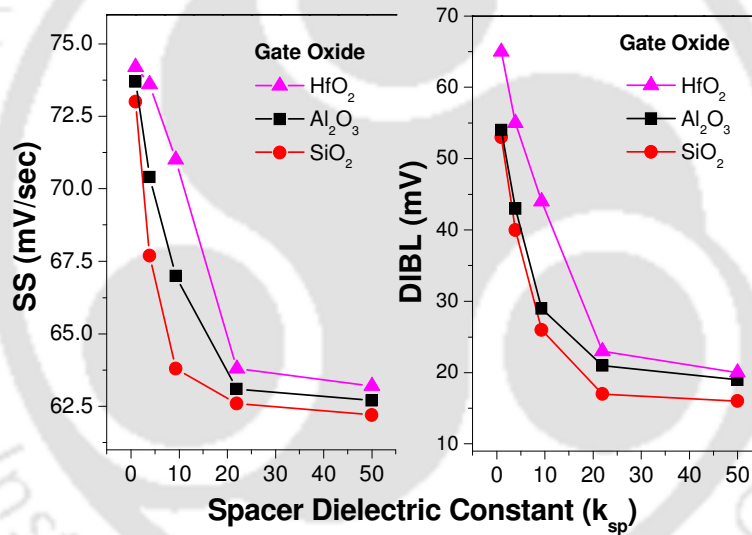


Figure 5.16: SS and DIBL variation with respect to spacer dielectric constant for different gate oxide. $EOT = 1$ nm, $L = 20$ nm, $N_A = 1 \times 10^{19} \text{ cm}^{-3}$ and $T_{si} = 10$ nm.

actually increases than physical gate length and hence OFF-state current decreases. Fig. 5.16 presents subthreshold slope (SS) and drain induced barrier lowering (DIBL) variation with respect to spacer dielectric constant for gate oxides SiO_2 , Al_2O_3 and HfO_2 . As aforementioned, SS is extracted as the gate voltage which could bring one decade change in drain current in the subthreshold region. DIBL is extracted as the threshold voltage change when drain voltage shifts from -50 mV to -1 V. SS and DIBL decreases with increasing spacer dielectric constant for all three gate oxides for reasons explained above. SiO_2 gate oxide has the lowest value of SS and DIBL for all spacer dielectric constant values considered. As there is no p-DGJLT reported yet, the n-channel counterpart of simulated I_D - V_{GS} results are calibrated with [46] in our previous report [99].

5.4 Summary

The OFF-state current decreases by more than one order of magnitude using high-k spacer and ON-state current (at $V_{DS} = 1$ V) is very marginally higher for low-k spacer in a double-gate JLT for all gate dielectrics considered, unlike tunnel FET and conventional MOSFET. I_{ON}/I_{OFF} ratio has increased with increasing spacer dielectric constant and was highest for SiO_2 among the three gate oxides considered. SiO_2 gate oxide has lower value of SS and DIBL for all spacer dielectrics compared to Al_2O_3 and HfO_2 gate oxides. It is concluded that, as far as subthreshold characteristics are concerned, low-k gate oxide combined with high-k spacer dielectric material offers the best performance. Intrinsic gain and transconductance to drain current ratio increases with increase in spacer dielectric constant; however, output conductance and unity gain cut-off frequency decreases with spacer dielectric constant. The effect of spacer width on device performance has also been studied. I_{ON} decreases slightly with increasing spacer width. I_{OFF} is insignificantly affected by W_{sp} . I_{ON}/I_{OFF} ratio is almost constant till a W_{sp} of ~ 15 nm and decreases slightly with further increase in W_{sp} .

I_{ON} , SS and DIBL are degraded with increasing fringing fields at constant EOT for a p-DGJLT, like its n-channel counterpart [30]. This is in contrast with TFET, where I_{ON} increases with increasing k value of gate oxide [25]. V_T of p-DGJLT decreases with increase in k similar to n-DGJLT. With inclusion of spacer dielectrics on both sides of the gate oxides, SS and DIBL are improved; however, V_T and I_{ON} are degraded similar to n-channel counterpart of same dimension [30]. ON-state current variation with k_{sp} is marginal for DGJLT contrast to TFET [26]. Thus, it is concluded that n and p-channel DGJLT show similar performance trends in presence of high-k gate dielectrics and spacer dielectrics unlike a TFET.

Chapter 6

Enhancing the Transconductance and other Device Performances of a DGJLT

6.1 Introduction

To realize high performance circuits, high transconductance and small drain conductance and high transition frequency transistors are essential. MOSFET has been the basic building block of high performance, high-speed, and high-density integrated circuits, in both analog and digital domain for last few decades. Excellent high-speed characteristics have been achieved through improved design, the use of higher mobility substrate material, and most importantly, gate length scaling. The high channel doping concentration in a JLT, reduces its carrier mobility, which lower its drive current and hence transconductance. Short-channel effects and gate transport efficiency are two important issues need to be addressed to improve the JLT performance. Gate transport efficiency is associated to the average transport velocity of electrons traveling through the channel, which is related to the electric field distribution along the channel. In a FET, electrons enter into the channel with a low initial velocity; gradually accelerating toward the drain and electron drift velocity is maximum near the drain. That is the electrons move faster in the region near the drain but relatively slower in the region near the source. Hence, the speed of the device is affected by a relatively slow electron drift velocity in the channel near the source region. To increase the transport efficiency and hence transconductance, gate material with different workfunctions are used (with higher workfunction towards the source). The major challenge now is to find different metals with suitable workfunctions and a way to integrate them into the CMOS process. The inherent fringing capacitance between the two gates is significantly high as the separation of the two gates becomes closer to the channel depths. Some integration schemes suggested to integrate metal gates into CMOS flow are fully-silicided metal gates (FuSi) [100–102], two different band edge metal gates [103], metal wet etch process [104], metal interdiffusion process [105], and single metal gate with selectively tuned workfunction by patterning and implanting a workfunction modifying species into one of the electrodes [106–108]. However, each technology has its own advantages and disadvantages and is best suited for specific

applications, depending on the requirements for the workfunction of the metal gates.

Dual-material gate (DMG) devices offer improved carrier transport efficiency, transconductance and the drain output resistance compared to single-material gate conventional MOSFETs [109-116]. By adjusting the metal work functions, channel potential and electric field distributions along the channel can be controlled. Razavi et al. have reported that a dual material gate-oxide stack, double-gate conventional MOSFET reduces the impact of hot carrier effect and threshold voltage roll-off [109]. Long et al. have experimentally shown that DMG MOSFET offers simultaneous improvement of SCE as well as transconductance [110]. Kasturi et al. have reported that dual material gate silicon on Nothing (SON) MOSFET gives higher early voltage and reduced drain conductance thereby improving analog performance of the device [111-112]. Ghosh et al. have shown by analytical modelling that dual metal gate stack surrounding gate MOSFET shows superior performance than conventional MOSFET [113]. As the operation principle of junctionless transistor is different from conventional MOSFET, it is interesting to see the performance of dual-material gate devices compared to single-material JLT. Of late, Lou et al., have reported that for a junctionless transistor, analog performance can be improved by incorporating a dual-material gate instead of single-material gate [115]. Combining the advantages of junctionless transistor, dual-material gate and high-k spacer dielectrics, we propose DMG-SP DGJLT. We have studied the analog circuit performance parameters viz. drain current (I_D), transconductance (G_m), transconductance to drain current ratio (G_m/I_D), early voltage (V_{EA}), intrinsic gain ($G_m R_O$), and unity gain cut-off frequency (f_T) of a 40-nm gate length (L), n-type symmetric DMG-SP DGJLT with the help of extensive device simulations. An electrostatic potential model is derived to validate our demonstration.

The leakage current due to gate tunneling in very thin oxides changes by almost one decade for every single atomic layer deviation due to processing variations as well which is in fact technology dependant. Also, thin SiO_2 films are prone to damage due to mechanical stress which results in additional gate leakage. To prevent direct gate tunneling in very thin oxides, replacement of SiO_2 gate dielectric by alternative materials with higher permittivity is used now days as mentioned. However, introduction of these high-k dielectrics comes with its own set of problems such as – its interfacing with silicon layer and enlarged fringing field affects on channel region. A thin passivating layer of SiO_2 between bulk and high-k dielectric, so as to form a gate-dielectric stack, is a healthy approach to balance between the advantages and limitations of high-k/Si system. However, there are issues related to integration of the two oxides along with stability and reliability issues. The performance and stability of a transistor can be improved using double-stacked active layers with proper material as gate oxide [116]. Combining the advantages of dual material gate along with double-layer gate stack, we also propose a junctionless architecture called DM-DGS DGJLT. We have studied the analog circuit performance parameters for the device.

As the channel length of MOSFETs are approaching sub-20 nm era, a series of channel mobility

improvement techniques called “technology boosters” have been introduced by industry. Some of them are— use of strain silicon, introduction of alternate channel material like Germanium, group III-V compounds etc. The junctionless transistor architecture is particularly well suited to germanium because a large part of the current transport is in the bulk of the semiconductor, thereby reducing the impact of imperfect semiconductor-insulator interfaces on electric characteristics. In germanium, the lower transport mass (m^*) of electron and hole is responsible for higher electron and hole mobilities. Junctionless transistor was fabricated on bulk [117] as well as on silicon-on-insulator [118-119] substrate using germanium as substrate material. Development of a high-quality gate dielectric on germanium was challenging [120-121]. Also, smaller direct band gap gives rise to high tunneling leakage [122-123]. Inversion-mode (germanium-substrate) MOSFETs exhibit high sensitivity to the quality of the gate dielectric material. There is a rapid degradation in mobility with decreasing equivalent oxide thickness (EOT) in Ge MOSFETs even if a high-k dielectric is used [124]. However, because of bulk conduction mechanism and reduced vertical electric field, JLT is expected to be less sensitive to the interface imperfections [40]. Ideally, MOSFETs fabricated on Germanium-on-insulator (GeOI) substrate have no leakage current flowing to the substrate; however, fabrication of ultra-thin Ge layers is challenging. Here, germanium is also studied as a substrate material in junctionless transistors for improved mobility and device performances for a bulk planar junctionless transistor (BPJLT) and compared the results with the device with silicon as substrate material.

6.2 A Dual-Material Gate Junctionless Transistor with High-k Spacer for Enhanced Analog Performance

6.2.1 Device Structure and Simulation Set up

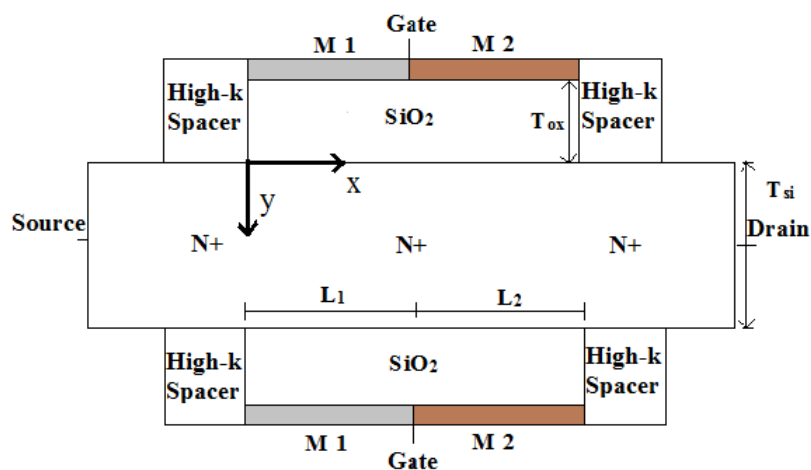


Figure 6.1: Crosssectional view of an n-type dual-material gate junctionless symmetric double-gate transistor with high-k spacer (DMG-SP DGJLT).

The device structure for an n-type symmetric DMG-SP DGJLT is shown in Fig. 6.1. A dual-material

gate (DMG) DGJLT has two metal gates, M1 and M2, with different work functions, denoted by W_{M1} and W_{M2} respectively. The first lateral gate is called control gate and the second one, the screening gate. Metal, M1 has higher workfunction than M2, such that threshold voltage of M1, $V_{T(M1)}$ is greater than $V_{T(M2)}$. Long et al. reported that threshold voltage (V_T) and workfunction of the two gate materials are governed by the relation [110]

$$\Delta V_T = S \Delta W \quad (6.1)$$

$S = 1$ for silicon MOSFET. We define L_{M1} and L_{M2} as channel lengths for metal M1 and M2 respectively; and $L = L_{M1} + L_{M2}$ is the total channel length. The gate length ratio of the two metal gates and their workfunction difference affects the device characterises significantly [110-112]. Recently, Lou et al. have reported that in a DMG JLT, out of different combinations of L_{M1} and L_{M2} ; $L_{M1}/L = 1/2$ and work function difference, $\delta W = 0.5$ give the overall best characteristics of the device [115].

Table 6.1: Process/Device Parameters for simulation of SMG/DMG/DMG-SP

Parameter	SMG	DMG	DMG-SP
L (nm)	40	40	40
$L_{M1}:L_{M2}$ (nm)	—	20:20	20:20
$W_{M1}:W_{M2}$ (eV)	5.2 : 5.2	5.2 : 4.7	5.2 : 4.7
N_D (cm ⁻³)	1.12e19	0.93e19	1.18e19
T_{ox} (nm) (EOT)	1 (SiO ₂)	1 (SiO ₂)	1 (SiO ₂)
W_{sp} (nm) (HfO ₂)	—	—	10
T_{si} (nm)	10	10	10

For DMG and DMG-SP devices, W_{M1} and W_{M2} are set to be 5.2 eV and 4.7 eV respectively, which correspond to acceptable threshold voltage for the devices [Au (Gold)/Pd (Palladium)/Pt (Platinum)/Ir (Iridium) etc. may be used for M1 and Ag (Silver)/Sb (Antimony)/Ti (Thallium)/Rh (Rhodium) etc may be used for M2. There is good co-integration of Ag-Au, Ag-Pt etc]. We have kept $L_{M1}:L_{M2} = 20$ nm: 20 nm for DMG-SP and DMG DGJLT. The devices are optimized by adjusting channel doping concentration (N_D) values so as to have threshold voltage (V_T) of 0.25 V corresponding to drain current of 10^{-7} A at drain voltage of 50 mV. The source and drain extensions (L_S and L_D) are taken as 30 nm. HfO₂ (dielectric constant = 22) is used as a spacer dielectric material for DMG-SP DGJLT. Thinner spacer width is taken for aforementioned reasons. The process and device parameters used for simulations in this work are summarized in Table 6.1. The simulations were carried out using two carriers, the Fermi-Dirac model without impact ionization, doping concentration-dependent carrier mobility and electric field-dependent carrier model. Band gap narrowing model was included. Shockley-Read-Hall (SRH) recombination / generation were included in the simulation to account for

leakage currents. The density gradient model was utilized to account for quantum mechanical effects.

6.2.2 Simulation Results and Discussion

Fig. 6.2 shows the potential and electrical field distributions along the channel direction at drain voltage (V_{DS}) = 1 V and gate voltage (V_{GS}) of 1 V. The potential distributions of DMG and DMG-SP DGJLT have abrupt change on the workfunction transition point from W_{M1} to W_{M2} , whereas SMG DGJLT follows a monotonous trend from source to drain. This enhances the electric field of DMG and DMG-SP with two peaks, but for SMG DGJLT, there is only one peak near the drain. DMG DGJLT has much lower electric field peak near the drain side compared to SMG DGJLT indicating that it suppresses SCE and hot carrier effect more effectively. SCE suppression is even relatively better for DMG-SP DGJLT. The electric field peak of DMG-SP DGJLT shifts towards the drain side because of more fringing lines. The electron velocity in the channel can be controlled by first peak with proper workfunctions of the metal gates [111].

Fig. 6.3 shows the drain current for the devices at a drain voltage (V_{DS}) of 50 mV in both linear (right) and log (left) scale. High-k spacer enhances the fringing electric fields through the spacer and depletes the silicon beyond the gate edges in the OFF-state, which improves subthreshold characteristics as aforementioned [90]. Thus, DMG-SP has marginally better subthreshold slope (SS) compared to DMG DGJLT. However, SMG devices have slightly lower SS than DMG devices [111-112]. JLT exhibits zero vertical electric field in the ON-state due to flat band region and is marginally affected by spacers having different dielectric constant value (not shown) [115].

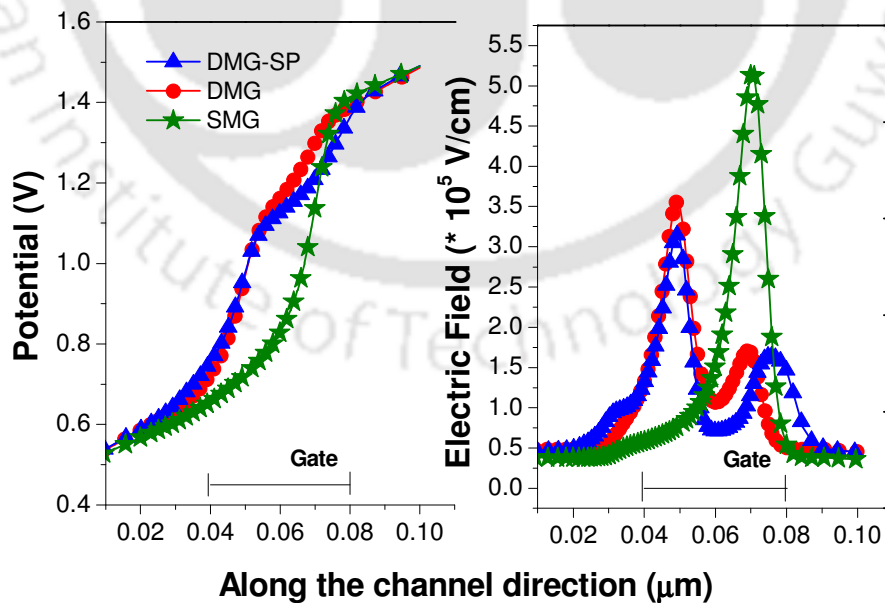


Figure 6.2: Potential and electric field distribution of SMG, DMG and DMG-SP DGJLT along the channel direction at $V_{DS} = 1$ V for $L = 40$ nm, silicon thickness (T_{si}) = 10 nm, gate equivalent oxide thickness (EOT), $T_{ox} = 1$ nm.

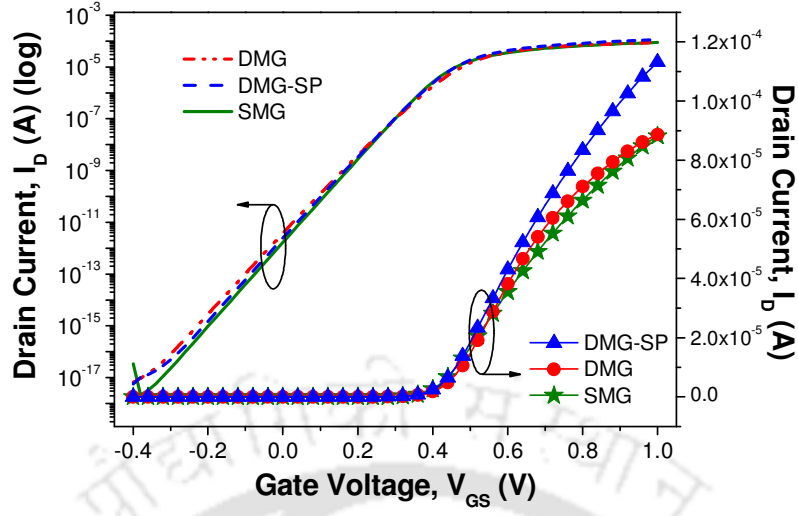


Figure 6.3: Drain current of SMG, DMG and DMG-SP DGJLT with gate voltage at $V_{DS} = 50$ mV for $L = 40$ nm, $T_{si} = 10$ nm, and $T_{ox} = 1$ nm. Both linear (right) and log scale (left) curves are shown.

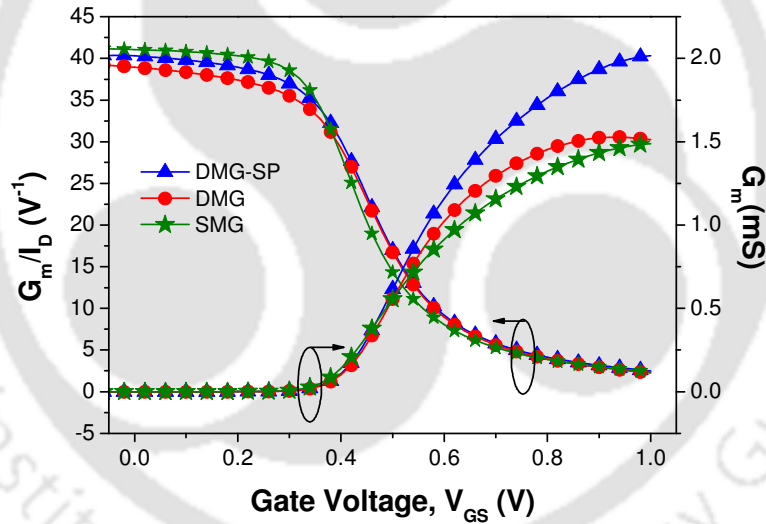


Figure 6.4: Transconductance (G_m) and transconductance to drain current ratio (G_m/I_D) with respect to gate voltage for the devices at $V_{DS} = 1$ V for $L = 40$ nm, $T_{si} = 10$ nm, and $T_{ox} = 1$ nm.

The transconductance, $G_m (= \partial I_D / \partial V_{GS})$ is a figure of merit which indicates how well a device converts a voltage to a current. Below gate voltage of $V_{GS} \sim 0.5$ V, all three devices have almost similar value of G_m . After $V_{GS} = 0.6$ V, DMG-SP has highest G_m followed by DMG and SMG DGJLT as shown in Fig. 6.4. Due to potential uplift at workfunction transition, G_m is increased for DMG devices compared to SMG devices. DMG-SP DGJLT has highest value of G_m at higher gate voltage due to high fringing electric fields and lesser channel resistance in it, compared to other two devices. In JLT, drain current is mainly due to the bulk current; and since its value is smaller, transconductance

is inferior as compared to conventional inversion mode devices (not shown) as mentioned. The values of G_m for DM-DGS, DMG and SMG DGJLT are 2 mS, 1.5 mS and 1.49 mS respectively at $V_{GS}=1$ V. Transconductance to drain current ratio (G_m/I_D) is also plotted with respect to gate voltage, V_{GS} in Fig. 6.4 for a drain voltage, V_{DS} of 1 V. SMG DGJLT has the highest value of G_m/I_D followed by DMG-SP and DMG DGJLT in the subthreshold region. The values of G_m/I_D for SMG, DMG-SP and DMG DGJLT are 40.3 V^{-1} , 38.9 V^{-1} and 37.4 V^{-1} respectively at $V_{GS} = 0.2 \text{ V}$. A slight smaller value of subthreshold current for SMG implies its higher G_m/I_D value in the subthreshold region. G_m/I_D is mainly controlled by body factor of the devices in weak inversion regime; however its value decreases in moderate/strong inversion regime due to the lower mobility at higher doping concentration as

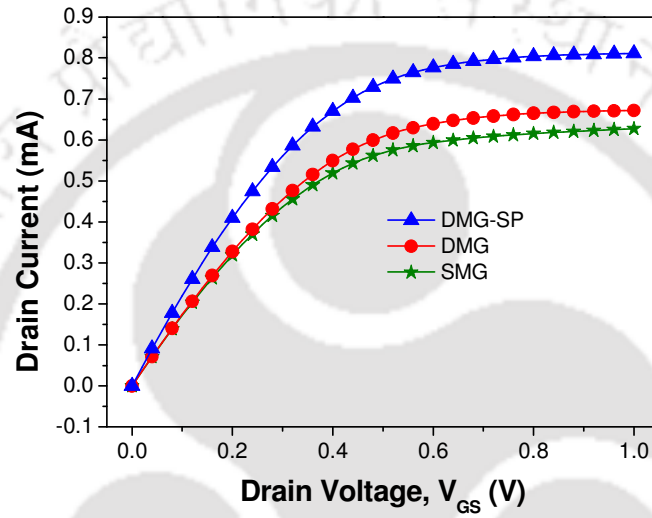


Figure 6.5: Output current with respect to drain voltage at $V_{GS} = 1 \text{ V}$ for $L = 40 \text{ nm}$, $T_{si} = 10 \text{ nm}$, and $T_{ox} = 1 \text{ nm}$.

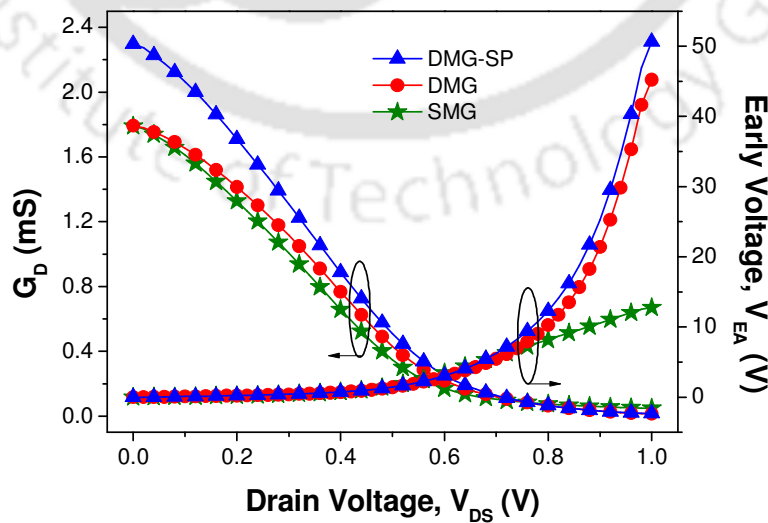


Figure 6.6: Output conductance (G_D) and early voltage (V_{EA}) with respect to drain voltage for the devices at $V_{GS} = 1 \text{ V}$ for $L = 40 \text{ nm}$, $T_{si}=10 \text{ nm}$, and $T_{ox} = 1 \text{ nm}$.

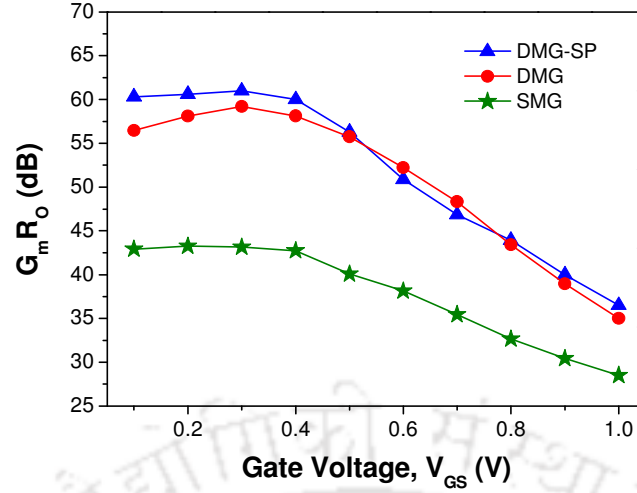


Figure 6.7: Intrinsic gain ($G_m R_o$) with respect to gate voltage for the devices at $V_{DS} = 1$ V for $L = 40$ nm, $T_{si} = 10$ nm, and $T_{ox} = 1$ nm.

mentioned. Fig. 6.5 shows the drain current (I_D) with respect to drain voltage for the devices at $V_{GS} = 1$ V. DMG-SP has higher output current followed by DMG and SMG DGJLT due to high fringing electric fields and lower SCEs. Fig. 6.6 presents the output conductance $G_D (= \partial I_D / \partial V_{DS})$ with respect to V_{DS} at a gate voltage of 1 V. The DMG-SP DGJLT carries higher output conductance compared to other two devices till drain voltage of ~ 0.6 V, because of its higher output current. At low V_{DS} (till ~ 0.55 V), output conductance is governed by channel length modulation (CLM) and at higher V_{DS} , it is governed by drain induced barrier lowering (DIBL), if impact ionization is not taken into account [125]. The value of G_D for DMG-SP, DMG and SMG DGJLT are 1.7 mS, 1.4 mS and 1.3 respectively at $V_{DS} = 0.2$ V. However, G_D decreases with drain voltage because of more collisions of carriers. At higher V_{DS} ($= 1$ V), DMG devices have marginally lower G_D than SMG devices. Fig. 6.6 also presents the early voltage (V_{EA}) with respect to V_{DS} at a gate voltage of 1 V. DMG-SP architecture offers slightly higher value of V_{EA} in the ON-state due to smaller short channel effects in it, because of more gate-coupling with the channel compared to other two devices. The values of V_{EA} for DMG-SP, DMG and SMG DGJLT are 50.6 V, 45.2 V and 12.8 V respectively at a drain voltage of 1 V. Like G_D , early voltage at lower V_{DS} is dominant by CLM and at higher V_{DS} , it is dominant by DIBL. Thus, the curve brings out that DMG-SP architecture has lower values of CLM and DIBL compared to DMG and SMG DGJLT. The higher value of V_{EA} for DMG-SP is attributed to the higher vertical gate coupling. The intrinsic gain ($A_v = G_m R_o$ or, $G_m (V_{EA} / I_{D(sat)})$) with respect to gate voltage is plotted in Fig. 6.7 at $V_{DS} = 1$ V. Dual-material gate devices offer higher A_v in comparison to single-material gate devices because of higher transconductance for aforementioned reasons. The gain values for DMG-SP, DMG and SMG DGJLT are 60.6 dB, 58 dB and 43.2 dB at $V_{GS} = 0.2$ V; and 36.5 dB, 35 dB and 28.5 dB at $V_{GS} = 1$ V respectively. Gate capacitance $C_G (= C_{GS} + C_{GD})$ with

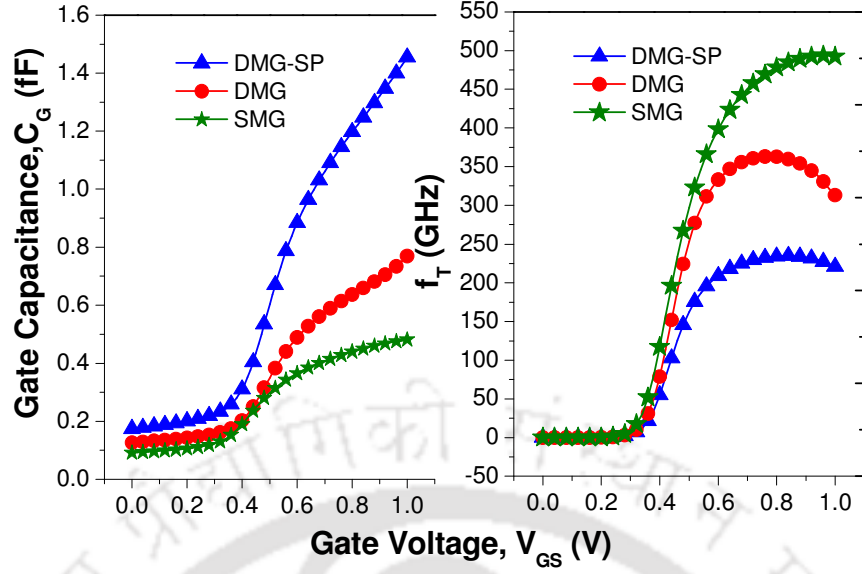


Figure 6.8: Gate Capacitance, C_G ($= C_{GS} + C_{GD}$) and unity gain cut-off frequency (f_T) with respect to gate voltage for the devices at $V_{DS} = 1$ V for $L = 40$ nm, $T_{si} = 10$ nm, and $T_{ox} = 1$ nm.

respect to gate voltage for the devices are plotted in Fig. 6.8 at $V_{DS} = 1$ V. Where, C_{GS} and C_{GD} are gate-to-source and gate-to-drain capacitances respectively. All the capacitances are extracted from the small-signal ac device simulations at a frequency of 1 MHz. DMG-SP has highest C_G compared to DMG and SMG DGJLT. This is attributed to higher fringing field lines of high-k spacer dielectric. Fig. 6.8 also shows the variation of unity gain cut-off frequency ($f_T = G_m / \{2\pi(C_{GS} + C_{GD})\}$) with gate voltage for $V_{DS} = 1$ V. At lower V_{GS} (till $V_{GS} = \sim 0.35$ V), the f_T is almost similar for all the devices due to almost same values of transconductance. However, SMG DGJLT presents superior f_T compared to other two devices at higher gate voltage, due to its considerably lower value of gate capacitance. The values of f_T for DMG-SP, DMG and SMG DGJLT are 220 GHz, 312 GHz, and 492 GHz respectively at V_{GS} of 1 V. The value of f_T for DMG-SP can be increased by using a spacer dielectric having lower dielectric constant. However, it is at the cost of higher SS than present state.

6.2.3 Electrostatic Potential Model Derivation and Verification

We have derived an electrostatic potential model for dual-material gate DGJLT to validate our demonstration taking vacuum as spacer material. In subthreshold region, where the silicon layer is fully depleted, the Poisson's equation for $0 < x < L$ and $0 < y < T_{si}$ can be written as

$$\frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} = -\frac{qN_D}{\epsilon_{si}} \quad (6.2)$$

Where, q = charge of electron, N_D = channel carrier concentration and ϵ_{si} = permittivity of silicon. A parabolic approximation of the potential in the y -direction can be assumed as [70, 127-128]

$$\psi(x, y) = \psi_0(x) + c_1(x)y(1 - y/T_{si}) \quad (6.3)$$

This satisfies the condition, $(\partial\psi/\partial y)_{y=T_{si}/2} = 0$. The surface potential $\psi_0(x)$ and coefficient $c_1(x)$ are related to each other by [70]

$$c_1(x) = \left(\frac{\partial\psi}{\partial y} \right)_{y=0} \approx \frac{C_{ox}}{\epsilon_{si}} [\psi_0(x) - \psi_G] \quad (6.4)$$

Where $C_{ox} = \epsilon_{ox}/T_{ox}$ is the oxide capacitance per unit area and $\psi_G = V_{GS} - V_{FB} = V_{GS} - (1/q)[\Phi_M - \chi - E_G/2]$ is the potential on the gate electrode with work function Φ_M and bias V_{GS} . χ is the electron affinity and E_G is the band-gap of silicon. Using equations, (6.2)–(6.4) the surface potential to a good approximation can be written as

$$\psi_0(x) = \psi(x, 0) = Ae^{x/\lambda} + Be^{-x/\lambda} + \psi_C \quad (6.5)$$

With

$$\lambda = \sqrt{T_{si} \frac{\epsilon_{si}}{2C_{ox}}}, \quad \psi_C = \psi_G + \frac{qN_D T_{si}}{2C_{ox}}$$

The constants, A and B are to be determined from boundary conditions. For dual material gate MOSFET as mentioned above, where first material has higher workfunction than the second, the expressions for flat band voltage can be written as

$$\begin{aligned} V_{FB1} &= \phi_{MS1} = \phi_{M1} - \phi_{si} \\ V_{FB2} &= \phi_{MS2} = \phi_{M2} - \phi_{si} \end{aligned} \quad (6.6)$$

ϕ_{si} is the silicon workfunction. Now, using equations (5), (7) and (8), the potential for regions concerning metal1 (M1) and metal2 (M2) can be written as

$$\begin{aligned} \psi_1(x, y) &= \psi_{01}(x) + c_{11}(x)y(1 - y/T_{si}) \\ \psi_2(x, y) &= \psi_{02}(x) + c_{12}(x)y(1 - y/T_{si}) \end{aligned} \quad (6.7)$$

Where

$$\begin{aligned} \psi_{01}(x) &= \psi_1(x_1, 0) = A_1 e^{x/\lambda} + B_1 e^{-x/\lambda} + \psi_{C1} \\ \psi_{02}(x) &= \psi_2(x_2, 0) = A_2 e^{x/\lambda} + B_2 e^{-x/\lambda} + \psi_{C2} \\ \psi_{C1} &= \psi_{G1} + \frac{qN_D T_{si}}{2C_{ox}}, \quad \psi_{C2} = \psi_{G2} + \frac{qN_D T_{si}}{2C_{ox}} \\ c_{11} &\approx \frac{C_{ox}}{\epsilon_{si}} [\psi_{01}(x) - \psi_{G1}], \quad \psi_{G1} = V_{GS} - V_{FB1} \\ c_{12} &\approx \frac{C_{ox}}{\epsilon_{si}} [\psi_{02}(x) - \psi_{G2}], \quad \psi_{G2} = V_{GS} - V_{FB2} \end{aligned} \quad (6.8)$$

x_1 and x_2 are gate lengths for metal1 (L_1) and metal2 (L_2) respectively. The constants A_1 , A_2 , B_1 and B_2 are determined from boundary conditions 1) to 4) below [114, 129].

1) The surface potential at the interface of two dissimilar gate materials for the front gate is continuous

$$\psi_1(L_1, 0) = \psi_2(L_1, 0) \quad (6.9)$$

2) The electric flux at the interface of two materials of the front gate is continuous

$$\left. \frac{d\psi_1(x, y)}{dx} \right|_{x=L_1} = \left. \frac{d\psi_2(x, y)}{dx} \right|_{x=L_1} \quad (6.10)$$

3) The electric flux at the front gate-oxide interface is continuous

$$\begin{aligned} \left. \frac{d\psi_1(x, y)}{dy} \right|_{y=0} &= \frac{\epsilon_{ox}}{\epsilon_{si}} \frac{\psi_1(x, y)|_{y=0} - V_{GS} + V_{FB1}}{T_{oxf}}, \text{ Under } M_1 \\ \left. \frac{d\psi_2(x, y)}{dy} \right|_{y=0} &= \frac{\epsilon_{ox}}{\epsilon_{si}} \frac{\psi_2(x, y)|_{y=0} - V_{GS} + V_{FB2}}{T_{oxf}}, \text{ Under } M_2 \end{aligned} \quad (6.11)$$

Similar equation exists for back gate-oxide interface.

4) The potential at the source and drain end are

$$\psi_1(0, 0) = \psi_{01}(0) = V_{bi} \quad (6.12)$$

$$\psi_2(L_1 + L_2, 0) = \psi_{02}(L_1 + L_2) = V_{bi} + V_{DS} \quad (6.13)$$

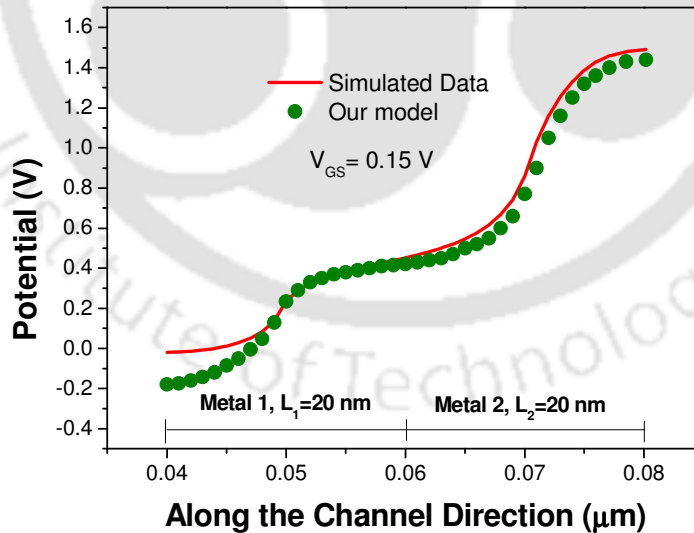


Figure 6.9: Calibration of potential in DMG DGJLT devices along the channel direction at $V_{DS} = 1$ V for $L = 40$ nm, $T_{si} = 10$ nm, and $T_{ox} = 1$ nm taking vacuum as spacer material.

V_{bi} is the built-in voltage. Using equation (6.7) – (6.13), the potential at regions under metal M_1 and M_2 i.e., $\psi_1(x, y)$ and $\psi_2(x, y)$ can be found out. As shown in Fig. 6.9, our model is in close agreement

with simulated results except near the source and drain regions. This is perhaps because, as the channel length is small, the depletion region actually extends towards source and drain side [101] which we have not considered here. As we have not developed drain current model for the devices, our simulated I_D - V_{GS} characteristic for SMG DGJLT is calibrated with [46].

6.3 A Dual Material Double-Layer Gate Stack JLT for Enhanced Analog Performance

6.3.1 Device Structure and Simulation Set up

The device structure for an n-type symmetric DM-DGS DGJLT is shown in Fig. 6.10. Operation of DMG DGJLT is explained in section 6.2.1. For DMG and SMG DGJLT, SiO_2 is used as a gate oxide material having thickness of 2 nm. For DM-DGS DGJLT, SiO_2 (equivalent oxide thickness (EOT) = 1 nm) is stacked with high-k gate dielectric material (HfO_2) of EOT = 1 nm. All three devices namely, DM-DGS, DMG and SMG are optimized by adjusting channel doping concentration (N_D) values such that each has a threshold voltage (V_T) of 0.31 V corresponding to drain current of 10^{-7} A at a drain voltage of 50 mV. The source and drain extensions (L_S and L_D) are taken as 10 nm. The process and device parameters used in this work are summarized in Table 6.2. The simulations are carried out using two carrier scheme, Fermi-Dirac model without impact ionization, doping concentration-dependent carrier mobility and electric field-dependent carrier model. Band gap narrowing model is included. Shockley-Read-Hall (SRH) recombination/ generation are employed in the simulation to account for leakage currents. The density gradient model is utilized to account for quantum mechanical effects.

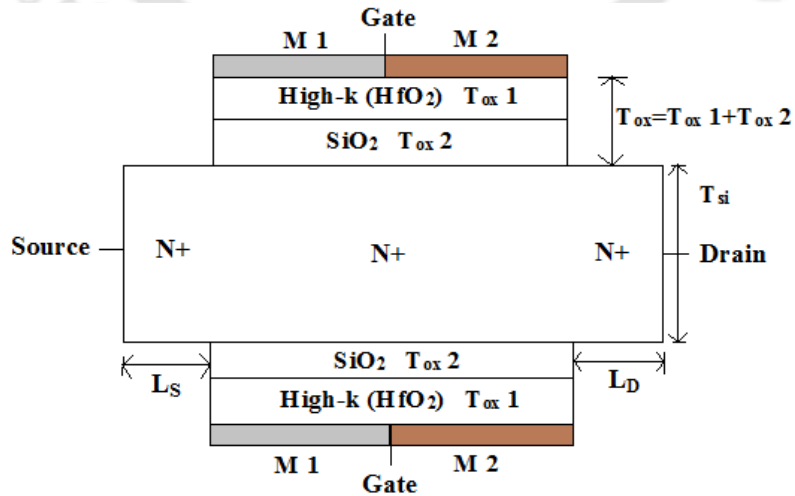


Figure 6.10: Cross-sectional view of n-type dual material double-layer gate stack double-gate junctionless transistor (DM-DGS DGJLT).

Table 6.2: Process/Device Parameter for simulation of SMG/DMG/DM-DGS

	SMG	DMG	DM-DGS
L (nm)	40	40	40
$L_{M1}:L_{M2}$ (nm)	—	20:20	20:20
$W_{M1}:W_{M2}$ (eV)	5.2 : —	5.2 : 4.7	5.2 : 4.7
N_D (cm ⁻³)	9.6 E+18	7.85 E+18	8 E+18
T_{ox} (nm) (EOT)	2 (SiO ₂)	2 (SiO ₂)	2(SiO ₂ :1nm, HfO ₂ :1nm)
T_{si} (nm)	8	8	8

6.3.2 Simulation Results and Discussion

Fig. 6.11 shows the potential and electrical field distributions along the channel direction near the silicon-oxide interface for a drain voltage (V_{DS}) = 1 V and gate voltage (V_{GS}) of 1 V. The potential distributions of DMG and DM-DGS DGJLT have abrupt change at the workfunction transition point from W_{M1} to W_{M2} , whereas SMG DGJLT follows a monotonous trend from source to drain. This enhances the electric field of DMG and DM-DGS with two peaks, but for SMG DGJLT there is only one peak near the drain. Out of the three devices mentioned, DM-DGS has lowest peak near the drain, indicating that it suppresses SCE and hot carrier effect more effectively. This is due to better gate control of DM-DGS on the channel region. Below gate voltage of $V_{GS} \sim 0.55$ V, all three devices have almost similar value of G_m . After $V_{GS} = 0.7$ V, DM-DGS has highest G_m followed by DMG and SMG DGJLT as shown in Fig. 6.12. Due to potential uplift at workfunction transition, G_m is increased for

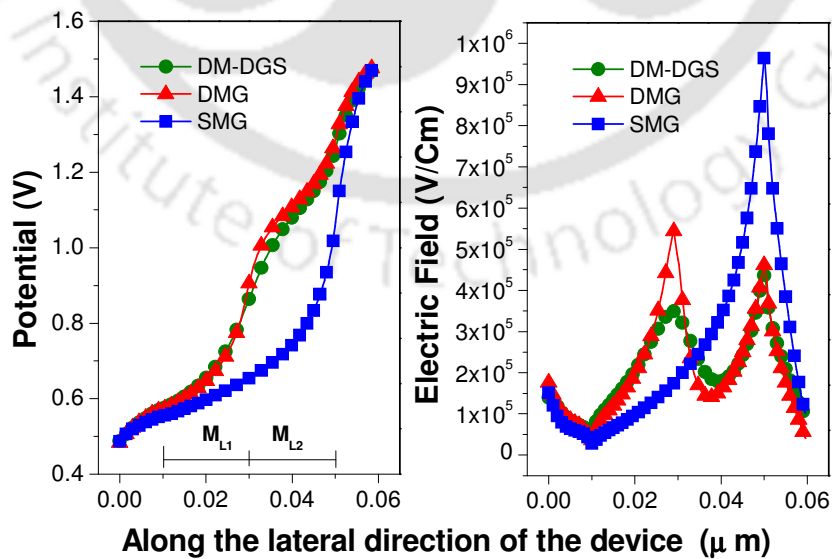


Figure 6.11: Potential and Electric field of SMG, DMG, DM-DGS devices along the channel direction near the silicon-oxide interface at $V_{DS} = 1$ V.

DM-DGS and DMG DGJLT. The values of G_m for DM-DGS, DMG and SMG DGJLT are 1.52 mS, 1.45 mS and 1.37 mS respectively at $V_{GS} = 0.9$ V. The G_m/I_D with respect to gate voltage, V_{GS} is plotted in Fig. 6.12 for a drain voltage, V_{DS} of 1 V. The values of G_m/I_D for SMG, DMG and DM-DGS DGJLT are 39.92 V^{-1} , 36.94 V^{-1} , 36.82 V^{-1} respectively at $V_{GS} = 0.2$ V. A smaller value of subthreshold slope (SS) for SMG implies its higher G_m/I_D value in the subthreshold region. G_m/I_D is mainly controlled by the body factor of devices in weak inversion regime; however its value decreases in moderate/strong inversion regime due to the lower mobility at higher doping concentration [33] as above mentioned.

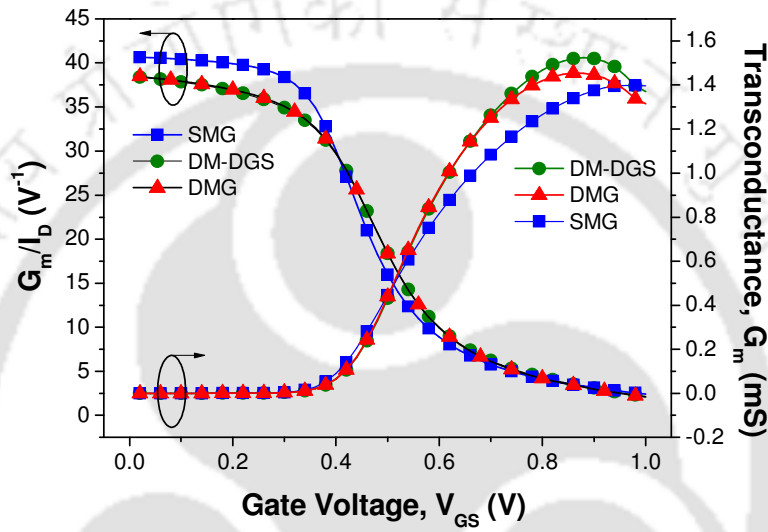


Figure 6.12: Transconductance (G_m) and transconductance to drain current ratio (G_m/I_D) with respect to gate voltage for the devices at $V_{DS} = 1$ V.

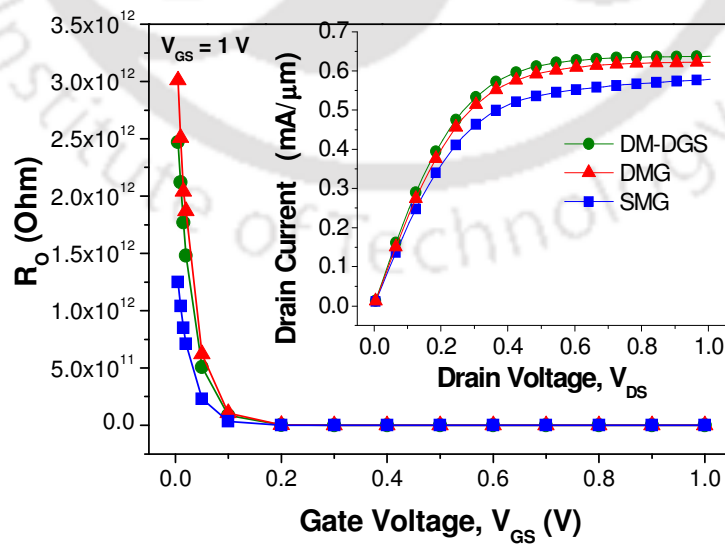


Figure 6.13: Output resistance (R_O) with respect to gate voltage and drain current with respect to drain voltage (insight) for the devices at $V_{DS} = 1$ V.

Insight of Fig. 6.13 shows the drain current (I_D) with respect to drain voltage for the devices at $V_{GS} = 1$ V. DM-DGS has higher output current, followed by DMG and SMG DGJLT for aforementioned reasons. Fig. 6.13 also presents the output resistance (R_O) with respect to V_{GS} . DMG architecture offers slightly higher value of R_O in the subthreshold region due to smaller slope in I_D - V_{DS} characteristics as compared to DM-DGS, followed by SMG DGJLT as can be seen from the figure. However, the value of R_O is highest for DM-DGS followed by DMG and SMG DGJLT for gate voltage of ~ 0.5 V or higher. The values of R_O for DM-DGS, DMG and SMG DGJLT are 44.4 k Ω , 29.3 k Ω and 16.5 k Ω respectively at a gate voltage of 1 V.

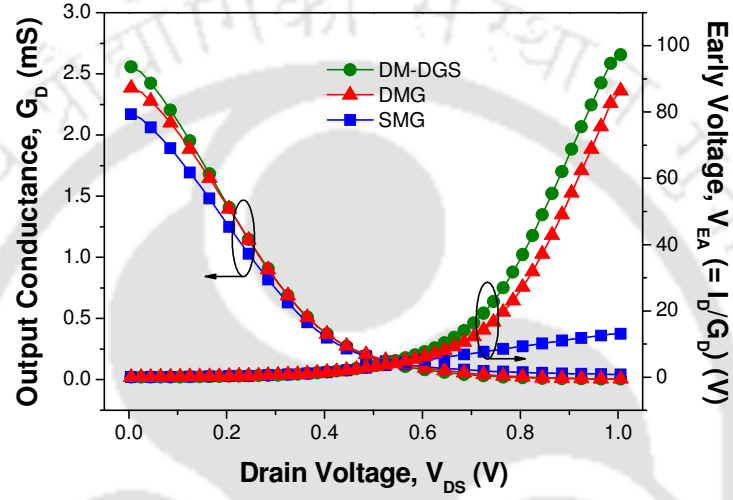


Figure 6.14: Output conductance (G_D) and early voltage (V_{EA}) with respect to gate voltage for the devices at $V_{DS} = 1$ V.

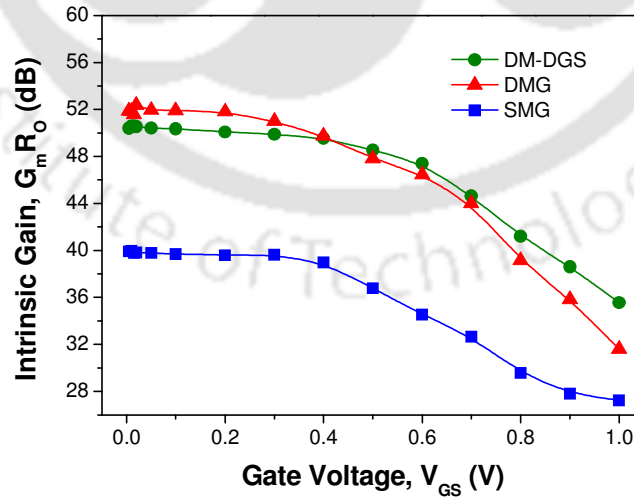


Figure 6.15: Intrinsic gain ($G_m R_O$) with respect to gate voltage for the devices at $V_{DS} = 1$ V.

Fig. 6.14 presents the output conductance $G_D (= \partial I_D / \partial V_{DS})$ variation of the devices with drain voltage, V_{DS} for a fixed value of $V_{GS} = 1$ V. The DM-DGS DGJLT carries higher output current and

hence output conductance compared to other two devices. The curve brings out that DM-DGS architecture has lower values of CLM and DIBL compared to DMG and SMG DGJLT. The value of G_D for DM-DGS, DMG and SMG DGJLT are 1.42 mS, 1.4 mS and 1.25 mS respectively at $V_{GS} = 0.2$ V. However, G_D decreases with gate voltage because of higher mobility and hence more collisions. Early voltage (V_{EA}) with respect to V_{GS} is also shown in Fig. 6.14. Early voltage can be derived from output resistance and vice versa as $V_{EA} = R_O I_{D(sat)}$ or, I_D/G_D . Where, $I_{D(sat)}$ is the saturation current. After a gate voltage of ~ 0.5 V, DM-DGS has higher early voltage followed by DMG and SMG DGJLT. At a gate voltage of 1 V, the values of V_{EA} are 97 V, 86 V and 14 V for DM-DGS, DMG and SMG DGJLT respectively. Like G_D , early voltage at lower V_{DS} is dominant by CLM and at higher V_{DS} , it is dominant by DIBL. The better performance of DM-DGS is attributed to the superior vertical gate coupling as well as lesser lateral drain control on drain current [111]. The intrinsic gain (A_V) with respect to V_{GS} is also plotted in Fig. 6.15. Dual metal gate devices offer higher A_V in comparison to single metal gate devices because of higher transconductance as well as output resistance for aforementioned reasons. The gain values for DM-DGS, DMG and SMG DGJLT are 50.1dB, 51.8 dB, 39.5 dB at $V_{GS} = 0.2$ V; and 35.5 dB, 31.5 dB and 27.2 dB at $V_{GS} = 1$ V respectively.

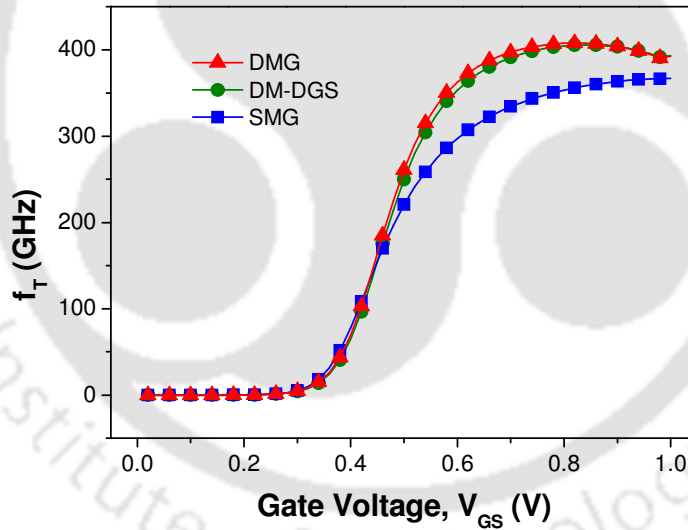


Figure 6.16: Cut-off frequency (f_T) with respect to gate voltage for the devices at $V_{DS} = 1$ V.

Fig. 6.16 shows the variation of f_T ($f_T = G_m / 2\pi(C_{GS} + C_{GD})$) with V_{GS} for $V_{DS}=1$ V. C_{GS} and C_{GD} are gate-to-source and gate-to-drain capacitances respectively. All the capacitances are extracted from the small-signal ac device simulations at a frequency of 1 MHz. At lower V_{GS} , till 0.45 V, f_T is almost same for all the devices due to almost same values of transconductance. The DM-DGS and DMG DGJLT possess almost same value of f_T for $V_{GS} > \sim 0.45$ V. However, SMG DGJLT presents lower f_T compared to other two devices at higher gate voltage. The presented I_D - V_{GS} characteristics for SMG DGJLT are calibrated with [46].

6.4 Bulk Planar Junctionless Transistor on Germanium Substrate

6.4.1 Device Operation and Simulation Setup

For all simulations, a uniform doping concentration of $N_D=1.5 \times 10^{19} \text{ cm}^{-3}$ throughout the source-channel-drain regions, channel length (L) of 20 nm and channel thickness (T_{si}) of 10 nm are considered for all simulations. SiO_2 is used as gate material having thickness of 1 nm. For all simulations, a uniform doping concentration of $N_D = 1.5 \times 10^{19} \text{ cm}^{-3}$ throughout the source-channel-drain regions is taken. SiO_2 is used as gate material having thickness of 1 nm. The simulations are carried out using two carriers, the drift-diffusion model without impact ionization. Band-gap narrowing, Schottky-Read-Hall mechanisms and Quantum correction models are included. The mobility model includes both doping and transverse-field dependence.

6.4.2 Simulation Results and Discussion

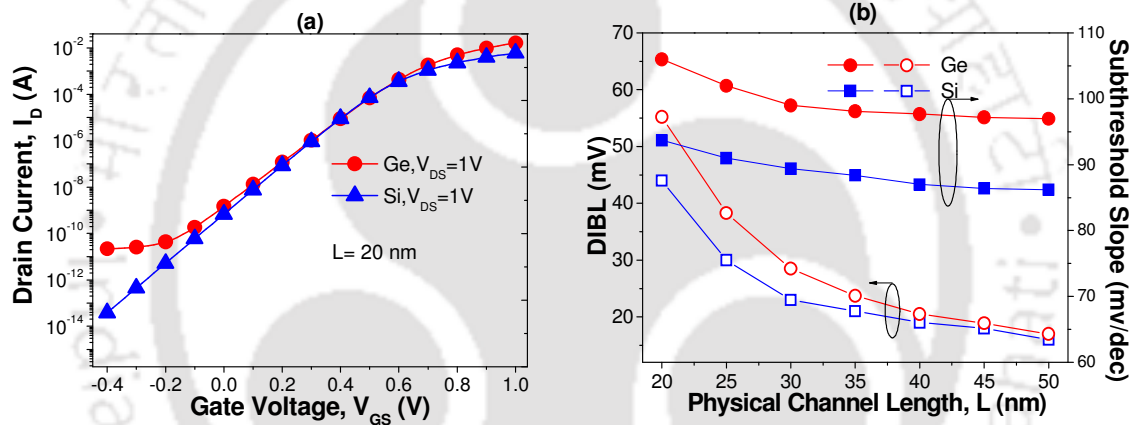


Figure 6.17: (a) Transfer characteristics for Si and Ge-BPJLT and (b) Variation of DIBL and SS with channel length. $T_{\text{si}} = 10 \text{ nm}$, $T_{\text{ox}}=1 \text{ nm}$, $N_D=1.5 \times 10^{19} \text{ cm}^{-3}$.

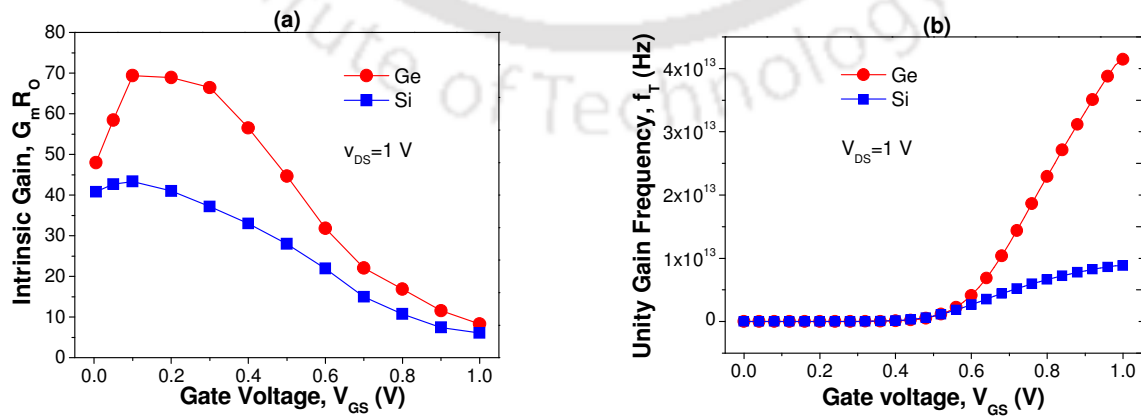


Figure 6.18: Variation of (a) intrinsic gain and (b) unity gain cut-off frequency with V_{GS} . $L = 20\text{ nm}$, $T_{\text{si}} = 10 \text{ nm}$, $T_{\text{ox}}=1 \text{ nm}$, $N_D=1.5 \times 10^{19} \text{ cm}^{-3}$.

The gate workfunctions for Si-BPJLT and Ge-BPJLT are adjusted as 5.332 eV, 4.994 eV respectively so that the threshold voltage are equal ($V_T = 0.25\text{V}$) for both the devices corresponding to drain current of 10^{-7} A at $V_{DS}=50\text{ mV}$. Fig. 6.17 (a) shows the transfer characteristics of BPJLT for silicon and germanium substrate materials at $V_{DS}=1\text{ V}$ for $L=20\text{ nm}$. It is seen that ON-state current is higher for Ge-substrate compared to Si-substrate because of higher mobility of the former. Fig. 6.17 (b) shows the drain induced barrier lowering (DIBL) and subthreshold slope (SS) variation with channel length, ranging from 20 to 50 nm. Ge-BPJLT has inferior drain induced barrier lowering (DIBL) and subthreshold slope (SS) compared to Si-BPJLT. The intrinsic gain ($G_m R_O$) is higher for Ge-BPJLT than Si-BPJLT as seen from Fig. 6.18 (a) at $V_{DS}=1\text{ V}$. The unity gain cut-off frequency ($f_T = G_m / 2\pi (C_{GS} + C_{GD} + C_{GB})$) is higher for Ge-BPJLT beyond gate voltage of $\sim 0.6\text{ V}$ as shown in Fig. 6.18 (b) at $V_{DS}=1\text{ V}$, where, C_{GS} , C_{GD} and C_{GB} are gate-to-source, gate-to-drain and gate-to-body capacitance respectively.

6.4 Summary

High-k spacer is incorporated in a dual-material gate symmetric double-gate junctionless transistor (DGJLT) architecture forming DMG-SP DGJLT. The device characteristics for analog applications are investigated and a fair comparison with DMG and SMG DGJLT are performed by setting the threshold voltage same for all devices considered, by constant current method. DMG-SP offers superior transconductance, early voltage and intrinsic gain compared to DMG and SMG DGJLT. However, SMG DGJLT has higher G_m/I_D value as compared to the other two devices in the subthreshold region. DMG DGJLT has inferior unity gain cut-off frequency compared to SMG DGJLT for higher gate voltage. DMG-SP DGJLT with high-k spacer dielectric material has even lesser f_T , because of yet higher gate capacitance compared to DMG DGJLT. By using spacer dielectric of lower dielectric constant, f_T of DMG-SP DGJLT can be increased to similar value as DMG DGJLT, however at the cost of increased SS. Transconductance can further be increased by incorporating strain silicon. An electrostatic potential model has been developed to support our simulation results. The model is in good agreement with simulated data. Derivation of complete drain current model including short channel parameters is another scope of research.

A dual material double-layer gate stack (DM-DGS) structure was incorporated in symmetric double-gate junctionless transistor (DGJLT), forming DM-DGS DGJLT. The device characteristics for analog applications were investigated and a fair comparison with DMG and SMG DGJLT was performed by setting the threshold voltage same for all devices. DM-DGS offered superior transconductance, early voltage and intrinsic gain compared to DMG and SMG DGJLT. However, SMG DGJLT has higher G_m/I_D value as compared to the other two devices. Unity gain cut-off frequency was almost similar for DM-DGS and DMG DGJLT architecture at higher gate voltage.

BPJLT using silicon substrate shows better performance for drain induced barrier lowering (DIBL), subthreshold slope (SS), output resistance (R_o), however, BPJLT with germanium substrate offers better performance in terms of I_{ON}/I_{OFF} ratio, intrinsic gain ($G_m R_o$) and unity gain frequency (f_T). G_m/I_D ratio is higher for Si-BPJLT till $V_{GS}=0.45$ V, beyond which Ge-BPJLT performs better. The main problem in using germanium as substrate material is that Ge-gate oxide interface. GeO_2 is used as a gate oxide material for Ge as substrate material. However, Ge- GeO_2 interface is not as good as Si- SiO_2 interface because of surface roughness of the former which degrades the gate control on substrate region.



Chapter 7

Channel Potential and Drain Current models for shorter-channel length DGJLT

7.1 Introduction

Looking at the low leakage currents and other advantages as mentioned in previous chapters, a JLT can be adjusted as a prospective candidate for low power circuit design applications in future technology nodes, and therefore, an analytical compact model of junctionless transistor is sought after. Since the device physics of DGJLT is fundamentally different than the JB MOSFETs, the existing models for DG JB MOSFETs do not directly apply. There are many reports on analytical/semi-analytical modelling for potential and drain current either for long-channel or short-channel length junctionless transistor in double-gate, trigate and gate-all-around architecture till date [44, 46, 48, 63-64, 67, 71, 130-141]. Some of them are valid only in subthreshold region and some are applicable from subthreshold to accumulation region. Also, some of the models are developed piecewise (region-wise) and some are non-piecewise. Gnani et al. reported a charge based cylindrical model for JLT [63]. Chen et al. reported a surface potential based piecewise model for drain current for long channel DGJLT [67]. Sallese et al. demonstrated a charge based model for drain current for long channel DGJLT [48], which may cause some convergence problem as indicated by [67]. Lime et al. demonstrated a charge based simple compact model for drain current of DGJLT [130]. Duarte et al. proposed a nonpiecewise full-range drain current model for long-channel DGJLT [64]. They also proposed an analytical bulk current model using the depletion width concept for long channel DGJLT [46], but neglected the accumulation region. They also have reported a compact model of quantum electron density at the subthreshold region for DGJLT [131]. They also proposed a nonpiecewise model for long channel junctionless cylindrical nanowire FETs [132]. Chiang derived a quasi-2D threshold voltage model for short-channel DGJLT [71]. Gnudi et al. proposed a semianalytical model of the subthreshold current of DGJLT [129]. Trevisoli et al. derived a physically-based threshold voltage definition and extraction method for trigate JLT [133]. Trevisoli et al. also reported threshold voltage model for JLT with cylindrical and rectangular geometries [134]. Trevisoli et al. proposed a drain current model accounting short-channel-effects for a p-type gate-all-around JLT [135]. Gnudi et

al. proposed an analytical model for threshold voltage variability due to random dopant fluctuations in junctionless FETs [44]. Cerdeira et al. reported a charge based continuous model for long channel DGJLT [65]. They also demonstrated an empirical potential model for long channel DGJLT [136]. Variable separation technique was used for potential and drain current modeling of DGJLT for short channel-lengths which was valid in subthreshold region [69]. Yesayan et al. proposed an explicit drain current model for long channel DGJLT using charge based method [137]. Hu et al. proposed an analytical model for electric potential, threshold voltage and subthreshold swing of short-channel junctionless surrounding-gate MOSFETs [138]. Woo et al. proposed an analytical threshold voltage model of junctionless DGJLT with localized charges [139]. Li et al. proposed the subthreshold behaviour models for nanoscale short-channel junctionless cylindrical surrounding-gate MOSFETs [140]. Trevisoli et al. proposed a surface potential based drain current analytical model for short-channel trigate junctionless nanowire transistors valid in subthreshold region [141]. There are few potential models for shorter channel length double-gate junctionless transistors which are valid in subthreshold region only. Jiang et al. proposed a physics-based analytical model of electrostatic potential for short-channel junctionless double-gate MOSFETs (JLDGMTs) operated in the subthreshold regime only by solving 2D Poisson's equation in channel region by a method of series expansion similar to Green's function [142]. Jin et al. derived potential model by solving 2-D Poisson's equation using "variable separation technique" for deep nanoscale short channel asymmetric junctionless Double-Gate (DG) MOSFETs valid in the subthreshold region [143]. Holtij et al. reported analytical 2D potential model within ultra-scaled junctionless double-gate MOSFETs (DG MOSFETs) valid in the subthreshold regime using the Schwarz-Christoffel transformation [144]. Accurate potential and drain current models, valid from depletion to accumulation regions of operation, for shorter channel length double-gate junctionless transistor, are still rare in literature.

7.2 A Surface Potential based Drain Current model for Short-Channel Junctionless Double-Gate MOSFETs (DGJLT)

In this work, potential and drain current models, covering all regions of operation, are targeted for a shorter channel length double-gate junctionless transistor (DGJLT). A two-part approach, known as the "variable separation technique" is applied to derive the channel potential, in which the total potential is divided into long channel part and short channel part. Such a method gives quite accurate results in short channel regime, because, while deriving the short channel part of potential, one can include a large set of eigenvalues and details will be presented in later section. Threshold voltage and drain induced barrier lowering (DIBL) parameters are extracted from the model. The potential model as well as the extracted parameters is then compared to professional TCAD simulation results.

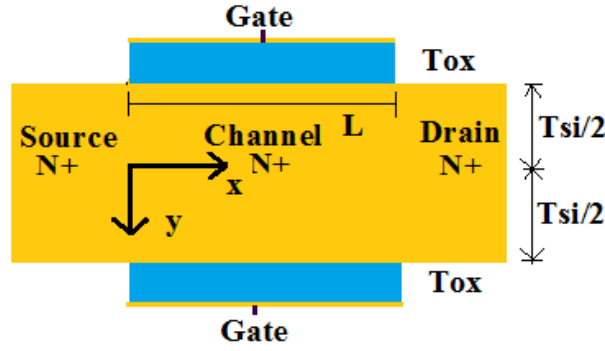


Figure 7.1: Cross-sectional view of symmetric n-channel double-gate junctionless transistor (DGJLT) with channel direction.

7.2.1 Model Derivation

The Poisson's equation considering both fixed and mobile charges in the silicon region can be written as

$$\frac{d^2\Psi(x, y)}{dx^2} + \frac{d^2\Psi(x, y)}{dy^2} = \frac{qN_D}{\epsilon_{si}} \left(e^{(\Psi(x, y) - V)/U_T} - 1 \right) \quad (7.1)$$

Where, $\Psi(x, y)$ is the channel potential, ϵ_{si} is the permittivity of silicon, V is electron quasi-Fermi potential, $U_T = kT/q$ is the thermal voltage, N_D is the channel doping concentration and q is the charge of electron. Hole density is neglected as compared to electron density. The coordinates, x and y are as shown in Fig 7.1. Equation (7.1) has no direct analytical solution. One way to solve (7.1) is variable separation technique, which states that the total potential can be divided into long channel part (1D) and short channel part (2D) i.e.,

$$\Psi(x, y) = \Psi_I(y) + \Psi_{II}(x, y) \quad (7.2)$$

Where, $\Psi_I(y)$ is the potential which is related to only y direction (long channel part) and $\Psi_{II}(x, y)$ is related to both x and y direction of the potential variation (short channel part) with below stated boundary conditions.

Expression for $\Psi_I(y)$:

$\Psi_I(y)$ is expressed as

$$\frac{d^2\Psi_I}{dy^2} = \frac{qN_D}{\epsilon_{si}} \left(e^{(\Psi_I(y) - V)/U_T} - 1 \right) \quad (7.3)$$

With boundary conditions

$$\left. \frac{\partial \Psi}{\partial y} \right|_{y=\pm \frac{T_{si}}{2}} = \Psi_s = \frac{C_{ox}}{\epsilon_{si}} \left(V_{GS} - V_{FB} - \Psi \left(\frac{T_{si}}{2} \right) \right) \quad (7.4)$$

$$\left. \frac{\partial \Psi}{\partial y} \right|_{y=0} = 0$$

Equation (7.4) has no closed form solution even though it looks simple. Integrating (7.4), we obtain

$$E_s^2 = \frac{2qN_D U_T}{\epsilon_{si}} \left[e^{(\Psi_s - V)/U_T} - e^{(\Psi_0 - V)/U_T} - \left(\frac{\Psi_s - \Psi_0}{U_T} \right) \right] \quad (7.5)$$

Where, Ψ_s and Ψ_0 are the potential at the surface and centre of the channel respectively. Thus, once the relation between Ψ_s and Ψ_0 is known, the potential at any point in the silicon body can be determined. The Gauss's law connects the surface potential with gate voltage as

$$Q_{SC} = -2\epsilon_{si} \frac{d\Psi}{dx} \Big|_{x=\pm \frac{T_{si}}{2}} = -2C_{ox} (V_G - V_{FB} - \Psi_s) \quad (7.6)$$

Q_{SC} being the space charge density per unit area, $C_{ox} = \epsilon_{ox} / T_{ox}$ is the oxide capacitance, V_{FB} is the flat band voltage. Combining (7.5) and (7.6)

$$(V_G - V_{FB} - \Psi_s)^2 = \frac{2qN_D \epsilon_{si} U_T}{C_{ox}^2} \left[e^{(\Psi_s - V)/U_T} - e^{(\Psi_0 - V)/U_T} - \left(\frac{\Psi_s - \Psi_0}{U_T} \right) \right] \quad (7.7)$$

a) For depletion region ($V_{FB} < V_G < V_{FB} + V_{DS}$) with $V_{DS} > 0$, the equation (7.7) after some mathematical reformations can be written as [67]

$$\Psi_s = V_G - V_{TH} - \frac{qN_D T_{si}}{8C_{si}} - V_T \text{Lambertw} \left[\frac{qN_D T_{si}}{4C_{ox} U_T} e^{(V_G - V_{TH} - V)/U_T} \right] \quad (7.8)$$

Where, Lambertw is the Lambert W-function, which is the inverse of the function $z = W(z)e^{W(z)}$. V_T is the threshold voltage and $(\Psi_0 - \Psi_s)$ is the difference of centre and surface potential given by,

$$\begin{aligned} V_T &= V_{FB} - qN_D T_{si} / 2C_{eff} \\ C_{eff}^{-1} &= (4C_{si})^{-1} + (C_{ox})^{-1}, \quad C_{si} = \epsilon_{si} / T_{si} \\ \Psi_0 - \Psi_s &= qN_D T_{si}^2 / 8\epsilon_{si} \end{aligned} \quad (7.9)$$

The expression of V_T in (7.9) is valid when channel length is higher. The V_T for shorter-channel device is given later section.

b) For accumulation region ($V_G > V_{FB} + V_{DS}$)

The relation between centre and surface potential $\{\Psi_s - \Psi_0 (= \alpha, \text{say})\}$ is given by [48]

$$\Psi_s - \Psi_0 = \frac{qN_D T_{si}^2}{8\epsilon_{si}} \left(e^{\frac{\Psi_0 - V}{U_T}} - 1 \right) \quad (7.10)$$

Equation (7.10) can also be expressed as [65]

$$\Psi_s - \Psi_0 = -\frac{qN_D T_{si}}{8C_{si}} + U_T \text{Lambertw} \left[\frac{qN_D T_{si}}{8C_{si} U_T} e^{\frac{qN_D T_{si}}{8C_{si} U_T} \frac{\Psi_s - V}{U_T}} \right] \quad (7.11)$$

Now, using (7.7) and (7.11), the relation between surface potential with gate voltage can be obtained as [65]

$$(V_G - V_{FB} - \Psi_s)^2 = \text{sign}(\alpha) \left(\frac{q^2 N_D^2 T_{si} \epsilon_{si}}{C_{ox}^3} \right) \left[e^{(\Psi_s - V)/U_T} - 1 - \left(1 + \frac{8C_{si} U_T}{qN_D T_{si}} \right) \right. \\ \left. \times \left\{ -\frac{qN_D T_{si}}{8C_{si} U_T} + \text{Lambertw} \left[\frac{qN_D T_{si}}{8C_{si} U_T} e^{\frac{qN_D T_{si}}{8C_{si} U_T}} e^{\frac{\Psi_s - V}{U_T}} \right] \right\} \right] \quad (7.12)$$

For accumulation region ($V_{GS} > V_{FB} + V_D$), $\alpha > 0$. Equation (7.12) can only be solved numerically. The centre potential can be derived using equations (7.8) – (7.12), also explained in [136].

Expression for $\Psi_{II}(x, y)$:

$\Psi_{II}(x, y)$ is expressed as

$$\frac{d^2 \Psi_{II}(x, y)}{dx^2} + \frac{d^2 \Psi_{II}(x, y)}{dy^2} = 0 \quad (7.13)$$

$$\Psi_{II}(0, y) = V_{bi} - \Psi_I(y)$$

$$\Psi_{II}(L, y) = V_{DS} + V_{bi} - \Psi_I(y)$$

with the boundary conditions

$$\epsilon_{si} \frac{\partial \Psi_{II}(T_{si}/2, x)}{\partial x} = -C_{ox} \Psi_{II}\left(\frac{T_{si}}{2}, x\right) \quad (7.14)$$

$$\left. \frac{\partial \Psi_{II}}{\partial y} \right|_{y=0} = 0$$

Equation (7.13) is a mixed boundary value problem and it is already solved by many groups [145]-[146]. The final solution is

$$\Psi_{II}(x, y) = \left\{ A_0 e^{\frac{2\mu_n(x-L)}{T_{si}}} + A_1 e^{\frac{2\mu_n x}{T_{si}}} \right\} \times \cos(\mu_n y) \quad (7.15)$$

Where,

$$A_0 = B_1 \left[V_{DS} + V_{bi} \left(1 - e^{-\frac{2\mu_n L}{T_{si}}} \right) \right] - B_2 \Psi_{S(\text{Long})} \quad (7.16)$$

$$A_1 = B_1 \left[V_{bi} \left(1 - e^{-\frac{2\mu_n L}{T_{si}}} \right) - V_{DS} e^{-\frac{2\mu_n L}{T_{si}}} \right] - B_2 \Psi_{S(\text{Long})}$$

$$B_1 = \frac{4 \times \sin(\mu_n)}{2\mu_n + \sin(2\mu_n) \left(1 - e^{-\frac{2\mu_n L}{T_{si}}} \right)}, \quad B_2 = \frac{4\mu_n \times \cos\left(\frac{\mu_n}{2}\right) \left(1 - e^{-\frac{2\mu_n L}{T_{si}}} \right)}{2\mu_n + \sin(2\mu_n) \left(1 - e^{-\frac{2\mu_n L}{T_{si}}} \right)} \quad (7.17)$$

$\Psi_{S(\text{Long})}$ is the long channel surface potential. The eigen-value μ_n is the periodic n^{th} root of this equation and determined using the permittivity and thickness of both silicon and oxide. It can have infinite possible values for μ . However, first 1-2 iteration(s) give quite good result.

$$2\mu_n \tan(\mu_n) = \frac{\epsilon_{ox} T_{si}}{T_{ox} \epsilon_{si}} \quad (7.18)$$

Now, putting the expressions of $\Psi_I(y)$ and $\Psi_{II}(x,y)$ in equation (7.2), the total potential in the channel region of a short channel DGJLT can be determined.

Threshold voltage extraction

A schematic plan for calculating the threshold voltage (V_T) is given in Fig. 7.2. The threshold voltage is given by the following expression, and it is valid for longer as well as shorter channel length devices [147]

$$V_T = V_{GS} + \Delta V_{GS} \left(\frac{U_T \ln(N_D / n_i) - \Psi_{\min(V_{GS1})}}{\Psi_{\min(V_{GS2})} - \Psi_{\min(V_{GS1})}} \right) \quad (7.19)$$

$\Psi_{\min(V_{GS1})}$ and $\Psi_{\min(V_{GS2})}$ are the minimum potentials at two gate-to-source voltages V_{GS1} and V_{GS2} . Assuming a linear relationship between $\Psi_{\min}$ and V_{GS} in the subthreshold region, threshold voltage can be extracted using (13).

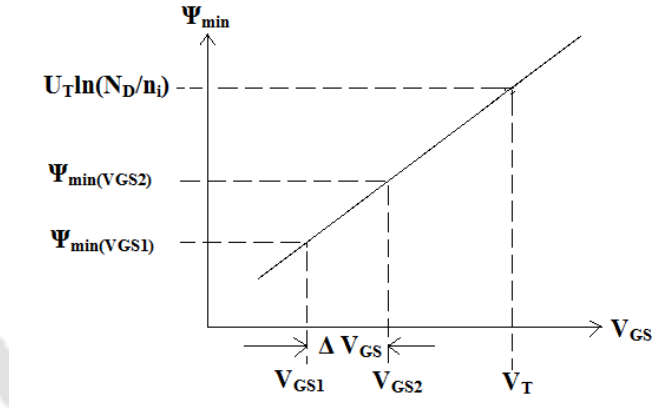


Figure 7.2: Schematic plan for calculating the threshold voltage. Here, $V_T = V_{GS}$ at $U_T \ln(N_D/n_i) = \Psi_{\min}$. ΔV_{GS} is the difference between two voltages in the subthreshold region.

Drain induced barrier lowering (DIBL) is defined as the change in threshold voltage when drain voltage changes from 50 mV to 1 V i.e.,

$$DIBL = V_T|_{V_{DS}=50mV} - V_T|_{V_{DS}=1V} \quad (7.20)$$

7.2.2 Discussion and Verification of Model

To validate the model results, they are compared with electrical characteristics for the devices simulated using 2D ATLAS device simulator with version 5.19.20.R [72]. Lombardi mobility model is employed, accounting for the dependence on the impurity concentrations as well as the transverse

and longitudinal electric field values. Shockley-Read-Hall (SRH) recombination model is included in the simulation to account for leakage currents. Because of high channel doping concentration, Fermi-Dirac carrier statistics without impact ionization is utilized in the simulations. Band gap narrowing model (BGN) is also incorporated to take care of the band gap narrowing effect which may arise due to highly doped channel regions. Quantum effect is not considered here. Channel doping concentration N_D of 5×10^{18} and $1 \times 10^{19} \text{ cm}^{-3}$, equivalent gate oxide thickness (EOT) = 2 nm, silicon thickness (T_{si}) = 10, 15 nm are considered for TCAD simulation. Channel width (W) is $1 \mu\text{m}$. In addition, p-type polysilicon is used having doping concentration 10^{20} cm^{-3} . The interface charge concentration (N_{ss}) is considered as $5 \times 10^{10} \text{ cm}^{-3}$. A constant mobility (μ_e) of $100 \text{ cm}^2/\text{V.s}$ is assumed.

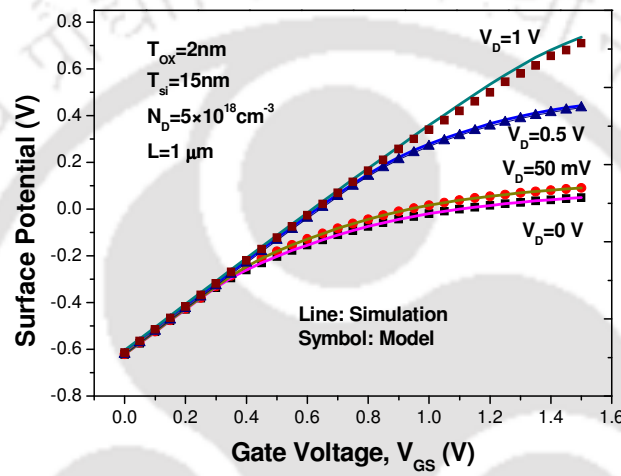


Figure 7.3: Surface potential with respect to gate voltage near the drain side for $V_D=0 \text{ V}$, 50 mV, 0.5 V and 1 V. $L=1 \mu\text{m}$, $T_{si}=15 \text{ nm}$, $T_{ox}=2 \text{ nm}$, $N_D=5 \times 10^{18} \text{ cm}^{-3}$ and source/drain extension length=50 nm. Flat band voltage (V_{FB}) is considered as $\sim 1.1 \text{ eV}$.

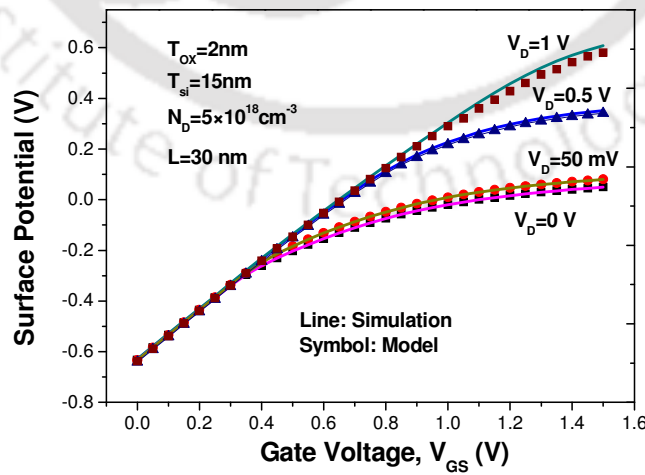


Figure 7.4: Surface potential with respect to gate voltage near the drain side for $V_D=0 \text{ V}$, 50 mV, 0.5 V and 1 V. $L=30 \text{ nm}$, $T_{si}=15 \text{ nm}$, $T_{ox}=2 \text{ nm}$, $N_D=5 \times 10^{18} \text{ cm}^{-3}$ and source/drain extension length=10 nm. Flat band voltage (V_{FB}) is considered as $\sim 1.1 \text{ eV}$.

For channel length of 1 μm , source/drain extension length (L_S/L_D) is taken as 50 nm; and for channel length of 30 nm-80 nm, L_S/L_D is taken as 10 nm to avoid parasitic resistance effect. Calculations are performed on Mathematica computational software. Fig. 7.3 shows the surface potential with respect to gate voltage, for different values of $V_D=0\text{ V}$, 50 mV, 0.5 V and 1 V respectively for channel length of 1 μm . The simulation and model curves are in close agreement. Fig. 7.4 shows the surface potential with respect to gate voltage, for different values of $V_D=0\text{ V}$, 50 mV, 0.5 V and 1 V respectively for channel length of 30 nm. The marginal difference may be due to the inclusion of source and drain

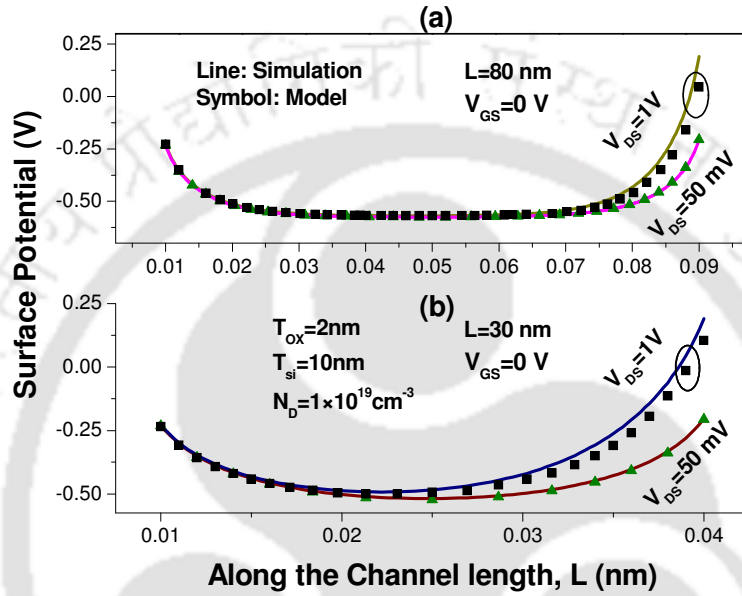


Figure 7.5: Surface potential along the channel for (a) $L=80\text{ nm}$ (long channel) at $V_D=50\text{ mV}$, 1V (b) $L=30\text{ nm}$ (short channel). $T_{si}=10\text{ nm}$, $T_{ox}=2\text{ nm}$, $N_D=1 \times 10^{19}\text{ cm}^{-3}$, $V_{GS}=0\text{ V}$ and source/drain extension length=10 nm. Flat band voltage (V_{FB}) is considered as $\sim 1.1\text{ eV}$.

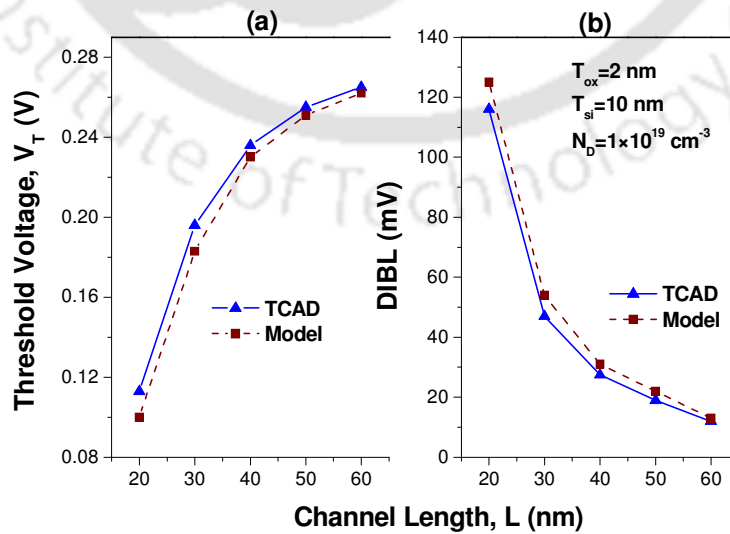


Figure 7.6: (a) Threshold voltage (V_T) at $V_{DS}=50\text{ mV}$ for $L=20\text{ nm}$ to 60 nm (b) drain induced barrier lowering (DIBL) for $L=20\text{ nm}$ to 60 nm. $T_{si}=10\text{ nm}$, $T_{ox}=2\text{ nm}$, $N_D=1 \times 10^{19}\text{ cm}^{-3}$.

extension resistances in TCAD characteristics; and the exclusion of fringing electric fields and quantum effects in the model. Fig. 7.5 (a) and (b) shows the potential along the channel direction, 0.5 nm away from the Si-SiO₂ interface, at $V_{DS} = 50$ mV and 1 V respectively keeping $V_{GS}=0$ V at gate length of 80 nm and 30 nm. Both the simulation and model plots are in close agreement. There is marginal difference of potential towards the drain side between model and simulation. For example, for $L = 30$ nm at $V_{DS} = 1$ V this difference are 86.4 mV. Fig. 7.6 (a) and (b) shows the threshold voltage and drain induced barrier lowering characteristics extracted from model and simulation, for different gate lengths. The values obtained from model and simulation are in close agreement. The marginal difference of threshold voltage between model and TCAD results for say, $L=20$ nm and $L=60$ nm are 0.013 and 0.003 V respectively. The difference of DIBL between model and TCAD results are 9 mV and 1 mV for $L = 20$ nm and $L = 60$ nm respectively.

7.2.3 Drain Current Model

The mobile charge density Q_m can be written as

$$Q_m = Q_{SC} - Q_d \quad (7.21)$$

$Q_d = qN_D T_{si}$ is the fixed charge density. The drain current can be expressed as (using (7.7))

$$\begin{aligned} I_D &= -\mu \frac{W}{L} \int_0^{V_{DS}} Q_m dV \\ &= -\mu \frac{W}{L} \int_0^{V_{DS}} [2C_{ox}(V_G - V_{FB} - \Psi_s) + Q_d] dV \end{aligned} \quad (7.22)$$

It is assumed that $V_s=0$ and $V_D=V_{DS}$. W is the width of the device and Ψ_s (long-channel part + short-

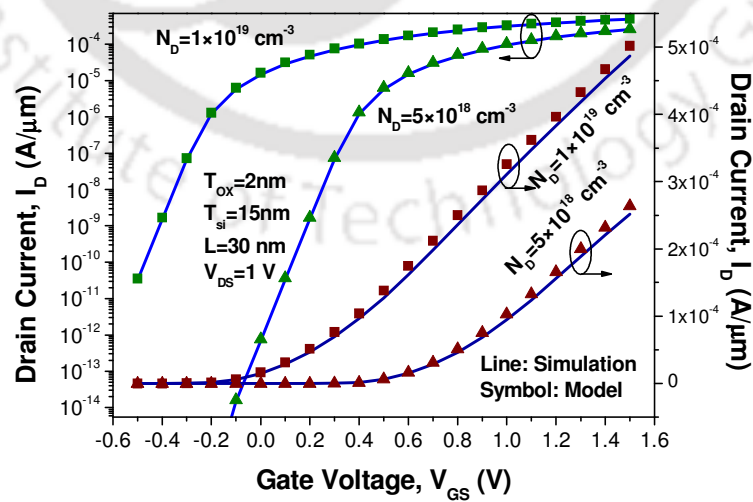


Figure 7.7: Drain current with respect to gate voltage for $N_D=5 \times 10^{18} \text{ cm}^{-3}$ and $1 \times 10^{19} \text{ cm}^{-3}$. $L=30$ nm, $T_{si}=15$ nm, $T_{ox}=2$ nm, $V_{DS}=1$ V and source/drain extension length=10 nm. Flat band voltage (V_{FB}) is considered as ~ 1.1 eV. Lines show the TCAD simulations and symbols shows model results.

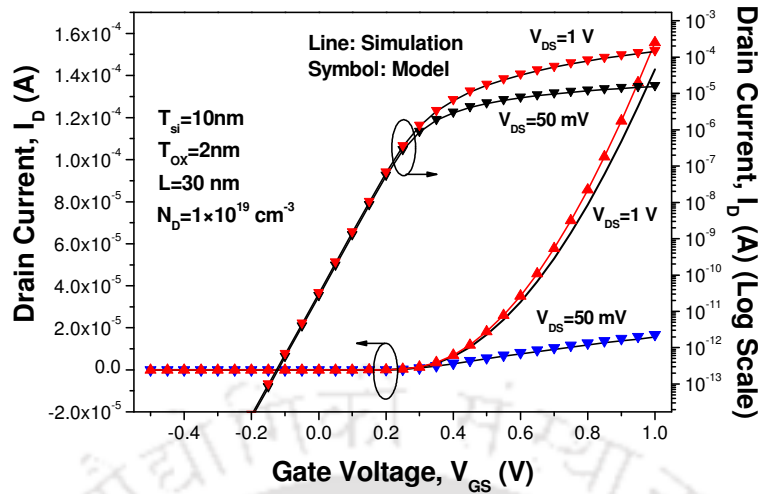


Figure 7.8: Drain current with respect to gate voltage for $T_{si}=10$ nm, $L=30$ nm, $T_{ox}=2$ nm $N_D=1 \times 10^{19}$ cm^{-3} and source/drain extension length=10 nm at $V_{DS}=50$ mV and 1 V. Lines show the TCAD simulations and symbols show model results.

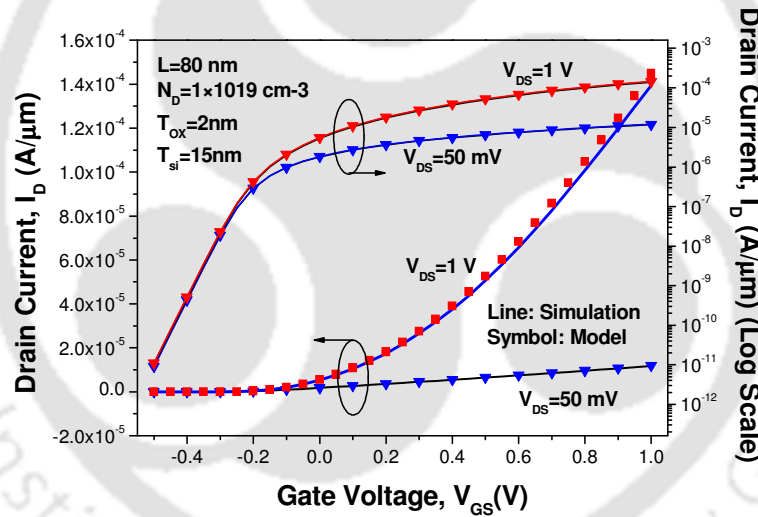


Figure 7.9: Drain current with respect to gate voltage for $L=80$ nm, $T_{si}=15$ nm, $T_{ox}=2$ nm, $N_D=1 \times 10^{19}$ cm^{-3} and source/drain extension length=10 nm at $V_{DS}=50$ mV and 1 V. Lines show the TCAD simulations and symbols show model results.

channel part) is the surface potential. Fig. 7.7 shows the drain current with respect to gate voltage for different values of N_D i.e., $8 \times 10^{18} \text{ cm}^{-3}$ and $1 \times 10^{19} \text{ cm}^{-3}$ at a drain voltage of 1 V. Same current values are plotted in both logarithmic (left) and linear scales (right). The model results (symbols) are in close agreement with TCAD simulation (lines) in all regions of device operation, i.e., subthreshold to accumulation region. The subthreshold slope obtained from model is almost equal to TCAD results. As expected, current saturates at higher gate voltage. Also, saturation current increases with increase in channel doping concentration as usual. The current in the accumulation region is obtained

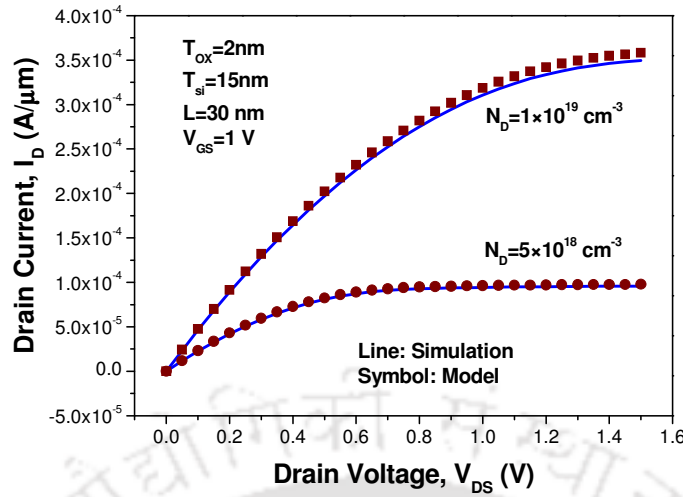


Figure 7.10: Drain current with respect to drain voltage for $N_D=5 \times 10^{18} \text{ cm}^{-3}$ and $1 \times 10^{19} \text{ cm}^{-3}$. $L=30 \text{ nm}$, $T_{si}=15 \text{ nm}$, $T_{ox}=2 \text{ nm}$, $V_{GS}=1 \text{ V}$ and source/drain extension length= 10 nm . Flat band voltage (V_{FB}) is considered as $\sim 1.1 \text{ eV}$. Lines show the TCAD simulations and symbols shows model results.

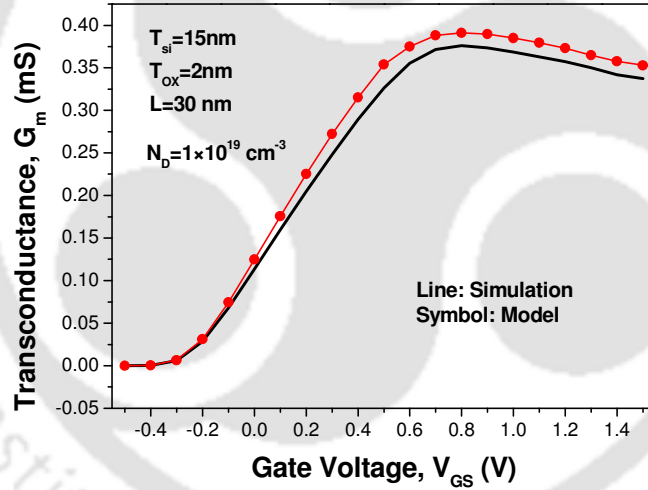


Figure 7.11: Transconductance with respect to gate voltage for $L=30 \text{ nm}$, $T_{si}=15 \text{ nm}$, $T_{ox}=2 \text{ nm}$, $N_D=1 \times 10^{19} \text{ cm}^{-3}$ at $V_{DS}=1 \text{ V}$ and source/drain extension length= 10 nm . Lines show the TCAD simulations and symbols shows model results.

numerically. The subthreshold slope extracted from model and TCAD are in close agreement for long as well as short channel DGJLT. For example, for a DGJLT with $L=30 \text{ nm}$, $T_{si}=10 \text{ nm}$, $T_{ox}=2 \text{ nm}$ and $N_D=1 \times 10^{19} \text{ cm}^{-3}$, the subthreshold slope is 63 mV/dec as extracted from TCAD, which is almost similar to the value extracted from model. Fig. 7.8 shows the transfer characteristic for $T_{si}=10 \text{ nm}$, $L=30 \text{ nm}$, $T_{ox}=2 \text{ nm}$ and $N_D=1 \times 10^{19} \text{ cm}^{-3}$ at gate voltages V_{GS} of 50 mV and 1 V . Both TCAD (solid line) and model results (symbols) are in close agreement. Fig. 7.9 shows the drain current with respect to gate voltage for $L=80 \text{ nm}$, $T_{si}=15 \text{ nm}$, $T_{ox}=2 \text{ nm}$ and $N_D=1 \times 10^{19} \text{ cm}^{-3}$ at $V_{DS}=1 \text{ V}$. Lines show the

TCAD simulations and symbols shows model results. TCAD (solid line) and model results (symbols) are in good agreement. Fig. 7.10 presents the drain current with respect to drain voltage for different values of N_D i.e., $8 \times 10^{18} \text{ cm}^{-3}$ and $1 \times 10^{19} \text{ cm}^{-3}$ at a gate voltage of 1 V for $L=30 \text{ nm}$. The models (symbols) are in close accord with TCAD simulation (lines). The transconductance with respect to gate voltage for $L=30 \text{ nm}$, $T_{\text{si}}=15 \text{ nm}$, $T_{\text{ox}}=2 \text{ nm}$, $N_D=1 \times 10^{19} \text{ cm}^{-3}$ at $V_{\text{DS}}=1 \text{ V}$ is shown in Fig. 7.11. TCAD simulations (symbols) and model results (lines) are not in close match at higher gate voltages. Fig. 7.12 shows the output conductance with respect to drain voltage for $L=30 \text{ nm}$, $T_{\text{si}}=15 \text{ nm}$, $T_{\text{ox}}=2 \text{ nm}$, $N_D=1 \times 10^{19} \text{ cm}^{-3}$ at $V_{\text{GS}}=1 \text{ V}$. Both TCAD and model results are in close agreement.

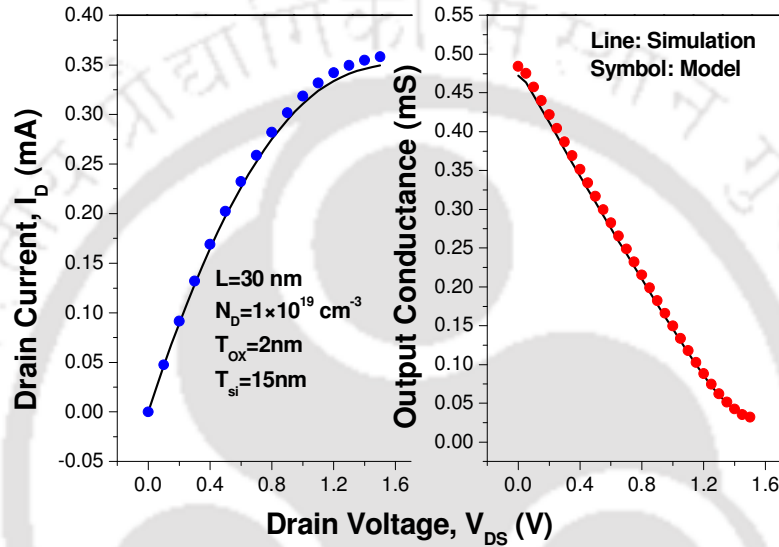


Figure 7.12: Drain current and output conductance with respect to drain voltage for $L=30 \text{ nm}$, $T_{\text{si}}=15 \text{ nm}$, $T_{\text{ox}}=2 \text{ nm}$, $N_D=1 \times 10^{19} \text{ cm}^{-3}$ at $V_{\text{GS}}=1 \text{ V}$ and source/drain extension length=10 nm. Lines show the TCAD simulations and symbols shows model results.

7.3 Summary

A semi-analytical model is proposed to calculate the channel surface potential as well as drain current for shorter channel length symmetric double-gate junctionless transistor with potential two parts approach. Carrier mobility is assumed constant. Quantum effects are not considered. The model is valid in depletion to accumulation region of operation. Threshold voltage and drain induced barrier lowering parameters were extracted from model. Assessment of the model with TCAD simulations confirms its legitimacy. Consideration of short-channel and quantum effects in the model is another scope for future research.

Chapter 8

Suggested Fabrication Steps for a DGJLT

8.1 Introduction

On 22 October 1925, the first patent for the transistor principle was filed in Canada by Austrian-Hungarian physicist Julius Edgar Lilienfeld [19]. The Lilienfeld's transistor is a field-effect device, much like modern MOS devices but does not contain any junction. It consists of a thin semiconductor film deposited on a thin insulator layer, itself deposited on a metal electrode. The latter metal electrode serves as the gate of the device. Current flows in the resistor between two contact electrodes, in much the same way that drain current flows between the source and drain in a modern MOSFET. Unfortunately, the technology available at that time would never have been able to produce a working device [26].

Recently many groups have fabricated the junctionless transistor following Lilienfeld's first transistor. The first successful junctionless transistor in nanowire gated resistor architecture has been reported by Colinge's group at Tyndall National Institute, Ireland in 2010 [26]. Subsequently, Choi et al. experimentally investigated the sensitivity of threshold voltage to the variation of silicon nanowire width in junctionless gate-all-around transistor [41]. Su et al. experimentally investigated the feasibility of junctionless gate-all-around polycrystalline silicon (poly-Si) nanowire transistors utilizing only one heavily doped poly-Si layer to serve as source, channel, and drain regions. According to them such scheme appears of great potential for future system-on-panel and 3-D IC applications [45]. Yu et al. fabricated junctionless nanowires (JNT) with Germanium channels by a CMOS-compatible top-down process [148]. The transistors so fabricated exhibit the lowest subthreshold slope for JNT with Germanium channels. Tang et al. presented a simple and low-cost fabrication method for junctionless transistors based on the dopant-assisted etching and oxidation effects. The proposed technique generates a monolithic elevated source/drain (S/D) structure without the addition of any elevation or recession process. This allows high current flow when the transistor is turned on and ensures full depletion of carriers when the transistor is turned off. [149]. Jiang et al. fabricated junctionless flexible oxide-based electric-double layer thin-film transistors (TFTs) on paper substrates at room temperature [150]. Such junctionless paper TFTs can provide a new opportunity for

flexible paper electronics and low-cost portable-sensor applications. Junctionless low-voltage transparent indium-zinc-oxide (IZO) thin-film transistors (TFTs) gated by SiO_2 -based solid electrolyte films are fabricated on glass substrates by a full room-temperature process [151]. The attractive feature of such TFTs is that the channel and source/drain electrodes are the same ultrathin IZO film without any source/drain electrodes. Bartsch et al. developed a novel double-transduction principle for silicon nanowire resonators, which exploits the depletion charge modulation in a junctionless field effect transistor body and the piezoresistive modulation [152].

8.2 Basic fabrication steps for a semiconductor device

Modern CMOS technologies require more than 200 fabrication steps. In this chapter a possible and very simple process flow is proposed for double-gate junctionless transistor (DGJLT). The sequence of steps is a combination of the following operations [25]

- Wafer processing to produce proper type of substrate
- Photolithography to precisely define each region
- Oxidation, deposition, and ion implantation steps for adding/modifying of materials
- Etching to remove materials from the wafer

Wafer Processing

The starting material in a CMOS technology that is the wafer must be of very high quality in terms of purity. The wafer must be grown as a single-crystal silicon body having minimum defects or parasitic impurities. The wafer must contain proper amount of doping impurity with type to have the requisite resistivity. Czochralski method is popularly used to achieve this purpose. Here, a seed of crystalline silicon is immersed in molten silicon and gradually pulled out while rotating. Hereby large single-crystal cylindrical “ingot” is formed that can be sliced into wafers. The surface damages that may be caused because of slicing are overcome by polishing and chemically etching the wafer. Typically wafers are 4-12 inch of diameter and 500 to 775 μm thick. Semiconductor industry has already accepted 18 inch wafer with a thickness of 925 μm for the near future. The resistivity of the wafer is typically 0.05 to 0.1 $\Omega\cdot\text{cm}$. Each 12 inch wafer cost around \$200-500 and one 8 inch wafer costs around \$30-40 depending on market demand [153].

Photolithography

It is the process of transferring the circuit layout information into the wafer with extreme precision. The layout consists of polygons representing different types of layers e.g. n-well, source/drain region,

polysilicon, contacts etc. First, the layers or patterns are written to a transparent glass mask by a precisely controlled electron beam. The mask is placed in the wafer which was originally covered by a photoresist, and the pattern is projected into the wafer by ultraviolet light. Finally, the exposed photoresist is etched. That is a single iteration of photolithography combines several steps in sequence. It involves cleaning, preparation, photoresist application, exposure to UV light and developing, etching and photoresist removal. Modern clean rooms use automated, robotic wafer track systems to coordinate the process. Each mask costs several dollars. Therefore, the cost of each chip depends on the number of mask steps used for the fabrication process. The purchase price of a photomask can range from \$1,000 to \$100,000 for a single high-end phase-shift mask. As many as 30 masks (of varying price) may be required to form a complete mask set [153].

Oxidation

Silicon forms a uniform oxide layer on surface with very little strain in the lattice. In addition to serving as a gate dielectric, SiO_2 acts a protective coating in many steps of fabrication. SiO_2 is grown in by placing the exposed silicon in an oxidising atmosphere such as oxygen at around 1000°C . The oxide growth depends on the type and pressure of atmosphere, temperature and doping of silicon. The thickness of the oxide affects the current handling capability, noise and reliability of the devices in a chip [153].

Ion Implantation

The process of penetration of dopants into an exposed silicon area by accelerating it as a high energy focussed beam is called ion implantation. The doping level is determined by the intensity and duration of the implantation. According to the depth of the silicon area, the energy intensity of the beam is fixed. Ion implantation damages the silicon lattice extensively. Therefore, silicon is heated for about 1000°C for 15 to 30 minutes to form the lattice bonds again. This process is called annealing. However, annealing too leads diffusion of dopants and broadening the profile in all directions. Therefore, annealing is done only once after completing all implantations has been completed. The implant beam is generally tilted by 7-9 degrees to avoid side diffusion [153].

Deposition and Etching

Device fabrication requires deposition of various materials like polysilicon, dielectric materials separating interconnect layers and metal layers as interconnects. A common method of forming polysilicon is “Chemical Vapour Deposition at low pressure (LPCVD)”, whereby wafers are placed in a furnace filled with a gas that creates the desired material through a chemical reaction.

Etching is the process of removal of unnecessary materials from the rest. It is a very crucial step and precise control is required. Depending on the speed, type of material to be etched, accuracy and selectivity required in the etching step, any one of the following steps are used

- a) Wet etching: Wafer is placed in a chemical liquid (Low precision)
- b) Plasma etching: Bombarding the wafer with a plasma gas (High precision)
- c) Reactive Ion Etching (RIE): Ions are produced in a gas bombard the wafer

8.3 Suggested fabrication steps for DGJLT with cross-sectional views

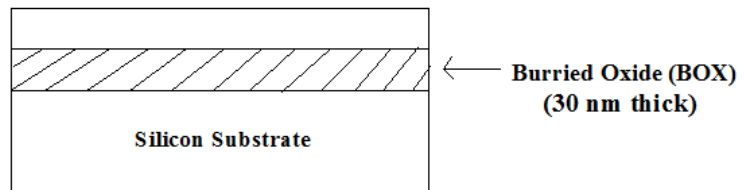
We have extensively followed the fabrication steps used by Colinge's group [26] for suggesting the possible fabrication steps for n-type double-gate junctionless transistor. We have performed the required process simulation for obtaining DGJLT structure and obtained the electrical characteristic of the so obtained structure using VisualFab and Gds2Mesh and 3D Genius device simulator from Cogenda [73]. Cogenda is an established vendor of Technology Computer Aided Design (TCAD) software employed for both process and device simulations.

The possible process steps for DGJLT are given below. Simplistic view of two dimensional cross-sectional views of major fabrication steps for suggested fabrication of double-gate junctionless transistor (DGJLT) are also given.

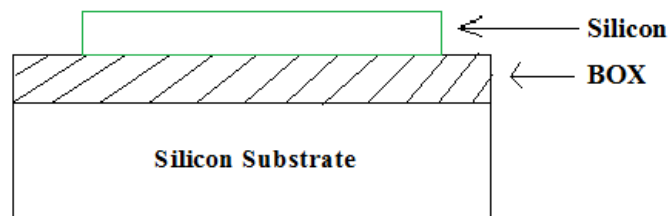
1. Starting with SOI wafers and using electron-beam lithography, silicon layer of 10 nm wide and 10 nm thick is defined. The cross-sectional view is shown in Fig. 8.1 (a), (b).
2. The silicon layer is uniformly doped by ion implantation using arsenic dopants (n-type device). The implant energies and doses are chosen to yield uniform doping concentration $1.5 \times 10^{19} \text{ cm}^{-3}$. Gate oxide of 3-nm thickness are grown. The resulting cross-sectional view is shown in Fig. 8.1 (c), (d).
3. The gate is formed by deposition of a 50-nm-thick layer of amorphous silicon at a temperature of 550°C in a low-pressure chemical vapour deposition (LPCVD) reactor. The cross-sectional view after lithography and patterning is shown in Fig. 8.1 (e).
4. After heavy P+ gate doping using boron ions at a dose of $2 \times 10^{14} \text{ cm}^{-2}$, the samples are annealed in nitrogen ambient at 900°C for 30 min. The cross-sectional view is shown in Fig. 8.1 (f).
5. The gate electrodes are then patterned and etched in a reactive-ion etch chamber. The cross-sectional view is shown in Fig. 8.1 (g).
6. After gate patterning, a protective SiO_2 layer is deposited (not shown), contact holes were etched, and electrical contact was made using classical TiW–aluminium metallization

process. The cross-sectional view is shown in Fig. 8.1 (h).

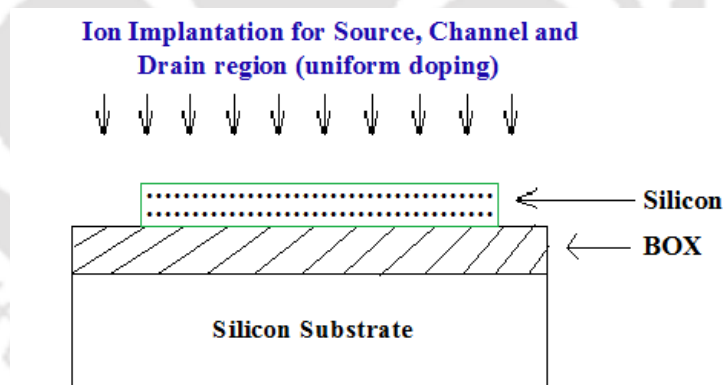
7. After gate patterning no doping step is performed so that doping type and concentration of source channel and drain region remains same.



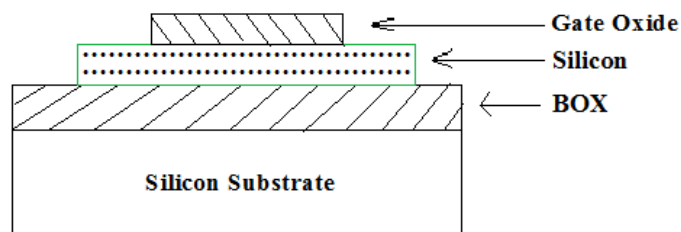
(a) Starting silicon on insulator (SOI) wafer



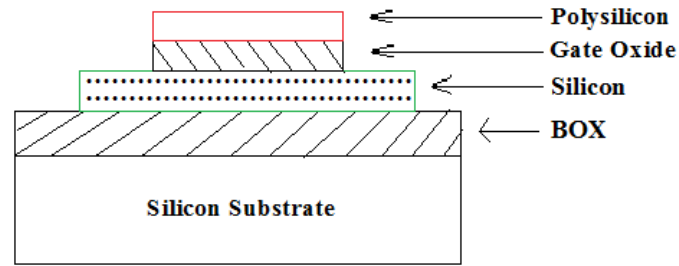
(b) Silicon device layer after lithography and pattern



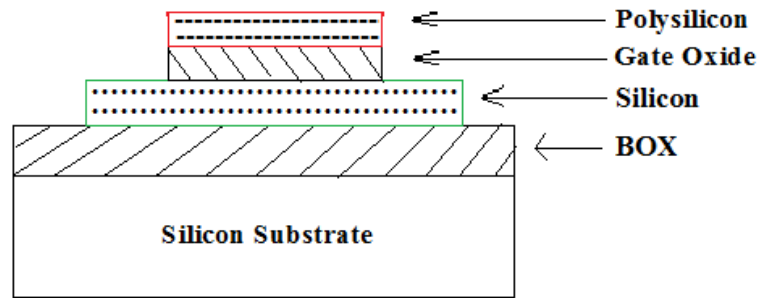
(c) Silicon device layer uniformly doped



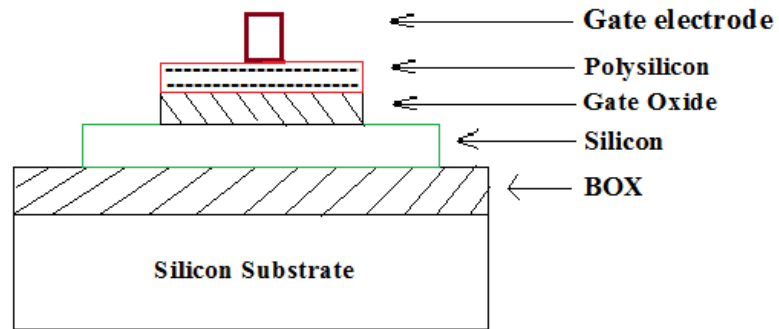
(d) After gate oxide growth and patterning



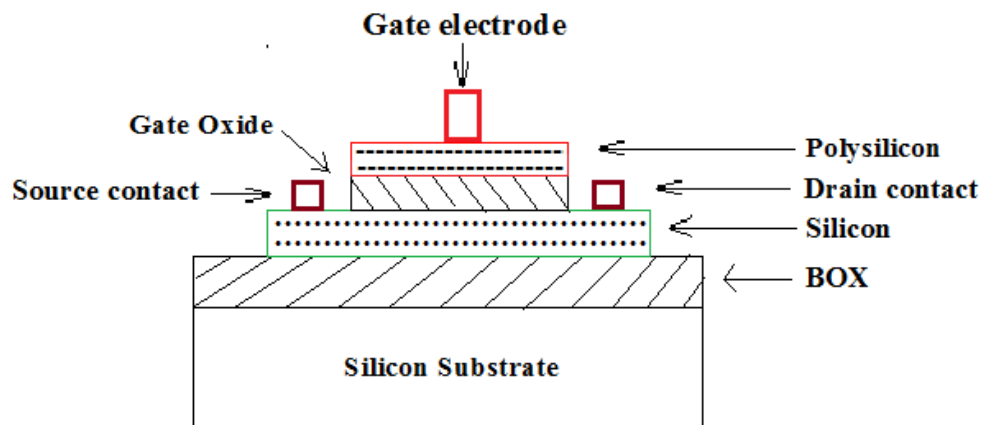
(e) After gate material deposition and etching



(f) After gate material doping annealing



(g) After gate electrode metal deposition and patterning



(h) After gate electrode deposition, patterning and contact holes etched

Figure 8.1: Two dimensional cross-sectional views after major fabrication steps of double-gate junctionless transistor (DGJLT).

The cross-sectional view of symmetric double-gate junctionless transistor is shown in Fig. 8.2.

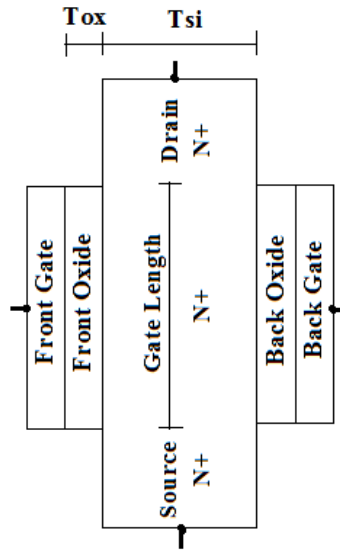


Figure 8.2: Crosssectional two dimensional view of n-channel symmetric double-gate junctionless transistor (DGJLT).

8.4 Results of process simulation obtained by Cogenda simulator

Fig. 8.3 shows the structure of DGJLT obtained after Cogenda process simulation. The figure also shows the different materials used in the structure with dimensions. The SOI wafer has substrate thickness of 100 nm and doped with p-type impurity having concentration $2 \times 10^{17} \text{ cm}^{-3}$. The buried oxide (BOX) above the substrate is 30 nm thick. The gate length (L) and gate oxide thickness (T_{ox}) considered are 10 nm and 3 nm respectively. The silicon thickness (T_{si}), width (W) and height (H) are all considered as 10 nm. Source and drain region lengths are 15 nm each. Depth of the shallow trench isolation (STI) is considered as 20 nm and the thickness of the inter-layer dielectric (ILD) dielectric is 100 nm. The thickness of semiconductor layer is kept very thin to have full depletion of carriers when the device is turned off. Also, the semiconductor is heavily doped to get a reasonable amount of current flow when the device is turned on. Putting these two constraints together forces the use of nanoscale dimensions and high doping concentrations.

In Cogenda, Gds2Mesh tool constructs 3D device models from planar mask layouts, according to a set of process rules and process parameters, and large through extruding 2D graphs to 3D objects. Process rules are central to Gds2Mesh, as they define how 3D objects are constructed from 2D graphs, how doping profiles are placed, and the mesh constraints. Each process is argued by a set of parameters. One can load a mask file in Gdsii format. Apart from loading a GDSII mask layout,

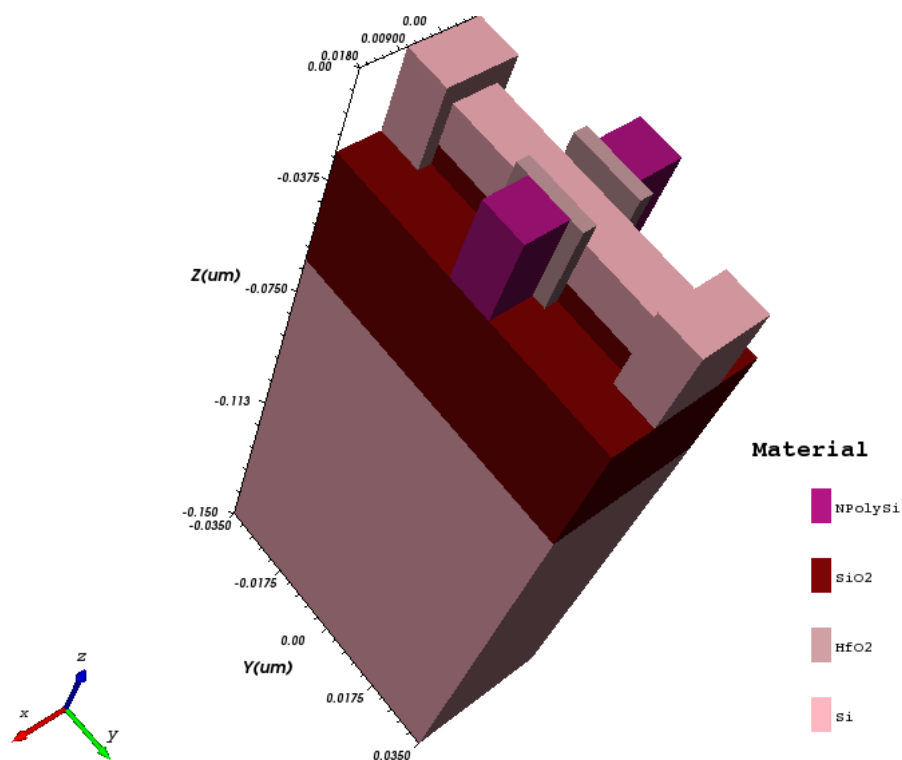


Figure 8.3: DGJLT structure from Cogenda process simulator.

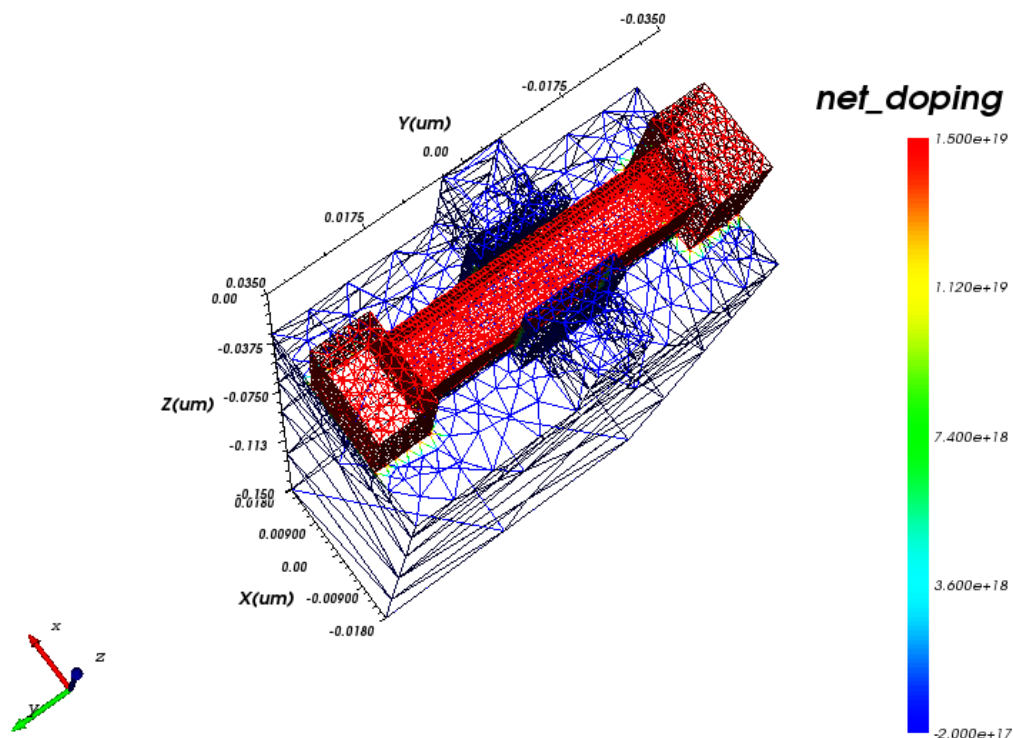
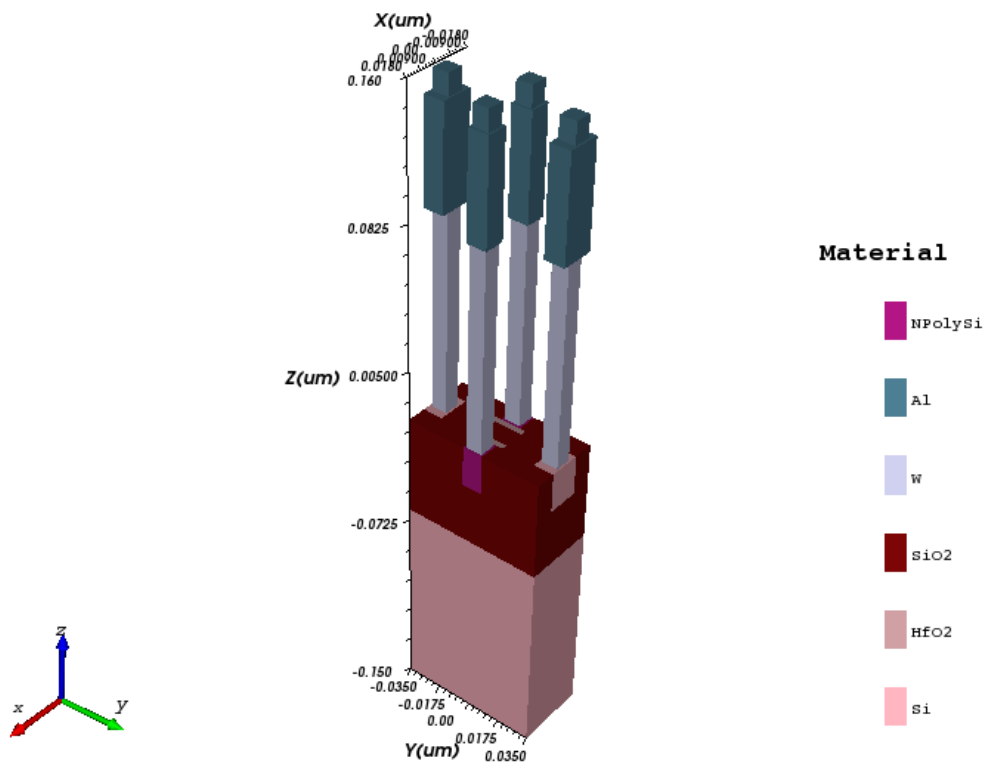
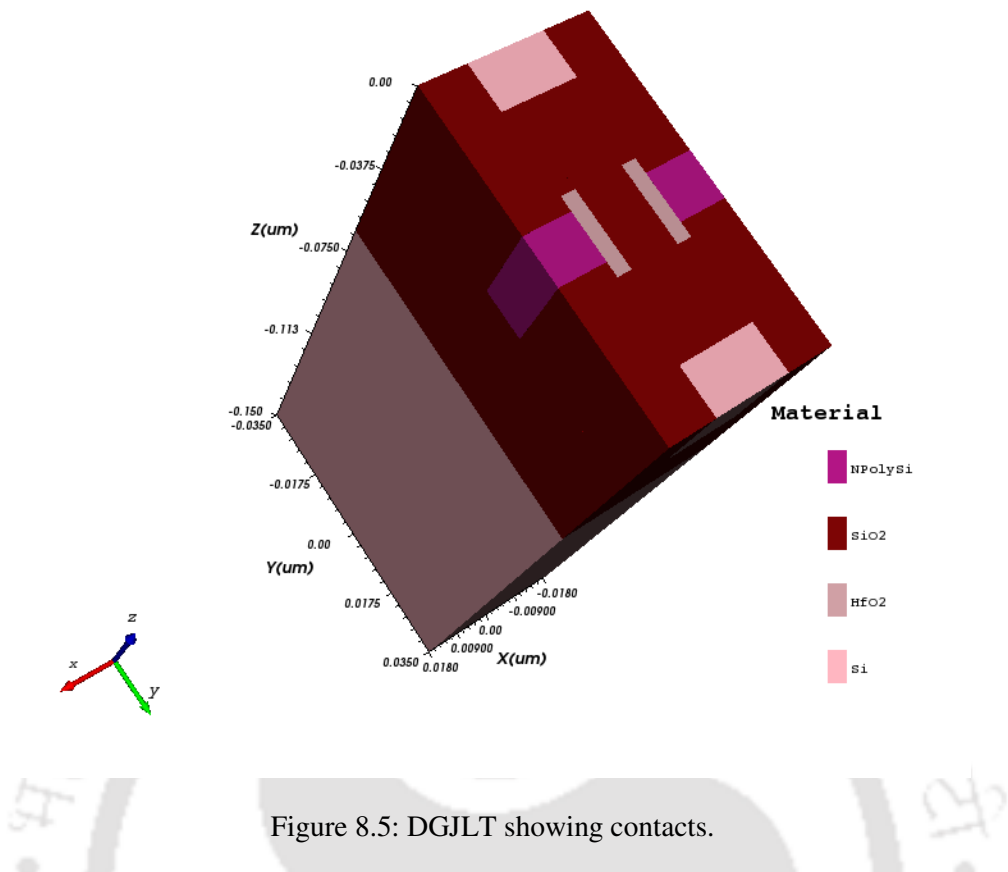


Figure 8.4: DGJLT with meshing and doping.



one can define simple masks with polygon items. In principle, Gds2Mesh is able to construct models of any circuit blocks fabricated with planar processes, as long as a suitable mask layout (GdsII file) and a process library (similar to CMOS013) are present. Figure 8.4 shows the meshing and doping concentrations for device simulation. Very fine meshing is desirable for accurate electrical characteristics. In Cogenda meshing as well as doping is also performed in Gds2Mesh.

Fig. 8.5 shows the device structure with contacts namely, source, drain and gate contacts. The two gates are shorted for symmetric operation (our case). The semiconductor and metal form ohmic contact here. Fig. 8.6 shows the final device structure with electrodes. Electrodes, composed of aluminium material are placed in contact window (w). Design rule length unit (lmd) lambda is 0.02 μm . Thickness of Metal 1 is 50 nm and thickness of Passivation above IMD2/Metal3 is 100 nm.

8.5 Electrical characteristic of the device so obtained from Cogenda simulator

The transfer characteristic (I_D vs. V_{GS}) of the DGJLT structure is shown in Fig. 8.7. Mobility model accounting for the dependence on the impurity concentrations well as the transverse and longitudinal electric field values is employed. Shockley-Read-Hall (SRH) recombination model is included in the simulation to account for leakage currents. Because of high channel doping concentration, Fermi-Dirac carrier statistics without impact ionization is utilized in the simulations. Band gap narrowing model (BGN) is also incorporated to take care of the band gap narrowing effect which may arise due to highly doped channel regions. HfO_2 is used as a gate oxide material with assumed permittivity of 22. Gate length and gate oxide thickness are taken as 10 nm and 3 nm respectively. Silicon doping

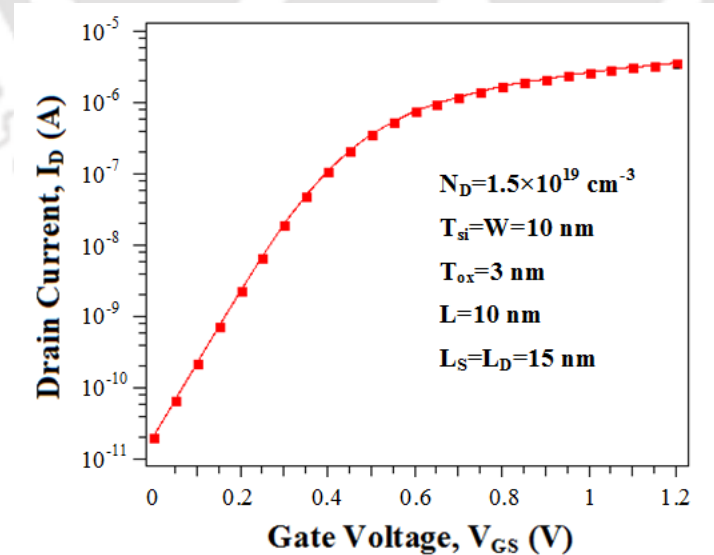


Figure 8.7: I_D versus V_{GS} characteristics of the structure for $T_{ox}=3$ nm, $N_D=1.5 \times 10^{19} \text{ cm}^{-3}$, $T_{si}=W=10$ nm, $L=10$ nm, source/drain lengths=15 nm at $V_{DS}=50$ mV and gate workfunction=5.4 eV.

concentration is taken as $1.5 \times 10^{19} \text{ cm}^{-3}$. The gate workfunction is considered as 5.4 eV. The detailed

code for process as well as device simulation used in this chapter is shown in appendix.

8.6 Summary

We have suggested possible fabrication steps for n-type double-gate junctionless transistor using 3D device and process simulator from Cogenda TCAD vendor. Transfer characteristic is extracted from the structure so developed from process simulation.



Chapter 9

Conclusions and Future Scope of the Work

9.1 Conclusion

Low power and high performance devices are in demand for today's microelectronics market. Recently, junctionless transistor has proven itself as a very promising device in this arena. The work carried out in this thesis was divided into three parts. The first part discusses about the analog and digital performances; process and temperature effects of a double-gate junctionless transistor. In the second part, the effects of the fringing fields on the device and circuit performances of a JLT are discussed. Different architectures to improve the analog performance of a JLT are examined with the help of extensive device simulations. An analytical channel potential model for shorter-channel dual-material gate DGJLT valid in subthreshold region is developed. Also, a semi-analytical electrostatic potential and a drain current model for single-material gate DGJLT are derived. Finally, the process simulation of DGJLT is carried out with the help of Genesis device simulator in the third part.

It is observed that

- Double-gate JLT show better device performance characteristics in terms of SCEs, G_m/I_D and intrinsic gain compared to its similar dimension IM counterpart and later device outperforms in terms of speed.
- DGJLT electrical parameters are more immune to channel length variations. However, there is a notable threshold voltage change of the device with silicon thickness compared to a JB device.
- Unlike JB MOSFET, overall performance of a DGJLT is not degraded much by increase in temperature and use of high-k gate dielectrics.
- Both n and p-channel DGJLT show similar performance trends in presence of high-k gate dielectrics and spacer dielectrics, unlike a TFET, where the trends are reported to be opposite.

For the improvement of transconductance of a DGJLT following structures/methods are adopted –

- Hetero-gate-dielectric DGJLT (HG-DGJLT) with spacers
- A dual-material gate DGJLT with high-k spacer (DMG-SP DGJLT)

- A dual material double-layer gate stack DGJLT (DM-DGS DGJLT)
- Germanium as an alternate substrate material to silicon

With the inclusion of high-k spacers on both sides of the gate oxide, controllability of gate terminal on the silicon region increases resulting improvements the SCEs as well (however, using appropriate gate workfunction, the I_{OFF} and I_{ON} can be traded with spacers). HG-DGJLT improves SCEs and f_T . DMG-SP DGJLT offers well improvement of transconductance. DM-DGS DGJLT performance in terms of G_m is inferior to DMG-SP DGJLT, however, its performance is marginally better than DMG DGJLT. While, germanium as substrate material offers better transconductance and f_T , silicon-substrate provides better SCEs. The potential model for dual-material gate; and the potential and drain current model for single-material gate DGJLT are in close agreement with professional TCAD simulation results for same device dimensions and bias conditions.

On a serious note, junctionless technology is already in use in semiconductor industries. In fact, all the new vertical NAND flash memories by Samsung, S K Hynix, Micronix use polysilicon junctionless transistors. For JLT to come in the mainstream technology node, following issues must be addressed. In a JLT, because of very high channel doping ($\sim 8 \times 10^{18} \text{ cm}^{-3}$ – $8 \times 10^{19} \text{ cm}^{-3}$), there is more threshold voltage variability with respect to doping concentration and silicon thickness compared to conventional junction-based MOSFET. This threshold voltage and transistor mismatches which will affect circuit performances. To control such high uniform doping throughout source-channel-drain region for small silicon thickness (~ 5 – 10 nm) and that too within cost limit is a challenge especially for non-planar kind of structure. Moreover, because of lower mobility of JLT compared to IM devices, makes it lesser suitable for high speed applications.

9.2 Future Scope of the Work

The findings presented in this work are mostly based on the simulation results including appropriate models. This helped us to arrive at a qualitative understanding of the device operation. More rigorous information can be obtained by full quantum simulations using either non-equilibrium green's function (NEGF) approach or Wigner-function approach. There is lot of scope for compact modelling for circuit simulation of shorter channel length JLT which includes all short channel effects like hot carrier effect, velocity saturation effect, drain induced barrier lowering effect etc. Designing circuits using these devices for low power applications is a fine scope of work. Also, implementation of the working models in spice simulator for circuit simulation is another scope for extending the thesis work. Studying the reliability issues in DGJLT and developing compact models with reliability issues in the model is excellent scope of research. Co-implementation of junctionless and organic transistors is another scope of research which is expected to have bunch applications in extreme low power applications. Also, junctionless tunnel FETs has immense potential towards low power circuit design applications.

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List of Publications

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- Ratul Kr. Baruah, Roy P. Paily, “Impact of High-k Spacer on Device Performance of a Junctionless Double-Gate Transistor”, *Journal of Computational Electronics*, Springer, vol. 12 pp. 14–19, 2012.
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