



INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI
SHORT ABSTRACT OF THESIS

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SHORT ABSTRACT

In advanced CMOS process, the device performance characteristics gets affected by changes in the number of fingers due to shallow trench isolation effect, which in turn changes the circuit performance. A systematic design procedure based on g_m/I_D , g_{mb}/I_D and normalized current (I_D/W) characteristics is presented. This methodology is used to evaluate the device geometry by considering the number of fingers which meets the desired specifications. A PVT intensive bulk-driven OTA with improved gain is introduced, which is able to work under sub-0.5 V supply voltage. The gain of the bulk-driven input stage is improved with cross-coupling of active load transistor bulk-terminals. An additional cross-forward stage assists in increasing the gain of second stage. The cross-forward also improves the driving capability of OTA without any stability issue. An ultra-low-voltage pseudo-differential bulk-driven OTA with rail-to-rail input/output swing is presented for low-frequency applications. The proposed design employs an auxiliary circuit at input stage to improve the effective transconductance of bulk-driven input stage. The enhanced transconductance leads to improvement in gain and gain-bandwidth product of OTA. In addition, a Class-AB output stage is designed through a cross forward stage which improves current efficiency and gain of the amplifier. The proposed design operates at supply voltage of 0.3-V and total current consumption is 170 nA.

The drive strength of bulk-driven device is very less as compared to gate-driven counterparts which shows the effect on the slew rate of OTA. The power-efficient bulk-driven Class-AB operational transconductance amplifiers are presented for driving the large capacitive loads under low-voltage environment. The proposed OTAs employ adaptive biasing and adaptive loads to improve the slew rate. In addition, a slew rate enhancer (SE) is employed to further improve the dynamic performance. The SE circuit consists of current-feedback loop which recursively copies the part of output driving current and increases the bias current of SE. The intended capabilities and advantages of the proposed designs are verified through post-layout simulations. A final evaluation of the performance of the proposed OTAs compared with the state-of-the-art designs.