



Abstract

The work carried out in this thesis is divided into three parts. The first part discuss the study on carbon nanotube (CNT) interconnects. The second part will be dealing with the modeling of CNT based transistors and design of analog circuits based on CNTs. The final part will present the fabricated thin film transistors based on single walled carbon nanotubes (SWCNTs). The study on the SWCNT interconnects is focused on the estimation of their magnetic inductance at various bias voltages. The analysis of magnetic inductance is carried out for the ground-signal-ground (GSG) configuration of SWCNT based interconnects having various dimensions and different percentage of metallic SWCNT (m-SWCNT) purities. The results indicate a variation in the loop inductance value as high as 34% for closely spaced semi-global interconnects.

The study on the SWCNT transistor modeling aims to develop closed-form equations for the drain current and drain to source voltage for CNT field effect transistor (CNFET) in terms of its dimensions. Although these proposed models are based on curve fitting method, they provide a quick first order numerical estimate of drain current and drain to source voltage of the CNFET. The estimated values of the current and voltage using the proposed equations are in close agreement when compared to a SPICE compatible model and measured results of a fabricated device. The CNFET based analog circuits such as common source amplifiers and differential amplifier are designed using the proposed equations. The simulation results shows a better performance of the CNFET amplifiers in terms of the DC gain and gain band width product at the same power power consumption when compared to the conventional CMOS counterparts. A study on the performance of CNFET amplifiers for parameter variations like diameter, spacing and number of CNTs are also presented.

The final and major part of thesis presents the fabrication and characterization of various types of semiconducting nanotube thin-film transistors (SN-TFTs). Nine dif-

ferent SN-TFTs of various dimensions having HfO_x or SiO_2 as gate dielectric material, consisting of global, local, top or dual gate structures with the thin-film of 90% or 95% purity of semiconducting SWCNT (s-SWCNT) fabricated under similar process conditions are investigated. The wafer scale SN-TFTs consisting of nanotubes of 95% enriched s-SWCNTs have demonstrated a higher on-off current ratio compared to the devices with 90% purity s-SWCNTs. A technique to deposit the nanotube thin-film of densities 40-45 SWCNTs/ μm^2 over the silanized HfO_x surface was introduced for the first time. The HfO_x based global back gate SN-TFTs have shown a lower threshold voltage, higher current density and higher mobility compared to the SiO_2 based devices. The HfO_x based local back gate SN-TFTs are fabricated on wafer scale and devices have exhibited the lowest threshold voltage, steeper subthreshold slope, higher current density and higher mobility compared to other reported devices. The dual gate SN-TFT has shown steepest subthreshold slope among the reported SN-TFTs and has a higher mobility and a lower threshold voltage compared to single gate SN-TFTs.