INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI
SHORT ABSTRACT OF THESIS

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SHORT ABSTRACT

Technology advancement in the area of IC design allows billions of transistors to be on a single chip, which allows the developments of the modern days' chip multiprocessors with larger core counts (in range of 100 cores or more). The increased core count in a chip multiprocessor urges the necessity of the high bandwidth memory, and high-speed on-chip interconnects. To fulfill the needs of the chip multiprocessors, many future generations on-chip interconnects as well as memory designs have been proposed.

Once the chip multiprocessor is fabricated, we need to use it efficiently. Therefore, to utilize the capabilities of the chip multiprocessors and get the best possible performance, application mapping emerged as a prominent area in the domain of chip multiprocessor research. In the past, application mapping on to the chip multiprocessors has mainly considered the task to core mapping, and not the data to memories, as on-chip memory was smaller (in megabytes). However, for the current as well as future generation chip multiprocessors where modern network-on-chip organizations and 3D-stacked memories have been proposed, investigating the impact of the application mapping and associated data placement becomes crucial.

Therefore, this thesis proposes the techniques to efficiently map the applications on to the chipmultiprocessors considering the different current as well as future architectural design variations of the chip multiprocessor systems to improve the system performances. Specifically, we consider the following current as well as future CMP architecture designs in terms of memory and NOC.

- 3D-stacked memory: In this architectural design, we consider a large main memory which is placed on top of the processor layer in a 3D-stacked manner. This main memory can be of type-DRAM only, DRAM along with SRAM buffer, DRAM as a cache, DRAM as a cache along with the SRAM buffer, and DRAM-PCM based hybrid memory.
- NOC: In this architectural design, we consider an on-chip interconnection network between the cores of the CMP which is either a 2D-mesh organization of the electrical interconnects (termed as 2D-mesh NOC), or a combination of electrical as well as optical interconnects (termed as hybrid NOC).