



INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI  
SHORT ABSTRACT OF THESIS

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**SHORT ABSTRACT**

Power Distribution has become a challenging issue in System-on-Chip (SoC) design. Generally, a power grid network is created for the distribution of power from the power pads to all the underlying functional blocks. During the process of power distribution, the power grid lines suffer from IR drop and electromigration (EM) issues. Existing methods of designing power grid are time-consuming as it checks for IR drop and EM violations over many iterations of the design cycle. Therefore, in this thesis, solutions to overcome these power grid design challenges are presented using AI/ML approaches. In the first work, a probabilistic solution for the power grid analysis problem is proposed, with which voltages of the circuit nodes can be obtained efficiently. The proposed solution is faster with the same level of accuracy than its previous works. In the second work, design space exploration (DSE) for obtaining critical optimum power grid design is proposed using a heuristic approach. From which, optimum IR drop and metal routing area are obtained using evolutionary computation-based heuristic approach. In the third work, machine learning approaches are used for the power grid design problem. This work aims to predict the power grid interconnect widths of all interconnects while satisfying certain constraints. The proposed work achieves a significant speedup over the traditional approach with an acceptable accuracy limit. In the final work, a method for electromigration-aware lifetime prediction of the power grid network is presented during the design time using a machine learning technique. The presented method is faster than the state-of-the-art aging prediction models and closest to the accurate state-of-the-art physics-based model. Overall in this thesis work, it is demonstrated that AI/ML approaches can be a good alternative for the traditional power grid design approaches, which is fast and can speed up the overall design cycle for future intricate SoC design.