**Investigations on Noise Cancellation and Linearity Improvement in Low Power LNAs and Receivers**




***Indrajit Das***

# Investigations on Noise Cancellation and Linearity Improvement in Low Power LNAs and Receivers

*A*

*Thesis submitted*

*for the award of the degree of*

**DOCTOR OF PHILOSOPHY**

By

**INDRAJIT DAS**


DEPARTMENT OF ELECTRONICS AND ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI

GUWAHATI - 781039, ASSAM, INDIA

SEPTEMBER 2021

# Certificate

This is to certify that the thesis entitled "**Investigations on Noise Cancellation and Linearity Improvement in Low Power LNAs and Receivers**," submitted by **Indrajit Das** (146102003), a research scholar in the *Department of Electronics and Electrical Engineering, Indian Institute of Technology Guwahati*, for the award of the degree of **Doctor of Philosophy**, is a record of an original research work carried out by him under my supervision and guidance. The thesis has fulfilled all requirements as per the regulations of the institute and in my opinion has reached the standard needed for submission. The results embodied in this thesis have not been submitted to any other University or Institute for the award of any degree or diploma.

Date:

Dr. Nagarjuna Nallam
Assistant Professor
Dept. of Electronics and Electrical Engg.
Indian Institute of Technology Guwahati
Guwahati - 781 039, Assam, India.

Dedicated to

**My Family**

# Acknowledgements

Even though I kept this section for the last, I must say its significance is no less! This section is about a journey that has become a part of my life over the past few years. To summarize in a sentence, my PhD journey was full of ups and downs; it was challenging at times and indeed fulfilling at others! During this period, I have had the opportunity to interact with many people who have helped me in various ways, sometimes directly and sometimes indirectly. It would be sheer injustice to not mention these people because they all had their influence on the way the last few years were.

First, I would like to thank my supervisor Dr. Nagarjuna Nallam, for guiding me through my PhD journey. I thank him for providing me an opportunity to work under him. The most important thing that I have tried to learn from him is perseverance and dedication. I thank him for the numerous technical discussions that we had over the years, which have helped me improve my logical thinking abilities. There were times when research ideas have failed to materialize, leading to disappointments. I thank him for being there with me during those times and consistently trying to motivate me in various ways. I sincerely thank him for all his efforts to make this thesis possible! I would like to thank my doctoral committee members Prof. Roy P. Paily, Prof. Rakhesh Singh Kshetrimayum, and Dr. D Pamu, for their valuable suggestions on my research work. I would also like to thank the EEE department staff for their help in various paperwork from time to time.

I would like to thank my PhD lab mates Kamlesh and Prateek for being co-passengers of this journey. They were the go-to people for me whenever I was stuck with any kind of technical issues starting from simulations to measurements. Together, we have spent many late nights in the lab, especially during the times of tape-out. I thank them for all the uncountable bits of help during these years. I must say, I also have got inspired by them in many ways from time to time. Apart from our lab times, the times we have shared over a coffee or over lunch are also memorable. Kamlesh, your birthday celebrations can't be forgotten for all the right and the wrong reasons! I also thank my other friends from the department Rahul bhai, Pralay, Vimal, Tasleem, for their valuable time. I thank the seniors for their guidance and various suggestions. I must say, the various technical discussions that I had with Hari bhaiya, Saroj da, and Vinay bhaiya have helped in many ways.

Then comes my group of people, who fortunately were all from other departments. The best thing is that it ensured that we would discuss everything other than PhD whenever we meet. That was like a breath of fresh air, which helped me remain fresh even during tough times. First, I have to mention Siddhanta and Gundappa, with whom I share such a good bonding, something that we expect to retain for years to come. All the good times

spent together, the trips, and parties shall remain as memorable highlights of my Guwahati chapter. With people like Omkar, Kabiraj, and Gundappa, even failed bike trips are unforgettable. It's because of Pradip that many musical explorations happened. Thanks to Gundappa and Siddhanta for being partners in those experiences. Pixelate can't be forgotten! Thanks to Kundan and Jumi for the quality times. Apart from that, Sreeja, Sohenii, Arnab da..and the list continues to grow! The contribution of these people is immense to my well-being at IITG.

Finally, comes the people who are the closest to heart, my family! I do not really know how to acknowledge the contribution of my parents, Mr. Bijoy Kumar Das and Mrs. Santana Das, in making me who I am today. Thanks for all the love and support during the difficult times. I would like to thank my elder brother Dr. Arindam Das for inspiring me in various ways over the years. Thanks to boudi Samipa Das and bhaipo Ahan (and Ayansh now) for giving me updates about various family events and festivals that I might have missed attending. Finally, thanks to Ms. Megha for her constant support throughout these years. I might not be able to thank you enough for all the positive changes you have brought to my life! Thanks for being there through thick and thin!

*Indrajit Das*

# Abstract

Thermal noise-canceling radio-frequency (RF) circuits are available in the literature for more than two decades now. Yet, no systematic methodologies are available to analyze and design these noise-canceling circuits. The main objective of this thesis is to develop a generic theory of noise-canceling circuits and use it in the analysis and design of new noise-canceling circuits. A feedback-based noise-canceling model is developed as part of this work to explain the operation of existing noise-canceling circuits. The proposed model is validated through the analysis, design, and simulation of known noise-canceling low-noise-amplifiers (LNAs) and receivers. Further, a new systematic methodology to generate all multi-transistor noise-canceling circuits is developed in this thesis.

Based on the proposed methodology, the thesis also develops a few new noise-canceling circuits. One such circuit is a low-power partial noise-canceling complementary common-gate (CG) LNA. The performance of the LNA is further improved using a complementary linearization technique. The LNA effectively uses low-power techniques around a CG structure to reduce the power consumption by four times for a given input impedance. The complementary transistors are appropriately designed with optimum biasing to achieve linearization within the circuit. A prototype of the proposed LNA is implemented in a standard 180 nm complementary metal-oxide-semiconductor (CMOS) technology. Laboratory measurements show that the LNA has an input third-order intercept point (IIP3) $> 0$ dBm from 0.1-to-1 GHz while consuming only 0.735 mW of dc power in the high-linearity mode of operation. In the low-noise mode of operation, the LNA has a minimum noise figure (NF) of $3.41$ dB while consuming $1.2$ mW of dc power. The proposed LNA achieves one of the best figure-of-merit (FOM) among all existing low-power inductorless wideband LNAs in the literature.

Due to its low-power, low-noise, and high-linearity characteristics, the proposed complementary common-gate (CCG) amplifier can also be used as a baseband amplifier in receivers. In this work, a low-power N-path mixer-first receiver is designed using the proposed CCG amplifier as a trans-impedance amplifier (TIA). A prototype receiver is implemented in a 180 nm CMOS process. The receiver operates from 0.3 to 1.3 GHz with a conversion gain of $21.9$ dB. In measurements, the receiver achieved an in-band (IB) IIP3 of $+7.2$ dBm

and a noise figure of $5.8$ dB while consuming $0.34$ mW power per TIA at $1$ GHz. The measured spurious-free dynamic range (SFDR) at $1$ GHz is $76.9$ dB. Overall, the mixer-first receiver presented in this work achieved a good in-band SFDR while consuming the lowest static power.

# Contents

# List of Figures

# List of Tables

# 1

# Introduction



## Contents

## 1.1 Introduction

The usage of wireless communication systems, such as mobile phones, has increased exponentially over the last few decades. With every new generation of radio access technology (RAT), there is a continuous rise in the performance requirements, such as sensitivity, linearity and blocker tolerance of a radio frequency (RF) front-end [1]. The power consumption of modern RF front-ends is also rising to meet these high-performance requirements. Another important requirement of a modern radio receiver is the support for multiple communication standards that are spread across the frequency spectrum. One possible way to support multiple frequency bands is to use several dedicated narrow-band radios in parallel [2]. Alternatively, a wideband low noise amplifier (LNA)-based architecture, such as the one shown in Fig. 1.1 [3–5], can also be used for this purpose. In Fig. 1.1, the LNA operates over a wide range of frequencies. The receiver can be tuned for a specific communication standard by varying the LO frequency and baseband (BB) filter bandwidth. The sensitivity of this wideband receiver largely depends on the noise performance of the LNA. If the LNA is designed to have a high gain, the noise contribution of the subsequent stages can also be minimized. Wideband LNAs can be designed with [6–11] or without inductors [12–20]. Inductorless wideband LNAs [12–20] are preferred in integrated receivers because of their small area.

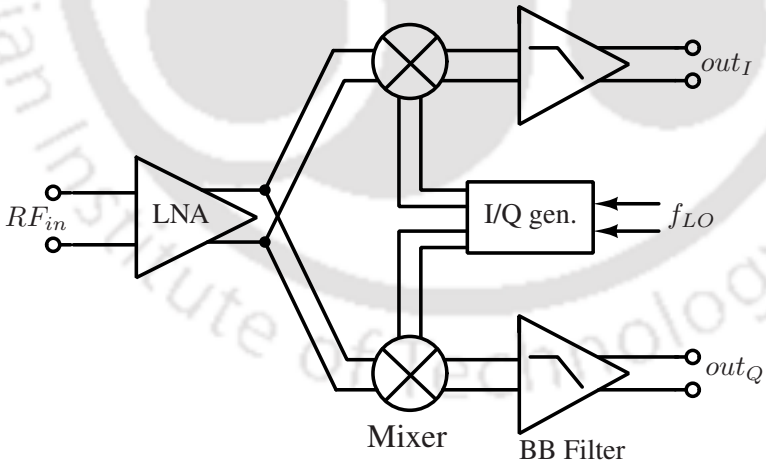



**Figure 1.1:** Block diagram of a wideband direct-conversion receiver chain.

In order to achieve high-performance, the RF front-ends typically require high power. However, portable electronic devices need to operate within a stringent power budget to enhance battery life. Typically, two types of power consumption are associated with a radio receiver [3–5, 21–27]: dynamic and static. The dynamic power consumption is due to the clock buffers driving the mixer switches, while the static power consumption is due

to the RF LNA and the baseband low pass filter. In radio receivers, the dynamic power consumption depends on the supply voltage and the node parasitic-capacitances. With technology scaling, both supply voltage and node capacitances are reduced, and thus the dynamic power consumption is also minimized. The static power consumption in an RF front-end constitutes a significant portion of a receiver's total power budget [4, 28–32]. The objective of this thesis is to improve the noise and linearity performance in low-power wideband LNAs and receivers.

The rest of this chapter is organized as follows. A brief introduction to LNAs is provided in section 1.1.1, followed by a review of low-power wideband LNAs and their limitations. Section 1.3 provides a performance comparison of low-power LNAs. Section 1.4 provides the problem formulation and organization of the thesis is described in section 1.5.

### 1.1.1 Introduction to LNAs

An LNA has to amplify the received signal of power level $-80$ to $-100$ dBm while adding as low thermal noise as possible. The LNA input impedance should be matched with the antenna impedance to minimize reflections at the antenna-LNA interface. The noise performance of an RF circuit is characterized by a parameter called noise factor (F). The noise factor of a circuit is defined as the ratio of input signal-to-noise ratio (SNR) to the output SNR [12]. Hence,

$$F = \frac{SNR_i}{SNR_o}, \tag{1.1a}$$

where $SNR_i$ and $SNR_o$ are the input and output signal-to-noise ratios, respectively. Noise figure (NF) is noise factor expressed in decibels (dB), i.e., $NF\ (dB) = 10 \times log_{10}(F)$. Fig. 1.2 shows the block diagram of an LNA with its input and output signal and noise. Let $S_i$ and $N_i$ represent the signal power and noise power at the input of the LNA. Similarly, $S_o$ and $N_o$ represent the signal power and noise power at the LNA output. Both signal and noise at the input get amplified by the gain of the LNA, which is $G$. Additionally, the amplifier adds its own noise $N_a$ at the output. Hence, the noise factor, given in equation (1.1a), can be represented as

$$\begin{aligned} F &= \frac{(S_i/N_i)}{(S_o/N_o)} \\ &= \left(\frac{S_i}{S_o}\right).\left(\frac{N_o}{N_i}\right) \\ &= \frac{1}{G} \cdot \frac{GN_i + N_a}{N_i} \\ &= 1 + \frac{N_a/G}{N_i}. \end{aligned} \tag{1.2a}$$

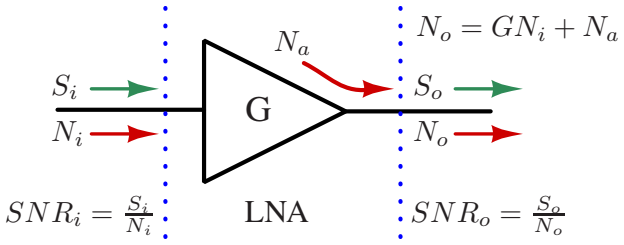



**Figure 1.2:** An LNA with its input and output signal and noise.

From equation (1.2a), one needs to increase gain and reduce the noise added by the amplifier to minimize the noise factor. Hence, an LNA should provide sufficient gain to the incoming RF signals while adding very low noise of itself.

Apart from the gain and noise factor, linearity is another essential property of an LNA. When a large signal is applied to the input of an amplifier, signal compression occurs because of device nonlinearity. Signal compression is characterized using the parameter 1-dB compression point (P1dB), which is the input signal level for which the gain falls by 1 dB [12]. Additionally, when input tones of two or more frequency components are applied to the input of the amplifier, third-order intermodulation (IM3) components are generated [12]. If the amplitudes of the input tones rise, the IM3 products increase sharply. Input third-order intercept point (IIP3) is an estimate of the input power level for which the fundamental and the IM3 components at the output become equal [12].

### 1.1.2 Wideband LNAs

Two well-known wideband LNAs are resistive shunt feedback (RSF) LNA and common-gate (CG) LNA. Fig. 1.3(a) shows the circuit diagram of a CG LNA. In the circuit shown in Fig 1.3(a), $R_s$ is the source resistance, and $R_1$ is the load resistance. Let $g_{m1}$ represent the transconductance of M1. The input impedance of the CG LNA is equal to $1/g_{m1}$ (if channel-length modulation and body effect are neglected) [12]. One has to choose $g_{m1} = 1/R_s$ to provide appropriate input matching. The noise factor of the CG LNA (denoted as $F_{CG}$) can be derived as

$$F_{CG} = 1 + \gamma_m + 4\frac{R_s}{R_1}, \tag{1.3a}$$

where $\gamma_m$ is the themal noise coefficient of a MOS transistor. If $R_1$ is designed such that $4R_s/R_1 \ll 1$, equation (1.3a) reduces to $F_{CG} \approx (1 + \gamma_m)$. Even in that case, the NF of a CG LNA reaches 3 dB (for $\gamma_m \approx 1$).

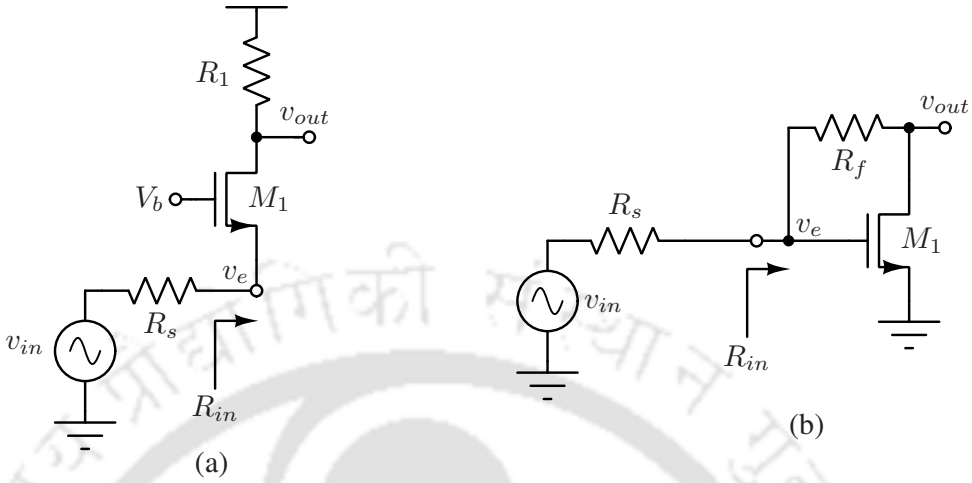



**Figure 1.3:** (a) a common-gate LNA [12], (b) A resistive shunt feedback LNA [12].

Fig. 1.3(b) shows the circuit diagram of a resistive shunt-feedback (RSF) LNA. In the circuit shown in Fig 1.3(b), $R_s$ is the source resistance, and $R_f$ is the feedback resistance. Let $g_{m1}$ represent the transconductance of the MOS transistor M1. The input impedance of the circuit is equal to $1/g_{m1}$ (if channel-length modulation is neglected) [12]. Under the condition for input matching, $g_{m1} = 1/R_s$. The noise factor of the RSF LNA ($F_{_{RSF}}$) is given by

$$F_{_{RSF}} = 1 + \gamma_m + \frac{4R_s}{R_f}. \tag{1.4a}$$

For $\gamma_m \approx 1$, the NF of the RSF LNA exceeds 3 dB even if $4R_s/R_f \ll 1$.

In the two wideband LNAs discussed, the matching device's $g_m$ is decided by the input impedance requirement and cannot be increased arbitrarily. Hence, the input impedance and NF of an inductorless wideband LNA are tightly coupled with each other.

## 1.2 Low power wideband LNAs and their limitations

Section 1.1 highlighted the importance of low power operation in RF receiver front-ends. This section gives an overview of existing low-power techniques for the design of wideband LNAs and highlights their limitations. Different low-power design techniques have been categorized into three main sub-categories, such as- current-reuse technique, $g_m$-boosting technique, and sub-threshold or low supply-voltage design.

### 1.2.1 Current-reuse technique

Sharing the same DC current among multiple input transconductors is a frequently-used technique to achieve low power operation. This technique, referred to as current-reuse, has been used to design various low-power wideband LNAs [33–44] in the literature. Fig. 1.4(a) and 1.4(b) demonstrate the use of the current-reuse technique in a resistive shunt-feedback LNA [33, 36, 38, 42] and a common-gate LNA [39], respectively. In the circuits shown in Fig. 1.4, the LNA's effective transconductance is the sum of the pMOS and the nMOS transconductances. As a result, the effective transconductance gets doubled for a given DC current. [34] employed a CG amplifier with active feedback where the CS feedback stage reuses the same DC current of the input transistor. A current-reused CG LNA with shunt and series peaking technique is adopted in [35] to achieve ultra-wideband operation at low-power levels. A complementary current-reuse with a tunable active shunt-feedback scheme is used to design an ultra-low-power (ULP) wideband LNA in [40]. In [40], the input transistor reuses the feedback stage's current to improve the current efficiency of the designed LNA. [41] used low-current active feedback in a complementary current-reuse RSF LNA to reduce the power consumption.

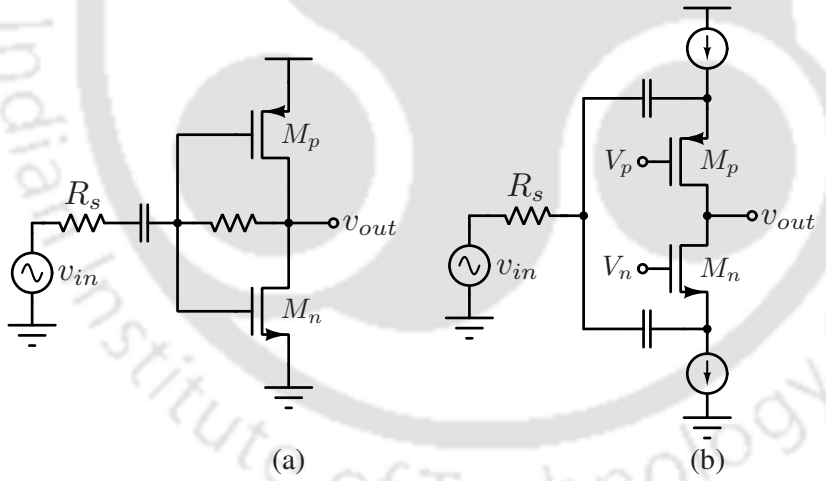



**Figure 1.4:** Current-reuse technique in (a) a resistive shunt feedback LNA [33] and (b) a common-gate LNA.

### 1.2.2 $g_m$-boosting technique

In a $g_m$-boosting technique, the effective $g_m$ of the input transistor is increased compared to a CG amplifier biased with a given DC current. This technique can reduce the power level needed to achieve the input match while simultaneously improving the noise factor. In literature, the $g_m$-boosting technique has been employed to design various low-power LNAs [36, 37, 42, 45–52]. Fig. 1.5(a) shows the capacitor cross-coupled $g_m$-boosting technique [45–47, 50] in a fully differential CG LNA. As shown in Fig. 1.5(b) [48], an inductive transformer can

be used to achieve higher $g_m$-boosting at no additional power. However, transformer-based $g_m$-boost requires a large silicon area and results in a narrow band operation. Another possibility is to use active $g_m$-boost based on a CS amplifier [53, 54], as shown in Fig. 1.5(c). [51] demonstrated the effect of back gate control in an active boost CG LNA to achieve low power consumption. The LNA in [36] employed capacitor cross-coupling along with positive-negative feedback to achieve low power consumption. [52] employed a triple cross-coupling technique to design an ultra-low-power CMOS LNA for WPAN applications. [42] used current-reuse negative feedback on a $g_m$-boosted CG structure to design a low-power LNA for sub-GHz applications.

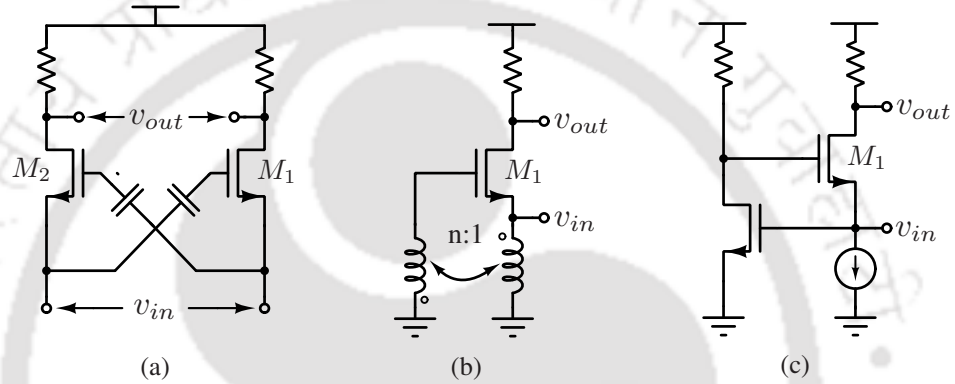



**Figure 1.5:** (a) A capacitor cross-coupled differential CG LNA [45–47]. (b) Transformer based $g_m$-boost [48]. (c) CS based active $g_m$-boost [53].

### 1.2.3 Sub-threshold and low supply-voltage architectures

Apart from the discussed techniques, another possible way of achieving low-power is to adopt a sub-threshold design [52, 55] or use a low supply voltage [38, 39, 56]. [55] employed sub-threshold biasing to achieve low-power operation while utilizing the Miller effect for wideband input matching. [57] employed sub-threshold biasing along with gain-boosting to a folded cascode structure to design a low-power LNA. A forward body biasing (FBB) technique is employed in [56] to achieve low-power wideband input impedance matching at a low supply voltage of 0.5 V. An ultra-low-voltage (ULV) operation with an inductive series peaking in the feedback path is employed in [38] to design a low-power ultra-wideband (UWB) LNA. [39] demonstrated the importance of FBB to improve the intrinsic gain in ULV circuits with no additional power consumption. FBB and a complementary current-reuse technique are used to design an ultra-low-power (ULP) wideband LNA at a supply voltage as low as 0.4 V [39]. [58] employed body floating with self-bias technique to reduce the threshold voltage ($V_{Th}$) of the MOS transistor to achieve low-power operation in a wideband LNA.

### 1.2.4 Summary of existing low-power techniques and their limitations

Tab. 1.1 presents a brief summary of existing low-power LNAs in the literature.

**Table 1.1:** Performance summary of existing low-power LNAs in the literature

| | Low-power Techniques | Inductor present? | Operating Freq. (GHz) | Gain (dB) | 3-dB BW (GHz) | NF (dB) | IIP3 (dBm) | Power (mW) |
|---|---|---|---|---|---|---|---|---|
| Access 2021 [54] | Multi-mode LNA with $g_m$-boosting | No | – | 16.8 | 4 | 6.6 | $-16.4$ | 0.35 |
| | | No | – | 19.4 | 5.2 | 5.4 | $-16.8$ | 0.9 |
| ISCAS 2018 [42] | $g_m$-boosted CG + current-reuse negative feedback | No | $0.04-0.8$ | 14.27 | 0.76 | 6.5 | $-5.74$ | 0.49 |
| MWCL 2017 [52] | Sub-threshold operation + triple cross-coupling | No | $0.4-1$ | $15.5-18$ | 0.6 | 4.2 | $-14$ to $-21$ | 0.2 |
| ISLPED 2017 [51] | Back gate control + active boost CG | No | $0.45-6$ | 16.8 | 5.55 | 7.3 | $-16$ | 0.3 |
| TMTT 2016 [40] | Current-reuse + tunable active shunt-feedback | No | $0.1-2.2$ | 12.3 | 2.1 | $4.9-6$ | $-9.5$ | 0.4 |
| AICSP 2014 [36] | Capacitor cross coupling + positive negative feedback | No | $0.5-2.5$ | 15 | 2 | $3.9-5$ | $+3.1$ | 0.91 |
| MWCL 2021 [58] | Body floating + Self-bias technique | Yes | $2.3-9.1$ | 9.4 | 6.8 | 3.89 | $-6.8$ | 1.36 |
| TCAS-II 2020 [44] | Forward body bias + negative feedback capacitor | Yes | $2.4-3.35^{\star}$ | 10 | $0.95^{\star}$ | 4 | 0 | 0.6 |
| MWCL 2020 [59] | Gate-source transformer feedback | Yes | $21.2-24$ | 19.1 | 2.8 | 3.6 | $-31$ | 0.99 |
| TCAS-II 2019 [60] | Forward-body-bias + self-balanced pseudo resistor | Yes | $2.26-2.56^{\star}$ | 10.4 | $0.3^{\star}$ | 3.46 | $-8.4^{\dagger}$ | 1.31 |
| JSSC 2016 [39] | Current-reuse + forward body biasing | Yes | $0.6-4.2$ | 14 | 3.6 | 4 | $-11.5$ to $-9.5$ | 0.25 |
| TVLSI 2015 [38] | Current-reuse + low voltage + inductive series peaking | Yes | $0.1-7$ | 12.6 | 6.9 | $5.5-6.5$ | $-6$ to $-9$ | 0.75 |
| MWCL 2014 [37] | Current-reuse + $g_m$-boosting | Yes | $2.3-2.6$ | 14.7 | 0.3 | 4.8 | $+2$ | 0.58 |
| RFIC 2011 [43] | Current-reuse + forward body biasing | Yes | $2-2.3$ | 13.9 | 0.3 | 5.14 | $-9.3$ | 0.21 |

$\star$ Estimated from figures, † Estimated from IIP3 = IIP1 + 9.6 dB

From Tab. 1.1, most of the existing low-power LNAs either have a suboptimal noise figure or suffer from poor linearity performance. The LNAs presented in [38, 40, 42, 43, 51, 54] achieve sub-mW power levels but at the expense of degraded noise and linearity performance. The LNAs in [39, 52, 58–60] offer a moderate NF but suffer from a poor linearity performance. Moreover, the circuit in [60] contains multiple inductors and has a low 3-dB bandwidth (BW). The resistor feedback technique in [36] helps to achieve a good linearity performance;

however, the design procedure of the LNA is more involved due to the positive feedback. The work presented in [37] also achieves a good linearity performance but requires an inductor to tune-out the output capacitance and has a low 3-dB BW. [44] achieves moderately good NF and linearity at low power levels, but requires multiple inductors for its operation.

As discussed in section 1.1.1, the NF of an LNA is a measure of the additional noise that the LNA adds to the incoming RF signal. Typically, NF needs to be as low as possible to maintain a good output SNR at a certain power budget. In inductorless wideband LNAs, the NF and the input impedance matching are tightly coupled with each other [12]. Consequently, one cannot choose an arbitrarily high value of transconductance to achieve an improved noise performance since that would degrade the input matching as well. $g_m$-boosting can relax the trade-off between the input matching and NF to some extent [45–48, 53, 54]. However, the amount of advantage obtained in NF is fixed in the case of a capacitor cross-coupling technique [45–47]. Higher $g_m$-boost can be obtained by employing an active boost technique [53, 54]; however, additional power consumption is required for the boosting amplifier, which makes it less suitable for low-power applications. Furthermore, the extra noise contributed by the active boost stage reduces the NF advantage to some extent. The input transistors of the LNA may be biased in the sub-threshold region to reduce power consumption. However, sub-threshold operation typically leads to a degraded noise performance. All this makes achieving low NF at low power levels a challenging problem.

The relation between nonlinearity and power consumption needs further discussion. The output voltage ($V_{out}$) of a nonlinear system for a given input voltage ($V_s$) can be represented as [12]

$$V_{out} = a_1 V_s + a_2 V_s^2 + a_3 V_s^3 + ... + a_n V_s^n,$$

where $a_1, a_2, a_3, ...a_n$ are the Taylor series coefficients of the output. In an amplifier, $a_1$ represents the linear gain of the system, while $a_2, a_3, ...$ are the second, third and higher order distortion coefficients. Here,

$$a_n = \frac{1}{n!}\left[\frac{\partial^n V_{out}}{\partial {V_s}^n}\right].$$

The IIP3 of such a system can be given by [12]

$$A_{IIP3} \approx \sqrt{\frac{4}{3}.\frac{a_1}{a_3}} \tag{1.7a}$$

From equation (1.7a), one needs to increase $a_1$ and decrease $a_3$ for enhancing the linearity of an amplifier. $a_1$ depends on the available $g_m$ and is inherently proportional to the power consumption of the system. On the

other hand, the third order distortion coefficient $a_3$ is typically a device-dependent parameter. Hence, it is not straight-forward to achieve any arbitrarily small value of $a_3$ from the circuit design perspective. Consequently, the achieved linearity performance of an amplifier significantly depends on the available $g_m$ and effectively on the power consumption of the circuit. The dependence of achieved linearity performance on the power consumption is also reported in the literature [61]. According to [61], both P1dB and IIP3 improves with increasing gate overdrive voltage which requires the power consumption to be increased. This makes it a challenging problem to achieve a high linearity performance at low power levels.

## 1.3 Low power LNAs with low NF or high linearity

Various techniques have been proposed to improve the noise [16, 62–67] or the linearity performance [41, 68, 69] of low-power wideband LNAs. In this section, these noise and linearity improvement techniques have been discussed.

### 1.3.1 Low power LNAs with low NF

Most of the low-power LNAs presented in Tab. 1.1 have reported a slightly high NF. One of the main reasons behind the poor noise performance is the trade-off that exists between input impedance match and the noise figure of a wideband LNA [12]. [70] employed a combination of active and passive $g_m$-boosting to achieve an optimized noise performance. [62] demonstrated wideband LNAs with improved noise performance by using a technique called noise cancellation (NC). A combination of current-reuse and partial noise cancellation is employed in [62] to achieve improved noise performance along with wideband low-power operation. NC technique, along with current-reuse and inductive $g_m$-boosting, is used to design a ULV, ULP, wideband LNA in [65]. [63] employed double $g_m$ enhancement along with partial NC to achieve an optimized noise performance at low power levels. In [64], the noise performance of a sub-threshold LNA is improved by employing noise cancellation. Overall, [62–65] used partial noise cancellation and other low-power techniques to achieve an optimized noise performance at low power levels. Using noise cancellation, the achieved NF of an LNA can be further reduced [16, 66, 67]; however, at the expense of increased power consumption. [16] proposed a gain-enhanced NC technique to increase the gain at the NC condition while the input matching is maintained. [66] employs a noise-canceling balun LNA, where the inherent gain of the CS stage is reused to boost the transconductance of the CG stage.

Tab. 1.2 shows a performance summary of low-power NC wideband LNAs in the literature. From Tab. 1.2, [62, 63, 65] achieved optimized noise performance at low power levels. The works presented

**Table 1.2:** Performance summary of low-power noise-canceling LNAs in the literature

| | Inductor present? | Operating Freq. (GHz) | Gain (dB) | 3-dB BW (GHz) | NF (dB) | IIP3 (dBm) | Power (mW) |
|---|---|---|---|---|---|---|---|
| TCAS-II 2021 [71] | No | $0.13-93$ | $16.6-19.6$ | 0.8 | $3.6-5$ | $>-8.5$ | 3 |
| TCAS-I 2020 [72] | No | $0.05-1.3$ | $24-27.5$ | 1.25 | $2.3-3$ | $-2.2$ | 5.7 |
| TCAS-I 2018 [62] | No | $0.2-2.7$ | 21.2 | 2.5 | $3-3.5$ | $-2$ | 0.96 |
| | No | $0.1-4.3$ | 21.2 | 4.2 | $2.8-4$ | $-7.7$ | 2 |
| E. Lett. 2014 [63] | No | $0.35-0.95$ | 14 | 0.6 | $3.7-4.6$ | – | 0.4 |
| TMTT 2012 [66] | No | $0.1-2$ | 16.6 | 1.9 | 3.8 | $+0.5$ | 3 |
| TCAS-I 2012 [16] | No | $0.1-5.3^{\star}$ | $10.7^{\Delta}$ | 5.2 | $2.9-5.4$ | $-6$ | 7 |
| TCAS-I 2010 [67] | No | $0.2-3.8$ | 19 | 3.6 | $2.8-3.4$ | $-4.2$ | 5.7 |
| | No | $0.2-3.8$ | 14.8 | 3.6 | $3.5-4.1$ | $-3.8$ | 3.2 |
| JSSC 2021 [73] | Yes | $0.02-4.5$ | 15.2 | 4.48 | $2.09-3.2$ | $-4.62$ to $-3.53$ | 4.5 |
| TMTT 2021 [74] | Yes | $1-11$ | 17 | 10 | $3.5-5.5$ | $-2.8$ | 9 |
| TCAS-II 2019 [75] | Yes | $0.5-7$ | 16.8 | 6.5 | $2.87-3.77$ | $-4.5$ | 11.3 |
| TCAS-II 2018 [64] | Yes | $2-5$ | 13 | 3 | $6-8$ | $-9.5^{\dagger}$ | 1.8 |
| ISCAS 2013 [65] | Yes | $3.2-10$ | 15 | 6.8 | $4.5-5.3$ | $-2$ to $-7$ | 0.41 |

$\star$ Estimated from figures, $\Delta$ Power gain, † Simulated IIP3

in [16, 66, 67, 71–75] further improved the noise performance of an LNA at the expense of increased power consumption. However, almost all the NC LNAs shown in Tab. 1.2 provide a sub-optimal linearity performance. Only [66] achieved a moderately good IIP3, however at a slightly higher power level. From the current discussion, NC technique has demonstrated great potential in improving the noise performance of low-power wideband LNAs, however the linearity performance achieved in these circuits are not satisfactory in general. All this makes noise cancellation a potential technique that deserves further investigation.

In general, noise-canceling technique has shown potential to achieve extremely low NF in wideband LNAs [13–15, 17–20, 26, 67, 76]. In all these circuits, the noise of the matching amplifier is completely canceled using an auxiliary amplifier. The auxiliary amplifier needs to be biased at significantly higher power than the main amplifier to make its noise contribution negligible [13–15, 17–20, 26, 67, 76]. However, low-power applications cannot afford such high power budget, and employs a partial noise cancellation scheme instead [62–65].

### 1.3.2 Low power LNAs with high linearity

The same technique that cancels noise [13, 14] in a wideband LNA can also cancel the third-order nonlinearity to achieve high-linearity performance. [15, 77] effectively used the noise-and-distortion canceling technique to achieve high linearity performance in an LNA. Apart from noise-and-distortion cancellation, many other linearization techniques have been proposed [15, 78–87]. Source-degeneration is one such technique, which improves the linearity of an amplifier because of feedback. However, source degeneration using an inductor also gives rise to second-order interaction [78], which eventually restricts the amount of linearity improvement.

Harmonic termination [79–81] can alleviate the second-order interaction problem to some extent. [82, 83] showed the importance of applying an optimum bias voltage to a MOS transistor for achieving improved linearity performance. In the derivative superposition (DS) method proposed in [85], the third derivatives of drain current from the main and auxiliary transistors are added to cancel distortion. Since the DS method employs multiple transistors in parallel with their gates connected, it is also known as the multiple gated transistor (MGTR) technique [85]. DS method using dual nMOS transistors may degrade the second-order nonlinearity, while the third-order nonlinearity is improved. To avoid the degradation of second-order nonlinearity, a complementary DS method is proposed [15, 86]. In a complementary DS method, complementary MOS transistors (one pMOS and one nMOS transistor) are effectively used to minimize both second-and-third order nonlinearity coefficients [15, 86]. A complementary multi-gated transistor (MGTR) technique is employed in [87] to achieve a high linearity performance. However, a majority of these linearization techniques [15, 77, 81, 84, 86, 87] require sufficiently high power levels ($> 10$ mW) making them less suitable for low-power applications.

In recent times, [41, 68] utilized complementary derivative superposition and active shunt feedback to achieve high linearity performance while low power is ensured by a complementary current-reuse CS amplifier, combined with a low-current active feedback. [69] improved the linearity performance of a sub-threshold LNA without additional power consumption by using passive components. Tab. 1.3 showcases the achieved performance of these low-power high-linearity LNAs in the literature. From Tab. 1.3, [41, 68, 88] have achieved high-linearity performance, however a slightly higher power consumption is needed. Moreover, the design of [41, 68] requires complex optimization technique to achieve the best performance. [69] improved the linearity performance at extreme low-power levels; however, the design contains inductors and is narrow-band.

**Table 1.3:** Performance summary of low-power high-linearity LNAs in the literature

| | Inductor present? | Operating Freq. (GHz) | Gain (dB) | 3-dB BW (GHz) | NF (dB) | IIP3 (dBm) | Power (mW) |
|---|---|---|---|---|---|---|---|
| MWCL 2021 [88] | No | $0.1-1$ | 14 | 0.9 | 4 | $+2$ | 2.7 |
| TCAS-I 2019 [68] | No | $0.2-3.9$ | 15.7 | 3.7 | 3.1 | $+8.7$ | 3.3 |
| | No | $0.2-2.7$ | 14.5 | 2.5 | 4.6 | $-1$ | 1.2 |
| TCAS-I 2017 [41] | No | $0.1-2.1$ | 19.2 | 2 | 2.4 | $+8.6$ | 3.11 |
| | No | $0.1-1.2$ | 21.2 | 1.1 | 2.6 | $+6$ | 1.52 |
| TCAS-I 2018 [69] | Yes | $1.8^{\dagger}$ | 14.8 | – | 3.7 | $-3.7$ | 0.336 |

† Center frequency

## 1.4 Problem formulation

Noise cancellation [11–20, 26, 31, 67, 76, 77, 86, 89–97] is a frequently-used technique to overcome the fundamental trade-off between input impedance match and NF in wideband LNAs and receivers. A variety of noise-canceling LNAs and receivers have been proposed in the literature. We identified that having a single generic model that can explain the operation of all these NC LNAs and receivers would be useful. So, the first objective of this thesis is to investigate the possibility of a unified theory that can simplify the analysis of different NC circuits using a single generic model.

Developing new noise-canceling circuits requires a different approach compared to other circuit development. Hence, we define the second objective of this thesis as to develop a systematic methodology for generating new flicker and thermal noise-canceling circuits.

The LNAs presented in [38–40, 42, 43, 51, 52] operate at sub-mW power levels, but sacrifice on the noise and linearity performance. [16, 62, 64, 67] employed noise-canceling technique to lower the NF, but requires increased power levels. The LNAs presented in [16, 62, 64, 67] also have a poor IIP3. The LNAs presented in [20, 41, 51, 68, 69] either consume $> 1$ mW DC power or have an IIP3 $< 0$ dBm. All this leads to the third objective of this thesis which is to investigate and design an inductorless wideband LNA that consumes $< 1$ mW DC power and can achieve $> 0$ dBm IIP3 without deteriorating the noise figure.

In recent years, mixer-first [29–31, 95, 98–120] receivers have gained popularity because of their frequency translational nature and high linearity. The works presented in [29–31, 95, 106, 111] improve the performance metrics of a mixer-first receiver, but at the expense of an increased power budget. A few works [102, 114–117, 121] have proposed techniques to reduce the power consumption of a mixer-first receiver. However, the works presented in [102, 114–117, 121] either have degraded in-band linearity or a high noise figure (NF). The receivers presented in [122–124] achieves ultra-low-power operation but requires additional circuitry before the mixer stage. So, to reduce the power consumption of a mixer-first receiver without degrading its performance metrics is a problem worth addressing.

Out of the two types of power consumption associated with a mixer-first receiver, dynamic power consumption is technology dependent. In an advanced CMOS process, dynamic power consumption can be significantly reduced because of reduced parasitics. The dynamic power can be reduced to some extent by using higher on resistance for the mixer switches but at the expense of degraded noise figure. Other than that, a designer has minimal control over the dynamic power levels once the technology node is fixed. On the other hand, the static power constitutes a significant percentage of the total power consumed in a high-linearity mixer-first re-

ceiver [29–31]. Hence, reducing the baseband power consumption of a mixer-first receiver while simultaneously achieving a good noise and linearity performance is the fourth problem that we address in this thesis.

## 1.5 Organization of the thesis

The thesis has been organized into six chapters. Among them, this chapter (chapter 1) introduces the thesis and provides a brief literature survey. The motivation behind the current work is also outlined in this chapter. The rest of this thesis is organized as follows.

We have studied the noise-canceling technique in detail and developed a generic theory of noise-canceling circuits. This study and the observations are described in chapter 2.

The development of a systematic methodology for generating new flicker and thermal noise-canceling circuits is presented in chapter 3. By using the developed method, three new NC circuits are derived, designed, and simulated.

Chapter 4 presents a low-power partial noise-canceling complementary common-gate (CCG) LNA developed using the systematic method discussed in chapter 3. The LNA can also achieve high linearity by employing optimum biasing for the complementary transistors. A prototype of the proposed circuit is implemented in a standard 180 nm CMOS technology. This chapter presents the performance characterization of the proposed circuit that includes a comparison with other relevant works.

The analysis, design, and implementation of a mixer-first receiver is presented in chapter 5. In the implemented mixer-first receiver, the LNA presented in chapter 4 is employed as the baseband trans-impedance amplifier (TIA). The proposed amplifier helps to reduce the baseband power consumption significantly without degrading the receiver's overall performance. A prototype of the proposed receiver is implemented in a standard 180 nm CMOS technology, and the measured performance parameters are compared with other mixer-first receivers in the literature.

Chapter 6 summarizes the works presented in this thesis and provides conclusive remarks. It also presents a discussion on the future research directions evolving from this thesis.

# 2

# Generalized Theory of Noise-Canceling Circuits



**Contents**

## 2.1 Introduction

Noise cancellation (NC) breaks the trade-off between input impedance and noise figure in wideband LNAs [11–16, 77, 86, 89–92], making it possible to tune them independently. Traditionally, the noise-canceling technique is explained with the help of a block diagram shown in Fig. 2.1 [13]. In Fig. 2.1, the input signal from a source with an internal resistance $R_s$ is simultaneously fed to a matching amplifier and a voltage-sensing amplifier. The matching amplifier stage provides the source impedance match at the input of the LNA ($Z_{inm} = R_s$), and the voltage-sensing amplifier provides a voltage gain without loading the source (i.e., high $Z_{inv}$). The input-referred noise voltage of the matching amplifier ($\overline{v_{inm}^2}$) is sensed and processed by the voltage-sensing amplifier. Finally, the outputs of the two stages are combined in such a way that the noise contribution of the matching device is nullified while constructively adding the signals from both paths.

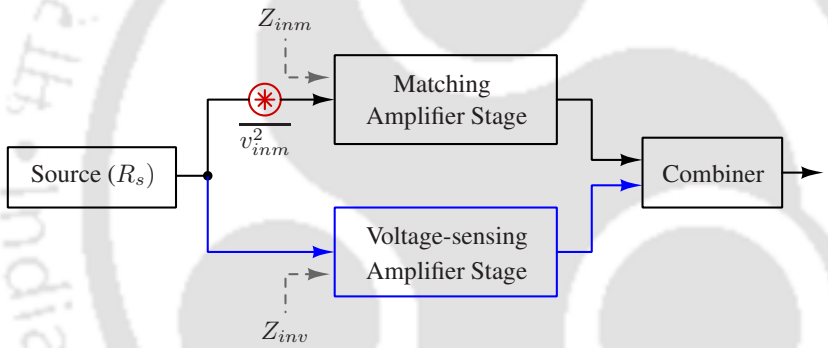



**Figure 2.1:** Block diagram representation of the noise cancellation technique in LNAs [13].

### 2.1.1 Necessary conditions for noise cancellation

The key to the noise-canceling principle is the identification of two nodes in a circuit (matching amplifier) that satisfy one of the following two conditions.

- At the two nodes, the signal appears with the same polarity, but the instantaneous noise appears with opposite polarity.
- The signal appears with opposite polarity, but the instantaneous noise appears with the same polarity at the two nodes.

Once such nodes (which are suitable for NC) are identified, extra circuitry can be added to scale the (signal+noise) voltage at these nodes appropriately and combine them so that the noise is canceled at the output.

### 2.1.2 Motivation of this work

Many noise-canceling LNAs [11–16, 77, 86, 89–92] have been proposed in the literature. However, a single systematic method to analyze these different noise-canceling circuits is not reported. Having a generic theory could unify the analysis of various NC circuits. Such a theory is also advantageous in developing new NC circuits for future requirements. In this work, we first review existing NC circuits in the literature, followed by the development of a unified feedback-feedforward NC model.

### 2.1.3 Understanding existing noise-canceling circuits

In literature, the noise-canceling technique was first introduced in a resistive shunt-feedback (RSF) LNA [13]. [14] proposed a noise-canceling common-gate common-source (CG-CS) LNA. Fig. 2.2(a) and 2.2(b) show the circuit diagrams of a resistive shunt-feedback (RSF) LNA and a common-gate (CG) LNA. In Fig. 2.2(a), $i_{n1}$ represents the instantaneous noise current of the MOS transistor $M_1$. The instantaneous noise current flows through $R_f$ and $R_s$ and causes two instantaneous noise voltages at the gate and drain nodes of $M_1$. The instantaneous noise voltage at gate and drain nodes of $M_1$ due to the instantaneous noise current $i_{n1}$ have the same polarity. However, the signal voltage appears with opposite polarity at the gate and drain nodes of $M_1$. In the CG LNA shown in Fig. 2.2(b), the instantaneous noise voltage due to the noise current $i_{n1}$ appears with opposite polarity at the drain and source nodes of the CG transistor, but the signal voltage appears with the same polarity.

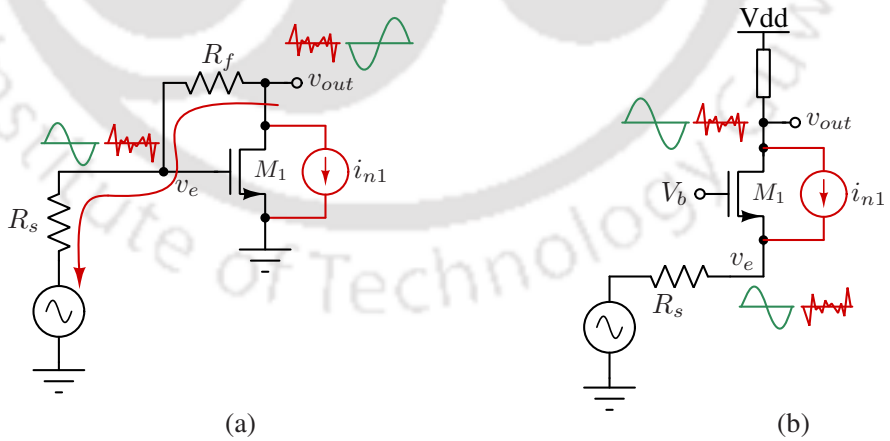



**Figure 2.2:** (a) A resistive shunt feedback LNA, and (b) a common-gate LNA.

In the RSF LNA shown in Fig. 2.2(a), an auxiliary path can be added from the $v_e$ node to the output to cancel the noise of $M_1$. The resulting RSF NC LNA is shown in Fig. 2.3(a) [13], where the gate and drain voltages of $M_1$ are scaled by $-A_{aux}$ and $+1$, respectively, before combining them. $A_{aux}$ is properly set to cancel the

noise of $M_1$, while signals from the two paths are added at the final output $v'_{out}$. In the CG LNA shown in Fig. 2.2(b), an auxiliary path is added to cancel the matching transistor's noise. The resulting CG NC LNA is shown in Fig. 2.3(b) [14], where the source voltage of the CG transistor is first scaled by a factor of $-A_{cs}$, using a common-source (CS) amplifier. Output is taken differentially between the drains of CG and CS transistors. By choosing an appropriate gain $A_{cs}$ for the CS amplifier, the noise of the CG transistor can be canceled at the output.

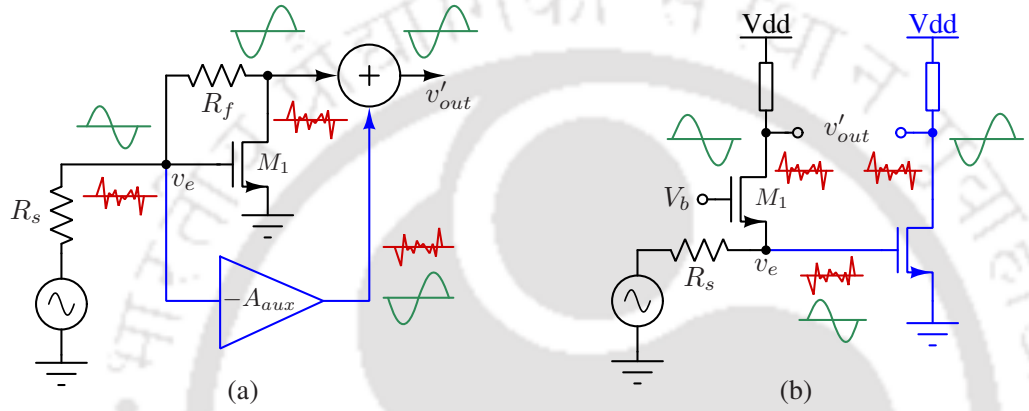



**Figure 2.3:** (a) A resistive shunt feedback noise-canceling LNA [13,16,89], and (b) a CG noise-canceling LNA [11,14,15].

The techniques proposed in [15, 17–20, 26, 67, 76] further improve the performance of noise-canceling circuits. [15] presented an inductorless broadband LNA with simultaneous noise and distortion cancellation. An NC differential LNA with a composite nMOS/pMOS cross-coupled transistor pair is presented in [17]. In [26], an RSF noise-canceling LNA with a feedforward path from the input to the cascode device is presented. A CG noise-canceling LNA with local feedback from the auxiliary path to the main path is presented in [67]. [18] proposed a complementary noise-canceling CMOS LNA with enhanced linearity. A noise-canceling balun LNA with a modified current-bleeding technique is proposed in [19]. [20] proposed a triple-path noise-canceling CG-CS LNA with a dual complementary pMOS-nMOS configuration. [76] presents an NC receiver with mutual noise cancellation between the main path and the auxiliary path using a transformer.

The NC principle is also used in the design of wideband frequency-tunable receivers presented in [31,94–97]. In these receivers [31,94–97], the matching device can be modeled as a floating resistor. Fig. 2.4(a) shows the block diagram representation of a NC-receiver [31]. In Fig. 2.4(a), the resistor $R_{in}$ represents the matching device. The output is taken differentially between the voltage measurement path ($\alpha V_{R_{in}}$) and the current measurement path ($-r_m I_{R_{in}}$). The noise of $R_{in}$ can be nulled at the output by setting $r_m = \alpha R_s$. Fig. 2.4(b) shows an implementation of the NC-receiver. The mixer in Fig. 2.4(b) is a current-driven passive mixer, and the

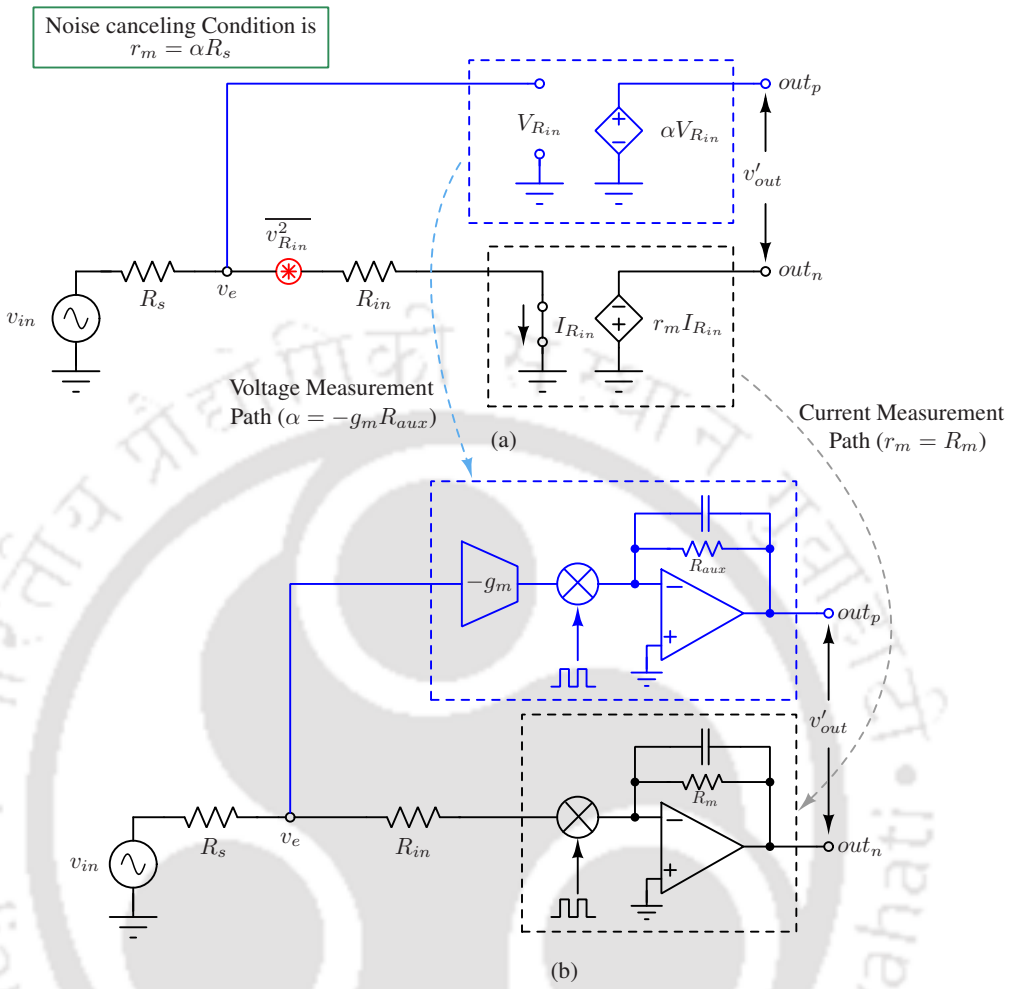



**Figure 2.4:** (a) Block diagram representation of the noise cancellation technique in receivers [31, 95, 97]. (b) A frequency translated noise-canceling receiver [31, 95, 97].

trans-impedance amplifier (TIA) acts as a current-to-voltage converter.

## 2.2 Broad classification of noise reduction techniques

Feedforward and feedback are the two well-known techniques used to reduce amplifier noise [125]. The models of these two techniques are briefly reviewed in this section.

### 2.2.1 Feedforward noise cancellation

Feedforward noise cancellation can be explained with the help of a block diagram, shown in Fig. 2.5 [125]. In Fig. 2.5, $A_m$ is the main amplifier whose noise needs to be canceled at the final output. $N_m$ is the output noise of $A_m$. The output of the main amplifier is first scaled down by a factor $\gamma_1$ and combined with a delayed version

of the input signal. If $\gamma_1 = 1/A_m$, the signal is canceled, leaving only the noise at the output of the combiner. Hence, $X_1$ is a scaled version of the noise $N_m$. $X_1$ is further amplified by an auxiliary amplifier ($A_{aux}$) and subtracted from the main amplifier's output to cancel $N_m$. The amplitude of $A_{aux}$ is set such that the main amplifier noise is completely canceled at the final output $Z$. In Fig. 2.5, $\tau_1$ and $\tau_2$ represent the delay blocks in the auxiliary path and the main path, respectively. The delay blocks ensure phase matching of the signals for combining.

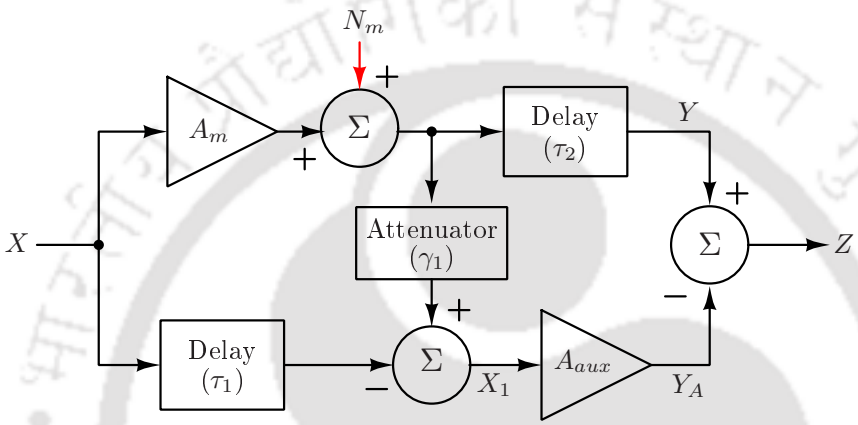



**Figure 2.5:** Block diagram of a feedforward noise-canceling amplifier [125].

The following equations are valid for the feedforward noise-canceling amplifier shown in Fig. 2.5.

$$Y = A_m X + N_m \tag{2.1a}$$

$$Y_A = A_{aux} X_1 = A_{aux}(\gamma_1 N_m) \tag{2.1b}$$

$$\begin{aligned} Z &= Y - Y_A \\ &= A_m X + N_m(1 - A_{aux}\gamma_1) \end{aligned} \tag{2.1c}$$

For canceling main amplifier noise at the output Z, one needs to set $A_{aux} = 1/\gamma_1 = A_m$.

### 2.2.2 Feedback noise reduction

The usage of negative feedback can reduce amplifier noise. Fig. 2.6 shows the block diagram of a negative feedback amplifier. In Fig. 2.6, $X$ represents the input signal, $Y$ represents the output signal, $A_m$ is the gain of the main amplifier, $e$ represents the error signal, $N_m$ is the noise added by the main amplifier, and $\beta$ is the feedback factor.

Assuming the main amplifier is noiseless, the block diagram of the negative feedback amplifier (shown in Fig. 2.6) can be simplified to the one in Fig. 2.7(a). Similarly, Fig. 2.7(b) represents the block diagram of the

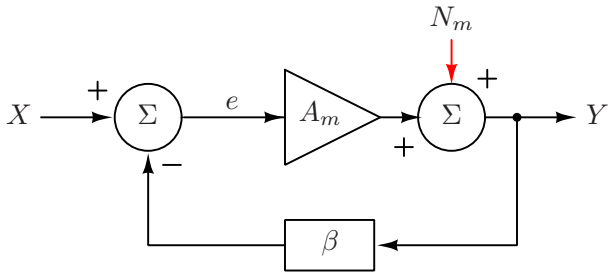



**Figure 2.6:** Block diagram of a negative feedback amplifier.

negative feedback amplifier when input is grounded, and only the noise is present. Fig. 2.7(a) and Fig. 2.7(b) are used for computation of transfer function with respect to input signal and noise, respectively. The following expressions for the error ($e$) and the output ($Y$) signals can be derived from Fig. 2.6 and Fig. 2.7.

$$e = \frac{1}{1 + A_m\beta}X - \frac{\beta}{1 + A_m\beta}N_m \tag{2.2a}$$

$$Y = \frac{A_m}{1 + A_m\beta}X + \frac{1}{1 + A_m\beta}N_m \tag{2.2b}$$

From (2.2b), it can be seen that both the signal and noise of the main amplifier are reduced by a factor $(1 + A_m\beta)$ at the output. Though feedback can reduce the output noise of the amplifier, it will not improve the signal to noise ratio [126].

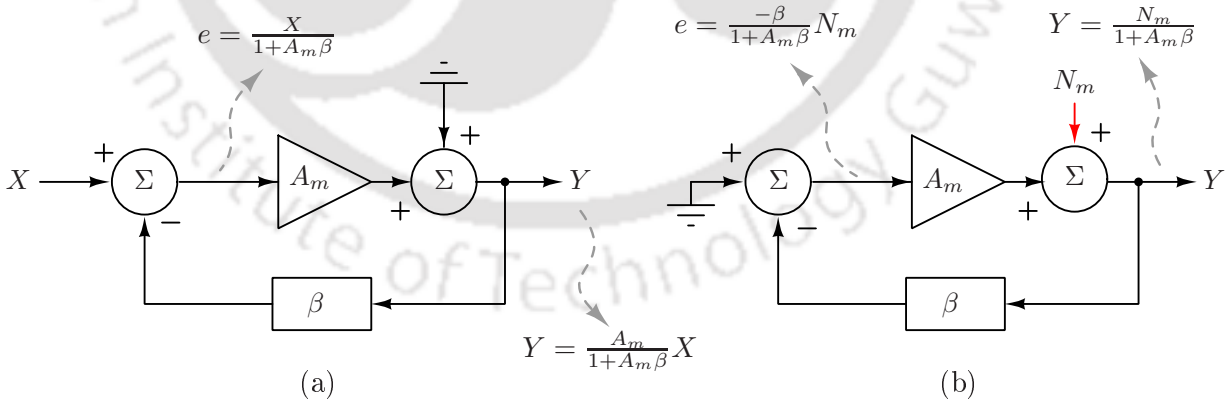



**Figure 2.7:** (a) Computation of the transfer function with respect to the input signal, and (b) computation of the transfer function with respect to the noise signal.

## 2.3 Proposed feedback-feedforward noise-canceling model

The previous section presented the models of feedforward noise cancellation and feedback noise reduction techniques. In this section, the understanding acquired from these two techniques are used to develop the proposed feedback-feedforward noise-canceling model.

Even though feedback can not cancel noise by itself, the use of feedback gives an opportunity to cancel amplifier noise with the help of an auxiliary path. In the expressions of $e$ and $Y$ (given by (2.2a) and (2.2b) respectively), the noise $N_m$ has an opposite polarity, whereas the input signal $X$ has the same polarity. This difference in polarity of the noise, at nodes $e$ and $Y$, provides an opportunity to cancel the noise $N_m$ at the output. This kind of relation between signal and noise at two nodes in a circuit occurs because of the presence of negative feedback within the matching amplifier. By adding a feedback amplifier, having a gain of $A_{aux}$ from the error node to the output, the noise Nm can be canceled, as shown in Fig. 2.8.

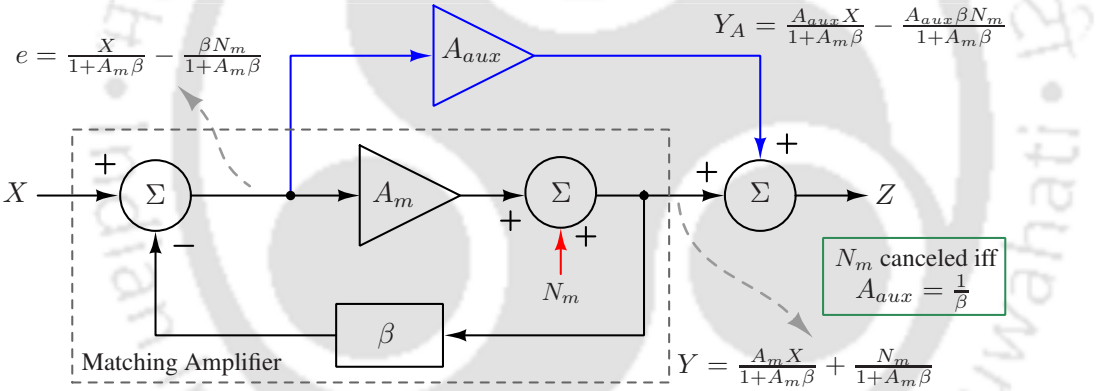



**Figure 2.8:** Adding a feedforward amplifier $A_{aux}$ to cancel the noise of $A_m$ at the output $Z$.

The following expression can be derived from the block diagram in Fig. 2.8.

$$Y_A = \frac{A_{aux}}{1 + A_m\beta}X - \frac{A_{aux}\beta}{1 + A_m\beta}N_m \tag{2.3}$$

In the block diagram, as shown in Fig. 2.8, the output is taken from $Z$ instead of $Y$. From Fig. 2.8, noise $N_m$ can be canceled at the final output if $A_{aux} = 1/\beta$. Let us define $A_{aux} = 1/\beta$ as the condition for NC. Under the

NC condition, the overall gain of the system can be computed as follows.

$$\frac{Z}{X} = \frac{Y}{X} + \frac{Y_A}{X} \tag{2.4a}$$

$$= \frac{A_m}{1 + A_m\beta} + \frac{1/\beta}{1 + A_m\beta} \tag{2.4b}$$

$$= \frac{1}{\beta} \text{ or } A_{aux} \tag{2.4c}$$

So, the condition for noise cancellation is $A_{aux} = 1/\beta$; and under the NC condition, the overall gain of the system is $Z/X = 1/\beta$. The gain from the error node $e$ to the output node $Z$ can be computed as follows.

$$\frac{Z}{e} = \frac{Z}{X}.\frac{X}{e} = \frac{1}{\beta}.(A_m\beta + 1) \tag{2.5a}$$

$$= A_m + \frac{1}{\beta} \text{ or } A_m + A_{aux} \tag{2.5b}$$

The summary of the current discussion is as follows. The possibility of noise cancellation arises due to the negative feedback in the matching amplifier. If the matching amplifier's feedback factor is $\beta$, then an auxiliary amplifier having a gain $A_{aux} = 1/\beta$ can be added from the error node to the output node for canceling the matching amplifier noise. Under the NC condition, the overall gain of the amplifier is equal to $1/\beta$ [127].

## 2.4 Validating proposed theoretical claims on existing NC circuits

In this section, the theoretical claims proposed in the previous section are validated using known NC circuits. For this purpose, macro-models of various circuit components like a resistor and a MOSFET are developed first. These macro-models are then used to generate system-level models of the following three NC circuits: a common-gate NC LNA, a resistive shunt feedback NC LNA, and a wideband NC receiver. Finally, the developed system-level models are compared with the proposed feedback-feedforward NC model, shown in Fig. 2.12.

### 2.4.1 Macro-models of different circuit components

In this section, macro-models of various circuit components are developed.

#### 2.4.1.1 Macro-model of a floating resistor

Fig. 2.9(a) shows a floating resistor $R_f$ and its instantaneous thermal noise current $i_n$ between the nodes X and Y. In Fig. 2.9(a), $v_x$ is the voltage at X, $v_y$ is the voltage at Y, $i_x$ is the current flowing out of X, and $i_y$ is the current flowing into Y.

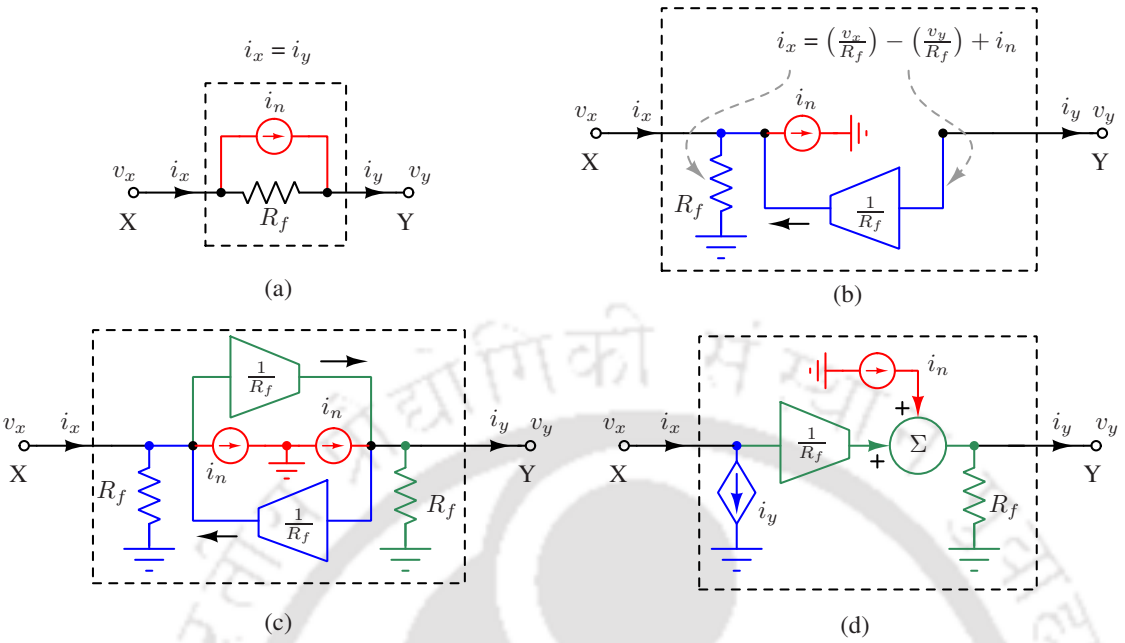



**Figure 2.9:** (a) A floating resistor $R_f$ and its instantaneous thermal noise current $i_n$. (b) A three component model of the current $i_x$. (c) A complete model of the floating resistor in (a) [111]. (d) Another model of the floating resistor using a current controlled current source.

Using nodal analysis in Fig. 2.9(a) gives the following equations.

$$i_x = \left(\frac{v_x - v_y}{R_f}\right) + i_n$$
$$= \left(\frac{v_x}{R_f}\right) - \left(\frac{v_y}{R_f}\right) + i_n \tag{2.6a}$$

$$\text{and, } i_x = i_y \tag{2.6b}$$

The three terms in the expression of $i_x$ in (2.6a) are modeled using the following three components in Fig. 2.9(b): a grounded resistor ($v_x/R_f$), a transconductor ($v_y/R_f$), and a current source ($i_n$). In Fig. 2.9(c), a similar three-component model of $i_y$ is added to complete the floating resistor's equivalent model. An equivalent model similar to Fig. 2.9(c) is also used in one recent work [111]. An alternate way of modeling a floating resistor is as shown in Fig. 2.9(d), where a current-controlled current source is used to model $i_x$ ($= i_y$). Any one of these two models (Fig. 2.9(c) and Fig. 2.9(d)) can be used to represent a floating resistor.

### 2.4.1.2 Macro-model of a single MOSFET

For small signals, a MOSFET in saturation (as shown in Fig. 2.10(a)) can be modeled as a transconductance stage with a voltage summer at the input and a current summer at the output as shown in Fig. 2.10(b). The voltage

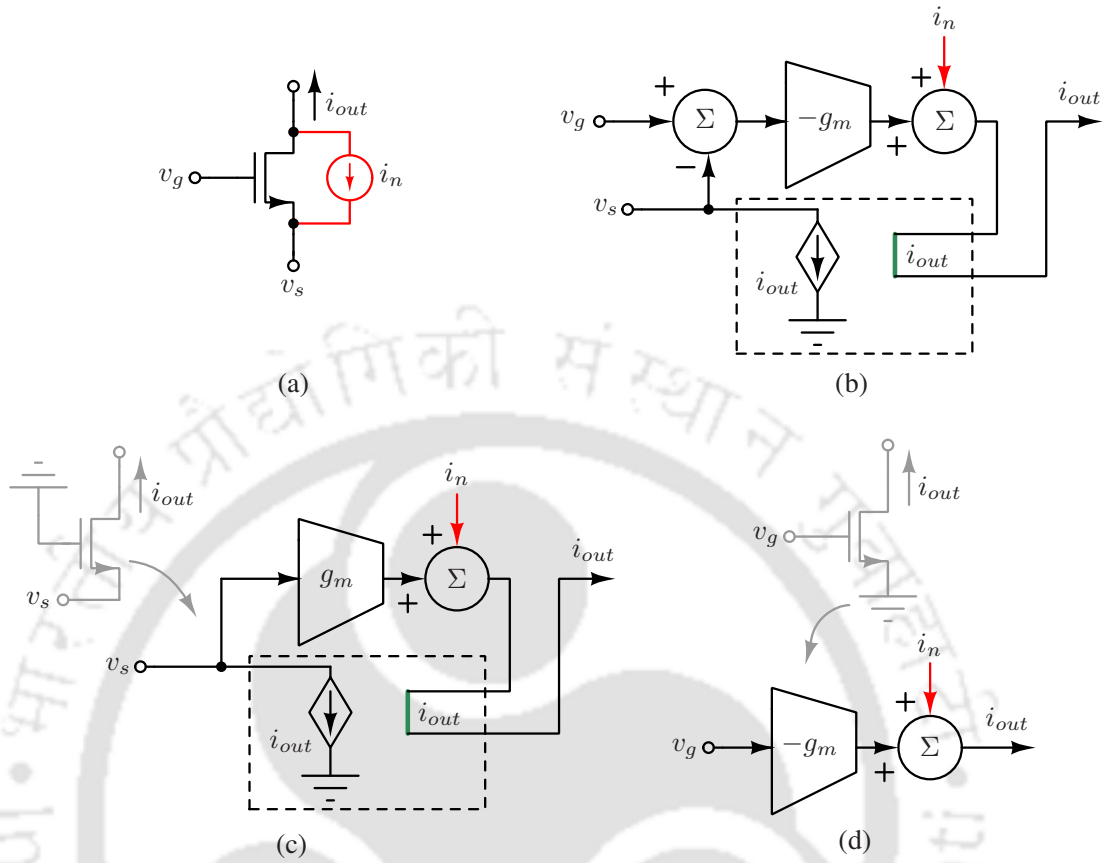



**Figure 2.10:** (a) MOSFET voltage and current convention. (b) A generic model of a MOSFET including the output noise current and the current sensing feedback. (c) Simplified model of a CG configuration. (d) Simplified model of a CS configuration.

summer at the input operates on the gate and source voltages of the MOSFET. In Fig. 2.10(b), the instantaneous thermal noise current ($i_n$) of the MOSFET is added to the output current with the help of a current summer at the output. In the macro model shown in Fig. 2.10(b), a current-controlled current source (CCCS) is included at the source terminal to account for the inherent current sensing feedback that exists in a MOSFET. Output resistance and all capacitances of the MOSFET are ignored in this model. For a CG configuration, the model in Fig. 2.10(b) can be simplified to the one shown in Fig. 2.10(c). The model a CS configuration is developed in a similar manner and is shown in Fig. 2.10(d).

### 2.4.2 Developing system-level models of existing NC circuits

System-level models are generated using the macro-models developed in the previous subsection.

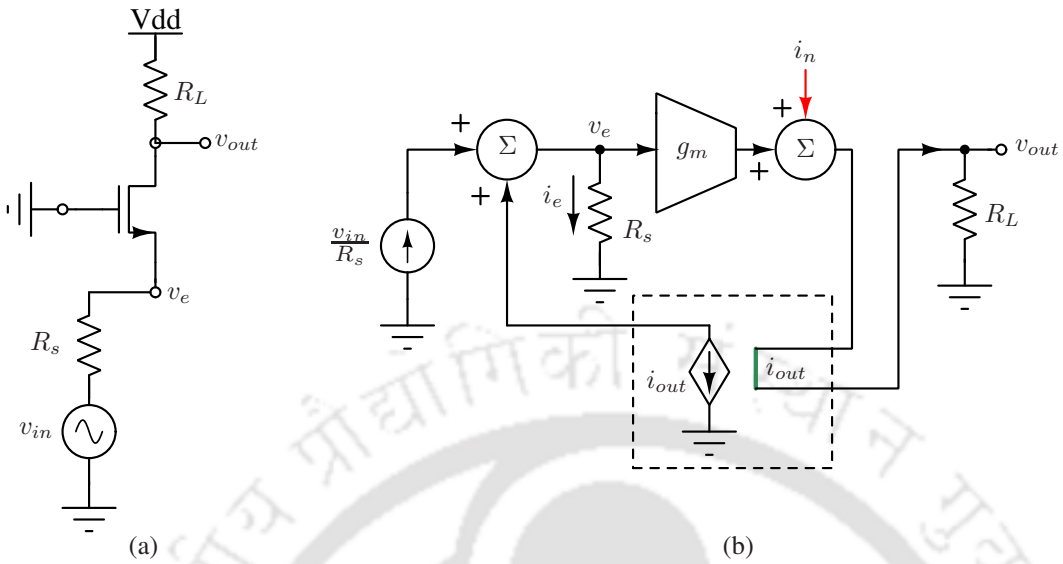



**Figure 2.11:** (a) A CG amplifier, and (b) a feedback model of it.

#### 2.4.2.1 System-level model of a common-gate NC LNA

A common-gate amplifier with an input voltage source $v_{in}$ and a source resistance $R_s$ is shown in Fig. 2.11(a). The circuit in Fig. 2.11(a) can be redrawn, as shown in Fig. 2.11(b), using the CG model shown in Fig. 2.10(c). In Fig. 2.11(b), the input voltage source is converted to its equivalent current source. From Fig. 2.11(b), the error and output voltages can be derived as follows.

$$v_e = \frac{1}{1+g_m R_s} v_{in} - \frac{R_s/R_L}{1+g_m R_s} v_n \tag{2.7a}$$

$$v_{out} = \frac{g_m R_L}{1+g_m R_s} v_{in} + \frac{1}{1+g_m R_s} v_n \tag{2.7b}$$

where $v_n = i_n R_L$.

In the expressions of $v_e$ and $v_{out}$ (from (2.7a) and (2.7b)), the noise has opposite polarities, whereas the input signal has the same polarity. The CG amplifier block diagram (as shown in Fig. 2.11(b)) can be compared with the block diagram of a negative feedback amplifier, as shown in Fig. 2.6. By comparing (2.7a) and (2.7b) with equations (2.2a) and (2.2b), the following expressions for $A_m$ and $\beta$ can be obtained.

$$A_m = g_m R_L \tag{2.8a}$$

$$\beta = \frac{R_s}{R_L} \tag{2.8b}$$

Similar to Fig. 2.8, a feedforward amplifier of gain $|1/\beta|$ needs be added to Fig. 2.11(b) to cancel the noise

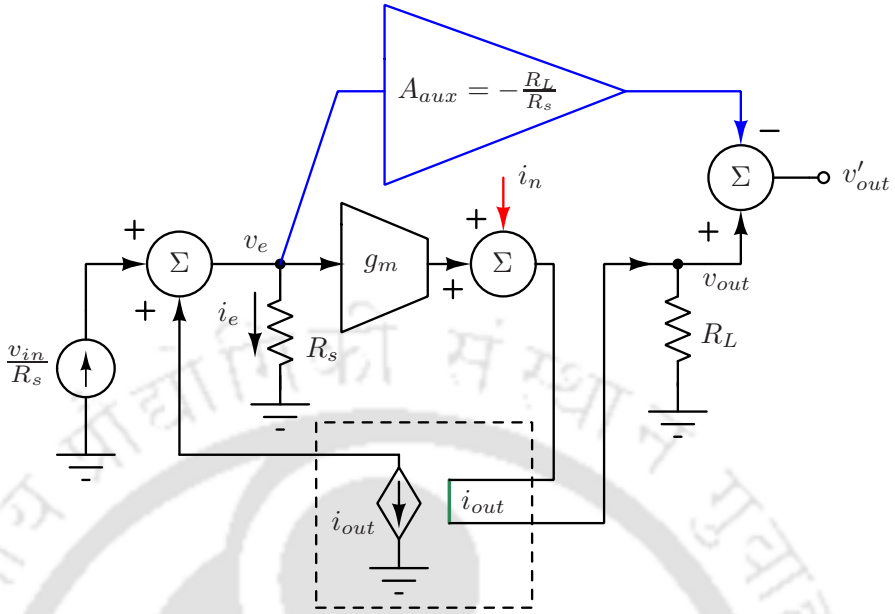



**Figure 2.12:** Adding a feedforward amplifier of gain $A_{aux} = -R_L/R_s$ to cancel the noise of the input transistor in a CG amplifier.

voltage $v_n$ at the output. The complete model of the CG noise-canceling LNA is shown in Fig. 2.12. Under this noise-canceling condition, the overall gain of the system ($v'_{out}/v_{in}$) is equal to $(R_L/R_s)$, i.e. $|1/\beta|$.

#### 2.4.2.2 System-level model of a resistive shunt feedback NC LNA

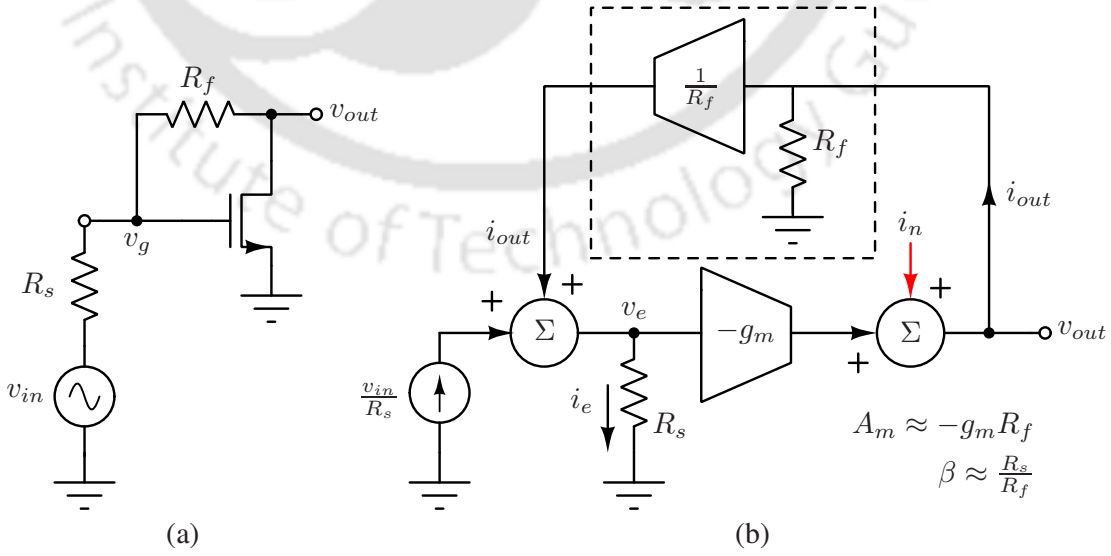



**Figure 2.13:** (a) A resistive shunt feedback amplifier, and (b) its approximate feedback model.

Resistive shunt feedback LNA is another circuit where noise cancellation is employed. Fig. 2.13(a) shows

the schematic of a resistive shunt feedback LNA. For a high loop gain value, the shunt feedback LNA (shown in Fig. 2.13(a)) can be redrawn, as shown in Fig. 2.13(b) using the proposed CS model (as shown in Fig. 2.10(d)). In Fig. 2.13(b), only half of the proposed resistor model is used to represent the feedback resistor $R_f$. This is done to represent the unidirectional flow of signal through $R_f$. The remaining half of the resistor model will be added later for completeness of the analysis.

From Fig. 2.13(b), the error voltage $v_e$ and the output voltage $v_{out}$ can be expressed as

$$v_e = \frac{1}{1+g_m R_s} v_{in} + \frac{R_s/R_f}{1+g_m R_s} v_n \tag{2.9a}$$

$$v_{out} = \frac{-g_m R_f}{1+g_m R_s} v_{in} + \frac{1}{1+g_m R_s} v_n \tag{2.9b}$$

where $v_n = i_n R_f$.

From (2.9a) and (2.9b), the noise voltage ($v_n$) has the same polarity in the expressions of $v_e$ and $v_{out}$, whereas the input signal ($v_{in}$) has opposite polarity in these expressions. Equations (2.9a) and (2.9b) can be compared with (2.2a) and (2.2b), respectively, to obtain the following expressions for $A_m$ and $\beta$ (voltage transfer functions in a trans-impedance amplifier are being analyzed).

$$A_m = -g_m R_f \tag{2.10a}$$

$$\beta = -\frac{R_s}{R_f} \tag{2.10b}$$

To cancel the noise voltage $v_n$ at the output, a feedforward amplifier of gain $R_f/R_s$ can be added from $v_e$ to $v_{out}$ in Fig. 2.13(b). The resulting NC shunt feedback LNA is shown in Fig. 2.14. Under the NC condition, the overall gain ($v'_{out}/v_{in}$) of the circuit in Fig. 2.14 is equal to $(R_f/R_s)$, i.e., $|1/\beta|$.

The circuit in Fig. 2.13(a) has an extra feedforward path due to the bi-directional nature of the resistor $R_f$ which was not included in Fig. 2.13(b). Fig. 2.15 includes the complete model of the resistor $R_f$. From Fig. 2.15, $v_e$ and $v_{out}$ expressions can be derived as

$$v_e = \frac{1}{1+g_m R_s} v_{in} + \frac{R_s/R_f}{1+g_m R_s} v_n \tag{2.11a}$$

$$v_{out} = \frac{1-g_m R_f}{1+g_m R_s} v_{in} + \frac{1+R_s/R_f}{1+g_m R_s} v_n \tag{2.11b}$$

where $v_n = i_n R_f$.

From (2.11a) and (2.11b), to cancel the noise voltage $v_n$ at the output, $v_e$ needs to be scaled by a factor of $-(1+R_f/R_s)$ and combined with $v_{out}$ to obtain the noiseless output $v'_{out}$. The complete model of a NC resistive shunt feedback LNA is shown in Fig. 2.15. The modified NC condition from Fig. 2.15 is

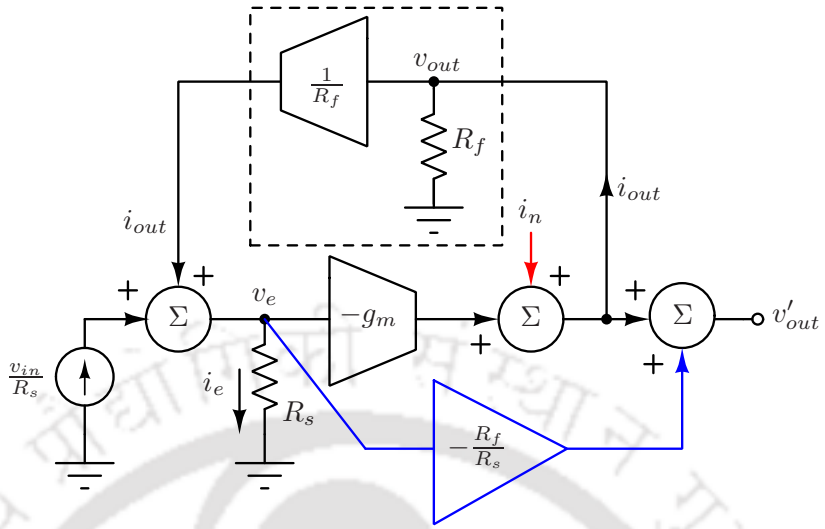



**Figure 2.14:** Canceling the noise of the input transistor in a shunt feedback amplifier using a feedforward amplifier of gain $-\frac{R_f}{R_s}$.

$A_{aux} = -(1 + R_f/R_s) = -(1 + |1/\beta|)$. Under the modified NC condition, the overall gain of the system is equal to $(R_f/R_s)$, i.e., $|1/\beta|$.

#### 2.4.2.3 System-level model of a wideband NC receiver

The main path of the wideband noise-canceling receiver, shown in Fig. 2.4(b), is redrawn in Fig. 2.16(a). The floating resistor $R_{in}$ in Fig. 2.16(a) is replaced with its model in Fig. 2.16(b). In Fig. 2.16(b), a current-controlled voltage source, similar to the one in Fig. 2.4(a), is used to model the combination of the current driven mixer and the trans-impedance amplifier (TIA).

From Fig. 2.16(b), the error voltage $v_e$ and the output voltage $out_n$ can be expressed as

$$v_e = \frac{1}{1 + \frac{R_s}{R_{in}}} v_{in} - \frac{-R_s/r_m}{1 + \frac{R_s}{R_{in}}} v_n \tag{2.12a}$$

$$out_n = \frac{-r_m/R_{in}}{1 + \frac{R_s}{R_{in}}} v_{in} + \frac{1}{1 + \frac{R_s}{R_{in}}} v_n \tag{2.12b}$$

where $v_n = -i_n r_m$.

From (2.12a) and (2.12b), the noise voltage has the same polarity in the expressions of $v_e$ and $out_n$, whereas the input signal has opposite polarity in these expressions. (2.12a) and (2.12b) can be compared with

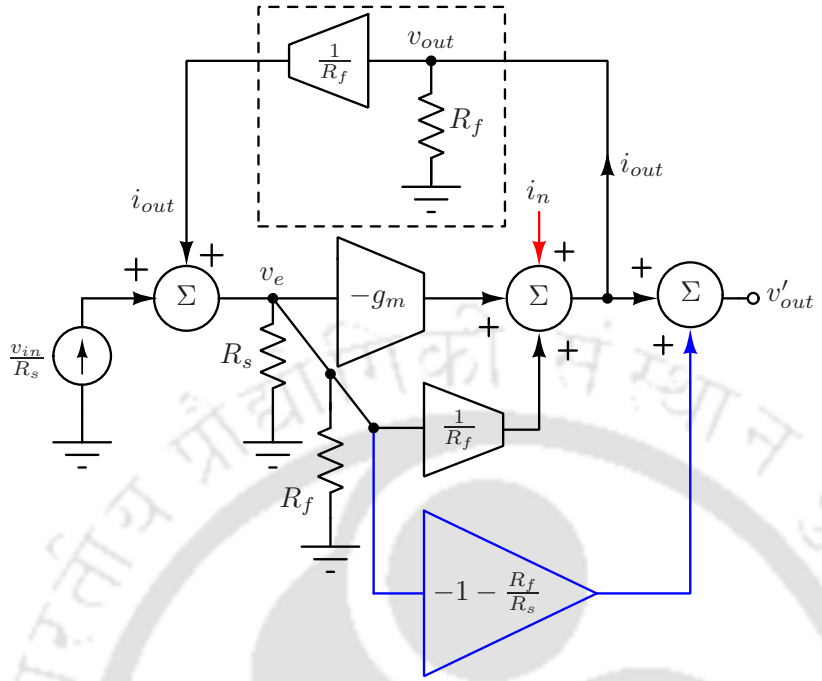



**Figure 2.15:** The complete model of the RSF noise-canceling LNA shown in Fig. 2.1(b).

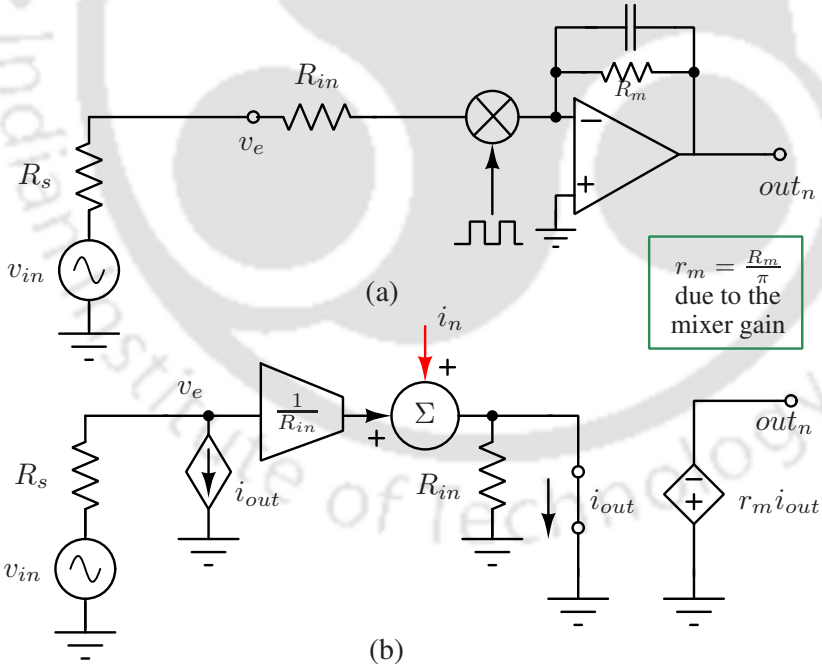



**Figure 2.16:** (a) Main path of the noise-canceling receiver from Fig. 2.4(b), and (b) its feedback model.

(2.2a) and (2.2b), respectively, to obtain the following expressions for $A_m$ and $\beta$.

$$A_m = \frac{-r_m}{R_{in}} = \frac{-R_m}{\pi R_{in}} \tag{2.13a}$$

$$\beta = \frac{-R_s}{r_m} = \frac{-\pi R_s}{R_m} \tag{2.13b}$$

For canceling the noise voltage $v_n$ at the output, a feedforward path can be added from $v_e$ to the output as shown in Fig. 2.4(b). To nullify the noise of the main path, the gain of the auxiliary path should be equal to $R_m/(\pi R_s)$ (=$|1/\beta|$). The resulting NC receiver is the same as the one in Fig. 2.4(b). Under the NC condition, the overall gain ($v'_{out}/v_{in}$) of the NC receiver is equal to $R_m/(\pi R_s)$, i.e., $|1/\beta|$.

## 2.5 Simulation verification

In this section, the three circuits presented in section 2.4 are simulated to verify the proposed theoretical claims. In the implementation, ideal components (such as VCVS, VCCS, and ideal switch) are used for all the elements, except for the matching device. For simulations, only the matching device's noise is considered since all other elements are ideal. All simulations presented in this section are performed using a standard 180 nm CMOS technology.

### 2.5.1 A common-gate NC LNA

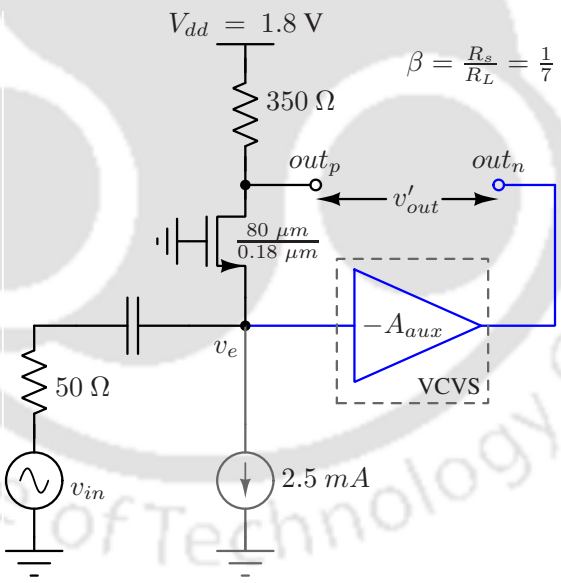



**Figure 2.17:** Simulated CG noise-canceling LNA.

A CG noise-canceling LNA, as shown in Fig. 2.17, is designed. A load resistance ($R_L$) of 350 Ω and a source resistance ($R_s$) of 50 Ω are used in the current implementation. From equation (2.8b), $\beta = R_s/R_L = 1/7$. The input transistor is biased to achieve a transconductance of 20 $m\mho$ ($= 1/R_s$) to ensure input impedance matching. An auxiliary amplifier $A_{aux}$ (implemented using a VCVS) is added to the circuit, as shown in Fig. 2.17, to cancel the input transistor's noise.

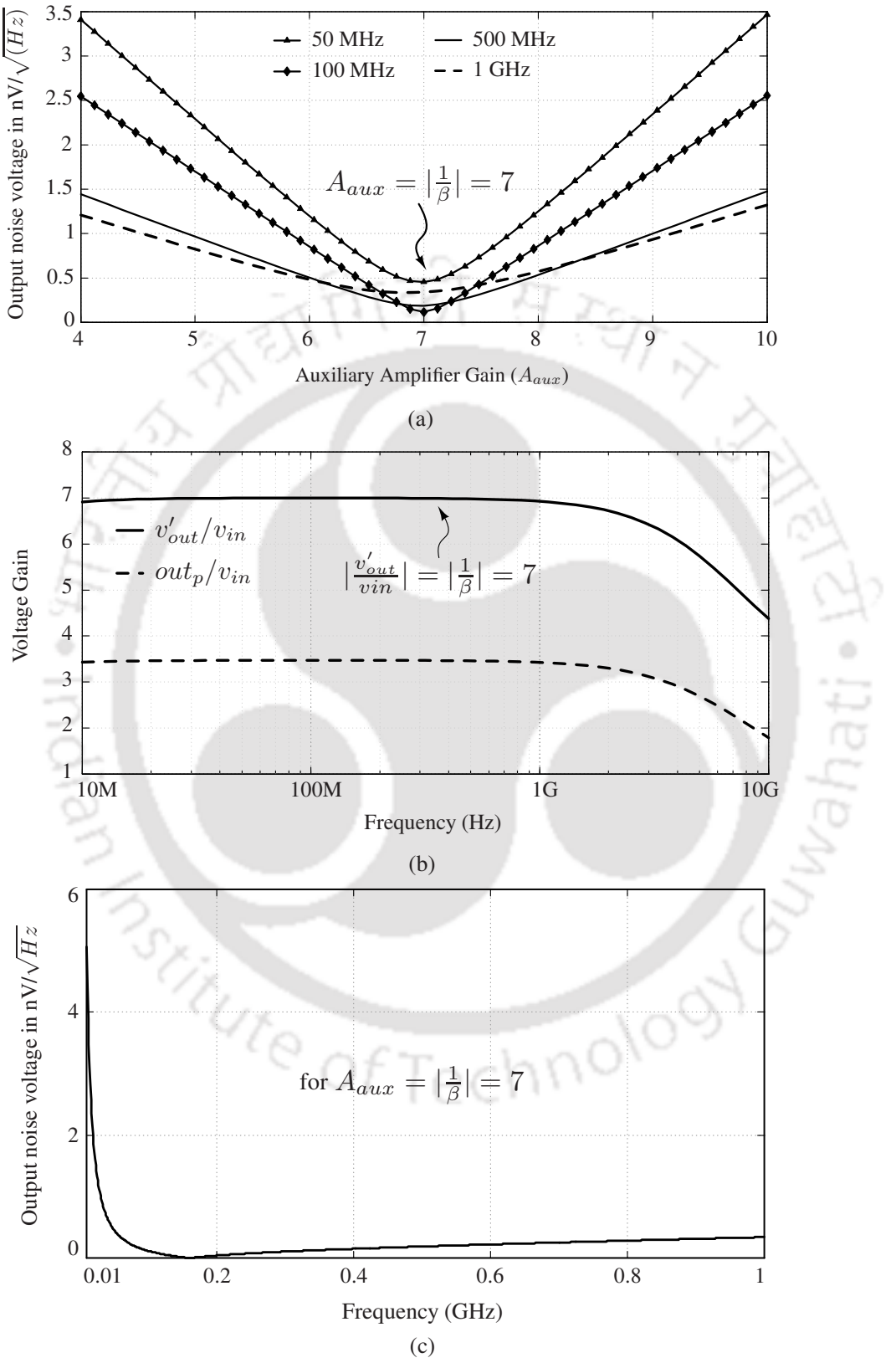



**Figure 2.18:** (a) Variation of output noise voltage of the CG noise-canceling LNA shown in Fig. 2.17 with auxiliary amplifier gain, (b) differential gain of the LNA at the noise-canceling condition and (c) output noise voltage of the LNA with respect to frequency at the NC condition.

Noise analysis is performed on the circuit shown in Fig. 2.17 by sweeping the gain of the auxiliary amplifier $A_{aux}$. Differential output ($v'_{out}$) noise voltage from this analysis is plotted for multiple fixed frequencies and is shown in Fig. 2.18(a). From this figure, it can be observed that the output noise voltage is a minimum for $A_{aux} = |1/\beta| = 7$, which is the noise-canceling condition. Fig. 2.18(b) shows the gain of the implemented CG NC LNA under this condition of noise cancellation. From Fig. 2.18(b), the CG NC LNA has a mid-band gain of 7 ($= |1/\beta|$) under the noise-canceling condition. Both these results verify the proposed theoretical claims for CG NC LNA. Fig. 2.18(c) shows the differential output noise voltage of the CG NC LNA with varying frequency for an auxiliary path gain ($A_{aux}$) of 7. The impedance between $v_{in}$ and $v_e$ node is $R_s + 1/(sC_{DC})$, where $C_{DC}$ is the DC blocking capacitor. While computing the noise-canceling condition, the frequency-varying components were neglected for the purpose of simplification. However, at very low frequencies, the effective noise-canceling condition gets modified from the computed value because of the impedance of the DC blocking capacitor. For this reason, output noise voltage increases at very low frequency. On the higher frequency side, the impact of the parasitic capacitances ($C_{gs}$ and $C_{gd}$) starts to show up, leading to a slight increase in the output noise voltage.

### 2.5.2 A resistive shunt feedback NC LNA

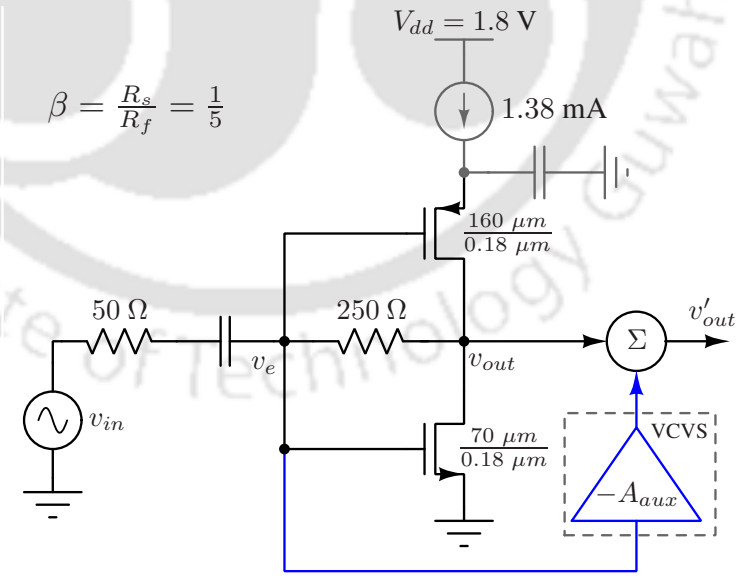



**Figure 2.19:** Simulated RSF noise-canceling LNA.

An RSF noise-canceling LNA, as shown in Fig. 2.19, is designed for simulation. A feedback resistance ($R_f$) of 250 Ω and a source resistance ($R_s$) of 50 Ω are used in the current implementation. From (2.10b),

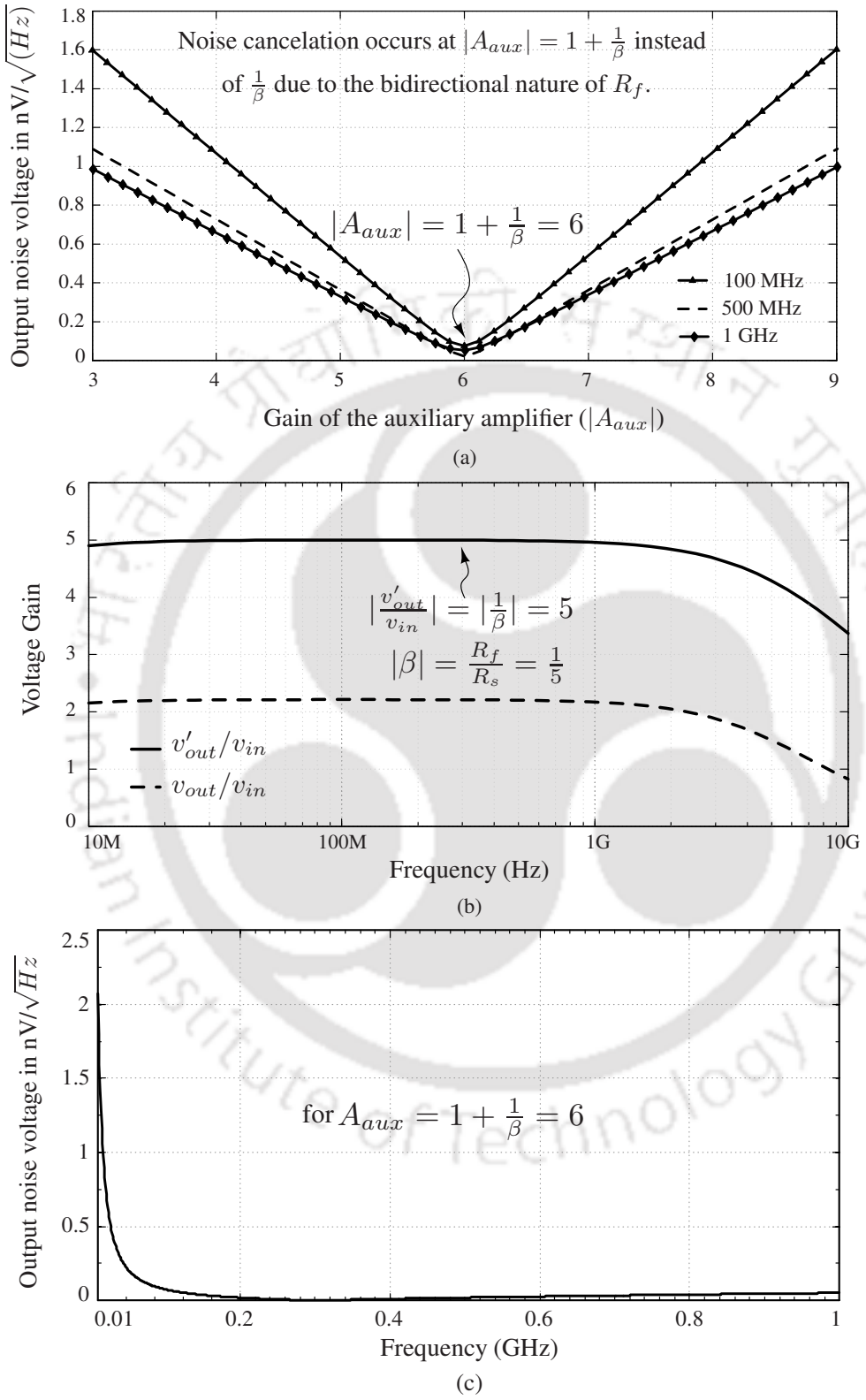



**Figure 2.20:** (a) Variation of output noise voltage of the RSF noise-canceling LNA with auxiliary amplifier gain, (b) gain of the LNA at the noise-canceling condition and (c) output noise voltage of the LNA with respect to frequency at the NC condition.

$|\beta| = R_s/R_f = 1/5$. An inverter is used as a transconductor and is biased such that the input impedance is equal to the source impedance. An auxiliary amplifier $A_{aux}$ is added to the circuit to cancel the noise of the transconductor, as shown in Fig. 2.19.

Noise analysis is performed on the circuit shown in Fig. 2.19 by sweeping the gain of the auxiliary amplifier $A_{aux}$ at multiple fixed frequencies. The resulting output noise voltage from this analysis is shown in Fig. 2.20(a). From this figure, the output noise is a minimum when $A_{aux} = 1 + |1/\beta| = 6$. Fig. 2.20(b) shows the gain of the amplifier under this noise-canceling condition (i.e., $A_{aux} = 1 + |1/\beta| = 6$). From Fig. 2.20(b), the mid-band gain of the implemented RSF noise-canceling LNA is equal to 5 $(= |1/\beta|)$. Fig. 2.20(c) shows the differential output noise voltage of the RSF NC LNA with varying frequency for an auxiliary path gain ($A_{aux}$) of 6. From Fig. 2.20(c), output noise voltage rises for frequencies lower than 100 MHz due to the presence of the DC blocking capacitor. The output noise voltage degrades slightly for high frequencies (towards 1 GHz) because of the parasitic capacitances associated with a MOS transistor.

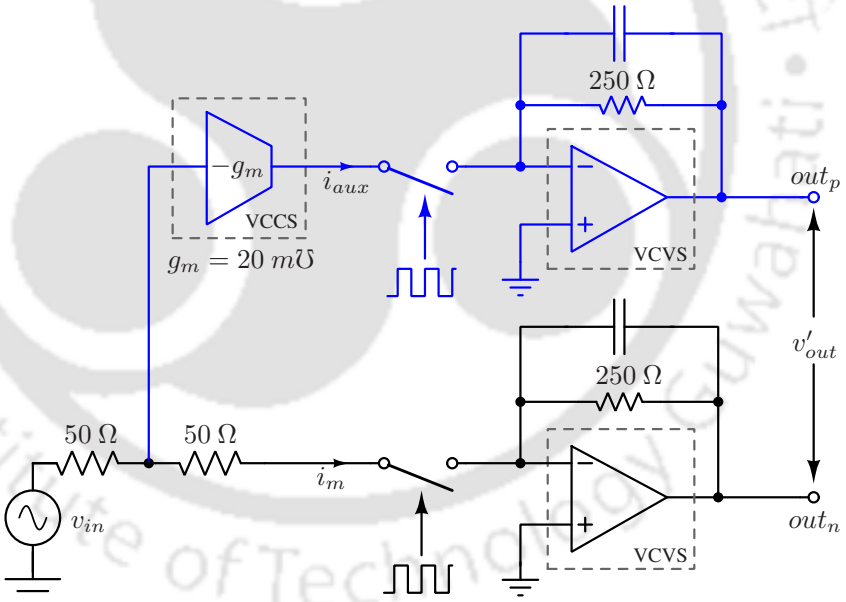



**Figure 2.21:** Simulated noise-canceling receiver.

### 2.5.3 A wideband frequency-translational NC receiver

A frequency translational noise-canceling (FTNC) receiver, as shown in Fig. 2.21, is designed using all ideal elements except for the matching resistor. $R_{in}$ of 50 Ω, $R_m$ of 250 Ω, and $R_{aux}$ of 250 Ω are used in the FTNC implementation. The down-conversion mixer is implemented using an ideal switch. A square wave of 1 GHz is used as the local oscillator signal. The TIA is implemented with the help of a VCVS and a resistor connected

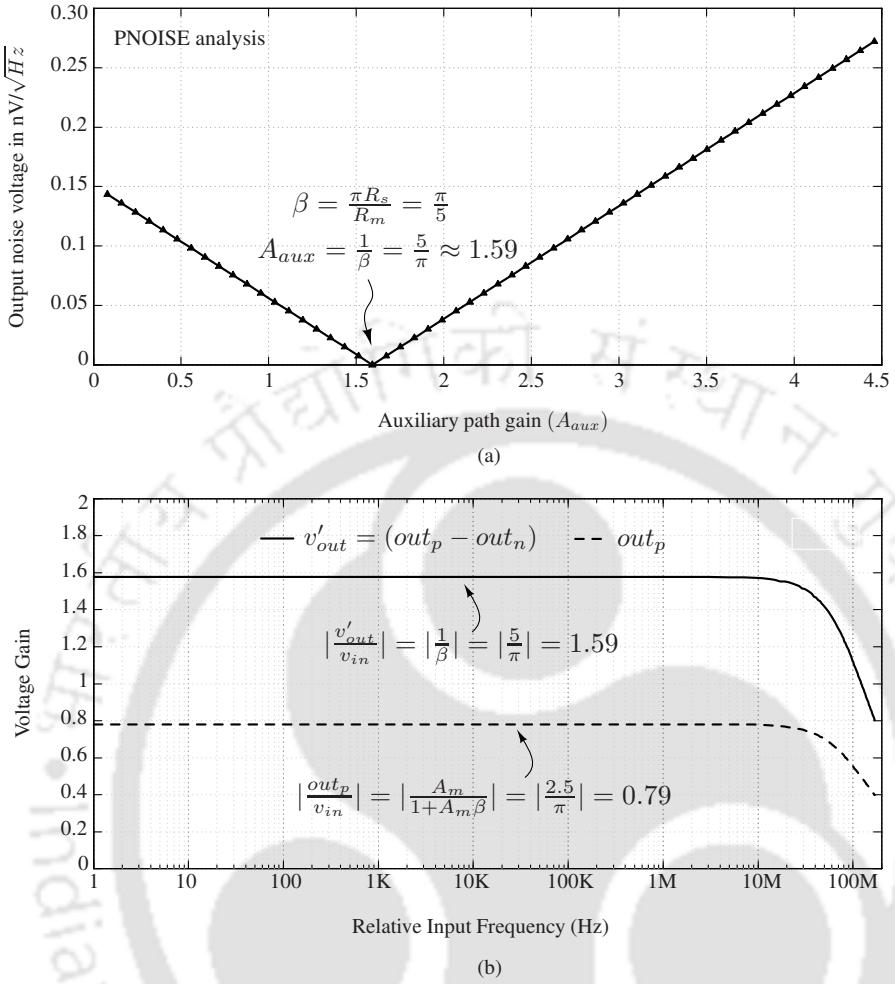



**Figure 2.22:** (a) Variation of the output noise voltage of the NC-receiver with auxiliary path gain, and (b) the overall voltage gain of the NC-receiver at the noise-canceling condition.

across it. The TIA is designed to have a bandwidth of 100 MHz.

Noise analysis is performed on the circuit shown in Fig. 2.21, by sweeping the gain of the transconductor in the auxiliary path. The resulting output noise voltage from this analysis is shown in Fig. 2.22(a). From Fig. 2.22(a), the output noise is a minimum when $A_{aux} = |1/\beta| = |R_m/(\pi R_s)| \approx 1.59$ (when $g_m = 20m\mho$). One can observe that unlike Fig.2.18(a) and Fig. 2.20(a), Fig. 2.22(a) demonstrates absolute zero output noise under the noise-canceling condition. The reason is that, in the NC receiver shown in Fig. 2.21, the matching device is modeled as a single ideal resistor (of 50 Ω) as compared to MOS transistors of 180 nm technology used in the simulated NC LNAs (shown in Fig. 2.17 and Fig. 2.19). Since the ideal resistor does not have any parasitic capacitance associated with it, complete cancellation of the output noise is observed at the NC condition (as shown in Fig. 2.22(a)). Fig. 2.22(b) shows the gain of the receiver under

this noise-canceling condition (i.e., $A_{aux} = |1/\beta| \approx 1.59$). From Fig. 2.22(b), the conversion gain of the noise canceling receiver is equal to $1.59$ $(= |1/\beta|)$.

## 2.6 Summary

In this work, well-known noise-canceling LNAs and receivers have been studied to identify the similarities in their working principle. It is shown that noise-canceling opportunity in all these circuits arises due to the negative feedback in the main path. The expressions for noise-canceling conditions and the overall gains of the NC-circuits are derived. The following claims have been made regarding the operation of noise-canceling circuits.

- Although noise cancellation is often explained as a feedforward technique in literature, the noise-canceling opportunity in existing NC-LNAs has arisen due to the presence of negative feedback in the main amplifier.
- If the feedback factor of the main amplifier is $\beta$, then the gain of the auxiliary amplifier ($A_{aux}$) needed to cancel the noise of the main amplifier is equal to $|1/\beta|$.
- Under this noise-canceling condition (i.e., $A_{aux} = |1/\beta|$), the overall gain of the NC-wideband amplifier, including the source resistance is equal to $|1/\beta|$.
- The above-stated claims are valid even in the case of wideband NC-receivers in which a floating resistor is used for the impedance matching.

The proposed theoretical claims are verified by the design and simulation of three NC circuits (two NC-LNAs and a wideband NC-receiver).

In an NC circuit, complete cancellation of the main path noise depends on the precise selection of the auxiliary path gain. In case of a mismatch between desired gain and the actual gain of the auxiliary path, the overall noise performance will degrade. The effect of noise cancellation can also reduce if there is a phase mismatch between the main and the auxiliary paths. The NC LNA presented in [128] employed reconfigurable phase-tuning lines shown in [129] in both the main and auxiliary paths to achieve optimized noise cancellation over a large bandwidth. Once the main path noise is absolutely canceled, the overall output noise of an NC LNA is just the auxiliary path noise. [73] employed techniques to reduce the noise contribution of the auxiliary path of an NC LNA. Mutual noise cancellation between the main and the auxiliary paths of an LNA is explored in [76]. However, achieving an absolute zero output noise voltage may not be feasible in a practical circuit with all actual components.

भारतीय प्रौद्योगिकी संस्थान गुवाहाटी
Indian Institute of Technology Guwahati

# 3

# Systematic Generation of Flicker and Thermal Noise-Canceling Circuits



**Contents**

## 3.1 Proposed systematic methodology

In the previous chapter, we proposed a generic theory of noise-canceling circuits and developed a few key observations about their operation. The proposed theoretical claims were validated using simulations on existing noise-canceling circuits. It can be observed that, so far, the use of the NC technique has been limited within RF LNAs [11–20, 26, 67, 76, 77, 86, 89–92] and receivers [31, 94–97] only. A major reason behind this low penetration of the noise cancellation technique is the lack of a systematic method for generating NC circuits.

In this work, we present a systematic method for generating noise-canceling circuits. Previous works [130] and [131] presented methods to systematically generate all possible two-transistor transconductors and LNAs, respectively. [127] demonstrated a feedback based analysis of noise-canceling circuits. In the proposed method, rather than starting with elementary circuits and searching for noise cancellation opportunities, we first develop elementary noise-canceling circuit models. In the next step, we provide appropriate input excitations to achieve signal summation at the output. Finally, suitable auxiliary paths are added to cancel the main path's noise while the signal is added at the output.

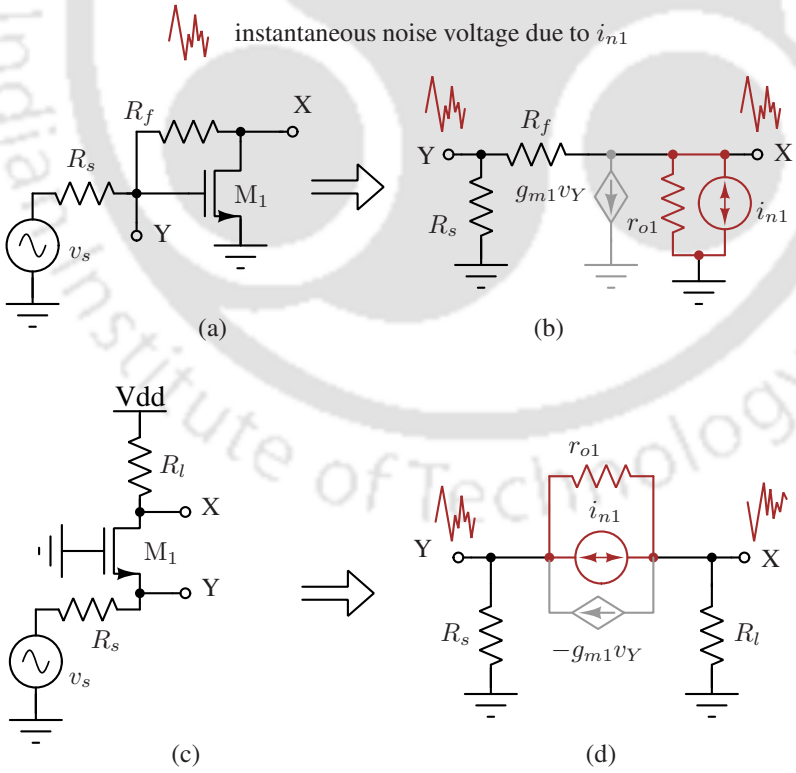



**Figure 3.1:** (a) A shunt feedback amplifier and (b) its noise model. (c) A common-gate amplifier and (d) its noise model. In (b) and (d), only noise due to MOSFET is considered.

Fig. 3.1(a) shows a shunt feedback amplifier, and Fig. 3.1(b) shows its noise equivalent model. Here only the

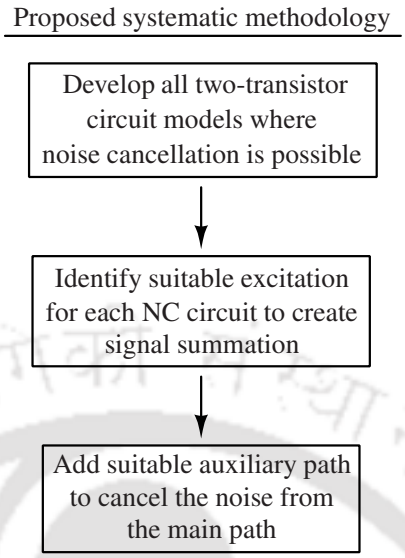



**Figure 3.2:** Proposed systematic methodology for generating noise-canceling circuits.

noise due to the MOS transistor is considered. From Fig. 3.1(b), noise due to $i_{n1}$ can be canceled at the final output by taking a weighted difference of the two voltages $v_X$ and $v_Y$. To benefit from noise cancellation, one needs to excite the shunt-feedback amplifier in a way to create out-of-phase signal voltages at the nodes X and Y. The single-ended excitation, as shown in Fig. 3.1(a), satisfies this condition.

Fig. 3.1(c) and Fig. 3.1(d) show a CG amplifier and its equivalent noise model, respectively. Here also, only the noise due to the MOS transistor is considered. From Fig. 3.1(d), noise due to $i_{n1}$ can be canceled if we take a weighted sum of the voltages $v_X$ and $v_Y$. For noise cancellation to be effective, we need to excite the CG amplifier to create the signal voltages with the same polarity at nodes X and Y. The single-ended excitation $v_s$, as shown in Fig. 3.1(c), satisfies this condition.

One can notice that the equivalent noise models in Fig. 3.1(b) and Fig. 3.1(d) actually corresponds to a single loop with two resistors and a current source (leaving out the dependent current source for now). The only difference between the models in Fig. 3.1(b) and Fig. 3.1(d) is the location of the noisy current source. As there are only three branches (Y-gnd, Y-X, and X-gnd) in the model, we can only construct two different models, as shown in Fig. 3.1(b) and Fig. 3.1(d). The third possibility in which the noisy current source will be from Y to gnd is similar to the model in Fig. 3.1(b).

It is observed that only two noise-canceling models are possible when the circuit has a single noise source. Both these noise models have been explored in the literature. In this work, we explore noise-canceling possibility in circuits having two noise sources present within a single circuit loop. Overall, the key steps of the proposed

systematic methodology can be summarized, as shown in Fig. 3.2. The first step of the systematic method is to generate all two-transistor circuit models where noise cancellation is possible. Once the suitable two-transistor models are chosen, appropriate signal excitation is applied to the circuits to ensure signal summation at the output. Finally, suitable auxiliary paths are added to cancel noise from the main path.

### 3.1.1 Generating two-transistor noise models

In this section, we systematically generate all possible two-transistor noise models. If we insert one more noisy current source into the three-node (X, Y, and gnd) model shown in Fig. 3.1, three different circuit models, as shown in Fig. 3.3, can be generated.

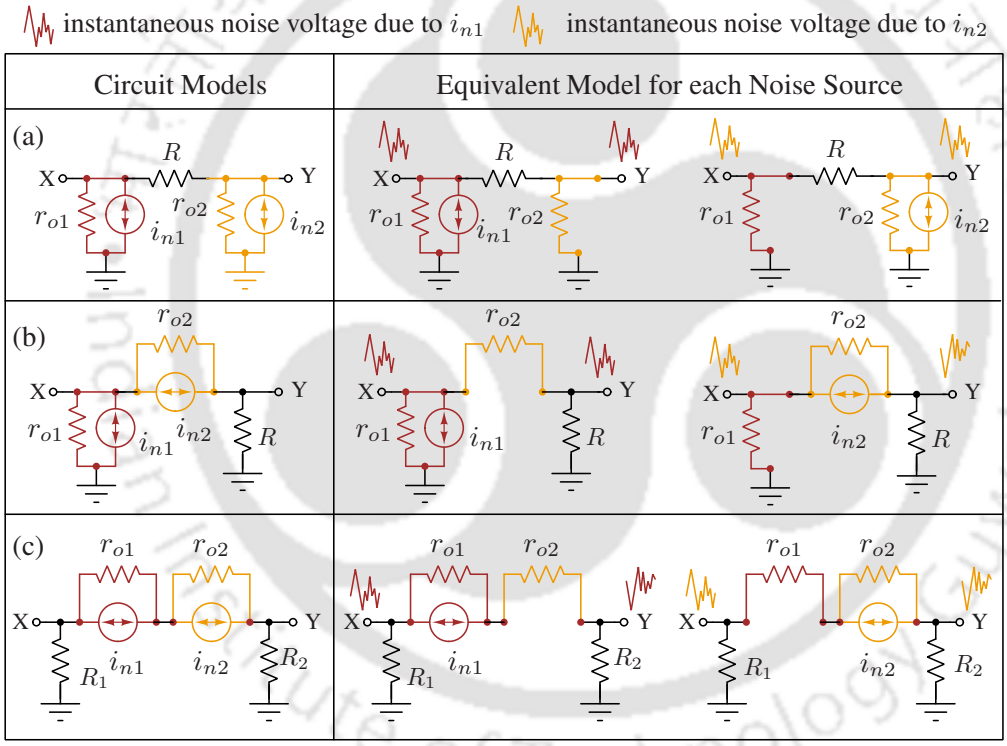



**Figure 3.3:** Three possible noise models of two transistor circuits.

If we replace the resistance $R_s$ in Fig. 3.1(b) with a noisy current source, we get the circuit model shown in Fig. 3.3(a). The noise voltages at X and Y have the same polarity. If we take a weighted difference of the voltages $v_X$ and $v_Y$, we can cancel the noise. Interestingly, noise due to both $i_{n1}$ and $i_{n2}$ can be canceled but may require different weights for perfect cancellation. For the noise-canceling technique to be effective, one needs to excite this circuit to create out-of-phase signal voltages at X and Y.

If we replace the resistance $R_s$ in Fig. 3.1(d) with a noisy current source, we get the circuit model shown in

Fig. 3.3(b). Unlike the model in Fig. 3.3(a), the noise voltages at X and Y in this circuit have the same polarity due to $i_{n1}$ but opposite polarity due to $i_{n2}$. Therefore in the circuits derived from this model, if we design the circuit to cancel the noise due to $i_{n1}$, the effect of $i_{n2}$ will be enhanced at the output and vice versa.

The third possible circuit model is shown in Fig. 3.3(c). In this circuit, both the current sources are in series and are in the X-Y branch. Even though this is not exactly a three-node model, it also provides an opportunity to cancel the noise due to both the noisy current sources $i_{n1}$ and $i_{n2}$. As shown in Fig. 3.3(c), the noise voltages at nodes X and Y due to $i_{n1}$ (and $i_{n2}$) have opposite polarities. If we take a weighted sum of the voltages $v_X$ and $v_Y$, we can cancel the noise. Similar to the circuit model in Fig. 3.3(a), here also the noise due to both $i_{n1}$ and $i_{n2}$ can be canceled but may require different weights for perfect cancellation. To be benefited from the noise cancellation, one needs to excite this circuit to create in-phase signal voltages at nodes X and Y.

### 3.1.2 Construction of circuits from the derived models

Frequently-used noise-canceling circuits, such as NC LNAs [11,13,16] and receivers [31,94], have one thing in common. These circuits have a low input impedance to satisfy the criterion of input impedance matching. However, the noise-canceling possibility has not been explored in circuits having a high input impedance. In this work, we systematically explore noise-canceling circuits belonging to either of the following two categories: circuits having a high input impedance and circuits having a low input impedance.

Once the suitable models for noise cancellation are chosen, the noise current sources within these models are first replaced with MOS transistors. Next, appropriate input excitation is given to the MOS transistors to maintain desired signal operation. Finally, an auxiliary path is properly added to cancel the main path's noise while the signals from both paths get added at the final output. For generating noise-canceling circuits with high input impedance, the input signals are applied to the gate terminals of the MOS transistors. Similarly, NC circuits with low input impedance can be generated by applying inputs to the source terminals of the MOS transistors (employing a shunt-feedback-based common-source structure is another possibility).

## 3.2 Generating NC circuits with high input impedance

In this section, our main focus is to generate noise-canceling circuits with high input impedance using the two-transistor noise models derived in section 3.1.1. To construct circuits corresponding to the model shown in Fig. 3.3(a), the noisy current sources $i_{n1}$ and $i_{n2}$ need to be replaced with MOS transistors. As we can use either nMOS or pMOS transistors for $i_{n1}$ and $i_{n2}$, we get four possible two-transistor circuits as shown in Fig. 3.4. From the discussion in section 3.1.1, one can recall that the noise voltages at X and Y in these circuits will have

the same polarity. For the noise-canceling technique to be effective, we need to excite these circuits to create out-of-phase signal voltages at X and Y.

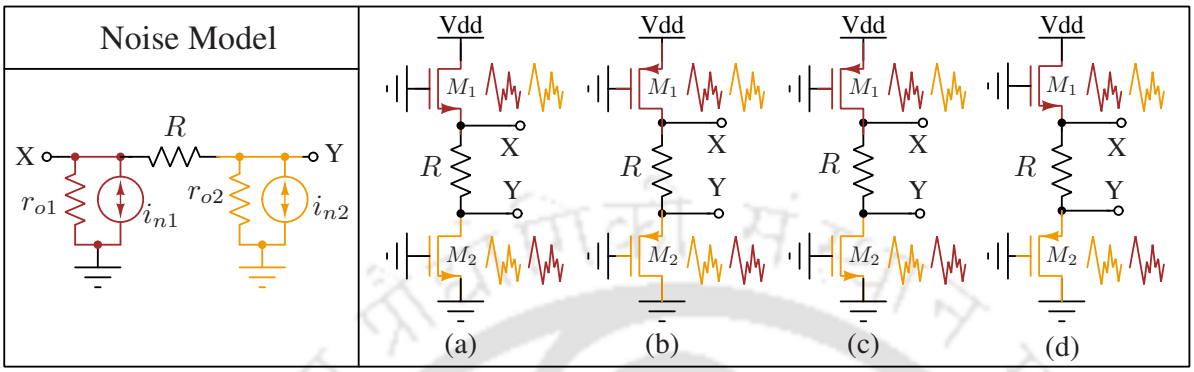



**Figure 3.4:** Four possible noise-canceling circuits that are derived from the noise model shown in Fig. 3.3(a).

In Fig. 3.4(a), the top nMOS transistor is in common-drain (CD) configuration and the bottom nMOS transistor is in common-source (CS) configuration. To create out-of-phase signal voltages at X and Y in Fig. 3.4(a), one can apply the same input signal to the gates of both the nMOS transistors (gate bias voltages may be different). The complete circuit with input and output signal polarities is shown in Fig. 3.5(a). One can notice that this circuit can be seen as a balun amplifier with unequal amplitudes. Fig. 3.4(b) is a pMOS version of the circuit topology shown in Fig. 3.4(a), and the complete circuit (with signal and noise polarities) is shown in Fig. 3.5(b).

The circuits in Fig. 3.4(c) and Fig. 3.4(d) use one nMOS and one pMOS transistors. In Fig. 3.4(c), both the transistors are in CS configuration and therefore act as amplifiers. The transistors in Fig. 3.4(d) are in CD configuration and thus act as source followers. To create the out-of-phase signals at X and Y, the circuits in Fig. 3.4(c) and Fig. 3.4(d) need to be excited with differential input signals as shown in Fig. 3.5(c) and Fig. 3.5(d), respectively. The circuit in Fig. 3.5(c) is a fully differential amplifier, and the circuit in Fig. 3.5(d) is a fully differential buffer. In all the circuits shown in Fig. 3.5, the instantaneous noise voltages at X and Y are in-phase, and the signal voltages at X and Y are in out-of-phase. To cancel the noise, one can combine the voltages from X and Y with the help of two amplifiers (or attenuators), $A_1$ and $A_2$, as shown in Fig. 3.6. The main circuit in Fig. 3.6 can be any one of the circuits shown in Fig. 3.5.

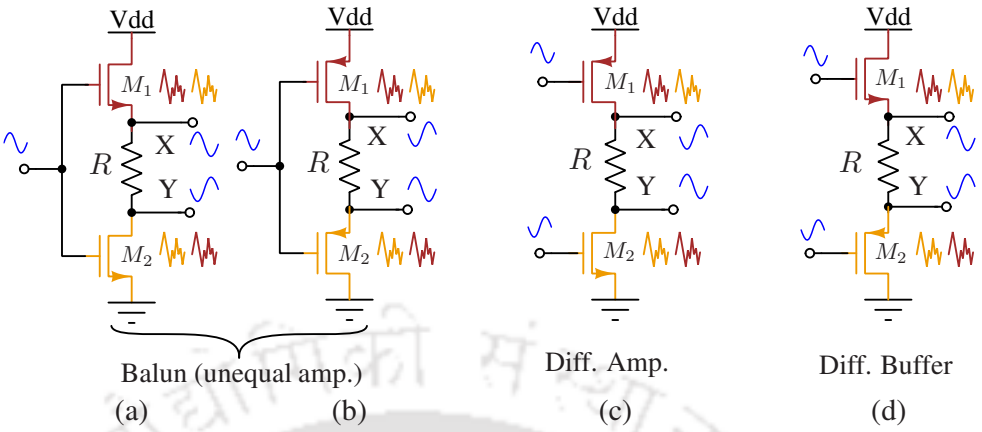



**Figure 3.5:** Noise-canceling circuits with proper excitation to achieve signal summation. (a) and (b) are balun amplifiers, (c) is a fully differential amplifier, and (d) is a fully differential buffer.

### 3.2.1 Deriving the noise-canceling condition

In all the circuits derived from the model given in Fig. 3.3(a), the instantaneous noise voltages $v_{X,n}$, $v_{Y,n}$ at the nodes X and Y can be shown to be

$$v_{X,n} = \frac{(R + r_{o2})r_{o1}}{r_{o1} + r_{o2} + R}\, i_{n1} + \frac{r_{o2}r_{o1}}{r_{o1} + r_{o2} + R}\, i_{n2}, \tag{3.1a}$$

$$v_{Y,n} = \frac{r_{o1}r_{o2}}{r_{o1} + r_{o2} + R}\, i_{n1} + \frac{(R + r_{o1})r_{o2}}{r_{o1} + r_{o2} + R}\, i_{n2}. \tag{3.1b}$$

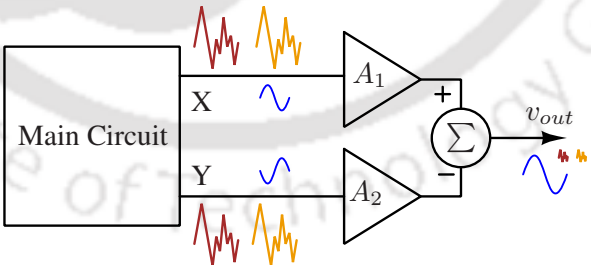



**Figure 3.6:** Amplifiers (or attenuators) $A_1$ and $A_2$ provide the scaling factors required to cancel the noise. Main circuit can be any one of the circuits shown in Fig. 3.5.

To cancel the noise at the final output, one has to use the additional amplifiers shown in Fig. 3.6. The output

noise voltage $v_{out,n}$ in Fig. 3.6 is given by

$$\begin{aligned} v_{out,n} &= A_1 v_{X,n} - A_2 v_{Y,n} \\ &= \frac{(A_1 - A_2) r_{o1} r_{o2} + A_1 r_{o1} R}{r_{o1} + r_{o2} + R}\, i_{n1} + \frac{(A_1 - A_2) r_{o1} r_{o2} - A_2 r_{o2} R}{r_{o1} + r_{o2} + R}\, i_{n2}. \end{aligned} \tag{3.2a}$$

From (3.2a), it can be observed that the noise voltage due to $i_{n1}$ can be canceled entirely if $A_1/A_2 = r_{o2}/(r_{o2} + R)$. Similarly, the noise voltage due to $i_{n2}$ can be canceled entirely if $A_1/A_2 = (r_{o1} + R)/r_{o1}$. It can be observed that for any non-zero value of $R$, $\frac{r_{o2}}{(r_{o2}+R)} < 1$ and $\frac{(r_{o1}+R)}{r_{o1}} > 1$. Hence both the conditions for noise cancellation cannot be satisfied simultaneously. In the present analysis, both $A_1$ and $A_2$ are assumed to be ideal noiseless amplifiers. In a practical scenario, the overall noise performance of the circuit after the cancellation of main circuit noise is limited by the noise contribution of $A_1$ and $A_2$.

### 3.2.2 Simulation results

The circuits in Fig. 3.5 are simulated in a CMOS 65 nm technology to verify the noise cancellation in the derived circuits. The amplifiers $A_1$ and $A_2$ are implemented using ideal voltage-controlled voltage sources (VCVS).

#### 3.2.2.1 Noise-canceling differential amplifier

The circuit in Fig. 3.5(c) is designed to verify the flicker and thermal noise cancellation at the output. Fig. 3.7(a) shows the final circuit operating on a 1.2 V supply voltage. The differential input signal is assumed to have a DC common-mode voltage of 0.6 V. The circuit consumes 18 $\mu$A of current. The resistance values as per the noise model in Fig. 3.3(a) are $r_{o1} = 89$ k$\Omega$, $r_{o2} = 43$ k$\Omega$ and $R = 40$ k$\Omega$. From (3.2a), noise due to $M_1$ can be completely canceled if we choose $A_1/A_2 = r_{o2}/(r_{o2} + R) = 0.5$. Otherwise, noise due to $M_2$ can be completely canceled if we choose $A_1/A_2 = (r_{o1} + R)/r_{o1} = 1.44$. To verify the mentioned noise-canceling conditions, $A_1/A_2$ is varied, and the input-referred noise at 1 Hz is plotted in Fig. 3.7(b). One can observe the noise-canceling conditions when only one of $i_{n1}$ and $i_{n2}$ is present. If noise currents due to both M1 and M2 are present, output noise voltage is minimized if we choose $A_1/A_2 = 0.76$.

Fig. 3.8(a) shows the voltage gain at X, Y, and at the final noise-canceled output when $A_1/A_2 = 0.76$. Fig. 3.8(b) shows the input-referred noise of the circuit with (at output) and without (at X or Y) noise cancellation. From Fig. 3.8(b), one can observe that both flicker and thermal noises can be canceled in this derived circuit.

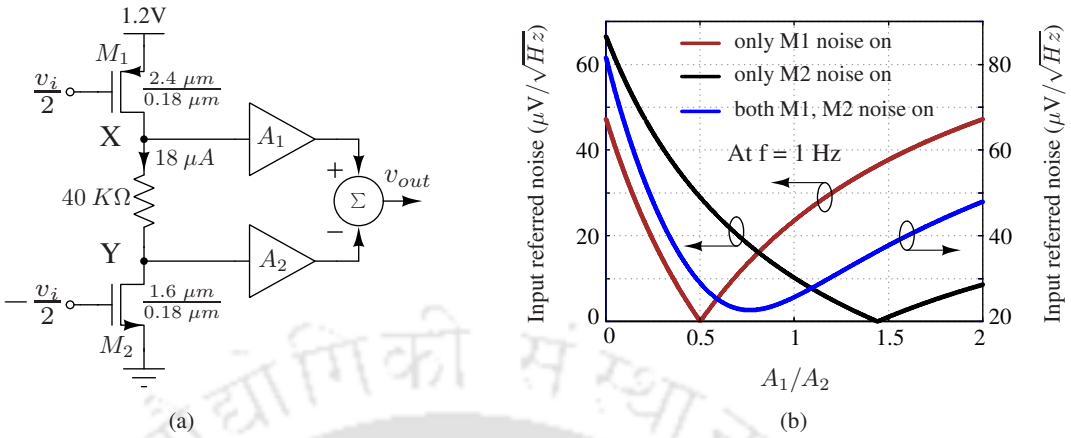



**Figure 3.7:** (a) A noise-canceling differential amplifier. (b) The input referred noise voltage of the differential amplifier at 1 Hz with varying $A_1/A_2$ ratio.

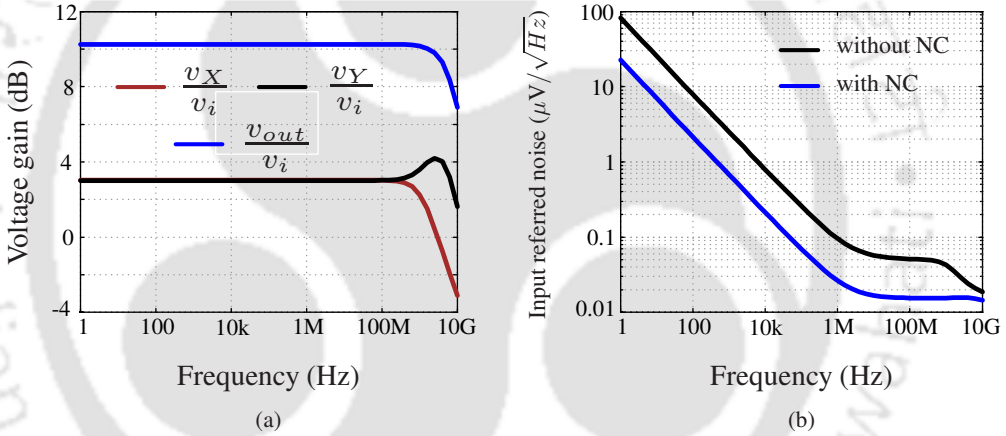



**Figure 3.8:** (a) Voltage gain at X, Y and final output for the NC differential amplifier. (b) Input referred noise voltage of the differential amplifier with and without noise cancellation.

### 3.2.2.2 Noise-canceling differential buffer

A noise-canceling differential buffer is designed based on the circuit topology presented in Fig. 3.5(d). The final circuit, with all component values and biasing, is shown in Fig. 3.9(a). Since the potential application of this NC buffer is as an output stage for measurements, differential output $(v_X - v_Y)$ without any extra circuitry is preferred. For the sake of completeness, the scaling factors $A_1$ and $A_2$ are varied, and the input-referred noise voltage is plotted in Fig. 3.9(b).

The circuit is designed to offer 50 Ω output impedance at the nodes X and Y. Fig. 3.9(c) shows the $|S_{22}|$ at the nodes X and Y. Fig. 3.10(a), and Fig. 3.10(b) show the voltage gain and noise figure (NF) of the circuit. From Fig. 3.10(b), one can observe that the NF is significantly lower when differential output is considered.

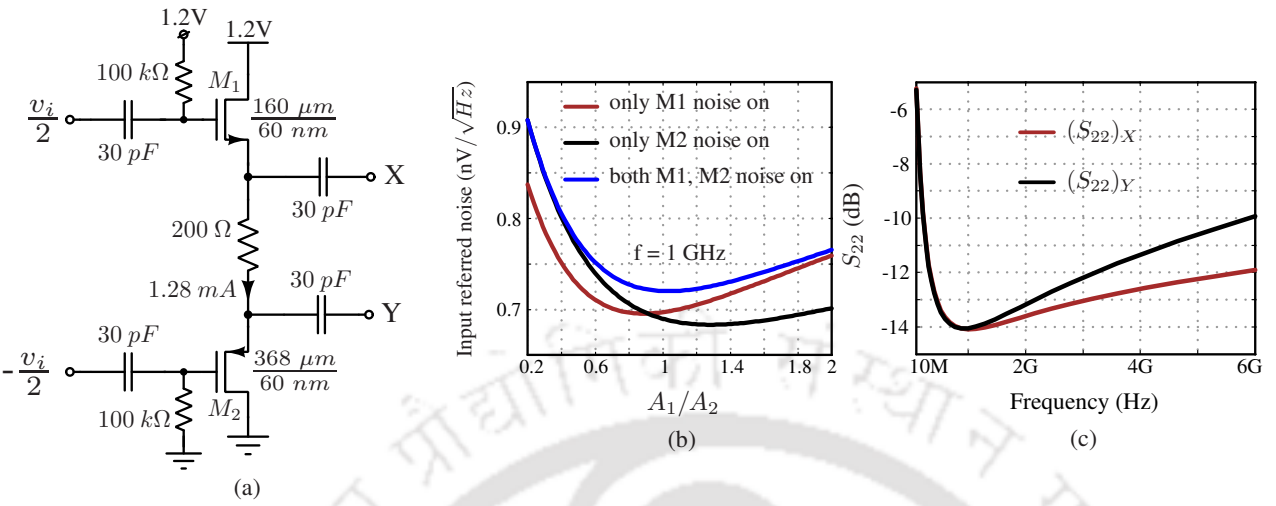



**Figure 3.9:** (a) Noise-canceling differential buffer, (b) noise-canceling condition, and (c) $|S_{22}|$ plots at its differential output nodes.

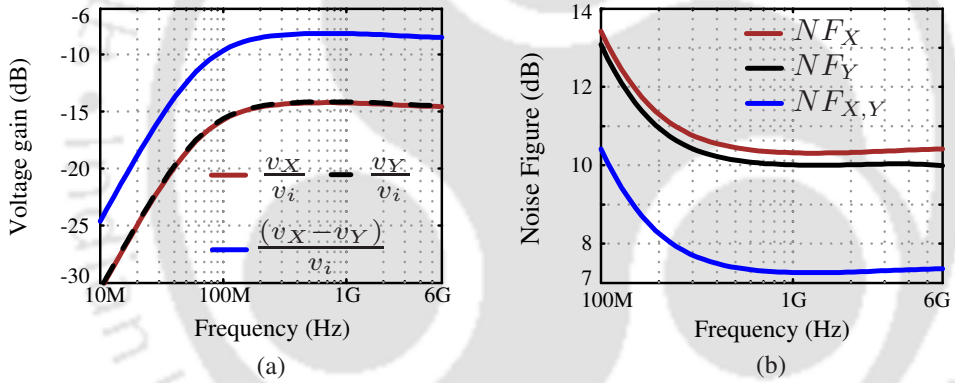



**Figure 3.10:** (a) Voltage gain at the two differential outputs of the NC buffer, (b) single-ended NF at the nodes X, Y and the NF when the output is differential.

### 3.2.2.3 Noise-canceling balun amplifier

The circuit shown in Fig. 3.5(a) is designed to operate on a 1.2V supply voltage. Fig. 3.11(a) shows the balun amplifier with the component values and bias. The circuit consumes a DC current of 133 $\mu$A. The resistance values as per the noise model are $r_{o1} = 1/g_{m1} = 0.55$ kΩ, $r_{o2} = 14$ kΩ and $R = 4$ kΩ.

From (3.2a), the noise due to $M_1$ can be completely canceled if we choose $A_1/A_2 = r_{o2}/(r_{o2} + R) = 0.77$. The noise due to $M_2$ can be completely canceled if we choose $A_1/A_2 = (R + r_{o1})/r_{o1} \approx 8.2$. To verify these noise-canceling conditions, $A_1/A_2$ is varied, and the input-referred noise voltage at 200 kHz is plotted in Fig. 3.11(b). Fig. 3.11(b) verifies the derived noise-canceling conditions. If the noise currents due to both M1 and M2 are present, output noise voltage is minimized when $A_1/A_2 = 4$.

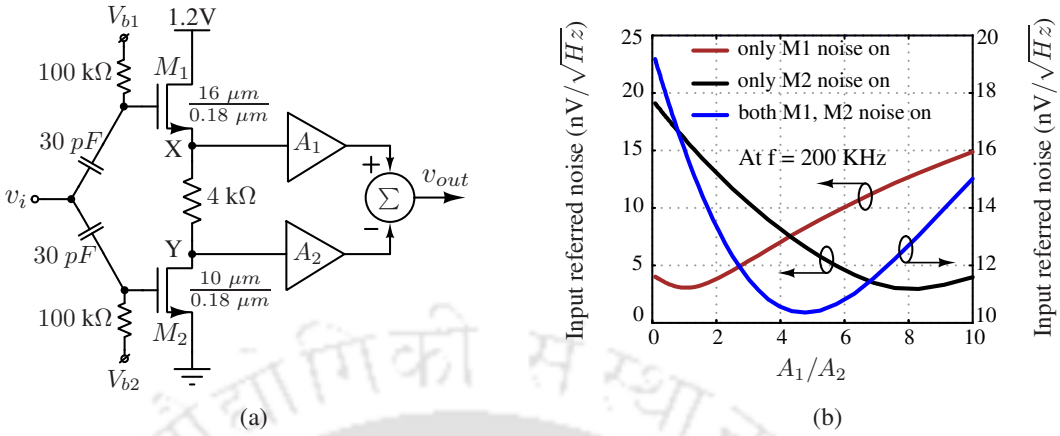



**Figure 3.11:** (a) Noise-canceling balun amplifier, (b) Condition of noise cancellation for the circuit shown in Fig. 3.11(a).

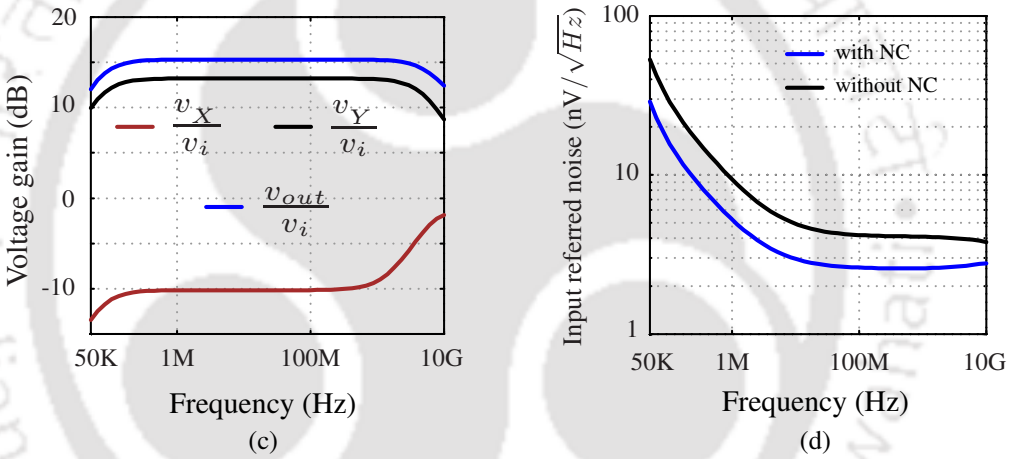



**Figure 3.12:** (a) Voltage gain at X, Y and final output of the circuit shown in Fig. 3.11(a), and (b) input referred noise voltage with and without noise cancellation for the same circuit.

Fig. 3.12(a) shows the voltage gain at nodes X, Y, and output for the circuit shown in Fig. 3.11(a) when $A_1/A_2 = 4$ ($A_2 = 1$ and $A_1 = 4$). As expected, $v_Y$ is an amplified version of the input, and $v_X$ is an attenuated version of the input. The input-referred noise voltage with and without noise cancellation is shown in Fig. 3.12(b).

## 3.3 Generating NC circuits with low input impedance

This section focuses on generating noise-canceling circuits with low input impedance. For achieving low input impedance, one may apply an input signal to the source node of a common-gate (CG) circuit. We observed that the noise model, shown in Fig. 3.3(a), is not suitable for designing amplifiers with a CG configuration because of the position of the input transconductors in the current-reused signal chain. Moreover, one possible

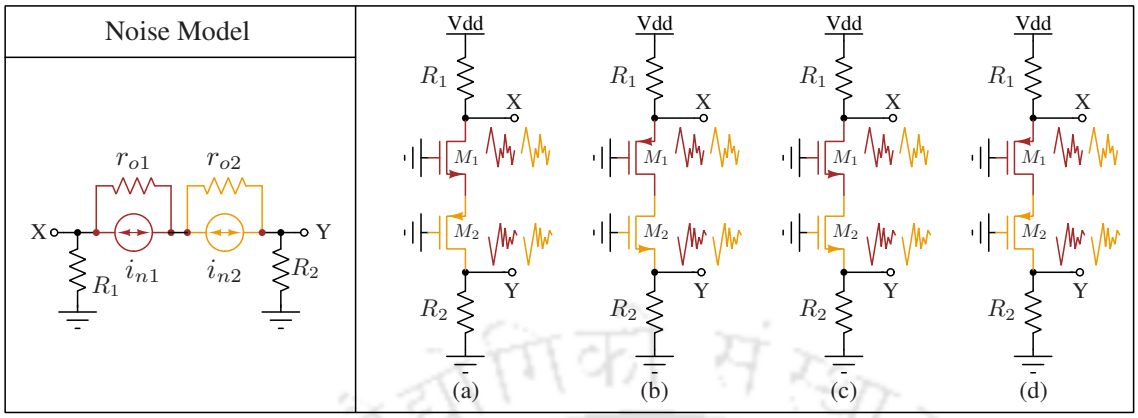



**Figure 3.13:** Four possible noise-canceling circuits that are derived from the noise model shown in Fig. 3.3(c).

demerit of the noise model shown in Fig. 3.3(b) was identified in section 3.1.1. The drawback is that the noise from one noise source gets canceled while the other source's noise gets added at the output. Hence, the model in Fig. 3.3(b) is not beneficial. The model shown in Fig. 3.3(c) is explored further to generate new noise-canceling circuits with low input impedance. To construct the circuits from the model shown in Fig. 3.3(c), one can replace the noisy current sources $i_{n1}$ and $i_{n2}$ with transistors. Therefore, four possible two-transistor circuits, as shown in Fig. 3.13, is obtained.

In the circuits shown in Fig. 3.13, input signals can be applied to one or more of the following three terminals: X, Y, or the intermediate node (let us denote the intermediate node as Z). Using this method on the models shown in Fig. 3.13, one can develop the circuits shown in Fig. 3.14(a)-3.14(d). In the amplifier topology given in Fig. 3.14(a), the input is applied to Z, while the output is available at both X and Y. The nodes X and Y can be combined to get the advantage of current-reuse. Fig. 3.14(b) is similar to Fig. 3.14(a), with the locations of the pMOS and nMOS transistors interchanged. In Fig. 3.14(b), the input is simultaneously given to both X and Y to achieve transconductance advantage, while the output is taken from Z. In the circuit shown in Fig. 3.14(c), the input is given at Y, and output is taken from X. The circuit, shown in Fig. 3.14(d), is a pMOS version of Fig. 3.14(c). All the circuits, shown in Fig. 3.14(a)-3.14(d), can work as an amplifier with low input impedance. The circuits shown in Fig. 3.14(a)-3.14(d) can be used to develop noise-canceling LNAs by adding suitable auxiliary amplifiers. Fig. 3.14(e) shows the architecture of a noise-canceling LNA where the main amplifier can be anyone from Fig. 3.14(a)-3.14(d). In Fig. 3.14(e), the amplifiers $A_1$ and $A_2$ serve as auxiliary stages of the noise-canceling LNA.

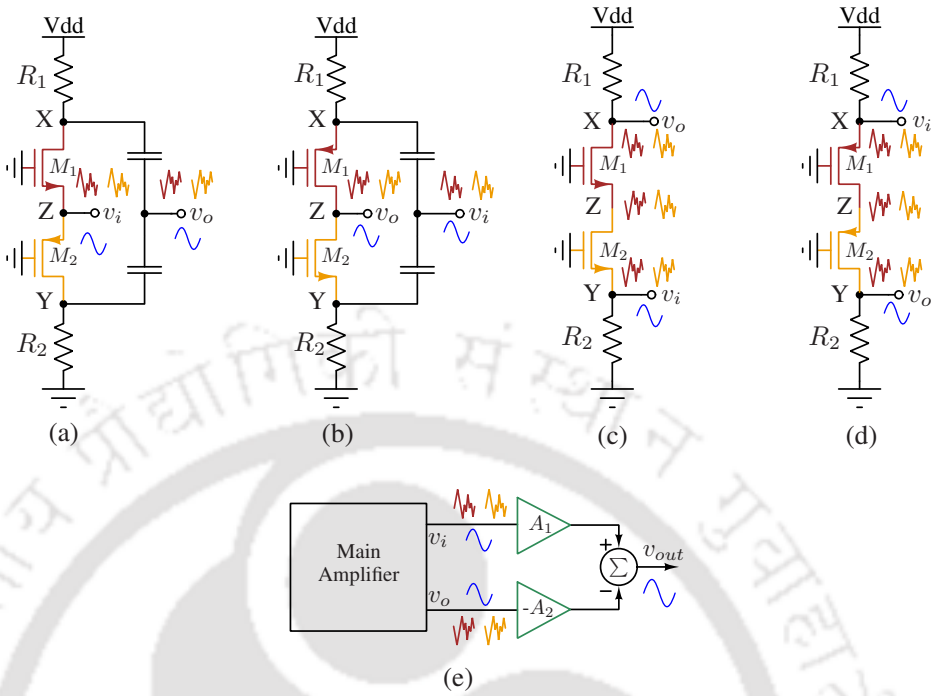



**Figure 3.14:** (a) Circuit developed from Fig. 3.13(a) with input excitation at Z and output taken from both X and Y. (b) Circuit developed from Fig. 3.13(b) with input excitation given at both X and Y while output is taken from Z. (c) Circuit developed from Fig. 3.13(c) with input excitation at Y and output taken from X. (d) A pMOS version of the circuit shown in Fig. 3.14(c). (e) Generic amplifiers $A_1$ and $A_2$ provide the scaling factors required to ensure noise cancellation. The main amplifier can be any one of the amplifiers shown in Fig. 3.14(a) - 3.14(d).

### 3.3.1 Analyzing the developed NC circuits with low input impedance

In the NC LNA architecture shown in Fig. 3.14(e), the gains of $A_1$ and $A_2$ need to be appropriately set to cancel the main amplifier's noise. The main amplifier can be any one of the amplifiers shown in Fig. 3.14(a)-3.14(d). The instantaneous noise voltage at the $v_{out}$ node of the NC LNA (as shown in Fig. 3.14(e)) is

$$v_{out,n} = A_1 v_{i,n} + A_2 v_{o,n}, \tag{3.3a}$$

where $v_{i,n}$ and $v_{o,n}$ are the instantaneous noise voltage at the input and output node of the main amplifier.

Let us consider the main amplifier is the one shown in Fig. 3.14(a). For the noise current $i_{n1}$, the instantaneous noise voltage generated at the input and output node of the main amplifier is

$$v_{i,n1} \approx i_{n1} R_i,$$

$$v_{o,n1} \approx -i_{n1} R_o,$$

where $R_i$ and $R_o$ represent the input and output node resistances of the main amplifier. From equation (3.3a),

the instantaneous noise current $i_{n1}$ can be canceled at the $v_{out}$ node if

$$\frac{A_1}{A_2} \approx \frac{R_o}{R_i}. \tag{3.5a}$$

A similar analysis shows that the instantaneous noise current $i_{n2}$ can be canceled at the final output for the same gain setting of the auxiliary amplifiers (as given in equation (3.5a)). Therefore, in an NC LNA designed using the amplifier in Fig. 3.14(a), noise due to both $i_{n1}$ and $i_{n2}$ can be simultaneously canceled at the final output. It can be shown that noise due to $i_{n1}$ and $i_{n2}$ can also be simultaneously canceled if the main amplifier is as shown in Fig. 3.14(b).

The amplifier topologies given in Fig. 3.14(c) and 3.14(d) are well-known cascode common-gate LNAs in the literature [12]. In these LNAs, the cascode device has a significant noise contribution [12]. If noise cancellation is attempted on the amplifier shown in Fig. 3.14(c), the noise due to $i_{n2}$ (which corresponds to the matching device $M_2$) can be canceled for a noise-canceling condition similar to equation (3.5a). However, it can shown that the condition for canceling $i_{n1}$ noise (which corresponds to the cascode device $M_1$) would be different. As a result, the noise due to both $i_{n1}$ and $i_{n2}$ cannot be simultaneously canceled. The amplifier in Fig. 3.14(d) has identical noise performance as the one in Fig. 3.14(c).

Therefore, the amplifier topologies, as shown in Fig. 3.14(a) and 3.14(b), are good candidates for noise cancellation. Also, they have the extra advantage of current reuse, which makes them suitable for low-power operation. The next chapter further explores the amplifier topologies in Fig. 3.14(a) and 3.14(b) to design low-power noise-canceling LNAs.

## 3.4 Summary

The majority of the two-transistor amplifiers presented in this chapter employ both the transistors either in CS or in CG configuration. However, the CS+CG cascode [132] is another frequently-used amplifier topology in the literature. Cascode topology provides many advantages, such as increased output impedance and improved output-input isolation [132]. Because of these advantages, cascode topology has been widely used in the design of various LNAs [133–136]. The LNA presented in [77] has employed cascode topology in the auxiliary stage of a noise-canceling LNA. Finally, the main idea of this work was to explore new amplifier topologies where noise cancellation can be done.

A systematic methodology for generating new noise-canceling circuits is developed and presented in this chapter. Three new NC circuits having high input impedance are derived, designed, and simulated using

the proposed systematic method. Additionally, architectures of noise-canceling circuits having low input impedance are developed. The proposed systematic approach may be extended further to derive many more new noise-canceling circuits.

Indian Institute of Technology Guwahati

# 4

# A Low-Power Partial Noise-Canceling Complementary Common-Gate LNA

**Contents**

## 4.1 Developing low-power partial noise-canceling common-gate LNA

Chapter 1 presented a brief overview of low-power wideband LNAs in the literature. It was observed that a majority of the low-power LNAs in the literature [20, 36, 37, 41, 43, 51, 62, 137–139] either offer a high noise figure or suffer from a poor linearity performance. This chapter investigates the design of low-power wideband LNAs with an optimized noise and linearity performance.

In noise-canceling (NC) LNAs, the noise of the auxiliary amplifier is not canceled [13, 14]. Therefore, the overall noise performance of an NC LNA is determined by the noise contribution of the auxiliary amplifier [13,14]. To achieve the best noise performance, noise of the auxiliary amplifier needs to be minimized. For this, the auxiliary amplifier needs to consume significantly higher power than the main amplifier [13–15, 17–20, 26, 67, 76]. However, the primary motivation of this work is to design a low-power LNA with optimized noise performance rather than LNAs consuming high power to achieve the best noise performance. In order to achieve low-power operation, the auxiliary amplifier also needs to operate at low power levels.

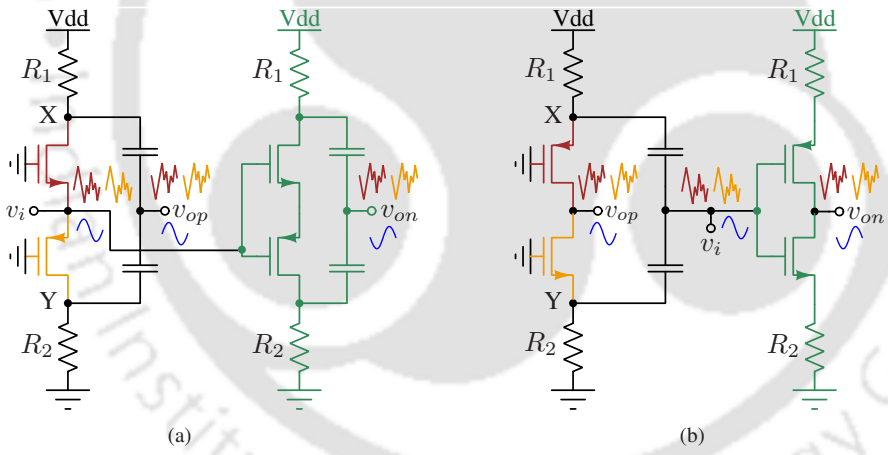



**Figure 4.1:** (a) A single-ended input and differential-output noise-canceling LNA derived from Fig. 3.14(a). (b) A single-ended input and differential-output noise-canceling LNA derived from Fig. 3.14(b). In both the LNAs given in (a) and (b), the auxiliary amplifier is identical to the main amplifier.

In the previous chapter, amplifier topologies given in Fig. 3.14(a) and 3.14(b) were identified as potential candidates for designing noise-canceling LNAs. Using the circuits shown in Fig. 3.14(a) and 3.14(b), two low-power NC LNAs having a single-ended input and differential-output are derived. The derived LNAs are shown in Fig. 4.1(a) and 4.1(b). In the LNA topologies presented in Fig. 4.1(a) and 4.1(b), the auxiliary amplifiers are identical to main amplifiers. Other amplifier structures like a CS amplifier can also be used as the auxiliary stage. However, the current-reused structure shown in Fig. 4.1 is preferred in this work because of low-power consumption. Moreover, the complementary structure employed in the auxiliary stage

has the potential to achieve high linearity, which will be discussed later. In case of differential input, the topologies presented in Fig. 4.1(a) and 4.1(b) can be developed into two fully differential NC LNAs as shown in Fig. 4.2(a) [140] and 4.2(b), respectively. The same MOSFET that provides input matching as a CG amplifier (i.e., the main amplifier) also works as an auxiliary CS amplifier for the differential path. As a result, the main amplifier noise is not completely canceled in these architectures. However, compared to a differential CG LNA, these LNAs provide an improved noise performance because of partial noise cancellation. A circuit similar to Fig. 4.2(b) was also reported in [62]. In [62], $R_1$ and $R_2$ are implemented using current sources to accommodate lower supply voltage. However, current sources are generally more nonlinear than resistors and degrade the linearity performance of the LNA given in Fig. 4.2(b). The load resistance of the LNA in Fig. 4.2(b) is approximately the drain-to-source resistance ($r_{ds}$) of the MOS transistors, while in Fig. 4.2(a), $R_1$ (or $R_2$) comes in parallel to $r_{ds}$. Since, $R_1$ (or $R_2$) is smaller than $r_{ds}$, the LNA shown in Fig. 4.2(a) has lower load resistance than the one in Fig. 4.2(b). As a result, the LNA shown in Fig. 4.2(a) has higher bandwidth than the LNA in Fig. 4.2(b). Because of these reasons, the LNA topology, given in Fig. 4.2(a), is chosen for implementation in this work. Detailed analysis of the LNA shown in Fig. 4.2(a), is presented in the next section.

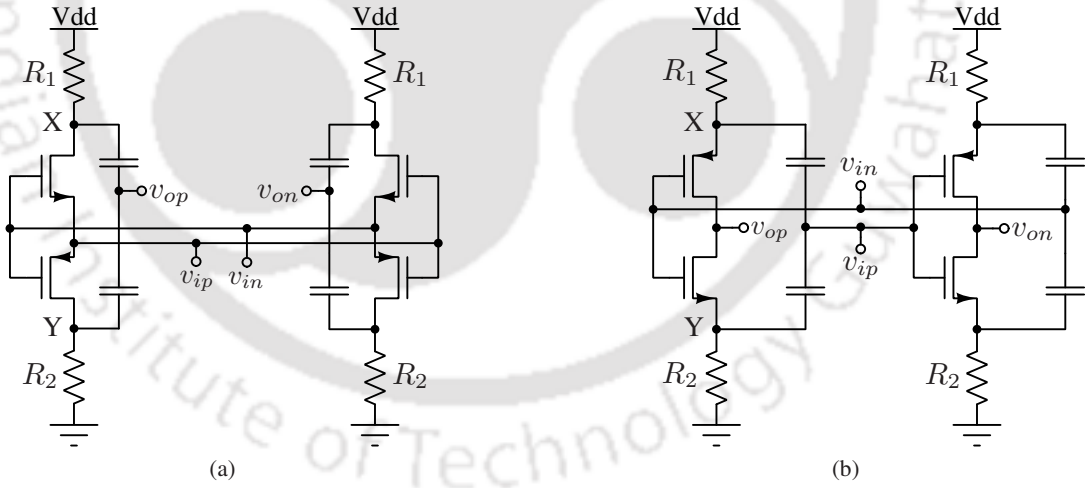
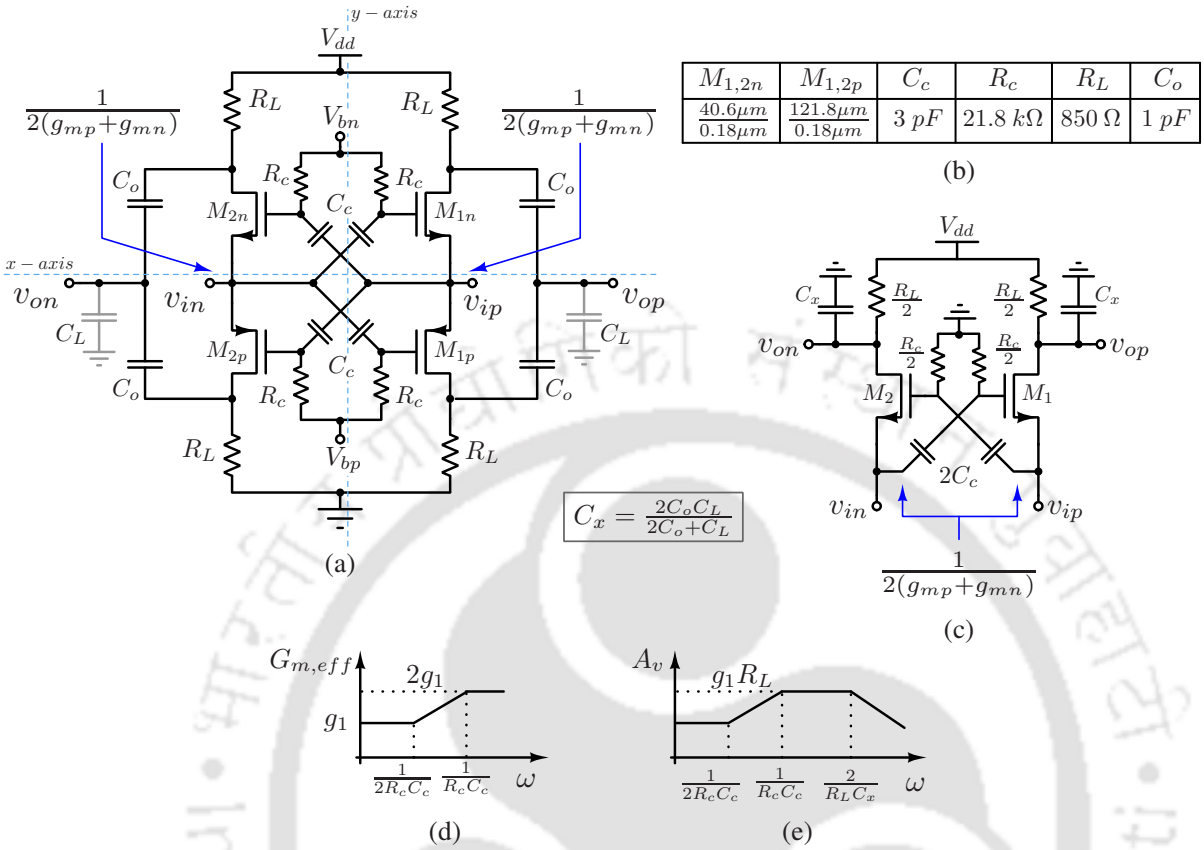



**Figure 4.2:** (a) A fully-differential partial noise-canceling LNA derived from Fig. 4.1(a). (b) A fully-differential partial noise-canceling LNA derived from Fig. 4.1(b).

## 4.2 Analysis and design of the proposed LNA

In this section, we present the analysis of the proposed LNA followed by the design methodology.




| $M_{1,2n}$ | $M_{1,2p}$ | $C_c$ | $R_c$ | $R_L$ | $C_o$ |
|---|---|---|---|---|---|
| $\frac{40.6\mu m}{0.18\mu m}$ | $\frac{121.8\mu m}{0.18\mu m}$ | 3 $pF$ | 21.8 $k\Omega$ | 850 $\Omega$ | 1 $pF$ |

(b)

**Figure 4.3:** (a) Proposed low-power partial noise-canceling common-gate LNA, (b) component values used in the implementation of the LNA, (c) simplified differential equivalent circuit of the proposed LNA, (d) variation of the effective transconductance of the LNA with frequency, and (e) typical magnitude plot of the LNA with frequency.

### 4.2.1 Input impedance and gain

The low-power fully-differential partial noise-canceling complementary common-gate (CCG) LNA used in this work, is shown in Fig. 4.3(a). The four transistors $M_{1p,n}$ and $M_{2p,n}$ act both as common-gate (CG) as well as common-source (CS) amplifiers. Differential input is simultaneously applied to the gate and the source terminals of the two nMOS transistors ($M_{1n}$, $M_{2n}$) in Fig. 4.3(a) to enhance the effective $g_m$ of each transistor by a factor of two [45–48]. Similar $g_m$-enhancement occurs for the two pMOS transistors ($M_{1p}$, $M_{2p}$) also. These two pMOS and nMOS CG pairs are vertically stacked so that the DC current is reused. The pMOS and nMOS drain voltages are combined using two output capacitors $C_o$. The output is taken differentially, as shown in Fig. 4.3(a). Fig. 4.3(b) shows the component values used in the implementation of the LNA. Let $g_{mp}$ and $g_{mn}$ represent the transconductances of pMOS and nMOS transistors, respectively. Similarly, $r_{op}$ and $r_{on}$ represent the drain-to-source resistances of pMOS and nMOS transistors, respectively. For a given differential input

$(v_{ip} - v_{in})$, the effective in-band transconductance of the circuit can be shown to be equal to $2(g_{mp} + g_{mn})$, which is approximately four times more than the transconductance of a single CG amplifier biased at the same current.

The proposed LNA has both the x-axis and y-axis symmetries and can be folded along either of the two axes for the purpose of analysis. Fig. 4.3(c) shows a reduced circuit obtained by folding the circuit along the x-axis. The transistors $M_{1n}$ and $M_{1p}$ from Fig. 4.3(a) are combined into a single transistor $M_1$ in Fig. 4.3(c), such that the transconductance of $M_1$ is $g_1 = (g_{mp} + g_{mn})$. Similarly, $M_{2n}$ and $M_{2p}$ are combined into a single transistor $M_2$. The effective load resistance at each output node of the equivalent circuit is $R_L/2$. $C_L$ denotes the load capacitance to the circuit, which in this case is the capacitance seen at the input of the output buffer stages. $C_x$ represents the effective capacitance present at the output node, where $C_x = (2C_oC_L)/(2C_o + C_L)$. The bias network, consisting of resistor $R_c$ and capacitor $C_c$, is also scaled, as shown in Fig. 4.3(c). Assuming that the load resistance $R_L$ is much smaller than the MOSFET output impedances, the effective transconductance of the circuit in Fig. 4.3(c) is

$$\begin{aligned} G_{m,eff} &\approx \frac{1 + s2R_cC_c}{1 + sR_cC_c} g_1 \\ &\approx \frac{1 + s2R_cC_c}{1 + sR_cC_c} (g_{mp} + g_{mn}). \end{aligned} \tag{4.1a}$$

Fig. 4.3(d) shows the typical variation of the effective transconductance with frequency. After the pole frequency $1/(R_cC_c)$, the effective transconductance is $\approx 2(g_{mp} + g_{mn}) = 2g_1$. Assuming $r_{op}, r_{on} \gg R_L$, the input impedance of the circuit in the passband can be shown to be as follows.

$$Z_{in} \approx \frac{1}{2(g_{mp} + g_{mn})} = \frac{1}{2g_1} \tag{4.2a}$$

From equation (4.2a), for a given input impedance, the proposed LNA requires approximately four-times smaller current compared to a single CG amplifier. This current is also much smaller than what is typically needed in a shunt-feedback LNA [29, 30]. If we bias the transistors such that $g_{mp} = g_{mn} = g_m$, then we need $g_m = 1/4R_s$ for input matching with a source resistance of $R_s$. Therefore, the $g_m$ requirement per transistor (and hence the bias current) in the proposed LNA is four-times smaller than that of a CG LNA.

The voltage gain of the circuit in Fig. 4.3(c) can be obtained as

$$\begin{aligned} A_v &\approx \frac{1 + s2R_cC_c}{1 + sR_cC_c} (g_{mp} + g_{mn}) \frac{R_L/2}{1 + s(R_LC_x/2)} \\ &= \frac{(1 + s2R_cC_c)(R_L/2)}{(1 + sR_cC_c)(1 + s(R_LC_x/2))} (g_{mp} + g_{mn}). \end{aligned} \tag{4.3a}$$

A magnitude Bode plot of the voltage gain is shown in Fig. 4.3(e). The mid-band voltage gain of the proposed LNA is $\approx 2(g_{mp}+g_{mn})(R_L/2) = g_1 R_L$.

### 4.2.2 Noise

Fig. 4.4 shows the different noise sources present in the LNA. In Fig. 4.4, $\overline{i_{n1}^2} = \overline{i_{n2}^2} = 4kT\gamma_m g_1$, $\overline{v_{n,R_L}^2} = 4kT(R_L/2)$, $\overline{v_{n,R_c}^2} = 4kT(R_c/2)$ and $\overline{v_{n,R_s}^2} = 4kTR_s$, where $\gamma_m$ is the thermal noise coefficient of a MOS transistor. The instantaneous noise due to the MOS transistors gets partially canceled at the output. Partial noise cancellation is also reported in references [48, 49] employing capacitor cross-coupling technique. However, compared to [48, 49], this work targets to design a low-power wideband LNA with an optimized noise and linearity performance to achieve an overall good figure-of-merit (FOM). For deriving the output noise voltage of the circuit, one needs to estimate the noise transfer function of $i_{n1}$ (or $i_{n2}$) first. Considering only the noise current $i_{n1}$ is present in the circuit, the instantaneous noise voltage generated at the output nodes $v_{op}$ and $v_{on}$ can be derived as

$$\overline{v_{n1,op}} = -\frac{R_L}{2}\left[\frac{g_1 R_s' + 1}{2g_1 R_s' + 1}\right]\overline{i_{n1}}, \tag{4.4a}$$

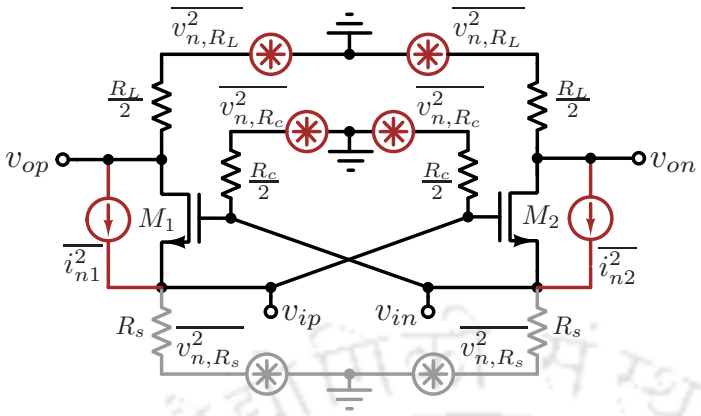
$$\overline{v_{n1,on}} = -\frac{R_L}{2}\left[\frac{g_1 R_s'}{2g_1 R_s' + 1}\right]\overline{i_{n1}}, \tag{4.4b}$$

where $R_s' = R_s||(R_c/2)$. Because of differential operation between $v_{op}$ and $v_{on}$, the instantaneous noise voltage at the output due to the noise current $i_{n1}$ is

$$\begin{aligned}\overline{v_{n1,out}} &= \overline{v_{n1,op}} - \overline{v_{n1,on}} \\ &= -\frac{R_L}{2}\left[\frac{1}{2g_1 R_s' + 1}\right]\overline{i_{n1}}\end{aligned} \tag{4.5a}$$

Noise current $i_{n2}$ has an identical transfer function as $i_{n1}$. Finally, the total output noise voltage at the differential output can be derived as

$$\begin{aligned}\overline{v_{n,out}^2} = 2{A_v}^2\left[\frac{R_s'/R_s}{1+2g_1R_s'}\right]^2\overline{v_{n,R_s}^2} + \left[\frac{R_L}{2}\right]^2\left[\frac{1}{2g_1R_s'+1}\right]^2\overline{i_{n1}^2} + \left[\frac{R_L}{2}\right]^2\left[\frac{1}{2g_1R_s'+1}\right]^2\overline{i_{n2}^2} \\ + 2\frac{{A_v}^2}{(1+2g_1R_s')^2}\left[\frac{2R_s'}{R_c}\right]^2\overline{v_{n,R_c}^2} + 2\overline{v_{n,R_L}^2}\end{aligned} \tag{4.6a}$$




$$\overline{i^2_{n1,n2}} = 4kT\gamma_m g_1$$
$$\overline{v^2_{n,R_L}} = 4kT(R_L/2)$$
$$\overline{v^2_{n,R_c}} = 4kT(R_c/2)$$
$$\overline{v^2_{n,R_s}} = 4kTR_s$$
$$g_1 = (g_{mp} + g_{mn})$$

**Figure 4.4:** Simplified version of the LNA showing different noise sources.

The noise factor of the proposed LNA can be derived as

$$\begin{aligned} F &= 1 + \frac{\frac{1}{(1+2g_1R'_s)^2}\left\{\left[\frac{R_L}{2}\right]^2\overline{i^2_{n1}} + \left[\frac{R_L}{2}\right]^2\overline{i^2_{n2}} + 2A_v^2\left[\frac{2R'_s}{R_c}\right]^2\overline{v^2_{n,R_c}}\right\} + 2\overline{v^2_{n,R_L}}}{2A_v^2\left[\frac{R'_s/R_s}{1+2g_1R'_s}\right]^2\overline{v^2_{n,R_s}}} \\ &= 1 + \frac{\gamma_m}{4g_1R_s}\left[\frac{R_s}{R'_s}\right]^2 + \frac{[1+2g_1R'_s]^2}{2g_1^2R_sR_L}\left[\frac{R_s}{R'_s}\right]^2 + \frac{R_s}{R_c/2}. \end{aligned} \tag{4.7a}$$

In the noise factor expression given in (4.7a), the second term is due to the noise contribution of the MOS transistors, and the third term is because of the load resistors. The second term can be reduced by selecting higher values of $g_1$, keeping the input impedance matching intact. A high value of $R_L$ can reduce the noise contribution from the third term. The fourth term represents the noise contribution of the biasing resistor ($R_c$). The noise contribution of $R_c$ can be reduced by choosing $R_c \gg R_s$ ($R_c = 21.8$ k$\Omega$ in the current implementation). For $R_c \gg R_s$, (4.7a) can be simplified to

$$F \approx 1 + \frac{\gamma_m}{4g_1R_s} + \frac{[1+2g_1R_s]^2}{2g_1^2R_sR_L}. \tag{4.8a}$$

In the current implementation, $R_L = 850\ \Omega$. The value of $g_1$ can be modified by varying the bias voltages of the nMOS and pMOS transistors, once their dimensions are fixed. In this work, we analyzed and measured the performance of the proposed LNA at two different biasing conditions, which correspond to two different $g_1$ values ($11.34\ m\mho$ and $8.6\ m\mho$). The two mentioned biasing conditions are associated with two modes of operation of the LNA. Details of the two operating modes of the LNA are discussed later in this chapter.

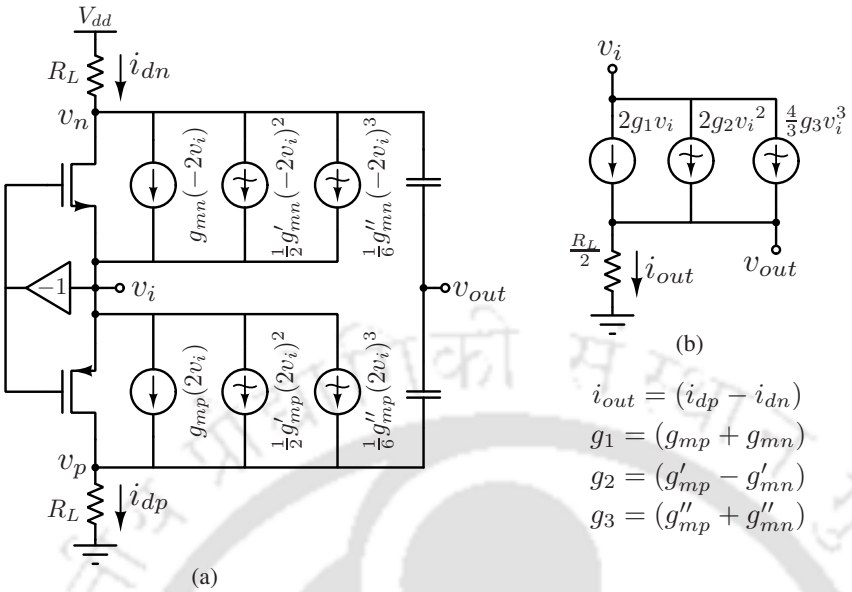



**Figure 4.5:** (a) Single-ended version of the LNA showing pMOS and nMOS distortion currents, (b) simplified single-ended model of the proposed LNA for nonlinearity analysis.

### 4.2.3 Linearity

One key advantage of the proposed LNA is the possibility of inherent linearization within the circuit [15, 141]. In the proposed LNA, the distortion is mainly caused by the nonlinear transconductance of the MOS transistors. Considering up to a third-order nonlinearity, the small-signal drain current of a MOS transistor is [142], [143]:

$$i_{ds} = g_m v_{gs} + \frac{g'_m}{2!} v_{gs}^2 + \frac{g''_m}{3!} v_{gs}^3,$$

where $g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$, $g'_m = \frac{\partial^2 I_{DS}}{\partial V_{GS}^2}$ and $g''_m = \frac{\partial^3 I_{DS}}{\partial V_{GS}^3}$. Fig. 4.5(a) shows a single-ended version of the proposed LNA with all the distortion currents due to pMOS and nMOS transistors. In Fig. 4.5(a), the drain currents of the pMOS and nMOS transistors are

$$i_{dp} = g_{mp}(2v_i) + \frac{1}{2}g'_{mp}(2v_i)^2 + \frac{1}{6}g''_{mp}(2v_i)^3,$$
$$i_{dn} = g_{mn}(-2v_i) + \frac{1}{2}g'_{mn}(-2v_i)^2 + \frac{1}{6}g''_{mn}(-2v_i)^3.$$

The pMOS and nMOS currents are combined at the output using two capacitors $C_o$ [141]. The combined output current, as shown in Fig. 4.5(b), is [15]

$$\begin{aligned} i_{out} &= (i_{dp} - i_{dn}) \\ &= 2(g_{mp} + g_{mn})v_i + 2(g'_{mp} - g'_{mn})v_i^2 + \frac{4}{3}(g''_{mp} + g''_{mn})v_i^3 \\ &= \left[2g_1 v_i + 2g_2 v_i^2 + \frac{4}{3}g_3 v_i^3\right], \end{aligned} \tag{4.11a}$$

where

$$\begin{aligned} g_2 &= (g'_{mp} - g'_{mn}) \\ g_3 &= (g''_{mp} + g''_{mn}). \end{aligned}$$

From the output-current expression in (4.11a), the second-order nonlinear terms can be canceled if $g'_{mp}$ and $g'_{mn}$ are properly matched. Moreover, the intrinsic third-order nonlinearity of the LNA can be reduced by biasing the pMOS and nMOS transistors near the zero-crossings of $g''_{mp}$ and $g''_{mn}$, respectively.

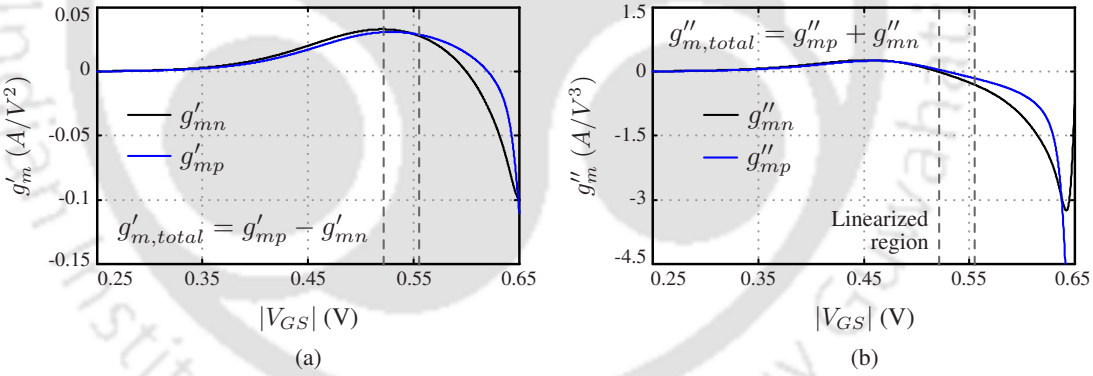



**Figure 4.6:** Simulated (a) $g'_{mp}$ and $g'_{mn}$, and (b) $g''_{mp}$ and $g''_{mn}$ for the pMOS and nMOS transistors used in this work.

Typical variations of $g'_{mn}$, $g'_{mp}$, $g''_{mn}$, and $g''_{mp}$ with the gate-to-source bias voltage $V_{GS}$ are shown in Fig. 4.6. From Fig. 4.6, within the optimum $V_{GS}$-range $V_{GS,opt} \approx (540 \pm 10)$ mV, the magnitudes of $g'_{mp}$ and $g'_{mn}$ are almost equal and the third-order distortion coefficients $g''_{mp}$ and $g''_{mn}$ have near-zero values.

### 4.2.4 Design methodology

The biasing of the proposed LNA is set using two external voltages, $V_{bp}$ and $V_{bn}$. Fig. 4.7(a) and 4.7(b) show the noise figure and IIP3 of the designed LNA with varying $V_{bp}$ and $V_{bn}$. From Fig. 4.7, it is observed that the bias settings for high linearity and low NF are different. Hence, simultaneous low-noise and high-linearity

operations are not feasible. However, one can select the proposed LNA's operating point based on the target specification in terms of NF and IIP3. In this work, we have analyzed and measured the LNA performance for the following two operating points, as marked in Fig. 4.7: a high-linearity mode and a low-noise mode.

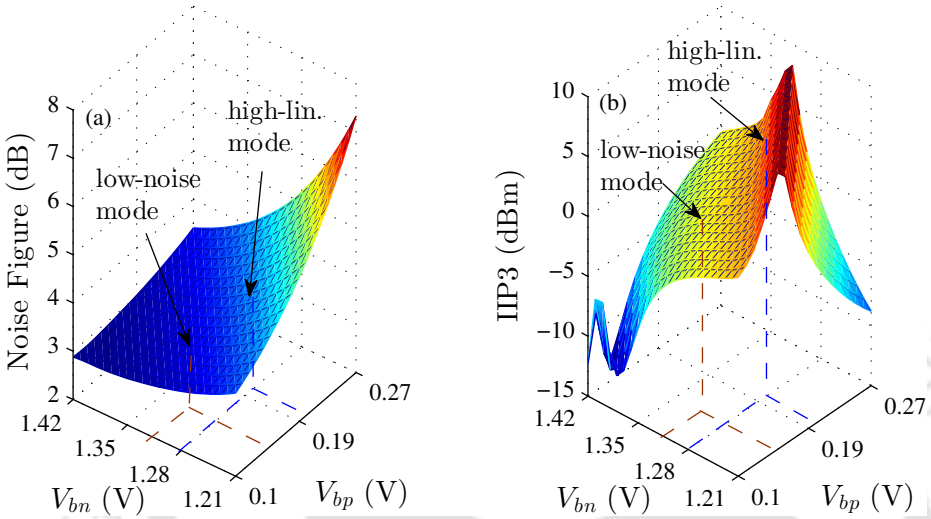



**Figure 4.7:** Simulated (a) NF, (b) IIP3 of the implemented LNA with varying bias voltages $V_{bp}$ and $V_{bn}$.

The design methodology of the proposed LNA is summarized in the following points.

(i) For input-match, one needs $g_{mp} = g_{mn} \approx 1/4R_s$. If one wants to operate the transistors at a $g_m/I_D$ of $x$, the current requirement of the LNA is $\approx\ 1/(2R_s x)$.

(ii) Once a value of $x$ is chosen, appropriate transistor widths can be chosen based on the $I_D/W$ plots [68].

(iii) For low NF, one needs $R_L \gg 8R_s$. However, the value of $R_L$ is limited by the maximum allowed voltage drop across it. Assuming a maximum voltage drop of $V_{dd}/4$ across each resistor, $R_L$ should be less than $V_{dd}R_s x$.

(iv) One has to choose $R_c \gg R_s$ for better NF. $C_c$ value can be chosen based on the lower 3-dB frequency requirement of the LNA.

(v) One can generate the $g'_m$ and $g''_m$ plots as in Fig. 4.6 to find out the $V_{GS,opt}$ range. Once $V_{GS,opt}$ is known, one can choose $V_{bn} = (V_{dd}/2 + V_{GS,opt})$ and $V_{bp} = (V_{dd}/2 - V_{GS,opt})$ as the initial bias voltages to achieve high IIP3.

(vi) Using Fig. 4.7, one can set the operating point of the LNA depending on the target performance specification.

## 4.3 Implementation details and measurement results

A prototype LNA is implemented in TSMC 180 nm 1P6M CMOS technology, where it occupies an active area of 0.08 mm$^2$. The photographs of the PCB and the die are shown in Fig. 4.8(a) and 4.8(b), respectively. The LNA consumes 490 $\mu$A and 800 $\mu$A of current from a 1.5 V supply voltage in the high-linearity mode and the low-noise mode, respectively. Two common-drain buffers are used at the output of the LNA for testing purposes. The chip also consists of standalone buffers to facilitate the de-embedding of the buffer performance. The die is enclosed in a 56-pin quad-flat no-leads (QFN) package and mounted on an FR-4 printed circuit board (PCB) for testing. Off-chip baluns from minicircuits (TCM2-33X+) are used for single-ended to differential and differential to single-ended conversions.

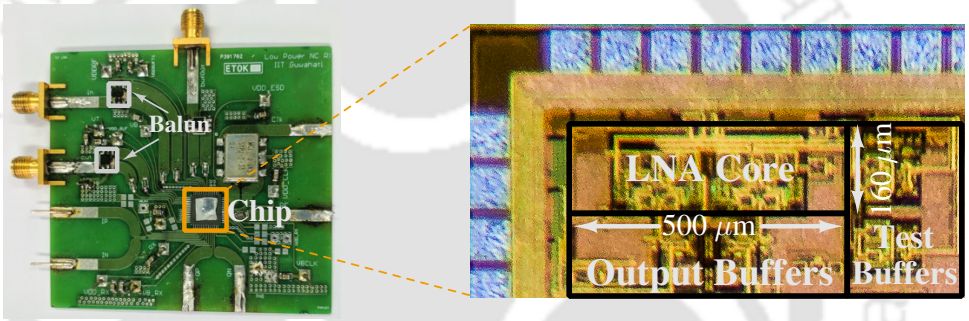



**Figure 4.8:** Photographs of the (a) testing board and (b) the die.

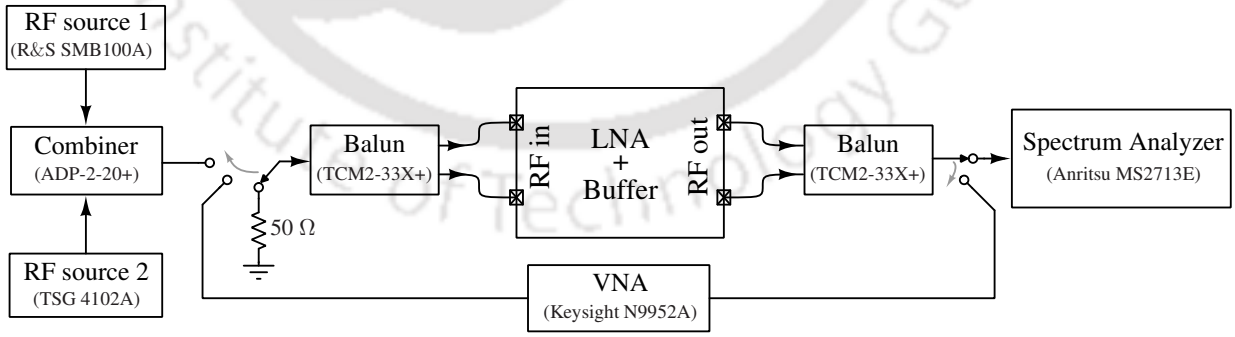



**Figure 4.9:** LNA test-setup with various measuring instruments.

The S-parameters of the LNA is measured using the Keysight N9952A vector network analyzer (VNA). Fig. 4.10(a) shows the measured $|S_{11}|$ and $|S_{22}|$ of the implemented LNA for the two modes of operation. Both $|S_{11}|$ and $|S_{22}|$ are $<-10$ dB over the frequency range of interest. The LNA is stable at all frequencies. Fig. 4.10(b) shows the measured stability factor ($K$) [138]. Anritsu MS2713E spectrum analyzer is used in

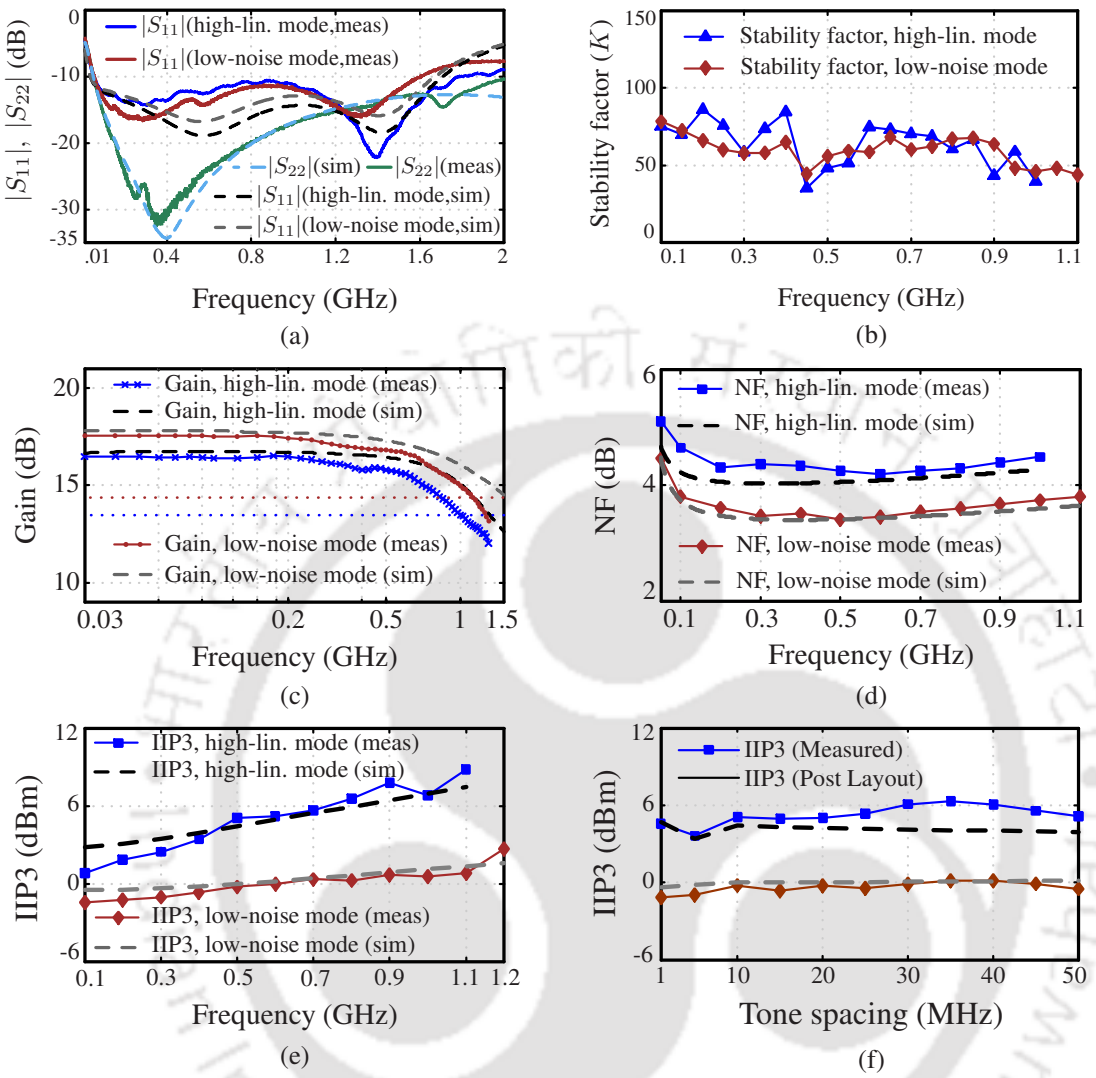



**Figure 4.10:** Measured (a) $|S_{11}|$ and $|S_{22}|$, (b) stability factor (including output buffers), (c) voltage gain and (d) NF of the LNA. Measured IIP3 of the LNA (e) with input frequency (for 10 MHz tone spacing), and (f) with tone spacing at 500 MHz.

gain, NF, and IIP3 measurements. The two-tone signal for IIP3 measurement is generated using two signal sources, TSG 4102A and R&S SMB100A, and an off-chip combiner. The test-setup with various measuring instruments is shown in Fig. 4.9. Fig. 4.10(c) shows the measured voltage gain of the LNA. In high-linearity and low-noise modes, the LNA has a peak voltage gain of 16.5 dB and 17.5 dB, respectively. Fig. 4.10(d) shows the NF of the LNA. In high-linearity mode, the LNA has a measured NF of $4.19 - 4.65$ dB over the frequency range of $0.1 - 1$ GHz. In low-noise mode, the LNA has a lower NF of $3.41 - 3.81$ dB over the frequency range of $0.1 - 1.1$ GHz. Fig. 4.10(e) shows the measured IIP3 of the LNA at different frequencies. The separation between the two tones for this measurement is 10 MHz. At 500 MHz, the LNA has a measured

IIP3 of $\approx +5.1$ dBm and $\approx -0.2$ dBm in high-linearity mode and low-noise mode, respectively. The IIP3 is also measured with varying tone spacing around 500 MHz. Fig. 4.10(f) shows the measured IIP3 with varying tone spacing. The LNA has a measured input-referred 1-dB compression point (P1dB) of $\approx -14.8$ dBm at 500 MHz for the high-linearity mode of operation.

Tab. 4.1 shows a summary of the LNA performance and provides a comparison with other relevant LNAs. From Tab. 4.1, the proposed LNA has the highest IIP3 among the sub-mW LNAs [38–40, 52, 62, 68]. The following FOM [62] is often used to compare wideband LNAs.

$$FOM = 20\log_{10}\left[\frac{BW[GHz]G_{av}[lin.]IIP3[mW]}{P_{dc}[mW](NF_{av}[lin.]-1)}\right],$$

where $G_{av}$ represents average voltage gain, $NF_{av}$ represents the average NF, BW represents the bandwidth in GHz, and $P_{dc}$ is the DC power consumption in mW. The proposed LNA has achieved the second highest $FOM$ among the sub-mW LNAs shown in Tab. 4.1.

**Table 4.1:** Performance summary of the proposed LNA and a comparison with other sub-mW LNAs

| | Inductor present? | Tech. (nm) | Freq. (GHz) | Gain (dB) | NF (dB) | IIP3 (dBm) | Power (mW) | Area ($mm^2$) | $FOM$ |
|---|---|---|---|---|---|---|---|---|---|
| **T.W. (high-lin. mode)** | No | 180 | $0.1-1$ | 16.5 | $4.19-4.65$ | $+5.1^{\star}$ | 0.735 | 0.08 | 22 |
| **T.W. (low-noise mode)** | No | 180 | $0.1-1.1$ | 17.5 | $3.41-3.81$ | $-0.2^{\star}$ | 1.2 | 0.08 | 11.76 |
| TCAS-I 2019 [68] | No | 28 | $0.2-2.4$ | 15 | 4.5 | $-6.5$ | 0.5 | 0.005 | 8.17 |
| | No | 65 | $0.2-2.7$ | 14.5 | 4.6 | $-1$ | 1.2 | 0.005 | 11.87 |
| TCAS-I 2018 [62] | No | 65 | $0.2-2.7$ | 21.2 | $3-3.5$ | $-2$ | 0.96 | 0.05 | 23.08 |
| | No | 65 | $0.1-4.3$ | 21.2 | $2.8-4$ | $-7.7$ | 2 | 0.05 | 9.25 |
| ISCAS 2018 [42] | No | 90 | $0.04-0.8$ | 14.27 | 6.5 | $-5.74$ | 0.49 | $0.365^{\nabla}$ | $-5.7$ |
| MWCL 2017 [52] | No | 180 | $0.4-1$ | $15.5-18$ | 4.2 | $-14$ to $-21$ | 0.2 | 0.27 | $-5.95$ |
| TCAS-I 2017 [41] | No | 130 | $0.1-1.2$ | 21.2 | 2.6 | $+6$ | 1.52 | 0.007 | 30.6 |
| ISLPED 2017 [51] | No | 28 | $0.45-6$ | 16.8 | 7.3 | $-16$ | 0.3 | 0.0015 | $-4.16$ |
| TMTT 2016 [40] | No | 130 | $0.1-2.2$ | 12.3 | $4.9-6$ | $-9.5$ | 0.4 | 0.005 | $-1.78$ |
| AICSP 2014 [36] | No | 65 | $0.5-2.5$ | 15 | $3.9-5$ | $+3.1$ | 0.91 | 0.385 | 21.5 |
| E. Lett. 2014 [63] | No | 130 | $0.35-0.95$ | 14 | $3.7-4.6$ | – | 0.4 | 0.06 | – |
| JSSC 2012 [70] | No | 130 | $0.1-2.7$ | 20 | 4 | $-12$ | 1.32 | 0.007 | $-3.2$ |
| TCAS-II 2018 [64] | Yes | 180 | $2-5$ | 13 | $6-8$ | $-9.5^{\dagger}$ | 1.8 | 0.72 | $-13.6$ |
| JSSC 2016 [39] | Yes | 130 | $0.6-4.2$ | 14 | 4 | $-11.5$ to $-9.5$ | 0.25 | 0.396 | 13.07 |
| TVLSI 2015 [38] | Yes | 90 | $0.1-7$ | 12.6 | $5.5-6.5$ | $-6$ to $-9$ | 0.75 | 0.23 | 8.89 |
| MWCL 2014 [37] | Yes | 180 | $2.3-2.6$ | 14.7 | 4.8 | $+2$ | 0.58 | $0.39^{\nabla}$ | 5.36 |
| RFIC 2011 [43] | Yes | 180 | $2-2.3$ | 13.9 | 5.14 | $-9.3$ | 0.21 | 1.5 | $-10.2$ |

$\star$ At 500 MHz center frequency; $\nabla$ Including pads; † Simulated IIP3

## 4.4 Summary

This chapter presented a sub-mW inductorless wideband LNA with partial noise cancellation and high linearity. In the proposed LNA topology, $g_m$-linearization is achieved without any power overhead. The designed LNA has an IIP3 $>$ 0 dBm from 0.1-to-1 GHz while consuming only 0.735 mW of DC power in the high-linearity mode of operation. In the low-noise mode of operation, the LNA has a minimum NF of 3.41 dB while consuming 1.2 mW of DC power.

# 5

# A Mixer-First Receiver With a Low-Power Complementary Common-Gate TIA



**Contents**

## 5.1 Introduction to mixer-first receivers

Over the last decade, N-path passive mixer-first receivers [29–31, 95, 98–120] have become a popular choice for surface acoustic wave (SAW)-less fully integrated radio receivers. The key features of an N-path passive mixer-first receiver are its frequency translational property and high linearity. In this chapter, we first provide an overview of N-path mixer-first receivers followed by the implementation of a mixer-first receiver with the proposed complementary common-gate (CCG) TIA.

### 5.1.1 Overview of N-path passive mixer-first receivers

An N-path passive mixer-first receiver contains N identical parallel paths, which are driven by N non-overlapping clock pulses. The first block in each path is a passive mixer that receives and down-converts the incoming RF signal. The absence of RF gain degrades the NF of a passive mixer-first receiver slightly. However, the achieved linearity of N-path passive mixer-first receivers is superior to the traditional LNA-first receivers [26, 28, 32, 144, 145]. As a result, mixer-first receivers in the literature [29, 30, 99–101, 105–109] have achieved an improved spurious-free dynamic range (SFDR) compared to their LNA-first counter-parts [26, 28, 32, 144, 145].

Fig. 5.1(a) shows the architecture of a four-path passive mixer-first receiver [98]. In Fig. 5.1(a), $R_s$ is the source resistance. The four paths get successively turned on by the four non-overlapping 25% duty cycle clock pulses. The four non-overlapping clock pulses ($p_1$, $p_2$, $p_3$, and $p_4$) of period $T_{LO}$ are shown in Fig. 5.1(b). The mixer outputs are filtered using the shunt capacitors ($C_{sh}$). The intermediate frequency (IF) components of the mixer output are further processed using the baseband amplifiers. Amplifiers in a shunt-feedback configuration are generally used in the baseband stage of a passive mixer-first receiver [98]. Each passive mixer can be treated as a switch having a series resistance $R_{sw}$. Since the clock pulses are completely non-overlapping, only one $R_{sw}$ is active at a time. Hence, the series resistance of all the switches can be lumped together and treated as a single resistor of the same value, as shown in Fig. 5.1(c). The input impedance of the baseband amplifier is represented by $Z_B$. [98] further simplified the analysis of a passive mixer-first receiver and presented a linear time-invariant (LTI) model as shown in Fig. 5.1(d). In the mixer-first receiver LTI model, $R_{sh}$ accounts for the power loss due to the up-conversion by harmonics of the local oscillator (LO), and $\gamma$ is a topology-dependent constant. For an N-path passive mixer-first receiver, the parameters $\gamma$ and $R_{sh}$ can be represented as [98]

$$\gamma = \frac{\text{sinc}(\frac{\pi}{N})^2}{N} \tag{5.1a}$$

$$R_{sh} = (R_s + R_{sw})\frac{N\gamma}{1 - N\gamma} \tag{5.1b}$$

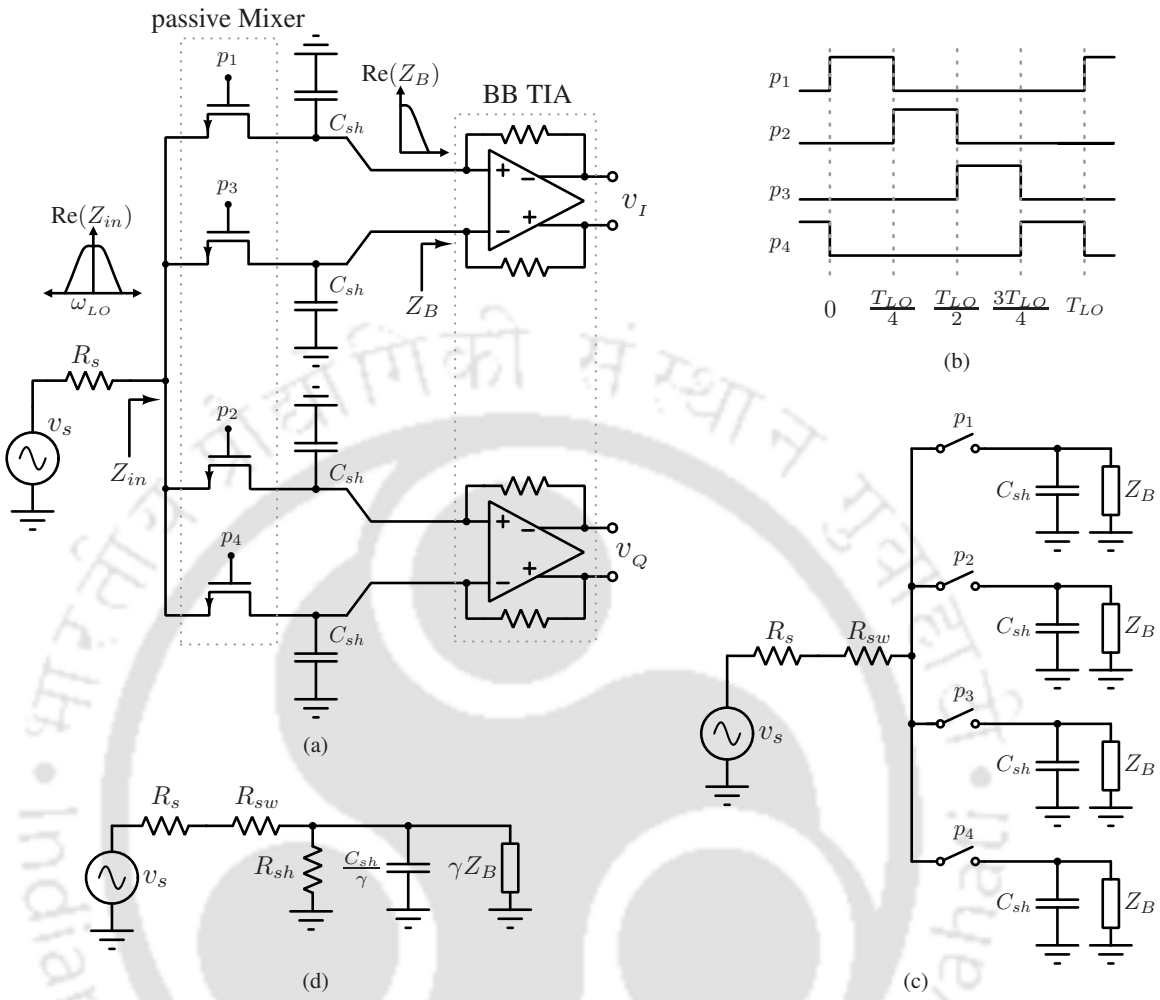



**Figure 5.1:** (a) A four-path passive mixer-first receiver [98]. (b) The four non-overlapping clock pulses of period $T_{LO}$. (c) A simplified model of a four-path passive mixer-first receiver [98]. (d) The LTI model of a passive mixer-first receiver [98].

From Fig. 5.1(d), the input impedance ($Z_{in}$) of the mixer-first receiver can be represented as [98]

$$Z_{in} = R_{sw} + \left(R_{sh} || \frac{\gamma}{j\omega_{IF} C_{sh}} || \gamma Z_B\right), \tag{5.2a}$$

where $\omega_{IF} = (\omega_{RF} - \omega_{LO})$ is the frequency of the down-converted signal. From (5.2a), one needs to design $R_{sw}$ and $Z_B$ properly to achieve the 50 Ω impedance required at the RF input. Because of the frequency translational property of N-path mixers, the baseband impedance seen at the output of the mixer is translated to the RF port. As a result, one may tune the N-path passive mixer-first receiver to a desired frequency band just by changing the clock frequency.

In an N-path passive mixer-first receiver, the baseband stage is the only static power-consuming block since the RF LNA is removed. In high-linearity mixer-first receivers presented in [29–31], the static power constitutes

a considerable percentage of the total power budget. Various techniques are proposed in [102, 114–117, 121] to reduce the power consumption of passive mixer-first receivers. The mixer-first receiver in [114] uses a noise-power optimized multi-path current-reused baseband amplifier. An RF-to-BB current-reuse technique is proposed in [115] to reduce the power consumption in N-phase mixer-first receivers. [121] proposed a low-power blocker-tolerant receiver with a gain-boosted mixer-first topology. Features like indirect BB amplification and double-RF N-path filtering were explored in [121]. An optimized supply voltage is used to reduce the power consumption in the mixer-first receiver that is demonstrated in [116]. [102] proposed a low-power gain-boosted N-path mixer-first receiver with switched BB extraction. [117] proposed a passive mixer-first low-power wake-up-receiver using a ring-based local oscillator (LO). [122] demonstrated an ultra-low-power passive-mixer-based receiver using a passive LNA before the mixer stage. However, it [122] requires a large off-chip inductor, and frequency tunability is compromised. [123] proposed a technique to harvest energy from the out-of-band RF blockers to extend the battery life of a receiver. However, the technique in [123] requires extra inductors, and the receiver is not frequency tunable. [124] achieves low-power operation by removing the requirement of multiphase clock generation circuitry. However, an extra RF phase shift network is needed before the mixers for the receiver's quadrature operation.

In a mixer-first receiver, the TIA provides the input-match and has a major effect on the overall noise and linearity performance of the receiver. The shunt-feedback topology is the most commonly used TIA in mixer-first receivers. The linearity, noise performance, and power consumption are tightly coupled with each other in a mixer-first receiver with a shunt-feedback TIA [146]. Typical trade-offs involved in the design of the TIA for a mixer-first receiver are shown in Fig. 5.2 [147]. Opamp (or OTA) based shunt-feedback TIAs usually exhibit poor linearity and require an additional linearization technique, such as noise-and-distortion cancellation [147], to improve the in-band linearity. The noise-and-distortion canceling technique, which is frequently used in the design of RF LNAs [20, 75], requires significantly high power to be dissipated in the auxiliary stage.

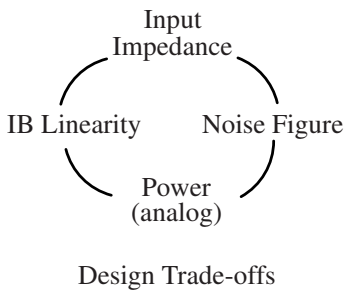



**Figure 5.2:** Typical trade-offs in the design of the TIA for a mixer-first receiver [147].

The complementary common-gate (CCG) LNA developed in the previous work has many useful features. The proposed four-transistor-LNA has a high transconductance efficiency. It achieves good noise-and-linearity performance at low power levels because of partial noise cancellation and an inherent linearization technique. In this work, the same LNA is redesigned to be used as the baseband TIA. The designed TIA is used to develop a frequency-agile receiver front-end working in the frequency range $0.3 - 1.3$ GHz.

## 5.2 Mixer-first receiver with a complementary common-gate TIA

Fig. 5.3 shows the block diagram of the implemented four-phase mixer-first receiver using the CCG TIA in the baseband. In Fig. 5.3, $R_s$ denotes the source resistance, $C_{sh}$ is the shunt capacitance at the input of the TIA, and $C_b$ is an off-chip DC blocking capacitor at the RF input. The mixer switches are implemented using nMOS transistors. The mixer is DC-coupled to the TIA. The gates of the mixer transistors are biased to resolve the DC-offset problem caused by the DC-coupling. An on-chip frequency divider (/2) and a set of combinational logic circuits are used to generate the four non-overlapping LO signals ($p_1 - p_4$) required for the mixer. The design details of each of these blocks are discussed in section 5.4.

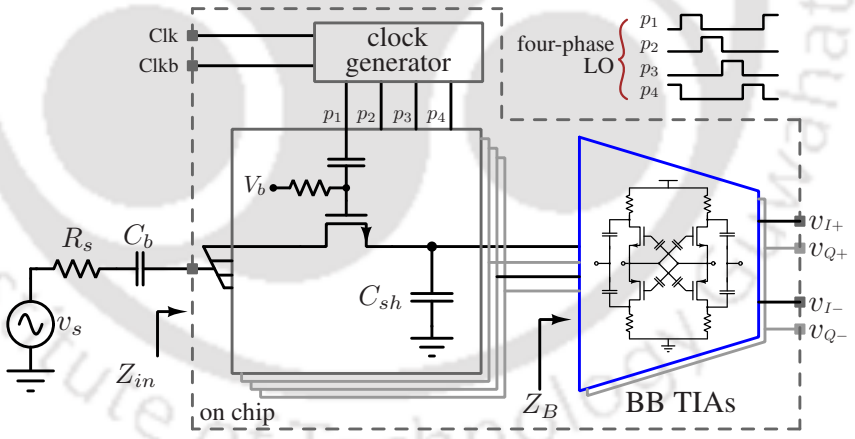



**Figure 5.3:** Block diagram of the implemented four-phase mixer-first receiver.

The same analysis that was presented in chapter 4.4 for the LNA is equally valid for the baseband TIA. From the analysis given in section 4.2, the mid-band voltage gain of the baseband TIA is

$$A_v \approx 2(g_{mp} + g_{mn})\frac{R_L}{2} = g_1 R_L, \tag{5.3a}$$

where $g_{mp}$ and $g_{mn}$ represent the transconductances of the pMOS and nMOS transistors, respectively. $R_L$ denotes the load resistance and $g_1 = (g_{mp} + g_{mn})$. Similarly, the input impedance of the baseband TIA in the

passband can be represented as

$$Z_B \approx \frac{1}{2(g_{mp}+g_{mn})} = \frac{1}{2g_1} \tag{5.4a}$$

## 5.3 Receiver analysis

In this section, we present the theoretical analysis of the mixer-first receiver based on the LTI model presented in Fig. 5.1(d) [98]. Fig. 5.4 shows the LTI model of the proposed mixer-first receiver [98]. As per the LTI model [98], the shunt capacitance ($C_{sh}$) and the baseband input-impedance ($Z_B$) are scaled by the factor $\gamma$. For a four-path mixer-first receiver, $\gamma \approx 0.203$ and $R_{sh} \approx 4.3(R_s + R_{sw})$ [98]. The LTI model shown in Fig. 5.4 is used in the following subsections to derive different performance parameters of the proposed mixer-first receiver.

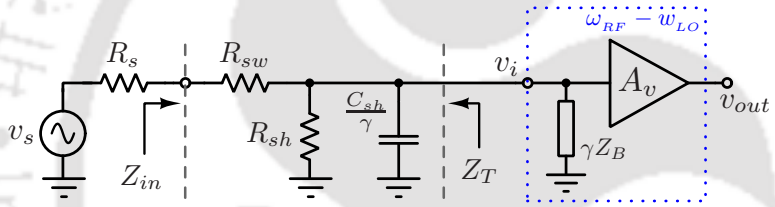



**Figure 5.4:** An LTI model of the receiver [98].

### 5.3.1 Input impedance

The input impedance of the TIA is $\gamma Z_B$, where $Z_B = 1/(2g_1)$ (from equation (5.4a)). From equation (5.2a), the input impedance of the receiver is

$$\begin{aligned} Z_{in} &= R_{sw} + \left(R_{sh} \,||\, \frac{\gamma}{j\omega_{IF} C_{sh}} \,||\, \frac{\gamma}{2g_1}\right) \\ &= R_{sw} + \left(\frac{1}{\frac{1}{R_{sh}} + j\omega_{IF}\frac{C_{sh}}{\gamma} + \frac{2g_1}{\gamma}}\right). \end{aligned} \tag{5.5a}$$

Typically a low resistance is chosen for the mixer switches to minimize their noise contribution. Leaving $R_{sw}$ aside, the designers can vary the transconductance $g_1$ to achieve impedance matching at the RF input. Fig. 5.5(a) shows a comparison of analytical (Eq. (5.5a)) and simulated real part of $Z_{in}$ with varying $g_1$. In this simulation, all ideal components are used, with their values being those corresponding to the actual implementation. From Fig. 5.5(a), we need a transconductance of around 2 m℧ for a $\approx 50\ \Omega$ input impedance. Fig. 5.5(b) and 5.5(c) shows a comparison of analytical (Eq. (5.5a)) and simulated real and imaginary parts of the input impedance at

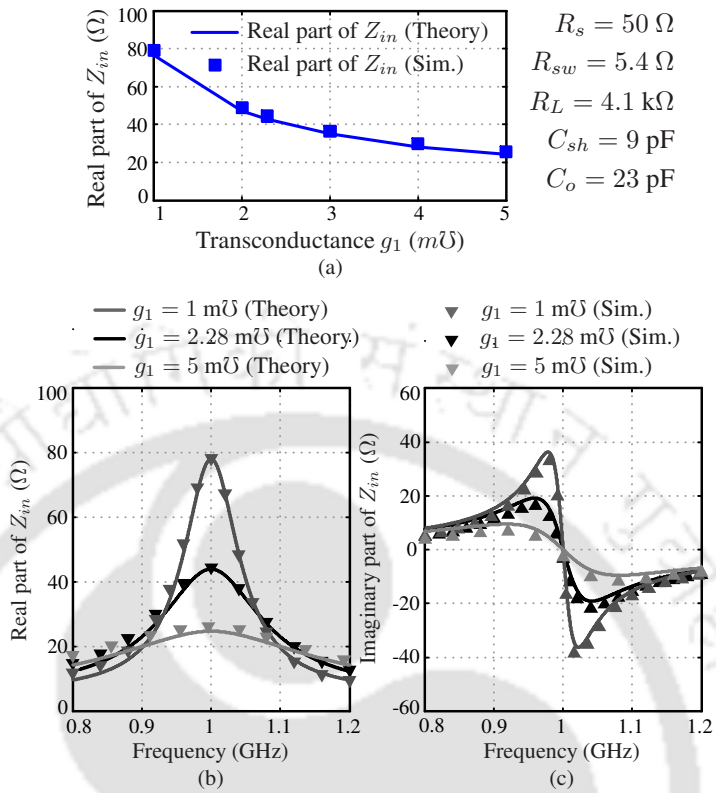



**Figure 5.5:** (a) Real part of $Z_{in}$ of the receiver with varying baseband transconductance ($g_1$) for $f_{LO} = 1$ GHz. Comparison of analytical (Eq. (5.5a)) and simulated values of (b) real and (c) imaginary parts of $Z_{in}$ for $f_{LO} = 1$ GHz. Ideal transconductors are used to realize the baseband stage in these simulations.

1 GHz LO frequency for three different $g_1$ values.

### 5.3.2 Conversion gain

Let $R_a = (R_s + R_{sw})$. The impedance seen from the baseband input node towards the mixer is

$$Z_T = R_a \,||\, R_{sh} \,||\, \frac{\gamma}{j\omega C_{sh}}.$$

From Fig. 5.4, the voltage at the input of the baseband TIA ($v_i$) can be represented as

$$\begin{aligned} v_i &= \frac{\left(R_{sh} \,||\, \frac{\gamma}{2g_1} \,||\, \frac{\gamma}{j\omega C_{sh}}\right)}{\left[R_a + \left(R_{sh} \,||\, \frac{\gamma}{2g_1} \,||\, \frac{\gamma}{j\omega C_{sh}}\right)\right]} v_s \\ &= \frac{Z_T \,||\, \frac{\gamma}{2g_1}}{R_a} v_s \\ &= \frac{1}{1+T_o}\left[\frac{Z_T}{R_a}\right] v_s, \end{aligned}$$

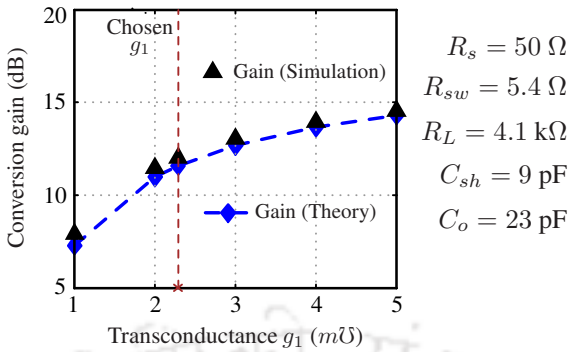



**Figure 5.6:** Comparison of analytical and simulated conversion gain of a single-path of the receiver (including the source resistance) with varying baseband transconductance ($g_1$) for $f_{LO} = 1$ GHz.

where $T_o = 2(g_1/\gamma)Z_T$. The conversion gain of a single-path of the receiver (including the source resistance) is

$$\begin{aligned} G = \frac{v_{out}}{v_s} &= \left(\frac{v_i}{v_s}\right).\left(\frac{v_{out}}{v_i}\right) \\ &= \frac{1}{1+T_o}\left[\frac{Z_T}{R_a}\right]A_v, \end{aligned} \tag{5.8a}$$

where $A_v$ is the gain of the baseband TIA and is given by (5.3a). Fig. 5.6 shows a comparison of the analytical (Eq. (5.8a)) and simulated conversion gain of the receiver with varying $g_1$.

### 5.3.3 Noise

Fig. 5.7 shows all the noise sources present in the proposed mixer-first receiver. As per the receiver LTI model [98], we need to scale all the baseband components, including $g_1$, by the factor $\gamma$. In Fig. 5.7, $\overline{i_{n1}}$ and $\overline{i_{n2}}$ represent the instantaneous noise current of the baseband transconductor. $\overline{i_{n1}^2} = \overline{i_{n2}^2} = 4kT\gamma_m(g_1/\gamma)$, where $\gamma_m$ is the thermal noise coefficient of a MOS transistor. Let us assume that the biasing resistor $R_c \gg Re(Z_T)$, such that its noise contribution can be ignored. By employing analysis similar to section 4.2.2 (LNA noise analysis), the output noise voltage of the baseband TIA can be derived as

$$\overline{v_{n,B}^2} = \left[\frac{1}{1+T_o}\right]^2\left(\frac{\gamma R_L}{2}\right)^2\left[4kT\gamma_m\frac{g_1}{\gamma}\right] + 2kT\gamma R_L \tag{5.9a}$$

Let $\overline{v_{n,s}^2} = 4kTR_s$, $\overline{v_{n,sw}^2} = 4kTR_{sw}$ and $\overline{v_{n,sh}^2} = 4kTR_{sh}$ represent the mean square thermal noise voltage densities of the resistors $R_s$, $R_{sw}$ and $R_{sh}$ respectively. The output noise voltage of the receiver is

$$\overline{v_{n,Rx}^2} = G^2\left[\overline{v_{n,s}^2} + \overline{v_{n,sw}^2} + \left(\frac{R_a}{R_{sh}}\right)^2\overline{v_{n,sh}^2}\right] + \overline{v_{n,B}^2} \tag{5.10a}$$

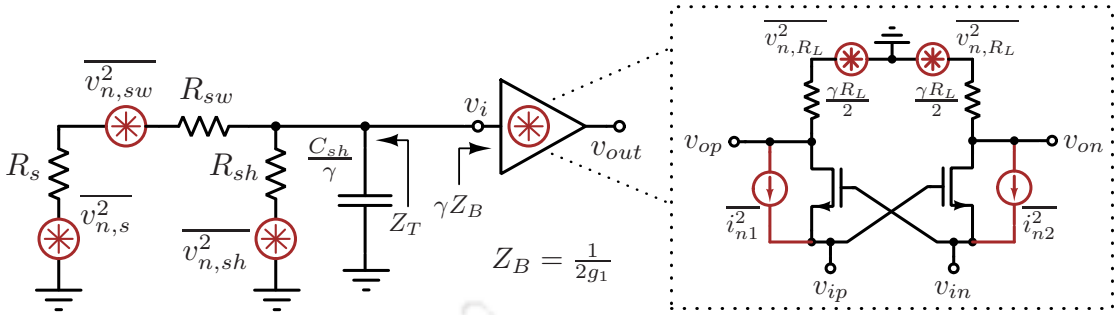



**Figure 5.7:** LTI model of the mixer-first receiver with all the noise contributing components.

From (5.10a), the noise factor of the receiver can be derived as

$$\begin{aligned} F &= 1 + \frac{R_{sw}}{R_s} + \frac{R_{sh}}{R_s}\left(\frac{R_a}{R_{sh}}\right)^2 + \frac{\overline{v^2_{n,B}}}{(G)^2 4kTR_s} \\ &= 1 + \frac{R_{sw}}{R_s} + \frac{R_{sh}}{R_s}\left(\frac{R_a}{R_{sh}}\right)^2 + \frac{\gamma\gamma_m}{4g_1R_s}\left(\frac{R_a}{Z_T}\right)^2 \\ &\quad + \frac{\gamma(1+T_o)^2}{2{g_1}^2R_sR_L}\left(\frac{R_a}{Z_T}\right)^2 \end{aligned} \tag{5.11a}$$

Fig. 5.8 shows a comparison of analytical (Eq. (5.11a)) and simulated noise figures for different values of $g_1$. In this work, a $g_1$ of 2.28 m℧ is chosen for the implementation. This design choice ensures a good input match, a single-path conversion gain of $\approx$ 12 dB (including the source resistance), and an estimated NF $<$ 4 dB.

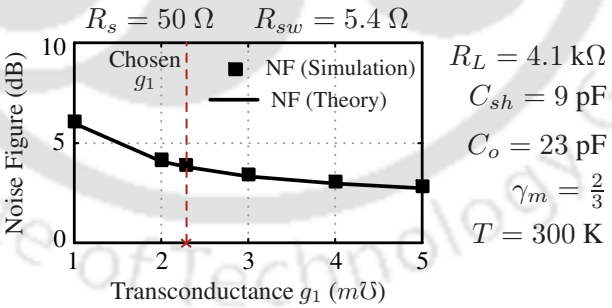



**Figure 5.8:** Comparison of analytical and simulated noise figure of the receiver with varying baseband transconductance ($g_1$) for $f_{LO} = 1$ GHz. Ideal transconductors with noise current-sources are used in the baseband stage for these simulations.

### 5.3.4 Linearity

In general, the mixer-switches are highly linear [104], and the overall in-band linearity of a mixer-first receiver is dominated by the linearity of the baseband TIA. In the present analysis, it is assumed that the mixer switches are completely linear, and distortion is caused by the baseband transconductors only.

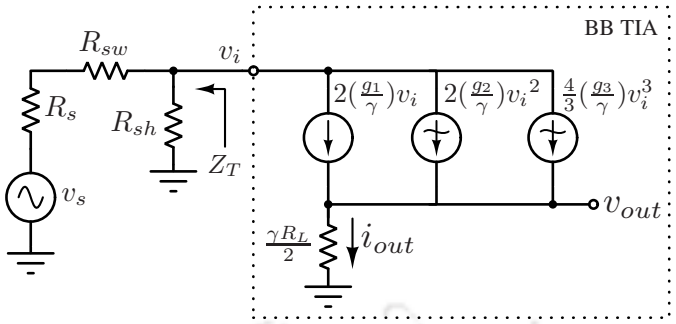



**Figure 5.9:** An in-band LTI model of the mixer-first receiver showing the distortion currents of the baseband TIA.

Fig. 5.9 shows an in-band LTI model of the mixer-first receiver, including the nonlinear current components in the TIA. The following equation can be written using the nodal analysis on the circuit shown in Fig. 5.9.

$$\frac{v_i - v_s}{R_a} + \frac{v_i}{R_{sh}} + 2\frac{g_1}{\gamma}v_i + 2\frac{g_2}{\gamma}{v_i}^2 + \frac{4}{3}\frac{g_3}{\gamma}{v_i}^3 = 0 \tag{5.12a}$$

Using the output current equation in (4.11a), the output voltage can be represented as

$$\begin{aligned} v_{out} &= \frac{\gamma R_L}{2} i_{out} \\ &= \frac{\gamma R_L}{2}\left[2\frac{g_1}{\gamma}v_i + 2\frac{g_2}{\gamma}{v_i}^2 + \frac{4}{3}\frac{g_3}{\gamma}{v_i}^3\right] \end{aligned} \tag{5.13a}$$

Using equations (5.12a) and (5.13a), the fundamental and third harmonic coefficients of the gain are

$$\begin{aligned} A_1 &= \frac{g_1 R_L}{(1+T_o)}\left[\frac{Z_T}{R_a}\right], \\ A_3 &= \frac{2}{3}\frac{g_3 R_L}{(1+T_o)^4}\left[1 - \frac{3{g_2}^2}{g_1 g_3}\frac{T_o}{(1+T_o)}\right]\left[\frac{Z_T}{R_a}\right]^3. \end{aligned}$$

Hence, the in-band IIP3 of the receiver is

$$\begin{aligned} A_{IIP3,IB} &= \sqrt{\frac{4}{3}.\left|\frac{A_1}{A_3}\right|} \\ &= \sqrt{2\left|\frac{g_1}{g_3}.\frac{(1+T_o)^3}{\left[1 - \frac{3{g_2}^2}{g_1 g_3}\frac{T_o}{(1+T_o)}\right]}.\left[\frac{R_a}{Z_T}\right]^2\right|} \end{aligned} \tag{5.15a}$$

In the above expression, the term $\left[\frac{3{g_2}^2}{g_1 g_3}\frac{T_o}{(1+T_o)}\right]$ in the denominator is due to the second-order interaction [15, 141]. The even-order harmonics, due to feedback, gets multiplied by the input tones to generate this distortion term. This term degrades the IIP3 because $g_1$ and $g_3$ usually have opposite signs. However, if $g'_{mp}$ and $g'_{mn}$ are properly matched, then $g_2$ is almost equal to zero. $g_3$ can be reduced if pMOS and nMOS transistors are

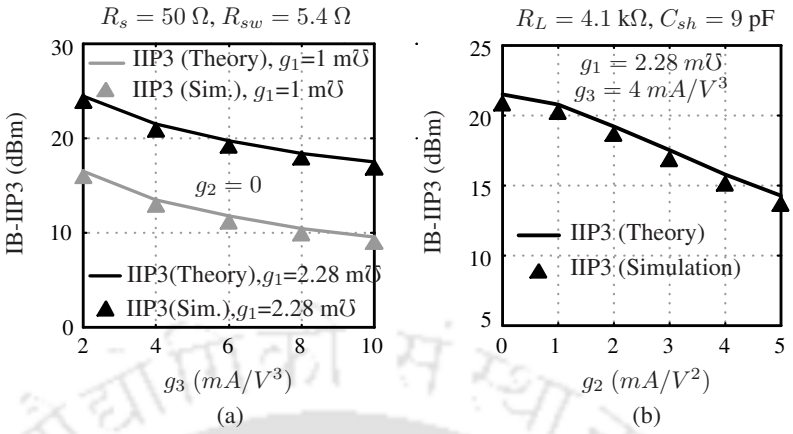



**Figure 5.10:** (a) Comparison of simulated and analytical (Eq. (5.15a)) IB-IIP3 of the receiver at $f_{LO} = 1\ GHz$ with varying $g_3$. $g_2$ is considered zero for this analysis. (b) Effect of second-order distortion on the IB-IIP3 of the receiver at $f_{LO} = 1\ GHz$ for $g_1 = 2.28\ m℧$ and $g_3 = 4\ mA/V^3$. Ideal transconductors with nonlinear current source models are used in the baseband stage for these simulations.

appropriately biased, such that both $g''_{mp}$ and $g''_{mn}$ have near-zero values. Fig. 5.10(a) shows a comparison of simulated and analytical (Eq. (5.15a)) IB-IIP3 of the receiver with varying $g_3$. The second-order distortion coefficient ($g_2$) is assumed to be zero in the analysis shown in Fig. 5.10(a). Fig. 5.10(b) shows the effect of second-order distortion on the receiver IIP3. It is observed that the IB-IIP3 of the receiver decreases with an increase in second-order distortion.

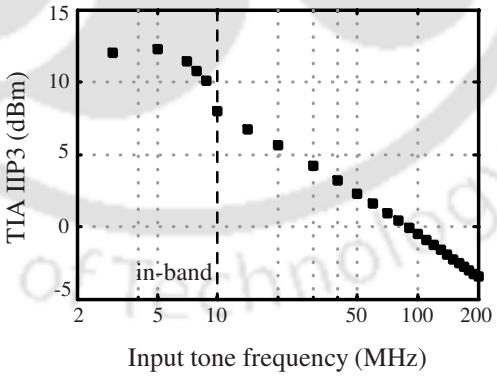



**Figure 5.11:** Simulated IIP3 of the proposed TIA with the varying input tone frequency. The component values used in the implementation of the TIA are shown in Fig. 5.19(c).

The employed linearization technique is not effective in improving the out-of-band (OOB) IIP3 of the receiver. One can set $|g_2| \approx 0$ (by proper design of the transconductors) at low frequencies, but $|g_2|$ increases with frequency due to parasitic feedback paths [141]. Also, the optimum gate-bias voltage for a MOS transistor changes with varying input-tone frequency [83]. Hence, for a specific gate-bias voltage, the linearity improvement

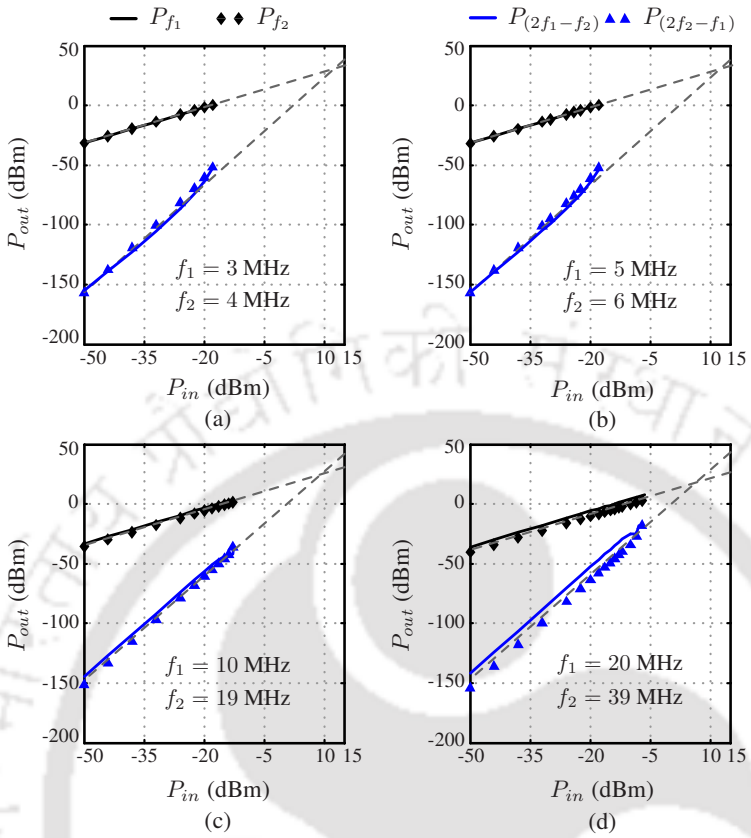



**Figure 5.12:** Simulated output power levels $P_{f_1}$, $P_{f_2}$, $P_{(2f_1-f_2)}$, $P_{(2f_2-f_1)}$ of the designed TIA with varying $P_{in}$ for the following input tone frequencies: (a) $f_1 = 3$ MHz, $f_2 = 4$ MHz, (b) $f_1 = 5$ MHz, $f_2 = 6$ MHz, (c) $f_1 = 10$ MHz, $f_2 = 19$ MHz and (d) $f_1 = 20$ MHz, $f_2 = 39$ MHz.

may not be uniform with varying input tone frequencies. Fig. 5.11 shows the simulated IIP3 of the designed TIA with varying input-tone frequency. The component values and the bias-voltages used in the TIA implementation are given in the following section. From Fig. 5.11, it is observed that the linearity performance of the TIA degrades beyond its bandwidth (which is 10 MHz in the current design).

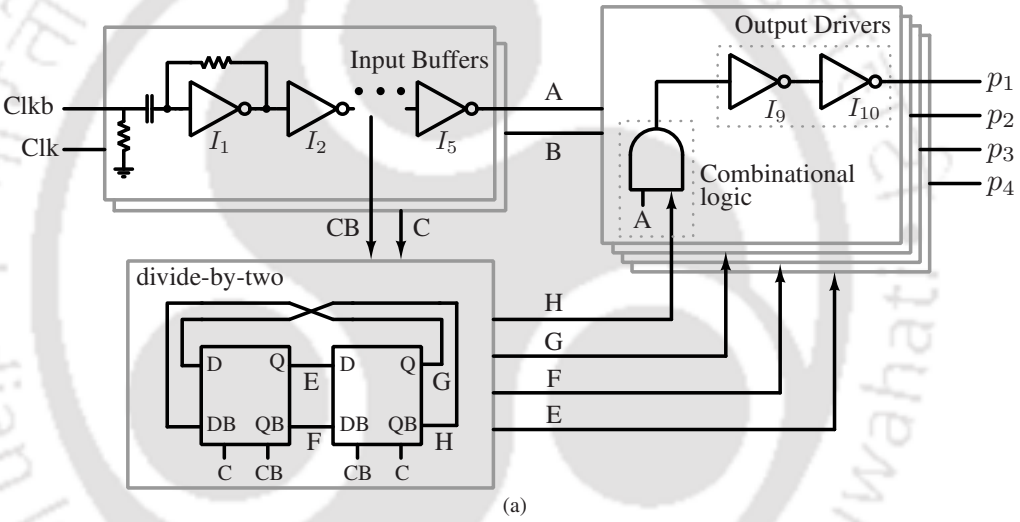
In order to understand the effect of input tone frequency on the IIP3 of the baseband TIA, the linear $\{P_{f_1}, P_{f_2}\}$ and IM3 $\{P_{(2f_1-f_2)}, P_{(2f_2-f_1)}\}$ output components are plotted in Fig. 5.12 with varying input power and for different input tone combinations. The magnitudes of the two IM3 components are completely identical when the two input tones are in-band, as shown in Fig. 5.12(a) and 5.12(b). Even when the tones are just outside the bandwidth of the TIA, the IM3 components show good symmetry (as shown in Fig. 5.12(c)). However, as the tones move further away from the TIA-bandwidth, some IM3 mismatch starts to appear, as shown in Fig. 5.12(d). When the two input tones are within the bandwidth of the system, the even-order terms go through identical responses, and good symmetry can be observed between the higher $(2f_2 - f_1)$ and lower $(2f_1 - f_2)$ IM3 components [86]. However, when the input tones are out-of-band, the different even-order terms experience

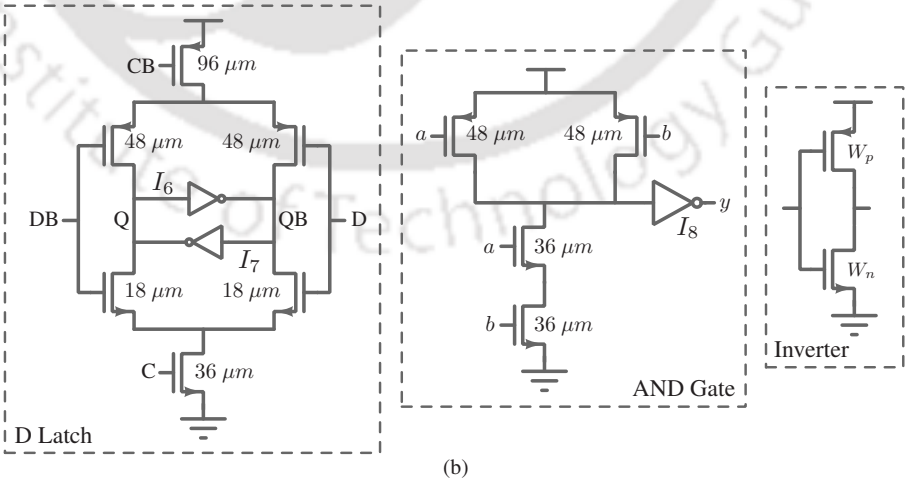
different amplitude and phase responses, eventually leading to the asymmetry in the IM3 components [86]. This asymmetry becomes larger as the offset between the two input tones increases [86].

## 5.4 Receiver design

### 5.4.1 Design of Non-overlapping Clock Generator

An on-chip clock divider and a set of combinational logic circuits are used to generate the four non-overlapping clock signals $p_1 - p_4$. Fig. 5.13(a) shows the gate-level schematic of the non-overlapping clock generator. An external clock signal is converted to a differential clock using an off-chip splitter (SYPJ-2-33+) and then fed to the non-overlapping clock generating circuit.




| Inverter | $I_1$ | $I_2$ | $I_3$ | $I_4$ | $I_5$ | $I_6$ | $I_7$ | $I_8$ | $I_9$ | $I_{10}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| Inverter sizes $W_p$ ($\mu m$) | 62.4 | 96 | 144 | 144 | 144 | 33.6 | 33.6 | 72 | 124.8 | 307.2 |
| $W_n$ ($\mu m$) | 23.4 | 36 | 54 | 54 | 54 | 12.6 | 12.6 | 27 | 46.8 | 115.2 |

(c)

**Figure 5.13:** Schematic of the non-overlapping clock generator.

The first stage of the non-overlapping clock generator is a shunt-feedback LNA that provides a broadband input match. The high-frequency clock (at $2f_{LO}$) is then converted to a square wave using a chain of inverters ($I_2 - I_5$) and fed to the divide-by-two circuit. The frequency divider consists of two back-to-back connected D-latches, as shown in Fig. 5.13(a). The output of the divide-by-two circuit is a set of four 50% duty-cycled clocks at $f_{LO}$: $E$, $F$, $G$, and $H$. These 50% duty-cycled clocks ($E$, $F$, $G$, and $H$) are combined with the $2f_{LO}$ clocks to generate the non-overlapping 25% duty-cycled clocks at $f_{LO}$. A set of inverters ($I_9 - I_{10}$) is used at each output of the non-overlapping clock generator to drive the mixer switches. Fig. 5.13(b) shows the transistor-level schematics of the D-latch, AND-gate, and the inverter. The dimensions of the pMOS and nMOS transistors used in all the inverters are mentioned in Fig. 5.13(c). A channel length of 180 nm is chosen for all the transistors used to implement the non-overlapping clock generator.

### 5.4.2 Mixer design

Switches of the mixer are realized using nMOS transistors. Separate biasing is applied at the gates of the nMOS transistors using a resistor of 11 kΩ and a capacitor of 3.3 pF, as shown in Fig. 5.3. The gate biasing helps to overcome the DC offset present at the source nodes of mixer-switches. The size of the switches poses a trade-off between the dynamic power consumption and the noise figure of the receiver. The IIP3 of the receiver is also a strong function of the switch width below a threshold value. Fig. 5.14 shows the variation of noise figure and input third-order intercept point (IIP3) of the mixer switches with varying gate-width in 180 nm CMOS process. Ideal TIAs are used in this simulation. A size of $120\mu m/0.18\mu m$ is chosen for the nMOS transistors in this implementation. From Fig. 5.14, the theoretical bounds defined by the mixer are NF $\geq$ 1.9 dB and an IIP3 of $\leq +18$ dBm. Each mixer switch is followed by a shunt capacitor ($C_{sh}$) of 9 pF in the current implementation.

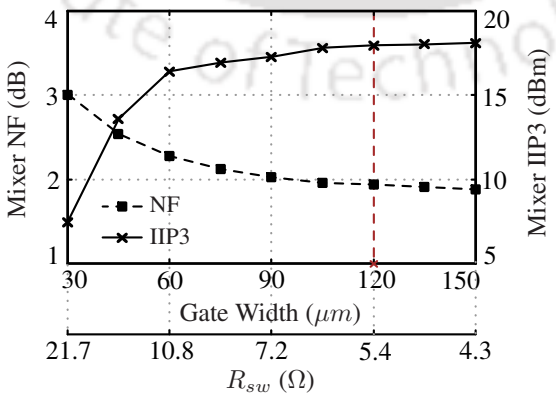



**Figure 5.14:** Simulated noise figure and IIP3 of the mixer switches with varying gate-width for a channel length of 180 nm.

### 5.4.3 Baseband TIA design

The baseband TIA is the only block that consumes the static power in a mixer-first receiver. Since the objective of the current work is to design a low-power mixer-first receiver, the TIA is optimized for the smallest power consumption possible. For 50 Ω impedance matching at the RF input, we need a transconductance of $\approx 1.14\ m\mho$ per transistor ($g_1 = 2.28\ m\mho$) in the TIA. The bias network (as shown in Fig. 4.3(a)) of the TIA is implemented using a resistor ($R_c$) of 20 kΩ and a capacitor ($C_c$) of 20 pF. The drain nodes of the MOS transistors are terminated with load resistances ($R_L$) of 4.1 $k\Omega$. The pMOS and nMOS drain voltages are combined using two output capacitors ($C_o$) of 23 pF.

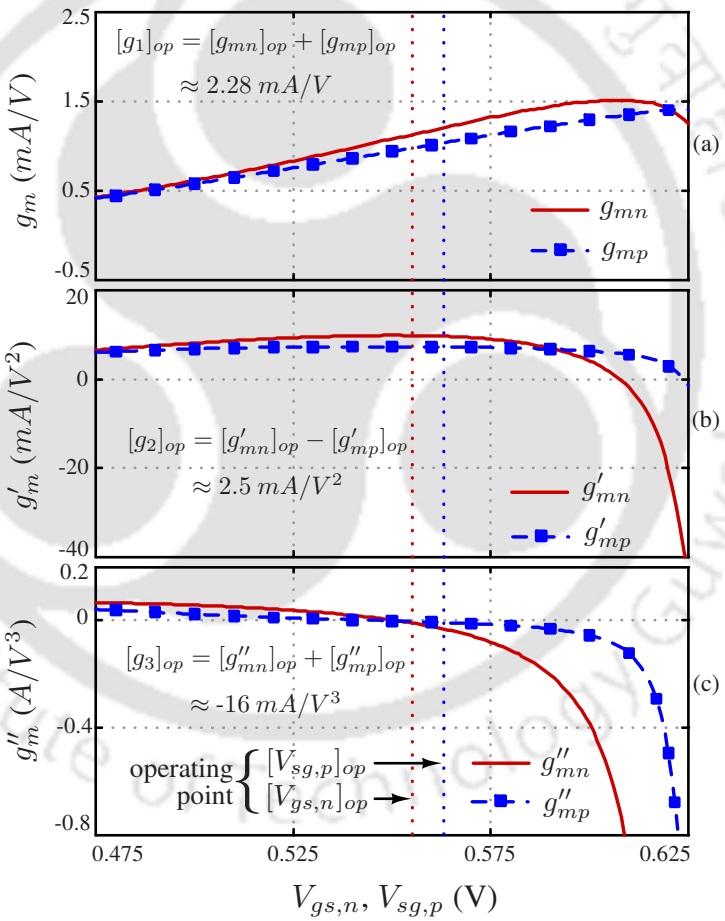



**Figure 5.15:** Simulated (a) transconductance, (b) second-order distortion coefficients and (c) third-order distortion coefficients of the pMOS and nMOS transistors with varying gate-to-source voltage. Selected transistor dimensions are: $(W/L)_n = 30\mu m/0.5\mu m = 60$, $(W/L)_p = 88.5\mu m/0.5\mu m = 177$.

The dimensions and the biasing voltages of the transistors are chosen to optimize the linearity. In this design, nMOS transistors of $(W/L)_n = 30\mu m/0.5\mu m$ and pMOS transistors of $(W/L)_p = 88.5\mu m/0.5\mu m$ are used. Fig. 5.15(a), 5.15(b), and 5.15(c) show the first-order, second-order, and third-order transconductances of the

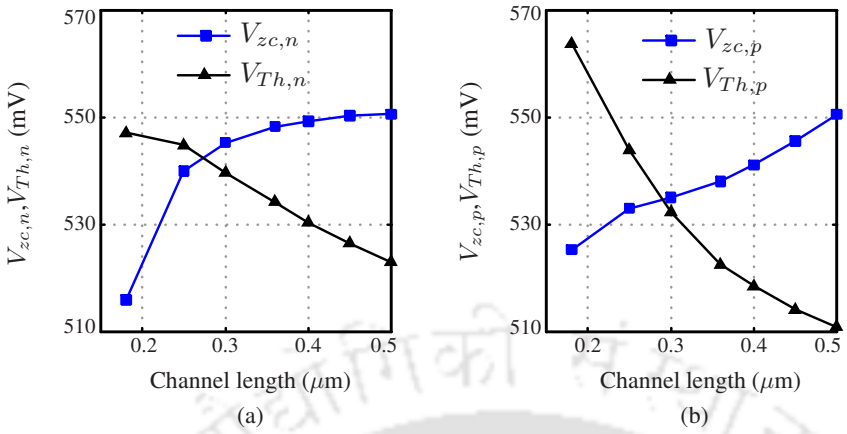



**Figure 5.16:** Variation of $g_m''$-zero-crossing gate-to-source voltage and threshold voltage of an (a) nMOS, (b) pMOS transistor with channel length. $(W/L)_n = 60$ and $(W/L)_p = 177$ is used in these simulations.

nMOS and pMOS transistors used in this design. For best linearity, one has to operate the nMOS and pMOS transistors at bias voltages, which results in $g''_{mn} \approx g''_{mp} \approx 0$. One also has to ensure $g'_{mn} \approx g'_{mp}$ to mitigate the second-order interaction induced third-order nonlinearity. From Fig. 5.15, the optimum gate-to-source voltages are found to be $\approx 555$ mV for nMOS and $\approx 563$ mV for pMOS transistors.

The optimum gate-to-source voltage for best linearity also depends on the channel length of the transistors. Let, $V_{zc,n}$ and $V_{zc,p}$ represent the $g_m''$-zero-crossing gate-to-source voltage of the nMOS and pMOS transistor, respectively. Fig. 5.16(a), 5.16(b) shows the typical variations of $g_m''$-zero-crossing voltage and threshold voltage with varying channel length. From Fig. 5.16, it can be observed that $V_{zc,n}$ (or $V_{zc,p}$) is lower than the threshold voltage $V_{Th,n}$ (or $V_{Th,p}$) for small channel length devices. Therefore, one has to operate the transistors in sub-threshold in small channel-length designs for the linearization technique to be effective. In general, sub-threshold operation leads to reduced bandwidth and increased noise. As a result, the implementation of the employed linearization technique in advanced technology nodes while maintaining the required bandwidth and noise performance is a challenging task. In the present implementation, $0.5\ \mu m$ channel length is chosen to avoid sub-threshold operation, and also to reduce the flicker noise.

In the proposed TIA, one can set $V_{gs,n} \approx 555$ mV and $V_{sg,p} \approx 563$ mV by different combinations of $V_{bn}$ and $V_{bp}$ values. Fig. 5.17(a) shows the variation of TIA IIP3 with bias voltages $V_{bn}$ and $V_{bp}$. In the present implementation, we have chosen $V_{bn} = 1.45$ V, and $V_{bp} = 0.33$ V. Fig. 5.17(b) and 5.17(c) show the IIP3 variation at extreme PVT corners. From Fig. 5.17, the TIA can achieve high linearity performance at any given PVT condition subject to the proper selection of the bias voltages. The automatic setting of bias voltages for high IIP3 requires further research and is not explored in this work.

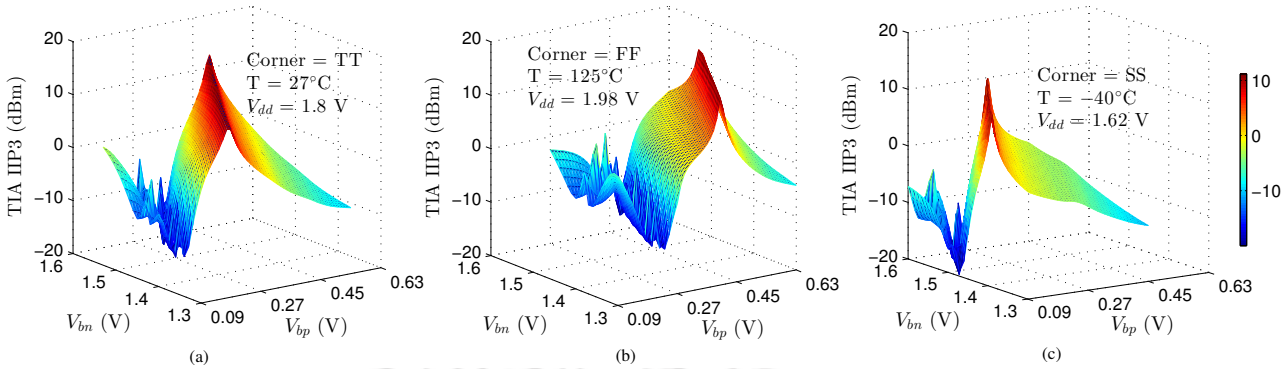



**Figure 5.17:** Simulated IIP3 of the proposed TIA with varying bias voltages $V_{bp}$ and $V_{bn}$ at the following three PVT settings: (a) corner = TT, $V_{dd} = 1.8$ V, $T = 27°$ C, (b) corner = FF, $V_{dd} = 1.98$ V, $T = 125°$ C and (c) corner = SS, $V_{dd} = 1.62$ V, $T = -40°$ C.

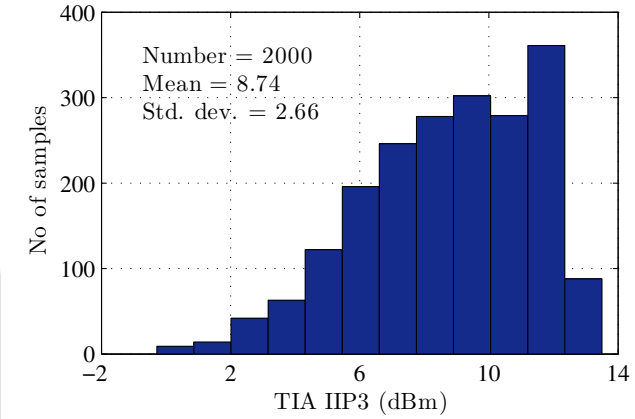
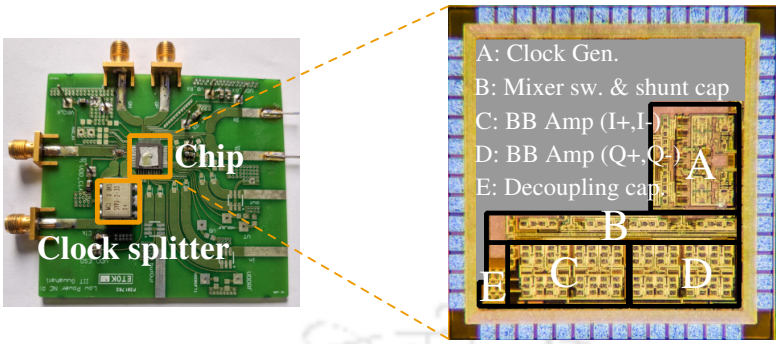



**Figure 5.18:** Variation of TIA IIP3 from Monte-Carlo simulation.

Fig. 5.18 shows the distribution of TIA IIP3 under the statistical variation of process and device mismatches. The obtained samples have a statistical mean of 8.74 dBm with a standard deviation ($\sigma$) of 2.66 dBm. Around 64.2% of the total samples lie within $\pm$ 1$\sigma$ of the mean value.

## 5.5 Measurement results

A prototype receiver is implemented in a standard 180 nm CMOS technology. The chip is enclosed in a 56-pin QFN package and mounted on an FR-4 PCB for testing. The testing PCB and the chip micrograph is shown in Fig. 5.19(a) and 5.19(b), respectively. Fig. 5.20 shows the receiver test-setup with various measuring instruments. All bias voltages (for switches and transconductors) are supplied externally. If not mentioned otherwise, the following TIA bias voltages are used in all the measurements: $V_{bn} = 1.45$ V and $V_{bp} = 0.33$ V.




(a) (b)

| $M_{1,2n}$ | $M_{1,2p}$ | $C_{sh}$ | $C_c$ | $R_c$ | $R_L$ | $C_o$ |
|---|---|---|---|---|---|---|
| $\frac{30\mu m}{0.5\mu m}$ | $\frac{88.5\mu m}{0.5\mu m}$ | $9\ pF$ | $20\ pF$ | $20\ k\Omega$ | $4.1\ k\Omega$ | $23\ pF$ |

(c)

**Figure 5.19:** Photographs of the (a) testing board and (b) chip. (c) Component values used in the implementation of the mixer-first receiver.

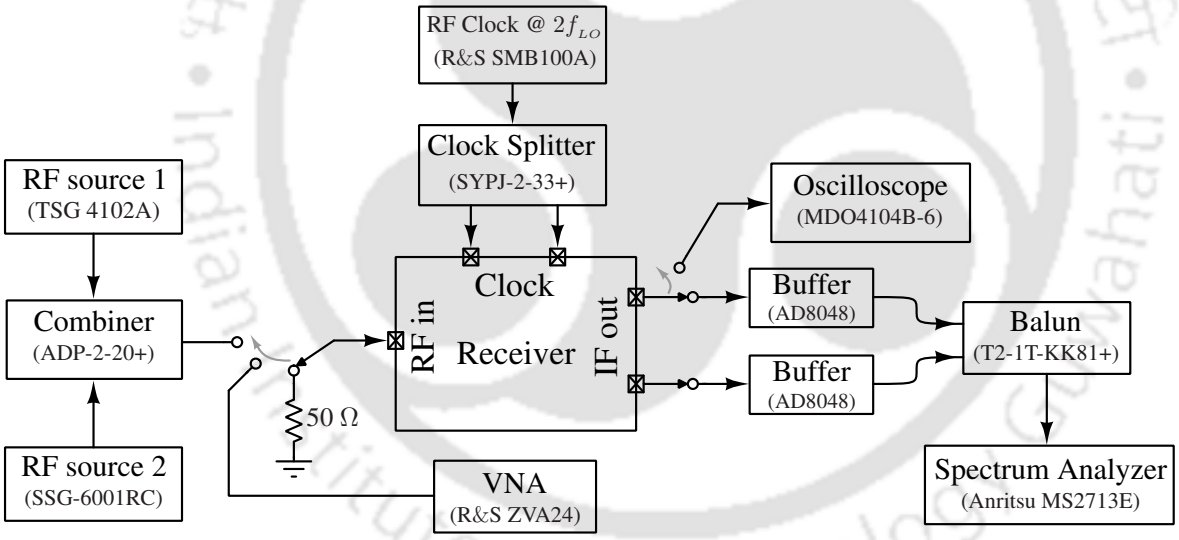



**Figure 5.20:** Receiver test-setup with various measuring instruments.

The component values used in the implementation are shown in Fig. 5.19(c).

The receiver is tunable from 0.3 GHz to 1.3 GHz. Depending on the frequency of operation, the clock path consumes 21.6-75 mA of current from a 1.8 V supply voltage. Each baseband TIA consumes around 188.9 $\mu$A from a 1.8 V power supply resulting in a 0.68 mW of power consumption for the receiver (Rx). The non-overlapping clock generator consumes $\approx$ 100 mW/GHz from a 1.8 V supply voltage. Table 5.1 shows the dynamic power distribution of the non-overlapping clock generator at 1 GHz.

**Table 5.1:** Dynamic power distribution of the clock generator at 1 GHz

| Block | Power (mW) |
|---|---|
| Input buffers | 44.6 |
| divide-by-two | 13 |
| Combinational logic | 14.7 |
| Output drivers | 27.7 |
| Total | 100 |

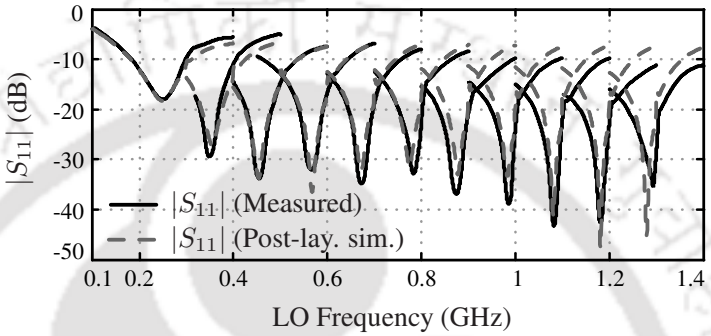



**Figure 5.21:** Measured $|S_{11}|$ plot of the receiver at different LO frequencies.

Fig. 5.21 shows the measured $|S11|$ of the receiver. The receiver has an $|S11| < -15$ dB and a conversion gain greater than 20 dB over the frequency range 0.3-to-1.3 GHz. Fig. 5.22 shows the measured conversion gain and noise figure of the receiver at 1 GHz LO with varying IF frequency. The measured BB bandwidth is $\approx$ 10 MHz. The designed receiver has an almost flat noise figure for $>$ 3 MHz IF frequency. The measured conversion gain and NF of the receiver at different LO frequencies are shown in Fig. 5.23. The measured NF varies from 5.7 dB to 6.3 dB over the LO frequency range 0.3-to-1.3 GHz for an IF frequency of 4 MHz. Fig. 5.24 shows the simulated NF of the receiver at 1 GHz LO frequency in the presence of a blocker at two different offset frequencies: $\Delta f/BW = 5$ and $\Delta f/BW = 10$. Fig. 5.25(a) and 5.25(b) show the measured receiver gain with varying bias voltage $V_{bp}$ and $V_{bn}$, respectively.

The imbalance between the in-phase (I) and the quadrature-phase (Q) output paths are characterized using the test setup shown in Fig. 5.26(a). The gain and phase mismatches are estimated from the time-domain waveforms of the output signals using an oscilloscope. Fig. 5.26(b) shows the four output signals $(I+, I-, Q+, Q-)$ when the LO is at 500 MHz, and the RF input is at 498 MHz. For 500 MHz LO, the measured gain and phase errors are $\approx$ 0.1 dB and $\approx$ 3.6°, respectively, which leads to an estimated image rejection of $\approx$ 30 dB [12]. Fig. 5.27(a) and 5.27(b) show the measured I/Q gain and phase errors at different LO frequencies, respectively. Between 0.4-1.1 GHz, the gain error is $\leq$0.5 dB, and the phase error is $\leq$ 5.5°. The current

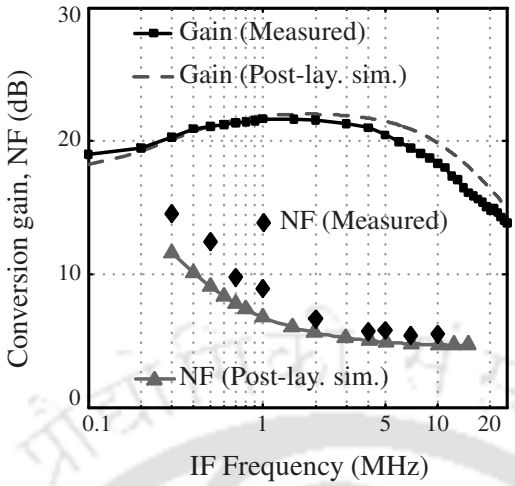



**Figure 5.22:** Measured conversion gain and noise figure of the receiver at 1 GHz LO with varying IF frequency.

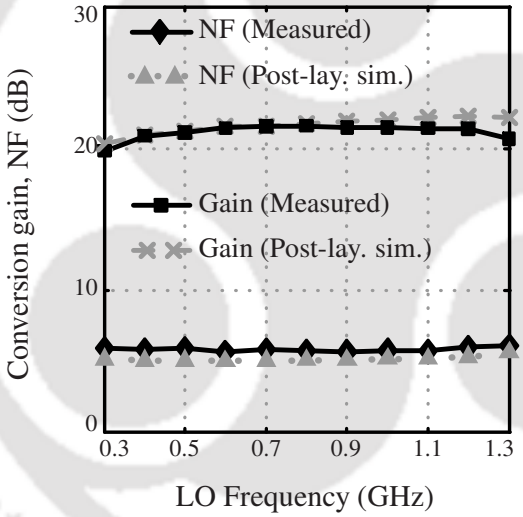



**Figure 5.23:** Measured conversion gain and noise figure of the receiver at different LO frequencies.

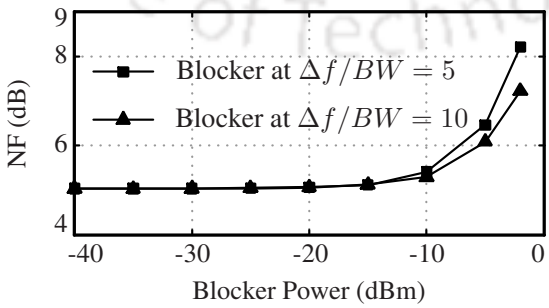



**Figure 5.24:** Simulated noise figure of the receiver at 1 GHz LO frequency in the presence of a blocker.

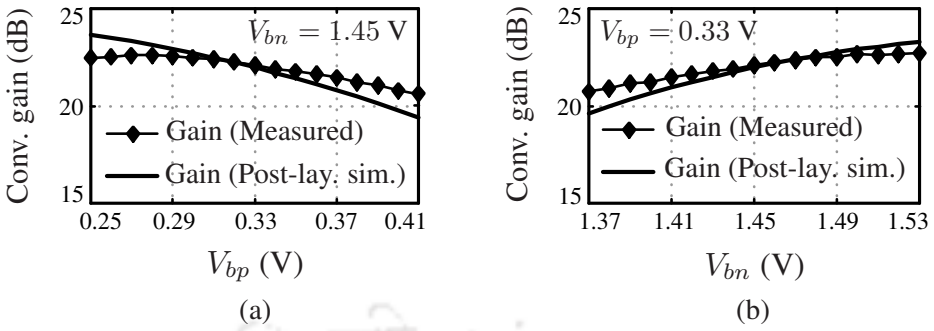



**Figure 5.25:** Measured conversion gain of the receiver at 1 GHz LO frequency with varying bias voltage (a) $V_{bp}$ and (b) $V_{bn}$.

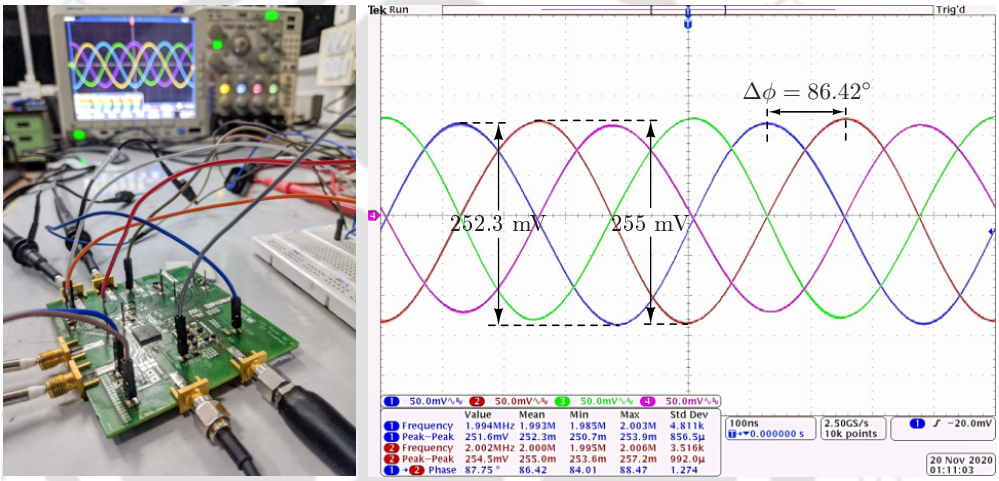



**Figure 5.26:** (a) Photograph of the test setup for the measurement of I/Q gain and phase errors. (b) The four output waveforms ($I+, I-, Q+, Q-$) for $-23$ dBm 498 MHz RF input with 500 MHz LO.

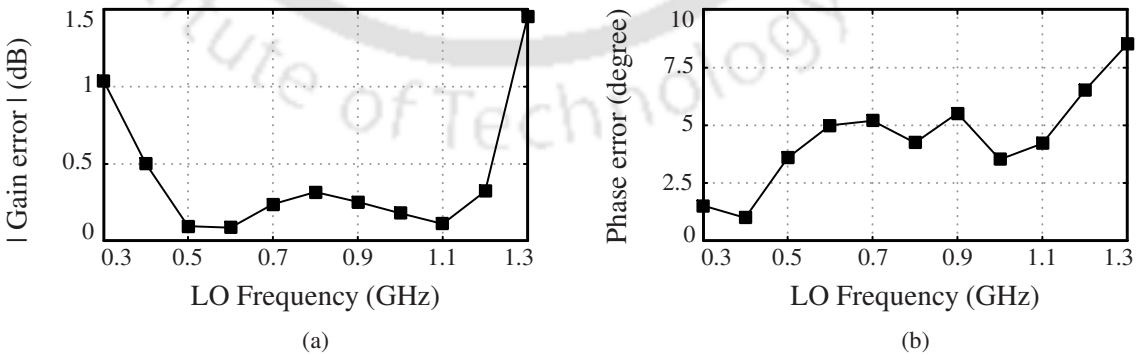



**Figure 5.27:** Measured I/Q (a) gain error and (b) phase error of the receiver at different LO frequencies.

implementation of the receiver does not have an I/Q calibration circuitry, which, if present, can reduce the I/Q mismatches.

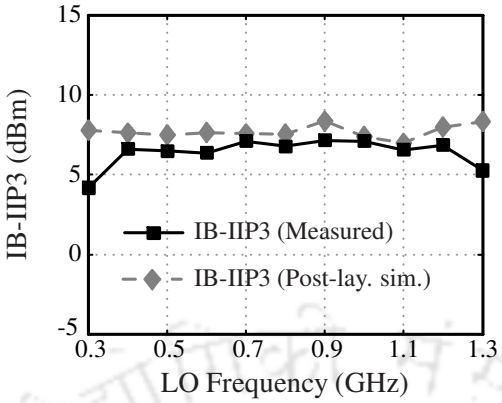



**Figure 5.28:** Measured IB-IIP3 of the receiver at different LO frequencies.

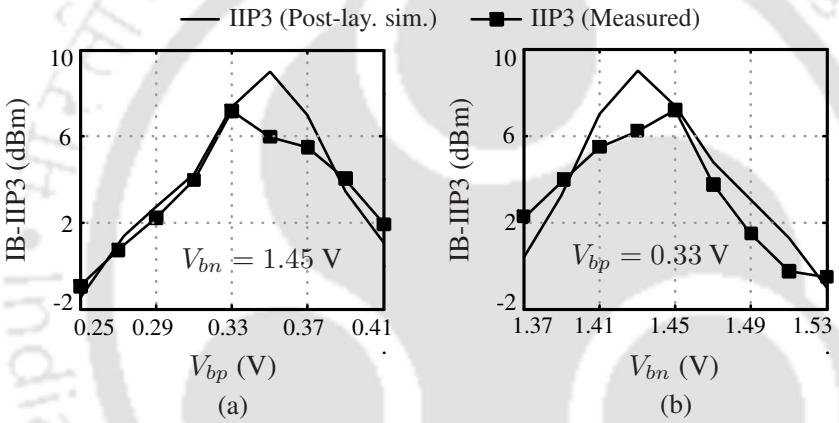



**Figure 5.29:** Measured IB-IIP3 of the receiver at 1 GHz LO frequency with varying TIA bias voltage (a) $V_{bp}$ and (b) $V_{bn}$.

Fig. 5.28 shows the measured IB-IIP3 of the receiver at different LO frequencies. The receiver has $\approx +7.2$ dBm measured IB-IIP3 at 1 GHz LO frequency. Bias voltages of the baseband TIA play an important role in the obtained IIP3 of the receiver. Fig. 5.29(a) and 5.29(b) show the measured IB-IIP3 of the receiver with varying $V_{bp}$ and $V_{bn}$, respectively. Out-of-band (OOB) IIP3 measurements are carried out using two tones at $f_1 = f_{LO} - \Delta f$ and $f_2 = f_{LO} - 2\Delta f + 1$ MHz, where $f_{LO}$ is the LO frequency and $\Delta f$ is the frequency offset from the LO frequency. The receiver has an OOB-IIP3 of $4.5$ dBm at an offset of twice the bandwidth. Fig. 5.30(a) shows the measured OOB-IIP3 of the receiver at 1 GHz LO frequency for varying $\Delta f/BW$. Similarly, OOB-IIP3 points are measured at various LO frequencies for a fixed frequency offset $\Delta f/BW = 2$. Fig. 5.30(b) shows the variation of OOB-IIP3 across the LO frequency range (for a $\Delta f/BW = 2$).

Table 5.2 shows a comparison of this work with different mixer-first receivers reported in the literature. The IB-IIP3 of the proposed receiver is on par with the high-linearity mixer-first receivers and much better than the

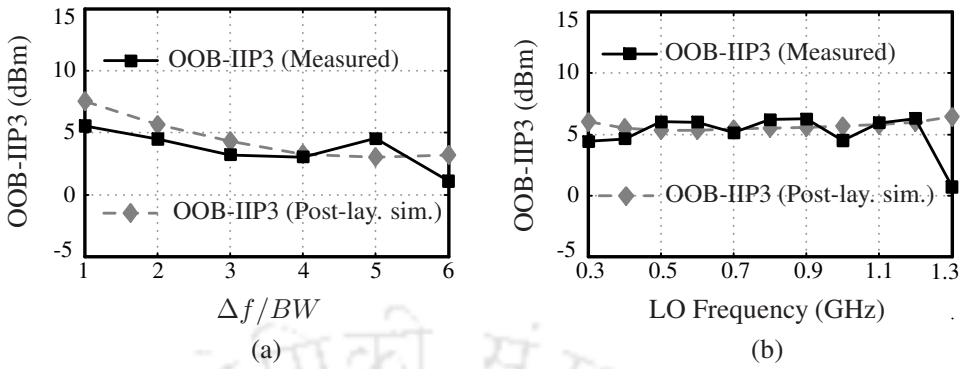



**Figure 5.30:** (a) Measured OOB-IIP3 of the receiver for varying $\Delta f/BW$ at 1 GHz LO frequency. (b) Measured OOB-IIP3 of the receiver at different LO frequencies for $\Delta f/BW = 2$.

low-power mixer-first receivers or noise-canceling mixer-first receivers. The clock power consumption of the proposed receiver is slightly on a higher side, but can be significantly reduced if implemented in an advanced CMOS process (because of reduced parasitic capacitances in an advanced CMOS process). Although [31, 109] achieve a better noise figure by employing the RF noise-canceling technique, their Rx power consumption is much higher than the proposed work. The proposed receiver has achieved a wider frequency tuning range with similar noise performance as compared to recent discrete-time mixer-first receivers [112, 113]. Overall, the implemented mixer-first receiver achieved a good in-band SFDR while consuming the lowest Rx power.

**Table 5.2:** Performance comparison with recent mixer-first receivers

| | | Tech. (nm) | Gain (dB) | $f_{RF}$ (GHz) | BB BW (MHz) | NF (dB) | IB-IIP3 (dBm) | IB-SFDR (dB)‡ | OOB-IIP3 (dBm @ $\Delta f/BW$) | Supply (V) | Power (mW) | | Area ($mm^2$) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | Rx | Clock | |
| **This Work** | | 180 | 21.9 | 0.3-1.3 | 10 | 5.7-6.3 | +7.2 | 76.9 | 4.5 @ 2 | 1.8 | **0.68** | 100$^{\diamond}$ | 0.728 |
| High Linearity | JSSC20 [147] | 180 | 31.4 | 0.2-1.2 | 18 | 3.4-4 | +14.5 | 83.2 | 39.8 | 1.8 | 19.8 | 45-135 | 0.54 |
| | SSCL19 [108] | 28 | 32.4 | 0.5-2 | 130 | 5.5$^{\clubsuit}$ | $-12^{\boxplus}$ | 64.3 | 21 @ 3 | 1.8/1.2 | 21.6 | 7.8$^{\diamond}$ | 0.16 |
| | JSSC19 [29] | 28 | 16 | 0.1-2 | 6.5 | 4.1-10.3 | $+5^{\dagger}$ | 76.6 | 44 @ 12.3 | 1.2/1 | 30 | 33$^{\diamond}$ | 0.49 |
| | JSSC18 [30] | $45^{\pi}$ | 21 | 0.2-8 | 10 | 2.3-5.4 | $0^{\dagger}$ | 73.4 | 39 @ 8 | 1.2 | 50 | 30$^{\diamond}$ | 0.8 |
| | ISSCC17 [106] | 65 | 23 | 0.1-1 | 1.25-20 | $7^{\in}$ | +8 | 76.7 | 21 @ 1.2 | 1.2/1 | $64-84$ mA$^{\perp}$ | | 2.3 |
| | TMTT16 [101] | 28 | 35 | 0.4-3.5 | 50 | 2.4-2.6 | $+8^{\dagger}$ | 79.7 | 20.5 @ 3.3 | $1.1/1.5^{\theta}$ | 38-75$^{\star}$ | | 0.23 |
| | ESSCIRC15 [119] | 65 | 40 | 0.8-3 | – | 5.5-7.8 | – | – | 17 | – | $32-38$ | | 0.5 |
| | JSSC14 [111] | 65 | 26.5 | 0.2-2.6 | 12 | 7.5 | +21 | 85 | 18 @ 37.5 | 1.2 | 13.9 | 3.4-22.8 | $<0.2$ |
| Low Power | RFIC18 [120] | $45^{\pi}$ | $14-40$ | 0.1-3 | 20-165 | 3-6 | – | – | – | 0.9/1.8 | $16^{\odot}$ | | 1.95 |
| | JSSC17 [102] | 65 | 36 | 0.84-1.88 | 9 | $3.2^{\xi}$ | −12 | 65.9 | 8 @ 8.88 | 1 | 13 | 3.3-7 | $0.038^{\nabla}$ |
| | ISSCC15 [121] | 65 | 38 | 0.1-1.5 | 2 | 1.5-2.9 | – | – | 13 | 0.7, 1.2 | $11^{\ominus}$ | | 0.028 |
| | JSSC14 [115] | 65 | 51±1 | 0.15-0.85 | 9 | 4.6±0.9 | −12 | 65.5 | 17.4 | 1.2/2.5 | 7.5 | 3.1-8.7 | 0.55 |
| | JSSC13 [114] | 65 | 37 | 0.7-3.2 | $0.1-20$ | 7-16 | $-43^{\dagger}$ | 42.7 | 6 | 1.3 | 1.8 | 8.2-10.2$^{\bullet}$ | 2.9 |
| | RFIC13 [110] | 65 | 20-36 | 0.1-0.8 | $5^{\dagger}$ | $3.6^{\square}$ | – | – | $7^{\square}$ | 1.2/1.6 | $23^{\times}$ | | 0.33 |
| RF Noise Canceling | JSSC15 [109] | 65 | 42 | 0.7-3.8 | 10 | $1.6-3.2$ | $-10^{\dagger}$ | 68.3 | 1 @ $5^{\dagger}$ | 1.2 | 7.44-20.4 | 12-26.4 | 0.15 |
| | JSSC12 [31] | 40 | 72 | 0.08-2.7 | 2 | 1.9 | – | – | 13.5 @ 40 | 1.3 | 31.2 | 3.9-46.8 | 1.2 |
| Discrete Time | JSSC19 [112] | $22^{\beta}$ | 13-14 | 0.6-1.3 | 16 | 5-6 | – | – | 25 @ 10 | 0.8 | $0^{\heartsuit}$ | 0.4-0.78 | 0.23 |
| | JSSC18 [113] | 65 | 35 | 0.1-0.6 | – | 4.6-9 | – | – | 31 | 1.1/1.25 | 24 | 9.5-55.8 | 1.63 |

‡ IB-SFDR = $\frac{2}{3}$[IB-IIP3+174-10log(1MHz)-NF]; $\clubsuit$ At $f_{LO} = 2$ GHz; $\diamond$ per 1 GHz; † Estimated from figures; $\pi$ SOI; $\theta$ 1.5 V for LDO;
$\boxplus$ Two-tones test with the first tone near center band and the second one near band edge; $\star$ Total power (includes on-chip LDOs);
$\xi$ At 1.88 GHz; $\in$ Excludes balun loss; $\perp$ Total current; $\nabla$ Includes transmitter (Tx) area; $\bullet$ Includes VCO power; $\odot$ At 1 GHz;
$\ominus$ At 1.5 GHz; $\square$ At maximum gain setting; $\times$ At 800 MHz LO; $\beta$ FDSOI; $\heartsuit$ No integrated baseband.

## 5.6 Summary

This chapter has demonstrated a four-phase passive mixer-first receiver with a low-power complementary common-gate TIA. The TIA is designed to exploit a complementary linearization technique without any additional power consumption. The receiver presented in this work has achieved an NF of 5.8 dB and an IB-IIP3 of +7.2 dBm with the lowest power consumption of 0.68 mW for baseband circuitry. Overall, the receiver achieved a measured IB-SFDR of 76.9 dB at 1 GHz.

भारतीय प्रौद्योगिकी संस्थान गुवाहाटी
Indian Institute of Technology Guwahati

# 6

# Conclusion and Future Scope



**Contents**

## 6.1 Summary and conclusion

This thesis investigated noise and linearity improvement techniques for low-power LNAs and receivers. A generic theory that can explain the operation of various noise-canceling circuits in the literature was proposed. The proposed generic theory unifies the analysis of existing noise-canceling circuits and highlights a few key insights into their operation [127]. The proposed theoretical claims were validated using circuit-level simulations. A systematic methodology was developed in this thesis for generating new flicker and thermal noise-canceling circuits. The proposed systematic method was used to design noise-canceling amplifiers and buffers with high input impedance [148]. A low-power partial noise-canceling complementary common-gate (CCG) LNA was also developed using the proposed method. The LNA was designed to achieve high IIP3 using a complementary linearization technique. For the linearization technique to be effective, the complementary transistors need to be properly biased. The same LNA was employed as the baseband trans-impedance amplifier (TIA) of a passive mixer-first receiver achieving high in-band linearity at low power levels. Prototypes of both the LNA and the mixer-first receiver were implemented in a standard 180 nm CMOS technology. The performance parameters of the designed LNA and the mixer-first receiver [149] were measured and compared with other relevant works in the literature.

Even though the LNA had high IIP3, it suffered from a poor 1-dB compression point. This is because the $g_m''$ values of complementary transistors deviate from their nominal values at high input power levels. Further, the optimal bias voltages required for high linearity vary with PVT. A negative feedback-based automatic optimal bias-setting scheme, if developed, is useful in maintaining the high linearity at various corners. In the proposed complementary CG LNA, it is not possible to achieve simultaneous low-NF and high-IIP3. Even though the dynamic power consumption of the prototype receiver is high, it can be reduced using low-power non-overlapping clock generation circuitry presented in [150]. Overall, it is the opinion of the author that one should use noise cancellation only to break the trade-off between NF and any other parameter of interest. In a noise-canceling LNA/receiver, the design of the main path is governed by the input matching condition while the auxiliary path is typically designed to have significantly lower noise than the main path. If not for satisfying the input matching criterion, one could use just the auxiliary stage as a stand-alone amplifier and still have similar noise performance as the noise-canceling amplifier.

## 6.2 Scope of future work

The study presented in this dissertation leads to several directions for future research.

- There are many recent reports on thermal noise-canceling phase-locked loop (PLL) [151–153] and analog-to-digital converter (ADC) [154, 155]. Whether or not the generic feedback-feedforward model proposed in this thesis helps analyze these NC PLLs and ADCs, needs further investigation.

- This thesis has explored architectures of noise-canceling amplifiers and buffers with high input impedance. However, another potential application of the NC technique is in the design of active filters [156]. Active inductors have been employed in the design of active filters in [157–159]. The work presented in [160] canceled the noise of an active inductor employed at the input of an LNA to achieve low noise operation with a reduced area. Application of the noise-canceling technique in active filter design is a potential research area for the future.

- Output buffers are required in many applications either to drive low-resistive load or to connect to measuring instruments. Many a time, these output buffers are required to have 50 $\Omega$ output impedance and low noise performance. So, a noise-canceling output buffer that breaks the trade-off between output impedance and NF is a future research direction.

- Clock-speed and current consumption of today's high-performance processing units continues to rise, resulting in increased power supply noise (PSN). With supply voltages being reduced, even minor fluctuations in supply can deteriorate the signal quality. Consequently, preserving the signal and power integrity in a high-speed, low-power system has become a major challenge [161]. One of the representative metrics of signal quality degradation due to the power supply noise is power supply induced jitter (PSIJ) [162–164]. PSIJ is typically classified as a deterministic jitter, and in such cases, the amplifier typically acts as a CG topology. Noise-canceling technique may be useful in removing PSIJ in high-speed digital circuits such as PLL, analog-to-digital converter (ADC), serializer/deserializer (SerDes) and clock data recovery (CDR) circuits etc. Future research can be carried out in this direction.

भारतीय प्रौद्योगिकी संस्थान गुवाहाटी
Indian Institute of Technology Guwahati

# Bibliography


[1] "3GPP specifications," https://www.3gpp.org/specifications/specifications, accessed: 2021-03-15.

[2] F. Svelto, M. B. Vahidfar, and M. Brandolini, "Reconfigurable Si RF receiver front-ends for multistandard radios," in *2008 European Conference on Wireless Technology*, 2008, pp. 33–36.

[3] S. Lee, J. Bergervoet, K. S. Harish, D. Leenaerts, R. Roovers, R. van de Beek, and G. van der Weide, "A broadband receive chain in 65nm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, 2007, pp. 418–612.

[4] N. Poobuapheun, W. Chen, Z. Boos, and A. M. Niknejad, "An inductorless high dynamic range 0.3-2.6 GHz receiver CMOS front-end," in *2009 IEEE Radio Frequency Integrated Circuits Symposium*, 2009, pp. 387–390.

[5] M. Valla, G. Montagna, R. Castello, R. Tonietto, and I. Bietti, "A 72-mW CMOS 802.11a direct conversion front-end with 3.5-dB NF and 200-kHz 1/f noise corner," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 970–977, Apr. 2005.

[6] Y. Shim, C. Kim, J. Lee, and S. Lee, "Design of full band UWB common-gate LNA," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 10, pp. 721–723, 2007.

[7] H. Wu, R. Hu, and C. F. Jou, "Complementary UWB LNA design using asymmetrical inductive source degeneration," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 7, pp. 402–404, 2010.

[8] Y. Lin, C. Wang, G. Lee, and C. Chen, "High-performance wideband low-noise amplifier using enhanced $\pi$-match input network," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 3, pp. 200–202, 2014.

[9] B. Guo and X. Li, "A 1.6-9.7 GHz CMOS LNA linearized by post distortion technique," *IEEE Microw. Wireless Compon. Lett.*, vol. 23, no. 11, pp. 608–610, 2013.

[10] K. Chen, J. Lu, B. Chen, and S. Liu, "An ultra-wide-band 0.4-10-GHz LNA in 0.18-$\mu$m CMOS," *IEEE Trans. Circuits Syst. II*, vol. 54, no. 3, pp. 217–221, 2007.

[11] C.-F. Liao and S.-I. Liu, "A broadband noise-canceling CMOS LNA for 3.1-10.6-GHz UWB receivers," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 329–339, Feb. 2007.

[12] B. Razavi, *RF Microelectronics (2nd Edition) (Prentice Hall Communications Engineering and Emerging Technologies Series)*, 2nd ed. USA: Prentice Hall Press, 2011.

[13] F. Bruccoleri, E. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 275–282, Feb. 2004.

[14] S. Blaakmeer, E. Klumperink, D. Leenaerts, and B. Nauta, "Wideband balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1341–1350, Jun. 2008.

[15] W. Chen, G. Liu, B. Zdravko, and A. M. Niknejad, "A highly linear broadband CMOS LNA employing noise and distortion cancellation," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1164–1176, May 2008.

[16] K.-H. Chen and S.-I. Liu, "Inductorless wideband CMOS low-noise amplifiers using noise-canceling technique," *IEEE Trans. Circuits Syst. I*, vol. 59, no. 2, pp. 305–314, Feb. 2012.

[17] M. El-Nozahi, A. A. Helmy, E. Sanchez-Sinencio, and K. Entesari, "An inductor-less noise-cancelling broadband low noise amplifier with composite transistor pair in 90 nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 1111–1122, May 2011.

[18] B. Guo, J. Chen, L. Li, H. Jin, and G. Yang, "A wideband noise-canceling CMOS LNA with enhanced linearity by using complementary nmos and pmos configurations," *IEEE J. Solid-State Circuits*, vol. 52, no. 5, pp. 1331–1344, 2017.

[19] S. Kim and K. Kwon, "A 50-MHz-1-GHz 2.3-dB NF noise-cancelling balun-LNA employing a modified current-bleeding technique and balanced loads," *IEEE Trans. Circuits Syst. I*, vol. 66, no. 2, pp. 546–554, Feb. 2019.

[20] H. Yu, Y. Chen, C. C. Boon, P. Mak, and R. P. Martins, "A 0.096-mm$^2$ 1-20 GHz triple-path noise-canceling common-gate common-source LNA with dual complementary pMOS-nMOS configuration," *IEEE Trans. Microw. Theory Tech.*, vol. 68, no. 1, pp. 144–159, Jan. 2020.

[21] J. Han and K. Kwon, "RF receiver front-end employing IIP2-enhanced 25% duty-cycle quadrature passive mixer for advanced cellular applications," *IEEE Access*, vol. 8, pp. 8166–8177, 2020.

[22] X. Yi, G. Feng, Z. Liang, C. Wang, B. Liu, C. Li, K. Yang, C. C. Boon, and Q. Xue, "A 24/77 GHz dual-band receiver for automotive radar applications," *IEEE Access*, vol. 7, pp. 48 053–48 059, 2019.

[23] J. Kim, D. R. Utomo, A. Dissanayake, S. Han, and S. Lee, "The evolution of channelization receiver architecture: Principles and design challenges," *IEEE Access*, vol. 5, pp. 25 385–25 395, 2017.

[24] G. Feng, X. Yi, F. Meng, and C. C. Boon, "A W-Band switch-less Dicke receiver for millimeter-wave imaging in 65 nm CMOS," *IEEE Access*, vol. 6, pp. 39 233–39 240, 2018.

[25] J. Kim and J. Silva-Martinez, "Low-power, low-cost CMOS direct-conversion receiver front-end for multistandard applications," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2090–2103, Sep. 2013.

[26] X. Wang, J. Sturm, N. Yan, X. Tan, and H. Min, "0.6-3-GHz wideband receiver RF front-end with a feedforward noise and distortion cancellation resistive-feedback LNA," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 2, pp. 387–392, Feb. 2012.

[27] M. K. Hedayati, A. Abdipour, R. Sarraf Shirazi, M. J. Ammann, M. John, C. Cetintepe, and R. B. Staszewski, "Challenges in on-chip antenna design and integration with RF receiver front-end circuitry in nanoscale CMOS for 5G communication systems," *IEEE Access*, vol. 7, pp. 43 190–43 204, 2019.

[28] A. Parssinen, J. Jussila, J. Ryynanen, L. Sumanen, and K. A. I. Halonen, "A 2-GHz wide-band direct conversion receiver for WCDMA applications," *IEEE J. Solid-State Circuits*, vol. 34, no. 12, pp. 1893–1903, 1999.

[29] Y. Lien, E. A. M. Klumperink, B. Tenbroek, J. Strange, and B. Nauta, "High-linearity bottom-plate mixing technique with switch sharing for N-path filters/mixers," *IEEE J. Solid-State Circuits*, vol. 54, no. 2, pp. 323–335, Feb. 2019.

[30] Y. C. Lien, E. A. M. Klumperink, B. Tenbroek, J. Strange, and B. Nauta, "Enhanced-selectivity high-linearity low-noise mixer-first receiver with complex pole pair due to capacitive positive feedback," *IEEE J. Solid-State Circuits*, vol. PP, no. 99, pp. 1–13, 2018.

[31] D. Murphy, H. Darabi, A. Abidi, A. A. Hafez, A. Mirzaei, M. Mikhemar, and M. F. Chang, "A blocker-tolerant, noise-cancelling receiver suitable for wideband wireless applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2943–2963, Dec. 2012.

[32] J. Rogin, I. Kouchev, G. Brenna, D. Tschopp, and Qiuting Huang, "A 1.5-V 45-mW direct-conversion WCDMA receiver IC in 0.13-$\mu m$ CMOS," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2239–2248, 2003.

[33] S. B. T. Wang, A. M. Niknejad, and R. W. Brodersen, "Design of a sub-mW 960-MHz UWB CMOS LNA," *IEEE J. Solid-State Circuits*, vol. 41, no. 11, pp. 2449–2456, Nov. 2006.

[34] K. Allidina and M. N. El-Gamal, "A 1V CMOS LNA for low power ultra-wideband systems," in *2008 15th IEEE International Conference on Electronics, Circuits and Systems*, 2008, pp. 165–168.

[35] J. Lee, H. Park, H. Chang, and T. Yun, "3.4-mW common-gate and current-reused UWB LNA," in *2012 IEEE 12th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, 2012, pp. 33–36.

[36] J. Sun, S. Diao, G. Feng, and F. Lin, "A 0.5-2.5 GHz 910 $\mu$W complementary LNA employing positive-negative feedback," *Analog Integrated Circuits and Signal Processing*, vol. 80, no. 2, pp. 163–172, May 2014.

[37] Z. Li, Z. Wang, M. Zhang, L. Chen, C. Wu, and Z. Wang, "A 2.4 GHz ultra-low-power current-reuse CG-LNA with active $g_m$-boosting technique," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 5, pp. 348–350, May 2014.

[38] K. A. M. Parvizi and M. N. El-Gamal, "A sub-mW, ultra-low-voltage, wideband low-noise amplifier design technique," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 23, no. 6, pp. 1111–1122, Jun. 2015.

[39] M. Parvizi, K. Allidina, and M. N. El-Gamal, "Short channel output conductance enhancement through forward body biasing to realize a 0.5 V 250 $\mu$W 0.6-4.2 GHz current-reuse CMOS LNA," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 574–586, Mar. 2016.

[40] M. Parvizi, K. Allidina, and M. N. El-Gamal, "An ultra-low-power wideband inductorless CMOS LNA with tunable active shunt-feedback," *IEEE Trans. Microw. Theory Tech.*, vol. 64, no. 6, pp. 1843–1853, Jun. 2016.

[41] M. De Souza, A. Mariano, and T. Taris, "Reconfigurable inductorless wideband CMOS LNA for wireless communications," *IEEE Trans. Circuits Syst. I*, vol. 64, no. 3, pp. 675–685, Mar. 2017.

[42] W. Chen, S. Yang, and K. Cheng, "A 1.2 V 490 $\mu$W sub-GHz UWB CMOS LNA with current reuse negative feedback," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018, pp. 1–4.

[43] C. J. Jeong, W. Qu, Y. Sun, D. Y. Yoon, S. K. Han, and S. G. Lee, "A 1.5V, 140$\mu$A CMOS ultra-low power common-gate LNA," in *2011 IEEE Radio Frequency Integrated Circuits Symposium*, Jun. 2011, pp. 1–4.

[44] J. Hsieh and K. Lin, "A 0.6-V low-power variable-gain LNA in 0.18-$\mu$m CMOS technology," *IEEE Trans. Circuits Syst. II*, vol. 67, no. 1, pp. 23–26, 2020.

[45] Wei Zhuo, S. Embabi, J. P. de Gyvez, and E. Sanchez-Sinencio, "Using capacitive cross-coupling technique in RF low noise amplifiers and down-conversion mixer design," in *Proceedings of the 26th European Solid-State Circuits Conference*, Sep. 2000, pp. 77–80.

[46] D. J. Allstot, Xiaoyong Li, and S. Shekhar, "Design considerations for CMOS low-noise amplifiers," in *2004 IEE Radio Frequency Integrated Circuits (RFIC) Systems. Digest of Papers*, Jun. 2004, pp. 97–100.

[47] W. Zhuo, X. Li, S. Shekhar, S. H. K. Embabi, J. P. de Gyvez, D. J. Allstot, and E. Sanchez-Sinencio, "A capacitor cross-coupled common-gate low-noise amplifier," *IEEE Trans. Circuits Syst. II*, vol. 52, no. 12, pp. 875–879, Dec. 2005.

[48] Xiaoyong Li, S. Shekhar, and D. J. Allstot, "$G_m$-boosted common-gate LNA and differential colpitts VCO/QVCO in 0.18-$\mu m$ CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2609–2619, 2005.

[49] A. El Sayed, A. K. Mishra, A. H. Ahmed, A. H. M. Shirazi, S.-P. Woo, Y.-S. Choi, S. Mirabbasi, and S. Shekhar, "A Hilbert transform equalizer enabling 80 MHz RF self-interference cancellation for full-duplex receivers," *IEEE Trans. Circuits Syst. I*, vol. 66, no. 3, pp. 1153–1165, 2019.

[50] C. Lin, T. S. Kalkur, and M. Morin, "A 2.4GHz common-gate LNA using on-chip differential inductors in a 0.18$\mu m$ CMOS technology," in *2009 International Conference on Electrical, Communications, and Computers*, 2009, pp. 183–188.

[51] J. Zaini, F. Hameau, T. Taris, D. Morche, P. Audebert, and E. Mercier, "A tunable ultra low power inductorless low noise amplifier exploiting body biasing of 28 nm FDSOI technology," in *2017 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, Jul. 2017, pp. 1–6.

[52] H. Liu and Z. Zhang, "An ultra-low power CMOS LNA for WPAN applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 2, pp. 174–176, Feb. 2017.

[53] I. Ramez Chamas and S. Raman, "Analysis, design, and X-band implementation of a self-biased active feedback $g_m$-boosted common-gate CMOS LNA," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 3, pp. 542–551, 2009.

[54] T. Taris, J. Desevedavy, F. Hameau, P. Audebert, and D. Morche, "Inductorless multi-mode RF-CMOS low noise amplifier dedicated to ultra low power applications," *IEEE Access*, vol. 9, pp. 83 431–83 440, 2021.

[55] W. Wu, O. Novak, C. T. Charles, and X. Fan, "A low-power 3.1-5GHz ultra-wideband low noise amplifier utilizing Miller effect," in *2009 IEEE International Conference on Ultra-Wideband*, 2009, pp. 255–259.

[56] J. Liu, H. Liao, and R. Huang, "0.5 V ultra-low power wideband LNA with forward body bias technique," *Electronics Letters*, vol. 45, pp. 289–290(1), Mar. 2009.

[57] A. Zafarian, I. Kalali Fard, A. Golmakani, and J. Shirazi, "A 0.4V 790$\mu$W CMOS low noise amplifier in sub-threshold region at 1.5GHz," in *2013 8th IEEE Design and Test Symposium*, 2013, pp. 1–6.

[58] J.-F. Chang and Y.-S. Lin, "3-9-GHz CMOS LNA using body floating and self-bias technique for sub-6-GHz 5G communications," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 6, pp. 608–611, 2021.

[59] B. Lu, Y. Wang, Y. Wu, C. Chiong, and H. Wang, "A submilliwatt K-band low-noise amplifier for next generation radio astronomical receivers in 65-nm CMOS process," *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 7, pp. 669–672, 2020.

[60] Chang and Chia-Hung, "A forward-body-bias CMOS LNA with ultra-low device junction leakage using intrinsic self-balanced pseudo resistor," *IEEE Trans. Circuits Syst. II*, vol. 66, no. 4, pp. 697–701, 2019.

[61] T. Soorapanth and T. H. Lee, "RF linearity of short-channel MOSFETs," in *In Proceedings of First International Workshop on Design of Mixed-Mode Integrated Circuits and Applications, pages 81 84*, 1997, pp. 81–84.

[62] Z. Pan, C. Qin, Z. Ye, Y. Wang, and Z. Yu, "Wideband inductorless low-power LNAs with $G_m$ enhancement and noise-cancellation," *IEEE Trans. Circuits Syst. I*, vol. 65, no. 1, pp. 26–38, Jan. 2018.

[63] Z. Li, L. Sun, and L. Huang, "0.4 mW wideband LNA with double $g_m$ enhancement and feed-forward noise cancellation," *Electronics Letters*, vol. 50, no. 5, pp. 400–401, Feb. 2014.

[64] A. R. A. Kumar, B. D. Sahoo, and A. Dutta, "A wideband 2 to 5 GHz noise canceling subthreshold low noise amplifier," *IEEE Trans. Circuits Syst. II*, vol. 65, no. 7, pp. 834–838, Jul. 2018.

[65] M. Parvizi, K. Allidina, F. Nabki, and M. El-Gamal, "A 0.4V ultra low-power UWB CMOS LNA employing noise cancellation," in *2013 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2013, pp. 2369–2372.

[66] J. Kim and J. Silva-Martinez, "Wideband inductorless balun-LNA employing feedback for low-power low-voltage applications," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 9, pp. 2833–2842, 2012.

[67] H. Wang, L. Zhang, and Z. Yu, "A wideband inductorless LNA with local feedback and noise cancelling for low-power low-voltage applications," *IEEE Trans. Circuits Syst. I*, vol. 57, no. 8, pp. 1993–2005, Aug. 2010.

[68] G. Guitton, M. de Souza, A. Mariano, and T. Taris, "Design methodology based on the inversion coefficient and its application to inductorless LNA implementations," *IEEE Trans. Circuits Syst. I*, vol. 66, no. 10, pp. 3653–3663, Oct. 2019.

[69] C. Chang and M. Onabajo, "Analysis and demonstration of an IIP3 improvement technique for low-power RF low-noise amplifiers," *IEEE Trans. Circuits Syst. I*, vol. 65, no. 3, pp. 859–869, 2018.

[70] F. Belmas, F. Hameau, and J. Fournier, "A low power inductorless LNA with double $\mathrm{g_m}$ enhancement in 130 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 5, pp. 1094–1103, May 2012.

[71] S. Tiwari and J. Mukherjee, "An inductorless wideband gm-boosted balun LNA with nMOS-pMOS configuration and capacitively coupled loads for sub-GHz IoT applications," *IEEE Trans. Circuits Syst. II*, pp. 1–1, 2021.

[72] S. Kim and K. Kwon, "Broadband balun-LNA employing local feedback gm-boosting technique and balanced loads for low-power low-voltage applications," *IEEE Trans. Circuits Syst. I*, vol. 67, no. 12, pp. 4631–4640, 2020.

[73] A. Bozorg and R. B. Staszewski, "A 0.02-4.5-GHz LN(T)A in 28-nm CMOS for 5G exploiting noise reduction and current reuse," *IEEE J. Solid-State Circuits*, vol. 56, no. 2, pp. 404–415, 2021.

[74] Z. Liu, C. C. Boon, X. Yu, C. Li, K. Yang, and Y. Liang, "A 0.061-mm$^2$ 1-11-GHz noise-canceling low-noise amplifier employing active feedforward with simultaneous current and noise reduction," *IEEE Trans. Microw. Theory Tech.*, vol. 69, no. 6, pp. 3093–3106, 2021.

[75] H. Yu, Y. Chen, C. C. Boon, C. Li, P. Mak, and R. P. Martins, "A 0.044-mm$^2$ 0.5-to-7-GHz resistor-plus-source-follower-feedback noise-cancelling LNA achieving a flat NF of 3.3$\pm$0.45 dB," *IEEE Trans. Circuits Syst. II*, vol. 66, no. 1, pp. 71–75, 2019.

[76] M. Rahman and R. Harjani, "A sub-1-V 194-$\mu$W 31-dB FOM 2.3 $-$ 2.5-GHz mixer-first receiver frontend for WBAN with mutual noise cancellation," *IEEE Trans. Microw. Theory Tech.*, vol. 64, no. 4, pp. 1102–1109, Apr. 2016.

[77] J. Jussila and P. Sivonen, "A 1.2-V highly linear balanced noise-cancelling LNA in 0.13-$\mu$m CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 3, pp. 579–587, Mar. 2008.

[78] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed. Cambridge University Press, 2003.

[79] Keng Leong Fong, "High-frequency analysis of linearity improvement technique of common-emitter transconductance stage using a low-frequency-trap network," *IEEE J. Solid-State Circuits*, vol. 35, no. 8, pp. 1249–1252, 2000.

[80] J. S. Fairbanks and L. E. Larson, "Analysis of optimized input and output harmonic termination on the linearity of 5 GHz CMOS radio frequency amplifiers," in *Radio and Wireless Conference, 2003. RAWCON '03. Proceedings*, 2003, pp. 293–296.

[81] V. Aparin and L. E. Larson, "Linearization of monolithic LNAs using low-frequency low-impedance input termination," in *ESSCIRC 2004 - 29th European Solid-State Circuits Conference (IEEE Cat. No.03EX705)*, 2003, pp. 137–140.

[82] B. Toole, C. Plett, and M. Cloutier, "RF circuit implications of moderate inversion enhanced linear region in MOSFETs," *IEEE Trans. Circuits Syst. I*, vol. 51, no. 2, pp. 319–328, 2004.

[83] V. Aparin, G. Brown, and L. E. Larson, "Linearization of CMOS LNA's via optimum gate biasing," in *IEEE Int. Symp. Circuits Syst.*, vol. 4, May 2004, pp. 748–751.

[84] Yongwang Ding and R. Harjani, "A +18 dBm IIP3 LNA in 0.35 $\mu m$ CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, 2001, pp. 162–163.

[85] Tae Wook Kim, Bonkee Kim, and Kywro Lee, "Highly linear RF CMOS amplifier and mixer adopting MOSFET transconductance linearization by multiple gated transistors," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, 2003*, 2003, pp. 107–110.

[86] D. Im, I. Nam, H.-T. Kim, and K. Lee, "A wideband CMOS low noise amplifier employing noise and IM2 distortion cancellation for a digital TV tuner," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 686–698, Mar. 2009.

[87] B. Guo, J. Gong, and Y. Wang, "A wideband differential linear low-noise transconductance amplifier with active-combiner feedback in complementary MGTR configurations," *IEEE Trans. Circuits Syst. I*, vol. 68, no. 1, pp. 224–237, 2021.

[88] D. Kim, S. Jang, J. Lee, and D. Im, "A broadband PVT-insensitive all-nMOS noise-canceling balun-LNA for subgigahertz wireless communication applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 2, pp. 165–168, 2021.

[89] Y.-H. Yu, Y.-S. Yang, and Y.-J. Chen, "A compact wideband CMOS low noise amplifier with gain flatness enhancement," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 502–509, Mar. 2010.

[90] D. Im and I. Nam, "A wideband digital TV receiver front-end with noise and distortion cancellation," *IEEE Trans. Circuits Syst. I*, vol. 61, no. 2, pp. 562–572, Feb. 2014.

[91] E. Klumperink and B. Nauta, "Software defined radio receivers exploiting noise cancelling: A tutorial review," *Communications Magazine, IEEE*, vol. 52, no. 10, pp. 111–117, Oct. 2014.

[92] A. Amer, E. Hegazi, and H. F. Ragaie, "A 90-nm wideband merged CMOS LNA and mixer exploiting noise cancellation," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 323–328, Feb. 2007.

[93] Y.-H. Chien, K.-L. Fu, and S.-I. Liu, "A 3-25 Gb/s four-channel receiver with noise-canceling TIA and power-scalable LA," *IEEE Trans. Circuits Syst. II*, vol. 61, no. 11, pp. 845–849, Nov. 2014.

[94] D. Murphy, A. Hafez, A. Mirzaei, M. Mikhemar, H. Darabi, M. Chang, and A. Abidi, "A blocker-tolerant wideband noise-cancelling receiver with a 2 dB noise figure," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, Feb. 2012, pp. 74–76.

[95] D. Murphy, A. Mirzaei, H. Darabi, M. F. Chang, and A. Abidi, "An LTV analysis of the frequency translational noise-cancelling receiver," *IEEE Trans. Circuits Syst. I*, vol. 61, no. 1, pp. 266–279, Jan. 2014.

[96] H. Wu, M. Mikhemar, D. Murphy, H. Darabi, and M.-C. Chang, "A highly linear inductorless wideband receiver with phase and thermal-noise cancellation," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, Feb. 2015, pp. 1–3.

[97] D. Murphy, H. Darabi, and H. Xu, "A noise-cancelling receiver resilient to large harmonic blockers," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1336–1350, Jun. 2015.

[98] C. Andrews and A. C. Molnar, "Implications of passive mixer transparency for impedance matching and noise figure in passive mixer-first receivers," *IEEE Trans. Circuits Syst. I*, vol. 57, no. 12, pp. 3092–3103, Dec. 2010.

[99] E. A. M. Klumperink, H. J. Westerveld, and B. Nauta, "N-path filters and mixer-first receivers: A review," in *2017 IEEE Custom Integrated Circuits Conference (CICC)*, 2017, pp. 1–8.

[100] S. Krishnamurthy and A. M. Niknejad, "Design and analysis of enhanced mixer-first receivers achieving 40-dB/decade RF selectivity," *IEEE J. Solid-State Circuits*, pp. 1–12, 2019.

[101] C. Wu, Y. Wang, B. Nikolic, and C. Hull, "An interference-resilient wideband mixer-first receiver with LO leakage suppression and I/Q correlated orthogonal calibration," *IEEE Trans. Microw. Theory Tech.*, vol. 64, no. 4, pp. 1088–1101, Apr. 2016.

[102] G. Qi, P. Mak, and R. P. Martins, "A 0.038-$mm^2$ SAW-Less multiband transceiver using an N-path SC gain loop," *IEEE J. Solid-State Circuits*, vol. 52, no. 8, pp. 2055–2070, Aug. 2017.

[103] C. Wilson and B. A. Floyd, "Harmonic performance of mixer-first receivers with circulant-symmetric basebands," *IEEE Trans. Circuits Syst. I*, vol. 66, no. 1, pp. 161–174, Jan. 2019.

[104] D. Yang, C. Andrews, and A. Molnar, "Optimized design of N-phase passive mixer-first receivers in wideband operation," *IEEE Trans. Circuits Syst. I*, vol. 62, no. 11, pp. 2759–2770, Nov. 2015.

[105] M. K. Lenka and G. Banerjee, "A wideband blocker-tolerant receiver with frequency-translational resistive feedback," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 27, no. 5, pp. 993–1006, May 2019.

[106] S. Hameed and S. Pamarti, "A time-interleaved filtering-by-aliasing receiver front-end with $>$ 70 dB suppression at $<$ 4$\times$bandwidth frequency offset," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, Feb. 2017, pp. 418–419.

[107] A. Nejdel, M. Abdulaziz, M. Törmänen, and H. Sjöland, "A positive feedback passive mixer-first receiver front-end," in *2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, May 2015, pp. 79–82.

[108] G. Pini, D. Manstretta, and R. Castello, "A 260-MHz RF bandwidth mixer-first receiver with third-order current-mode filtering TIA," *IEEE Solid-State Circuits Letters*, vol. 2, no. 9, pp. 183–186, Sep. 2019.

[109] A. Nejdel, H. Sjöland, and M. Törmänen, "A noise-cancelling receiver front-end with frequency selective input matching," *IEEE J. Solid-State Circuits*, vol. 50, no. 5, pp. 1137–1147, May 2015.

[110] I. Choi and B. Kim, "A passive mixer-first receiver front-end without external components for mobile TV applications," in *2013 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Jun. 2013, pp. 145–148.

[111] D. H. Mahrof, E. A. M. Klumperink, Z. Ru, M. S. Oude Alink, and B. Nauta, "Cancellation of OpAmp virtual ground imperfections by a negative conductance applied to improve RF receiver linearity," *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1112–1124, May 2014.

[112] V. K. Purushothaman, E. A. M. Klumperink, B. T. Clavera, and B. Nauta, "A fully passive RF front end with 13-dB gain exploiting implicit capacitive stacking in a bottom-plate N-path filter/mixer," *IEEE J. Solid-State Circuits*, pp. 1–12, 2019.

[113] Y. Xu and P. R. Kinget, "A chopping switched-capacitor RF receiver with integrated blocker detection," *IEEE J. Solid-State Circuits*, vol. 53, no. 6, pp. 1607–1617, Jun. 2018.

[114] C. Andrews, L. Diamente, D. Yang, B. Johnson, and A. Molnar, "A wideband receiver with resonant multi-phase LO and current reuse harmonic rejection baseband," *IEEE J. Solid-State Circuits*, vol. 48, no. 5, pp. 1188–1198, May 2013.

[115] F. Lin, P. Mak, and R. P. Martins, "An RF-to-BB-current-reuse wideband receiver with parallel N-path active/passive mixers and a single-MOS pole-zero LPF," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2547–2559, Nov. 2014.

[116] S. Lee, I. Choi, H. Kim, and B. Kim, "A sub-mW fully integrated wide-band receiver for wireless sensor network," *IEEE Microw. Wireless Compon. Lett.*, vol. 25, no. 5, pp. 319–321, May 2015.

[117] J. Im, H. Kim, and D. D. Wentzloff, "A 220- $\mu$W 83-dBm 5.8-GHz third-harmonic passive mixer-first LP-WUR for IEEE 802.11ba," *IEEE Trans. Microw. Theory Tech.*, vol. 67, no. 7, pp. 2537–2545, Jul. 2019.

[118] E. Babakrpur and W. Namgoong, "Matching for concurrent harmonic sensing in an $M$-phase mixer-first receiver," *IEEE Trans. Circuits Syst. II*, vol. 64, no. 9, pp. 1017–1021, Sep. 2017.

[119] T. Tikka, K. Stadius, J. Ryynänen, and M. Kaltiokallio, "A 0.83 GHz mixer-first receiver with on-chip transformer balun in 65-nm CMOS," in *ESSCIRC Conference 2015 - 41st European Solid-State Circuits Conference (ESSCIRC)*, 2015, pp. 295–298.

[120] C. Wilson, J. Dean, and B. A. Floyd, "Mixer-first MIMO receiver with multi-port impedance tuning for decoupling of compact antenna systems," in *2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2018, pp. 112–115.

[121] Z. Lin, P. Mak, and R. P. Martins, "A 0.028 mm$^2$ 11mW single-mixing blocker-tolerant receiver with double-RF N-path filtering, $S_{11}$ centering, +13dBm OB-IIP3 and 1.5-to-2.9dB NF," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, 2015, pp. 1–3.

[122] Z. Liu, F. Yang, H. Jiang, X. Hao, J. Liu, and H. Liao, "An 89 $\mu$W MICS/ISM band receiver for ultra-low-power applications," in *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2017, pp. 1–4.

[123] O. Elsayed, M. Abouzied, and E. Snchez-Sinencio, "A 540 $\mu$W RF wireless receiver assisted by RF blocker energy harvesting for IoT applications with +18 dBm OB-IIP3," in *2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2016, pp. 230–233.

[124] A. Hasan and M. Helaoui, "Analysis, calibration, and performance evaluation of a generalized N-phase quadrature phase shift frequency selective receiver," *IEEE Trans. Microw. Theory Tech.*, vol. 67, no. 1, pp. 365–382, 2019.

[125] C. McNeilage, E. Ivanov, P. Stockwell, and J. Searls, "Review of feedback and feedforward noise reduction techniques," in *Proc. IEEE International Frequency Control Symp.*, May 1998, pp. 146–155.

[126] Paul R. Gray, Paul J. Hurst, Stephen H. Lewis and Robert G. Meyer, *Analysis and Design of Analog Integrated Circuits*. 605 Third Avenue, New York: John Wiley & Sons, Inc., 2001, ch. 11.

[127] I. Das and N. Nallam, "Noise cancelation? explained!: The role of feedback in noise-canceling LNAs and receivers," *IEEE Microwave Magazine*, vol. 18, no. 6, pp. 100–109, Sep. 2017.

[128] Z. Deng, J. Zhou, H. J. Qian, and X. Luo, "A 22.9-38.2-GHz dual-path noise-canceling LNA with 2.65-4.62-dB NF in 28-nm CMOS," *IEEE J. Solid-State Circuits*, pp. 1–1, 2021.

[129] Z. Deng, J. Zhou, H. J. Qian, and X. Luo, "High resolution reconfigurable phase-tuning line using self-shielded 3-D interdigital capacitor," *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 6, pp. 605–608, 2020.

[130] E. A. M. Klumperink, F. Bruccoleri, and B. Nauta, "Finding all elementary circuits exploiting transconductance," *IEEE Trans. Circuits Syst. II*, vol. 48, no. 11, pp. 1039–1053, Nov. 2001.

[131] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, "Generating all two-MOS-transistor amplifiers leads to new wide-band LNAs," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1032–1040, Jul. 2001.

[132] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 1st ed. McGraw-Hill, 2001.

[133] A. Madan, M. J. McPartlin, C. Masse, W. Vaillancourt, and J. D. Cressler, "A 5 GHz 0.95 dB NF highly linear cascode floating-body LNA in 180 nm SOI CMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 22, 2012.

[134] X. Fan, H. Zhang, and E. Sanchez-Sinencio, "A noise reduction and linearity improvement technique for a differential cascode LNA," *IEEE J. Solid-State Circuits*, vol. 43, no. 3, pp. 588–599, Mar. 2008.

[135] "A sub-2 dB NF dual-band CMOS LNA for CDMA/WCDMA applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, 2008.

[136] V. Vanukuru, A. Dutta, B. Swaminathan, S. Choppalli, R. Wolf, M. Jaffe, Y. Tan, R. Logan, J. E. Monaghan, and A. Joseph, "A 6.25 mW, +21 dBm OIP3, 0.85 dB NF, 2.5 GHz LNA employing high self gain device in $0.13\mu$m SOI technology," in *2020 IEEE 20th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, 2020.

[137] Z. Pan, C. Qin, Z. Ye, and Y. Wang, "A low power inductorless wideband LNA with $G_m$ enhancement and noise cancellation," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 1, pp. 58–60, Jan. 2017.

[138] E. A. Sobhy, A. A. Helmy, S. Hoyos, K. Entesari, and E. Sanchez-Sinencio, "A 2.8-mW sub-2-dB noise-figure inductorless wideband CMOS LNA employing multiple feedback," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 12, pp. 3154–3161, Dec. 2011.

[139] J. Borremans, P. Wambacq, C. Soens, Y. Rolain, and M. Kuijk, "Low-area active-feedback low-noise amplifier design in scaled digital CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 11, pp. 2422–2433, Nov. 2008.

[140] E. A. Ghany, "Linearity and noise improvement techniques employing low power in analog and RF circuits and systems," Ph.D. dissertation, Texas A&M University, 12 2012, https://hdl.handle.net/1969.1/148201.

[141] H. Zhang and E. Sanchez-Sinencio, "Linearization techniques for CMOS low noise amplifiers: A tutorial," *IEEE Trans. Circuits Syst. I*, vol. 58, no. 1, pp. 22–36, Jan. 2011.

[142] P. Wambacq and W. M. Sansen, *Distortion Analysis of Analog Integrated Circuits*. USA: Kluwer Academic Publishers, 1998.

[143] W. Sansen, "Distortion in elementary transistor circuits," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 3, pp. 315–325, Mar. 1999.

[144] I. Vassiliou, K. Vavelidis, T. Georgantas, S. Plevridis, N. Haralabidis, G. Kamoulakos, C. Kapnistis, S. Kavadias, Y. Kokolakis, P. Merakos, J. C. Rudell, A. Yamanaka, S. Bouras, and I. Bouras, "A single-chip digitally calibrated 5.15-5.825-GHz 0.18-$\mu m$ CMOS transceiver for 802.11a wireless LAN," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2221–2231, 2003.

[145] Trung-Kien Nguyen, Nam-Jin Oh, Viet-Hoang Le, and Sang-Gug Lee, "A low-power CMOS direct conversion receiver with 3-dB NF and 30-kHz flicker-noise corner for 915-MHz band IEEE 802.15.4 ZigBee standard," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 2, pp. 735–741, 2006.

[146] P. K. Sharma and N. Nallam, "Linearity and NF tradeoff in input-matched N-path mixer-first receivers with shunt-feedback TIAs," in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2019, pp. 1–4.

[147] P. K. Sharma and N. Nallam, "Breaking the performance tradeoffs in N-path mixer-first receivers using a second-order baseband noise-canceling TIA," *IEEE J. Solid-State Circuits*, vol. 55, no. 11, pp. 3009–3023, 2020.

[148] I. Das and N. Nallam, "Systematic generation of flicker and thermal noise canceling circuits," in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2019, pp. 1–4.

[149] I. Das and N. Nallam, "A four-phase passive mixer-first receiver with a low-power complementary common-gate TIA," *IEEE Access*, vol. 8, pp. 216 580–216 592, 2020.

[150] B. J. Thijssen, E. A. M. Klumperink, P. Quinlan, and B. Nauta, "30.4 A 370$\mu$W 5.5dB-NF BLE/BT5.0/IEEE 802.15.4-compliant receiver with $>$ 63dB adjacent channel rejection at $>$ 2 channels offset in 22nm FDSOI," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, 2020, pp. 466–468.

[151] A. Elshazly, R. Inti, W. Yin, B. Young, and P. K. Hanumolu, "A 0.4-to-3GHz digital PLL with supply-noise cancellation using deterministic background calibration," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, 2011, pp. 92–94.

[152] H. Yan, P. Qin, and D. Chen, "A new phase noise cancelling technique for fractional-N PLL," in *2014 12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, 2014, pp. 1–3.

[153] G. Urakawa, H. Kobayashi, J. Deguchi, and R. Fujimoto, "A noise-canceling charge pump for area efficient PLL design," in *2020 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, 2020, pp. 31–33.

[154] B. D. Sahoo and A. Inamdar, "Thermal-noise-canceling switched-capacitor circuit," *IEEE Trans. Circuits Syst. II*, vol. 63, no. 7, pp. 628–632, 2016.

[155] C. Ravi, D. James, V. Sarma, B. Datta Sahoo, and A. Inamdar, "Thermal noise canceling pipelined ADC," in *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2017, pp. 1–4.

[156] W. Sansen, "1.3 Analog CMOS from 5 micrometer to 5 nanometer," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, 2015, pp. 1–6.

[157] Z. Gao, J. Ma, M. Yu, and Y. Ye, "A fully integrated CMOS active bandpass filter for multiband RF front-ends," *IEEE Trans. Circuits Syst. II*, vol. 55, no. 8, pp. 718–722, 2008.

[158] R. Bhattacharya, A. Basu, and S. K. Koul, "A highly linear CMOS active inductor and its application in filters and power dividers," *IEEE Microw. Wireless Compon. Lett.*, vol. 25, no. 11, pp. 715–717, 2015.

[159] L. Pantoli, V. Stornelli, and G. Leuzzi, "Design considerations and effects of class-AB polarization in active filters realized by means of active inductors," in *2017 47th European Microwave Conference (EuMC)*, 2017, pp. 37–40.

[160] M. Moezzi and M. Sharif Bakhtiar, "Wideband LNA using active inductor with multiple feed-forward noise reduction paths," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 4, pp. 1069–1078, 2012.

[161] M. Swaminathan and A. Engin, *Power Integrity Modeling and Design for Semiconductors and Systems*, 1st ed. USA: Prentice Hall Press, 2007.

[162] J. N. Tripathi, V. K. Sharma, and H. Shrimali, "A review on power supply induced jitter," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 9, no. 3, pp. 511–524, 2019.

[163] H. Kim, J. Fan, and C. Hwang, "Modeling of power supply induced jitter (PSIJ) transfer function at inverter chains," in *2017 IEEE International Symposium on Electromagnetic Compatibility Signal/Power Integrity (EMCSI)*, 2017, pp. 591–596.

[164] J. N. Tripathi, A. Jain, M. Marinkovic, and R. Achar, "Analysis of PSIJ in the presence of both ground-bounce and transmission media," in *2018 IEEE 22nd Workshop on Signal and Power Integrity (SPI)*, 2018, pp. 1–3.

# List of Publications

## Journals

- I. Das and N. Nallam, "Noise cancelation? explained!: The role of feedback in noise-canceling LNAs and receivers," IEEE Microwave Magazine, vol. 18, no. 6, pp. 100-109, 2017.
- I. Das and N. Nallam, "A four-phase passive mixer-first receiver with a low-power complementary common-gate TIA," IEEE Access, vol. 8, pp. 216 580-216 592, 2020.

## Conference

- I. Das and N. Nallam, "Systematic generation of flicker and thermal noise canceling circuits," in 2019 IEEE International Symposium on Circuits and Systems (ISCAS), 2019, pp. 14.