INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI
SHORT ABSTRACT OF THESIS

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Thesis Title: Analysis, Design and Modeling of Approximate Adders for Error-resilient Applications

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SHORT ABSTRACT

Over the decades, Complementary Metal-Oxide-Semiconductor (CMOS) technology scaling has been the fundamental driver for computing. However, we are now in a phase where CMOS technology scaling is becoming less effective in improving the system capability. The consequence is that we must either accept that the computing systems are good enough or look for alternate avenues to advance them without significant technology progress. Recent studies show that there are several promising alternate avenues that jointly can improve the system capability equivalent to 2 − 3 decades of Moore's law. Approximate computing is one of them and has attracted a lot of attention of researchers. It should be noted that the concept of approximate computing trade-offs computation quality for computation efforts.

In recent years, several approximate adders have been proposed in the literature. The key design approach behind these approximate adders is to truncate the carry-chain. The two most commonly used approaches to truncate the carry-chain are: (i) Approximate Full Adder (AFA); and (ii) Equal Segment Adder (ESA). In the first approach, an N-bit adder is segmented into two sub-adders: (i) Accurate sub-adder that includes the higher order k bits; and (ii) Approximate sub-adder that includes the remaining lower order (N − k) bits. For accurate sub-adder, Full Adders (FAs) are used, whereas for approximate sub-adder, AFAs are used. In the second approach, an N-bit adder is segmented into several smaller disjoint or overlapping equally sized accurate sub-adders. The Carry-in (Cin) of all sub-adders is considered as 0. Consequently, all sub-adders become independent and operate in parallel. This thesis is divided into three parts in which analysis, designing, analytical modeling, optimization and applications of AFAs and ESAs are presented.

In the first part, four AFAs are proposed with design objective that Carry-out (Cout) should be independent of Cin with minimal error probability. Using the proposed AFAs, an N-bit approximate adder is designed which we call as "ApproxADD". In order to improve the Error Distance (ED) and Error Rate (ER) of ApproxADD, the concept of carry-lifetime and Error Detection and Correction (EDC) logic, respectively, is used. In this way, two more versions of ApproxADD are introduced. Further, analytical models are provided to estimate the accuracy, delay, power and area of ApproxADDs. The efficiency of ApproxADDs is evaluated by comparing them with existing approximate adders. Finally, the effectiveness of the proposed approach in real-life applications is examined via an image processing application.

In the second part, analytical models are proposed to estimate the accuracy, delay, power and area of ESAs. It should be noted that the proposed analytical models are generalized and superior (or at par) to the existing analytical models. From the proposed analytical models, it is observed that in an N-bit ESA, there exist multiple configurations which exhibit similar

accuracy, however, these configurations exhibit different delay, power and area. Therefore, for a given accuracy, the configurations which provide minimal delay, power and/or area need to be known apriori for efficient, intelligent and goal oriented implementations of ESAs. In this regard, an optimization framework is presented that exploits the proposed analytical models and reveals the optimal configurations. Further, from the proposed analytical models, it is observed that there is a scope and need of improvement in accuracy-effort curves of ESAs. For improving the accuracy-effort curves, modifications are proposed with design objective that the modified ESAs provide higher accuracy without imposing any additional delay, power and area overheads w.r.t. the original ESAs.

In the third part, the applicability of approximate adders in cryptography applications, yield enhancement and designing other approximate arithmetic operations is examined. First, an approximate Secure Hash Algorithm (SHA-1) is designed using ApproxADDs and evaluated over cryptographic hash functions. Further, analytical models are proposed to estimate the yield of approximate circuits. From the proposed analytical models, it is observed that approximate circuits can improve the functional and parametric yields due to decrease in area and delay, respectively. This is demonstrated with ApproxADDs. Further, in order to examine the effectiveness of approximate adders for designing other approximate arithmetic operations, an approximate Multiply-and-Accumulate (MAC) unit is designed using approximate adders. The effectiveness of approximate MAC unit is examined via an image processing application.