INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI
SHORT ABSTRACT OF THESIS

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Thesis Title: VLSI Testing of System on Chip : Incomplete Testing

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Key words for description of Thesis Work	:	System on Chip (SoC), stuck-at faults, incomplete testing, test power (TP), test application time (TAT), test data volume (TDV), test access mechanism (TAM), JTAG architecture, heuristic-based testing, approximate computing, Boolean satisfiability, bridging faults.

SHORT ABSTRACT

A System on Chip (SoC) integrates an entire electronic system, including components like memory (RAM and Flash), a GPU, I/O interfaces, an APU, security modules, and more, onto a single chip. Despite its compact design, SoCs can exhibit various faults, such as stuck-at, transition, and path delay faults, which can impair device performance. Testing SoCs is essential but challenging due to complex interconnections, limited internal access, temperature fluctuations during testing, and the need for synchronization between hardware and software. Additionally, test factors like test power (TP), test application time (TAT), test data volume (TDV), and costs further complicate the process. For deeply embedded cores, a test access mechanism (TAM) and JTAG architecture are typically used to evaluate and test the system effectively.

However, with the growing complexity of SoCs, traditional testing methods, though comprehensive, may become too slow or impractical. To address this, the thesis introduces heuristic-based incomplete testing approaches for large-scale SoCs. The work is divided into eight phases, covering literature reviews, incomplete testing methods for stuck-at faults (focusing on reducing TDV), optimization of TAT and TP, the application of approximate computing, and Boolean satisfiability-based methods for bridging faults. These approaches offer more scalable solutions for testing large SoCs, and the proposed methods are supported by experimental results and published works.