Short Abstract

This dissertation pursues efficient self-test approaches for manufacturing faults including a little emphasis on the transient faults and other logic level faults, e.g., packet deadlock, in the NoC channels in order to improve the yield and reliability in NoC-based communication systems. The main goal of this dissertation is to develop an environment for the test-time minimization problem in addition to associated issues, such as test area overhead, performance overhead at the runtime, etc. In order to reduce the test cost in terms of low test time, low area overhead, low-performance overhead, etc., the proposed test approach is divided into two parts: test algorithm and test scheduling. As the first pillar towards the goal, an on-line, distributed built-in-self-test (BIST) oriented test algorithm is proposed, that with the help of a test module (must be included in a modern NoC) has the capability in detecting a channel fault and identifying the faulty wires from the channel. As the second pillar to reach the goal, a suitable test scheduling scheme is proposed, which makes the present test solution scalable with respect to different network architectural characteristics: network size, channel width, and network type, i.e., large-scale NoC architectures in general. This dissertation contains five contributed works. First three contributions explore the test of stuck-at, open, and short faults in NoC channels. Here, the channels are assumed to follow the single fault model. The fourth contribution includes the test of manufacturing and transient faults in the channels. The final contribution includes the test of coexistent manufacturing channel-faults. In the last two contributions, a channel can be assumed to follow the multiple fault model. In all the contributions, experimental results reveal that the proposed solutions impose less test time, area, and performance overhead as compared to existing testing techniques.

Abstract

Today manycore, multiprocessor systems-on-chip (MPSoCs) have been introduced to cope with the growing demand for high-speed communication requirements of intensive-computing applications. However, in spite of rapid advancements in deep-submicron (DSM) technology and the seamless integration of intellectual property (IP) modules in the SoCs, these bus-based interconnection architectures have become unable to meet the performance requirements – bandwidth, throughput, latency, power, etc. in the applications where high-performance computation and communication is the dominant consideration. In other words, such SoCs often fail to sustain high-volume computation and high-speed communication among their components due to the use of global buses as the interconnects. The network-on-chip (NoC) as an alternate prevalent interconnection infrastructure has been continuously occupying the space of the SoC. An NoC comprises a large number of IP cores, routers, and high-speed channels (interconnects) that construct a structure (topology) spanning across the chip. However, aggressive CMOS scaling expedites interconnect and transistor wear-out, shortening the lifespan of these basic components which are often vulnerable to a number of manufacturing and transient faults due to aging, physical defects, or hostile attacks invoked by malicious third parties. For instance, basic classical logic level faults treated as the manufacturing faults, such as stuck-at, open, and shorts in NoC channels cause various system-level failures and subsequent degradation of reliability, yield, and performance of the computing platform. One approach to tackle channel-faults in NoCs is to replace the faulty channel-wires with spare wires. Such scheme is not cost-effective as the area overhead is substantially increased. Another approach is to exercise a fault-tolerant routing algorithm that directs traffic (application data packets) over channels by avoiding the faulty wires or an alternative fault-free path in order to connect the source and destination nodes, keeping the NoC functional. However, most of the fault-tolerant schemes do not consider any test mechanism for channels. One prerequisite of these approaches includes the knowledge about the health status of the channels which can only be inferred by an effective test method. Most of the commonly practiced approaches acknowledge numerous disadvantages in terms of test issues like high test volume, high silicon area overhead, high test time, low fault coverage, and lack of scalability.

This dissertation pursues efficient self-test approaches for manufacturing faults including a little emphasis on the transient faults and other logic level faults, e.g., packet deadlock, in the NoC channels in order to improve the yield and reliability in NoC-based communication systems. The main goal of this dissertation is to develop an environment for the test-time minimization problem in addition to associated issues, such as test area overhead, performance overhead at the runtime, etc. In order to reduce the test cost in terms of low test time, low area overhead, low-performance overhead, etc., the proposed test approach is divided into two parts: test algorithm and test scheduling. As the first pillar towards the goal, an on-line, distributed built-in-self-test (BIST) oriented test algorithm is proposed, that with the help of a test module (must be included in a modern NoC) has the capability in detecting a channel fault and identifying the faulty wires from the channel. As the second pillar to reach the goal, a suitable test scheduling scheme is proposed, which makes the present test solution scalable with respect to different network architectural characteristics: network size, channel width, and network type, i.e., large-scale NoC architectures in general. This dissertation contains five contributed works. First three contributions explore the test of stuck-at, open, and short faults in NoC channels. Here, the channels are assumed to follow the single fault model. The fourth contribution includes the test of manufacturing and transient faults in the channels. The final contribution includes the test of coexistent manufacturing channel-faults. In the last two contributions, a channel can be assumed to follow the multiple fault model. In all the contributions, experimental results reveal that the proposed solutions impose less test time, area, and performance overhead as compared to existing testing techniques.