Numerical Modeling and Analysis of Graphene-based Field-Effect Transistors

A

Thesis submitted

for the award of the degree of

DOCTOR OF PHILOSOPHY

By

Brajesh Rawat

DEPARTMENT OF ELECTRONICS AND ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI

GUWAHATI - 781 039, ASSAM, INDIA

August 2017

TH-1608_11610201

DECLARATION

This is to certify that the thesis entitled "**Numerical Modeling and Analysis of Graphene-based Field-Effect Transistors**", submitted by me to the *Department of Electronics and Electrical Engineering, Indian Institute of Technology Guwahati* for the award of the degree of **Doctor of Philosophy**. This is an original research work carried out by me under the supervision of **Prof. Roy P Paily**. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Signed:

Brajesh Rawat
Department of Electronics & Electrical Engineering,
Indian Institute of Technology Guwahati,
Guwahati-781039, Assam, India.

Date:

TH-1608_11610201

TH-1608_11610201

CERTIFICATE

This is to certify that the thesis entitled "**Numerical Modeling and Analysis of Graphene-based Field-Effect Transistors**", submitted by **Brajesh Rawat** (11610201), a research scholar in the *Department of Electronics and Electrical Engineering, Indian Institute of Technology Guwahati*, for the award of the degree of **Doctor of Philosophy**, is a record of an original research work carried out by him under my supervision and guidance. The thesis has fulfilled all requirements as per the regulations of the institute, and in my opinion has reached the standard needed for submission. The results embodied in this thesis have not been submitted to any other University or Institute for the award of any degree or diploma.

Signed:

Prof. Roy Paily
Department of Electronics & Electrical Engineering,
Indian Institute of Technology Guwahati,
Guwahati-781039, Assam, India.

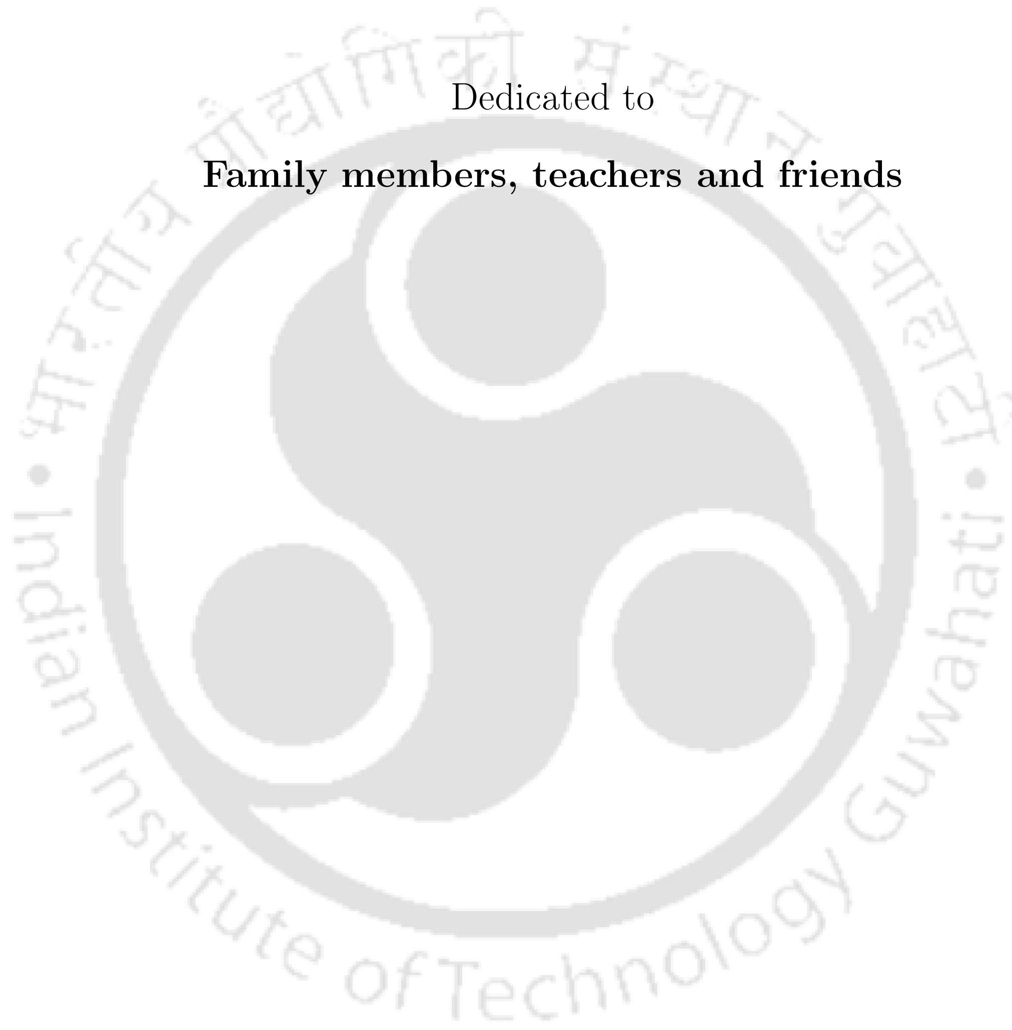
Date:

TH-1608_11610201

TH-1608_11610201

Dedicated to

Family members, teachers and friends



TH-1608_11610201

TH-1608_11610201

Acknowledgements

First and foremost, I feel it is a great privilege to express my deepest and most sincere gratitude to my supervisors Prof. Roy Paily for his continuing guidance and support throughout my research. His great insight into semiconductor device and encouragement allowed me to overcome all obstacles in making this work as complete as possible. I have no doubt that finishing my degree in a proper manner was impossible without the help, suggestions and advice from my supervisor.

I would also like to thank Dr. Amitabh Chatterjee for helping me to understand the quantum transport. I am also very thankful to my doctoral committee members Prof. Harshal B. Nemade, Prof. Deepak k. Goswami, Dr. Ramesh Kumar Sonkar, and Dr. Amit Acharyya for sparing their precious time to evaluate the progress of my work. I would also like to thank the Head of the Department and the other faculty members for their kind help and support in carrying out this work. I am grateful to the technical staff of the Department without their help, I could not have completed my work. My special thanks to Mrs. S. Josephine, Technical Officer, who has helped me in not only accessing the various lab resources but also helped me in correcting my publications.

My special thanks to my colleagues and friends at IIT Guwahati, Dr. Vinaya M M, Dr. Saroj Mondal, Pavan Kumar Manchi, Pallavi Mukhrejee, Moon Moon Bordeori for careful proofreading of publications and thesis, lively discussions, insightful comments and honest opinions on my research. I specially thank to my senior at VLSI Lab, Dr. Nagesh C H, Dr. Rahul Shrestha, Dr. Gaurav Saxena and Dr. Ratul Baruha for motivating, and providing useful guidance and resources. I would also like to extend my gratitude to Pralay Chakrabarty and Vimal Kumar Singh Yadav for providing his computer to carrying out my simulation work.

I would like to extend my sincere thanks to all my beloved friends, past and present - too big to list here. You guys have been excellent and it would be difficult to find a working group as good as you. They have always been around to provide useful suggestions and companionship. Someone or the other have sacrificed their time and have contributed directly or indirectly to my research work.

It does not become complete if I do not say any word about my school teachers, parents, my brothers and my sister-in-law. Whatever I am now is because of their continuous support and the encouragements. I do not know what to express but all I can say is I am incomplete and nothing without them.

TH-1608_11610201

Finally, I am indebted to Centre for Excellence In Nanoelectronics & Theranostic Devices, IIT Guwahati and Govt. of India for providing an opportunity, resources and financial support to carry out this research work.

Brajesh Rawat

TH-1608_11610201

Abstract

Graphene-based transistors are being explored extensively, and are now considered as a promising candidate for post-silicon electronics. Due to its high carrier mobility, high saturation velocity, high current densities and single atomic thickness, graphene field-effect transistor (G-FET) can be scaled to shorter channel lengths without encountering the adverse short channel effects that restrict the performance of existing devices. However, the absence of the energy gap in graphene sheet is proved to be a major limitation for FETs, as it causes poor ON/OFF current ratio for digital electronics and poor intrinsic gain for analog electronics. Many approaches, like lateral carrier constriction in nanoribbons (GNRs), vertical inversion symmetry breaking in bilayer graphene (BLG), and the combination of both in bilayer graphene nanoribbons (BLGNRs), have been suggested to open up an energy gap into the graphene.

The main objective of this work is to develop a quantum transport model for graphene-based field-effect transistors. For accurate analysis, quantum simulations are performed by solving ballistic non-equilibrium Green's function formalism (NEGF) self-consistently with 2-D Poisson's equation. Initially, a 1-D real-space transport model with analytically defined transverse modes is developed, and it can be easily extended to simulations of graphene, nanoribbons (BLGNRs), bilayer graphene (BLG), and bilayer graphene nanoribbons (BLGNRs) FETs. This 1-D transport assumption allows accurate results in a reasonable amount of time, which is essential for any quantum simulation.

A study on various forms of graphene-based field effect transistors is carried out to find their suitability for digital and/or analog/RF applications. Firstly, a study on graphene tunnel field-effect transistor (T-GFET) is carried out and it was found more suitable over G-FET for analog/RF applications. Further, two different FET structures are examined for BLGNR. A dual gate structure with chemically abrupt doped junctions is explored for digital applications, whereas a dual gate structure with electrostatically doped by back

TH-1608_11610201

gate is investigated for analog/RF applications. Finally, a BLGNR-TFET is explored for both low voltage digital and high-frequency RF applications. The device analysis has been carried out with respect to the oxide thickness, gate underlap, gate overlap, doping, device width, etc., to further improve the transistor performance.

In summary, in this thesis, a 1-D quantum transport model was developed for graphene-based FETs, and three specific graphene-based devices such as T-GFET, BLGNR-FET, and BLGNR-TFET were explored.

TH-1608_11610201

Contents

List of Figures xvii

List of Tables xxv

List of Acronyms xxvii

1 Introduction 1

1.1 Motivation . . . 2

1.2 Graphene for Electronics . . . 3

1.3 Transistor Figure of Merits and Trade-off . . . 5

1.4 State-of-art of Graphene-based MOSFETs . . . 7

1.4.1 Digital Electronics Applications . . . 7

1.4.2 Analog Electronics Applications . . . 12

1.5 Modeling of Nanoscale Devices . . . 14

1.6 Problem Definition . . . 17

1.7 Outline of Thesis . . . 18

2 Quantum Transport in Ballistic Graphene-based Transistors 21

2.1 Introduction . . . 22

2.2 NEGF Treatment of Quantum Transport . . . 23

2.3 Ballistic Transport in Graphene-based Transistors . . . 26

2.3.1 NEGF Treatment of Electronic Transport in GNR-FETs and G-FET . . . 26

2.3.2 NEGF Treatment of Electronic Transport in BLG-FET and BLGNR-FET . . . 31

2.3.3 2-D Electrostatics . . . 33

2.4 Results . . . 35

2.4.1 Simulation of GNR-FET . . . 36

2.4.2 Simulation of G-FET . . . 39

TH-1608_11610201

2.4.3 Simulation of BLGNR-FET . . . 41
2.5 Summary . . . 44
3 Analysis of Graphene Tunnel Field-Effect Transistor 45
3.1 Introduction . . . 46
3.2 Device Geometry and Performance Metrics . . . 47
3.3 Results . . . 48
3.3.1 Impact of Oxide Thickness . . . 51
3.3.2 Impact of Drain Underlap and Drain Overlap Lengths . . . 51
3.3.3 Impact of Channel and Drain Doping Concentrations . . . 52
3.3.4 Impact of Underlap and Overlap Lengths in a MD T-GFET . . . 55
3.3.5 Output Resistance and Intrinsic Gain . . . 56
3.3.6 C-GFET versus T-GFET . . . 57
3.3.7 Impact of Channel Length on Intrinsic Gain and Cutoff Frequency . . . 58
3.4 Summary . . . 58
4 Analysis of Bilayer Graphene Nanoribbon Field-Effect Transistors 61
4.1 Introduction . . . 62
4.2 Digital Performance . . . 62
4.2.1 Device Geometry and Performance Metrics . . . 63
4.2.2 ON-state and OFF-state Performance . . . 64
4.2.3 BLGNR-FET versus MLGNR-FET . . . 67
4.3 Analog/RF Performance . . . 69
4.3.1 Device Geometry and Performance Metrics . . . 69
4.3.2 Output Characteristics and Intrinsic Gain . . . 71
4.3.2.1 Effect of Bias Voltage . . . 73
4.3.2.2 Effect of Underlap . . . 74
4.3.3 Intrinsic RF Performance Metrics . . . 75
4.4 Summary . . . 76
5 Analysis of Bilayer Graphene Nanoribbon Tunnel Field-Effect Transistors 79
5.1 Introduction . . . 80
5.2 Device Geometry and Performance Metrics . . . 81

TH-1608_11610201

5.3 Digital Performance 82
5.3.1 ON-state and OFF-state Performance 82
5.3.2 BLGNR-TFET Versus MLGNR-TFET 87
5.4 Analog/RF Performance 90
5.4.1 Output Characteristics 90
5.4.2 Intrinsic Analog/RF Performance Metrics 92
5.4.3 RF Performance with Parasitics 95
5.5 Summary 97

6 Conclusions and Future Directions **99**
6.1 Conclusion 100
6.2 Future Directions 102

A Sancho-Rubio Algorithm **105**
A.1 Sancho-Rubio Algorithm for BLGNR-FET 106

B Carrier Statistics **109**
B.1 Carrier Statistics of Graphene, GNR, BLG and BLGNR 110

Bibliography **113**

List of Publications **120**

TH-1608_11610201

TH-1608_11610201

List of Figures

1.1 Schematic of different graphene MOSFET type, used in fabrication. 7

1.2 Schematic of different graphene-based structures to induce energy gap. (a) large-area graphene, (b) armchair graphene nanoribbon (GNR), (c) bilayer graphene, and (d) armchair bilayer graphene nanoribbon (BLGNR). 8

1.3 Schematic showing the physical transport mechanisms in MOSFET (left) and Tunnel FET (right). MOSFETs operate through thermionic emission over the barrier to the channel and thus have a fundamental limit in the steepness of switching. Tunnel FET operates through charge carriers transfer from one energy band into another and hence have potential to overcome this limitation. 10

1.4 Schematics of graphene-based TFET types: (a) planar geometry, (b) vertical heterostructure, and (c) BisFET or SymFET. 11

1.5 Qualitative shape of the output characteristics of a large-area graphene MOSFET with an n-type graphene channel, for different values of the top gate voltage, $V_{GS,top}$. The very narrow saturation region can be seen for moderate value of drain-to-source volatges [1]. 12

2.1 Schematic of (a) device coupled with two contacts, and (b) self-consistent procedure for device modeling. Where, H is the device Hamiltonian and U_{SC} is the self-consistent potential of the device, Σ_S and Σ_D is the self-energy matrices for source and drain contacts, respectively, n(r) is the electron density, and I_{DS} is the drain-to-source current. The μ_S and μ_D are the contacts Fermi levels, which are equal at equilibrium and differ by qV amount when a V bias applied across contacts. 23

2.2 Schematic of (a) N9 armchair edge GNR with the elementary cell (highlighted region), (b) 1-D unit cell with corresponding binding energy. Where, N denotes number of dimer lines or number of elementary cells along the width direction. 26

TH-1608_11610201

2.3 Schematic of 1-D elementary cell model of device having infinite contacts length. . . . 27

2.4 Schematic of (a) N=9 (W4) armchair edge BLGNR, where top and bottom layers represent by solid and dash lines, respectively, and (b) 1-D elementary cell with binding energy. 31

2.5 2D Simulation domain of double gate MOSFET. The channel is intrinsic and the gate length equals the channel length. The source and drain are the extension of channel and doped heavily. The dashed rectangular shows the element used to discretize the Poisson equation at (m,n). Uniformly spaced grids are used in both x and z directions, spatial constants are a and b respectively. An air spacer of 0.5 nm is assumed between the plane connecting the centers of carbon atoms and the interface of the oxide region to perform atomistic simulation. 34

2.6 Bandstructure of A-GNR as a function of k vector obtained from our calculations (solid lines) and from real-space approach (red triangles) [2] for (a) W12 (3p), (b) W13 (3p+1) and (c) W14 (3p+2) widths, where p is the integer and W12, W13 and W14 represent the widths of 1.46 nm, 1.62 and 1.74 nm. Where d_a=3a_c is the 1-D unit cell distance along length. 36

2.7 The variation of band gaps of A-GNRs as a function of width obtained (a) from our approach and (b) from DFT approach [3]. Our results are not matching with DFT results because the edge bond relaxation is not considered in simulation. 37

2.8 (a) Transfer characteristics of W12 AGNR-FET from our approach (solid lines) and Low's approach (circles). (b) Output characteristics of AGNR-FET from our approach (solid line), Low's approach (circles) and Zhao's real-space/mode space approach (dash line), at $V_{GS} = 0.5$ V. 38

2.9 Potential profile (left) and corresponding current spectra (right) of G-FET at $V_{GS} = -0.1$ V and $V_{DS} = 0.5$ V from our approach (solid lines) and Low's approach (circles). 39

2.10 Transfer and output characteristics of G-FET from our approach (solid lines) and Low's approach (circles). 40

TH-1608_11610201

2.11 Bandstructure of BLGNR as a function of k vector for (a) W12 (3p), (b) W13 (3p+1) and (c) W14 (3p+2) widths, where p is an integer and W12, W13 and W14 represent ribbon widths of 1.46 nm, 1.62 and 1.74 nm, respectively. Where d_a=3a_c is the 1-D unit cell distance along length. 42

2.12 The variation of band gaps of Armchair BLGNRs as a function of width obtained from (lines) our calculations based on 1-D RS and from (dots) DFT approach with edge effects [4]. For narrow widths, the edge effects become significant that cause deviation in our results with DFT data. 43

2.13 Energy gap, extracted from transmission spectra, with V_{diff} for W30 (3.74 nm) and W15 (1.87 nm) BLGNR widths. 43

3.1 Simulated tunnel graphene field effect transistor (T-GFET) geometry. 47

3.2 Output characteristics of nominal T-GFET for different positive V_{GS}. 48

3.3 (Left) T-GFET potential energy profile along the transport direction and (right) corresponding current spectra at V_{GS} = 0.4 V for V_{DS} = 0.3 V (dash line) and V_{DS} = 0.6 V (solid line). The current spectra shows the source-channel (S-C) tunneling regime and the channel-drain (C-D) tunneling regime separated in the energy axis. Where E_{FS} and E_{FD} are Fermi levels at the source and drain regions respectively, and E_{kch} is Dirac point energy in the channel. 49

3.4 The contribution of S-C and C-D tunneling currents in T-GFET for different V_{DS}, at (a) V_{GS} = 0.2 V, and (b) V_{GS} = 0.6 V. 50

3.5 (a) Output characteristics of T-GFET for different equivalent oxide thickness (EOT) at V_{GS} = 0.4 V, and (b) Corresponding potential energy profile in the channel region at V_{DS} = 0.6 V. 51

3.6 (a) Output characteristics of T-GFET for a drain overlap length, no drain overlap and underlap, and two different drain underlap lengths at V_{GS} = 0.4 V, and (b) Corresponding potential energy profile in the channel and drain regions for V_{DS} = 0.3 V and V_{DS} = 0.8 V for structures having 8-nm drain underlap, no drain underlap and drain overlap, and 8-nm drain overlap length. 52

TH-1608_11610201

3.7 Output characteristics of nominal T-GFET and modified doped (MD) T-GFET for different V_{GS}. Modified channel doping concentration is $N_C = 8 \times 10^{11}$ cm^{-2} and drain doping concentration is $N_D = 4 \times 10^{12}$ cm^{-2}. 53

3.8 Modified doped (MD) T-GFET potential energy profile, at $V_{GS} = 0.4$ V, for different V_{DS}. 54

3.9 (a) Output characteristic of MD T-GFET for three cases: 8nm drain underlap, no underlap and overlap, and 8-nm drain overlap, at $V_{GS} = 0.4$ V. (b) Corresponding potential energy profiles in the channel and drain regions at $V_{DS} = 0.3$ V and $V_{DS} = 0.8$ V. 55

3.10 Comparison of four different device structures: nominal T-GFET, T-GFET with 8-nm drain underlap, MD T-GFET, and MD T-GFET with 8-nm overlap at $V_{GS} = 0.4$ V. (a) Output resistance at $V_{DS} = 0.3$ V and $V_{DS} = 0.7$ V, and (b) Intrinsic gain at $V_{DS} = 0.3$ V and $V_{DS} = 0.7$ V. 56

3.11 Comparison between C-GFET and T-GFET obtained at $V_{DS} = 0.5$ V. (a) Transconductance (g_m), (b) Output resistance ($1/g_0$), (c) Intrinsic gain (A_{V0}), and (d) Cutoff frequency (f_T). 57

3.12 (a) Peak intrinsic gain versus channel length obtained at $V_{DS} = 0.5$ V, and (b)Peak cutoff frequency versus channel length obtained at $V_{DS} = 0.5$ V. The experimental results are based on self-aligned nanowire GFET [5]. 58

4.1 Schematic of simulated bilayer graphene nanoribbon FET (BLGNR) device. 63

4.2 Transfer characteristics of (a) bilayer graphene (BLG) FET, and (b) W60 width , (c) W30 width, and (d) W15 width BLGNR-FETs, at $V_{DS} = 0.2$ V. Where, $V_{diff} = V_{GS2} - V_{GS1}$ and $V_{\min} = (V_{GS2} - V_{GS1})/2$. 64

4.3 (a) Energy band profile along transport direction and (b) corresponding energy-resolved transmission spectra of W30 BLGNR-FET, at $V_{GS1} = V_{GS2} = 0$ V. Energy-resolved transmission spectra of (c) W30, (d) W60, (e) W15 BLGNR-FETs and (f) BLG-FET, at $V_{GS1} = -1$ V and $V_{GS1} = 0$ V. 66

4.4 Energy-resolved transmission spectra, at $V_{DS} = 0.2$ V of (a) W60 and (b) W15 BLGNR devices at $V_{diff} = 1$, (c) W60 MLGNR device at $V_{diff} = 0$ V and (d) W15 MLGNR device at $V_{diff} = 1$ V. 68

TH-1608_11610201

4.5 I_{ON}/I_{OFF} and I_{ON} of BLGNR and MLGNR devices as a function of device width, at $V_{DS} = 0.2$ V, for (a) $V_{diff} = 0$ V, and (b) $V_{diff} = 1$ V. Where, $V_{diff} = V_{GS2} - V_{GS1}$. . . 69

4.6 Schematic of simulated BLGNR-FET. The back gate is used to electrostatically doped the source and the drain regions. The zero voltage on the source terminal is taken as a reference. 70

4.7 Output characteristics of (a) W15 and (c) W30 BLGNR-FET at $V_{bias} = 1.2$ V for various top gate voltages. Corresponding current spectra of (b) W15 and (d) W30 device at $V_{GS1} = -0.2$ V for three different V_{DS} values. Where W15 and W30 represent the widths of 1.87 nm and 3.74 nm. 71

4.8 V_{DS} dependency of (a) Transconductance, g_m , (b) Output conductance, g_{ds}, and (c) intrinsic gain A_{V0} for W15 and W30 devices, at $V_{GS} = -0.2$ V and $V_{bias} = 1.2$ V. . . . 73

4.9 Impact of bias voltage on BLGNR-FET. (a) drain current (I_{DS}) and (b) intrinsic gain (A_{V0}) as function of V_{DS} for different bias voltages, at $V_{GS} = -0.2$ V and $V_{bias} = 1.2$ V. 74

4.10 Impact of underlap on BLGNR-FET. (a) drain current (I_{DS}) and (b) intrinsic gain (A_{V0}) as function of V_{DS} for different underlap length on the source and drain sides, at $V_{GS} = -0.2$ V and $V_{bias} = 1.2$ V. 75

4.11 Intrinsic RF performance metrics with respect to V_{GS}. (a) Transconductance, (g_m), and (b) intrinsic cutoff frequency (f_T) for W15 and W30 BLGNR-FETs, at $V_{DS} = 0.25$ V. Where W15 and W30 represent the widths of 1.87 nm and 3.74 nm. 76

5.1 Schematic of simulated BLGNR-TFET. 81

5.2 Influence of gate voltages on W15 (1.87 nm wide) BLGNR-TFET operation. (a) Transfer characteristics, and (b) the energy resolved current spectra at OFF-state for different V_{diff}, where, $V_{diff} = V_{GS2} - V_{GS1}$, $V_{\min} = (V_{GS2} - V_{GS1})/2$, and $E_{g,ch}$ is the bandgap in the channel energy region. 82

5.3 Impact of drain voltage and channel width on device operation. (a) Transfer characteristics of W15 (1.87 nm wide) BLGNR-TFET for various V_{DS} at $V_{diff} = 0$ V, and (b) Transfer characteristics for various bilayer ribbon widths at $V_{DS} = 0.2$ V. 84

TH-1608_11610201

5.4 Influence of device design parameters on W15 (1.87 nm wide) BLGNR-TFET operation. (a) The transfer characteristics at $V_{DS} = 0.2$ V and (b) corresponding band profile at the channel and drain region at $V_{GS1} = V_{GS2} = 0.1$V for six different structures: 1) nominal device (ND), 2) device with 5-nm drain underlap (UL), 3) device with 5-nm drain overlap (OL), 4) device with modified doping (MD) fractions, 5) MD fractions device with 5-nm underlap (MD+UL), and 6) MD fractions device with 5-nm overlap (MD+OL). 85

5.5 Performance comparison of MD+OL (dash line) with nominal device (solid line), at $V_{DS} = 0.2$ V. (a) I_{ON}/I_{OFF} and average subthreshold swing (SS), and (b) I_{ON} as a function bilayer ribbon width. 87

5.6 Performance comparison between BLGNR-TFET and MLGNR-TFET at $V_{DS} = 0.2$ V. (a)-(b) I_{ON} versus I_{ON}/I_{OFF}, (c)-(d) Intrinsic device delay (τ) versus I_{ON}/I_{OFF}, and (e)-(f) Power delay product (PDP) versus I_{ON}/I_{OFF} for W21, W18 and W15 (left side) and W12 and W9 (right side). These parameters are calculated only for n-type branch of transfer characteristics. 88

5.7 Output characteristics for different positive V_{GS} for (a) W15 BLGNR and (b) W30 BLGNR, where $V_{GS} = V_{GS1} = V_{GS2}$. 91

5.8 Output characteristics of nominal device (ND) and modified doped device with 5-nm drain overlap (MD+OL) for (a) W15 BLGNR and (b) W30 BLGNR, where $V_{GS} = V_{GS1} = V_{GS2}$. 92

5.9 Impact of V_{GS} on the intrinsic analog performance metrics, at $V_{DS} = 0.4$ V. (a) transconductance (g_m), (b) output conductance (g_{ds}), (c) intrinsic gain (A_{V0}), and (d) intrinsic cutoff frequency (f_T) as function of V_{GS}. 93

5.10 Impact of channel width on intrinsic analog/RF performance metrics. (a) The peak intrinsic gain and (b) the peak cutoff frequency as a function of bilayer ribbon width (W), at $V_{DS} = 0.4$ V. 94

5.11 The small-signal equivalent circuit model used to explore the impact of additional external parasitics on the RF performance metrics of BLGNR-TFETs. 95

TH-1608_11610201

5.12 Impact of parasitics on RF figure of merits. Plot of short circuit current gain ($|\mathrm{H}_{21}|$), maximum available gain (MAG), and voltage gain with open circuit load (A_v) in the presence of parasitics for (a) W15 device and (b) W30 device. Devices are biased at $V_{GS} = 0.4$V and $V_{DS} = 0.4$V, which is the maximum A_{V0} and f_T bias point in Fig. 5.10 for W15 device. The sold lines are obtained with $R_S = R_D = 100$ Ω-μm, $R_g = 0$ Ω-μm, $C_{\mathrm{int}} = C_{ext} = 0$ fF/μm and the dash lines are obtained with $R_S = R_D = 100$ Ω-μm, $R_g = 4\Omega$-μm, $C_{\mathrm{int}} = C_{ext} = 0.1$ fF/μm. 96

A.1 Schematic of BLGNR elementary cell in the source and the channel interface. The g_i is the surface Green's function for the i-th carbon ring inside the drain. The α is on-site energy, β_1, β_2 and β_3 are the first, second and third kind coupling matrix between neighboring rings, as described in section 2.3.2. 106

TH-1608_11610201

TH-1608_11610201

List of Tables

1.1 Performance comparison of graphene-based MOSFETs with Si MOSFET from digital applications point of view. 10
1.2 Performance of graphene-based TFET for digital applications. 12
1.3 Performance comparison of graphene-based MOSFETs with Si MOSFET from analog/RF applications point of view. 14
1.4 Classifications of transport models 15

2.1 Minimum error criterion of current calculation and the total simulation time for our approach and Low's approach. The simulation time is included the Poisson equation solving, when $V_{GS} = 0.5$ V and V_{DS} increases from 0 to 0.5 V by 0.05 V per step (shown in Fig. 2.8). The simulation were run on a four core 3.2 GHz CPU using parfor loop in MATLAB. 41

4.1 ON current and ON/OFF current ratio of BLGNR-FETs according to two definitions, at $V_{diff} = 0$ V and $V_{DD} = 0.2$ V. 65

5.1 Performance comparison of Six different device structures, at $V_{DS} = 0.2$ V. 86
5.2 Extrinsic RF Figure of Merits for W15 and W30 BLGNR-TFETs at internal $V_{DS} = 0.4$ V and $V_{GS} = 0.4$ V. 95

6.1 Comparison of graphene-based MOSFETs with Si-MOSFET and ITRS 2014 prediction 101
6.2 Digital Performance comparison of BLGNR-TFET with other material TFETs operating under 0.5 V. 102

TH-1608_11610201

TH-1608_11610201

List of Acronyms

A-GNR/AGNR	Armchair edged gaphene nanoribbon
A-BLGNR/ABLGNR	Armchair edged bilayer gaphene nanoribbon
BLG	Bilayer graphene
BLGNR	Bilayer graphene nanoribbon
BTBT	Band to Band tunneling
BTE	Boltzmann transport equation
BiSFET	Bilayer pseudospin field-effect transistor
C-D	Channel to drain
C-GFET	Conventional graphene field-effect transistor
CMOS	Complementary Metal-Oxide-Semiconductor
CNT	Carbon nanotube
CV	Conduction band
CVD	Chemical vapor deposition
DC	Direct current
DG	Double gate
EOT	Equivalent oxide thickness
FOM	Figure of Merit
GBT	Graphene base hot-electron transistor
GFET/G-FET	Gaphene field-effect transistor
GHz	Gegahetrz
GNR	Gaphene nanoribbon
HEMT	High electron mobility transistor
IC	Integrated Circuit
ITRS	International roadmap for semiconductor

TH-1608_11610201

LDOS	Local density of state
MD	Modified doping
MLGNR	Graphene nanoribbon
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
ND	Nominal device
NEGF	Non-equilibrium Green's function formalism
OL	Overlap
RF	Radio Frequency
SCE	Short channel effect
S-C	Source to channel
SOI	Silicon on insulator
SymEFT	Symmetric tunneling field effect transistor
TFET	Tunneling field-effect transistor
T-GFET	Graphene tunnel field-effect transistor
THz	Terahetrz
VB	Valance band

TH-1608_11610201

1

Introduction

Indian Institute of Technology Guwahati

Contents

1.1 Motivation 2
1.2 Graphene for Electronics 3
1.3 Transistor Figure of Merits and Trade-off 5
1.4 State-of-art of Graphene-based MOSFETs 7
1.5 Modeling of Nanoscale Devices 14
1.6 Problem Definition 17
1.7 Outline of Thesis 18

TH-1608_11610201

1.1 Motivation

Use of electronics has become an integral part of modern life, and we hardly think of the world without it. Everything from personal computer to coffee machine is full of electronic components and more specifically, integrated circuits (IC). In many ways, the most important element of IC is the field-effect transistor. Among the many task of transistors, the main works are to either act as a switch or act as an amplifier. Currently, the most common transistors are silicon-based metal oxide semiconductor field-effect transistors (MOSFETs), and more specifically complementary metal-oxide-semiconductor (CMOS) technology in which a n-type and p-type MOSFETs are connected together to form an inverter.

Aggressive scaling of CMOS technology has been a main key for continuous progress in silicon based technology because it leads to extraordinary improvements in the switching speed, density, functionality and cost of microprocessors. After five decades of fulfilling the Moore's law by continuously doubling transistor density in every 18 to 24 months, the industry is now manufacturing integrated circuits with transistors, which are of 20-nm or 14-nm channel length. As the present technology has entered into deep nanoscale regime, it becomes more and more difficult to further scale down the device dimension and simultaneously achieved best device performance. Currently, CMOS technology is facing two major challenges that results in high power consumption [6]: 1) stopping the rising leakage current due to adverse short channel effects (SCEs), and 2) increasing difficulty in further reducing the supply voltage due to the fundamental thermionic limitation of the steepness of turn-on characteristics, or subthreshold swing.

Over the past decade, considerable efforts have been made to extend the life of Si-MOSFET by introducing new fabrication steps or by making some improvement in the existing technology. An early development was started with strain engineering, adding germanium to silicon to alter the crystal properties, which had boosted speed and enabled the performance improvement with the scaling down of the device dimensions. The next challenge to the continues scaling was the rising issue of heat dissipation, but this problem was overcome by reducing the clock frequency and clever designing of microprocessor architectures (several parallel CPUs). However, these solutions may not carry the CMOS technology scaling much further into the future. New solutions, which give a new life to the MOSFET, have been developed to boost the effectiveness of gate control by creating a device with a thin layer of silicon, built on an insulating layer, which is called fully depleted silicon-on-insulator

TH-1608_11610201

(SOI), and by creating a conduction channel with a thin silicon "fin", which is called FinFET or Tri-Gate MOSFET [7]. While these architectures help for the moment, but achieving physical dimensions near the 'deeper nanoscale' regime of beyond 20 nm is a challenge for existing technologies [8]. The chip makers have moved from 20-nm to 14-nm, but the continued performance improvements comes to a gradual end [9] due to: 1) no economic advantage, 2) require extra circuitry to track and adapt performance variations, and 3) the density improvement is closer to 1.6× rather than 2×. Therefore, for the grow of semiconductor industry, incorporations of new materials or completely different transistor architectures are needed.

The International Technology Roadmap for Semiconductors (ITRS) refers the future transistor scenarios as 'More-Moore', 'More-than-Moore' and 'Beyond-CMOS' [10]. The first scenario is the expansion of the CMOS platform by conventional dimensional and functional scaling. More-than-Moore scenario is to allow the non-digital functionalities into the chip which do not necessarily scale according to "Moore's Law", but provide additional value in different ways to migrate from the system board-level into the package or onto the chip. Lastly, beyond-CMOS scenario refers to new information processing devices and architectures. Graphene transistors are a prime example of beyond-CMOS devices.

The outstanding electronic properties make graphene a promising material for post-silicon electronics. Carriers in graphene move faster than silicon, even though it has zero energy gap. Graphene has offered great potential of making devices with extremely thin channel, which would allow field-effect transistors in shorter channel lengths with higher speed. Within a period of ten years, GFET has grown from a single transistor in the lab to an integrated circuit. Despite the rapid progress in graphene transistors, there are still many issues that need to be solved before they gain commercial potential.

1.2 Graphene for Electronics

Graphene is a monolayer of carbon atoms arranged in a 2-D honeycomb lattice and is the mother of well known carbon materials, such as graphite, carbon nanotube (CNT) and fullerene. Since the discovery [11], graphene is being explored very extensively and several unique electronic properties has reported, such as 1) the highest room temperature carrier mobility and highest carrier saturation velocity of all known materials [1], 2) ballistic transport across the distances of several hundred nanometers

TH-1608_11610201

at low bias [12], 3) symmetric valance and conduction bands, 4) excels in thermal conductivity and mechanical stiffness, 5) sustain current density higher than the most conductive metals, etc.

These outstanding properties of graphene have attracted intense research activities to take advantage of this new material for improving existing electronic applications and inventing new ones. Some of the target applications of graphene includes digital electronics [13], radio-frequency (RF) electronics, [14], advanced sensors [15], semitransparent electronics [16], low power switches [17], solar cells [18], and battery energy storage [19]. While the absence of an energy gap in graphene imposes serious limitations on its application for digital electronics [1], many RF circuits have shown promising operating frequency with a low ON/OFF current ratio transistors [20]. Currently, graphene-based transistors are pushed closer to state-of-the-art in semiconductor radio-frequency transistors. Moreover, graphene's strong phonon interaction, process compatibility and electrochemical stability offer a possibility to add more functions to silicon-based CMOS devices, such as radio-frequency switches and optical modulators and photo-detectors.

The first fabricated graphene transistor was a back gate structure using exfoliated graphene on the top of a highly doped silicon wafer in which SiO_2 acting as gate oxide [11]. Since then, graphene transistor has been developed very rapidly and nowadays the fabrication has been reached wafer-scale level by using chemical vapor deposition (CVD) [21] and epitaxial SiC-graphene [22]. While most of the research works with graphene have focused on replacing the silicon channel, some groups have come up with several ideas to induce an energy gap in graphene, such as the formation of nanoribbon [23], bilayer graphene [24], chemical modified graphene [25] and single electron transistor [26]. However, some of these approaches have been unable to open an energy gap wider than 360 meV [27,28], which limits its ON/OFF current ratio. Moreover, they lead to the degradation of inherent electronic properties, like carrier moblity, of graphene [1]. On the other hand, to enhance ON/OFF current ratio, some groups have come up with different ideas for transistors, such as graphene transistors named BiSFET (bilayer pseudospin field-effect transistor) [29], SymFET (symmetric tunneling field effect transistor) [30] and GBT (graphene base hot-electron transistor) [31]. Except GBT, most of these devices are purely theoretical and have not been experimentally realized yet because of stringent requirement for device fabrication.

Specially, when the fabrication technologies are in the early stage of development for graphene, modeling can be a very powerful tool to evaluate different technology options and different device

TH-1608_11610201

structures. An understanding of the underlying physics aids in the optimization in both materials and architecture levels and can lower development costs by reducing the time and effort between design and fabrication of working prototypes. Therefore, in this work, the quantum transport modeling has been used to address issues and to evaluate different options for improving the performance in graphene-based MOSFETs.

1.3 Transistor Figure of Merits and Trade-off

Two major applications of semiconductor devices are in digital and radio-frequency (RF) ICs. The digital IC consists of logic gates, for example NAND and NOR, in which basically n-type and p-type transistors are connected together to perform a certain logic operation. The gate control enables the use of transistor as switch, which conducts high current when it is on, and very low current when it is off. On the other hand, in radio-frequency IC, transistor operates always operates in ON-state and the small-signals are superimposed on dc gate-to-source voltage that are to be amplified. With so many diverse expectations, it is sometime useful to have some Figure of merits (FOMs) that captures some key aspects of transistor performance. These FOMs also give the requirements and challenges that must be met to incorporate graphene into semiconducting devices.

- The gate voltage on the channel is enabled to use FET as switch, which requires high value of current in the ON-state and low value of current in OFF-state. The large ON current allows quick charging of a capacitive load which typically includes the gates of one or more subsequent transistors, while low OFF current provides low leakage current which mainly decides the static power dissipation. The ON/OFF current ratio is a very important FOM of digital switches, and a larger value is better. As per International roadmap for semiconductor (ITRS) 2011 requirement, 17 nm multigate MOSFET require ON current of 1628 $\mu A/\mu m$ and ON/OFF current ratio in between $10^4 - 10^7$ for high performance logic applications [32]. This value of ON/OFF ratio can only be achieved if the transistor channel is semiconducting and has a wide enough energy gap.

- Another important FOM to assess switching behavior is the subthreshold slope (SS). It represents the rate of increase of the current below the threshold voltage (i.e., $V_{GS} < V_{Th}$ for n-FETs).

$$SS = \frac{dV_G}{d(\log_{10}(I_{DS}))} \tag{1.1}$$

The subthreshold slope is expressed in millivolts per decade of current (mV/dec). A steepness of

TH-1608_11610201

subthreshold slope exhibits a faster transition between OFF-state and ON-state. SS should be as small as possible and its lower limit is 60 mV/dec for conventional Si MOSFETs.

- The important performance metric for RF transistor is the unity current gain frequency or cutoff frequency (f_T), which represents the maximum operating frequency at which a transistor might prove useful. It is also the most common measure of transistor speed. The intrinsic cutoff frequency defined as:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{1.2}$$

  Where, C_{gs} is the gate to source capacitance, C_{gd} is the gate to drain capacitance and g_m is the transconductance. To achieve high f_T, the transistor transconductance (g_m) should be high and all other elements of the equivalent circuit elements should be as small as possible.

- The intrinsic gain (A_{V0}) is also an important performance metrics of RF transistor, which is a measure of the maximum possible low-frequency small-signal voltage gain it can provide. The intrinsic gain is given as:

$$A_{V0} = \frac{g_m}{g_{ds}} \tag{1.3}$$

  The voltage gain of a transistor is generally maximized by lowering output conductance (g_{ds}) and hence operating it in the deep saturation mode.

- Another important parameter for RF transistor is the maximum oscillation frequency or unit power gain frequency (f_{max}). It represents how fast the channel power transmission is modulated by the gate voltage. The f_{max} is defined [20] as:

$$f_{\max} = \frac{f_T}{2\sqrt{g_{ds}(R_g + R_s) + 2\pi f_T R_g C_g}} \tag{1.4}$$

  Where, R_g and R_s are the resistance of the gate and source terminals, respectively, and C_g is the gate capacitance. The low output conductance (g_{ds}) is also one of the key factor in increasing the f_{max}. Thereby, a high f_{max} can be attained when the transistor is driven into deep saturation.

There are many key performance indicators for transistor: material specific parameters, such as energy gap, mobility and saturation velocity; digital circuit specific parameters, such as gate delay and dynamic switching energy; and analog circuit specific parameters, such as 3-dB bandwidth, GBW and noise. In this work, the focus is on the potential use of graphene as logic and analog transistors

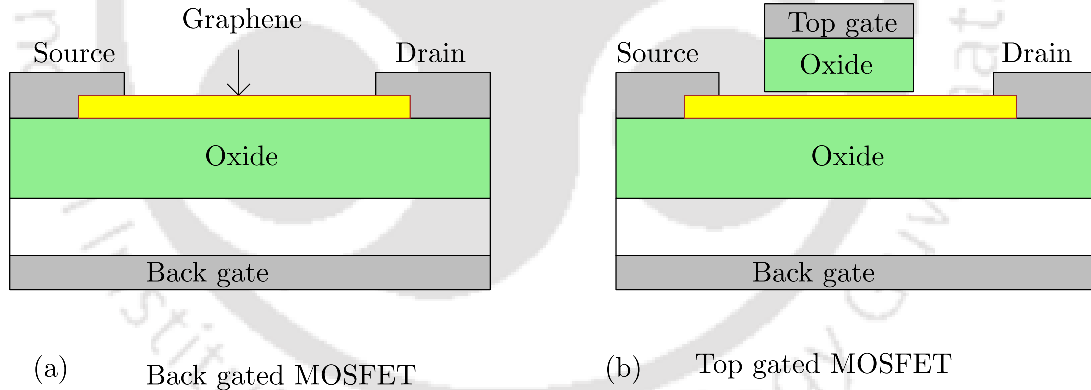
TH-1608_11610201

and therefore the discussion is limited to parameters at device level and not much at circuit level or at the application level. In analog transistors, the choice of some parameters mostly depends on the application. For example, an amplifier simultaneously requires high f_T and A_{V0}, while frequency multiplier and mixer need high f_T and f_{max}. Importantly, f_{max} and A_{V0} are closely related to each other, and the peak in both parameters can be achieved when the transistor drives into good current saturation. In this work, the intrinsic gain and cutoff frequency are widely preferred to estimate analog/RF performance of graphene-based transistors.

1.4 State-of-art of Graphene-based MOSFETs

Graphene has attracted considerable interest among the electron-device community. Until now, most of the work on graphene devices has been related to field-effect transistor. In the following section, the current status of graphene-based FETs and the most critical problems that remain to be resolved for digital and analog applications are discussed.

1.4.1 Digital Electronics Applications



(a) Back gated MOSFET (b) Top gated MOSFET

Fig. 1.1: Schematic of different graphene MOSFET type, used in fabrication.

Fig. 1.1(a) shows the first demonstrated graphene MOSFET concept in 2004. By mechanical exfoliation of graphite, single graphene layers are formed and it was transferred to a 300 nm SiO_2 which has grown over a doped silicon that served as a back gate [11]. This device structure has been good for proof of concept, but not suitable for realistic applications due to larger parasitics capacitances and poor gate control. In 2007, the first top-gated graphene MOSFET was reported [(Fig. 1.1(b)] and it represents the preferred option for practical applications [33]. Since then, the graphene transistors have been developed intensively and reached to the wafer scale fabrication. In particular, natural

TH-1608_11610201

graphene is gapless and the absence of the energy gap causes a larger OFF current. Therefore, the ON/OFF current ratios for graphene transistor are about 7-10 [34, 35], which is much lower than the $10^4 - 10^6$ range required for logic applications.

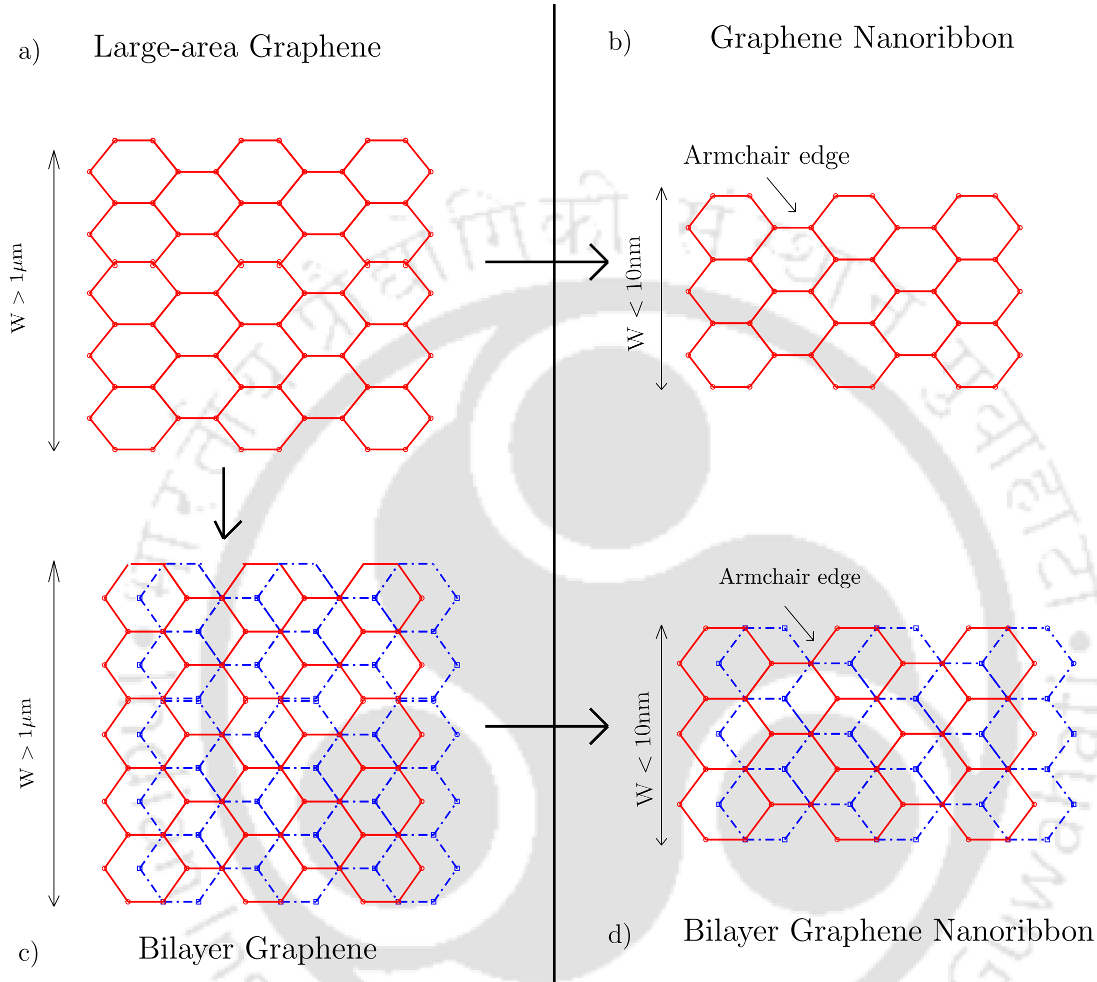


Fig. 1.2: Schematic of different graphene-based structures to induce energy gap. (a) large-area graphene, (b) armchair graphene nanoribbon (GNR), (c) bilayer graphene, and (d) armchair bilayer graphene nanoribbon (BLGNR).

However, there are many ways to modify the band structure and induce an energy gap in graphene. The two widely preferred approaches in transistors are (1) confining the large-area graphene in lateral direction to form graphene nanoribbon [Fig. 1.2(b)], and (2) vertical inversion symmetry breaking in bilayer graphene [Fig. 1.2(c)]. It has been found that graphene nanoribbons (GNRs) of sub-10 nm width are semiconducting due to lateral confinement of the electron wave function in the transverse direction and edge disorder induced Anderson localization [23, 36–38]. In particular, the energy gap opening in GNRs is inversely proportional to ribbon width and thus very narrow ribbon can induce

TH-1608_11610201

a significant energy gap for transistor operation. However, theoretical studies indicate that edge roughness can significantly degrade the performance of GNR-FETs [27, 39] and cause device-to-device variation. So far, the highest ON/OFF current ratios between $10^5 - 10^6$ have been reported at 6 K in FET with GNRs produced using chemically synthesized by phase derived method to achieve ultra-smooth edges [37], while the ON/OFF current ratio of 10^4 has been achieved at room temperature in FET with GNRs fabricated using edge narrowing methods [40]. Even though the most recent advancements allow the large-scale fabrication of GNR with controlled alignment and smooth edges [41, 42], very narrow ribbon width significantly reduces carrier mobility and hence the current density, which significantly lower the performance of GNR MOSFET compared to Si MOSFET [1]. Table 1.1 compares the graphene-based devices with Si MOSFET from a digital application point of view.

Second strategy is to apply the transverse electric field across bilayer graphene (BLG) that breaks inversion symmetry and induce an energy gap. Theoretical studies have shown that the energy gap of 200-250 meV can be reached with a vertical electric field of 1-3$\times 10^7$ V/cm [24, 43]. The experimental studies in BLG-FETs have reported an energy gap of 200-250 meV and maximum ON/OFF current ratio of about 100, which is significantly smaller for switching requirement [28, 44], as shown in Table 1.1. The challenges persists with BLG-FETs is that the field-induced energy gap is considerably smaller for logic transistor.

An alternate strategy to open a significant energy gap is by combining both bilayer graphene and GNRs to form bilayer graphene nanoribbon (BLGNRs) [Fig. 1.2(d)]. Recent experimental and theoretical studies have confirmed the energy gap opening in BLGNR by quantum confinement and vertical electric field [45–48]. Interestingly, recent experimental work with BLGNR-FET has demonstrated an I_{ON}/I_{OFF} ratio of over 3000 at room temperature for width wider than 40 nm [49] by applying a vertical electric field . This ON/OFF current ratio of BLGNR-FET has been 30 fold higher than the highest value reported for BLG-FET [43]. Until now, BLGNR-FETs have small ON/OFF current ratio for switching requirement, but they have shown significant energy gap at very narrow width. Therefore, further fabrication advancements are required to produce smooth edge BLGNR with narrow width in order to improve the device performance.

In MOSFETs, the charge carriers are thermally injected over the channel barrier, as shown in Fig. 1.3(left). A gate voltage reduces the energy barrier and increases the amount of charge carriers. This simple barrier-lowering strategy is the most widely used current-control mechanism in semiconductor

TH-1608_11610201

Table 1.1: Performance comparison of graphene-based MOSFETs with Si MOSFET from digital applications point of view.

Material	Device Type	E_g (eV)	L_g (nm)	I_{ON} ($\mu A/\mu m$)	I_{ON}/I_{OFF}	Remarks
Si	FinFET	1.12	20 nm	1200	10^3	[50]
Graphene	Top-gated	0	2,500	40	7-10	Experimental [34, 35]
GNR	Top-gated	0.1-1.8	20	>0.01	10^5-10^6 (>6k)$^{\Theta}$ 10^4 (RT)$^{\spadesuit}$	Experimental and Simulation [37, 42, 51]
BLG	Top-gated	0.2-0.25	1,600	<1	100 (RT) 2000 (20K)	Experimental and Simulation [28, 52]
BLGNR	Top-gated	0.1-1.5‡	1,500	>1	3000^{ϕ}	Experimental [49]

Θ: GNR of width $W < 5$ nm and fabricated using E-beam lithography; $\spadesuit$: GNR of $W < 5$ nm and fabricated using Edge-narrowing; $\ddagger$: Energy gap is theoretical [4, 47]; ϕ: BLGNR of width around 40 nm. GNR: nanoribbon; BLG: bilayer graphene; BLGNR: bilayer graphene nanoribbon.

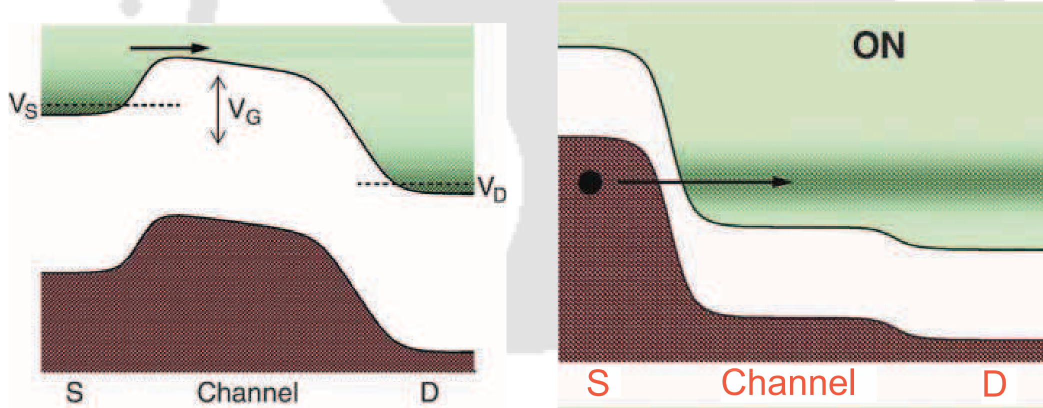


Fig. 1.3: Schematic showing the physical transport mechanisms in MOSFET (left) and Tunnel FET (right). MOSFETs operate through thermionic emission over the barrier to the channel and thus have a fundamental limit in the steepness of switching. Tunnel FET operates through charge carriers transfer from one energy band into another and hence have potential to overcome this limitation.

electronics. At room temperature, the current flowing over the barrier increases by a factor of 10 when the energy barrier is lowered by 60 millivolts; in other words, every "decade" of current change requires a change of 60 mV. The current leakage occurs below the device's threshold voltage, which is the voltage needed for the transistor to turn ON. To keep power consumption down, subthreshold swing should be kept as low as possible. Then, the device will need less voltage to be switched ON,

TH-1608_11610201

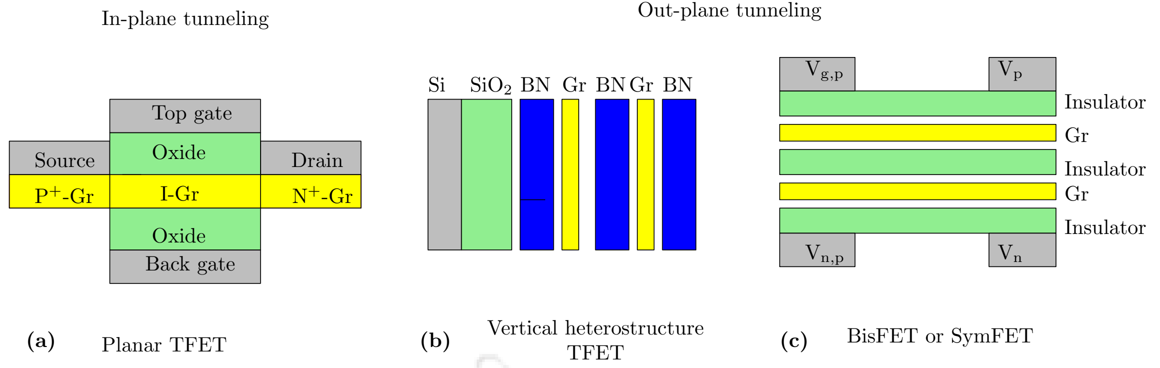


Fig. 1.4: Schematics of graphene-based TFET types: (a) planar geometry, (b) vertical heterostructure, and (c) BisFET or SymFET.

and it will leak less current when it's OFF.

Alternately, a transistor architecture that block the carrier flow at the OFF-state can be developed. A Tunnel FET, in which charge carriers transfer from one energy band into another is controlled by gate voltage [1.3(right)], should be able to switch with a much smaller voltage swing. This function can be realized in a reverse-biased p-i-n structure, as shown in Fig. 1.4(a). It has the same basic configuration of source, drain, and gate with similar electrical behavior when wired into circuits and therefore the CMOS fabrication strategy need not to be changed drastically. It turns out that silicon and germanium are not great for tunneling due to their indirect energy gap. The low ON-state current is a major limitation with Si and Ge-based TFETs.

The dominance of BTBT current with a small carrier effective mass and direct energy gap make graphene a most suitable material for TFET, which offers low OFF current and small subthreshold swing (SS). Due to 2-D nature, research groups have developed TFET with graphene based on in-plane and out-plane tunneling principle, as shown in Fig. 1.4. In plane TFETs based on nanoribbons [53–55] and bilayer graphene [44, 56] have shown promising performance for logic applications [Table 1.2], but GNR-TFETs suffer from low ON current problem and BLG-TFET requires very high gate voltage supplies. Out plane TFETs with graphene, such as vertical heterostructures [57], BiSFET [29] and SymFET [30], have also explored, which is based on tunneling through graphene-insulator-graphene junction, as shown in Fig. 1.4. These proposed structures are very suitable for digital applications with a higher ON/OFF current ratio, but they suffer from large parasitic capacitances, may severely degrade the performance metrics in real circuits. Moreover, experimental realization of these devices is very difficult with present semiconductor processing methods as they require extremely thin and high

TH-1608_11610201

quality dielectrics, high-quality graphene and low contact resistance. In summary, graphene is well suited for use in high-performance TFET because of ultra-body thickness, but many challenges exist for the experimental realization of graphene-based TFET.

Table 1.2: Performance of graphene-based TFET for digital applications.

Material	L_g (nm)	V_{DS} (nm)	I_{ON} ($\mu A/\mu m$)	I_{ON}/I_{OFF}	SS (mV/dec)	Remarks
GNR	40	0.2	225	6080	12	[27]
BLG	40	0.2	67	2910	35	[44, 56]
Vertical hetrostructure with GNR	–	1.5	$>10^4$	$600\text{-}10^{4\diamondsuit}$	<170	[58]

$\diamondsuit$: For device width of 5-1.3 nm;

1.4.2 Analog Electronics Applications

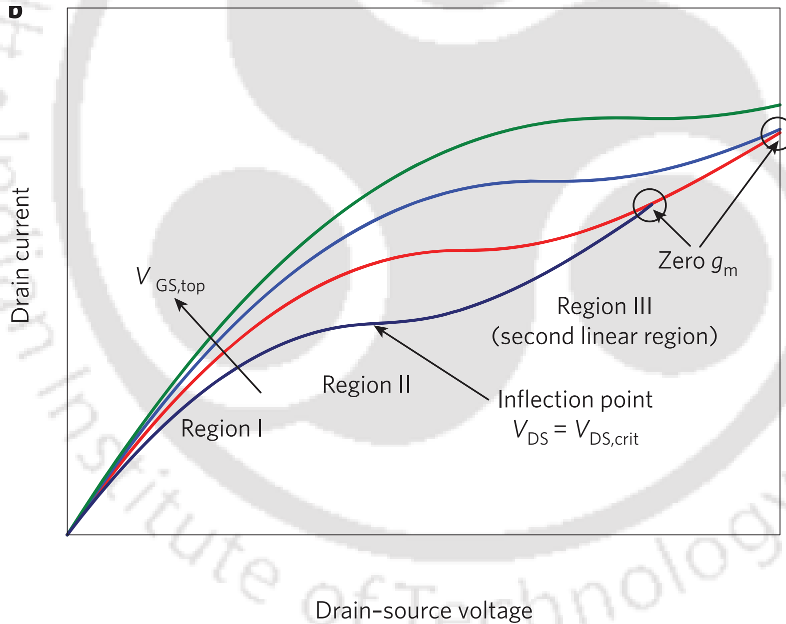


Fig. 1.5: Qualitative shape of the output characteristics of a large-area graphene MOSFET with an n-type graphene channel, for different values of the top gate voltage, $V_{GS,top}$. The very narrow saturation region can be seen for moderate value of drain-to-source volatges [1].

In contrast to digital electronics, graphene-based transistors have shown better performance for analog electronics. The high carrier mobility and high saturation velocity in graphene would allow high device transconductance (g_m) and high cutoff frequency (f_T) [59]. The first radio-frequency graphene transistors has been demonstrated by IBM Group that exhibits f_T equal to 26 GHz for channel length

TH-1608_11610201

of 150 nm after de-embedding the signal-ground pad parasitic [60]. Since then, the performance of high frequency graphene transistors has been quickly improved by using different substrates and fabrication methods [61–65]. So far, the highest f_T measured is about 1.4 THz for a gate length of 45-nm with self-aligned nanowire gate using exfoliated graphene [5]. Table 1.3 shows that the cutoff frequency of graphene transistor is higher than the maximum f_T measured in conventional Si MOSFET and III-V HEMTs, while the estimated f_{max} and A_{V0} in GFET are considerably smaller than that for short channel Si and InP MOSFETs. The reason for small f_{max} and A_{V0} is the weak current saturation or second linear region the output characteristics, as shown in Fig. 1.5. The weak saturation in long channel device has been attributed to velocity saturation [66,67], while their short channel counterparts has shown same behavior due to BTBT current [68, 69]. To achieve high A_{V0} and f_{max}, the output conductance (g_{ds}) should be minimized without degrading g_m value, and it can only be achieved by improving the current saturation without lowering current values in GFETs.

GNR-FETs are not very popular for RF applications due to low ON current that may degrade the cutoff frequency. The theoretical investigations done so far show that wide GNR-FETs have cutoff frequency at THz range, but the A_{V0} not very significant [70, 71]. Further, BLG-FET has found a promising device for high frequency applications. An experimental work on BLG-FET has demonstrated that an intrinsic gain of 35 dB is possible with the channel length of 2 μm [72], while theoretical works have reported an intrinsic gain of 20 dB with a cutoff frequency of 1.4 THz for 40 nm channel length [73, 74]. However, BLG-FET requires very high-voltage gate supplies, which is very difficult to attain in IC.

As conventional GFET suffers from weak current saturation, new device architecture can be explored. Although TFETs are particularly suitable for digital applications because of steeper subthreshold slope [79,80], some of the TFET architectures have shown promising RF performance metrics and they can be considered as a strong candidate for analog/RF applications [81, 82]. Early works on graphene based tunnel field effect transistors have particularly focused on the lateral and vertical heterostructures [30, 83]. These proposed structures are suitable for digital applications due to their high on/off ratio, but they are certainly not useful for analog/RF applications because of very narrow current saturation region and larger parasitic capacitances. The progress in fabricating high-performance RF GFETs has been very rapid during recent years and the prospect of using GFETs in embedded RF circuit, such as low-noise amplifier, mixers, frequency multipliers and resonator, is bright. Further-

TH-1608_11610201

Table 1.3: Performance comparison of graphene-based MOSFETs with Si MOSFET from analog/RF applications point of view.

Material	Device Type	L_g (nm)	g_m $(mS/\mu m)$	f_T (GHz)	f_{max} (GHz)	A_{V0}	Remarks
ITRS 2014	MOSFET	18	–	480	540	–	[75]
Silicon	MOSFET	29	1.3	485	–	20 dB	[76]
InP	–	<50	1.2	385	>1,100	15 dB	[77]
Graphene	Top-gate MOSFET	–	<2	1,400$^{\diamondsuit}$	42$^{\Theta}$	10 dB*	Experimental [5, 63]
Graphene	Doule-gated	20	0.8	>1,000	690	1 V/V	Simulation [68, 78]
BLG	Top-gated	40	8	1,500	3,000	20 dB	Simulation [73, 74]

$\diamondsuit$: For $L_g = 45$ nm; Θ: For $L_g = 140$ nm; $\star$: For $L_g = 300$ nm.

more, if f_{max} and A_{V0} can be improved without degrading f_T, its usage will extend to all RF circuity, including all power-sensitive blocks. In summary, the main challenge with graphene transistors for analog/RF applications is to improve the saturation behavior in their output characteristics without significantly degrading its current levels.

1.5 Modeling of Nanoscale Devices

The transport models as per their applicability and origin are categorized in Table 1.4. In the case of semi-classical formalism, the transport models for all limits are obtained from the simplification of Boltzmann transport equation (BTE) equation. In the classical limit, hydrodynamic, drift-diffusion and six moments equations are obtained from the moments of the Boltzmann transport equation (BTE), while BTE should be solved by the Monte Carlo method or the direct method to obtain the distribution function for quasi-ballistic channel description. These semiclassical models are usually developed by taking ensemble average of the particle motion, which are no longer capable of describing the carrier transport in nanoscale transistor. The transports in the nanoscale transistor are usually contributed by the quantum effects, such as 1) interference effects, 2) quantum mechanical tunneling, and 3) quantization in the inversion layer [84]. There are many quantum correction terms available to catch the essence of quantum behavior of electrons in the BTE equation, but the outcome of these models is very specific to particular condition and will not be able to capture the full quantum

TH-1608_11610201

transport effects [85]. For an example, the Wentzel-Kramer-Brillouin (WKB) approximation is widely used to incorporate tunneling through potential barriers of irregular shapes. The major drawback of this approximation is that it assumes well defined energy-momentum relation in device like the BTE does, whereas this is not true when the device lacks of translational symmetry in transport direction, especially at non-equilibrium condition.

Table 1.4: Classifications of transport models

Formalism	Classical limit	Quasi-ballistic limit	Ballistic limit
Semiclassical	-drift-diffusion -hydrodynamic -six moments equation	-MC* simulation -direct calculation	-analytic solution -moment equation
Quantum-Mechanical	-density-gradient -effective potential	-NEGF** -Winger function Pauli master equation	-ballistic NEGF -Schrödinger equation

∗: Monte-carlo;∗∗ Non-equilibrium Green's function.

The full quantum simulation can be developed by direct solving of Schrödinger equation self-consistently with Poisson equation. However, this approach is either poorly efficient from the computational point of view or only valid for idealized and simplified structures. A more efficient and simple way is to develop the quantum transport by solving the Schrodinger equation within non-equilibrium Green's function formalism (NEGF). The NEGF essentially solves Schrödinger equation with open boundary conditions and provides a sound basis for quantum-mechanical simulations that is needed for nanoscale devices. The NEGF is a very powerful technique to treat the quantum law of motion (tunneling and interface) by simply solving Green function and the dissipative scattering process by introducing Buttiker probes. Moreover, the computational time requirement for solving NEGF equation depends on the size of the device, rather than the whole system which is practically unsolvable.

The NEGF formalism was independently developed by Keldysh [86] and Kadanoff-Baym [87] to solve the non-equilibrium problems in statistical physics and it is based on the contour-ordered Green function, which was first introduced by Martin and Schwinger [88]. The NEGF approach is based on rigorous many body approach and is derived from the main assumptions: 1) a single particle approach and 2) a mean-field approximation. Therefore, NEGF approach cannot properly describe strongly correlated transport in the devices. NEGF theory has demonstrated its usefulness for simulating nanoscale transistors from conventional Si MOSFETs [89], MOSFETs with novel channel materials,

TH-1608_11610201

such as CNT [90], nanowire [91], graphene [92], molecular transistors [93], etc. The objective of NEGF is to get many several one-particle Green functions. In the steady-state condition, the governing equations for the retarded (G^r), lesser ($G^<$) and greater ($G^>$) Green's functions can be written [94] as

$$[E - H(r_1)]G^r(r_1, r_2; E) - \int dr\Sigma^r(r_1, r; E)G^r(r, r_2; E) = \delta(r_1 - r_2), \tag{1.5}$$

$$G^{>/<}(r_1, r_2; E) = \int dr \int dr' G^r(r_1, r; E)\Sigma^{>/<}G^a(r_2, r'; E), \tag{1.6}$$

where, H(r) is the single electron Hamiltonian, G^a is the advance Green's function, which is the Hermitian conjugate of retarded Green's function, $\Sigma^>$ and $\Sigma^<$ are the self-energy functions related to interactions. The main parameters of interest for transport is to obtain the retarded Green function from equation 1.5, which contains the information on the propagation of the electron wave function excited by the delta function source in space-time.

In the numerical solution, the matrix representation of the Green's functions is used. The discretization in real space basis is done by representing r_1 and r_2 with row and column indices of the matrices. The governing key equations describing non-equilibrium transport within a semiconductor device are presented in matrix form as follows

$$G^r(E) = [EI - H(E) - \Sigma(E)]^{-1}, \tag{1.7}$$

$$G^<(E) = G^r(E)\Sigma^<(E)G^a(E), \quad G^>(E) = G^r(E)\Sigma^>(E)G^a(E) \tag{1.8}$$

In these equations, $G^<$ and $G^>$ are correlation functions specifying electron and hole density spectra, respectively. $\Sigma^<$ and $\Sigma^>$ are the in-scattering and out-scattering self energies for electron and hole distribution functions. After the self-consistent solutions are obtained for the correlation functions, the electron and hole density spectrums, and the terminal current density spectrum can be evaluated as

$$n(r) = -i\int \frac{dE}{2\pi}G^<(E), \quad p(r) = i\int \frac{dE}{2\pi}G^>(E) \tag{1.9}$$

$$I_r(E) = \frac{q}{h}Trace[\Sigma(r, E)^< G(r, E)^> - \Sigma(r, E)^> G(r, E)^<] \tag{1.10}$$

Where, q is the elementary charge constant, and h is the Plank constant. In the ballistic simulation, both source and drain contacts are assumed to be in equilibrium state, but maintained at two different chemical potentials. The electron-electron interaction and electron defection from defects are incorporated by adding potential in the single electron Hamiltonian matrix, $H(r)$, while the interactions

TH-1608_11610201

between the contact reservoirs and the transport carrier system are measured by self-energy matrices ,Σ. On the other hand, in dissipative transport consideration, the carrier scattering are treated by introducing Büttiker probes in the channel region. The Büttiker probes are treated as reservoirs, Σ, similar to the source and drain. The chemical potential have to be computed self-consistently, to ensure that current at the scattering contacts is zero. On the other hand, the phonon-electron scattering is treated by Born approximation, and only the self-energies involving one phonon processes (absorption or emission) are included as higher order processes contribute less to the interaction.

Since the main purpose of this thesis is to make a reliable simulation framework for the nano-scale graphene-based FETs, NEGF formalism is used. As considered device has channel length smaller the electron mean free path and operated at low voltages, we are concentrating on the ballistic NEGF formalism in this work.

1.6 Problem Definition

Graphene has great potential as a new generation electronic device; however many technological challenges are still unsolved. As a molecular scale material, the intrinsic physical properties of graphene can be easily impacted by these material integration, device fabrication, and processing steps. There are many major challenges yet to be resolved before graphene can be successfully integrated into commercial devices, such as minimizing defect and impurity, lowering the graphene-metal contact resistance and reducing the parasitic effects. However, the rapid improvement in the material synthesis and device fabrication technology in the past few years has been a promising sign of the future, in which the ideal device can be realized. The current scope of this research is motivated by overcoming the challenges of ideal graphene device. The work in this thesis aims to address the following specific aspects of graphene transistors from a numerical modeling and applications aspects:

- Development of accurate and unified transport model for GFET, GNR-FETs, BLG-FET and BLGNR-FETs.
- Improvement of the current saturation without significantly degrading the current values for superior analog/RF performance.
- Investigation of the performance potential for novel bilayer graphene nanoribbon (BLGNR).

TH-1608_11610201

- Investigation of new device structure structure to improve the ON/OFF current ratio and the intrinsic gain.
- Investigation of device design parameters to achieve to best device performance.
- Investigation of graphene-based devices performance for digital circuit perspectives and comparison with existing devices.

1.7 Outline of Thesis

The thesis is organized into six chapters. The brief descriptions of each chapters are as follows.

Chapter 1 briefly describes about the motivation, problem definition, and the outline of the thesis.

Chapter 2 gives a brief brief summary of the NEGF simulation procedure for ballistic device. Firstly, NEGF treatment of the quantum transport for smooth edge GNR-FET and G-FET using a single 1-D tight-binding Hamiltonian matrix is presented. Subsequently, the differences in the transport equation for BLG-FET and BLGNR-FET is discussed. Finally, the developed transport models are verified with the previous simulation and experimental results.

Chapter 3 discusses the analysis of graphene tunnel FET (T-GFET) for analog/RF applications. It is mainly focused on the extraction of the intrinsic analog/RF performance metrics of T-GFET, in particular the intrinsic gain and cutoff frequency. Firstly, the saturation behavior in output characteristics of T-GFET is analyzed in detail. Then, the device parameters, such as gate oxide thickness, gate misalignment (drain underlap and drain overlap) and doping profile, are investigated systematically to engineer current saturation. Lastly, the analog performance metrics between G-FET and T-GFET are compared, and their dependence on the channel length is also presented.

Chapter 4 presents the performance analysis of BLGNR-FET structure with abrupt doped junctions for digital applications, while the electrostatically doped geometry is investigated for analog applications. Firstly, the important digital performance metrics of BLGNR-FET are analyzed for different widths and different bias voltages, and the results are compared with MLGNR-FET and BLG-FET transistors. Subsequently, the output characteristics of narrow and wide width BLGNR-FETs are studied in detail and the important device parameters are investigated to improve the analog performance. Furthermore, the gate voltage dependency of intrinsic current gain and intrinsic cutoff frequency has been discussed.

TH-1608_11610201

Chapter 5 presents the analysis and design of BLGNR-TFET for low voltage digital and high-frequency RF applications. It mainly focuses on the device physics and interplay of key device parameters, rather than estimation on the ultimate performance limits. Firstly, it presents the impact of device parameters and bias voltages on the transfer characteristics of narrow width BLGNR-TFET. Further, it presents the BLGNR-TFET performance metric from a circuit perspective, and compared the results with its counterpart MLGNR-TFET. Then, it discusses the output characteristics of two different width BLGNR-TFET devices and important analog performance metrics. Furthermore, RF figure of merits are investigated in the presence of external parasitics.

Chapter 6 mainly includes the conclusion of the current research and outlines a few directions for future work from a modeling prospective.

TH-1608_11610201

TH-1608_11610201

2

Quantum Transport in Ballistic Graphene-based Transistors

Indian Institute of Technology Guwahati

Contents

2.1	Introduction	22
2.2	NEGF Treatment of Quantum Transport	23
2.3	Ballistic Transport in Graphene-based Transistors	26
2.4	Results	35
2.5	Summary	44

TH-1608_11610201

2.1 Introduction

Due to unique band structure and excellent electronic properties, graphene and its counterparts, such as graphene nanoribbons (GNRs), bilayer graphene (BLG) and bilayer graphene nanoribbon (BLGNRs), are very promising materials for nanoelectronic applications. Graphene-based transistor has been developed rapidly and many details about the potential performance of these devices in real applications remain unclear. Especially, when the fabrication technology is in early stage of development for graphene, modeling can be a very powerful tool to: (i) estimate performance, (ii) compare their performance with CMOS devices, (iii) evaluate different device structures, (iv) check the feasible technology options, and (v) forecast process tolerance and defect related issues. The theoretical and simulation studies not only provide a fast and effective way to explore complex experimental design space, but also it provides important insights into the device physics and material aspects.

The operation and performance of device can be explored by simple analytical models and detailed numerical simulations. The analytical models for graphene and graphene-based MOSFETs have been developed by many groups [48, 95–99], and have become very useful for predicting the upper-limit performance. These models provide a qualitative understanding of device performance, but some of them have neglected quantum effects and some of them have missed important material properties. As the present device has channel length shorter than 30 nm and as graphene has long mean free path exceeding 1 μm [12, 100], the current is mostly contributed by ballistic electrons rather than scattering process. Therefore, nanoscale graphene-based devices need proper a TCAD (Technology Computer Aided Design) tool, which can take into account the ballistic transport, quantum confinement in the channel, and multidimensional tunneling combined with the essential physics of the respective material.

The full quantum simulation can be developed by directly solving Schrödinger equation self-consistently with Poisson equation. However, such approach is either poorly efficient from the computational point of view or only valid for idealized and simplified structures. The more efficient and simple way is to develop the quantum transport by solving the Schrodinger equation within non-equilibrium Green's function formalism (NEGF) [101]. The main and important parameter for efficient and accurate modeling of charge transport within NEGF is the Hamiltonian matrix that can be expressed in two possible ways: 1) real-space basis (atomistic basis) and 2) mode-space basis. The real-space basis easily fits to any kind of geometry, but it produces a matrix whose size is the total number of atoms, which is computationally intensive. On the other hand, the mode-space approach is developed by exploiting

TH-1608_11610201

energy subbands into convenient subset of the transverse modes as basis functions. The mode-space approach largely reduces the computational burden and is widely adapted with tight-binding Hamiltonian matrix for simulating nanoscale graphene FET (G-FET) [92, 102], GNR-FET [103, 104] and BLG-FET [52, 105].

While simulating the graphene and its counterparts, the Hamiltonian matrix will be varied from material to material, so will be the solutions of self-energy and NEGF equations. Therefore, in this work, the 1-D real space transport model with analytically defined transverse modes is developed that can be applied equally well to simulations of graphene and its counterparts. Firstly, the tight-binding Hamiltonian matrix proposed in [106] is simplified for armchair edged GNR-FETs. Then, the same transport model is extended for G-FET by changing transverse wave vector (k_y) values. With respected to [106], our approach provides simplified solution of self-energy matrices and retarded Green's function, which reduces the computational cost without compromising the accuracy. Further, BLG and BLGNR is expressed by the two single layer GNR Hamiltonian matrices, coupled by the hopping parameters corresponding to the overlaying atoms along the z direction. This allows to model BLGNR-FETs and BLG-FET by same transport equations as GNR-FETs and G-FET with only small modifications. The transport model for BLG-FET is same as in [105]; however, this approach helps to describe the electrical behavior of BLGNR-FET.

2.2 NEGF Treatment of Quantum Transport

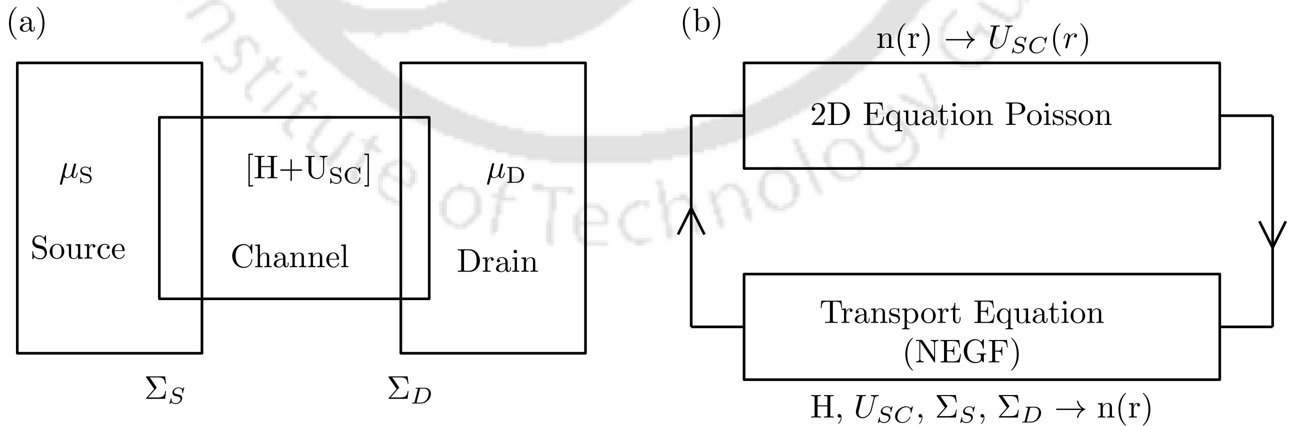


Fig. 2.1: Schematic of (a) device coupled with two contacts, and (b) self-consistent procedure for device modeling. Where, H is the device Hamiltonian and U_{SC} is the self-consistent potential of the device, Σ_S and Σ_D is the self-energy matrices for source and drain contacts, respectively, n(r) is the electron density, and I_{DS} is the drain-to-source current. The μ_S and μ_D are the contacts Fermi levels, which are equal at equilibrium and differ by qV amount when a V bias applied across contacts.

TH-1608_11610201

In this section, we give a brief summary of the NEGF simulation procedure for any ballistic device. The more detailed description of this technique can be found in [101, 107]. Fig. 2.1(a) shows the schematic of transistor with device channel connected with source and drain contacts. The device is described by the Hamiltonian matrix and self-consistent potential energy ($H + U_{SC}$), while the source and drain contacts are identified by their respective Fermi levels μ_S and μ_D. When V_S and V_D biases applied to the source and drain contacts, the Fermi levels are given as $\mu_S = E_f - qV_S \quad \mu_D = E_f - qV_D$, where E_f is the common Fermi energy in equilibrium. Fig. 2.1(b) shows the general concept of quantum transport simulation for ballistic device that is performed by self-consistent solving the transport equation and Poisson equation. The transport equation calculates the charge density, $n(r)$, and current, I_{DS}, while the Poisson equation calculates the effective potential inside the device due to electron-electron interaction and external perturbation.

In particular, the transport equation is widely solved through NEGF as it provides a simplistic way to incorporate complex structure and more efficient from computational point of view. For simulation through NEGF, the detail of device is accounted by same $[H + U_{SC}]$, but the coupling between the active device and the S/D contacts is described by the self-energy matrices, Σ_S/ Σ_D. Having gathered all the information (H, U_{SC}, Σ_S, Σ_D, μ_S and μ_D), the NEGF formalism provides clear and well defined relation that can be used to obtain the charge density and current. For more accurate analysis of transport in the device, it is necessary to self-consistently solve the charge distribution inside the device with corresponding electrostatic potential. The self-consistent potential energy includes the effect of the charge transfer into or out of the device form the source and the drain contacts as well as the effect of the electric field lines that penetrate into or inject out of the device from the gate contact.

Based on the discussion above, the overall simulation procedure through NEGF consists of following steps:

(i) The first step is to select an appropriate method from among the choices that are i.e., (i) to discretize all the operators, whether by finite-difference approach or finite-element approach, (ii) to describe the electron dynamic in the device, whether by effective mass approach or tight binding approach and (iii) to express matrices, whether by real-space or mode-space. We chose finite difference method for discretization, tight binding approach for electronic dynamic description, and real space approach for atomistic description of material.

(ii) The next and important step is to write down a suitable tight binding Hamiltonian matrix (H)

TH-1608_11610201

for a specific geometry that describes the bandstructure of device. If the Hamiltonian matrix size is the total number of atoms in the device, then the solution of the NEGF equations are computationally extensive. Therefore, it is important to identify an appropriate unit cell and a set of atomistic orbitals per atoms, which is adequate to describe the essential physics of material.

(iii) Having obtained an atomistic description of channel, the next step is to include the effect of source and drain contacts. The coupling of source and drain to the device is accounted by self-energy matrices (Σ_S and Σ_D), which basically describe the open boundary conditions for the Schrodinger equation. The self-energy involves the computation of surface Green's function, which is a computational demanding step, but a significant cost saving can be achieved by using Sancho-Rubio algorithm [108].

(iv) To begin the self-consistent procedure, an initial guess for self-consistent potential energy, $U_{SC}(\overrightarrow{r})$, is required. A better guess value may be obtained from a semiclassical solution of carrier statistics (e.g. ballistic BTE).

(v) After having all these information, the next task is to determine the retarded Green's function, $G^r(E)$, which describes the channel connection with contacts. This retarded Green's function can be used to obtain charge density, $n(r)$, on atomic sites.

(vi) Using charge density, a Poisson equation is solved to obtain the self-consistent potential profile of the device.

(vii) Step iii to Step vi are iterated until the difference in self-consistent potential energy is reached within a particular convergence criterion.

(viii) When convergence achieved, the current in the device can be computed by Launder formula [101].

The computationally extensive part of NEGF simulation is the solution of the retarded Green's function, which requires the inversion of a matrix for each energy grid point. In the ballistic limit, the computation burden is reduced because only a few columns of the Greens's function are needed for charge density computation. Nevertheless, reducing the size of the Hamiltonian matrix and developing computationally efficient approaches are of great importance for an atomistic simulation.

TH-1608_11610201

2.3 Ballistic Transport in Graphene-based Transistors

The aim of this thesis is to develop unified transport model for four graphene-based devices: (i) GNR-FETs, (ii) G-FET, (iii) BLGNR-FETs and (iv) BLG-FET. Our main focus is in the reduction of the computational effort in arriving at numerical convergence, so one can perform simulation in a reasonable amount of time for large-scale applications. The solution of NEGF equations are categorized into two groups. Firstly the NEGF equations are solved for GNR-FET and G-FET, then differences in these equations for BLGNR-FET and BLG-FET are presented. Lastly, the solution of Poisson's equation is discussed for 2-D MOSFET geometry.

2.3.1 NEGF Treatment of Electronic Transport in GNR-FETs and G-FET

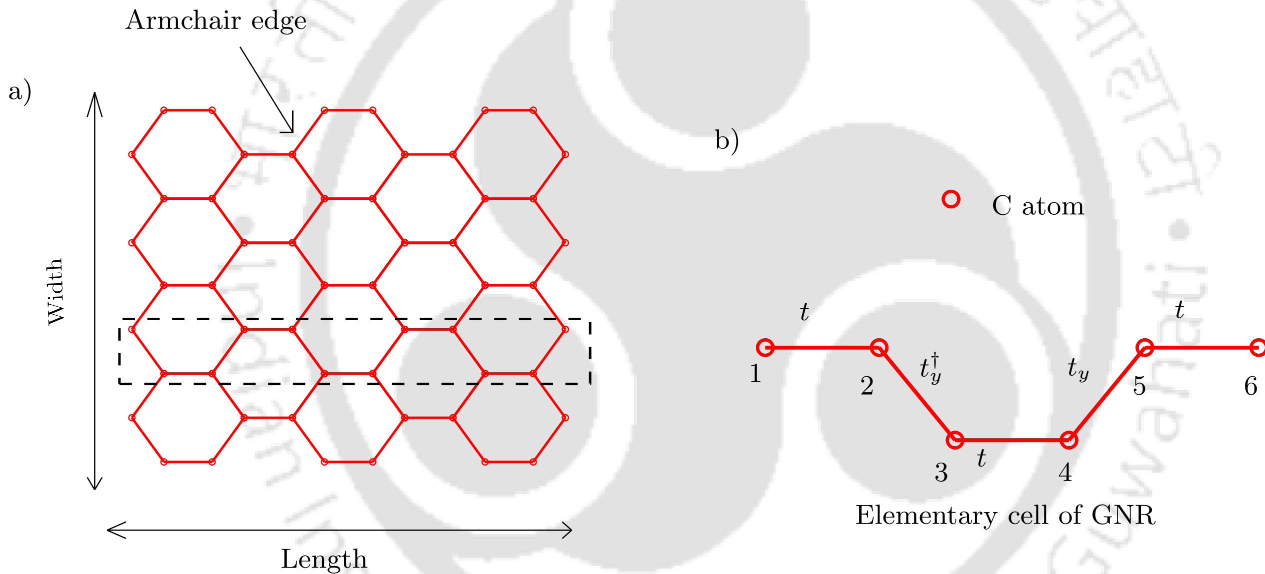


Fig. 2.2: Schematic of (a) N9 armchair edge GNR with the elementary cell (highlighted region), (b) 1-D unit cell with corresponding binding energy. Where, N denotes number of dimer lines or number of elementary cells along the width direction.

There are four orbitals in the outer electron shell of a carbon atom (s, p_x, p_y, and p_z). However, it has found that one p_z orbital per atom is sufficient for description of graphene bandstructure because the bands due to others orbital (s, p_x, p_y) are far from Fermi level and therefore not are significant for the electron transport. Fig. 2.2(a) shows the schematic of N=9 armchair edge GNR. To reduce the computation cost, we identify an elementary cell in GNR, which is repeating along the width, as shown by a box region in Fig. 2.2(a). In the graphene honeycomb lattice of carbon atoms, the charge transport can be described well by a simple nearest-neighbor tight binding model. Fig. 2.2(b) shows

TH-1608_11610201

the six atoms of elementary cell with nearest neighbor hopping energy. Low *et al.* has proposed the tight-binding Hamiltonian matrix for elementary cell with 2×2 coupling matrices [106]; however, their Hamiltonian matrix can be further simplified by using 1×1 coupling matrices. The Hamiltonian matrix with 1×1 coupling matrices from Fig. 2.2(b) can be constructed as

$$H(k_y) = \begin{bmatrix} [U_1] & [t] & & & & \\ [t] & [U_2] & [t_y^+] & & & \\ & [t_y] & [U_3] & [t] & & \\ & & [t] & [U_4] & [t_y] & \\ & & & [t_y^+] & [U_5] & [t] \\ & & & & [t] & [U_6] \end{bmatrix}_{N_x \times N_x} \tag{2.1}$$

Where, $U_i(x)$ is the self-consistent potential energy on the atomic sites, obtained from Poisson equation. The N_x is the total number of carbon atoms in the unit cell of device, t=2.7 eV is the nearest neighbor hopping between atoms on the same plan, and t_y is the nearest neighbor hoping between atoms on the different plan. The t_y is given as

$$t_y = t + te^{ik_y\Delta}$$

Where, $\Delta = \sqrt{3}a_{cc}$ is the lattice parameter, $a_{cc} = 1.42$ Å is the C-C bond distance and k_y is the transverse wave vector. In particular, the transport along the width is described in term of transverse modes and the k_y is used to define modes that is elaborated in last paragraph of this section.

Fig. 2.3: Schematic of 1-D elementary cell model of device having infinite contacts length.

The coupling of source and drain contacts to the device is described by source and drain self-energy matrices (Σ_S and Σ_D). Fig. 2.3 shows the elementary cell of entire device, where elementary cell are

TH-1608_11610201

divided into a left contact region (unit cells $0, -1, -2,...$), a channel region (unit cells $1, 2,...., \mathrm{M}-1, \mathrm{M}$) and a right contact region (unit cells $\mathrm{M}+1, \mathrm{M}+2,...$). It is observed that only the carbon atoms on the first and last rings of the device are coupled to the contacts. Thus, non-zero block for source self-energy matrix is the first 1×1 entry and drain self-energy matrix is the last 1×1 entry. The derivation of self-energy matrix is available in literature [101, 107]. Here, this concept is applied directly and the non-zero entries in the source and drain self-energy matrices is given as

$$\Sigma_S^{1,1}(k_y) = {t_y}^+ g_0 t_y \quad \Sigma_d^{N_x,N_x}(k_y) = t_y^+ g_{M+1} t_y \tag{2.2}$$

Where, g_0 and g_{M+1} are the surface Green's function for source and drain contacts. The surface Green's functions are the main elements required to solve equation 2.2. Due to strong periodicity of graphene lattice and small size of coupling matrices, the recursive algorithm can provide the close form solution for surface Green's functions. The recursive relation relates the surface Green's functions inside the source contact can be written as

$$\begin{aligned} g_0(k_y) &= \left[(E+i0^+)I - U_0 - tg_{-1}t\right]^{-1}, \\ g_{-1}(k_y) &= \left[(E+i0^+)I - U_{-1} - t_y g_{-2} t_y^+\right]^{-1}, \\ g_{-2}(k_y) &= \left[(E+i0^+)I - U_{-2} - tg_{-3}t\right]^{-1}, \\ g_{-3}(k_y) &= \left[(E+i0^+)I - U_{-3} - t_y^+ g_{-4} t_y\right]^{-1} \end{aligned} \tag{2.3}$$

The potential inside the source contact is constant, so $U_0 = U_{-1} = U_{-2} = U_{-3}$. Thus, $g_0 = g_{-2}$ and $g_{-1} = g_{-3}$ due to the periodicity of the graphene lattice. Using these relations, equation 2.3 can be represented in closed form as

$$g_0(k_y) = \frac{-(E-U_0)^2 + t^2 - t_y t_y^+ \pm \sqrt{\left[(E-U_0)^2 - t^2 - t_y t_y^+\right]^2 - 4(E-U_0)^2 \times t_y t_y^+}}{2(E-U_0) \times t_y t_y^+} \tag{2.4}$$

Similarly, the closed form solution can be obtained for drain surface Green's function. For elementary cell shown in Fig. 2.3, the surface Green's function for drain self-energy is same as computed in equation 2.4. Subsequently, the retarded Green's function, $G^r(E, k_y)$, in the ballistic limit can be calculated as

$$G^r(E, k_y) = [EI - H(k_y) - \Sigma_S(k_y) - \Sigma_D(k_y)]^{-1} \tag{2.5}$$

Where, E is the energy, I is the identity matrix. The straightforward way to compute $G^r(E, k_y)$ is by

TH-1608_11610201

inversion of matrix size $N_x \times N_x$, but it is a computationally expensive approach. Several methods have developed in the literature to reduce the computations exist with inversion of a full matrix, such as Recursive Green's Function algorithm [109], Contact Block Reduction (CBR) method [110] and Gauss Elimination (GE) method [111]. For the case of ballistic device, Gauss Elimination (GE) method is particularly efficient because only the few columns of $G^r(E, k_y)$ are needed. The column of interest in the $G^r(E, k_y)$ is determined by non-zero elements in the self-energy matrices. The local-density-of-states (LDOS) due to source and drain contacts can be obtained as

$$D_S = G\Gamma_S G^+ \quad \text{and} \quad D_D = G\Gamma_D G^+ \tag{2.6}$$

Where, $\Gamma_{\mathrm{S/D}} = i(\Sigma_{S/D} - \Sigma_{S/D}^+)$ is the energy level broadening by the source/drain contacts. In general, only diagonal entries of LDOS functions are important as they represent the density on the lattice sites. The non-zero energy in the $\Gamma_{\mathrm{S/D}}$ is the first and last elements, so the first and last column of retarded Green's function is important for LDOS computation. Therefore, the relevant columns from the Green's function is determined using Gauss elimination approach that can be given as

$$G_S = G(E, k_y)\backslash I_S \quad \text{and} \quad \mathrm{G_D = G(E, k_y)\backslash I_D} \tag{2.7}$$

Where, I_S and I_D are given by

$$I_S = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix}_{N_x} \quad \text{and} \quad \mathrm{I_D} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 1 \end{bmatrix}_{N_x} \tag{2.8}$$

Subsequently, the source and drain local density-of-states (LDOS) can be obtained from reduced Green's matrices as

$$D_S = G_S \Gamma_S^{1,1} G_S^+ \quad \text{and} \quad D_D = G_D \Gamma_D^{N_x, N_x} G_D^+ \tag{2.9}$$

The charge density on lattice sites is calculated as

$$Q(x) = (-q) \int_{-\infty}^{+\infty} dE \times \sum_{k_y} [\mathrm{D}_S(\mathrm{E, x, k_y}) \times \mathrm{f}_S(E) + \mathrm{D}_D(\mathrm{E, x, k_y}) \times \mathrm{f}_D(E)] \tag{2.10}$$

Where, q is the electron charge, and $\mathrm{f_{S/D}}(E)$ is the source/drain Fermi-Dirac distribution function

TH-1608_11610201

that given as $f_{S/D}(E) = 1/(1 + \exp((E - \mu_{S/D})/k_B T))$, k_B is the Boltzmann constant, T is the absolute temperature. This charge density is self-consistently solved with 2-D Poisson equation for a particular convergence criteria. When the convergence is achieved, the drain-to-source current density is computed as

$$I_{DS} = \frac{2q}{hW} \int dE \sum_{k_y} T_{k_y}(E)[f_S(E) - f_D(E)] \tag{2.11}$$

Where, h is the plank constant, W is the device width and the T is the transmission coefficient that can be computed as $T = \text{trace}\,[\Gamma_S D_D]$.

Coming to transverse wave vector (k_y), the geometry along the width is described by quantizing the transverse wave vector with appropriate boundary conditions. In case of GNR, the device width is finite and therefore Box boundary condition can justify the transport along the width. In particular, the armchair edge geometry has shown much better semiconducting properties than zig-zag edge geometry. Therefore, to define the arm-chair edge configuration, the k_y is quantized by imposing the box boundary condition in the Dirac equation [112] as

$$k_y = \frac{2\pi}{3\Delta} + \frac{2\pi p}{2W + \Delta} \pm \frac{2\pi}{3\Delta} \tag{2.12}$$

Where p is an integer and W denotes the bilayer ribbon width. The last term accounts the momentum of Dirac points, where positive/negative sign is employed when p is even/odd, respectively.

In the case of graphene, an atomistic arrangement is same as the GNR, but the width is much larger than the channel length. Therefore, a periodic boundary condition can justify the transport along the width. The Hamiltonian matrix of GNR is fitted well for bulk graphene, but k_y values is obtained by imposing Bloch periodic boundary condition with period equal to $\Delta = \sqrt{3}a_{cc}$. The k_y is quantized as

$$k_y = \frac{2\pi v}{\Delta_y}, \text{and} v = \pm 1, \pm 2, \pm 3 ... \pm n. \tag{2.13}$$

A significant computational saving can be achieved by defining k_y in a limited region of the Brillouin zone. It is found that the k_y values near to dirac point, $k_F = 2\pi/3\Delta$, are significant to reproduce bandstructure of graphene. In this work, the simulation is performed on 64 equidistant points for an interval suggested by Fiori in NANOTCAD Vides tool [92]. The computation of NEGF equations for G-FET remains the same as for GNR-FET case. Instead of a finite channel width, the device is infinite here, so that sums over modes are replaced by integrals over the transverse wave vector. Thus, the

TH-1608_11610201

charge density for G-FET can be obtained as

$$Q(x) = (-q)\int_{BZ} dk_y \int_{-\infty}^{+\infty} dE \times [\mathrm{D}_S(\mathrm{E,x,k_y})\times \mathrm{f}_S(E) + \mathrm{D}_D(\mathrm{E,x,k_y}) \times \mathrm{f}_D(E)] \tag{2.14}$$

Similarly, the drain-to-source current density for G-FET can be computed as

$$I_{DS} = \frac{2q}{hW}\int_{BZ} dk_y \int dE \times T_{k_y}(E)[f_S(E) - f_D(E)] \tag{2.15}$$

Our approach essentially translates 2-D graphene and GNR domian into several decoupled 1-D real-space lattice. The 1-D assumption is suited well for G-FET, while, for GNR-FET, this assumption is limited to the smooth edge case. Further, transport model of GNR-FET can be improved to take into account of edge bond relaxation and mode coupling for more realistic simulation. Subsequently, the NEGF equations are solved for BLGNR-FET and BLG-FET. In the following section, we present only, the differences in the NEGF equations, though entire model is developed for GNR-FET.

2.3.2 NEGF Treatment of Electronic Transport in BLG-FET and BLGNR-FET

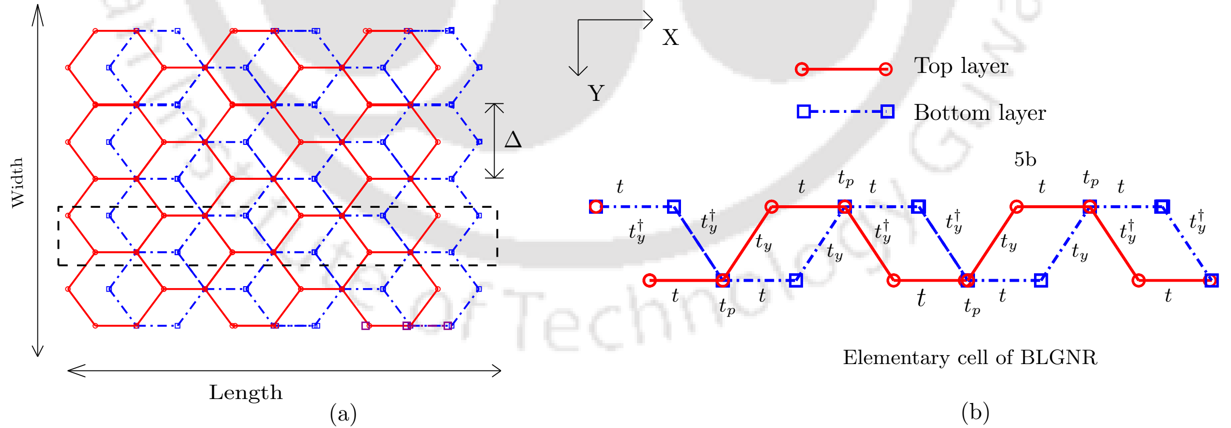


Fig. 2.4: Schematic of (a) N=9 (W4) armchair edge BLGNR, where top and bottom layers represent by solid and dash lines, respectively, and (b) 1-D elementary cell with binding energy.

Fig. 2.4(a) shows the schematic of n=9 armchair edge bilayer graphene nanoribbon (BLGNR). The considered BLGNR is composed of two A-B stacking of armchair edged GNRs. Similar to GNR, we identify the elementary cell, as highlighted in Fig. 2.4(b). The elementary cell of BLGNR consists of

TH-1608_11610201

two GNR elementary cells with the coupling in correspondence of overlaying atoms in the Z-direction. Therefore, Hamiltonian matrix of BLGNR can be expressed by adding hopping parameter $t_p = 0.35$ eV to the two GNR Hamiltonian matrices. Fig. 2.4(b) shows the elementary cell with the nearest neighbor hopping and Hamiltonian matrix from that can be constructed [105] as

$$H(k_y) = \begin{bmatrix} \alpha_1 & \beta_1 & & & & \\ \beta_1 & \alpha_2 & \beta_2 & & & \\ & \beta_2^+ & \alpha_3 & \beta_1 & & \\ & & \beta_1 & \alpha_4 & \beta_3 & \\ & & & \beta_3^+ & \alpha_5 & \beta_1 \\ & & & & \beta_1 & \alpha_6 \end{bmatrix}_{N_x \times N_x} \tag{2.16}$$

Where, N_x is the number of carbon atoms in the unit cell of BLGNR, α is the on-site coupling matrix, and $\beta_1, \beta_2, \beta_3$ are the coupling matrices between nearest neighbor carbon atoms. The coupling matrices are computed as

$$\begin{aligned} \alpha_i &= \begin{bmatrix} U_{ib} & 0 \\ 0 & U_{it} \end{bmatrix}, \qquad \beta_1 = \begin{bmatrix} t & 0 \\ 0 & t \end{bmatrix}, \\ \beta_2 &= \begin{bmatrix} t_y^+ & 0 \\ t_p & t_y \end{bmatrix} \quad and \quad \beta_3 = \begin{bmatrix} t_y & 0 \\ t_p & t_y^+ \end{bmatrix} \end{aligned} \tag{2.17}$$

Where, U_{ib} and U_{it} are the self-consistent potential energy on the bottom and top atomic sites, respectively. Due to weak periodicity of BLGNR lattice and 2×2 size of coupling matrices, the computation of surface Green's function using recursive algorithm is computationally intensive. Thereby, the surface Green's function for source and drain contacts are computed using the Sancho-Rubio iteration algorithm. The derivation of this algorithm for BLGNR is described in detail in Appendix A. Because the non-zero entry in self energy matrices is 2×2, first two and the last two columns of retarded Green's function are only required for calculating charge density and current at the ballistic limit. The relevant columns of the Green's function can be determined using Gauss elimination approach as

$$G_S = G(E, k_y) \backslash I_S \quad \text{and} \quad \mathrm{G_D = G(E, k_y) \backslash I_D} \tag{2.18}$$

TH-1608_11610201

Where, I_S and I_D are given by

$$I_S = \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}_{N_x \times 2} \quad \text{and} \quad \mathrm{I_D} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 1 & 0 \\ 0 & 1 \end{bmatrix}_{N_x \times 2} \tag{2.19}$$

The charge density and current from reduced Green's function matrices can be computed same way as discussed for case of GNR-FET. This 1-D assumption is suited well for bilayer ribbon with hydrogen passivated edges, as the electron-electron interaction at the edges of layers diminishes the edge bond relaxation [113].

BLG is basically composed of two A-B (Bernal) stacking of graphene sheet. Similar to GNR and graphene case, an atomistic arrangement in BLG is same as the BLGNR, but the width is much larger than the channel length. Thus, BLG-FET can be modeled by using the Hamiltonian matrix of BLGNR, but the k_y of G-FET is needed. Further, the charge and current densities can be computed as the same way as done for G-FET. This consideration of 1-D transport in BLG based transistors reduces the computation time, but when solving integral along the k_y, in which we preferred 64 k values, computation is still very demanding. The 1-D transport model of BLG-FET is the same as one developed by Fiori and Iannaccone [105]. The only difference is that the transport equations are modeled by solving NEGF, rather than directly solving Schrödinger equation in [105]. On the other hand, this 1-D transport assumption has proven to be useful in understanding operations of BLGNR-FETs, which is not yet available in the literature.

2.3.3 2-D Electrostatics

Appropriate treatment of electrostatic is necessary for accurately analyzing the device characteristics. For a given charge density, the Poisson equation is solved to obtain the electrostatic potential profile in the devices. Next, this computed potential profile is used as the input for the NEGF transport equation, and an improved estimate for the charge density is obtained. Since 1-D transport assumption in graphene-based devices limits the charge density and potential to constant values along the device width (y-axis), the Poisson equation is essentially became a 2-D problem along the length (x-axis) and the height of the device (z-axis). The Poisson equation for 2-D geometry shown in Fig. 2.5 can be

TH-1608_11610201

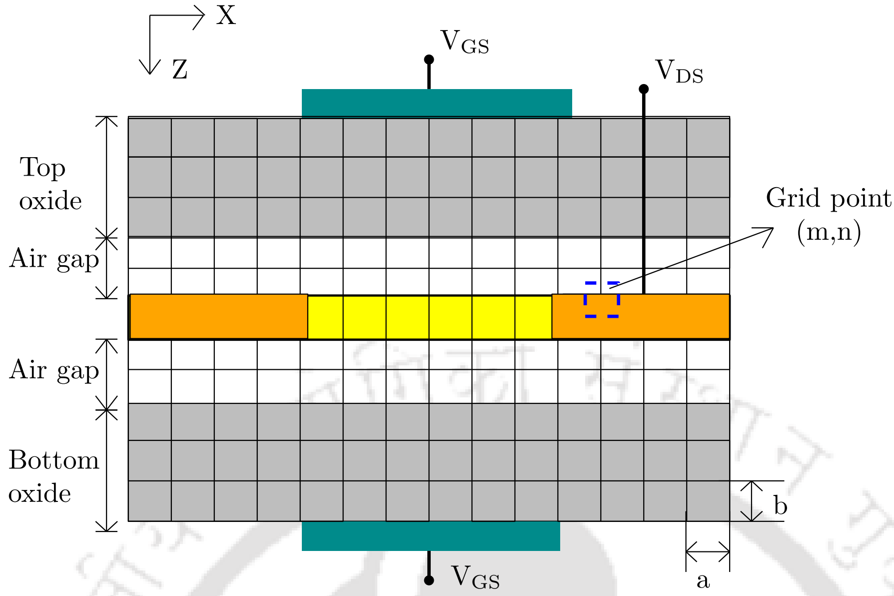


Fig. 2.5: 2D Simulation domain of double gate MOSFET. The channel is intrinsic and the gate length equals the channel length. The source and drain are the extension of channel and doped heavily. The dashed rectangular shows the element used to discretize the Poisson equation at (m,n). Uniformly spaced grids are used in both x and z directions, spatial constants are a and b respectively. An air spacer of 0.5 nm is assumed between the plane connecting the centers of carbon atoms and the interface of the oxide region to perform atomistic simulation.

written as

$$\nabla.[\varepsilon \nabla U_{SC}(x,z)] = qQ(x) \tag{2.20}$$

Where, ε is the dielectric constant, q is the charge of electron and Q(x) is the charge density on the graphene surface that can be given as.

$$Q(x) = (p - n + N_D - N_A) \tag{2.21}$$

Where, p/n is the holes/electrons concentrations, respectively, and N_D/N_A is the donors/aceptors concentrations, respectively. The derivative function of Poisson equation is discretized at the internal nodes using forward difference approximation. The discretized equation for an element at the grid point (m,n) in graphene and dielectric interface can be written as

$$\begin{split}\left(\frac{\varepsilon_{gr}+\varepsilon_{ins}}{2}\right)\left(\frac{b}{a}\right)(U_{m+1,n}+U_{m-1,n}) - 2\left(\frac{\varepsilon_{gr}+\varepsilon_{ins}}{2}\right)\left(\frac{b}{a}+\frac{a}{b}\right)U_{m,n} + (\varepsilon_{ins})\left(\frac{a}{b}\right)U_{m,n+1} \\ + (\varepsilon_{gr})\left(\frac{a}{b}\right)U_{m,n-1} = ab \times Q(x)\end{split} \tag{2.22}$$

TH-1608_11610201

Where, a and b are mesh spacings in the x and z directions, ε_{gr} is the dielectric constant of graphene and ε_{ins} is the dielectric constant of insulator. For the grid points on the graphene/insulator, the graphene/insulator surface, $\varepsilon_{gr}/\varepsilon_{ins}$ is replaced with $\varepsilon_{ins}/\varepsilon_{gr}$ in equation 2.22.

We now look the Poisson equation at the boundary nodes. For the nodes on boundaries with constant potential, the Dirichlet boundary conditions are imposed, whereas for other node boundaries, the Neumann boundary conditions are considered. At the gate contacts, the Dirichlet boundary conditions are imposed, which means U= -qV_G. The gate vacuum potential V_G is determined from the gate bias voltage and work-function difference between gate metal and graphene. The Neumann boundary conditions are considered by assuming the zero electric field in the direction normal to the boundary, $\vec{n}.\vec{\nabla}U = 0$. At the corner nodes, the same zero boundary condition is set [114].

Equation 2.22 is linear and easier to solve, but convergence of this equation is very poor, when the charge density from NEGF is inserted. To improve the convergence, a nonlinear inner loop, which takes quantum charge density and converts this charge into a quasi-Fermi level through a dummy function, is used. This nonlinear inner loop provides damping mechanism to update the potential energy, which helps to avoid larger change in the potential energy in successive iterations and therefore making coupled equation to converge efficiently and stably. The dummy function should be very close to the physical relation determined by carrier transport equation as possible for better convergence. Typically, semiclassical equilibrium carrier statistics with a dummy quasi-Fermi level are used as the dummy function [115]. The carrier statistics are used for simulating the all the four devices presented in Appendix B. Since the resulting Poisson equation is nonlinear, it is solved by an inner Newton-Raphson loop [114]. The Newton-Raphson approach provides quadratic convergence that will result in smaller the number of iterations.

2.4 Results

The purpose of this section is to show by some simple examples that the developed transport models are valid. The transport model for GNR-FET is verified by comparing simulation results with Low's approach [106] and Zhao's RS/MS approach [103], while the transport model for graphene-FET (G-FET) is only verified with Low's et al. approach [106]. Further, the transport model for BLGNR-FETs is verified by comparing the energy gap openings with previously reported theoretical works for BLGNRs [4, 47]. In the case of BLG-FET, Hamiltonian matrix and k_y are the same as developed

TH-1608_11610201

by Fiori and Iannaccone [52, 105]. The only difference with [52, 105] is that our simulation solves NEGF equation instead of direct Schrödinger equation and it would not make big difference in results. However, the energy gap opening with the gate voltage in BLG-FET is presented for understanding transport properties.

To simulate devices, the double gate geometry depicted in Fig. 2.5 is used. The channel is intrinsic with a length of 20 nm. The source and the drain regions are 20 nm long and doped to n-type with a molar fraction of $f_d = 5 \times 10^{-3}$. The SiO_2 having a dielectric constant of 3.9 and thickness of 1.5 nm is considered as top and bottom gate dielectrics.

2.4.1 Simulation of GNR-FET

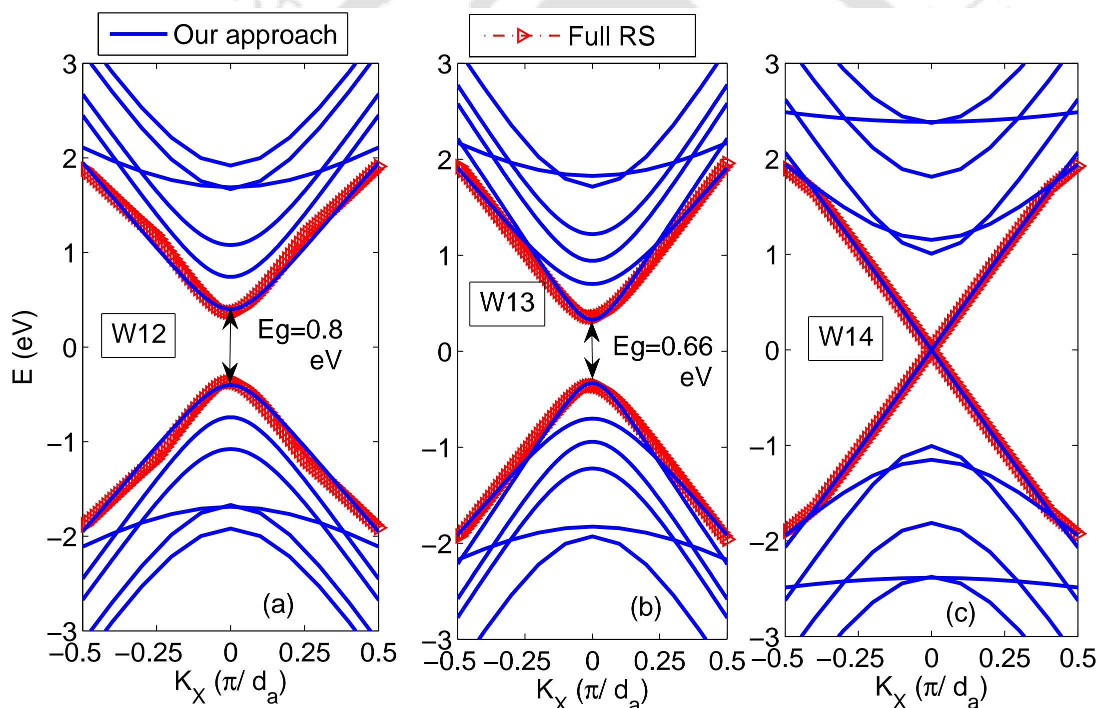


Fig. 2.6: Bandstructure of A-GNR as a function of k vector obtained from our calculations (solid lines) and from real-space approach (red triangles) [2] for (a) W12 (3p), (b) W13 (3p+1) and (c) W14 (3p+2) widths, where p is the integer and W12, W13 and W14 represent the widths of 1.46 nm, 1.62 and 1.74 nm. Where d_a=$3a_c$ is the 1-D unit cell distance along length.

In this work, GNR is classified using 1-D unit cell along the width direction. For examples, W12, W13, and W14 represent the numbers of elementary cells along width with ribbon widths of 1.46 nm, 1.62 and 1.74 nm, respectively. To show the difference in the three class of armchair edged GNRs (A-GNRs), we have computed the bandstructure from 1-D tight-binding Hamiltonian by using eigen states algorithm in [116]. Fig. 2.6 shows the conduction and valence subbands pairs for W12, W13,

TH-1608_11610201

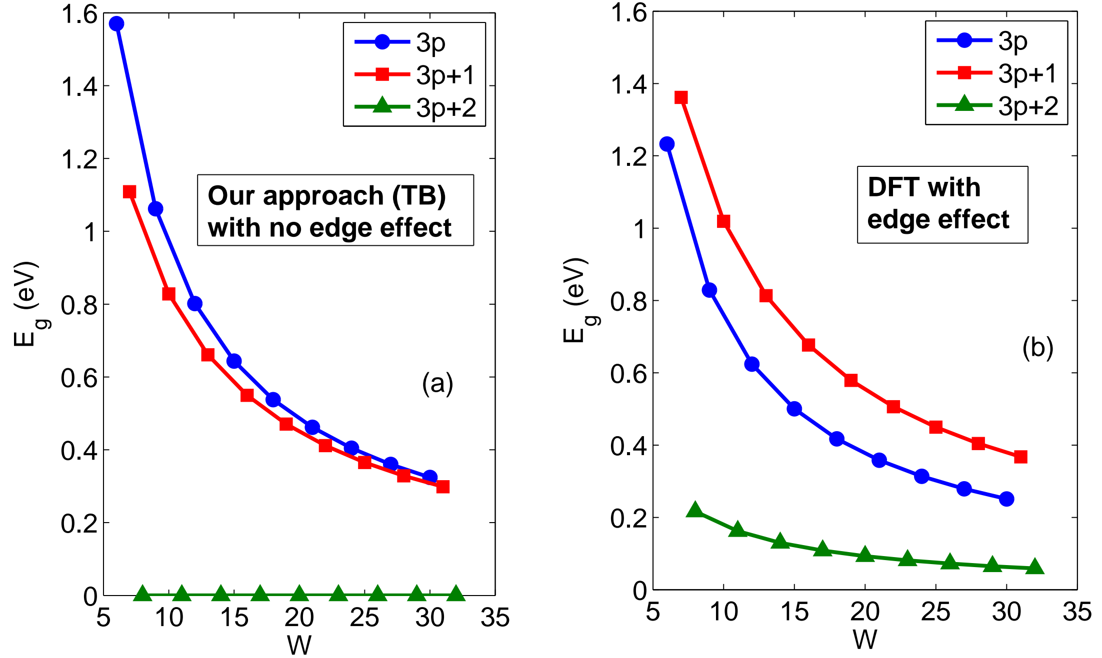


Fig. 2.7: The variation of band gaps of A-GNRs as a function of width obtained (a) from our approach and (b) from DFT approach [3]. Our results are not matching with DFT results because the edge bond relaxation is not considered in simulation.

and W14 A-GNRs, from our approach and real-space approach [2]. Further, the bandgap as a function of ribbon widths is shown in Fig. 2.7. Fig. 2.6 shows that the energy gap is strongly dependent on the number of elementary cells along the width. The W14 (3p+2) ribbon is shown semi-metallic behavior, whereas the energy gap in W12 (3p) A-GNR is higher than that of W13 (3p+1) A-GNR, where p is an integer. It is observed that our 1-D real-space approach gives an almost exact reproduction of the conduction and valence minima with the full real-space approach. It is observed from Fig. 2.7(a) that the energy gaps are closely related for 3p and 3p+1 classes of A-GNRs. This energy dependency on ribbon widths are in good agreement with reported full real-space tight-binding [2] and first-principle (DFT) [3, 112] calculations for smooth edge ribbons.

Since A-GNRs are geometrically terminated single graphene layers, their electronic structures are crucially influenced by edge configurations. In particular, the hydrogen atoms are used to terminate dangling bonds that results in about 12% increase of the binding energy between carbon atoms at the edges. In Fig. 2.7(b), we show the energy gap of A-GNRs with the presence of edge bond relaxation from DFT calculation [3]. When the edge bond relaxation is considered, there are no metallic nanoribbons and furthermore, the energy gaps are well separated into three different groups.

TH-1608_11610201

It is observed by comparing Fig. 2.7(a) and (b) that the energy gap opening from our approach are not agreed with DFT results. For 3p class A-GNR, our energy gap is higher than that DFT approach, while, for 3p+1 and 3p+2 classes of A-GNR, our energy gap is smaller than DFT results. The reason is that the edge bond relaxation is not considered in our simulation.

We find that it is very difficult to include the edge bond relaxation in our case as the Hamiltonian matrix is formulated by translating 2-D geometry into the 1-D cell to reduce computational time for quantum simulation. The reported work with edge bond relaxation are either based on full real-space approach [2,103,117] or full mode space approach [103], but we have simplified 1-D real-space approach for Hamiltonian construction to develop unified transport model for graphene sheet and nanoribbon devices. Therefore, the incorporation of edge bond relaxation is still challenging task in our simulation of nanoribbon devices.

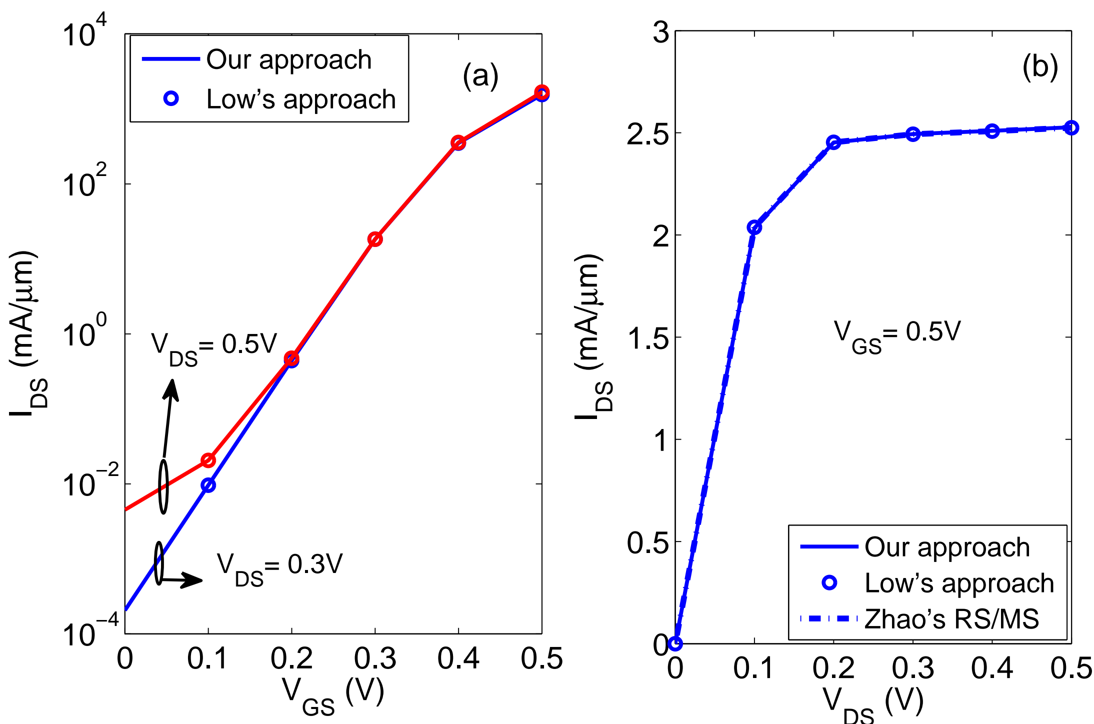


Fig. 2.8: (a) Transfer characteristics of W12 AGNR-FET from our approach (solid lines) and Low's approach (circles). (b) Output characteristics of AGNR-FET from our approach (solid line), Low's approach (circles) and Zhao's real-space/mode space approach (dash line), at $V_{GS} = 0.5$ V.

Fig. 2.8(a) compared the transfer characteristics of AGNR-FET from our approach and Low's approach. It is observed that two methods give nearly identical results for all bias voltages. It is also become important to compare our 1-D real-space transport assumption with full real-space and mode-

TH-1608_11610201

space results. To ease the comparison, we have benchmarked device with smooth edge W12 AGNR-FET proposed by Zhao and Guo [103]. This geometry is very similar to our simulation geometry, expect that the channel, source and drain lengths are scaled to 10 nm. Fig. 2.8(b) shows the output characteristics of W12 AGNR-FET from our approach, Low's approach [106] and Zhao's real-space/mode space approach, at $V_{GS} = 0.5$ V. It is observed that our approach excellently reproduces the results both from Zhao's real-space/mode-space results. The good agreement between our approach and real-space approach results from the constant potential around the width.

2.4.2 Simulation of G-FET

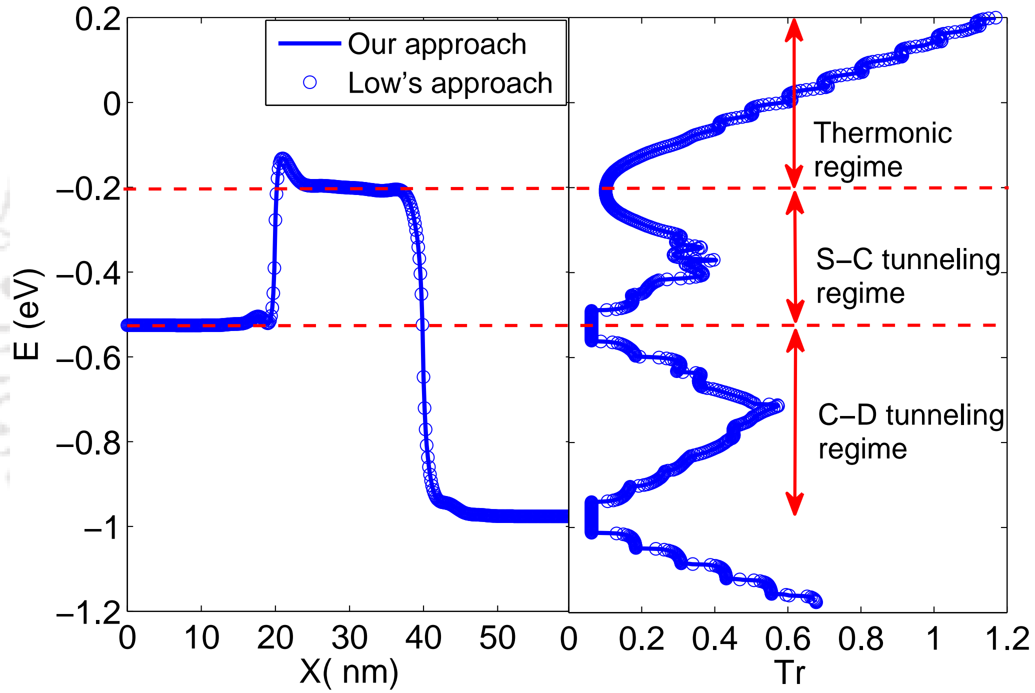


Fig. 2.9: Potential profile (left) and corresponding current spectra (right) of G-FET at $V_{GS} = -0.1$ V and $V_{DS} = 0.5$ V from our approach (solid lines) and Low's approach (circles).

Fig. 2.9 shows the device potential profile and corresponding transmission spectra of G-FET from our approach and Low's approach at $V_{GS} = -0.1$ V and $V_{DS} = 0.5$ V. It is observed that our approach agrees well with Low's approach [106]. Fig. 2.9(b) shows that the transport regime at OFF-state is the sum of three contributions: I is the thermionic current regime, II is source-channel the chiral band to band tunneling current regime (S-C chiral BTBT) and III is the drain-channel band to band tunneling (C-D BTBT) current regime. These tunneling regimes play an important role in the electrical characteristics of G-FET. The transmission is non-zero for all energies which indicates that the energy

TH-1608_11610201

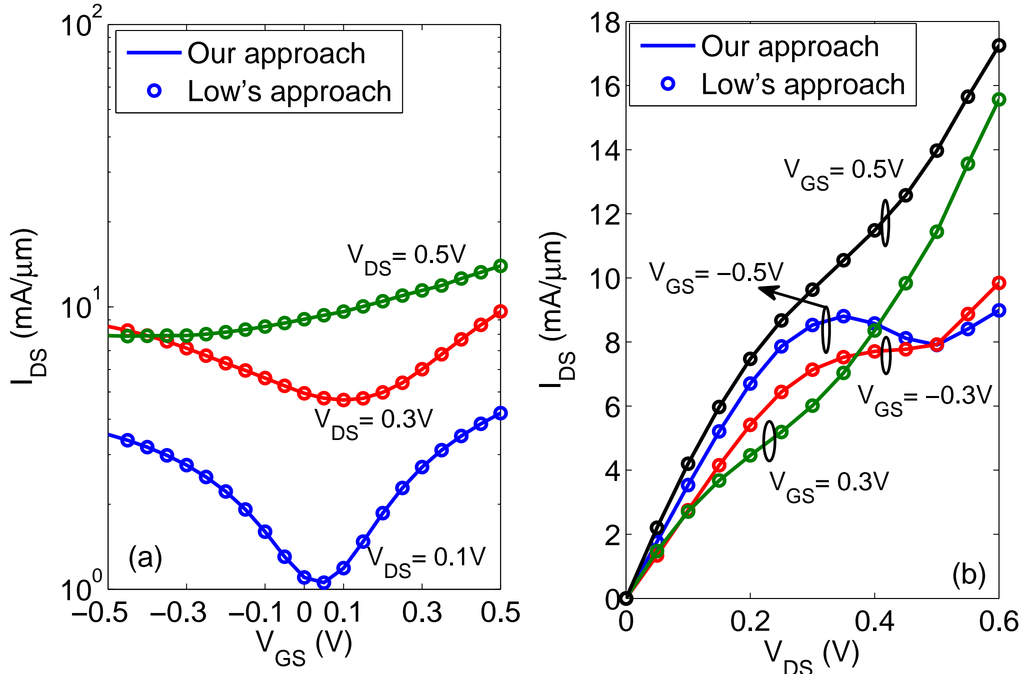


Fig. 2.10: Transfer and output characteristics of G-FET from our approach (solid lines) and Low's approach (circles).

gap is zero, but there are transmission valleys, which separates the regimes in the transmission spectra. The transmission valley is a consequence of the k_y-dependent pseudo-energy gap due to the influence of electron states on both sides of the gated region. The deepness of the transmission valley is dependent on the gate length. This current regimes and pseudo-energy gap are in good agreement with transport model based on Fourier transform of operators by Alacron et al. [118].

The accuracy of our approach is tested under different conditions. The transfer characteristics and the output characteristics of G-FET are compared with Low's approach, as shown in Fig. 2.10. It can be noticed that the our approach agrees well Low's approach for all bias voltages. The ambipolar behavior is observed in transfer characteristics and the $\max(I_{DS})/\min(I_{DS})$ ratio for graphene FET is about 3-6. In output characteristics, the quasi linear behavior is appeared for positive V_{GS} values, while negative differential resistance (NDR) is exhibited for negative V_{GS} values. This behaviors in the output characteristics are matched well with other simulation studies for short channel graphene-FET [68, 119, 120], while the agreement with experiments [66, 121] is only qualitative due to the gap between the conditions considered in the simulation (20-nm channel length and ballistic transport in ideal graphene) and the limitations of the present graphene technology (e.g., contact resistance and

TH-1608_11610201

interface effects). The above investigations show that the parameters and assumptions considered in this simulation are acceptable.

Table 2.1: Minimum error criterion of current calculation and the total simulation time for our approach and Low's approach. The simulation time is included the Poisson equation solving, when $V_{GS} = 0.5$ V and V_{DS} increases from 0 to 0.5 V by 0.05 V per step (shown in Fig. 2.8). The simulation were run on a four core 3.2 GHz CPU using parfor loop in MATLAB.

	Low's approach	Our approach
Error Criterion	$>$0.001	$>$0.001
Simulation time for W12 GNR-FET	13.62 mins	2.13 mins
Simulation time for G-FET	150.6 mins	19.03 mins

To see the advantages of our approach, Table 2.1 compare the computed simulation time for charge and current calculation, when $V_{GS} = 0.5$ V and V_{DS} increases from 0 to 0.5 V by 0.05 V per step (shown in Fig. 2.8) with Low's approach. The comparison shows that our approach reduces the computational time by about one order of magnitude for both GNR-FET and G-FET. Using proposed approach, one can perform simulations in a reasonable amount of time, which is essential for large-scale applications and device optimizations. Our approach is highly advantageous in reducing the computational burden, and it is valid when the potential variation around the ribbon is much smaller and subbands are uncoupled.

2.4.3 Simulation of BLGNR-FET

Similar to GNR, BLGNR is also classified using 1-D unit cell along the width direction. The W12, W13, and W14 represent bilayer ribbon widths of 1.46 nm, 1.62 and 1.74 nm, respectively. Fig. 2.11 shows the confinement induced energy gap of three different armchair edged BLGNR widths. It is observed, by comparing Fig. 2.6 and Fig. 2.11, that the confinement-induced energy gap in BLGNRs is considerably smaller than that of GNRs because of the interlayer coupling. However, BLGNRs offer more low energy bands than GNRs for the same width due to their small effective mass. The more low energy bands promise the better ON current with BLGNR devices.

Fig. 2.12 shows energy gaps of armchair BLGNRs as a function of width obtained from our 1-D real-space calculation and DFT calculation with edge effect [4,113]. It is observed that the energy gap for smooth edged A-BLGNR is agreed with DFT results with the edge effects for width is over W18 (2.4 nm). The reason for that there exists an electron-electron interaction between the layers at the

TH-1608_11610201

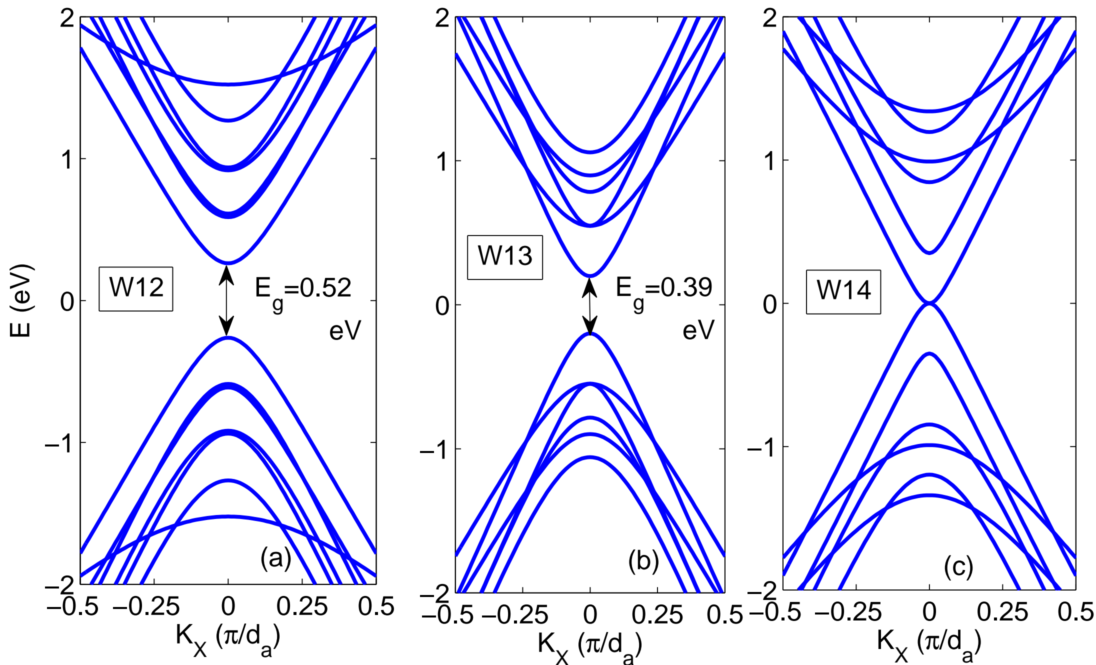


Fig. 2.11: Bandstructure of BLGNR as a function of k vector for (a) W12 (3p), (b) W13 (3p+1) and (c) W14 (3p+2) widths, where p is an integer and W12, W13 and W14 represent ribbon widths of 1.46 nm, 1.62 and 1.74 nm, respectively. Where d_a=$3a_c$ is the 1-D unit cell distance along length.

edges that diminish the edge effects as compared to single layer GNR narrow widths. However, the difference in energy gap between our approach and DFT calculation is smaller as compared to single layer GNR for width smaller than W18. Therefore, our simulation study for BLGNR-FETs can be closed to a real device.

Fig. 2.13 shows the energy gap opening with differential gate voltages ($V_{diff} = V_{GS2} - V_{GS1}$) for W30 (3.74 nm) and W15 (1.87 nm) BLGNR devices. It is observed from Fig.2.13 that the energy gap for wide bilayer ribbon is consistently increased with increasing the gate electric field, while the energy gap for narrow bilayer ribbon is first decreased and then increased. Previous theoretical works have found a critical energy gap of around 0.21 eV [4, 47, 48]. For bilayer ribbon width having the energy gap above/below the critical value, the vertical electric field decreases/increases the energy gap, respectively. Our results follow similar electric field dependency with respect to the critical energy gap. It shows that the parameters and edge approximation considered in this simulation are acceptable. Therefore, the energy gap is determined by confinement in narrow BLGNR width and by the gate voltage in wide BLGNR width.

TH-1608_11610201

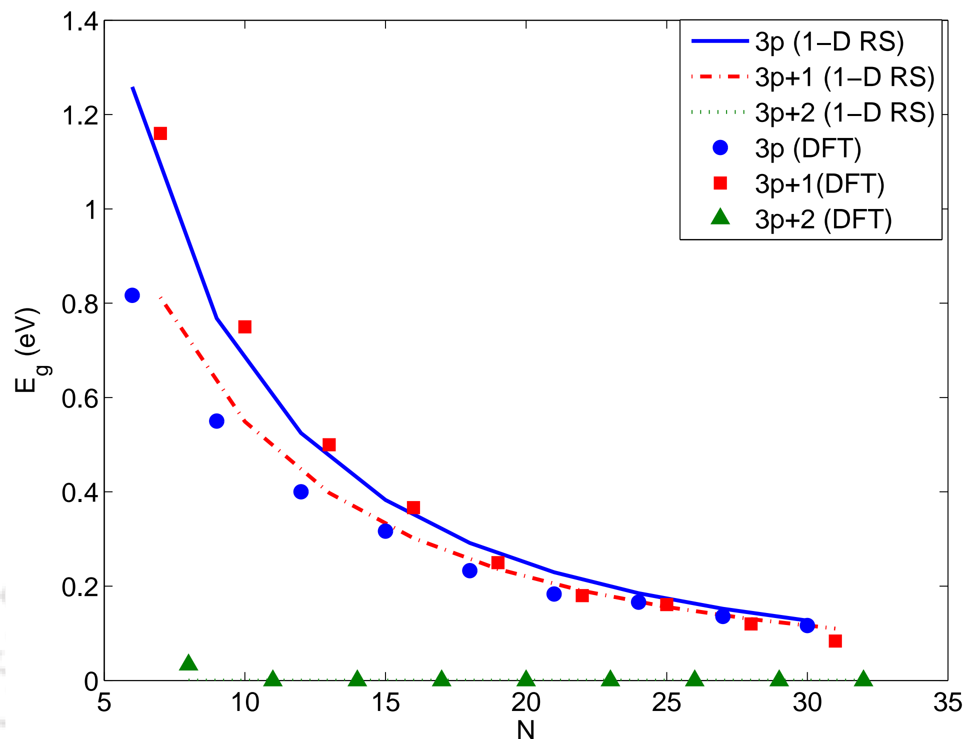


Fig. 2.12: The variation of band gaps of Armchair BLGNRs as a function of width obtained from (lines) our calculations based on 1-D RS and from (dots) DFT approach with edge effects [4]. For narrow widths, the edge effects become significant that cause deviation in our results with DFT data.

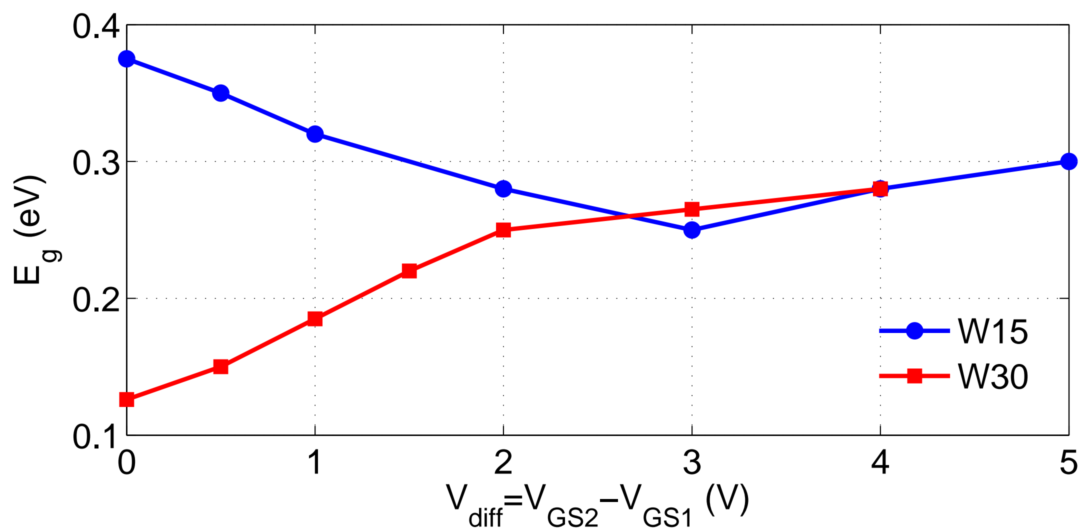


Fig. 2.13: Energy gap, extracted from transmission spectra, with V_{diff} for W30 (3.74 nm) and W15 (1.87 nm) BLGNR widths.

TH-1608_11610201

2.5 Summary

The 1-D real-space transport model with analytically defined transverse modes was developed. This model can be applied equally well to the simulations of G-FET, GNR-FET, BLG-FET and BLGNR-FET with only small modifications. A significant computational saving can be achieved for G-FET and GNR-FET simulations by using 1×1 coupling matrices. The BLG and BLGNR were expressed by the two single layer GNR Hamiltonian matrices, coupled by the hopping parameters corresponding to the overlaying atoms along the z direction. This was allowed to model BLGNR-FET and BLG-FET by same transport equations as GNR-FET and G-FET with only small modifications. Devices based on graphene are in the development stage, and the quantum simulator proposed can be a powerful tool to evaluate various technology options and device structures.

TH-1608_11610201

3

Analysis of Graphene Tunnel Field-Effect Transistor

Contents

3.1 Introduction 46
3.2 Device Geometry and Performance Metrics 47
3.3 Results 48
3.4 Summary 58

TH-1608_11610201

3.1 Introduction

Graphene has been considered as one of the promising material for analog/RF applications due to its excellent electronic properties such as higher carrier mobility and higher saturation velocity that would allow high device transconductance (g_m) and high device cutoff frequency (f_T) [11,20,65]. However, the absence of bandgap in graphene leads to quasi-saturation and negative differential resistance (NDR) in the output characteristics of long channel and short channel devices [66, 69]. This produces larger output conductance (g_{ds}) compared to transconductance and consequently, reduces the intrinsic gain and the oscillation frequency. Thus, the main challenge with graphene field-effect transistors (GFETs) for analog applications is to improve the saturation behavior in their output characteristics without significantly degrading its current levels.

It has been reported that transport in GFET is largely contributed by the band to band tunneling (BTBT) up to channel lengths of 50 nm [78]. Also, Alarcon *et al.* have recently observed that the source to channel (S-C) BTBT is responsible for the onset of current saturation in conventional GFET (C-GFET), while the channel to drain (C-D) BTBT and thermionic current dominance suppresses saturation behavior [118]. Interestingly, Ganapathi *et al.* have recently proposed that the current saturation in GFET can be improved by p-type doping in the drain underlap region to enhance the BTBT tunneling current dominance [68]. These observations suggest that the BTBT is the dominant current component in GFET, and also the one that determines the behavior in their output characteristics. Therefore, a tunnel field-effect transistor (TFET), in which the S-C BTBT current is controlled by gate voltage, can be a viable option in graphene devices to achieve better current saturation without significantly degrading its current levels. Moreover, graphene tunnel field-effect transistor (T-GFET) can be a more promising candidate for good gate electrostatic control because graphene device in general has smaller quantum capacitance than Si-TFET, and TFET geometry offers even smaller quantum capacitance compared to MOSFET geometry in the case of larger V_DS, [122, 123].

Early works on graphene based tunnel field effect transistors have particularly focused on the out-plane tunneling, such as lateral [83], vertical heterostructures [57], BisFET [29] and SymFET [30]. These proposed structures are suitable for digital applications due to their high on/off ratio, but they are certainly not useful for analog/RF applications because of very narrow current saturation region and larger parasitic capacitances. Therefore, this work considers a planner p-i-n T-GFET with MOSFET like operation, for analog/RF applications. Our main focus is on the extraction of

the intrinsic analog/RF performance metrics of T-GFET, in particular the intrinsic gain and cutoff frequency.

3.2 Device Geometry and Performance Metrics

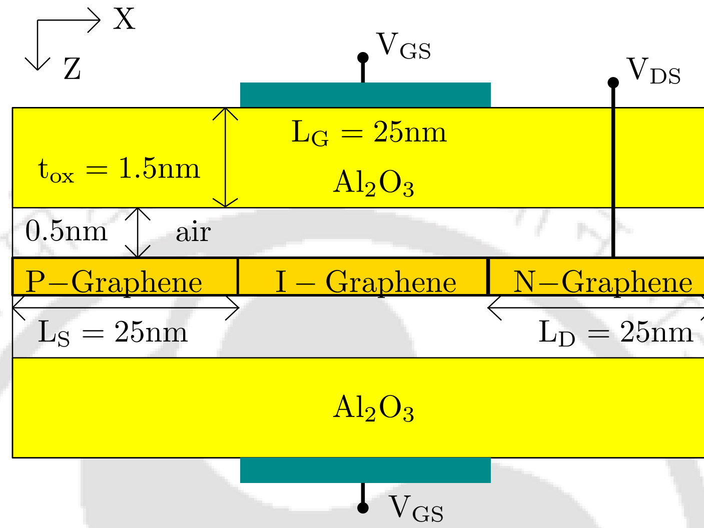


Fig. 3.1: Simulated tunnel graphene field effect transistor (T-GFET) geometry.

The simulated double gate (DG) p-i-n T-GFET geometry is shown in Fig. 3.1. The intrinsic 2-D graphene sheet is served as a channel, having a length of 25 nm. The source and drain regions of length 25 nm are the extension of the channel and are doped to p-type and n-type, respectively with a doping concentration of 4×10^{13} cm^{-2}. When n-i-n C-GFET is used for performance comparison, all the simulation parameters are kept identical except that the source region doping is changed to n-type. The Al_2O_3 serves both as top and bottom gate oxides having a physical thickness of 1.5 nm and dielectric constant of 10. This 1.5 nm physical thickness of Al_2O_3 is equivalent to an effective oxide thickness (EOT) of 0.6 nm. Atomistic simulation for graphene layer and a continuum simulation for the oxide regions (with a given dielectric constant) is performed. In this connection, an air spacer of 0.5 nm is assumed between the plane connecting the centers of carbon atoms and the interface of the oxide region, otherwise the graphene atoms merge with dielectric atoms, which is practically never feasible. The air spacer of 0.5nm is a reasonable value and it is approximately equal to the atomic distance. This air spacer is only a simulation consideration and it is not an intended step during the device fabrication. In particular, DG geometry is employed in the simulation because it reduces short

TH-1608_11610201

channel effects and provides larger on current. Initially, both the gate are perfectly aligned, when the gate misalignment is considered in the later simulations, both the gates are misaligned equally.

The usual quasi-static approximation is used to evaluate high frequency performance of T-GFETs [78,97]. The intrinsic performance metrics are computed by running the self-consistent DC simulations, as discussed in Chapter 2 for G-FET. In particular, intrinsic gate capacitance (C_g), the transconductance (g_m) and the output conductance (g_{ds}) are calculated as

$$C_g = \left.\frac{\partial Q_{ch}}{\partial V_{GS}}\right|_{V_{DS}}, \quad g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}}, and \quad g_{ds} = \left.\frac{\partial I_{DS}}{\partial V_{DS}}\right|_{V_{GS}} \tag{3.1}$$

Where, Q_{ch} is the average charge in the channel. Subsequently, the intrinsic gain (A_{V0}) and the intrinsic cut-off frequency (f_T) can be computed as

$$A_{V0} = \frac{g_m}{g_{ds}} \qquad f_T = \frac{g_m}{2\pi C_g} \tag{3.2}$$

3.3 Results

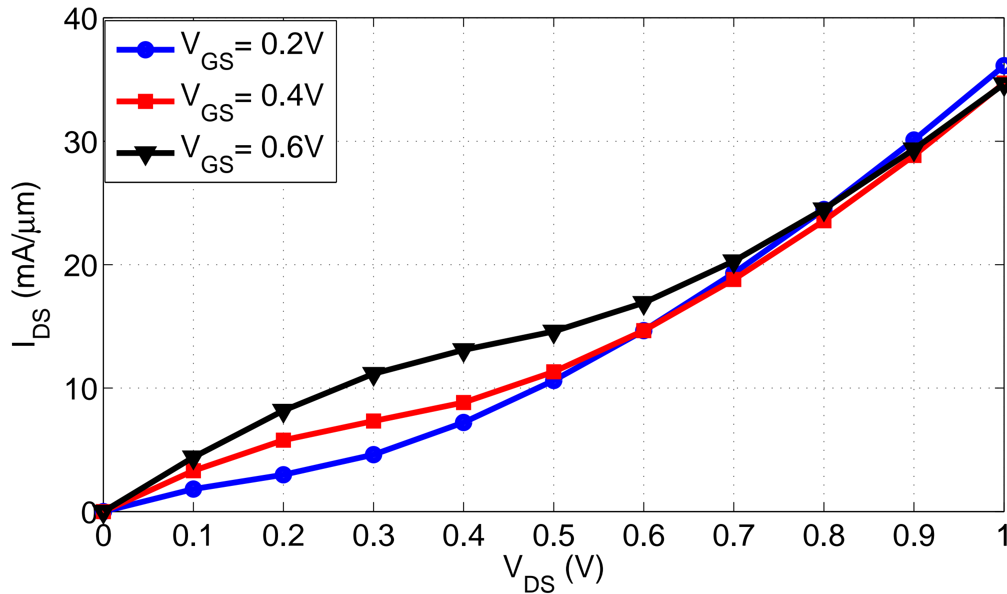


Fig. 3.2: Output characteristics of nominal T-GFET for different positive V_{GS}.

Fig. 3.2 shows the output characteristics of nominal T-GFET, at room temperature, for positive gate voltages. The current saturation is possible only for intermediate V_{DS}, at the larger gate voltages. While, at small gate voltages, the quasi-linear increment in the current density is appeared for all V_{DS}. The output characteristics of T-GFET is similar to previous reports of short channel GFET [68, 118]

TH-1608_11610201

as well as experimentally obtained for long channel GFET [66, 124].

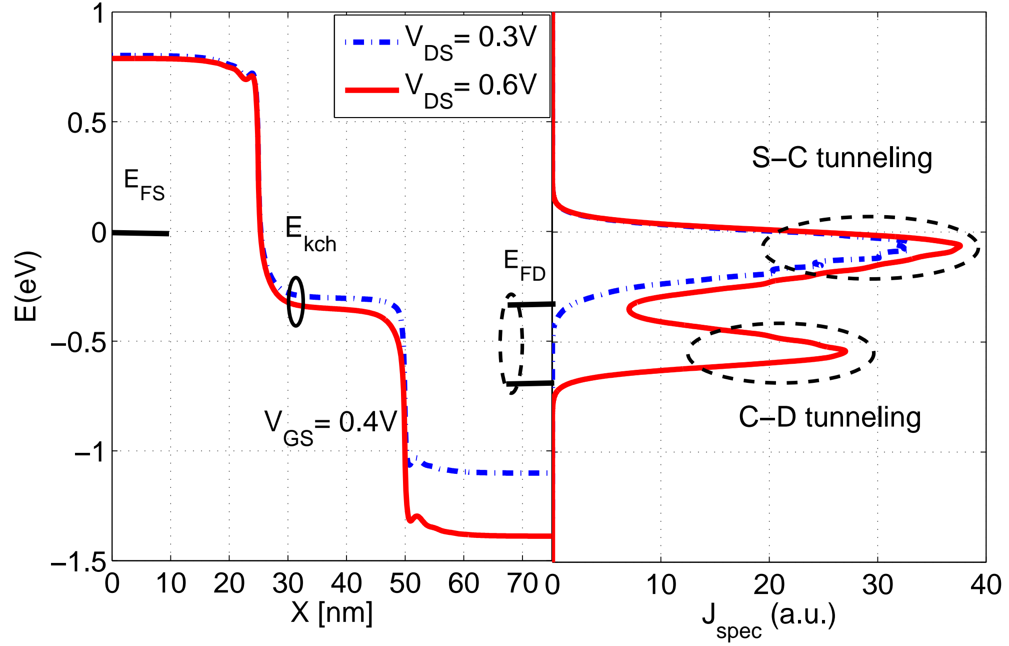


Fig. 3.3: (Left) T-GFET potential energy profile along the transport direction and (right) corresponding current spectra at $V_{GS} = 0.4$ V for $V_{DS} = 0.3$ V (dash line) and $V_{DS} = 0.6$ V (solid line). The current spectra shows the source-channel (S-C) tunneling regime and the channel-drain (C-D) tunneling regime separated in the energy axis. Where E_{FS} and E_{FD} are Fermi levels at the source and drain regions respectively, and E_{kch} is Dirac point energy in the channel.

The physical origin of quasi-saturation and quasi-linear behavior can be better understood by observing the contribution of tunneling current components in drain current [Fig. 3.3] and analyzing their distribution with V_{DS} [Fig. 3.4]. The Fig. 3.3 shows the self-consistent potential energy profile of T-GFET along the transport direction and the corresponding current spectra, at $V_{GS} = 0.4$ V, for two different V_{DS} values. For $V_{DS} = 0.3$ V (dash lines), the current spectra is only due to the source-channel (S-C) tunneling from the hole states at the source region to the electron states at the channel region. However, for $V_{DS} = 0.6$ V (solid lines), the current spectra contains additional channel-drain (C-D) tunneling component from the hole states at the channel region to the electron states at the drain region. This C-D tunneling current causes accumulation of holes in the channel region, as these holes do not contribute to the current flow. Consequently, it lowers the channel potential energy and brings increment in the S-C tunneling current, as shown in Fig. 3.3. For $V_{GS} = 0.6$ V, a transmission valley separates current regimes in the current spectra and it is due to the pseudoenergy gap by k_y states around the channel potential energy.

Fig. 3.4 shows the distribution of the S-C and the C-D tunneling currents in the output character-

TH-1608_11610201

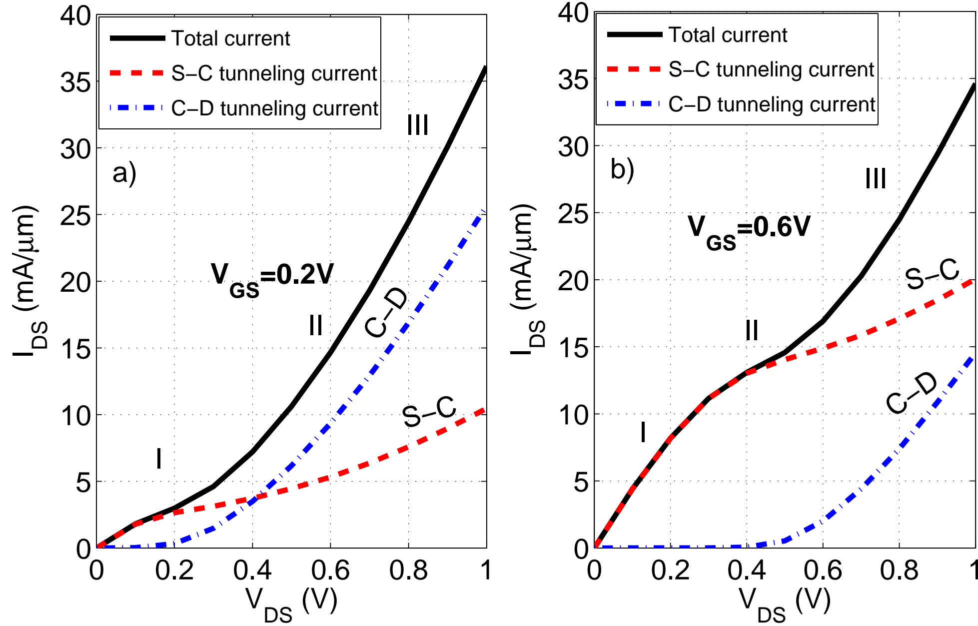


Fig. 3.4: The contribution of S-C and C-D tunneling currents in T-GFET for different V_{DS}, at (a) $V_{GS} = 0.2$ V, and (b) $V_{GS} = 0.6$ V.

istics for (a) $V_{GS} = 0.2$ V, and (b) $V_{GS} = 0.6$ V. It is observed for $V_{GS} = 0.2$ V that, because of the small gate induced barrier in the channel, the C-D tunneling current becomes significant even from small V_{DS}. This leads to linear increment to the total current for all V_{DS} values [region I, region II and region III in Fig. 3.4(a)]. On the other hand, for $V_{GS} = 0.6$ V, the current density is only due to the S-C tunneling at small V_{DS} values [region I in Fig. 3.4(b)]. For intermediate values of V_{DS}, this S-C tunneling current saturates because of the pseudoenergy gap around the channel potential energy and causes saturation in the total current [region II in Fig. 3.4(b)]. At larger V_{DS}, the C-D tunneling current contribution becomes significant, which linearly increases the total current, and it is called the second linear region [region III in Fig. 3.4(b)].

In summary, the current saturation in the output characteristics of T-GFET is possible when the C-D tunneling current becomes negligible. Subsequently, we examine that whether the contribution of C-D tunneling current can be reduced by the right choice of device parameters, such as gate oxide thickness, drain underlap and drain overlap, and doping profile.

TH-1608_11610201

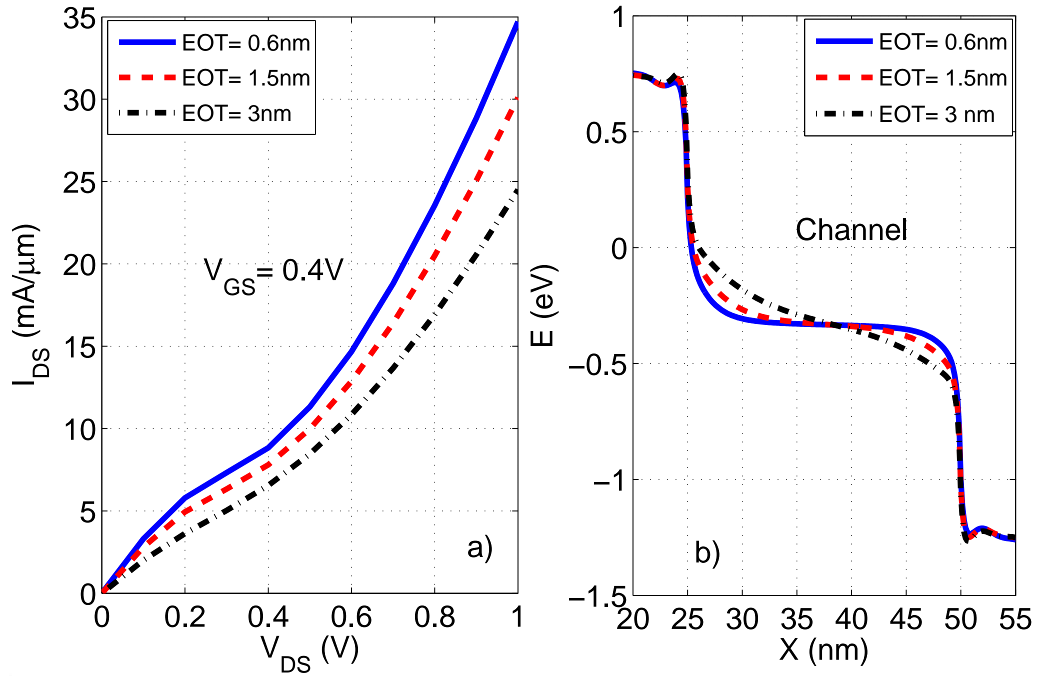


Fig. 3.5: (a) Output characteristics of T-GFET for different equivalent oxide thickness (EOT) at $V_{GS} = 0.4$ V, and (b) Corresponding potential energy profile in the channel region at $V_{DS} = 0.6$ V.

3.3.1 Impact of Oxide Thickness

Fig. 3.5(a) shows the output characteristics for three different EOT, which represents three different physical thickness of Al_2O_3. It is observed from Fig. 3.5(a) that a decrease of EOT enhances the quasi-saturation and second linear region in the output characteristics. This can be understood by analyzing the device potential energy in the channel region for different EOT, as shown in Fig. 3.5(b). The C_{ox}/C_q becomes smaller with the decreasing the oxide thickness, which makes barrier thinner and results in steeper source- channel and drain-channel junctions. A narrow S-C barrier width results in larger S-C tunneling current, and improves the onset of current saturation. Moreover, thinner C-D tunneling barrier width results in larger C-D tunneling current, and makes the second linear region more pronounced. Therefore, the smallest possible EOT can be an optimal choice in T-GFET to enhance onset of current saturation.

3.3.2 Impact of Drain Underlap and Drain Overlap Lengths

Fig. 3.6(b) shows that a larger drain underlap length cause low DOS section at the C-D junction for larger V_{DS}, which widens the C-D barrier width. Thus, an increase in the underlap length decreases the C-D tunneling current and reduces the current dependence in the second linear region, as observed

TH-1608_11610201

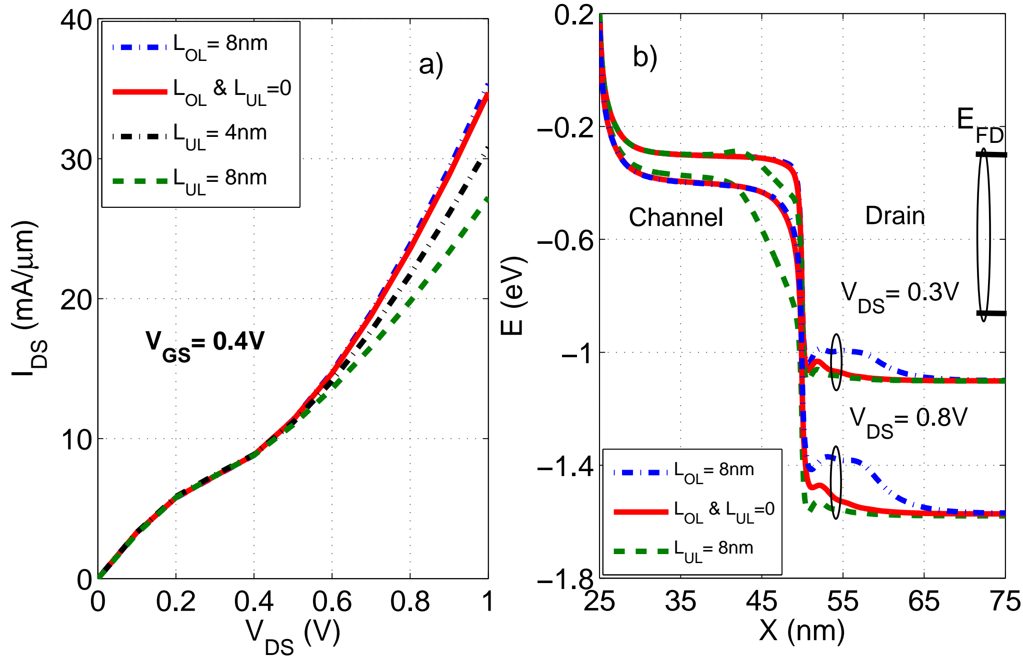


Fig. 3.6: (a) Output characteristics of T-GFET for a drain overlap length, no drain overlap and underlap, and two different drain underlap lengths at $V_{GS} = 0.4$ V, and (b) Corresponding potential energy profile in the channel and drain regions for $V_{DS} = 0.3$ V and $V_{DS} = 0.8$ V for structures having 8-nm drain underlap, no drain underlap and drain overlap, and 8-nm drain overlap length.

in Fig. 3.6(a). In contrast, at small V_{DS}, the current density is only due to the S-C tunneling, it is unaffected by the drain underlap length. It is also observed from Fig. 3.6 that an increase of drain overlap length does not significantly affect the device output characteristics. This is because the change in the potential energy by the drain overlap is the outside of the transmission energy window [E_{FS}, E_{FD}] (here E_{FS}=0 and $E_{FD} = V_{DS}$). In summary, the drain underlap, which is present in all experimental graphene transistors, can be a suitable parameter in T-GFET to reduce the second linear region.

3.3.3 Impact of Channel and Drain Doping Concentrations

With the recent advancement of the doping engineering in the graphene transistors [63,125], doping control can be one of the most preferable choice for device performance optimization. If the doping in the drain region is decreased and channel region is lightly doped to n-type, the C-D tunneling current can be significantly suppressed because of the widening of tunneling barrier width for a gradual doping profile at the C-D junction. Consequently, the S-C component of current also increases because of the narrowing of the tunneling barrier width with an abrupt doping profile at the S-C junction. Therefore,

TH-1608_11610201

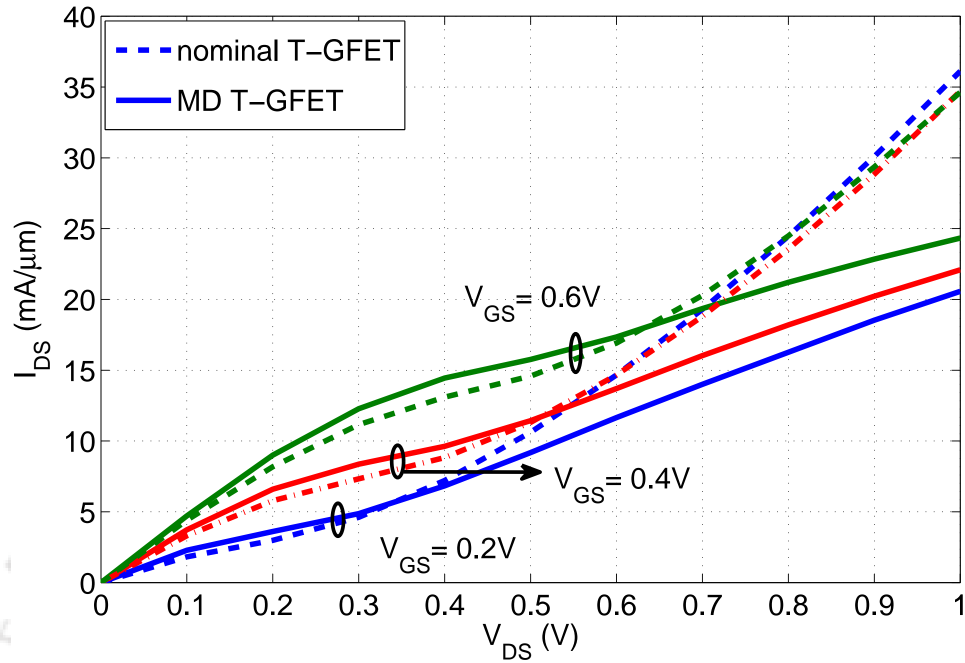


Fig. 3.7: Output characteristics of nominal T-GFET and modified doped (MD) T-GFET for different V_{GS}. Modified channel doping concentration is $N_C = 8 \times 10^{11}$ cm^{-2} and drain doping concentration is $N_D = 4 \times 10^{12}$ cm^{-2}.

a better drain region doping concentration will be 10× smaller than the source region, and the channel region is doped to n-type with the doping concentration 5× smaller than the drain region. Fig. 3.7 compares the output characteristics between nominal T-GFET and modified doped (MD) T-GFET, for three different gate voltages. It is observed that the suggested doping concentrations effectively enhances the current saturation as well increases the current levels. The reason for improved current saturation in MD T-GFET can be understood by examining the device potential energy profiles for different V_{DS}, as shown in Fig. 3.8. The observations from potential energy profile and corresponding effects on the output characteristics are as follows:

- When sufficient positive gate voltage is applied, the carrier concentration in the channel becomes comparable to the drain. Therefore, the increase in V_{DS} from 0V to 0.3 V, appears across the C-D junction, which in turn increases channel-drain junction depletion region width. The increment in the channel depletion width lowers the channel potential energy corresponding to V_{DS} changes, as observed in Fig. 3.8. This increases the S-C junction electric field and leads to a gradual increase in the S-C BTBT current with V_{DS}. As a result, the current density increases gradually in this V_{DS} range.

TH-1608_11610201

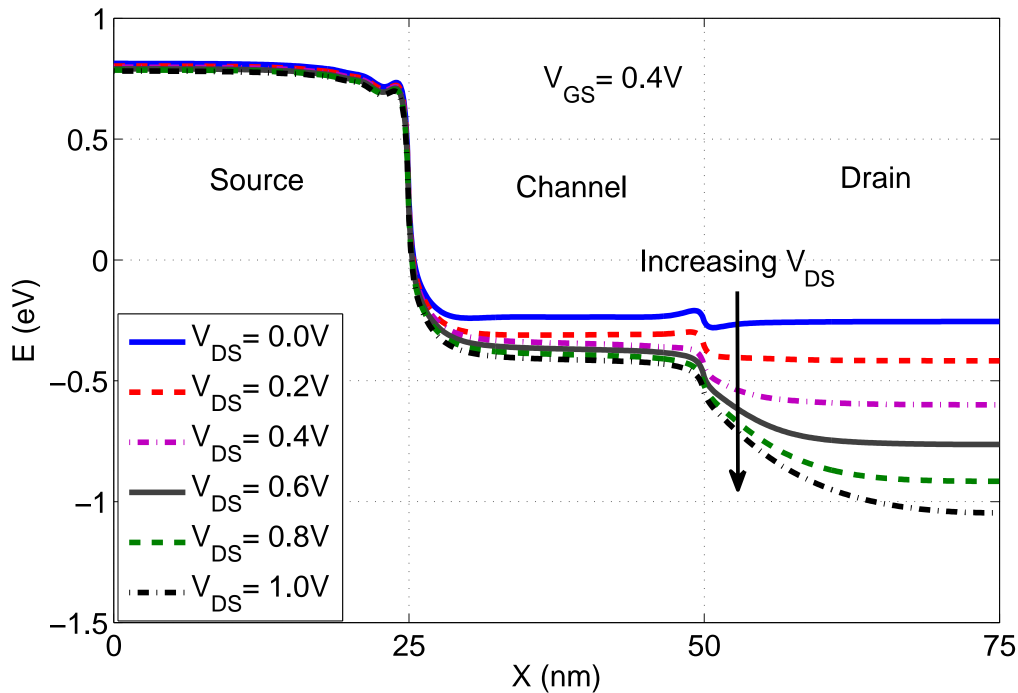


Fig. 3.8: Modified doped (MD) T-GFET potential energy profile, at $V_{GS} = 0.4$ V, for different V_{DS}.

- For increasing V_{DS} beyond 0.3 V, the electron concentration in the channel becomes smaller because of the larger depletion region. This reduces the drain voltage effects on the channel potential energy, and consequently saturates the S-C tunneling current. However, at high V_{DS}, a small C-D component of current is still present that weakens the current saturation by preventing the saturation of the channel potential energy.

- To further minimize the C-D tunneling current, the drain doping concentration can be decreased, but it may bring an early device breakdown for high drain voltages. Therefore, for a particular V_{DS}, the desirable drain doping concentration is such that $E_{KD,V_{DS}} > E_{FD,V_{DS}}$, where E_{KD} is the drain region Dirac point energy and E_{FD} is the drain region Fermi energy level, at same V_{DS} (here, $E_{FD} = V_{DS}$).

Hence, modified doping concentrations in the channel and the drain are capable of partially suppressing the C-D tunneling current, and reducing the holes accumulation for high V_{GS}. However, the current saturation is not improved for small V_{GS} values. This is because the S-C tunneling current is still smaller compared to the C-D tunneling current. The gate voltage range, in which the current saturation is possible, can be altered by tailoring the channel doping concentrations.

TH-1608_11610201

3.3.4 Impact of Underlap and Overlap Lengths in a MD T-GFET

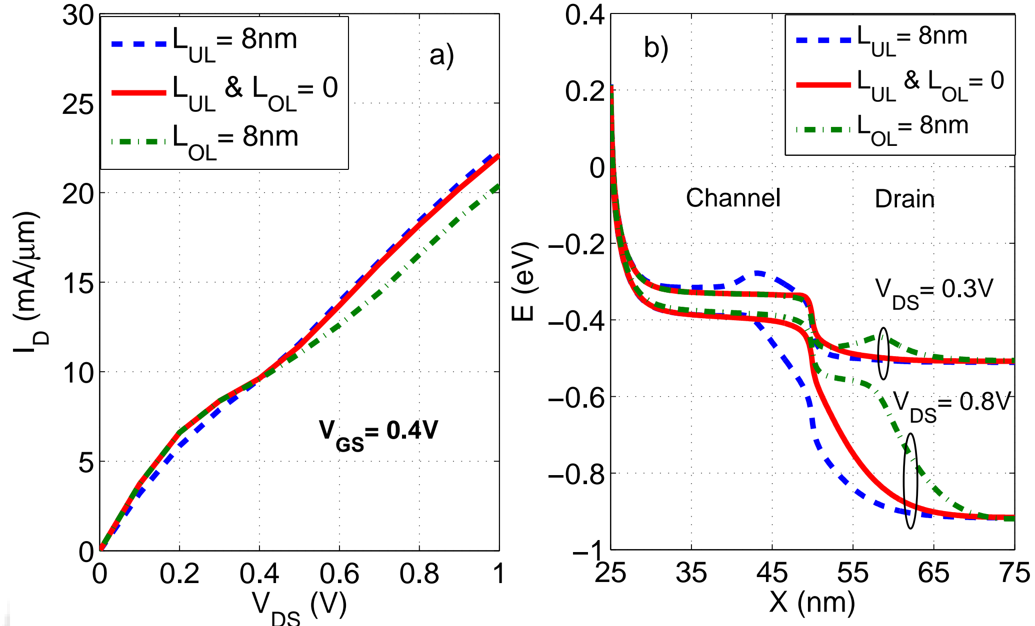


Fig. 3.9: (a) Output characteristic of MD T-GFET for three cases: 8nm drain underlap, no underlap and overlap, and 8-nm drain overlap, at $V_{GS} = 0.4$ V. (b) Corresponding potential energy profiles in the channel and drain regions at $V_{DS} = 0.3$ V and $V_{DS} = 0.8$ V.

Having appreciated with the effect of underlap on the saturation behavior of a nominal T-GFET, it might seem that drain underlap and overlap in MD-TFET should further suppress the C-D tunneling current. It is observed in Fig. 3.9(a) that a larger drain overlap length in MD T-GFET further enhances the current saturation, while a larger drain underlap length degrades the saturation behavior. To understand this further, the corresponding device potential profile along the transport direction is plotted in Fig. 3.9(b) at two different V_{DS} values for three cases: 8 nm underlap, no underlap and overlap, and 8 nm overlap. For the case of underlap, the S-C tunneling current decreases at small V_{DS} because the rise of the potential energy in the underlap region, while the S-C tunneling tunneling current increases at high V_{DS} because the increases of the drain field effect into the channel. As a result, the current density is marginally decreased for small V_{DS} values and marginally increased for high V_{DS} values. On the other hand, for the case of overlap, a larger drain overlap in MD T-GFET decreases the C-D tunneling current because the increase of the band bending distance at C-D junction for high V_{DS} values. In contrast, the S-C tunneling current is insensitive to the drain overlap length, the current density is unchanged for small V_{DS}.

TH-1608_11610201

Therefore, the drain overlap along with appropriate channel and the drain doping concentrations is an effective design strategy to enhance V_{DS} window for the current saturation. Subsequently, the effectiveness of the saturation region in all the above described structures is analyzed by estimating their output resistance and intrinsic gain.

3.3.5 Output Resistance and Intrinsic Gain

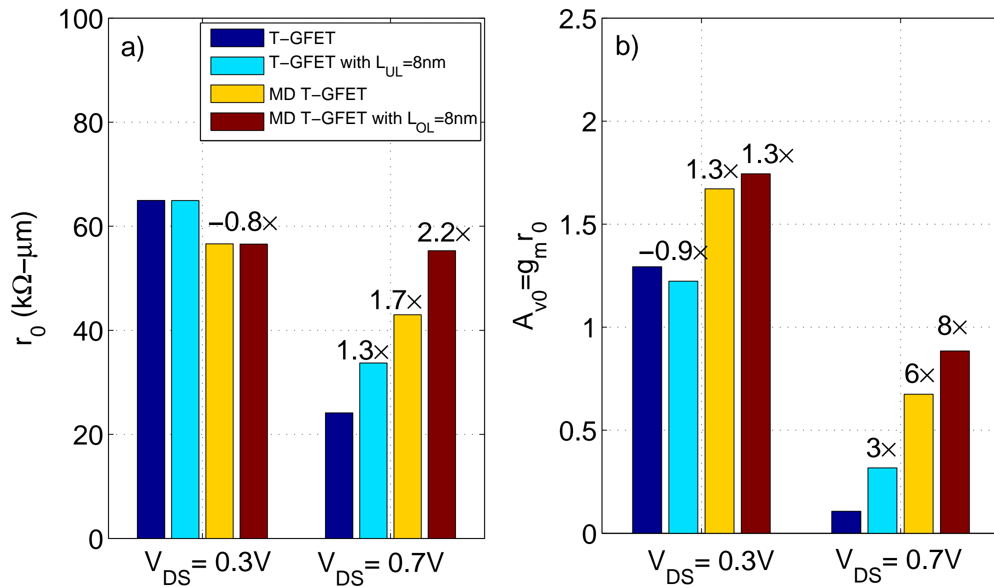


Fig. 3.10: Comparison of four different device structures: nominal T-GFET, T-GFET with 8-nm drain underlap, MD T-GFET, and MD T-GFET with 8-nm overlap at $V_{GS} = 0.4$ V. (a) Output resistance at $V_{DS} = 0.3$ V and $V_{DS} = 0.7$ V, and (b) Intrinsic gain at $V_{DS} = 0.3$ V and $V_{DS} = 0.7$ V.

Fig. 3.10 shows the comparison of the output resistance and the intrinsic voltage gain, at $V_{GS} = 0.4$ V, in four different architectures: nominal T-GFET, T-GFET with 8-nm drain underlap, MD T-GFET, and MD T-GFET with 8-nm overlap. It is observed that peak intrinsic gain for MD T-GFET with 8-nm overlap is about 1.3× higher than nominal T-GFET at $V_{DS} = 0.3$ V. Whereas, at $V_{DS} = 0.7$ V, MD T-GFET with 8-nm overlap lead to a factor of 2.2× improvement in the output resistance, 3.6× improvement in g_m (not shown) and that results in 8× improvement in intrinsic gain.

Hence, the appropriate drain overlap with control channel and drain doping concentrations in T-GFET increases the peak intrinsic gain and also reduces V_{DS} dependency of maximum intrinsic gain. This reduced V_{DS} dependency of intrinsic gain improves T-GFET linearity and stability for high frequency applications. It makes T-GFET a promising device for high frequency multiplier and RF mixer circuits. On the other hand, T-GFET peak intrinsic gain still needs to be improved to build RF

TH-1608_11610201

amplifiers and oscillators. However, it should be noted that the drain doping reduction may increase the drain series resistance and the drain overlap may increase the drain capacitance. This might cause deterioration in the RF performance parameters. The relative benefits of T-GFET over C-GFET geometry are investigated by comparing analog/RF performance parameters, in the following section.

3.3.6 C-GFET versus T-GFET

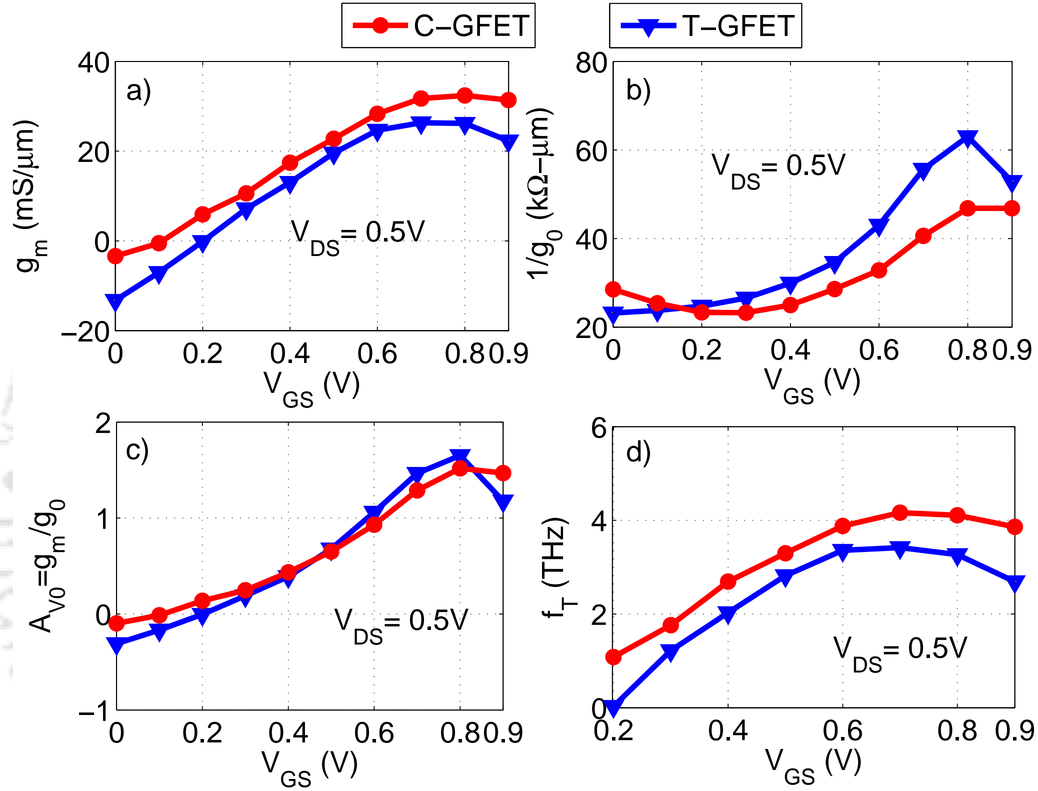


Fig. 3.11: Comparison between C-GFET and T-GFET obtained at $V_{DS} = 0.5$ V. (a) Transconductance (g_m), (b) Output resistance ($1/g_0$), (c) Intrinsic gain (A_{V0}), and (d) Cutoff frequency (f_T).

The T-GFET has smaller current values and hence smaller the transconductance compared to a C-GFET, as shown in Fig. 3.11(a). Both C-GFET and T-GFET show the linear increment of the transconductance for moderate values of V_{GS}. For larger V_{GS}, both the devices show the transconductance peaks, when the BTBT leakage current (S-C tunneling in C-GEFT or C-D tunneling in T-GFET) becomes negligible. It is observed from Fig. 3.11(b) and Fig. 3.11(c) that the extent of current saturation with respect to V_{DS} in T-GFET increases the output resistance and brings in 1.2× higher intrinsic gain compared to C-GFET at the expense of marginal reduction in the cutoff frequencies, as seen in Fig. 3.11(d).

TH-1608_11610201

3.3.7 Impact of Channel Length on Intrinsic Gain and Cutoff Frequency

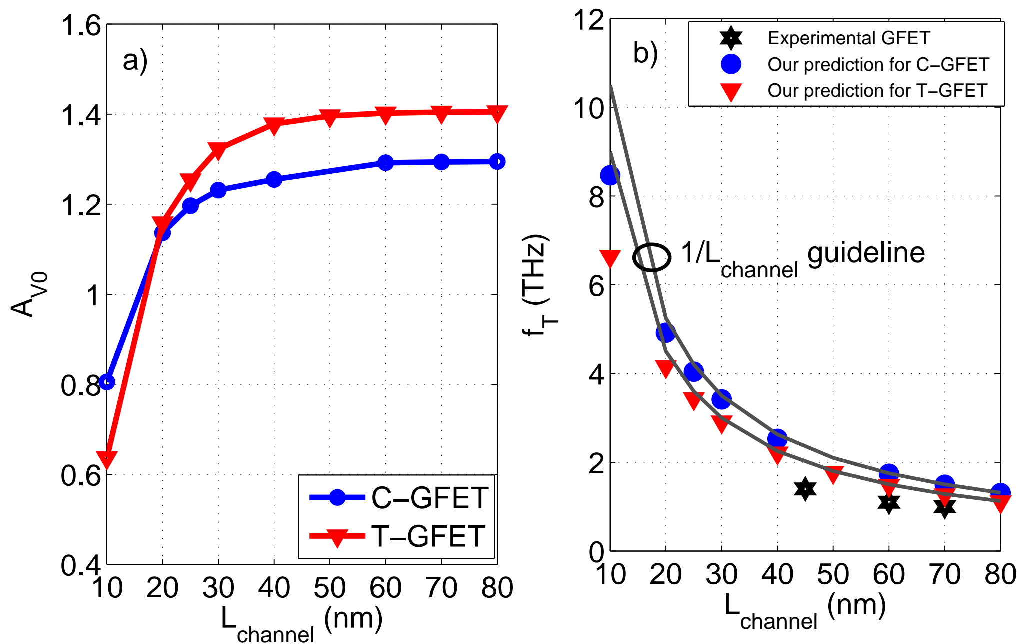


Fig. 3.12: (a) Peak intrinsic gain versus channel length obtained at $V_{DS} = 0.5$ V, and (b)Peak cutoff frequency versus channel length obtained at $V_{DS} = 0.5$ V. The experimental results are based on self-aligned nanowire GFET [5].

Fig. 3.12(a) shows that the intrinsic gain of T-GFET becomes independent of the channel length beyond 40-nm. T-GFET has larger degradation in the intrinsic gain compared to C-GFET for channel lengths below 40-nm. The intrinsic gains of both C-GFET and T-GFET are greatly reduced at 10-nm channel, which is in agreement with graphene nanoribbon findings [126]. In Fig. 3.12(b), the intrinsic cutoff frequencies of both C-GFET and T-GFET devices show $1/L_{channel}$ dependence for channel lengths ranging from 20-nm to 80-nm. This scaling trend of intrinsic cutoff frequency for C-GFET is in good agreement with experimental result [62] and other simulated results [68, 78]. Besides, the simulated cutoff frequencies of ballistic C-GFET are higher as compared to the experimentally obtained values of GFET [5] for same channel lengths. These differences may be due to the assumption of ballistic transport and neglecting of the parasitic effects and interface effects, in the simulation.

3.4 Summary

T-GFET has shown marginally higher (20%) intrinsic gain compared to C-GFET. It has found that an appropriate selection of device parameters in T-GFET can significantly suppress the C-D tunneling

TH-1608_11610201

current and improve the current saturation. In particular, an 8-nm overlap with suitable doping profile leads to 2.2× improvement in the output resistance, 3.6× improvement in g_m, and 8× improvement in intrinsic gain, especially at larger V_{DS}. Therefore, a planar TFET with graphene offers several benefits and is expected to be an alternative candidate to C-GFET for analog/RF applications.

TH-1608_11610201

TH-1608_11610201

4

Analysis of Bilayer Graphene Nanoribbon Field-Effect Transistors

Contents

4.1 Introduction . . . 62
4.2 Digital Performance . . . 62
4.3 Analog/RF Performance . . . 69
4.4 Summary . . . 76

TH-1608_11610201

4.1 Introduction

The cutting of graphene into nanoribbons (GNRs) and the applying vertical electric field across bilayer graphene (BLG) are two widely preferred strategies to induce an energy gap, but each alone is insufficient to achieve better device performance both for digital and analog applications. The combination of both BLG and GNR to form bilayer graphene nanoribbon (BLGNR) has offered the potential to induce a significant energy gap [4, 47]. Recent experimental study on 40 nm wide BLGNR-FET has reported an ON/OFF current ratio of about 3000 at room temperature [49], which is 30 fold higher than the highest value reported for BLG-FET [43]. This ON/OFF current ratio with BLGNR-FET is smaller for switching requirement, but the fabrication advancements to produce smooth edge BLGNR with narrow width can significantly improve the ON/OFF ratio. Apart from logic applications, BLGNR-FETs can also be a strong candidate for analog/RF applications as they offer strong suppression for both 1/f and phase noises [127]. The major advantage with BLGNR is that the energy gap is less sensitive to edge disorders compared to GNRs, and therefore these materials do not need to highly precise lithography [113, 128].

In this chapter, a systematic study of BLGNR-FET is carried out by an in-house developed quantum simulator (Chapter 2), which incorporates the physical properties of BLGNR and structural aspects of FET. Our main focus is on the characterizations of BLGNR-FET with different device widths and other key drivers behind those characteristics, rather than the estimation of ultimate performance limits of these devices. The digital performance of BLGNR-FET is evaluated in double gate device structure with chemically doped source and drain regions to achieve better gate electrostatic control, while an electrostatically doped device geometry by a back gate is preferred for analog/RF performance evaluation as it simple for fabrication and serve advantage for wide BLGNR.

4.2 Digital Performance

It could be inferred from Fig. 2.13 that the energy gap in BLGNR strongly depends on the width and the gate electric field. Therefore, BLGNR of different widths is considered here for digital performance evaluation. Especially, bilayer widths of 3M family are used as they have better semiconducting properties than two other families (3M+1 and 3M+2) of BLGNR [4], where M is a positive integer.

TH-1608_11610201

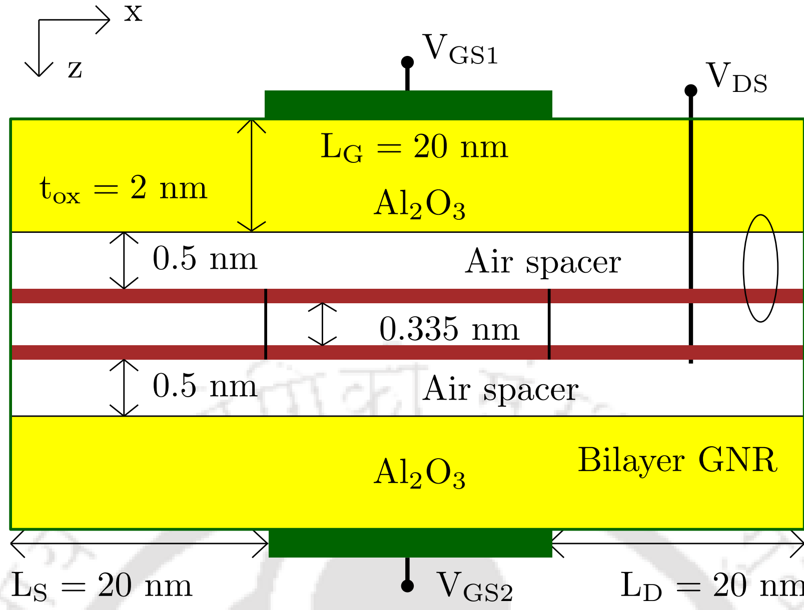


Fig. 4.1: Schematic of simulated bilayer graphene nanoribbon FET (BLGNR) device.

4.2.1 Device Geometry and Performance Metrics

Fig. 4.1 shows the schematic of considered DG BLGNR-FET for digital performance metric evaluation. The BLGNR is composed of two A-B (Bernal) stacking of armchair-edged GNRs, and the dangling bonds at the edges are assumed to be saturated by hydrogen atoms. The interlayer distance is considered to be the equilibrium value of 0.335 nm. The intrinsic BLGNR is used as a channel, having a length of 20 nm. The source and the drain regions are 20 nm long and doped to n-type with a molar fraction of $f_d = 3 \times 10^{-3}$. The Al_2O_3 having a dielectric constant of 10 and thickness of 2 nm is considered as top and bottom gate dielectrics, to obtain an equivalent oxide thickness of 0.78 nm. Similar to Fig. 2.5, an air spacer of 0.5 nm is assumed between the plane connecting the center of carbon atoms and the interface of the oxide region, but it is not shown in the schematic. BLGNR is classified using 1-D unit cell along the width direction. For an example, W15 and W30 represent the numbers of elementary cells along width direction with widths of 1.87 nm and 3.74 nm, respectively. The scaling of bilayer ribbon width is realized by varying the numbers of elementary cells.

The conventional way of computing ON current (I_{ON}) is $I_{DS}(V_{GS} = V_{DD}, V_{DS} = V_{DD})$ and OFF current (I_{OFF}) is $I_{DS}(V_{GS} = 0, V_{DS} = V_{DD})$. For bilayer devices, this definition results in very small ON/OFF current ratio, which is insignificant for performance comparison with other graphene-based transistors. Therefore, experimental groups [28, 43, 49] define I_{ON} and I_{OFF} as a maximum I_{DS} and

TH-1608_11610201

minimum of I_{DS}, respectively, and the same definition is employed in this work. In the simulation, the difference of bottom and top gate voltage $V_{diff} = V_{GS2} - V_{GS1}$ is used for characterization to visualize the effect of confinement-induced energy gap at $V_{diff} = 0$ V and the effect of field-induced energy gap at $V_{diff} \neq 0$ V.

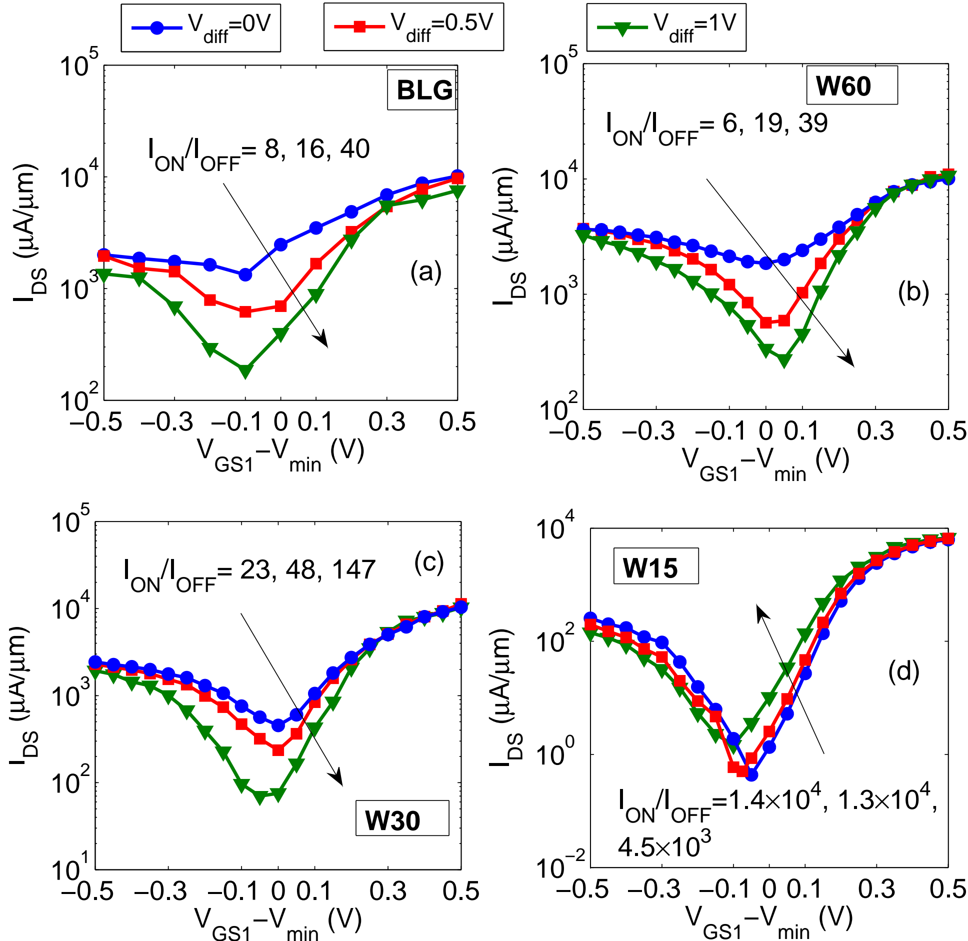


Fig. 4.2: Transfer characteristics of (a) bilayer graphene (BLG) FET, and (b) W60 width , (c) W30 width, and (d) W15 width BLGNR-FETs, at $V_{DS} = 0.2$ V. Where, $V_{diff} = V_{GS2} - V_{GS1}$ and $V_{\min} = (V_{GS2} - V_{GS1})/2$.

4.2.2 ON-state and OFF-state Performance

It is observed from Fig. 4.2(a) that the ON current of BLG-FET is higher than that of Si (0.35 mA/μm) and III-V compound (0.55 mA/μm) MOSFETs for same channel length [129], but the ON/OFF current ratios are smaller than 40. Because, the field-induced energy gap is within few hundred millielectron volts, and it causes larger BTBT current in the OFF-state. It could be inferred from Fig. 4.2(b) to (d) and Table 4.1 that the ON current (method 1) of BLGNR-FET for all the widths is nearly same with that of BLG-FET and interestingly the ON/OFF current ratios of BLGNR-

FET increases significantly with decreasing width. The reasons for small OFF current and significant ON current in BLGNR-FETs are as follows.

Table 4.1: ON current and ON/OFF current ratio of BLGNR-FETs according to two definitions, at $V_{diff} = 0$ V and $V_{DD} = 0.2$ V.

	I_{ON}(μA/μm)		I_{ON}/I_{OFF}	
Width	Method 1[a]	Method 2[b]	Method 1[a]	Method 2[b]
BLG	1×10^4	3.5×10^3	8	2.6
W60 (7.4 nm)	1.3×10^4	3.8×10^3	6	2
W30 (3.74 nm)	1×10^4	2.7×10^3	23	6
W18 (2.24 nm)	6.1×10^3	1×10^3	751	83
W15 (1.87 nm)	4.7×10^3	139	1.4×10^4	318
W12 (1.49 nm)	4×10^3	2.4	1.5×10^6	892
W9 (1.12 nm)	1.5×10^3	1.2	7.4×10^{11}	4.4×10^3

[a] Method 1: $[I_{ON}, I_{OFF}] = [\max(I_{DS}), \min(I_{DS})]$.
[b] Method 2: $[I_{ON}, I_{OFF}] = [I_{DS}(V_{GS1} = V_{\min} + V_{DD}), I_{DS}(V_{GS1} = V_{\min})]$, at $V_{DS} = V_{DD}$.

- For bilayer ribbons having energy gap below critical value, narrowing the width (till critical energy gap of ribbon) attributes to small increase in the energy gap. This increment reduces the source-channel BTBT tunneling current, which in turn improves the gate electrostatic control. The improved gate control results in larger field-induced energy gap opening for narrower BLGNR-FET. It is evident from Fig. 4.3 that, at $V_{diff} = 1$ V, the energy gap opening for W30 BLGNR-FET is larger than that of W60 BLGNR-FET and BLG-FET. A larger energy gap decreases OFF current and hence increases ON/OFF current ratio for narrowing the device width, as shown in Fig. 4.2(b) and (c). However, for bilayer ribbons having energy gap above critical value, narrowing the width (lesser than W30) leads to significant confinement-induced energy gap, which results in much smaller OFF current compared to wider width devices [Fig. 4.2(d)]. Besides, the applying differential gate voltage across such widths decreases the energy gap, which increases the OFF current as well as the ON current and overall decreases ON/OFF current ratio.

- Smaller effective mass materials result in more energy separation from the quantum confinement [107]. Therefore, wider BLGNR has more energy subbands within the same energy range than

TH-1608_11610201

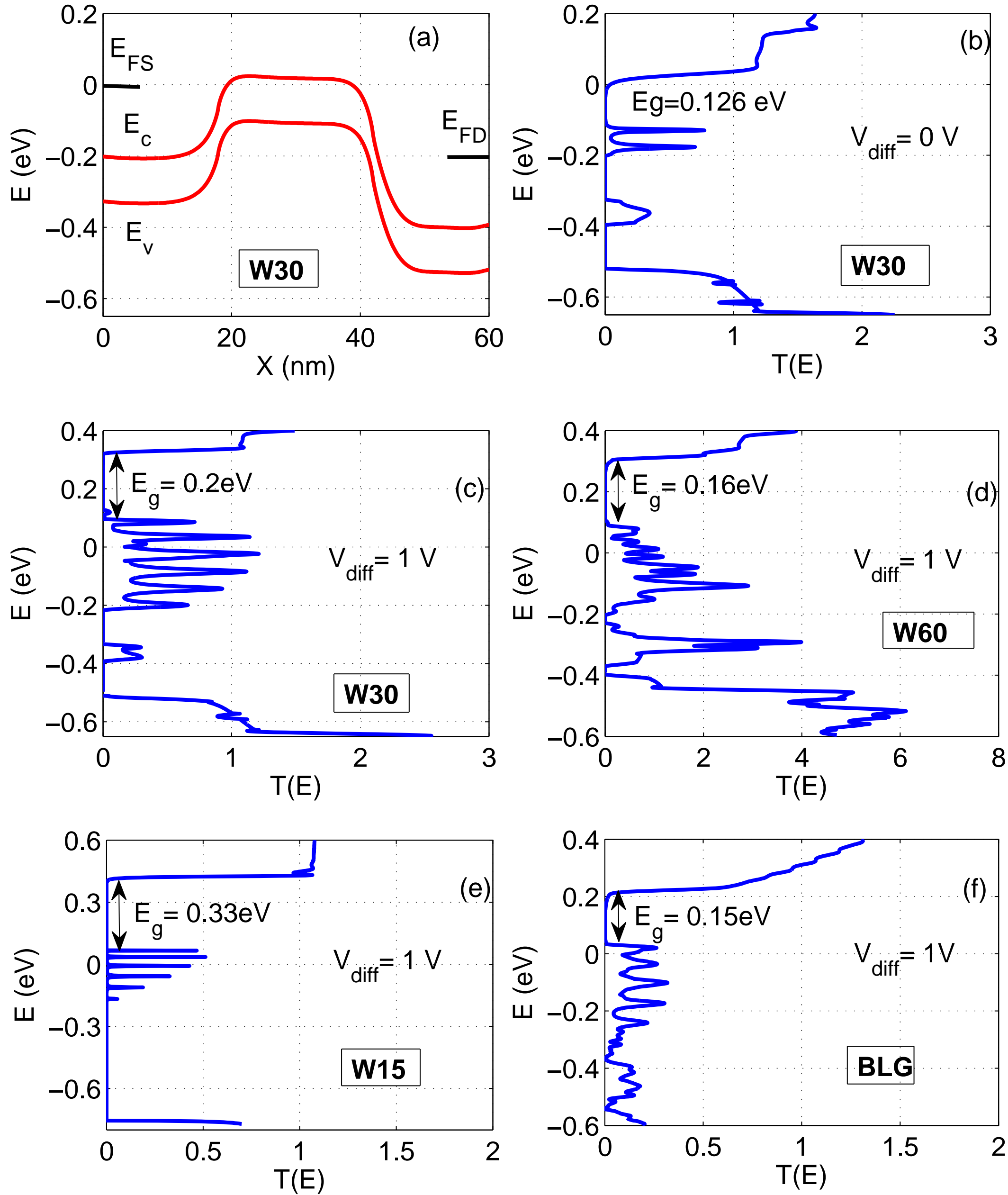


Fig. 4.3: (a) Energy band profile along transport direction and (b) corresponding energy-resolved transmission spectra of W30 BLGNR-FET, at $V_{GS1} = V_{GS2} = 0$ V. Energy-resolved transmission spectra of (c) W30, (d) W60, (e) W15 BLGNR-FETs and (f) BLG-FET, at $V_{GS1} = -1$ V and $V_{GS1} = 0$ V.

that of BLG and GNR. This is evident from the magnitude of transmission coefficient of BLGNR and BLG, as shown in Fig. 4.3. The increase in energy bands provides more energy states in the conduction band (CB) and the valance band (VB). The availability of additional energy states in both CB and VB leads to larger current components values. As a result, ON current for BLGNR devices is comparable to that of BLG device. However, for narrow BLGNR device, the increased effective mass restricts energy separation [48], but improved gate control leads to a comparable ON current in BLG-FET.

Table 4.1 compares the ON current and ON/OFF current ratio of BLGNR devices according to two definitions. It is observed from that the significant ON/OFF current ratio with BLGNR-FETs can be achieved for very narrow width. With the recent experimental progress in obtaining smooth edge GNR devices with very narrow width [41, 42] suggests that narrow BLGNR devices may ultimately be feasible.

4.2.3 BLGNR-FET versus MLGNR-FET

The advantages of BLGNR-FETs over MLGNR-FETs can be better investigated by comparing transmission spectra, ON current and ON/OFF current ratio. Figure 4.4 shows the energy-resolved transmission spectra of BLGNR and MLGNR devices for W60 and W15 widths, at $V_{DS} = 0.2$ V. In particular, the transmission spectra for W15 MGNR device is plotted at $V_{GS1} = -1$ V and $V_{GS2} = 0$ V to highlight the associated energy gap value. The following observations are made by comparing the transmission spectra of BLGNR and MLGNR devices.

- The confinement-induced energy gap in MLGNR is relatively higher than BLGNR for same ribbon width. This difference in energy gap arises because of interlayer coupling in BLGNR. However, for wider width, it is observed that a larger gate electric field in BLGNR significantly higher the energy gap than the MLGNR.

- For the same energy window, the transmission coefficient of BLGNR is about 2× higher than MLGNR-FET for the same width condition. This is because the reduced energy gap accompanied by smaller carrier effect mass in BLGNR results in more low energy states. This high transmission coefficient promises better ON-state performance with BLGNR-FET.

Fig. 4.5 shows ON current and ON/OFF current ratio between BLGNR and MLGNR devices at $V_{diff} = 0$ V (confinement-induced energy gap case) and $V_{diff} = 1$ V (field-induced energy gap case).

TH-1608_11610201

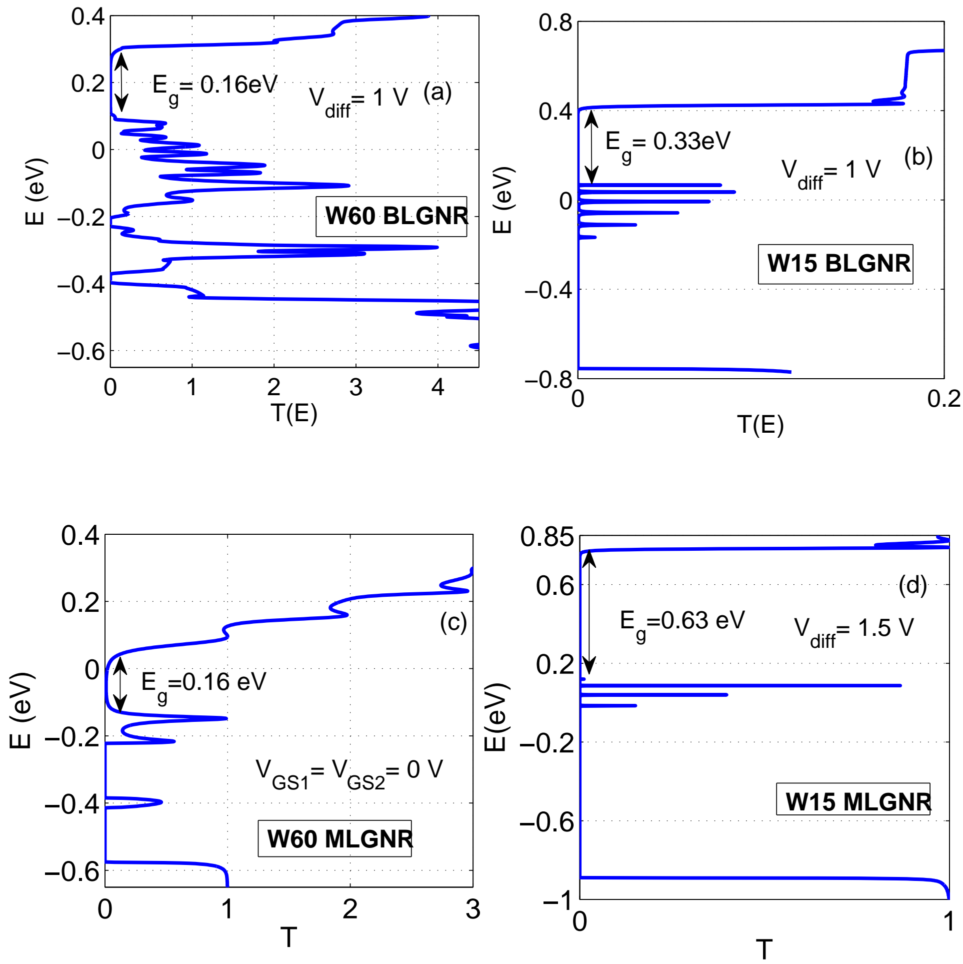


Fig. 4.4: Energy-resolved transmission spectra, at $V_{DS} = 0.2$ V of (a) W60 and (b) W15 BLGNR devices at $V_{diff} = 1$, (c) W60 MLGNR device at $V_{diff} = 0$ V and (d) W15 MLGNR device at $V_{diff} = 1$ V.

It is observed that, at $V_{diff} = 0$ V, the ON/OFF current ratio of BLGNR devices is smaller than MLGNR devices, even though BLGNR devices have around 2× higher ON current. This is because the reduced energy gap results in higher OFF current. However, for $V_{diff} = 1$ V, BLGNR of devices width wider than W42 have marginally higher ON/OFF current ratio with approximately 2× higher ON current compared to MLGNR devices. The reason is that the field-induced energy gap in BLGNR devices is marginally higher than the confinement induced energy gap in MLGNR at this gate voltage [Fig. 4.3]. Such results are in good agreement with experimentally obtained results for BLGNR and MLGNR devices [49]. Therefore, at wide width, BLGNR devices can give better performance than MLGNR at high differential gate voltage. However, achieving high gate voltage is difficult in IC and it also increases wiring problem. For very narrow ribbon, BLGNR devices have significantly higher

TH-1608_11610201

ON current than MLGNR devices, but their ON/OFF current ratio are considerably smaller compared to MLGNR-FET because of considerably smaller energy gap. Therefore, at narrow width, BLGNR devices fail to produce advantage over MLGNR.

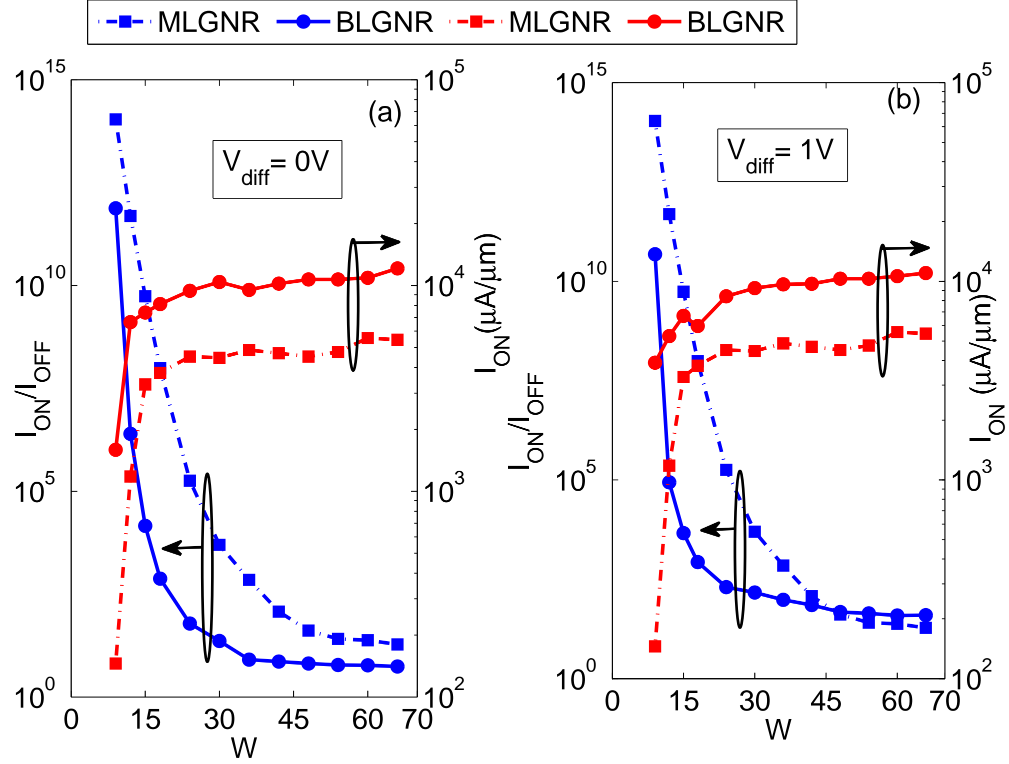


Fig. 4.5: I_{ON}/I_{OFF} and I_{ON} of BLGNR and MLGNR devices as a function of device width, at $V_{DS} = 0.2$ V, for (a) $V_{diff} = 0$ V, and (b) $V_{diff} = 1$ V. Where, $V_{diff} = V_{GS2} - V_{GS1}$.

4.3 Analog/RF Performance

The main demand with graphene based transistor for analog/RF applications is to obtain current saturation in the output characteristics without lowering the current values. To observe the impact of energy gap on the current saturation, we have investigated W15 and W30 BLGNR devices as both devices have opposite electric field-dependency [Fig. 2.13]. Furthermore, MLGNR devices are not used here for performance comparison as they are not very popular for RF applications due to their low ON current.

4.3.1 Device Geometry and Performance Metrics

Fig. 4.6 shows the schematic of the simulated dual gate BLGNR-FET, which is identical to device structures used in the experiments of graphene [66, 73], but aggressively scaled to reduce the compu-

TH-1608_11610201

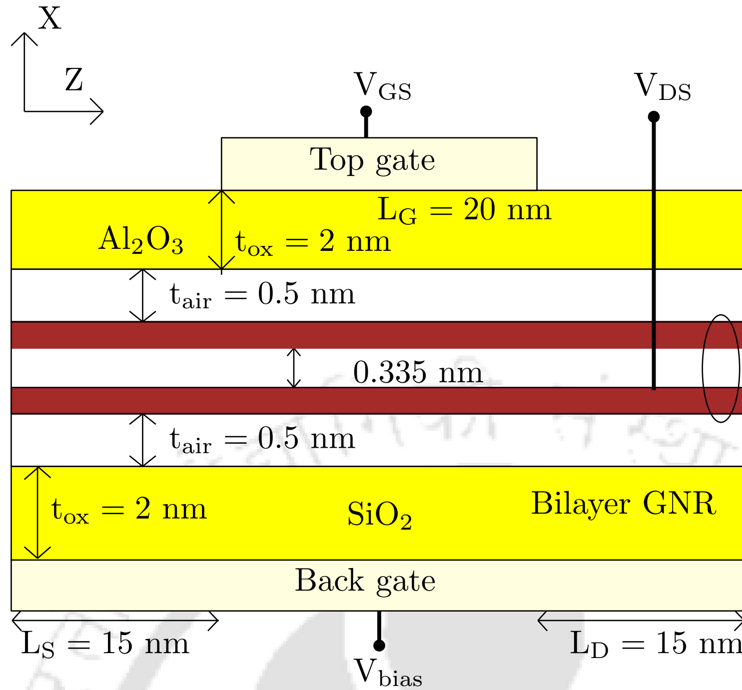


Fig. 4.6: Schematic of simulated BLGNR-FET. The back gate is used to electrostatically doped the source and the drain regions. The zero voltage on the source terminal is taken as a reference.

tational cost. This structure is most widely employed in experiments due to its simplicity. However, it is certainly not ideal for RF applications as the back gate dielectric may introduce larger parasitic capacitance. The intrinsic BLGNR with interlayer spacing of 0.335 nm is used as the channel, the source and the drain. The BLGNR is basically composed of two Bernal (A-B) stacking of armchair edged nanoribbon, and the unsaturated bonds at the edges are assumed to be passivated by hydrogen atoms. In particular, the edge bond relaxation in BLGNR, which arises from the hydrogen passivation of edge states, is diminished by the electron-electron interaction at the edges [113]. Therefore, simulation study of BLGNR-FET can be very close to a realistic device. The BLGNR is placed on SiO_2 of physical thickness of 2 nm, which serves as a back gate oxide. The back gate serves two purposes: 1) create doping in the device and 2) enhance the energy gap for wider devices. The Al_2O_3 of dielectric constant 10 is taken as a top gate oxide with physical thickness of 2 nm (EOT= 0.78 nm), which is the main gate for channel charge modulation. The high-frequency performance of BLGNR devices is assessed by evaluating the small signal parameters from the obtained source to drain current density and channel charge density (Q_{ch}) values, as discussed in Chapter 3.

TH-1608_11610201

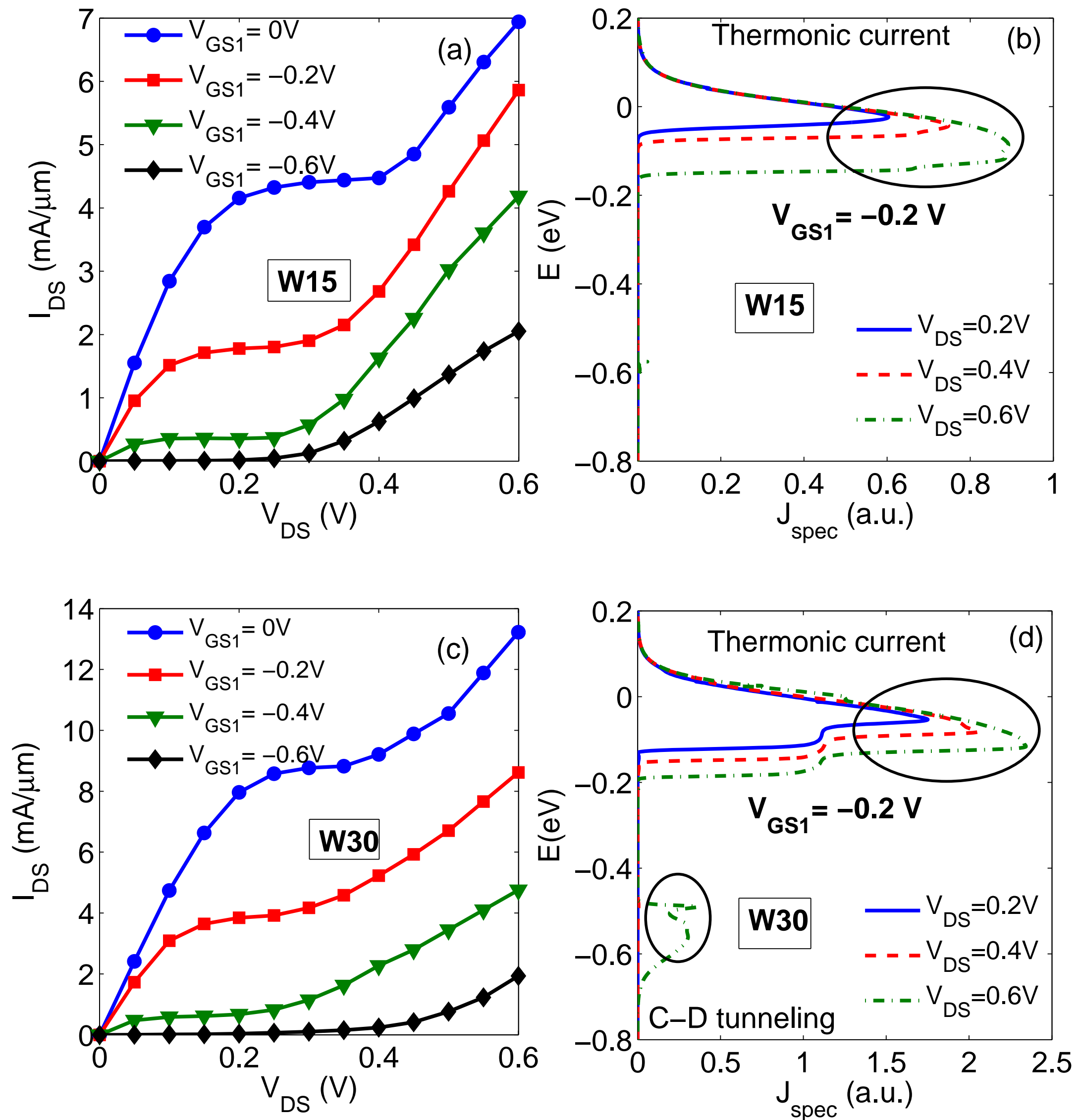


Fig. 4.7: Output characteristics of (a) W15 and (c) W30 BLGNR-FET at V_{bias} = 1.2 V for various top gate voltages. Corresponding current spectra of (b) W15 and (d) W30 device at $V_{GS1} = -0.2$ V for three different V_{DS} values. Where W15 and W30 represent the widths of 1.87 nm and 3.74 nm.

4.3.2 Output Characteristics and Intrinsic Gain

Fig. 4.7(a) and (c) show the output characteristics of W15 and W30 devices, respectively at $V_{bias} = 1.2$ V for different top gate voltages. At high V_{DS}, the weak current saturation is observed for both the devices. Such behavior in the output characteristics is very common in the case of graphene-based FETs [66, 68, 118, 121]. Despite having significant difference in the confinement-induced energy gap, both the devices show quite similar behavior in the output characteristics: the current saturation

TH-1608_11610201

is exhibited for moderate V_{DS} and quasi-linear increases is appeared for high V_{DS} values. The physics behind for this behavior can be better understood by analyzing the contribution of current components at different V_{DS} values.

Fig. 4.7(b) and 4.7(d) show the current spectra of W15 and W30 devices, respectively at $V_{GS1} = -0.2$ V and $V_{bias} = 1.2$ V for three different V_{DS} values. It is observed from Fig. 4.7(b) that the current for W15 device is essentially due to thermionic current component for all V_{DS}, however the contribution of thermionic current increases gradually with V_{DS}. The reason is that the drain field weakly screens the channel and source electric field due to relatively small concentration of carriers. This in turn lowers the channel and source region potential energy profile, which leads to gradual increases in the thermionic current components. Therefore, the weak saturation for W15 device is due to usual short channel effect, especially drain-induced barrier lowering (DIBL).

It is observed from Fig. 4.7(d) that the current for W30 device is due to thermionic emission for low V_{DS}, while the current is included additional channel-to-drain tunneling (C-D tunneling) current component at high V_{DS}. The contribution of the C-D tunneling increases linearly with V_{DS}, which causes pile-up of holes in the channel as these holes do not contribute to the current flow. Consequently, it lowers the channel potential energy and leads to linear increase in the thermionic current with V_{DS}. Besides, the drain field lowers the channel potential energy at high V_{DS}. Therefore, the screening from drain field and the contribution of the C-D tunneling for W30 device result in quasi-linear increase in the current at high V_{DS}. At more negative V_{GS} values, the conduction band of the channel is pushed above the E_{FS} that increases the contribution of the C-D tunneling from moderate V_{DS}. This in turn narrows the V_{DS} window for current saturation with decreasing V_{GS} values. Subsequently, the extent of current saturation among W15 and W30 devices is examined by investigating V_{DS} dependency on the intrinsic gain.

Fig. 4.8 shows transconductance (g_m), output resistance (r_o), and the intrinsic gain (A_{V0}) as a function of V_{DS} at $V_{GS1} = -0.2$ V and $V_{bias} = 1.2$ V. It is observed from Fig. 4.8(a) that g_m of W15 device is decreased gradually with increasing V_{DS}. However, g_m of W30 device is first decreased due to DIBL, then it is increased due to gradual increases in the C-D tunneling current contribution. It could be inferred from Fig. 4.8(b) that better current saturation with W15 device provides higher peak output resistance than that of W30 device. Despite W15 device has lower g_m, a higher output resistance brings in higher peak intrinsic gain compared to W30 device. More importantly, it is observed from Fig.4.8(c)

TH-1608_11610201

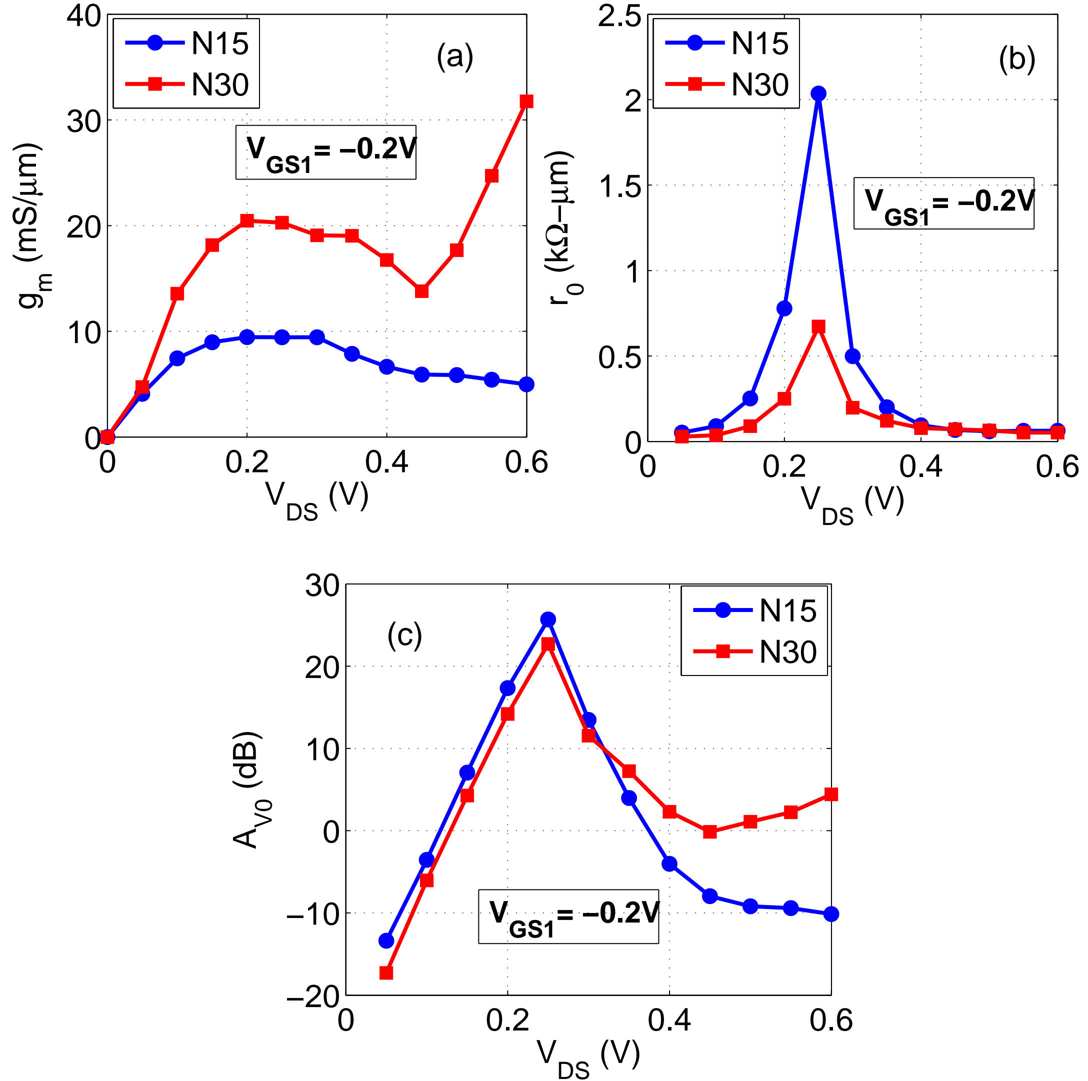


Fig. 4.8: V_{DS} dependency of (a) Transconductance, g_m , (b) Output conductance, g_{ds}, and (c) intrinsic gain A_{V0} for W15 and W30 devices, at $V_{GS} = -0.2$ V and $V_{bias} = 1.2$ V.

that the intrinsic gain of BLGNR devices are varied sgnificantly with V_{DS}. These variations in the intrinsic gain might produce distortions in the amplification or reduce the effective gain. Subsequently, we have examined that whether the V_{DS} window for saturation can be effectively engineered by the right choice of device design parameters, such as bias voltage and underlap over the source and the drain regions.

4.3.2.1 Effect of Bias Voltage

Fig. 4.9(a) and (b) show the output characteristics and intrinsic gain, respectively of W30 device at $V_{GS1} = -0.2$ V for various bias voltages (V_{BS}). It is observed that an increase of bias voltage increases

TH-1608_11610201

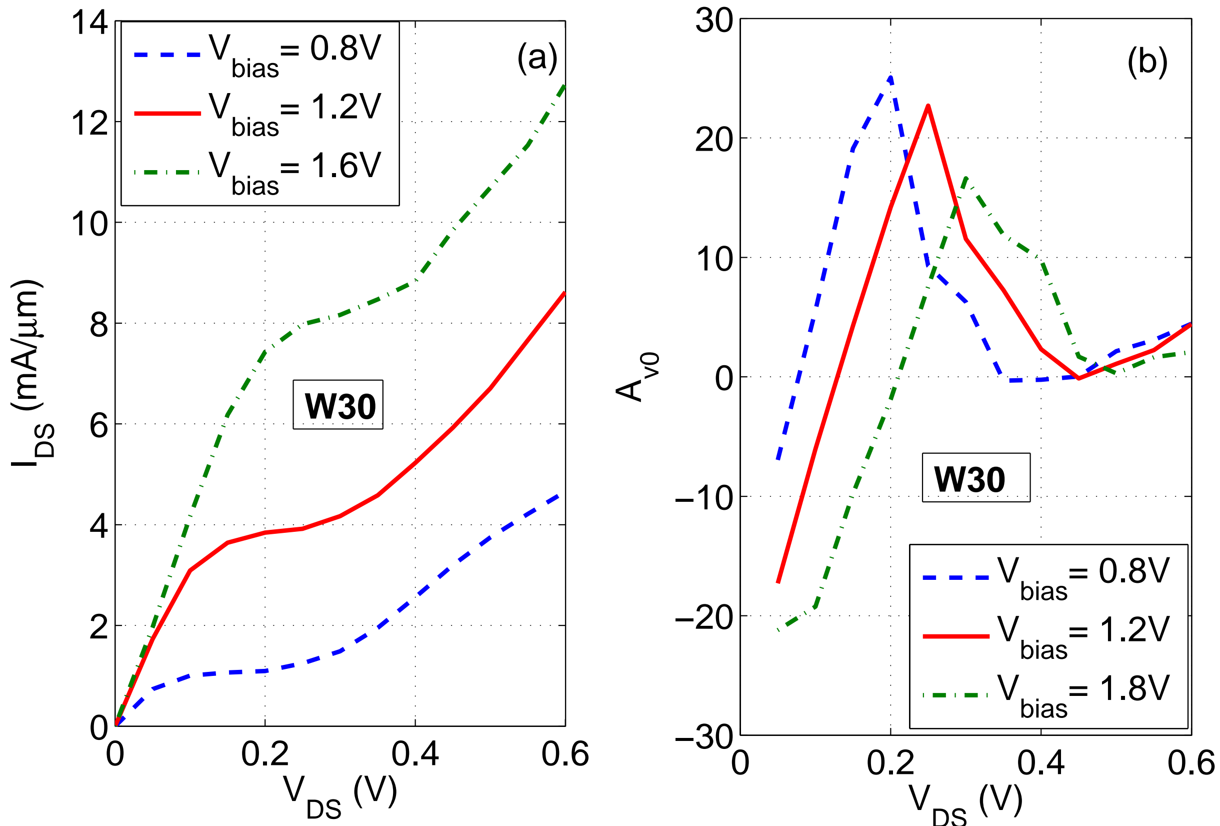


Fig. 4.9: Impact of bias voltage on BLGNR-FET. (a) drain current (I_{DS}) and (b) intrinsic gain (A_{V0}) as function of V_{DS} for different bias voltages, at $V_{GS} = -0.2$ V and $V_{bias} = 1.2$ V.

the current density, but weakens the current saturation. This is because a larger V_{BS} increases the doping density in the device and hence increases the field in the drain region. Consequently, it causes DIBL even with early V_{DS} values. Fig. 4.9(b) shows that the weak current saturation reduces the peak intrinsic gain and shift the maximum gain point to high V_{DS}. Therefore, a moderate V_{BS} can be an optimal choice in T-GFET to enhance the peak intrinsic gain with sufficient current values. The current values are very important because they mainly decide the RF metrics.

4.3.2.2 Effect of Underlap

Until now, some underlap is always present in all experimental graphene transistors and controlling its dimensions is also easier. Fig. 4.10(a) and (b) show the output characteristics and the intrinsic gain, respectively for different underlap lengths on the source and drain sides with a fixed channel length of 20 nm, at $V_{GS1} = -0.2$ V and $V_{bias} = 1.2$ V. It is observed that the underlap is not a critical design parameter as this geometry is more strongly coupled with the top and bottom gates, rather

TH-1608_11610201

than with the lateral source and drain contacts. However, a larger underlap reduces the drain voltage effect in the channel region, which improve the current saturation for moderate V_{DS} values. This in turn marginally increases the peak intrinsic gain, as observed in Fig. 4.10(b).

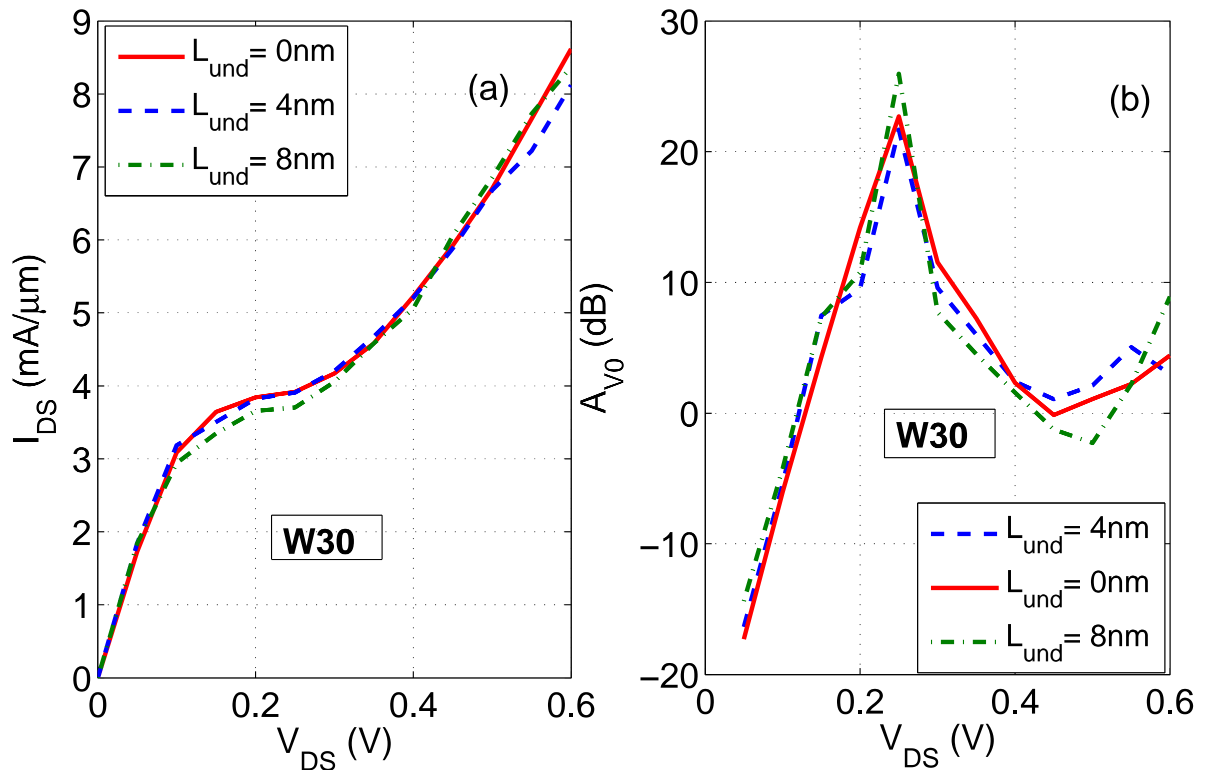


Fig. 4.10: Impact of underlap on BLGNR-FET. (a) drain current (I_{DS}) and (b) intrinsic gain (A_{V0}) as function of V_{DS} for different underlap length on the source and drain sides, at $V_{GS} = -0.2$ V and $V_{bias} = 1.2$ V.

4.3.3 Intrinsic RF Performance Metrics

Fig. 4.11 (a) and (b) shows the transconductance (g_m) and the cutoff frequency (f_T) as a function of V_{GS1} for N15 and N30 devices, at $V_{DS} = 0.3$ V. The intrinsic cutoff frequency ($f_T = g_m/2\pi C_g$) is an important RF performance metric that corresponds to maximum operating device frequency. It is observed from Fig. 4.11(a) that g_m of both the devices increases linearly with V_{GS}. This shows that the devices are operated in perfect quantum capacitance limit (QCL), $C_{OX} >> C_Q$, where C_{OX} is the oxide capacitance and C_Q is the quantum capacitance. Fig. 4.11(b) shows that the cutoff frequency of W15 device is higher than that of W30 device even though it has smaller g_m. The reason for that a lower DOS in W15 device results in much smaller quantum capacitance compared to W30 device. Since the device operating under QCL, a smaller quantum capacitance results in smaller gate

TH-1608_11610201

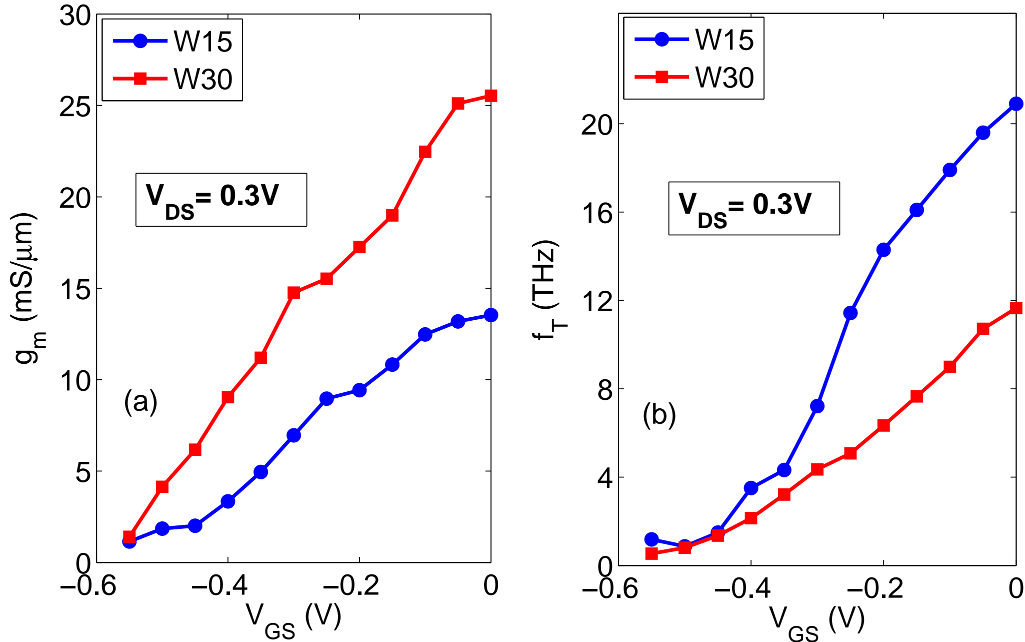


Fig. 4.11: Intrinsic RF performance metrics with respect to V_{GS}. (a) Transconductance, (g_m), and (b) intrinsic cutoff frequency (f_T) for W15 and W30 BLGNR-FETs, at V_{DS} = 0.25 V. Where W15 and W30 represent the widths of 1.87 nm and 3.74 nm.

capacitance and consequently higher cutoff frequency. It is also observed that the difference in g_m and the cutoff frequency between W15 and W30 devices become smaller for more negative V_{GS1} values. This is because the gate modulation of channel potential energy becomes slower for W15 device due to larger contribution of tunneling current (S-C tunneling).

4.4 Summary

This work has explored the possibility of realizing MOSFET by using the tunable-gap property of BLGNRs. The results show that both field and confinement tuning of energy gap are not a very promising technique for achieving appropriate switching characteristics. However, BLGNR-FETs have found more suitable compared to BLG-FET as they offer higher ON/OFF current without considerably degrading the maximum ON current values. Moreover, BLGNR-FETs can overcome the small ON current problem of MLGNR-FETs, but they require much narrower ribbon widths than MLGNR-FETs to achieve substantial ON/OFF current ratio. BLGNR-FETs have shown limited applicability for digital applications, but they can be promising candidate for high frequency RF application with intrinsic gain greater than 20 dB and cutoff frequency in terahertz (THz) range for width smaller

TH-1608_11610201

than W30. Further, the exploration in the design space, such as new structure, can be done to boost switching characteristics and reduces V_{DS} dependency of the intrinsic gain.

TH-1608_11610201

TH-1608_11610201

5

Analysis of Bilayer Graphene Nanoribbon Tunnel Field-Effect Transistors

Contents

5.1	Introduction	80
5.2	Device Geometry and Performance Metrics	81
5.3	Digital Performance	82
5.4	Analog/RF Performance	90
5.5	Summary	97

TH-1608_11610201

5.1 Introduction

Tunnel FET (TFET) is a promising device for next-generation low-power digital applications, but the low ON current of Si-TFETs is proved to be a serious limitation. Graphene is a very appealing material for TFET as it can provide high ON current with a small carrier effective mass. However, the absence of an energy gap makes large-area graphene device unable to switch OFF properly. Besides, TFETs based on counterparts of graphene, such as monolayer nanoribbon (MLGNRs) and bilayer graphene (BLG), have shown promising ON/OFF current ratio and subthreshold swing (SS) for logic applications [27, 44, 53, 56], but GNR-TFETs suffer from low ON current problem and BLG-TFET requires very high gate voltage supplies. On the other hand, the interlayer TFET based on graphene such as vertical heterostructures [57], BiSFET [29] and SymFET [30] have also found very suitable for digital applications with high ON current and ON/OFF current ratio, but they suffer from large parasitic capacitances, which may severely degrade the performance metrics in real circuits.

The study in previous chapter has shown that BLGNR-FETs have high ON current, but their ON/OFF current ratio are insufficient for switching requirement. TFET with BLGNR can allow smaller OFF current, while a moderate energy gap and small effective mass with BLGNR can maintain high ON current. Therefore, TFET with BLGNR can be a strong candidate for low voltage digital applications. Even though TFETs are particularly suitable for digital applications because of steeper subthreshold slope [79, 80], some of the TFET architectures have shown promising RF performance metrics and they can be considered as a strong candidate for analog/RF applications [81,82]. Therefore, BLGNR-TFET can also be used for high frequency RF applications. Even, they can be more desirable candidate for RF applications as BLGNR devices offer strong suppression for both 1/f and phase noises [127]. Moreover, the successful fabrication of metal contact induced doping in graphene devices suggests that nanoscale production of BLGNR-TFET with CMOS compatible process may be feasible in near future [56, 130].

The performance of BLGNR-TFET is evaluated by developed quantum-mechanical simulation (chapter 2), which includes the essential physics of BLGNR and the electrostatics of TFET. The aim of this work is to design and optimize the BLGNR-TFET for low voltage digital and analog applications. The main objective of this chapter is to characterize BLGNR-TFET with different width and investigate drivers behind those characteristics, rather than estimate the ultimate performance limits.

TH-1608_11610201

5.2 Device Geometry and Performance Metrics

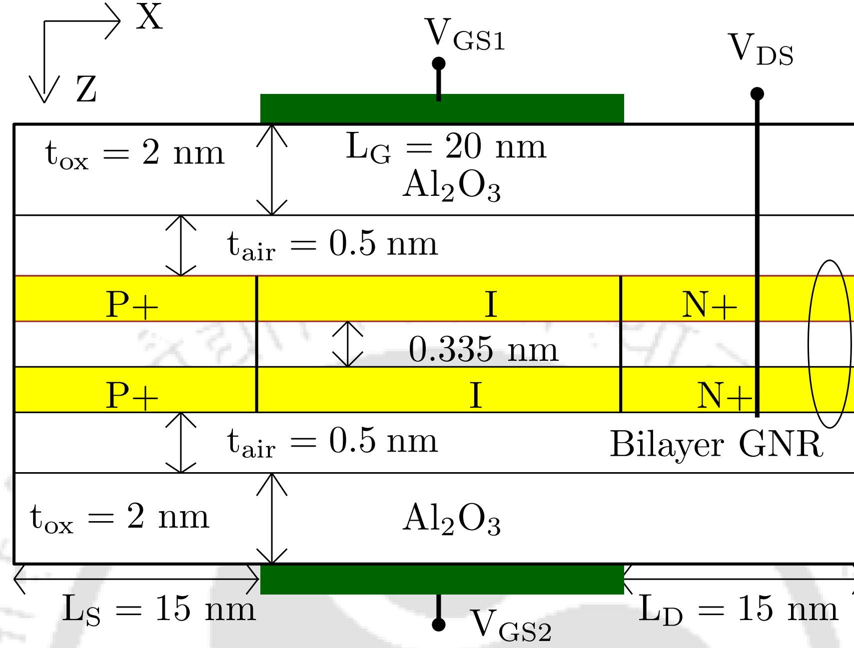


Fig. 5.1: Schematic of simulated BLGNR-TFET.

The designed p-i-n type double gated BLGNR-TFET is shown in Fig. 1, where the intrinsic BLGNR of length 20 nm is used as a channel. The considered BLGNR is Bernal (A-B) stacking of two armchair-edged GNR. The source and drain regions of length 15 nm are the extensions of channel, and are doped with a molar fraction of $f_s = f_d = 5 \times 10^{-3}$ to obtain p-type and n-type regions, respectively. The 2 nm Al_2O_3 is considered as top and bottom gate oxides, which is equivalent to a SiO_2 thickness of 0.78 nm. Similar to Fig. 2.5, an air spacer of 0.5 nm is assumed between the plane connecting the center of carbon atoms and the interface of the oxide region, but it is not shown in the schematic of BLGNR-TFET. Like in previous chapter, BLGNR is classified using 1-D unit cell along the width direction. The scaling of bilayer ribbon width is realized by varying the numbers of elementary cells.

The OFF current (I_{OFF}) and ON current (I_{ON}) are extracted by scanning the transfer characteristics with a constant $V_{DD} = 0.2$ V window [131] as $[I_{OFF}, I_{ON}] = [I_{DS}(V_{GS} = V_{GS\,\min}, V_{DS} = V_{DD}), I_{DS}(V_{GS} = V_{GS\,\min} + V_{DD}, V_{DS} = V_{DD})]$, where V_{GSmin} is the gate voltage for minimum current density. The average subthreshold swing (SS) is computed by taking average of SS within the V_{DD} window, where the I_{OFF} and I_{ON} have been determined. A quasi-static approximation is considered for projecting the high frequency performance of BLGNR devices. The intrinsic gain (A_{V0}) and in-

TH-1608_11610201

trinsic cutoff frequency (f_T) are calculated from the acquired dc drain-to-source current density and quantum charge density, as discussed in chapter 3.

5.3 Digital Performance

Due to the narrow energy gap, TFET with BLGNR can enable high performance at low supply voltage. Fig. 2.13 shows that a vertical electric field is increased the energy gap for bilayer ribbon having energy gap below the critical value (around 0.21 eV), whereas for bilayer ribbon having energy gap above the critical value, the energy gap is first decreased and then decreased with the vertical electric field. The use of wide BLGNR will require multiple high voltage supplies to achieve significant energy gaps; therefore, in this study, narrow bilayer ribbon, especially W15 device having a width of 1.87 nm, is preferred for initial performance analysis and optimization. Later, narrow bilayer widths of 3M family [W9, W12, W18 and W21 represent the width of 1.12 nm, 1.49 nm, 2.24 nm and 2.61 nm, respectively.] are used in performance comparison as they have better semiconducting properties than two other families (3M+1 and 3M+2) of BLGNR, where M is a positive integer [4].

5.3.1 ON-state and OFF-state Performance

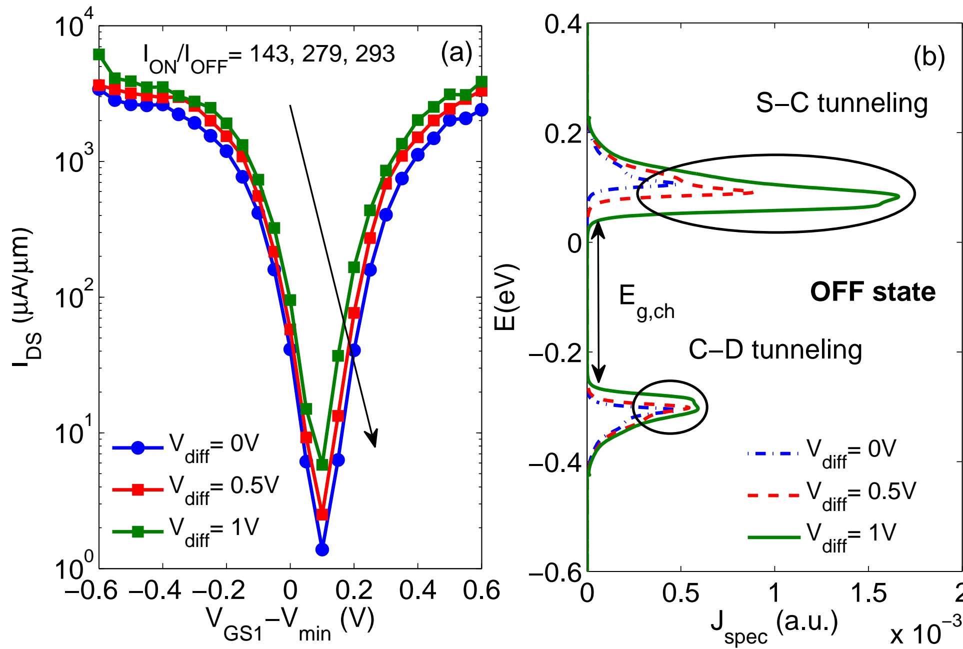


Fig. 5.2: Influence of gate voltages on W15 (1.87 nm wide) BLGNR-TFET operation. (a) Transfer characteristics, and (b) the energy resolved current spectra at OFF-state for different V_{diff}, where, $V_{diff} = V_{GS2} - V_{GS1}$, $V_{\min} = (V_{GS2} - V_{GS1})/2$, and $E_{g,ch}$ is the bandgap in the channel energy region.

TH-1608_11610201

The impact of different gate voltage (V_{diff}) on the transfer characteristics of W15 BLGNR-TFET at $V_{DS} = 0.2$ V is shown in Fig. 5.2(a). As V_{diff} increases, the reduction in the energy gap increases OFF current (I_{OFF}) more prominent as compared to ON current (I_{ON}). This in turn deteriorates the ON/OFF current (I_{ON}/I_{OFF}) ratio. It is also observed that, even at $V_{diff} = 0$ V, the ON/OFF current ratio of W15 is insufficient for international roadmap for semiconductors (ITRS) switching requirement.

To understand reason for small ON/OFF current ratio and to explore the effect of V_{diff}, Fig. 5.2(b) plots the current spectra at the OFF-state for three V_{diff}. It is evident that the OFF-state current is contributed by two current components: 1) the source to channel BTBT (S-C tunneling), and 2) the channel to drain BTBT (C-D tunneling). The S-C tunneling current is controlled by gate voltage, but the C-D tunneling current is due to the limited energy gap opening, which causes the valance band edge of the channel region elevated higher than the conduction band edge of the drain region. This contribution of the C-D tunneling under OFF-state increases the OFF current and hence reduces the ON/OFF current ratio. Moreover, the presence of the C-D tunneling current under OFF-state reduces the gate electrostatic control, and thus degrades subthreshold swing (SS). On the other hand, a larger V_{diff} allows more C-D tunneling current as well as S-C tunneling current under OFF-state, which further degrades the ON/OFF current ratio. Therefore, we have preferred a $V_{diff} = 0$ V, and explored other device design parameters to boost ON/OFF current ratio.

Fig. 5.3(a) shows that decreasing of V_{DS} is one way to improve the ON/OFF current ratio. A lower V_{DS} lift up the conduction band edges (CB) of the drain above the valance band edges (VB) of the channel, which reduces the contribution of the C-D tunneling current and hence significantly decreases the OFF current. In contrast, the ON current is unaffected with decreasing of V_{DS} as it is only due to the S-C tunneling current. The reduction in the C-D tunneling current with V_{DS} also leads to symmetric currents both for positive and negative V_{GS}. It makes BLGNR-TFET a better ambipolar device with a same threshold voltage both for p-mode and n-mode. A TFET can only provide a steep inverse substhreshold slope if the band gaps in source and channel act as band pass filter. This can be obtained only in the case of a large band gap materials in source and drain regions. Otherwise, the carriers are tunnel between the conduction and valence band and this is the main source for leakage. So any means to lower leakage needs to work on the band gap in source and drain. A smaller V_{ds} can only mitigate the impact of a small band gap in the channel.

TH-1608_11610201

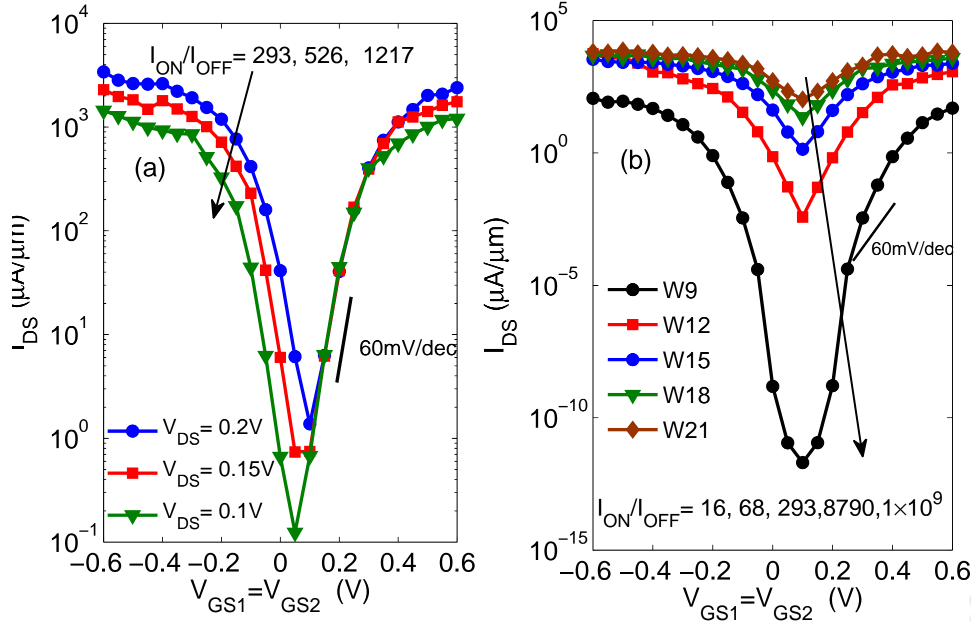


Fig. 5.3: Impact of drain voltage and channel width on device operation. (a) Transfer characteristics of W15 (1.87 nm wide) BLGNR-TFET for various V_{DS} at $V_{diff} = 0$ V, and (b) Transfer characteristics for various bilayer ribbon widths at $V_{DS} = 0.2$ V.

An alternate way to boost ON/OFF current ratio is by decreasing the bilayer ribbon width. The previous studies on MLGNR devices have shown significant improvement in the ON/OFF current ratio with reducing the ribbon width [53, 126]. Fig. 5.3(b) shows the transfer characteristics for 3M family of BLGNR devices. With decreasing the bilayer ribbon width (W), the I_{OFF} is decreased significantly due to an increase of the energy gap, while the I_{ON} is also decreased due to reduce in the low-energy subbands. The more prominent decrease in the OFF current compared to the ON current, largely increases the ON/OFF current ratio. It may be noted that the ON/OFF current and minimum SS for smallest device width (W9 channel) are about 1.735×10^9 and 11 mV/dec, but the ON current is merely 3.5 nA/μm. It is also found that the ON/OFF current ratio in BLGNR devices change appreciably with channel width due to larger variation in the energy gap. Therefore, BLGNR devices require careful selection of channel width, and very narrow width cannot be a better choice for digital circuits due to low ON current.

Subsequently, we have examined that an appropriate selection of device parameters, such as drain underlap, drain overlap and doping profile, can be an efficient way to achieve lower OFF current without considerably degrading ON current. Importantly, these particular device parameters can be controlled easily with present semiconductor processing methods. The underlap or overlap is always

TH-1608_11610201

present in all fabricated graphene devices and controlling their dimensions is also easier. Besides, the substitutional doping on the reactive edges of nanoribbon is an efficient method to achieve the desired doping in nanoribbon based devices [42].

Fig. 5.4 shows the transfer characteristics and corresponding band profile at $V_{GS1} = V_{GS2} = 0.1$ V for six different BLGNR-TFET structures: 1) nominal device (ND), 2) ND with 5-nm drain underlap (UL), 3) ND with 5-nm drain overlap (OL), 4) modified doping (MD) fractions, 5) MD fractions device with 5-nm underlap (MD+UL), and 6) MD fractions with 5-nm overlap (MD+OL). Correspondingly, Table 5.1 summarizes the important performance parameters for all six structures. To study the impact of underlap, the gate length is fixed at 20 nm, but the channel length is increased to 25 nm. Similarly, the drain region length is extended to 20 nm for the case of drain overlap.

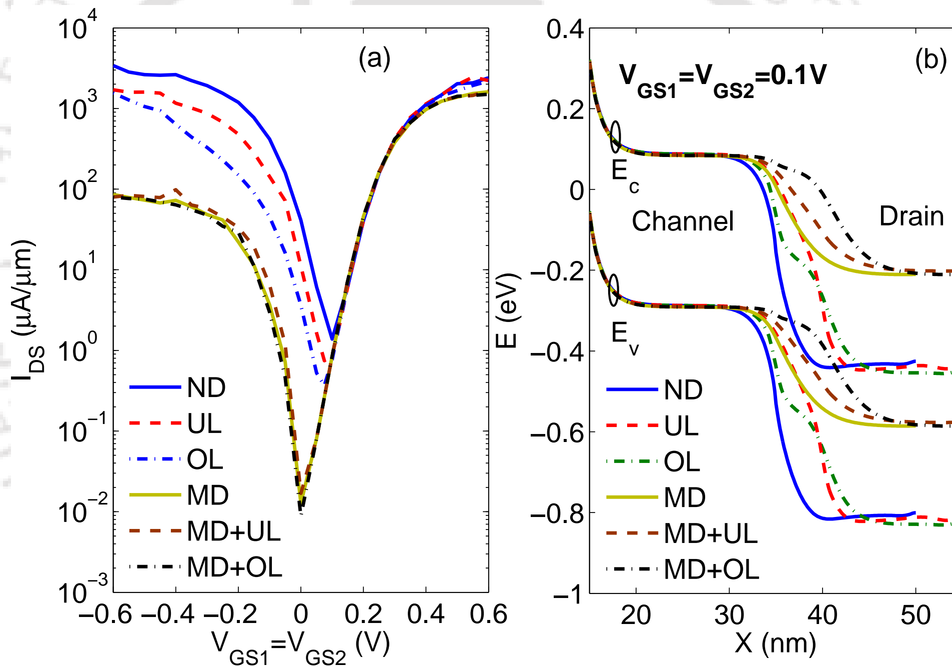


Fig. 5.4: Influence of device design parameters on W15 (1.87 nm wide) BLGNR-TFET operation. (a) The transfer characteristics at $V_{DS} = 0.2$ V and (b) corresponding band profile at the channel and drain region at $V_{GS1} = V_{GS2} = 0.1$V for six different structures: 1) nominal device (ND), 2) device with 5-nm drain underlap (UL), 3) device with 5-nm drain overlap (OL), 4) device with modified doping (MD) fractions, 5) MD fractions device with 5-nm underlap (MD+UL), and 6) MD fractions device with 5-nm overlap (MD+OL).

It is observed from Fig. 5.4(b) that both the drain side underlap and overlap over the nominal device increase the band-bending distance at channel-drain (C-D) junction, which in turn widens the C-D junction barrier width. The wider barrier width leads to exponential decrease in the C-D tunneling current. This in turn decreases OFF current without affecting ON current and hence increases ON/OFF

TH-1608_11610201

Table 5.1: Performance comparison of Six different device structures, at $V_{DS} = 0.2$ V.

Structures	$I_{ON}(\mu A/\mu m)$	I_{ON}/I_{OFF}	$SS_{min}(mV/dec)$	$SS_{avg}(mV/dec)$
ND	404	293	61	81
UL	422	488	58	74
OL	353	496	52	74
MD	45	2707	48	58
MD+UL	45	3619	49	56
MD+OL	45	5180	48	53

ND: nominal device, UL: 5-nm drain underlap, OL: 5-nm drain overlap, and MD:Modified doping fractions.

current ratio. Besides, the drain overlap more effectively pin the potential energy in overlap region of the drain, which largely suppress the C-D tunneling. As a result, ON/OFF current and SS for overlap case is better than underlap case, as shown in Table 5.1.

The tunneling barrier at the C-D junction can be widened effectively by designing the channel and drain region doping level such that the conduction band edge of the drain is located above the valance band edge of the channel. This type of band profile is achieved by decreasing the drain doping and by lightly doping the channel region with same dopant type as that of the drain region. Therefore, an appropriate drain doping fraction can be $[f_d = f_s/8]$, and the channel region can be doped to n-type with a doping fraction $[f_{ch} = f_s/80]$, where f_s the source doping fraction. It is observed from Fig. 5.4(a) and (b) that modifying doping fractions (MD) considerably increases band-bending at channel-drain (C-D) junction and leads to an extraordinary ON/OFF current ratio of 2707 with an minimum SS of 48 mV/dec. Although the S-C tunneling current is unaffected by MD, the ON current is decreased due to the left-side shift of V_{GSmin}, where the OFF state has minimum contribution of the S-C tunneling current.

Having made an improvement by a suitable MD, it is also shown that 5-nm drain underlap and overlap upon an MD device is further reduced the C-D tunneling current from OFF state, which improves the ON/OFF current ratio without affecting the SS. The impact of overlap and underlap in MD is very similar to that observed in nominal device case. Therefore, modified doping fraction with drain overlap can be an effective design strategy to boost ON/OFF ratio and reduce SS in any material TFET.

The performance improvement with MD+OL scheme over the nominal device is examined by

TH-1608_11610201

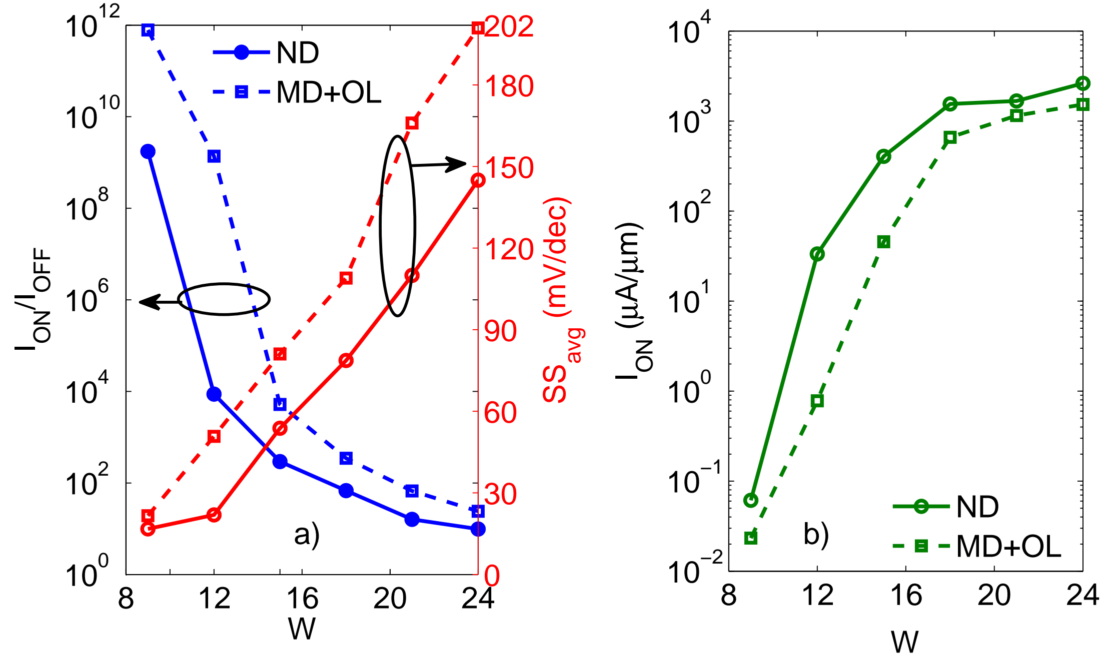


Fig. 5.5: Performance comparison of MD+OL (dash line) with nominal device (solid line), at $V_{DS} = 0.2$ V. (a) I_{ON}/I_{OFF} and average subthreshold swing (SS), and (b) I_{ON} as a function bilayer ribbon width.

comparing the ON/OFF current ratio, average SS and ON current for various device widths, in Fig. 5.5. For W≤12, MD+OL scheme is significantly higher ON/OFF current ratio and lower SS, but their ON current are lower than that of the nominal device. However, MD+OL scheme provides advantage for 12<W< 18. For such widths, MD+OL scheme brings in $I_{ON}/I_{OFF} > 10^3$ and an $SS_{avg} < 80$ mV/dec, where the nominal device has poor performance due to the very small energy gap. However, the performance improvement with MD+OL scheme is not significant for ribbons wider than W21. This is because the confinement-induced energy gaps are considerably smaller for such widths (Table **??**).

Subsequently, the benefits of BLGNR-TFET over MLGNR-TFET for logic applications can be better estimated by comparing the ON current, intrinsic speed and switching energy as a function of ON/OFF current ratio.

5.3.2 BLGNR-TFET Versus MLGNR-TFET

Fig. 5.6 shows the ON current, intrinsic delay time and power-delay product (PDP) as a function of ON/OFF current ratio among BLGNR-TFET and MLGNR-TFET for different ribbon widths. These results are divided into two groups: 1) narrow widths (left side): W21, W18 and W15, which having

TH-1608_11610201

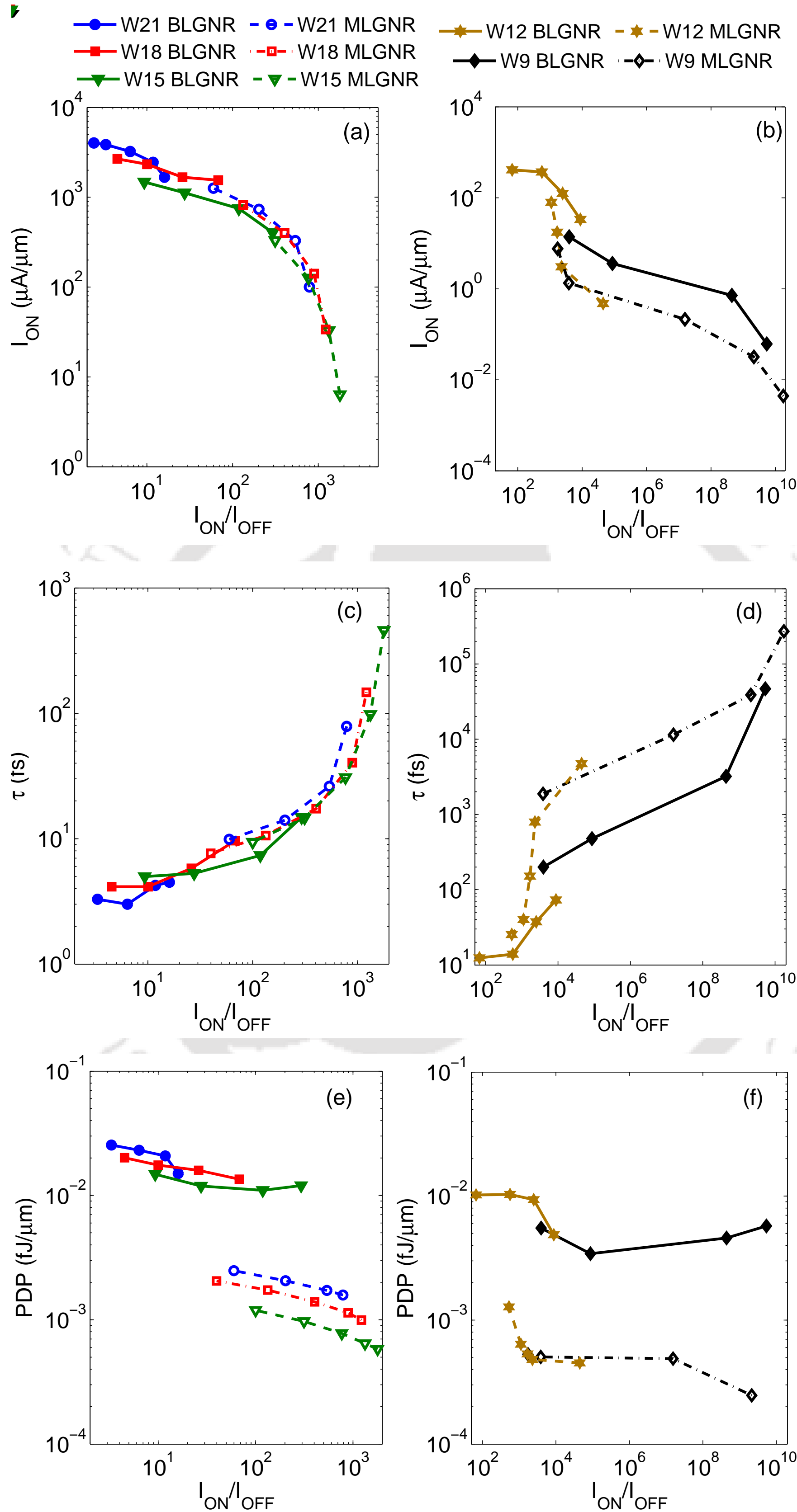


Fig. 5.6: Performance comparison between BLGNR-TFET and MLGNR-TFET at $V_{DS} = 0.2$ V. (a)-(b) I_{ON} versus I_{ON}/I_{OFF}, (c)-(d) Intrinsic device delay (τ) versus I_{ON}/I_{OFF}, and (e)-(f) Power delay product (PDP) versus I_{ON}/I_{OFF} for W21, W18 and W15 (left side) and W12 and W9 (right side). These parameters are calculated only for n-type branch of transfer characteristics.

TH-1608_11610201

moderate ON/OFF current ratios, and 2) very narrow widths (right side): W12 and W9, which having significant ON/OFF current ratios. The ON and OFF currents for each BLGNR device are obtained from the transfer characteristics in Fig. 5.3(b) by sweeping a constant $V_{GS} = V_{DD}$ window with 0.05 V for n-type branch. Similar procedure is adopted for the case of MLGNR-TFET.

It is observed from Fig. 5.6(a) that narrow BLGNR devices have higher ON current compared to MLGNR devices at small ON/OFF current ratio. Surprisingly, the ON current of W15 BLGNR is comparable to that of W21 and W18 MLGNR devices, even though MLGNRs have larger the ON/OFF current ratio at the same ON current. At narrow width, BLGNR fails to produce an advantage over MLGNR, in term of ON current. However, BLGNR devices have produce advantage over MLGNR for very narrow width, as shown in Fig. 5.6(b). At very narrow width, BLGNR devices have provided about 2-8× higher ON current with the same ON/OFF current ratio than that of MLGNR devices. The reason for better ON current is that the reduced energy gap accompanied by smaller carrier effect mass in BLGNR results in more low energy states, which allows higher tunneling efficiency.

The intrinsic device delay, which measures the switching speed of a device, is computed as $\tau = (Q_{ON} - Q_{OFF})/I_{ON}$, where Q_{ON} and Q_{OFF} are the overall charges induced in the device at the ON-state and OFF-state, respectively [122]. It is observed from Fig. 5.6(c) and (d) that the BLGNR has smaller intrinsic device delay time compared to MLGNR at same channel width. The τ vs I_{ON}/I_{OFF} curve inversely follows the I_{ON} vs I_{ON}/I_{OFF} curve (Fig. 5.6(a) and(b)), even the differences in delay between BLGNR and MLGNR devices are nearly equal to their differences in ON current for same ON/OFF current ratio.

The PDP, which estimates the switching energy of the device, is calculated as $PDP = (Q_{ON} - Q_{OFF})V_{DD}$ [122]. It is observed from Fig. 5.6(e) and (f) that BLGNR devices have around 1-5× higher switching energy than that of MLGNR devices at same channel width. This is because the amount of charge induced in switching operation of BLGNR is marginally higher than MLGNR. When moving from lower ON/OFF to higher ON/OFF current ratio, PDP decreases because the charge density reduces in ON to OFF state transition. Therefore, at very narrow channel widths, BLGNR can be a better device over MLGNR for digital applications with higher ON current and higher intrinsic speed.

The parasitic capacitances and resistances are neglected in our simulation, but in the real device, these will further degrade the τ and PDP. To get an approximate estimation of the extrinsic τ and PDP, an enhancement factor of 1.3-1.6× can be applied to BLGNR-TFET as ITRS 2009 estimated

TH-1608_11610201

similar enhancement factor to the total capacitance for multigate MOSFET [53].

5.4 Analog/RF Performance

The main demand with graphene based transistor for analog/RF applications is to realize good saturation in the output characteristics without lowering the current values. To observe the impact of energy gap on the current saturation, we have investigated W15 and W30 BLGNR devices, where W15 and W30 represent the width of 1.87 and 3.74 nm. Instead of large different gate voltage, we selected $V_{diff} = 0$V for performance analysis and optimization, so the C-D tunneling contribution is minimum. Furthermore, MLGNR devices are not used here for performance comparison as they are not very popular for RF applications due to their low ON current.

5.4.1 Output Characteristics

Fig. 5.7 shows the output characteristics of W15 and W30 devices for various positive V_{GS}, where $V_{GS} = V_{GS1} = V_{GS2}$. Unlike large-area graphene TFET (Fig. 3.2), BLGNR-TFETs have exhibited better current saturation for intermediate V_{DS} values. It is observed that W15 device has wider saturation region than that of W30 for intermediate V_{DS}, while the quasi-linear increment in the current is exhibited in both devices at high V_{DS}. The underlying physics behind this behavior can be understood by observing the contribution of current components at different V_{DS}. Fig. 5.7(b) and 5.7(d) show the current spectra for W15 device and W30 device, respectively at $V_{GS} = 0.4$ V for different V_{DS}. It is observed that the current saturation is possible for V_{DS} values where the current is essentially due to the S-C tunneling current, whereas the weak saturation or quasi-linear behavior is appeared for V_{DS} values where the contribution of C-D tunneling current becomes significant. The contribution of the C-D tunneling increases linearly with V_{DS}, which causes pile-up of holes in the channel as these holes do not contribute to the current flow. Consequently, it gives rise to quantum capacitance of form $C_Q = 2/h \times \sqrt{8m^*/(E_{ch} - E_{FD})}$ [132], where E_{ch} is the channel potential energy and E_{FD} is the drain Fermi level. When C_Q becomes comparable to C_{ox}, it lowers channel potential energy and leads to linear increase in the S-C tunneling current with V_{DS}, as shown in Fig. 5.7(d). As a result, the overall current increases linearly at high V_{DS}. Due to a small energy gap in W30 device, the contribution of the C-D tunneling becomes significant even from low V_{DS}, which narrows the V_{DS} window for current saturation.

The quasi-linear increment in the current may result in larger variations in the intrinsic gain with

TH-1608_11610201

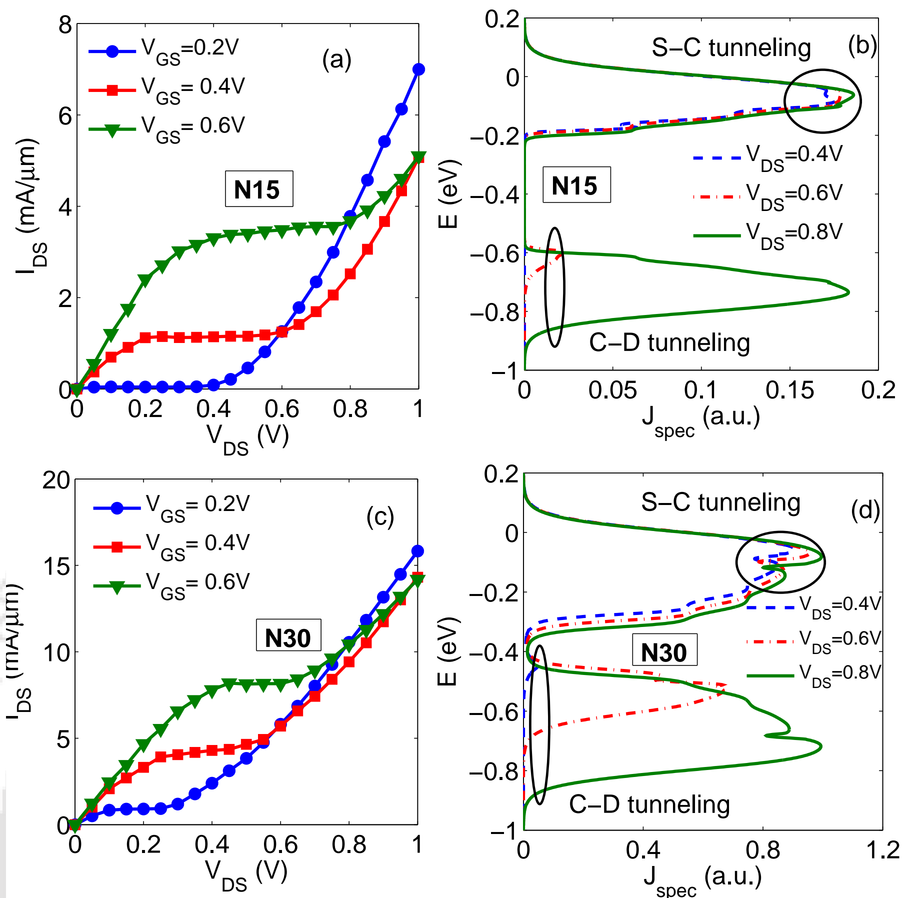


Fig. 5.7: Output characteristics for different positive V_{GS} for (a) W15 BLGNR and (b) W30 BLGNR, where $V_{GS} = V_{GS1} = V_{GS2}$.

respect to V_{DS}. These variations in the intrinsic gain might produce distortions in the amplification or even reduce the effective gain. We have examined that if the proposed modified doping with 5-nm drain overlap (MD+OL) design strategy in digital section (section 5.3) can also be significant to extent the V_{DS} window for saturation.

Fig. 5.8(a) and (b) show the output characteristics of W15 and W30 devices, respectively for nominal and MD+OL cases at different positive V_{GS}. It is observed from Fig. 5.8(a) that MD+OL for W15 device considerably suppresses the C-D tunneling current, and reduces the quasi-linear increment at larger V_{DS}. It is seen from Fig. 5.8(b) that MD+OL scheme for W30 device enhances the current saturation at moderate V_{DS}, but the quasi-linear increment is still present. It is more pronounced at larger V_{GS} that MD+OL decreases the current density slope at low V_{DS} values and marginally increases the current density at moderate V_{DS}. At low V_{DS} and high V_{GS}, the conduction band edge of the drain region is lifted above the conduction band edge of the channel region because of relatively

TH-1608_11610201

low doping concentration in the drain region. This condition in turn decreases the contribution of S-C current and hence reduces the current density. At moderate V_{DS}, the doping in both the regions becomes comparable, which causes the drain voltage to drop across the C-D junction. This case in turn increases the contribution of S-C tunneling current and hence increases the overall current density. At larger V_{DS} the drop across the channel region becomes smaller, because of relatively low doping concentration in the channel region. This in turn improves the saturation in the output characteristics. However, due to a small energy gap in W30 device, the C-D component of current is still present at high V_{DS}, and it weakens the current saturation.

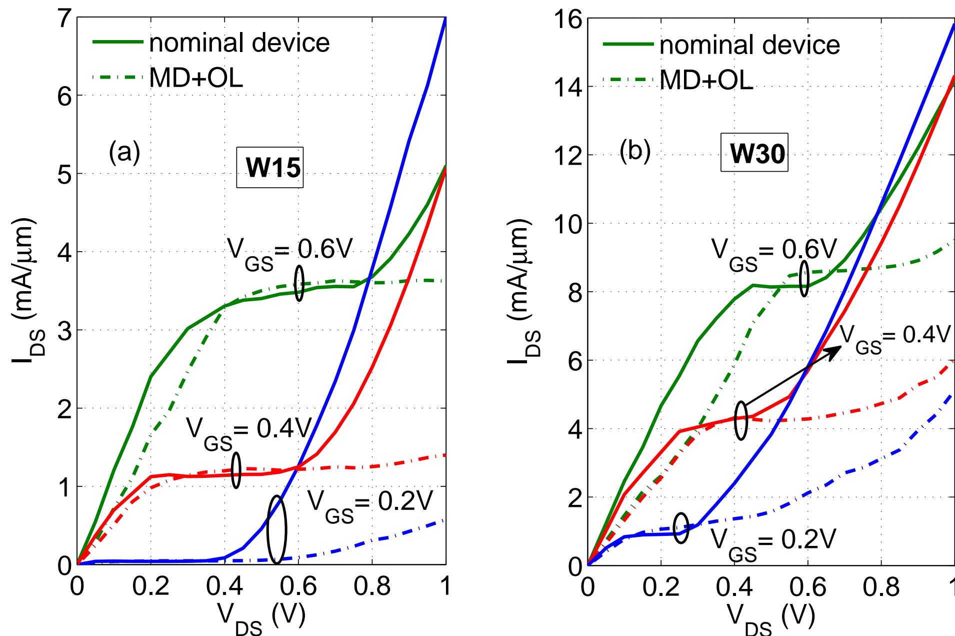


Fig. 5.8: Output characteristics of nominal device (ND) and modified doped device with 5-nm drain overlap (MD+OL) for (a) W15 BLGNR and (b) W30 BLGNR, where $V_{GS} = V_{GS1} = V_{GS2}$.

Therefore, proper designing of doping profile with a suitable drain overlap is also a useful design strategy to improve the analog performance metrics of any TFET. It is noted that the drain overlap may increase the drain capacitance, which might degrade the extrinsic RF performance of BLGNR-TFET.

5.4.2 Intrinsic Analog/RF Performance Metrics

The V_{GS} dependency on transconductance (g_m), output conductance (g_{ds}), intrinsic gain (A_{V0}) and cutoff frequency (f_T) is presented in Fig. 5.9. It is observed from Fig. 5.9 that the $g_m - V_{GS}$ curve has negative values for larger positive gate voltage range. This is because larger contribution of C-D tunneling current is shifted the $V_{GS,min}$ towards more positive gate voltage. In a nominal device,

TH-1608_11610201

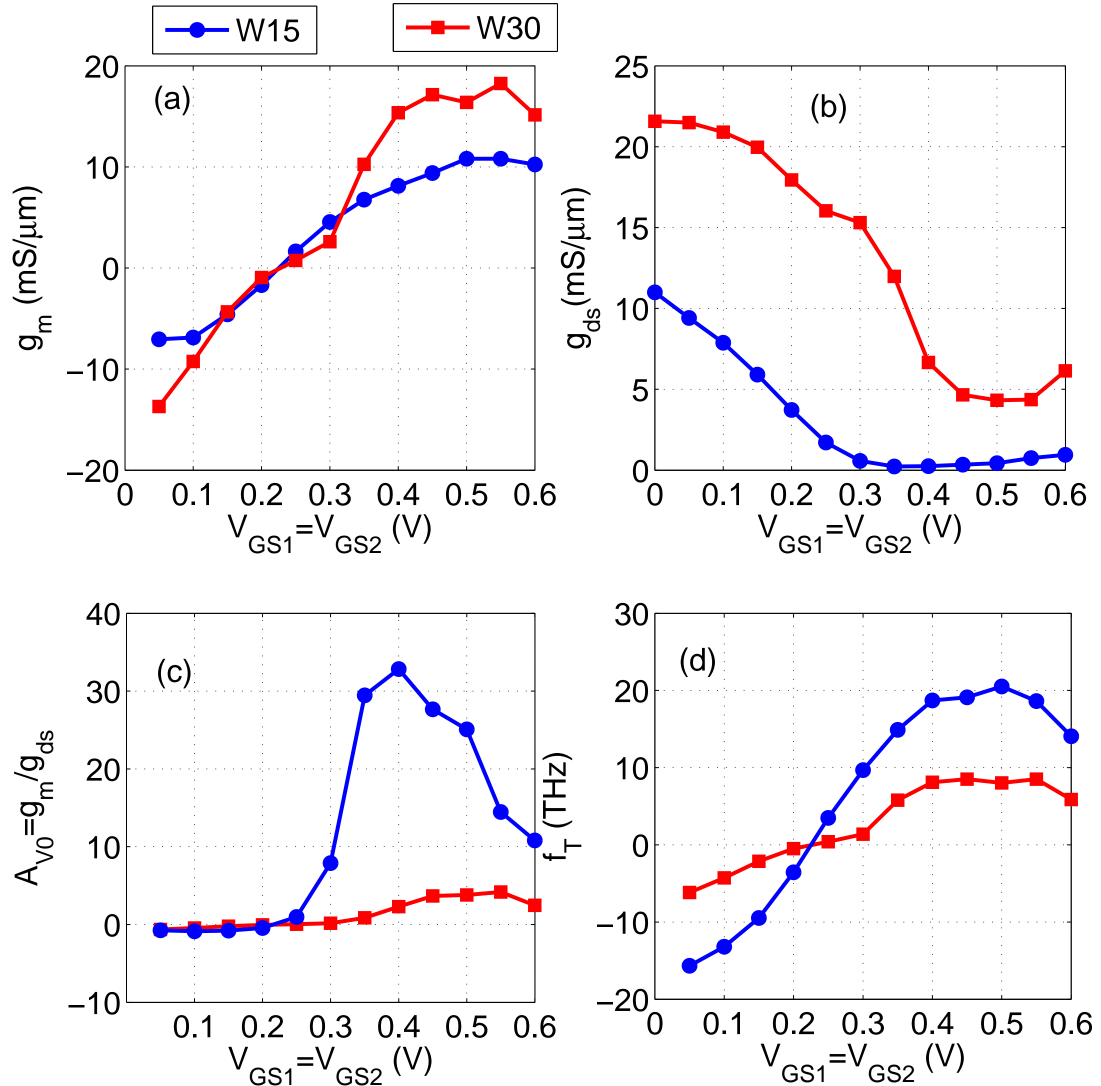


Fig. 5.9: Impact of V_{GS} on the intrinsic analog performance metrics, at $V_{DS} = 0.4$ V. (a) transconductance (g_m), (b) output conductance (g_{ds}), (c) intrinsic gain (A_{V0}), and (d) intrinsic cutoff frequency (f_T) as function of V_{GS}.

the $V_{GS,min}$ is generally occurred at $V_{GS,min} = V_{DD}/2$. However, the peak in g_m of W15 device is appeared, when the S-C tunneling contribution becomes significant. Fig. 5.9(b) shows that the output conductance (g_{ds}) is inversely followed the g_m curve.

It is seen that a higher drive current with W30 device results in approximately 2× higher g_m than that of W15 device, but the weak saturation with W30 device causes considerably smaller g_{ds} than that of W15 device. The smaller g_{ds} with W15 device results in nearly 7× smaller peak intrinsic gain than that of W30 device. Surprisingly, the cutoff frequencies of W15 device are also considerably higher than that of W30 device. The reason larger cutoff frequency is that gate capacitance of W15 device

TH-1608_11610201

is considerably smaller than that of W30 device. The lower density-of-states (DOS) in W15 device brings in small quantum capacitance. As a device is operating under the quantum capacitance limit ($C_{OX} >> C_Q$), the smaller quantum capacitance (C_Q) produces lower gate capacitance.

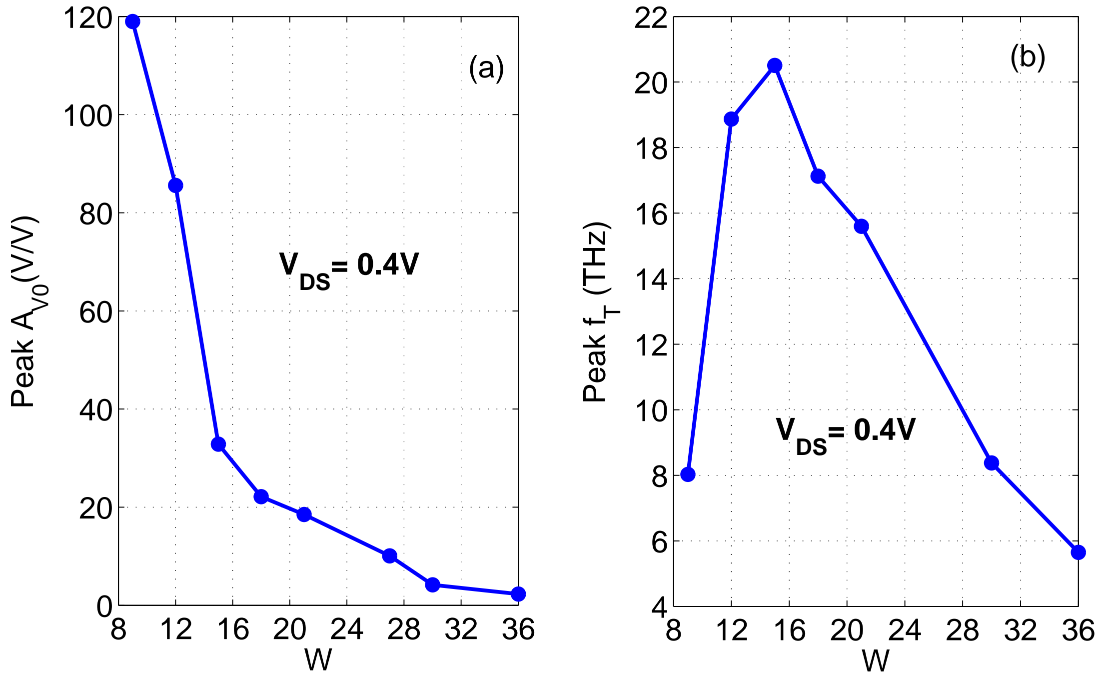


Fig. 5.10: Impact of channel width on intrinsic analog/RF performance metrics. (a) The peak intrinsic gain and (b) the peak cutoff frequency as a function of bilayer ribbon width (W), at $V_{DS} = 0.4$ V.

Fig. 5.10(a) and (b) show the peak intrinsic gain and peak cutoff frequency, respectively, as a function of channel widths (W), at $V_{DS} = 0.4$ V. With the decreasing the bilayer ribbon width, the peak intrinsic gain increases largely due to the improved current saturation. However, the peak cutoff frequency is first increased with respect to a decreasing bilayer ribbon width, then it is decreased for very narrow widths. This behavior is because, the g_m becomes comparatively smaller than gate capacitance at very narrow widths. This can attribute from $I_{DS} - V_{GS}$ curve shown for different W in Fig. 5.3(b) that the drive current becomes much smaller for W9 and W12 devices compared to other devices. Such trend in f_T with ribbon widths is opposite to that finds in vertical GNR tunnel FET, where the cutoff frequency shows consistently improvement with decreasing the ribbon width [58]. Therefore, it can be noted that the channel width of BLGNR-TFET has the more dominant effect on the analog and digital performance metrics, and selecting the optimum width with proper device parameters would bring substantial advantages.

TH-1608_11610201

Having estimated the intrinsic analog/RF performance metrics, it is became important to analyze the RF performance metric associated with the parasitic capacitances and resistances. This will give a rough estimation of RF performance in the realistic device.

5.4.3 RF Performance with Parasitics

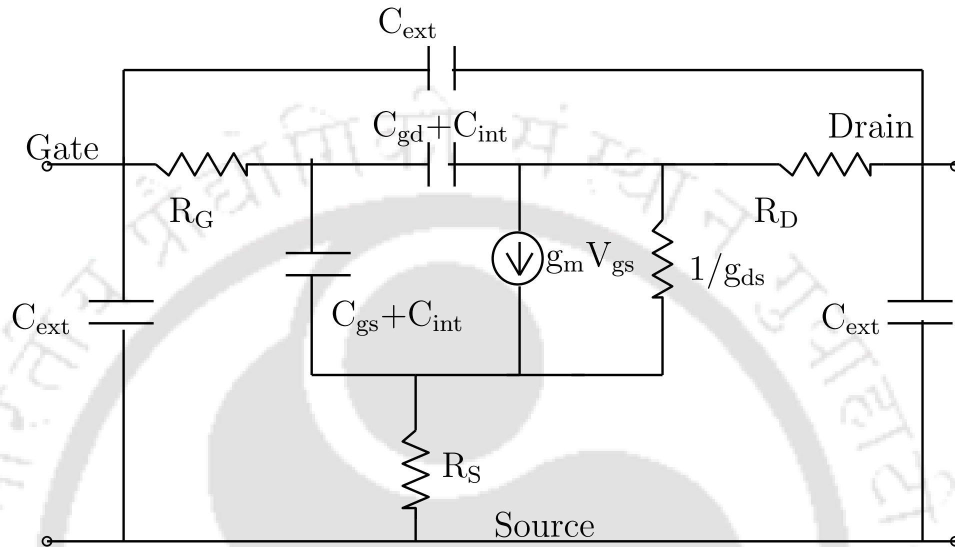


Fig. 5.11: The small-signal equivalent circuit model used to explore the impact of additional external parasitics on the RF performance metrics of BLGNR-TFETs.

Table 5.2: Extrinsic RF Figure of Merits for W15 and W30 BLGNR-TFETs at internal V_{DS} = 0.4 V and V_{GS} = 0.4 V.

Attribute	$R_S = R_D = 100$ Ω-μm, $R_g = 0$ Ω-μm, $C_{\text{int}} = C_{ext} = 0$ fF/μm		$R_S = R_D = 100$ Ω-μm, $R_g = 4$Ω-μm, $C_{\text{int}} = C_{ext} = 0$ fF/μm		$R_S = R_D = 100$ Ω-μm, $R_g = 4$Ω-μm, $C_{\text{int}} = C_{ext} = 0.1$ fF/μm	
	W15	W30	W15	W30	W15	W30
GBW (THz)	75	7.5	72	7	4.4	2.5
f_T (THz)	16	2.3	16	2.3	1.6	0.951
f_{max} (THz)	40	6.8	37	6.8	6.6	4

We now investigate the impact of external parasitic capacitances and resistances on the RF performance metrics, such as unity current gain frequency or cutoff frequency (f_T), unity power gain frequency or maximum oscillation frequency (f_{max}) and gain-bandwidth product (GBW). Fig. 5.11 presents the small-signal model under usual quasi-static approximation, which is widely used to explore the high frequency performance of MOSFET [133]. The electrode resistance are taken account by introducing source and drain series resistances (R_S and R_D) , and the gate resistance (R_G) . The extra

TH-1608_11610201

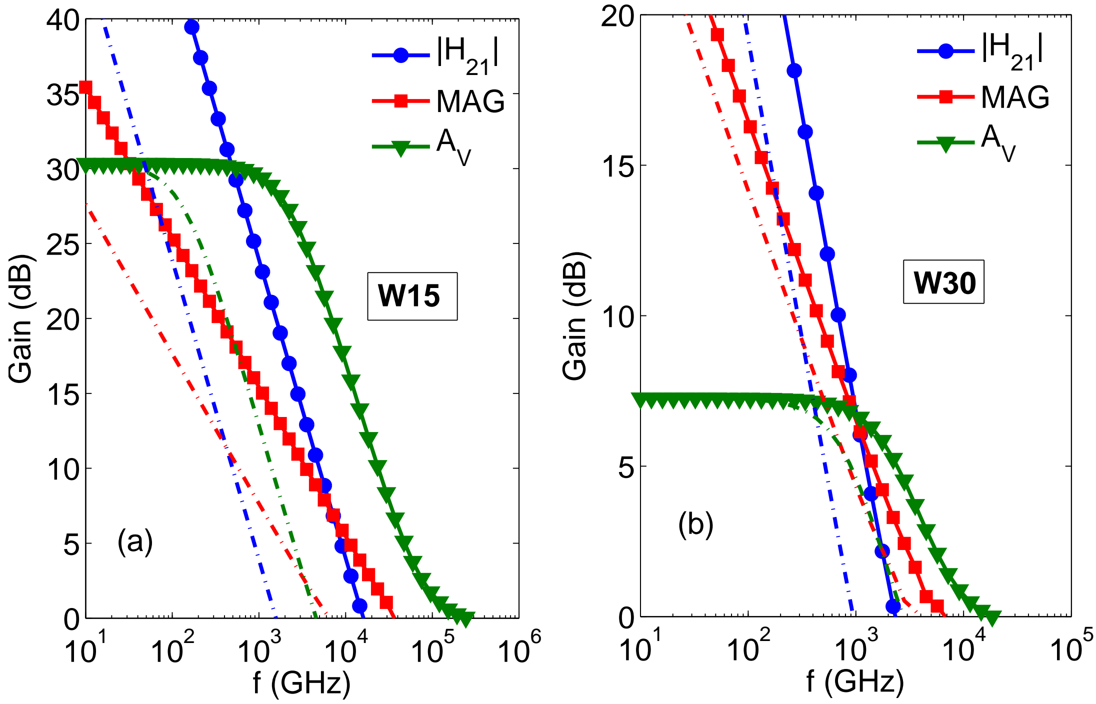


Fig. 5.12: Impact of parasitics on RF figure of merits. Plot of short circuit current gain ($|H_{21}|$), maximum available gain (MAG), and voltage gain with open circuit load (A_v) in the presence of parasitics for (a) W15 device and (b) W30 device. Devices are biased at $V_{GS} = 0.4$V and $V_{DS} = 0.4$V, which is the maximum A_{V0} and f_T bias point in Fig. 5.10 for W15 device. The sold lines are obtained with $R_S = R_D = 100$ Ω-μm, $R_g = 0$ Ω-μm, $C_{\text{int}} = C_{ext} = 0$ fF/μm and the dash lines are obtained with $R_S = R_D = 100$ Ω-μm, $R_g = 4\Omega$-μm, $C_{\text{int}} = C_{ext} = 0.1$ fF/μm.

parasitic capacitances between the internal and the external terminals of the gate and the source/drain electrodes are given by C_{int} and C_{ext}, respectively. The external parasitic capacitances and resistances values are taken to be the minimum values possible for graphene-based transistors [97, 120, 134]. The g_m and g_{ds} are calculated from the obtained DC current values, while the C_{gs} and C_{ds} are computed by separating the charge contribution relative to injection from source/drain of the ballistic transport model. To compute extrinsic RF performance metrics of BLGNR-TFETs, Y-parameters are derived from the small signal model.

Fig. 5.10 shows the short circuit current gain $H_{21} = |Y_{12}/Y_{11}|$, maximum available gain (MAG) [135], and voltage gain with open circuit load $A_V = |Y_{21}/Y_{22}|$ as a function of frequency without parasitic capacitances (solid line) and with (dash line) parasitic capacitances at $V_{GS} = V_{DS} = 0.4$V for (a) W15 device and (b) W30 device. Table 5.2 further summarize the frequency figure of merits of W15 and W30 devices for different parasitic conditions, which are obtained by extrapolating the magnitude of curves in Fig. 5.12 to unity (0 dB). It is observed that the RF figure of merits for W15

TH-1608_11610201

and W30 devices are well above 1 THz even with the parasitic conditions included, except the f_T of W30 device is nearly about 1 THz for worst case parasitic values. The f_T is insensitive to the gate resistance, but f_{max} and GBW are degraded in the presence of gate resistance. It is observed that RF performance metrics of W15 device is strongly degraded in the presence of the parasitic values compared to the W30 device. The reason is because the internal capacitance values in W15 device becomes comparatively smaller than the external capacitance values. The intrinsic RF figure of merits for W15 device is considerably higher than W30 device; however, they become comparable to that of W30 device for worst case parasitic values. All reported values of f_{max} for both devices are higher than that obtained values in the fabricated (40-70 GHz) [136] and simulated (1.5-3 THz) graphene transistors [120] as well as the carbon nanotube FET [97]. Therefore, considered BLGNR-TFETs have offered the potential to achieve intrinsic and extrinsic device operation in THz range and attaining such frequency limits is essentially depended on the experimental advancement of these devices.

5.5 Summary

The intrinsic performance potential of BLGNR-TFETs has evaluated using the atomistic quantum simulations for analog and digital applications. At very narrow ribbon widths, BLGNR-TFET has found advantageous than MLGNR-TFET as it can deliver higher ON currents, lower intrinsic device delay, nearly same ON/OFF current ratio at the cost of marginally higher switching energy. It has found that the narrow width BLGNR-TFETs are limited by their moderate energy gaps; however, an appropriate selection of the channel and the drain doping fractions with drain overlap can offer an $I_{ON}/I_{OFF} > 10^3$ and $SS_{avg} < 90$ mV/dec at $V_{DD} = 0.2$ V. The analysis of BLGNR-TFET has shown considerably higher intrinsic gain for smaller channel widths, whereas the cutoff frequency decreases at very narrow widths. The narrow width BLGNR-TFET promises potential characteristics for ultra-low power digital and analog integrated circuits operating at terahertz (THz) frequencies.

TH-1608_11610201

TH-1608_11610201

6

Conclusions and Future Directions

Indian Institute of Technology Guwahati

Contents

6.1 Conclusion 100
6.2 Future Directions 102

TH-1608_11610201

6.1 Conclusion

As the devices based on graphene are in the development stage, this work has contributed in a numerous way to the field of device modeling, and their applications. The purposes of this work are to a develop simulation tool for graphene-based devices, and to use that tool to understand device behavior and to explore device optimization strategies. The major contributions and the respective conclusions are as follows.

- The initial work involves the development of a quantum transport model that reduces the computational burden without losing accuracy.
  - The 1-D elementary cell assumption has led to the development of a unique tight-binding Hamiltonian matrix for graphene-based materials, which allows one to use the same transport equations for all graphene-based transistors with only small modifications and thus easier implementation of NEGF equations for graphene-based FETs.
  - Simplification of coupling matrices with 1×1 size provides easy solution for self-energy matrices and Green's function such that it largely reduces the computational time for quantum-transport simulation of G-FET and GNR-FET. This allows the use of the developed quantum transport model for device optimization and exploration of circuit performance parameters.
- The dominance of BTBT current with a small carrier effective mass and direct energy gap makes graphene a most suitable material for use in tunnel FET (TFET). As conventional graphene field-effect transistor (C-GFET) suffers from weak current saturation, a planar graphene tunnel field-effect transistor (T-GFET) is explored for analog/RF applications.
  - T-GFET has shown 20% higher peak intrinsic gain without significantly degrading the cutoff frequency compared to C-GFET, as shown in Table 6.1.
  - T-GFET has weak current saturation similar to C-GFET, but an appropriate selection of device parameters, like oxide thickness or drain overlaps or channel & drain doping concentrations, significantly enhances the current saturation and consequently reduces the V_{DS} dependency of intrinsic gain. The optimized (Modified doping with drain overlap) T-GFET is expected to be a promising device for high frequency multiplier and RF mixer

TH-1608_11610201

circuits; however it needs further performance improvement to build RF amplifiers and oscillators.

– T-GFET offers several advantages, and is expected to be an alternative candidate to C-GFET for analog/RF applications.

Table 6.1: Comparison of graphene-based MOSFETs with Si-MOSFET and ITRS 2014 prediction

Attribute	ITRS 2014 [75]	Si-MOSFET [76]	C-GFET	T-GFET$^{\diamondsuit}$	BLG-FET [74]	BLGNR-FET*	BLGNR-TFET*
L_{ch} (nm)	18	29	25	40	25	20	20
g_m (mS/μm)	–	1.3	30	25	8	10	10
A_{V0} (μA/μm)	–	20 dB	1 dB	3 dB	20 dB	25 dB	38 dB
f_T (GHz)	480	485	4,000$^{\Theta}$	3,500$^{\Theta}$	1,500	20,000 $^{\Theta}$	1,600
f_{max} (GHz)	540	–	–	–	–	–	6.6

$\diamondsuit$: Proposed Work; $\star$: Proposed work with W15 device; Θ: Intrinsic value;

- Due to significant energy gap opening by the confinement and vertical symmetry breaking, FET with BLGNRs is evaluated for digital and analog applications.

  – The BLG-FET with chemically doped source and drain regions has shown promising ON current even at very narrow width, but the ON/OFF current ratio has only become significant at very narrow ribbon width. The BLGNR-FETs can overcome the small ON current problem of the MLGNR-FETs; however, they require much narrower ribbon width to achieve substantial ON/OFF current ratio.

  – An electrostatically doped BLGNR-FETs through a back gate is found to be a promising candidate for high frequency RF application with intrinsic gain greater than 20 dB and the intrinsic cutoff frequency in THz range.

- Motivated by the BLGNR-FET performance, a Tunnel FET with BLGNR is explored for low voltage digital and high frequency RF operations.

  – BLGNR-TFET exhibits good characteristics for ultra-low power digital and analog integrated circuits operating at terahertz (THz) frequencies.

  – Table 6.2 benchmarks the digital performance of BLGNR-TFETs with other material TFETs. The intrinsic delay and PDP are computed by traditional equations as $\tau = C_g V_{DD}/I_{ON}$ and

TH-1608_11610201

Table 6.2: Digital Performance comparison of BLGNR-TFET with other material TFETs operating under 0.5 V.

Attribute	Ge-Si [79]	BLG$^{\Theta}$ [56]	MLGNR$^{\diamondsuit}$	BLGNR*	MD+OL BLGNR†
L_{ch} (nm)	20	40	20	20	20
V_{DS} (V)	0.4	0.2	0.2	0.2	0.2
I_{ON} (μA/μm)	400	67	0.4761	33.373	0.7819
I_{ON}/I_{OFF}	4×10^5	2910	4×10^4	8790	1×10^9
SS_{min} (mV/dec)	80	35	15	44	16
C_G (fF/μm)	0.69	0.32	0.015	0.043	0.057
τ (fs)	690	955	3477	257	14580
PDP (fJ/μm)	0.11	0.013	0.0006	0.0017	0.0023

Θ: Bilayer graphene (BLG);
$\diamondsuit$: W12 device; $\star$: Proposed work with W12 device;
$\dagger$: W12 device with modified doping concentration and 5-nm drain overlap (MD+OL).

$PDP = C_g V_{VDD}^2$, respectively. For logic applications, BLGNR-TFET showed better performance of higher intrinsic speed (τ) and smaller switching energy (PDP) than other TFETs, except MLGNR-TFET. Moreover, optimized (MD+OL) device provides higher ON/OFF current ratio and nearly the same switching energy as compared to nominal BLGNR-TFET; however, it has considerably lower ON current, which reduces the device speed.

- For analog/RF electronics, BLGNR-TFET offered a peak intrinsic gain of around 38 dB and a cutoff frequency of about 18 THz. Table 6.1 shows that intrinsic gain and cutoff frequency of BLGNR-TFET are significantly higher than other graphene-based devices.

Simulations developed in this study can not be directly applied to practical use as the present devices suffer from defect and impurity, larger graphene-metal contact resistance and hence larger parasitic effects. The simulation is presented for ideal graphene-based transistors and obtained parameters are indicators only. The very rapid progress made by experimentalists would finaly decide whether these devices will be available in the near future.

6.2 Future Directions

Some of the future research scope is inspired by the following challenges arise out of the numerical modeling, device structures and circuit applications.

TH-1608_11610201

- **Device Modeling:** The transport models are developed by self-consistently solving 1-D transport equation and 2-D Poisson equation. Significant improvement is required at the modeling level to incorporate additional features.

  – To obtain more accurate electrostatic and to incorporate complex device structures, it is important to develop a 3-D Poisson solver, which runs efficiently and couples with the transport solver nicely.

  – Even though the fabrication of smooth edge is easier with recent advancement, real nanoribbons are always seriously affected by edge roughness, due to the difficulties in achieving edge control with atomic precision. Therefore, transport model of GNR-FET can be improved to take into account of edge bond relaxation and mode coupling for more realistic simulation.

  – The electronic properties in the experimental graphene-based devices influence by scattering due to impurity, defects, substrate interactions etc [137, 138]. Therefore, future studies should focus on understanding the interplay of these scattering mechanisms. The impact of electron-phonon scattering in graphene-FET and GNR-FET has done in previous literature [139–141]; however this analysis can be carried out in bilayer devices. The scattering analysis can also be done in TFET structure of graphene-based materials.

- **Device Performance:**

  – In the experiments reported so far, multiple nanoribbons devices are often fabricated as array with wide contacts. The simulation of an array field effect transistors with BLGNR can be a future study.

  – The developed self-consistent quantum transport simulation enables the extraction of intrinsic circuit elements of the device. To estimate the digital and analog performance metrics in realistic device, the extrinsic parasitic capacitances and resistance of device are to be incorporated, but accurate values of parasitic capacitances and resistance are not available in literature for bilayer devices. The open structure simulation of array field effect transistors with monolayer nanoribbon or BLGNR can be done using the CAD tools, such as COMSOL Multiphysics, ANSYS, etc to extract exact parasitic capacitance for these devices.

  – The gate tunneling current can be included in the simulation by adding the self-energy for the gate [142].

TH-1608_11610201

  - The effect of strain, which are practically important nowadays, can also be included. The strain in bilayer devices may be exploited to enhance the performance of the transistors [143].

- **Circuit Performance:** After achieving understanding of a single transistor, it is important to think about how to put many graphene-based transistors together and assess their circuit performance.

  - The developed model for graphene-FET and GNR-FETs enables fast simulation, so it can be used to investigate the performance such as delay and power for simple graphene-based digital and analog circuits. However, the quantum simulation for bilayer devices is computationally expensive. Therefore, a SPICE model, which describes the behavior of experimental transistors, needs to be developed and applied to investigate the circuit performance.
  - As BLGNR-TFET has shown promising performance for digital and analog applications, an inverter or ring oscillator can be designed to evaluate their dynamic performance, while common source amplifier and operational transconductance amplifier (OTA) can designed to verify their circuit performance for analog/RF applications.

TH-1608_11610201

A

Sancho-Rubio Algorithm

Indian Institute of Technology Guwahati

Contents

A.1 Sancho-Rubio Algorithm for BLGNR-FET 106

TH-1608_11610201

A.1 Sancho-Rubio Algorithm for BLGNR-FET

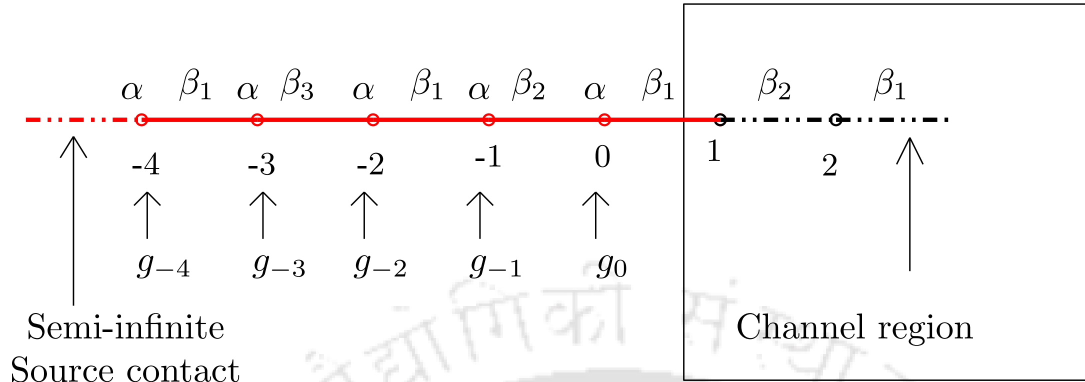


Fig. A.1: Schematic of BLGNR elementary cell in the source and the channel interface. The g_i is the surface Green's function for the i-th carbon ring inside the drain. The α is on-site energy, β_1, β_2 and β_3 are the first, second and third kind coupling matrix between neighboring rings, as described in section 2.3.2.

When the lattice has weak neighbourhood singularities, simple iterative scheme for calculating the surface Green's function may need hundreds of iterations in order to get an accurate result. Sancho and Rubio [108] have developed an iterative scheme for solving the surface and bulk Green's function that converges much faster than iterative scheme. This method involves replacing the original chain by an effective one with twice the lattice constant, meaning each layer plus its two nearest neighbours in the original chain are replaced by an effective layer in the new chain. After n iterations, 2^n unit cells are taken into account instead of n unit cells. The original Sancho-Rubio iterative scheme only included the Hamiltonian matrix, while the overlap matrix S is assumed to be an identity matrix. We present below, as an example how this method is developed for the source contact of BLGNR shown in Fig. A.1.

We start with the definition of Green's function. The Green's function for source (left) contact is $A_{LL}g_L = I$ and it can be written in matrix form using Fig. A.1 as

$$\begin{bmatrix} EI-\alpha & \beta_1 & & & & \\ \beta_1^+ & EI-\alpha & \beta_3 & & & \\ & \beta_3^+ & EI-\alpha & \beta_1 & & \\ & & \beta_1^+ & EI-\alpha & \beta_2 & \\ & & & \beta_2^+ & EI-\alpha & \beta_1 \\ & & & & \beta_1^+ & EI-\alpha \end{bmatrix} \begin{bmatrix} \bullet & \bullet & \bullet & \bullet & \bullet & \bullet \\ \bullet & \bullet & \bullet & \bullet & \bullet & g_{-4,0} \\ \bullet & \bullet & \bullet & \bullet & \bullet & g_{-3,0} \\ \bullet & \bullet & \bullet & \bullet & g_{-2,-1} & g_{-2,0} \\ \bullet & \bullet & \bullet & \bullet & g_{-1,-1} & g_{-1,0} \\ \bullet & \bullet & \bullet & \bullet & g_{0,-1} & g_{0,0} \end{bmatrix} = I \quad \text{(A.1)}$$

The quantity of interest in equation A.1 is $g_{0,0}$, which can be obtained by taking the block matrix

TH-1608_11610201

multiplication of A_{LL} and the last column of g_L as

$$\begin{bmatrix} EI-\alpha & \beta_1 & & & & \\ \beta_1^+ & EI-\alpha & \beta_3 & & & \\ & \beta_3^+ & EI-\alpha & \beta_1 & & \\ & & \beta_1^+ & EI-\alpha & \beta_2 & \\ & & & \beta_2^+ & EI-\alpha & \beta_1 \\ & & & & \beta_1^+ & EI-\alpha \end{bmatrix} \begin{bmatrix} g_{-5,0} \\ g_{-4,0} \\ g_{-3,0} \\ g_{-2,0} \\ g_{-1,0} \\ g_{0,0} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 1 \end{bmatrix} \tag{A.2}$$

The equations from matrix can be written as

$$\begin{aligned} (EI-\alpha)g_{0,0} &= I - \beta_1^+ g_{-1,0}, \\ (EI-\alpha)g_{-1,0} &= -\beta_2^+ g_{-2,0} - \beta_1 g_{0,0}, \\ (EI-\alpha)g_{-2,0} &= -\beta_1^+ g_{-3,0} - \beta_2 g_{-1,0}, \\ (EI-\alpha)g_{-3,0} &= -\beta_3^+ g_{-4,0} - \beta_1 g_{-2,0}, \\ (EI-\alpha)g_{-4,0} &= -\beta_1^+ g_{-5,0} - \beta_3 g_{-3,0} \end{aligned} \tag{A.3}$$

Using $u_1 = (EI-\alpha)^{-1}\beta_1$, $u_2 = (EI-\alpha)^{-1}\beta_2$, $u_3 = (EI-\alpha)^{-1}\beta_3$, $v_1 = (EI-\alpha)^{-1}\beta_1^+$, $v_2 = (EI-\alpha)^{-2}\beta_1^+$ and $v_3 = (EI-\alpha)^{-1}\beta_3^+$, equation A.3 can be written after the substitutions of surface Greens's functions as

$$g_{-2,0} = v_1(v_3 g_{-4,0} + u_1 g_{-2,0}) + u_2(v_2 g_{-2,0} + u_1 g_{0,0}) \tag{A.4}$$

$$(I - v_1u_1 - u_2v_2)g_{-2,0} = v_1v_3 g_{-4,0} + u_2u_1 g_{0,0}$$

The other terms can be defined in similar manner as

$$(I - v_1u_1 - u_3v_3)g_{-4,0} = v_1v_2 g_{-6,0} + u_3v_1 g_{-2,0}, \tag{A.5}$$

$$(I - v_1u_1 - u_2v_2)g_{-6,0} = v_1v_3 g_{-8,0} + u_2u_1 g_{-2,0} \tag{A.6}$$

Using $u_{21} = (I - v_1u_1 - u_2v_2)^{-1}u_2u_1$, $u_{31} = (I - v_1u_1 - u_3v_3)^{-1}u_3u_1$, $v_{13} = (I - v_1u_1 - u_2v_2)^{-1}v_1v_3$ and $v_{12} = (I - v_1u_1 - u_3v_3)^{-1}v_1v_2$, equation A.4 is simplified as

$$\begin{aligned} g_{-2,0} &= v_{13} g_{-4,0} + u_{21} g_{0,0}, \\ g_{-4,0} &= v_{12} g_{-6,0} + u_{31} g_{-2,0}, \\ g_{-6,0} &= v_{13} g_{-8,0} + u_{21} g_{-4,0} \end{aligned} \tag{A.7}$$

TH-1608_11610201

Substituting the high order surface Green's function into lower order, equation A.7 can be simplified as

$$g_{-4,0} = vg_{-8,0} + ug_{0,0}$$
$$g_{-8,0} = vg_{-12,0} + ug_{-4,0} \tag{A.8}$$

Now, the general expression for equation A.8 can be written as

$$g_{-4n,0} = vg_{-4n-4,0} + ug_{-4n+4,0} \tag{A.9}$$

Where, n= 1,2,3..N-4, $u = (I - v_{21}u_{21} - u_{31}v_{13})^{-1}u_{31}u_{21}$ and $v = (I - v_{21}u_{21} - u_{31}v_{13})^{-1}v_{12}v_{13}$. The process of substituting Green's function can be repeated until magnitude of higher order surface Green's function terms become approximately zero. After inserting higher order terms into equation A.3, the chain of equation can be obtained as

$$g_{-1,0} = (u_1 + v_2u_{12} + v_2u_{13}u + ...)g_{0,0} + (v_2u_{13}v)g_{-8,0} \tag{A.10}$$

With $\theta = u_1 + v_2u_{12} + v_2u_{13}u + ...$ and $\eta = v_2u_{13}v$, the process of substitution is repeated until $\eta < \delta$ in which δ is arbitrarily small. Then, equation A.10 can be expressed as

$$g_{-1,0} = \theta g_{0,0} \tag{A.11}$$

By substituting $g_{-1,0}$ in the first equation of A.3, the surface Green's function of left contact can be obtained as

$$g_{0,0} = (EI - \alpha - \beta_2^+\theta)^{-1} \tag{A.12}$$

Similar approach can be used to obtain the surface Green's function of drain contact.

TH-1608_11610201

B

Carrier Statistics

Indian Institute of Technology Guwahati

Contents

B.1 Carrier Statistics of Graphene, GNR, BLG and BLGNR 110

TH-1608_11610201

B.1 Carrier Statistics of Graphene, GNR, BLG and BLGNR

To improve the convergence of Poisson's equation with quantum charge density, a nonlinear inner loop, which takes quantum charge density and converts this charge into a quasi-Fermi level through a dummy function, is used. A semiclassical equilibrium carrier statistics with a dummy quasi-Fermi level is employed as the dummy function for better convergence. Herein, the analytical expression of carrier statistics for graphene, GNR, BLG and BLGNR is presented. The general expression of electron and hole densities is

$$n = \int_0^\infty dE \rho(E) f(E) \quad p = \int_0^\infty dE \rho(E) \times (1 - f(E)) \tag{B.1}$$

Where, E is the energy, f(E) is the Fermi-Dirac distribution function. The ρ is the density of states (DOS), which depends on material geometry. The DOS for 2-D graphene sheet is given [123] as

$$\rho_{GR}(E) = \frac{g_s g_v}{2\pi(\hbar v_f)^2} |E| \tag{B.2}$$

Where, $g_s = 2$ is the spin degeneracy, $g_v = 2$ is the valley degeneracy, $\hbar$ is the reduced Planck's constant, $v_f = 10^8$ cm/s is the Fermi velocity of carriers in graphene, and E is the energy. The situation changes when GNRs are cut from infinite graphene sheets. Consider a GNR of width W. In the case of GNR, the electron wave vector in the transverse direction (y-direction) is quantized by hard-wall boundary conditions to be $k_y = n\pi/W(n = \pm1, \pm2, ..)$. By inserting this k_y into the energy dispersion relation of graphene, the DOS relation for GNRs can be obtained as discussed in [123]. The total DOS relation for GNR is given as by

$$\rho_{GNR}(n, E) = \sum_n \frac{g_s g_v}{\pi \hbar v_f} \frac{E}{\sqrt{E^2 - E_n^2}} \Theta(E - E_n) \tag{B.3}$$

where, $\Theta(...)$ is the Heaviside unit step function and $E_n = n\pi\hbar v_f/W = nE_g/2$.

The DOS for bilayer graphene (BLG) is obtained by solving Dirac equation in [144]. The analytical expression can be given as

$$\rho_{BLG}(E) = \frac{g_s g_v}{4\pi(\hbar v_f)^2} |t_p + 2E| \tag{B.4}$$

Where, $t_p = 0.35$ eV is the interlayer coupling energy. Similar to GNR case, the total DOS for BLGNR is derived by inserting quantized k_y into BLG energy dispersion relation. The total DOS for BLGNR

TH-1608_11610201

is given as

$$\rho_{BLGNR}\left(n,E\right)=\sum\nolimits_{n}\frac{g_s g_v}{2\pi\hbar v_f}\frac{\left(2E+t_p\right)}{\sqrt{E^2-E_n^2-t_pE}}\Theta\left(E-E_n\right) \tag{B.5}$$

TH-1608_11610201

TH-1608_11610201

Bibliography

[1] S. Frank, "Graphene transistors," *Nature Nanotechnology*, vol. 5, no. 7, pp. 487–496, 2010.

[2] R. Sako, H. Hosokawa, and H. Tsuchiya, "Computational study of edge configuration and quantum confinement effects on graphene nanoribbon transport," *IEEE Electron Device Letters*, vol. 32, no. 1, pp. 6–8, 2011.

[3] Y.-W. Son, M. L. Cohen, and S. G. Louie, "Energy gaps in graphene nanoribbons," *Phys. Rev. Lett.*, vol. 97, p. 216803, Nov 2006.

[4] B. Sahu, H. Min, A. H. MacDonald, and S. K. Banerjee, "Energy gaps, magnetism, and electric-field effects in bilayer graphene nanoribbons," *Phys. Rev. B*, vol. 78, p. 045404, Jul 2008.

[5] L. Liao, J. Bai, R. Cheng, Y.-C. Lin, S. Jiang, Y. Qu, Y. Huang, and X. Duan, "Sub-100 nm channel length graphene transistors," *Nano Letters*, vol. 10, no. 10, pp. 3952–3956, 2010.

[6] T. SAKURAI, "Perspectives of low-power VLSI's," *IEICE Trans. Electron*, vol. E87-C, pp. 429–436, 2004.

[7] H. S. P. Wong, D. J. Frank, P. M. Solomon, C. H. J. Wann, and J. J. Welser, "Nanoscale CMOS," *Proceedings of the IEEE*, vol. 87, no. 4, pp. 537–570, Apr 1999.

[8] K. Kim, "From the future si technology perspective: Challenges and opportunities," in *2010 International Electron Devices Meeting*. Institute of Electrical and Electronics Engineers (IEEE), dec 2010.

[9] R. K. Cavin, P. Lugli, and V. V. Zhirnov, "Science and engineering beyond moore's law," *Proceedings of the IEEE*, vol. 100, no. Special Centennial Issue, pp. 1720–1749, May 2012.

[10] ITRS 2015, http://www.semiconductors.org/clientuploads/Research_Technology/ITRS/2015/6_2015.

[11] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric field effect in atomically thin carbon films," *Science*, vol. 306, no. 5696, pp. 666–669, 2004.

[12] A. S. Mayorov, R. V. Gorbachev, S. V. Morozov, L. Britnell, R. Jalil, L. A. Ponomarenko, P. Blake, K. S. Novoselov, K. Watanabe, T. Taniguchi, and A. K. Geim, "Micrometer-scale ballistic transport in encapsulated graphene at room temperature," *Nano Letters*, vol. 11, no. 6, pp. 2396–2399, jun 2011.

[13] K. Kim, J.-Y. Choi, T. Kim, S.-H. Cho, and H.-J. Chung, "A role for graphene in silicon-based semiconductor devices," *Nature*, vol. 479, no. 7373, pp. 338–344, nov 2011.

[14] M. Dragoman, D. Neculoiu, D. Dragoman, G. Deligeorgis, G. Konstantinidis, A. Cismaru, F. Coccetti, and R. Plana, "Graphene for microwaves," *IEEE Microwave Magazine*, vol. 11, no. 7, pp. 81–86, Dec 2010.

[15] E. W. Hill, A. Vijayaragahvan, and K. Novoselov, "Graphene sensors," *IEEE Sensors Journal*, vol. 11, no. 12, pp. 3161–3170, Dec 2011.

[16] F. Withers, O. D. Pozo-Zamudio, A. Mishchenko, A. P. Rooney, A. Gholinia, K. Watanabe, T. Taniguchi, S. J. Haigh, A. K. Geim, A. I. Tartakovskii, and K. S. Novoselov, "Light-emitting diodes by band-structure engineering in van der waals heterostructures," *Nature Materials*, vol. 14, no. 3, pp. 301–306, feb 2015.

[17] R. Ma, Q. Chen, W. Zhang, F. Lu, C. Wang, A. Wang, Y. H. Xie, and H. Tang, "A dual-polarity graphene NEMS switch ESD protection structure," *IEEE Electron Device Letters*, vol. 37, no. 5, pp. 674–676, May 2016.

TH-1608_11610201

[18] X.-F. Lin, Z.-Y. Zhang, Z.-K. Yuan, J. Li, X.-F. Xiao, W. Hong, X.-D. Chen, and D.-S. Yu, "Graphene-based materials for polymer solar cells," *Chinese Chemical Letters*, vol. 27, no. 8, pp. 1259 – 1270, 2016.

[19] E. Yoo, J. Kim, E. Hosono, H. shen Zhou, T. Kudo, and I. Honma, "Large reversible li storage of graphene nanosheet families for use in rechargeable lithium ion batteries," *Nano Letters*, vol. 8, no. 8, pp. 2277–2282, aug 2008.

[20] F. Schwierz, "Graphene transistors: Status, prospects, and problems," vol. 101, no. 7, July 2013, pp. 1567–1584.

[21] K. S. Kim, Y. Zhao, H. Jang, S. Y. Lee, J. M. Kim, K. S. Kim, J.-H. Ahn, P. Kim, J.-Y. Choi, and B. H. Hong, "Large-scale pattern growth of graphene films for stretchable transparent electrodes," *Nature*, vol. 457, no. 7230, pp. 706–710, jan 2009.

[22] C. Berger, Z. Song, T. Li, X. Li, A. Y. Ogbazghi, R. Feng, Z. Dai, A. N. Marchenkov, E. H. Conrad, P. N. First, and W. A. de Heer, "Ultrathin epitaxial graphite: 2d electron gas properties and a route toward graphene-based nanoelectronics," *The Journal of Physical Chemistry B*, vol. 108, no. 52, pp. 19 912–19 916, dec 2004.

[23] D. Gunlycke, D. A. Areshkin, and C. T. White, "Semiconducting graphene nanostrips with edge disorder," *Applied Physics Letters*, vol. 90, no. 14, p. 142104, 2007.

[24] P. Gava, M. Lazzeri, A. M. Saitta, and F. Mauri, "*Ab initio* study of gap opening and screening effects in gated bilayer graphene," *Phys. Rev. B*, vol. 79, p. 165431, Apr 2009.

[25] R. R. Nair, W. Ren, R. Jalil, I. Riaz, V. G. Kravets, L. Britnell, P. Blake, F. Schedin, A. S. Mayorov, S. Yuan, M. I. Katsnelson, H.-M. Cheng, W. Strupinski, L. G. Bulusheva, A. V. Okotrub, I. V. Grigorieva, A. N. Grigorenko, K. S. Novoselov, and A. K. Geim, "Fluorographene: A two-dimensional counterpart of teflon," *Small*, vol. 6, no. 24, pp. 2877–2884, nov 2010.

[26] C. Stampfer, E. Schurtenberger, F. Molitor, J. Guttinger, T. Ihn, and K. Ensslin, "Tunable graphene single electron transistor," *Nano Letters*, vol. 8, no. 8, pp. 2378–2383, aug 2008.

[27] M. Luisier and G. Klimeck, "Performance analysis of statistical samples of graphene nanoribbon tunneling transistors with line edge roughness," *Applied Physics Letters*, vol. 94, no. 22, 2009.

[28] F. Xia, D. B. Farmer, Y. ming Lin, and P. Avouris, "Graphene field-effect transistors with high on/off current ratio and large transport band gap at room temperature," *Nano Letters*, vol. 10, no. 2, pp. 715–718, feb 2010.

[29] S. Banerjee, L. Register, E. Tutuc, D. Reddy, and A. MacDonald, "Bilayer PseudoSpin field-effect transistor (BiSFET): A proposed new logic device," *IEEE Electron Device Letters*, vol. 30, no. 2, pp. 158–160, feb 2009.

[30] P. Zhao, R. Feenstra, G. Gu, and D. Jena, "SymFET: A proposed symmetric graphene tunneling field-effect transistor," *Electron Devices, IEEE Transactions on*, vol. 60, no. 3, pp. 951–957, March 2013.

[31] S. Vaziri, G. Lupina, C. Henkel, A. D. Smith, M. Ostling, J. Dabrowski, G. Lippert, W. Mehr, and M. C. Lemme, "A graphene-based hot electron transistor," *Nano Letters*, vol. 13, no. 4, pp. 1435–1439, apr 2013.

[32] International Technology Roadmap for Semiconductors, "Process integration, devices and structures," http://www.itrs2.net/2011-itrs.html, 2011, [Online; accessed 20-September-2016].

[33] M. C. Lemme, T. J. Echtermeyer, M. Baus, and H. Kurz, "A graphene field-effect device," *IEEE Electron Device Letters*, vol. 28, no. 4, pp. 282–284, April 2007.

[34] J. Kedzierski, P. L. Hsu, P. Healey, P. Wyatt, and C. Keast, "Epitaxial graphene transistors on SiC substrates," in *2008 Device Research Conference*, June 2008, pp. 25–26.

[35] J. Kedzierski, P. L. Hsu, A. Reina, J. Kong, P. Healey, P. Wyatt, and C. Keast, "Graphene-on-insulator transistors made using C on Ni chemical-vapor deposition," *IEEE Electron Device Letters*, vol. 30, no. 7, pp. 745–747, July 2009.

[36] M. Evaldsson, I. V. Zozoulenko, H. Xu, and T. Heinzel, "Edge-disorder-induced anderson localization and conduction gap in graphene nanoribbons," *Physical Review B*, vol. 78, no. 16, oct 2008.

TH-1608_11610201

[37] X. Li, X. Wang, L. Zhang, S. Lee, and H. Dai, "Chemically derived, ultrasmooth graphene nanoribbon semiconductors," *Science*, vol. 319, no. 5867, pp. 1229–1232, feb 2008.

[38] M. Y. Han, B. Özyilmaz, Y. Zhang, and P. Kim, "Energy band-gap engineering of graphene nanoribbons," *Phys. Rev. Lett.*, vol. 98, p. 206805, May 2007.

[39] Y. Yoon, G. Fiori, S. Hong, G. Iannaccone, and J. Guo, "Performance comparison of graphene nanoribbon FETs with schottky contacts and doped reservoirs," *IEEE Transactions on Electron Devices*, vol. 55, no. 9, pp. 2314–2323, sep 2008.

[40] D. Wei, L. Xie, K. K. Lee, Z. Hu, S. Tan, W. Chen, C. H. Sow, K. Chen, Y. Liu, and A. T. S. Wee, "Controllable unzipping for intramolecular junctions of graphene nanoribbons and single-walled carbon nanotubes," *Nature Communications*, vol. 4, p. 1374, jan 2013.

[41] J. et al., "Direct oriented growth of armchair graphene nanoribbons on germanium," *Nature Commun.*, vol. 6, pp. 1–8, August 2015.

[42] W. Xu and T.-W. Lee, "Recent progress in fabrication techniques of graphene nanoribbons," *Mater. Horiz.*, vol. 3, pp. 186–207, 2016.

[43] E. V. Castro, K. S. Novoselov, S. V. Morozov, N. M. R. Peres, J. M. B. L. dos Santos, J. Nilsson, F. Guinea, A. K. Geim, and A. H. C. Neto, "Biased bilayer graphene: Semiconductor with a gap tunable by the electric field effect," *Phys. Rev. Lett.*, vol. 99, no. 21, nov 2007.

[44] G. Fiori and G. Iannaccone, "Ultralow-voltage bilayer graphene tunnel FET," *IEEE Electron Device Letters*, vol. 30, no. 10, pp. 1096–1098, Oct 2009.

[45] B. N. Szafranek, D. Schall, M. Otto, D. Neumaier, and H. Kurz, "Electrical observation of a tunable band gap in bilayer graphene nanoribbons at room temperature," *Appl. Phys. Lett.*, vol. 96, no. 11, 2010.

[46] M. H. Oliveira, Jr., J. M. J. Lopes, T. Schumann, L. A. Galves, M. Ramsteiner, K. Berlin, A. Trampert, and H. Riechert, "Synthesis of quasi-free-standing bilayer graphene nanoribbons on SiC surfaces," *Nature Commun.*, vol. 6, pp. 1–5, February 2015.

[47] S. Bala Kumar and J. Guo, "Multilayer graphene nanoribbon under vertical electric field," *Journal of Appl. Phys.*, vol. 110, no. 4, 2011.

[48] H. Tsuchiya, H. Hosokawa, R. Sako, N. Hasegawa, and M. Ogawa, "Theoretical evaluation of ballistic electron transport in field-effect transistors with semiconducting graphene channels," *Japanese Journal of Appl. Phys.*, vol. 51, no. 5R, p. 055103, 2012.

[49] W. J. Yu and X. Duan, "Tunable transport gap in narrow bilayer graphene nanoribbons," *Scientific Reports*, vol. 3, pp. 1–5, February 2013.

[50] C. C. W. et al., "High performance 22/20nm FinFET CMOS devices with advanced high-k/metal gate scheme," in *2010 International Electron Devices Meeting*, Dec 2010, pp. 27.1.1–27.1.4.

[51] W. S. Hwang, K. Tahy, X. Li, H. G. Xing, A. C. Seabaugh, C. Y. Sung, and D. Jena, "Transport properties of graphene nanoribbon transistors on chemical-vapor-deposition grown wafer-scale graphene," *Applied Physics Letters*, vol. 100, no. 20, p. 203107, 2012.

[52] G. Fiori and G. Iannaccone, "On the possibility of tunable-gap bilayer graphene FET," *Electron Device Lett., IEEE*, vol. 30, no. 3, pp. 261–264, March 2009.

[53] S. K. Chin, D. Seah, K. T. Lam, G. S. Samudra, and G. Liang, "Device physics and characteristics of graphene nanoribbon tunneling FETs," *IEEE Transactions on Electron Devices*, vol. 57, no. 11, pp. 3144–3152, Nov 2010.

[54] X. Yang, J. Chauhan, J. Guo, and K. Mohanram, "Graphene tunneling FET and its applications in low-power circuit design," in *Proceedings of the 20th Symposium on Great Lakes Symposium on VLSI*, ser. GLSVLSI '10. New York, NY, USA: ACM, 2010, pp. 263–268.

[55] K. T. Lam, D. Seah, S. K. Chin, S. B. Kumar, G. Samudra, Y. C. Yeo, and G. Liang, "A simulation study of graphene-nanoribbon tunneling FET with heterojunction channel," *IEEE Electron Device Letters*, vol. 31, no. 6, pp. 555–557, June 2010.

TH-1608_11610201

[56] T. K. Agarwal, A. Nourbakhsh, P. Raghavan, I. Radu, S. D. Gendt, M. Heyns, M. Verhelst, and A. Thean, "Bilayer graphene tunneling FET for sub-0.2 V digital CMOS logic applications," *IEEE Electron Device Letters*, vol. 35, no. 12, pp. 1308–1310, Dec 2014.

[57] D. Logoteta, G. Fiori, and G. Iannaccone, "Graphene-based lateral heterostructure transistors exhibit better intrinsic performance than graphene-based vertical transistors as post-CMOS devices," *Sci. Rep.*, vol. 4, p. 6607, oct 2014.

[58] N. Ghobadi and M. Pourfath, "A comparative study of tunneling FETs based on graphene and GNR heterostructures," *IEEE Trans. on Electron Devices*, vol. 61, no. 1, pp. 186–192, Jan 2014.

[59] Y. Wu, D. B. Farmer, F. Xia, and P. Avouris, "Graphene electronics: Materials, devices, and circuits," *Proceedings of the IEEE*, vol. 101, no. 7, pp. 1620–1637, jul 2013.

[60] Y.-M. Lin, K. A. Jenkins, A. Valdes-Garcia, J. P. Small, D. B. Farmer, and P. Avouris, "Operation of graphene transistors at gigahertz frequencies," *Nano Letters*, vol. 9, no. 1, pp. 422–426, 2009, pMID: 19099364.

[61] R. Cheng, J. Bai, L. Liao, H. Zhou, Y. Chen, L. Liu, Y.-C. Lin, S. Jiang, Y. Huang, and X. Duan, "High-frequency self-aligned graphene transistors with transferred gate stacks," *Proceedings of the National Academy of Sciences*, vol. 109, no. 29, pp. 11 588–11 592, jul 2012.

[62] Y. Wu, Y.-m. Lin, A. A. Bol, K. A. Jenkins, F. Xia, D. B. Farmer, Y. Zhu, and P. Avouris, "High-frequency, scaled graphene transistors on diamond-like carbon," *Nature*, vol. 472, no. 7341, pp. 74–78, April 2011.

[63] Y. Wu, K. A. Jenkins, A. Valdes-Garcia, D. B. Farmer, Y. Zhu, A. A. Bol, C. Dimitrakopoulos, W. Zhu, F. Xia, P. Avouris, and Y.-M. Lin, "State-of-the-art graphene high-frequency electronics," *Nano Letters*, vol. 12, no. 6, pp. 3062–3067, 2012.

[64] Y.-M. Lin, K. Jenkins, D. Farmer, A. Valdes-Garcia, P. Avouris, C.-Y. Sung, H.-Y. Chiu, and B. Ek, "Development of graphene FETs for high frequency electronics," in *Electron Devices Meeting (IEDM), 2009 IEEE International*, Dec 2009, pp. 1–4.

[65] I. Meric, C. Dean, S.-J. Han, L. Wang, K. Jenkins, J. Hone, and K. Shepard, "High-frequency performance of graphene field effect transistors with saturating IV-characteristics," in *Electron Devices Meeting (IEDM), 2011 IEEE International*, Dec 2011, pp. 2.1.1–2.1.4.

[66] I. Meric, M. Y. Han, A. F. Young, B. Ozyilmaz, P. Kim, and K. L. Shepard, "Current saturation in zero-bandgap, top-gated graphene field-effect transistors," *Nature Nanotechnology*, vol. 3, no. 11, pp. 654–659, December 2008.

[67] J. Chauhan and J. Guo, "High-field transport and velocity saturation in graphene," *Applied Physics Letters*, vol. 95, no. 2, p. 023120, jul 2009.

[68] S.-J. Han, D. Reddy, G. D. Carpenter, A. D. Franklin, and K. A. Jenkins, "Current saturation in submicrometer graphene transistors with thin gate dielectric: Experiment, simulation, and theory," *ACS Nano*, vol. 6, no. 6, pp. 5220–5226, jun 2012.

[69] G. Fiori, "Negative differential resistance in mono and bilayer graphene p-n junctions," *Electron Device Letters, IEEE*, vol. 32, no. 10, pp. 1334–1336, Oct 2011.

[70] I. Imperiale, S. Bonsignore, A. Gnudi, E. Gnani, S. Reggiani, and G. Baccarani, "Computational study of graphene nanoribbon FETs for RF applications," in *2010 International Electron Devices Meeting*, Dec 2010, pp. 32.3.1–32.3.4.

[71] I. Imperiale, A. Gnudi, E. Gnani, S. Reggiani, and G. Baccarani, "High-frequency analog GNR-FET design criteria," in *2011 Proceedings of the European Solid-State Device Research Conference (ESSDERC)*, Sept 2011, pp. 303–306.

[72] B. N. Szafranek, G. Fiori, D. Schall, D. Neumaier, and H. Kurz, "Current saturation and voltage gain in bilayer graphene field effect transistors," *Nano Letters*, vol. 12, no. 3, pp. 1324–1328, 2012.

[73] G. Fiori, D. Neumaier, B. N. Szafranek, and G. Iannaccone, "Bilayer graphene transistors for analog electronics," *IEEE Transactions on Electron Devices*, vol. 61, no. 3, pp. 729–733, March 2014.

TH-1608_11610201

[74] G. Fiori and G. Iannaccone, "Insights on radio frequency bilayer graphene FETs," in *2012 International Electron Devices Meeting*. Institute of Electrical & Electronics Engineers (IEEE), dec 2012.

[75] K. Kim, J.-Y. Choi, T. Kim, S.-H. Cho, and H.-J. Chung, "A role for graphene in silicon-based semiconductor devices," *Nature*, vol. 479, no. 7373, pp. 338–344, nov 2011.

[76] S. Lee, B. Jagannathan, S. Narasimha, A. Chou, N. Zamdmer, J. Johnson, R. Williams, L. Wagner, J. Kim, J.-O. Plouchart, J. Pekarik, S. Springer, and G. Freeman, "Record RF performance of 45-nm SOI CMOS technology," in *2007 IEEE International Electron Devices Meeting*. Institute of Electrical and Electronics Engineers (IEEE), dec 2007.

[77] R. Lai, X. B. Mei, W. R. Deal, W. Yoshida, Y. M. Kim, P. H. Liu, J. Lee, J. Uyeda, V. Radisic, M. Lange, T. Gaier, L. Samoska, and A. Fung, "Sub 50 nm InP HEMT device with fmax greater than 1 THz," in *2007 IEEE International Electron Devices Meeting*, Dec 2007, pp. 609–611.

[78] J. Chauhan and J. Guo, "Assessment of high-frequency performance limits of graphene field-effect transistors," *Nano Research*, vol. 4, no. 6, pp. 571–579, 2011.

[79] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proceedings of the IEEE*, vol. 98, no. 12, pp. 2095–2110, Dec 2010.

[80] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, pp. 329–337, Nov 2011.

[81] H. Liu, S. Datta, and V. Narayanan, "Steep switching tunnel FET: A promise to extend the energy efficient roadmap for post-CMOS digital and analog/RF applications," in *Low Power Electronics and Design (ISLPED), 2013 IEEE International Symposium on*, Sept 2013, pp. 145–150.

[82] A. Mallik and A. Chattopadhyay, "Tunnel field-effect transistors for analog/mixed-signal system-on-chip applications," *Electron Devices, IEEE Transactions on*, vol. 59, no. 4, pp. 888–894, April 2012.

[83] G. Fiori, A. Betti, S. Bruzzone, and G. Iannaccone, "Lateral graphene hBCN heterostructures as a platform for fully two-dimensional transistors," *ACS Nano*, vol. 6, no. 3, pp. 2642–2648, 2012.

[84] D. Vasileska, H. R. Khan, S. S. Ahmed, C. Ringhofer, and C. Heitzinger, "Quantum and coulomb effects in nanodevices," *International Journal of Nanoscience*, vol. 04, no. 03, pp. 305–361, 2005.

[85] T. Grasser, *Advanced Device Modeling and Simulation*. World Scientific Publication, 2003.

[86] L. V. Keldysh, "Diagram technique for nonequilibrium processes," *Sov. Phys. JETP.*, vol. 20, pp. 1018–1026, 1965.

[87] R. Bersohn, "Quantum statistical mechanics. l. p. kadanoff and g. baym. benjamin, new york, 1962. 203 pp. illus. paper, 4.95; *cloth*,6.95," *Science*, vol. 139, no. 3553, pp. 399–400, 1963.

[88] P. C. Martin and J. Schwinger, "Theory of many-particle systems. i," *Physical Review*, vol. 115, no. 6, p. 1342, 1959.

[89] Z. Ren, S. Goasguen, A. Matsudaira, S. S. Ahmed, K. Cantley, Y. Liu, Y. Gao, X. Wang, and M. Lundstrom, "NanoMOS," May 2006. [Online]. Available: https://nanohub.org/resources/1305

[90] G. W. Budiman, Y. Gao, X. Wang, S. Koswatta, and M. Lundstrom, "Cylindrical cnt mosfet simulator," Aug 2008.

[91] A. Martinez, A. R. Brown, S. Roy, and A. Asenov, "NEGF simulations of a junctionless si gate-all-around nanowire transistor with discrete dopants," in *Ulis 2011 Ultimate Integration on Silicon*, March 2011, pp. 1–4.

[92] "Nanotcad vides," Available:http://www.nanohub.org/tools/vides.

[93] M. Paulsson, F. Zahid, S. Datta, and M. McLennan, "Molctoy," Jun 2005.

[94] S. Jin, "Modeling of quantum transport in nano-scale MOSFET devices," Ph.D. dissertation, Seoul Natinoal University, South Korea, Feb. 2006.

TH-1608_11610201

[95] F. Pasadas and D. Jimenez, “Large-signal model of graphene field-effect transistors-part i: Compact modeling of gfet intrinsic capacitances,” *IEEE Transactions on Electron Devices*, vol. 63, no. 7, pp. 2936–2941, July 2016.

[96] S. A. Thiele, J. A. Schaefer, and F. Schwierz, “Modeling of graphene metal-oxide-semiconductor field-effect transistors with gapless large-area graphene channels,” *Journal of Applied Physics*, vol. 107, no. 9, p. 094505, 2010.

[97] S. O. Koswatta, A. Valdes-Garcia, M. B. Steiner, Y.-M. Lin, and P. Avouris, “Ultimate RF performance potential of carbon electronics,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 10, pp. 2739–2750, oct 2011.

[98] G. Liang, N. Neophytou, D. E. Nikonov, and M. S. Lundstrom, “Performance projections for ballistic graphene nanoribbon field-effect transistors,” *IEEE Transactions on Electron Devices*, vol. 54, no. 4, pp. 677–682, April 2007.

[99] M. Cheli, G. Fiori, and G. Iannaccone, “A semianalytical model of bilayer-graphene field-effect transistor,” *IEEE Transactions on Electron Devices*, vol. 56, no. 12, pp. 2979–2986, Dec 2009.

[100] L. Wang, I. Meric, P. Y. Huang, Q. Gao, Y. Gao, H. Tran, T. Taniguchi, K. Watanabe, L. M. Campos, D. A. Muller, J. Guo, P. Kim, J. Hone, K. L. Shepard, and C. R. Dean, “One-dimensional electrical contact to a two-dimensional material,” *Science*, vol. 342, no. 6158, pp. 614–617, 2013.

[101] S. Datta, “Nanoscale device modeling: the Green’s function method,” *Superlattices and Microstructures*, vol. 28, no. 4, pp. 253 – 278, 2000.

[102] V. H. Nguyen, F. Mazzamuto, J. Saint-Martin, A. Bournel, and P. Dollfus, “Graphene nanomesh-based devices exhibiting a strong negative differential conductance effect,” *Nanotechnology*, vol. 23, no. 6, p. 065201, 2012.

[103] P. Zhao and J. Guo, “Modeling edge effects in graphene nanoribbon field-effect transistors with real and mode space methods,” *J. Appl. Phys.*, vol. 105, no. 3, p. 034503, 2009.

[104] R. Grassi, A. Gnudi, E. Gnani, S. Reggiani, and G. Baccarani, “Mode space approach for tight binding transport simulation in graphene nanoribbon fets,” *IEEE Transactions on Nanotechnology*, vol. 10, no. 3, pp. 371–378, May 2011.

[105] G. Fiori and G. Iannaccone, “Performance analysis of graphene bilayer transistors through tight-binding simulations,” in *Computational Electronics, 2009. IWCE ’09. 13th International Workshop on*, May 2009, pp. 1–4.

[106] T. Low, S. Hong, J. Appenzeller, S. Datta, and M. Lundstrom, “Conductance asymmetry of graphene p-n junction,” *Electron Devices, IEEE Trans. on*, vol. 56, no. 6, pp. 1292–1299, June 2009.

[107] S. Datta, *Quantum Transport Atom to Transistor.* Cambridge University Press, 2005.

[108] M. P. L. Sancho, J. M. L. Sancho, and J. Rubio, “Highly convergent schemes for the calculation of bulk and surface green functions,” *Journal of Physics F: Metal Physics*, vol. 15, no. 4, pp. 851–858, 1985.

[109] R. Venugopal, Z. Ren, and M. Lundstrom, “Simulating quantum transport in nanoscale mosfets: ballistic hole transport, subband engineering and boundary conditions,” *IEEE Transactions On Nanotechnology*, vol. 2, no. 3, pp. 135–143, sep 2003.

[110] H. Khan, D. Mamaluy, and D. Vasileska, “Self-consistent treatment of quantum transport in 10 nm FinFET using contact block reduction (CBR) method,” *Journal of Computational Electronics*, vol. 6, no. 1-3, pp. 77–80, dec 2006.

[111] Y. M. Sabry, T. M. Abdolkader, and W. F. Farouk, “Simulation of quantum transport in double-gate mosfets using the non-equilibrium green’s function formalism in real-space: A comparison of four methods,” *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, vol. 24, no. 4, pp. 322–334, 2011.

[112] L. Brey and H. A. Fertig, “Electronic states of graphene nanoribbons studied with the dirac equation,” *Phys. Rev. B*, vol. 73, p. 235411, Jun 2006.

TH-1608_11610201

[113] K.-T. Lam and G. Liang, "An ab initio study on energy gap of bilayer graphene nanoribbons with armchair edges," *Applied Physics Letters*, vol. 92, no. 22, 2008.

[114] Z. Ren, "Nanoscale MOSFETs: Physics, simulation, and design," Ph.D. dissertation, Purdue Univ., West Lafayette, IN, Dec. 2001.

[115] J. Guo, "Carbon nanotube electronics: modeling, physics, and applications," Ph.D. dissertation, Purdue Univ., West Lafayette, IN, 2004.

[116] M. Luisier, A. Schenk, W. Fichtner, and G. Klimeck, "Atomistic simulation of nanowires in the $sp^3d^5s^*$ tight-binding formalism: From boundary conditions to strain calculations," *Phys. Rev. B*, vol. 74, p. 205323, Nov 2006.

[117] R. Grassi, S. Poli, E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, "Tight-binding and effective mass modeling of armchair graphene nanoribbon fets," *Solid-state electronics*, vol. 53, no. 4, pp. 462–467, 2009.

[118] A. Alarcon, V.-H. Nguyen, S. Berrada, D. Querlioz, J. Saint-Martin, A. Bournel, and P. Dollfus, "Pseudosaturation and negative differential conductance in graphene field-effect transistors," *Electron Devices, IEEE Transactions on*, vol. 60, no. 3, pp. 985–991, March 2013.

[119] R. Grassi, T. Low, A. Gnudi, and G. Baccarani, "Contact-induced negative differential resistance in short-channel graphene FETs," *Electron Devices, IEEE Transactions on*, vol. 60, no. 1, pp. 140–146, Jan 2013.

[120] R. Grassi, A. Gnudi, V. Di Lecce, E. Gnani, S. Reggiani, and G. Baccarani, "Exploiting negative differential resistance in monolayer graphene FETs for high voltage gains," *Electron Devices, IEEE Transactions on*, vol. 61, no. 2, pp. 617–624, Feb 2014.

[121] S.-J. Han, D. Reddy, G. D. Carpenter, A. D. Franklin, and K. A. Jenkins, "Current saturation in submicrometer graphene transistors with thin gate dielectric: Experiment, simulation, and theory," *ACS Nano*, vol. 6, no. 6, pp. 5220–5226, 2012.

[122] S. O. Koswatta, M. S. Lundstrom, and D. E. Nikonov, "Performance comparison between p-i-n tunneling transistors and conventional MOSFETs," *IEEE Transactions on Electron Devices*, vol. 56, no. 3, pp. 456–465, March 2009.

[123] T. Fang, A. Konar, H. Xing, and D. Jena, "Carrier statistics and quantum capacitance of graphene sheets and ribbons," *Applied Physics Letters*, vol. 91, no. 9, 2007.

[124] Y. Wu, D. B. Farmer, W. Zhu, S.-J. Han, C. D. Dimitrakopoulos, A. A. Bol, P. Avouris, and Y.-M. Lin, "Three-terminal graphene negative differential resistance devices," *ACS Nano*, vol. 6, no. 3, pp. 2610–2616, 2012.

[125] L. Zhao et al., "Visualizing individual nitrogen dopants in monolayer graphene," *Science*, vol. 333, no. 6045, pp. 999–1003, 2011.

[126] Y. Ouyang, Y. Yoon, and J. Guo, "Scaling behaviors of graphene nanoribbon FETs: A three-dimensional quantum simulation study," *Electron Devices, IEEE Transactions on*, vol. 54, no. 9, pp. 2223–2231, Sept 2007.

[127] Y.-M. Lin and P. Avouris, "Strong suppression of electrical noise in bilayer graphene nanodevices," *Nano letters*, vol. 8, no. 8, pp. 2119–2125, 2008.

[128] M. P. Lima, A. Fazzio, and A. J. R. da Silva, "Edge effects in bilayer graphene nanoribbons: *Ab initio* total-energy density functional theory calculations," *Phys. Rev. B*, vol. 79, p. 153401, Apr 2009.

[129] J. A. del Alamo, "Nanometre-scale electronics with III-V compound semiconductors," *Nature*, vol. 479, p. 317, Nov. 2011.

[130] J. Zheng, Y. Wang, L. Wang, R. Quhe, Z. Ni, W.-N. Mei, Z. Gao, D. Yu, J. Shi, and J. Lu, "Interfacial properties of bilayer and trilayer graphene on metal substrates," *Sci. Rep.*, vol. 3, jun 2013.

[131] J. Guo, A. Javey, H. Dai, and M. Lundstrom, "Performance analysis and design optimization of near ballistic carbon nanotube field-effect transistors," in *Electron Devices Meeting, 2004. IEDM Technical Digest. IEEE International*, Dec 2004, pp. 703–706.

TH-1608_11610201

[132] J. Knoch and J. Appenzeller, "Tunneling phenomena in carbon nanotube field-effect transistors," *physica status solidi (a)*, vol. 205, no. 4, pp. 679–694, 2008.

[133] Y. Tsividis, *Operation and Modeling of the MOS Transistor*. Oxford University Press, 2008.

[134] K. D. Holland, N. Paydavosi, N. Neophytou, D. Kienle, and M. Vaidyanathan, "RF performance limits and operating physics arising from the lack of a bandgap in graphene transistors," *IEEE Transactions on Nanotechnology*, vol. 12, no. 4, pp. 566–577, jul 2013.

[135] M. S. Gupta, "Power gain in feedback amplifiers, a classic revisited," *IEEE Transactions on Microwave Theory and Techniques*, vol. 40, no. 5, pp. 864–879, May 1992.

[136] Z. Guo, R. Dong, P. S. Chakraborty, N. Lourenco, J. Palmer, Y. Hu, M. Ruan, J. Hankinson, J. Kunc, J. D. Cressler, C. Berger, and W. A. de Heer, "Record maximum oscillation frequency in C-face epitaxial graphene transistors," *Nano Letters*, vol. 13, no. 3, pp. 942–947, mar 2013.

[137] C. D. Cress, J. G. Champlain, I. S. Esqueda, J. T. Robinson, A. L. Friedman, and J. J. McMorrow, "Total ionizing dose induced charge carrier scattering in graphene devices," *IEEE Transactions on Nuclear Science*, vol. 59, no. 6, pp. 3045–3053, Dec 2012.

[138] S. Sarkar, K. R. Amin, R. Modak, A. Singh, S. Mukerjee, and A. Bid, "Role of different scattering mechanisms on the temperature dependence of transport in graphene," *Scientific Reports*, vol. 5, p. 16772, nov 2015.

[139] Y. Yoon, D. E. Nikonov, and S. Salahuddin, "Role of phonon scattering in graphene nanoribbon transistors: Nonequilibrium green's function method with real space approach," *Applied Physics Letters*, vol. 98, no. 20, p. 203503, 2011.

[140] F. Mazzamuto, V. H. Nguyen, V. N. Do, C. Caer, C. Chassat, J. Saint-Martin, and P. Dollfus, "Phonon and electron transport in graphene nanoribbons," *2010 14th International Workshop on Computational Electronics*, pp. 1–4, oct 2010.

[141] A. Yazdanpanah, M. Pourfath, and M. Fathipour, "A Numerical Study of Line-Edge Roughness Scattering in Graphene Nanoribbons," vol. 59, no. 2, pp. 433–440, 2012.

[142] M. Luisier and A. Schenk, "Two-dimensional tunneling effects on the leakage current of MOSFETs with single dielectric and high gate stacks," *IEEE Transactions on Electron Devices*, vol. 55, no. 6, pp. 1494–1501, June 2008.

[143] K. Khaliji, M. Noei, S. M. Tabatabaei, M. Pourfath, M. Fathipour, and Y. Abdi, "Tunable bandgap in bilayer armchair graphene nanoribbons: Concurrent influence of electric field and uniaxial strain," *IEEE Transactions on Electron Devices*, vol. 60, no. 8, pp. 2464–2470, Aug 2013.

[144] S. Bhattacharya and S. Mahapatra, "Negative differential conductance and effective electron mass in highly asymmetric ballistic bilayer graphene nanoribbon," *Physics Letters A*, vol. 374, no. 28, pp. 2850 – 2855, 2010.

TH-1608_11610201

List of Publications

Journal Publications

1. **Brajesh Rawat**, and Roy Paily, "Analysis of graphene Tunnel Field-Effect Transistors for Analog/RF Applications," ***IEEE Transactions on Electron Devices,*** Vol. 62, no. 8, pp. 2663-2669, August- 2015.

2. **Brajesh Rawat**, and Roy Paily, "Performance Projection of Bilayer Graphene Nanoribbon FET through Quantum-Mechanical Simulation," ***Semiconductor Science and Technology***, Vol. 32, no. 12, pp. 125004-125012 December- 2016.

3. **Brajesh Rawat**, and Roy Paily, "Performance Evaluation of Bilayer Graphene Nanoriibon Tunnel FETs for Digital and Analog applications " ***IEEE Transactions on Nanotechnology***, Vol. 16, no. 3, pp. 411-416 May- 2017.

4. **Brajesh Rawat**, and Roy Paily, "Modeling of Graphene-based Field-Effect Transistor through 1-D Real-Space Approach," **under revision in *Journal of Computational Electronics***.

Conference Publications

1. Brajesh Rawat, and Roy Paily " Modeling of Graphene and Graphene Nanoribbon Field-Effect Transistors with a Single 1-D Hamiltonian Matrix ", *2015 18th International Workshop on Physics of Semiconductor Devices (IWPSD)*, IISC Bangalore, p-366.

2. Brajesh Rawat, and Roy Paily " Analysis of Quasi-saturation behavior and Negative Differential Resistance in Graphene FETs ", *2014 2nd International Conference on Emerging Electronics (ICEE)*, IISC Bangalore.

3. Brajesh Rawat, and Roy Paily " Performance Comparison between Graphene based Conventional MOSFET and TFET for Analog Applications ", *2014 National conference on transport properties in Low dimension system.*

TH-1608_11610201

TH-1608_11610201