INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI
SHORT ABSTRACT OF THESIS

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SHORT ABSTRACT

The rapid increase in complexity of VLSI circuits with the advent of Deep Sub-Micron (DSM) technology causes development of faults during their normal operation. Such faults cannot be detected by off-line test or Built-In-Self-Test (BIST) techniques, thus, On-line Testing (OLT) is becoming an essential part in Design for Testability (DFT). Most of the existing works presented in the literature on OLT of digital circuits have emphasized on the followings:-- non-intrusiveness, totally self-checking, low area overhead, high fault coverage, low detection latency, etc. However, in DSM era, several other factors need to be considered, namely flexibility, coverage for advanced fault models, scalability, handling asynchronous circuits, etc. Considering all these facts, the main objective of this thesis is to design and develop efficient OLT schemes for detection of faults on-the-fly in digital VLSI circuits. In the first contribution of the thesis, we propose an Ordered Binary Decision Diagram (OBDD) based OLT scheme for digital circuits by considering “number of tap points” as a new design parameter to provide flexibility in the OLT perspective. Experimentally, it is seen that minimization of tap points (i.e., measurement limitation) has minimal impact on fault coverage and detection latency but it reduces area overhead of the on-line tester significantly. In the second contribution of the thesis, we propose an OBDD based OLT scheme for both feedback and non-feedback bridging faults. Experimentally, we have seen that consideration of feedback bridging faults along with non-feedback ones, improves fault coverage with marginal increase in the area overhead compared to schemes only involving non-feedback faults. In the third contribution of the thesis, we propose a High Level Decision Diagram (HLDD) based OLT scheme at Register Transfer Level (RTL) model of circuits in order to improve the scalability. Experiments on different benchmark circuits show that it achieves lower area overhead at similar fault coverage compared to OLT schemes at gate level. In the final contribution of the thesis, we propose an OBDD based OLT scheme for Speed Independent asynchronous (SI) circuits, which has low area overhead. The scheme is applied to different SI benchmark circuits and it is found that the area overhead of the on-line tester is much less compared to that of the existing Mutex approach.