Performance Enhancement Techniques for Low-Voltage Bulk-Driven Circuits

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Performance Enhancement Techniques for Low-Voltage Bulk-Driven Circuits

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To

My Family

for their love and support

My guide

Prof. Shaik Rafi Ahamed

for his guidance and inspiration

DECLARATION

*This is to certify that the thesis entitled "**Performance Enhancement Techniques for Low-Voltage Bulk-Driven Circuits**", submitted by me to the Indian Institute of Technology Guwahati for the award of the degree of **Doctor of Philosophy** is a bonafide work carried out by me under the supervision of **Prof. Shaik Rafi Ahamed**. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.*

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CERTIFICATE

*This is to certify that the this thesis entitled "**Performance Enhancement Techniques for Low-Voltage Bulk-Driven Circuits**" submitted by **Harikrishna Veldandi (11610233)**, a research scholar in the Department of Electronics and Electrical Engineering, Indian Institute of Technology Guwahati, for the award of degree of **Doctor of Philosophy**, is a record of an original research work carried out by him under my supervision and guidance. The thesis has fulfilled all requirements as per the regulations of the institute and in my opinion has reached the standard needed for submission. The results embodied in this thesis have not been submitted to any other University or Institute for the award of any degree or diploma.*

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Abstract

In recent years, the use of battery operated electronic devices such as cell phones, medical devices, gaming consoles, music players and laptops has been increasing. Low-power design is important for battery-operated devices. Such devices employs system-on-chip (SoC) for improved performance, lower cost and smaller size and it generally consists of analog, digital and mixed-signal circuits. The speed of integrated circuits has been increased as a result of scaling down in feature-size of CMOS devices. Also, the maximum allowable supply voltage of thin-oxide CMOS devices is reduced to ensure the reliability of circuit. However, the threshold voltage of advanced CMOS devices is not scaled down at the same rate as that of the supply voltage, in order to limit their leakage current. The smaller channel length CMOS devices and low-supply voltage benefits the digital circuits in terms of higher speed, better integration and power efficiency. On other hand, short channel effects and second-order effects degrades the analog circuits performance. While this evolution in CMOS technology is very beneficial for digital, and is not so for analog circuits.

The sizing of analog circuits to meet the desired performance is challenging since the short-channel effects and layout-dependent effects becomes a critical issue in sub-nanometer CMOS process. These issues demand a development of a systematic design procedure for circuit design by considering some major effects of sub-nanometer nodes to meet the desire specifications. Operational transconductance amplifier (OTA) is a basic building block in analog and mixed-signal systems. The performance of OTA influences the functioning of analog and mixed-signal circuits such as active filters, ADC/DAC, low-dropout regulators and buffer amplifiers. The OTA performance parameters such as gain, gain-bandwidth, slew rate, linearity and noise undergo degradation under low-voltage environment. Therefore, topological modifications to the conventional techniques are necessary to enhance the performance of OTA when they are operating under low-voltage environment. The reliability becomes a major concern in sub-nanometer technology nodes. The performance parameters undergo large deviations when circuits are subjected to unavoidable process-voltage-temperature (PVT) variations. These demand for development of analog circuits which are PVT insensitive. The conventional techniques based on gate-driven circuits are not suitable for low-voltage environment. Therefore, this research work is to develop low-voltage and low-power OTAs using bulk-driven MOSFET with improved performance in sub-nanometer CMOS technology.

In advanced CMOS process, the device performance characteristics gets affected by changes in the number of fingers due to shallow trench isolation effect, which in turn changes the circuit performance. A systematic design procedure based on g_m/I_D, g_{mb}/I_D and normalized current (I_D/W) characteristics is presented. This methodology is used to evaluate the device geometry by considering the number of fingers which meets the desired specifications. The gate-driven Miller-compensated two-stage OTA and bulk-riven current mirror OTA are chosen as examples for validation of the proposed method.

A PVT intensive bulk-driven OTA with improved gain is introduced, which is able to work under sub-0.5 V supply voltage. The gain of the bulk-driven input stage is improved with cross-coupling of active load transistor bulk-terminals. An additional cross-forward stage assists in increasing the gain of second stage. The cross-forward also improves the driving capability of OTA without any stability issue. The proposed design can drive capacitive loads up to 50 pF, with only a small reduction in phase margin.

An ultra-low-voltage pseudo-differential bulk-driven OTA with rail-to-rail input/output swing is presented for low-frequency applications. The proposed design employs an auxiliary circuit at input stage to improve the effective transconductance of bulk-driven input stage. The enhanced transconductance leads to improvement in gain and gain-bandwidth product of OTA. A partial positive feedback technique is employed to improve the gain. In addition, a Class-AB output stage is designed through a cross forward stage which improves current efficiency and gain of the amplifier. The proposed design operates at supply voltage of 0.3-V and total current consumption is 170 nA. This OTA can be used as a tunable transconductance amplifier by varying the bias voltage of auxiliary amplifier. Further, a tunable second order $G_m - C$ low pass filter is designed using the proposed OTA.

The drive strength of bulk-driven device is very less as compared to gate-driven counterparts which shows the effect on the slew rate of OTA. The power-efficient bulk-driven Class-AB operational transconductance amplifiers are presented for driving the large capacitive loads under low-voltage environment. In conventional circuits, the slew rate of the amplifier is limited by the static bias current. The proposed OTAs employ adaptive biasing and adaptive loads to improve the slew rate. In addition, a slew rate enhancer (SE) is employed to further improve the dynamic performance. The SE circuit consists of current-feedback loop which recursively copies the part of output driving current and increases the bias current of SE. As a result, the slew rate is improved significantly. The proposed OTA with SE can drive the large capacitive loads upto 2 nF with rail-to-rail output swing. The

proposed OTAs are operates at supply voltage of 0.5-V.

All the proposed OTAs are designed in a UMC 65-nm CMOS process. The intended capabilities and advantages of the proposed designs are verified through post-layout simulations. A final evaluation of the performance of the proposed OTAs compared with the state-of-the-art designs.

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List of Acronyms

ADC	Analog-to-Digital Converters
AC	Alternating Current
CBF	Current Boosting Factor
CF	Cross Forward
CFB	Current Feedback
CLM	Channel Length Modulation
CMOS	Complementar Metal-Oxide Semiconductor
CM	Common Mode
CMFB	Common-Mode Feedback
CMRR	Common-Mode Rejection Ratio
DC	Direct Current
DAC	Digital-to-Analog Converter
FOM	Figure of Merit
FVF	Flipped Voltage Follower
FG-MOSFET	Floating Gate MOSFET
GBW	Gain-Bandwidth
IC	Integrated Circuit
ICMR	Input Common Mode Range
IoT	Internet of Things
IRN	Input Referred Noise
LCD	Liquid Crystal Display
LPF	Low Pass Filter
LDE	Layout Dependent Effect
LDO	Low-Dropout Regulators

MFGS	Multifinger Gate Structure
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
nMOS	n-channel MOSFET
OTA	Operational Transconductance Amplifier
OD	Oxide Diffusion
pMOS	p-channel MOSFET
PPF	Partial Positive Feedback
PSRR	Power Supply Rejection Ratio
PVT	Process, Voltage and Temperature
RF	Radio Frequency
RHP	Right-Half-Plane
SE	Slew rate Enhancer
SoC	System-on-Chip
SNR	Signal-to-Noise Ratio
STI	Shallow Trench Isolation
THD	Total Harmonic Distortion
UGF	Unity Gain Frequency
UMC	United Microelectronics Corporation
VLSI	Very Large Scale Integration
WI	Weak Inversion
WPE	Well Proximity Effect

List of Symbols

As this thesis consists of various equations with many symbols, the meaning of variables and physical constants are listed below so that readers can refer easily. Also, common MOSFET equations and a general note about the symbol convention are provided.

A_{CM}	Comm-mode voltage gain
A_{DM}	Differential-mode voltage gain
A_V	Voltage gain
$C_{ox}^{/}$	Gate-oxide capacitance per area ($= \frac{\varepsilon_0.\varepsilon_r}{t_{ox}}$)
C_{gs}	Gate to source capacitance
C_L	Load capacitance
ε_0	Permittivity of free space ($\approx 8.85 \times 10^{-18}\ F/\mu m$)
ε_r	Relative permittivity ($= 3.97$ for SiO_2)
f_T	Transition frequency
g_{ds}	Drain-source conductance
g_m	Transistor gate transconductance
g_{mb}	Transistor bulk-transconductance
γ	Body-effect coefficient
I_B	Bias current
I_D	Drain current
I_S	Transistor characteristic current
k_B	Boltzmann constant ($\approx 1.38 \times 10^{-23}\ J/K$ or $\approx 8.6 \times 10^{-5}\ eV/K$)
K_{fn}	Flicker noise coefficients for nMOS
K_{fp}	Flicker noise coefficients for pMOS
L	Channel length of MOS transistor
L_{eff}	Effective channel length of MOS transistor

λ	Channel length modulation parameter
N_F	Number of fingers
n	Sub-threshold slope factor
q	Magnitude of electrical charger on electron ($\approx 1.602 \times 10^{-19}\ C$)
r_{ds}	Drain-source resistance
T	Absolute temperature
t_{ox}	Gate-oxide thickness
t_s	Settling time
μ_0	Mobility
μ_{eff}	Effective mobility
V_{BN}	nMOS bias voltage
V_{BP}	pMOS bias voltage
V_{CM}	Common-mode input voltage
V_{DD}	Supply voltage
V_{iN}	Input voltage with 180° phase shift
V_{iP}	Input voltage
V_{out}	Output voltage
V_{REF}	Reference voltage
V_T	Thermal voltage ($= K_B T/q$)
V_{TH}	Threshold voltage
V_{TO}	Threshold voltage for zero substrate bias
V_{GS}	Gate-source voltage
V_{DS}	Drain-source voltage
W_F	Finger width
W	Channel width
W_{eff}	Effective channel width

1

Introduction

Contents

1.1 Introduction

In recent years, the demand for emerging battery-operated portable and wearable electronics devices such as mobile phones, music players, and biomedical instruments (hearing aids, implantable cardiac pacemakers and heart-rate detectors) has been increasing. Most of these applications use system-on-chip (SoC) that consists of analog, digital, and intrinsic mixed-signal circuits. In order to extend the battery life in these systems, their SoC design should be more power efficient. The interaction among the different factors heading to the continuous growth of electronic devices can be better understood with the aid of Fig. 1.1. Note that behind the progress of integrated circuits, there is always a driving factor dictated by technology limitations and a driving factor related to market demand.

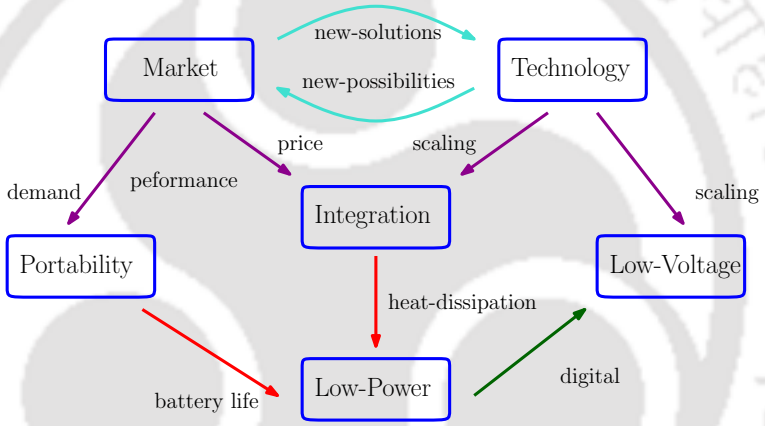


Figure 1.1: Factors driving the low-power and low-voltage trend [1]

The increasing demand for portable systems such as computers, digital communication systems and consumer electronics poses new challenges before the semiconductor industry. The driving force for this trend is the ability of the industry to produce faster and more power-efficient circuits, which is mainly due to the continuous scaling of the CMOS technology. The evolution in CMOS technology is motivated by decreasing price-per-performance for digital circuitry [3]. The continuous scaling of the MOSFET channel length (L) increases the maximum number of transistors per unit area. According to Moore's law, the amount of components per chip doubles every 24 months [1]. The speed of integrated circuits and more electronic functions per unit area has increased as a result of miniaturization and at the same time the maximum allowable supply voltage (V_{DD}) has decreased. Hence, a relatively large threshold voltage (V_{TH}) needs to be maintained to limit the OFF current in transistors.

The CMOS technology offers the unique possibility of integration of both analog and digital circuits

on the same chip. The low-supply voltage is especially beneficial to digital integrated CMOS circuits, since their power consumption is proportional to the square of the supply voltage, i.e., reducing the supply voltage to half will reduce the power consumption to a quarter from its original value. In analog signal processing the power consumption is not directly related to the supply voltage but, instead, it is basically set by the required signal-to-noise ratio (SNR) and the frequency of operation (or the required bandwidth).

The analog circuits employed in applications such as wireless sensor networks, wearable battery powered systems, and implantable circuits for biological applications need to consume very low amount of power such that the entire system can survive for a very long time without the need for changing or recharging battery. Using new power supply techniques such as energy harvesting and printable batteries, is another reason for reducing power dissipation.

1.1.1 Motivation

The current scope of this research is motivated by the implementation of analog circuits with challenges imposed by sub-nanometer CMOS technologies. This work is to develop low-power operational transconductance amplifiers (OTAs) for low-voltage applications. Since, OTA is a basic building block in analog and mixed-signal circuits such as analog filters, ADC/DAC converters, low-dropout regulators (LDOs), sample and hold circuits, references circuits and buffer amplifiers. The analog and mixed-signal circuits may require multiple OTAs, where the power consumption of individual OTA is critical in order to prolong the battery life. Hence optimizing the performance of individual components while keeping the power consumption low is critical to build an overall energy efficient system. Therefore, one must design an OTA to operate with as low a power as possible while maintaining an acceptable noise performance and linearity requirement. One of the most important features in low-voltage amplifier designs is ensuring that the amplifier maintains constant behaviour in the presence of rail-to-rail input common-mode variations while providing a rail-to-rail output to maximize SNR. Therefore, an efficient input stage for low-voltage operation is essential while designing OTA.

The conventional analog circuits are mainly based on gate-driven differential transistor pairs, where the input signal modulates the gate voltage of input devices. This approach is unsuitable for low supply voltage due to the V_{th} limitation in signal path. The input devices operate in the conductance region only for input common-mode level toward positive or negative supply rail. The input common-mode range of gate-driven circuits can be extended with the help of complementary input differential stage

or dynamic level shifter. But these circuits require complex biasing circuits to minimize the dead zone in the input range.

In recent years, various low-voltage design techniques such as bulk-driven, floating-gate, self-cascode and low$-V_{th}$ MOSFETs have been developed, which are capable of reducing the power supply requirements [4, 5]. Among these, the bulk-driven MOSFET is one of the most promising technique for design of analog circuits in low-voltage environment. Here, the input signal drives bulk-terminal of the input MOSFET devices while a sufficient gate voltage keeps the input devices in conducting region even for rail-to-rail input common-mode range. This approach eliminates V_{th} requirement in input signal path, thereby pushing the minimum operational supply voltage to its limit. However, the bulk-driven devices have few disadvantages like, low transconductance, increased area, and large input capacitance from its well structure. The bulk-transconductance (g_{mb}) of bulk-driven MOSFET is considerably smaller (2-5 times) than that of gate transconductance (g_m), which affects the gain, input noise and frequency response of the OTA. In addition, the drive strength of bulk-driven devices is very poor as compared to the gate-input counterparts.

For the aforementioned reasons, in this thesis, the performance degradation issues in low-voltage bulk-driven OTAs are addressed along the following directions.

- Improving the speed (i.e., gain-bandwidth (GBW)) of bulk-driven circuits under low-voltage environment.
- In low-voltage operation, boosting the gain is more difficult due to the absence of the transistor cascoding, and will cost more area and power consumption.
- The low-voltage circuits has to provide rail-to-rail output swing in order to maximize the SNR. In addition, the amplifier should maintain the constant behaviour in the presence of process, voltage and temperature (PVT) and input common-mode voltage variation while providing a rail-to-rail output.
- Improving the driving capability of bulk-driven OTAs under low-voltage environment.

1.1.2 Problem formulation

OTA is one of the most important building blocks of analog and mixed-mode systems. The bulk-driven transistors are normally used for designing an OTA with rail-to-rail operating range. However,

bulk-driven devices have certain limitations as mentioned in the previous Section. 1.1.1. In order to overcome these limitations, in this thesis, we proposed several techniques. The goal of this thesis is to develop power-efficient bulk-driven OTAs for low-voltage applications. To meet this goal the following specific contributions are attempted in this thesis.

- A systematic design procedure is suggested to minimize the variation of circuit performance due to layout dependent effects.
- Investigation of high DC-gain bulk-driven OTA topology for low-voltage and low-power applications.
- An ultra-low-voltage bulk-driven with rail-to-rail input/output swing is investigated for low-frequency applications.
- An adaptive biasing and slew rate enhancer techniques are suggested for improving the driving capability of low-voltage bulk-driven OTAs.

The scaling of power consumption is proportional to that of operating frequency of OTA. The tuning of operating frequency with required specifications is the main objective of this work. Overall, this thesis is aimed at improving the performance of bulk-driven OTAs under low-voltage environment. The intended capabilities and advantages of the suggested techniques are verified through post-layout simulations.

1.2 Contributions of the Thesis

This thesis is aimed for improving the performance of bulk-driven OTAs for low-voltage applications. The primary contributions of the thesis are listed below:

1.2.1 Design of analog circuits with STI effect

Nanoscale CMOS circuit design extensively employs multifinger layout technique to alleviate the performance degrading parasitic and mismatch effects that are typically observed with single-finger layout. However, a continuous increase in the number of fingers (N_F) accompanied by a simultaneous decrease in their finger width could lead to the penalty of a higher degree of variation in the MOSFET's small-signal parameters. It is due to the heightened shallow trench isolation (STI) stress that gets

developed in such devices. The optimisation of circuit performance with the arbitrarily fixed number and width of fingers would be ambiguous.

In this work, the initial approach involves investigation of current-voltage ($I-V$) characteristics of a MOSFET as a function of number of fingers. It has been found that both the drain current and transconductance get affected by the N_F. This explore a development of systematic methodology for multifinger MOSFET based circuits. In order to validate the methodology, Miller-compensated two-stage OTA and bulk-driven current mirror OTA are designed by considering STI effect. It is also found that the parameters of the designs are matched well with the set of desired specifications.

1.2.2 A low-voltage PVT-insensitive bulk-driven OTA with enhanced DC-gain

A PVT-insensitive bulk-driven OTA with enhanced DC-gain for low-voltage applications is described. A cross-coupled active load is employed at the bulk-driven input stage to enhance the gain of OTA. A cross-forward (CF) gain stage was placed between the input and output stages of the OTA to enhance the output stage transconductance. The CF stage improves the phase margin of OTA and keeps the amplifier stable even for large capacitive loads (up to 50 pF) and also improves overall DC-gain. The proposed design can drive capacitive loads up to 50 pF, with only a minor reduction in phase margin. The proposed design employs triple-well CMOS process in order to access the bulk-terminal of nMOS transistor. The OTA input stage is nMOS bulk-driven which provides the consistent performance under PVT variations.

1.2.3 An ultra-low-voltage bulk-driven OTA for low-frequency applications

An ultra-low-voltage pseudo-differential bulk-driven OTA with enhanced transconductance for low-frequency applications is presented. The design employs an auxiliary circuit at bulk-driven input stage in order to improve the effective transconductance of OTA. The enhanced transconductance leads to improvement in DC-gain and GBW of OTA. To further enhance the gain, a partial positive feedback technique is employed. In addition, push-pull output stage is designed through a CF stage, that improves the current efficiency and gain of the amplifier. This OTA can be used as a tunable transconductance amplifier by varying bias voltage of auxiliary amplifier. In addition, the proposed transconductance amplifier is used to design a tunable second-order G_m-C low-pass filter. The proposed design operates at supply voltage of 0.3-V and total current consumption is 170 nA, which makes this design is suitable for low-voltage, low-power applications.

1.2.4 Low-voltage Class-AB bulk-driven OTAs with improved slew rate

In this task, two different Class-AB bulk-driven OTAs are designed to realize analog voltage buffers capable of driving the large capacitive loads.

(i) In the first design, a low-voltage, high driving capability Class-AB bulk-driven OTA with minimal current consumption is considered. The proposed OTA consists of adaptively biased Class-AB differential input stage to improve the effective transconductance. The adaptive loads relying on cascode current mirrors, configured in partial positive feedback mode to enhance the overall gain of OTA. Because of adaptive biasing and adaptive load configuration, the driving capability of OTA increases for a large change in input voltage. The bulk-driven input stage helps to achieve rail-to-rail common-mode input operation.

(ii) In the second design, the bulk-driven OTA with slew rate enhancer (SE) which further improves the driving capability, is considered. The SE circuit consists of current-feedback loop which recursively copies the output driving current and increases the bias current of SE circuit. As a result, the slew rate is improved significantly. The proposed OTA can drive the large capacitive loads upto 2 nF with help of SE and it can provide rail-to-rail input and output swing.

1.3 Organization of the Thesis

The thesis is organized into seven chapters. The brief descriptions of these chapters are as follows.

Chapter 1 introduces the need of low-voltage design, briefs about the motivation, and problem definition, and finally provides the outline of the thesis.

Chapter 2 focuses on approaches which directly or indirectly target the low-voltage design by minimizing the effect of threshold voltage in signal path. Several conventional and unconventional low-voltage design techniques to obtain low-power operations are compared. Following the selection of the appropriate bulk-driven technique, the bulk-driven MOSFET removes V_{th} from the signal path and problems associated with several recent bulk-driven circuit are also discussed in this chapter.

Chapter 3 describes the anlog circuit performance variations due to layout dependent effects. A systematic design procedure for analog circuit designs with consideration of shallow trench isolation effect is presented. To validate the proposed method, a simple Miller compensated two-stage OTA has been considered.

In Chapter 4, a PVT-insensitive high DC-gain bulk-driven OTA with rail-to-rail input/output swing is presented. A cross forward stage improves the gain and driving capability of the OTA. The performance of the proposed OTA is compared with the state-of-the-art techniques.

In Chapter 5, an ultra-low-voltage pseudo-differential OTA for low-frequency applications is presented. This chapter discusses about transconductance and gain enhancement of bulk-driven OTAs. Based on the proposed OTA a tunable $G_m - C$ filter is designed for low-frequency applications.

Chapter 6 presents power-efficient Class-AB bulk-driven OTAs with improved slew rate to drive the large capacitive loads. It also describes adaptive biasing, adaptive loads and slew rate enhancer for improving the driving capability. Finally, the performance of the proposed high slew rate OTAs are compared with the existing designs.

In Chapter 7, the conclusions of this current research and outline of a few directions for future work is presented.

2

Literature Survey on Low-Voltage and Low-Power OTAs

Contents

This chapter covers device and circuit aspects of low-power analog CMOS design. The fundamental limits constraining the design of low-power circuits are first reviewed with an emphasis on the implications of supply voltage reduction. New design techniques that are appropriate for low-power and/or low-voltage circuits are presented.

2.1 Introduction

Low-voltage, low-power topologies of analog and mixed-signal designs have gained tremendous importance due to increased demand for portable devices. The current trend towards low-power design is mainly driven by two forces: First, low-power is the major goal of autonomous portable products for which speed and/or dynamic range might have to be sacrificed. Next, the high-performance VLSI systems based on advanced CMOS technologies provides high speed and high integration density. This has experienced a dramatic increase of heat dissipation that is now reaching a fundamental limit.

Analog circuits are primarily fabricated in standard digital CMOS processes so that they can be operated at the same supply voltage. This avoids the complexity involved in generating various supply voltages. The most efficient way to reduce the power consumption of digital circuits is definitely to reduce the supply voltage. On the other hand, the reduction of the supply voltage is also required to maintain the electric field at an acceptable level. The rules for analog circuits are quite different than those applied to digital circuits.

Unfortunately, in analog circuits, lowering the supply voltage does not lead to reduction in power consumption. Since, the circuits power is consumed to maintain the energy of the signal above the thermal noise in order to achieve the required SNR and the desired bandwidth [6].

2.2 CMOS Technology Scaling Trade-offs

In this section, the fundamental trade-offs associated with CMOS technology scaling are discussed. The scaling down of device geometry leading to very large scale integration at a lower fabrication cost. It helps in achieving higher speed and lower power consumption. In general, CMOS technology scaling (referred to as reduction in MOSFET devices dimensions) allows increased packing densities and higher performance in integrated circuits. It has been the ability to scale CMOS technology in a predictable and consistent manner that has led to the proliferation of CMOS ICs. The primary goals of scaling in CMOS technology are to increase the density and improve the performance of digital integrated

circuits. For each generation, a 30% reduction in gate length yields a roughly 50% reduction in gate area, or a doubling of the packing density. To ensure reliability with reduction in the device dimensions, a low-voltage has to be used.

2.3 Scaling Trends in Analog CMOS Technologies

The advanced CMOS technologies improve the analog circuit performance in terms of lower area, reduced parasitics, higher speed with maximum allowable supply voltage. As technologies are scaled-down, g_m tends to increase, since the gate capacitances reduces in proportion to L. However, in order to make use of few advantages of small channel length devices, some mixed-mode designs use the combination of both small and large channel length devices. But, the designs which use only small channel length devices are normally avoided in analog circuits. Some of the major drawbacks of the use of small channel length devices are as follows [7–9]:

- The drain resistance (r_{ds}) of the short-channel devices is small due to channel length modulation (CLM) effect [3]. The degradation of r_{ds} results in reduction of intrinsic gain ($g_m r_{ds}$).
- Most of the analog circuits are biased using various current sources and sinks [10]. The current source (or a sink) requires high output resistance to maintain the constant current over a wide output voltage range. In strong inversion, large CLM effect causes a wide variation in the drain current as a function of the output voltage. This becomes even worse in weak inversion due to the exponential dependence of the drain current on the drain voltage. When using small channel length devices, the current mirroring does not remain constant over the output voltage range.
- The drain resistance of short channel devices varies with V_{DS}. This shows a major effect on the reduction in the linear gain of the circuit, and it strengthens the harmonic components of the signal. This causes decrease in the power of the fundamental frequency component, which in turn degrades the total harmonic distortion (THD) performance.
- The smaller channel length decreases the effective channel area of the transistor. But, the threshold voltage mismatch and noise are inversely proportional to the effective channel area [9]. Hence, the short channel devices are more sensitive to the mismatch variations.

The disadvantages of low supply voltage are as follows [7]:

- The scaling in V_{DD} directly affects the maximum operating frequency of the transistor.
- The limited output swing degrades the SNR of analog circuits.
- In analog circuits, where lower supply voltage does not lead automatically to lower power consumption. As V_{DD} is scaled down, the output swing will reduce, which affects the SNR. The analog circuits require additional current in order to maintain desired SNR due to supply voltage reduction.

The short channel devices are very useful to design the high frequency analog circuits because of larger bandwidth. As discussed, the short channel devices degrade the analog circuits performance. The conventional circuit architectures will tend to fail when designed using smaller channel length and low supply voltage. Hence, there is a need to develop new design techniques for sub-nanometer CMOS devices.

2.4 Comparison of Low-Voltage Analog Circuit Design Techniques

Continuing technology feature-size scaling requires a proportional downscaling of the V_{DD} to maintain device reliability. At the same time, relatively large threshold voltages need to be maintained to limit the OFF current in transistors [11]. But, the V_{TH} and drain-source saturation voltage of sub-nanometer CMOS technologies do not scale at same rate as the V_{DD}. The high V_{TH} in CMOS technology is the main limiting factor in low-voltage circuit designs. To overcome the high V_{TH} barrier in sub-nanometer CMOS process several design techniques were proposed in [4, 5].

Several techniques have been explored to implement low-voltage circuits with a rail-to-rail input common-mode range (ICMR), such as complementary input stage [12–16], dynamic level shifter [17,18], floating-gate [19–21], and bulk-driven transistor [22, 23]. The advantages and disadvantages of these techniques are as follows:

- *Complementary input stage*: This is the traditional approach to implement a rail-to-rail input stage and is obtained by connecting in parallel a p-channel and an n-channel differential pair [12–16]. This technique requires additional circuits to control the transistor bias currents to maintain a constant transconductance over the entire signal swing range [24]. Moreover, this approach is not suitable for extremely lower supply voltages. Since, there is a dead region in the middle of the input voltage range [23].

- *Dynamic level shifter*: The use of dynamic level shifters have been the most popular approach to obtain a rail-to-rail input stage [17,18]. However, the level shifters require large on-chip area, which is unacceptable in modern CMOS ICs.

- *Floating-Gate MOSFET (FG-MOSFET)*: FG-MOSFETs are used to achieve rail-to-rail input range with low-voltage power supply [19–21]. The V_{TH} of FG-MOSFET can be made programmable with proper selection of bias voltage, hence suitable for ultra-low-voltage applications. The FG-MOSFETs consumes large silicon area compared to conventional transistor. It offers low transconductance which results in low gain, poor noise performance, and smaller bandwidth. The output resistance is reduced due to the capacitive coupling between the floating gate and drain terminal. Moreover, there is uncertain amount of charge trapped at the floating gate during fabrication [19]. Hence, an additional programming is required to minimize the effect of trapped charge [25].

- *Bulk-driven MOSFET*: In this technique, the input signal is applied to the bulk (the back gate or the body) of an input device while the gate is biased to create a conducting channel between the source and the drain [22]. The input devices operate in conducting region even for rail-to-rail input common-mode range. This approach eliminates V_{TH} requirement in the input signal path, hence it is suitable for ultra-low supply voltages. The output resistance of bulk-driven transistor is similar to that of a gate-driven counterpart. The bulk-driven transistors provides better linearity as compared to gate-driven circuits. However, the bulk-transconductance is considerably smaller (2-5 times) than that of gate transconductance. The low transconductance affects DC-gain, noise performance and frequency response of bulk-driven circuits. Moreover, the input voltage of bulk-driven transistors is limited to a value, which is less than 0.7-V to avoid latch up problem [23]. In applications, where both pMOS and nMOS bulk-driven transistors are present, triple-well CMOS process is required, which increases the cost process and chip area.

Finally, from the above discussion, it can be concluded that the bulk-driven technique is a good choice for low-voltage circuit design. Bulk-driven MOSFETs have several advantages like high output resistance, good linearity, no extra fabrication steps requirement, and compatibility with the standard CMOS technology. The input voltage limitation can be overcome by use of V_{DD} of less than 0.7-V. Thus, in this thesis, more emphasis is given on performance enhancement techniques of low-voltage

bulk-driven circuits.

2.5 State-of-art Bulk-driven OTAs

The OTA is one of the important circuit present in most of the analog and mixed-signal systems such as pre-amplifiers, integrators, switched capacitor circuits, analog filters and data converters. In order to obtain better performance of these systems, the OTA need to be designed to provide optimal performance interms of DC-gain, speed, slew rate and linearity. Moreover, performance of OTA should be less sensitive to PVT variations.

Several works so far have been reported in the literature on the design of bulk-driven circuits. However, many important issues remained unaddressed in these works. Hence, in this thesis, we made an attempt to address the various challenges encountered in the design of bulk-driven circuits.

2.5.1 Enhancement of small-signal performance

Over several years, several works on low-voltage circuits which can operate with a supply voltage of 1-V or below have been reported [4,5]. The input impedance of bulk-driven circuits drop significantly when the p-n junction of an input transistor (pMOS/nMOS) is forward biased. The circuits may drive into the latch-up state when the V_{DD} exceeds 0.7-V.

From past few years, bulk-driven technique has been adopted to implement a number of low-voltage analog building blocks such as operational amplifiers [11,23,24,26–42], current mirrors [43–45], current conveyors, [46,47], voltage followers [48,49], buffers [50], voltage controlled oscillators [51], level shifters [52–54] and phase locked loop [55].

In general, the bulk-driven OTAs offer low gain and operate at low speed due to small g_{mb}. Various solutions have been proposed in the literature to improve the performance of bulk-driven OTAs [11,23,24,26–41,56–61]. The majority of bulk-driven OTAs are designed for improving the DC gain and GBW. In low-voltage environment, the gain of bulk-input OTA can be improved by either cascading the multiple stages or using gain enhancement techniques, or both. In [62], partial positive feedback (PPF) technique is proposed for gain and transconductance enhancement of low-voltage OTAs. The bulk-driven OTAs in [23, 26, 33–36] employ PPF technique to improve the gain. An ultra-low-voltage folded-cascoded OTAs presented in [26, 63] for very low-frequency applications. In this work, an array of composite transistors are used instead of conventional MOS transistors, to enhance the DC gain. Nevertheless, the composite transistor occupies large on-chip area compared to the conventional

transistor. A self-cascode MOSFET structure which boosts the output resistance and enhances the gain, is reported in [31]. Sub 1-V bulk-driven architectures based on two-stage topology were proposed in [11, 31, 32] to improve the gain. These topologies employ Miller compensation in order to the save power and area. In other designs [24, 39, 40], a three-stage topology is employed to improve the gain and bandwidth of OTA. But, these multi-stage topologies need a complex compensation network for stability, which in turn consumes additional power and area. In [24], a process insensitive self-biased bulk-driven OTA is presented, which reduces the current consumption due to the biasing circuit and improves the common-mode and power-supply rejection performance. But, the performance of self-biased OTA is sensitive to the temperature and supply voltage variations.

Recently, the bulk-driven OTAs which operate with a supply voltage of 1-V or below are proposed in [11, 23, 24, 28–31, 33, 36, 37, 40, 60, 64]. In [23, 26, 33–36, 64], PPF technique is employed to enhance effective transconductance of bulk-driven OTA with a low current consumption. In addition, auxiliary blocks such as differential amplifier [34, 37] and current-shunt amplifier [38] are also employed to improve the transconductance. To further improve the transconductance, the auxiliary differential pairs are employed to deliver the input signal to the gate terminal. In [27–29], current recycling technique have been used to improve transconductance of bulk-driven input stage. In these designs, the small signal current passes through two signal paths, which leads to boost the transconductance. However, these approaches are not suitable for sub 1-V design because of the cascode structure which limits the signal swing. A multi-signal path input stage is employed in [28] to enhance the transconductance of folded-cascode bulk-driven topology. In [30], bulk-driven OTA is implemented using flipped voltage follower to improve the linearity and dynamic performance.

Some of these designs reported in [27–29] operate at relatively high voltage and the designs in [23, 24, 30, 33–36] are relatively more sensitive to PVT variations. Although the topologies in [24, 40] operate at low supply voltages, they consume more power and occupies more area. Hence, there is a need for new PVT insensitive OTAs which can work with sub 1-V supplies and smaller quiescent currents.

The techniques presented so far are used to improve the transconductance and gain of bulk-driven OTAs. But, no efforts has been made to improve the large-signal performance parameters such as slew rate. So, in this thesis, more emphasis is given on slew rate enhancement of bulk-driven circuits.

2.5.2 Enhancement of large-signal performance

The feedback amplifiers which can drive large capacitive loads are required in many modern applications such as LDOs, peak detectors, headphone and LCD drivers [65–67]. The output buffers determine the speed, resolution, voltage swing, and power dissipation of a LCD column driver [68]. In addition, hundreds or thousands of buffer amplifiers are integrated into one driver IC, so, the buffer should occupy a small die area and consume low static power.

In general, the output buffers are realized by operational amplifiers with unity-gain feedback. Although these amplifiers often operate at low-voltage and consume low-power, they fail to meet the DC gain and bandwidth requirements. For large C_L, the buffer needs to provide a large output current for quick slewing and faster settling. Moreover, the circuits operating at low supply voltage needs rail-to-rail input and output swings to maintain required SNR and dynamic range.

In sub-nanometer CMOS technologies, due to lower supply voltages, multi-stage architectures are preferred to obtain high DC gain. In conventional techniques, as C_L increases the compensation of multi-stage amplifier becomes very difficult. Since, the large C_L reduces the magnitude of the secondary pole and decreases the phase margin of OTA. Moreover, the OTAs with fixed biased current limits its maximum output current and causes slewing for large C_L. The slew rate can be improved by using a large value of bias current. Based on this principle, several techniques such as adaptive biasing [69–76] and dynamic biasing amplifiers [67, 77–79] are used in the literature. In [38, 80, 81], adaptive biasing technique is employed to improve the slew rate of the bulk-driven OTAs. However, these designs have limited driving capability i.e., high currents are required to drive large C_L.

In [2,65,67–69,76,78,82–99], several techniques are presented to enhance the slew rate of gate-driven OTAs. But, these topologies operate at high V_{DD}. The Class-A OTAs have poor large-signal behavior due to constant bias current source and results a limited output current [2]. The Class-AB OTAs boost the dynamic current for a large differential voltage, as presented in [2, 82, 83]. The bias current of these OTAs varies with the differential input voltage. In [76, 83], a quasi floating-gate technique is employed for slew rate enhancement. To boost the tail current, positive feedback techniques are employed in [69, 84, 85]. These amplifiers recursively copy the output driving current and increase the tail current of the input differential pair during slewing.

In dynamic biasing, the current in output stage is boosted for large signals by measuring the differential input voltage. In [65,67,68,78,86–97], dynamic biasing techniques are employed to enhance

the dynamic current of the buffer amplifier. In these designs, comparator senses the rising and/or falling edges of the input waveform to turn on a push/pull transistor to charge/discharge the output load [68]. But, a current mismatch is required to turn off the output transistors during static operation [67]. For rail-to-rail column driver, a pair of complementary high-speed amplifiers are employed in [87, 98]. In [99], a buffer amplifier is presented with slew rate calibration. Because of calibration, the amplifier can adjust the output current according to C_L.

In summary, the existing bulk-driven topologies are not suitable to drive the large C_L under low-voltage environment. Hence, there is need for new high driving capability low-voltage bulk-driven OTAs.

2.6 Summary

In this chapter, the state-of-the-art techniques used to design low-voltage and low-power analog circuits were presented. First, an overview of the low-voltage and low-power design challenges are presented, and various low-voltage design techniques are briefly described later. Next, the literature review on bulk-driven OTAs have been presented. Moreover, several small-signal and large-signal performance enhancement techniques were also described. The following chapters describe the main contribution of this research.

3

Design of Analog Circuits with STI Effect

Contents

3.1 Introduction

The continuous shrinking of device dimensions in the modern CMOS fabrication technologies simultaneously requires a proportional downscaling of the V_{DD} to maintain device reliability. Also, the relative magnitude of MOSFET OFF current cannot be retained if the V_{TH} does not scale down at the same rate as the supply voltage [39]. Both these factors impose serious challenges for the design of analog circuits.

In addition, as the MOSFET sizes reach the nanoscale regime, a new type of variability known as layout-dependent effect (LDE) [99–121] needs to be addressed in the modern analog and mixed-signal circuit designs and is considered to be as the secondary concern of the circuit design. In particular, two dominant LDEs such as shallow trench isolation (STI) [99, 106–116] and well proximity effect (WPE) [102,117] are found to be significantly affect the V_{TH} and mobility (μ_0) of devices in advanced technology nodes. This is true even in the general analog integrated circuit building blocks.

The WPE is conditioned by the process and depends on the position of a MOSFET in relation (distance) to the well edge. The schematic symbols have no information about such position. During implant process, atoms can scatter laterally from the edge of photoresist mask and embed in the silicon surface in the vicinity of the well edge. This results a change in surface concentration with lateral distance from the mask edge. This lateral non-uniformity in well doping causes the variation in V_{TH} and other electrical characteristics with the distance of the transistor to the well-edge. The WPEs can be minimized by keeping all well edges at consistent distances in all four directions from MOS devices and adding dummy active region oxide diffusion (OD) shapes to minimize OD-OD effects [117].

In nanometer technologies, STI is used to isolate active transistor regions in the layout. In typical fabrication technologies, shallow blocks of STI made of silicon-di-oxide (SiO_2), are inserted into a much larger three-dimensional silicon structure [107]. The STI induces thermal residual stress in active silicon due to the post-manufacturing mismatch between thermal expansion coefficients of SiO_2. The amount of STI around an active region depends on the layout of the design, STI results in placement-dependent variations in the transistor μ_0 and V_{TH} of the active devices. In addition, STI is critical for multifinger devices with extremely narrow width [99,109–116,118]. The STI is a function of finger width (W_F) and length of diffusion, which is the length of the diffusion region under the gate from STI edge to STI edge. The STI wells on the active area of devices, is a by-product of the fabrication process and has increasingly significant impact on the circuit behaviour. Transistor sizing and layout

without considering these effects at a pre-layout stage may result in suboptimal design and layout iterations.

The impact of STI stress on device parameters and the resulted linearity degradation appear as a penalty of multifinger devices for RF and analog design. Hence, it is desirable to develop an accurate and efficient method to analyse the influence of the STI stress on circuit performance comprehensively at a full-chip level. However, choosing a W_F and number of fingers (N_F) to optimize circuit performance is a challenging problem.

In [107], an analytical model based on inclusion theory in micromechanics is employed to accurately estimate the stresses and the strains induced in the active region by the surrounding STI in the layout. The induced changes in μ_0 and V_{TH} are computed at the transistor level, and then propagated to the gate and circuit levels to predict circuit-level delay and leakage power for a given placement.

The two new layouts derived from the standard multifinger MOSFET, i.e., narrow-OD and multi-OD to observe the STI transverse stress effect on g_m, effective mobility (μ_{eff}) and transition frequency (f_T) and most importantly, the low-frequency noise are analysed for both RF and analog circuits design [99, 108–113]. The sub-threshold characteristics of multifinger transistors have been studied in [114]. The sub-threshold slope does not depend only on the gate length but also on N_F. The channel stress variations of multifinger gate structure (MFGS) are modeled empirically using 3-D technology, computer aided design simulations [115, 116]. These stress models along with a model for inverse narrow width effect to establish a physics-based relationship between effective drive current and N_F in MFGS.

Several layout aware design methodologies are proposed [103–106, 118–121], to analyze MOS characteristics and the circuit performance under LDEs. An accurate and efficient finite-element method-based stress simulator has been developed to characterize the influence of STI stress on the performance of RF and analog circuits by considering detailed layout and process information [103]. In [103], the effect of STI stress on the performance of real circuits is studied and established corresponding optimization strategies. The circuit performance variation due to STI effect can be minimized by proper placement of devices. The LDE aware analytical analog placement algorithm is proposed in [105], to mitigate the influence of the LDEs while improving circuit performance, where, the LDEs were transformed into a non-linear analytical placement models. In order to verify the effect of STI stress, a ring oscillator has been designed by varying the N_F of the device [106]. As N_F changes, there is a

deviation in frequency performance of oscillator. In [106], the oscillation frequency is adjusted near to original value by tweaking the N_F of pMOS and nMOS devices. The performance of low noise amplifier is analyzed in [118], as a function of N_F with fixed width transistor.

Layout aware design methodologies that take into account the layout dependent effects at early stage of schematic design are proposed in [104, 120]. Using this methodology, the circuit designer will be aware of device characteristics variation such as V_{TH} and μ_0. The design procedure generates multiple layout for each sub-circuit and checks the electrical constraints of the overall circuit and compares it with reference specifications. But, this method is time consuming process and is not suitable for a large number of transistors.

Use of multifinger technique for layout of analog circuits has the advantage of reduced parasitic and mismatch effects that are commonly associated with the conventional single-finger layouts [122, 123]. On the other hand, a higher value of N_F results in the reduction of W_F and a smaller gate resistance. This will lead to a higher degree of variation in the I_D and g_m of the MOSFET due to STI effect on devices [112]. Such a variation in small-signal parameters cannot be neglected and hence the design of analog circuits to meet the desired set of specifications is a non-trivial and challenging task. In conventional analog IC design, the designers employ analytical methodologies in order to find dimensions of circuit for a required specification [10]. These are straightforward techniques with the requirement of additional iterations for fine tuning and re-simulations to close the design process. Other design methodologies in [124,125], are based on analytical synthesis, give direct relation between I_D, terminal voltages and small-signal characteristics for the given specifications. Nevertheless, these methods are not suitable for low-voltage circuits based on nanoscale devices.

The designs proposed in [103–106,118–121], varied the N_F on a trial and error basis until the design specifications are met. Apparently, redesigning the circuit and redrawing the layout at each iteration is the major drawback of these procedures. Therefore, in this thesis, we proposed a new procedure for designing analog circuits by considering the STI effect on multifinger MOSFET devices. Unlike the other designs, the proposed design uses $\frac{g_m}{I_D}$ and $\frac{I_D}{W}$ characteristics [126], rather than the analytical expressions. In the proposed design procedure, initially, the design parameters are calculated by using g_m/I_D methodology for the desired circuit specifications. In next step, to draw the multifinger layout of the circuit, the N_F of each designed parameter is calculated from the maximum available W_F (or desired W_F). Due to STI stress on multifinger MOSFET, the device performance characteristics gets

affected by changes in N_F, which in turn changes the circuit performance. Therefore, to achieve consistent circuit performance with multifinger devices, the design parameters are re-sized by using I_D/W characteristics for the obtained N_F. In this thesis, we considered the design of a two-stage OTA to validate the proposed methodology.

3.2 Characteristics of Multifinger MOSFET

While making the layout of any circuit, multifinger MOSFETs are extensively employed to reduce the parasitic effects. Because of STI effect in multifinger MOSFETs, deviations occur in device current and this becomes severe in sub-nanometer regime. The spacing among fingers, as well as the distance between the edge finger and the boundary of STI are predefined in the process model. The performance of a MOSFET is determined by its small-signal parameters such as gate transconductance (g_m), drain conductance (g_{ds}), and bulk-transconductance g_{mb}. All these parameters depend on the current flow through the device and it is imperative that a constant current through the device should be maintained to avoid variations in circuit performance.

3.2.1 Drain current characteristics of multifinger MOSFET

The linear $I-V$ model used for nano-scale CMOS device is given in (3.1), g_m can be derived from the differential of I_D w.r.t. V_{GS} and can be written as (3.2) [113]. The effective width (W_{eff}) for multifinger MOSFETs is expressed by (3.3), in which ΔW represents width extension created by STI.

$$I_D = W_{eff} C_{ox(inv)} \left(V_{GS} - V_{TH} - \lambda V_{DS}\right) \mu_{eff} \frac{V_{DS}}{L_{eff}} \tag{3.1}$$

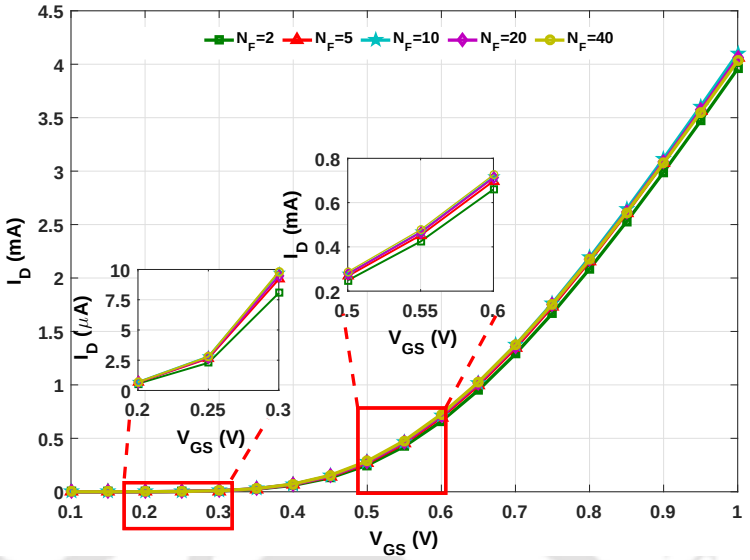
$$g_m = \frac{\partial I_D}{\partial V_{GS}} = W_{eff} C_{\mathrm{ox}(inv)} \mu_{eff} \frac{V_{DS}}{L_{eff}} \tag{3.2}$$

$$W_{eff} = (W_F + \Delta W) \times N_F \tag{3.3}$$

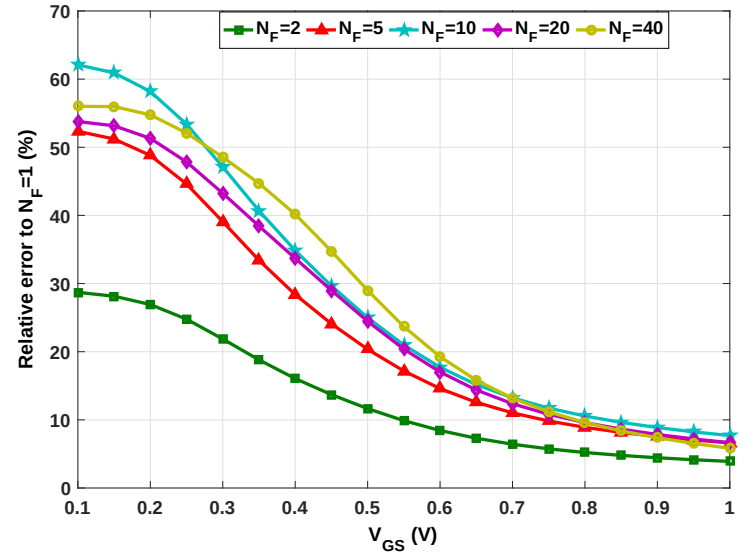
where $C_{ox(inv)}$ is oxide thickness under inversion, L_{eff} is the effective channel length and λ is the channel length modulation parameter.

The $I-V$ relation of MOS transistor operating in the weak inversion region is given by [127]

$$I_D = I_S \frac{W_{eff}}{L_{eff}} \exp\left(\frac{V_{GS} - V_{TH}}{nV_T}\right)\left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right) \tag{3.4}$$



(a)



(b)

Figure 3.1: Characteristics of nMOS for $V_{DS} = 0.5$-V, $W = 20\ \mu m$, and $L = 0.2\ \mu m$ (a) $I - V$ characteristics for different N_F, (b) Relative error of I_D with respect to $N_F = 1$

where I_S is the characteristic current, $V_T\ (= k_B T/q)$ is the thermal voltage and is approximately equal to 25 mV at $T = 27°$ C, and n stands for sub-threshold slope factor. All other symbols have their usual meaning.

If drain-source voltage is $V_{DS} \geq 4V_T$, then the effect of V_{DS} on drain current is very minimal, therefore the drain current can be approximated as follows [8, 127].

$$I_D \approx I_S \frac{W_{eff}}{L_{eff}} \exp\left(\frac{V_{GS} - V_{TH}}{nV_T}\right) \tag{3.5}$$

The g_m of transistor operating in weak inversion is given by

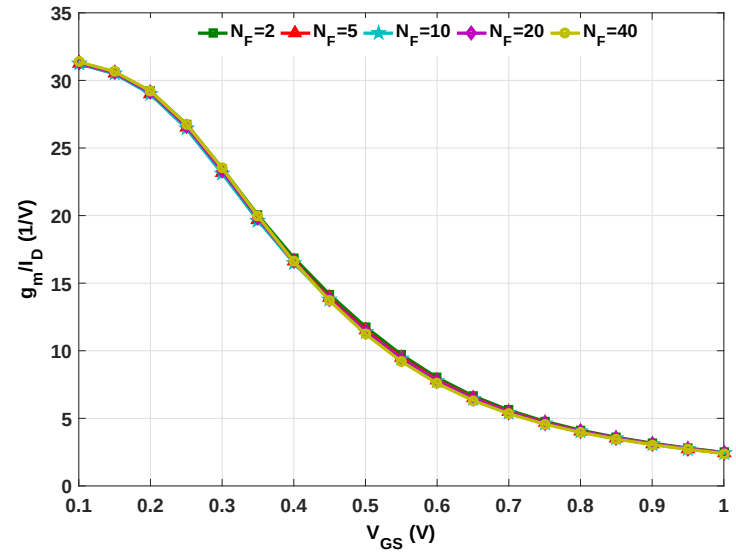
$$g_m = \frac{I_D}{nV_T} \tag{3.6}$$

To observe the STI effect on multifinger MOSFET, the drain current I_D characteristics are plotted as a function N_F (the values are 1, 2, 5, 10, 20 and 40), which is shown in Fig. 3.1(a). The error plot of I_D relative to $N_F = 1$ is shown in Fig. 3.1(b). It can be observed from Fig. 3.1(b) that the change of I_D could be as high as 60% in the sub-threshold region of the MOSFET, though it reduces to less than 10% as the device operating regime changes from weak inversion to strong inversion.

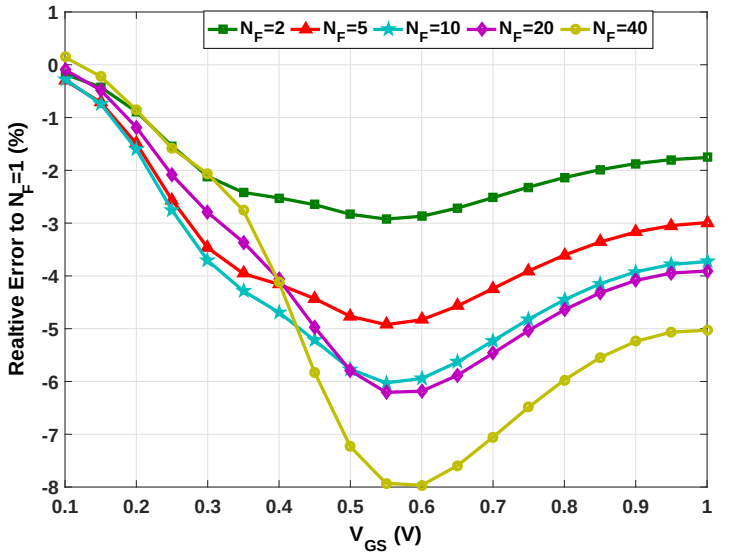
3.2.2 $\frac{g_m}{I_D}$ characteristics of multifinger MOSFET

As discussed in previous Section 3.2.1, I_D changes due to variation in N_F and hence this affects the small-signal parameters of the MOSFET. It is essential to derive the characteristics independent of N_F. The g_m/I_D characteristics for different N_F is shown in Fig. 3.2(a). The error plot of g_m/I_D relative to $N_F = 1$ is shown in Fig. 3.2(b). It can be observed from Fig. 3.2(b) that the g_m/I_D characteristics vary with a maximum error of 8% only. The g_m/I_D characteristics are nearly independent of N_F. Hence, a design based on the g_m/I_D characteristics of a MOSFET allows for a unified synthesis methodology that will be valid for all regions of its operation.

Once the transistor of a given W is characterized over a range of g_m/I_D, the g_m/I_D based parameters can be generalized to a transistor of an arbitrary width. Such a methodology will hold as long as the parameter of interest scales with W. This universal quality of the g_m/I_D versus I_D/W curve can be exploited during the design phase, when the transistors aspect ratios (W/L) are unknown. Once the value of the g_m/I_D ratio is chosen for desired channel length L, i.e., the device operation region is determined, the W of the transistor can be determined from the I_D/W curve for the required bias current.



(a)



(b)

Figure 3.2: Characteristics of nMOS for $V_{DS} = 0.5$-V and $W = 20\ \mu m$, and $L = 0.2\ \mu m$ (a)Transconductance-to-drain current ratio (g_m/I_D) characteristics of nMOS for different N_F, (b) Relative error of g_m/I_D with respect to $N_F = 1$

3.3 Miller-Compensated Two-Stage OTA

To attain high value of DC-gain with low-supply voltage using only a single-stage amplifier is challenging task. Cascading of multiple gain stages is a popular and conventional technique for obtaining high DC-gain. But, this causes instability due to multiple poles, hence a compensation circuit will be required to make the OTA stable. We employed the conventional Miller-compensation technique

for two-stage OTA stability [10]. The schematic of two-stage OTA and its small-signal equivalent model are shown in Fig. 3.3 and 3.4, respectively. Here, C_C is the compensation capacitance, C_1 and C_{out} are the parasitic capacitances, and C_L is the load capacitance. The total output capacitance of the amplifier C_2 is $C_{out} + C_L$. The voltage transfer function that results from the addition of C_C is given in (3.7), where g_{m1} (g_{m6}) is the transconductance of the differential pair $M_1 - M_2$ (output stage M_6), and R_1 (R_2) is the output resistance of the first (second) stage. Also, C_1 and C_2 represents the effective node capacitances at input and output stages, respectively.

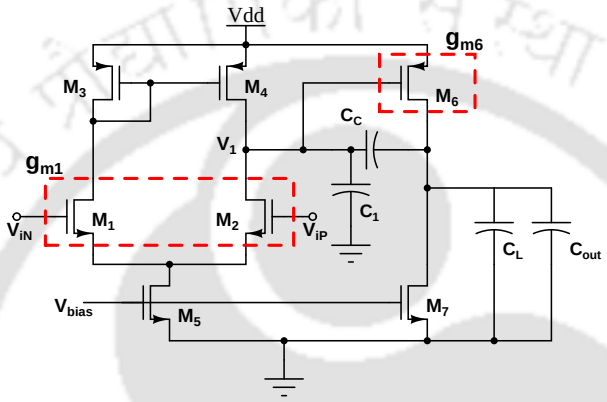


Figure 3.3: Schematic of Miller-compensated two-stage OTA.

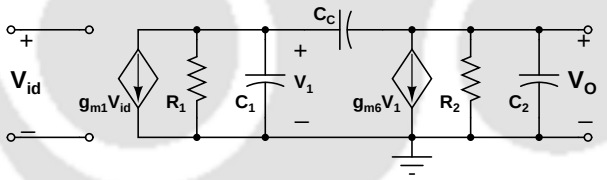


Figure 3.4: small-signal equivalent of two-stage OTA with compensation.

$$\frac{V_o(s)}{V_{in}(s)} = \frac{g_{m1}g_{m6}R_1R_2\left(1 - s\frac{C_C}{g_{m6}}\right)}{1 + s\left[R_1(C_1 + C_C) + R_2(C_2 + C_C) + g_{m6}R_1R_2C_C\right] + s^2R_1R_2\left[C_1C_C + C_2C_C + C_1C_C\right]} \tag{3.7}$$

The expressions for two-stage OTA DC-gain, pole and zero locations can be derived from its transfer function which is given in (3.7). The low-frequency voltage gain (A_V) of OTA is given by

$$A_V = g_{m1}R_1g_{m2}R_2 \tag{3.8}$$

The dominant pole is located at

$$p_d \approx -\frac{1}{g_{m6}R_1R_2C_c} \tag{3.9}$$

and the non-dominant pole is located at

$$p_{nd} \approx -\frac{g_{m6}C_C}{C_2C_C + C_2C_1 + C_CC_1} \tag{3.10}$$

If load capacitance C_L is much greater than C_1 and C_{out}, then $C_2 \approx C_L$, and if C_C is greater than C_1, C_{out} and (3.10) can be approximated as

$$p_{nd} \approx -\frac{g_{m6}}{C_L} \tag{3.11}$$

A feed-forward path from input stage to output causes a Right-Half-Plane (RHP) zero and is located at

$$z_1 = \frac{g_{m6}}{C_c} \tag{3.12}$$

The frequency corresponding to dominant pole, non-dominant pole and RHP zero are $f_{pd} \approx \frac{1}{2\pi g_{m6}R_1R_2C_c}$, $f_{pnd} \approx \frac{g_{m6}}{2\pi C_L}$ and $f_z = \frac{g_{m6}}{2\pi C_c}$, respectively [124].

3.4 Design Procedure for Two-Stage OTA

In this section, the design procedure for Miller-compensated two-stage OTA based on the g_m/I_D characteristics is presented. This determines the geometry of MOSFETs and bias current of the circuit without considering the multifinger effect. The gain-bandwidth of two-stage is given by [124]

$$f_u = A_V f_{pd} \approx \frac{g_{m1}}{2\pi C_C} \tag{3.13}$$

where f_u represents the gain-bandwidth product which is approximately equal to unity gain frequency (UGF) for a stable system.

The normalized frequency of non-dominant pole (P_N) and RHP zero (Z_N) corresponds to f_u are given in (3.14) and (3.15), respectively.

$$P_N = \frac{f_{pnd}}{f_u} = \frac{g_{m6}}{g_{m1}}\frac{C_C}{C_L} \tag{3.14}$$

$$Z_N = \frac{f_z}{f_u} = \frac{g_{m6}}{g_{m1}} \tag{3.15}$$

The phase margin (ϕ_M) of Miller-compensated two-stage OTA is given by [10]

$$\phi_M = 180 - \tan^{-1}\left(\frac{f_u}{f_{pd}}\right) - \tan^{-1}\left(\frac{f_u}{f_{pnd}}\right) - \tan^{-1}\left(\frac{f_u}{f_z}\right) \tag{3.16}$$

The P_N and Z_N are determined from the ϕ_M of amplifier. Here, P_N and Z_N values will be greater than 1 for ϕ_M of 60° since $f_{pnd}, f_z > f_u$ and $f_{pd} << f_u$, and (3.16) can be approximated as follows.

$$\phi_M = 90 - \tan^{-1}\left(\frac{1}{P_N}\right) - \tan^{-1}\left(\frac{1}{Z_N}\right) \tag{3.17}$$

The compensation capacitance C_C can be obtained by combining (3.14) and (3.15) and is given as

$$C_C = \frac{P_N}{Z_N} C_L \tag{3.18}$$

Fig. 3.5 shows the g_m/I_D, I_D/W versus V_{GS} characteristics for both nMOS and pMOS, obtained through simulations using a UMC 65-nm CMOS technology. For each transistor, the g_m/I_D factor is determined first from the design specifications of the OTA. Next, the normalized current I_D/W is determined for each transistor from the g_m/I_D and I_D/W versus V_{GS} curves. Then, once the drain current value is found, the W of each transistor can be obtained. All design parameters (bias current, W and L of MOSFET, C_C etc.) of the OTA are directly influenced by its design specifications. The transistors L are mainly determined by the trade-off between area and DC-gain. The larger channel length enhances the DC gain but it increases the parasitic of devices and area of the OTA. The channel length is considered as 0.2 μm (which is approximately 3 times of minimum channel length) to make the trade-off between the area and DC gain. Moreover, the flicker noise and input referred offset are also decrease due to their inverse relation with L [9].

The step-by-step design procedure for Miller-compensated two-stage OTA is described as follows:

Step 1: To determine the dimension of any MOSFET in a circuit, first determine the bias voltage or g_m/I_D and the bias current from the circuit specification. Trace the normalize current value of respective bias point from Fig. 3.5. Then the width of K^{th} MOSFET can be obtained from (3.19) and is given as

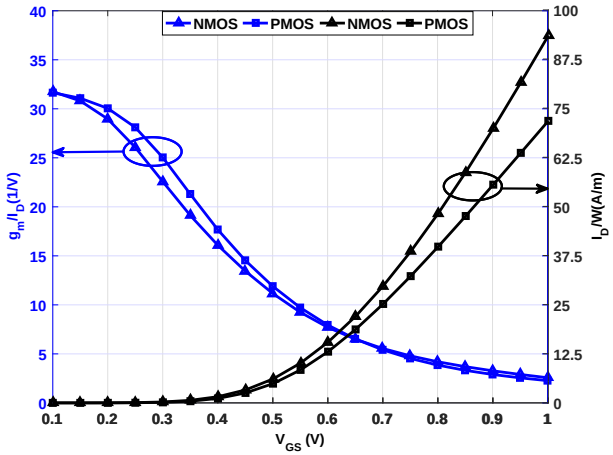


Figure 3.5: Transconductance-drain current ratio($\frac{g_m}{I_D}$) and normalized current ($\frac{I_D}{W}$) curves of nMOS and pMOS devices ($V_{DS} = 0.5$ V and $W = 10\ \mu m$, and $L = 0.2\ \mu m$).

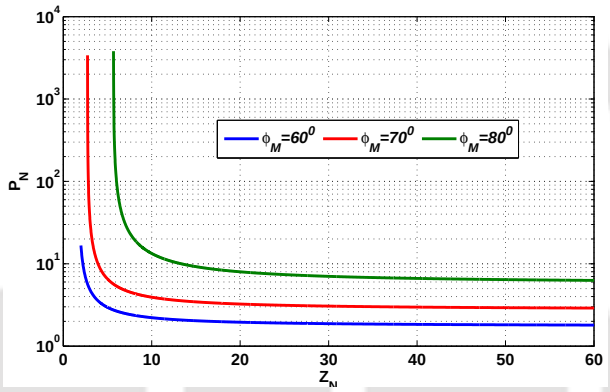


Figure 3.6: Normalized values of non-dominant pole (P_N) and Right-Half-Plane zero (Z_N) w.r.t f_u for different phase margins.

$$W_K = \frac{I_{DN}}{\left(I_D/W\right)_N} \tag{3.19}$$

where W_K, I_{DK} and $(I_D/W)_K$ are the width, drain current and normalized current of K^{th} MOSFET ($K = 1, 2, 3....7$).

Step 2: Estimate the compensation capacitance C_C from the ϕ_M of OTA. From simulation results shown in Fig. 3.6, find the optimum location of P_N and Z_N of a desired phase margin and substitute in (3.18). For the ϕ_M of 60°, the optimum values of P_N and Z_N were found to be 2.2 and 10, respectively. By substituting P_N and Z_N in (3.18), the value of C_C obtained as $0.22C_L$.

Step 3: The input differential stage bias current depends on the internal slew rate (SR_{int}) and compen-

sation capacitor. The bias current of input stage can be expressed as

$$I_{D1} = \frac{SR_{int} \times C_C}{2} \tag{3.20}$$

Step 4: The dimensions of input differential stage transistors ($M_1 - M_2$) depend on the SR_{int} and gain-bandwidth product of OTA and are given as follows:

$$\left(\frac{g_m}{I_D}\right)_1 = 4\pi \frac{f_u}{SR_{int}} \tag{3.21}$$

$$W_1 = \frac{I_{D1}}{\left(I_D/W\right)_1} \tag{3.22}$$

Step 5: The geometry of tail current sink MOSFET (M_5) is calculated from the minimum value of input common mode range ($ICMR_{min}$), using the relation $V_{DS5} = ICMR_{min} - V_{GS1}$, where V_{GS1} is gate-source voltage of M_1. The current sink transistors M_7 and tail current sink transistor M_5 is biased at a voltage of $V_{GS5} = V_{GS1} + V_{DS5}$. The geometry of M_5 is given by

$$W_5 = \frac{2I_{D1}}{\left(I_D/W\right)_5} \tag{3.23}$$

Step 6: Current mirror load transistors (M_3 and M_4) geometry (W_3 and W_4) is calculated from the maximum value of input common mode range ($ICMR_{max}$) which is given by

$$V_{GS3} = V_{DD} - ICMR_{max} - V_{DS1} + V_{GS1} \tag{3.24}$$

where $V_{DS} > 4V_T$, to make weak inversion current independent of V_{DS}

$$W_3 = \frac{I_{D3}}{(I_D/W)_3} \tag{3.25}$$

Step 7: A major proportion of power consumption occurs due to current in second stage, I_{D6}. After selecting the optimum values from Fig. 3.6, (3.15) is used to calculate output transconductance (g_{m6}). A negative slew rate (i.e., external slew rate (SR_{ext})) can result from the output stage because of its dependence on the C_L and load current (I_{D7}). To minimize the offset voltage, the operating region of M_6 should be same as M_3 and M_4 i.e., $V_{GS3} = V_{DS4} = V_{GS6}$.

For symmetry in slew rate, I_{D7} is taken as $I_{D7} = SR_{ext}(C_C + C_L)$. Current through M_6 is a function of output transconductance i.e., $g_{m6} = Z_N g_{m1}$ and is given by

$$I_{D6} = \frac{g_{m6}}{\left(g_m/I_D\right)_3} \tag{3.26}$$

The current through the second stage will be considered among the maximum of I_{D6} and I_{D7}, which gives the values for output transistor widths W_6 and W_7.

$$W_6 = \frac{\max\{I_{D6}, I_{D7}\}}{\left(I_D/W\right)_3}, W_7 = \frac{\max\{I_{D6}, I_{D7}\}}{\left(I_D/W\right)_5} \tag{3.27}$$

Step 8: The systematic offset voltage and current imbalance in the output stage can be minimized by the following condition [10]

$$\frac{\left(\frac{W}{L}\right)_5}{2\left(\frac{W}{L}\right)_{3,4}} = \frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_6} \tag{3.28}$$

3.5 Bulk-driven Current Mirror OTA

In order to show the STI effect on bulk-driven circuits, design of bulk-driven OTA is considered. The schematic diagram of bulk-driven current mirror OTA is shown in Fig. 3.7. The topology is so selected to achieve highly linear voltage-to-current conversion under low supply voltage conditions. The input stage of OTA consists of pMOS bulk-driven differential pair M_1 and M_2, and diode connected M_3 and M_4 devices which acts as an active load. To turn on the bulk-driven input devices, the gate terminal of these devices is connected to a sufficient bias voltage V_{BP2}. Then, the operation of the bulk-driven MOS transistors is similar to a depletion type MOSFET. The current in input devices is modulated due to variation in the bulk-terminal voltage. The differential inputs V_{iN} and V_{iP} are applied across the bulk-terminal of M_1 and M_2, respectively. The current replication branch implemented using M_7 and M_9 which copies the current variation in M_1 to the output stage. The Class-AB output stage implemented using M_6 and M_8 devices. The DC-gain of the bulk-driven OTA shown in Fig 3.7 is given by

$$A_{DC} \approx \frac{B.g_{mb1,2}}{g_{ds6} + g_{ds8}} \tag{3.29}$$

where, B current scaling factor, $g_{mb1,2}$ is the small-signal bulk-transconductance of $M_{1,2}$, and g_{d6}

and g_{d8} represents conductance of M_6 and M_8, respectively.

The dominant pole frequency of bulk-driven OTA is given by

$$f_{Pout} = 1/(2\pi R_o C_L) \tag{3.30}$$

where, C_L is the effective load capacitance at the output node.

From (3.29) and (3.30), the gain-bandwidth product of bulk-driven OTA can be written as

$$GBW = B.g_{mb1,2}/(2\pi C_L) \tag{3.31}$$

The internal poles at node N_1 and N_2 are $f_{PN_1} = g_{m3}/(2\pi C_{N_1})$ and $f_{PN_2} = g_{m3}/(2\pi C_{N_2})$, where $C_{N_1} = C_{gs3} + C_{gs7}$ and $C_{N_2} = C_{gs4} + C_{gs6}$ are the parasitic capacitance at nodes N_1 and N_2, respectively. Typically, the condition $3GBW < f_{PN_1,N_2}$ is used to achieve required phase margin.

The quiescent current in M_1, M_2, M_3 and M_4 is $I_B/2$ and BI_B in M_6, M_7, M_8 and M_9. In order to achieve desired GBW for a given a given load C_L, from (3.31), either B and/or I_B should be large. An increase in I_B leads to increase in static power dissipation. Moreover, an increase in B leads to larger parasitic capacitances at nodes N_1 and N_2, which in turn reduces the phase margin.

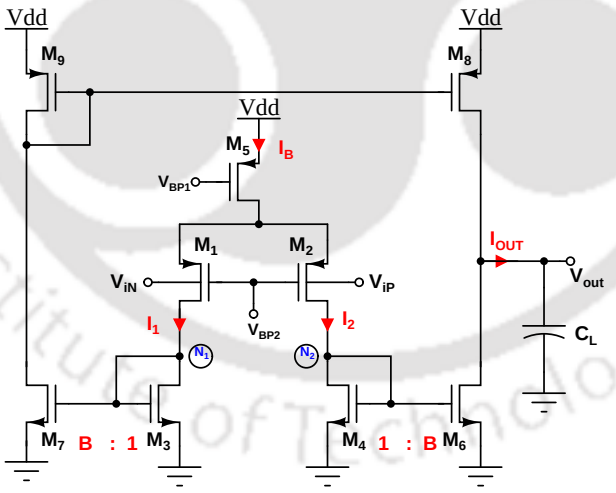


Figure 3.7: Schematic of bulk-driven current mirror OTA.

3.6 Design Procedure for Bulk-driven Current Mirror OTA

In this section, the design procedure for bulk-driven current mirror OTA based on the g_m/I_D and g_{mb}/I_D characteristics is presented. This determines the geometry and bias current of the MOS

devices without considering the multifinger effect. For low-frequency applications, the channel length is considered as 1 μm to minimize the trade-off between the area and DC gain. In order to achieve high g_{mb} and to reduce the size of differential pair, the channel length of bulk-driven input devices is 0.5 μm to achieve high g_{mb}.

As discussed in previous Section 3.2.2, the g_m/I_D characteristics are nearly independent of N_F hence the gate-driven devices are sized using g_m/I_D characteristics. Similarly, the bulk-driven MOS devices are sized using g_{mb}/I_D characteristics. Fig. 3.8 illustrates the g_{mb}/I_D characteristics of bulk-driven pMOS for different value of N_F. It can be observed from Fig. 3.8 that the g_{mb}/I_D of bulk-driven MOS vary with a maximum error of 2% only. Hence, the g_{mb}/I_D characteristics can be used to find the geometry of bulk-driven MOS devices from the given specifications. Fig. 3.9 illustrates the g_m/I_D characteristics of pMOS device for different bulk-source (V_{BS}) voltages. These characteristics are used to size the bulk-driven devices for different common mode input voltage.

The step-by-step design procedure for bulk-driven current mirror OTA is described as follows:

Step :1 To calculate the dimension of gate-driven MOSFETs, the bias voltage or g_m/I_D and the bias current are determined from the circuit specifications. The width of K^{th} MOSFET can be obtained from (3.19), using the normalize current value of respective bias point from Fig. 3.10.

Step :2 The bias current of bulk-driven differential stage bias depends on the GBW of OTA. The effective transconductance of OTA is given by

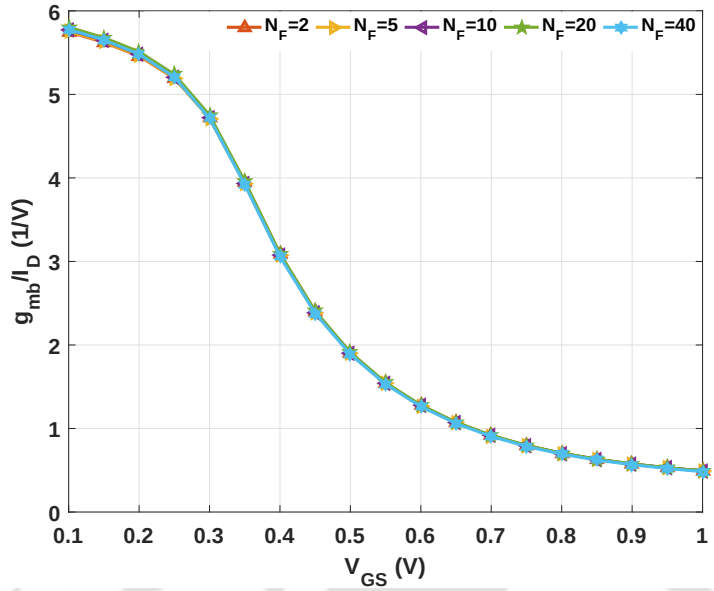
$$g_{mb1} = \frac{GBW \times 2\pi \times C_L}{B} \tag{3.32}$$

The current scaling factor B decides the current requirement in the output stage for the desired bandwidth. The bias current of input stage can be evaluated g_{mb}/I_D characteristics by choosing desired operation region. The bias current of M_1 and M_2 is given by

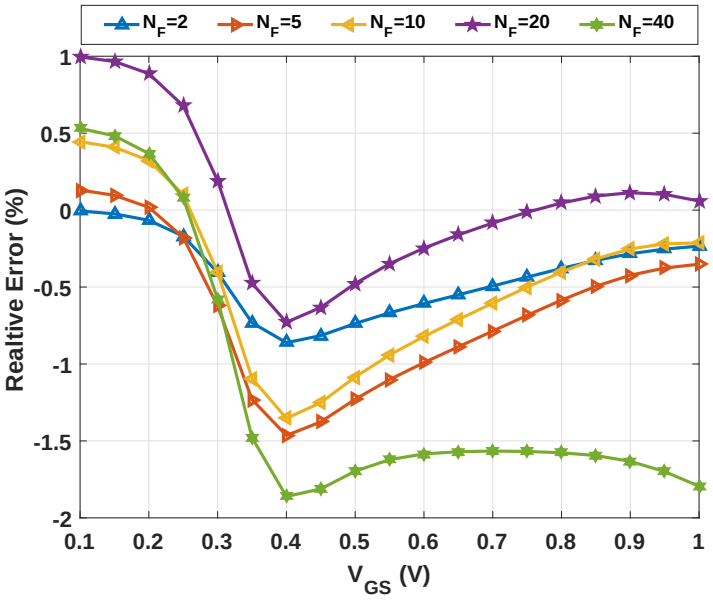
$$I_{D1,2} = \frac{g_{mb1}}{\left(g_{mb}/I_D\right)_1} \tag{3.33}$$

$$W_{1,2} = \frac{I_{D1}}{\left(I_D/W\right)_1} \tag{3.34}$$

Step :3 The current $I_{D3,4}$ in diode connected devices M_3 and M_4 is equal to $I_{D1,2}$. The geometry of



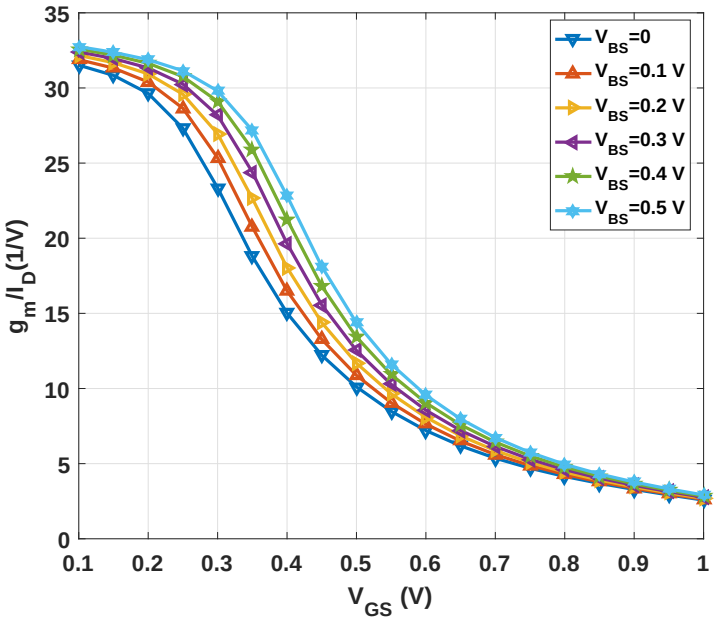
(a)



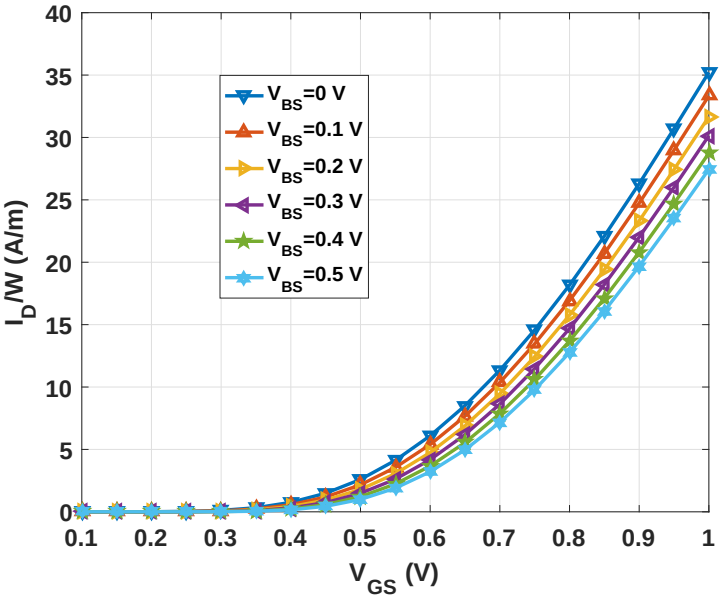
(b)

Figure 3.8: Characteristics of bulk-driven pMOS for V_{DS} = 0.5-V, V_{BS} = 0.25-V and W = 20 μm, and $L = 0.5$ μm (a)Transconductance-to-drain current ratio (g_{mb}/I_D) characteristics of pMOS for different N_F, (b) Relative error of g_m/I_D with respect to $N_F = 1$

$W_{3,4}$ can be calculated from I_D/W characteristics in Fig. 3.10 by selecting the desired operating region. The geometry of M_3 and M_4 is given by



(a)



(b)

Figure 3.9: Characteristics of pMOS for $V_{DS} = 0.5$-V and $W = 10\ \mu m$, and $L = 0.5\ \mu m$ (a) Transconductance-to-drain current ratio (g_m/I_D) characteristics for different V_{BS}, (b) Normalized current (I_D/W) characteristics for different V_{BS}.

$$W_{3,4} = \frac{I_{D1,2}}{\left(I_D/W\right)_{3,4}} \tag{3.35}$$

Step :4 The bias current of M_5 is equal to $2.I_{D1,2}$ and the width of M_5 is given by

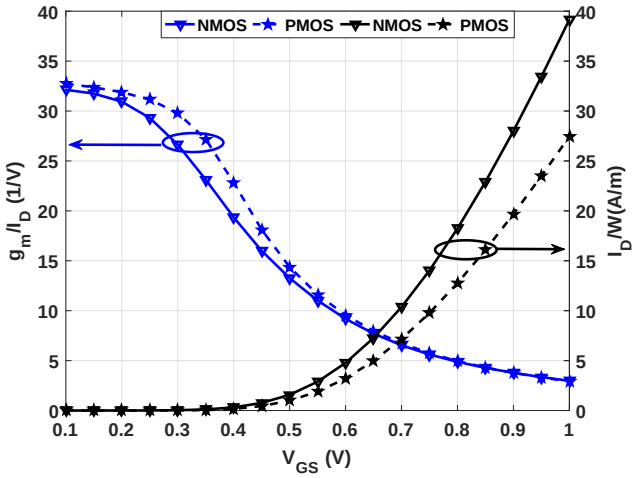


Figure 3.10: Transconductance-drain current ratio($\frac{g_m}{I_D}$) and normalized current ($\frac{I_D}{W}$) curves of nMOS and pMOS devices ($V_{DS} = 0.5$ V and $W = 10\ \mu m$, and $L = 1\ \mu m$).

$$W_5 = \frac{2.I_{D1,2}}{\left(I_D/W\right)_5} \tag{3.36}$$

Step :5 The bias current in $M_{6,7}$ is equal to $B.I_{D1,2}$ and the width of M_6 and M_7 is given by

$$W_{6,7} = \frac{B.I_{D1,2}}{\left(I_D/W\right)_{3,4}} \tag{3.37}$$

Step :6 Similarly, the bias current in $M_{8,9}$ also equal to $B.I_{D1,2}$ and the size of M_8 and M_9 is given by

$$W_{8,9} = \frac{B.I_{D1,2}}{\left(I_D/W\right)_{8,9}} \tag{3.38}$$

3.7 Extraction of Design Parameters with STI Effect

Following the steps 1-8 mentioned in Section 3.4, the design parameters are computed for two-stage OTA using specifications listed in Table 3.1. These specifications mainly target the low-frequency applications such as audio signal processing with the bandwidth of 25 kHz. The load capacitance is assumed to be 2 pF. The obtained design parameters of two-stage OTA are tabulated in Table 3.2.

The circuits are designed using a UMC 65-nm CMOS technology and the maximum allowable MOSFET single finger width is 10 μm. In order to represent the MOS device as multiple fingers, the device width should be more than 10 μm. Due to STI stress on multifinger MOSFET, the device performance characteristics get affected by changes in N_F, which in turn changes the circuit

Table 3.1: Design specifications of two-stage OTA

Specification	Value
V_{DD}(V)	0.5
C_L (pF)	2
DC-gain :A_V (dB)	> 40
Gain-bandwidth: f_u (MHz)	4
Phase margin: ϕ_M (deg)	60
Slew rate: $(V/\mu s)$	2
Input common-mode range: ICMR (V)	$0.25 - 0.3$

Table 3.2: Design parameters of two-stage OTA for the specifications given in Table. 3.1.

Parameter	Value	Units
C_C	0.44	pF
W_1	140	μm
W_2	140	μm
W_3	18.5	μm
W_4	18.5	μm
W_5	16.5	μm
W_6	200	μm
W_7	70	μm

performance and does not meet its specifications.

Traditionally, the N_F will be obtained by dividing the total width by the maximum allowable W_F. This procedure works well for the long-channel CMOS devices due to negligible STI effect. For small-channel CMOS devices with STI effect, the conventional method for finding the W_F is by tweaking the width of each MOSFET until the circuit meets the specifications. This is a difficult and time consuming process. Moreover, as the transistor count increases in a circuit, the process becomes more complicated. To overcome these constraints, we proposed a new design procedure. In which, the geometry of MOSFET is resized by plotting the normalized current characteristics (i.e., I_D/W) using each design parameter for different values of N_F. The normalized current characteristics for different N_F is shown in Fig. 3.11, whereas the device dimensions assumed as $W = 20\ \mu m$ and $L = 0.2\ \mu m$.

As discussed, the g_m/I_D characteristics are less affected due change in N_F. Therefore, the new geometries of each design parameter is evaluated using g_m/I_D and I_D/W characteristics. Before evaluation of new geometries, the minimum N_F for each design parameter need to be calculated from maximum available finger width of CMOS process. And, the new device geometry is calculated for the respective N_F using I_D/W characteristics. The step-by-step procedure for resizing of design

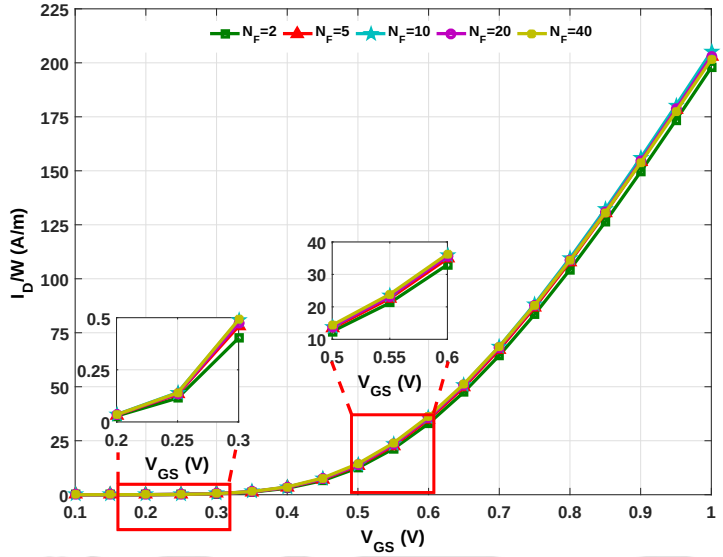


Figure 3.11: Normalized current I_D/W characteristics of multifinger MOSFET ($W = 20\ \mu m$, $L = 0.2\ \mu m$, $V_{DS} = 0.5$ V).

parameters with STI effect is described as follows:

Step 1: The minimum N_F of each transistor is calculated using total device width (W) of transistor and maximum allowable finger width ($W_{F,max}$). In UMC 65-nm CMOS process the $W_{F,max} = 10\ \mu m$. If the device width is greater than $W_{F,max}$, then the device is represented as multifinger device. If any fractional value appears during N_F calculations, which is approximated to the next integer value because N_F should be a integer number. The expression of N_F is given by

$$N_F = \left\lceil \frac{W_K}{W_{F,\max}} \right\rceil \tag{3.39}$$

where W_K represents width of K^{th} transistor

Example: From Table 3.2, the transistor M_5 should represented as multiple finger, since $W_5 = 16.5\ \mu m$ which is greater than $10\ \mu m$ and N_F of M_5 is equal to 2. Similarly, the N_F will be calculated each transistor.

Step 2: In direct scaling, the finger width W_F is calculated for the N_F (obtained from Step 1).

$$W_F = \frac{W_K}{N_F} \tag{3.40}$$

Example: The W_F of M_5 transistor is $8.25\ \mu m$

Step 3: As discussed in Section 3.2, the MOSFET characteristics get affected due to STI effect (i.e., change in N_F). Hence, it is necessary to re-size multifinger devices by considering the STI effect. In proposed method, the I_D/W characteristics of each transistor is extracted like in Fig. 3.11 for N_F (obtained from step 1) and the new geometries for two-stage OTA computed using the following relation:

$$(W_K)_{N_F} = \frac{I_{DK}}{\left[\left(I_D/W\right)_K\right]_{N_F}} \tag{3.41}$$

where, $(W_K)_{N_F}$ is width of K^{th} MOSFET with consideration of N_F, I_{DK} is drain current of K^{th} transistor, $\left[\left(I_D/W\right)_K\right]_{N_F}$ is normalized current of K^{th} device for N_F (obtained from step 1)

Note: The bias conditions of each transistors remain same as before (i.e., V_{GS}, I_D calculated using design procedure in Section 3.4 for a given specification in Table 3.1).

Example: The width of M_5 calculated for required N_F (obtained from Step 1) is 13.5 μm.

Step 4: The finger width of multifinger device for required N_F is given by

$$(W_F)_{N_F} = \frac{(W_K)_{N_F}}{N_F} \tag{3.42}$$

where $(W_F)_{N_F}$ is finger width obtained for required N_F

Example: The $(W_F)_{N_F}$ of M_5 transistor is 6.75 μm

In order to show the STI effect of multifinger MOSEET on circuits performance, in this work, we considered three different cases such as T_1, T_2 and T_3. The $W_{F,max}$ for T_1, T_2 and T_3 is assumed as 10 μm, 5 μm and 2.5 μm, respectively.

By following the steps 1-4 mentioned above, for different test cases the designed parameters are resized. The design parameters for different test cases, using direct scaling and proposed method are listed in Table 3.3. It is clear from Table 3.3 that as compared to the direct scaling, the device finger width for the proposed method is less under the same biasing condition. For example, the transistors W_1 and W_2 in Fig. 3.3, require 14 fingers with each finger width of 10μm using direct scaling whereas using the proposed design the width of each finger is only 5.3 μm for same number of fingers.

Table 3.3: Design parameters of two-stage OTA with STI effect and direct scaling

Design Parameter	Width (μm) $N_F = 1$	T_1 ($W_{F,\max} = 10\mu m$)			T_2 ($W_{F,\max} = 5\mu m$)			T_3 ($W_{F,\max} = 2.5\mu m$)		
		N_F	$W_F(\mu m)$	$(W_F)_{N_F}$ (μm)	N_F	$W_F(\mu m)$	$(W_F)_{N_F}$ (μm)	N_F	$W_F(\mu m)$	$(W_F)_{N_F}$ (μm)
$W_{1,2}$	140	14	10	5.3	28	5	2.66	56	2.5	1.45
$W_{3,4}$	18.5	2	9.25	8.75	4	4.6	4.25	8	2.3	2
W_5	16.5	2	8.25	6.75	4	4.1	3	8	2	1.45
W_6	200	20	10	8.75	40	5	4.25	80	2.5	2
W_7	70	7	10	6.3	14	5	3	28	2.5	1.5

N_F: Number of Fingers; W_F: Finger width obtained from direct scaling; $(W_F)_{N_F}$: Finger width obtained for required N_F.

The design parameters of bulk-driven current mirror OTA are calculated using the step by step procedure outlined in Section 3.5 and are tabulated in Table 3.4. The design parameters of bulk-driven OTA are summarized in Table 3.5. In Table 3.5, the channel length of $M_{1,2}$ devices is 0.5 μm and other devices is 1 μm.

Table 3.4: Design specifications for bulk-driven current mirror OTA

Specification	Value
V_{DD}(V)	0.5
C_L (pF)	10
DC-gain :A_V (dB)	> 15
Gain-bandwidth: f_u (kHz)	100
Phase margin: ϕ_M (deg)	60

Table 3.5: Design parameters of bulk-driven OTA for the specifications given in Table. 3.4.

Parameter	Value	Units
W_1	55.6	μm
W_2	55.6	μm
W_3	7.1	μm
W_4	7.1	μm
W_5	63.4	μm
W_6	188	μm
W_7	188	μm
W_8	879	μm
W_9	879	μm

By following the Steps 1-4 mentioned above, the designed parameters of bulk-driven OTA are resized for different test cases. The design parameters for different test cases, using direct scaling and proposed method are tabulated in Table 3.6.

Table 3.6: Design parameters of bulk-driven OTA with STI effect and direct scaling

Design Parameter	Width (μm) $N_F = 1$	T_1 ($W_{F,\max} = 10\mu m$)			T_2 ($W_{F,\max} = 5\mu m$)			T_3 ($W_{F,\max} = 2.5\mu m$)		
		N_F	$W_F(\mu m)$	$(W_F)_{N_F}$ (μm)	N_F	$W_F(\mu m)$	$(W_F)_{N_F}$ (μm)	N_F	$W_F(\mu m)$	$(W_F)_{N_F}$ (μm)
$W_{1,2}$	55.6	6	9.26	8.2	12	4.63	4	24	2.31	2
$W_{3,4}$	7.1	1	7.1	7.1	2	3.55	3.25	4	1.77	1.65
W_5	63.4	7	9.01	8.39	14	4.52	4.17	28	2.26	2.1
$W_{6,7}$	188	19	9.89	6.6	38	4.95	3.56	76	2.47	2
$W_{8,9}$	879	88	9.98	9	176	5	4.52	352	2.49	2.29

N_F: Number of Fingers; W_F: Finger width obtained from direct scaling; $(W_F)_{N_F}$: Finger width obtained for required N_F.

3.8 Simulation Results

In order to study the efficiency of the proposed method in mitigating the STI effect, we carried out simulations using a UMC 65-nm CMOS technology. The simulations performed for the different test cases of design parameters given in Table 3.3. In all cases T_1, T_2 and T_3, we considered C_L is 2 pF for two-stage OTA and 10 pF for bulk-driven OTA.

Simulated magnitude and phase response of two-stage OTA is shown in Fig. 3.12. It is clear from Fig. 3.12 that, in direct scaling method, the responses obtained for T_1, T_2 and T_3 are different. Whereas, the results obtained using the proposed design exhibits approximately similar responses. Hence, it is evident from Fig. 3.12 that the STI effect is minimized using the proposed design methodology.

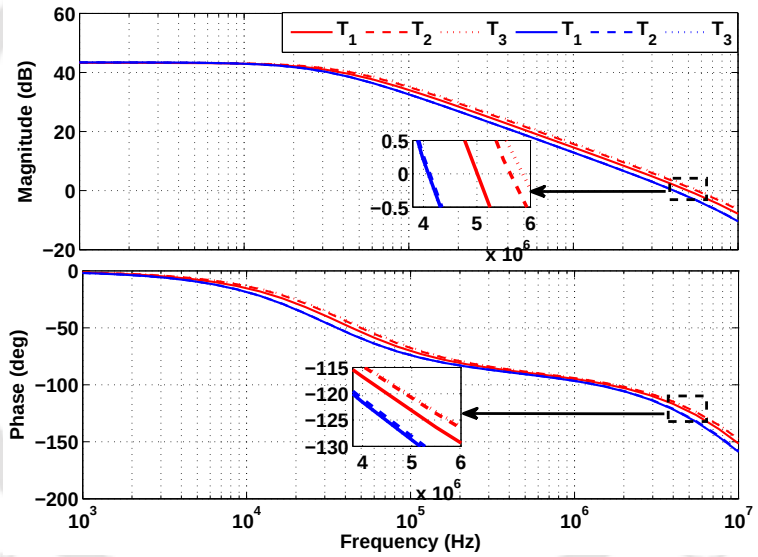


Figure 3.12: Simulated magnitude and phase response of OTA with STI effect (blue) and without STI effect (red).

The transient response is obtained by operating the OTA in non-inverting unity gain configuration with 1 MHz square wave applied at the input and a load capacitance of 2 pF. Fig. 3.13 (a) illustrates the output of proposed OTA with STI effect (blue waveform) as well as the direct scaling without STI effect (red waveform). Fig. 3.13 (b) shows the zoomed portion at the rising edge and the falling edge of output. It can be easily noted down from the zoomed portion that the proposed method minimized STI effect efficiently.

The OTA parameters obtained using the proposed and direct scaling methods are listed in Table.

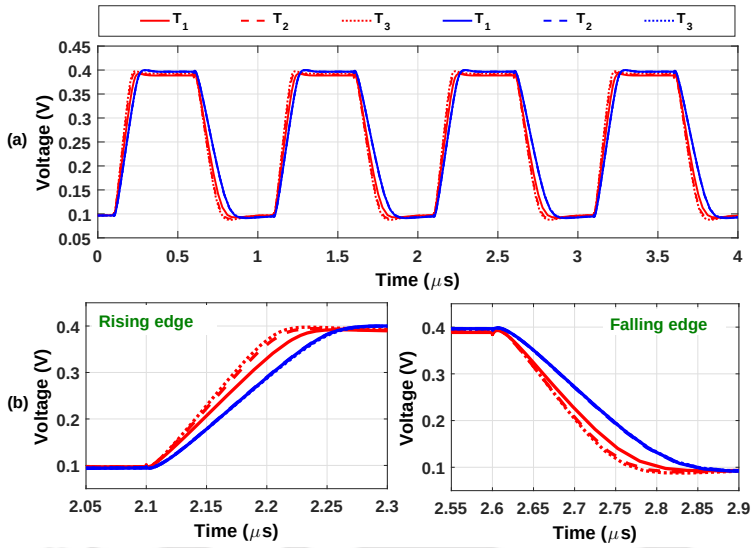


Figure 3.13: Simulated large-signal response (a) and its zoomed portion (b) of the multifinger OTA with STI effect (blue) and without STI effect (red).

Table 3.7: Simulated two-stage OTA performance parameters for the test cases mentioned in Table. 3.3

OTA Parameter	Value	Results					
		T_1		T_2		T_3	
		D	P	D	P	D	P
DC-gain (dB)	> 40	43	43.5	43	43.5	43	43.5
f_u (MHz)	> 4	5	4.1	5.6	4.12	5.9	4.15
Phase margin (deg.)	> 60	57	58.2	55	58.5	54	59
Slew rate ($V/\mu s$)	> 2	2.3	2.06	2.7	2.07	2.88	2.1
Power (μW)	minimum	4.9	3.27	5.2	3.28	5.3	3.3

D: Direct scaling without STI effect consideration; P: Proposed method with consideration of STI effect

3.7. The DC-gain mainly depends on the channel length, hence remains almost same for all the three cases. However, in direct scaling method, the UGF and slew rate change with N_F due to variation in drain current caused by STI effect. The proposed method considered the STI effect (i.e., variation in N_F) during the design of OTA, hence the UGF and slew rate are nearly constant. Moreover, in direct scaling, the OTA achieves the targeted specifications but it consumes more power as compared to proposed method. In case of T_3 in Table. 3.7, the OTA consumes 40% additional power because of STI effect.

Fig. 3.14 illustrates the simulated open-loop output voltage characteristics of two-stage OTA for different cases. From the simulation it can be noted that, the circuit becomes non-linear with direct scaling due to the fact that the output DC operating point moves towards one of the supply rails (

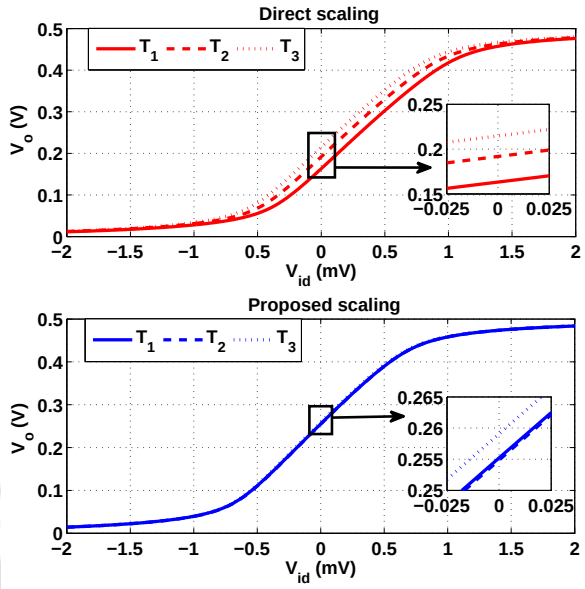


Figure 3.14: Simulated DC open-loop output voltage characteristics of OTA with respect to differential input voltage.

V_{DD} or GND). This results in limited output swing under open-loop conditions and generates distorted output, i.e., clipping occurs in output signal with direct scaling. In the proposed scaling, the two-stage OTA provides the maximum output swing for all test cases since the output bias voltage is always close to its initial bias point i.e., at mid of supply voltage.

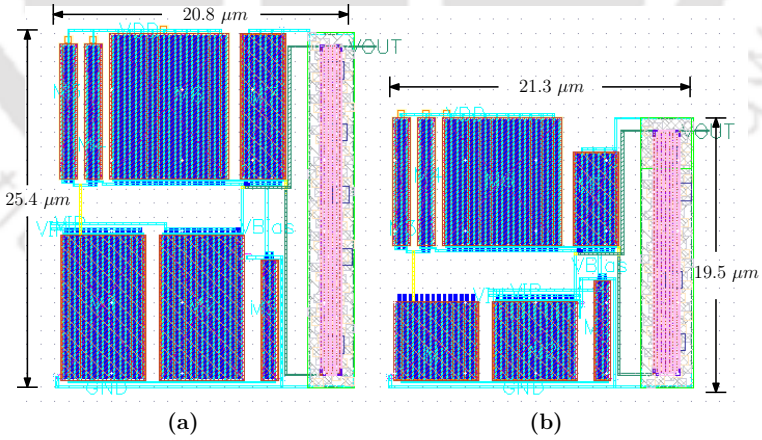


Figure 3.15: Layout of two-stage OTA: (a) with multifinger MOSFETs using direct scaling and (b) with multifinger MOSFETs using proposed scaling

The layout of two-stage OTA for the test case T_1 is shown in Fig. 3.15. The OTA layout based on multifinger devices with direct scaling and proposed scaling is shown in Fig. 3.15 (a) and (b), respectively. The area of two-stage OTA with multifinger MOSFETs using proposed scaling method

is 20 % less compared with direct scaling.

The magnitude and phase response of bulk-driven OTA is shown in Fig. 3.16. It is clear from Fig. 3.16 that, in direct scaling method, there is a variation in the responses of T_1, T_2 and T_3 test cases. Whereas the proposed design exhibits approximately similar responses and the deviation is negligible. Hence, it is clear from Fig. 3.16 that the STI effect is minimized in the bulk-driven circuit using the proposed design methodology.

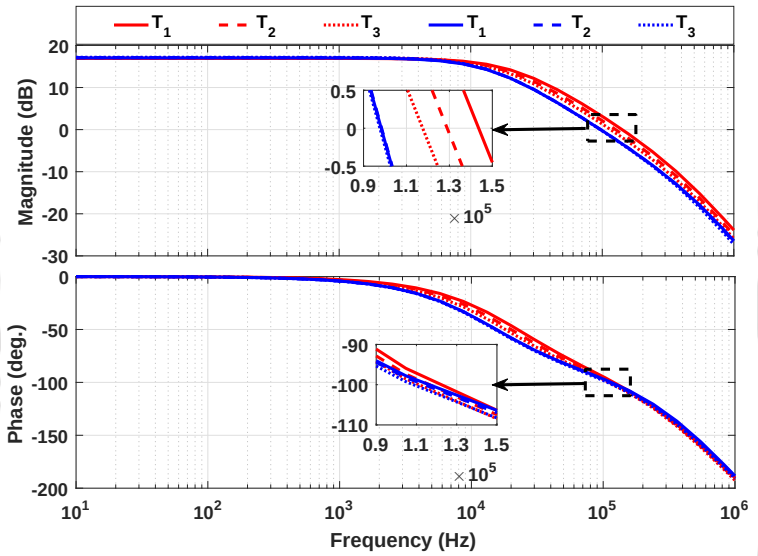


Figure 3.16: Simulated magnitude and phase response of bulk-driven OTA with STI effect (blue) and without STI effect (red).

Fig. 3.13 (a) illustrates the transient response of the bulk-driven OTA with STI effect (blue waveform) as well as the direct scaling without STI effect (red waveform). Fig. 3.13 (b) shows the zoomed portion at the rising edge and the falling edge of output. It is evident from Fig. 3.13 (b) that the proposed method minimized STI variation in the transient response.

The open-loop output voltage characteristics of bulk-driven OTA for different cases is shown in Fig. 3.18. It is clear from Fig. 3.18 that the bulk-driven circuit becomes non-linear with direct scaling due to shift in the output DC bias point. However, in the proposed scaling, the output bias voltage is always closer to its initial bias point in all cases.

The performance parameters of bulk-driven OTA obtained using the proposed and direct scaling methods are listed in Table. 3.8. It is clear from Table 3.8 that the performance varies with changes in direct scaling method. Moreover, the bulk-driven OTA with direct scaling consumes more power because of STI effect.

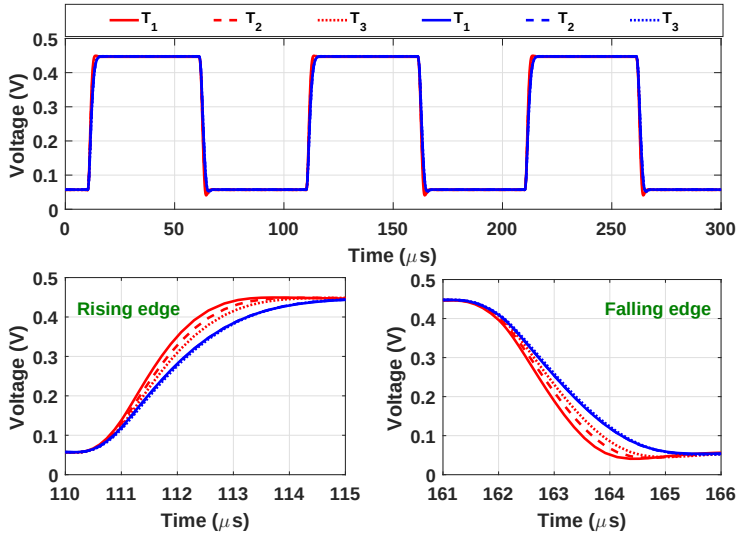


Figure 3.17: Simulated large-signal response (a) and its zoomed portion (b) of the multifinger bulk-driven OTA with STI effect (blue) and without STI effect (red).

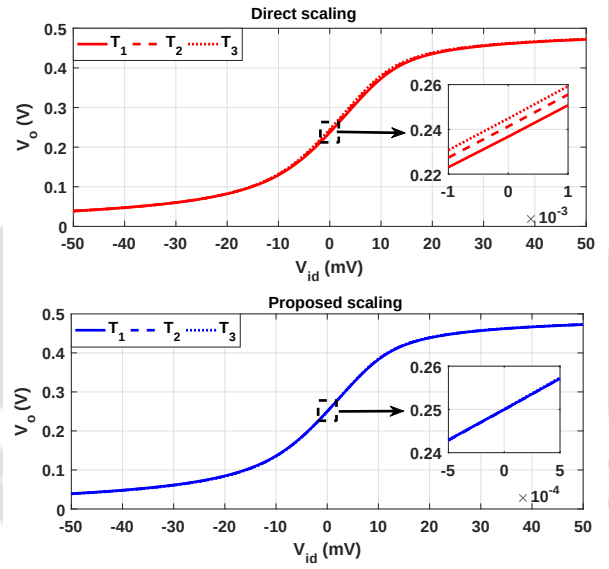


Figure 3.18: Simulated DC open-loop output voltage characteristics of bulk-driven OTA with respect to differential input voltage.

Fig. 3.15 illustrates the layout of bulk-driven OTA for the test case T_1 in Table 3.6. The layout of bulk-driven TOA based on multifinger devices with direct scaling and proposed scaling is shown in Fig. 3.15 (b) and (c), respectively. The area of OTA with multifinger MOSFETs using proposed scaling method is 8 % less compared to direct scaling.

Table 3.8: Simulated bulk-driven OTA performance parameters for the test cases mentioned in Table. 3.6

OTA Parameter	Value	Results					
		T_1		T_2		T_3	
		D	P	D	P	D	P
DC-gain (dB)	> 15	16.91	17	16.96	17.1	17	17.2
f_u (kHz)	> 100	145.9	99.2	132	99.4	119.8	98.7
Phase margin (deg.)	> 60	75	84	77.8	83.5	79	83.5
Power (μW)	minimum	2.56	1.55	2.22	1.55	1.97	1.54

D: Direct scaling without STI effect consideration; P: Proposed method with consideration of STI effect

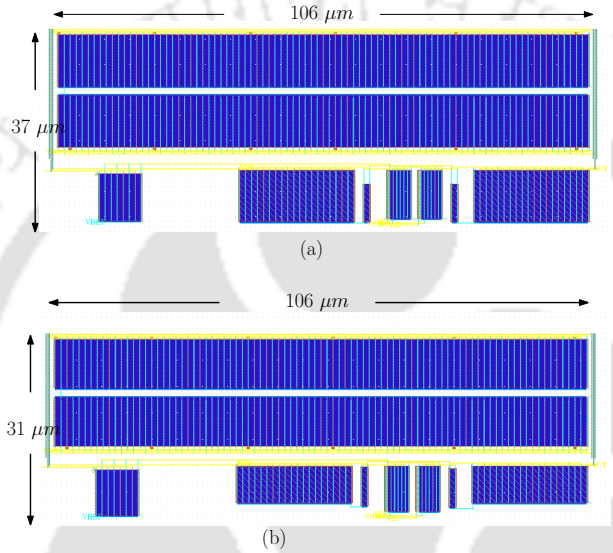


Figure 3.19: Layout of bulk-driven current mirror OTA: (a) with multifinger MOSFETs using direct scaling and (b) with multifinger MOSFETs using proposed scaling.

3.9 Summary

In this chapter an analysis of current-voltage (I-V) characteristics of a MOSFET as a function of number of fingers has been performed. A methodology was proposed to design analog circuits by using g_m/I_D, g_{mb}/I_D and I_D/W characteristics, and N_F is considered while sizing the design parameters. To validate the proposed methodology, Miller-compensated two-stage OTA and bulk-driven OTA is designed for the desired set of specifications. The OTAs performances are matched with the given specifications even for changes in N_F. Also, the proposed method reduces the OTA area as compared to multifinger design with direct scaling.

4

A Low-Voltage PVT-Insensitive Bulk-Driven OTA with Enhanced DC-gain

Contents

4.1 Introduction

The design of high performance with low-power analog circuits is becoming increasingly challenging with the sub-micron CMOS technology. OTA is an important building block in analog circuits and the efficient design of OTA will lead to greater enhancement in the overall analog circuit performance. Design of a high-gain OTA with low-voltage supply is a challenging task, since the conventional cascoding technique is not suitable for OTA with low-voltage supply, due to limitation on signal swing. The OTA should provide high gain to ensure the closed loop transfer function independent of the overall forward path gain, when used in the negative feedback loop. One essential challenge in high resolution and high speed OTA design is simultaneous increase of gain and unity gain frequency. To accomplish these requirements, it is necessary to develop new design techniques to improve the gain with low-voltage supply without loss of performance.

This chapter discusses a PVT-intensive pseudo-differential bulk-driven OTA operating in weak inversion region suitable for low-voltage applications. The proposed bulk-driven OTA offers high DC-gain and high GBW. The amplifier uses a bulk-driven input for rail-to-rail input operation and a differential Class-AB output stage for rail-to-rail output swing. The proposed design employs a partial positive feedback technique for increasing the low-frequency gain of the bulk-driven OTA. In addition, a cross-forward (CF) stage is used to further improve the driving capability and DC-gain. Moreover, the proposed design performance is insensitive to PVT variation..

4.2 Pseudo-Differential Bulk-Driven OTA with Enhanced DC-gain

Schematic of the proposed pseudo-differential bulk-driven OTA shown in Fig. 4.1, the main amplifier consists symmetrical of transistor pairs i.e., each transistor is accompanied by its counterpart in the opposite branch. These transistors operate in the weak inversion region and biased at mid-of-supply voltage (i.e., $V_{DD}/2$) to obtain desired bias current. In order to achieve the maximum voltage swing, the input and output common-mode node voltages are set to $V_{DD}/2$. The input stage is designed using a triple-well CMOS process with access to the bulk-terminal of nMOS transistor. The bulk terminals of active load transistors at input stage are biased at common-mode voltage in order to reduce the V_{TH} of device which makes it easy to operate at low-voltage. The proposed OTA architecture mainly consists of input, output, and cross-forward stages.

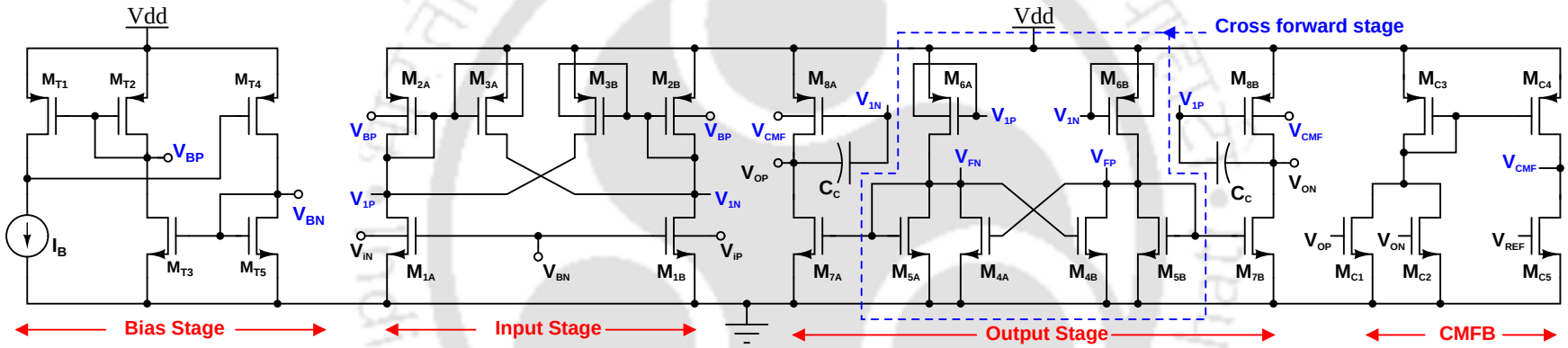


Figure 4.1: Schematic of the proposed pseudo-differential bulk-driven OTA

In addition, a CMFB circuit is employed for the output stage. It will help in keeping the output common-mode node voltage to a known reference voltage (V_{REF}). The details of the different stages are discussed in the sub-sequence subsections.

4.2.1 Input stage

A bulk-driven pseudo-differential pair comprises of $M_{1A,B} - M_{3A,B}$ used as the input stage of the proposed OTA. Differential inputs V_{iN} and V_{iP} are applied across the bulk terminal of M_{1A} and M_{1B}. The input stage is loaded with diode connected pMOS transistors $M_{2A} - M_{2B}$. Another pair of pMOS transistors $M_{3A} - M_{3B}$, were configured in a cross-coupled mode to cancel gate transconductance and to enhance the gain of the input stage. The bulk terminals of $M_{3A} - M_{3B}$ are also connected in a cross-coupled manner, which helps in further improvement of gain. For differential input signal, the cross-coupled pair acts as partial positive feedback and produces a negative transconductance which reduces the overall load conductance. This sets the differential-mode gain of the first stage to a high value. For common-mode input signal, the first stage gain is a low value, because the cross-coupled pair acts as negative feedback hence increases the overall load conductance.

4.2.2 Cross-forward stage

The CF stage formed with transistors $M_{4A,B} - M_{6A,B}$, is a part of the output stage. The differential output of the first stage is attached to common source transistors M_{6A} and M_{6B} which are loaded with cross-coupled transistors M_{4A} and M_{5B}. This arrangement offers finite DC-gain for differential-mode signals, and enhances transconductance of output stage and overall DC-gain of OTA. It also helps to improve the stability of OTA for large capacitive loads. Moreover, the CF stage subtracts common-mode signals and offers a smaller common-mode gain, resulting in the improvement of CMRR of OTA.

4.2.3 Output stage

The output stage consists of two identical common-source transistor pairs $M_{7A} - M_{8A}$ and $M_{7B} - M_{8B}$. In order to obtain Class-AB operation at the output nodes, the differential output of CF stage is connected to M_{7A} and M_{7B}, transforming it into an active amplifying device. Here, CF stage acts as a current replication branch and also offers finite voltage gain. The load driving capability of OTA depends upon the output stage transconductance. For large capacitive loads, the Miller compensated OTAs require large transconductance at output stage [10]. For this, a high current is required at the

output stage to maintain the desired stability. Instead, the use of CF stage in the proposed design enhances the output stage transconductance with only a small current in the output stage.

4.2.4 CMFB stage

When the input common-mode voltage changes in fully-differential OTA architectures, the output node voltage will saturate to one of the supply rails due to the mismatch between transistors. Hence, we employed CMFB circuit for the proposed pseudo-differential OTA, to maintain the output common-mode voltage at reference voltage (V_{REF}). The CMFB circuit in Fig. 4.1 is based on one discussed in [31]. The CMFB circuit, constituting transistors M_{C1} to M_{C4}, performs the tasks of the common-mode detection and reference comparison. If there is any mismatch between output common-mode voltages of OTA, the feedback mechanism adjusts both the output node voltages to the desired value (i.e., V_{REF}). The CMFB circuit offers finite gain and improves CMRR with common mode input. The bandwidth of CMFB circuit should be more than that of OTA in order to avoid compensation for CMFB circuit.

4.2.5 Bias stage

In Fig. 4.1, the bias voltages V_{BP} and V_{BN} are generated using bias generator circuit [128]. The transistors $M_{T1} - M_{T5}$ with bias current source I_B are arranged in a feedback configuration to generate bias voltages V_{BP} and V_{BN}. With this arrangement, the bias voltages will change according to the PVT variations.

4.3 Analysis of the Proposed High Gain OTA

The important performance parameters of OTA, such as differential gain, common-mode gain and input-referred noise (IRN) are analyzed. The proposed pseudo-differential circuit is symmetrical and parameters of the transistor M_{kA} are equal to M_{kB} with opposite phase (k = 1, 2, 3, ...8). The mathematical equations for the performance parameter are expressed as function MOSFET small-signal parameters such as bulk transconductance (g_{mbk}), gate transconductance (g_{mk}) and drain conductance (g_{dsk}) of k^{th} transistor .

4.3.1 Differential-mode analysis

In Fig. 4.1, the bulk-driven transistors M_{1A} and M_{1B} at input stage are loaded with diode connected transistors M_{2A} and M_{2B}. To improve the gain, transistors M_{3A} and M_{3B} are cross-

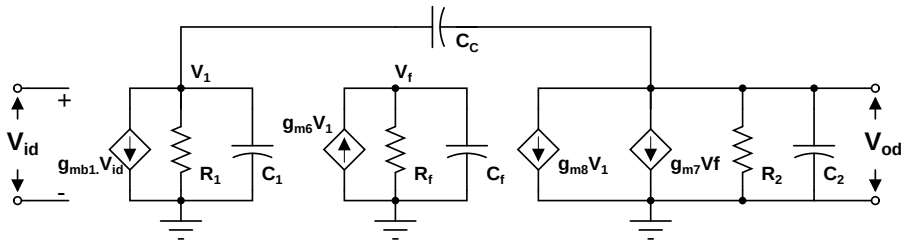


Figure 4.2: Small-signal circuit model of the proposed OTA for frequency analysis

coupled, which gives a negative transconductance and cancels the effect of diode transistors M_{2A} and M_{2B} and hence improves the overall gain of input stage. The gain of OTA depends on the channel length of MOS devices.

In differential-mode, the frequency characteristics can be studied using its small-signal equivalent model in Fig. 4.2. The differential gain (A_{DM}) of the circuit is derived by nullifying all frequency dependence components in the small-signal model and is given by equation (4.1). The A_{DM} is ratio of differential output voltage ($V_{od} = V_{OP} - V_{ON}$) to differential input voltage ($V_{id} = V_{iP} - V_{iN}$). The partial positive feedback configuration cancels the gate transconductance and offers larger gain. Here, the major part of differential DC-gain is contributed by the output stage. Due to presence of CF sage, the effective output stage transconductance of OTA is enhanced to $g_{m6}R_f$ with R_f being the effective output resistance of CF stage (i.e., at node FN/FP).

$$A_{DM} = \frac{g_{mb1}}{(g_{ds1} + g_{ds2} + g_{m2} - g_{m3} + g_{ds3} - g_{mb3})} \cdot \frac{\left(g_{m8} + g_{m7}\frac{g_{m6}+g_{mb6}}{g_{ds6}+g_{ds5}+g_{m5}+g_{ds4}-g_{m4}}\right)}{(g_{ds7} + g_{ds8})} \tag{4.1}$$

In Fig. 4.2, R_1, R_2 and R_f represents the effective resistance of input, output and cross-forward stages, respectively. C_1 and C_f are the parasitic capacitance of input and cross-forward stages, respectively, and C_2 is load capacitance at output stage.

4.3.2 Common-mode analysis

This analysis is performed to understand the effect of common-mode signal on the output nodes (V_{OP} and V_{ON}) by calculating the common-mode gain (A_{CM}). The CMRR defined as the ratio of A_{DM} to A_{CM}, is another performance parameter of OTA. Which is used to measure the ability of the OTA to reject common-mode signals. The A_{CM} is calculated using the equivalent half-circuit of the proposed OTA and the expression for A_{CM} is given by

$$A_{CM} = \frac{g_{mb1}}{(g_{ds1} + g_{ds2} + g_{m2} + g_{m3} + g_{ds3} + g_{mb3})} \cdot \frac{\left(g_{m8} - g_{m7}\frac{g_{m6}+g_{mb6}}{g_{ds6}+g_{ds5}+g_{m5}+g_{ds4}+g_{m4}}\right)}{\left(g_{mb8}\frac{g_{mc4}}{g_{dsc4}+g_{dsc5}} + g_{ds7} + g_{ds8}\right)} \tag{4.2}$$

For common-mode input signal, the cross coupled transistor configuration provides negative feedback at input and CF stages, resulting in a lower resistance. The CF stage reduces the output stage transconductance and hence lowers the common-mode gain. The CMFB circuit acts as an amplifier for common-mode input and it reduces the overall common-mode gain of OTA.

4.3.3 Noise analysis

The noise performance of a multi-stage amplifier is dominated by the gain of its input stage at low and medium frequencies [40]. The noise contribution of second stage is negligible compared to input stage. The first stage of the proposed OTA has a gain >20 dB. The power spectral-density of IRN $S_{v(f)}$ for a bulk-driven transistor in weak inversion is given by equation (4.3).

$$S_v(f) = \frac{8}{3}\frac{K_B T g_m}{g_{mb}^2} + \frac{K_F}{C_{OX} W L f}\frac{g_m^2}{g_{mb}^2} \tag{4.3}$$

The total IRN voltage of proposed OTA is given by (4.4), which comprises of both thermal and flicker noise components. Both noise components are expressed individually for comparison purpose. The input-referred flicker noise voltage ($V_{n,1/f}^2$) and thermal noise voltage ($V_{n,th}^2$) are given by equation (4.5) and (4.6), respectively.

$$\overline{V_{n,in}^2} = \overline{V_{n,th}^2} + \overline{V_{n,1/f}^2} \tag{4.4}$$

$$\overline{V_{n,1/f}^2} = \frac{2}{C_{OX} f g_{mb1}^2}\left[\frac{K_{fn} g_{m1}^2}{W_1 L_1} + \frac{K_{fp} g_{m2}^2}{W_2 L_2} + \frac{K_{fp} g_{m3}^2}{W_3 L_3}\right] \tag{4.5}$$

$$\overline{V_{n,th}^2} = \frac{8 K_B T}{3 g_{mb1}}\left[\frac{g_{m1} + g_{m2} + g_{m3}}{g_{mb1}}\right] \tag{4.6}$$

where, K_{fn}, K_{fp} flicker noise coefficients for nMOS and pMOS transistors, respectively. All the other symbols have their usual meanings.

The IRN will be large for a bulk-driven OTAs because of low bulk-transconductance. It is clear from (4.5) that the flicker noise component is more dominant in the low-frequency range. The flicker

noise can be minimized by choosing the large size input transistor for required bias current. By increasing the transconductance of input stage (i.e., g_{mb1}) thermal noise can be reduced. There is a trade-off between the noise and biasing current of input stage.

4.3.4 Frequency compensation

The small-signal equivalent model of circuit Fig. 4.1 is shown in Fig. 4.2. This model is similar to that of a conventional Miller compensation model [10], except for an additional transconductance (g_{m7}) component at the output stage. The transconductance of output stage is enhanced by the common source amplifier formed by $M_{4A,4B} - M_{6A,6B}$ and loads arranged in cross-coupled fashion. The intermediate stage between input and output stages creates a cross-forward path. The pole due to intermediate stage appears at higher frequencies and it does not show any effect on stability. The dominant pole and the non-dominant pole are real and widely located due to compensation capacitor (C_C). The unity gain frequency of OTA is given by

$$\text{UGF} \approx \frac{g_{mb1}}{2\pi C_C} \tag{4.7}$$

4.4 Simulation Studies

In order to validate the proposed OTA topology, the circuit is designed and post-layout simulations are carried out in a UMC 65-nm CMOS process. Long-channel MOS devices offer high due to high drain resistance. However, the parasitic capacitance will increase as area of device increases and this results in poor frequency performance. Hence, the moderate channel length (0.5 μm) devices are chosen to minimize the trade-off between gain and parasitic capacitance. The threshold voltage of nMOS (V_{THn}) and pMOS (V_{THp}) transistor is 0.38 V and 0.42 V, respectively, and channel length of both devices is equal to 0.5 μm. The design of proposed OTA is targeted for the following specifications:

- DC-gain: >60 dB
- Unity gain frequency: >500 kHz
- Phase margin: >60°
- Load capacitance: 20 pF
- Supply voltage: 0.5-V

Unlike the conventional two-stage OTA reported in [10], the proposed pseudo-differential OTA contains an additional CF stage. The cross-forward path time constant depends on cross-coupled current mirrors. The effect of pole due to cross-forward stage and the RHP zero due compensation capacitance can be ignored near the unity gain frequency. The dominant pole (P_{d1}) and first non-dominant pole (P_{d2}) are real and are widely separated due to compensation capacitor. The dominant pole at output node of first stage (i.e., node $V1$ in Fig. 4.1) is given by

$$P_{d1} \approx -\frac{1}{R_1 R_2 g_{mII} C_C} \tag{4.8}$$

The first non-dominant pole (P_{d2}) at node V_O is given by

$$P_{d2} \approx -\frac{g_{mII}}{C_L} \tag{4.9}$$

where, $g_{mII} = g_{m8} + g_{m7}\frac{g_{m6}+g_{mb6}}{g_{ds6}+g_{ds5}+g_{m5}+g_{ds4}-g_{m4}}$

The RHP zero due to feed-forward path is given by

$$Z_{d1} \approx \frac{g_{mII}}{C_C} \tag{4.10}$$

The second non-dominant pole (P_{d3}) due to cross-forward stage is given by

$$P_{d3} \approx -\frac{1}{R_f C_f} \tag{4.11}$$

where, R_f represents output resistance of CF stage and is equal to $R_f = \frac{1}{g_{ds6}+g_{ds5}+g_{m5}+g_{ds4}-g_{m4}}$ and C_f is the parasitic capacitance at output node of CF stage.

As discussed in Chapter 3, in order to achieve required phase margin (i.e., $> 60°$) the pole P_{d2} should placed at the location which is 2.2 times that of UGF and RHP zero should keep at the location which is atleast 10 times away from the UGF. To drive large load capacitance (i.e., 20 pF) with UGF of 500 kHz, conventional design requires large compensation capacitance this results in huge current requirement in the input and output stages. However, in the proposed, the cross-forward stage improves the output stage transconductance g_{mII} with low quiescent current, and it reduces the compensation capacitance (C_C) and also improves the UGF of OTA. In order to meet the given specifications the following design steps are followed:

Step 1: The C_C of OTA can be evaluated using the following expression:

$$C_C = 2.2\frac{g_{mb1}}{g_{mII}}C_L \tag{4.12}$$

If $g_{mII} = K_1 * g_{mb1}$, then $C_C = \frac{2.2}{K_1}C_L$. Where K_1 represents the ratio of transconductance at output and input stages given by

$$K_1 = \frac{g_{m8} + g_{m7}A_{CF}}{g_{mb1}} \tag{4.13}$$

where, A_{CF} represents the gain of cross-forward stage, $A_{CF} = \frac{g_{m6}+g_{mb6}}{g_{ds6}+g_{ds5}+g_{m5}+g_{ds4}-g_{m4}}$. The A_{CF} can be adjusted by changing the current ratio of M_4 and M_5. The maximum gain of CF stage can be achieved if $g_{m4} = g_{ds6} + g_{ds5} + g_{m5} + g_{ds4}$, which creates second non-dominant pole near the UGF and causes stability issues. Hence, the CF is designed such that the pole due to CF stage occurs at very high frequency.

Step 2: The input stage of OTA is designed to obtain the desired transconductance g_{mb1} given by

$$g_{mb1} = 2\pi C_C \times UGF \tag{4.14}$$

Step 3: Design the output stage (i.e., g_{mII}) for a arbitrary value of K_1 which is normally greater than 10. Here, g_{mII} is combination of second stage transconductance and cross-forward stage gain. By increasing the gain of CF stage A_{CF}, the current requirement in input and output stages can be minimized. The gain of A_{CF} increases due to increase in output resistance R_f. However, for large value of R_f, the p_{d2} move towards near UGF which causes OTA unstable. Hence, there is a limitation on DC-gain of cross-forward stage.

Step 4: All the devices are sized using g_m/I_D and g_{mb}/I_D methodology (as discussed in Chapter 3).

Step 5: After extracting the device sizes of input and output stage, check the DC-gain and stability of OTA.

Step 6: Increase the value of K_1 and repeat steps from 1 to 5 until the desired specifications are met.

The dimensions of transistors and operating conditions are extracted from design steps, the compensation capacitance (C_C) of 0.85 pF is obtained which meets the stability and UGF requirement.

The open-loop magnitude and phase characteristics of the proposed amplifier at different load conditions is shown in Fig. 4.3 and outcome parameters are summarized in Table. 4.1. The CF stage enhances the output stage transconductance and keeps the non-dominant pole at higher frequencies and hence the OTA is expected to remain stable for larger loads. The proposed OTA is able to drive a load capacitance of up to 50 pF with only a small reduction in unity gain frequency. Also, it gives a phase margin larger than 55°.

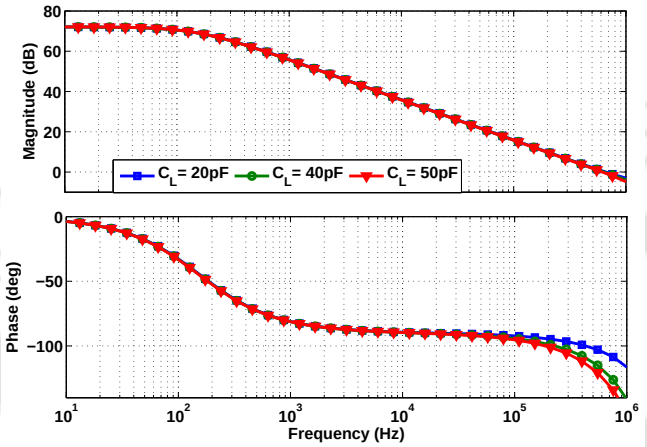


Figure 4.3: Simulated open-loop frequency response of the proposed OTA for different C_L.

Table 4.1: DC-gain, UGF, and phase margin with different load conditions.

Parameter	C_L		
	20 pF	40 pF	50 pF
DC-gain (dB)	72	72	72
UGF (kHz)	680	655	630
Phase margin (deg.)	74	60	55

To observe the open-loop frequency due to process variation, the corner simulations have been performed with a C_L of 20 pF and a supply voltage of 0.5-V. The magnitude and phase responses for different corners are shown in Fig. 4.4. At typical corner, the low-frequency voltage gain is 72 dB and the phase margin is 74° at a unity gain frequency of 680 kHz. To observe the effect of various process corners on the noise performance, noise analysis has been performed and the response is shown in Fig. 4.5. From the simulation results, it can observed that the noise response is minimally deviated from the typical value for different process corners. At power line frequency (i.e., at 50 Hz), the CMRR and PSRR is approximately equal to 120 dB and 144 dB, respectively. The observed CMRR and PSRR values at 50 Hz are good enough to reject the power line interference in biomedical applications.

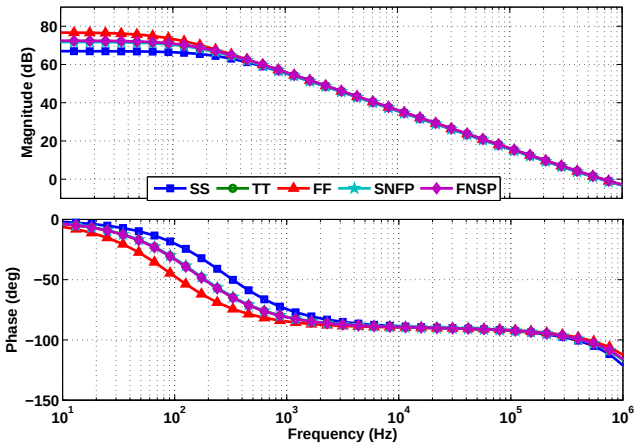


Figure 4.4: Simulated frequency response of OTA with different corners of the process model.

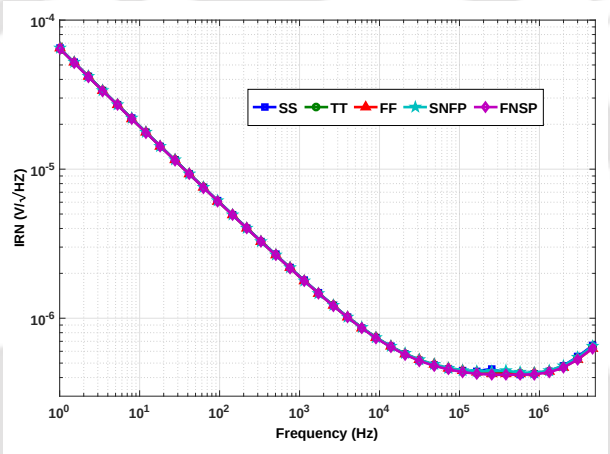


Figure 4.5: Simulated input-referred noise response for different process corners.

The CMFB circuit stability simulation results is shown in Fig. 4.6. The loop gain of CMFB is 30.4 dB and provides bandwidth of 307 kHz with phase margin of 61.2°.

To observe performance of OTA in closed-loop condition, the proposed OTA is configured as voltage buffer with the help of resistive feedback network [39]. In order to avoid the loading effect, the feedback resistance should be large as compared to the output node resistance (i.e., R_2). The buffer linear output swing range is observed by sweeping the differential input voltage (V_{id}). The DC characteristics of voltage buffer and its corresponding error plot $V_{out} - V_{id}$ is shown in Fig. 4.7. It is clear from Fig. 4.7 that the design offers rail-to-rail output swing for rail-to-rail input, where the output is closer to input with negligible error voltage.

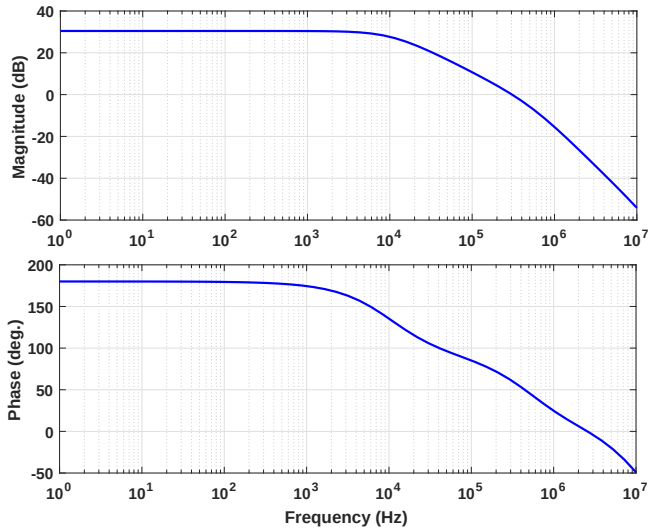


Figure 4.6: Stability simulation results of CMFB loop.

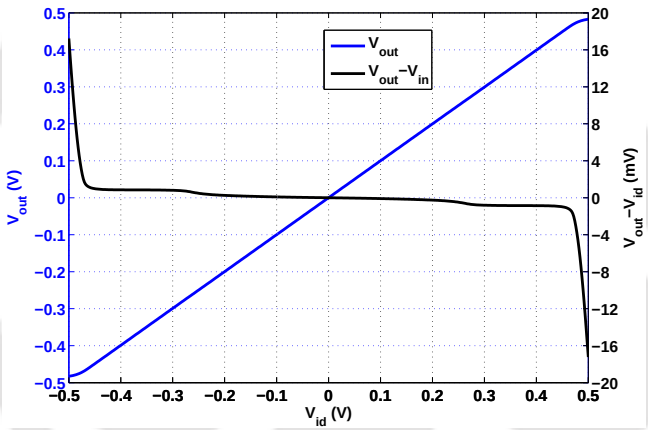


Figure 4.7: Simulated DC input and output characteristics of the unity-gain amplifier

To observe the settling and slewing behavior of the proposed OTA, a step voltage of 0.5-V at a frequency of 10 kHz is applied to the voltage buffer, and the transient response is shown in Fig. 4.8. The differential slew rate, which corresponds to the time interval for the differential output voltage to change from 10% to 90% of the input pulse, is obtained as 0.16 $V/\mu s$ and settling time (t_s) is 10 μs for 1% steady state error.

The proposed OTA can be used as a tunable transconductor whose transconductance varies over a wide range by varying the bias voltage of input transistors M_{1A} and M_{1B}. Bias voltages V_{BP} and V_{BN} are generated with the help of a constant bias current I_B source and diode connected MOS transistors as shown in Fig. 4.1. The change in I_B results in a corresponding variation of V_{BP} and V_{BN} as shown

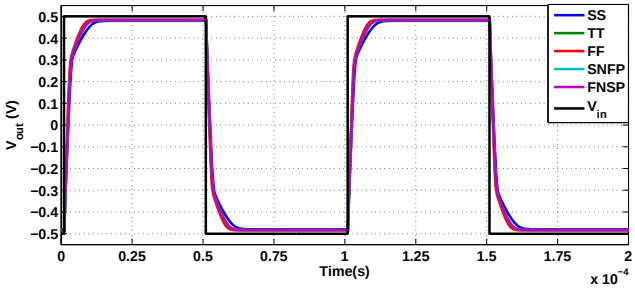


Figure 4.8: Simulated transient response of the unity gain amplifier for different corners.

by Fig. 4.9. The change in V_{BN} results in the variation of input transconductance. V_{BP} is employed for bulk-biasing of M_{2A} and M_{2B}. The node voltages of input stage V_{1P} and V_{1N} are equal even with change in bias current because of cross-coupled connection.

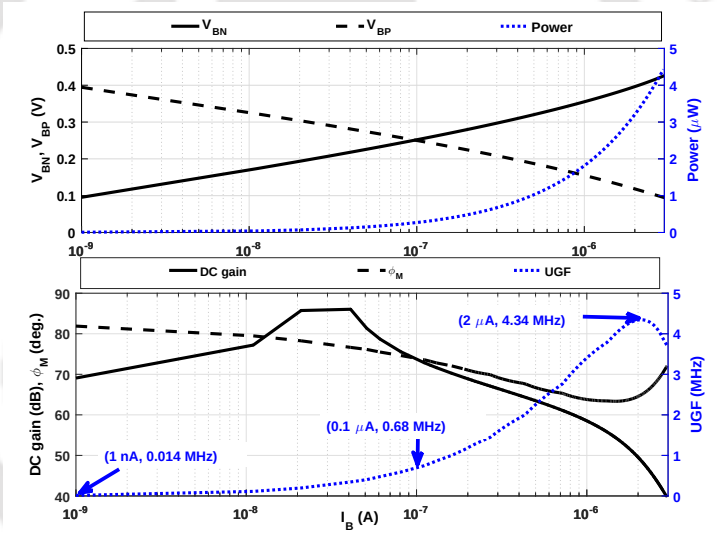


Figure 4.9: DC-gain, UGF and phase margin of the proposed OTA with I_B variation.

In order to verify the robustness of the proposed amplifier, simulations were performed for different PVT conditions. The AC, DC, and transient analyses have been performed at different corners of CMOS process such as SS, SF, TT, FS, and FF, for supply-voltages of 0.45-V, 0.5-V, and 0.55-V. The temperature has been varied from -55°C to 120°C. It has been observed that the amplifier remains operative and shows consistent performance under these circumstances.

The parameters of the proposed OTA for different PVT cases are summarized in Table 4.2, 4.3 and 4.4. It is clear from Table 4.2, 4.3 and 4.4 that the proposed OTA performance is PVT-insensitive. Since, in all PVT cases, the proposed OTA meets the desired specifications i.e., DC-gain > 65 dB,

UGF > 500 kHz, and phase margin > 60°. The OTA shows even better performance in 65% cases, offering high DC-gain > 70 dB, UGF > 600 kHz, and phase margin > 70°.

In order to improve the voltage gain of the OTA, a partial positive feedback technique is employed. The cross-coupled transistors M_{3A}, M_{3B} and M_{4A}, M_{4B} are introduce partial positive feedback at input stage and cross forward stage, respectively. The positive feedback generates the negative resistance at the drain node of $M_{2A,B}$ and $M_{5A,B}$, which partially compensate the conductance of the diode-connected transistors $M_{2A,B}$ and $M_{5A,B}$. Thus lowering the load conductance of the first stage and consequently improving its voltage gain. Note, that in order to keep the circuit stable, the resulting conductance at the drain node of $M_{2A,B}$ and $M_{5A,B}$ should always be positive, which leads to the following condition:

$$g_{m3} < g_{m2} + g_{ds2} + g_{ds3} + g_{ds1} \tag{4.15}$$

$$g_{m4} < g_{m5} + g_{ds5} + g_{ds4} + g_{ds6} \tag{4.16}$$

In practical realizations, special care should be taken to fulfil the (4.15) and (4.16) in the presence of possible device mismatch and PVT variations. As the proposed design meets the above criteria since we left some bias margin for the PVT variations while designing the OTA.

Monte Carlo analysis is performed at room temperature for 1000 samples with 20 pF capacitive load and supply voltage of 0.5-V. The Monte Carlo simulation results are summarized in Table 4.5. From Table 4.5, it can be observed that the mean value (μ) of each parameter is closer to its typical value, and standard deviation (σ) is very small compare to its mean value. The ratio between σ and μ shows sensitivity for process and mismatch variations and it is < 5% for the proposed OTA design.

To validate the operation of the proposed OTA under process and device mismatch variation, the Monte Carlo simulation has been performed with sigma value of 3, to investigate the variation effect on UGF, phase margin, DC-gain and CMRR and concerned histogram plots are shown in Fig. 4.10. The mean value of UGF, phase margin, DC-gain and CMRR have been found to be 678.6 kHz, 74°, 72.2 dB and 122 dB, respectively, at C_L of 20 pF. The layout of the proposed design is shown in Fig. 4.11.

Table 4.2: Simulated parameter for process and temperature variations, V_{DD}=0.45-V.

V_{DD}=0.45-V															
Process corner	SS			TT			FF			SNFP			FNSP		
Temperature (^{o}C)	-55	27	120	-55	27	120	-55	27	120	-55	27	120	-55	27	120
DC-gain (dB)	59.5	62.4	60.6	66	67	63.4	71	70.5	62	66.3	67	62.2	65.4	67	64
UGF (KHz)	675	644	508	719	664	517	730	670	518	702	647	507	733	680	526
Phase margin (deg)	69.4	70	71	72.3	72.6	73.2	72	75	75	724	73	73.6	72.6	72.4	74
Slew rate (↑)(V/ms)	72	114	134	106	137	158	124	158	176	101	140	160	105	136	158
Slew rate(↓)(V/ms)	72	114	134	106	137	158	124	158	177	102	141	161	105	136	159
CMRR (dB) @ DC	125	113	105	147	117	108	137	120	107	137	118	108	133	116	107
PSRR (dB) @ DC	104	119	113	117	135	110	139	120	103	115	137	111	114	133	114
$t_s^+(\mu s)$ 1%	15.4	10.5	9.1	11.3	9	7.9	9.9	8	7.2	11.5	8.8	7.8	11.4	9	8
$t_s^+(\mu s)$ 0.1%	18.5	13.3	11.5	14.1	11.2	10	12.1	9.8	9	14.2	10.9	9.9	14.3	11.2	10.1
$t_s^-(\mu s)$ 1%	15.4	10.5	9	11.3	9	7.9	9.8	7.9	7.1	11.5	8.7	7.8	11.4	9	7.9
$t_s^-(\mu s)$ 0.1%	18.6	13.3	11.5	14.1	11.2	10	12.1	9.9	9.1	14.	10.8	9.8	14.3	11.3	10.1
IRN at 10 kHz ($\frac{\mu V}{\sqrt{Hz}}$)	0.76	0.72	0.77	0.77	0.72	0.77	0.77	0.72	0.77	0.77	0.72	0.78	0.76	0.72	0.77
Total current (μA)	3.82	4.07	4.84	4.14	4.8	6.5	4.73	6.45	10.3	4	4.4	5.7	4.3	5.4	7.9

Table 4.3: Simulated parameter for process and temperature variations, V_{DD}=0.5-V.

V_{DD}=0.5-V															
Process corner	SS			TT			FF			SNFP			FNSP		
Temperature (^{o}C)	-55	27	120	-55	27	120	-55	27	120	-55	27	120	-55	27	120
DC-gain (dB)	66.3	67	64.5	71	72	68	77.7	76.2	66	72	72	66.2	72	72.4	69
UGF (KHz)	725	668	521	740	698	527	742	681	526	724	662	517	755	696	536
Phase margin (deg)	71.5	71.6	72	74	74	74.3	76.4	76	76	74	74	75	74	73.7	74
Slew rate(↑)(V/ms)	81	134	156	122	159	184	143	182	206	112	163	186	123	158	184
Slew rate(↓)(V/ms)	81.2	134	156	122	159	184	143	182	206	112	163	186	123	158	184
CMRR (dB) @ DC	140	117	109	138	121	112	140	126	111	145	122	111	135	121	112
PSRR (dB) @ DC	117	124	125	126	145	119	142	131	111	125	137	120	124	139	122
$t_s^+(\mu s)$ 1%	17.2	11.7	10.1	10.6	10	8.7	11.1	8.9	7.9	13.2	9.7	8.6	13	10.1	8.7
$t_s^+(\mu s)$ 0.1%	19.3	14.7	12.4	16	12.2	10.8	13.6	10.7	9.8	16	11.9	10.6	16.1	12.4	11
$t_s^-(\mu s)$ 1%	17.2	11.7	10.1	10.6	10	8.7	11.1	8.8	7.9	13.2	9.7	8.6	13	10.1	8.7
$t_s^-(\mu s)$ 0.1%	19.5	14.6	12.5	16	12.2	11	13.6	10.7	9.9	16	11.9	10.5	16.1	12.4	11
IRN at 10 kHz ($\frac{\mu V}{\sqrt{Hz}}$)	0.76	0.72	0.77	0.76	0.72	0.77	0.77	0.72	0.77	0.77	0.72	0.78	0.76	0.7	0.77
Total current (μA)	4.48	4.8	5.65	4.84	5.6	7.6	5.5	7.5	11.9	4.7	5.2	6.6	5.1	6.3	9.2

Table 4.4: Simulated parameter for process and temperature variations, V_{DD}=0.55-V.

V_{DD}=0.55-V															
Process corner	SS			TT			FF			SNFP			FNSP		
Temperature (^{o}C)	-55	27	120	-55	27	120	-55	27	120	-55	27	120	-55	27	120
DC-gain (dB)	71	71.4	69	78	78.7	73.4	87.5	88.6	70.1	78	78.2	71	78.3	79.7	75.5
UGF (KHz)	745	682	530	750	690	534	750	690	534	736	673	524	756	706	543
Phase margin (deg)	73.3	73	73.4	75.6	75.2	75	77.6	77.2	77	75.7	75.6	76	75.3	75	75
Slew rate(↑)(V/ms)	88	151	172	135	178	203	160	202	230	121	182	205	139	176	204
Slew arate(↓)(V/ms)	88	151	172	135	178	203	160	202	230	121	182	205	139	176	204
CMRR (dB) @ DC	136	121	113	141	128	118	148	138	115	144	128	116	139	128	119
PSRR (dB) @ DC	124	129	137	134	146	128	151	147	118	133	142	128	133	145	130
$t_s^+(\mu s)$ 1%	17.5	11	9.6	12.2	9.3	8.3	10.3	10.6	7.6	12.6	9	8.1	12.2	9.3	8.3
$t_s^+(\mu s)$ 0.1%	19.5	15.4	14.1	16.5	13	12.5	14	11.6	11.5	16.7	12.6	12.1	16.5	13	13
$t_s^-(\mu s)$ 1%	17.4	11.1	9.6	12.2	9.4	8.3	10.3	10.7	7.6	12.6	9	8.1	12.2	9.4	8.3
$t_s^-(\mu s)$ 0.1%	19.5	15.4	14.1	16.4	13	12.6	14	116	11.4	16.7	12.6	12.1	16.5	13.1	13.2
IRN at 10 kHz ($\frac{\mu V}{\sqrt{Hz}}$)	0.76	0.72	0.77	0.76	0.72	0.77	0.77	0.72	0.77	0.77	0.72	0.77	0.76	0.71	0.76
Total current (μA)	3.16	5.5	6.5	5.56	6.4	8.7	6.3	8.6	13.6	5.4	5.96	7.6	5.8	7.2	10.5

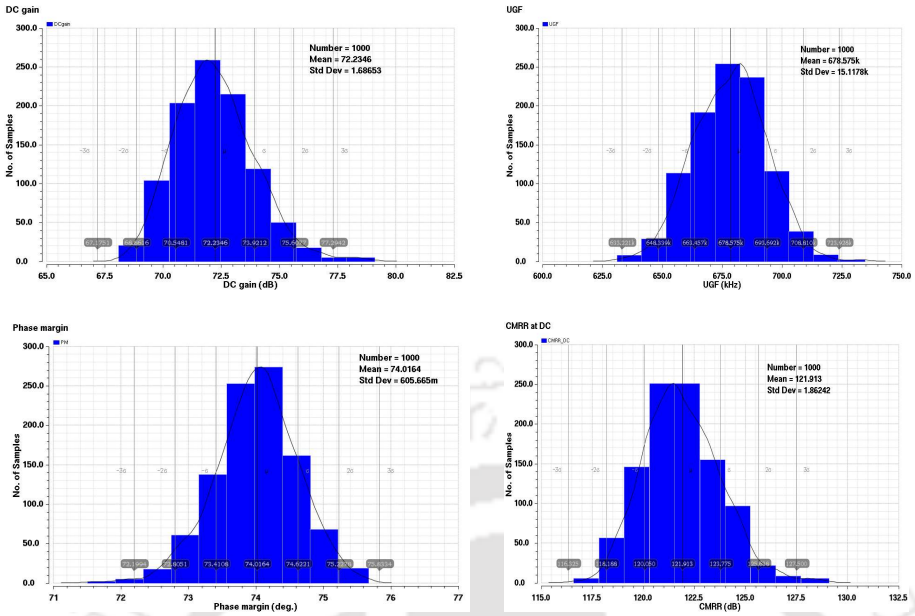


Figure 4.10: Histogram of DC-gain, UGF, phase margin and CMRR from Monte Carlo simulation for 1000 runs.

Table 4.5: Monte Carlo simulation results

Parameter	μ^*	σ^{**}	σ/μ	Parameter	μ^*	σ^{**}	σ/μ
DC-gain (dB)	72.2	1.68	2.3 %	Slew rate(↑)(V/ms)	159.3	7.5	4.7 %
UGF (kHz)	678.6	15.1	2.2 %	Slew rate(↓(V/ms)	159.3	7.5	4.7 %
Phase margin (deg.)	74	0.6	0.8 %	$t_s^+(\mu s)$ 1%	10.01	0.435	4.3 %
CMRR (dB) @ DC	122	1.8	1.5 %	$t_s^+(\mu s)$ 0.1%	12.25	0.6	4.9 %
PSRR (dB) @ DC	141.6	1.86	1.3 %	$t_s^-(\mu s)$ 1%	10	0.432	4.3 %
IRN at 10 kHz ($\frac{\mu V}{\sqrt{Hz}}$)	0.72	0.003	0.4 %	$t_s^-(\mu s)$ 0.1%	12.25	0.6	4.9 %

Note: $*$: Mean value ; $**$: standard deviation

4.5 Performance Summary and Comparison

For performance comparison of various parameters of different OTAs, we adopted the definition of figure-of-merit (FOM) given in [11,26]. It useful to evaluate the efficiency of different OTAs which are operated at a different supply voltage and load conditions. The FOM dimensions of each performance parameter is not similar and higher a FOM is the indication of efficient design. The definition of FOMs for various small-signal and large-signal parameters as follows:

The FOM expressions for UGF is given by

$$\text{IFOM}_S = \text{UGF} \times \frac{C_L}{\text{I}_\text{T}} \left[\frac{\text{MHz} \times \text{pF}}{\mu A}\right] \times 100 \tag{4.17}$$

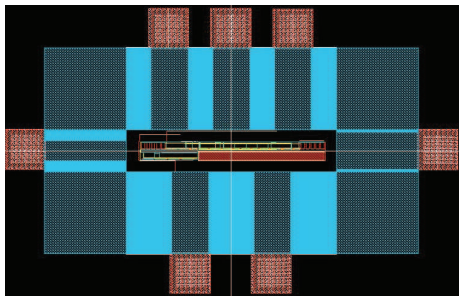


Figure 4.11: Layout of the proposed bulk-driven OTA.

where IFOM$_S$ captures the energy efficiency of OTA.

The FOM of slew rate is given by

$$\text{IFOM}_L = \text{Slew rate} \times \frac{C_L}{\text{I}_\text{T}} \left[\frac{V}{\mu s} \times \frac{\text{pF}}{\mu A}\right] \times 100 \tag{4.18}$$

where IFOM$_L$ represents the current boosting factor of OTA, which is ratio of maximum output current to total quiescent current consumption of OTA.

In addition to these, another FOMs are required to reflect the efficiency of DC-gain and low-voltage operation. Since, the proposed OTA in this chapter is mainly designed to achieve high gain under low-voltage operation.

The FOM expression for DC-gain is given by

$$\text{FOM}_{A_V} = \text{DC} - \text{gain} \times \frac{\text{UGF} \times \text{C}_\text{L}}{\text{Power}} \left[\frac{\text{dB} \times \text{MHz} \times \text{pF}}{\mu W}\right] \times 100 \tag{4.19}$$

where FOM$_{A_V}$ describes the performance of OTA at very low frequencies.

Another FOM also calculated to reflect the low-voltage operation and it is given by [26]

$$\text{IFOM}_T = \frac{V_{THn} + |V_{THp}|}{V_{DD}} \times \frac{UGF \times C_L}{\text{I}_\text{T}} \left[\frac{\text{MHz} \times \text{pF}}{\mu A}\right] \times 100 \tag{4.20}$$

where the first term captures the extent of low-voltage operation and the second term captures the energy efficiency (i.e.,IFOM$_S$).

The performance parameters of proposed and existing low-voltage OTAs are summarized in Table 4.6. The performance of the proposed OTA is also verified with the scaling down in the supply voltage. The simulation results with supply voltage of 0.35-V are summarized in Table 4.6.

Table 4.6: Performance summary and comparison with existing sub-1 V bulk-driven OTAs in literature.

Parameter	**This work**		[28]	[30]	[36]	[38]	[40]$^{\otimes}$	[24]$^{\otimes}$	
CMOS Technology (nm)	65		180	180	50	180	180	65	
Output type (S/D)	D		D	D	D	S	S	S	
Supply (V_{DD}) (V)	0.5	0.35	1.2	±0.25	0.4	0.5	0.7	0.5	0.35
DC-gain (dB)	72	55	65.5	112	60	67.8	57.5	46	43
UGF (MHz)	0.68	0.6	147	0.07	2.2	0.00326	3	38	3.6
Phase margin (deg.)	74	68	81	53	56	69	60	76	56
Slew rate(↑)(V/μs)	0.159	0.19	69.3	0.057	0.86	0.00084	1.8	43	5.6
Slew rate(↓)(V/μs)	0.159	0.19	69.3	–	–	0.00059	3.8	–	–
IRN ($\mu V/\sqrt{Hz}$) at 10 kHz	0.72	0.72	5.9 at 1 Hz	0.7	0.12	0.56 at 1 kHz	0.1 at 1 MHz	0.938	0.926
CMRR (dB) @ DC	121	106	–	133	80 at 5 kHz	–	19	35	46
PSRR (dB) @ DC	145	88	–	119	–	–	52.1	37	35
1% $t_s(+)(\mu s)$	10	7.5	0.02	–	–	210	1.3	–	–
1% $t_s(-)(\mu s)$	10	7.5	0.02	–	–	301	1	–	–
C_L (pF)	20		5	15	20	15	20	3	
I_T (μA)	5.75	4.15	300	1.2	60	0.052	36.3	364	48.6
Power (μW)	2.875	1.453	360	0.724	24	0.026	25.41	182	17
Area (mm^2)	0.01		0.022	0.019	–	–	0.02	0.005	
IFOM$_S$	236	289	245	87	73	94	165	31	22
IFOM$_L$	55	91	115	71	28	24	154	35	34
FOM$_{A_V}$	34059	45438	13368	16240	10998	12204	13575	2879	2703
IFOM$_T$	378$^{\triangle}$	661$^{\triangle}$	204	175	87	86	189	37	38

Note: $\otimes$: measurement results; S: single ended ; D: differential ; –: not reported; $\triangle$: threshold voltage of nMOS and pMOS transistor: V_{THn} =0.48-V and V_{THp} = 0.32-V.

$\text{IFOM}_S = \text{UGF} \times \frac{C_L}{\text{I}_\text{T}} \left[\frac{\text{MHz}\times\text{pF}}{\mu A}\right] \times 100$; $\text{IFOM}_L = \text{Slew rate} \times \frac{C_L}{\text{I}_\text{T}} \left[\frac{V}{\mu s} \times \frac{\text{pF}}{\mu A}\right] \times 100$;

$\text{FOM}_{A_V} = \text{DC}-\text{gain} \times \frac{\text{UGF}\times\text{C}_\text{L}}{\text{Power}} \left[\frac{\text{dB}\times\text{MHz}\times\text{pF}}{\mu W}\right] \times 100$; $\text{IFOM}_T = \frac{V_{THn}+|V_{THp}|}{V_{DD}} \times \frac{UGF\times C_L}{\text{I}_\text{T}} \left[\frac{\text{MHz}\times\text{pF}}{\mu A}\right] \times 100$

From Table 4.6, it is clear that the proposed OTA exhibits better performance compared to the works presented in [24, 28, 30, 36, 38, 40]. The proposed design gives a highest FOM for small and large-signal parameters such as UGF and slew rate under low-voltage environment. It is also clear from Table 4.6, that the proposed design provides a minimum of twice small-signal efficiency (FOM_S) compared to the best existing works. Moreover, the large-signal performance of the proposed design is more efficient compared to the designs with supply voltage of 0.5-V or less [24, 30, 36, 38]. It can be seen from Table 4.6, the FOM_{A_V} of the proposed OTAs is twice that of the best existing OTA. The $IFOM_T$ is calculated by incorporating technology parameter (i.e.,V_{TH} of CMOS) and supply voltage. The $IFOM_T$ of the proposed design is two to three times more compared to existing designs. The FOM's of the proposed OTA with low-supply voltage of 0.35-V is 1.5 times more than that of 0.5-V supply. In summary, the proposed topology exhibits better performance at supply voltage of 0.35-V.

4.6 Summary

In this chapter, a high gain pseudo-differential bulk-driven OTA has been proposed. The proposed OTA is capable of operating under low supply voltages and hence well suited for sub-nanometer CMOS technologies. A partial positive feedback technique is employed to improve the gain of input stage. The cross forward stage at the output stage improved the driving capability and over all DC-gain of OTA. To study the robustness of the OTA, simulations were carried out with different PVT conditions. The total power consumption was approximately 1.45 μW and 2.9 μW for the supply voltage of 0.35-V and 0.5-V, respectively. It is found that the proposed OTA can drive upto load capacitance of 50 pF without any stability issues and offers the unity gain frequency of 617 kHz and phase margin of 55°. In summary, the proposed OTA provides high DC-gain and shows better FOM as compared to existing OTAs.

5

An Ultra-Low-Voltage Bulk-Driven OTA for Low-Frequency Applications

Contents

5.1 Introduction

At very low-voltage conditions fully differential OTA is preferred over single-ended for better output signal swing. In general, the differential input stage is biased using a tail current source which intrinsically attenuates the common-mode signals. At very lower supply voltages the tail current source can be removed without much degradation in the circuit performance, such amplifier normally referred as pseudo-differential amplifier is considered in this work. One of the challenges in designing of such circuits is obtaining high DC-gain and high common-mode rejection ratio (CMRR) with low supply voltage.

A new ultra-low-voltage, ultra-low-power pseudo-differential bulk-driven OTA is presented in this chapter. The proposed design employs an auxiliary circuit at input stage to improve the effective transconductance of bulk-driven OTA. The enhanced transconductance leads to improvement in DC-gain and GBW of OTA. To further enhance the gain, a PPF technique is employed. In addition, a Class-AB output stage is designed through a cross forward stage that improves current efficiency and gain of the amplifier. The PPF and cross forward stage also improves the CMRR of pseudo-differential OTA. This OTA can be used as a tunable transconductance amplifier by varying bias voltage of auxiliary circuit. Further, a tunable second order $G_m - C$ low-pass filter is also designed using the proposed OTA.

5.2 Pseudo-Differential Bulk-Driven OTA Circuit Design

In this Section, the sub-blocks of conventional and proposed bulk-driven OTA are explained. The operating principle of auxiliary amplifier and cross-forward stage is also described in this section. Moreover, in this section, the performance of the proposed design which uses auxiliary amplifier and cross-forward stage is compared with the conventional design.

5.2.1 Bulk-driven pseudo-differential input stage

The circuit diagram of conventional bulk-driven pseudo-differential input stage OTA reported in [62] is shown in Fig. 5.1 (a). The two inputs V_{iP} and V_{iN} are connected to the bulk-terminal of pMOS transistors $M_{1A,B}$ and $M_{2A,B}$, and their g_{mb} contributes the input transconductance. For an input common-mode voltage of $V_{DD}/2$ (0.15 V), the resulting small body-source forward bias lowers the V_{th} which causes a further increase in the inversion level. The diode connected transistors M_{2A} and

M_{2B} sets the common-mode voltages (V_{1p}, V_{1n}) to $V_{DD}/2$ and is used as bias voltage for the next stage (i.e., output stage). However, the diode connected configuration decreases the gain of input stage. In order to overcome this, additional transistors M_{1A} and M_{1B} are connected in parallel to M_{2A} and M_{2B}, respectively, as shown in Fig. 5.1 (a). Note that the gate terminals of M_{1A} and M_{1B} are connected in cross-couple manner. The partial positive feedback created due to cross-coupled connection of M_{1A} and M_{1B} cancels the gate transconductance of M_{2A} and M_{2B}, respectively, which in turn increases DC gain [62]. Moreover, the cross-coupled configuration eliminates the need of CMFB circuit at input stage.

Let the bulk-transconductance, gate transconductance and drain-source conductance of $M_{N\in\{1,2,...,N\}}$ are represented by g_{mbN}, g_{mN} and g_{dsN}, respectively. The differential DC gain of conventional input stage design in Fig. 5.1 (a) is given by

$$A_{1,Conv} = \left(\frac{g_{mb1} + g_{mb2}}{g_{ds1} + g_{ds2} + g_{ds3} + g_{m2} - g_{m1}}\right) \tag{5.1}$$

In conventional design (i.e., Fig. 5.1 (a)), the input transistors M_{1A} and M_{1B} are loaded by the nMOS transistors M_{3A} and M_{3B} which act as current source. Hence, the effective transconductance is equal to $g_{mb1} + g_{mb2}$ only, this results in low DC gain and low UGF. However, in the proposed design, the M_{3A} and M_{3B} acts as active element due to inclusion of an auxiliary circuit. The modified bulk-driven pseudo-differential input stage with auxiliary stage is shown in Fig. 5.1 (b). The auxiliary stage consists of bulk-driven common source amplifier with diode-connected load (M_{5A} and M_{5B}). The inputs V_{iP} and V_{iN} are cross connected to bulk terminal of M_{4A} and M_{4B}, respectively, as shown in Fig. 5.1 (b). The output of auxiliary stage drives the gate of M_{3A} and M_{3B} and hence the effective transconductance of input stage increases. The proposed input-stage design provides higher DC gain and transconductance as compared with the conventional design.

As the proposed circuit is perfectly symmetrical, using the small-signal equivalent circuit of the input stage, the effective transconductance (g_{mbI}) of bulk-driven input stage with auxiliary circuit can be approximated as follows

$$g_{mbI} = g_{mb1} + g_{mb2} + g_{m3}\frac{g_{mb4}}{g_{m5} + g_{ds5} + g_{ds4}} \approx 4.g_{mb1} \tag{5.2}$$

In Fig. 5.1 (b), the current flowing through $M_{1A,B}$, $M_{2A,B}$ and $M_{4A,B}$ are equal i.e., $g_{mb1} = g_{mb2} = g_{mb4}$ and the current flows through $M_{3A,B}$ is twice that of $M_{5A,B}$, which implies $g_{m3} = 2.g_{m5}$.

The effective transconductance of input stage with auxiliary amplifier is approximately twice when compared to the conventional input stage design shown in Fig. 5.1 (a). The differential gain of the proposed bulk-driven input stage is given by

$$A_{1,Prop} = \frac{g_{mbI}}{g_{ds1} + g_{ds2} + g_{ds3} + g_{m2} - g_{m1}} \tag{5.3}$$

where, g_{mbI} is the effective transconductance of bulk-driven input stage with auxiliary amplifier from (5.2).

The effective transconductance of the proposed OTA is higher than that of the conventional OTA design. Hence, there is a improvement in the overall DC-gain of the proposed OTA.

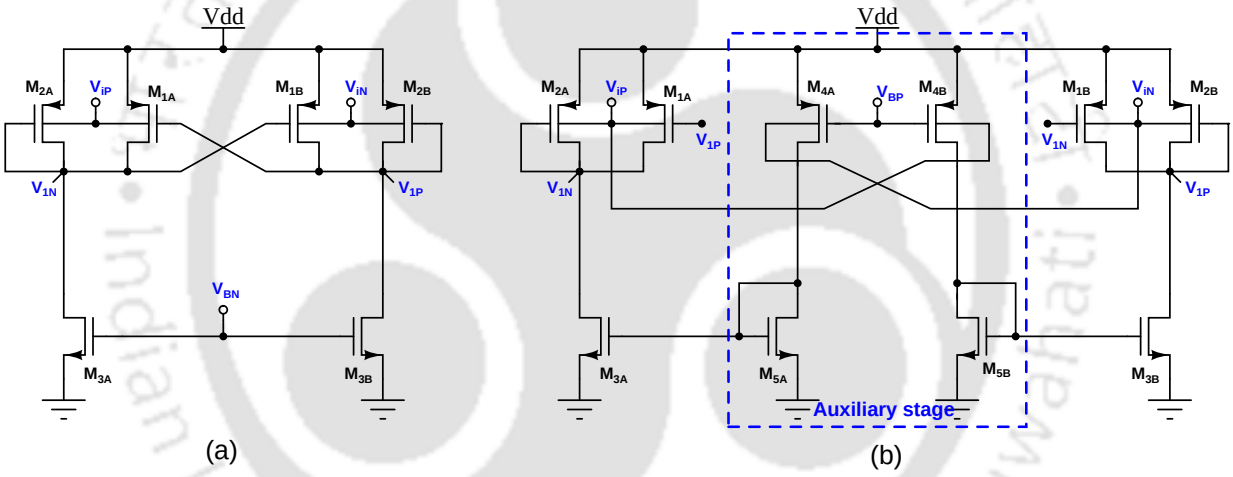


Figure 5.1: Bulk-driven pseudo-differential input stage (a) without auxiliary stage (b) with auxiliary stage.

The common-mode gain of conventional and proposed input stage design is given in (5.4) and (5.5), respectively.

$$A_{1,CM,Conv} = \left(\frac{g_{mb1} + g_{mb2}}{g_{ds1} + g_{ds2} + g_{ds3} + g_{m2} + g_{m1}}\right) \tag{5.4}$$

$$A_{1,CM,Prop} = \left(\frac{g_{mbIC}}{g_{ds1} + g_{ds2} + g_{ds3} + g_{m2} + g_{m1}}\right) \tag{5.5}$$

where, $g_{mbIC} = g_{mb1} + g_{mb2} - g_{m3}\left(\frac{g_{mb4}}{g_{m5}+g_{ds4}+g_{ds5}}\right)$

It is clear from (5.4) and (5.5) that the proposed design is less sensitive to input common-mode

variation as compared with the conventional design.

5.2.2 Differential output stage

As discussed in Sub-Section 5.2.1, the bulk-driven input stage shown in Fig. 5.1 (a) provides a small gain due to low bulk-transconductance g_{mb}. In order to improve the overall gain of OTA, a gate-driven second stage (i.e., output stage) is cascaded to the bulk-driven input stage. The conventional differential output stage based on common source amplifier with a current source load is shown in Fig. 5.2 (a). The gate-driven common source amplifier acts as a second stage of OTA which provides high gain as compared to first stage (i.e., input-stage). The second gain stage is implemented using $M_{4A,B} - M_{5A,B}$ transistors. Miller compensation technique employed for frequency stability of OTA [10] and a compensation capacitor is placed in between gate-source of $M_{4A,B}$ as shown in Fig. 5.2 (a). The DC gain of conventional output stage is given by

$$A_{2,Conv} = \frac{g_{m4}}{g_{ds4} + g_{ds5}} \tag{5.6}$$

However, OTA with conventional input and output stages provides low DC gain and low UGF. Even after cascading the two gains stages, the DC gain is still very low. Hence, it is necessary to increase the gain of output stage further. The proposed differential output stage with an additional cross-forward stage is shown in Fig. 5.2 (b).

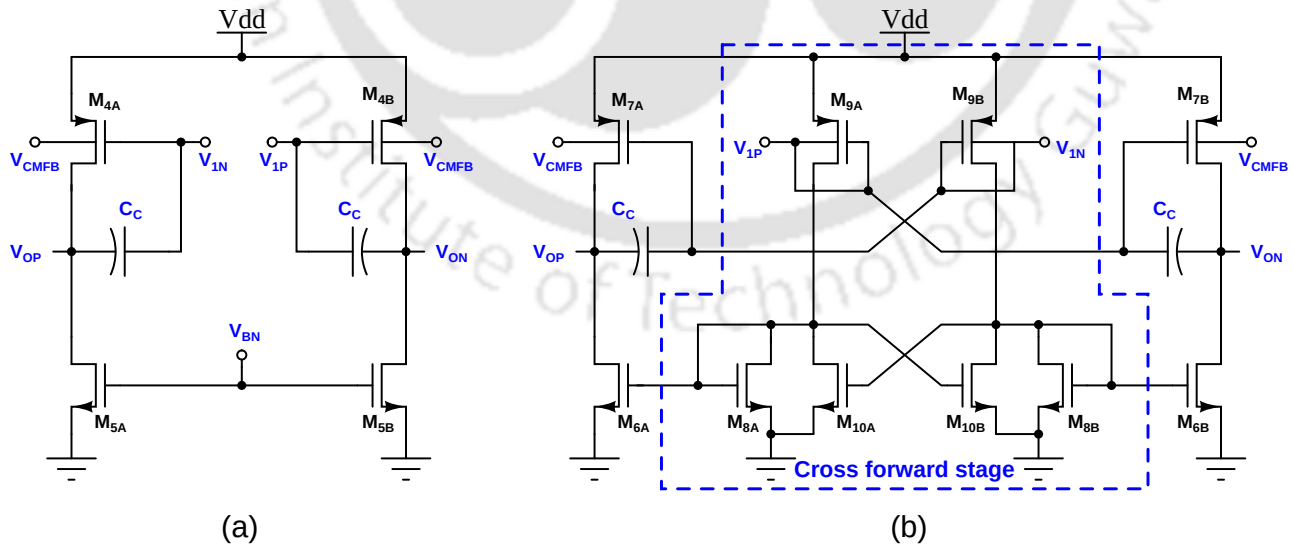


Figure 5.2: Differential output stage (a) conventional without cross-forward stage (b) proposed with cross-forward stage (CMFB circuit is not shown).

The proposed output stage of OTA operates as Class-AB amplifier without degrading the linearity.

In order to achieve an adequate gain without reducing the output swing, a gate-input stage $M_{6A,B} - M_{10A,B}$ is cascaded to the input stage. As shown in Fig. 5.2, output of first stage (V_{1n} and V_{1p}) is amplified along the two paths. One path reaches the positive output through M_{7B} and the other through M_{9B}, M_{8B} and M_{6B}. In a similar manner, the negative output is provided by M_{9A}, M_{8A}, M_{6A} and M_{7A}. The Class-AB structure of output stage reduces the common-mode gain because common signal in one path cancels the signal in another path due to 180° phase difference.

To enhance the transconductance of output stage, the output of first stage is connected to $M_{9A,B}$ and $M_{7A,B}$. The signals with opposite phase are connected in a cross-coupled manner. The negative (positive) output of first stage is connected to M_{7A} and M_{9B} (M_{7B} and M_{9A}). The intermediate stage comprising of $M_{9A,B} - M_{10A,B}$ forms a common-source amplifier with cross-coupled current shunt loads as shown in Fig. 5.2 (b). The low-frequency gain of cross forward stage is given by

$$K = \frac{g_{m9} + g_{mb9}}{g_{ds9} + g_{ds8} + g_{ds10} + g_{m8} - g_{m10}} \tag{5.7}$$

The output stage formed by $M_{7A,B}$ and $M_{6A,B}$, provides Class-AB operation. The output of first stage and cross forward stage is connected to the gates of $M_{7A,B}$ and $M_{6A,B}$, respectively. The additional DC gain due to the output stage alone is given by

$$A_{2,Prop} = \frac{g_{m7} + K.g_{m6}}{g_{ds6} + g_{ds7}} \tag{5.8}$$

The transconductance of output stage depends on the gain of intermediate stage (i.e., cross-forward stage) and current in output stage. It is clear from (5.8) and (5.6) that the effective output transconductance of the proposed design is K times more as compared to conventional Class-A output stage. The proposed OTA achieves a large transconductance at output stage with a small amount of additional current through cross forward stage. Moreover, the pole due to intermediate stage appears at higher frequencies which is higher than unity gain frequency and it show less effect on stability of OTA.

5.2.3 CMFB stage

A CMFB circuit aids the differential OTAs to prevent the output voltages from saturating to one of the power rails when the input common-mode voltage changes. This maintains both the output node voltages at same desired reference voltage (V_{REF}), which is normally half of the supply voltage

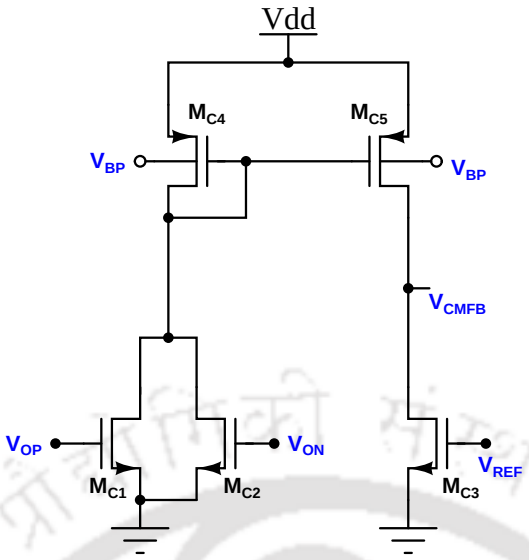


Figure 5.3: Schematic of CMFB circuit for conventional and proposed output stages in Fig. 5.2.

($V_{DD}/2$). The CMFB stage is realized by $M_{C1} - M_{C5}$ as shown in Fig. 5.3 and is employed in both the conventional and proposed designs. Here, the output node voltage signals (V_{OP} and V_{ON}) are connected to the gate terminals of M_{C1} and M_{C2}, and the difference of these voltages is converted into a current using transistor M_{C5}. This current is compared with the constant current which is generated by M_{C3}. The gate of M_{C3} is biased with a reference voltage and generates constant current. The difference between these two currents change the common-mode feedback voltage (V_{CMFB}) and is fed back to the bulk terminal of output stage transistors (i.e., M_{7A} and M_{7B}). The CMFB circuit acts as a voltage buffer for differential input signal. It sets the desired output node voltage by adjusting the bulk voltage of M_{7A} and M_{7B}. The DC gain of CMFB circuit with common-mode input signal is given by

$$A_{CMFB} \approx \left(\frac{g_{mc5} \times \frac{g_{mc4}}{g_{mc1}+g_{mc2}}}{g_{dsc3} + g_{dsc5}} \right) \tag{5.9}$$

5.3 Analysis of the Conventional and Proposed Bulk-driven OTAs

The complete schematic diagrams of conventional and proposed bulk-driven OTAs are shown in Fig. 5.4 and 5.5, respectively. The performance parameters such as differential gain, common-mode rejection ratio (CMRR), input-referred noise (IRN) and power supply rejection ratio (PSRR) are analyzed and analytical expressions are derived for both designs.

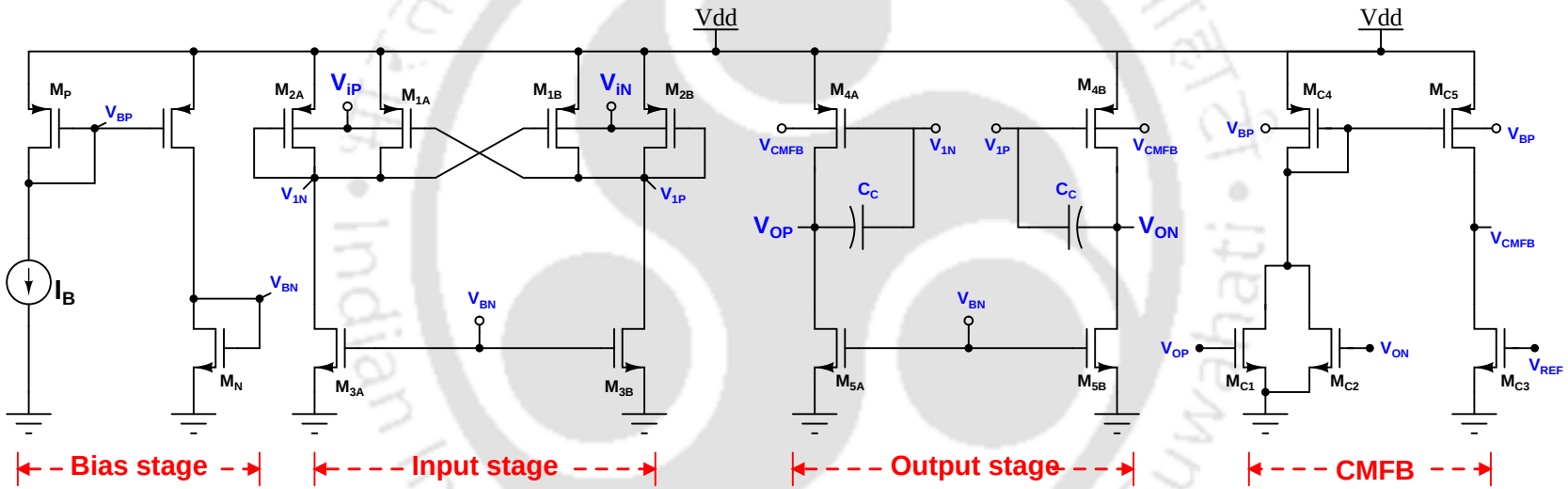


Figure 5.4: Schematic of the conventional pseudo-differential bulk-driven OTA.

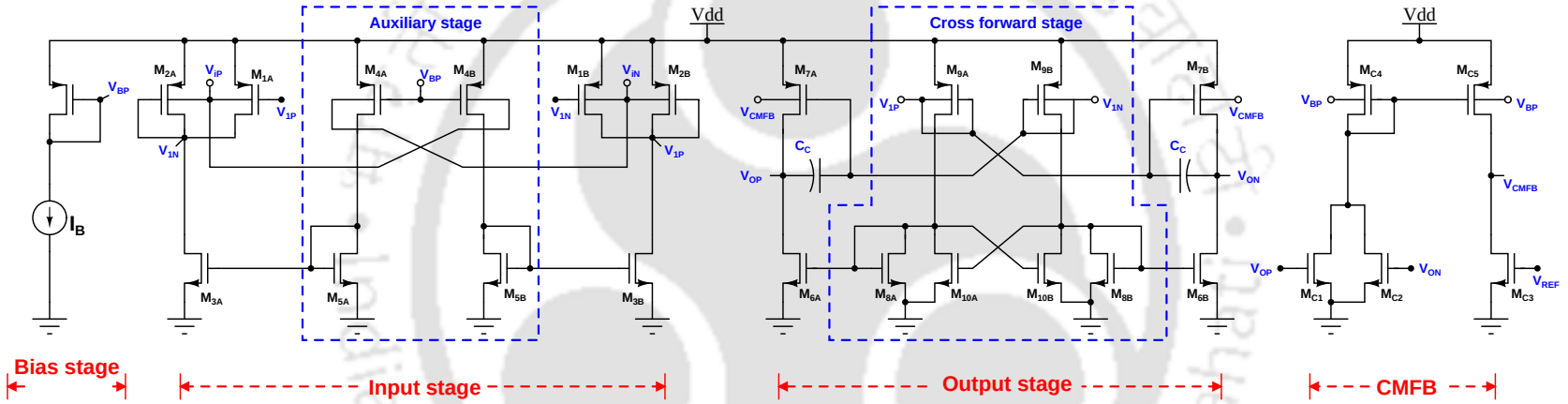


Figure 5.5: Schematic of the proposed pseudo-differential bulk-driven OTA.

5.3.1 Analysis of Differential-Mode Configuration

In differential-mode, the OTA acts as an amplifier and improves the strength of the differential input signal. In conventional OTA design, the gate inputs of M_{1A} and M_{1B} form a partial positive feedback which adds a negative resistance to the output and boosts the differential DC gain.

To further increase the gain of OTA, a gate-driven circuit used as the second stage. The differential-mode gain from input to output node $A_{DM,Conv}$ of conventional OTA shown in Fig. 5.4) is given by

$$A_{DM,Conv} = \left(\frac{g_{mb1} + g_{mb2}}{g_{ds1} + g_{ds2} + g_{ds3} + g_{m2} - g_{m1}}\right)\left(\frac{g_{m4}}{g_{ds4} + g_{ds5}}\right) \tag{5.10}$$

The conventional OTA provides low gain because of low input g_{mb} and major part of DC gain is contributed by the second stage which is evident from (5.10). The conventional design provides a low DC gain which is of the order of less than 40 dB.

In order to improve the transconductance and gain, the proposed design employed an additional circuitry comprises of auxiliary stage and CF stage. The auxiliary circuit improves the effective transconductance of input stage and CF stage enhances the gain of output stage which is evident from (5.8). Differential-mode gain $A_{DM,Prop}$ of the proposed OTA shown in Fig. 5.5 is given by

$$A_{DM,Prop} = \left(\frac{g_{mbI}}{g_{ds1} + g_{ds2} + g_{ds3} + g_{m2} - g_{m1}}\right)\left(\frac{g_{mII}}{g_{ds6} + g_{ds7}}\right) \tag{5.11}$$

where $g_{mbI} = g_{mb1} + g_{mb2} + g_{m3}\left(\frac{g_{mb4}}{g_{m5}+g_{ds4}+g_{ds5}}\right)$, $g_{mII} = g_{m7} + g_{m6}\left(\frac{g_{m9}+g_{mb9}}{g_{ds8}+g_{ds9}+g_{ds10}+g_{m8}-g_{m10}}\right)$

It is clear from (5.10) and (5.11) that the proposed OTA offers higher gain as compared to conventional design. The CF stage enhances the overall DC gain of the proposed OTA and auxiliary circuit at input stage improves the effective transconductance.

5.3.2 Analysis of Common-Mode Configuration

In order to understand the effect of common-mode signal on the output nodes, the common-mode gain (A_{CM}) is computed. The CMRR of OTA is defined as the ratio of A_{DM} to A_{CM}. An ideal differential amplifier would have infinite CMRR. In bulk-driven circuits, as g_{mb} being smaller than g_m the common-mode signal is strongly suppressed. For common mode input signal, the cross-coupled configuration provides negative feedback and hence results in a lower output resistance and smaller A_{CM}. The common-mode gain of the conventional bulk-driven OTA as shown in Fig. 5.4 is given by

$$A_{CM,Conv} = \left(\frac{g_{mb1} + g_{mb2}}{g_{ds1} + g_{ds2} + g_{ds3} + g_{m2} + g_{m1}}\right)\left(\frac{g_{m4}}{g_{mb4} \times A_{CMFB} + g_{ds4} + g_{ds5}}\right) \tag{5.12}$$

It is clear from (5.12) that the common source amplifier at the second stage of the conventional design results a large common mode gain. For common-mode signal, the auxiliary circuit employed in the proposed design reduces effective transconductance g_{mIC} and thereby decreases the common-mode gain. In addition, the CF stage at the output stage of the proposed design reduces the output stage transconductance g_{mIIC} which further reduces the common-mode gain. Hence, the overall common-mode gain $A_{CM,Prop}$ of the proposed OTA is very small as compared to conventional design. The expression for the common-mode gain of the proposed design is given by

$$A_{CM,Prop} = \left(\frac{g_{mbIC}}{g_{ds1} + g_{ds2} + g_{ds3} + g_{m2} + g_{m1}}\right)\left(\frac{g_{mIIC}}{g_{mb6} \times A_{CMFB} + g_{ds7} + g_{ds9}}\right) \tag{5.13}$$

where, $g_{mbIC} = g_{mb1} + g_{mb2} - g_{m3}\left(\frac{g_{mb4}}{g_{m5}+g_{ds4}+g_{ds5}}\right)$, $g_{mIIC} = g_{m7} - g_{m6}\left(\frac{g_{m9}+g_{mb9}}{g_{ds8}+g_{ds9}+g_{ds10}+g_{m8}+g_{m10}}\right)$, CMFB circuit gain: $A_{CMFB} = \left(\frac{g_{mc5} \times \frac{g_{mc4}}{g_{mc1}+g_{mc2}}}{g_{dsc3}+g_{dsc5}}\right)$

5.3.3 Noise analysis

The input referred noise performance of OTA mainly depends on the effective transconductance of input stage and it is related to current flow though input devices. Flicker-noise which depends on the geometry of the input devices is more dominant compared to other noises at lower frequencies. At higher frequencies, the thermal noise becomes dominant and it can be reduced by enhancing effective transconductance of input stage. The input-referred noise of bulk-driven circuits is intrinsically large due to smaller value of body transconductance g_{mb} compared to the gate transconductance g_m. The total input referred noise ($\overline{V_{n,in}^2}$) is combination of flicker noise ($V_{n,1/f}^2$) and thermal noise ($V_{n,th}^2$).

The expression of the total input referred noise for the conventional bulk-driven OTA can be expressed as

$$\overline{V_{n,in,\text{Conv}}^2} = \frac{2}{C_{OX} f (g_{mb1} + g_{mb2})^2}\left[\frac{K_{fn} g_{m1}^2}{W_1 L_1} + \frac{K_{fp} g_{m2}^2}{W_2 L_2} + \frac{K_{fp} g_{m3}^2}{W_3 L_3}\right] + \frac{8 K_B T}{3\,(g_{mb1} + g_{mb2})}\left[\frac{g_{m1} + g_{m2} + g_{m3}}{g_{mb1} + g_{mb2}}\right] \tag{5.14}$$

Similarly, the input referred noise of the proposed bulk-driven OTA in Fig. 5.5 can be written as

$$\overline{V^2_{n,in,Prop}} = \frac{2}{C_{OX} f g^2_{mbI}} \left[\frac{K_{fn} g^2_{m1}}{W_1 L_1} + \frac{K_{fp} g^2_{m2}}{W_2 L_2} + \frac{K_{fp} g^2_{m3}}{W_3 L_3} \right] + \frac{8 K_B T}{3 g_{mbI}} \left[\frac{g_{m1} + g_{m2} + g_{m3}}{g_{mbI}} \right] \tag{5.15}$$

where, K_{fn}, K_{fp} flicker noise coefficients for nMOS and pMOS transistors, respectively, g_{mbI} represents the effective transconductance of the proposed input stage as shown in Fig. 5.1 (b). All the other symbols have their usual meanings.

It is clear from (5.14) and (5.15) that the input referred noise of the proposed bulk-driven OTA is less compared to the conventional design because of enhanced transconductance.

5.3.4 PSRR analysis

Power supply rejection ratio (PSRR) is the capability of OTA to suppress the power supply fluctuations at output signal. It is given by the ratio of the change in supply voltage to the equivalent output voltage it produces. PSRR is defined as the gain from the input to the output divided by the gain from the supply to the output [129] and it is given by

$$PSRR = \frac{A_{DM}}{A_{PSR}} \tag{5.16}$$

The power supply rejection gain $A_{PSR,Conv}$ of the conventional circuit with respect to power supply variations is given by

$$A_{PSR,Conv} \approx \frac{g_{m7} + g_{mb7} - K_1 g_{m7}}{g_{mb7} \times A_{CMFB} + g_{ds6} + g_{ds7}} \tag{5.17}$$

where, PSR gain of input stage $K_1 \approx \frac{g_{m1}+g_{mb1}+g_{m2}+g_{mb2}}{g_{m1}+g_{mb1}+g_{m2}+g_{mb2}+g_{ds1}+g_{ds2}+g_{ds3}}$ and PSR gain of CMFB circuit $A_{CMFB} = \frac{g_{mc5} \times \frac{g_{mc4}}{g_{mc1}+g_{mc2}}}{g_{dsc3}+g_{dsc5}}$.

In the proposed design, the cross-forward configuration in output stage offers a negative transconductance, which results in the decrease of power supply gain, thus giving a high PSRR. Hence, the proposed bulk-driven OTA is also insensitive to supply variations. The PSR gain $A_{PSR,Prop}$ of the proposed OTA is given by

$$A_{PSR,Prop} \approx \frac{g_{m7} + g_{mb7} - K_F g_{m6} - K_1 g_{m7}}{g_{mb7} \times A_{CMFB} + g_{ds6} + g_{ds7}} \tag{5.18}$$

Where, PSR gain of auxiliary stage $K_{AX} \approx \frac{g_{m4}+g_{mb4}}{g_{m5}+g_{ds4}+g_{ds5}}$,

PSR gain of input stage: $K_1 \approx \frac{g_{m1}+g_{mb1}+g_{m2}+g_{mb2}-g_{m3} \times K_{AX}}{g_{m1}+g_{mb1}+g_{m2}+g_{mb2}+g_{ds1}+g_{ds2}+g_{ds3}}$

PSR gain of cross forward stage: $K_F \approx (1 - K_1)\left(\frac{g_{m9}+g_{mb9}}{g_{m8}+g_{m10}+g_{ds8}+g_{ds8}+g_{ds10}}\right)$

PSR gain of CMFB circuit $A_{CMFB} = \frac{g_{mc5} \times \frac{g_{mc4}}{g_{mc1}+g_{mc2}}}{g_{dsc3}+g_{dsc5}}$

5.3.5 Frequency Compensation

In the multi-stage design, a simple Miller-compensation technique is employed for stability [10]. This can be achieved by placing a compensation capacitor (C_C) between input stage and output node (i.e., high impedance nodes). This separates the poles and locates them at large distance to improve the phase margin [10]. The unity gain frequency (f_u) of Miller compensated OTA shown in Fig. 5.4 and 5.5 is given given by

$$f_{u,Conv} \approx \frac{g_{mb1} + g_{mb2}}{2\pi C_C} \tag{5.19}$$

$$f_{u,Prop} \approx \frac{g_{mbI}}{2\pi C_C} \tag{5.20}$$

In (5.20), g_{mbI} represents the effective transconductance of the proposed OTA expressed in (5.2). The proposed OTA provides higher UGF as compared to conventional design because of its enhanced transconductance.

5.4 Simulation Results of Pseudo-Differential Conventional and Proposed OTA

The conventional and proposed bulk-driven OTAs are designed and post-layout simulations performed using UMC 65-nm CMOS process. The input, output and intermediate common-mode voltage levels of the amplifier are equal to mid of the supply voltage (i.e., $V_{DD}/2$). Both OTAs operate with supply voltage of 0.3-V, and the total quiescent current of conventional and proposed designs are 110 nA and 170 nA, respectively.

In order to improve the performance parameters such DC gain, UGF, slew rate and CMRR, the proposed OTA requires an additional quiescent current of 60 nA (54%). In both OTAs, on-chip compensation capacitance C_C of 0.35 pF is employed for stability. The channel lengths of nMOS and pMOS devices are 2 μm and 1 μm, respectively. In the following, post-layout simulation results are presented for the conventional and proposed design.

Simulated performance parameters of conventional and proposed OTA are summarized in Table.

5.1. It can be observed from Table. 5.1 that the proposed OTA shows better performance as compared to conventional except phase margin. In post-layout simulation, the phase margin of the proposed OTA is decreased due to the parasitic effects of devices and metal lines.

Table 5.1: Comparison of simulation results of conventional and proposed OTA design.

Parameter	Conventional	Proposed
Power supply (V)	0.3	0.3
Current dissipation (nA)	110	170
Load capacitance (pF)	5	5
DC gain (dB)	29	60.5
UGF (kHz)	15	70.5
Phase margin (°)	62	53
Slew rate (+/−) (mV/μs)	7.3/7.28	25.5/25.7
IRN ($\mu V/\sqrt{Hz}$) at 1 kHz	3.42	2.82
CMRR (dB) at 1 Hz	53.2	126
PSRR$^+$ (dB) at 1 Hz	59	90
Settling time (t_s) (+/−) (μs)	69.7/70	48.2/46.2

Fig. 6.9 illustrates the magnitude and phase frequency response of the conventional and proposed OTAs for a load capacitance (C_L) of 5 pF. The proposed OTA provides a DC gain of 60.5 dB which is 37 times higher than that of conventional OTA. It also clear from Fig. 6.9 that the proposed design shows 4 times improvement in UGF with a small reduction in phase margin compared to the traditional design. The UGF of the conventional and proposed designs are 15 kHz and 70 kHz, respectively, which indeed demonstrates the enhanced transconductance of the proposed technique.

The common-mode and power supply rejection ratio responses for the conventional and proposed bulk-driven OTA are shown in Fig. 5.7. It is clear from Fig. 5.7 that the proposed OTA provides high CMRR ($\approx$ 126 dB), due to the PPF configuration at the input and output stage of OTA. Since, PPF acts as negative feedback for common-mode signal and hence results in low common-mode gain. In addition, the CMFB circuit acts as an amplifier for common-mode signal which further improves the CMRR. Moreover, the auxiliary stage in the proposed design minimizes the common-mode signal variation which is evident from equation (5.5).

Fig. 5.8 illustrates the stability simulation results of CMFB circuit. In conventional and proposed designs the CMFB circuit remain same and hence the CMFB stability simulation results are same for both OTAs. It can be observed from Fig. 5.8 that the CMFB circuit DC gain is 30 dB, UGF is 307.1 kHz and phase margin is 61°.

Fig. 5.9 illustrates the input-referred noise (IRN) power spectral density response of both OTAs.

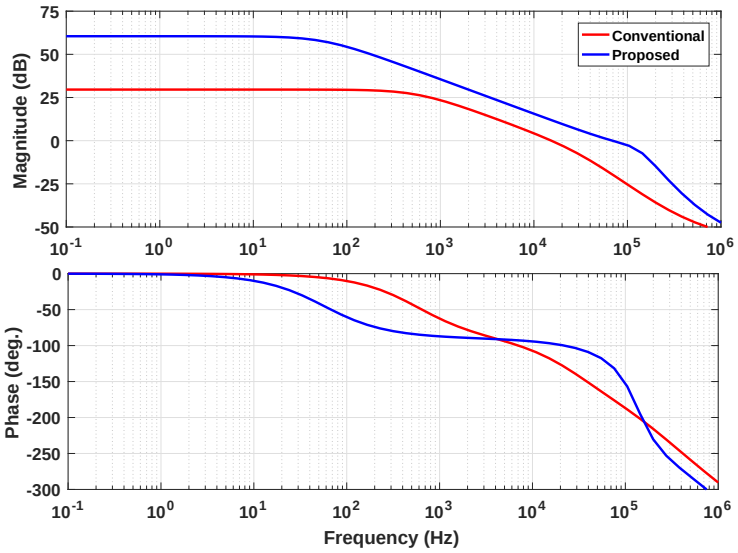


Figure 5.6: Simulated magnitude and phase response for conventional and proposed Miller-compensated OTA approaches.

Note that the thermal noise of the traditional and proposed bulk-driven OTAs at 1 kHz are 3.42 $\mu V/\sqrt{Hz}$ and 2.82 $\mu V/\sqrt{Hz}$, respectively. The proposed bulk-driven OTA shows a small noise power spectrum density compared to the traditional OTA because of higher effective transconductance as demonstrated by (5.14) and (5.15).

The large-signal response for the OTAs are observed in unity gain feedback mode. Simulation results of unity gain amplifiers for a 0.3-V_{p-p} pulse input with load capacitance (C_L) of 5 pF are depicted in Fig. 5.10. The differential slew rate of the proposed amplifier at rising and falling edges are 25.5 mV/μs and 25.7 mV/μs, respectively, which is 3.5 times more than the slew rate of traditional OTA. The 1% rise settling times for the conventional and proposed designs are 69.7 μs and 48.2 μs, respectively. Note that the OTA with the auxiliary and cross-forward stage has the shortest settling time.

The DC input and output voltage characteristics of unity gain amplifier are shown in Fig. 5.11. This demonstrates that the enhanced gain of the proposed OTA can be achieved at a rail-to-rail input voltage range. It is evident from Fig. 5.11 that the proposed bulk-driven OTA gives a rail-to-rail output voltage for rail-to-rail input voltage and the error voltage ($V_{out} - V_{in}$) near supply rails is less than 5 mV. The conventional OTA gives high gain error because of its low voltage gain which is approximately 100 mV near supply rails.

The transient response of the proposed amplifier in unity gain configuration with sinusoidal input

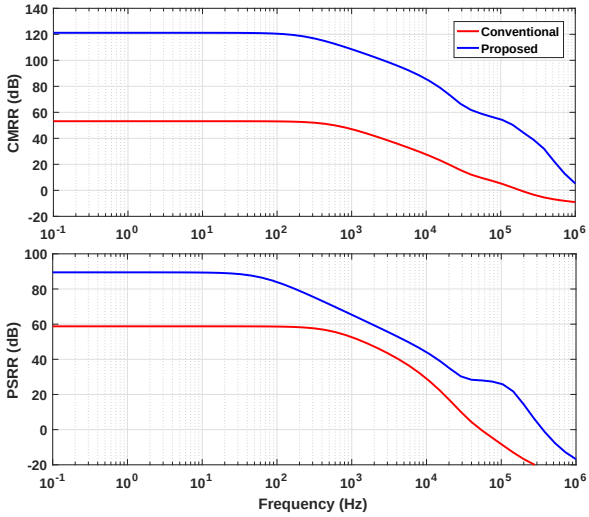


Figure 5.7: Common-mode and power supply rejection responses of conventional and proposed OTAs.

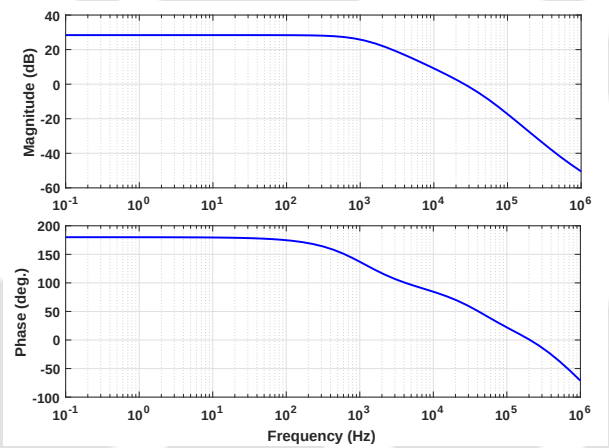


Figure 5.8: Simulation results of CMFB circuit stability.

is shown in Fig. 5.12. The proposed design gives rail-to-rail output for all common-mode voltages; the maximum output swing of OTA is 293 mV_{p-p} which is 97.6% of the total supply voltage.

The proposed bulk-driven OTA can be used as a tunable transconductance device, which is useful to design tunable active G_m-C filters. In weak inversion region, the transconductance of OTA is linearly varies with the bias current. This allows linear control over the range of cut-off frequency of the filter. The transconductance of OTA can be tuned by altering bias voltage (V_{BP}) of auxiliary input pMOS transistors (M_{3A} and M_{3B}) as shown in Fig. 5.5. The V_{BP} is generated using bias current I_B with a diode-connected pMOS device M_B. The change in bias current results in change in bias voltage V_{BP}. In pMOS, the increase in the current reduces the value of V_{BP}, which results

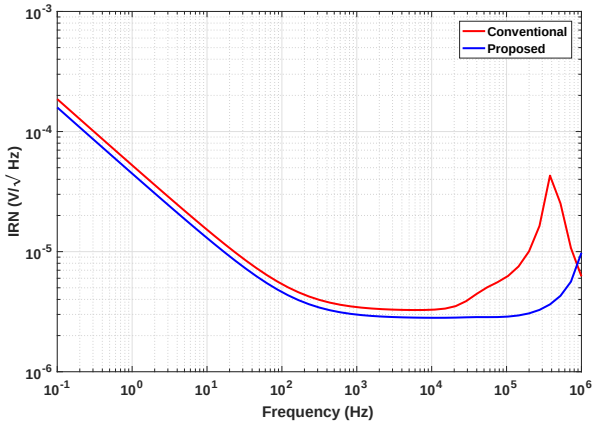


Figure 5.9: Simulated input-referred noise response of conventional and proposed OTAs.

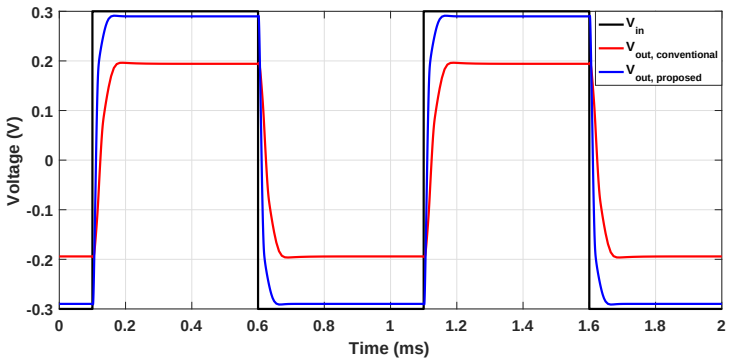


Figure 5.10: Simulated large-signal response of OTAs in unity gain configuration.

a larger current in input stage that lead to high transconductance. The internal node voltages in a circuit varies with I_B due to cross-coupled configuration. Moreover, the output node voltages (V_{OP} and V_{ON}) are maintained at mid of supply voltage using the CMFB circuit.

The open-loop frequency response of OTA for different values of I_B is shown in Fig. 5.13. The performance parameters of amplifier such as DC gain, UGF and phase margin with respect to I_B is shown in Fig. 5.14. By changing the bias current I_B from 1 nA to 200 nA, the effective transconductance of OTA varies approximately from 26 nA/V to 1250 nA/V.

In order to study the performance of the proposed OTA with respect to supply, temperature and process corners variation, simulations were performed for corners (SS,TT,FF,SNFP,FNSP) at temperature of 0 °C, 27 °C and 80 °C with supply variation of ± 10%. The PVT simulation results are summarized in Table 5.2, 5.3 and 5.4. It is clear from Table 5.2, 5.3 and 5.4 that the parameters of amplifier are less sensitive to temperature variation for different PVT corners. In most of the cases,

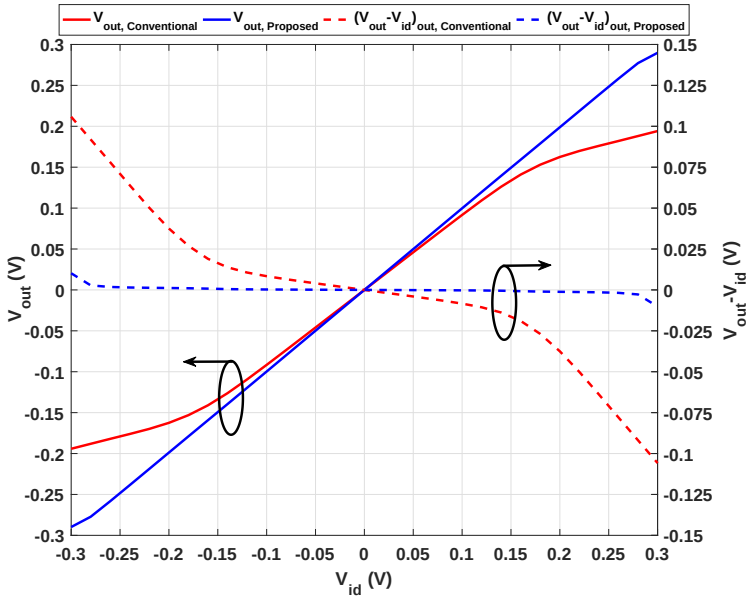


Figure 5.11: Simulated input common-mode range of both OTAs (conventional and proposed) in unity gain feedback mode.

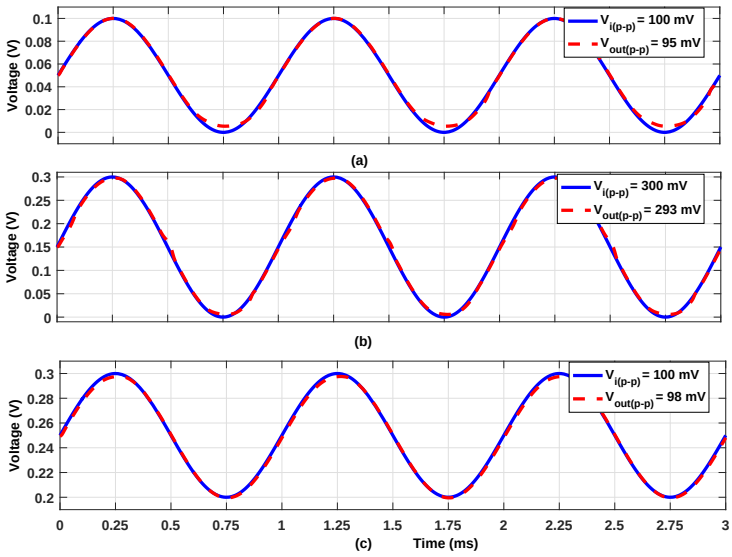


Figure 5.12: Transient response of proposed OTA in unity gain configuration with sinusoidal input: (a) V_{CM} = 25 mV, (b) V_{CM} = 150 mV and (c) V_{CM} = 250 mV

the DC gain is greater than 50 dB and the UGF is higher than 60 kHz with acceptable phase margin of more than 50°.

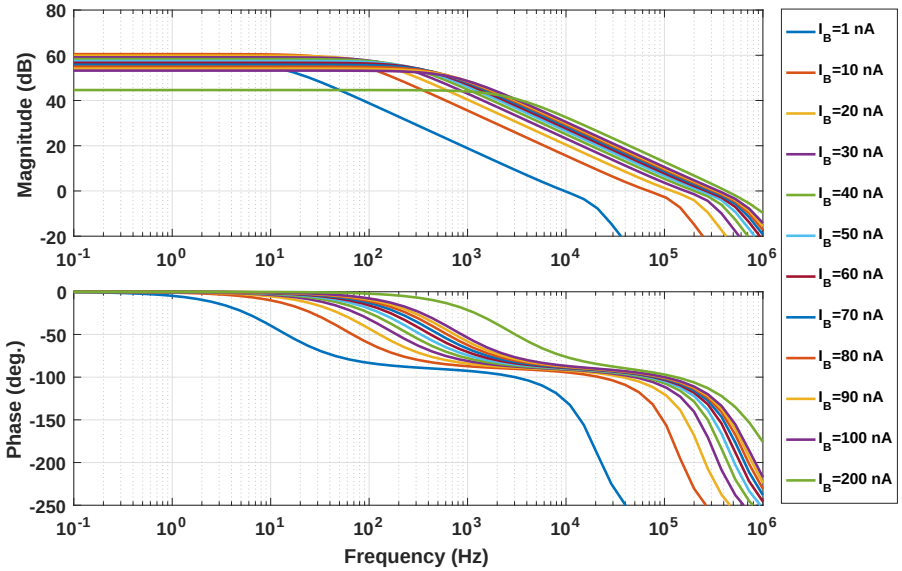


Figure 5.13: Simulated magnitude and phase response of the proposed OTA with different bias current I_B.

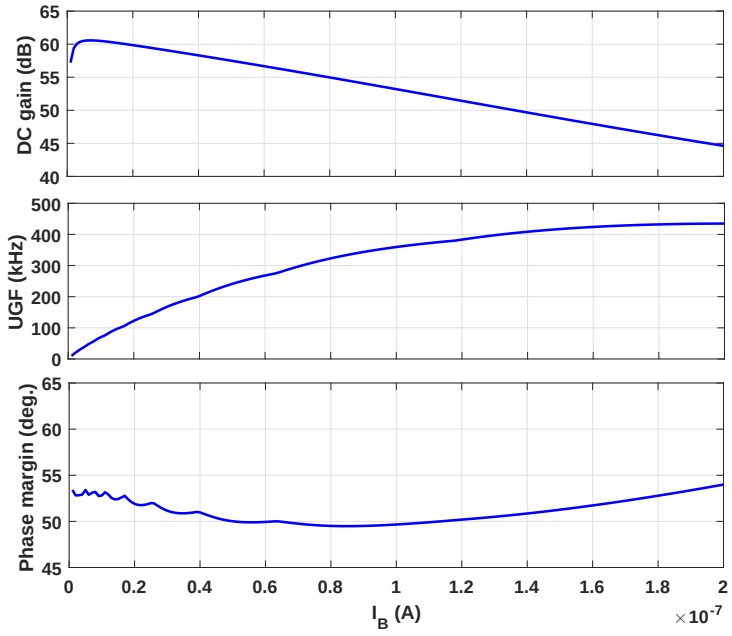


Figure 5.14: The proposed OTA DC gain, UGF and phase margin with respect to bias current I_B.

Table 5.2: Performance parameters of OTA over process and temperature variation (V_{DD} = 0.27 V)

Parameter	Corner @ Temp=0°C					Corner @ Temp=27°C					Corner @ Temp=80°C				
	SS	TT	FF	SNFP	FNSP	SS	TT	FF	SNFP	FNSP	SS	TT	FF	SNFP	FNSP
DC-gain (dB)	53	58.5	60	58	57.7	56	57.8	57	57.3	57.6	54	51.6	44	50.3	51
UGF (kHz)	41.65	51.5	61.4	51	51	46.8	52.8	61	53	51	50	52.4	52.1	52.5	51
Phase margin (°)	64.9	66	66.3	63	68.5	63.2	64.4	64.6	62	68.5	60	62.2	65.8	62	62
Slew rate (↑)(mV/μs)	13.27	17	20	16.7	16.7	16.3	18.9	21.6	18.6	16.7	19.3	20.9	22.4	20.1	21.6
Slew rate (↓)(mV/μs)	13.37	17.3	20.4	17	17	16.6	19.2	22	19	17	19.7	21.4	22.9	20.6	22
ts^+ (V/μs)	67.9	53.3	45.1	53.7	54.7	55.3	47.5	41.5	48.1	47.4	45.9	41.6	37.1	42.3	40.3
ts^- (V/μs)	67.2	52.5	44.3	52.6	53.5	54.7	46.8	40.7	47.2	46.6	44.7	40.8	36	41.8	39.4

Table 5.3: Performance parameters of OTA over process and temperature variation (V_{DD} = 0.3 V)

Parameter	Corner @ Temp=0°C					Corner @ Temp=27°C					Corner @ Temp=80°C				
	SS	**TT**	**FF**	**SNFP**	**FNSP**	**SS**	**TT**	**FF**	**SNFP**	**FNSP**	**SS**	**TT**	**FF**	**SNFP**	**FNSP**
DC-gain (dB)	60	62	62.3	61.7	62	59.2	60.5	58.6	59.4	59.5	56.4	53.7	46.3	52.7	53.5
UGF (kHz)	60	61.5	75	69	67	62.5	70.2	73.5	69.4	67.5	61.5	65	63.4	65.6	63.4
Phase margin (°)	55.4	55	55.7	60	65.5	55	53	54.6	51	56	51	55	57	51.5	52
Slew rate (↑)(mV/μs)	17.5	22.7	26	21.6	23	21.8	25.5	28.3	24.5	24.8	24.5	26.7	29	25.7	27.6
Slew rate (↓)(mV/μs)	17.7	23	26.7	22.1	23.5	22.5	25.7	28.4	24.7	25.4	25.1	27.4	30	26.6	30.3
ts^+ (V/μs)	65.8	53.9	46.2	54.7	54.1	55.8	49.4	43.3	49.8	49.2	47.4	43.6	39	44.8	42.6
ts^- (V/μs)	65.7	53.6	45.8	54.1	53.8	55.1	48.5	42.8	48.7	48.6	46.8	42.7	38.6	43.1	41.4

Table 5.4: Performance parameters of OTA over process and temperature variation (V_{DD} = 0.33 V)

Parameter	**Corner @ Temp=0°C**					**Corner @ Temp=27°C**					**Corner @ Temp=80°C**				
	SS	TT	FF	SNFP	FNSP	SS	TT	FF	SNFP	FNSP	SS	TT	FF	SNFP	FNSP
DC-gain (dB)	63	63.6	63.2	63.3	63.7	61.6	61.5	60	61	61.5	57.3	54.8	47.4	53.6.	54
UGF (kHz)	73.8	83.8	94	86.2	81.3	74	81.7	89.3	83.8	79.3	72.3	74.5	72.2	75	72.3
Phase margin (°)	59.2	58.3	57.6	54	61.8	56	56	57	52.3	59.3	52.3	55.6	61.4	55	67
Slew rate (↑)(mV/μs)	20.3	28.2	31.7	25	28.9	26.5	30	33.1	29	30.5	29.4	31.6	34.8	30.3	32.8
Slew rate (↓)(mV/μs)	20.4	29	32.6	25.4	29.6	27	30.8	34.1	29.7	31.4	30.3	32.6	35.9	31.4	33.9
ts^+ (V/μs)	67.5	55.8	45.5	57.9	566	58.3	51.3	45.5	51.5	51.3	50.1	45.4	41	46.2	45.2
ts^- (V/μs)	67	55	44.6	57	54.5	57.8	50.6	44.6	51	50.6	49.3	44.5	41	45.7	44.1

Table 5.5: Monte Carlo simulation results of proposed OTA for 1000 samples.

Parameter	μ^*	σ^*	$\sigma/\mu(\%)$
DC-gain (dB)	60.45	0.12	0.2
UGF (kHz)	70.3	4.9	7
Phase margin (°)	52.6	4.3	8.2
CMRR (dB)	126.9	0.15	0.1
Slew rate (↑) (mV/μs)	25	0.72	2.9
Slew rate (↓) (mV/μs)	25.2	0.75	3
ts^+ (μs)	50.1	1.45	2.9
ts^- (μs)	51.5	1.34	2.6

* μ: mean value σ: standard deviation

To examine the robustness of the proposed OTA against process and mismatch variations, Monte Carlo simulations were performed and the results are summarized in Table 5.5. The ratio between mean (μ) and standard deviation (σ) are calculated to check sensitivity due to process and mismatch variations. It is evident from Table 5.5 that the proposed OTA is robust against process variations since parameters are less than 10% sensitive.

The magnitude and phase responses obtained using Monte Carlo simulation for 1000 runs is shown in Fig. 5.15. The OTA parameters such as DC gain, CMRR, UGF and phase margin histogram are depicted in Fig. 5.16. The layout of the proposed OTA shown in Fig. 5.17 occupies an active area of $\approx$0.003 mm^2 (75 $\mu m \times$ 40 μm).

5.5 Design of $G_m - C$ Filter

For processing of low-frequency signals such as biomedical and audio, we considered the design of a tunable $G_m - C$ Butterworth low-pass filter using the proposed OTA. The performance of filter strongly depends on the basic building block, i.e., transconductance cell. The biquad filter is realized by replacing the passive elements of a RLC band pass filter with transconductor-capacitor arrangement. Here, inductor is replaced with a gyrator-capacitor arrangement and the resistor is replaced with a negative transconductor circuit. The conventional biquad filter topology is adopted from [130] and the block diagram of filter configuration is shown in Fig. 5.18. The transfer function of Butterworth biquad filter and conventional second-order low-pass filters are given in (5.21) and (5.22), respectively.

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{G_{m1}}{g_{m4}}\frac{G_{m3}G_{m4}}{C_1C_2}}{s^2 + \frac{G_{m2}}{C_1}s + \frac{G_{m3}G_{m4}}{C_1C_2}} \tag{5.21}$$

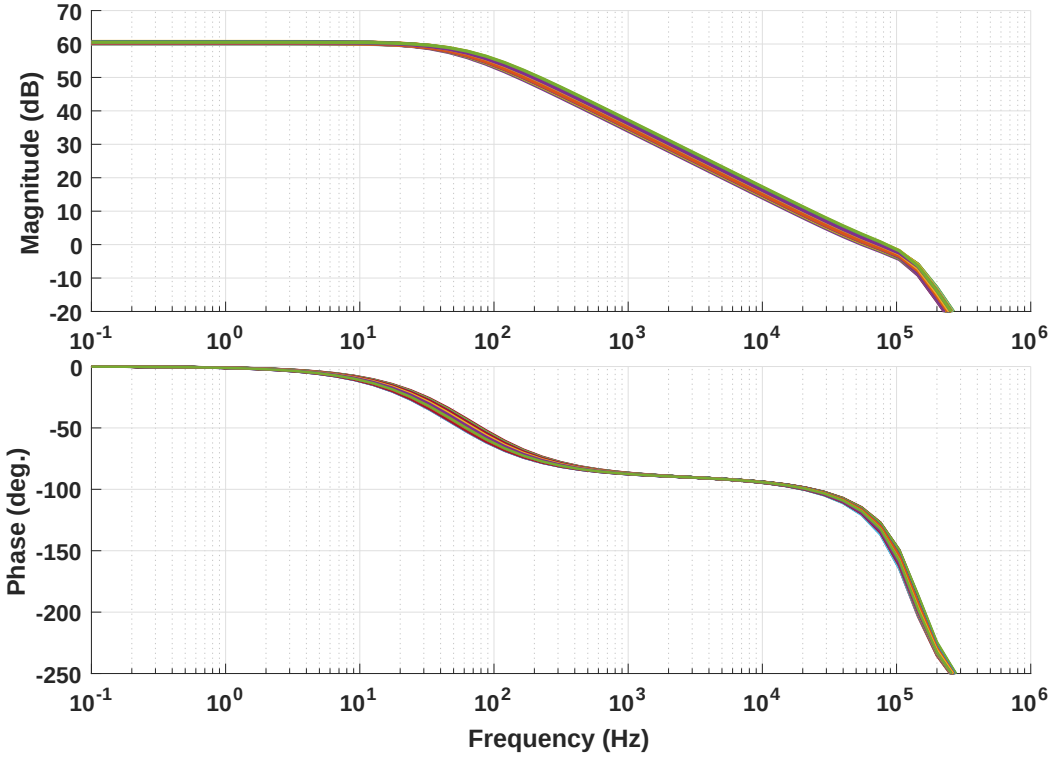


Figure 5.15: Magnitude and phase response of Monte Carlo simulation for 1000 samples (I_B=10 nA).

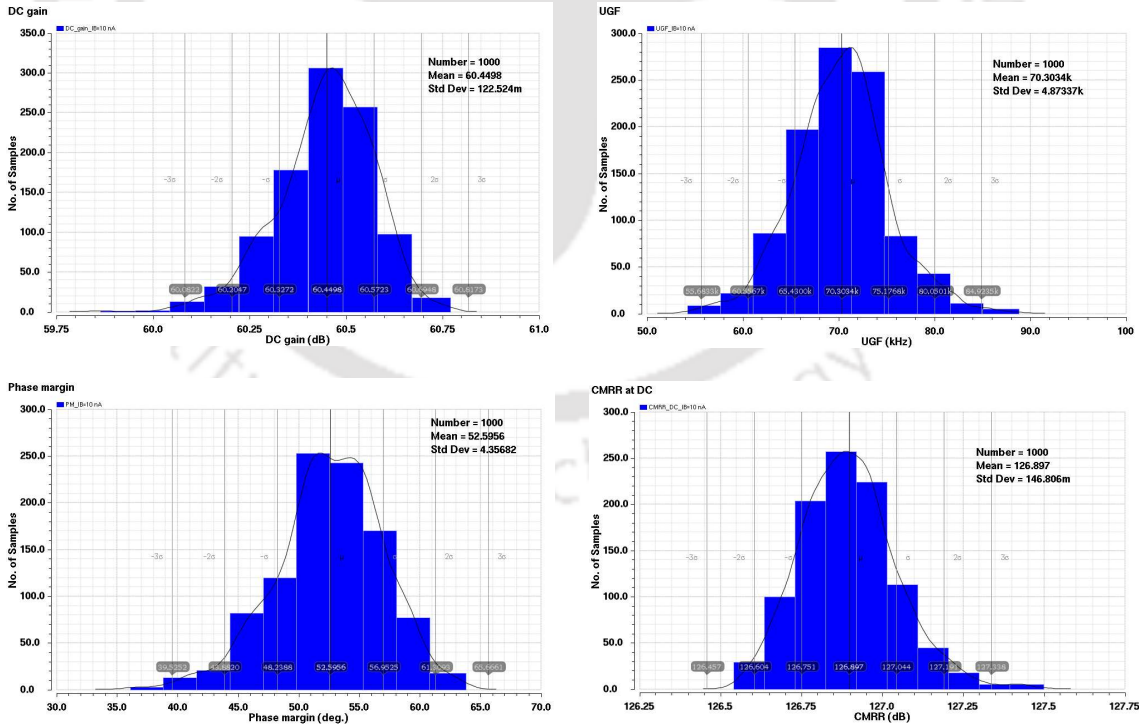


Figure 5.16: Monte Carlo simulation results for 1000 samples (I_B=10 nA).

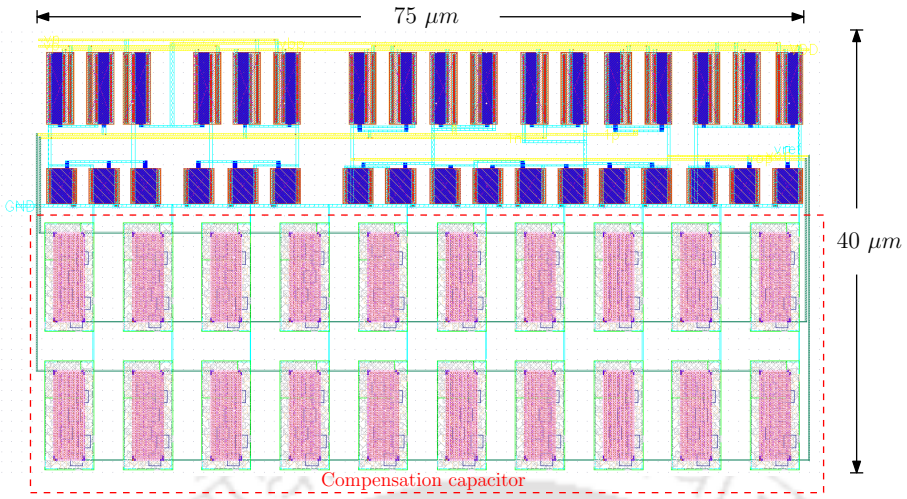


Figure 5.17: Layout of the pseudo-differential bulk-driven OTA.

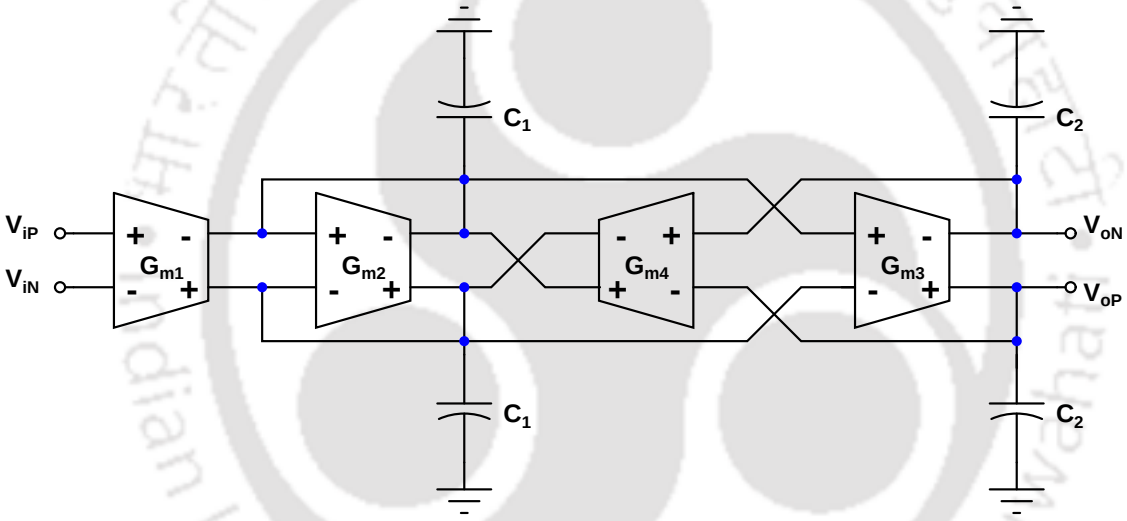


Figure 5.18: Fully differential biquad low-pass filter structure.

$$H(s) = \frac{A_P \omega_o^2}{s^2 + \frac{\omega_o^2}{Q} s + \omega_o^2} \tag{5.22}$$

where $G_{m1} - G_{m4}$ is the effective transconductance of OTA and C_1 and C_2 are the load capacitance of the filter. By comparing with the transfer function of standard low-pass filter, the pass band gain (A_P), corner frequency (f_o) and quality factor (Q) can be obtained as follows:

$$A_P = \frac{G_{m1}}{G_{m4}} \tag{5.23}$$

$$f_o = \frac{1}{2\pi}\sqrt{\frac{G_{m3}G_{m4}}{C_1C_2}} \tag{5.24}$$

and

$$Q = \sqrt{\frac{G_{m3}G_{m4}}{G_{m2}^2}}\sqrt{\frac{C_1}{C_2}} \tag{5.25}$$

All the transconductance $G_{m1} - G_{m4}$ cells used in filter circuit are identical ($G_{m1} = G_{m2} = G_{m3} = G_{m4} = G_m$). Substituting this in (5.23)−(5.25) results passband gain of unity and equations (5.24) and (5.25) reduced to

$$f_o = \frac{1}{2\pi}\frac{G_m}{\sqrt{C_1C_2}} \tag{5.26}$$

$$Q = \sqrt{\frac{C_1}{C_2}} \tag{5.27}$$

The filter cutoff frequency can be tuned either by changing the value of transconductance or the load capacitance. In the previous section, we proposed OTA which acts as tunable transconductance amplifier by changing the gate voltage of auxiliary amplifier at its input stage. Due to that, the value of capacitance is maintained constant and the change in G_m will alter the cutoff frequency of the filter. The filter is designed to achieve cutoff frequency of 20 kHz with the bias current of 10 nA.

The proposed OTA offers transconductance of 140 nS with bias current of 10 nA. The quality factor of the biquad filter is assumed unity, for that load capacitance is set to 1 pF ($C_1 = C_2 = 1$ pF). The cutoff frequency of filter as per (5.26) is approximately equal to 22.4 kHz which is closer to the desired value (i.e., f_c=20 kHz).

5.6 Simulation Results of $G_m - C$ Filter

The proposed 0.3-V pseudo-differential bulk-driven OTA is used to design a second-order fully differential Butterworth $G_m - C$ low-pass filter. It is clear from Section. 5.4 that the transconductance cell performance parameters are insensitive to the process and temperature variations which implies that the performance of filter is also insensitive to these variations. In filter design, the load capacitance C_1 and C_2 are set to 1 pF, which does not effect stability of OTA. The second-order Butterworth low-pass filter is also simulated in a UMS 65-nm CMOS process operating with supply voltage of 0.3-V.

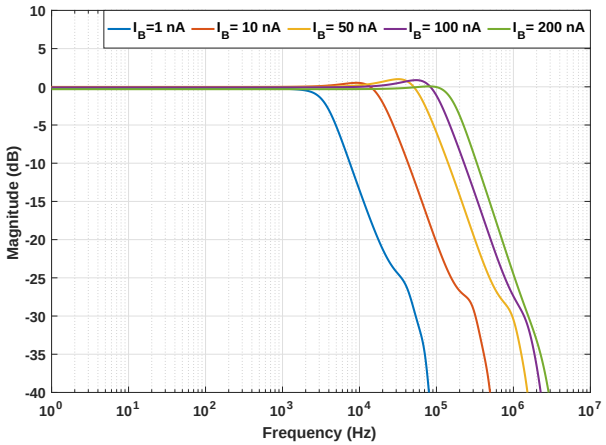


Figure 5.19: Simulated frequency response of the $G_m - C$ biquad filter.

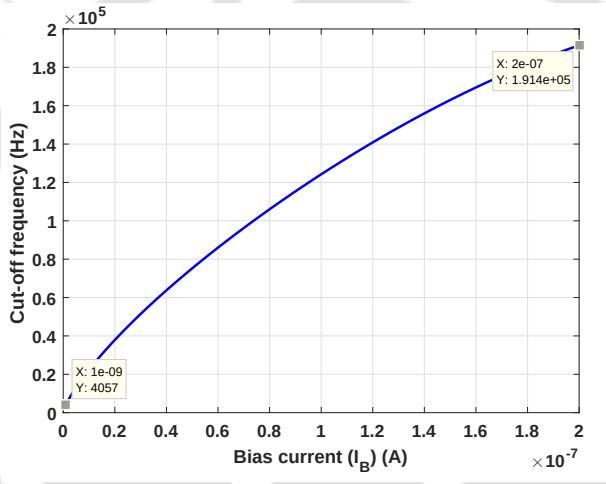
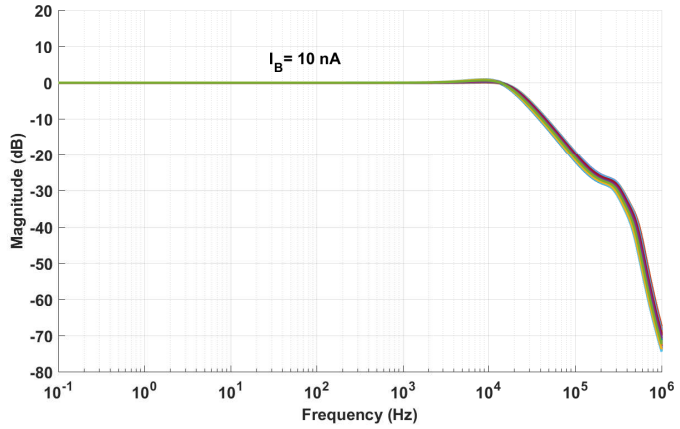


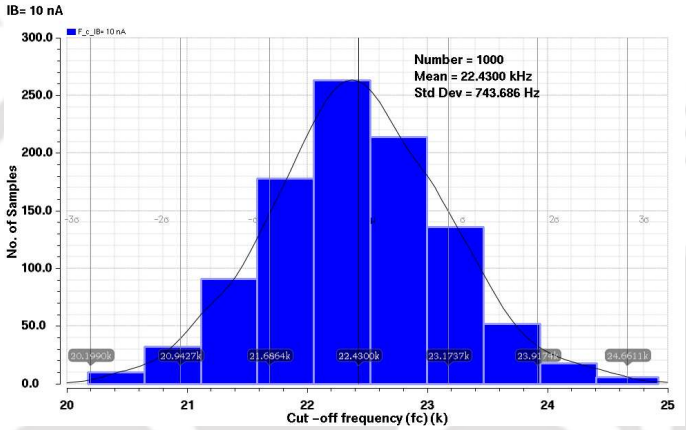
Figure 5.20: Cutoff frequency (f_c) of the $G_m - C$ filter with respect to bias current (I_B) variation.

The magnitude frequency response of filter is shown in Fig. 5.19. It is clear from Fig. 5.19 that a tunable cutoff frequency, which can be widely varied in the range of 4 kHz to 190 kHz, is obtained by varying the bias current I_B from 1 nA to 200 nA. Fig. 5.20 illustrates the cutoff frequency of the filter with respect to bias current I_B.

In order to observe the filter response due to process variations, the Monte-Carlo analysis of biquad filter is performed for 1000 samples at different bias current $I_B = 10$ nA. The corresponding magnitude response of the biquad $G_m - C$ filter is shown in Fig. 5.21(a) and the histogram of filter cutoff frequency is depicted in Fig. 5.21(b). It can be seen from Fig. 5.21(b) that the deviation in filter cutoff frequency due to process variation with in the acceptable limit with a relative error of 3.3%. Layout of the biquad filter is shown in Fig. 5.22, occupies an active area of 0.022 mm^2 (310



(a)



(b)

Figure 5.21: Monte Carlo simulation results of $G_m - C$ filter for 1000 samples (I_B=10 nA) (a) magnitude response (b) histogram of the cutoff frequency (f_c).

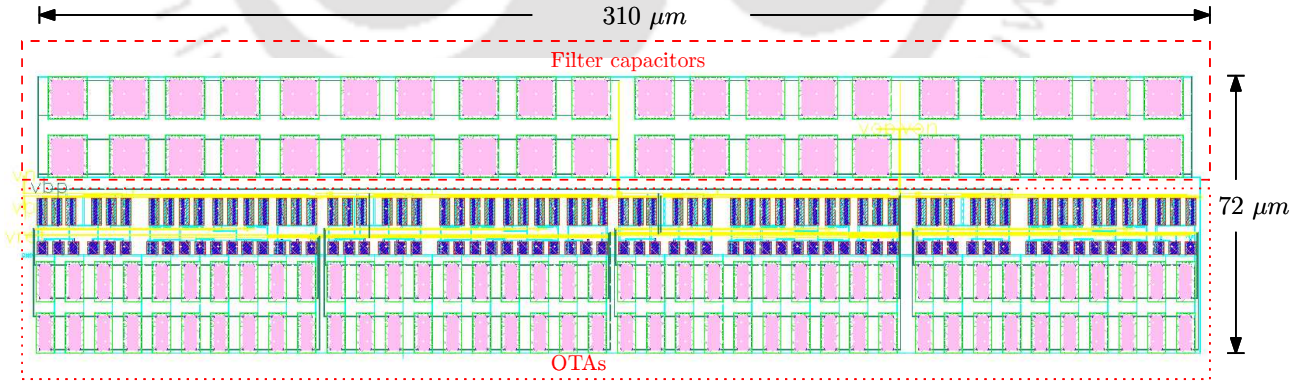


Figure 5.22: Layout of fully differential biquad $G_m - C$ low pass filter.

$\mu m \times 72\ \mu m$).

5.7 Comparative Studies

The performance parameters of proposed OTA and state-of-the-art sub-1 V designs are summarized in Table 5.6. In Chapter 4, the efficiency of UGF and slew rate is evaluated using IFOM_S and IFOM_L, respectively. The proposed OTA operating at a low supply voltage shows better IFOM_S and IFOM_L compared to other existing works [11, 26, 31]. Compared to state-of-the-art designs, the proposed design shows five times improvement in small-signal (IFOM_S) and 2.5 times improvement in large-signal performance (IFOM_L). The noise floor is the range which is acceptable for low-frequency applications. As the CMRR of the proposed OTA is high, this circuit can be used to process the signals encountered in biomedical applications.

In [11,31], the R-C miller compensation technique was used to minimize the current in the output stage of the OTA by means of pole-zero cancellation. However, when the OTAs are designed for low-frequency operations, the resistor value becomes very large (typically in the order of MΩs). Because of the large value of resistor, such OTAs [11,31] occupy large silicon area. In contrast, the proposed OTA occupies a smaller area of 0.003 mm^2 because circuit does not employ any resistors for compensation.

Table 5.6: Comparison of proposed OTA with state-of-the-art bulk-driven OTAs.

Parameters	[31]$^{\otimes}$	[26]$^{\otimes}$	[32]	[131]	[24]$^{\otimes}$		[60]	This Work
CMOS technology	0.18 μm	130 nm	0.18 μm	50 nm	65 nm		0.18 μm	65 nm
Output type (S/D)	D	S	D	D	S		S	D
Supply (V_{DD}) (V)	0.5	0.25	0.5	0.4	0.5	0.35	0.6	0.3
DC-gain (dB)	65	60	38.5$^{\alpha}$	58.6	46	43	82	60
Compensation	R-C Miller	Miller	Miller	R-C Miller	Damping		g_m−C	Miller
UGF (MHz)	0.55	0.0019	0.027	2.31	38	3.6	0.019	0.07
Phase margin (deg.)	50	79.2	69	50	57	56	60	53
Slew rate ($\uparrow/\downarrow$) (V/μs)	0.23 *	0.00064/-0.00077	–	1.2*	43*	5.6*	0.012*	0.025/-0.025
Noise ($\mu V/\sqrt{Hz}$)	0.432 at 1 kHz	3.3 at 0.1 kHz	2 at 0.1 kHz	0.164 at 10 kHz	0.94**	0.926**	0.16 at 1 kHz	2.82 at 1 kHz
CMRR (dB) at 1 Hz	86 at 5 kHz	–	53.15	92 at 5 kHz	35	46	130.2 at 100 Hz	126
PSRR^{+} (dB) at 1 Hz	76 at 5 kHz	–	–	64 at 5 kHz	37	35	–	90
PSRR^{-} (dB) at 1 Hz	–	–	–	–	–		–	91
C_L (pF)	20	15	5	20	3		15	5
I_T (μA)	56	0.072	0.6	79.6	364	48.6	0.667	0.17
Power (μW)	28	0.018	0.3	31.8	182	17	0.4	0.051
Area (mm^2)	0.052	0.083	–	–	0.005		–	0.003
IFOM$_S$	20	37.5	22.5	58	31.3	22.2	43	205
IFOM$_L$	8.21	13	–	30	35.4	34.5	27	73.5

Note: $\otimes$: measurement results; S: single ended; D: differential; α: pre-amplifier designed for gain of 40 dB; –: not reported; $*$: average value; $**$: noise frequency not defined;

$$\text{IFOM}_S = \text{UGF} \times \frac{C_L}{\text{I}_\text{T}} \left[\frac{\text{MHz}\times\text{pF}}{\mu A}\right] \times 100;$$

$$\text{IFOM}_L = \text{Slew rate} \times \frac{C_L}{\text{I}_\text{T}} \left[\frac{V}{\mu s} \times \frac{\text{pF}}{\mu A}\right] \times 100$$

5.8 Summary

A low-voltage, low-power pseudo-differential bulk-driven OTA which operates at a low supply voltage of 0.3-V, has been proposed. Simulation results show that the proposed OTA has a better FOM compared to other reported bulk-driven OTAs. Also, the proposed OTA gives a high CMRR value of 126 dB. Since, the bulk-driven differential stage provides small transconductance at the input stage, which results low common-mode gain. Also, the partial positive feedback configuration at the input and output stages provides a low common-mode gain. The proposed OTA performance is less affected due to temperature and process variations, which is evident from corner simulations. The total quiescent current consumption of the proposed OTA is 170 nA and occupies an active area of 0.003 mm^2. Because of these advantages, the proposed design is suited for low-voltage, low-power applications such as biomedical signal acquisition systems and portable systems. In addition, the proposed OTA is also employed to design a second order tunable $G_m - C$ low-pass filter.

6

Low-Voltage Class-AB Bulk-Driven OTAs with Improved Slew rate

Contents

6.1 Introduction

Analog voltage buffer is the most important building block of analog and mixed-signal systems such as LCD drivers, signal monitoring, testing, and to drive large C_L [132]. OTA can be used as a buffer when it is configured in unity gain mode. In order to drive large C_L at higher speed, OTA requires high slew rate. For the output to settle faster, the OTA also requires sufficient DC-gain and GBW. In order to satisfy all these requirements with minimum quiescent current consumption, there is a need for new OTA topology which can operate under low-voltage environment. In order to maintain sufficient SNR, the rail-to-rail operation has become necessary in low-voltage design [36, 133].

The adaptive biasing circuits are often employed to overcome the slew rate limitation [2,69]. In [69], a set of current mirrors are used to boost the bias current during large-signal operation. Another way to attain high slew rate of OTA is by increasing the current in active load of the differential input stage. Here, a local common mode feedback technique is employed with conventional Class-A differential pair to work as Class-AB amplifier [2, 40]. In this case, the maximum differential current of differential pair is twice the quiescent current. However, this approach necessitates the use of a large feedback resistor for sufficient current boosting, which is incompatible with larger phase margin. The current boosting ability of OTA is expressed by the current boosting factor (CBF) defined as the ratio of the maximum load current ($I_{out-MAX}$) to the differential pair bias current (I_B) i.e., $CBF = I_{out-MAX}/I_B$. The existing topologies discussed so far, either require large bias current to improve the slew rate or demands high supply voltage which in turn consumes more power. Hence, in this chapter, we proposed high driving capability low-voltage Class-AB bulk-driven OTAs with improved slew rate.

6.2 Proposed Circuit Implementation

In low-voltage environment, it is difficult to drive large C_L with fast settling time, since the bias current is usually quite small in weak inversion region. Moreover, the bulk-driven circuits have less driving capability as compared to gate-driven circuits. Hence, there is a need for new bulk-driven topology which can drive the large C_L with high speed.

Depending on system needs, OTA requires high DC-gain, high slew rate and large GBW. The high slew rate and GBW ensure small settling time, whereas the high gain improves the settling accuracy. Unfortunately, all these requirements are difficult to reach with Class-A circuits since the maximum output current is limited by the input stage bias current. Hence, there is a trade-off between slew

rate and power consumption. To achieve these desired features, Class-AB circuits are often employed. These circuits provide well-controlled quiescent currents, which can be made very low in order to reduce static power consumption.

6.2.1 Adaptive biasing

In order to obtain Class-AB bulk-driven OTA, we first consider the conventional bulk-driven Class-A OTA is shown in Fig. 6.1, which uses a constant bias current I_B to meet the desired GBW and slew rate. The expressions for UGF and slew rate of OTA are given by

$$\mathrm{UGF} = \frac{\mathrm{G_m}}{2\pi \mathrm{C_L}} \tag{6.1}$$

$$\text{Slew rate} = \frac{\mathrm{I_{out}}}{\mathrm{C_L}} \tag{6.2}$$

where, G_m represents effective transconductance, I_{out} is output current and C_L is load capacitance of OTA.

The effective transconductance G_m of Class-A OTA in Fig. 6.1 is equal to $g_{mb1,2}$. The UGF and output current of Class-A OTA in weak inversion region is given by

$$UGF_{\mathrm{Class-A}} = \frac{g_{mb1,2}}{2\pi C_L} \tag{6.3}$$

$$I_{\mathrm{out,Class-A}} = 2.BI_B \tanh\left(\frac{V_{id}}{2nV_T}\right) \tag{6.4}$$

where, B is output current mirror (M_6 and M_8) ratio, V_{id} is the differential input voltage. All the other symbols have their usual meanings. The differential input voltage (V_{id}) of gate-driven and bulk-driven circuits is equal to $V_{iP} - V_{iN}$ and $(n-1)(V_{iP} - V_{iN})$, respectively.

It is clear from (6.4) that for large V_{id} the maximum output current of Class-A OTA is limited to $2BI_B$, which causes slewing at output node. The Class-AB OTAs are often employed to reduce the slewing effect. This is due to the fact that, for large V_{id} the output current of Class-AB OTA is not limited by input stage bias current I_B.

The conventional Class-A OTA in Fig. 6.1 is transformed into Class-AB by using adaptive biasing circuit at input stage as shown in Fig. 6.2. Here, the adaptive biasing circuit is realized with the help of bulk-driven flipped voltage follower (FVF). The cross connected FVF cells provides Class-

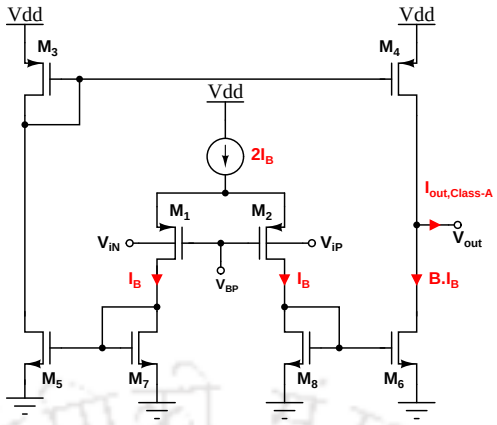


Figure 6.1: Schematic of current mirror OTA (Class-A) [2].

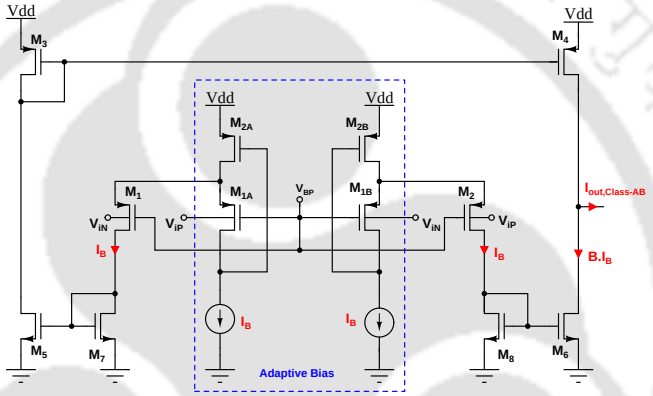


Figure 6.2: Schematic of OTA with adaptive bias (Class-AB).

AB operation at input stage. Each FVF cell comprises of transistors M_{1A}/M_{1B}, M_{2A}/M_{2B} and bias current I_B. The differential inputs V_{iP} and V_{iN} are connected to bulk-terminals of M_2, M_{1A} and M_1, M_{1B} transistors, respectively. The FVF copies input signal V_{iP} (V_{iN}) to source of M_1 (M_2), which results the effective transconductance twice that of conventional (i.e., Class-A OTA) OTA. The effective transconductance of Class-AB OTA is approximately $2g_{mb1,2}$ and UGF is given by

$$UGF_{\text{Class}-\text{AB}} \approx \frac{2.g_{mb1,2}}{2\pi C_L} \tag{6.5}$$

At quiescent condition, both input transistors M_1 and M_2 carries equal current of I_B. For $Vid >> 0$ ($V_{iP} >> V_{iN}$), the current in M_1 increases and is not limited to quiescent current I_B. Whereas current through M_2 decreases which is less than the quiescent current I_B. Similarly, when $Vid << 0$ ($V_{iP} << V_{iN}$) the current in M_2 increases and current through M_1 decreases. In Class-AB OTAs, the dynamic current is boosted for large V_{id} and it is larger than the input quiescent current levels. The

output current expression of Class-AB OTA is given by

$$I_{\text{out,Class}-\text{AB}} \approx 2BI_B \sinh\left(\frac{V_{id}}{nV_T}\right) \tag{6.6}$$

The normalized output current characteristics of Class-A and Class-AB OTAs are depicted Fig. 6.3. It is evident from Fig. 6.3 that the maximum output current of Class-A OTA is limited to $2I_B$ even for larger V_{id}. On the other hand, the Class-AB OTA output current is much larger than bias current $2I_B$. Therefore, it is possible to achieve large dynamic current using adaptive biasing with a low standby current. The adaptive biasing improves the driving capability of OTA.

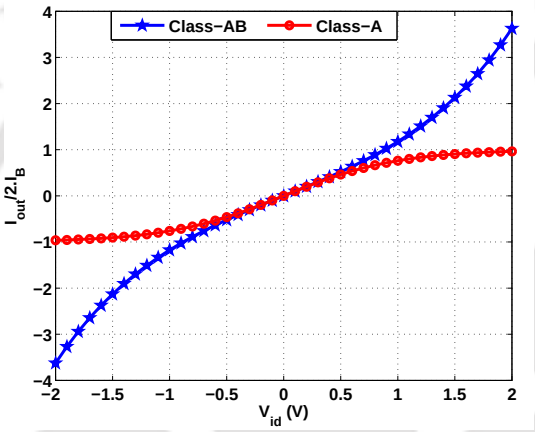


Figure 6.3: MATLAB simulation results for normalized output current characteristics of Class-A and Class-AB OTA for B=1.

Fig. 6.4 illustrates the schematic simulation results for the output current of Class-A and Class-AB OTAs. Here, we considered the supply voltage of 0.5-V. It is clear from Fig. 6.4 that the adaptive biasing improves output current at lower input voltages which are $< \pm 0.5$-V.

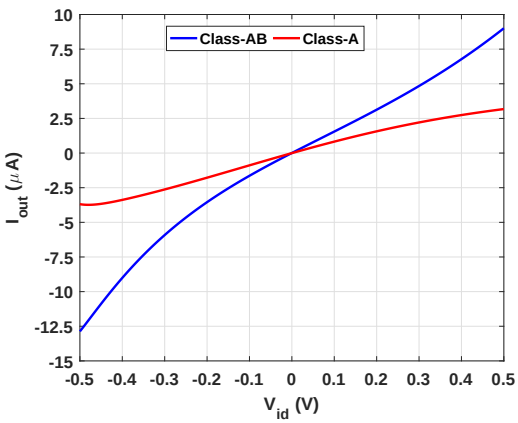


Figure 6.4: Simulation results for the output current (I_{out}) characteristics of Class-A and Class-AB OTA with B=10 and $I_B = 0.25$ μA.

6.2.2 Adaptive loads

The CBF also depends on the load resistance of input stage [134]. For high output current, a larger value of load resistance is required at the input stage. But, the large resistance causes stability issues in case of small-signal variations. The additional dynamic current can be obtained by using the cascode current mirror as an active load of the input stage [82]. This current mirror gain depends on the variation in the input voltage. The operating region of the active load transistors changes with variation in input voltage. This results variation in load resistance and hence acts as an adaptive load. The current mirror gain is unity for small-signal voltage variation. However, for large differential input voltage, the current mirror gain is greater than 1 and yields a larger output current.

Schematic of various cascode current mirror load configurations are shown in Fig. 6.5. In Fig. 6.5, the Type II and Type III act as adaptive loads due to variation in the input current (I_{in}). These loads shows a variation in load resistance due to change in the operating region of transistors [82, 83]. For low supply voltage, these loads can be operated in weak inversion region and shows a large variation in the load resistance with low quiescent currents.

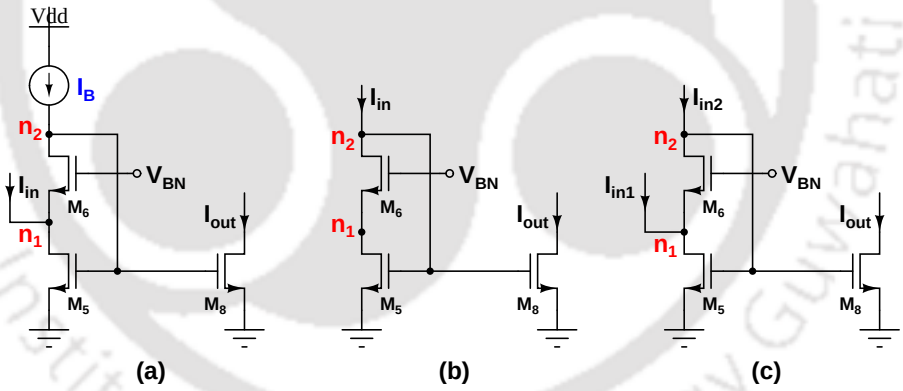


Figure 6.5: Schematic of non-linear current mirror (a) Type I (b) Type II (c) Type III.

In Type I load, the impedance at node n_1 is very low and hence large I_{in} can flow through node n_1 due to variation in the input voltage. But, the variation in I_{in} does not effect node voltage of n_1 and hence drain-to-source voltage (V_{DS}) of M_5 remain constant [133]. The MOS transistor M_5 connected in shunt feedback configuration and it translates the changes in I_{in} into a compressed voltage at node n_2. The replica of changes I_{in} is generated using the voltage variation at n_2 and output transistor M_8.

The current-voltage relations for Class-AB operation of input stage using Type I load are given in

Table 6.1: The output current of non-linear current mirror Type I load.

M_6 Weak inversion $V_{GS} < V_{TH}$, $V_{DS} \geq 0.1$ V M_5 Linear Region $V_{GS} < V_{TH}$, $V_{DS} < 0.1$ V	M_6 Strong Inversion $V_{GS} \geq V_{TH}$, $V_{DS} \geq V_{DS,sat}$ V M_5 Linear Region $V_{GS} \geq V_{TH}$, $V_{DS} < V_{DS,sat}$ V
$I_{D5} = I_o\left(\frac{W}{L}\right)_5 \exp^{\frac{V_{GS5}-V_{TH}}{nV_T}} \left(1 - \exp^{\frac{-V_{DS5}}{V_T}}\right)$; $I_{D5} = I_B + I_{in}$	$I_{D5} = \beta_5 \left(V_{GS5} - V_{TH}\right).V_{DS5}$; $I_{D5} = I_B + I_{in}$
$V_{GS5} = V_{TH} + nV_T \ln\left(\left(I_B + I_{in}\right) \Big/ I_o\left(\frac{W}{L}\right)_5 \left(1 - e^{\frac{-V_{DS5}}{V_T}}\right)\right)$	$V_{GS5} = V_{TH} + \frac{I_{D5}}{\beta_5 V_{DS5}}$
$I_{D8} = \frac{W_8}{W_5}\left(\frac{I_B + I_{in}}{1 - \exp^{\frac{-V_{DS5}}{V_T}}}\right)$	$I_{D8} = \frac{\beta_8}{2}\left(\frac{I_B + I_{in}}{\beta_5 V_{DS5}}\right)^2$
$I_{in} = I_B e^{\frac{-V_{id}}{nV_T}}$	$I_{in} = \frac{\beta_{1,2}}{2}\left(\sqrt{\frac{2I_B}{\beta_{1,2}}} - V_{id}\right)^2$
$I_{D8} = \frac{W_8}{W_5}\left(\frac{I_B + I_B e^{\frac{-V_{id}}{nV_T}}}{1 - e^{\frac{-V_{DS5}}{V_T}}}\right)$	$I_{D8} = \frac{\beta_8}{2}\left\{\frac{I_B}{\beta_5 V_{DS5}} + \frac{\beta_1}{2\beta_5 V_{DS5}}\left(\sqrt{\frac{2I_B}{\beta_1}} - V_{id}\right)^2\right\}^2$

Table 6.1, with left and right side column represents the current-voltage relations for weak inversion and strong inversion region, respectively. The output current for weak inversion condition is given in (6.7) and denominator of (6.7) becomes approximately if $V_{DS5} > 4V_T$.

$$I_{D8,TypeI} = \frac{W_8}{W_5}\left(\frac{I_B + I_B e^{\frac{-V_{id}}{nV_T}}}{1 - e^{\frac{-V_{DS5}}{V_T}}}\right) \tag{6.7}$$

In Type II load, as I_{in} increases, the V_{GS} of M_6 increases and this results in V_{DS} of M_5 to decrease. If $V_{DS5} < 4V_T$, transistor M_5 enters into triode region. This causes a large voltage variation at node n_2 (i.e., V_{GS} of M_5). The Type II load delivers a large dynamic current as compared to Type I due to voltage variation at n_1 (i.e., V_{DS5}). The output current of Type II adaptive load is given by

$$I_{D8,TypeII} = \frac{W_8}{W_5}\left(\frac{I_B e^{\frac{-V_{id}}{nV_T}}}{1 - e^{\frac{-V_{DS5}}{V_T}}}\right) \tag{6.8}$$

In order to further improve the dynamic current, the Type III load which is functionality equivalent to the combination of Type I and Type II is used. In Fig. 6.5 (c), as the input current I_{in2} increases, the node voltage of n_1 decreases similar to Type II load. As discussed, in Type I load the voltage at node n_1 is not influenced by the variation in I_{in1}. Nevertheless, the combination of I_{in1} and I_{in2} increases overall node voltage of n_2 (i.e., V_{GS} of M_5). This results in a large dynamic current and the output current of M_8 is given by

$$I_{D8,TypeIII} = \frac{W_8}{W_5}\left(\frac{2I_B e^{\frac{-V_{id}}{nV_T}}}{1-e^{\frac{-V_{DS5}}{V_T}}}\right) \tag{6.9}$$

This conclude that the adaptive biasing and adaptive load techniques improve the dynamic performance of the circuit. The implementation of low-voltage bulk-driven Class-AB OTAs using these configurations are detailed in the following sections.

6.3 Low-Voltage Super Class-AB Bulk-Driven OTA with Adaptive Biasing and Adaptive Load

The schematic diagram of the bulk-driven OTA with adaptive biasing and adaptive load is shown in Fig. 6.6. To provide rail-to-rail driving capability, the proposed OTA is composed using bulk-driven differential input stage and a push-pull output stage. The adaptively biased input stage is implemented using cross-coupled bulk-driven FVF which is able to source a large amount of current for large V_{id} and hence, the output current of OTA is not be limited by the input stage bias current I_B. In Fig. 6.6, each FVF cell is implemented using a bulk-driven transistor $M_{1A/1B}$, a diode-connected transistor $M_{2A/2B}$ which is connected in a shunt feedback and a biasing current source I_B. The CBF mainly depends upon the output current of OTA and input stage bias current at quiescent state. The adaptive biasing provides a variable bias current for input differential pair ($M_{3A/3B}$ and $M_{4A/4B}$) during the presence of input signal. This reduces the quiescent current consumption without degrading the transient behaviour.

The proposed OTA in Fig. 6.6 employs Type III adaptive load at the input stage. Each branch of input differential pair splits into two-paths using the transistors $M_{3A/3B}$ and $M_{4A/4B}$ which carries an equal bias current of I_B. The drain terminal of these transistors is connected to node $n_{2A/2B}$ and $n_{1A/1B}$, respectively, as shown in Fig. 6.6. The differential input voltages V_{iP} and V_{iN} are connected to bulk-terminal of transistor M_{1A}, M_{3B}, M_{4B} and M_{1B}, M_{3A}, M_{4A}, respectively. The gate terminal of these transistors is connected to a bias voltage V_{BP}. The cross-connected FVF cell copies the opposite phase input signal (V_{iP}/V_{iN}) and drives the source of input differential pair transistors (V_{iP} to M_{3A}, M_{4A} and V_{iN} to M_{3B}, M_{4B}). As a result, the effective transconductance of input stage gets doubled by driving the bulk and source terminals of input stage. The input stage is operated in Class-AB by means of adaptive biasing, thus improves the dynamic performance.

As discussed in previous Section. 6.2.2, adaptive loads improves the dynamic current which results

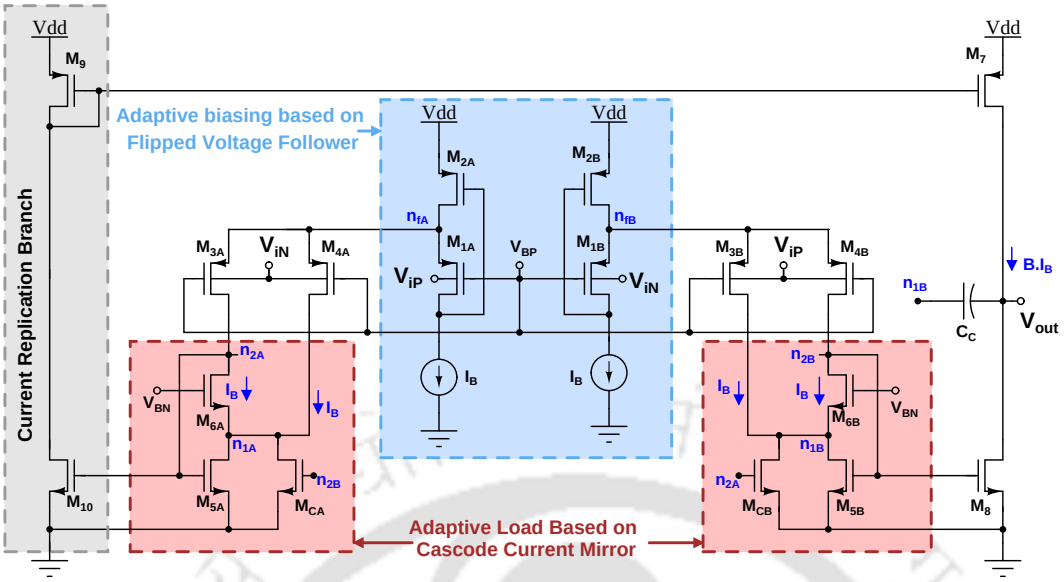


Figure 6.6: Schematic of bulk-driven OTA with adaptive biasing and adaptive load.

in CBF of OTA also to improve. In quiescent condition, all the transistors in Fig. 6.6 operates in a weak inversion region. In this case, transistors M_{5A} and M_{5B} operates in weak inversion, but close to the boundary of triode region (i.e., $V_{DS5A,5B} \approx 4V_T$) and the overall input resistance of active load is small. However, if current in M_{3A}/M_{3B} increases, this causes an increase in V_{GS} of M_{6A}/M_{6B} that decreases the V_{DS} of M_{5A}/M_{5B}, thus driving it to the triode region. Hence, input resistance increases and features a drastic change in V_{GS} of M_{5A}/M_{5B}. Due to reduction in V_{DS} of M_{5A}/M_{5B}, these transistors require large V_{GS} to accommodate the increased current. In addition, the low impedance node n_{1A}/n_{1B} can sink large current variations from the input stage (i.e., current variation in M_{4A} and M_{4B}). The shunt feedback transistor M_{5A}/M_{5B} translates these current variations into voltage variations at node n_{2A}/n_{2B} (i.e., V_{GS} of M_{5A}/M_{5B}). The current variation in both input pairs $M_{3A/3B}$ and $M_{4A/4B}$ improves the V_{GS} of M_{5A}/M_{5B} drastically. The output stage transistors M_8 and M_7 copy the voltage variations at node n_{2A}/n_{2B} and produce the output current.

Apart from this, a pair of transistors M_{CA} and M_{CB} are configured in a cross-coupled configuration to cancel gate transconductance of M_{5A} and M_{5B}. This improves effective resistance at node n_{2A} and n_{2B} and hence gain of input stage increases. For large V_{id}, one of the cross-connected transistors (M_{CA}/M_{CB}) will go into the cut-off region, this causes further improvement in the V_{GS} of M_{5A}/M_{5B}. The voltage variation at node n_{2A}/n_{2B} can be used to boost the current in output transistor M_8/M_{10}. As the transistors in Fig. 6.8 are operating in weak inversion region, the output current of Class-AB

bulk-driven OTA is given by

$$I_{out} = \pm 2.BI_B \left(\frac{e^{\frac{|V_{id}|}{nV_T}} - e^{-\frac{|V_{id}|}{nV_T}}}{1 - e^{\frac{-V_{DS5A/5B,min}}{V_T}}} \right) \tag{6.10}$$

where, $V_{DS5A/5B,min}$ represents the minimum V_{DS} of diode connected transistor (M_{5A} and M_{5B}). The overall DC- gain of bulk-driven OTA without slew rate enhancer is given by

$$A_{DC,\text{w/o SE}} \approx \left(\frac{2\left(g_{mb3} + g_{mb4}\right)}{g_{ds4}} \right) \left(\frac{g_{m8} + g_{m7} \times \frac{g_{m10}}{g_{m9}}}{g_{ds7} + g_{ds8}} \right) \tag{6.11}$$

6.4 Low-Voltage Class-AB Bulk-Driven OTA with Slew rate Enhancer

The schematic diagram of bulk-driven Class-AB OTA with slew rate enhancer (SE) is shown in Fig. 6.7. The SE circuit further improves the driving capability of OTA. Two SE circuits are placed in between Class-AB input stage and push-pull output stage through current replication branch as shown in Fig. 6.7. The SE placed in the right and left side provides large dynamic current during the rising and falling edges of the differential input voltage, respectively.

The SE with current feedback (CFB) loop is shown in Fig. 6.8. In the SE circuit, the tail current is made input signal dependent by adding an additional feedback current (I_F) source to the main tail current source i.e., I_B. The current feedback loop is realized using transistors $M_{16A/16B} - M_{19A/19B}$.

The reference current (I_R) source is generated by means of current subtractor ($M_{13A/13B} - M_{16A/16B}$). It is copied to the tail current source of SE with the help of nonlinear current mirror ($M_{17A/B} - M_{19A/B}$) in current feedback loop. At quiescent condition i.e., $V_{id} = 0$, $I_F = K.I_R$, where K is called the current feedback factor. The CFB loop in Fig. 6.8 adjust the feedback current (I_F) with respect to change in the input differential voltage. The mathematical expression of reference current in CFB loop can be expressed as [69]

$$I_R = I_P - I_N = \frac{I_B \left(e^{\frac{-V_{2d}}{nV_T}} - 1 \right)}{(K+1) - (K-1)\, e^{\frac{-V_{2d}}{nV_T}}} \tag{6.12}$$

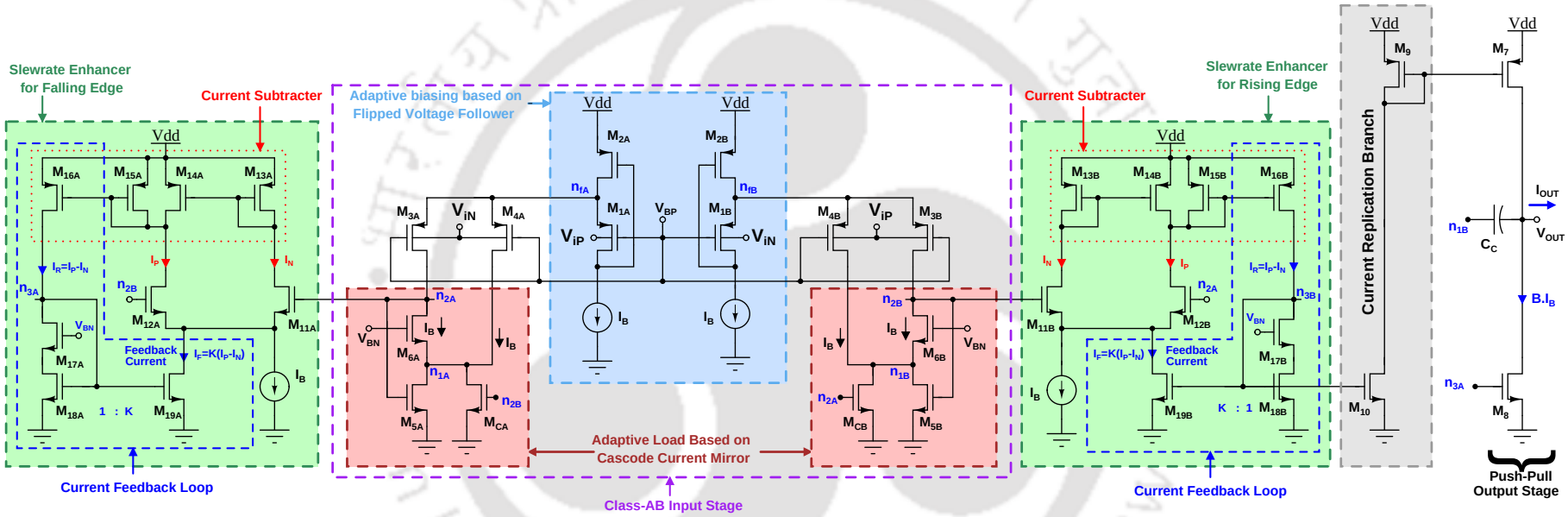


Figure 6.7: Schematic of Class-AB bulk-driven OTA with slew rate enhancer.

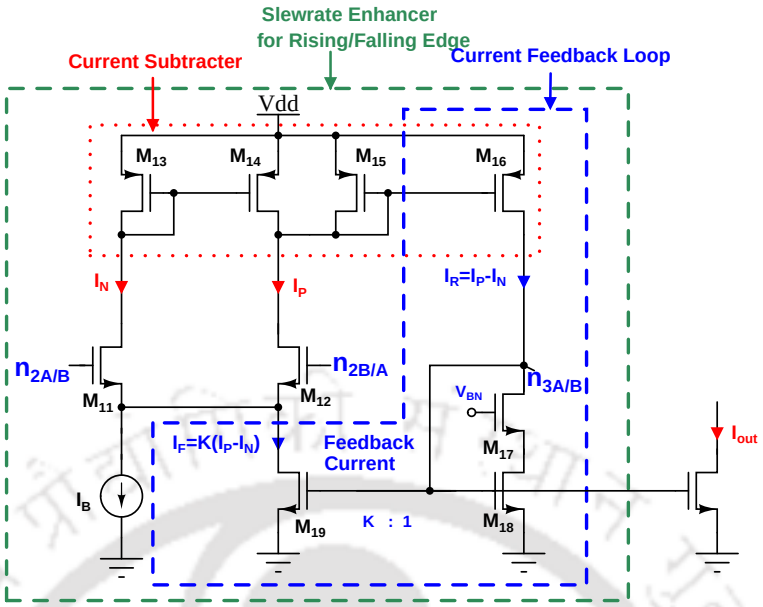


Figure 6.8: Schematic diagram slew rate enhancer.

In (6.12), V_{2d} represents the differential input voltage across the SE circuits (i.e., differential output voltage of input stage) and it is given by

$$V_{2d} = \begin{cases} nV_T \ln\left\{\dfrac{e^{\frac{V_{id}}{nV_T}}}{\left(1-e^{-\frac{V_{DS5A/5B,min}}{V_T}}\right)}\right\} & \text{for } V_{id} > 0 \\ nV_T \ln\left\{e^{\frac{V_{id}}{nV_T}}\left(1-e^{-\frac{V_{DS5A/5B,min}}{V_T}}\right)\right\} & \text{for } V_{id} < 0 \end{cases} \tag{6.13}$$

where, $V_{DS5A/5B,min}$ is the minimum V_{DS} across diode connected transistor (M_{5A} and M_{5B}) in the cascode-current mirror at the input stage.

As the differential input voltage changes i.e., $V_{id} > 0$ or $V_{id} < 0$, the feedback current I_F will be higher than I_R. This is because of the fact that as I_R increases, the V_{DS} of M_{18A}/M_{18B} decreases driving it into triode region. To accommodate the increased current I_R, V_{GS} of M_{18A}/M_{18B} will increase (i.e., voltage of node n_{3A}/n_{3B}). As a result, the feedback current I_F will be higher than I_R. This increases the tail current of SE, and improves the driving capability. The I_F of SE can be obtained as

$$I_F = K(I_P - I_N) = \frac{K}{\left(1-e^{\frac{-V_{DS18A/18B,min}}{V_T}}\right)} \cdot \frac{I_B\left(e^{\frac{-V_{2d}}{nV_T}}-1\right)}{(K+1)-(K-1)\,e^{\frac{-V_{2d}}{nV_T}}} \tag{6.14}$$

where, $V_{DS18A/18B,min}$ is the minimum V_{DS} of diode connected transistors M_{18A} and M_{18B} in CFB loop.

The current feedback loop in slew rate enhancer creates partial positive feedback which improves the DC-gain of OTA. The approximated analytical expression for DC-gain of slew rate enhancer circuit ($A_{DC,SE}$) can be written as

$$A_{DC,\mathrm{SE}} \approx \frac{\frac{g_{m16}}{g_{m18}}\left(\frac{g_{m12}+g_{m11}}{2g_{m15}}\right)}{1-\frac{g_{m16}}{g_{m18}}.\frac{g_{m19}}{g_{m15}}\left(\frac{g_{m12}-g_{m11}}{g_{m12}+g_{m11}}\right)} \tag{6.15}$$

The voltage variation at node n_{3A} and n_{3B} is used to drive the output transistors M_8 and M_{10}. In unity-gain configuration of OTA, the CFB loop recursively copies output driving current and increases the bias current of SE until the input and output voltages become equal. The differential output current (I_{out}) of OTA with SE is given by

$$I_{out} = \frac{\pm B}{\left(1-e^{\frac{-V_{DS18A/18B,min}}{V_T}}\right)}\left(\frac{I_B\left(e^{\frac{-|V_{2d}|}{nV_T}}-1\right)}{(K+1)-(K-1)\,e^{\frac{-|V_{2d}|}{nV_T}}}\right) \tag{6.16}$$

where, V_{2d} represents differential input voltage of SE and it is given in (6.13), $V_{ds18A/18B,min}$ is the minimum V_{DS} across diode connected transistor (M_{18A}/M_{18B}) in CFB loop, and B is current scaling factor of output stage. It is clear from (6.16) that the combination of adaptive biasing and adaptive load with slew rate enhancer increases the driving capability and improves the slew rate significantly. The overall DC-gain of bulk-driven OTA with SE is given by

$$A_{DC,\mathrm{w/i\ SE}} \approx \left(\frac{2\,(g_{mb3}+g_{mb4})}{g_{ds4}}\right)\left(\frac{g_{m8}+\frac{g_{m7}\times g_{m10}}{g_{m9}}}{g_{ds7}+g_{ds8}}\right)A_{DC,\mathrm{SE}} \tag{6.17}$$

The proposed OTAs in Fig 6.6 and 6.7 employ an indirect feedback compensation technique to provide the stability [135]. Here, a compensation capacitor (C_C) is connected in between low-impedance node n_{1B}, output node V_{out}. This provides an acceptable phase margin ($> 45°$) even for large C_L but with a small reduction in UGF.

6.5 Simulation Results

The proposed Class-AB bulk-driven OTAs are designed and post-layout simulations performed using UMC 65-nm CMOS process, with 0.5-V supply voltage and 100 pF load capacitance. The bias

current at input stage (I_B) is set to 0.25 μA, current scaling factor B of the output stage is set to 10. The total quiescent current (I_T) of Class-AB OTA with and without SE is equal to 6.25 μA, 4.25 μA, respectively. On-chip compensation capacitor (C_C) of 1 pF is used to stabilize the amplifier. In order to maximize the signal swing, the input/output quiescent voltage is normally set to $V_{DD}/2$ and the bias voltages V_{BN} and V_{BP} are set to 0.25-V. Through simulations, small-signal parameters such as DC gain, GBW and large-signal parameter such as slew rate of OTA were observed. The OTA in Fig. 6.6 is considered as a Class-AB bulk-driven OTA without SE.

The open-loop frequency response of the proposed OTA with and without SE is illustrated in Fig. 6.9. Note that the OTA with SE shows 150% improvement in UGF with a small reduction in phase margin compared to the OTA without SE. It is clear from Fig. 6.9 that the DC-gain of the proposed design with SE is improved by 17 dB. The OTA with and without SE provides input referred noise of 651 $nV/\sqrt{Hz}$ at 100 kHz.

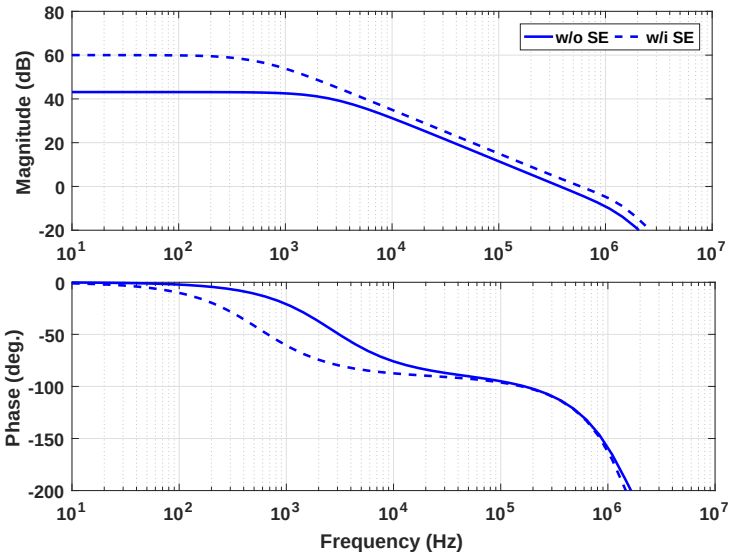


Figure 6.9: Open-loop frequency response of the proposed bulk-driven OTAs.

The voltage buffer is designed by configuring the proposed OTAs in unity gain feedback mode. Fig. 6.10 illustrates the simulated DC output voltage characteristics of voltage buffer and its corresponding error plots ($V_{out} - V_{in}$). It is apparent from Fig. 6.10 that both OTAs are offering rail-to-rail output swing, and OTA with and without SE offers an error voltage of $\pm$1.5 mV and $\pm$7.5 mV, respectively, near supply rails. As compared to OTA with SE, the error voltage of OTA without SE is more because of low-voltage gain.

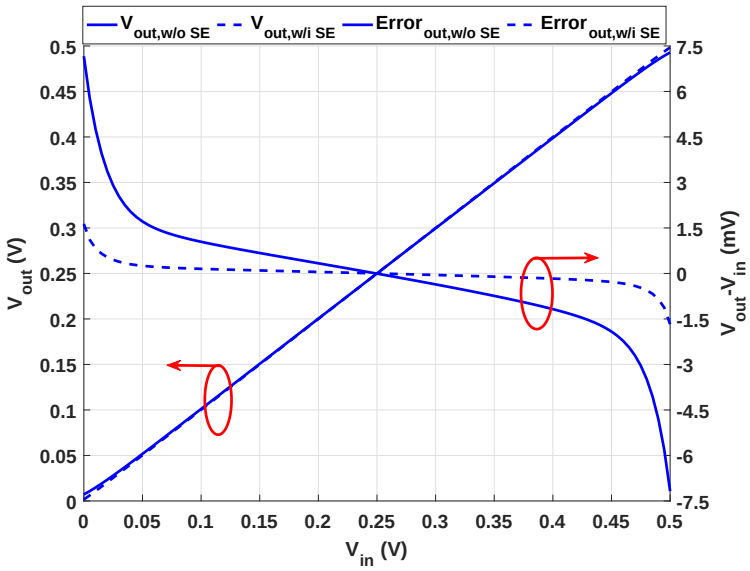


Figure 6.10: Simulated DC output and error voltage characteristics of unity gain amplifier.

Fig. 6.11 illustrates the transient response of the unity-gain amplifier for an input pulse of 0.5 V_{p-p} amplitude and frequency of 40 kHz with a load capacitance of 100 pF. The average slew rate of the OTA with SE is 0.93 V/μs which is 10 times that of slew rate of the OTA without SE. To observe the steady state behaviour, transient simulation is performed using 40 kHz pulse with an amplitude of 10 mV_{p-p} and simulation results are shown in Fig. 6.12. It is clear from 6.12 that the OTA without SE shows better settling response for small-signal input due to its high phase margin. However, for large-signal input the OTA with SE shows better settling response due to high slew rate and it is evident from Fig. 6.11.

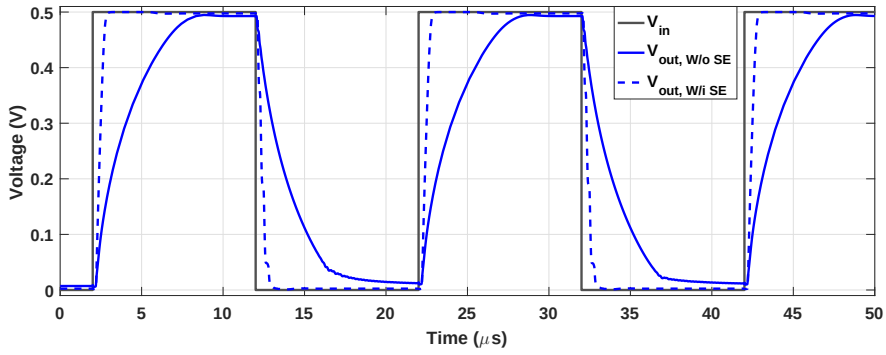


Figure 6.11: Transient response of OTAs in unity gain configuration for large step pulse.

In order to observe the large-signal response under different load conditions, a 20 kHz square wave

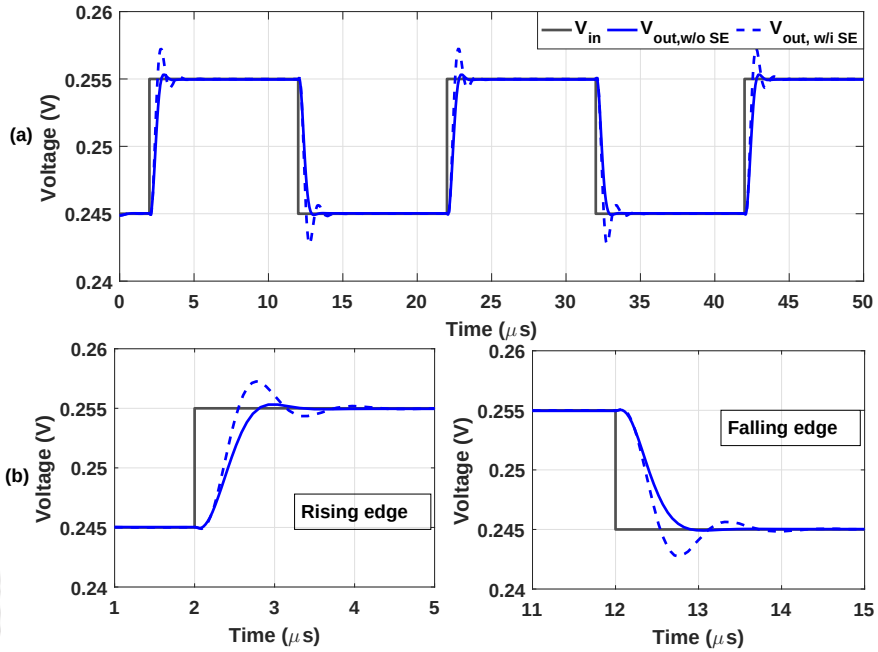


Figure 6.12: Transient response of OTAs in unity gain configuration for small step pulse and its zoomed version.

is applied with a step input voltage of 0.5 V_{p-p} to unity gain amplifier. The transient responses of the proposed OTA with and without SE for different load capacitors is shown in Fig. 6.13. It is evident from Fig. 6.13 that the proposed OTA (with SE) offers rail-to-rail swing even with large C_L of 2 nF. The average settling time is 9.5 μs for 1% error, which is an acceptable value for small and large size LCD column drivers [68, 87]. The applications where a load capacitance around 100 pF or more is used are reference buffers in data converters, IO buffers for measurement test setup, LCD column driver of display panels, and error amplifier in capacitor-less low dropout regulators.

The small-signal performance parameters such as DC gain, UGF and phase margin obtained for the proposed amplifiers by varying the common-mode input voltage V_{CM} are shown in Fig. 6.14. It is clear from Fig. 6.14 that the parameters are less sensitive to the common-mode input voltage variation. Whereas, the variation of DC gain, UGF and phase margin are less than $\pm$1.6%, $\pm$9% and $\pm$2.8%, respectively, using a typical value of V_{CM}=0.25 V. In order to operate OTA without any stability issues, the performance of OTA should be insensitive to the common-mode component of the input signal. This target is achieved without imposing any restriction on the operating frequency range of the circuit.

Transient simulations have been performed to obtain the response of unity gain amplifiers. These

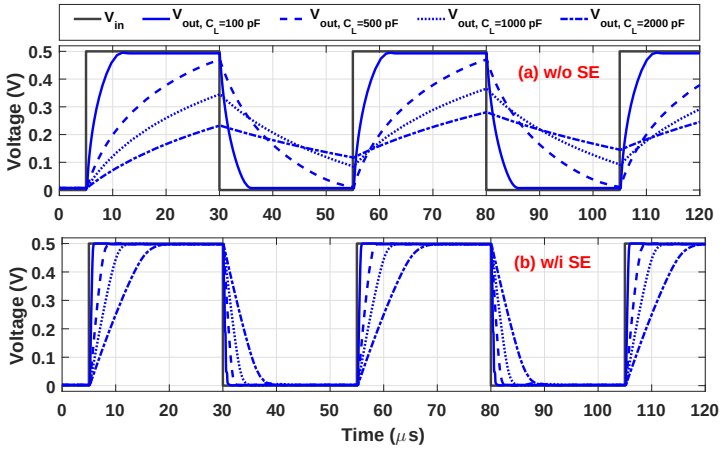


Figure 6.13: Large-signal transient response of unity gain amplifier with different C_L.

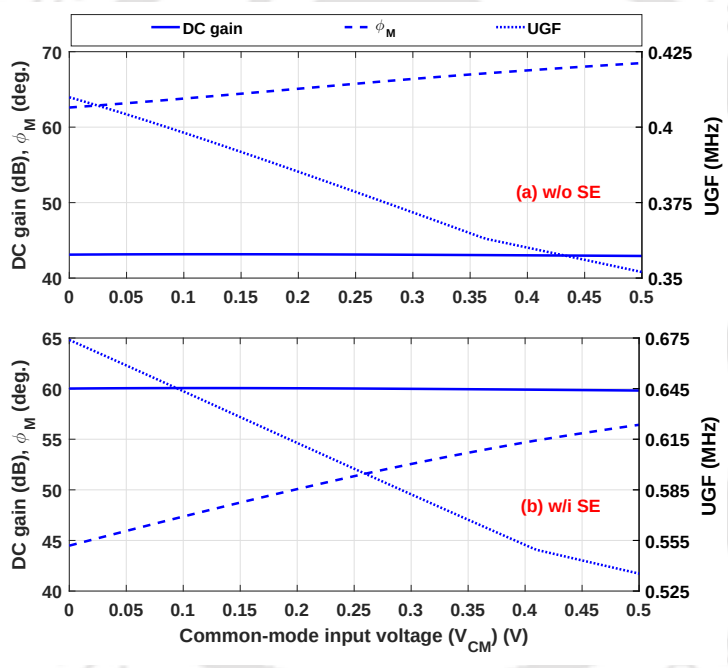


Figure 6.14: DC gain, unity gain frequency and phase margin (ϕ_M) w.r.t common-mode input voltage (V_{CM}).

simulation uses sinusoidal input signal with different common mode voltages levels of 50 mV, 250 mV and 450 mV. Simulation results of the amplifier without and with SE are shown in Fig. 6.15 and Fig. 6.16, respectively. These results represent the rail-to-rail capabilities of the proposed OTAs in time-domain. The amplifier without and with SE in unity gain configuration offer a total harmonic distortion (THD) of -40 dB,-41 dB using 20 kHz, 50 kHz sinusoidal input, respectively. Here, the amplitude of sinusoidal input amplitude is set to 500 mV_{p-p}.

The proposed OTAs can be used as a tunable transconductance amplifier by varying the bias

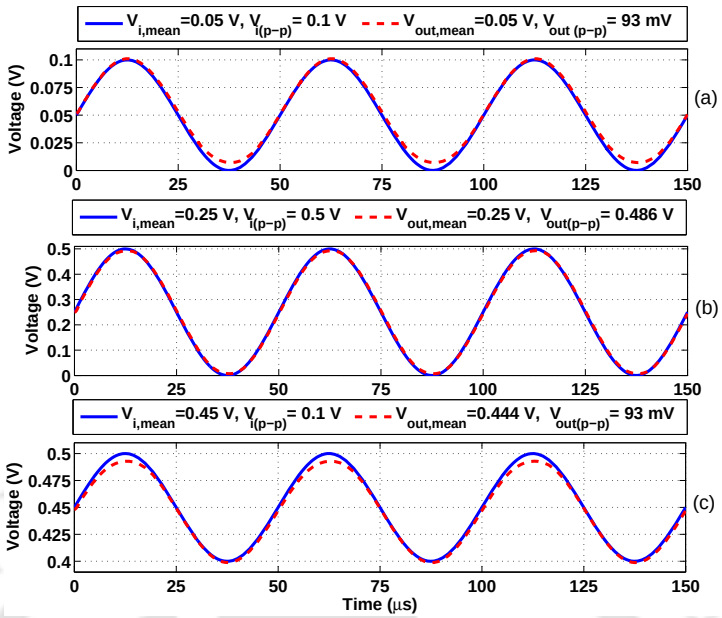


Figure 6.15: Transient response of OTA without SE in unity gain configuration for different common-mode voltage levels (a) V_{CM}=50 mV, (b) V_{CM}=250 mV and (c) V_{CM}=450 mV.

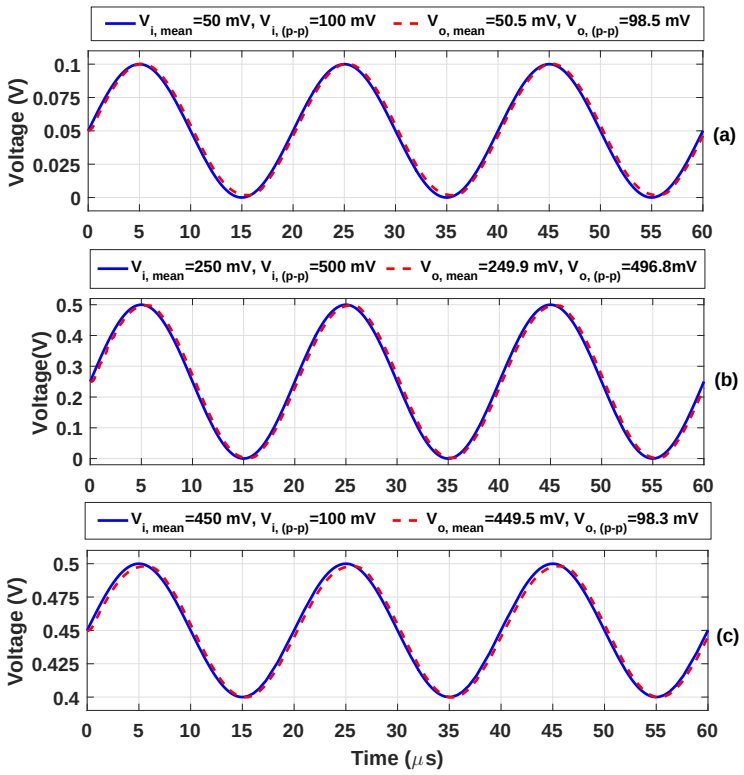


Figure 6.16: Transient response of OTA with SE in unity gain configuration for different common-mode voltage levels (a) V_{CM}=50 mV, (b) V_{CM}=250 mV and (c) V_{CM}=450 mV.

current I_B of input stage. Fig. 6.17 shows the simulation results of the proposed Class-AB bulk-driven OTAs with bias current variation.

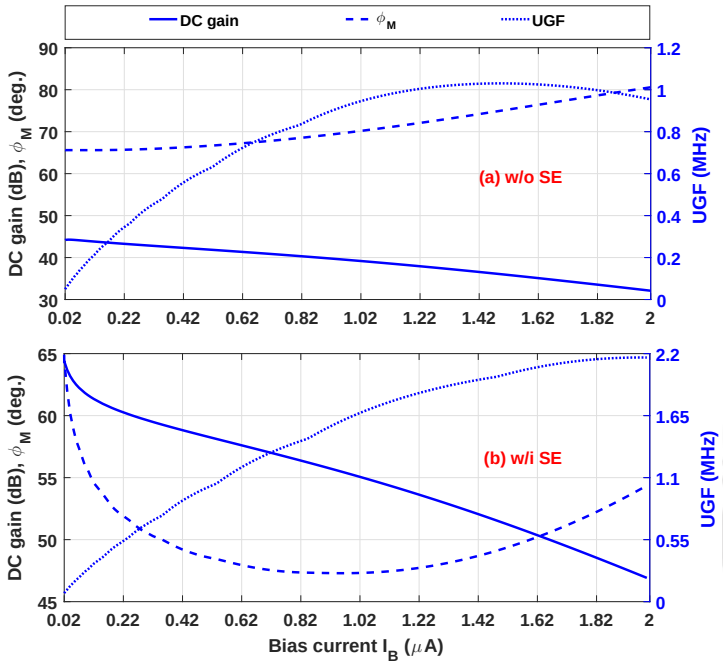


Figure 6.17: The DC-gain, UGF and phase margin of the proposed OTA with and without SE, due to I_B variation.

In order to verify the robustness of the proposed OTAs for process variations, Monte Carlo simulation is performed for 1000 samples. The performance parameters of OTA without and with SE are summarized in Table 6.2 and 6.3, respectively. It can be observed that the parameters are less deviated from the mean value. The DC gain, UGF, phase margin and CMRR histogram plots of OTA without and with SE is shown in Fig. 6.18 and 6.19, respectively.

The robustness of the amplifier against process and temperature variations is investigated using corner simulations at -55°C, 27°C, and 120°C and the results at different corners (SS, TT, FF, SNFP, FNSP) are summarized in Table 6.4 and 6.5. It is clear from Table 6.4 and 6.5 that the proposed amplifiers remain stable across process and temperature variations. The OTA provides a minimum phase margin of 63° without SE and 49° with SE. The remaining performance parameters are insensitive to temperature and corner variations.

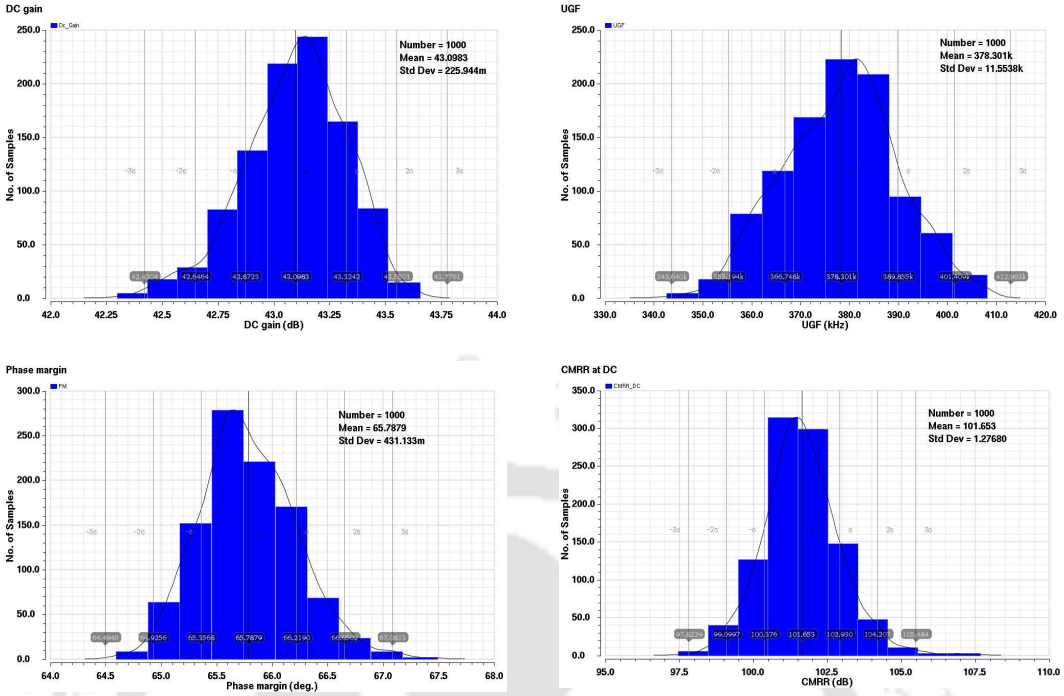


Figure 6.18: Monte Carlo simulation results without slew rate enhancer.

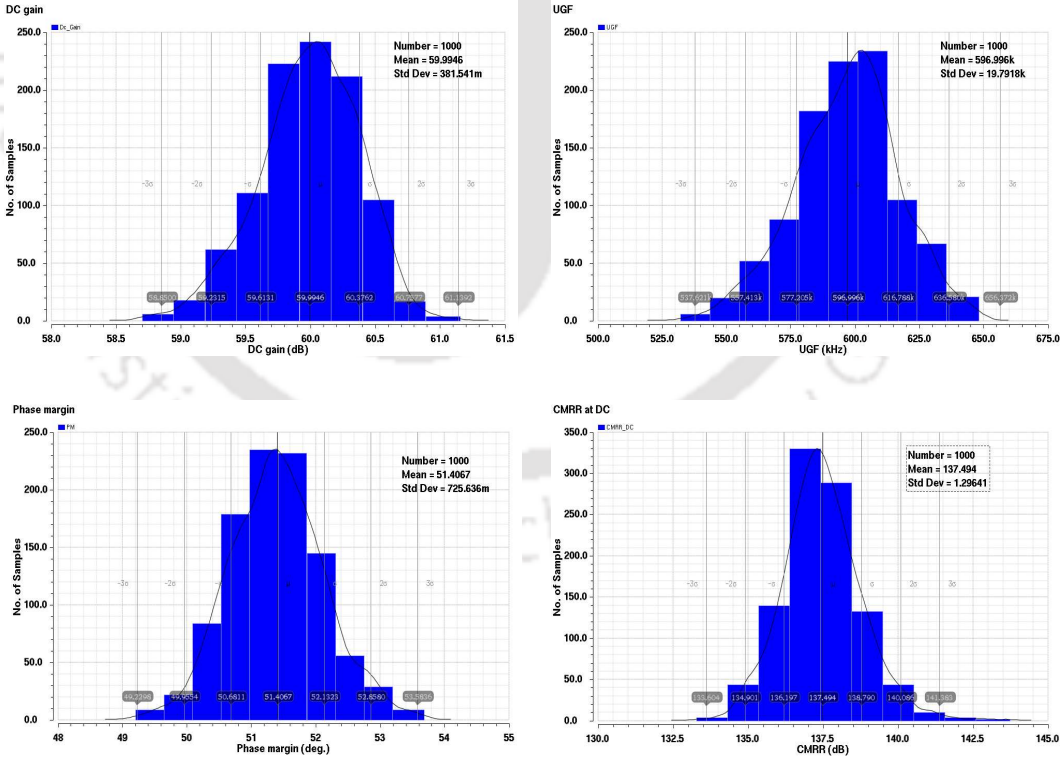


Figure 6.19: Monte Carlo simulation results with slew rate enhancer.

Table 6.2: Simulated results of OTA without SE from Monte Carlo analysis (1000 runs).

Parameter	μ	σ	σ/μ
DC gain (dB)	43	0.23	0.5 %
UGF (kHz)	378	11.5	3 %
Phase margin (deg.)	67.6	0.43	0.6 %
Slew rate (↑)(mV/μs)	94.2	3.2	3.4 %
Slew rate (↓)(mV/μs)	102.2	2.7	2.6 %
t_s^+ (μs)(1%)	6	0.23	3.8 %
t_s^- (μs)(1%)	5.4	0.28	5.2 %
CMRR at DC (dB)	101	1.3	1.3 %
PSRR$^+$ at DC (dB)	44	0.22	0.5 %
PSRR$^-$ at DC (dB)	44	0.22	0.5 %
Noise (nV/$\sqrt{Hz}$)	651	2.3	3.5 %

Note: μ: mean value; σ: standard deviation

Table 6.3: Simulated results of OTA with SE from Monte Carlo analysis (1000 runs).

Parameter	μ	σ	σ/μ
DC gain (dB)	60	0.38	0.64 %
UGF (kHz)	597	19.8	3.3 %
Phase margin (deg.)	51.4	0.72	1.4 %
Slew rate (↑)(V/μs)	0.91	0.078	8.6 %
Slew rate (↓)(V/μs)	0.93	0.023	2.4 %
t_s^+ (μs)(1%)	0.85	0.07	8.2 %
t_s^- (μs) (1%)	0.76	0.05	6.5 %
CMRR at DC (dB)	137	1.3	0.94 %
PSRR$^+$ at DC (dB)	61.1	0.38	0.62 %
PSRR$^-$ at DC (dB)	61.5	0.4	0.65 %
Noise (nV/$\sqrt{Hz}$) at 10 kHz	651	2.27	0.34 %

Note: μ: mean value; σ: standard deviation

Table 6.4: Corner simulation results of the OTA without SE at different temperatures (C_L= 100 pF).

Parameter	Process corner														
	SS			TT			FF			SNFP			FNSP		
Temperature (^{o}C)	-55	27	120	-55	27	120	-55	27	120	-55	27	120	-55	27	120
DC gain (dB)	42	42	39	46	43	38	47	43	35	44	42	37	47	44	38
UGF (kHz)	288	316	307	395	378	345	466	445	352	372	376	338	404	377	328
Phase margin (deg.)	71	68	67	65	66	67	64	65	72	68	67	70	63	64	65
Slew rate(↑)(mV/μs)	69	85	92	83	94	114	104	118	149	86	99	125	80	90	106
Slew rate(↓)(mV/μs)	64	77	96	97	102	117	116	122	160	92	103	128	99	101	111
CMRR at DC (dB)	99	122	86	155	101	76	110	94	64	120	99	69	135	103	81
PSRR$^+$ at DC (dB)	43	43	40	46	44	40	47	44	39	45	43	40	47	44	39
PSRR$^-$ at DC (dB)	44	43	40	48	44	41	49	44	43	47	43	42	49	44	39
$t_s^+(\mu s)$ 1%	8.6	7.2	6.3	6.8	6.1	5	5.6	4.9	3.8	6.5	5.6	4.4	7.1	6.5	5.4
$t_s^-(\mu s)$ 1%	7.7	6.4	5.7	5.8	5.4	5.1	4.8	5.5	3.6	6	5.3	4.4	5.7	5.5	5.3
Noise (nV/$\sqrt{Hz}$) at 10 kHz	0.57	0.66	0.73	0.56	0.651	0.71	0.56	0.64	0.71	0.56	0.65	0.71	0.56	0.65	0.7

Table 6.5: Corner simulation results of the OTA with SE at different temperatures (C_L= 100 pF).

Parameter	Process corner														
	SS			TT			FF			SNFP			FNSP		
Temperature (^{o}C)	-55	27	120	-55	27	120	-55	27	120	-55	27	120	-55	27	120
DC gain (dB)	57.7	57.6	55	63	60	56	65	62	49	61	59	55	63	61	56
UGF (kHz)	490	502	524	610	597	591	720	709	589	607	604	542	608	598	600
Phase margin (deg.)	49	49	50	48	51	57	52	57	64	50	52	61	48	51	54
Slew rate($\uparrow$)(mV/μs)	203	466	705	586	919	1161	998	592	868	476	889	1170	566	853	1093
Slew rate($\downarrow$)(mV/μs)	279	644	829	725	939	842	1154	965	604	545	910	1266	885	940	1439
CMRR at DC (dB)	134	152	121	154	137	110	149	130	67	148	135	104	158	139	115
PSRR$^+$ at DC (dB)	58	59	56	64	61	58	66	63	45	62	60	57	64	62	57
PSRR$^-$ at DC (dB)	60	59	57	65	61	58	68	64	41	64	61	58	66	62	58
$t_s^+(\mu s)$ 1%	2.8	1.4	1	1.1	0.83	0.88	1.1	0.99	0.74	1.3	0.84	0.98	1.2	0.89	0.78
$t_s^-(\mu s)$ 1%	2	1	0.8	0.89	0.78	1.2	0.54	0.88	1.3	1	0.75	1.2	0.8	0.67	0.81
Noise (nV/$\sqrt{Hz}$) at 10 kHz	0.57	0.66	0.73	0.56	0.651	0.71	0.56	0.64	0.71	0.56	0.65	0.71	0.56	0.65	0.7

Layout of Class-AB bulk-driven with adaptive biasing and adaptive loads is shown in Fig. 6.20, occupies an active area of 0.0055 mm^2 (82 μm × 68 μm). The layout of Class-AB bulk-driven OTA with SE is depicted in Fig. 6.21, which occupies an active area of 0.0087 mm^2 (128 μm × 68 μm)

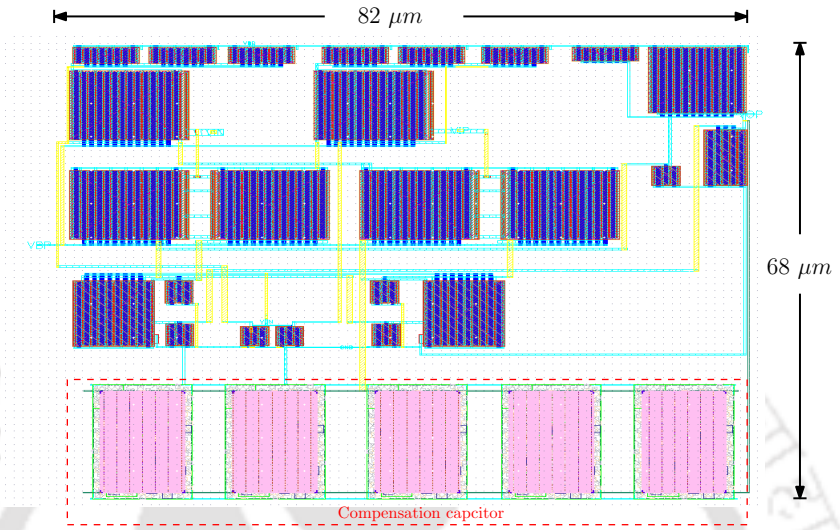


Figure 6.20: Layout of the Class-AB bulk-driven OTA without SE.

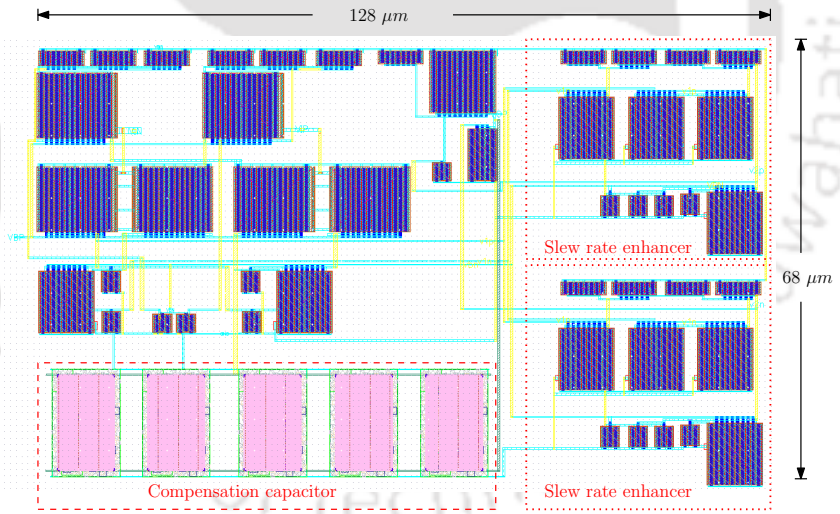


Figure 6.21: Layout of the Class-AB bulk-driven OTA with SE.

6.6 Performance Comparison

The performance of proposed Class-AB bulk-driven OTAs are compared with state-of-the-art sub-1 V designs and various performance parameters are summarized in Table 6.6. In order to show the efficiency of proposed OTAs, the IFOM$_S$, IFOM$_L$, FOM$_{A_V}$ and IFOM$_T$ are calculated.

Table 6.6: Performance summary and comparison with reported works.

Parameter	[76]$^{\otimes}$	[75]$^{\otimes}$	[80]	[42]$^{\otimes}$	[36]	[26]$^{\otimes}$	[40]$^{\otimes}$	**This work**	
								w/o SE (Fig. 6.6)	w/i SE (Fig. 6.7)
CMOS technology	0.5 μm	0.18 μm	0.18 μm	0.35 μm	50 nm	130 nm	0.18 μm	65 nm	
Output type (S/D)	S	D	S	S	D	S	S	S	
Supply (V_{DD}) (V)	$\pm$1	1.8	0.8	0.6	0.4	0.25	0.7	0.5	
Driving method	Gate	Gate	Bulk	Bulk	Bulk	Bulk	Bulk	Bulk	
DC gain (dB)	81.7	72	44.3	73.5	60	60	57.5	43.1	60
UGF (MHz)	4.75	86.5	1.45	0.013	2.2	0.0019	3	0.38	0.6
Phase margin (deg.)	60	50	87	54.1	56	79.2	60	66	51
Slew rate*(V/μs)	8.7	74.1	3.5	0.0147	0.86	0.0007	2.8	0.096	0.93
Output range (V) % of V_{DD}	–	–	–	Rail-to-Rail	–	Rail-to-Rail	0.15-0.7 78.5%	7.5m-492.5m 97%	1.5m-497.5m 99.2%
t_s^* (μs)(to 1%)	0.085	–	0.4	–	–	–	1.15	5.75	0.8
THD**	-24 at 100 1	–	–	-57.7 at 1 0.52	-40 at 1 0.384	-54 at 0.15 –	-54 at 100 0.4	-40 at 20 0.5	-41 at 50 0.5
CMRR at DC (dB)	91	–	–	67.4 at 100 Hz	80 at 5 kHz	–	19	101	137
PSRR$^+$ at DC (dB)	71	–	–	58.1 at 100 Hz	–	–	52.1	44	61
PSRR$^-$ at DC (dB)	79	–	–	–	–	–	66.4	44	61
IRN (nV/$\sqrt{Hz}$) at 100 kHz	49 at 1 MHz	0.8	–	290 at 1 kHz	120 at 10 kHz	3300 at 0.1 kHz	100	651	651
C_L (pF)	70	200	50	15	20	15	20	100	
I_T (μA)	60	6611	62	0.92	60	0.072	36.3	4.25	6.25
Power (μW)	120	11900	49.6	0.55	24	0.018	25.41	2.125	3.125
Area (mm^2)	0.024	0.07	–	–	–	0.06	0.02	0.0055	0.0087
IFOM$_S$	554	262	117	21	73.3	37.5	165	894	960
IFOM$_L$	1015	224	282	24	28.6	13	154	226	1488
FOM$_{A_V}$	22638	10467	6475	2606	11000	9500	13577	77073	115200
IFOM$_T$	443	–	–	41.3	87.2	67.4	189	1430$^{\triangle}$	1536$^{\triangle}$

NOTE: $\otimes$: measurement results; S: single ended, D:differential; w/i: with; w/o: without; –: not reported $*$: average value; $**$: the formate is THD (dB), frequency(kHz), input voltage peak-to-peak(V); $\triangle$: the threshold voltage of nMOS and pMOS transistor is V_{THn} =0.48-V and V_{THp} = -0.32-V.

$\text{IFOM}_S = \text{UGF} \times \frac{C_L}{\text{I}_\text{T}} \left[\frac{\text{MHz}\times\text{pF}}{\mu A}\right] \times 100$; $\text{IFOM}_L = \text{Slew rate} \times \frac{C_L}{\text{I}_\text{T}} \left[\frac{V}{\mu s} \times \frac{\text{pF}}{\mu A}\right] \times 100$;

$\text{FOM}_{A_V} = \text{DC}-\text{gain} \times \frac{\text{UGF}\times\text{C}_\text{L}}{\text{Power}} \left[\frac{\text{dB}\times\text{MHz}\times\text{pF}}{\mu W}\right] \times 100$; $\text{IFOM}_T = \frac{V_{THn}+|V_{THp}|}{V_{DD}} \times \frac{UGF\times C_L}{\text{I}_\text{T}} \left[\frac{\text{MHz}\times\text{pF}}{\mu A}\right] \times 100$

According to FOM, the proposed OTAs outperforms as compared to existing designs which is apparent from Table 6.6. In all cases, the FOM values of the proposed OTA with SE are better than that of existing gate-driven and bulk-driven designs. In particular, the IFOM$_L$ of the proposed OTA with SE is 1488 which is approximately 1.5 times higher than the best existing gate-driven OTA reported in [76]. When compared only with bulk-driven amplifiers, IFOM$_L$ of the proposed OTA with SE is 5 times higher than the best existing design reported in [80].

6.7 Summary

In this chapter, two power-efficient Class-AB bulk-driven OTAs with improved slew rate have been presented. The adaptive biasing and adaptive loads at the input stage enhanced the effective transconductance and slew rate of OTA. In addition, the SE circuit based on current feedback loop further improved the slew rate and settling time significantly. The proposed Class-AB OTA with SE can drive 100 pF and 2000 pF loads with 1% settling times of 0.81 μs and 9.5 μs, respectively. As compared to state-of-the-art designs, the proposed designs provides better FOM and are suitable for low-voltage applications such as LCD column drivers.

7

Conclusions and Future Works

Contents

In this dissertation, the importance of the low-voltage and low-power circuits in battery operated systems is first discussed. Next, the challenges involved in the design of low-voltage circuits in sub-nanometer CMOS technology are described. The literature on low-voltage design techniques has been reviewed. The effects of the scaling of CMOS technology are briefly discussed. Bulk-driven technique has been employed to deal with the harsh voltage swing limitation. But, there are many challenges in sub-nanometer bulk-driven CMOS circuits. To address these challenges, in this thesis, we proposed different OTA topologies for bulk-driven circuits. This chapter summarizes the main contributions of this thesis. A few directions for future research in relation to the main findings are also presented.

7.1 Summary of Contributions

- In advanced CMOS process, the device performance characteristics gets affected by changes in the number of fingers due to STI effect, which in turn changes the circuit performance. A systematic design methodology for designing analog circuits in sub-nanometer CMOS technology has been presented. This methodology is used to evaluate the device geometry by considering the number of fingers. The Miller-compensated two-stage OTA nad bulk-driven current mirror are chosen as example circuits for validation of the proposed methodology.

- A PVT-insensitive bulk-driven OTA with improved DC-gain is presented. The gain of the bulk-driven input stage is improved by use of cross-coupling of bulk-terminal of active load transistors. An additional cross-forward stage assists in increasing the gain of second stage. It also improved the driving capability of OTA without any stability issues. The proposed design is able to drive the capacitive loads of up to 50 pF, with only a small reduction in phase margin.

- An ultra-low-voltage pseudo-differential bulk-driven OTA with rail-to-rail input/output swing is designed for low-frequency applications. An auxiliary circuit is employed to improve the effective transconductance of OTA. A partial positive feedback technique is used to improve the gain. In addition, push-pull output stage is designed through a cross forward stage which improved the current efficiency and gain of the amplifier. Further, a tunable second order $G_m - C$ low pass filter is designed using the proposed OTA.

- Power-efficient bulk-driven Class-AB OTAs with improved slew rate are presented. The proposed designs are suitable for driving the large load capacitance under low-voltage environment. The

slew rate and GBW are improved with help of adaptive biasing, adaptive load and slew rate enhancer circuits. The proposed design with slew rate enhancer can drive the capacitive loads upto 2 nF with rail-to-rail output swing.

7.2 Future Work

There are number of issues which require further investigation in order to enhance the performance of the bulk-driven circuits. A few possible research directions are listed.

- The noise optimization of bulk-driven OTAs is major concern in signal acquisition system for very low-frequency applications.
- The switched capacitor circuits require high gain and less settling time OTAs. Improving the settling time of bulk-driven OTAs under low-voltage environment is one of the future work.
- The proposed Class-AB OTA with slew rate enhancer can be used as error amplifier by incorporating minor changes in compensation scheme, for designing the capacitor-less low-dropout regulators.
- Improving the settling time and noise performance of high slew rate OTAs needs further investigation. Noise and settling time are important parameters for designing the reference buffer of high resolution SAR-ADCs.

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List of Publications

Journal Publications

1. **Harikrsihna Veldandi** and Shaik Rafi Ahamed, "A 0.3-V Pseudo-Differential Bulk-input OTA for Low Frequency Applications," *Circuits, Systems, and Signal Processing, vol. 37, no. 12, pp. 1531-5878, Dec 2018.*

2. **Harikrsihna Veldandi** and Shaik Rafi Ahamed, "Low-Voltage PVT-Insensitive Bulk-Driven OTA with Enhanced DC-gain in 65-nm CMOS process," *AEU - International Journal of Electronics and Communications, vol. 90, pp. 88-96, Apr 2018.*

3. **Harikrsihna Veldandi** and Shaik Rafi Ahamed, "Design Procedure for Multifinger MOSFET Two-stage OTA with Shallow Trench Isolation Effect," *IET Circuits, Devices & Systems, vol. 12, no. 5, pp. 513-522, Sep 2018.*

4. **Harikrsihna Veldandi** and Shaik Rafi Ahamed, "An Ultra-Low-Voltage Bulk-Driven Analog Voltage Buffer with Rail-to-Rail Input/Output Range," *Circuits, Systems, and Signal Processing, vol. 36, no. 12, pp. 4886-4907, Dec 2017.*

Manuscripts Under Review

1. **Harikrsihna Veldandi** and Shaik Rafi Ahamed, "Low-Voltage Bulk-Driven Class-AB OTA with Improved Slew Rate," in *IEEE Transactions on Circuits and Systems II.* ***Status: Revised manuscript resubmitted***

Conference Publications

1. **Harikrsihna Veldandi** and Shaik Rafi Ahamed,"A 1-V High-gain Two-stage Self-cascode Operational Transconductance Amplifier," in *2017 Innovations in Power and Advanced Computing Technologies (i-PACT), Vellore, India, pp. 1-4, April. 2017.*

2. **Harikrsihna Veldandi** and Shaik Rafi Ahamed,"A 0.5 V, 80-nW Pseudo-Differential Two-stage OTA in 0.18 μm CMOS Technology," in *2015 Annual IEEE India Conference (INDICON), New Delhi, India, pp. 1-5 Dec. 2015*