

**MICRO-SCALE POWER MANAGEMENT INTERFACE
CIRCUITS FOR IOT NODE**



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MICRO-SCALE POWER MANAGEMENT INTERFACE CIRCUITS FOR IOT NODE

A

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To
My Parents
My Best Friends and My Guide



DECLARATION

*This is to certify that the thesis entitled “**Micro-Scale Power Management Interface Circuits for IoT Node**”, submitted by me to the Indian Institute of Technology Guwahati for the award of the degree of **Doctor of Philosophy** is a bonafide work carried out by me under the supervision of **Prof. Roy P Paily** . The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.*

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CERTIFICATE

*This is to certify that the this thesis entitled “**Micro-Scale Power Management Interface Circuits for IoT Node**” submitted by **Saroj Mondal (11610219)**, a research scholar in the Department of Electronics and Electrical Engineering, Indian Institute of Technology Guwahati, for the award of degree of **Doctor of Philosophy**, is a record of an original research work carried out by him under my supervision and guidance. The thesis has fulfilled all requirements as per the regulations of the institute and in my opinion has reached the standard needed for submission. The results embodied in this thesis have not been submitted to any other University or Institute for the award of any degree or diploma.*

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Abstract

There is a great interest in powering Internet-of-Things (IoT) nodes by scavenging ambient energy, such as solar radiation, thermal gradient, vibration, or radio frequency (RF) waves. Based on the applications and area of deployment, appropriate energy sources are utilized for powering the wireless-sensor node. As the ambient conditions are changing, one can not directly connect the harvester to the load as the power is not regulated. Moreover, the available scavenged energy may not be sufficient for powering the sensor nodes all the time. Apart from that, unlike a battery, a harvester has a continuous source of power without depletion, but if it is not extracted continuously, the same would be unutilized and lost. Therefore, an interface circuit in between the load and the harvester is needed, in order to maintain regulation both at the input and load.

The first part of this work focuses on the development of on-chip switched capacitor based DC-DC boost converter for micro-scale energy harvesting systems. We present a novel idea of single-phase tree-topology charge pump (SPT-QP), which provides better charge transfer capability, reduced charge sharing time, less complexity, and minimum power transfer loss. A systematic analysis is presented to estimate the optimal parameters for maximizing the system efficiency. The proposed interface circuits have been designed using 0.18- μm CMOS technology node and the circuit simulations demonstrate that the proposed strategy offers peak efficiency 70%, under wide range of light intensities.

The second part of the thesis deals with an on-chip photovoltaic power harvesting system with a low-overhead adaptive maximum power point tracking scheme for IoT nodes. The proposed scheme tracks the maximum power points within 12 μs by utilizing an inherent negative feedback loop, within a tracking error of 0.6%. The tracking range has been improved by $\sim 57\%$ using a current-starved voltage controlled oscillator (CS-VCO) instead of a polynomial VCO. The overhead area and power consumed by this tracking scheme are approximately 0.013% and 0.1%, respectively. Using commercially available solar cell of area 11.3 cm^2 , the proposed system can provide 833 μW of power with a light intensity of 600 lux. The proposed energy

processing circuit has been designed using 0.18- μm CMOS technology node and the circuit simulations demonstrate that the proposed scheme can track maximum power point (MPP) under rapidly changing atmospheric conditions with a peak tracking efficiency of 99%.

The final part of the thesis focuses on improving the overall system efficiency by a suitable architectural change. An efficient power management architecture for solar energy harvesting system is suggested. The proposed architecture utilizes a single DC-DC converter when there is enough ambient energy and two DC-DC converters when there is insufficient ambient energy, to supply the load requirements. By regulating the intermediate voltage, system efficiency has been improved by 9% when two DC-DC converter are used. This work also addresses the start-up issue which is a major bottleneck encountered in any self-powered system. The entire power management system has been designed using 0.18- μm CMOS technology node and the circuit simulations demonstrate that the proposed architectural changes bring in a system efficiency of 82.4% under different light conditions. In addition to that, a hardware setup is created using commercially available ICs and solar cells, in order to validate the proposed power management system. The measurement results indicate that the system is practically realizable.

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List of Acronyms

| | |
|--------|---|
| AFE | Analog Front End |
| BiTe | Bismuth Telluride |
| CBC | Capacitive Boost Converter |
| CCM | Continuous Conduction Mode |
| CL-LDO | Capacitor Less Low Dropout |
| CMOS | Complementary MetalOxideSemiconductor |
| Comp | Comparator |
| CPU | Central Processing Unit |
| CS | Current Sensor |
| CS-VCO | Current-Starved Voltage Control Oscillator |
| CTS | Charge Transfer Switch |
| CU | Control Unit |
| DCM | Discontinuous Conduction Mode |
| DICM | Design Time Component Matching |
| DSP | Digital Signal Processing |
| DVS | Dynamic Voltage Scaling |
| EA | Error Amplifier |
| EEG | Electroencephalography |
| EEPROM | Electrically Erasable Programmable Read-Only Memory |
| e.m.f | Electromotive Force |
| EMI | Electromagnetic Interference |
| FOC | Fractional Open-Circuit Voltage |

| | |
|------------|---|
| FOCV | Fractional Open-Circuit Voltage |
| FSCI | Fractional Short-Circuit Current |
| FOM | Figure of Merit |
| GBW | Gain Bandwidth |
| HC | Hill Climbing |
| IBC | Inductive Boost Converter |
| IC | Integrated Circuit |
| IoT | Internet-of-Things |
| LDO | Low Dropout |
| LDR | Low Dropout Regulator |
| Li-ion | Lithium-Ion |
| LiPON | Lithium Poly Oxide Nitride |
| MC | Monte-Carlo |
| MCU | Micro-Controller Unit |
| μ -Pro | Micro-Processor |
| MOSFET | Metal-Oxide-Semiconductor Field Effect Transistor |
| MPP | Maximum Power Point |
| MPPT | Maximum Power Point Tracking |
| NFC | Negative Feedback Control |
| NiCd | Nickel-Cadmium |
| NMOS | N-type Metal-Oxide-Semiconductor |
| NiMH | Nickelmetal hydride battery |
| OT | Over Temperature |
| OV | Over Voltage |
| PCB | Printed Circuit Board |
| PC | Personal Computer |
| P&O | Perturb and Observe |
| PMOS | P-type Metal-Oxide-Semiconductor |

| | |
|--------|---|
| PS | Photosensors |
| PV | Photovoltaic |
| PV-PC | PV pilot cell |
| P-VCO | Polynomial VCO |
| PZT | Lead Zirconate Titanate |
| QP | Charge Pump |
| RF | Radio Frequency |
| SC | Supercapacitor |
| SoC | System-on-Chip |
| SPL-QP | Single-Phase Liner-topology Charge Pump |
| SPT-QP | Single-Phase Tree-topology Charge Pump |
| TG | Transmission Gate |
| TPT-QP | Two-Phase Tree-Topology Charge Pump |
| UMC | United Microelectronics Corporation |
| UV | Under Voltage |
| VCO | Voltage Controlled Oscillator |
| ZCD | Zero Current Detector |



1

Introduction

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1.1 Introduction

The internet of things (IoT) is the internetworking of physical devices, vehicles, buildings and other items-embedded with electronics, software, sensors, actuators, and network connectivity that enable these objects to collect and exchange data [1]. A typical block diagram of an IoT is shown in Fig. 1.1. It comprises of few sensors for detecting the things of interest, an analog front-end to process and digitize them, a DSP processor to decipher the data, and a transceiver to establish a connection with the local hub, where one can make recommended decisions [2] [3]. Energy efficiency, long operational lifetime, and low cost are the primary design goals of these systems [4]. Over the last decade, extensive research has been carried out to bring down the power consumption of each of these sub-blocks by process scaling, parallelism, and aggressive duty cycling and typical power reduction achieved are listed in Table 1.1. These improvements led these ICs to operate over an year with a 1 cm³ lithium-ion battery, however, such a power reduction is insufficient for cases where the battery replacement/recharge is not possible [5]. Therefore, a system to harvest ambient energy through scavenging techniques is necessary for battery-less operation. This chapter begins with a brief discussion of power management architectures for a battery operated as well as self powered IoT systems and popular energy harvesting sources. Subsequently the thesis organization is presented.

Table 1.1: Power consumption of each of a typical IoT node

| Verma et. al, VLSI-09 [6] | Conventional node for wireless EEG | Recent wireless EEG node with processing capability |
|--------------------------------------|---|--|
| Capturing signals | 75 μ W | 75 μ W |
| Digital processing | - | 2 μ W |
| Radio | 1733 μ W | 43 μ W |
| Total | 1808 μ W | 120 μ W |

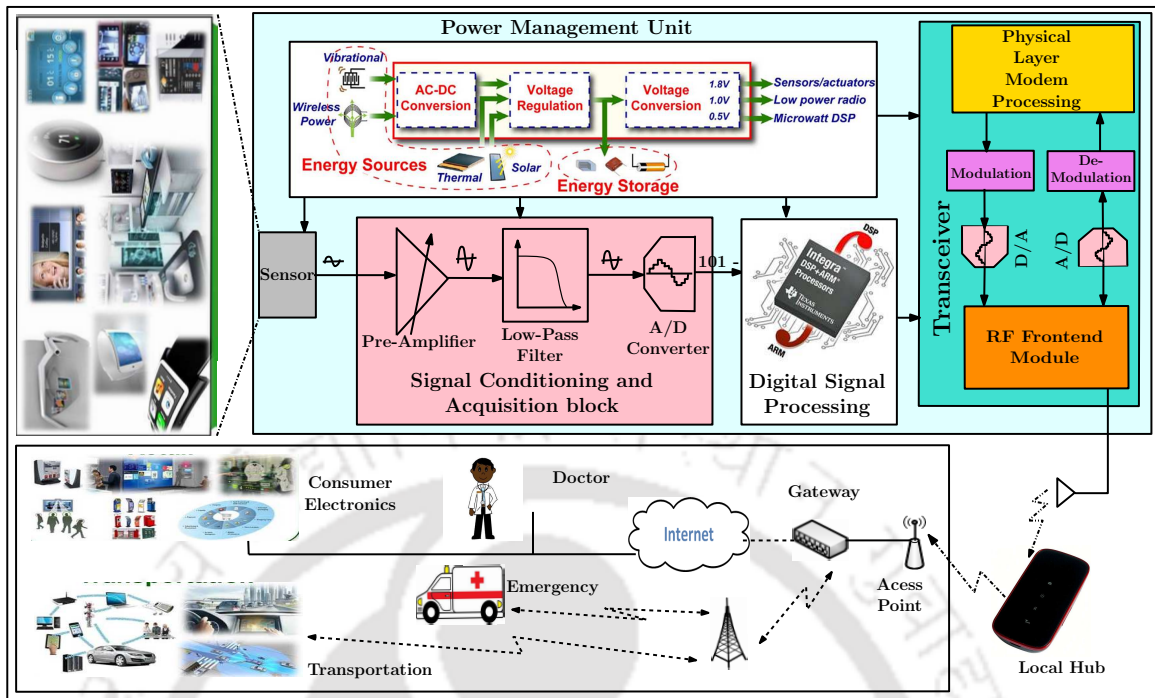


Figure 1.1: Block diagram of a standard IoT node.

1.2 Power Delivery in Portable Systems

Most of the hand-held electronic devices are powered by Li-ion based batteries as they offer higher gravimetric and volumetric energy density compared to other rechargeable batteries, i.e., nickelcadmium (NiCd), nickelmetal hydride (NiMH), etc. Lithium-ion based batteries almost push the physical limits of electro-chemistry and allow smaller and lightweight rechargeable batteries for IoT nodes [4]. However, it shows a wide variation of cell voltages from its nominal voltage during the discharge cycles [7]. This restricts in establishing a direct connection between the load and the battery. Therefore, an intermediate DC-DC converters are essential to maintain regulation at the load irrespective of the variation of cell voltage and the load current. A typical block diagram of a traditional battery operated IoT node is shown in Fig. 1.2.

As the dynamic voltage scaling (DVS) has become an attractive method to minimize the power consumption, multiple voltage regulators are essential to power each of these sub-blocks due to their different functionalities, operating methods, and speed [8]. Traditionally, many used a linear regulator as it offers low cost on-chip solution and provides good transient and

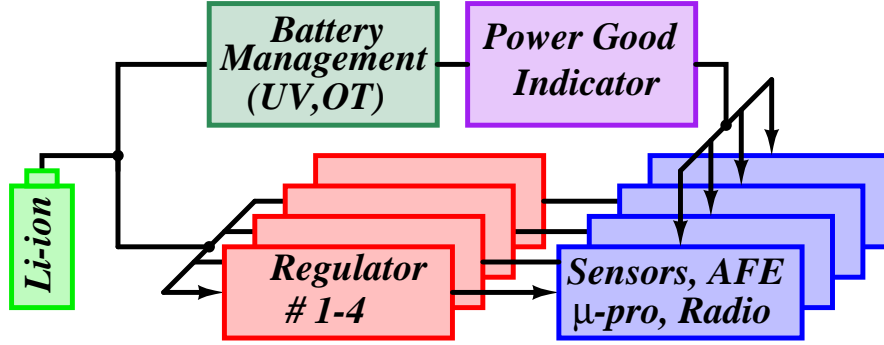


Figure 1.2: Block diagram of a traditional battery operated system.

ripple characteristics [9]. Basically, it controls the resistance of a transistor in order to regulate the output voltage. On the other hand, a switching regulator provides scaled supply voltage without degrading the conversion efficiency. The switching regulator could be inductive [10], capacitive [11] or hybrid combination of these [12]. In order to protect the battery from under-voltage (UV) and over-temperature (OT), a battery management unit is required. A “power good” indicator is also required to inform the load that the battery has enough energy to power load circuits. As the battery is the only energy source, one can shut-down the system when there is no load requirements. Eventually, the system goes in shut-down mode and battery goes into self discharge state.

1.3 Power Delivery in Self-Powered Systems

A typical power management architecture of a self-power IoT or wireless sensor nodes is shown in Fig 1.3. Ambient sources (i.e., light, heat, vibration, or RF wave) are used for powering these nodes, instead of a fixed energy source. Generally, photovoltaic, thermoelectric, and piezoelectric harvesters are used to convert light, heat, and vibrational energy to electrical energy, respectively [13] [14] [15] [16]. The output power of these harvesters are not in a form such that one can directly supply to the load circuits. Therefore, one needs an interface circuit in between harvesters and loads to process output voltages and currents of harvester’s to some usable form for the load circuits. To do so, the converted electrical energy is transferred to a rechargeable battery or a supercapacitor using a boost charger and then the storage energy is

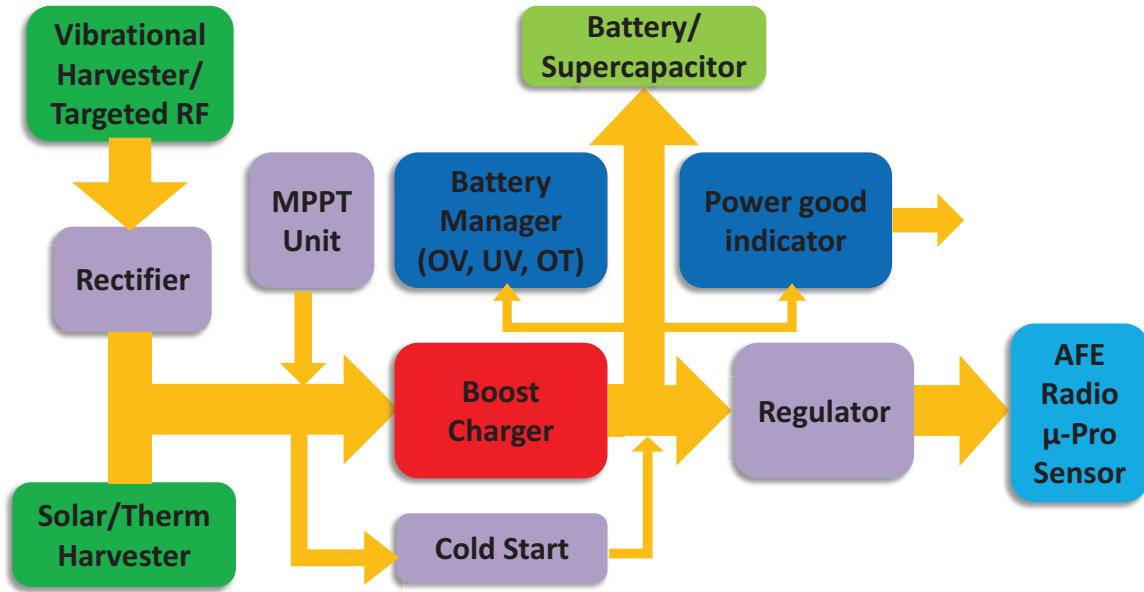


Figure 1.3: Power management architecture of a self-powered IoT node.

transferred to the respective loads through different gain setting regulators. The AC harvesters such as vibrational and targeted RF, need a rectifier circuit to convert AC output into a DC voltage. In comparison with battery operated system, a self-powered system not only needs under voltage (UV) and over temperature (OT) protection, but also needs over voltage (OV) protection circuit. A cold start block is also needed to bring-up the system from the sleep-state to an active-state when the harvester output voltage is lower than the MOSFET threshold voltage. Unlike a battery, the harvester is an unlimited power source, and if one does not extract the power all the time, the same would be lost. Therefore, to extract the maximum power from the harvester, one has to offer optimal impedances dynamically, and to do that one needs a maximum power point tracking (MPPT) block. Next sub-section will discuss about popular energy sources.

1.3.1 Scavenging Light Energy

One of the easiest way to harvest energy is to do it from the ambient light energy. When light imping between the junctions of n-type and p-type semiconducting materials, photons with enough energy will break the electron hole pair which subsequently will be separated by the

internal electric field into the n-doped and p-doped materials, respectively. Due to these excess electrons and holes, the system will fall into an imbalance state as the internal electric field does not allow recombination. Now, if one connects these two materials using an external cable, the excess carrier, electrons and holes, will start flowing by generating a current, which is nothing but short circuit current $I_{PH,SC}$ as shown in Fig. 1.4. The short circuit current is proportional to the amount of irradiation impinging on the solar cell. Commercially available micro-scale solar cells may be based on crystalline, amorphous, or dye-sensitized semiconductors. Each cell has its own advantages: crystalline is quite efficient in outdoor light condition, however, not so efficient in indoor situation. Whereas, amorphous or dye-sensitized shows much better conversion efficiency in indoor situation, and offers a conversion efficiency of 15 – 20%. The typical power density varies from $10\mu\text{W}/\text{cm}^2$ to $10\text{mW}/\text{cm}^2$ under indoor and outdoor light conditions, respectively.

The electrical equivalent model of a PV cell and its $I - V$, $P - V$ characteristics are shown in Fig. 1.4. The equivalent electrical model is composed of a current source $I_{PH,SC}$, forward biased diode D_{PV} , parasitic series resistance R_S , and equivalent shunt resistance, R_{SH} . $I_{PH,SC}$, represents the illumination level, R_S represents finite conductance of the material and contact resistance, and R_{SH} represents the microscopic defect in solar cell, which provides an alternative path for the generated photocurrent. Ideally, R_S should be zero and R_{SH} should be infinite. However, in reality there is some non-zero series resistance and finite shunt resistance, which reduces the conversion efficiency of the solar cell. I_{PH} , V_{PH} , and P_{PH} represent the PV cell output current, voltage, and power, respectively. From the PV cell power voltage characteristics it is evident that, the amount of extractable power depends on cell voltage, V_{PH} , and one can extract the maximum power by setting the PV cell voltage to the maximum power point (MPP) voltage, i.e., $V_{PH} = V_{MPP}$. Typically, mini-solar panel [17] (1 or 2 in series) offers open circuit voltage of 200 – 900 mV and maximum output power of 0.5 – 4 mW with a variation of ambient light intensities from 500 – 2000 lux.

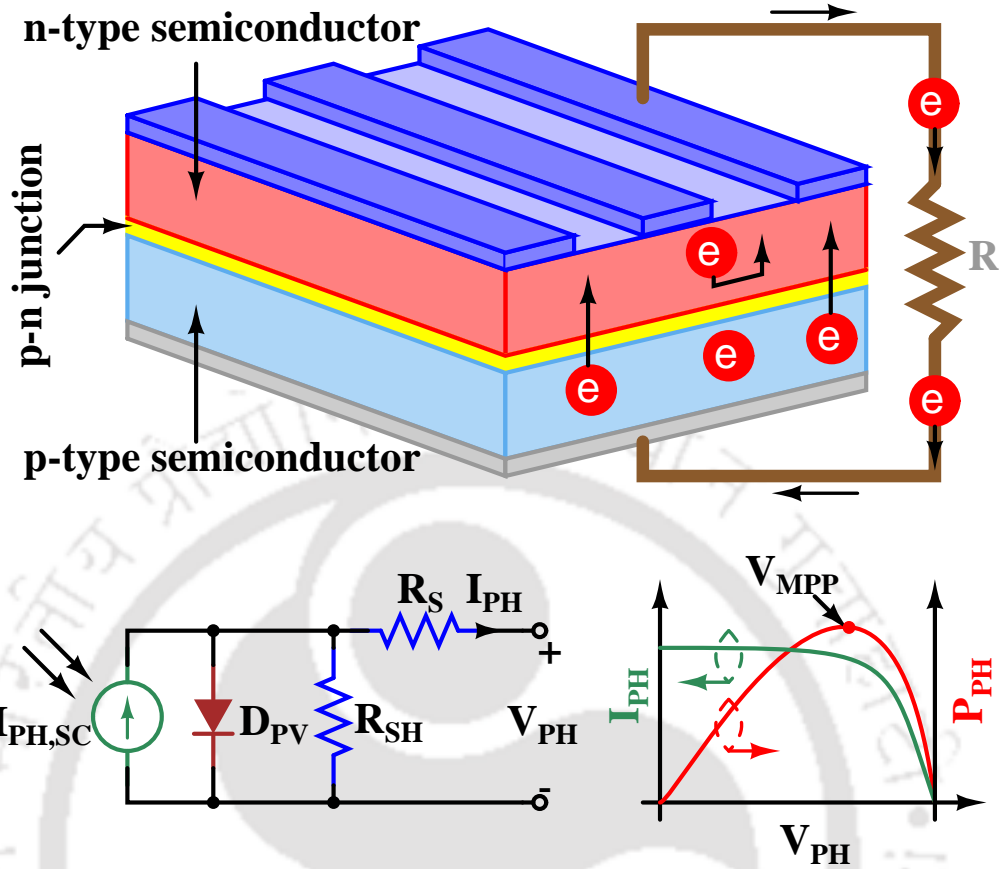


Figure 1.4: Electrical model of a photovoltaic cell and its $I - V$, $P - V$ characteristics.

1.3.2 Scavenging Heat Energy

A thermoelectric harvester converts the heat energy in the form of temperature gradient into electrical energy and vice-versa [10]. The physics involved in thermoelectric harvester is the Seebeck effect and it can be illustrated by a thermocouple. Generally, thermocouple is made up with a p-type and n-type materials and connected electrically in series but thermally in parallel as shown in Fig. 1.5. When there exists a temperature difference across this material, heat begins to flow from hotter to the cooler side by transferring excess electron and hole in the n-side and in p-side, respectively. Now, if one closes the circuit, current begins to flow and a voltage is developed across the thermocouple which is proportional to the temperature gradient (ΔT) applied across the thermoelectric element. Therefore, one can model it electrically by considering a voltage source, V_T , in series with a resistance, R_{TH} , as shown in Fig. 1.5. The

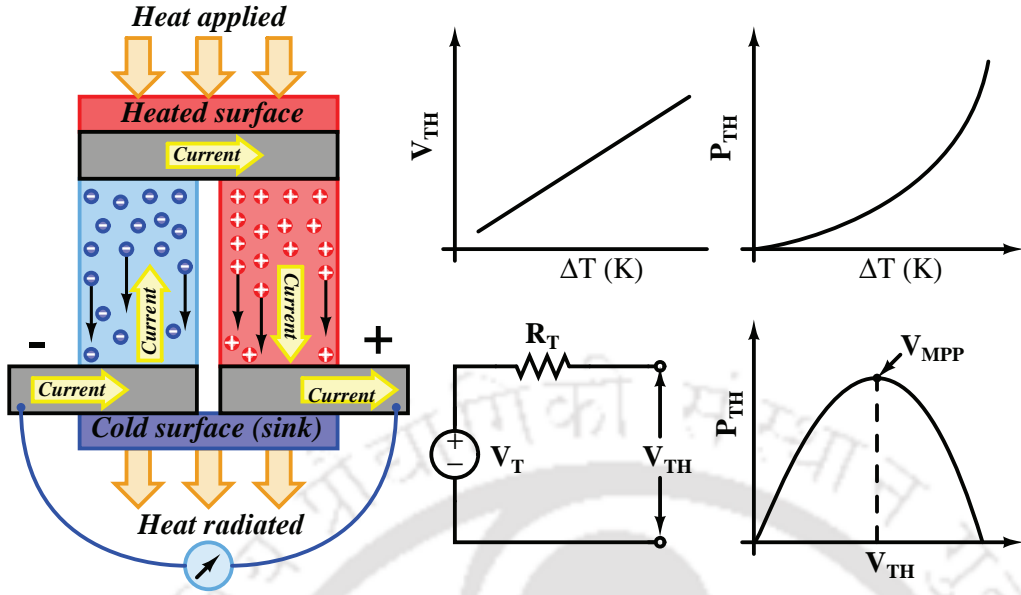


Figure 1.5: Micro-thermoelectric generator and its electrical model, $V - \Delta T$, $P - \Delta T$, and $P - V$ characteristics.

open circuit voltage, V_T , can be expressed as $S \cdot \Delta T$, where S is the seebeck coefficient and ΔT is the temperature difference applied across the thermocouple. The resistor, R_{TH} , represents the resistance offered by metal interconnection and attached surface pellets. The variation of output voltage, V_{TH} , and output power, P_{TH} , with respect to ΔT and the variation of output power with respect to open circuit voltage are also shown in Figure 1.5. As the internal impedance is modeled by a resistor, a one-time impedance matching circuit is required to extract the maximum power from the thermoelectric harvester. Therefore, there is no tracking mechanism involved to extract the maximum power.

Typically, a thermocouple generates very little amount of voltage in the order of $200 \mu V$ per kelvin (K). Therefore, to build up higher voltages, many such cells are placed electrically in series and thermally in parallel as shown in Fig. 1.6. The typical power density achieved is $40 - 60 \mu W/cm^3$ for wearable applications and $2.5 - 5.0 mW/cm^3$ for industrial applications with a temperature difference of $2 - 3 K$ and $9 - 10 K$, respectively.

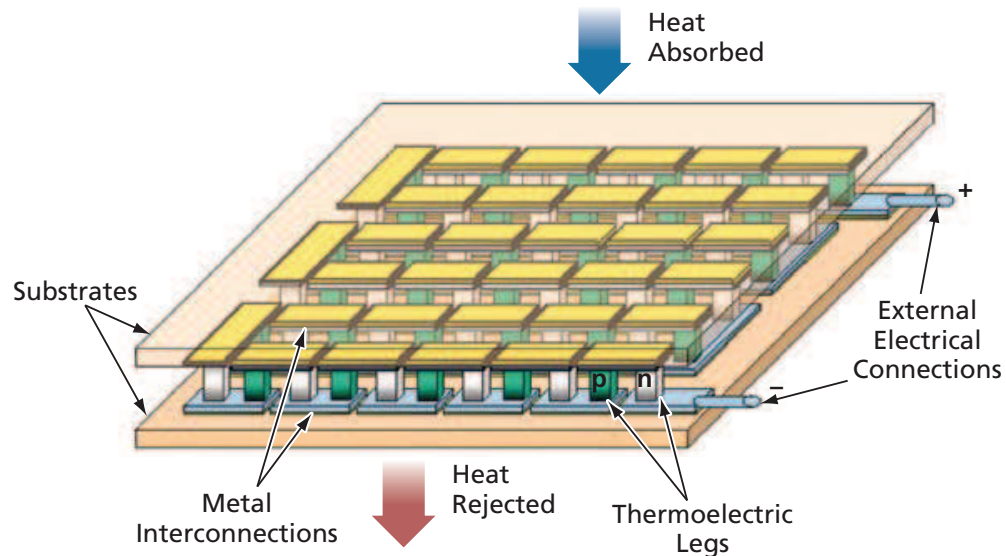


Figure 1.6: A typical thermoelectric generator [18].

1.3.3 Scavenging Vibrational Energy

Another way to get the energy is from ambient mechanical vibration. Generally, vibrational harvesters are broadly classified into two categories, electromagnetic vibration systems and piezoelectric vibration systems. In an electromagnetic vibration system, a mass allotted to a coil swings between a permanent magnetic field and produces electromotive force (e.m.f) proportional to the strength of the magnetic field, number of turns of the coil, and the velocity of the relative motion. The physics involved in this process is the Faraday's Law. On the contrary, in a piezoelectric vibration system, a mechanical strain is applied to a piezoelectric device, which deforms the structure and is converted to electrical energy proportional to the applied strain. A basic representation of piezoelectric harvester and its electrical model with output power voltage characteristic are shown in Fig. 1.7. The sinusoidal current source is modeled by assuming that the input vibrations are sinusoidal in nature. C_P and R_P represent the plate capacitance and the resistance of the piezoelectric material, respectively. Unlike other harvesters, piezoelectric harvester has higher internal impedance and results in a lower output current and a higher output voltage. As the harvester outputs are sinusoidal in nature, it demands a rectifying circuits before feeding it to the load circuits. In this regard, a full-

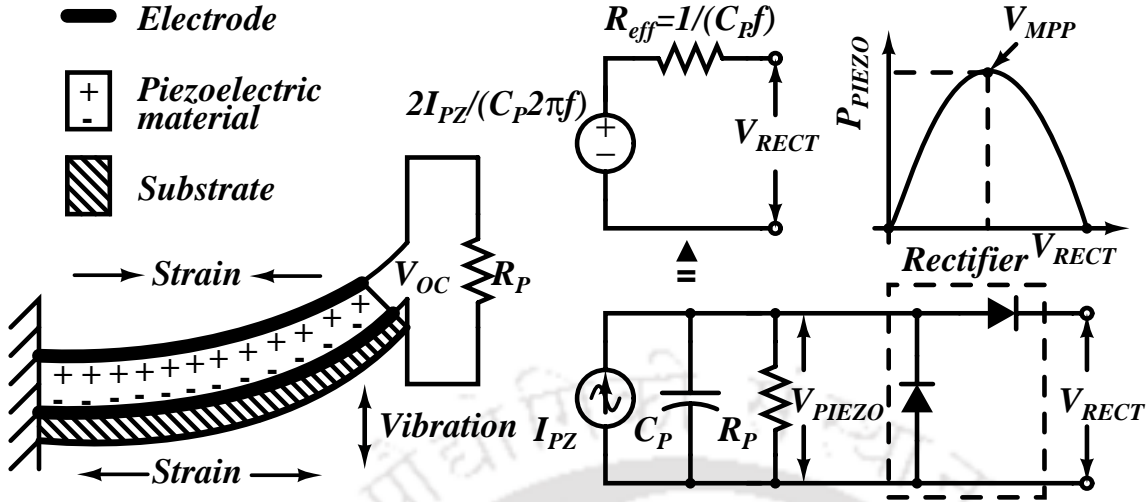


Figure 1.7: Basic model of piezoelectric energy harvester and its electrical equivalent model with P-V characteristic

bridge rectifier or a voltage doubler are commonly used as rectifier circuit to convert the AC voltage to DC voltage. Even in the presence of diode non-idealities, voltage doubler usually provides higher output power in comparison to a full-bridge rectifier [19]. The typical vibration bandwidth of wearable and industrial settings are varied between 1 – 2 Hz and 50 – 60 Hz, respectively. Therefore, systems which give typical power density in micro-watt will be useful for wearable applications, and typical power density of several milliwatts will be suitable for industrial applications. As the internal impedance of this harvester is fixed like a thermoelectric harvester, one does not require any tracking mechanism for extracting maximum power out of this harvester. Table 1.2 summarizes the requirements of solar, thermal, and vibrational harvesters.

1.4 Energy Storage Options for Portable Systems

Typically, in an indoor situation one can get few tens of microwatts of power from the harvester, whereas in an industrial or bright sunlight condition, one could expect few milliwatts of power per centimeter square or cube, depending upon the type of the harvester. Once the energy is taken out from the harvester it can be stored in a rechargeable battery or a super capacitor before powering to the load.

Table 1.2: Comparison of Solar, Thermal, and Vibrational Harvesters

| Parameters | Materials and size | Ambient conditions | Harvested [¶] voltage | Output [‡] impedance | Output power | Tracking required? |
|-------------------------|-------------------------------|-----------------------------------|--------------------------------|-------------------------------|----------------|--------------------|
| Solar [17] | Silicon, 11.3 cm ² | 500-2k lux | 300-800 mV | 0.05-2 k Ω | 0.5-4 mW | Yes |
| Thermal [20] | BiTe, 50 cm ² | 2-9 K | 50-300 mV | 5-10 Ω | 50-500 μ W | No [#] |
| Vibrational [21] | PZT, 1 cm ³ * | 2.5 ms ⁻² , 120-225 Hz | 2.4-3.2 V | 10-150 k Ω | 335 μ W | No [#] |

*: cantilever length varied from 9-25 millimeters; [¶]: open circuit voltages are given, but it will be lowered during closed circuit operation; [‡]: matched impedance needed to be present for optimal power transfer; [#]: one time setting.

1.4.1 Why Do We Need a Storage Unit?

Most of the IoT systems are heavily duty cycled to reduce the overall power consumption and to make it self-power alive. The typical input-output power characteristics of the sensor nodes and their differences are shown in Fig. 1.8. The curve in red color indicates the power consumption of the sensor node for processing and transmitting the sensed data. The peak of the red curve represents waking-up of the sensor node for transmitting the data and it is very intermittent in nature. Whereas, the green curve shows the average power available from a solar cell to power the load. It is clear from the figure that the average input power of the sensor node is not sufficient during waking-up of the sensor node. So, one can not connect the solar cell directly to the load circuit. Therefore, one needs a storage unit in order to match the input and output power needed. The storage unit accumulates all the energy when the sensor node is in sleep state and delivers to the load when it is demanded. The characteristic of the storage is shown in blue color curve. So, it essentially smoothens the functionality of the sensor node. The typical characteristic of an energy buffer should therefore be: i) how much energy it can store for a given FOM (figure of merit) factor, ii) whether it can supply the load when there is demand, and iii) it should have very low self-discharge rate.

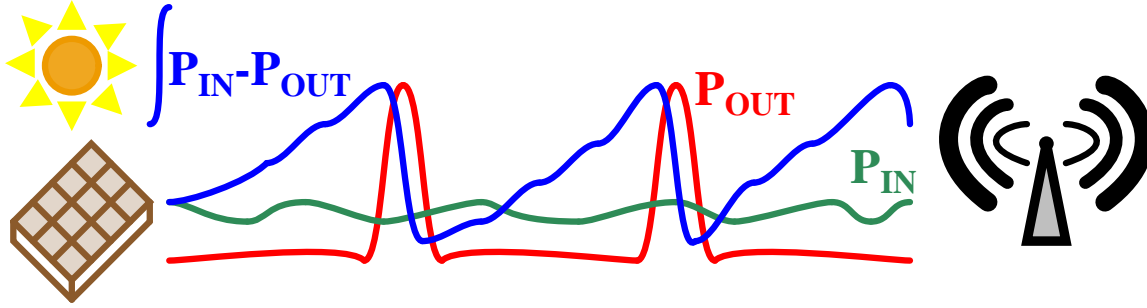


Figure 1.8: Input power and output power characteristic of a sensor node.

1.4.2 Conventional Batteries

Conventional batteries, like AA or AAA (NiCd, NiMH), offer high capacity, 0.3–2500 *mAH*, and low internal impedance. Due to low internal impedance, they can deliver even few hundred *mA* of load current. However, they have high self-discharge rate compared to others batteries. On the contrary, coin-cells have low charge storage capacity and high internal impedance. As the internal impedance is high, it cannot deliver sufficient amount of current to the load. In order to enhance the current one needs to store much energy by using a decoupling capacitor connected parallel to the coin cell. Moreover, the conventional batteries have very limited recharge cycles, say few hundreds, as they lose their capacity with repeated recharge cycles.

1.4.3 Thin Film Batteries

As conventional batteries suffer with high self-discharge rate and limited period recharge cycles, thin-film batteries offer very low self-discharge rate and higher recharge cycles. Generally, thin-film batteries are made up of lithium poly oxide nitride (LiPON), a solid-state electrolyte, which has very low self-discharge rate of, 1 – 2% over a year, and higher rechargeable cycles upto, 5K-10K. Apart from that, they have high internal impedance and low storage capacity like 2 – 3 *mAH*, and can deliver 30 – 40 *mA* of load current. Therefore, thin-film batteries could be a good candidate for IoT application.

1.4.4 Supercapacitor

Supercapacitor is another alternative for the temporary storage of harvested energy. As its energy is not chemically stored, it has millions of recharge cycles and is able to deliver as much as power demanded by the load. However, it has very high self-discharge rate and poor charge storage capacity of 10 – 100 μ AH. Recently, many are using thin-film batteries along with small supercapacitors in order to combine the benefits of both, so that one can deliver as much power as demanded by load while keeping their self-discharge minimum.

1.5 Motivation for this Work

Harvesting energy from ambient sources (i.e., vibration, heat, light, or RF) or bio-potential inside mammals (Endo-Cochlear Potential [3]) has become an attractive and promising option for powering up the chips. Extracting the maximum energy, with minimum loss, from an energy harvesting sources is one of the primary design goal of an energy processing circuit, and to realize it, an optimized energy processing circuitry is required. Moreover, the energy processing circuits should be stable with respect to the source and load variations [5]. In summary, functions expected from an interface circuit are as follows:

- Provide a clean regulated supply to the load circuits.
- Maintain regulation if there is an instantaneous change in ambient conditions and/or in load requirements.
- Maintain regulation even if there is not enough ambient conditions to meet the demand of the load for a small period of time.
- Offer optimal impedance dynamically to the harvester such that it can deliver maximum power to the interface circuit all the time.
- Boost the harvested voltage when it is less than the required load voltage, to such an extent that it can meet the load requirements.

- Bring-up the system from the sleep-state to an active-state if the harvester output voltage is much lower than the MOSFET threshold voltage.

Extensive research has been carried out by the industry and academia and a number of articles have been reported on micro-scale energy processing circuits [22, 23, 4, 24, 25, 26]. The energy transfer capability of an energy processing circuit depends on its implementation technology, architecture and circuit topology, input and output voltages, and device sizes [24]. Therefore, design of an efficient on-chip miniaturized low power energy processing circuit for all conceivable electronic applications is a key and active research area of micro-scale energy harvesting system. Traditionally, high efficiency and small form factor have been achieved by utilizing the superior semiconductor and magnetic components. However, the role of a control circuit in achieving high efficiency and small form factor need to be studied in detail while designing a power converter.

1.6 Problem Definition

The task of an energy processing circuit is not only to provide desired voltage or current for the load circuit but also to account the source characteristic, load variation, and environmental changes such that overall system energy can be optimized [5]. Apart from that, minimizing the number of external components and making it completely system-on-chip is highly desirable in autonomous wireless micro-sensor nodes and biomedical implants. Moreover, individual block level improvements will give some benefits but to get the full advantage from a system level perspective, one has to make reforms at architectural level. Therefore, this thesis aims to address the following specific aspects of an interfacing circuit which connects a solar energy harvester to an IoT node.

- Design complete on-chip, inductor-less, high-frequency switching power converters for micro-scale energy transducer.
- Improvement of charge transfer capability and charge sharing time.
- Estimation of optimal parameters for maximizing the system efficiency.

- Proposal of low-overhead adaptive maximum power point tracking (MPPT) scheme for micro-scale solar energy harvesting system.
- Reduction of hardware cost without compromising the performance of energy processing circuit.
- Proposal of an efficient architecture to improve end-to-end efficiency of the energy processing circuit.

1.7 Thesis Contributions and Chapter Organization

This thesis contributes to the power management interface circuits, starting with a novel DC-DC converter block design and finally, a new switched capacitor based power management architecture where multiple blocks are involved.

Chapter 2

This chapter deals with different topologies of on-chip DC-DC converter for portable electronics. Basic configurations of converters available in literature are reviewed based on their topologies. The major design considerations are discussed and suggestions are made about which topology is preferred for a specific application. Analytical expressions and analysis are presented in order to get a clear understanding of their dynamics and behavior. A detailed state-of-the-art review of the important regulators are reported.

Chapter 3

This chapter deals with an on-chip inductor-less switching power converter for micro scale energy transducer. A novel single-phase tree-topology charge pump (SPT-QP) circuit, which has better charge transfer capability, reduced charge sharing time, less complexity, and minimum power transfer loss is presented. Analytical modeling is also carried out to estimate the optimal parameters for maximizing the system efficiency. The proposed interface circuits have been designed using 0.18- μm CMOS technology node and the circuit simulations demonstrate that the proposed strategy offers a system efficiency of 70%, under different light conditions.

Chapter 4

This chapter deals with on-chip photovoltaic power harvesting system with low-overhead adaptive maximum power point tracking (MPPT) scheme for μ -scale photovoltaic harvester. A discussion among many reports related to maximum power point tracking scheme that are suitable for micro-scale energy harvesting system is given. This is followed by a description of the proposed power management system and detailed circuit implementation. The concept behind inherent negative feedback based MPPT scheme is also presented. An analytical model is developed to quantify the proposed idea and to optimize the MPPT circuit accordingly. Measurement and simulation results are combined to illustrate the MPPT circuit functioning.

Chapter 5

This chapter starts with a discussion of previously reported works which are suitable for micro-scale energy harvesting systems and finally presents an efficient on-chip power management architecture for solar energy harvesting system. The architecture utilizes single DC-DC converter to maintain regulation at the load, when there is not enough ambient condition to supply load requirements. This chapter also addresses the start-up issue which is a major bottleneck encountered by any self-powered system. Using commercially available ICs and solar energy harvesters, a hardware setup is created to validate a micro-scale power management system. The measurement results indicate that the system is practically realizable.

Chapter 6

This last chapter provides major conclusions of the work done and suggests some of the open problems related to possible future research.

2

On-Chip DC-DC Converters

Contents

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2.1 Introduction

Due to the advancement of micro-electronic technology, sophisticated electronic devices have fulfilled the demand of wider functional capability, multiple connectivity (wired/wireless) options, several digital/analog interfaces, larger data storage capacity, and higher signal processing capability. Incorporation of analog and RF capabilities along with these features in a same die, enhances the system functionality at minimum power, cost, and footprint, and provides us a system-on-chip (SoC) solutions. However, the presence of different functionalities in a single SoC, demands large number of independent and well-isolated power supplies from a single energy source. In a typical mixed-signal SoC, there could be 30 isolated power domains for analog and RF blocks [27]. Therefore, generating energy efficient multiple independent power supplies from a single energy source is a key research area in the power management ICs.

In order to get many independent power supplies from a single energy source, regulators are essential to meet scaled voltages to the respective loads. Moreover, the influence of the large voltage variation at the input must be reduced to more acceptable levels. Fundamentally, there are two methods for generating independent regulated power supply from an energy source, like a battery: linear regulator and switching regulator [28], [29]. Linear regulators are widely preferred over switching regulator as they consume less area, avoid external passive components (capacitor/inductor), have less number of pad/pins, and provide on-chip solution [30]. However, they are able to produce a lower regulated voltage only from a higher non-regulated input voltage. Apart from that, they offer poor power conversion efficiency especially when the regulated voltage goes farther away from the input voltage. On the contrary, switching regulator offers higher conversion efficiency, $\sim 80-95\%$, and provides output voltage several times higher or lower than the input supply voltage. However, it requires multiple off-chip components (inductor/capacitor) and hence large number of package pins/pads, which practically allows only for few independent power supplies in a given SoC application. Nevertheless, there are some applications where high output voltage is required to power up the noise sensitive circuits. In such applications, a switching regulator is used to provide higher output voltage and a linear

regulator is used to provide low noise output voltage. In summary, both linear and switching regulators have their places in today's market and there is a great demand for efficient on-chip regulators in a mixed-signal SoC.

2.2 Linear Regulators

Basically, a linear regulator consists of a reference generator associated with a start-up circuit, a protection circuit associated along with a current sense element, an error amplifier (EA), a pass element, and a feedback network as illustrated in Fig. 2.1. The reference generator is a bandgap reference and provides a stable dc bias voltage with limited current driving capabilities, whereas the protection circuitry ensures its stability during the load current variations [28]. In order to regulate the output voltage, it essentially controls the resistance of the pass element by comparing the sampled output voltage with a reference voltage. The regulating performance can be measured by key design considerations: stability at a very light load condition, line/load regulation, line/load transient, and power supply rejection ratio [9]. The number of pass elements and their type entirely depend on the design specification and the applications [31]. If it is an NMOS transistor, one could expect good transient and ripple behavior as the source is connected to the load terminal and drain is connected to the supply terminal. However, the conversion efficiency will be poor as the load voltage goes farther away from the input voltage. On the contrary, if it is a PMOS transistor, one could expect better conversion efficiency as the dropout voltage is lower compared to the former. However, the transient and ripple behavior show poor performance compared to the former case [28]. Let us take an example in $0.18 \mu\text{m}$ technology node, where the supply, threshold and overdrive voltages are 1.8 V, 500 mV (with non-zero body-bias), and 200 mV, respectively. The maximum conversion efficiency one may achieved 50% and 88% if the pass element is either an NMOS transistor or a PMOS transistor, respectively, and assumed losses are negligible compared to the load current. Therefore, PMOS based linear regulators are accepted for battery operated electronic devices, and it plays a critical role in determining the operation lifetime of a battery. The PMOS based linear regulators are widely referred in literature as low dropout (LDO) regulator (LDR) [32].

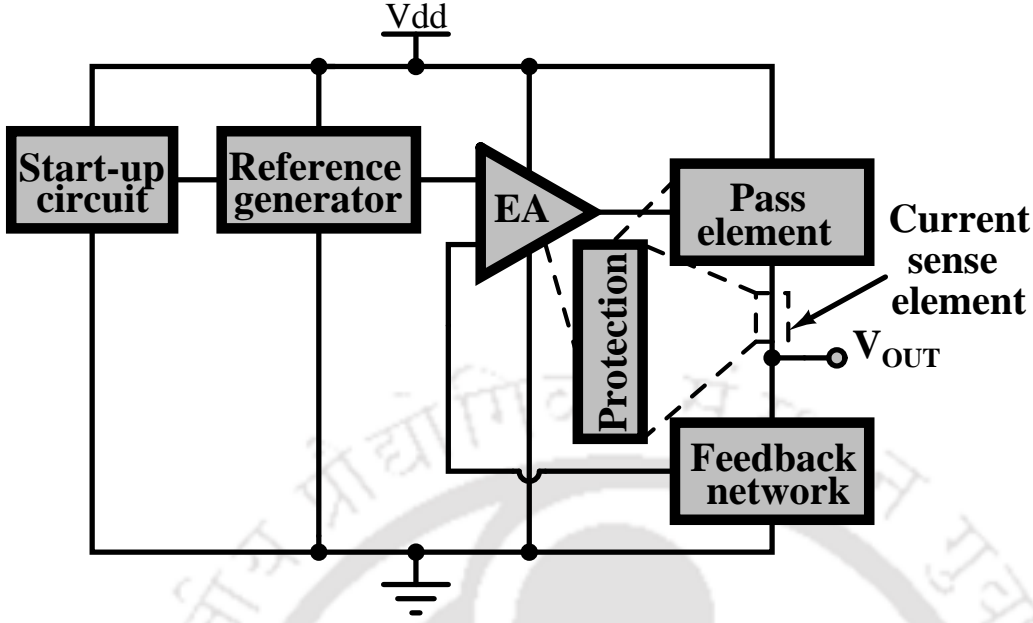


Figure 2.1: Block diagram of a generic series regulator

2.2.1 LDO Regulator

The circuit diagram of an on-chip LDO regulator is shown in Fig. 2.2. To achieve the stability and good transient behavior, usually a very large value off-chip load capacitor C_L , in the order of several micro-farads is used [33]. However, this large capacitor can not be realized in current technology nodes, so one needs an external pin for mounting this load capacitor with regulator. To overcome this issue, an on-chip capacitor in the order of tens of picofarad, has been incorporated instead of an off-chip capacitor and such a scheme is widely known as capacitorless LDO (CL-LDO) regulator [34, 35]. Due to this on-chip capacitor, stability has been degraded as there will be several poles present even before the unity gain frequency. Among these uncompensated poles two are major: one at the output of the error amplifier, ω_{P1} , which is the dominant one, and another is at the load terminal, ω_{P0} , as shown in Fig. 2.2. The capacitor C_1 represents $C_{gs} + C_{gb}$ of the pass transistor and capacitor C_2 represents $C_{gd} + C_m$, where C_{gs} , C_{gb} , and C_{gd} are gate to source capacitance, gate to body capacitance, and gate to drain capacitance of the pass transistor, respectively, whereas C_m is the miller-compensation capacitance. Generally, the pass transistor M_P is very large in order to drive a high load current

and to reduce V_{DSAT} , therefore, C_{gs} and C_{gd} are in the range of 60 – 80 pF and 10 – 20 pF, respectively [35]. So, the location of poles of a CL-LDO regulator are given by:

$$\omega_{P1} = \frac{g_{o,EA}}{(C_1 + (1 + A_P) C_2)} \quad (2.1)$$

$$\omega_{P0} = \frac{g_{out}}{C_L} \quad (2.2)$$

where $g_{out} = g_{ds} + g_L + g_\beta$, $g_L = \frac{1}{R_L}$, $g_\beta = \frac{1}{R_{F1} + R_{F2}}$, $A_P = \frac{g_{mp}}{g_{out}}$, R_L is the load impedance, g_{mp} is the transconductance of the pass transistor, and $g_{o,EA}$ is the output conductance of the error amplifier. Thus, from equation (2.1) and (2.2), it is clear that the pole ω_{P1} is the dominant one as its having higher effective capacitance and impedance compared to the ω_{P0} and it resides at low frequencies within the range of several hundreds of kilohertz. Since, the pole ω_{P1} depends on the pass transistor gain A_P , its frequency will vary approximately with $\sqrt{I_L}$ as there is a dependency of pass transistor gain with $\frac{1}{\sqrt{I_L}}$. One can understand this dependency by placing the expressions of g_{mp} and g_{out} in equation (2.1). On the contrary, ω_{P0} directly depends on the load current I_L as g_{out} is directly proportional to I_L . Therefore, with respect to the load current I_L , the variation of dominant pole frequency ω_{P1} will be lower compared to the non-dominant pole frequency ω_{P0} . If the load current is increased, output impedance and gain will be reduced by $\sqrt{I_L}$ amount and the dominant and non-dominant pole frequencies will be increased by $\sqrt{I_L}$ and I_L amount, respectively. As a result, this would improve the phase margins as the non-dominant pole moves far away from the GBW. On the contrary, the output impedance and gain will be increased by reducing load current, but the poles frequencies are lowered and the phase margin is degraded as the non-dominant pole moves close to the GBW. So spacial care has to be taken while designing LDOs with minimum load current.

Apart from the stability, the load transient is another major design consideration. A CL-LDO regulator requires an internal fast transient path to compensate the absence of large external capacitor for achieving minimal overshoot/undershoot with fast settling time. It has been observed in the literature [35, 36, 37] that the overshoot/undershoot during large load current step can be minimized by improving the slew rate. The slew rate of an LDO basically depends on the gate capacitance of the pass transistor and the bias current of the error amplifier.

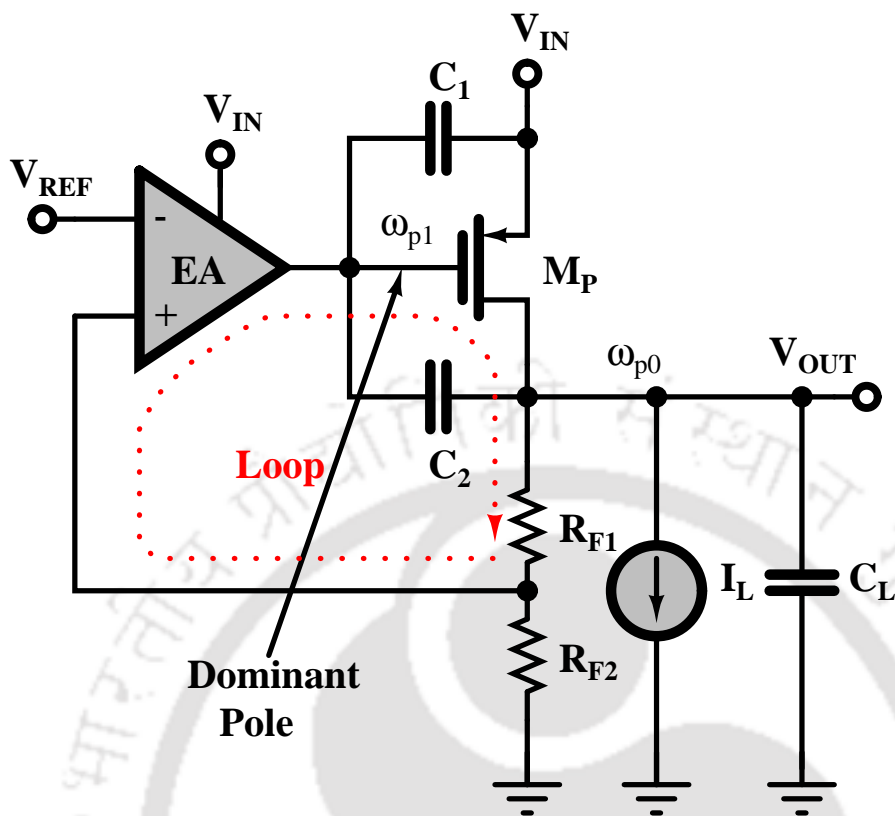


Figure 2.2: Conventional CL-LDO regulator

Therefore, one can improve the load transient by increasing the charging or discharging current at the gate of the pass element during the transient event. In order to do that Milliken et. al. introduced a differentiator with a low input impedance and high output impedance, which is nothing but a current gain amplifier, in the feedback loop to provide extra current for charging and discharging the gate capacitance of the pass element [35]. Whereas, Ho et. al. incorporated transconductance amplifiers in the feedback loop in order to improve the slew rate for better transient response [37]. In summary, the main idea behind all of them is to increase the charging and discharging current at the gate of the pass element during transient events.

2.3 Inductor Based DC-DC Converter

An ideal inductive-boost converter circuit diagram without a driving circuitry is shown in Fig. 2.3. It comprises of on-chip inductor, switches, and capacitors. By applying complemen-

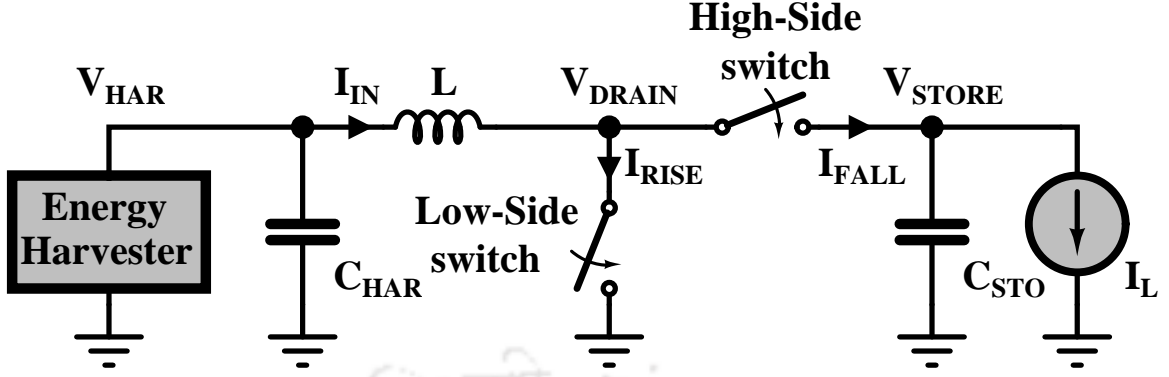


Figure 2.3: Inductive boost converter using ideal switches.

tary switching signals, one can achieve an output voltage several times higher than the input voltage. The magnitude of the output voltage mainly depends on the number of turns of the inductor coil, switching frequency, and the duty cycle of the applied clock signal. The function of the output capacitor C_{STO} is to maintain constant load voltage by utilizing the stored energy. During the positive half cycle of clock Φ , Low-Side switch is turned-on and High-Side switch is turned-off and the voltage available from the harvester causes a current to flow in the inductor L and to store the harvested energy in the form of magnetic field around the inductor. During the negative half cycle of clock Φ , Low-Side switch is turned-off and High-Side switch is turned-on, which momentarily establishes a path from the input to output and allows the inductor to discharge the stored magnetic field in the form of electric charge to the output capacitor. In order to realize switches, n-type and p-type MOSFETs are utilized for Low-Side switch and High-Side switch, respectively, as shown in Fig. 2.5.

Basically, an inductive-boost converter operates either in one of two modes: continuous conduction mode (CCM) or discontinuous conduction mode (DCM) [38]. In CCM, current flows continuously through the inductor during the entire switching cycle, whereas, in DCM, current is not continuously flowing through the inductor and even have zero current for a portion of the entire switching cycle as shown in Fig. 2.4. The basic difference between these two modes are: in CCM, the inductor current can be negative if the load current is below the average ripple current, whereas in DCM, the inductor current is prevented from flowing

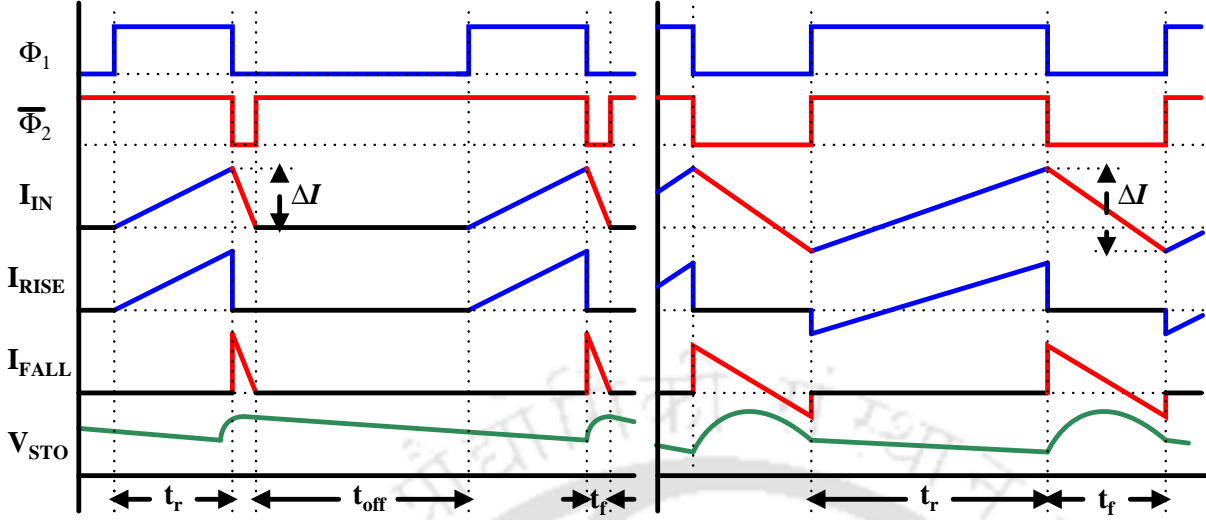


Figure 2.4: Waveforms of discontinuous conduction mode (left) and continuous conduction mode (right) boost converter.

negative. Therefore, there are three unique states in DCM: the on-state (inductor charging phase), off-state (inductor discharging phase), and idle stage (in which there is no negative current), and the first two states are identical to the CCM case except during the on-time and off-time periods. For low power applications (in the order of few hundreds of micor-watt), DCM is efficient compared to the CCM, because the High-Side switch will be turned-off after a negative current flows in the inductor, which will eventually depleted the stored charge from the output capacitor C_{STO} and lower the output voltage. However, there is a challenge in DCM design, that is to synchronize the High-Side switch with the moment when the inductor current falls to zero.

2.3.1 Discontinuous conduction mode boost converter

The discontinuous conduction mode power stage input output relationship is quite different from the continuous conduction mode power stage. And the voltage conversion relationship depends on number of design variables, as the following derivation shows. Fig. 2.5 depicts the boost converter operation in DCM. During the first switching phase Φ_1 , the inductor current ramps up to $V_{HAR} \times t_1 / L$ and during the second switching phase Φ_2 , the inductor current ramps

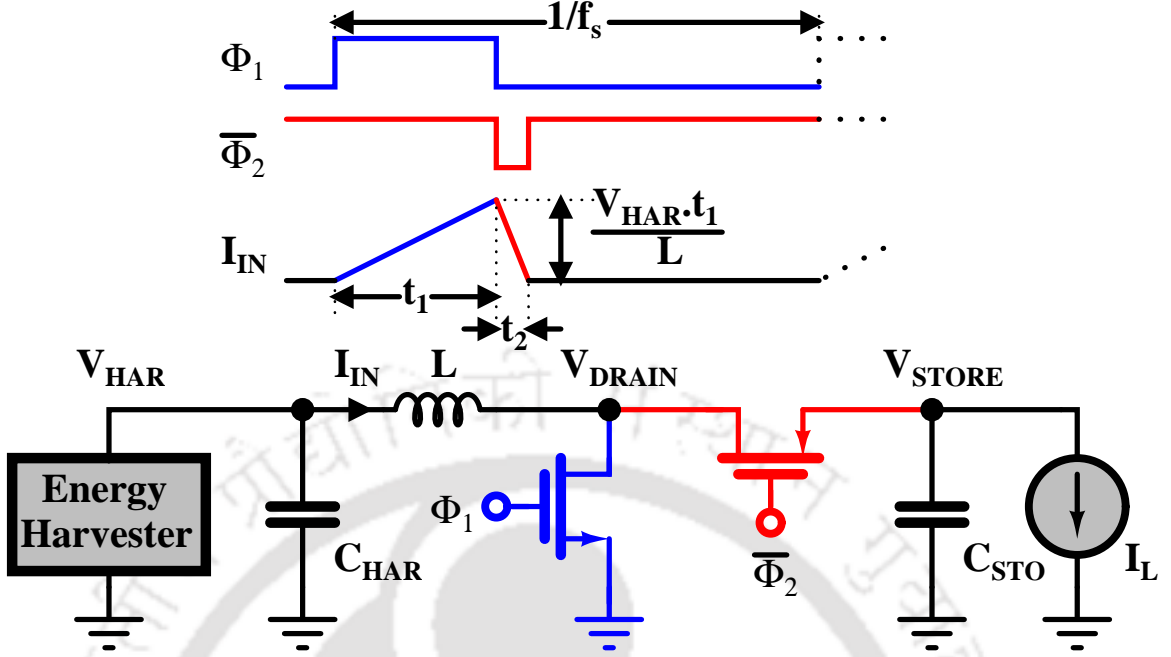


Figure 2.5: Inductive boost converter using nFET and pFET as the Low-Side switch and the High-Side switch, respectively.

down to $(V_{HAR} - V_{STORE}) \times t_2/L$ and the inductor volt-second rule gives the relationship as

$$V_{STORE} = V_{HAR} \left(1 + \frac{t_1}{t_2} \right) \quad (2.3)$$

where L is the value of inductor, V_{HAR} is the output voltage of the energy harvester, t_1 is the time duration of Φ_1 , and t_2 is the time duration of Φ_2 . From equation (2.3), it is clear that the output voltage V_{STORE} can reach several times higher than the input voltage V_{HAR} if one changes the time duration of t_1 and t_2 accordingly. The output current can be defined as the average over the complete switching cycle of the inductor current during the t_2 interval and can be expressed as,

$$I_L = \frac{V_{STORE}}{R_L} = \frac{1}{T_S} \times \left[\frac{1}{2} \times I_{PK} \times t_2 \right] \quad (2.4)$$

where, R_L represents the load and I_{PK} is the peak inductor current as shown in Fig. 2.5. By substituting $I_{PK} = V_{HAR} \times t_1/L$ in equation (2.4) one can get,

$$t_2 = \frac{2 \times V_{STORE} \times L \times T_S}{V_{HAR} \times R_L \times t_1} \quad (2.5)$$

Now, by comparing equation (2.3) and (2.5), one can get the DCM boost voltage conversion relationship as

$$V_{STORE} = V_{HAR} \times \left(\frac{1 + \sqrt{1 + \frac{4 \times D^2}{K}}}{2} \right) \quad (2.6)$$

where, $K = \frac{2L}{R_L T_S}$ and $D = \frac{t_1}{T_S}$. The above equation (2.6) shows that the voltage conversion relationship is a function of the input voltage V_{HAR} , duty cycle D , inductance L , switching frequency $1/T_S$, and the output load resistance R_L . In a typical application, usually input voltage range, output voltage, and load current are given by the power stage specifications and by substituting these parameters one can predict the inductor value to maintain the DCM operation.

The output capacitance is generally selected to limit the load voltage ripple as per the specification. The amount of capacitance required for a particular load current I_L and load voltage ripple ΔV_{STORE} is given as

$$C \geq \frac{I_{L(max)} \times \left(1 - \sqrt{\frac{2 \times L}{R_L \times T_S}} \right)}{f_S \times \Delta V_{STORE}} \quad (2.7)$$

Now, let us see the efficiency of an inductive boost converter when it operates as a DCM. The average input energy can be expressed as

$$\begin{aligned} \overline{E_{IN}} &= \frac{\text{Input power}}{f_S} = \frac{\overline{I_{IN}} \times V_{HAR}}{f_S} \\ &= \frac{V_{HAR} \times I_P}{2} (t_1 + t_2) \end{aligned} \quad (2.8)$$

where

$$\overline{I_{IN}} = \frac{V_{HAR} \times t_1 \times (t_1 + t_2) \times f_S}{2 \times L}, \quad (2.9)$$

I_P is the peak current of the first switching phase Φ_1 and f_S is the switching frequency of the boost converter. Now using equation (2.3) one can rewrite the equation (2.8) as follows:

$$\overline{E_{IN}} = \frac{V_{HAR} \times I_P \times t_1 \times V_{STORE}}{2 \times (V_{STORE} - V_{HAR})} \quad (2.10)$$

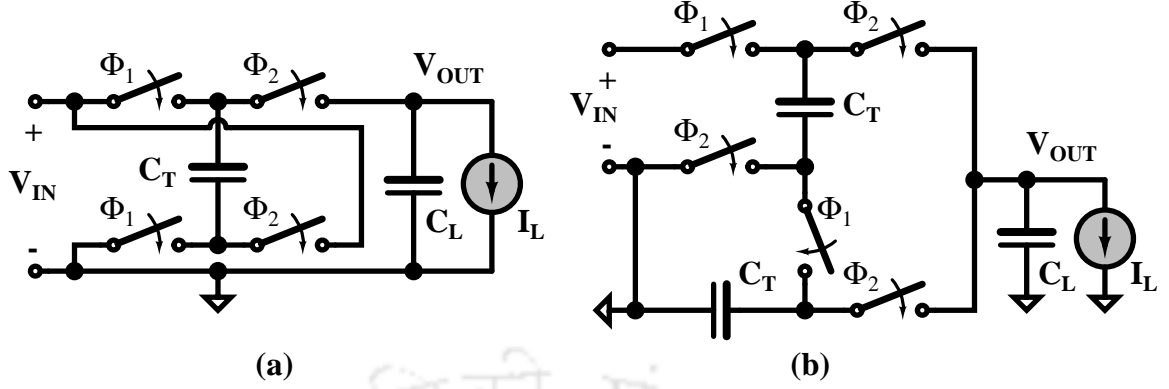


Figure 2.6: Switched capacitor DC-DC converters (a) voltage multiplied-by-2 circuit, (b) voltage divided-by-2 circuit

Similarly, one can calculate the average output energy as follows:

$$\begin{aligned} \overline{E_{OUT}} &= \frac{\overline{I_{OUT}} \times V_{STORE}}{f_s} \\ &= \frac{1}{2} \times I_P \times t_2 \times V_{STORE} \end{aligned} \quad (2.11)$$

where

$$\overline{I_{OUT}} = \frac{1}{2} \times t_2 \times \frac{V_{HAR} \times t_1}{L} \times f_s. \quad (2.12)$$

Now, from equation (2.3) and (2.11) one can get

$$\overline{E_{OUT}} = \frac{V_{HAR} \times I_P}{2} (t_1 + t_2) \quad (2.13)$$

and the efficiency of this inductive boost converter is

$$\eta = \frac{\overline{E_{OUT}}}{\overline{E_{IN}}} = 1 \quad (2.14)$$

So, the equation (2.14) indeed gives an interesting result, that there is no loss while transferring the energy from the input to output. Which means, one can achieve output voltages several times higher than the input voltage without losing any energy, i.e., 100% efficiency. However, in practical implementation the efficiency goes down to 90 – 95% due to the control losses (i.e., quiescent current) and the power transfer losses (i.e., inductor losses, switched resistor losses, and parasitic capacitance losses).

2.4 Switched Capacitor Based DC-DC Converter

Switched capacitor based DC-DC converter transfers energy by periodically charging and discharging of capacitors from the supply to the load. Fig. 2.6 shows switched capacitor based step-up (voltage multiplied-by-2) and step-down (voltage divided-by-2) converters. It comprises only of capacitors and switches, and avoids magnetic elements to perform voltage conversion. To understand the working principle of a switched capacitor based DC-DC converter, consider the step-up converter, with voltage multiplied-by-2 circuit. It comprises of a single charge transfer capacitor C_T and four switches, which are driven by two complementary phases of Φ_1 and Φ_2 . During the positive phase of Φ_1 , C_T being connected to the power supply and is charged to V_{IN} , while the load capacitor C_L being connected to the load and discharged by the current load I_L . Now, during the positive phase of Φ_2 , switches change their state and connect the capacitor C_T in between the input and output terminals and allow to discharge part of the stored charge to both C_L and I_L . So, in steady state one could expect twice the input voltage minus the loss due to the current through load, as given by

$$V_{OUT|Step-up} = 2V_{IN} - \frac{I_L \times T_S}{C_T} \quad (2.15)$$

where T_S represent the time duration of the clock cycle. So, in steady state without any load, the output voltage reaches twice the input voltage. Since the same amount of charge q flows into C_T from the supply and flows out of the C_T into C_L during the positive phase of Φ_1 and Φ_2 , respectively, then the efficiency of the circuit without any loss in load can be written as,

$$\eta_{Step-up} = \frac{V_{OUT}^2}{2V_{IN}^2 + V_{IN}V_{OUT}}. \quad (2.16)$$

From the equation (2.16) it is clear that the 100% efficiency will be achieved at only one point, when the ratio between output and input is equal to the steady state value, without any load. Now, let us consider the step-down converter with voltage divided-by-2 circuit, which comprises of two charge transfer capacitor C_T (equal in value) and four switches. During the the positive half-cycle of clock Φ_1 , two charge transfer capacitors are connected in series and is charged to

V_{IN} , while the load capacitor C_L is discharged by the load current I_L . On the other hand, during the positive half-cycle of clock Φ_2 , switches change their positions and connect two charge transfer capacitors in parallel to the load capacitor and dump the charge gained onto the load. In steady state the output voltage will be half of the input voltage minus the loss due to the current load as given by

$$V_{OUT|Step-down} = \frac{V_{IN}}{2} - \frac{I_L \times T_S}{C_T}, \quad (2.17)$$

and at no-load, the converter maintains an output voltage which is half of the input voltage. Therefore, the actual output voltage of a step-up or a step-down converter depends on the load current I_L , charge transfer capacitor C_T , and the switching frequency $1/T_S$. It is to be noted that for a step-down converter, every cycle q amount of charge is extracted from the source and $2q$ amount of charge flows into the C_L and the overall efficiency of this circuit can be given by

$$\eta_{Step-down} = \frac{\text{Energy deliver to the load/cycle}}{\text{Energy extracted from the supply/cycle}} = \frac{2q \times V_{OUT}}{q \times V_{IN}} = \left(1 - \frac{\Delta V}{V_{NL}}\right) \quad (2.18)$$

where $\Delta V = I_L T_S / C_T$ and V_{NL} is the no-load voltage and its equal to $V_{IN}/2$ for this topology. It is clear from the equation (2.18) that, 100% efficiency will be achieved when the output voltage V_{OUT} is equal to the no-load voltage V_{NL} and further away the V_{OUT} is from the V_{NL} , the system efficiency is degraded. Therefore, to improve efficiency in both topologies, step-up or step-down converter, multiple gain setting converters are provided and one needs to select one whose no-load voltage is closer to the desired load voltage [39, 40].

2.5 Summary and Conclusions

This chapter has discussed the basic fundamentals of on-chip DC-DC converters for portable electronics. Analytical expressions and analysis are provided to get a clear understanding of their functional behavior and dynamics. Major design considerations are discussed and several suggestions are made in order to improve their performance. From the above discussions, one can conclude that switching regulators are preferred over the linear regulator as they offer higher power conversion efficiency and their ability to generate higher or lower regulated voltage

from a non-regulated supply voltage without compromising the conversion efficiency. The switching regulator can be implemented either as inductive, capacitive or hybrid combination of these (not discussed in here and one may refer [12] for details). Ideally, inductive boost converter offers 100% efficiency, whereas capacitive converter offers 100% efficiency only at one point when the output voltage is equal to the no-load voltage of this topology. However, the present fabrication processes does not allow integration of high quality inductors for power management applications, and thus conversion efficiency degrades linearly with the technology node. Moreover, at low harvested power levels it requires large on-chip inductor, which increases EMI noise and system size. On the contrary, switched capacitor DC-DC converters can easily be integrated in present technology node and are favored for form-factor constrained applications. However, they suffer with poor conversion efficiency when the load voltage goes farther away from the no-load voltage, and one can mitigate this problem by incorporating multiple gain setting converters and by choosing one whose no-load voltage is closer to the desired load voltage.

3

On-Chip Switched Capacitor DC-DC Converters

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3.1 Introduction

The switched capacitor based boost charger is widely referred in literature as charge-pump circuit. A charge pump (QP) is an electronic circuit that can generate output voltage several times higher than the supply voltage or lower than the ground potential, by pumping or sharing the charges from one capacitor to others [41]. An efficient on-chip inductor-less switching power converter for solar energy harvesting is presented. The proposed energy efficient switching power converter improves the charge transfer capability as well as charge sharing time from the harvester to the load. We also present an analytical model to estimate the optimal parameters for maximizing the system efficiency. The proposed interface circuits have been designed and simulated using 0.18- μm CMOS technology node and the circuit simulations demonstrate that the proposed strategy offers system efficiency of 70%, under three different light conditions.

3.2 Literature Survey

The basic idea of a charge pump technique was first introduced by Cockcroft and Walton in 1932, where they managed to build up a potential more than 800 kilovolts from a 200 kilovolt transformer, in order to accelerate the subatomic particles to disintegrate a lithium nucleus into two alpha particles [42]. But, this model was not suitable for monolithic integrated circuit because, on-chip capacitors are limited to few hundreds of picofarads with large stray capacitances and the output impedance increases rapidly as the number of multiplying stages are increased [43]. To overcome these problems, Dickson [44] has proposed a linear topology which is similar model like Cockcroft-Walton as shown in Fig. 3.1 (a). Due to the presence of diode connected MOS transistors, every clock cycle $C_{pump} \times V_{TH}$ amount of charge is not transferred from one stage to the next stages and the situation will be even worse as one move on to farther stages as the bulk to source voltage increases and hence the threshold voltage of the MOSFET, V_{TH} . Therefore, a scheme is required which eliminates V_{TH} drop and allow to transfer full charge to later stages. In order to do that, Wu and Chang introduced a QP topology [45] which utilizes dynamic feedback control mechanism in charge transfer switches

(CTS) to eliminate the charge transfer loss resulted from V_{TH} drop as shown in Fig. 3.1 (b). Although, this topology offers better pumping gain than Dickson QP, however, it suffers with redistribution loss between the last stage and the output capacitor. Moreover, due the presence of a diode connected MOS in the last stage, it suffers with body effect and threshold voltage loss. To mitigate these problem, Feng-Su et. al. proposed a modified version of Wu and Chang's QP [46] with PMOS charge transfer switch as shown in Fig. 3.1 (d). This topology utilizes deep n-well technology, which allows to connect the bulk terminal of NMOS and PMOS to its source terminal for avoiding body effects. Moreover, by using PMOS CTSs instead of NMOS CTSs, reverse charge sharing and conduction loss have been reduced. On the contrary, by using PMOS CTSs, this topology fails to operate, if the supply voltage V_{DD} is below the MOSFET threshold voltage. Ming et. al. proposed a two branch charge pump circuit [41] using two CTSs branches and a compensated structure in each stage, which allows the charge pump operation below MOSFET threshold voltage as shown in Fig. 3.1 (c). In this topology two branches operate like independent QP circuit and deliver the load at both the half-cycle of clock Φ or Φ_B . Therefore, it improves pumping efficiency, with reduced output ripple, smaller CTSs, and lower redistribution loss. Although, this topology has many advantages, still not suitable for low supply voltage (few hundreds of millivolt) applications. Because, the CTSs can not be turned on completely, especially at the last pumping nodes, i.e., node 3 and 6. Chao Lu et. al. [47] proposed a tree-topology QP similar to Ming QP, to mitigate the minimum supply voltage restrictions as shown in Fig. 3.1 (f). Tree-topology improves the charge transfer capability by reducing charge sharing time. The above mentioned QP circuits transfer charge from the input to the load by non-overlapping clock signals. In order to reduce the area, complexity, power consumption, and reverse charge sharing, Ansari et. al. [48] replaced the non-overlapping clock signals with a single phase charge pump as shown in Fig. 3.1 (e). However, due to the presence of diode connected MOS transistor, its operation is restricted to voltages below the MOSFET threshold voltage. Moreover, it also suffers with large charge sharing time and poor charge transfer capability from the input to the load.

A detailed comparison of major contribution in charge pump circuits along with the pro-

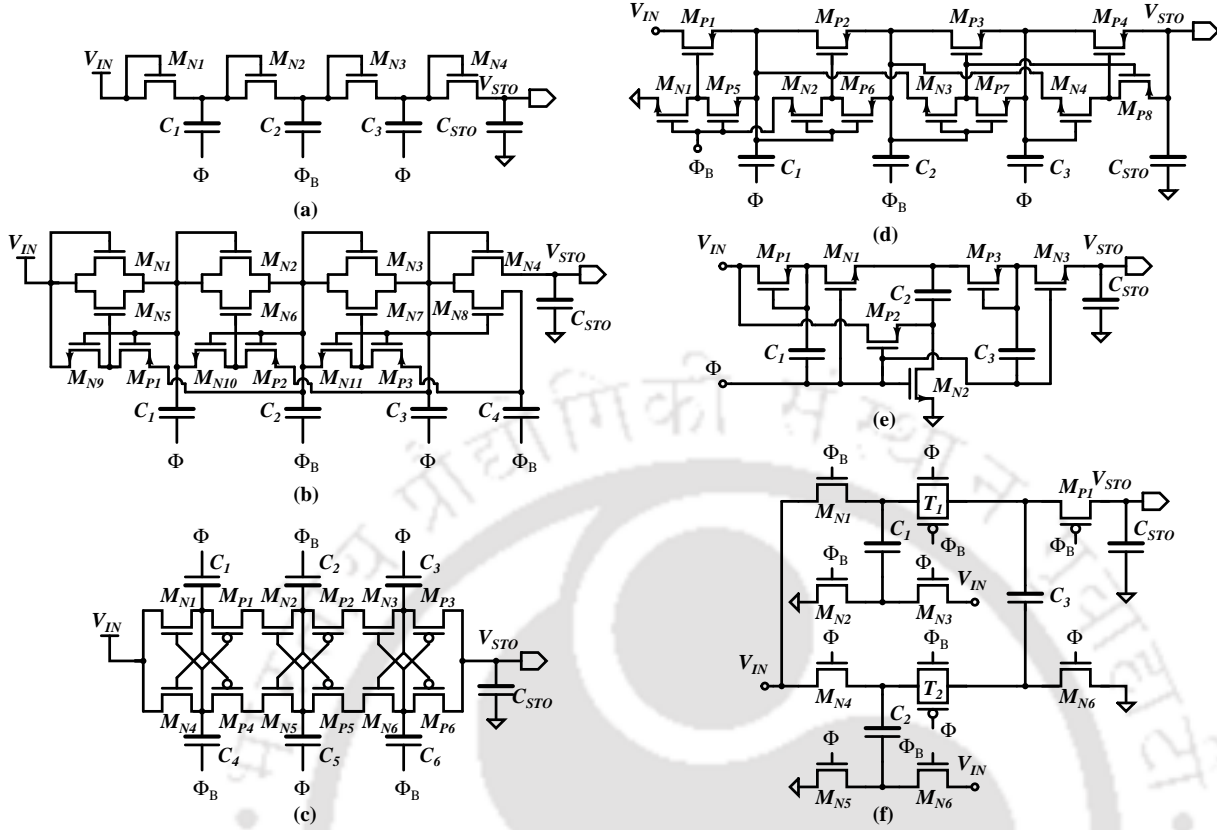


Figure 3.1: Charge pump topologies for $V_{OUT} = 4 \times V_{IN}$: (a) Dickson QP, (b) Wu and Changs QP, (c) Ming QP, (d) Feng QP, (e) Ansari QP, and (f) Chao-Lu QP.

posed one are summarized in Table 3.1. It is evident that the two-phase tree-topology QP (TPT-QP) is better in some aspect (such as, pumping efficiency, charge transfer capability, gate oxide reliability, power conversion efficiency, etc.) than the linear-topology. Whereas, single-phase linear-topology QP (SPL-QP) performs better in some other aspect (like complexity, hardware cost, dynamic loss, etc.) than the TPT-QP. Therefore, to retain the advantages of both and mitigate their individual limitations, both these topologies can be combined. In that direction, we present a single-phase tree-topology QP (SPT-QP), which have better charge transfer capability, reduced charge sharing time, less complexity, and minimum power transfer loss. Moreover, by placing PMOS and NMOS switches appropriately and by carefully controlling their gate voltage signals, the proposed QP achieves better pumping efficiency and lower reverse charge sharing. In addition to it, a systematic analysis is presented to estimate the optimal transistor width of the QP circuit for higher system efficiency.

Table 3.1: Comparison of state-of-the-Art charge pump (QP) topologies simulated for $V_{OUT} = 4 \times V_{IN}$ in 0.18- μm CMOS technology node

| Design parameters | [44]* | [45]* | [46]* | [41]* | [47]** | [48]* | Proposed** |
|---|-------------|-------------|--------------|--------------|--------------|--------------|--------------|
| Topology | TPL-QP | TPL-QP | TPL-QP | TPT-QP | TPT-QP | SPL-QP | SPT-QP |
| Minimum input voltage | $>V_{TH}$ | $>V_{TH}$ | $<V_{TH}$ | $<V_{TH}$ | $<V_{TH}$ | $>V_{TH}$ | $<V_{TH}$ |
| Power MOS and fly cap. count | 4, 3 | 14, 4 | 12, 3 | 12, 6 | 12, 3 | 6, 3 | 8, 3 |
| Non-overlapping clock generator | required | required | required | required | required | not required | not required |
| Pumping efficiency (%) | ~ 55 | ~ 63 | ~ 89 | ~ 97 | ~ 93 | ~ 63 | ~ 93 |
| Output ramp-up current (μA) | ~ 1.70 | ~ 2.70 | ~ 16.87 | ~ 21.42 | ~ 595.4 | ~ 2.52 | ~ 268.4 |
| Reverse charge sharing | moderate | higher | lower | higher | higher | moderate | lower |
| Power transfer loss @ each MOST (μA) | ~ 6.28 | ~ 4.52 | ~ 3.57 | ~ 2.68 | ~ 24.72 | ~ 3.39 | ~ 24.0 |
| Total power consumption (μW)*** | ~ 76 | ~ 108 | ~ 110 | ~ 90 | ~ 437 | ~ 38 | ~ 256 |
| Power conversion efficiency (%) | ~ 38 | ~ 62 | ~ 74 | ~ 75 | ~ 67 | ~ 43 | ~ 76 |
| Gate oxide reliability | poor | poor | poor | good | good | poor | good |
| Energy harvesting application | limit | limit | allow | allow | allow | limit | allow |

TPL-QP: two-phase linear QP; TPT-QP: two-phase tree QP; SPL-QP: single phase liner QP; SPT-QP: single phase tree QP; N.B:

$V_{clk} = 1$ V and $f_{clk} = 10$ MHz; *: $V_{IN} = 1$ V, $C = 10$ pF, and $C_{STO} = 50$ pF; **: $V_{IN} = 330$ mV, $C = 500$ pF, and $C_{STO} = 4$ nF;

***: $P_{total} = P_{loss} + P_{sub_ckt}$

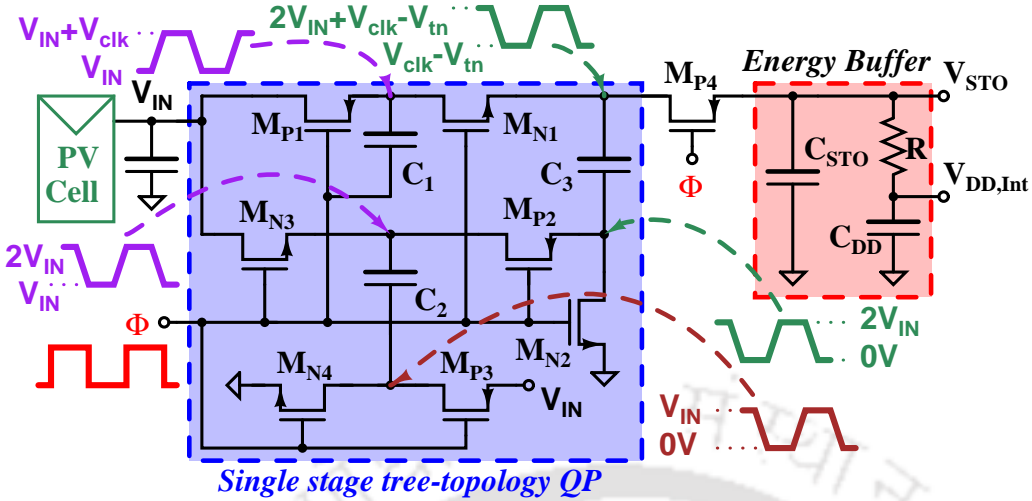


Figure 3.2: Tree-topology single-clock charge pump circuit.

3.3 Proposed Tree-Topology Charge Pump Circuit

The proposed single stage QP circuit and the corresponding voltage waveforms are illustrated in Fig. 3.2. A current starved ring oscillator with progressive sizing inverters are used for generating clock signal, which is shown in Fig. 3.3. Photovoltaic cell (PV cell) has been chosen as an input energy source to power the load circuit. In order to avoid the body effect issue on MOSFETs, triple-well process is used. The energy buffer represents a super capacitor or a rechargeable battery, where the harvested energy is being stored to supply the load and the interface circuits. The architecture is similar to the work presented in [47]. However, in terms of hardware cost, complexity, area, and conversion efficiency, the proposed one performs better than the tree topology of [47]. The operation mechanism of the proposed QP is as follows: during the positive half cycle, the capacitor C_2 will be charged by the harvester, and the capacitor C_1 will transfer its charges to C_3 . During the negative half cycle, the capacitor C_1 will be charged by the harvester, and the capacitors C_2 and C_3 along with V_{IN} will transfer their charge to the next stage capacitor or to the storage capacitor C_{STO} . Unlike linear QP, tree-topology QP utilizes both the half cycles (positive and negative) to extract charges from the harvester, which, in turn improves charge sharing time and charge transfer capabilities. Diode-connected MOS devices are avoided, in order to achieve the better pumping gain. Moreover, by carefully

placing MOS switches (PMOS or NMOS) with appropriate gate control signals, reverse charge sharing is minimized. For example, the switch M_{P1} and M_{N1} could be NMOS and PMOS instead of PMOS and NMOS with C_2 node voltage as a gate bias instead of V_{clk} . But, in that case it would degrade the performance, as one inspect the gate to source voltage for both positive and negative half cycles. The transistors M_{P3} and M_{N4} act as individual switches, which are responsible for transferring charges from V_{IN} to V_{STO} . In a similar manner, M_{N2} & M_{P2} and M_{N3} & M_{P3} switches are also responsible for charge transfer. The maximum output voltage that can be achieved for an N number of stages can be estimated as

$$V_{STO} = (2N + 1) V_{IN} + N \left[V'_{clk} - V_{tn} - \frac{2I_{OUT}}{(C + C_S) f_{clk}} \right] \quad (3.1)$$

and the average output current will be

$$I_{OUT} = \frac{(C + C_S) f_{clk}}{2N} \left[(2N + 1) V_{IN} + N (V'_{clk} - V_{tn}) - V_{STO} \right] \quad (3.2)$$

where $V'_{clk} = [C/(C + C_S)V_{clk}]$, V_{tn} is the threshold voltage of the NMOS transistor, C is the stage capacitance, C_S is the stray or parasitic capacitance, and V_{clk} is the amplitude of the clock signal.

As the number of stages plays a critical role to maximize the net harvested power and to minimize the silicon area, one may express the optimal number of stages by utilizing the analysis presented in [49] or [50], which is

$$N_{OP,Power} = 2 \left(\frac{V_{STO} - V_{IN}}{V'_{clk} + 2V_{IN} - V_{tn}} \right) \quad (3.3)$$

With the help of optimal number of stages, one gets the required value of C for a single phase tree-topology QP.

3.4 Power Transfer Loss from a System Level Perspective

When the harvested energy is passed through an interface circuit, it loses its energy due to the on resistance of the MOS transistor (conduction loss), switching of MOS transistor (dynamic

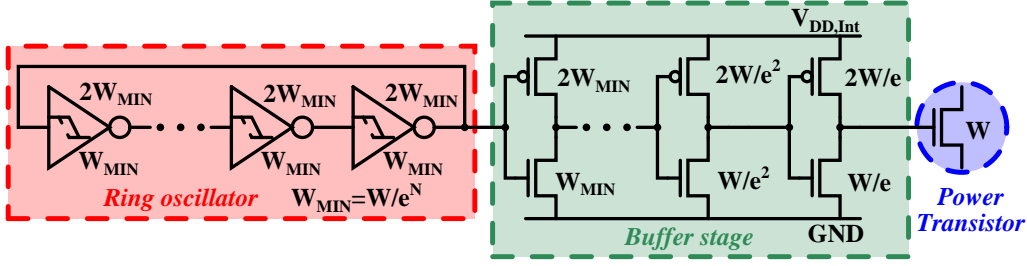


Figure 3.3: Schematic view with proper sizing of a ring oscillator, buffer stage, and power transistor.

loss), biasing (quiescent loss), and leakage (leakage loss). To achieve higher efficiency, these power loss of the interface circuit has to be minimized. An analytical model has been presented for estimating these losses and several suggestions are made to reduce the power transfer losses.

3.4.1 Conduction power loss

The conduction loss of a MOS transistor is independent of the switching frequency and is determined by its on-resistance R_{ON} and average current I_{ON} as expressed in

$$P_{CON,LOSS} = \frac{I_{ON}^2 (N_N + 2N_P) L_n}{\mu_n C_{OX} W_n [2 (V_G - V_{Tn}) - (V_S + V_D)]} \quad (3.4)$$

where N_N and N_P are the number of n-MOS and p-MOS power transistors in QP circuit, and assume $\mu_n = 2\mu_p$ and $V_{Tn} = |V_{Tp}|$. The conduction loss can be reduced by decreasing V_{DS} , V_{Tn} or by increasing transistor size. The reduction of threshold voltage demands a process change and would also cause an exponential increase in the leakage currents. On the other hand, a higher transistor size degrades the overall system form factor. Alternatively, conduction power loss can be reduced if $(V_S + V_D)$ is reduced, and it is observed that the tree-topology has smaller $V_S + V_D$ compared to the linear topology [47].

3.4.2 Switching power loss

To estimate the switching power loss, one should consider the charging and discharging of the gate capacitance of the power MOS transistors, buffer stages, and the voltage control oscillator as shown in Fig. 3.3. If the gate oxide capacitance per unit area is C_{OX} , internal

supply voltage is $V_{DD,Int}$, and the switching frequency is f_{clk} , then the switching loss will be

$$P_{SW_P,LOSS} = C_{OX}(WL)_n V_{DD,Int}^2 f_{clk} (N_N + 2N_P). \quad (3.5)$$

To drive a heavy load with least propagation delay, a buffer stage is added. The buffer stage consists of a series of progressively sized inverters, and its propagation delay is minimized when each stage bears the same effort, \hat{e} . With the help of [51], the switching loss of buffer stage is calculated in

$$\begin{aligned} P_{SW_B,LOSS} &= (N_N + 2N_P) \left\{ C_{OX} L_n V_{DD,Int}^2 f_{clk} \sum \left(\frac{2W_n}{\hat{e}} + \frac{W_n}{\hat{e}} \right) \right. \\ &\quad \left. + \left(\frac{2W_n}{\hat{e}^2} + \frac{W_n}{\hat{e}^2} \right) + \dots + (2W_{n,min} + W_{n,min}) \right\} \\ &= 3(N_N + 2N_P) C_{OX}(WL)_n V_{DD,Int}^2 f_{clk} \left(\frac{1 - (\frac{1}{\hat{e}})^N}{\hat{e} - 1} \right) \\ &\approx \frac{3C_{OX}(WL)_n V_{DD,Int}^2 f_{clk}}{(\hat{e} - 1)} (N_N + 2N_P) \end{aligned} \quad (3.6)$$

and one may further simplify by putting $N_N = N_P = N$ in

$$P_{SW_B,LOSS} \approx N C_{OX}(WL)_n V_{DD,Int}^2 f_{clk}. \quad (3.7)$$

The switching power loss due to the ring oscillator is

$$P_{SW_R,LOSS} = \frac{3P}{\hat{e}^N} C_{OX}(WL)_n V_{DD,Int}^2 f_{clk} (N_N + 2N_P) \quad (3.8)$$

where P is the number of inverter in the ring oscillator.

Therefore, one can estimate the total switching loss, as indicated in

$$\begin{aligned} P_{SW,LOSS} &= (P_{SW_P,LOSS} + P_{SW_B,LOSS} + P_{SW_R,LOSS}) \\ &= C_{OX}(WL)_n V_{DD,Int}^2 f_{clk} (N_N + 2N_P) \left\{ 1 + \frac{1}{(\hat{e} - 1)} + \frac{3P}{\hat{e}^N} \right\}. \end{aligned} \quad (3.9)$$

Since, the transistor width is directly proportional to the switching loss and inversely proportional to the conduction loss, one has to find an optimal transistor width, such that the power transfer loss will be minimum.

The total power transfer loss of an interface circuit is given in

$$\begin{aligned}
 P_{LOSS} &= P_{COND,LOSS} + P_{SW,LOSS} + P_{BIAS,LOSS} \\
 &= \frac{I_{ON}^2 (N_N + 2N_P) L_n}{\mu_n C_{OX} W_n [2(V_G - V_{Tn}) - (V_S + V_D)]} \\
 &\quad + C_{OX} (WL)_n V_{DD,Int}^2 f_{clk} (N_N + 2N_P) \\
 &\quad \times \left\{ 1 + \frac{3}{(\hat{e} - 1)} + \frac{3P}{\hat{e}^N} \right\} + I_{BIAS} V_{DD,Int}
 \end{aligned} \tag{3.10}$$

in which $P_{BIAS,LOSS}$ is the biasing power loss due to the static biasing current in analog circuits like amplifier, current mirror, bandgap reference, etc. The leakage loss in a sub-threshold transistor is comparatively small, and is ignored in this application. Equation (3.10) can be optimized with respect to the transistor width W_n as indicated in

$$W_{OP} = \frac{I_{ON}}{C_{OX} V_{DD,Int}} \times \frac{1}{\sqrt{2\mu_n f_{clk} [2(V_G - V_{Tn}) - (V_S + V_D)] \left\{ 1 + \frac{3}{(\hat{e}-1)} + \frac{3P}{\hat{e}^N} \right\}}}. \tag{3.11}$$

Therefore, optimal power transfer loss of an energy harvesting interface circuit is obtained in

$$\begin{aligned}
 P_{LOSS,OP} &= P_{BIAS,LOSS} + (N_N + 2N_P) I_{ON} V_{DD,Int} L_n \\
 &\quad \times \sqrt{\frac{f_{clk} \left\{ 1 + \frac{3}{(\hat{e}-1)} + \frac{3P}{\hat{e}^N} \right\}}{\mu_n [2(V_G - V_{Tn}) - (V_S + V_D)]}}.
 \end{aligned} \tag{3.12}$$

3.5 Measurement and Simulation Results

The proposed QP circuit was implemented in 0.18- μm CMOS technology and its layout is shown in Fig. 5.6. Post-layout simulation is carried out using standard foundry MOSFET models to validate the design. Due to the presence of switching converter, harvester voltage experiences ripple and it is suppressed by a capacitor, $C_{HAR} = 10 \text{ nF}$, in this implementation.

3.5.1 Photovoltaic harvester

To emulate the photovoltaic harvester in simulation engine one can use an electrical equivalent model with the appropriate model parameters as an input energy source. To find the model

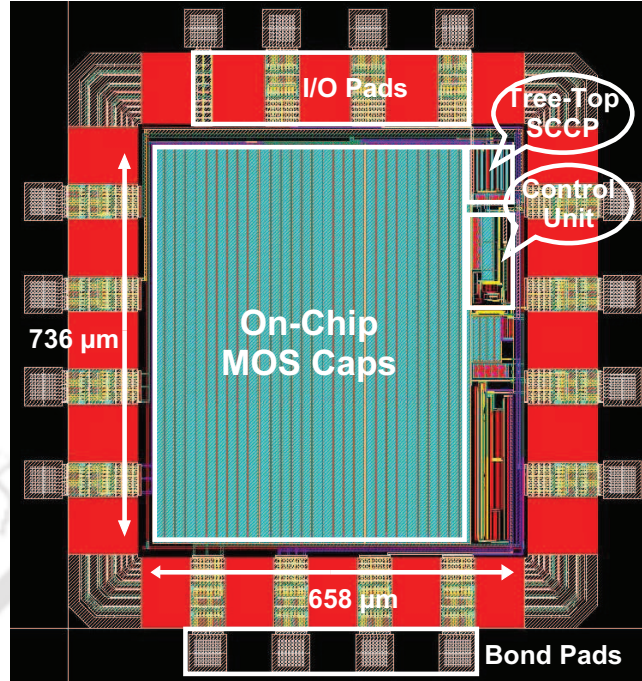


Figure 3.4: Layout of the proposed power delivery interface circuit.

parameters, we have conducted an experiment with two commercial PV cell (Model 1-100, from Solar World Inc. [17]) connected in series. A 40-Watt bulb is used as the light source and to emulate ambient variations, position of the light bulb with respect the harvester is varied. In order to vary the load resistance, a standard potentiometer with the range of 0 – 10 K Ω is used. Fig. 3.5 shows the output current variation with respect to PV cell terminal voltage for three different light conditions, 500 lux, 1000 lux, and 1500 lux, respectively. It may be noted that for a given light intensity, the output of solar cell behaves like a current source combined with a voltage limiter and at the transition point (where area under the curve is maximum), it offers maximum output power. Now, from the slope of measured $I - V$ characteristic (dotted lines), one can calculate the equivalent series (R_S) and shunt (R_{SH}) resistances for the equivalent electrical model of a PV cell. The slope near to the open circuit voltage corresponds to the series resistance and the slope near to the short circuit current corresponds to shunt-resistance. After fitting these parameters with appropriate short-circuit current, I_{SC} , and number of diodes in the electrical model, simulation is carried out and the results are plotted in Fig. 3.5 (solid lines).

There is a mismatch in the open circuit voltage at 1500 lux, but for an energy processing circuit,

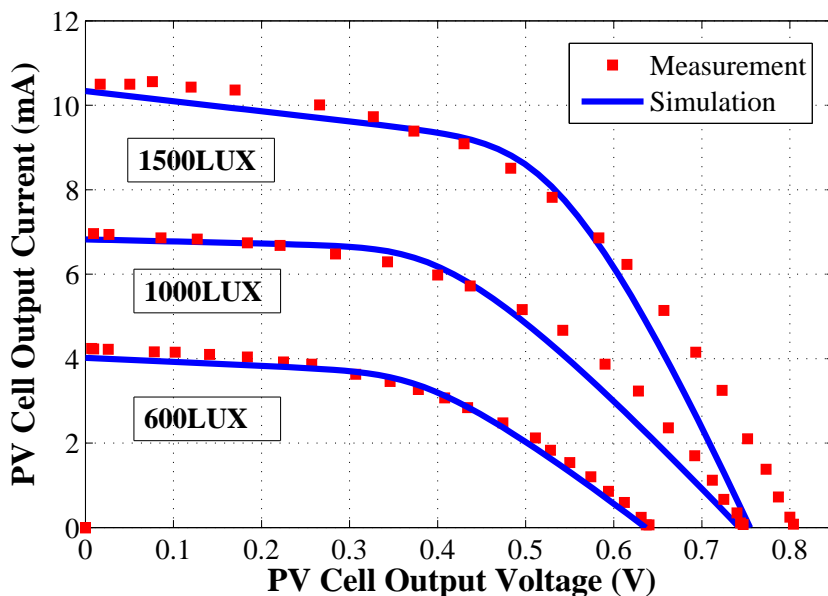


Figure 3.5: Output current variation with respect to PV cell terminal voltage for three different light conditions.

matching is important at the transition point, where the PV cell offers maximum power to the interface circuit. Fig. 3.6 shows comparison between measured and spice simulation of output power vs. PV cell terminal voltages for different light conditions. For this implementation 600 lux light intensity was chosen to supply 1 *mW* load for load voltage of 1 V.

3.5.2 Tree-topology single-clock charge pump

Unlike a battery, the energy harvester is a power source, and if the generated power from the harvester is not extracted the same would be lost. Now, to extract maximum power from the harvester one has to maintain the PV cell terminal voltage at its maximum power point voltage, which are 0.408 V for 600 lux, as shown in Fig. 3.6. Therefore, the input impedance of the QP can be adjusted by varying its switching frequency to present optimal impedance to the harvester. Now, by assuming 10% parasitic capacitance and the average switching frequency, 20 MHz, the optimal number of stages can be estimated as, $N_{OP} = 1$, and the value of stage capacitor is obtained as, $C = 195$ pF, for this implementation.

Equation (3.10) is plotted in Fig. 4.9 to find an optimal transistor width, W_{OP} , for minimum

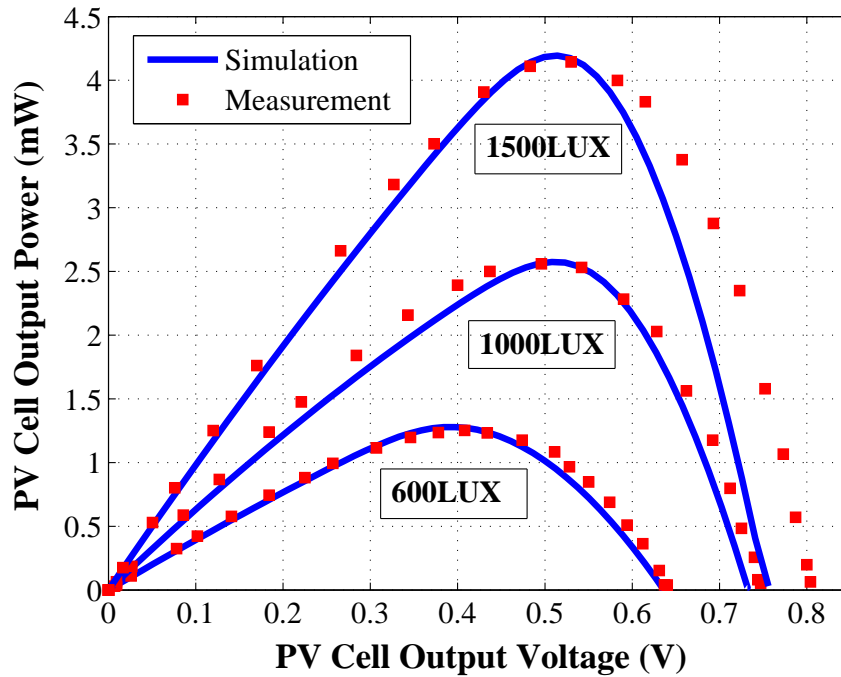


Figure 3.6: Measured and spice simulated output power vs. PV terminal voltage.

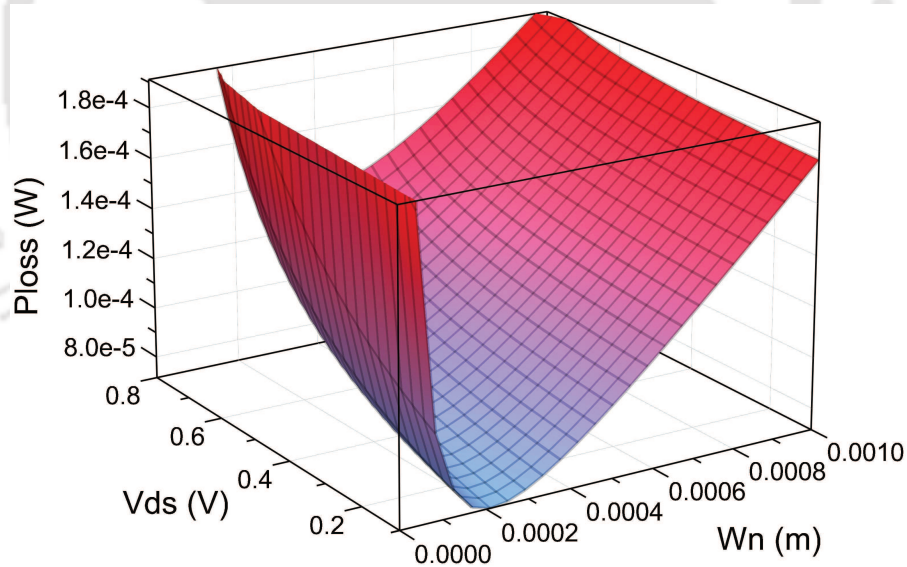


Figure 3.7: Optimal power transistor width for minimum power transfer loss.

power transfer loss. It shows the power transfer loss verses transistor width for different values of V_{DS} . The power transfer loss and the optimal power transistor width increase when the V_{DS} drop increases. The optimal transistor width is $220 \mu\text{m}$ for zero V_{DS} . However, in real

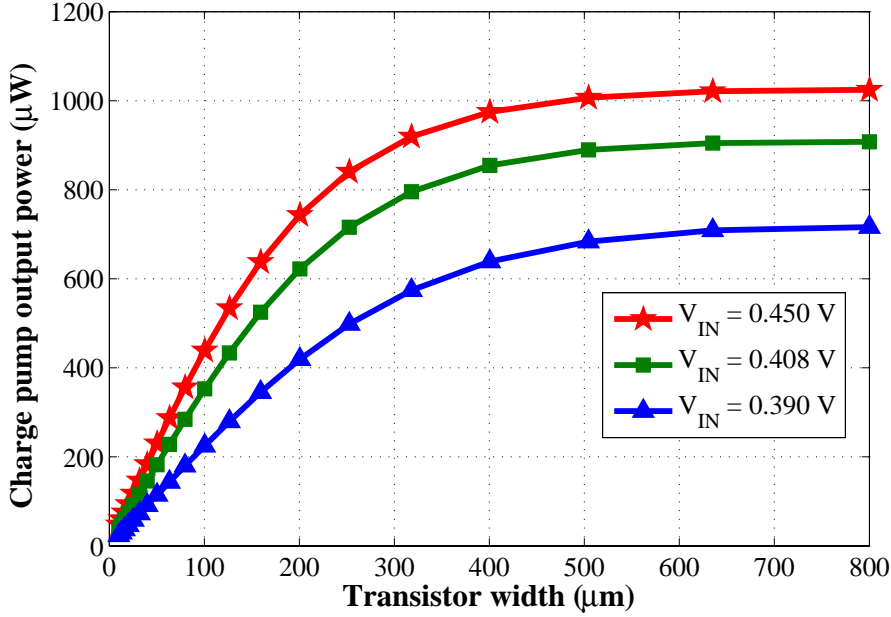


Figure 3.8: Output power verses transistor width.

implementation, there will be some V_{DS} drop across the transistors. To validate these findings we simulated output power by varying transistor width for different values of input voltage as shown in Fig. 3.8. It is evident that, up to $300 \mu\text{m}$, the output power is increased linearly and therefore, a transistor width of, $300 \mu\text{m}$ is chosen for this implementation.

Power conversion efficiency can be improved by minimizing power transfer losses. Fig. 3.9 shows a comparison of power transfer loss verses switching frequency among linear topology (Linear) [52], chow-lu tree-topology (Tree) [47], and proposed tree-topology (SC-Tree). As expected, power transfer loss is minimum for the proposed tree-topology for different values of V_{IN} and it is improved by almost 50%. The power transfer loss is higher for the linear topology, because it has higher drain to source voltage drop compared to the other topologies. Moreover, the linear and tree-topology need more number of transistors, demanding higher conduction and switching losses, compared to the proposed topology.

The simulated output power of the chow-Lu tree-topology QP (Tree) and the new proposed QP circuit (SC-Tree) under different input voltages and load conditions are compared in Fig. 3.10. For a fair comparison, transistor and pumping capacitor sizes are kept same for both

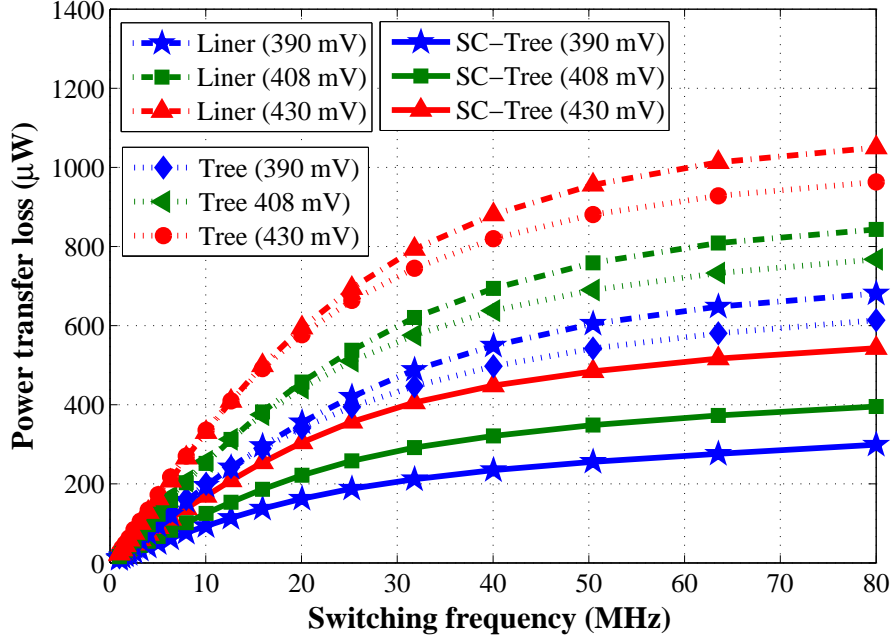


Figure 3.9: Comparison of power transfer loss vs. switching frequency.

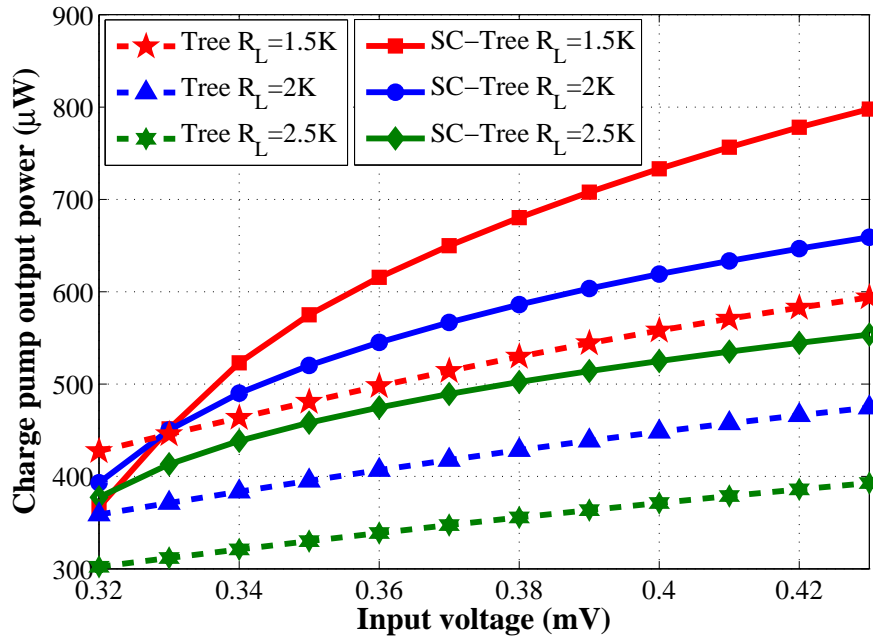


Figure 3.10: Charge pump output power vs. input voltage.

the topologies. The output power of the proposed QP circuit with different input voltages are much higher than the chow-Lu QP circuit, as the power transfer loss is minimum. This implies that the proposed topology has a better pumping performance than the existing linear and tree

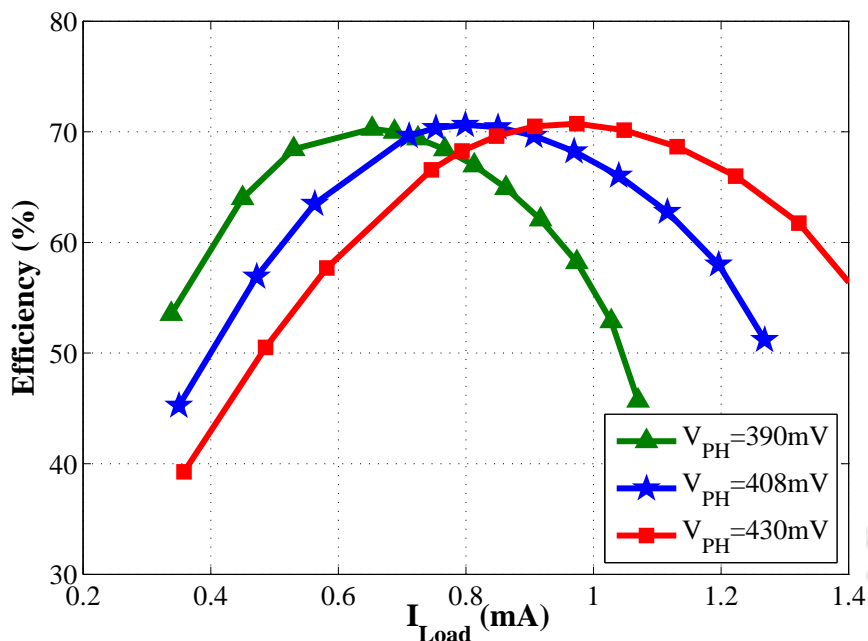


Figure 3.11: Power converter efficiency (harvester to energy buffer) vs. load current.

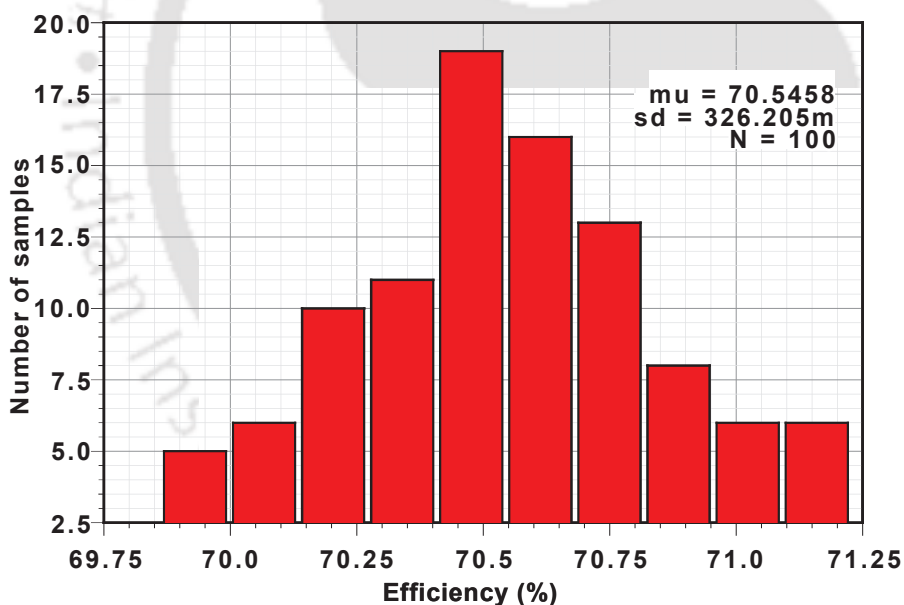


Figure 3.12: Monte-carlo simulation results of the power converter circuit.

topologies.

In order to investigate the power conversion efficiency with different load currents, simulations are carried out with different solar conditions, as shown in Fig. 3.11. The maximum peak efficiency achieved by the power converter while maintaining optimal harvester impedance is

found to be 70%. It is to be noted that the peak efficiency is almost constant under three different light conditions. 100 points monte-carlo (MC) analysis is performed to investigate the effect of process variation, between die to die and within a die (using design kit by UMC), on the proposed circuit, as is shown in Fig. 3.12. MC simulations shows that the process variations have made very minimal changes on the system efficiency, i.e., $70 \pm 0.3\%$.

Table 3.2 shows the performance comparison of the state-of-the-art power converter circuits for energy harvesting applications. The proposed power converter is suitable for solar energy harvesting applications and it maintains a peak efficiency, 70%, over a wide load range.

3.6 Summary and Conclusions

This chapter has discussed major contributions among many state-of-the-art charge pump topologies, which are suitable for micro-scale energy harvesting systems. A new single-phase tree-topology charge pump is suggested for solar energy harvesting systems, which has a better charge transfer capability and charge sharing time. This chapter has explained different power transfer loss mechanisms within a switched capacitor DC-DC converter. Analytical expressions are given and several suggestions are made to reduce the power transfer losses. It has been observed that, the power transistor width is directly proportional to the switching loss and inversely proportional to the conduction loss and therefore, there is some optimal transistor width where the power transfer loss is minimum. A systematic design methodology is also suggested to achieve higher system efficiency. Measurement and simulation results are produced to illustrate the proposed charge pump circuit functioning.

Table 3.2: Performance comparison among stat-of-the art

| Parameters | Shao [53]* | Doms [54]* | Chow[47]** | Ansari [48]** | Shih [55]* | Lu [56]** | Proposed** |
|------------------------------|-----------------------|--------------------|-----------------------|-------------------------|--------------------|----------------------|--------------------|
| Process | 0.35 μm | 0.35 μm | 65 nm | 0.35 μm | 0.13 μm | 45 nm | 0.18 μm |
| Energy Source | solar | thermal | solar | battery | solar | solar | solar |
| Input Voltage (V) | 2.1-3.5 | > 0.6 | 0.28-0.33 | 1.2 | 0.40-0.47 | 0.45 | 0.39-0.43 |
| Output Voltage (V) | 3.6-4.4 | 2.0 | 1.0 | 3.8 | 1.4 | 0.9 | 1.0 |
| Sw. Freq. (MHz) | 0.7-2.3 | 0.042-0.32 | 20 | 1.0-5.0 | 0.6-1.0 | 6.25-11.11 | 17-23 |
| Load Range | 100-775 μW | 1.0 mW | 190-681 μW | 3.64-4.92 μW | 11 μW | 46-170 μW | 0.6-1.1 mW |
| End-to-End Effi. (%) | 50-67 | 70 | not mentioned | 87-89*** | 58 | 33-40 | 70 |
| Core area (mm ²) | 0.043**** | 59***** | 0.27***** | not mentioned | 0.42***** | 0.61***** | 0.48***** |
| Application | Eng. Har. | Eng. Har. | Eng. Har. | high voltage | Eng. Har. | Eng. Har. | Eng. Har. |

*On chip measured results; **Postlayout simulation results; ***Power transfer losses are not considered; **** without pumping capacitors; *****with pumping capacitors; Eng. Har.: Energy harvesting

4

Interface Circuits for Solar Energy Harvester

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4.1 Introduction

Scavenging energy from ambient sources like, vibration, solar radiation, thermal gradient or radio frequency waves has become an attractive and promising option for powering an IoT node. Due to the high power density and ubiquitous nature of light, a PV cell has been chosen as an energy source for powering an IoT node. However, in some applications like biomedical implants, boiler, sensor nodes, *etc.* where light is difficult to reach, one may think about biopotential [3], thermoelectric harvester [18], or piezoelectric harvester [57] for powering IoT nodes. The typical power density of a PV cell [17] varies approximately from tens of μW per cm^2 to several hundred of μW per cm^2 for indoor and outdoor light conditions, and it is sufficient to meet the supply requirement of an IoT node. However, it suffers from a poor conversion efficiency of approximately $\sim 10 - 40\%$, and it would degrade further when the ambient light intensities are changing from one condition to another. Thereby, the conversion efficiency may be improved by tracking and offering optimal impedance dynamically.

Extracting maximum power from a photovoltaic harvester with minimum power transfer loss is one of the primary design goals of an energy processing circuit. Unlike a battery, harvester has a continuous source of unlimited power without depletion, and if power were not extracted, the same would be lost. To extract the maximum power one has to offer an optimal impedance to a harvester, and in order to reduce the power transfer loss, a low-overhead efficient architecture is needed. This chapter presents a fully integrated photovoltaic power harvesting system with a low-overhead adaptive maximum power point tracking (MPPT) scheme for Internet-of-Things (IoT) nodes. The proposed scheme tracks the maximum power points within $12 \mu\text{s}$ by utilizing an inherent negative feedback loop, within a tracking error of 0.6%. The tracking range has been improved by $\sim 57\%$ using a current-starved voltage controlled oscillator (CS-VCO) instead of a polynomial VCO. The overhead area and power consumed by this tracking scheme are approximately 0.013% and 0.1%, respectively. Using commercially available solar cell of area 11.3 cm^2 , the proposed system can provide $833 \mu\text{W}$ of power with a light intensity of 600 lux. The proposed energy processing circuit has been designed using 0.18-

μm CMOS technology node and the circuit simulations demonstrate that the proposed scheme can track maximum power point (MPP) under rapidly changing atmospheric conditions with a peak tracking efficiency of 99%.

4.2 Literature Survey

A good number of publication on MPPT has been reported since 1968 to till date, which are summarized in [58] and [59]. However, very few of them are suitable for micro-scale energy harvesting systems due to the constraints of the minimum operational voltage range, off-chip components, hardware cost, power consumption, *etc.* [60]. Therefore, low-overhead, low-cost, low-voltage range, SoC MPPT scheme is desired in order to transfer maximum power with minimum loss to the load circuit. Although, the MPPT technique is quite mature and well explored, the research in scavenging solar power for an IoT node is quite recent. Raghunathan et. al [61] and Jiang et. al [62] made their first attempt to supply a sensor node using a small PV cell to avoid human intervention or servicing. In those implementations, the output of a PV cell is directly connected to a rechargeable battery or a supercapacitor with an appropriate reverse current protection. Near MPP is achieved by carefully choosing PV module with respect to battery voltage, which is a one-time decision approach. Therefore, there is no MPP tracking mechanism in real time scenario. Moreover, the scavenging process will stop once the PV cell voltage is lesser than the sum of battery voltage and threshold voltage of the device. To mitigate these problems, Simjee et. al [13] implemented an MPPT scheme for a wireless sensor node, based on fractional open-circuit voltage (FOC) technique. From the empirical data analysis, it has been observed that there exists a near-linear relationship between the maximum power point voltage (V_{MPP}) and the open circuit voltage (V_{OC}) under varying light conditions and temperature levels. Thereby, once the proportionality constant (K_{PV}) is known, V_{MPP} can be computed periodically by momentarily shutting down the power converter and measuring open circuit voltage. However, this periodically turned-on and turned-off of the power converter increases power consumption and causes temporary power loss to the load, which will degrade the system efficiency and load regulation. To overcome this problem Brunelli et. al [63] report

an improved design technique where an additional pilot PV cell is used to reduce the power consumption and the temporary power loss at the load. However, a true-MPP may not be achieved, as there exists mismatch between die-to-die and within a die. Moreover, the fraction or proportionality constant also varies with different light intensities, temperatures, and solar cells, with a typical range of values varies in between $\sim 0.65-0.80$ [13]. Therefore, this type of scheme is also another one-time design and implementation scheme for a specific PV cell and not an adaptive one. Thereby, researchers progressed to hill-climbing and Perturb and observe (P&O) methods where one can achieve true MPP by adjusting perturbation step size [64]. In this method, a variable perturbation is given in the duty ratio of a power converter which will perturb PV cell current and effectively change the operating voltage in the PV cell. However, this scheme will fail to achieve true MPP under rapidly changing atmospheric conditions. Moreover, this scheme requires power hungry current/voltage sensors, analog and digital comparators, flip-flops, micro-controller, etc. In order to reduce hardware cost and power consumption Shao et. al [53] introduced a dedicated hardware based on hill climbing algorithms which eliminate the micro-controller unit. However, still this system requires power hungry current sensor, analog and digital comparators, and a separate decision generation block. Lu et. al [56] present a low overhead MPPT algorithm based on negative feedback control loop which eliminates the power hungry current/voltage sensor and microcontrollers, by which the power consumption is reduced significantly. However, the scheme requires a polynomial VCO, which comprises of analog comparator, bulky resistor and capacitor, current mirror circuit, MOS transistors, and a ring oscillator. Moreover, the hardware implementation is not exactly reflected by their mathematical interpretation. On the contrary, presented work provides an efficient MPPT scheme which avoids extra circuitries and utilize inherent negative feedback control loop to track the maximum power point.

4.3 Overall Energy Harvesting System

The block diagram of the proposed power management architecture is shown in Fig. 4.1. It comprises of a power converter (DC-DC₁), a CS-VCO, and a low dropout (LDO) regulator

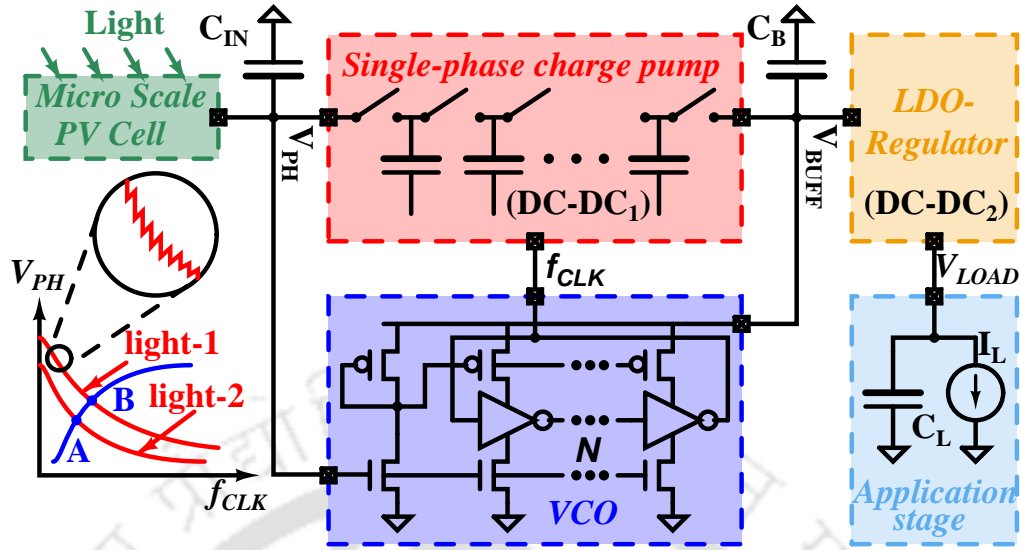


Figure 4.1: Block diagram of the power management unit for an IoT node.

(LDR). The PV cell converts the light energy into electrical energy and transfers it to the energy buffer (battery/super-capacitor) through the power converter and an LDR provides regulation to the application stage. A switched-capacitor based power converter has been chosen instead of an inductive boost converter [65] to avoid large EMI noise, bonding-wires noise, the effective series inductance of the off-chip components, PCB trace, and extra pads and pins [43, 66]. CS-VCO is used to vary the switching frequency of the power converter with respect to the variation of PV cell voltage (V_{PH}). As the ambient light intensities are changing over the time, there will be a mismatch in energy get-in and get-out, and one needs a storage unit (C_B) to utilize the whole energy efficiently. LDO regulators are used to minimize the voltage drop between the energy buffer and the application stage for obtaining higher end-to-end efficiency. Apart from that, it provides an isolation between the noisy power converter output to the noise-sensitive load circuits. Due to the presence of switching converter, harvester voltage will experience ripples and one can suppress it by placing an input capacitor (C_{IN}) in between PV cell and the power converter.

Basically, the architecture consists of a two-stage DC-DC converter. The first converter comprises of charge pump circuit and the CS-VCO, whereas the second converter is the LDO regulator. The first one offers an optimal input impedance necessary to extract maximum power

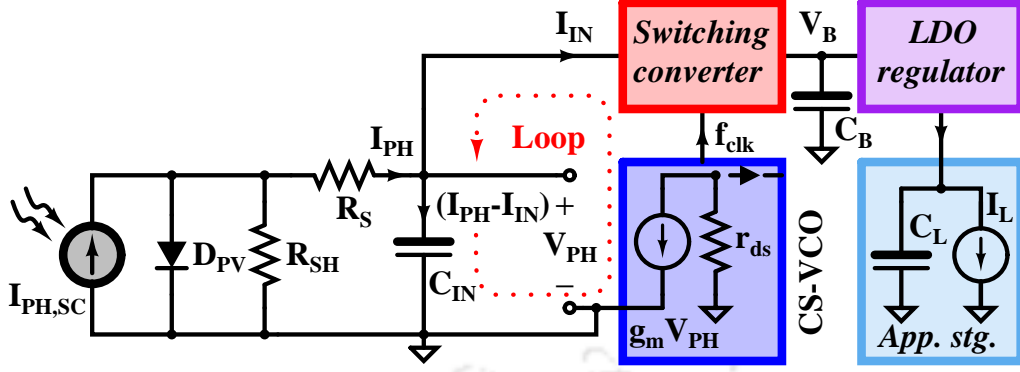


Figure 4.2: Simplified block diagram of the proposed architecture for understanding the inherent negative feedback loop for tracking maximum power points.

from the harvester to the energy processing circuits, whereas the second one provides a stable regulated supply to the load circuit. To adjust the input impedance of the power converter dynamically with various light conditions, switching frequencies of the power converter are varied. Once the input impedance of the power converter is matched with the harvester impedance, maximum power transfer will be taking place from the harvester to the interface circuit. The frequency at which maximum power transfer take place is known as maximum power point frequency, f_{MPP} . In order to practically realize it, an inherent negative feedback control loop is utilized, which comprises of PV cell, power converter, and CS-VCO as shown in Fig. 4.2. Let us assume, in absence of light, the current through the PV cell is zero, and hence V_{PH} , I_{PH} , I_{IN} and f_{clk} are also equal to zero. As soon as the light impinges on the PV cell, a non-zero photocurrent begins to flow in the input capacitor C_{IN} , accordingly. Once the capacitor C_{IN} is charged up to a certain limit, CS-VCO starts oscillating and enable the switching converter for transferring charges from the PV cell to the supercapacitor, C_B . As the part of I_{PH} , i.e., I_{IN} , is flowing through the switching converter, charging current of C_{IN} , i.e., $I_{PH} - I_{IN}$, starts reducing and eventually becomes zero once $I_{PH} = I_{IN}$. At that point, CS-VCO locks its frequency and remains in its state until there is any change in ambient conditions. Now, if there is a change in ambient condition, I_{PH} will be either increased/decreased depending on the light intensity. However, I_{IN} will not change immediately due to the delay involve in the feedback loop and hence, the error current ($I_{PH} - I_{IN}$) either goes up/down depending on the ambient condition

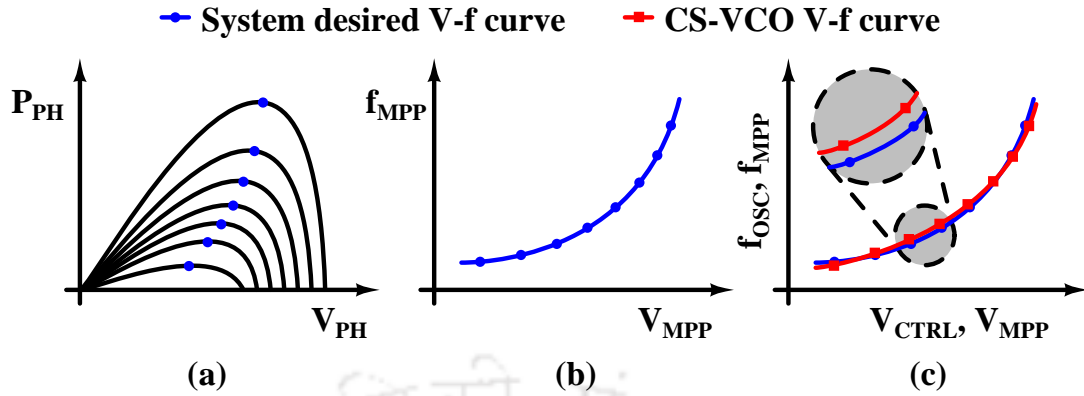


Figure 4.3: (a) PV cell output power voltage characteristics, (b) System desired V-f characteristic, and (c) CS-VCO and system desired V-f characteristics.

and it will reflect on V_{PH} , accordingly. Once the V_{PH} is changed, f_{clk} will change and hence, the input impedance of the switching converter will change. Due to the change in input impedance, the converter will transfer more/less current to the buffer stage, and the error current will go down/up and finally becomes zero after few iterations.

Now, in order to make sure that the locking frequency is the maximum power point (MPP) frequency, CS-VCO has to be designed in such a way that it passes through all the system desired MPP points as illustrated in Fig. 4.3. Fig. 4.3(a) shows the PV cell power voltage characteristics and MPPs under different light intensities. To extract maximum power from this PV cell, power converter input voltage has to be the MPP voltage, which is marked with blue dots. In order to get these MPP voltages (V_{MPP}), CS-VCO has been disconnected from the loop and plotted the combined characteristics of PV cell and switching converter in Fig. 4.3(b), which is nothing but system desired V-f characteristic. Now, one has to design a VCO, which will approximate the desired V – f curve well enough such that the disparity between them is negligible as shown in Fig. 4.3(c). Therefore, every stable point will be the maximum power point of this feedback control loop.

Fig. 4.4 shows the complete circuit diagram of the proposed power management unit. To emulate the PV cell in the simulation engine, an electrical equivalent model is used as an input energy source. The switched-capacitor power converter is basically a charge pump circuit, which generates output voltage several times higher or lower than the supply voltage or

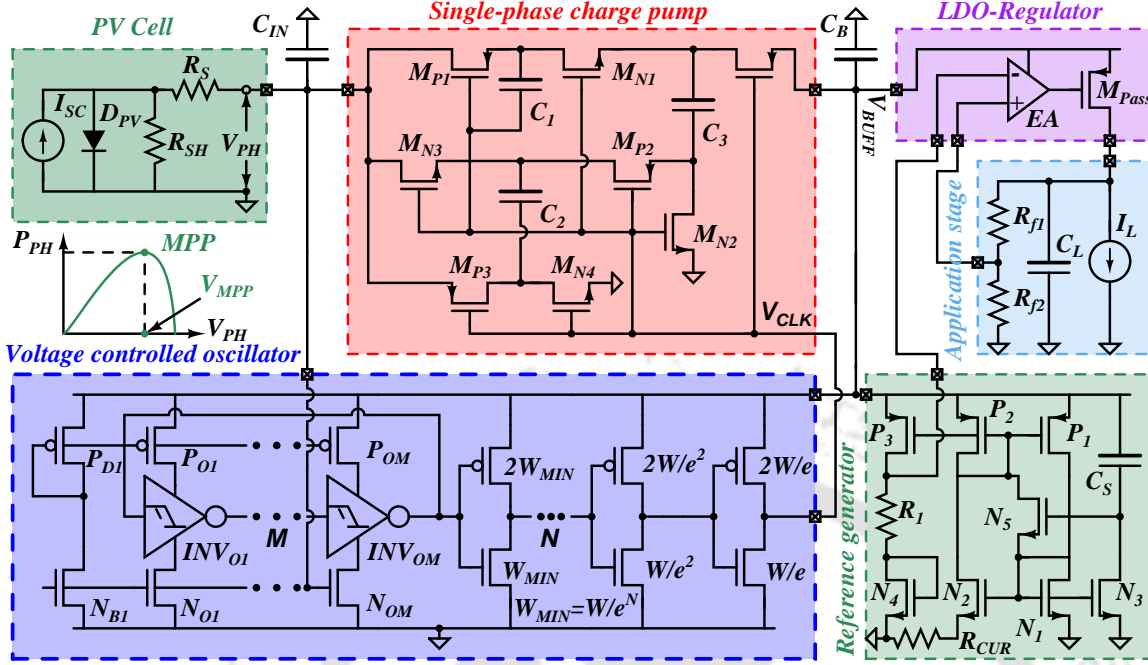


Figure 4.4: Circuit diagrams of the proposed power management interface circuit.

ground potential [41]. Generally, it is made up of pumping capacitors and MOS switches, and transfer charges from the harvester to the buffer stage with the help of clock signals. In this implementation, single stage single-phase tree-topology charge pump circuit is used, as it has better charge transfer capability, reduced charge sharing time, less complexity, and minimum power transfer loss compared to the other topologies [67]. The sizes of pumping capacitors (C_1 , C_2 , and C_3) and MOS transistors (M_{N1} - M_{N4} and M_{P1} - M_{P3}) are kept same as in [67]. An array of a five-stage current-starved inverter ($M = 5$) is used to achieve the desired clock frequencies for MPPT. V_{BUFF} and V_{PH} are used for power supply and controlling the oscillation frequency. The (W/L) of P_{D1} and N_{B1} are kept at $(0.72/0.36)$ micrometer and (W/L) of $P_{O1} - P_{OM}$ and $N_{O1} - N_{OM}$ are kept at $(0.72/0.18)$ micrometer, respectively. The (W/L) of PMOS and NMOS of current starved inverters ($INV_1 - INV_M$) are kept at $(0.72/0.36)$ micrometer for this implementation. To drive heavy loads, an array of progressively sized inverters are incorporated after the oscillator and their sizes are given in the figure itself. Where W is the width of combined power transistors which are driven by the CS-VCO and e represents each stage effort. The detailed discussion of progressive sizing inverters are made in [51] and [67]. The

LDO voltage regulator comprises a reference generator, an error amplifier followed by a common source stage, and a feedback network. The regulator senses any output voltage deviations and correspondingly makes changes in the gate to source voltage of the pass-transistor using an error amplifier, such that it provides sufficient current to the load to maintain load regulation. A capacitor-less LDO (CL-LDO) regulator has been chosen to reduce the number of external components and provide system-on-chip solution [9]. A type-A error amplifier (EA) is used for this implementation [9] and sizings are made accordingly to achieve 40 dB gain. The W/L of the pass transistor (M_{Pass}) is chosen as (2000/1) micrometer. A subthreshold current reference circuit is chosen from [68] for reference generator as the conventional bandgap reference restricts its operation below 1.25 V. In application stage, C_L represents parasitic capacitors and integrated capacitors at the output node, and it is in the order of picofarads range. Previous works report start-up circuits [69, 70] and therefore, this implementation does not focus the startup issues but assumes that the supercapacitor (C_B) is initially charged to bring up the system from the sleep state to an active state. An analytical modeling for MPPT has been carried out in the next section to quantify the proposed idea.

4.4 MPPT Schemes Suitable for IoT Applications

The circuit which tracks and offers the optimal load impedance/voltage for extracting maximum power from the harvester is known in the literature as maximum power point tracking (MPPT) circuit. While transferring maximum power to the load circuit, the power overhead by an MPPT block can not be ignored in a micro-scale solar energy harvesting system. Therefore, low hardware cost MPPT scheme is desired for IoT applications. A comparison of a major characteristic of different MPPT schemes suitable for micro-scale energy harvesting systems along with the proposed one is summarized in Table 4.1. In comparison with other implementations, the advantages of proposed scheme is apparent. The proposed scheme utilizes the inherent negative feedback control loop to track the maximum power point voltage and to stabilize the system. For this implementation, switching frequencies are varied to adjust the input impedance of the power converter.

Table 4.1: Comparison of MPPT scheme suitable for micro-scale energy harvesting systems

| Design parameters | DICM[61] | FSCI[71] | FOCV[13] | P&O[72] | HC[53] | NFC[56] | Proposed* |
|-----------------------------|---------------|------------|------------|------------|---------------|------------|------------|
| Implementation Complexity? | Low | Medium | Low | High | Medium | Low | Low |
| Sensors Required? | No | Yes | Yes | Yes | Yes | No | No |
| Microcontroller Required? | No | Yes | Yes | Yes | No | No | No |
| Depends on PV spec.? | Yes | Yes | Yes | No | No | No | No |
| Adaptive MPPT? | No | No | No | Yes | Yes | Yes | Yes |
| Impedance match by varying? | not described | Duty ratio | Duty ratio | Duty ratio | Clock frq. | Clock frq. | Clock frq. |
| Convergence Speed? | Zero | Medium | Medium | Varies | Varies | Fast | Fast |
| Tracking Error? (%) | ~ 12 | ~ 20 | ~ 5-11** | ~ 4.0 | not described | ~ 0.2-0.69 | ~ 0.1-0.6 |
| Tracking range? | not described | Small | Small | Wide | Medium | Medium | Wide |
| Switching converter type? | not described | Inductive | Inductive | Inductive | Capacitive | Capacitive | Capacitive |
| Hardware Cost? | Zero | Medium | Low | High | Medium | Low | Low |

DICM: Design Time Component Matching; FSCI: Fractional Short-Circuit Current; FOCV: Fractional Open-Circuit Voltage; P&O: Perturb and observe; HC: Hill Climbing; NFC: Negative Feedback Control; *: Based on NFC; **: Compared to P&O.

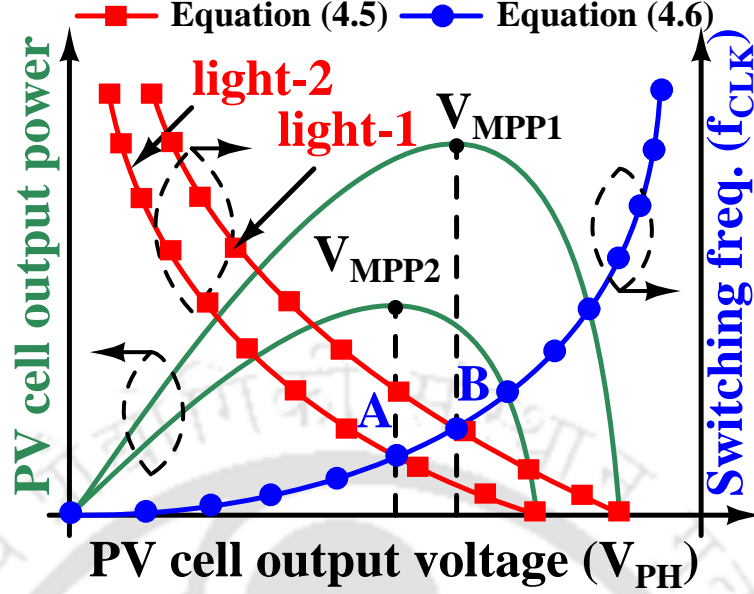


Figure 4.5: Two independent relationships between f_{CLK} and V_{PH} that arise from different sources: i) change in converter input impedance and hence V_{PH} with f_{CLK} (the red lines) under two different light intensities, ii) the change in f_{CLK} with VCO control voltage (the blue line), and iii) PV cell power variation with respect to V_{PH} under two different light conditions (the green lines)

4.5 Analytical Modeling for Proposed MPPT Scheme

In steady state, the output current and voltage of a single-phase tree-topology charge pump [67] can be modeled as

$$I_{OUT} = \frac{(C + C_S) f_{clk}}{2N} [(2N + 1)V_{PH} + N(V'_{clk} - V_{tn}) - V_{BUFF}] \quad (4.1)$$

$$V_{BUFF} = (2N + 1)V_{PH} + N \left[V'_{clk} - V_{tn} - \frac{2I_L}{(C + C_S) f_{clk}} \right] \quad (4.2)$$

and the input current can be modeled as

$$I_{IN} = N \times I_{OUT} + I_{QP,LOSS} \quad (4.3)$$

where $V'_{clk} = [C/(C + C_S)V_{clk}]$, V_{clk} is the amplitude of the clock signal, V_{tn} is the threshold voltage of the NMOS charge transfer switch (CTS), C is the stage capacitance, C_S is the stray capacitance, N is the ideal voltage step-up ratio, V_{BUFF} is the output voltage, and $I_{QP,LOSS}$ is the charge pump's internal current loss. The $I_{QP,LOSS}$ can be modeled as $f_{clk} \times \beta$, where β is

a constant parameter and its value depends on the specific design [52]. The effect of loading condition can be visualized by writing an expression of V_{BUFF} from the equation (4.1) by replacing I_{OUT} with I_L as given in equation (4.2). Now, if one increased/decreased the load current from the steady state value, the output voltage (V_{BUFF}) will goes down/up, provided the solar condition is unaltered. Once the PV cell is connected with this charge pump, the input current and voltage will be the PV cell output current (I_{PH}) and voltage (V_{PH}). In reference [56], the I_{PH} is approximately modeled as

$$I_{PH} \approx I_{SAT} \left\{ e^{\frac{q}{AKT}(V_{OC})} - e^{\frac{q}{AKT}(V_{PH})} \right\} \quad (4.4)$$

where V_{OC} is the open circuit voltage, and can be used as an electrical parameter for representing different light irradiance. For simplicity, the temperature variation on I_{PH} along with light irradiance is neglected. Therefore, from equation (4.1), (4.3), and (4.4), one can write an expression of a charge pump switching frequency as

$$f_{clk} = \frac{2 \times I_{SAT} \left\{ e^{\frac{q}{AKT}(V_{OC})} - e^{\frac{q}{AKT}(V_{PH})} \right\}}{(C + C_S) \left[(2N + 1)V_{PH} + N(V'_{clk} - V_{tn}) - V_{BUFF} \right] + \beta}. \quad (4.5)$$

The equation (4.5) is illustrated in Fig. 4.5 for two different light intensities. It shows the variation of V_{PH} with respect to switching frequencies. At zero switching frequency, there is no charge transfer take place through the power converter, therefore V_{PH} is equal to V_{OC} . Once the switching frequency increases, the charge transfer will take place and V_{PH} start reducing accordingly. In other words, the input impedance of the power converter is reduced as one increases the switching frequency. The maximum power transfer will be taking place, once the input impedance of the power converter matches with the PV cell impedances. Therefore, the optimal switching frequency f_{MPP} can be obtained by substituting V_{PH} with V_{MPP} and V_{OC} with V_{MPP}/α (because, it has been found in literature, [73] and [13], that the maximum power point voltage is a fraction of open circuit voltage of a PV cell) in equation (4.5) as given by

$$f_{MPP} = \frac{2 \times I_{SAT} \left\{ e^{\frac{q}{\alpha AKT}(V_{MPP})} - e^{\frac{q}{AKT}(V_{MPP})} \right\}}{(C + C_S) \left[(2N + 1)V_{PH} + N(V'_{clk} - V_{tn}) - V_{BUFF} \right] + \beta} \quad (4.6)$$

where α is almost constant for a given PV cell and its typical value for this implementation

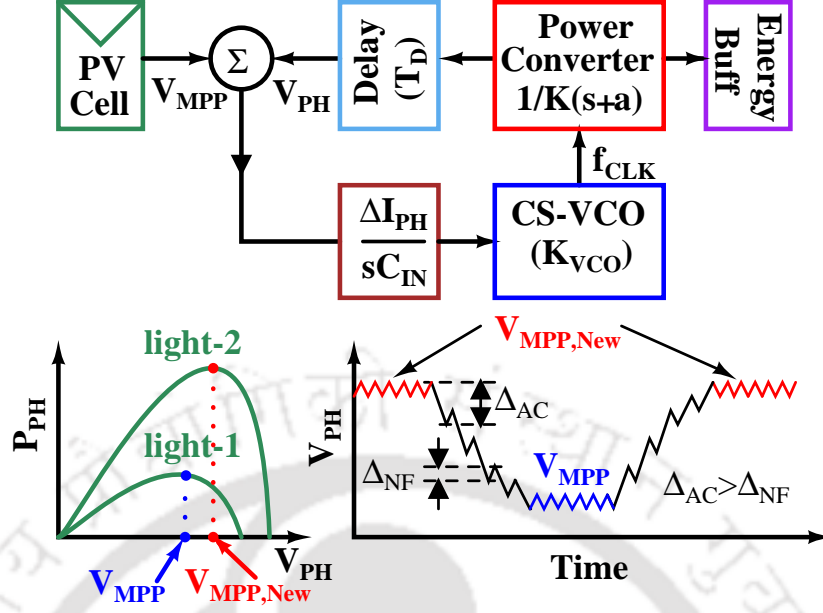


Figure 4.6: Block diagram of the inherent negative feedback control loop for MPPT scheme.

is ~ 0.65 . The characteristic of equation (4.6) is illustrate in Fig. 4.5. It shows the optimal switching frequencies for different MPP voltages. It is to be noted that, for a given light intensity there is only one intersection point (either A or B) between these two curves and the system will settle at that operating point. Therefore, as the generated switching frequencies of the CS-VCO follows equation (4.6), the whole system will be stabilized at the maximum power points, and it can be modeled as discussed in [74] and [75],

$$f_{\text{OSC}} = \frac{I_{\text{SS}}}{2M \times V_{\text{BUFF}} (C_{in} + C_{gd_p} + C_{db_n} + C_{gd_n} + C_{db_p})} \quad (4.7)$$

where I_{SS} is the tail current and M is the number of delay stages in the ring oscillator. The value of I_{SS} depends on sizes and operating regions of P_{D1} and N_{B1} transistors. The total node capacitance of each delay stage can be modeled as $C_{in} + C_{gd_p} + C_{db_n} + C_{gd_n} + C_{db_p}$, where C_{in} , C_{gd_n} , C_{gd_p} , C_{db_n} , and C_{db_p} , represent next stage input capacitance, gate to drain and drain to bulk capacitances of nMOS and pMOS transistors, respectively.

Now, in order to understand the closed loop tracking behavior, a simplified block diagram of the inherent negative feedback control loop is shown in Fig. 4.6, where ΔI_{PH} represents the change in ambient condition and T_D represents the delay in the feedback loop. The input

capacitor C_{IN} acts as an integrator and the power converter acts as a feedback network. The CS-VCO is modeled as a K_{VCO} , which represent the gain/sensitivity of the VCO. Actually, CS-VCO has a polynomial relationship with respect to control voltage, however, in order to get quick inside of the system and avoid a more complex term from equations, it is approximated as a linear relationship instead of a polynomial relationship. Therefore, the forward path gain $G(s)$ and the feedback path gain $H(s)$ can be model as ω_u/s and $1/K(s+a)$, respectively, where $\omega_u = K_{VCO}/C_{IN}$, K is the feedback factor, and a is the power converter time constant. The expected V_{MPP} is a known value for a given light intensity and a given PV cell. In order to get this value under different light intensities, an experiment has been conducted with two PV cells connected in series and the details can be found section 4.6.1. However, when one uses the same prototype but with a different PV cell, the expected V_{MPP} value is not known a priori, unless one measure's it using a proper experimental setup. For such a case, one has to redesign the CS-VCO so that it should follow the system desired $V - f$ curve as shown in Fig. 4.3. The open-loop transfer function of this closed-loop system can be defined as

$$\frac{f_{CLK}(s)}{V_{MPP}(s)} = \frac{\omega_u (s + a)}{(s^2 + as + \frac{\omega_u}{K})}. \quad (4.8)$$

In order to incorporate the initial condition, one can expand equation (4.8) as

$$\begin{aligned} s^2 f_{CLK}(s) - s f_{CLK}(0^+) - \dot{f}_{CLK}(0^+) + a f_{CLK}(s) \\ - a f_{CLK}(0^+) + f_{CLK}(s) \frac{\omega_u}{K} = \omega_u s V_{MPP}(s) \\ - \omega_u V_{MPP}(0^+) + \omega_u a V_{MPP}(s) \end{aligned} \quad (4.9)$$

where, $f_{CLK}(0^+)$ and $V_{MPP}(0^+)$ represents the initial clock frequency and voltage, respectively.

First, in order to get the nature of solution, we have assumed that there is no delay in the feedback loop, i.e., $T_D = 0$. After rearranging equation (4.9), on can write as

$$\begin{aligned} f_{CLK}(s) = \frac{\omega_u (s + a) V_{MPP}(s) - V_{MPP}(0^+)}{(s^2 + as + \frac{\omega_u}{K})} \\ + \frac{f_{CLK}(0^+) (s + a) + \dot{f}_{CLK}(0^+)}{(s^2 + as + \frac{\omega_u}{K})}. \end{aligned} \quad (4.10)$$

To get the time domain response for a step input, equation (4.10) can be expanded into partial

fraction as

$$f_{\text{CLK}}(s) = \frac{A}{s} + \frac{Bs + C}{(s^2 + as + \frac{\omega_u}{K})} + \frac{f_{\text{CLK}}(0^+)(s + a)}{(s^2 + as + \frac{\omega_u}{K})}. \quad (4.11)$$

The derivative of the output initial condition, $\dot{f}_{\text{CLK}}(0^+)$, is neglected for simplicity. After decomposing in partial fraction, coefficients A , B , and C are obtained as Ka , $-Ka$, and $(\omega_u - Ka^2)$, respectively. After substituting the respective coefficients in (4.11), one can get

$$f_{\text{CLK}}(s) = \frac{Ka}{s} + \frac{1}{(s + \frac{a}{2})^2 + (\frac{\omega_u}{K} - \frac{a^2}{4})} \left\{ -Ka \left(s + \frac{a}{2} \right) + \left(\omega_u - \frac{Ka^2}{2} \right) + f_{\text{CLK}}(0^+)(s + a) \right\} \quad (4.12)$$

In order to get the time domain response of equation (4.12), Inverse Laplace Transform operation was performed and the final expression is shown in equation (4.13). Basically, equation (4.13) represents the variation of clock frequency over the time when the system is excited with a step input. Due to the involvement of sinusoidal terms in equation (4.13), it is not easy to draw some inferences from such a long equation.

$$f_{\text{CLK}}(t) = Ka \left\{ 1 - \exp\left(-\frac{a}{2}t\right) \cos\left(\sqrt{\frac{\omega_u}{K} - \frac{a^2}{4}}t\right) \right\} + \frac{\left\{ \left(\omega_u - \frac{Ka^2}{2} \right) + f_{\text{CLK}}(0^+)(s + a) \right\}}{\sqrt{\frac{\omega_u}{K} - \frac{a^2}{4}}} \times \exp\left(-\frac{a}{2}t\right) \sin\left(\sqrt{\frac{\omega_u}{K} - \frac{a^2}{4}}t\right) \quad (4.13)$$

In order to get a quick insight of the system, one can approximately model the transfer function of power converter as $1/K$ instead of $1/K(s+a)$, to avoid sinusoidal terms. With this assumption, equation (4.8) can be approximated as

$$\frac{f_{\text{CLK}}(s)}{V_{\text{MPP}}(s)} = \frac{\omega_u}{(s + \frac{\omega_u}{K})}, \quad (4.14)$$

and by following the above procedure, one can approximate equation (4.13) as

$$f_{\text{CLK}}(t) = f_{\text{CLK}}(0^+) \exp\left(-\frac{\omega_u}{K}t\right) + KV_{\text{MPP}}(t) \left(1 - \exp\left(-\frac{\omega_u}{K}t\right)\right). \quad (4.15)$$

The first term indicates that the initial clock frequency decays exponentially and the second term indicates that the desired clock frequency grows exponentially. At $t \rightarrow \infty$, the exponential term goes to zero and one may approximate equation (4.15) as

$$f_{\text{CLK}}(t) \approx KV_{\text{MPP}}(t) \approx f_{\text{MPP}}(t). \quad (4.16)$$

However, practically it never reaches the exact value of f_{MPP} , because the exponential term does not reach to zero value, and one can estimate the required time to reach 99% of the desired clock frequency is given by

$$t = \frac{2K}{\omega_u} \ln(10) \simeq 4.6 \frac{K}{\omega_u} \quad (4.17)$$

So, the term $\frac{K}{\omega_u}$, represents time, and one can choose ω_u in such a way that the system offers an optimum solution. This is the key parameter which defines the maximum convergence speed of an MPPT scheme.

It is to be noted that the equation (4.15) is derived by assuming there is no delay in the feedback loop. Now, let us consider equation (4.14) with delay T_D , and define it as

$$\frac{1}{\omega_u} \frac{df_{\text{CLK}}(t)}{dt} = V_{\text{MPP}}(t) - \frac{f_{\text{CLK}}(t - T_D)}{K}. \quad (4.18)$$

In order to get the time domain response, for a step input signal from 1 to 0, one can approximate equation (4.18) as given in equation (4.19). The reason for doing that, is to eliminate the $V_{\text{MPP}}(t)$ terms from the equation (4.18), as we are interested to see the behavior at $t > 0$.

$$\textcircled{a} t = 0 \left\{ \frac{df_{\text{CLK}}(t)}{dt} = -\frac{\omega_u}{K} f_{\text{CLK}}(t - T_D) \right. \quad (4.19)$$

The equation (4.19) implies that the time derivative of the function is same as the delayed function, which is nothing but an exponential function and one can verify it by inspecting

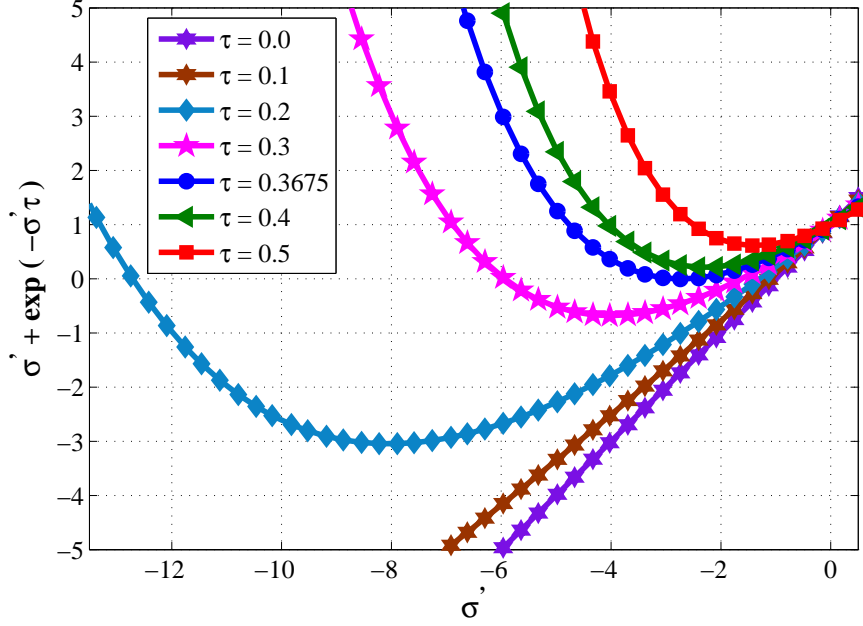


Figure 4.7: The nature of solutions of the differential equation (4.22) at different values of τ .

functions and its derivative. Therefore, a delayed exponential is still exponential in nature, but with a scaling factor of $-(\omega_u/K) \exp(-T_D)$, and one can obtain the approximate solution of equation (4.19) as follows:

$$f_{\text{CLK}}(t) = f_{\text{CLK}} \exp(\sigma t). \quad (4.20)$$

Now, from equation (4.20) and (4.19) one can get

$$\frac{\sigma K}{\omega_u} + \exp(-\sigma t) = 0. \quad (4.21)$$

As equation (4.21) can not be solved directly, one can solve it numerically by normalizing σ and T_D with $\frac{\omega_u}{K}$ and $\frac{K}{\omega_u}$, respectively, as follows:

$$\sigma' + \exp(-\sigma' \tau) = 0, \quad (4.22)$$

where σ' and τ represents normalized σ and T_D . Fig. 4.7 shows the nature of solutions of the differential equation (4.22) at different values of τ . The case, $\tau = 0$ represents no delay in the feedback loop and the case, $\tau > 0$ represents the presence of delay in the feedback loop. From

the figure, it is apparent that there exist two solutions for small values of τ and no solution for large values of τ . Which means, if the delay, T_D , is much smaller than the time constant K/ω_u , negative feedback loop can track MPPs as there exist some solutions for a smaller value of τ . As the delay increases, the two solutions approach each other and for a particular delay, two solutions converge to a single point. To calculate the optimal value of τ , one needs to differentiate equation (4.22) with respect to σ' and substitute the value of σ' back to equation (4.22). The desired value of τ , obtained is 0.3675, and it tells that if the delay is $\sim 36\%$ of the time constant K/ω_u , one can expect the fastest response. In summary, an appropriate delay in the feedback loop improves the system response, because, time delay introduces a negative phase shift in the loop transmission, and thus decreases the phase margin. A certain amount of delay brings the phase margin to an optimal value ($\sim 50-70$ degrees [76]) and will minimize the settling time. Any delays larger than this value, result in underdamped and eventually oscillatory responses that cause settling time to increase. Hence, there is an optimum value of the time delay that results in the fastest system response.

To understand the concept intuitively an example of this negative feedback mechanism for MPP tracking is illustrated in Fig. 4.6. The variation of clock frequencies is reflected as a change in output voltage of the PV cell or input impedance of the power converter. Due to such change, the error voltage and hence the clock frequency eventually reduces. This process will continue until the error voltage goes to zero. Two light conditions, light-1 and light-2 are taken into consideration and their variations change the PV cell terminal voltage, V_{PH} , which is plotted over time. Δ_{AC} and Δ_{NF} represents the delta variations of PV cell terminal voltage by the ambient conditions and the negative feedback loop, respectively. If the ambient condition changes from light-1 to light-2, the targeted maximum power point will shift from V_{MPP} to $V_{MPP,New}$, due to increase in photocurrent under light-2 condition. However, due to the inherent delay in the control loop, the clock frequency will not change immediately and hence, there will not be any variation in the input impedance of the power converter. As the input impedance is fixed and I_{PH} is increased, momentarily V_{PH} and V_e will be increased by Δ_{AC} amount. Now, f_{CLK} starts increasing as V_e is increased, which will lower the input impedance

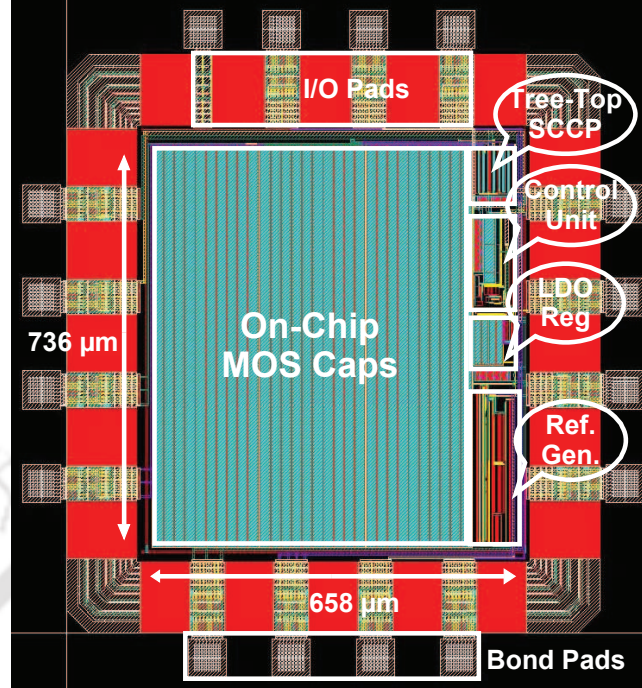


Figure 4.8: Layout of the proposed power delivery interface circuit.

of the power converter and therefore, more current can flow into the power converter. As a result, V_{PH} will be reduced by Δ_{NF} amount. The process will continue until $V_{PH} = V_{MPP,New}$. It is to be noted that the origin of the steady state error is due of the delay in the feedback loop and its magnitude will increase as delay increases. The control mechanism will be the same if one move from light-2 to light-1 instead of light-1 to light-2.

4.6 Measurement and Simulation Results

The proposed solar energy harvesting interface circuit was implemented in 0.18- μm CMOS technology and its layout is shown in Fig. 5.6. The layout dimensions of the interface circuit are 658- $\mu\text{m} \times 736\text{-}\mu\text{m}$. It is clear from the layout that the major area of occupation is mainly due to the flying capacitors. In order to validate the proposed architecture, post-layout simulations are carried out using standard foundry MOSFET models in 0.18- μm CMOS process. The input and load capacitances are chosen as 10 nF and 10 pF, respectively, to suppress input and output ripples. In order to reduce the simulation time, buffer capacitance is chosen as, 30 nF, for this

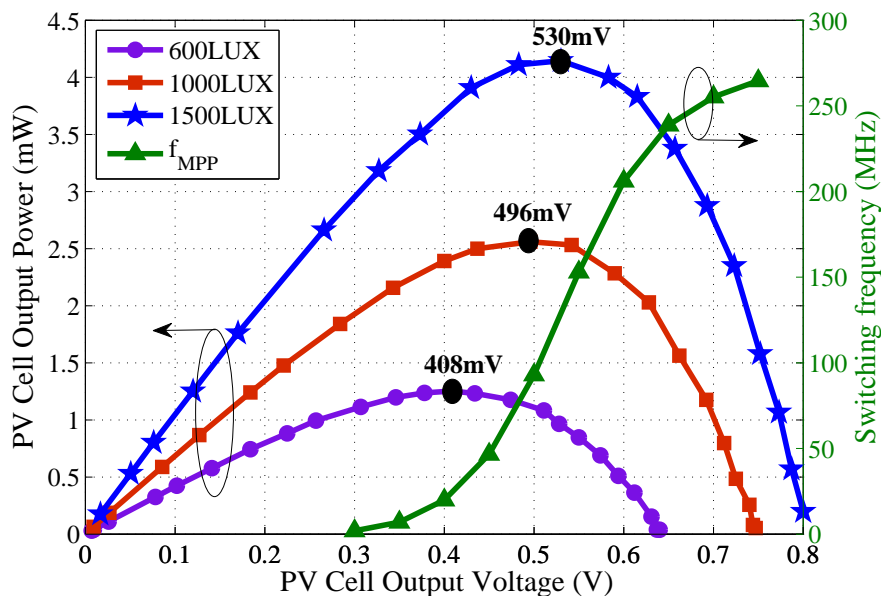


Figure 4.9: Variation of PV cell output power and power converter switching frequency with respect to PV cell terminal voltage.

implementation. However, in a real implementation, one has to choose a supercapacitor, in the order of millifarad or farad.

4.6.1 Photovoltaic harvester, CS-VCO, and power converter

An electrical equivalent model of a PV cell is used to emulate the PV cell in the simulation engine. To find model parameters of a PV cell equivalent circuit an experiment has been conducted with two series connected PV cell (Model 1-100, from Solar World Inc. [17]). The variation of output power with respect to PV cell terminal voltage for three different light conditions 600 lux, 1000 lux, and 1500 lux are plotted in Fig. 4.9. The model parameter values are: $I_{SC} = 4.01 \text{ mA}$, $R_{SH} = 1 \text{ K}\Omega$ and $R_S = 52 \Omega$ for 600 lux, $I_{SC} = 6.96 \text{ mA}$, $R_{SH} = 400 \Omega$ and $R_S = 25 \Omega$ for 1000 lux, and $I_{SC} = 10.8 \text{ mA}$, $R_{SH} = 400 \Omega$ and $R_S = 18 \Omega$ for 1500 lux, respectively. The maximum power point voltages are indicated in the figure, which are approximately 65% of their open circuit voltages. Fig. 4.9 also shows the variation of maximum power point frequency with respect to PV cell terminal voltage, which is generated from the CS-VCO.

The tracking range has been improved significantly by employing a CS-VCO instead of a [TH-1750_11610219](#)

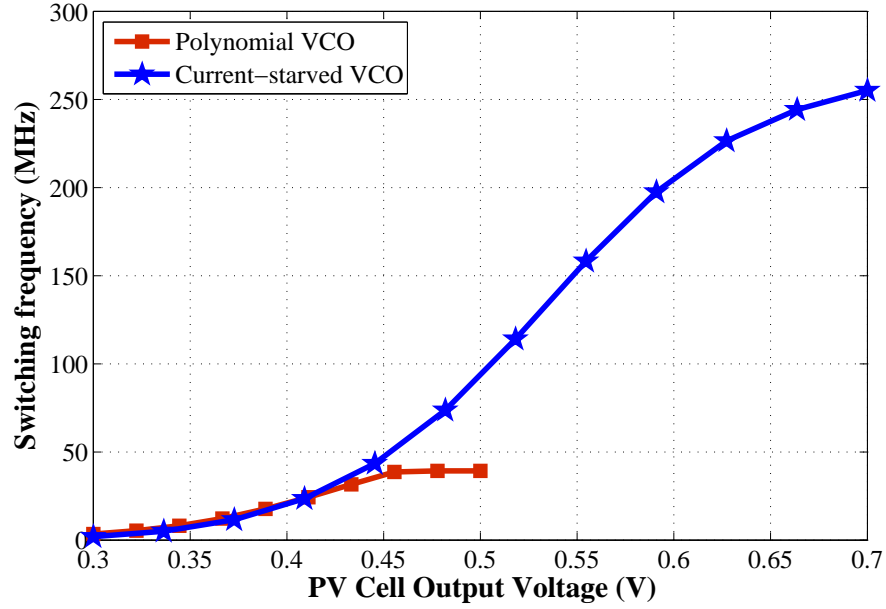


Figure 4.10: Voltage-frequency characteristics of Polynomial VCO and CS-VCO.

polynomial VCO. In order to quantify the improvement in the tracking range, the polynomial VCO of reference [56] has been reproduced in 0.18- μm technology node and simulation has been carried out with the supply voltage of 1 V. The control voltages versus switching frequencies of the polynomial VCO and the current-starved VCO are plotted in Fig. 4.10. It is apparent from the Fig. 4.10, that the polynomial VCO-frequency is uncontrollable for higher control voltages (> 0.45 V), as the op-amp involved in polynomial VCO will stop functioning for control voltages beyond 0.45 V. On the contrary, CS-VCO holds its property even at higher control voltages (up to ~ 0.65 V for this implementation), as there is no op-amp involved in CS-VCO design. In other words, by incorporating CS-VCO instead of a polynomial VCO, one could achieve a very wide input impedance tuning range MPPT system. In summary, the tracking range has been improved $\sim 57\%$ by incorporating CS-VCO in this implementation.

In order to validate the concept of MPPT discussed in section 4.3, a simulation is carried out and plotted in Fig. 4.11. Basically, it shows two independent relationships between the same physical variables, f_{CLK} and V_{PH} , that arise from two different sources: one, from the joint modeling of a PV cell and power converter and other from the CS-VCO. Three different

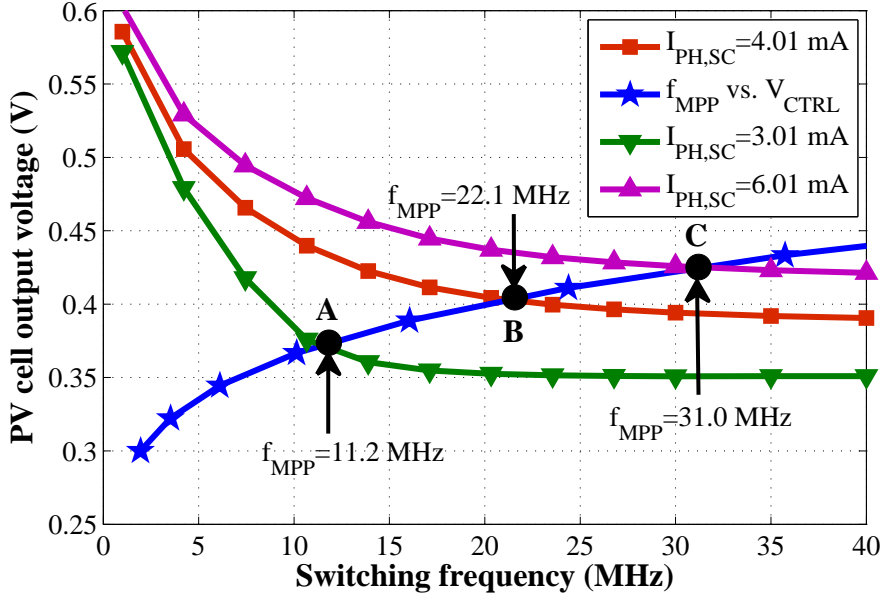


Figure 4.11: Independent relationship between f_{CLK} and V_{PH} that arises from the power converter and the VCO.

light intensities, i.e., $I_{PH,SC} = 3.01 \text{ mA}$, 4.01 mA and 6.01 mA , have taken into consideration and each of them are intersecting with the VCO dynamics ($f_{MPP} \text{ vs. } V_{CTRL}$) only on a single point as marked in *A*, *B*, and *C*, respectively. Therefore, once the loop is closed, the system will settle down to one of the operating point, *A*, *B*, or *C*, depending on the light intensity. In order to validate whether these intersection points are the maximum power points, a system level simulations are carried out and results are given in the next subsection.

4.6.2 MPPT Transients

After verifying PV cell, CS-VCO, switching converter, and other blocks individually, a combined simulation is performed to verify the MPPT functionality. To envision different light intensities, the photocurrent, I_{PH} , equivalent series resistance, R_S , and shunt resistance, R_{SH} , of the PV cell electrical model are varied from 1.01 mA to 6.96 mA , 25Ω to 52Ω , and 400Ω to $1 \text{ K}\Omega$, respectively. Fig. 4.12 and Fig. 4.13 show the transient behaviors of the PV cell terminal voltage, V_{PH} , and the power converter switching frequency, f_{CLK} , for six different light intensities. Initially, PV cell offers maximum output voltage with minimum output current to the CS-VCO and the power converter circuits. Due to this large voltage, CS-VCO generates a

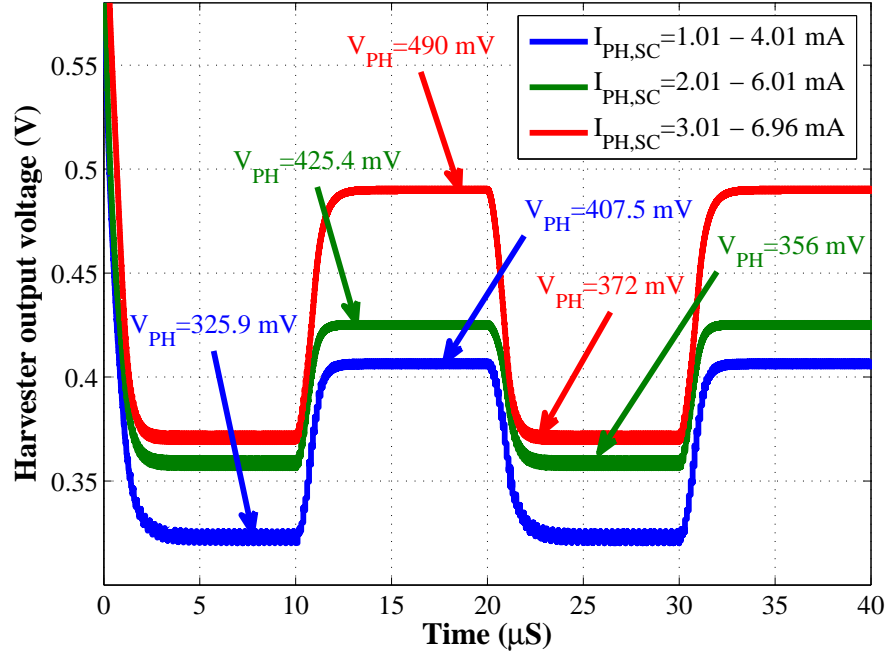


Figure 4.12: MPP tracking voltage (V_{PH}) for different light condition.

very high switching frequency, resulting in a lower V_{PH} as the converter start drawing current from the PV cell. Due to the lowering of V_{PH} , switching frequency may go down and enhance the V_{PH} again. With this back and forth delta variation of V_{PH} and f_{CLK} , negative feedback control loop will stabilize V_{PH} and f_{CLK} at a particular time, where both delta variations are almost comparable. This is eventually known as MPP voltage and frequency at that particular time. The proposed scheme successfully tracks the maximum power points with an average tracking error of $\pm 0.06\%$. Moreover, the proposed scheme takes very minimal time, approximately $12 - \mu s$, to settle at MPP even when the atmospheric condition rapidly varied from 400 lux to 1000 lux.

4.6.3 CL-LDO voltage regulator

To achieve better power supply rejection, error amplifier is implemented with an NMOS input differential pair with a PMOS current-mirror load transconductance amplifier [9]. The open loop frequency response of CL-LDO regulator for three different load currents is shown in Fig. 4.14. The open loop frequency response shows that the LDO is stable with sufficient

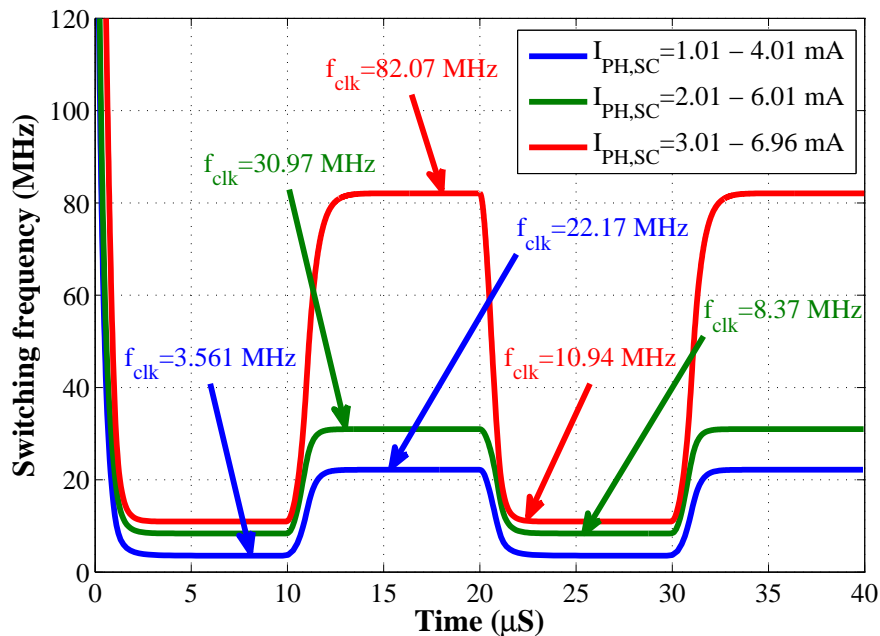


Figure 4.13: Switching frequency variation (f_{clk}) for different light condition.

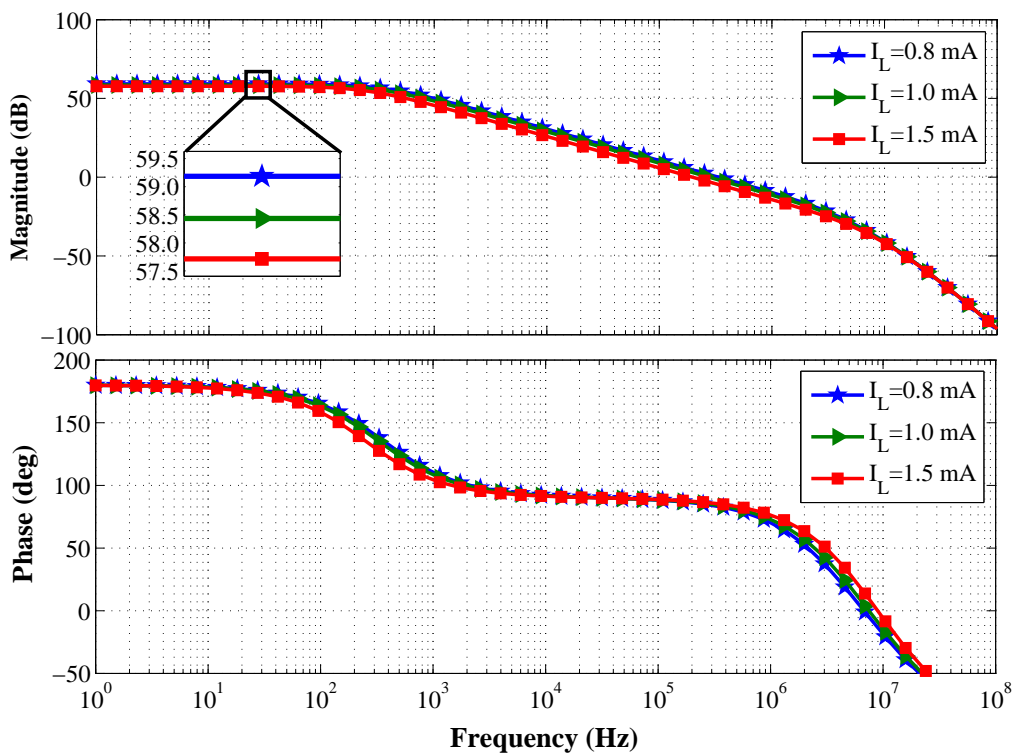


Figure 4.14: Full range open-loop AC response (0.8-1.5 mA load current).

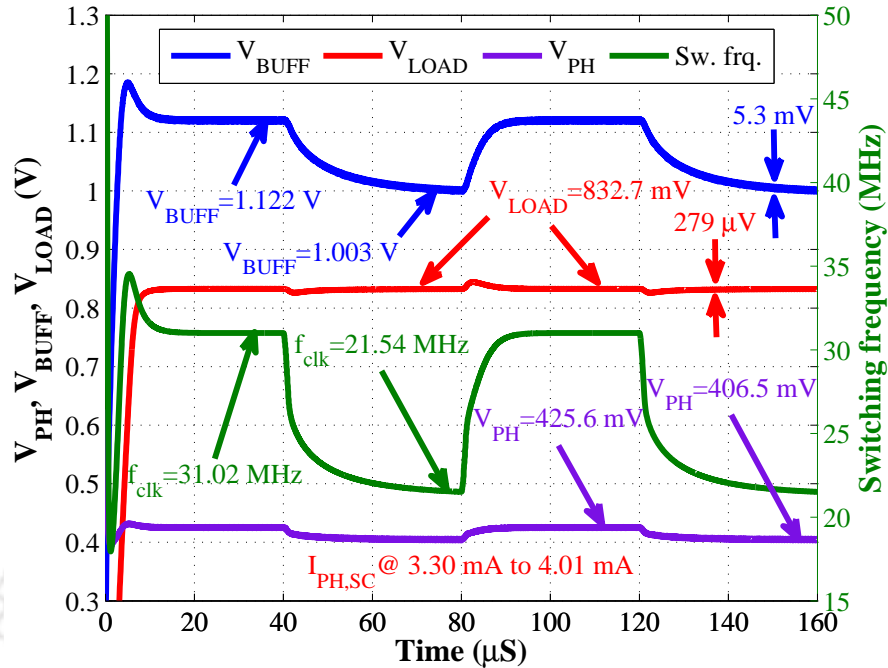


Figure 4.15: Complete system simulation after integrating all the blocks.

phase margin (90° for 0.8 mA , 84° for 1.0 mA , and 78° for 1.5 mA load currents). The open loop gain for different load currents is 59.19 dB for 0.8 mA , 58.43 dB for 1.0 mA , and 57.72 dB for 1.5 mA , respectively. The proposed architecture is designed to deliver at $833\text{ }\mu\text{A}$ load current at a load voltage of 833 mV , where the drop-out voltage is 167 mV . To measure the load regulation, a current pulse ($100\text{ }\mu\text{A}$ peak-to-peak) is applied to the load current and the achieved load regulation is 1.87 mV/mA .

4.6.4 Complete system simulation

After integrating all the individual components of power conditioning circuit, a system level simulation including all units as shown in Fig. 4.4 is performed. To emulate the light irradiance, the photocurrent, I_{PH} , is varied from 3.30 mA to 4.01 mA and the corresponding variation of PV cell terminal voltage, switching frequency, buffer voltage, and load voltages are presented in Fig. 4.15. For the PV cell terminal voltages, V_{PH} , 407 mV and 426 mV , the optimal switching frequencies achieved by control unit are 21.54 MHz and 31.02 MHz , and the buffer voltages are 1.003 V and 1.122 V , respectively. However, the load voltage is fixed at

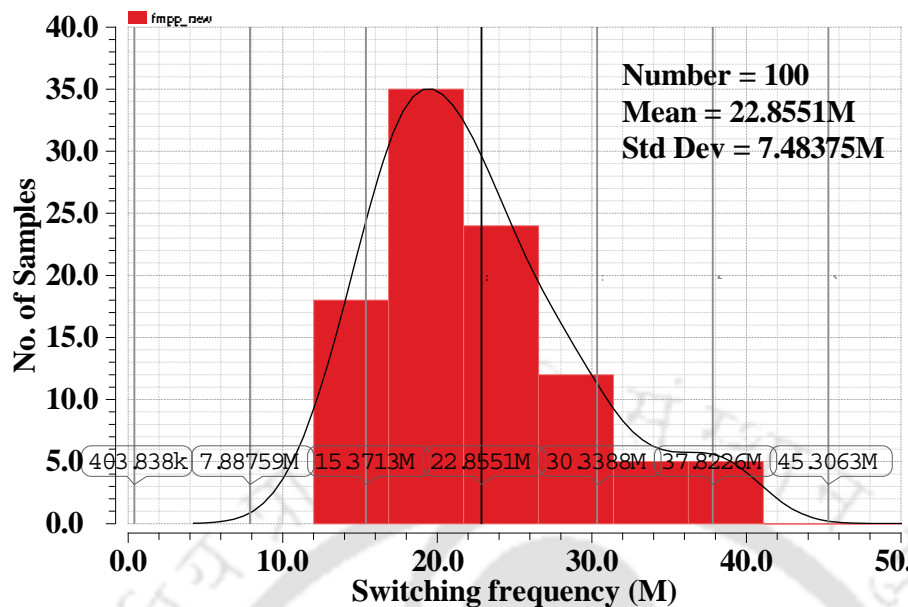


Figure 4.16: Monte Carlo analysis for maximum power point frequency, f_{MPP} , under both process and mismatch variation.

the desired voltage 833 mV. It takes 10 – 20 μ s to reach its steady state value for each light irradiance step. The interface circuit works satisfactorily once the photocurrent reaches above or equal to 3.30 mA. Otherwise, the buffer voltage may go below 1 V, and the regulator may stop working. Therefore, sufficient light condition should be provided such that $I_{PH} \geq 3.30$ mA. Ripple voltages of 297 μ V and 5.3 mV are obtained for load and buffer voltages, respectively. Therefore, the line regulation of CL-LDO is 0.05 V/V.

The VCO oscillation frequencies are generally quite sensitive to PVT variation unless special precautions are taken care. Nevertheless, due to the negative feedback, the entire system should not be very sensitive to the PVT variation. To confirm the same, a 100 points Monte Carlo analysis is carried out to investigate the variation of both process and mismatch, between die-to-die and within a die, on the maximum power point frequency, f_{MPP} , and the maximum power point voltage, V_{MPP} . The gaussian distributions of f_{MPP} and V_{MPP} at a temperature of 27°C are shown in Fig. 4.16 and Fig. 4.17, respectively. Out of 100 samples, approximately 79% of f_{MPP} and 71% of V_{MPP} fall within $\pm 1\sigma$ and almost 94% of f_{MPP} and 98% of V_{MPP} fall within $\pm 2\sigma$ of the mean value. The resulting standard deviation of V_{MPP} is 1.2% of the mean value,

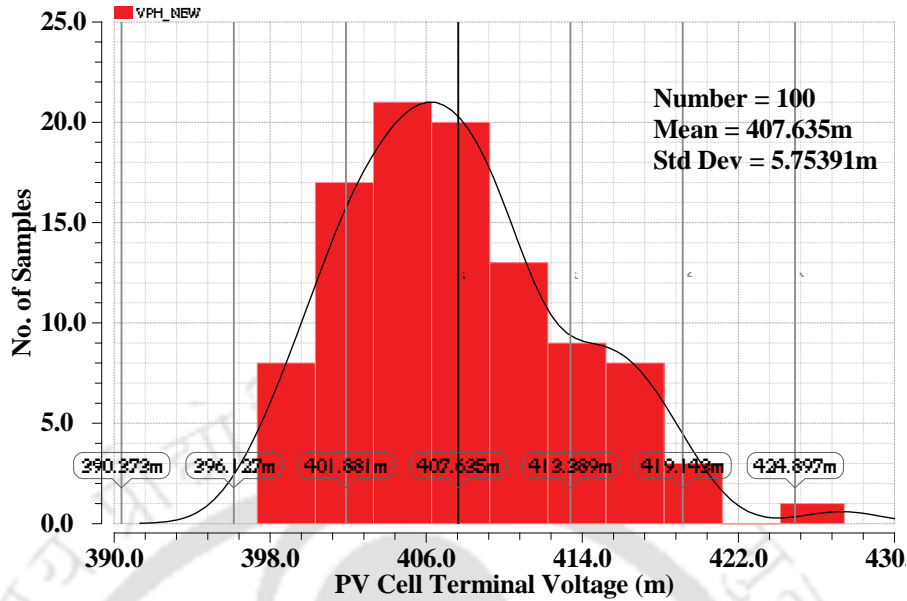


Figure 4.17: Monte Carlo analysis for maximum power point voltage, V_{MPP} , under both process and mismatch variation.

i.e., 407.63 mV. These results indicate that the process variations make very minimal impact on maximum power point voltage and hence, one can expect good die yield with proposed MPPT scheme.

Table 4.2 shows the performance comparison among the state-of-the-art micro-scale energy harvesting interface circuits for IoT node. The proposed architecture does not require any off-chip components like inductor or capacitors. Chip-area and PCB-area are not compared as the technology nodes are different. The highest switching frequency achieved in this work will allow smaller component size and chip-area. The proposed design stands out with respect to tracking error, tracking speed, MPPT overheads, MPPT consumption, and implementation complexity. The end-to-end efficiency is not compared as the power converter topologies (inductive and capacitive) are different. Among the capacitive boost converter, the proposed one has the higher power delivery capability and higher conversion efficiency. This power management system provides a regulated output voltage of 0.833 V, with a maximum output power of 833 μ W.

4.7 Summary and Conclusions

This work presented an efficient MPPT scheme for micro-scale solar energy harvesting system for powering an IoT node. The architecture employed single phase tree-topology charge pump as a power converter that has better charge sharing time and charge transfer capability. The proposed MPPT scheme was able to track the maximum power point successfully with a tracking error of 0.1 – 0.6%. The proposed tracking approach takes few microsecond to track MPP and avoids extra hardware such as an integrator, current sensor, and microcontroller. This work does not address the startup issue and made an assumption that the supercapacitor is initially charged to power up the system. The approximate overhead area and power consumed by this tracking scheme are $67 - \mu\text{m}^2$ and 467 nW and in terms of percentage 0.013% and 0.1% (under 600 Lux), respectively. It is also to be noted that by incorporating MPPT scheme $125 \mu\text{W}$ of power (0.45 J per hour) is additionally harvested when the ambient light intensities are varied from 2.01 mA to 4.01 mA , and it would be even higher if $I_{PH,SC}$ variation is large.

Table 4.2: Performance Comparison among state-of-the-art MPPT scheme suitable for micro-scale energy harvesting systems

| Parameters | Park [73] | Simjee [13] | Shao [53] | Qiu [77] | Sourav [72] | Chao [56] | This work |
|-------------------------------|------------------------------------|-------------------------------|------------------------------------|----------------------------|--|----------------------------------|------------------------------------|
| Technology node | Discrete ICs | Discrete ICs | 0.35 μm | 0.25 μm | 0.35 μm | 45 nm | 0.18 μm |
| Power generated by PV cell | 400 mW@ 1000 lux | 450 mW@ not described | 785 μW @ 1141 lux | 10 mW@ not described | 340 μW @ 1500 lux | 444 μW @ 2152 lux | 1.25 mW@ 600 lux |
| MPP Voltage (V) | 3.50@ $V_{OC}=4.05\text{V}$ | 5.0@ $V_{OC}=7.1\text{V}$ | 2.74@ $f_{MPP}=2.1\text{MHz}$ | 1.4@ $V_{OC}=2\text{V}$ | 0.410@ t_{CH}, t_{DCH} $=1.86\mu\text{s}, 470\text{ns}$ | 0.364@ $f_{MPP}=11\text{MHz}$ | 0.408@ $f_{MPP}=22\text{MHz}$ |
| Energy buffer(s) | 70mAh battery & two 22F SC@2.3V | 100F SC@2.5V | 125mAh battery | 3V battery | 3.3V battery & SCs | 1 μF SC @0.9V | 30nF capacitor @1V [♣] |
| Load condition | 4.1V@10-50mA | not mentioned | 4.4V@120 μA | 5.0V@2.0mA | 1.88V@300 μA | 170 μW | 833 μW |
| Converter type | IBC@ $\eta=85\%$ | IBC@ $\eta=65\%$ | CBC@ $\eta=67\%$ | IBC@ $\eta=87\%$ | IBC@ $\eta=83\%$ | CBC@ $\eta=40\%$ | CBC@ $\eta=70\%$ |
| MPPT scheme | FOCV@ K_{PV} = not described | FOCV@ $K_{PV}=0.70$ | HC method | HC method | P&O method | NFC method | Inherent NFC |
| Tracking Error | ~ 15% | ~ 5-11% [#] | not described | not described | 4% | ~ 0.2-0.69% | ~ 0.1-0.6% |
| Tracking speed | not described | not described | not described | not described | ~ 30 s | ~4.5-7.0 μs | ~ 12 μs |
| MPPT overheads | MCU, PS, Comp. | ADC, MCU, PS, Comp., PV-PC | CS, Comp., DFF TGs, logic gates | MCU, Comp. CS, ZCD | MCU, Comp. DFFs, ZCD | Integrator P-VCO | CS-VCO |
| MPPT consumes | 500 μA @3.3V | 2.93mA@ V_{PH} [¶] | Not discussed | 3.5 μA @1V | 5 μW | 180 μW | 467 nW |
| Fully-integrated | No | No | Yes | No | Yes [♣] | Yes | Yes |

PS: Photosensors; CS: Current sensor; ZCD: Zero current detector; Comp.: Comparator; SC: Supercapacitor; IBC: Inductive boost converter; CBC: Capacitive boost converter; PV-PC: PV pilot cell; TG: Transmission gate; P-VCO: Polynomial VCO; t_{CH} : inductor charging time; t_{DCH} : inductor discharge time; [♣]: to reduce simulation time nF capacitor has been chosen; [¶]: consider MCU and PS; [#]: Compared to P&O; [♣]: inductor footprint of $12 \times 12 \text{ mm}^2$.



5

Efficient Power Management Architecture for Solar Energy Harvester

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5.1 Introduction

An efficient micro-scale power management architecture for self-powered wireless-sensor node is presented in this chapter. To supply the load requirements, the proposed architecture utilizes a single DC-DC converter when there is enough ambient energy and two DC-DC converters when there is insufficient ambient energy. By regulating the intermediate voltage, system efficiency has been improved by $\sim 9\%$ when two DC-DC converter are used. Moreover, the proposed scheme avoids the linear regulator and present a complete on-chip switched capacitor based architecture in order to achieve higher end-to-end efficiency. The entire power management system has been designed using $0.18\text{-}\mu\text{m}$ CMOS technology node and the circuit simulations demonstrate that the proposed architectural changes bring in a system efficiency of 82.4% under different light conditions. In addition to that, a hardware setup is created using commercially available ICs and solar energy harvesters, in order to validate the proposed power management system. The measurement results indicate that the system is practically realizable.

5.2 Traditional Power Management Architecture

Traditionally people were using two stages of DC-DC converters in between the harvester and loads as shown in Fig. 5.1. The first converter (DC-DC_1) is used to present optimal input impedance to the harvester for transferring maximum power from the harvester to the interface circuit as well as for boosting the input voltage to a level such that it meets the load requirements. Whereas, the second converter (DC-DC_2) is used to provide a clean regulated supply to the noise sensitive analog/RF blocks. Therefore, both the input and output voltages of the interface circuits are set differently by the system requirements. In order to have self-powering capability, energy harvesters are used along with the battery. For vibrational or RF harvester, a rectifier circuit is needed for converting AC output to a DC output voltage. To protect the battery from under voltage (UV), over voltage (OV), and over temperature (OT), a battery management unit is required. To inform the load regarding the status of battery, a

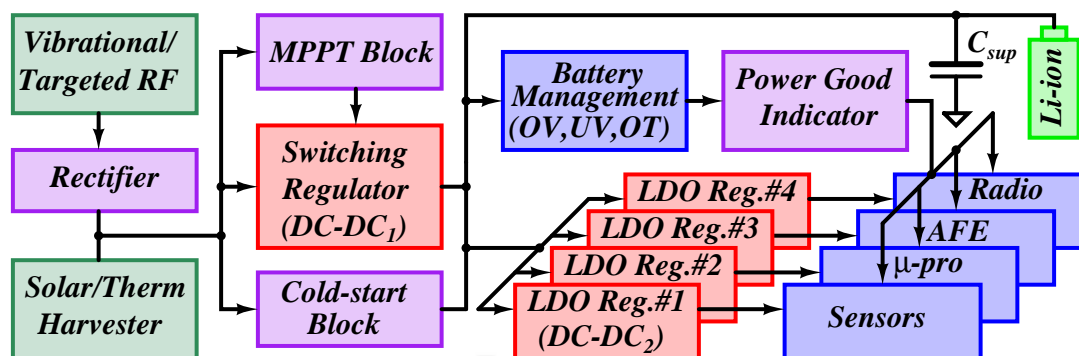


Figure 5.1: Typical power management unit of an IoT node.

power good indicator is also required. A cold-start block has been incorporated to bring-up the system from the sleep-state to an active-state, when the harvester output voltage is lower than the MOSFET threshold voltage. Finally, in order to extract maximum power from the harvester, one needs to offer optimal impedances dynamically, and to do that one needs a maximum power point tracking (MPPT) block.

In this architecture the energy is processed twice before it reaches to the load circuits, and the overall efficiency will be $\eta_{DC-DC,1} \times \eta_{DC-DC,2}$ and its typical values lies between 65 – 75% [23, 10]. Therefore, improving the efficiency of either one of these two converters, will improve the system efficiency and conversely, degrade the system efficiency. Extensive research has been carried out and a number of article has been reported on switching regulators [23, 47, 77] and LDO regulators (LDR) [9, 78] for power management applications. Among them Qiu et. al. [77] and Chung et. al. [78] are able to achieve a maximum efficiency 85% for both switching and LDO regulators. Therefore, one can expect a maximum end-to-end efficiency of $\sim 72\%$ for a two-regulator system, which means, ideally $\sim 28\%$ power is consumed (or dissipated) by the power management circuit itself. It is to be noted that, this much amount of power will consume by the interface circuit even when input has enough or more than enough ambient energy to supply the load requirements.

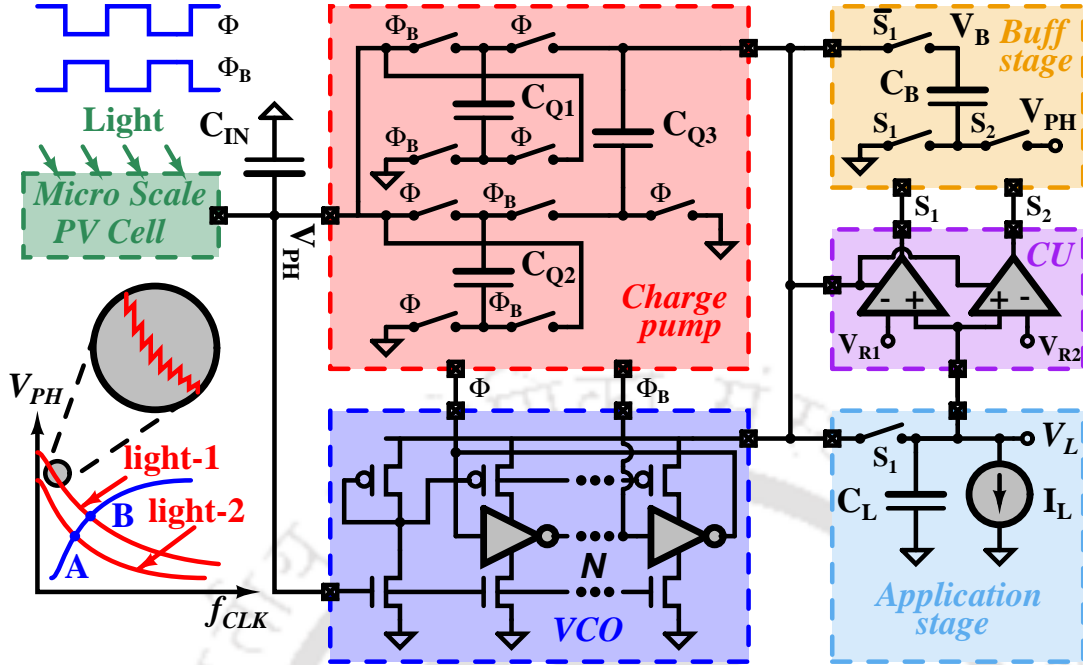


Figure 5.2: Proposed power management architecture for IoT node.

5.3 Proposed Architecture

One of the key issues with this architecture is that, the first converter has a fixed voltage conversion ratio, which means that its output voltage will vary with the input voltage, i.e., with ambient condition. As a result, the efficiency of the second converter, i.e., an LDO, and that of the entire system will also vary with the ambient condition and much of the extracted power may simply be dissipated within the LDO, which is not desirable for any application. Another key issue is that, it utilizes two DC-DC converter even if there is an enough ambient energy to power the load circuit. In order to address these issues, in this chapter an efficient architecture has been proposed to maintain the regulation at the intermediate node, i.e., between these two converters, when there is a change in ambient conditions and an alternate scheme which utilizes single DC-DC converter when there is enough ambient condition to power the load.

The proposed power management architecture is shown in Fig. 5.2. It comprises of a switched capacitor boost converter, a current-starved voltage control oscillator (CS-VCO), a control unit (CU), a buffer stage, and an application stage. In this work Photovoltaic (PV) cells

are used as the energy source for powering the sensor node. A tree-topology charge pump [47] is adopted as switching converter for better charge transfer capability, compared to a linear charge pump topology, and an array of current starved inverters along with phase shifters are used for generating non-overlapping clock signals. The control unit comprises of a reference generator, analog comparators, and logic gates to generate required control signals for the system. The reference generator, generates two reference voltages V_{R1} and V_{R2} , where V_{R1} is greater than V_{R2} by few tens of mV . Their difference should be higher than the op-amp offset voltage, in order to avoid unwarranted triggering of the comparator. The buffer stage has two modes: one is, storage mode (when $S_1 = 1$ and $S_2 = 0$) and another is converter (DC-DC) mode (when $S_1 = 0$ and $S_2 = 1$). During the storage mode, it will store the excess energy into a buffer capacitor C_{STO} and during the converter mode, it will act as a linear charge pump circuit, which will pump the stored energy into the application stage. The storage mode will be activated once there is enough ambient energy to supply the load and converter mode will be activated once there is insufficient ambient energy to supply the load. In order to bring-up the system from the sleep-state to an active-state, one needs a start-up circuit, which will generate an auxiliary voltage higher than the MOSFET threshold voltage. Previous works report start-up circuits [69, 70] and therefore, this implementation does not focus the startup issues but assumes that the supercapacitor (C_B) is initially charged.

The proposed architecture utilizes single DC-DC converter in order to maintain regulation at both the input and the output. To adjust the input impedance of the power converter, switching frequencies are varied from few MHz to tens of MHz . Once the input impedance of the power converter is matched with the harvester impedance, maximum power transfer will be taking place from the harvester to the interface circuit. The frequency at which maximum power transfer take place is known as maximum power point frequency, f_{MPP} . In order to realize it, an inherent negative feedback control loop is utilized as discussed in [56], which comprises of a PV cell, a power converter, and a voltage control oscillator. To understand the concept, Fig. 5.2 illustrates two independent relationship between the same physical variables, f_{CLK} and V_{PH} , that arise from different sources: i) change in converter input impedance and

hence V_{PH} with f_{CLK} (the red lines) under two different light conditions, and ii) the change in oscillation frequency f_{CLK} with PV cell voltage (the blue line). It may be noted that, for a given light intensity, there is only one intersection point (either A or B) between these two curves and the system will settle at that operating point. In other words, at zero switching frequency, there will be no charge transfer takes place through the power converter and thus V_{PH} will be the open circuit voltage, V_{OC} . As the switching frequency increases, the charge transfer take place and V_{PH} will begin to reduce since the input impedance of the power converter decreases. On the contrary, the oscillator frequency is reduced as V_{PH} starts decreasing. This brings the possibility of an equilibrium point (either point A or B), where both curves will intersect each other and the circuit will lock on that particular switching frequency. In order to make sure that the intersection points are indeed the maximum power point, one has to design the VCO carefully, such that it touches all f_{MPP} points for the given frequency range.

In order to provide regulated power supply when there is enough ambient energy to supply the load, a scaled version of the load voltage is compared with the internal reference voltages, V_{R1} and V_{R2} . To connect the charge pump either to the application stage (when $V_L < V_{R1}$) or to the buffer-stage (when $V_L > V_{R1}$), two control signals, S_1 and S_2 , are generated. Due to the complementary switching between buffer and the application stages, one could expect few tens of mV supply ripple along with the regulated power supply. The magnitude of this ripple depends on the op-amp offset voltage and the delay in feedback loop. On the contrary, if there is insufficient ambient energy to supply the load, i.e., $V_L < V_{R2}$, control signals will connect both the charge pump and the buffer stage (converter mode) with the application stage in order to maintain the load regulation. Therefore, when there is enough or more than enough ambient energy to supply the load, proposed architecture has utilized single DC-DC converter (i.e., charge pump) and store excess energy into a buffer stage, and the architecture has utilized two DC-DC converter (i.e., charge pump and buffer stage) when there is insufficient ambient energy to supply the load. The detailed circuit implementation and operations of the proposed architecture are discussed in the next section.

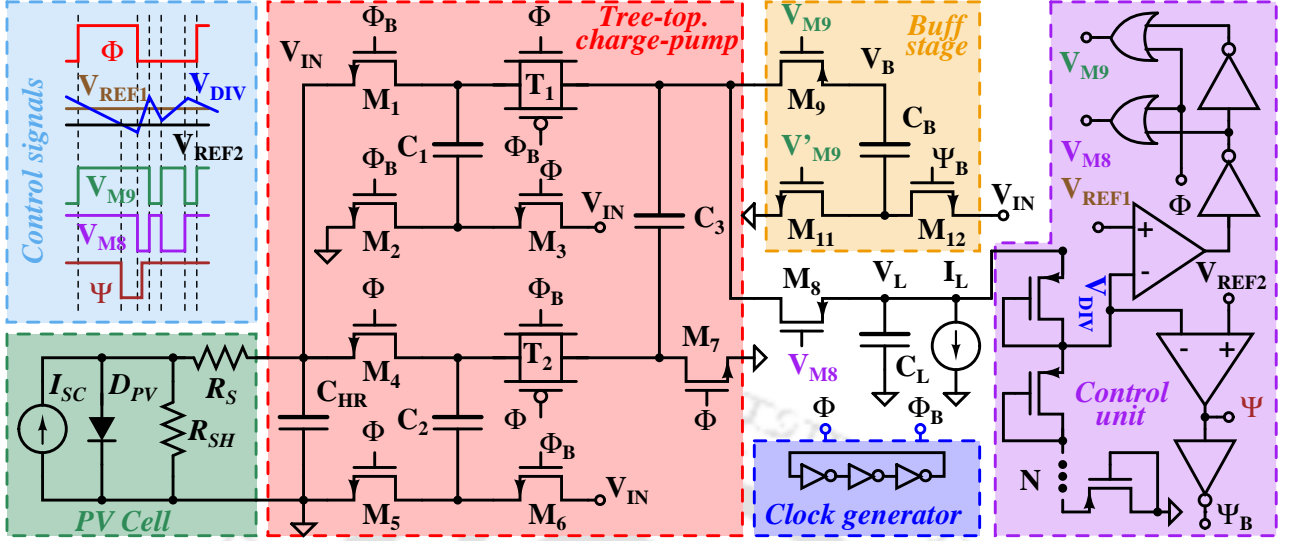


Figure 5.3: Circuit diagram of the proposed power management architecture.

5.4 Circuit Implementation

Fig. 5.3 shows the complete circuit diagram of the proposed power management architecture. To realize charge transfer switches (CTSs), n-MOS and p-MOS transistors, and transmission gates are employed. Placement of respective CTSs are made based on their terminal voltages in order to get lower on resistance [79]. Pumping capacitors are realized by on-chip MOS gate capacitors to achieve compact chip area. Current starved inverters are employed to make the ring oscillator and phase shifter circuits are used to generate non-overlapping clock signals as shown in Fig. 5.5. In order to drive heavy load (gate capacitor of the CTSs) with least propagation delay, buffer stages are added after the phase shifter. The buffer stage consists of a series of progressively sized inverters and its propagation delay will be minimized when each stage bears the same effort [51]. In order to get a scaled version of load voltage with low power consumption and small area, a voltage divider is formed by cascading PMOS transistors in subthreshold regime instead of a traditional resistor divider circuit. Two analog comparators are used to compare the scaled load voltage, V_{DIV} , with two reference voltages, V_{REF1} and V_{REF2} . Depending on which comparator triggers, power converter will connect either buffer stage or application stage. A two-stage open loop transconductance amplifier with push-pull

inverters in cascade, is used to realize the comparator circuit, as described by Allen in [76]. However, spacial care has been taken into consideration to realize high speed (> 50 MHz) as well as low voltage ($V_{DD} = 1$ V) applications. CMOS inverters and logic gates are used for generating complementary switching signals for utilizing the buffer stage either as a storage mode or as a converter mode. Due to the presence of a switching converter in between the harvester and load, harvester voltage will experience some ripple, and one can suppress it by placing a capacitor, C_{HR} , in between the harvester and switching converter.

During the positive half cycle of clock Φ , capacitor C_2 will be charged from the harvester and capacitor C_1 will be discharged to the capacitor C_3 . While, in negative half cycle of clock Φ , capacitor C_1 is getting charged from the harvester and capacitors C_2 and C_3 along with V_{PH} will discharge either capacitor C_{LOAD} or C_{STO} , depending on the control signals V_{M8} and V_{M9} . In order to generate these control signals, $Comp_1$ compares V_{DIV} with V_{REF1} and triggers either V_{M8} or V_{M9} during the negative half cycle of Φ , and their corresponding timing diagrams are shown in Fig. 5.3. If V_{DIV} is lower than V_{REF1} during the negative half cycle of Φ , V_{M8} will trigger the M_8 transistor and V_{M9} will turn off both M_9 and M_{11} transistors, in order to maintain load regulation. Once the input energy meets the supply requirements, i.e., $V_{DIV} > V_{REF1}$, M_8 will be turn off and $M_{9,11}$ will be turned on for storing the excess energy. Therefore, due to complementary switching between application stage and buffer stage, V_{LOAD} is regulated and the remaining excess energy, is stored in the storage capacitor C_{STO} , for future uses. Now, if V_{DIV} is even lower than V_{REF2} , that means, the scavenging energy is not sufficient to meet the load requirements, a control signal Ψ will trigger the M_{12} transistor, which will then allow the discharge of C_{STO} to the C_{LOAD} in order to mitigate any imbalances between available input energy and the output energy. In order to validate this idea, a system level simulation is carried out and a hardware setup is created using commercially available ICs, capacitors, and solar mini-panels and they are described in the section 5.6.6.

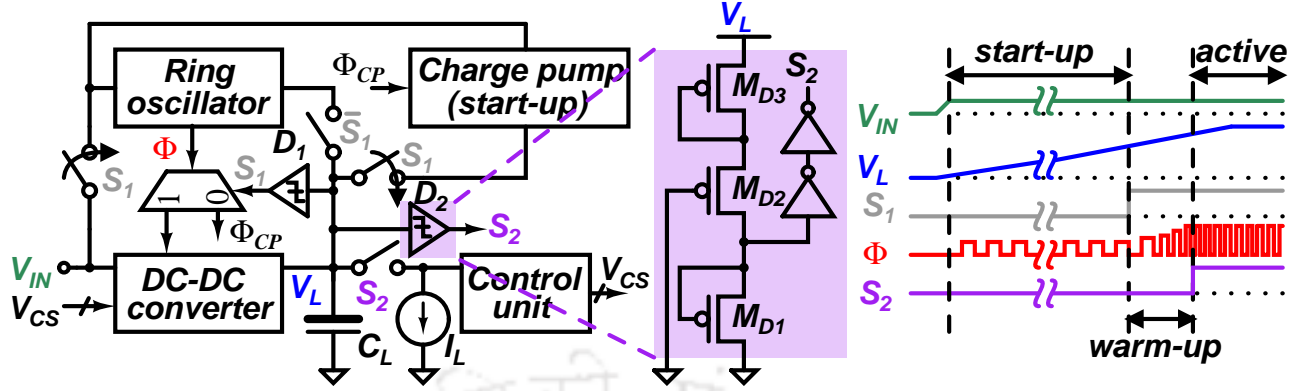


Figure 5.4: Block diagram of the proposed system architecture and the waveforms during its operation sequence.

5.5 Start-up mechanism of the Proposed Power Management Unit

The major bottleneck in any self-powered system is, how to bring-up the system from the sleep-state to an active-state if the input voltage is lower than the MOSFET threshold voltage. One requires a startup mechanism to overcome this problem. The start-up circuit generates an auxiliary voltage which is higher than the MOSFET threshold voltage. Extensive research has been carried out on the startup mechanism [10, 25, 23, 80, 69]. However, very few of them [80, 69] are suitable for on-chip solutions and therefore, we propose an on-chip self-startup mechanism for solar energy harvesting system. The detailed block diagram of the proposed power management unit with startup mechanism is shown in Fig. 5.4. It comprises of DC-DC switching converter, a low voltage ring-oscillator, a charge pump circuit for start-up, voltage detectors, and a control unit. The initial status of switches (i.e., on or off) are shown in figure, when these are controlled by control signals S_1 and S_2 .

Basically, there are three operation modes - start-up, warm-up, and active, which are controlled by detector's triggering voltages. During the start-up mode, S_1 control signal connects the inputs to the ring oscillator and charge pump circuit, and disconnects ring oscillator from the load capacitor, whereas S_2 control signal disconnects the control unit, load circuit, and the ring oscillator from the load capacitor C_L . Now, the load capacitor, C_L , will be charged by

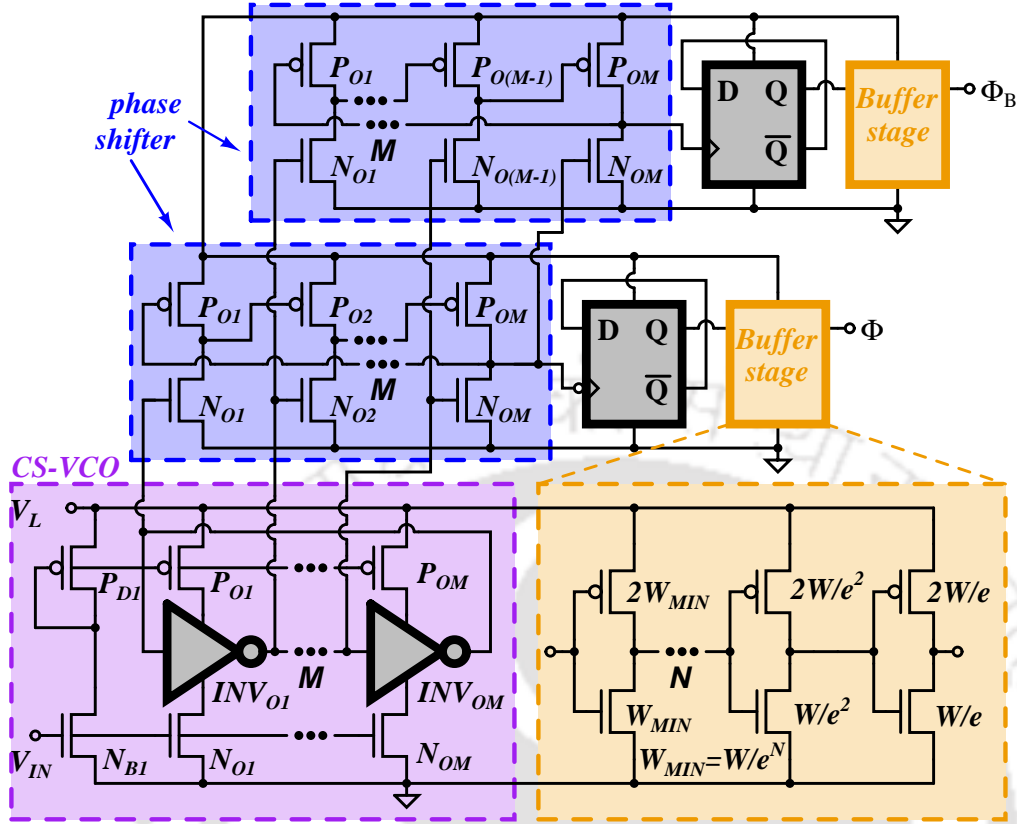


Figure 5.5: Non-overlapping clock generator circuit.

the charge pump circuit and rises the load voltage. Once the load voltage reaches the trigger voltage of detector (D_1), S_1 control signal changes its state and disconnect the start-up charge pump from the load capacitor and ring oscillator, and establishes two connections: one, in between the ring oscillator and DC-DC converter and another in between load capacitor and ring oscillator. This is the warm-up mode, where the DC-DC converter charges the load capacitor. Once the DC-DC converter starts transferring charges from the harvester to the load capacitor, the load voltage is increased, which will trigger the D_2 detector to establish connections to supply the load circuit and to initiate control unit. This is the active mode of operation.

The minimum start-up voltage of a power management unit (required to bring up from the sleep mode to the active mode) will be that voltage at which the ring oscillator starts oscillating between 0 to V_{IN} . Fig. 5.5 shows the circuit diagram of a non-overlapping clock generator. An array of five-stage current starved inverters ($M = 5$) and two phase-shifters are used to achieve

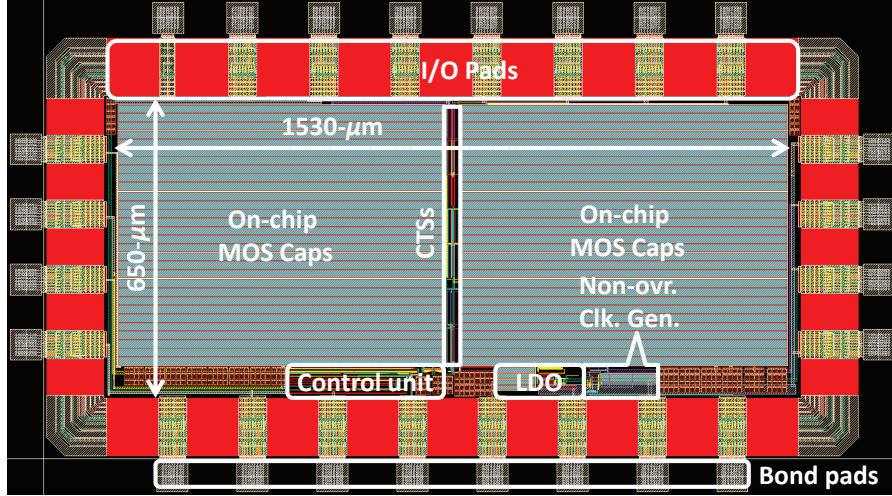


Figure 5.6: Layout of the proposed power management interface circuit.

the desired clock frequencies for maximum power point. In order to get 50% duty cycle, D -flip flops are used after the phase shifter circuits. Voltages V_L and V_{IN} are used for power supply and for controlling the oscillation frequency, respectively. The (W/L) of P_{D1} and N_{B1} are kept at $(0.36/0.18) \mu\text{m}$ and (W/L) of $P_{O1} - P_{OM}$ and $N_{O1} - N_{OM}$ are kept at $(1.80/0.18) \mu\text{m}$ and $(0.90/0.18) \mu\text{m}$, respectively. The (W/L) of PMOS and NMOS of current starved inverters ($INV_1 - INV_M$) are kept at $(0.90/0.18) \mu\text{m}$ and (W/L) of $P_{P1} - P_{PM}$ and $N_{P1} - N_{PM}$ are kept at $(0.72/0.18) \mu\text{m}$ and $(0.36/0.18) \mu\text{m}$, respectively, for this implementation. A reduced load clock load static master-slave register is used to realize $D - FF$ [81]. To drive heavy loads, an array of progressively sized inverters are incorporated after the $D - FF$ and their sizes are given in the figure itself, where, W represent the width of combined power transistors which are driven by the clock generator and e represents each stage efforts. A detailed discussion of progressive sizing inverters can be found in [51] and [67]. On-chip three-stage two-branch charge pump [41] is used for this application, as it offers better charge transfer capability with lower switching frequency. A reference-less low-power CMOS voltage detector circuit, described in [80], is used for voltage detection as shown in Fig. 5.4. By changing the appropriate length and width of M_{D1} and M_{D2} , one may vary the triggering voltages of the detector.

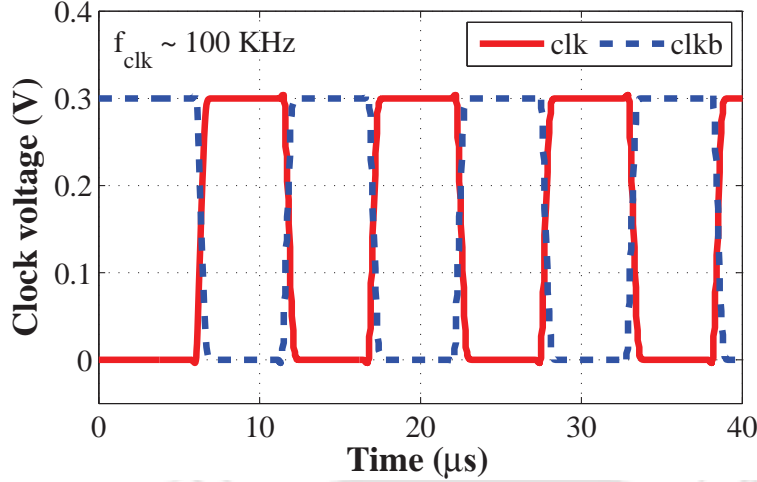


Figure 5.7: Simulated waveform of clk and clkb under 300 mV supply voltage.

5.6 Measurement and simulation results

The proposed power management interface circuit is designed and simulated in 0.18- μm CMOS technology and its layout is shown in Fig. 5.6. The layout dimensions of the interface circuit is 1530 – μm \times 650 – μm and the major area of occupation is mainly due to the pumping capacitors. Post-layout simulations are carried out using standard foundry MOSFET models. The sizes of the power transistors (W/L) and pumping capacitors are chosen as 600 $\mu\text{m}/0.18\mu\text{m}$ and 500 pF, respectively. In order to suppress the input ripples, C_{IN} is chosen as 12 nF and to reduce the simulation time, buffer capacitor C_B and load capacitor C_L are chosen as 30 nF and 10 nF, respectively.

5.6.1 Non-overlapping clock generator

To bring up the system from the off-state to active-state, it is very important that the ring oscillator employed must have rail to rail oscillation to transfer charge from the harvester to the load capacitor. The minimum input voltage required for the rail to rail oscillation is 90 mV. As the supply voltage is much lower than the MOSFET threshold voltage (~ 450 mV in 0.18 μm), all the devices in the ring oscillator will be in the sub-threshold region, which will degrade the output current drivability and the oscillation frequency. To improve the current drivability and

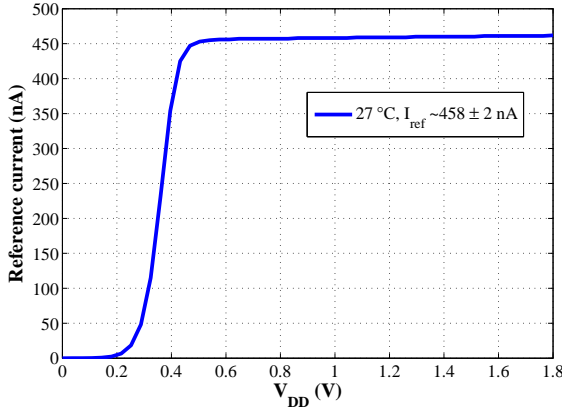


Figure 5.8: Simulated DC I-V curve of the current reference.

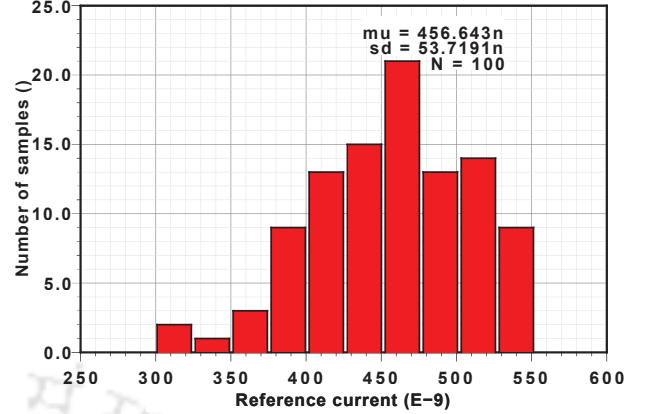


Figure 5.9: Monte carlo simulation results of the constant current reference circuit.

to achieve higher oscillation frequency, we have chosen a start-up voltage of 300 mV , for this application. Fig. 5.7 shows the simulated waveform of clk and $clkb$ of the ring oscillator under 300 mV supply voltage. The oscillation frequency achieved by this input voltage is 100 KHz , with a cost of 60.54 nW power consumption.

5.6.2 CMOS current reference circuit

The simulated DC I-V curve of the current reference circuit is shown in Fig. 5.8. The reference current has a very small dependency (i.e., a maximum of 4 nA) on the supply voltage (0.5 – 1.8 V). The variation of reference current was reduced by keeping longer channel length MOS (1 – μm). To keep all the transistor in sub-threshold region, proper transistor sizing and biasing are needed. Fig. 5.9 shows the monte-carlo simulations for 100 samples. Out of 100 samples, 21 samples are lie in the range of 450 – 475 nA , where the nominal value of the reference current is 458.3 nA .

5.6.3 Voltage detector

Another key building block of the proposed architecture is the voltage detector. The simulated waveform of voltage detectors, D_1 and D_2 , are shown in Fig. 5.10. In this design W/L of M_{D1} and M_{D2} for the detector D_1 are kept at $(88/0.18)\mu m$ and $(0.24/2.4)\mu m$, respectively, for achieving a trigger voltage of 690 mV . Whereas W/L of M_{D1} and M_{D2} for the detector D_2

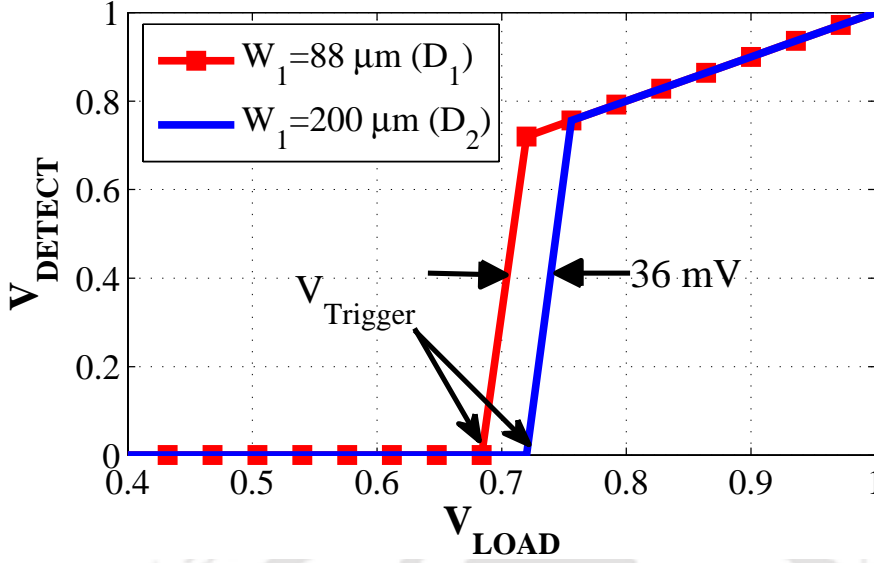


Figure 5.10: Simulation results of voltage detectors D_1 and D_2 .

are kept at $(200/0.18)\mu\text{m}$ and $(0.24/2.4)\mu\text{m}$, respectively, for achieving a higher trigger voltage at 725 mV . The W/L of M_{D2} and M_{D3} are kept same for both the detectors. The difference of triggering voltage of D_1 and D_2 are kept at 36 mV for this implementation and one may change this gap by choosing appropriate sizes for the MOS transistors.

5.6.4 Tree-topology charge pump circuit

To verify the relationship between QP switching frequency and its output power, simulations are carried by sweeping the switching frequencies from 1 MHz to 80 MHz . The simulation results for different values of V_{IN} have been plotted in Fig. 5.11. At lower switching frequencies (from 1 MHz to 20 MHz), the output power increases linearly, whereas, at higher frequencies (from 30 MHz to 80 MHz), the charge sharing is incomplete and the output power is saturated. Therefore, the switching frequencies are kept below 30 MHz to guarantee complete charge sharing within the given clock cycle. It is to be noted that, the input impedance of the power converter depends on its switching frequency, thereby, one has to choose a switching frequency such that, harvester can transfer maximum power to the harvester.

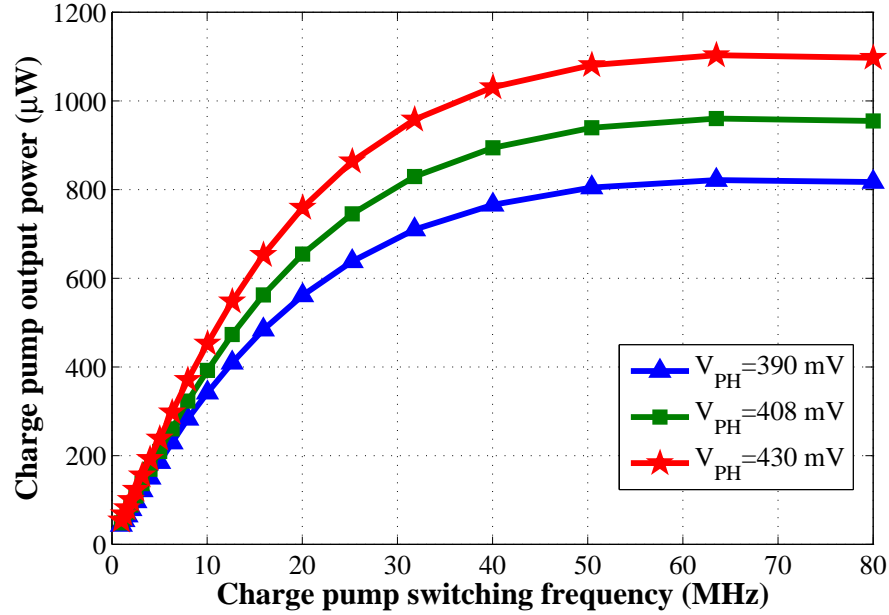


Figure 5.11: Charge pump output power vs. switching frequency.

5.6.5 Complete System Simulation

After integrating all the individual components of energy processing circuit, a system level simulation is carried out to quantify its benefits. First, we have simulated the complete system under enough ambient energy and afterwards have examined the behavior when there is insufficient ambient energy for a small period of time.

5.6.5.1 Under sufficient ambient energy

In such a light condition, the system will utilize only a single DC-DC converter to maintain regulation at the load and the excess energy will be preserved in a storage capacitor C_{STO} . To emulate such varying light irradiance, the photocurrent, I_{SC} , is varied from 2.70 mA to 3.50 mA which corresponds to 600 – 1000 lux, and corresponding variations of PV cell terminal voltage, energy storage voltage, and load voltages are presented in Fig. 5.12. For PV cell terminal voltages, (V_{PH}), 415 mV and 465 mV, the unregulated load voltages ($V_{LOAD,UR}$) reached are 1.04 V and 1.130 V, and regulated load voltage ($V_{LOAD,R}$) reached is 1.01 V, respectively. It took less than 20 μ s to reach its steady state value for each light irradiance step. The proposed

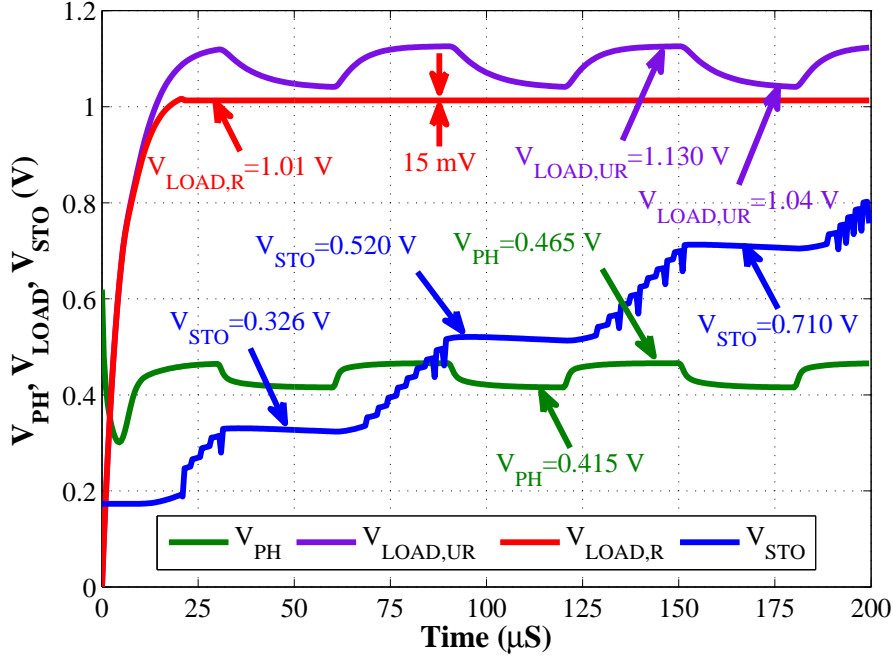


Figure 5.12: Complete system simulation when there is enough ambient energy to supply the load.

architecture will work properly once the photocurrent reached is above or equal to 2.70 mA , otherwise the load voltage will go below 1 V , and one may not be able to maintain the desired regulation at the load. Therefore, during this light condition, there will not be any excess energy that can be stored in a rechargeable battery. On the contrary, when the photocurrent reaches 3.50 mA , which is more than enough to supply the load, and the excess energy will be stored in a storage unit for further use, as shown in Fig. 5.12.

5.6.5.2 Under insufficient ambient energy

In this light condition, the proposed system will utilize the stored energy to maintain the load regulation. The variation of PV cell terminal voltage, and the regulated and unregulated load voltages are presented in Fig. 5.13. For PV cell terminal voltages 330 mV to 405 mV , the unregulated load voltage varies between 1.132 V to 0.922 V . Therefore, to maintain regulation at the load, one has to store the excess energy when V_{PH} is 405 mV and utilize this energy when V_{PH} is 330 mV . By doing so, one can achieve a regulated voltage of 1.01 V with 15 mV ripple, and one may reduce it further by minimizing opamp offset voltage.

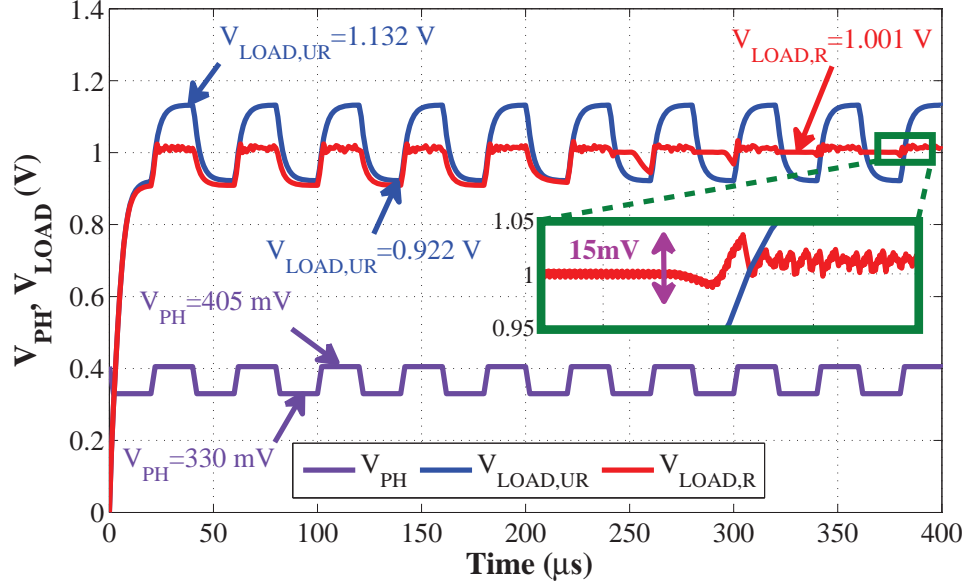


Figure 5.13: Complete system simulation at enough ambient energy to supply the load.

Fig. 5.14 shows the output of the control unit under two different light conditions: when there is enough ambient energy to supply the load and when there is insufficient ambient energy to supply the load. During the negative half cycle of clock, if the sample voltage, V_{DIV} , is higher than the reference voltage, V_{REF1} , control signal V_{M9} will turn on M_9 and M_{10} transistors, and V_{M8} control signal will turn off M_8 transistor. On the other hand, if the voltage V_{DIV} is lower than the reference voltage V_{REF1} , control signal V_{M8} will turn on M_8 transistor and turn off M_9 and M_{10} transistors, respectively, to maintain the regulation. However, if the voltage V_{DIV} is even lower than the second reference voltage V_{REF2} , then the control signal will turn-on M_{11} and M_9 transistors by the control signal Ψ , to transfer the charges from C_{STO} to C_{LOAD} . Therefore, an appropriate triggering of the control signals are occurred to provide better load regulation.

In order to calculate the effective system efficiency, one has to consider the power transfer loss due to both the control unit and the non-overlapping clock generator. The power consumed by the clock generator at a supply voltage 1 V is 12.3 μW , whereas, the control unit consume 18.3 μW at ~ 15 MHz clock frequency. Therefore, while calculating the net harvested power, one has to deduct these power from the output power. To calculate the overall system efficiency,

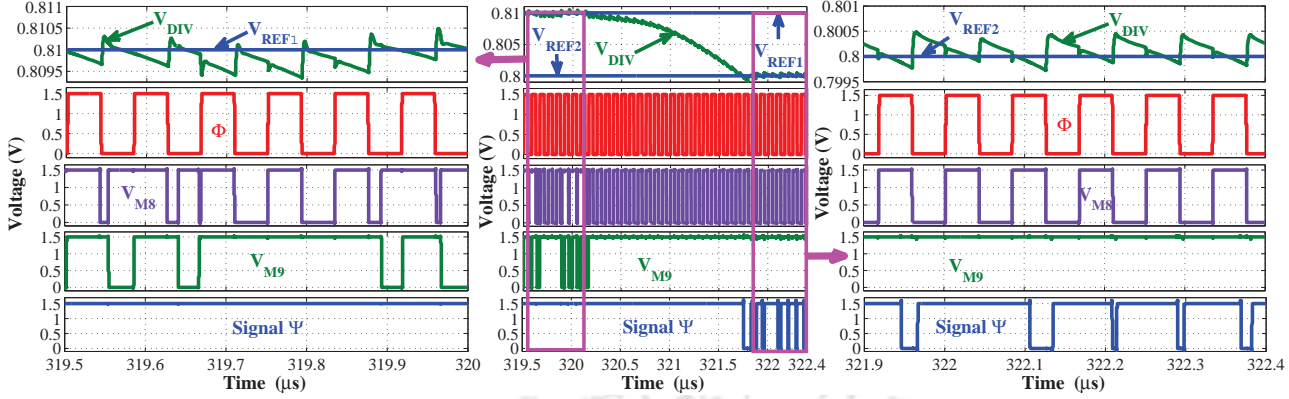


Figure 5.14: Control signals variation with respect to ambient conditions. Left hand side represents enough ambient energy whereas right hand side represent insufficient ambient energy conditions.

average input power and average output power are taken into consideration as the ambient condition are changing with time. Once the interface circuit provides regulation at the load, the overall efficiency of the system is calculated. To estimate the peak efficiency, one can refer to Fig. 5.13. The average input and output power during time frame of $361 - 399 \mu\text{s}$ are 1.188 mW and 1.01 mW , respectively, and the peak efficiency is 82.4% .

In order to compare with traditional power management architecture, a capacitor-less low-dropout regulator (CL-LDR) [9] has been incorporated (discussed in chapter 2) in between the switching regulator and the load, and the buffer stage is eliminated from the architecture. The error amplifier (EA) is designed to achieve a voltage gain 40 dB and the W/L of the pass transistor (M_P) is kept at $(2000/1)\mu\text{m}$ to deliver a load of $833 - \mu\text{W}$ with the supply voltage (V_{IN}) of 1 V . The open loop AC response shows a voltage gain of 59.22 dB and a phase margin of 84° . The overall efficiency achieved after incorporating the CL-LDR is $\sim 69.7\%$, where, $\eta_{DC-DC,1}$ (switching regulator), $\eta_{DC-DC,2}$ (CL-LDR), and $V_{LOAD,UR}$ are $\sim 84\%$, $\sim 83.3\%$, and 1.01 V , respectively. On the other hand, when the intermediate voltage ($V_{LOAD,UR}$) is reached 1.132 V , the CL-LDR and overall system efficiency have degraded to $\sim 73\%$ and $\sim 60\%$, respectively. On the contrary, by incorporating the buffer stage along with switching and CL-LDO regulators, the overall system efficiency has been reached to $\sim 69\%$, where $\eta_{DC-DC,1}$ and $\eta_{DC-DC,2}$ are $\sim 82.4\%$ and $\sim 83.3\%$, respectively. Therefore, by regulating the intermediate voltage, the system efficiency has been improved and the percentage of improvement depends on

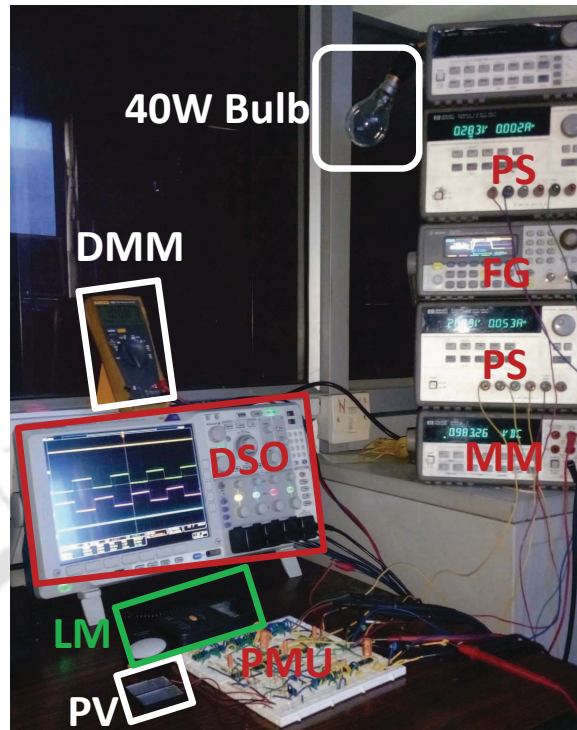


Figure 5.15: Hardware setup for the proposed power management architecture. PV: Photovoltaic Cell; LM: Lux Meter; PMU: Power Management Unit; DSO: Digital Oscilloscope; DMM: Digital Multimeter; MM: Multimeter; PS: Power Supply; FG: Function generator.

the changes in ambient variation of light intensity. For this specific example, system efficiency has been improved by $\sim 9\%$.

5.6.6 Experiment results

In order to validate the proposed power management scheme, a hardware setup is created using commercially available ICs, capacitors, and solar mini-panels as shown in Fig. 5.15. ICs ALD1103 [82], LM2903P [83], and HEF4071B [84] are used for MOSFETs, comparators, and OR gates, respectively. Three $1 \mu\text{F}$ capacitors and two $1000 \mu\text{F}$ capacitors are used for charge transfer and storage, respectively. Two series connected mini solar panels (Model 1-100, from Solar World Inc. [17]) are used to convert light energy to electrical energy. A digital lux meter (Mastech MS6610 [85]) is used to measure the light intensity. For system clock, Agilent-332501 function generator [86] is used and to generate non-overlapping clock signals phase shifter circuits are implemented using ALD1103 ICs. To represent ambient light energy,

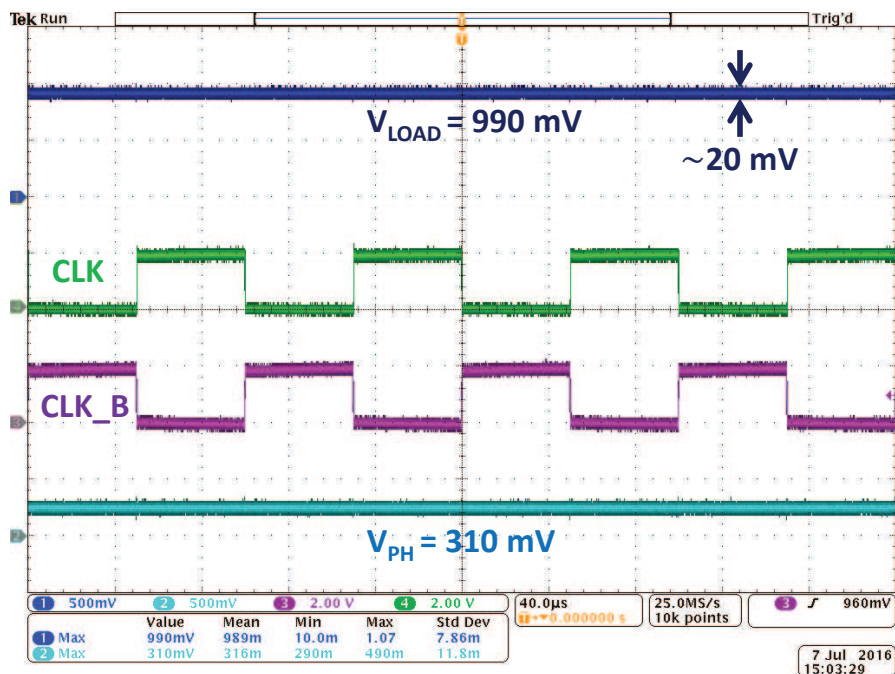


Figure 5.16: Measurement results of PV cell terminal voltage (V_{PH}), non-overlapping clock signals (CLK and CLK_B), and no-load output voltage (V_{LOAD}) at 100 lux light intensity.

40W light bulb is used for conducting the experiment. In order to vary the light intensity, distance between the light bulb and solar panels are varied.

Fig. 5.16 shows the measurement results of PV cell terminal voltage (V_{PH}), non-overlapping clock signals (CLK and CLK_B), and no-load output voltage (V_{LOAD}) at 100 lux light intensity. Under this light intensity, V_{PH} offers 310 mV to the interface circuit and with the help of non-overlapping clock signals, the load voltage reached is 990 mV with ± 20 mV ripple. Once the load is connected ($I_L \sim 100\mu\text{A}$), under this light intensity, V_{LOAD} is settled down to zero because of the insufficient light intensity for powering the load. Fig. 5.17 captures four images when the light intensity varies back and forth between 100 and 330 luxes. Fig 5.17(a) shows the initial stage waveforms where the light intensity changes from 100 lux to 330 lux. As soon as the light intensity increases, V_{PH} reaches ~ 375 mV and the load voltage starts increasing from the 0 V. Once the load voltage reaches ~ 1 V, buffer voltage V_{STO} starts increasing as shown in Fig 5.17(b). The PV cell terminal voltage is increasing once the load voltage and buffer voltage approaches the final value as shown in Fig. 5.17(b) and (c). Because, initially the

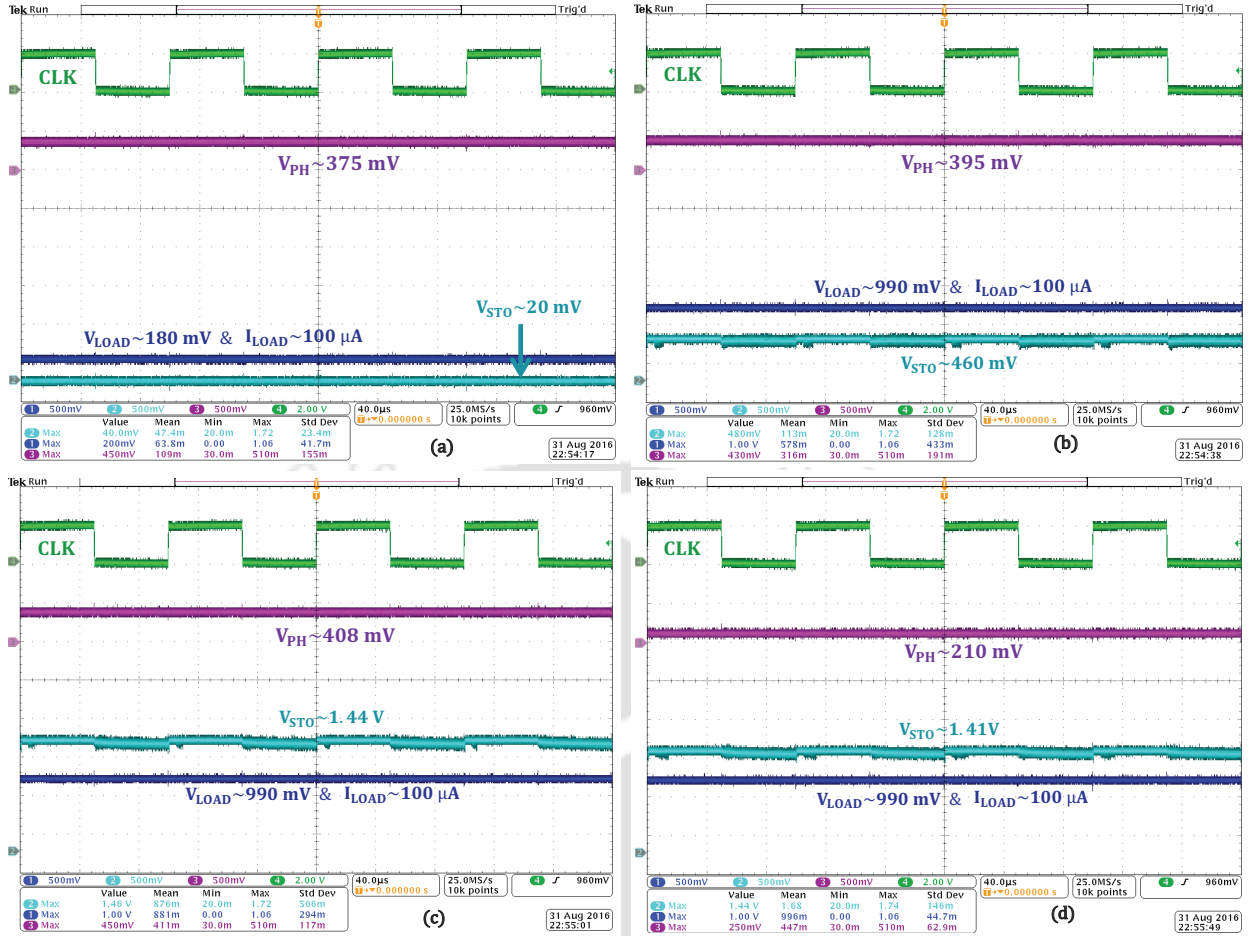


Figure 5.17: Transient response when the light intensities varies from 100 lux to 330 lux: (a) initial stage, when the light intensity change from 100 lux to 330 lux, (b) after 21 sec, while maintained light intensity ~ 330 lux, (c) after 44 sec, at ~ 330 lux light intensity, and (d) when the light intensity changes from 330 lux to 100 lux.

load capacitor was empty and the charge pump draws more current from the harvester, which eventually lowers the PV cell terminal voltage. Once the capacitor is charged, the load demand is reduced and eventually PV cell terminal current is reduced and the voltage is increased. After storing sufficient energy in the C_{STO} , light intensity was changed from 330 lux to less than 100 lux. Under such a condition, V_{PH} has come down to ~ 210 mV, which is not enough to maintain regulation at the load. In such a condition, the stored energy is utilized and the regulation is maintained at the load as shown in Fig. 5.17(d). Therefore, it is apparent from the measurement results that the proposed technique can maintain regulation at the load, irrespective of whether there is enough or not-enough ambient energies to supply the load.

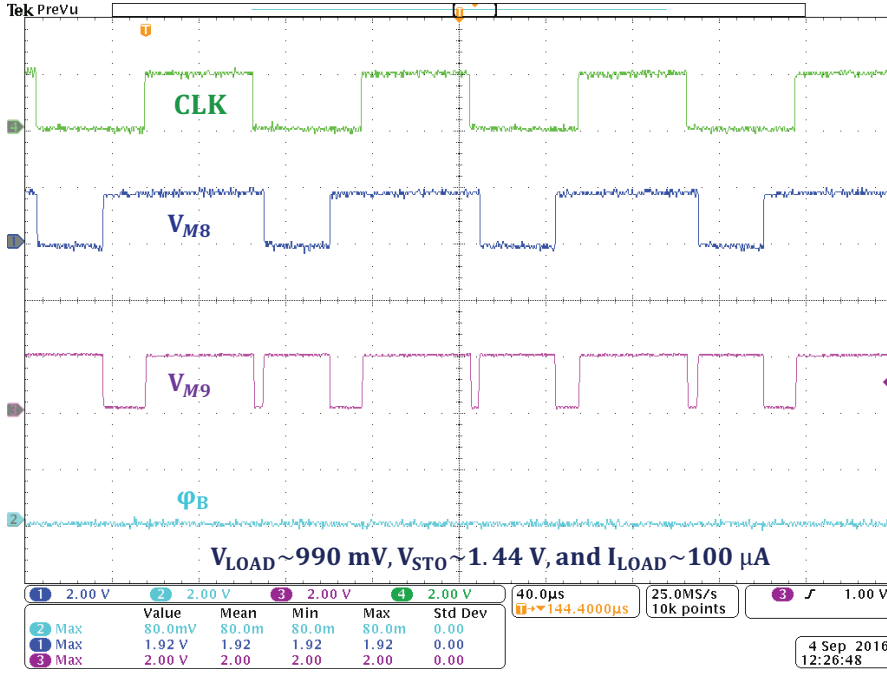


Figure 5.18: Measurement of control signals at 330 lux light intensity.

The measurement results of control signals at 330 lux and 100 lux light intensities are shown in Fig. 5.18 and 5.19, respectively. The 330 lux light intensity case represents enough ambient energy, whereas 100 lux light intensity represents a case in which enough ambient energy is insufficient to supply the load. At 330 lux light intensity, during the negative phase of clock, control signals V_{M8} and V_{M9} are generated alternatively to transfer the charge either to the load or to the storage unit, whereas the control signal Ψ_B remains at logic zero state, which means that the ambient energy is enough to maintain regulation at the load. On the contrary, at 100 lux light intensity, during the negative phase of clock, the control signals V_{M8} and V_{M9} are in logic zero and logic one state, respectively, whereas the control signal Ψ_B changes its state alternatively during the phases of clock. It indicates that the ambient energy is not enough to supply the load and to maintain regulation it utilizes the stored energy.

Table 5.1 shows the performance comparison among the state-of-the-art power management architectures for micro-scale solar energy harvesting systems. Among the capacitive boost converter, the proposed one has higher conversion efficiency and higher power delivery capability. Moreover, the proposed one has highest switching frequency which allows smaller component

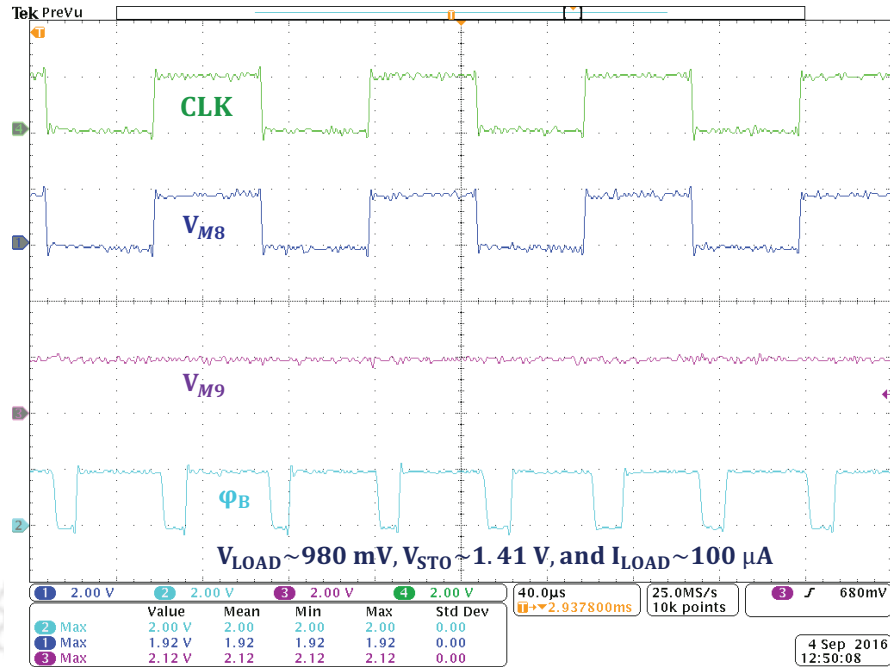


Figure 5.19: Measurement of control signals at 100 lux light intensity.

size and compact chip-area. Further, the proposed one has lower MPPT overhead as it utilize inherent negative feedback loop for maximum power point tracking.

5.7 Summary and Conclusions

This work focuses on improving the overall system efficiency by changing its architecture and utilizing the hardware efficiently. An efficient on-chip power management architecture for solar energy harvesting system is presented, with the following salient features: 1) a new switched capacitor based power management architecture for solar energy harvesting systems, which avoids linear regulator and utilizes simple charge pump concept in order to maintain regulation at the load, 2) utilizes a single DC-DC converter when there is enough ambient energy for maintaining regulation at both the input and load and stores excess energy in a supercapacitor, 3) utilizes the stored energy to maintain regulation when there is insufficient ambient energy to supply the load requirement, and 4) ensures higher LDR efficiency during varying ambient conditions, by maintaining proper intermediate voltage between switching regulator and LDR.

Table 5.1: Performance Comparison among state-of-the-art power management architecture for micro-scale energy harvesting systems

| Parameters | Ghosh [87] | Dallago [88] | Shao [53] | Shih [11] | Sourav [72] | Chao [56] | This work |
|--|---|--|--|---|---|---|---|
| Technology node | 0.50 μm | 0.35 μm | 0.35 μm | 0.13 μm | 0.35 μm | 45 nm | 0.18 μm |
| Energy source | solar | solar | solar | solar | solar | solar | solar |
| Input current and voltage to converter | $I_{PH} = 50\mu\text{A}$, $V_{PH} = 550\text{mV}$ | $I_{PH} = 8\mu\text{A}$, $V_{PH} = 560\text{mV}$ | $I_{PH} = 286\mu\text{A}$, $V_{PH} = 2.74\text{V}$ | $I_{PH} = 40\mu\text{A}$, $V_{PH} = 480\text{mV}$ | $I_{PH} = 1.58\text{mA}$, $V_{PH} = 410\text{mV}$ | $I_{PH} = 1.34\text{mA}$, $V_{PH} = 330\text{mV}$ | $I_{PH} = 3.06\text{mA}$, $V_{PH} = 408\text{mV}$ |
| Load condition | 2.81V@6.85 μW | 3.0V@2.9 μW | 4.4V@528 μW | 1.4V@11 μW | 1.88V@564 μW | 1.0V@170 μW | 1.0V@1.01mW |
| Converter type | IBC | IBC | CBC | CBC | IBC | CBC | CBC |
| Architecture | charger | two-stage | charger | charger | dual-path | charger | dual-path |
| MPP Voltage | not discussed | - | 2.74V@ $f_{MPP}=2.1\text{MHz}$ | - | 0.410@ t_{CH}, t_{DCH} =1.86 $\mu\text{s}, 470\text{ns}$ | 0.364@ $f_{MPP}=11\text{MHz}$ | 0.408@ $f_{MPP}=22\text{MHz}$ |
| MPPT scheme | HC method | no scheme | HC method | no scheme | P&O method | NFC method | Inherent NFC |
| System efficiency | 59% | 65% | 67% | 58% | 83% | 40% | 82.4% |

IBC: Inductive boost converter; CBC: Capacitive boost converter; P&O: Perturb and observe; HC: Hill Climbing; NFC: Negative Feedback Control; t_{CH} : inductor charging time; t_{DCH} : inductor discharge time.



6

Conclusions

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6.1 Conclusions

Energy efficiency of integrated circuits continues to be a major factor in determining the size, weight, and cost of portable electronic systems. Energy processing circuits act as an interface between energy harvesters and load, and they can be optimized to extract the maximum available power from it, depending on the specific harvester in use. This thesis has focused on energy processing circuits, making them more efficient in terms of power obtained, number of components used and overall cost of the final solution. The specific contributions made are listed below.

6.2 Summary of Contributions

Keeping in view of some of the requirements of forthcoming technologies, this thesis has suggested the following few solutions, from a converter to architectural level, related to the micro-scale solar energy harvesting system.

Single-phase tree-topology charge pump

- Generally, Two-phase tree-topology charge pump (TPT-QP) is better in some aspects (such as, pumping efficiency, charge transfer capability, gate oxide reliability, power conversion efficiency, etc.) than the linear-topology. Whereas, single-phase linear-topology charge pump performs better in some other aspects (like complexity, hardware cost, dynamic loss, etc.) than the TPT-QP. Therefore, to retain the advantages of both and to mitigate their individual limitations, both these topologies have been combined appropriately and had presented such a single-phase tree-topology QP, which have better charge transfer capability, reduced charge sharing time, less complexity, and minimum power transfer loss.
- A systematic analysis was presented to estimate the optimal transistor width of the charge pump circuit for higher system efficiency. In order to so, an analytical model has been developed for estimating losses involved and several suggestions are made to reduce the power transfer losses.

Low-Overhead adaptive MPPT scheme

- A fully integrated photovoltaic power harvesting system with low-overhead adaptive maximum power point tracking (MPPT) scheme for Internet-of-Things (IoT) nodes was presented. The proposed scheme utilizes the inherent negative feedback control loop to track the maximum power point voltage and to stabilize the system.
- An analytical model was developed to quantify the proposed idea and to optimize the MPPT circuit accordingly.

Efficient power management architecture

- An efficient power management architecture has been proposed to maintain regulation at both input and output sides dynamically when there is enough ambient energy, and to utilize the stored energy when there is insufficient ambient energy. The suggested architecture utilized a single DC-DC converter to maintain regulation at the load. Moreover, the proposed scheme avoided linear regulator and presented a complete on-chip switched capacitor based architecture.
- Using commercially available ICs, photovoltaic cells, capacitors, and resistors, a hardware setup was created to validate the proposed idea to maintain regulation at the load using a single DC-DC converter when there is enough ambient energy and two DC-DC converter when there is insufficient ambient energy.

6.3 Future Directions

Based on the work presented in this thesis, the following directions are suggested, as possible extensions for next generation energy processing circuits.

- Due to the advances in low power circuit design techniques, mm-scale wireless systems can be realized for wireless sensor nodes. But, a mm-scale photovoltaic harvester offers only few hundreds of nW power in an indoor light situation. Therefore, an efficient on-chip DC-DC up converter is required to bring up the output voltage to a level which is several times

higher than the input voltage, in order to replenish the battery. Generally, inductive boost converters are used to scavenge energy from the harvester, as they offer higher conversion efficiency. However, at low power levels, an inductive boost converter requires a large on-chip inductor, which demands large silicon area and offers power quality factor. On the other hand, switched capacitor DC-DC converter can be fully integrated as on-chip in a small area, and are also favored for small form-factor applications. However, in such a low power budget, switched capacitor DC-DC converter offers poor conversion efficiency due to the overhead of clock generator and level converter while driving the charge transfer switches. As a result, switched capacitor DC-DC converters pose extreme challenges below tens of micro-watt. Therefore, design of highly efficient switched-capacitor based DC-DC converter for such a low power budget can be explored.

- Although, we have considered single energy source for powering a wireless sensor node, one can combine energy from multiple energy sources in order to improve the overall system reliability and to increase the system functionality. To make such a system using switched capacitor circuits, one has to encounter a wide variation of input voltage, few tens of millivolt to few volts, in order to extract maximum power from the harvesters. To track such a wide variation of input impedance, from few tens Ohm to hundreds of kilo-Ohm, using switched capacitor technique is extremely challenging and not yet been demonstrated.
- Through our experiments in chapter 5, it has been observed that, if there is more than enough ambient energy to supply the load, the excess energy can be stored in the super capacitor or/and a rechargeable battery for future references. Now, if such situation continues for a long period of time a stage will come where, no more excess energy can be stored across the storage unit. Once the storage unit is fully charged, one needs to disconnect the harvester immediately from the interface circuit to maintain regulation at the load. Therefore, one needs a control circuit along with the energy processing circuit, which will prevent such a circumstance and possible system malfunctioning.

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- S. Mondal and R. Paily, “An efficient on-chip power management architecture for solar energy harvesting system”, *2016 29th International Conference on VLSI Design and 2016 15th International Conference on Embedded Systems (VLSID)*, Kolkata, India, pp. 224-229, Jan. 2016.
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