**INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI**
**SHORT ABSTRACT OF THESIS**

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Thesis Title: Investigations on Noise Cancellation and Linearity Improvement in Low Power LNAs and Receivers

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## SHORT ABSTRACT

Thermal noise-canceling radio-frequency (RF) circuits are available in the literature for more than two decades now. Yet, no systematic methodologies are available to analyze and design these noise-canceling circuits. The main objective of this thesis is to develop a generic theory of noise-canceling circuits and use it in the analysis and design of new noise-canceling circuits. A feedback-based noise-canceling model is developed as part of this work to explain the operation of existing noise-canceling circuits. The proposed model is validated through the analysis, design, and simulation of known noise-canceling low-noise-amplifiers (LNAs) and receivers. Further, a new systematic methodology to generate all multi-transistor noise-canceling circuits is developed in this thesis.

Based on the proposed methodology, the thesis also develops a few new noise-canceling circuits. One such circuit is a low-power partial noise-canceling complementary common-gate (CG) LNA. The performance of the LNA is further improved using a complementary linearization technique. The LNA effectively uses low-power techniques around a CG structure to reduce the power consumption by four times for a given input impedance. The complementary transistors are appropriately designed with optimum biasing to achieve linearization within the circuit. A prototype of the proposed LNA is implemented in a standard 180 nm complementary metal-oxide-semiconductor (CMOS) technology. Laboratory measurements show that the LNA has an input third-order intercept point (IIP3) > 0 dBm from 0.1-to-1 GHz while consuming only 0.735 mW of dc power in the high-linearity mode of operation. In the low-noise mode of operation, the LNA has a minimum noise figure (NF) of 3.41 dB while consuming 1.2 mW of dc power. The proposed LNA achieves one of the best figure-of-merit (FOM) among all existing low-power inductorless wideband LNAs in the literature.

Due to its low-power, low-noise, and high-linearity characteristics, the proposed complementary common gate (CCG) amplifier can also be used as a baseband amplifier in receivers. In this work, a low-power N-path mixer-first receiver is designed using the proposed CCG amplifier as a trans-impedance amplifier (TIA). A prototype receiver is implemented in a 180 nm CMOS process. The receiver operates from 0.3 to 1.3 GHz with a conversion gain of 21.9 dB. In measurements, the receiver achieved an in-band (IB) IIP3 of +7.2 dBm and a noise figure of 5.8 dB while consuming 0.34 mW power per TIA at 1 GHz. The measured spurious-free dynamic range (SFDR) at 1 GHz is 76.9 dB. Overall, the mixer-first receiver presented in this work achieved a good in-band SFDR while consuming the lowest static power.