Design of IR-UWB Transmitter and Receiver for IEEE 802.15.6 Wireless Body Area Network System

By

Babita Jajodia

A

Thesis Submitted

in Partial Fulfilment of the Requirements

for the Degree of

DOCTOR OF PHILOSOPHY

Department of Electronics and Electrical Engineering

Indian Institute of Technology Guwahati

Guwahati - 781 039, INDIA

April, 2019

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Declaration

This is to certify that the thesis entitled "**Design of IR-UWB Transmitter and Receiver for IEEE 802.15.6 Wireless Body Area Network System**", submitted by me to the Indian Institute of Technology Guwahati for the award of the degree of **Doctor of Philosophy** is a bonafide work carried out by me under the supervision of **Prof. Anil Mahanta and Prof. Shaik Rafi Ahamed**. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Certificate

This is to certify that the thesis titled "**Design of IR-UWB Transmitter and Receiver for IEEE 802.15.6 Wireless Body Area Network System**", submitted by **Babita Jajodia** (11610241), a research scholar in the *Department of Electronics & Electrical Engineering, Indian Institute of Technology Guwahati*, for the award of the degree of **Doctor of Philosophy**, has been carried out by her under our supervision and guidance. The thesis has fulfilled all requirements as per the regulations of the institute and in my opinion has reached the standard needed for submission. The results embodied in this thesis have not been submitted to any other University or Institute for the award of any degree or diploma.

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(Babita Jajodia)

Abstract

According to the statistics of World Health Organization (WHO), older people are the fastest-growing age group worldwide. The growing population of elderly people and increasing healthcare cost coupled with limited availability of trained health-care personnel and well-equipped hospitals and services (especially in developing countries) have led to the concept of active wellness management that permits early diagnosis and detection of ailments and follow-up actions through interaction between patients at their own home and medical experts and health-service providers over an extended period of time, and when warranted, takes emergent actions. The need for health-care systems using the technological advancements in wireless communications has witnessed the design of low power, intelligent and miniaturized invasive/non-invasive medical devices to be used on or around the human body or implanted in the human body for constant health monitoring and advice. This special type of wireless sensor networks (WSN) are referred to as Wireless Body Area Networks (WBAN). As the sensors are battery operated, it is of utmost importance that such nodes consume minimal energy. Thus the design of energy efficient and low-power transceiver architecture which greatly increases battery life is an important area in WBAN systems. The IEEE 802.15.6 standard is an international standard in WBANs for low power, short range and extremely reliable wireless communication within the surrounding area of the human body. This standard supports three physical layers (PHYs), namely, narrowband (NB) PHY, ultra-wideband (UWB) PHY and human-body communications (HBC) PHY. It is without a question that the Impulse Radio UWB (IR-UWB) signaling has a major advantage as regard the transmission power and energy consumption. This thesis focuses on design of an IR-UWB transceiver for BANs that exhibits satisfactory performance while fulfilling the 15.6 specifications and maintaining its structural and implementation simplicity - particularly in sub-nanometer technology.

This research work emphasizes the design of a low-complexity IR-UWB transceiver system for BANs strictly fulfilling the IEEE 802.15.6-2012 specifications and without violating the FCC rules

and regulations. This thesis attempts to devise an implementation architecture that enables the design of an energy-efficient and low-complexity 15.6 IR-UWB transceiver system for BANs.

The contributions of the Thesis are detailed in four chapters that may be grouped under two parts:

- IEEE 802.15.6 compliant IR-UWB transmitter using SRRC signaling pulse at the carrier frequency of f_c= 3.9936 GHz and a data rate of 0.4875 Mbps (Chapter 3 and Chapter 6)
- IEEE 802.15.6 compliant IR-UWB non-coherent energy detection based receiver at f_c= 3.9936 GHz with digital back-end (Chapter 4 and Chapter 5)

A brief description of the Chapters are as follows:

Chapter 3: IR-UWB Transmitter using SRRC Signaling Pulse

This chapter considers a method for approximation of an arbitrary signaling pulse by a piecewise linear approximation (PWLA) approach and details its practical implementation in simple mixed-signal circuits. The proposed PWLA approach has the potential to approximate a signaling waveform with a high degree of accuracy. Various PWLA approximations of the SRRC pulse are considered and compared in terms of cross-correlation (with the ideal pulse), power spectral density and implementation complexity. Using a six-segment PWLA SRRC pulse, a complete design of a 15.6 compliant IR-UWB transmitter operating at a carrier frequency f_c =3.9936 GHz and a data-rate of 0.4875 Mbps using PPM signaling is given. The transmitter is designed for both 2-ary and 16-ary PPM signaling.

Chapter 4: IR-UWB Non-coherent Energy Detection based Receiver

This chapter considers a design of an energy-efficient, non-coherent, energy-detection based receiver that uses a windowed integrator and a single-ended SAR ADC for "integration" and "digitization" followed by a new digital back-end for information extraction. The windowed integrator uses a new digital switching technique. The proposed single-ended SAR ADC uses a modified merged capacitor switching scheme for a capacitive reference DAC and works using a novel counter based SAR controller. The RF front-end is implemented using a single-to-differential LNA followed by a cascade of switchable inverter based gain stages feeding a squarer and an integrator for energy computation. BER performance of digital back-end are also carried out to validate the proposed energy detection based receiver. The receiver is designed for detection of information from the transmitter discussed in Chapter 3.

Chapter 5: DAC Switching Technique for Single-ended SAR ADCs

This chapter deals with developing an energy-efficient SAR ADC and proposes a new switching technique for the capacitive reference DAC employed in the SAR ADC. This technique brings down the switching energy in the first few comparison cycles where the switching energy consumption is the highest among the 'N' comparison cycles. Simulations are carried out to validate the proposed DAC switching technique and results are compared with the existing state-of-the-art DAC techniques.

Chapter 6: Design Methodology for Event-driven PWLA Waveform Generator

The PWLA approach of Chapter 3 essentially employs a state-machine controller whose clock is derived from the system clock and hence the durations of the line segments are constrained by the clock. The final part of the thesis focuses on providing a more accurate piece-wise linear approximation of a (signaling) waveform. To this end, an event-driven approach for PWLA pulse generator is considered and its performance evaluated. A set of "events" are generated at the break-points of a suitably chosen piece-wise linear approximations and these events in turn drives the PWLA segment generator to realize an arbitrary signaling waveform with a high degree of accuracy. Results show improved performance as compared to those in Chapter 3. Lastly, as a special case study, this approach is applied for approximation of a few selected IR-UWB pulses (Gaussian pulse and its derivatives). This study of the event-driven PWLA approach shows promising potential for applicability of the proposed pulse generator methodology in transceiver design.

In summary, it may be stated that this thesis has introduced a few circuit techniques along with an investigative study for design of energy-efficient and low power transceivers for IEEE 802.15.6 Wireless BANs.

Contents

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List of Abbreviations

2G/3G/4G	Second/Third/Fourth Generation
5G	Fifth Generation
AAL	Ambient Assisted Living
ADC	Analog-to-Digital Converter
AFH	Adaptive frequency hopping
AWGN	Additive White Gaussian Noise
BAN	Body Area Network
BCC	Body-Channel Communications
BCH	Bose-Chaudhuri-Hocquenghem
BCT	Body Channel Transceiver
BER	Bit Error Rate
BJT	Bipolar Junction Transistor
BPF	Band pass Filter
BTB	Body-to-body
BTG	Body-to-gateway
CCA	Clear Channel Assessment
CDR	Clock-and-data-recovery
CG	Common Gate
CMOS	Complementary Metal-Oxide-Semiconductor
CORDIC	COordinate Rotation DIgital Computer
CP-BFSK	Continuous-phase binary-frequency-shift-keying
CRC	Cyclic Redundancy Check
CS	Common Source
CWC	Centre for Wireless Communications

DAA	Detect and Avoid
DAC	Digital-to-Analog Converter
DBPSK	Differential Binary Phase-shift-keying
DCI	Direct Coupling Interface
DFSK	Differential Frequency Shift Keying
DGG	Digital-gradient Generator
DLL	Delay-locked-loop
DRF	Data Rate Field
DSSS	Direct Sequence Spread Spectrum
DQPSK	Differential Quadrature Phase-shift-keying
DWPT	Discrete Wavelet Packet Transform
ECG	Electrocardiogram
EEG	Electroencephalography
EIRP	Equivalent Isotropic Radiated Power
EMG	Electromyography
FBAR	Field Bulk Acoustic Resonator
FCC	Federal Communications Commission
FDSM	Frequency to Digital Sigma Delta Modulation
FEC	Forward Error Correction
FoM	Figure of Merit
FPGA	Field Programmable Gate Array
FSC	Frequency Shift Code
FSDT	Frequency Selective Digital Transmission
FTMNC	Frequency-translated mutual noise cancelling
GMSK	Gaussian Minimum Shift Keying
HARQ	Hybrid Automatic Repeat Request
HBC	Human Body Communications
HCS	Header Check Sequence
HME	Hub Management Entity
IBC	Intra-Body Communications

IDWPT	Inverse Discrete Wavelet Packet Transform
IEEE	The Institute of Electrical and Electronics Engineers
IL-DCO	Injection-locking digitally controlled oscillator
IoT	Internet of Things
IR-UWB	Impulse-Radio Ultra Wide Band
ISM	Industrial, Scientific and Medical
ITCS	Interactive Telecare System
LC	L stands for inductor and C stands for capacitor
LDC	Low Duty Cycle
LFSR	Linear Feedback Shift-Register
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low Pass Filter
M2M	Machine to Machine
MAC	Media Access Control
MBAN	Medical Body Area Network
MB-OFDM	Multi-band orthogonal frequency division multiplexing
MEMS	Micro-Electro-Mechanical Systems
MICS	Medical Implant Communications Service
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPDU	MAC protocol data unit
MSE	Mean-Squared Error
MT-CDMA	Multi-tone Code-division-multiple access
MUD	Multi-user Detection
NB	NarrowBand
NF	Noise figure or Noise factor
NRZI	Non-return-to-zero-inverted
NTT	Nippon Telegraph and Telephone
OFDM	Orthogonal Frequency Division Multiplexing
OOK	On-off Keying

OSI	Open System Interconnection
PAN	Personal Area Network
PER	Packet Error Rate
PHY	Physical Layer
PL	Path Loss
PLCP	Physical Layer Convergence Protocol
PLL	Phase-locked Loop
PPDU	Physical Layer Protocol Data Unit
PPG	Pulse Pattern Generator
PPM	Pulse Position Modulation
PSD	Power Spectral Density
PSDU	Physical Layer Service Data Unit
PSK	Phase shift keying
PWLA	Piece-wise Linear Approximation
QoS	Quality of Service
RF	Radio Frequency
RRC	Root Raised Cosine
RSSI	Received Signal Strength Indicator
S2P	Serial-to-parallel
SAR ADC	Successive Approximation Register ADC
SF	Spreading Factor
SFD	Start Frame Delimiter
SHR	Synchronization Header
SNR	Signal-to-Noise Ratio
SoC	System-On-Chip
SRRC	Square Root Raised Cosine
SUNs	Smart-metering Utility Networks
TH-PPM	Time Hopping PPM
TG6	Task Group 6
ULP	Ultra-low power

UWB	Ultra Wide Band
VCO	Voltage Controlled Oscillator
VGA	Variable Gain Amplifier
WBAN	Wireless Body Area Network
WBS	Wide Band Signaling
WMTS	Wireless Medical Telemetry System
WPAN	Wireless Personal Area Network
WSN	Wireless Sensor Network

1

Introduction to Body Area Networks

Contents

1.1 Introduction

According to the statistics of World Health Organization (WHO), older people are the fastest-growing age group worldwide [5]. It is estimated that by 2020 the number of people aged 60 years and older will outnumber children younger than 5 years and by 2050, the proportion of the world's population over 60 years will nearly double from 12% to 22%. As per the United Nations Population Division report of India [6], the ageing population (60 years or older) is projected to climb from 8% (in 2010) to 19% (in 2050). In the United Kingdom, the population over 85 years is predicted to increase three-fold by 2030 [7]; in the United States, the population over 65 years is expected to increase two-fold by 2040 [8]. In People's Republic of China, the population over 60 years is expected to double by 2040 [9]. By 2050, according to World Population prospects reported in [10], Japan is predicted to have the highest elderly population in human history with average age of 54 years. These worldwide statistics of ageing population necessitate a shift towards value-based, affordable and scalable healthcare solutions challenging the conventional and existing healthcare systems.

As people age, they are more likely to have mobility difficulties and suffer chronic ailments. There is an increasing trend in prevalence of chronic diseases at the global level. Such diseases - commonly termed as non-communicable diseases (NCD) - cannot be completely cured or eliminated. They tend to require lengthy and expensive treatments involving complex and ongoing care [11]. The four main types of NCDs are cardiovascular diseases (like heart attack and stroke), cancers, chronic respiratory diseases (such as chronic obstructed pulmonary disease and asthma) and diabetes [12]. Millions of people die every year as chronic diseases are the largest cause of death in the world. According to the scientific study of American College of Cardiology [13], cardiovascular diseases are one of the leading cause of death accounting to about one-thirds of deaths throughout the world. Cancer is the second leading cause of death globally (8.8 million deaths in 2015) accounting to approximately 70% of deaths occurring in low-and middle-income countries [14]. Visual impairment and blindness, hearing impairment and deafness, oral diseases and genetic disorders are other chronic conditions that account for a substantial portion of the global burden of disease.

The prognosis, however, is positive as a new research study by American Cancer Society [15] predicts that by 2050 cancer deaths would be eliminated for all age-groups except those over-80s through recent gains in early detection, prevention and treatment. As per WHO [16], Diabetes will be the seventh leading cause of death globally in 2030 roughly estimating 1.6 million deaths directly

caused by diabetes in 2015. Diabetes (Type-II) is the world's fastest growing chronic disease and is the leading cause of blindness and visual disability (due to diabetic retinopathy) and kidney failure. Overweight, obesity, unhealthy diet and lack of physical exercise are the key risk factors for Type-II diabetes and many other chronic diseases. Child overweight and obesity are increasing worldwide and incidence of diabetes-II among children is also increasing. Remote monitoring solutions would help overweight adults seeking ways to reduce overweight and obesity [17].

The growing population of elderly people and increasing healthcare cost coupled with limited availability of trained health-care personnel and well-equipped hospitals and services (especially in developing countries) have led to the concept of active wellness management that permits early diagnosis and detection of ailments and follow-up actions through interaction between patients at their own home and medical experts and health-service providers over an extended period of time, and when warranted, emergent actions are to be taken [1, 2]. This points to an increasing access to medical and assisting devices for people of all ages without affecting the normal life of the person. This has boosted research, development and production of health-care systems for people in low- and middle-income countries.

These systems should be capable of helping people living in remote areas to connect to the medical professionals stationed abroad or in urban areas for monitoring and collecting the information of the chronic conditions of a patient. Further, it should also help the aged people for medication, diet and exercise plans in accordance to the individual medical conditions. Such health-care system should be of minimum-cost, affordable, comfortable and user-friendly for people living in rural and remote areas.

The recent developments and technological advancements in wireless communication have enabled the use of low-power, intelligent and miniaturized invasive/non-invasive medical devices to be used on or around the human body or implanted in human body for constant health monitoring and advice [1, 18]. This special type of wireless sensor networks (WSN) are referred to as Wireless Body Area Networks (WBAN).

It is envisaged that the cost-effective WBAN healthcare systems will improve the long-term health care and constant physical monitoring without affecting the normal life of patients. This will allow constant physiological monitoring and allow mobility and flexibility to patients. Such a system will also track sudden life-threatening diseases and avoid in-hospital emergency monitoring of patients.

One of the potential technological innovations making huge difference to WBANs is the utilization

Table 1.1: Applications of WBANs

WBANs for Healthcare	Wearable WBANs	ECG [20–22], EEG [23], EMG and Muscle Fatigue [24], Parkinson Disease [25], Vital Signals monitoring [26]
		Assessing Soldier Fatigue and Battle Readiness [27]
		Aiding Professional and Amature Sport Training [18, 28]
		Sleep Staging [29], Asthma [30], Diabetes [31]
		Fall Detection [32, 33], Electrical Muscle Stimulation for Rehabilitation [34, 35]
	Implant WBANs	Cardiac Pacemakers [36], Cardioverter-Defibrillators [37]
		Retina Implants [38], Cochlear Implants [39, 40]
		Early Cancer detection [41]
		Wireless Capsule Endoscope [42, 43], Wireless Capsule for Drug Delivery [44]
		Deep Brain Stimulator [45, 46], Cortical Stimulator [47, 48]
	Remote Control of Medical Devices	Ambient Assisted Living (AAL) [49]
		Patient Monitoring [18, 26, 50]
		Tele-medicine Systems [51], Hearing Aids [52, 53]
Non-medical WBANs		Real-time Streaming & Entertainment Applications [18]
		Secure Authentication [54, 55]
		Emotion-Detection using Physiological Signals [56]

of 2G/3G/4G mobile communication technologies for delivering healthcare services throughout the world [11]. However, there are numerous non-technical factors such as acceptance, comfort, user friendliness, regulatory, affordability, ethical and legal issues that would need to be addressed.

The deployment of a collection of finite number of sensor nodes in WBAN creates opportunities for developing envisioned applications spanning from healthcare (medical) to consumer electronics (non-medical) [1, 19]. Each node in a WBAN [19] allows continuous monitoring of one's physiological parameters data such as electrocardiogram (ECG), electroencephalography (EEG), Electromyography (EMG), respiratory rate, blood pressure, body temperature etc providing greater mobility, flexibility and real-time feedback to patients without causing any discomfort [19]. WBANs will be a key solution for healthcare applications - the most promising field of application in a WBAN scenario. Table 1.1 presents some of the WBAN applications categorized into medical (healthcare) and non-medical applications.

Recent WBAN markets have introduced a few available proprietary and open technologies such as Sensium [57] - a seamless ambulatory monitoring system for early detection of patient deterioration. Z-wave [58] and Insteon [59] are the smart-home solutions while Wavenis Technology [60] is a well-known wireless solution for Machine to Machine (M2M) applications, such as environmental and healthcare monitoring. ANT/ANT+ [61], FitLinxx [62] and CONtinuous Athlete MOnitoring (CONAMO) [63] are the solutions well-suited for wellness applications, wireless activity monitors and health-tracking.

RuBee [64] based on the IEEE 1902.1 standard [65] is a solution for Defense and industrial Internet of Things (IoT) applications.

1.2 Evolution of Body Area Networks

Historically, the first research work on BAN was initiated in 1956 at the Radiology Research Lab, University of California, by R. Stuart Mackay [66] on radio telemetry from within the body. The extension of potential innovation of BAN began around 1995 with the work of T.G. Zimmerman on the early development of Personal Area Networks (PAN). Zimmerman [67] in the year 1996 demonstrated how electronic devices on and near the human body exchange digital information through near-field electrostatic coupling for intra-body communications (IBC). Later, around 2001, PAN representing applications and communications on, in and near the human body was named as BAN [68]. Later, in 2006, Professor Guang-Zhong Yang formally characterized the term "Body Sensor Networks" - also referred to as BANs - in the book [69].

Early research on BANs started with the work by Alex Pentland at the Massachusetts Institute of Technology (MIT) Media Lab with the development of a health-wear computing platform MITHril [70] - a BAN in the sense that multiple sensors are wired to a single processor. Excellent contributions were made by the academia for the deployment of BAN systems, such as, the CodeBlue Project at Harvard University [71], the Advanced Health and Disaster Network (AID-N) Project at Johns Hopkins University [72], Wearable Health Monitoring Systems (WHMS) developed at the University of Alabama [73], Ubiquitous Monitoring Environment for Wearable and Implantable Sensors (UbiMon) project at the Imperial College London [74] and AYUSHMAN project at Arizona State University [75]. Several state-of-the-art projects have contributed in establishing practical solutions for WBANs, like, LifeMinder [76], Mobi-Health [77, 78], the advanced care and alert portable telemedical monitor (AMON) [79], Microsystems Platform for Mobile Services and Applications (MIMOSA) [80], NASA-LifeGUARD [81], MagIC [82], m-Health [83], HealthGear [84], Wireless Monitoring system (Wi-MON) for Dengue [85], Medical Remote Monitoring of Clothes (MERMOTH) [86], HUMAN++ [87], Ad-hoc wireless sensor networks (ASNET) [88], BASUMA [89], eWatch [90], Personal Care Connect [91], MAHS [92], AlarmNet [93], CareNet [94], Wireless Motion Capture System with Accelerometers (WiMoCA) [95], Scalable Medical Alert and Response Technology (SMART) [96], VitalJacket [97], HeartToGo [98], HealthService 24 [99] and Personalized Anxiety Therapy thRough lOngitudinal &

User-aware Services (PATRONUS) [100] project.

1.3 Taxonomy of Body Area Networks

The various communication technologies providing appropriate solutions for deployment of BAN systems can be categorized as follows:

(i) **Human Body Communications (HBC):** HBC is also referred to as Intra Body Communications (IBC) or Body-Channel Communications (BCC). IBC exhibits the advantages of intrinsic security, interference-free communication and coexistence with other HBC WBANs (as transmission and reception of signals are confined to or close to the person's proximity) [1]. This technology [101, 102] uses the human body itself as the transmission medium for propagation of electrical signals. Based on how the electrical signals are transmitted, HBC can be sub-classified into two basic coupling types:

- Capacitive coupling: The signal is controlled by an electrical potential modeling the human body as a perfect conductor [103]. The signal quality is influenced by the surrounding environment (the dominant signal transmission pathway) around the body.
- Galvanic coupling: This is achieved by coupling the alternate current into the human body modeling the human body as a transmission line (waveguide) [104]. The dominant signal transmission pathway is the body tissue. This technique is capable of both on-body and in-body (implantable) device communications [105, 106].

(ii) **Molecular Communications:** These are the communication paradigms referring to the use of the molecule-level system for exchanging biochemical information between the transmitter and the receiver using nanotechnology [107] and nanomedicine [108]. Diffusion-based molecular communications due to its intrinsic biocompatibility have envisaged nanoscience applications, such as intracellular surgery with nanorobots [108] and target drug delivery [109]. For example, (i) a person is diabetic and is to be injected with insulin several times a day, (ii) a person is diagnosed with cancer and has to undergo chemotherapy with its debilitating side-effects.

(iii) **Ultrasonic Communications:** This technology explores the use of ultrasound (acoustic waves at non-audible frequencies nominally above 20 kHz) for transmission in the human body for

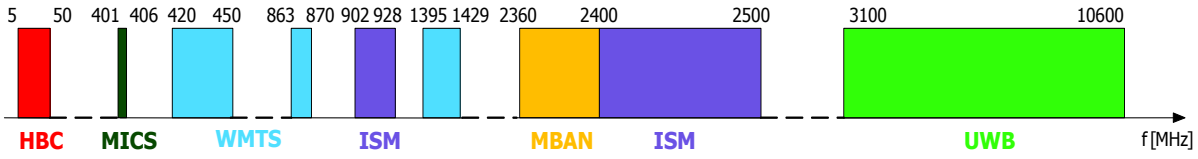

Figure 1.1: Frequency Bands for WBANs [1]

realization of intra-body area networks. It is well known that the acoustic waves are the preferred choice of transmission technology for underwater communications [110]. Human body is composed of up to 65% water [111] and is thus one of the most suitable medium for ultrasonic communication. Recently, Santagati *et al.* [112] have demonstrated experimentally the feasibility of impulsive ultrasonic intra-body communications.

(iv) **Radio Frequencies (RF) Technologies:** The existing radio technologies can be classified according to the operating frequency bands (regulated by Worldwide Communication Authorities). It is not straightforward for the WBAN designer to choose the most appropriate bands for the targeted applications. Fig. 1.1 illustrates the available frequency bands for WBANs and are described as follows:

- *Medical Implant Communication Service (MICS)* band is an universal RF band and is allocated the frequency band of 401-406 MHz, of which the core-band is 402-405 MHz. This band is proposed by the U.S. Federal Communications Commission (FCC) in 1999 [113] for use in implanted medical WBAN applications (such as cardiac pacemaker, implanted defibrillator and neurostimulator etc). It supports data rate up to 400 kbps and communication range up to 2 meters, i.e., for short-range intra-BAN communications [114]. Microsemi Corporation [115] offers three versions of commercially available MICS transceiver (ZL70101, ZL70102 and ZL70103) for implanted devices operating in the MICS band.
- *Wireless Medical Telemetry System (WMTS)* operates in three frequency bands (420-450 MHz, 863-870 MHz and 1395-1429 MHz) as shown in Fig. 1.1. WMTS is designed exclusively for medical telemetry (remote monitoring of a patient's health). The technology enables longer-range biosensor communication with the restriction that the technology be used only in hospitals [116]. A WBAN device is described in [117] that uses the combination of MICS and WMTS bands (thus applicable for both short-range and moderate-range

BAN communications).

- The *Industrial, Scientific and Medical (ISM)* band is an unlicensed band (902-928 MHz and 2.4- 2.5 GHz) defined by the International Telecommunication Union (ITU) [118] for purposes other than telecommunications and it supports high-data rate applications. Because of its world-wide free availability and being unlicensed, this 2.4-2.5 GHz ISM band is the most commonly used and an over-crowded RF band. Most of the standard solutions designed for WBANs operate in the ISM band (between 2.4-2.5 GHz). The ISM band applications are thus prone to significant coexistence issues and are sensitive to high probability of interference.
- The FCC [119] in May 2012 took an interesting action by allocating an operating frequency band (between 2.36 to 2.4 GHz with a 40 MHz spectrum) for a new *Medical Body Area Networks (MBAN)* licensed service. The MBAN band, importantly, is not an ISM band and thereby makes it possible to effectively mitigate the interference experienced by WBAN devices operating in the adjacent unlicensed (2.4-2.5 GHz) ISM band.
- *Ultra Wideband (UWB)* radio technology, defined by FCC [3] in 2012, is an unlicensed 3.1-10.6 GHz frequency spectrum. The only important factor specified by the FCC authorities [3] is that the mean maximum equivalent isotropic radiated power (EIRP) level or power spectral density (PSD) of an operating UWB device shall not exceed -41.3 dBm/MHz. The US mask defined by FCC [3] is the most liberal with the same maximum mean EIRP for UWB transmissions in the allowed spectrum of 3.1-10.6 GHz and also at sub-Gigahertz UWB band below 960 MHz. The European UWB mask [120] allows the same maximum EIRP limit for low-band (3.4-4.8 GHz) utilizing either 'detect and avoid' (DAA) or 'low duty cycle' (LDC) techniques. For high-band Group-1 (6-8.5 GHz), no mitigation techniques are used while for high-band Group-2 (8.5-9 GHz) only DAA technique is to be used. The Japanese UWB mask [121] also allows the same maximum mean EIRP limit in the low-band (3.1-4.8 GHz) with interference mitigation while in the high-band (7.25-10.25 GHz) devices do not support interference mitigation. The advantage of UWB mask over the ISM mask is that the maximum mean EIRP in UWB mask is around 30 dB below the maximum PSD for WBAN devices operating in the 2.4-2.5 GHz ISM band [122].

Table 1.2: Standard Protocols of different short-range wireless technologies

Standard	Technology	Frequency Band	Data Rate
IEEE 802.15.1-2002	Bluetooth V.1 802.5.1 [123]	2.4 GHz ISM	780 kbps
	Bluetooth V.2 + Enhanced Data Rate (EDR) [124,125]	2.4 GHz ISM	3 Mbps
	Bluetooth V.3 + High Speed (HS) [126]	2.4 GHz ISM, 5 GHz	3-24 Mbps
	Bluetooth V.4 + Low End Extension (LEE) [127]	2.4 GHz ISM	1 Mbps
	Bluetooth V.5 + Low Energy Long Range [128]	2.4 GHz ISM	2 Mbps
IEEE 802.15.4-2006 [129]	ZigBee [130]	868 MHz, 915 MHz, 2.4 GHz ISM	20, 40, 250 kbps
ECMA-368 [131]	MB-OFDM UWB †	3.1-10.6 GHz	Upto 480 Mbps
IEEE 802.15.4a-2007 ¶ [132]	UWB	3-5 GHz, 6-10 GHz, $<$ 1 GHz	0.11, 0.85, 6.81, 27.24 Mbps
IEEE 802.15.4-2011 ¶ [133]	UWB	249.6-749.6 MHz, 3.1-4.8 GHz, 6-10.6 GHz	0.11, 0.85, 6.81, 27.24 Mbps
IEEE 802.15.4-2015 ¶ [134]	HRP ‡ IR-UWB§	249.6-749.6 MHz, 3.1-4.8 GHz, 6-10.6 GHz	0.11, 0.85, 6.81, 27.24 Mbps
IEEE 802.15.6-2012‡‡ [2]	HBC	5-50 MHz	164.1, 328.1, 656.3, 1312.5 kbps
	NarrowBand (NB)	MICS (402-405 MHz)	75.9, 151.8, 303.6, 455.4 kbps
		WMTS (420-450 MHz, 863-870 MHz)	75.9, 151.8, 455.4 kbps
		ISM (902-928 MHz), 950-958 MHz	101.2, 202.4, 404.8 kbps
		MBAN, 2.4 GHz ISM	121.4, 242.9, 485.7, 971.4 kbps
	IR-UWB §	3.25-4.75 GHz, 6.25-10.25 GHz	0.487, 0.975, 1.95, 3.9, 7.8, 15.6 Mbps
	FM-UWB ††	3.25-4.75 GHz, 6.25-10.25 GHz	250 kbps

† MB-OFDM: Multi-band orthogonal frequency division multiplexing UWB
¶ Target: Low-Rate Wireless Personal Area Networks (WPANs)
‡‡ Target: Wireless Body Area Networks (WBANs)
§ IR-UWB: Impulse-Radio UWB
†† FM-UWB: Frequency Modulation UWB
‡ HRP: High Rate pulse repetition frequency

Table 1.2 summarizes different standardized versions of wireless communication standards technologies for short range wireless communication (with allocated frequency bands and possible data rates). Among all the IEEE standards, the IEEE 802.15.6-2012 standard [2] by the IEEE 802.15.6 Task Group TG6 is the only formally defined short-range, highly-reliable wireless communication standard for deployment of BAN systems and is not restricted to medical applications alone.

The IEEE 802.15.6-2012 Standard partitions the allotted UWB spectrum into two frequency groups: the Low-band (3.25 - 4.75 GHz) and the High-band (6.25 - 10.25 GHz). The two channels – each of 499.2 MHz bandwidth – centered at 3.9936 GHz and 7.9872 GHz respectively are considered

to be mandatory channels that a service provider is required to provide. The data rate of 0.4875 Mbps is considered as the mandatory data rate using the mandatory on-off signaling scheme.

1.4 Objectives of the Thesis

This thesis aims at exploring, developing and analyzing the performance of an IR-UWB transmitter and receiver for Body Area Networks (BAN) in compliance to the IEEE 802.15.6 [2] standard. The transmitter and the receiver operate in the mandatory low-band channel at the carrier-frequency of 3.9936 GHz and use the mandatory on-off signaling scheme at the mandatory data-rate of 0.4875 Mbps using a Square root raised cosine (SRRC) pulse.

1.5 Organization of the Thesis

The thesis is organized into seven chapters:

Chapter 1: Introduction to Body Area Networks

This Chapter gives an introduction to BANs/WBANs in general and the evolution of the latest WBAN Standard IEEE 802.15.6-2012 [2].

Chapter 2: Introduction to IEEE 802.15.6 Standard and Existing Transceivers for Body Area Networks (BANs)

This chapter gives an introduction to the IEEE 802.15.6 Standard specifying the essential features of the MAC and the PHY layers as a prelude to the design of the Transmitter and the Receiver as per the broad design specifications outlined in Section 1.3.

Chapter 3: IR-UWB Transmitter using SRRC Signaling Pulse

This chapter develops the design of an IEEE 802.15.6 compliant Impulse Radio Ultra-Wideband (IR-UWB) Transmitter for Wireless Body Area Networks in 180-nm CMOS technology. The transmitter operates at the mandatory data rate of 0.4875 Mbps in the mandatory low-band channel at 3.9936 GHz and employs a pulse position controller (PPC) to place a Square Root Raised Cosine (SRRC) pulse for a time-hopping pulse position modulation (TH-PPM) scheme. This transmitter features a novel piece-wise linear approximation (PWLA) approach for generation of the SRRC signaling pulse. It is found that the generated PWLA SRRC pulse is fully compliant with the WBAN spectral mask. The proposed PWLA approach has the potential to approximate an arbitrary signaling waveform with a high degree of accuracy and hence should be useful in transceiver realizations.

Chapter 4: IR-UWB Non-coherent Energy Detection based Receiver

For a relatively low data-rate application using PPM signaling considered in Chapter 3, an energy-detection based non-coherent receiver is an attractive solution for demodulation of information bits as it avoids local generation of the reference signal. Further, energy computation eliminates the need for a four-quadrant multiplier resulting in reduced hardware complexity and power consumption. Such an architecture is suitable in a BAN scenario involving battery-operated nodes. In this chapter, design and performance evaluation of a low-power energy-detection based non-coherent receiver employing "integrate and digitize" approach is proposed for demodulation of information bits transmitted by an IR-UWB transmitter developed in Chapter 3.

Chapter 5: DAC Switching Technique for Single-Ended SAR ADCs

SAR ADC is an attractive solution for signal acquisition in low-power portable and implantable devices [135–137] in BANs. The non-coherent energy detection based receiver described in Chapter 4 employs a single-ended SAR ADC. Although differential input SAR ADC is a superior solution for low-level signal acquisition due to its ability to suppress common-mode noise, single-ended SAR ADCs can nevertheless be a preferred solution especially when energy conservation is the over-riding concern and the SNR is at acceptable level. The capacitive reference DAC - employed in SAR ADC - contributes a significant portion to the total power consumption in SAR ADCs. The consumption of switching energy (during charging/discharging of the capacitive reference DAC) is the highest in the first few comparison cycles. Thus it is imperative to bring down the consumption of switching energy in the first few comparison cycles. Motivated by the work of Hu *et al.* [138], this thesis attempts to design a new DAC switching technique which brings down the consumption of switching energy in the first few comparison cycles. The proposed DAC switching technique digitizes an input signal in the amplitude range [0, V_{ref}] using a single reference voltage $\frac{V_{ref}}{2}$. The result shows an energy savings of 92.21% over the traditional 10-bit single-ended SAR ADC [139]. Further, as compared to Hu's method [138], the proposed technique shows about 37.6% reduction in switching energy.

Chapter 6: Design Methodology for Event-driven PWLA Waveform Generator

The PWLA approach for generation of a signaling pulse and presented in Chapter 3 assumes that the duration of each line segment approximating a portion of the given waveform is a multiple of some basic clock (derived from the system clock) and thereby facilitates the use of a simple state-machine controller. However, in the most general case, this assumption may not be valid. To overcome this

constraint an "Event-driven PWLA Approach" is developed and results vis-à-vis the SRRC waveform approximation are compared. While this method increases the hardware complexity, it has the potential to approximate an arbitrary waveform with a high degree of accuracy. As further examples, Gaussian waveform and a few of its derivatives are approximated and the goodness-of-fit is compared.

Chapter 7: Conclusions and Scope for Future Work

This Chapter concludes the thesis outlining the main contributions of the Thesis and discusses a few directions for further work in the area of Transceiver design.

2

Introduction to the IEEE 802.15.6 Standard and Existing Transceivers for BANs

Contents

2.1 The IEEE 802.15.6 Standard

The IEEE 802.15.6 standard defines the Media Access Control (MAC) and the Physical (PHY) layers, the two bottom layers of Open System Interconnection (OSI)-model protocol stack for BANs. The Node[1] Management Entity (NME) or Hub Management Entity (HME) exchanges network management information with MAC and PHY layer as well as other layers. The number of nodes that can exist in a BAN varies from *zero* to *nMaxBANSize* (*nMaxBANSize*= 64). The maximum number of BANs that can co-exist in a network is four and only one hub is allowed per BAN. Therefore, a maximum of 256 nodes can exist per network [140]. Each node is addressed by an one-octet BAN identifier (BAN ID) numbered from 0x00 to 0xFF. The network topology can be either a one-hop star topology or a two-hop extended star topology.

2.1.1 MAC Layer

The IEEE 802.15.6 TG6 group proposes a single MAC protocol, but a very flexible and sophisticated protocol that controls access to channels of all hubs and nodes. For establishment of common time-reference allocation and regardless of transmission of beacons, the channel (or time-reference axis) is divided into a series of equal length superframes (or beacon periods). Each superframe is again sub-divided into 256 allocation slots of equal length numbered from 0 to 255. The hub (or coordinator) can transmit beacons in any superframe other than inactive or restricted superframes. The hub operates either in beacon[2] mode or non-beacon[3] mode and coordinates the scheduling of channel access for nodes. This can be done through any one of the three following channel access modes [1, 141]:

- *Beacon Mode with Superframe Boundaries:* In this mode, periodic beacons are transmitted at the beginning of each active superframe. Each active superframe is divided into applicable access phases and is illustrated in Fig. 2.1. The access phases are:
  - Exclusive Access Phase (EAP): EAP1 and EAP2 are used for transmission of high-priority traffic (emergency data).
  - Random Access Phase (RAP): RAP1 and RAP2 are for regular traffic.

[1]Node: An independent device with communication capability
[2]Beacon Mode: Beacon is transmitted in every superframe for time-reference allocations except in inactive superframe.
[3]Non-beacon Mode: The time-referencing is established using superframes and allocation slots in place of transmitting beacons.

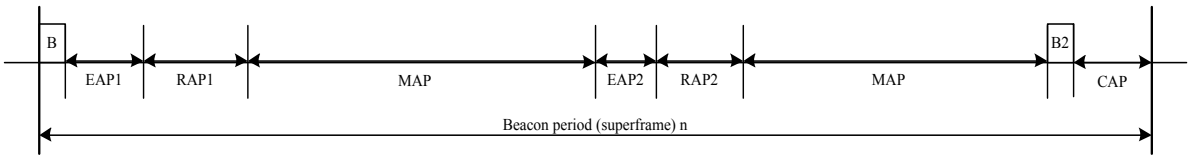

Figure 2.1: IEEE 802.15.6 Superframe Structure with Access Phases [2]

  - Managed Access Period (MAP): used for polled allocation intervals, scheduled allocation intervals (e.g. bi-link allocation, down-link allocation, delay bi-link allocation intervals) and unscheduled allocation intervals.
  - Contention Access Period (CAP): used for resource allocation using either Carrier-sense multiple access with collision avoidance[4] (CSMA/CA) or Slotted ALOHA[5] technique.

- *Non-beacon mode with Superframe Boundaries:* In this mode, the superframe is covered only by MAP and not by any other access phases.
- *Non-beacon mode without Superframe Boundaries:* In this mode, each node has to establish its own independent time-schedule since there is no superframe boundaries. The hub provides only unscheduled bi-link allocation intervals.

The MAC protocol ensures security paradigm with three different levels of security:

- *Level 0- Unsecured communication:* No measures for message authenticity, encrypted frames and integrity validation, confidentiality and privacy protection.
- *Level 1- Authentication but no Encryption:* Secured authentication but without encrypted frames; provides measures for authentication and integrity validation but without confidentiality and privacy protection
- *Level 2- Authentication and Encryption:* The most secured authentication with encrypted frames; provides measures for authentication and integration validation with privacy protection and confidentiality

[4]In CSMA/CA, a node shall transmit by obtaining a contended allocation selecting a backoff counter (BC) among the equiprobable values in the interval [0-CW(UP)], where CW: Contention Window Value and UP: Upper Priority

[5]In Slotted ALOHA, a node transmits in a given slot only if $z \leq CP[UP]$, where CP: Contention Probability value, UP: Upper Priority and $0 \leq z \leq 1$.

2.1.2 PHY Layer

The PHY layer acts as the data interface to the MAC layer under the control of Physical Layer Convergence Protocol (PLCP). The PHY layer serves three functionalities:

- Activation and deactivation of radio transceivers
- Indication of Clear Channel Assessment (CCA) to the MAC layer for verification of activity in wireless medium
- Data transmission and reception

The data to be transmitted, i.e., the Physical Layer Service Data Unit (PSDU) is the MAC frame from the MAC layer. The MAC frame consists of the following three subfields: a 7-octet MAC header, a variable-length MAC frame body (0-255 octets) and a 2-octet Frame Check Sequence (FCS).

As per Hernandez and Mucchi [142], the data transmission and reception can be sub-divided into two inter-linked tasks: (i) Construction of the Physical Layer Protocol Data Unit (PPDU) from the PSDU and (ii) Transformation of the PPDU frames into radio signals for transmission in the wireless medium. These two inter-linked tasks (construction and transmission of the PPDU frame) for each of the three PHY layers: HBC PHY, NB PHY and UWB PHY are described as follows.

2.1.2.1 HBC PHY

Fig. 2.2 presents the HBC PPDU structure. The PPDU frame format or the HBC packet structure is constructed by concatenation of PLCP Preamble, Start Frame Delimiter/Rate Indicator (SFD/RI), PLCP Header and PSDU/PHY Payload. The PLCP preamble and SFD/RI are fixed data patterns (hence they can be pre-generated) and are transmitted prior to the PLCP Header and the PSDU. The PLCP preamble is formed of four preamble sequences: PR1, PR2, PR3 and PR4. Each preamble sequence is generated by spreading a 64-bit Gold code sequence using a frequency shift code (FSC). The FSC for preamble generation is [0,1,0,1,0,1,0,1], since FSC uses a repeated [0,1] code and the spreading factor (SF) is 8 for HBC PHY. Gold code sequences have better cross-correlation properties compared to a maximum linear feedback shift-register (LFSR) sequences [143]. The PLCP preamble aids the receiver in packet synchronization (the start of the packet).

After packet synchronization, the SFD/RI determines the start of the PHY frame (for frame synchronization). For RI mode, the SFD/RI also indicates the packet data rate to the receiver inde-

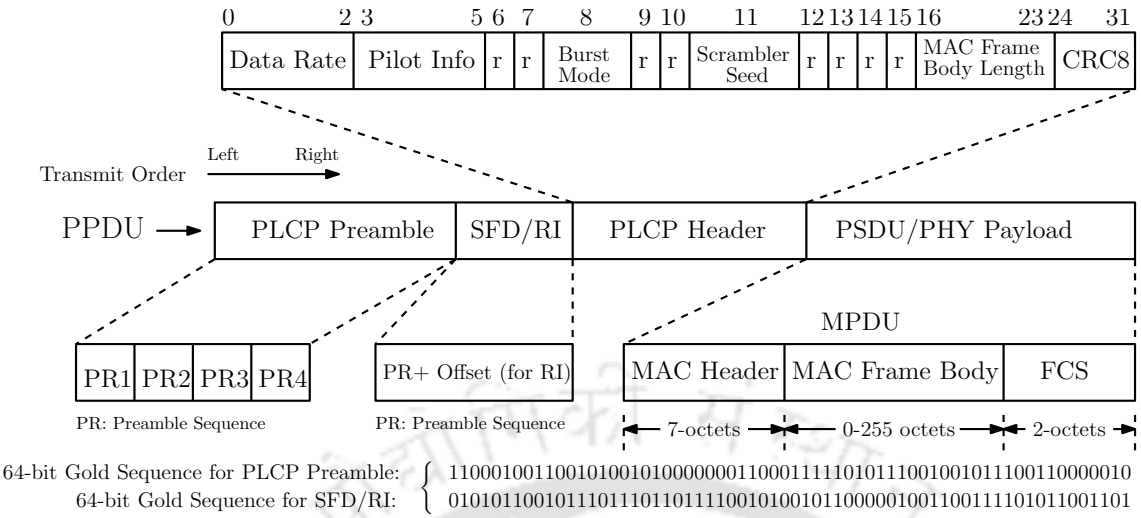

Figure 2.2: HBC PPDU Structure [2]

pendent of the data rate field (DRF) in the PLCP header. The advantage of using RI mode is that it allows same data rate for transmission of the PLCP header and the PSDU. This increases transmission efficiency. Unlike the PLCP preamble sequence, the sequence for SFD mode is generated by spreading a 64-bit gold sequence using the FSC as [0,1,0,1,0,1,0,1] and SF= 1. For RI mode, the sequence is generated by spreading a 76-bit code (a 64-bit gold sequence pre-appended with 12 zeros to take care of time offset) using FSC as [0,1,0,1,0,1,0,1].

The PLCP Header of 32 bits contains PHY information. It consists of the following sub-fields: the data rate of the PSDU (in DRF mode and not in RI mode), Pilot Info (contains information of optional pilot insertion period in PSDU to prevent loss of synchronization due to clock drift), burst mode (whether or not the next packet is a part of a burst of packets), scrambler seed (to eliminate long strings of ones and zeros in PSDU), MAC frame body length, Cyclic Redundancy Check 8 (CRC8) calculated over the PHY header and reserved bits: 'r'.

The concatenation of the PLCP Header and the PSDU is next mapped to chip (for frequency-spreading) using a Serial-to-Parallel (S2P) converter and Frequency Selective (FS)-Spreader structure as shown in Fig. 2.3. The serial data are partitioned into 4-bit symbols using S2P converter (Fig. 2.3). This is followed by mapping each 4-bit symbol into 16-bit chip using the Walsh symbol-to-chip mapper (Fig. 2.3). Next, each 16-bit chip is spread by applying different FSC (64/32/16/8 bits) for different input data rate (164/328/656/1312 kbps). This variable selection of FSC results in constant chip data rate of 42 Mcps regardless of the input data rate.

Symbol-to-chip Orthogonal Mapping

Bits	Orthogonal Code
0000	1111 1111 1111 1111
0001	1010 1010 1010 1010
0010	1100 1100 1100 1100
0011	1001 1001 1001 1001
0100	1111 0000 1111 0000
0101	1010 0101 1010 0101
0110	1100 0011 1100 0011
0111	1001 0110 1001 0110
1000	1111 1111 0000 0000
1001	1010 1010 0101 0101
1010	1100 1100 0011 0011
1011	1001 1001 0110 0110
1100	1111 0000 0000 1111
1101	1010 0101 0101 1010
1110	1100 0011 0011 1100
1111	1001 0110 0110 1001

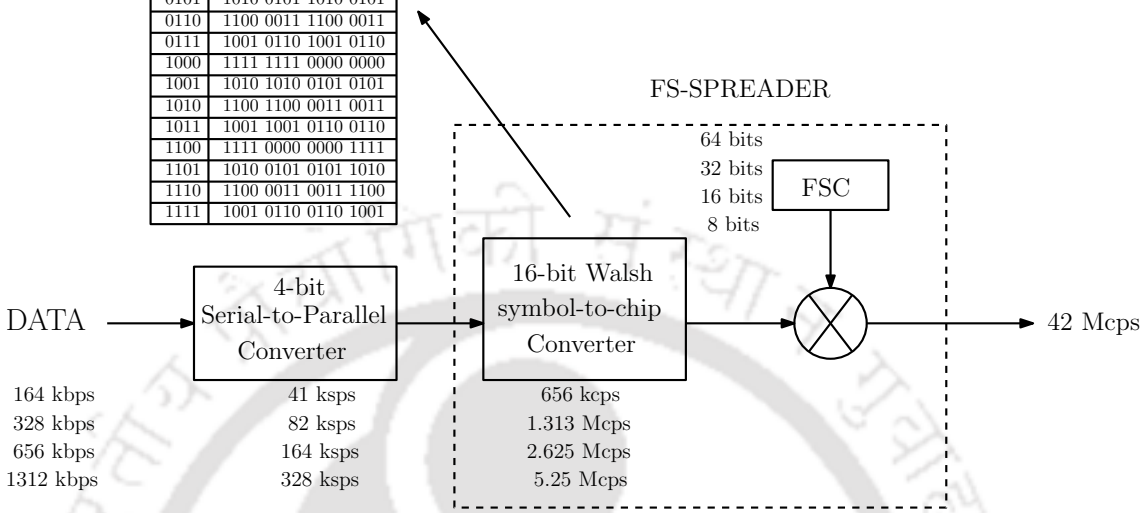

Figure 2.3: S2P and FS-Spreader Structure for PLCP Header and PSDU in HBC PHY [2]

The transmission of PPDU frame follows the frequency selective digital transmission (FSDT) scheme. The band of operation is centered at 21 MHz with the channel bandwidth of 5.25 MHz.

2.1.2.2 NB PHY

Fig. 2.4 illustrates the structure of the NB PPDU constructed by pre-appending the PLCP Preamble and the PLCP Header to the PSDU. The PLCP preamble aids the receiver in packet detection, timing synchronization and carrier-offset recovery. Two unique PLCP preambles are created for mitigation of false alarms from networks operating in the adjacent channels. Each preamble sequence of length 90 bits is constructed by the concatenation of a length-63 maximum length pseudo-noise sequence (m-sequence) and a 27-bit extension sequence as shown in Fig. 2.4. The 63-bit m-sequence is used for packet detection, coarse-timing synchronization and carrier-offset recovery. The 27-bit extension sequence is used for fine-timing synchronization.

The PLCP Header consists of the following sub-fields: a PHY Header, a four-bit Header Check Sequence (HCS) and Bose-Chaudhuri-Hocquenghem (BCH) parity bits for forward error correction (FEC). The PHY Header consists of the following sub-fields:

- RATE: it contains information of the data rate of the PSDU, the employed pulse shaping, the

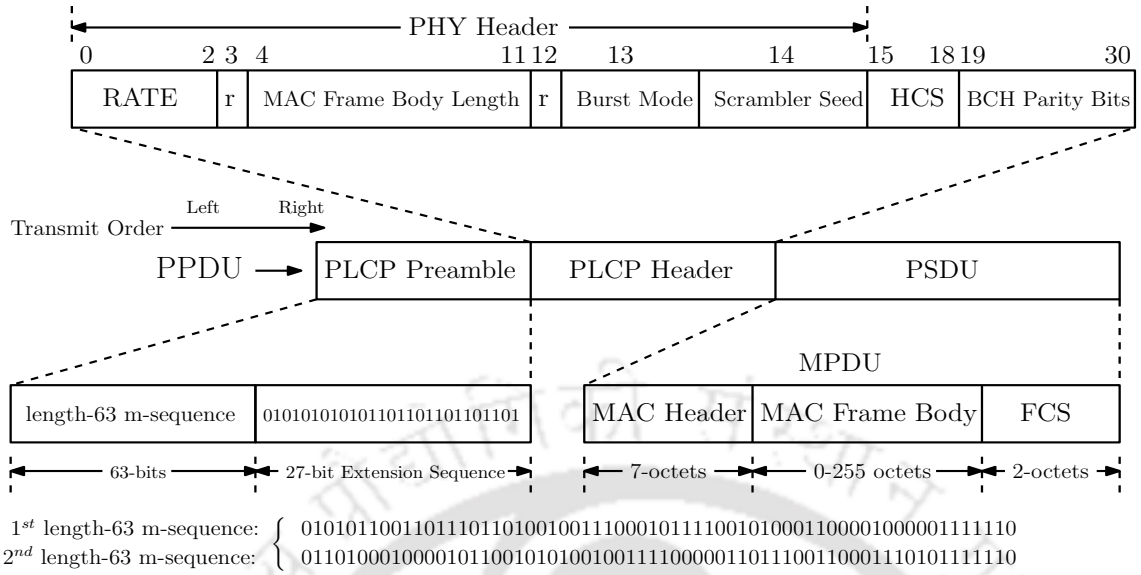

Figure 2.4: NB PPDU Structure [2]

type of modulation, the coding rate and the SF for the transmission of the PSDU

- MAC Frame Body Length: it contains information of the length of the MAC frame body
- Burst Mode: whether or not the next packet is a part of a burst of packets
- Scrambler seed: to eliminate long strings of ones and zeros in PSDU
- Reserved bits: 'r'

The four-bit HCS is generated from the PHY Header (of length 15 bits) by the Cyclic Redundancy Check 4 (CRC-4) polynomial $1 + x^2 + x^4$. The BCH parity bits are generated using a shortened BCH code (n=31, k=19, t=2) – a shortened code derived from a (n=63, k=51, t=2) BCH code. The concatenation of the PHY Header and HCS are the information bits to the BCH (31, 19, 2) code. The addition of the BCH parity bits improves the robustness of the PLCP Header.

The PLCP Preamble are directly mapped onto the desired constellation symbols as per the frequency band of operation. However, the PLCP Header and PSDU are configured prior of mapping the PPDU onto symbols. The PLCP Header are spread, interleaved and scrambled before being mapped onto symbols as shown in Fig. 2.5(a). The MPDU are configured before mapping to PSDU symbols as shown in Fig. 2.5(b) by the following steps: (i) Encoding using BCH (63,51) encoder (ii) addition of pad bits for alignment on a symbol boundary (iii) spreading with different SF determined by

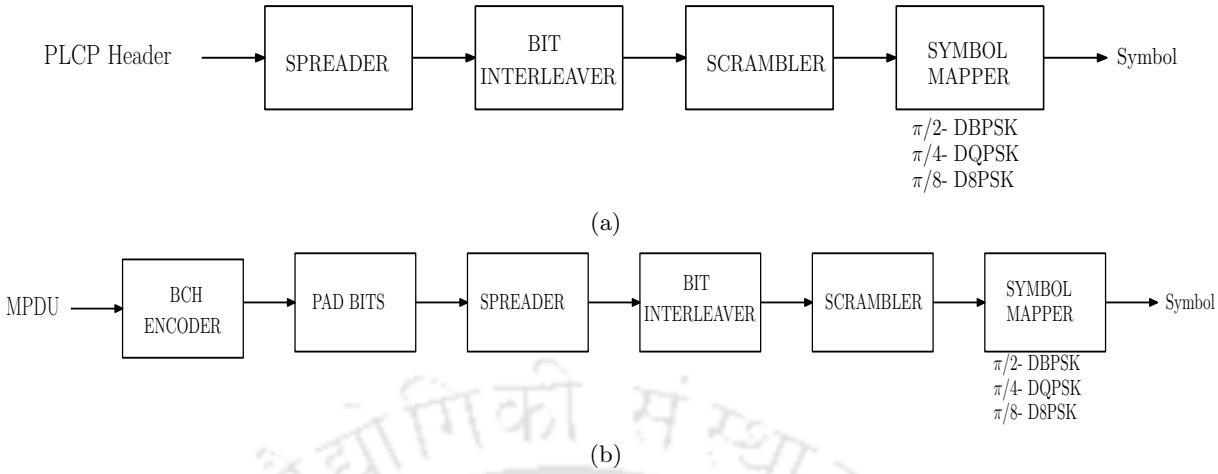

Figure 2.5: Transformation of PLCP Header and PSDU onto symbols for NB PHY structure [2]

frequency band of operation (iv) bit interleaving providing robustness against burst errors and (v) additive scrambling for elimination of long strings of '1' or '0's. The 2.4 GHz ISM and 2.36-2.4 GHz MBAN frequency bands use SF of 1, 2 or 4 while all other NB frequency bands use SF of 1 or 2.

The NB PHY employs differentially encoded phase-shift keying (DPSK) constellations, such as $\pi/2$- Differential binary-phase-shift-keying ($\pi/2$-DBPSK), $\pi/4$- Differential Quadrature-phase-shift-keying ($\pi/4$-DQPSK), $\pi/8$-Differential-8-phase-shift-keying ($\pi/8$-D8PSK) in all the frequency bands of operation except the 402-405 MHz band. The 402-405 MHz band uses Gaussian Minimum Shift Keying (GMSK) modulation. For DPSK constellation, the employed pulse shape is a Square Root Raised Cosine (SRRC) pulse while for GMSK, the pulse is a Gaussian pulse.

The SRRC pulse r(t) is given by (2.1) with a roll-off factor β and symbol period T_s (both are implementation dependent).

$$SRRC\ Pulse: \quad r(t) = \begin{cases} 1-\beta+4\frac{\beta}{\pi}, & \text{t} = 0 \\ \frac{\beta}{\sqrt{2}}\left[\left(1+\frac{2}{\pi}\right)sin\left(\frac{\pi}{4\beta}\right)+\left(1-\frac{2}{\pi}\right)cos\left(\frac{\pi}{4\beta}\right)\right], & t = \pm\frac{T_s}{4\beta} \\ \frac{sin\left[\pi\frac{t}{T_s}(1-\beta)\right]+4\beta\frac{t}{T_s}cos\left[\pi\frac{t}{T_s}(1+\beta)\right]}{\pi\frac{t}{T_s}\left[1-\left(4\beta\frac{t}{T_s}\right)^2\right]}, & otherwise \end{cases} \tag{2.1}$$

The Gaussian pulse g(t) is described in (2.2) with bandwidth-time product (BT) equal to 0.5.

$$Gaussian\ Pulse: \qquad g(t) = \frac{exp(\frac{-t^2}{2\delta^2})}{\sqrt{2\pi}\delta}, \qquad where\ \ \delta = \frac{\sqrt{ln(2)}}{2\pi BT} \tag{2.2}$$

2.1.2.3 UWB PHY

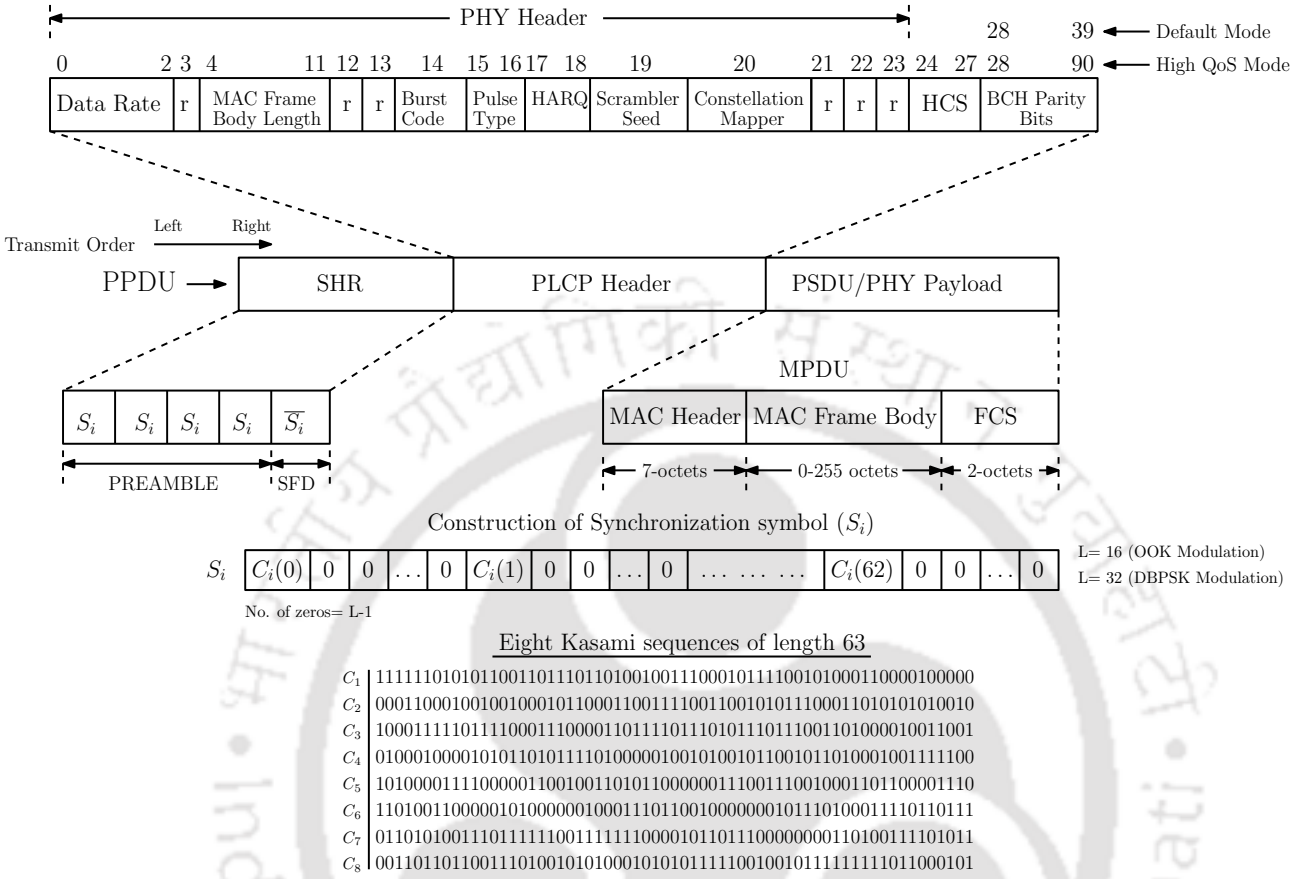

Figure 2.6: UWB PPDU Structure [2]

The IEEE 802.15.6 TG6 group defines two categories of UWB PHY: IR-UWB and FM-UWB. For applicability to a wide range of WBAN applications, the UWB PHY uses both IR-UWB and FM-UWB for defining two modes of operation. The modes are: (i) Default mode for both medical and non-medical applications and (ii) High Quality of Service (QoS) mode for high-priority medical applications only. The default mode supports IR-UWB as a mandatory PHY and FM-UWB as an optional PHY. However, for high QoS mode, the IR-UWB is the mandatory PHY with no inclusion of an optional PHY.

The PPDU or the UWB PHY frame format is formed by concatenation of the synchronization header (SHR), the PLCP Header and the PSDU (or PHY Payload) in that order. Fig. 2.6 gives a clear illustration of the UWB PPDU frame structure.

Construction of the SHR: The first component of the PPDU is the SHR. The construction of the SHR is similar in both the modes of operation. The SHR consists of two sub-fields: (i) Preamble

intended for timing synchronization, packet detection and carrier frequency offset recovery and (ii) Start-of-frame delimiter (SFD) for frame synchronization in the receiver. The preamble and the SFD are built with Kasami sequence of length 63. Kasami sequences have better cross-correlation properties compared to Gold code sequences [144]. The preamble is formed by four repetitions of the synchronization symbol S_i. Each synchronization symbol S_i is constructed from a Kasami sequence by zero-padding each bit of C_i with $(L-1)$ zeros as illustrated in Fig. 2.6. The Kasami sequence S_i can be only one of the eight Kasami sequences C_1, C_2, C_3, C_4, C_5, C_6, C_7 and C_8. The value of L depends on the employed modulation (L= 16 for OOK modulation or L= 32 for DBPSK modulation) during transmission of the SHR. Mathematically, the symbol S_i can be computed as:

$$S_i = C_i \otimes \delta_L \tag{2.3}$$

where $\otimes$ indicates the Kronecker product between Kasami sequence C_i and $\delta_L = (1, 0, \ldots, 0)_{1\times L}$.

After the construction of the preamble, the SFD (Fig. 2.6) is formed on the synchronization symbol $\overline{S_i}$. The symbol $\overline{S_i}$ is formed by zero-padding each bit of the sequence $\overline{C_i}$ (the bit-inversion or one's complement of C_i) with $(L-1)$ zeros. The bit-inversion of Kasami sequence is chosen for construction of the SFD, as they provide low cross-correlation with the preamble in order to minimize degradation during detection of the SFD. Mathematically, the SFD (or $\overline{S_i}$) can be computed as:

$$\overline{S_i} = \overline{C_i} \otimes \delta_L \tag{2.4}$$

where $\otimes$ indicates the Kronecker product between $\overline{C_i}$ and $\delta_L = (1, 0, \ldots, 0)_{1\times L}$.

For FM-UWB PHY, the SHR is formed only with preamble and no SFD. The preamble is formed by either one of the C_1-C_8 Kasami sequences without zero-padding. There is no repetition of the Kasami sequence in the preamble.

Construction of the PLCP Header: The PLCP Header, the second component of PPDU, consists of the following sub-fields: a 24-bit PHY Header, a 4-bit HCS sequence over the PHY header and BCH Parity bits. The PHY Header contains the information regarding data rate, length of the MAC Frame body, burst mode (decides whether or not the next packet is a part of burst of packets), the employed pulse waveform for transmission, Hybrid automatic repeat request (HARQ) retransmission flow, scrambler seed, the employed constellation (or symbol) mapping for on-off signaling and some reserved bits. The 24-bit PHY header is protected with a 4-bit CRC-4 ITU HCS. The appended BCH

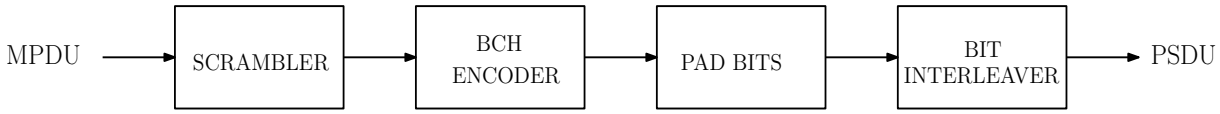

Figure 2.7: Configuration of MPDU to form PSDU for UWB PHY structure [2]

Table 2.1: Modulation Options of UWB PHYs for the Default and High QoS Modes of Operation [2]

Modes of Operation	UWB PHY	Modulation Options	Attribute	
			Mandatory	Optional
Default Mode	IR-UWB (Mandatory PHY)	On-off signaling†	✓	
		DBPSK		✓
		DQPSK		✓
	FM-UWB (Optional PHY)	FM-UWB	✓	
High QoS Mode	IR-UWB (Mandatory PHY)	On-off signaling		✓
		DBPSK	✓	
		DQPSK	✓	

†: Mandatory Symbol Mapper: Binary Signaling and Optional Symbol Mapper: 16-ary signaling

parity bits in the PLCP Header are generated onto 28 information bits (the concatenation of 24-bit PHY Header and 4-bit HCS). For the default mode, the PLCP appends 12 BCH parity bits generated using a BCH (n=40, k=28, t=2) code – a shortened code derived from the mother BCH (n=63, k=51, t=2) code. For the high QoS mode, the PLCP appends 63 BCH parity bits from a BCH (n=91, k=28, t= 10) code, a shortened version derived from the mother BCH (n=127, k=64, t=10) code [145].

Construction of the PSDU: The MPDU is configured to form the PSDU following the steps shown in Fig. 2.7. The first step is the additive scrambling of bits using a scrambler defined by the polynomial $g(x) = 1 + x^2 + x^{12} + x^{13} + x^{14}$. This step eliminates the dependency of the signal's power spectrum onto the actual MPDU data by eliminating long strings of 0's and 1's. The second step is BCH encoding of the scrambled data. For default mode, a BCH (n=63, k=51, t=2) code is used while for high QoS mode, a BCH (n=126, k= 63, t=10) code together with Type-II HARQ mechanism is used. The third step is addition of pad bits for alignment on a symbol boundary with respect to constellation mapper in the PHY Header. The last step is bit interleaving (using an algebraic interleaver) to provide robustness against error propagation. The major advantage of adopting bit interleaving is the effective handling of burst errors, as the correction capability of a BCH code is limited in case of burst errors. The algebraic interleaver denotes a new interleaved address $\Pi(n)$ of the index n defined by

$$\Pi(n) = nb_s \, Mod \; N_I \tag{2.5}$$

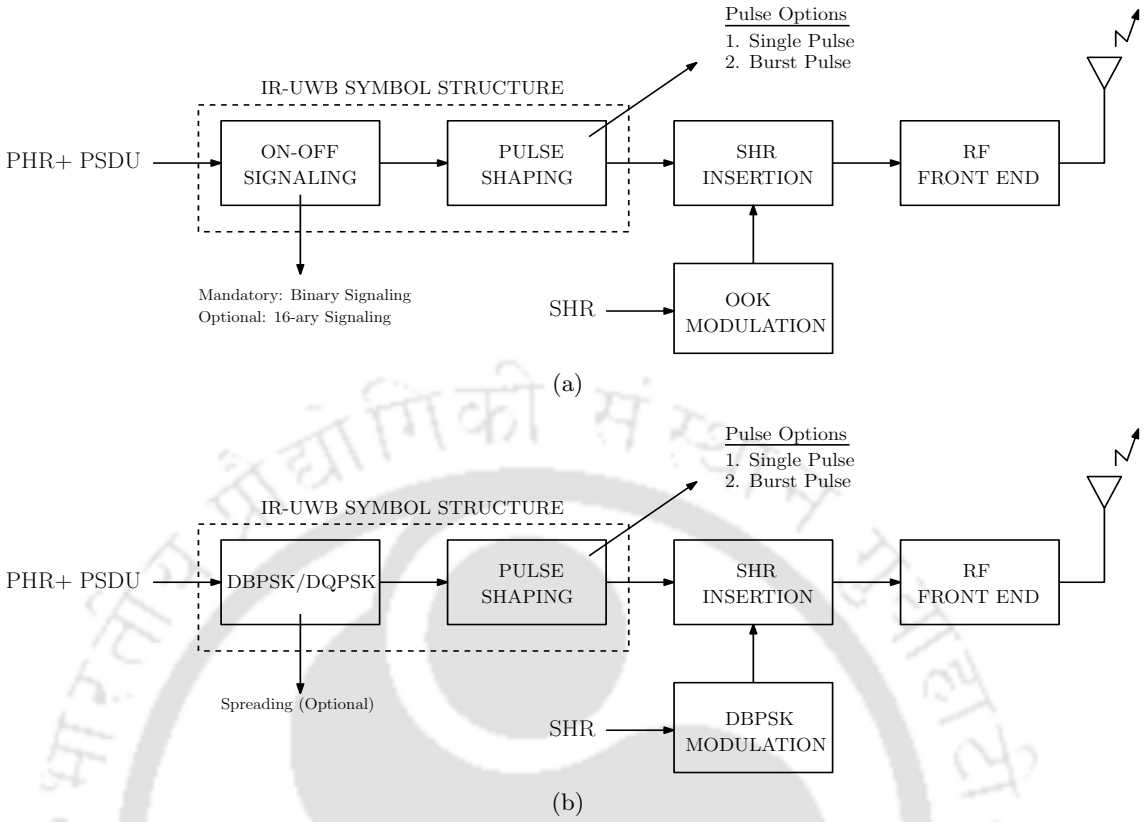

Figure 2.8: IR-UWB PHY Transmission Structure for (a) Default mode (b) High QoS mode of operation [2]

where N_I = Interleaver length set to 192, b_s= 37 and $Mod\ N_I$ represents modulo N_I arithmetic. The rule for the last interleaved block is to set $N_I = N_{rem}$, if $N_{rem} = rem\ (N_T, N_I) \neq 0$, where N_T is the total number of bits to be interleaved.

Transmission of the PPDU: The possible modulation options for transformation of the PPDU into radio signals are: (i) On-off Keying (OOK) modulation (ii) On-off Signaling: Binary signaling or 16-ary signaling (iii) Differentially encoded Binary-phase-shift-keying (DBPSK) (iv) Differentially encoded Quadrature-phase-shift-keying (DQPSK) and (v) FM-UWB: a combination of continuous-phase binary-frequency-shift-keying (CP-BFSK) and wideband FM. Table 2.1 summarizes modulation options of the UWB PHYs for the default and high QoS modes of operation.

In IR-UWB PHY, the PLCP handles the transmission of the PHR and the PSDU compared to the SHR. Both PHR and the PSDU employ the same principle of transmission concerning the chosen modulation option, the data rate, the pulse shape and the timing parameters.

Fig. 2.8(a) and Fig. 2.8(b) respectively illustrate the transmission structure of IR-UWB PHY for

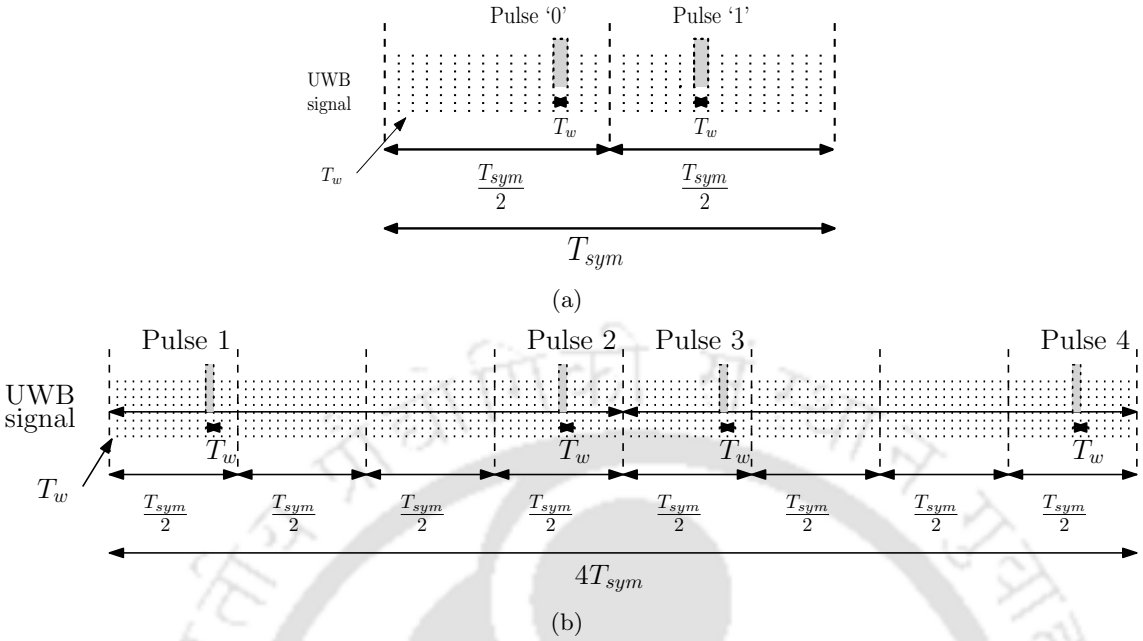

Figure 2.9: IR-UWB symbol structure for (a) 2-ary symbol mapper (b) 16-ary symbol mapper

Table 2.2: Symbol Mapper for 2-ary Waveform coding [2]

Data Symbol Decimal	Data symbol binary b_0	Codeword d_0, d_1
0	0	10
1	1	01

default mode and high QoS mode. A detailed description of the IR-UWB symbol structure for both the modes of operation is described below:

- ***On-off signaling:*** On-off signaling is a combination of M-ary waveform coding with OOK modulation. This signaling can also be termed as M-ary pulse position modulation (PPM). For binary signaling, the IR-UWB symbol structure for a 2-ary symbol of duration T_{sym} is shown in Fig. 2.9(a). The symbol duration T_{sym} consists of N_w= 32 pulse waveform positions (i.e. T_{sym}= $N_w T_w$). Each pulse waveform is of duration T_w. Each data symbol is coded into a 2-bit codeword (d_0, d_1) as shown in Table 2.2. If the data symbol is '0', the pulse is placed in the first half of the symbol duration on any one of the $N_w/2$ hopping positions. On the other hand, if the data symbol is '1', the pulse is placed on the second half of symbol duration on any one of the $N_w/2$ hopping positions. The hopping positions are determined by standard-specific time-hopping sequence generator [2] to support co-existence of multiple BANs.

Table 2.3: Symbol Mapper for 16-ary Waveform coding [2]

Data symbol decimal	Data symbol binary (b_0, b_1, b_2, b_3)	Codeword $(d_0, d_1, ...d_7)$
0	0000	00001111
1	0001	00010111
2	0010	00110011
3	0011	00011011
4	0100	01011010
5	0101	00111100
6	0110	01010101
7	0111	01100110
8	1000	01101001
9	1001	10011001
10	1010	10010110
11	1011	10100101
12	1100	10101010
13	1101	11000011
14	1110	11001100
15	1111	11110000

The IR-UWB symbol structure for a 16-ary symbol of symbol duration $4T_{sym}$ is shown in Fig. 2.9(b). The symbol duration is divided into eight intervals each of duration $T_{sym}/2$. Each data symbol is coded into eight-bit codeword and is shown in Table 2.3. For example, if the data symbol is '1001', the codeword is '10011001'. This results in transmission of four pulses, since the '1' and the '0' in the codeword indicates the presence and absence of IR-UWB pulse respectively. The four pulses are placed in the first, fourth, fifth and eight interval as shown in Fig. 2.9(b). The pulse is placed in any one of the $N_w/2$ hopping positions determined by time-hopping sequence generator [2].

The pulse waveform can be placed in accordance to either one of the two pulse options: (i) Single-pulse option or (ii) Burst pulse option: a concatenation of short pulses. For single-pulse option, a single long pulse of duration $T_w = T_p$ is employed, where T_p is the pulse duration. The burst pulse option follows the traditional concept of IR-UWB pulse with T_p less than or equal to 2 ns [146]. For burst pulse option, a burst of N_{cpb} concatenated and dynamically scrambled short pulses of duration $T_w = N_{cpb}T_p$ is employed where $N_{cpb} > 1$ and $T_p = 1/\text{PPRF}$, where PPRF is the peak pulse repetition frequency and is equal to 499.2 MHz[6]. The value of N_{cpb} varies from 1 to 32. The value N_{cpb}=1 refers to the single pulse option.

- ***DBPSK/DQPSK:*** The IR-UWB symbol structure for a DBPSK/DQPSK symbol of duration T_{sym} is shown in Fig. 2.10. The symbol duration T_{sym} consists of $N_w = 32$ pulse waveform

[6]Note: The PPRF of 499.2 MHz is applicable to the default mode and high QoS modes of operation

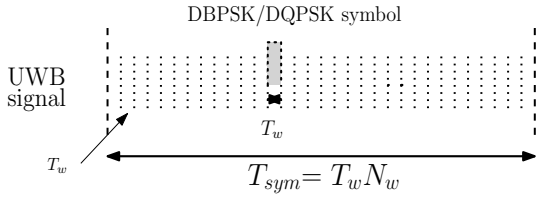

Figure 2.10: IR-UWB symbol structure for DBPSK/DQPSK symbol

Table 2.4: Generation of DBPSK symbol [2]

Information Bit (b_m)	Phase (ϕ_{m+1})
0	0
1	π

Table 2.5: Generation of DQPSK symbol [2]

Information Bits		Phase
g_{2m}	g_{2m+1}	ϕ_{m+1}
0	0	0
0	1	$\frac{\pi}{2}$
1	0	$\frac{3\pi}{2}$
1	1	π

positions (i.e. $T_{sym}= N_w T_w$). Each data symbol (one bit for DBPSK and two bits for DQPSK) is coded in such a way that the information is encoded in the phase-change of the consecutive DBPSK/DQPSK symbol. Table 2.4 and Table 2.5 illustrate generation of DBPSK and DQPSK symbols respectively. The DBPSK/DQPSK symbol is placed on any one of the N_w hopping position determined by time-hopping sequence generator [2]. The spreading of DBPSK/DQPSK symbol using a 7-bit Barker sequence is an optional feature employed for enhancement of interference rejection by making the amplitude level of side-lobes down to 1/N times (for N-bit Barker sequence) the peak signal [147]. Although the spreading technique enhances the interference rejection, the data rate however reduces by seven times the original data rate (without spreading). The single pulse option follows the same principle as used in on-off signaling. However, for burst pulse option, a burst of N_{cpb} concatenated and statically scrambled short pulses of duration $T_w= N_{cpb} T_p$ is employed. The value of N_{cpb} varies from 1 to 32. The value N_{cpb}=1 refers to the single pulse option.

Transmission of the SHR: An important feature of the SHR is that it is inserted right before transmission. The transmission of the SHR follows OOK modulation in case of default mode and

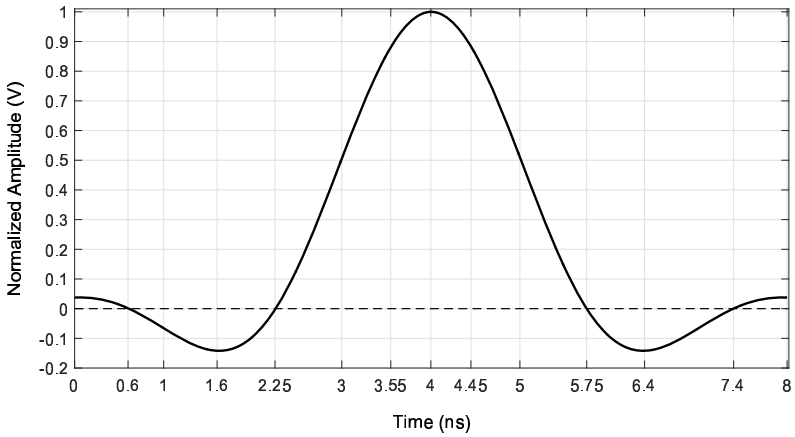

Figure 2.11: Reference pulse

follows DBPSK modulation in case of high QoS mode. The SHR is transmitted at the fixed data rate of 3.9 Mbps regardless of the data rate of the PHR and the PSDU. For single pulse option, a single pulse of T_w= 8 ns is employed. In case of burst pulse option, a burst of N_{cpb}= 4 concatenated and statically scrambled short pulses of duration $T_w = N_{cpb}T_p$ is employed for both OOK and DBPSK modulation.

PULSE SHAPE: There is no mandatory pulse shape for IR-UWB PHY. The Task Group TG6 define a set or a pool of IR-UWB pulse shapes that can be employed for transmission. The pulse shapes are as follows.

- ***Short Pulse Shape:*** Any short pulse shall be considered as a candidate pulse shape *p(t)* that is similar to the reference pulse *r(t)* defined by (2.6) with a roll-off factor β= 0.5 and T_s= T= 1/499.2 MHz.

$$Reference\ Pulse^{7}: \quad r(t) = \begin{cases} 1-\beta+4\frac{\beta}{\pi}, & t = 0 \\ \frac{\beta}{\sqrt{2}}\left[\left(1+\frac{2}{\pi}\right)sin\left(\frac{\pi}{4\beta}\right)+\left(1-\frac{2}{\pi}\right)cos\left(\frac{\pi}{4\beta}\right)\right], & t = \pm\frac{T_s}{4\beta} \\ \frac{sin\left[\pi\frac{t}{T_s}(1-\beta)\right]+4\beta\frac{t}{T_s}cos\left[\pi\frac{t}{T_s}(1+\beta)\right]}{\pi\frac{t}{T_s}\left[1-\left(4\beta\frac{t}{T_s}\right)^2\right]}, & otherwise \end{cases} \tag{2.6}$$

The reference pulse r(t) is shown in Fig. 2.11. However, the pulse *p(t)* is constrained with

[7]Equation (2.1) is repeated as Equation (2.6) for ready reference

the criterion that the absolute value of its cross-correlation with the SRRC reference pulse *r(t)* should be at least 0.8 in the main lobe. This type of pulse shape can be used for OOK, on-off signaling and DBPSK modulation and is applicable for both single pulse and burst pulse options.

- ***Chaotic Pulse Shape:*** Chaotic pulses are signals that are of near constant envelope produced by addition of different sawtooth or triangular waveforms. Since the addition of waveforms is frequency modulated, a chaotic pulse waveform *p(t)* can be expressed by (2.7) in complex baseband representation, where $f_i(t)$ is the instantaneous frequency deviation described by (2.8) and (2.9). Here, N_t is the number of sawtooth or triangular waveforms, A_i and T_i respectively are the amplitude and period of the i^{th} sawtooth/triangular waveform – defined in the interval $\frac{-T_i}{2} \leq t \leq \frac{T_i}{2}$.

$$p(t) = e^{j\left(2\pi \int\limits_{-T_w/2}^{t} f_i(t')\ dt'\right)} \tag{2.7}$$

$$f_i(t) = \sum_{i=1}^{N_t} S_i(t) \tag{2.8}$$

$$S_i(t) = \begin{cases} 2A_i\left[\frac{t}{T_i} - \lfloor \frac{t}{T_i} + 0.5 \rfloor\right], & \text{Sawtooth Waveform} \\ A_i\left[4\left|\frac{t}{T_i} - \lfloor \frac{t}{T_i} + 0.5 \rfloor\right| - 1\right], & \text{Triangular Waveform} \end{cases} \tag{2.9}$$

This type of pulse shape cannot be used for DBPSK/DQPSK modulation; however, it can be used for OOK, on-off signaling and is applicable to single pulse option only.

- ***Chirp Pulse Shape:*** Chirp pulses are passband signals that can be generated by highly linear voltage control oscillators (VCOs) [142]. A compliant chirp pulse in complex baseband representation is described by (2.10).

$$p(t) = \psi(t)\ e^{j\left(2\pi \int\limits_{-T_w/2}^{t} f_i(t')dt' + \theta_0\right)} \tag{2.10}$$

$$\psi(t) = \begin{cases} \psi_u(t), & \frac{-T_w}{2} \le t \le \frac{-T_w}{2} + T_u \\ 1, & \frac{-T_w}{2} + T_u \le t \le \frac{T_w}{2} - T_d \\ \psi_d(t), & \frac{T_w}{2} - T_d \le t \le \frac{T_w}{2} \\ 0, & elsewhere \end{cases} \tag{2.11}$$

$$f_i(t) = K_c t + f_{err}(t), \qquad \frac{-T_w}{2} \le t \le \frac{T_w}{2} \tag{2.12}$$

$$\sqrt{\frac{\int_{-T_w/2}^{T_w/2} f_{err}(t)^2 \, dt}{T_w}} \quad \le \quad 0.05\Delta f \tag{2.13}$$

Here, θ_0 is an arbitrary constant phase and $\psi(t)$ is a window function given by (2.11). Further, $\psi_u(t)$ and $\psi_d(t)$ are the arbitrary continuous monotonic non-negative functions that satisfies the conditions: (i) $\psi_u(-T_w/2) = 0$, (ii) $\psi_u(-T_w/2 + T_u) = 1$, (iii) $\psi_u(T_w/2 - T_d) = 1$ and (iv) $\psi_u(T_w/2) = 0$. T_u and T_d are transition times bounded by $0 < T_u \le 2$ ns and $0 < T_d \le 2$ ns, respectively. $f_i(t)$ is the instantaneous frequency of the chirp signal described by (2.12) with $K_c = \frac{\Delta f}{T_w}$ as the constant chirping slope. The frequency sweep of a chirp signal is $\Delta f = 520$ MHz and $f_{err}(t)$ is an arbitrary instantaneous frequency error function bounded by the relation (2.13). In case of an ideal chirp ($f_{err} = 0$), the pulse shape *p(t)* can be represented by (2.14).

$$p(t) = \psi(t) \; e^{j\left(2\pi \frac{K_c t^2}{2} + \theta_0\right)} \tag{2.14}$$

This type of chirp pulse shape can be used only in single pulse option for OOK, on-off signaling and DBPSK/DQPSK modulations.

FM-UWB PHY: The transmission structure of the FM-UWB PHY is shown in Fig. 2.12 and is described below:

- For CP-BFSK modulation, a sub-carrier signal *s(t)* of frequency $f_{sub} = 1.5$ MHz is employed. The signal s(t) defined in (2.15) generated from the information bearing signal *b(t)* – a bipolar Gaussian pulse shape with bandwidth-symbol duration product of 0.8 and modulating-carrier signal S(t) that can be either a triangular waveform, a sawtooth waveform, or a sine waveform.

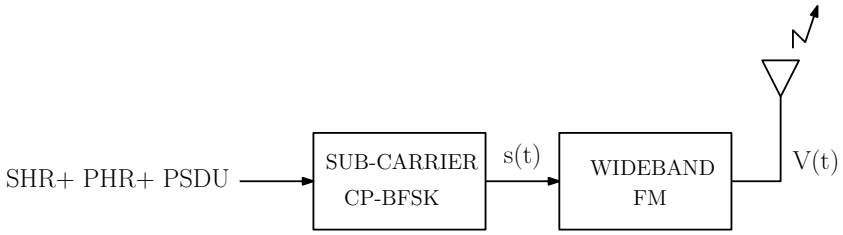

Figure 2.12: FM-UWB Transmission Structure [2]

The signal S(t) is given by (2.16), where A is the amplitude of the signal, ϕ_0 is the initial phase of the modulating-carrier signal and Δf_{sub} is the peak frequency deviation.

$$s(t) = A\ S\Big(2\pi f_{sub}t + 2\pi\Delta f_{sub}\int_{-\infty}^{t} b(t')dt' + \phi_0\Big) \tag{2.15}$$

$$S(t) = \begin{cases} 4\Big|f_{sub}t - \lfloor f_{sub}t + 0.5\rfloor\Big| - 1, & \text{Triangular Waveform} \\ 2\Big(f_{sub}t - \lfloor f_{sub}t + 0.5\rfloor\Big), & \text{Sawtooth Waveform} \\ sin(2\pi f_{sub}t), & \text{Sine Waveform} \end{cases} \tag{2.16}$$

- Next, the sub-carrier signal S(t) is modulated with wideband FM to create a constant-envelope signal V(t) as described by (2.17).

$$V(t) = A\ sin\Big(2\pi f_c t + 2\pi\Delta f\int_{-\infty}^{t} S(t')dt'\Big) \tag{2.17}$$

Here, A is the amplitude of the signal, Δf = K_0V is the peak frequency deviation, K_0 is the RF oscillator sensitivity in radian/volt and f_c is the central frequency of the UWB frequency band.

OPERATIONAL FREQUENCY BANDS: The 3.1-10.6 GHz UWB frequency band is divided into two frequency groups: low-band (3.25-4.75 GHz) and high-band (6.25-10.25 GHz) group as shown in Table 2.6. The low-band is again divided into three sub-bands or channels: Ch.#0, Ch.#1 and Ch.#2 (Table 2.6). The high-band group is also sub-divided into eight sub-bands or channels: Ch.#3, Ch.#4, Ch.#5, Ch.#6, Ch.#7, Ch.#8, Ch.#9 and Ch.#10 (Table 2.6). Each sub-band or channel is of bandwidth 499.2 MHz (∼500 MHz). Ch.#1 and Ch.#6 respectively are the mandatory channels in the low-band and in the high-band.

Table 2.6: UWB Operating Frequency Bands [2]

Band Group	UWB Channel	Central Frequency	Channel Bandwidth	Channel Attribute	
				Mandatory	Optional
Low-band (3.25- 4.75 GHz)	Ch.#0	3494.4 MHz	499.2 MHz		✓
	Ch.#1	3993.6 MHz		✓	
	Ch.#2	4492.8 MHz			✓
High-band (6.25- 10.25 GHz)	Ch.#3	6489.6 MHz			✓
	Ch.#4	6988.6 MHz			✓
	Ch.#5	7488 MHz			✓
	Ch.#6	7987.2 MHz		✓	
	Ch.#7	8486.4 MHz			✓
	Ch.#8	8985.6 MHz			✓
	Ch.#9	9484.8 MHz			✓
	Ch.#10	9984 MHz			✓

The channels Ch.#0, Ch.#2, Ch.#4, Ch.#6, Ch.#8 and Ch.#10 are even physical channels; Ch.#1, Ch.#3, Ch.#5, Ch.#7 and Ch.#9 are odd physical channels. Each physical channel has four possible logical channels, since each physical channel has a possible set of four preamble sequences (constructed from Kasami sequence shown in Fig. 2.6). The odd physical channel uses the first pool of Kasami sequences (C_1, C_2, C_3 and C_4) while the even physical channel uses the second pool of Kasami sequences (C_5, C_6, C_7 and C_8). The coordinator of a BAN scans all the logical channels of a particular physical channel and prefers the preamble sequence with minimum received power-level. As different BANs use different preamble sequences, the Kasami sequence improves coexistence of multiple BANs and also aids in interference mitigation.

TRANSMIT SPECTRAL MASK: The mandatory transmit spectral mask for both of the IR-UWB PHY and the FM-UWB PHY is described by

$$M(f) = \begin{cases} 0, & \mid f - f_c \mid < \frac{0.5}{T} \\ -60\left[\mid f - f_c \mid T - 0.5\right], & \frac{0.5}{T} \leq \mid f - f_c \mid < \frac{0.8}{T} \\ -10\left[\mid f - f_c \mid T - 0.8\right] - 18, & \frac{0.8}{T} \leq \mid f - f_c \mid \leq \frac{1}{T} \\ -20, & \mid f - f_c \mid > \frac{1}{T} \end{cases} \tag{2.18}$$

Here, f_c is the central frequency of either one of the physical channels (Ch.#0 to Ch.#10) and T= 1/499.2 MHz. Fig. 2.13 shows the transmit spectral mask for Ch.#1 (the mandatory low-band UWB channel).

Fig. 2.14 shows the relative power spectral density (PSD) of the reference pulse r(t) (Fig. 2.11). It is clear that the PSD of the pulse r(t) is within the transmit spectral mask. Hence, the SRRC

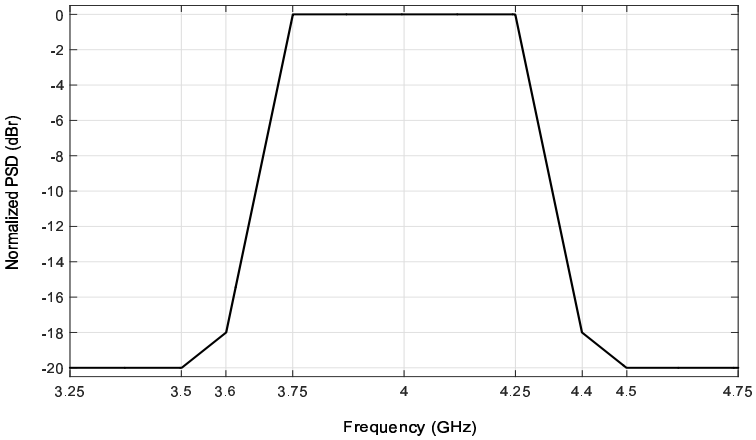

Figure 2.13: Transmit Spectral Mask for the mandatory low-band UWB Channel: Ch.#1

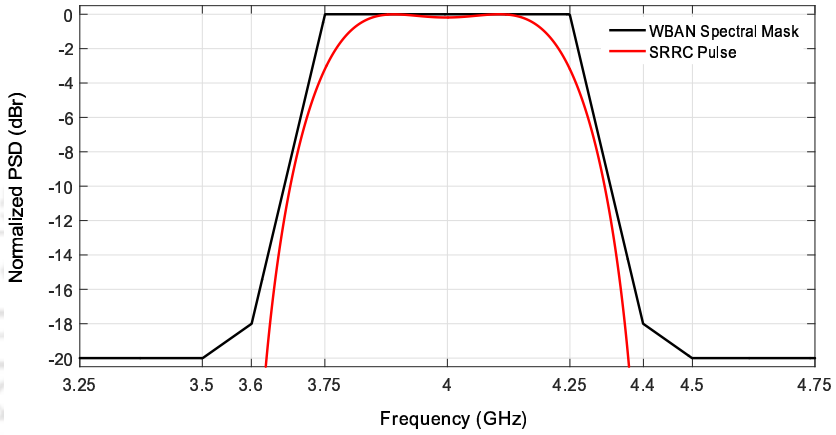

Figure 2.14: PSD of SRRC reference pulse r(t) centered at 3993.6 MHz (≈ 4 GHz) in the mandatory low-band UWB Channel (Ch.#1) satisfying the transmit spectral mask

reference pulse r(t) itself can be considered as the pulse shape p(t) for transmission. It may be noted that the SRRC pulse is not a physically realizable pulse – it can only be approximated.

Rules for the use of UWB PHY in a BAN Transceiver: A transceiver is a unit which contains a receiver and a transmitter for an effective two-way communication. The use of an IR-UWB transceiver and a FM-UWB transceiver in a BAN (constructed of a hub and devices) is defined in the following:

- A hub shall implement either an IR-UWB transceiver only
- A hub shall implement both IR-UWB and FM-UWB transceivers
- A device shall implement an IR-UWB transceiver only

Table 2.7: Mandatory Procedure of UWB PHYs in Default mode and High QoS mode [2]

UWB PHY Definitions	Default Mode		High QoS Mode
	IR-UWB	FM-UWB	IR-UWB
Mandatory PPDU	✓	✓	✓
Mandatory Data Rate	0.4875 Mbps	250 kbps	0.4875 Mbps
Mandatory Modulation	On-off signaling†	FM-UWB	DBPSK/DQPSK
Mandatory Physical Channel	(Ch.#1 and Ch.#6)*	Ch.#6	(Ch.#1 and Ch.#6)*
Mandatory Transmit Spectral Mask	✓	✓	✓
Mandatory HARQ	×	×	✓

†: Mandatory Symbol Mapper: Binary Signaling and Optional Symbol Mapper: 16-ary signaling
*: Implementers can choose any one of the physical channel: Ch.#1 or Ch.#6

Table 2.8: Data Rates for UWB PHYs in Default and High QoS Modes of Operation [2]

Modes of Operation	UWB PHY	Modulation Options	Data Rate	Attribute	
				Mandatory	Optional
Default Mode	IR-UWB	On-off signaling†	0.4875 Mbps	✓	
			0.975 Mbps		✓
			1.95 Mbps		✓
			3.9 Mbps		✓
			7.8 Mbps		✓
			15.6 Mbps		✓
	FM-UWB	FM-UWB	250 Kbps	✓	✓
High QoS Mode	IR-UWB	DBPSK	0.4875 Mbps	✓	
			0.975 Mbps		✓
			1.95 Mbps		✓
			3.9 Mbps		✓
			7.8 Mbps		✓
			0.557 Mbps‡		✓
		DQPSK	15.6 Mbps		✓
			1.114 Mbps‡		✓

†: Mandatory Symbol Mapper: Binary Signaling and Optional Symbol Mapper: 16-ary signaling
‡: Spreading Factor= 7

- A device shall implement a FM-UWB transceiver only
- A device shall implement both IR-UWB and FM-UWB transceivers

From the above definition, it is clear that a hub always needs to support and implement an IR-UWB transceiver compulsorily, although the IR-UWB transceiver is left unutilized in the same hub. But, a device can support and implement either one of the IR-UWB and FM-UWB transceivers.

The mandatory procedure of UWB PHYs for the design of an IR-UWB transceiver or a FM-UWB transceiver in default mode and high QoS mode of operation is illustrated in Table 2.7. The data rates for UWB PHYs in both the modes of operation is also illustrated in Table 2.8.

2.2 Transceivers for Body Area Networks: A State-of-the-Art Review

Several transceivers on BANs reported in literature in recent years are considered. These implementations are diverse; hence only a selected few – starting from the year 2000s are presented.

2.2.1 BCC/HBC Transceivers

In 2004, Shinagawa *et al.* [148] from NTT MicroSystem Integration Laboratories, Japan, developed a near-field sensing transceiver for intra-body communication based on electrooptic effect. This is the first successful 10 Mb/s half-duplex communication conforming to the IEEE 802.3 [149] standard involving human body communication (intra-body communication through clothes and inter-body communication between two persons by a handshake).

In 2006, Seong-Jun Song *et al.* [150,151] from Korea Advanced Institute of Science and Technology (KAIST) presented the first wideband signaling (WBS) transceiver with direct coupling interface (DCI) exploiting the *Bodywire* Channel [8]. The transceiver employs a non-return-to-zero (NRZ) data transmitter and an all-digital clock-and-data-recovery (CDR) based WBS receiver. In 2007, Song *et al.* [152] from KAIST proposed a low-power and scalable WBS transceiver adopting direct sequence spread spectrum (DSSS) technique for narrowband interference rejection and three-level pulse shaping for PPM signals in analog front-end. This transceiver exploits UWB-like pulse modulation and a 1-bit analog-to-digital converter (ADC) for pulse detection; however the ADC failed to provide the required dynamic range for cancelation of the interference. In 2008, Cho *et al.* [153,154] from KAIST proposed a body channel transceiver (BCT) utilizing adaptive frequency hopping (AFH) technique. The transceiver is designed to handle in-band interferences higher than -20 dBm. The BCT has four hopping sub-bands, each sub-band from a 90MHz band (the frequency range of BCC is from 30MHz to 120MHz as per the channel analysis [102]). In 2009, Cho *et al.* [155,156] from KAIST presented a dual-band transceiver compatible with the 30-70 MHz BCC band and the 402-405 MHz MICS band. The transceiver employs a variable AFH technique proposed in [153,154] for interference rejection and supports the concurrent operation of the BCC and the MICS band signals.

In 2009, Alberto Fazzi *et al.* [157] from Philips Research Group, The Netherlands, proposed a BCC transceiver coupling a wideband digital signal to the human body similar to [152]. The transceiver employs a Manchester coding data transmitter and a correlation-based receiver for attenuation of

[8]The frequency range of *Bodywire* Channel is from 10KHz to 100MHz

poorly correlated signals to the expected signal and for suppression of interference.

A few IEEE 802.15.6-compliant BCC transceivers are reported below:

In 2011, Joonsung Bae *et al.* [158, 159] from KAIST presented an IEEE 802.15.6 compliant BCC transceiver adopting a highly scalable double-FSK modulation scheme (based on UWB-FM [160]). The transceiver employs low-power circuit techniques: a reconfigurable LNA (low-noise amplifier) with contact impedance sensing technique, a current-reuse wideband modulator, a divider based local-oscillator (LO) generation with duty-cycle corrector and a divider based digital double-FSK modulator. Later, in 2012, Bae *et al.* [161] proposed a crystal-less BCC transceiver adopts an injection-locking digitally controlled oscillator (IL-DCO) [162] in place of a crystal-oscillator (XO). The transceiver employs an auto-frequency calibration technique using an IL-detector and scalable double-FSK modulation scheme [158, 159]. In 2012, Shikada and Wang [163] have developed an IR-type HBC transceiver that employs digital-data modulation using wide-band pulse signals [164] instead of a sinusoidal signal (which is preferred for narrow-band modulation schemes). A successful solution to the stringent HBC transmit spectral mask (one of the design challenge in HBC transceiver) was demonstrated by Liu *et al.* [165] by reducing the second-order intermodulation (IM2) products of the transmitting signal. Hyungwoo Lee *et al.* [166] from KAIST presented a state-of-the-art HBC transceiver with its applicability to multi-channel electro-puncture[9]. The transceiver employs an active-digital-bandpass filter (ADF) based transmitter to meet the stringent transmit spectral mask [2] and a power-hungry voltage-controlled oscillator (VCO) based BPSK demodulator at the receiver. Later on, Hyunwoo Cho [167] from KAIST proposed an HBC transceiver employing three key techniques: (i) An analog active filter rather than ADF [166] (ii) Delay-locked-loop (DLL) based BPSK demodulator instead of VCO-based demodulator [166] at the receiver (iii) a received signal strength indicator (RSSI) to measure the received signal power for low-power mode (LP-mode) receiver and (iv) a reconfigurable LNA with RSSI. The RSSI in [167] is the first RSSI presented for the HBC transceiver. Later, Jaeeun Jang *et al.* [168] proposed a low-power adaptive duty-controlled current reusing RSSI for HBC transceivers. This current-reusing technique reduces the power consumption of the RSSI to 45%.

Two state-of-the-art data rate enhancement techniques for an IEEE 802.15.6-compliant BCC transceiver are proposed: (i) a modified FSDT (M-FSDT) [169] and (ii) an amplitude modulated FSDT (AM-FSDT) [170]. The M-FSDT and AM-FSDT techniques provide maximum data rates

[9]Electro-puncture is a combination of acu-puncture and electro-stimulation for effectiveness in pain-relief, treatment of depression, addiction, gastro-intestinal disorders and obesity treatment

of 3.9375 Mbps and 2.625 Mbps, respectively. Later, Junghyup Lee *et al.* [171] presented a 60 Mb/s wideband BCC transceiver[10] employing three key techniques: (i) a three-level direct digital Walsh-coded signaling at the transmitter, (ii) transient-detection based receiver using differentiator-integrator and IL-based clock recovery and (iii) a high-input impedance (unlike a low-input impedance in [152, 154, 159, 166]) and an equalizer at the receiver front-end. Recently, Ji-Hoon Lee *et al.* [172] proposed a 150 Mb/s BCC transceiver employing a decision feedback equalization (DFE) technique achieving the maximum data rate of 150 Mb/s and 100 Mb/s comunicating through 20 cm and 1 m respectively through the human body.

Tsou *et al.* [173] presented a dual-mode HBC receiver adopting a FSDT-based transmitter [2]. Hyunwoo Cho *et al.* [174] presented a full-duplex dual band (40/160 MHz) BCC transceiver and a 13.56 MHz R-C oscillator based super-regenerative receiver[11]. The dual-band BCC transceiver employs 40 MHz sine wave and 160 MHz rectangular wave for modulation in the transmitter and the shared-loop BPSK receiver. The super-regenerative receiver employs an OOK transmitter and a R-C oscillator based receiver with interference rejection greater than 60 dB. Chung *et al.* [176] presented a high data rate (1 Mb/s-40 Mb/s) WBS BCC transceiver. The transceiver employs a non-return-to-zero-inverted (NRZI) data transmitter and a blind 7X oversampling CDR receiver. Recently, Chung *et al.* [177] presented an all-digital WBS BCC (1 Mb/s-20 Mb/s) transceiver adopting a NRZI data transmitter [176] and proposed a reference-less all-digital CDR receiver.

2.2.2 NB Transceivers

In 2006, Yu *et al.* [178] from National Chiao-Tung University, Taiwan, presented a multi-tone code-division-multiple access (MT-CDMA) based WBAN system operating in 1395-1400 MHz WMTS band for ubiquitous healthcare monitoring. The MT-CDMA scheme was developed by L. Vandendorpe [179]. Later, in 2011, Shih *et al.* [180] proposed an OFDM based wireless-body-on-chip (WiBoC) baseband transceiver operating in 1395-1400 MHz WMTS band. Later, in 2011, Vidojkovic *et al.* [181] from Imec[12] and Holst Centre presented an ultra-low power (ULP) WBAN transceiver employing an OOK transmitter and a super-regenerative receiver operating in 2.36-2.4 GHz MBAN and 2.4 GHz ISM frequency bands. Taris *et al.* [182] presented an ULP 2.4 GHz ISM transceiver employing device optimization approach. Xin Liu *et al.* [183, 184] presented an ULP 250-kbps baseband transceiver

[10]The upper bound of the data rate for an IEEE 802.15.6-compliant BCC transceiver is 1.3125 Mbps
[11]The super-regeneration technique [175] was first introduced by Edwin Armstrong in 1922
[12]Imec is International Medical Equipment Collaborative: An international R&D and innovation hub

employing a multi-functional digital timing synchronization algorithm (for packet synchronization and data recovery).

In 2012, Ghosh *et al.* [185] proposed a modulation technique - Differential Frequency Shift Keying (DFSK) for ULP WSNs and WBANs applications based systems operating in the MICS band. This technique uses the difference of a frequency tone-pair of an RF oscillator for significantly simplifying the transmitter design complexity presented in [186]. Sjöland *et al.* [187, 188] from Lund University, Sweden, presented a 2.45 GHz ULP transceiver employing a FSK transmitter (for high efficiency and low spurious emissions) and a direct-conversion receiver (to achieve minimum power consumption) architecture for devices suitable in WSNs and WBANs.

The IEEE 802.15.6-compatible NB transceivers are detailed as follows:

In 2012, Liu *et al.* [189] from Imec and Holst Centre presented the first ULP 2.3/2.4 GHz transmitter [190] for WSNs and WBANs in compliant with four wireless standards: Bluetooth V.4 [127] and IEEE 802.15.4 (ZigBee) [129] for WSN, IEEE 802.15.6 NB [2] for WBANs and IEEE 802.15.4g [191] for smart-metering utility networks (SUNs). Later, in 2013, Liu *et al.* [192] from Imec and Eindhoven University of Technology presented a multi-standard 2.4 GHz ISM/MBAN transceiver compliant to three wireless standards: Bluetooth V.4 [127], IEEE 802.15.4 (ZigBee) [129] and IEEE 802.15.6 MBAN [2]. The transceiver employed a 2.3/2.4 GHz polar transmitter [190] and a sliding-intermediate frequency (IF) receiver architecture. Bachmann *et al.* [193] presented a multi-standard digital baseband (DBB) for transceiver design in [192]. Wong *et al.* [194] presented a WBAN transceiver chip compatible to both the IEEE 802.15.6 NB [2] and Bluetooth V.4 [127] operating in the 2.4 GHz ISM and MBAN bands. The transceiver employed a polar-loop transmitter [195] and a dual-conversion sliding-IF receiver architecture [196]. Later, *BodySense*, a system-on-chip (SoC) – compliant to 802.15.6 NB/Bluetooth V.4 was demonstrated in [197] – an extension work of [194] from Toumaz MicroSystems Ltd. Zhang *et al.* [198] presented a dual-band half-duplex transceiver compatible to both the IEEE 802.15.6 NB and IEEE 802.15.4/ZigBee operating in the 400 MHz and 2.4 GHz ISM bands. The transceiver consists of a re-configurable sliding-IF architecture deploying a 1608-1988 MHz phase-locked-loop (PLL) frequency synthesizer (covering 400 MHz and 2.4 GHz frequency bands) instead of a high-tuning range frequency synthesizer.

In 2014, Kopta *et al.* [199, 200] from EPFL and CSEM, Switzerland proposed a 2.4 GHz ISM 15.6-compliant polar transmitter, that employs: (i) an Field Bulk Acoustic Resonator (FBAR) oscil-

lator [201] for generation of a high-frequency reference signal (ii) a DBB for transformation of cartesian to polar co-rdinate using a COordinate Rotation DIgital Computer (CORDIC) algorithm for low computational complexity. In 2015, Vidojkovic *et al.* from Imec, Eindhoven University of Technology and Fujitsu Laboratories, Japan, presented a highly-reconfigurable 15.6-compliant transceiver [202] operating in both the MICS band and the 420-to-450 MHz WMTS band. It employs a PLL-based transmitter and a zero-IF receiver. The transceiver supports scalable data rates from 11kb/s to 4.5 Mb/s covering all conventional implantable applications and multi-channel EEG applications [203]. Later, Masui *et al.* presented a 15.6-NB SoC [204] – fully-compliant with MICS and 420-to-450 MHz WMTS band. Rahman *et al.* [205] from the University of Minnesota, USA, proposed a 15.6-compliant 2.4 GHz ISM and MBAN multi-band transmitter. The transmitter employs digital multiplexing of phases (for $\pi/4$-DQPSK signals) using a passive phase generation technique [206]. Later, in 2016, Rahman *et al.* [207,208] presented a 15.6-NB receiver using a frequency-translated mutual noise cancelling (FTMNC) technique based on passive coupling unlike the traditional technique [192]. A number of 15.6-compliant NB PHY baseband transceivers on FPGAs and ASICs are presented in [209–212].

Srivastava *et al.* [213] proposed a receiver front-end for FM or FSK data operating in the (401-406 MHz) MICS band for a transmitter on a body worn device. The front-end employs the principle of frequency to digital sigma delta modulation (FDSM) avoiding the need of IF amplifiers and ADC in the receiver chain. Later, Srivastava *et al.* [214,215] presented a 15.6-compliant MICS band (401-406 MHz) OOK transmitter making it suitable for both wearable healthcare devices and implantable medical devices. It employs the principle of edge-combination and injection-locking techniques for low-power RF carrier generation. Very recently, Srivastava *et al.* [216] presented a 15.6-compliant low-power integrated wireless telemetry system (Bio-WiTel) for the emerging M2M communication framework for healthcare applications. The system uses a transmitter based upon multi-phase injection locking and edge-combining techniques [217] and a low-IF FSK receiver.

2.2.3 UWB Transceivers

Application of UWB in BANs was first presented in 2003 by Zasowski *et al.* [218] while investigating the UWB channel (from 3 GHz to 6 GHz) for a BAN in an anechoic chamber and in an office room placing both the transmitter and receiver antennas directly on the body. A historical review of research on UWB for BANs is presented below:

2.2.3.1 Performance Studies of UWB Transceivers

Research groups have significant contributions in development of low-complexity UWB transceiver solutions for BANs. Fort *et al.* [219] in the year 2006 evaluated the performance of rake and selective-rake (s-rake) receivers around a human torso for better understanding of UWB performance in BANs leading to practical receiver designs. Subsequently, the IEEE 802.15.4a-2007 standard [132] – an UWB-WPAN standard – brought a paradigm shift in the field of WSNs and WBANs. Domenicali and Benedetto [220] in 2007 analyzed the behaviour of a BAN composed of at most ten 802.15.4a sensor nodes[13] and adopted the 15.4a channel model [221]. In the same year, Rousselot *et al.* [222] presented the adequateness of 15.4a based BAN by validating the 15.4a UWB PHY layer and confirmed the possibility of a larger number of simultaneous transmissions.

Viittala *et al.* [223] studied the performance of single-band DS-UWB and FM-UWB systems in two different BAN channel models. The DS-UWB system utilizes an all-rake (a-rake) receiver[14] and a partial-rake (p-rake) receiver. The FM-UWB system uses a delay-line FM demodulator followed by a PLL. The two BAN channel models are the experimental channel model [224] developed at the Centre for Wireless Communications (CWC) and the IEEE 802.15.6-2009 [4] channel model. Although both the channel models are used, the 15.6-2009 channel model [4], however, is not precise enough as the CWC channel [224] to cover a real hospital environment as presented in [225].

Niemelä *et al.* [226] presented simulation studies of UWB receivers strictly following the IEEE 802.15.4a signaling format [132] under the CWC [224] channel model. The receivers employed were a coherent receiver, a non-coherent receiver (with and without convolutional coding) and an energy-detector receiver. This work was extended in [227] to study how different surroundings inside of a hospital influence the performance of 15.4a receivers (for example, in a regular hospital room – either lying down or standing, standing in hospital corridor or lying down in a surgery room). This was followed by performance evaluation of different rake receivers (a-rake, p-rake, and s-rake receivers) [228] and an optimized energy detector receiver adopting the IEEE 802.15.4a [132] transceiver system. Simulation results show that the p-rake receiver is a practical solution and is the simplest rake receiver. A detailed performance comparison of p-rake receiver with various number of rake fingers is presented in [229] under different hospital environments.

A performance study on the different IEEE 802.15.4a signaling format based IR-UWB receivers (a-

[13]The sensor nodes follow the IEEE 802.15.4a UWB signaling format
[14]The implementation of an all-rake receiver is highly complex

rake, s-rake, p-rake, and energy detector receivers) under two different BAN channels (on-body channel for WBAN and off-body channel for WPAN) using the CWC channel model [224] is presented in [230]. Further, the performance of different 15.4a IR-UWB receivers in two UWB hospital channels, the CWC [224] and the IEEE 802.15.6 CM3 [4] channel models, are presented in [231]. These performance studies carried out in the non-mandatory mode of 15.4a standard are presented in [232]. Niemelä *et al.* also present a few suggestions on enhancements of the IEEE 802.15.4a signaling format for its better usability to UWB BANs [233]. Ekome *et al.* [234] presented the performance study of 15.6-2010 [235] signaling format based BPSK-BPPM IR-UWB receivers using an one-finger rake-receiver and a non-coherent ED receiver under the 15.6 channel model [4]. However, this modulation scheme was later abandoned by the 15.6-2012 [2] standard. For the first time, Niemelä *et al.* [236] presented an IEEE 802.15.4-2011 [133] compliant ED based receiver with OOK and PPM. The detection performance were evaluated in the CWC and the 15.6 CM3 channel models. This work was extended using the 15.6-2012 [2] standard in place of 15.4-2011 [133] standard and is presented in [237]. Further, these energy detector receivers were evaluated for monitoring Parkinson disease [238]. The MUI vulnerability to these receivers is also studied and presented in [239]. Niemelä *et al.* [240] presented performance of different IR-UWB receivers with DBPSK adopting the 15.6 transceiver system.

Dotlic and Kohno from NICT[15] presented two differential detection techniques [241], classic DPSK [242] and the proposed sample-wise DPSK (S-DPSK) using the draft of the 802.15.6-2010 IR-UWB PHY layer [235]. These techniques were employed on two receiver architectures: duty-cycled sampling receiver and chirp receiver [243] given by the same authors. An interference study of these receiver architectures is also carried out in [241, 244] under different types of interference sources: NB, FM-UWB [160], WiMax[16] [245] and other co-located 15.6-2010 IR-UWB devices. An investigation on possible receiver structures for the preamble and the SFD is carried out in [246] for the IR-UWB 15.6-2010 PHY layer. Dotlic and Miura [247] applied the same S-DPSK differential detection technique to non-coherent IR-UWB PPM receivers. Simulation results show better performance in an sample-wise detection PPM (SD-PPM) receiver[17] to that of an ED-PPM receiver[18]. The chirp pulse compression[19] technique is investigated for ED-PPM and SD-PPM receivers in [248, 249] and for S-DPSK receivers

[15]NICT: National Institute of Information and Communications Technology, Japan
[16]WiMax operate in the low-band of the UWB frequency band
[17]S-PPM receiver correlates signals of different time windows
[18]ED-PPM receiver integrates signal energies in a given time window
[19]Chirp pulse compression technique is utilized if the transmitted waveform is a linear chirp pulse. This lowers the computational complexity in the case of digital implementation

in [243]. Dotlic and Miura also analyzed the 802.15.6-2012 [2] IR-UWB transceiver architecture with and without chirp pulse compression technique [250]. The receivers employed are S-DPSK, SD-PPM and ED-PPM receivers. Simulation results show that the ED-PPM receiver has acceptable performance for BANs and is a practical non-coherent receiver over the SD-PPM receiver from the point of view of implementation. The same authors also analyzed performance of three different types of receivers architectures: coherent quadrature sampling receiver, envelope-sampling receiver and ED receiver in [251] for OOK rather than the 15.6 compliant M-ary PPM.

Rousselot and Decotignie [252] from CSEM[20] evaluated the performance of three wireless solutions for BANs: (i) the WideMac [253] protocol with an IEEE 15.4a [132] IR-UWB transceiver (ii) the wireless sensor MAC (WiseMAC) [254] protocol with a commercially available NB TI-CC1100 [255] transceiver and (iii) the WiseMAC protocol with an FM-UWB [160] transceiver. Recently, Karvonen *et al.* [256] presented a dual-radio solution for BANs employing the 15.6 IR-UWB transmitter-only radio and a wake-up receiver (WUR). The IR-UWB transmitter is deployed for data transmission from the sensor nodes to the hub; the WUR is used for receiving control messages in the sensor nodes from the hub. The generic wake-up radio based MAC (GWR-MAC) [257], a WUR-based MAC protocol used in this dual-radio is a suitable solution for WSNs and WBANs. Several solutions of WUR architectures for WBANs are presented in [258].

Saadaoui *et al.* [259] analyzed a transceiver employing Discrete Wavelet Packet Transform (DWPT) in the transmitter and Inverse Discrete Wavelet Packet Transform (IDWPT) in the receiver. This technique can be a new method for many-to-one and one-to-many communication among BAN transceivers. Liu *et al.* [260] investigated performance of a 15.6-compliant IR-UWB transceiver system employing an ED receiver (for on-off signaling) and a cross-correlation based receiver (for DBPSK modulation).

2.2.3.2 FM-UWB Transceivers

The use of FM-UWB for medical applications is investigated in a preliminary feasibility study by Gupta *et al.* [261]. Some of the reported FM-UWB transceivers for BANs are described in the following:

Gerrits *et al.* [262] presented simulation results of an FM-UWB transceiver under the 15.6-2009 CM3 and CM4 channel models [4]. Further, the same authors carried out an interference mitigation study for in-band interference (from other FM-UWB radios and WiMaX [245]) and out-of-band

[20] CSEM: Swiss Center for Electronics and Microtechnology

interference (from WLANs [263] and the 2.4 GHz ISM band). Anis *et al.* [264, 265] presented an impulse-FM-UWB transceiver employing an OOK transmitter and a super-regenerative receiver. The major advantage of this transceiver architecture is it consists of two LC self-quenched oscillators, which generate and detect the impulse-FM-UWB data pattern in the transmitting and receiving mode.

Zhou *et al.* implemented a 3.7-4.3 GHz FM-UWB transceiver [266] with digital reconfiguration of sub-carrier modulation index β_{sub}, RF bandwidth B_{RF} and RF frequency band. Zhou and Chiang [267] present an overview of the sub-modules of FM-transceivers, such as, sub-carrier generation, its calibration and generation of RF FM. The sub-carrier is generated using an relaxation oscillator with embedded frequency synthesizer [267] while in [268] using a voltage controlled triangular oscillator with a PLL is employed. Recently, Kopta *et al.* [269] present an FM-UWB receiver capable of demodulating multiple FM-UWB signals in the same frequency band. The architecture employs an "approximate zero IF" approach.

2.2.3.3 Implant UWB Transceivers

Research groups have studied the promising use of UWB in implant BANs [270] and in the field of wireless capsule endoscopy[21] for real-time imaging. The use of UWB for endoscopy is possible as per the reports of UTCOMS (COMmunication System for Nano-scale USLI[22] designed Endoscope using UWB technology) in [271].

Gao *et al.* [272, 273] from Institute of Microelectronics, Singapore, proposed a wireless telemetry system for capsule endoscopy and successfully transmitted real-time image data to an external data station. The system employs an on-off LC VCO based transmitter and a non-coherent ED based receiver. An ex-vivo experiment with thick meat was performed for validation of the prototype endoscopy system. Santiago *et al.* [274] presented a transceiver architecture for capsule endoscopy integrating in-body transmitter and on-body receiver. The receiver employs a single-branch correlator with a pre-defined template pulse and supports transmission of uncompressed Video Graphics Array (VGA) video. This architecture was extended in [275] by adding cognitive radio features. The cognitive radio controller consists of two transceivers: (i) a 15.6-compliant IR-UWB transceiver and (ii) an MB-OFDM transceiver as per the ECMA-368 interface [131].

To the best of our knowledge, Santiago *et al.* [276] performed a living-body in-vivo experiment

[21] A capsule endoscope is a camera with the size and shape of a pill used for the visualization of the gastrointestinal tract and record images through the digestive tract for subsequent diagnosis and detection of gastrointestinal diseases

[22] ULSI stands for Ultra Large Scale Integration

(in the porcupine chirurgical model) for the first time using an MB-OFDM based transceiver. Later, Anzai *et al.* [277] performed the same in-vivo experimental evaluations using the IR-UWB transceiver with M-ary PPM scheme based transmitter and correlation detection based receiver. This work was extended as an optimized in-body to out-of-body IR-UWB transceiver [278] employing an M-ary PPM based transmitter and an FPGA implemented ED receiver. The ED receiver is preferred over correlation based receiver as there is no need for generation of the carrier and the template signal in an ED receiver. Performance evaluation of the transceiver was carried out using a biological-equivalent liquid phantom experiment. Based on these studies, it was surmised that IR-UWB with ED receiver is preferable over MB-OFDM with ED receiver for implementation of implantable BANs.

2.2.3.4 IR-UWB Transceivers

Ryckaert *et al.* from Imec in the year 2005 presented a PPM IR-UWB transmitter [279] that employs a triangular pulse generator and a ring oscillator (to generate a carrier signal for up-conversion) that are activated simultaneously for low-power consumption. Takizawa *et al.* [280] presented a vital-sign (EEG or ECG) monitoring system employing the 15.4a [132] signaling format. Simic *et al.* [281] presented a 15.4a IR-UWB BAN system employing simple pulse generator (for generation of bipolar pulses) in the transmitter and non-coherent energy-detection (ED) principle in the receiver. Later, Keong and Yuce [282] implemented a single-channel real-time ECG monitoring system employing non-coherent ED based receiver and aligned with rough draft of the IEEE 802.15.6-2008 [283] standard. Reddy and Ganapathy [284] presented the performance of multi-user detection (MUD) based receivers [285] over conventional rake receivers[23] adopting the 15.4a channel model [221]. Thiasiriphet and Lindner [286] presented a comb filter[24] based ED receiver that improves narrow-band interference (NBI). Helleputte and Gielen [287] presented an ULP complex analog correlating receiver architecture for WSNs and WBANs as power consumption is the main criterion.

Nakagawa *et al.* [288] implemented an IR-UWB transceiver that utilizes pulse pattern generator (PPG) in the transmitter and low-sampling frequency ADCs in the receiver. Zhao and Kwak [289] presented a novel PPM UWB transceiver employing Miller encoding of data [290] before PPM in the transmitter and a non-coherent detection in the receiver. Chae *et al.* [291] and Yuce *et al.* [292] presented UWB transceivers supporting 128-channel neural recording system and 8-channel EEG/ECG

[23] Rake receivers do not cancel multi-user interference
[24] An analog delay feedback loop with unity gain

system respectively. Kim *et al.* [293, 294] from Kwangwoon University, Seoul, analyzed and implemented a direct-sequence UWB (DS-UWB) system for BANs employing binary zero-correlation duration (ZCD) code [295] and pseudo-noise (PN) sequence as spreading codes. Simulation results showed that the system using a binary ZCD code is robust for multiple-access interference (MAI) and multipath fading environments.

Dokania *et al.* [296] presented a non-coherent OOK/BPSK transceiver employing an H-bridge based transmitter based on Wang *et al.* [297] and a non-coherent peak polarity detector based receiver. The architecture uses a pseudo-coherent self-correlated signature generation and a detection mechanism for classification of data or timing pulses.

Kim *et al.* [298] proposed a non-coherent ED based synchronization technique adopting the draft of IEEE 802.15.6-2010 [235] standard. Takei *et al.* [299] presented a hardware prototype of IR-UWB body sensor node with DBPSK modulation and MAC specifications of the 15.6-2010 [235] standard. The performance of this prototype was evualated with a single sensor node and a single hub. This work was extended in [300] with multiple sensor nodes communicating simultaneously to a single hub. A prototype of an IR-UWB body sensor node using off-the-shelf components is presented in [301, 302]. Thotahewa *et al.* [303] presented a dual-band IR-UWB sensor node using UWB for data transmission and NB for data reception. It overcomes the barrier of increased complexity in the UWB receiver since UWB receivers require complex hardware and consume comparatively higher power. Another dual-band sensor node is presented in [304] using UWB link for data transmission and a 433-MHz ISM band link for data reception. A similar dual-band sensor node is presented in [305] with interoperability of single-carrier UWB (SC-UWB) [306] and IEEE 15.4 ZigBee [129] for data transmission and reception.

Li and Hamaguchi [307] presented a prototype BAN built on high-band UWB (from 7.25 GHz to 10.25 GHz) adopting the 15.6-2010 draft [235]. Thotahewa *et al.* [308] presented an IR-UWB body sensor node that was a combination of IR-UWB receiver front-end and a FPGA-based controller (for synchronization and MAC communications). Chen *et al.* [309] implemented a 7.75-8.25 GHz chirp-UWB transceiver employing a digital-gradient generator (DGG) and a digitally controlled oscillator in the transmitter and an FSK demodulator (with wideband LNA and dual band-pass filters) in the receiver unlike that in conventional regenerative FSK receivers.

Im and Kim presented a non-coherent IR-UWB receiver [310] for QoS-sensitive BANs employing a code-multiplexed transmitted reference (CD-TR) receiver instead of the conventional TR receiver.

Performance was evaluated using the IEEE 802.15.6-2009 [4] channel model. The advantage of a CD-TR receiver over a conventional TR receiver is that there is no time-delay between the reference pulse and the data pulse. The improvement in QoS for UWB-BANs is shown by Yong *et al.* [311] using rake-receivers with maximum-ratio combining (MRC) schemes under the 15.6 channel model. Gao *et al.* [312] implemented an NBI robust IR-UWB transceiver SoC employing a LC-VCO based transmitter, a non-coherent ED receiver and a DBB architecture[25] presented by Toh *et al.* [313]. Vigraham and Kinget presented an NBI robust IR-UWB transceiver SoC in [314]. The authors present two different receiver architectures: an automatic threshold recovery demodulator based OOK receiver [315] and a CDR-based self-duty-cycled and synchronized receiver [316]. Another 3-5 GHz RF transceiver SoC is implemented in [317] robust to 2.4 GHz ISM NBI. The transceiver utilizes a digitally synthesized impulse generator in the transmitter and an non-coherent OOK ED receiver presented by Ha *et al.* [318]. Single and multiple NBI mitigation techniques by the use of pulse shaping for UWB BANs are presented by Rout and Das [319, 320].

Vauche *et al.* [321] implemented a 3.1-4.9 GHz transceiver using an edge combiner [322] (consisting of a pulse synthesizer and a delay-based BPSK modulator) in the transmitter and a non-coherent peak-voltage detector in the receiver. Ouvry *et al.* [323] presented a 15.6-2012 compliant hybrid transceiver "RUBYLB" chip employing a smart combination of a coherent quadrature receiver [324] and a non-coherent ED based receiver [325]. The coherent part of the receiver is used for data demodulation and the non-coherent part is for synchronization. Chougrani *et al.* presented the DBB architecture for this dual receivers in [326]. The authors have also presented a 15.6- synchronization technique [327] and its hardware implementation [328]. Recently, Manchi *et al.* [329] and Bondok *et al.* [330] have presented digital baseband architectures for 15.6 IR-UWB transceivers. A coexistence study of 15.6 IR-UWB receiver in presence of the 802.15.4a [133], the 802.15.4f [331] and FM-UWB interferers is presented by Hernandez and Miura [332]. Wang *et al.* [333] presented a 7-9.8 GHz IR-UWB transceiver compliant to both the 15.4a [132] and 15.6-2012 [2] standard. The transceiver employs a ring-oscillator based transmitter and duty-cycled receiver controlled by a DBB developed on a FPGA. Dehaese *et al.* [334] also presented a high band 7.2-8.5 GHz IR-UWB receiver covering both the 15.4a and 15.6 standards. This receiver employs a self-cycled and self-synchronized non-coherent ED based architecture.

Extensive research has been carried out by industry and academia and a number of research publications have been reported in the area of transceiver design for BANs. IR-UWB transceivers

[25]This architecture employs a D flip-flop based pulse detection algorithm

are emerging as an excellent option for on-body, off-body and implantable BAN systems due to its low-complexity, low-power consumption and low transmission power. The efficient design of an IR-UWB transceiver (the transmitter and the receiver) depends on its architecture and circuit topology. The design of an efficient, miniaturized, low power IR-UWB transceiver chip for all conceivable BAN applications is still a key and active research area. The improvements in the transmitter and the receiver in terms of advances at individual block-level will certainly give some benefits; however, in order to exploit the full advantage from system-level perspective, one has to make improvements at the architectural level.

This research work emphasizes the design of a low-complexity IR-UWB transceiver system for BANs – strictly fulfilling the IEEE 802.15.6-2012 [2] specifications and without violating the FCC rules and regulations [3]. This thesis attempts to devise an implementation architecture that enables the design of an energy-efficient and low-complexity 15.6 IR-UWB transceiver system for BANs.

2.3 Conclusions

In this chapter, a brief introduction to Wireless Body Area Network Standard - the IEEE 802.15.6 is presented with special reference to the IR-UWB PHY structure vis-à-vis the transmission bands (the mandatory and the optional bands), the data-rates, modulation schemes, the signaling pulse-shapes and the Quality-of-Service (Default-mode/High QoS mode). This is followed by an extensive literature-review of transceivers for BANs (for BCC/HBC PHY, NB PHY, IR-UWB and FM-UWB PHY) reported in literature and the key issues in WBAN transceiver design, namely, the cost, power consumption, size and complexity.

3

IR-UWB Transmitter using SRRC signaling pulse

Contents

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3.1 Introduction

This chapter presents the design and implementation of an IR-UWB transmitter operating in the mandatory physical channel of the low-band of the UWB frequency band, i.e., Ch.#1. The IR-UWB transmitter is applicable for the default mode of operation (see the mandatory procedure presented in Table 2.7). This transmitter design is specified for on-off signaling (binary signaling or 16-ary signaling) at the mandatory data rate of 0.4875 Mbps. The on-off signaling scheme and the data rate are the mandatory specifications. The transmitter uses an SRRC pulse as the signaling waveform p(t). A novel method for generation of the SRRC pulse by an N-segment piece-wise linear approximation (PWLA) approach is presented. The baseband SRRC pulse is up-converted by a double-balanced mixer, filtered by a simple first-order low-pass filter (LPF) to suppress the harmonics followed by coupling to an antenna via a balun transformer.

To the best of our knowledge, a few raised cosine (RC) pulse generators [335, 336] are reported in literature. The pulse generator employed in [335] generates a RC envelope directly using multiple pattern generators, delay-locked loop (DLL) and edge combiners (EDCOM). The pattern generator generate triangles of certain amplitudes when the delay signals from DLL trigger. The amplitude of each triangle is the sampling point of a raised cosine pulse at regular intervals of 1/(2×4 GHz). The design avoids the use of external filter or on-chip passive filters, but the disadvantage of this method is increase in hardware and high power consumption. The root-raised cosine (RRC) pulse generator in [336] employs oscillators, on-off switches and RRC filters and consumes high power. The pulse generators in [335, 336] are compliant to the FCC spectral mask [3] with a bandwidth of 1.4 GHz; however they do not comply with the 15.6 transmit spectral mask [2] of a bandwidth 500 MHz and hence is unsuitable for use in IR-UWB transmitter for BANs. This work presents a pulse generation method to generate a SRRC pulse compliant to IEEE 802.15.6 [2] IR-UWB transmitter for BANs with reduced hardware complexity.

The organization of the chapter is as follows. Section 3.2 illustrates the PWLA approach and describes the methodology for generation of an arbitrary signaling waveform. Using this approach, Section 3.3 describes three different approximations to the 15.6-compliant SRRC pulse defined in (2.1). Section 3.4 compares their performance in terms of percentage relative error, cross-correlation, power-spectral density and implementation complexity. Section 3.5 describes the implementation of the proposed 15.6 IR-UWB time-hopping PPM (TH-PPM) transmitter using a six-segment PWLA

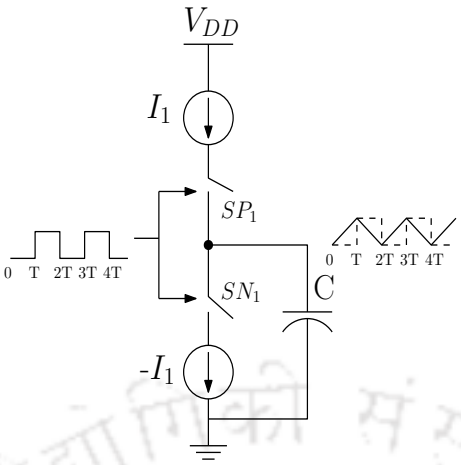


Figure 3.1: Charging and discharging a capacitor to generate a triangular waveform

SRRC pulse generator. Section 3.6 provides results and discussions followed by conclusions in Section 3.7.

3.2 Generation of Arbitrary Signaling Waveform using PWLA Approach

An arbitrary signaling waveform can be generated by PWLA of the given waveform followed by realization of each line segment as a voltage waveform. Each voltage waveform is realized by charging or discharging a capacitor by an appropriate current source. Assuming that the duration of each segment is a multiple of some basic time period T in order to facilitate a simple clock driven controller, let us consider an example for illustration as shown in Fig. 3.1. The capacitor C generates the line segments with positive slopes and negative slopes by alternately switching a positive and a negative current sources, I_1 and -I_1 respectively, for 'T' time duration. The switching of the capacitor from one current source to the other (equivalently, from one line-segment to another) is accomplished by switches SP_1 and SN_1 controlled by a digital signal.

The general block diagram of an N-segment (N= m+n)-segment PWLA waveform generator is illustrated in Fig. 3.2. It consists of m-positive and n-negative current sources digitally controlled by (N= m+n) control signals, namely, sig_1, sig_2, ..., sig_{m+n-2}, sig_{m+n-1} and $sig_{m+n=N}$. The breakpoint of each line-segment for the generation of N- PWLA segments is realized by switching the N-current sources from one state to the next.

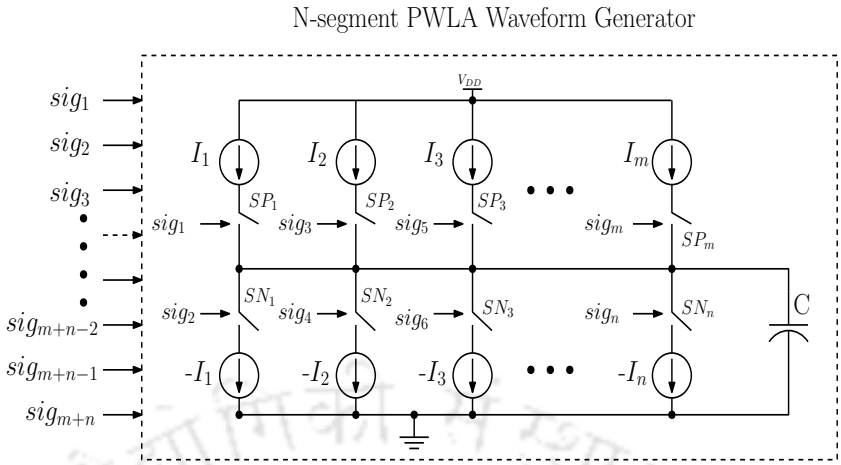


Figure 3.2: (N= m+n) - segment PWLA Waveform Generator with m-positive and n-negative current sources

3.3 Different Approximations of N-segment PWLA SRRC Pulse Generation

The SRRC pulse given by (2.6) is not a physically realizable waveform - it can only be approximated. The proposed PWLA approach is a practical approach for "generation" of SRRC pulse waveform to any desired degree of accuracy (subject to complexity and cost). The N-segment PWLA pulse waveform is realized following the N-segment PWLA waveform generator illustrated in Fig. 3.2. Different PWLA approximations[1] of the SRRC pulse are considered taking the time duration of each line segment to be a multiple of some basic time duration T (T= $1/f_{clk}$, where f_{clk} is the clock frequency). Next, the PWLA waveforms are realized by switching the current sources by the control signals sig_1, sig_2, ..., sig_{m+n-2}, sig_{m+n-1} and sig_{m+n} generated by a clock-driven digital controller. The various PWLA waveforms are next considered.

3.3.1 Four-segment PWLA SRRC Pulse

The four-segment PWLA SRRC pulse approximating the actual SRRC pulse is shown in Fig. 3.3(a). This can be generated by using a positive current source I_1 and a negative current source -I_1 controlled by signals sig_1 and sig_2 as illustrated in Fig. 3.3(b).

[1]Note: In this thesis, the acronym "PWLA" is used interchangeably to represent either "Piecewise Linear Approximation" or "Piecewise Linear Approximated".

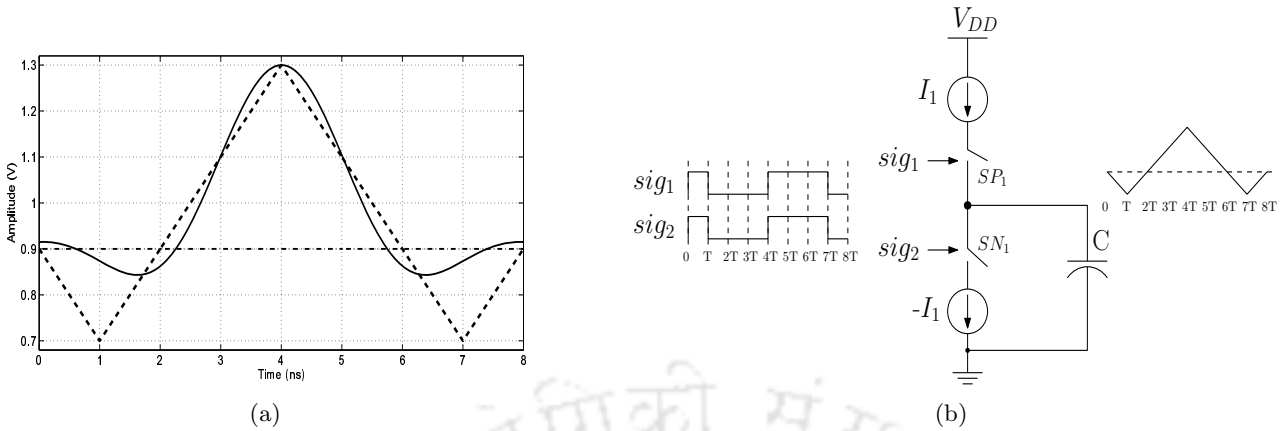


Figure 3.3: (a) Four-segment PWLA SRRC pulse approximating SRRC pulse (b) Four-segment PWLA SRRC Pulse Generator

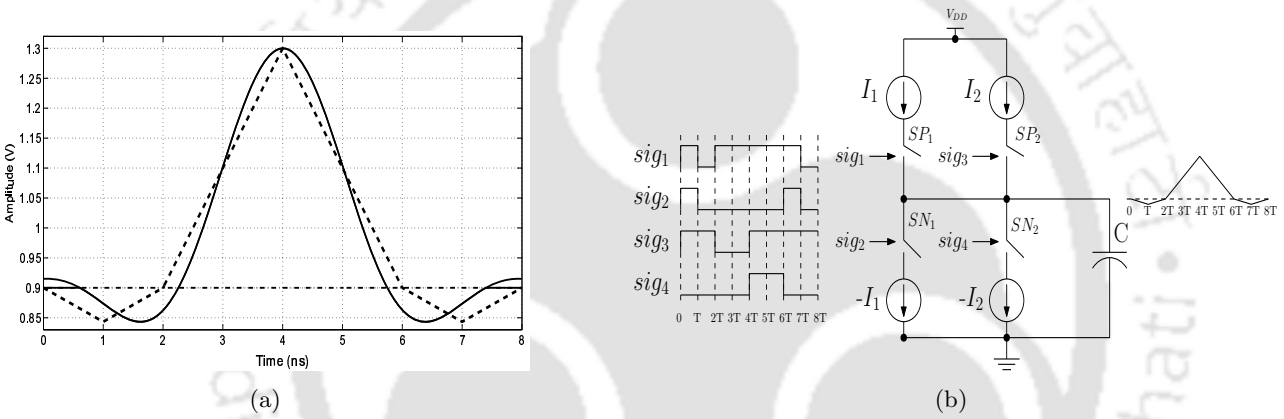


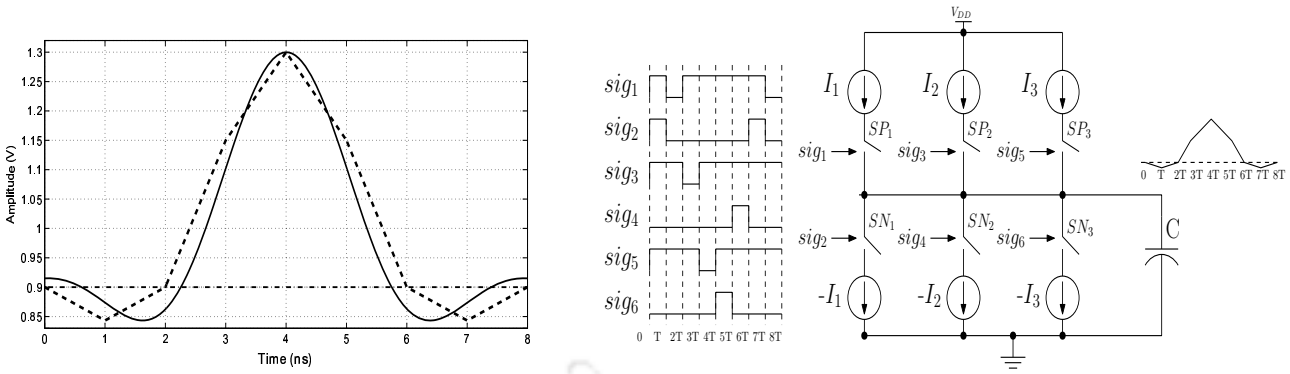
Figure 3.4: (a) Six-segment PWLA SRRC pulse approximating SRRC pulse (b) Six-segment PWLA SRRC Pulse Generator

3.3.2 Six-segment PWLA SRRC Pulse

A six-segment PWLA SRRC pulse is shown in Fig. 3.4(a). The six-segments are generated by switching two positive current sources I_1, I_2 and two negative current sources -I_1, -I_2 activated by the control signals sig_1, sig_2, sig_3 and sig_4 as illustrated in Fig. 3.4(b).

3.3.3 Eight-segment PWLA SRRC Pulse

An eight-segment PWLA SRRC pulse is shown in Fig. 3.5(a). This PWLA SRRC pulse can be generated using three positive current sources I_1, I_2, I_3 and three negative current sources -I_1, -I_2 and -I_3 that are switched into the charge/discharge of the capacitor at appropriate instants (Fig. 3.5(b)).



(a) (b)

Figure 3.5: (a) Eight-segment PWLA SRRC pulse approximating SRRC pulse (b) Eight-segment PWLA SRRC Pulse Generator

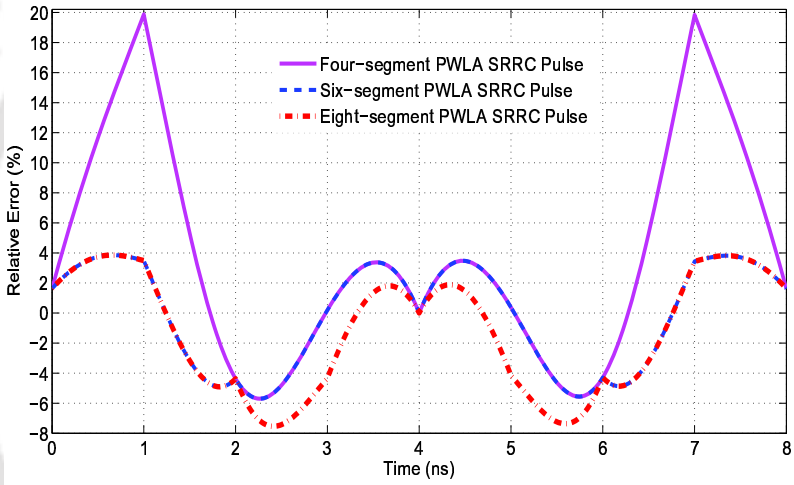


Figure 3.6: The percentage relative error of four-, six- and eight-segment PWLA SRRC pulse

3.4 Evaluation of the "best" PWLA SRRC pulse generation

The efficacy of various approximations can be evaluated in terms of percentage relative error, cross-correlation, the number of current sources and power spectral density (PSD):

3.4.1 Percentage Relative Error

The relative error gives the detailed description of discrepancy between the SRRC pulse and the PWLA SRRC pulse. The percentage relative error of different approximations of N-segment PWLA SRRC pulse with respect to the SRRC pulse is shown in Fig. 3.6. The four-segment PWLA SRRC pulse shows the worst relative error among the three PWLA SRRC approximations with a maximum relative error of 20%. The relative error of a six-segment PWLA SRRC pulse is in the range of +4%

Table 3.1: Normalized Cross-correlation of four-, six- and eight-segment PWLA SRRC Pulse

Different PWLA Approximations	Normalized Cross-correlation
Four-segment	0.887
Six-segment	0.927
Eight-segment	0.971

Table 3.2: No. of current sources required for four-, six- and eight-segment PWLA SRRC Pulse

Different PWLA Approximations	No. of Current Sources	
	Positive	Negative
Four-segment	1	1
Six-segment	2	2
Eight-segment	3	3

to -6% while that of an eight-segment approximation is in the range of +4% to -8%. The six-segment PWLA SRRC pulse shows the lowest relative error.

3.4.2 Cross-correlation

Table 3.1 shows the normalized cross-correlation of four-, six- and eight-segment PWLA approximations with SRRC pulse.

3.4.3 No. of Current Sources

Table 3.2 shows the number of current sources required for the generation of four-, six- and eight-segment PWLA approximations.

3.4.4 PSD

The normalized PSDs of four-, six- and eight-segment approximations with respect to the WBAN transmit spectral mask are shown in Fig. 3.7. It is clear that the PSD of the four-segment approximation violates the WBAN spectral mask while the PSDs of six- and eight-segment approximations meet the spectral mask. Further, it is clearly seen from Fig. 3.7 that even by increasing the number of PWLA segments from six to eight, the PSD is more or less invariant in the main lobe and is well within the mask in the side lobes.

Thus, it may be concluded that a six-segment approximation is the best choice in terms of performance and implementation complexity.

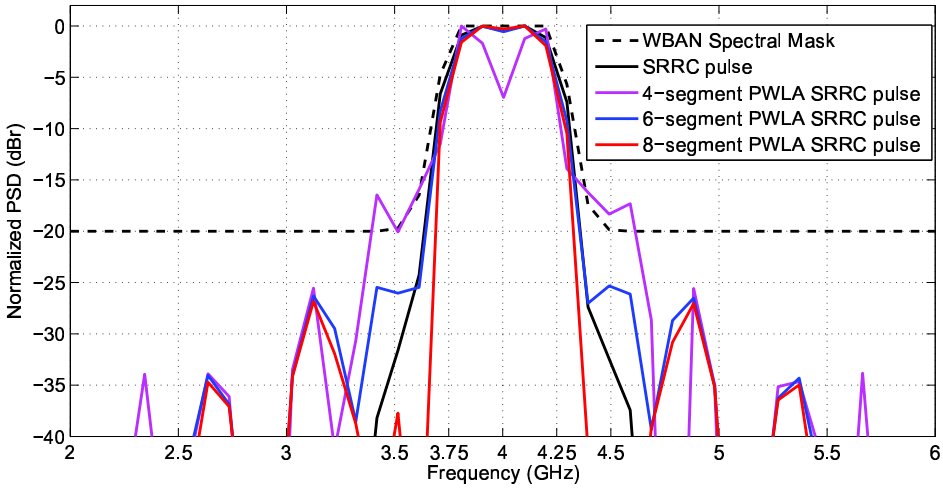


Figure 3.7: PSDs of four-, six- and eight-segment PWLA SRRC pulse

3.5 Proposed IR-UWB Time Hopping PPM (TH-PPM) Transmitter

The biological signals obtained by bio-sensors in wireless sensor nodes are conditioned and digitized. The digitized version of the signal are the information bits and serves as the input to the TH-PPM transmitter. The information bit are coded into 2-bit codeword for binary PPM and 8-bit codeword for 16-ary PPM. Each bit of the codeword is encoded in terms of position of a pulse p(t) of duration T_w (T_w= 64 ns) among $N_w/2$ (N_w= 32) positions within half of the symbol duration T_{sym}. The additional ($N_w/2$ - 1) waveform positions are used for time-hopping and to support multiple-BAN nodes for co-existence.

The architecture of the proposed IR-UWB TH-PPM transmitter is shown in Fig. 3.8. It consists of three blocks: Pulse Position Controller (PPC), six-segment PWLA SRRC pulse generator and up-conversion circuitry. The SRRC pulse generator contains two sub-blocks: controller and PWLA pulse generator. The inputs to the transmitter "CODEWORD" (1 or 0) and "PULSE POSITION" $\{h_3, h_2, h_1, h_0\}$ - specified by the "time-hopping sequence" come from the baseband processor which is not considered here. The transmitter is triggered by the signal "CODEWORD". When CODEWORD= 1, a pulse is transmitted and when CODEWORD= 0, no pulse is transmitted. A SRRC pulse is generated when bb_{trig}= 1 and is followed by up-conversion to the carrier frequency (f_c) at 4 GHz for transmission.

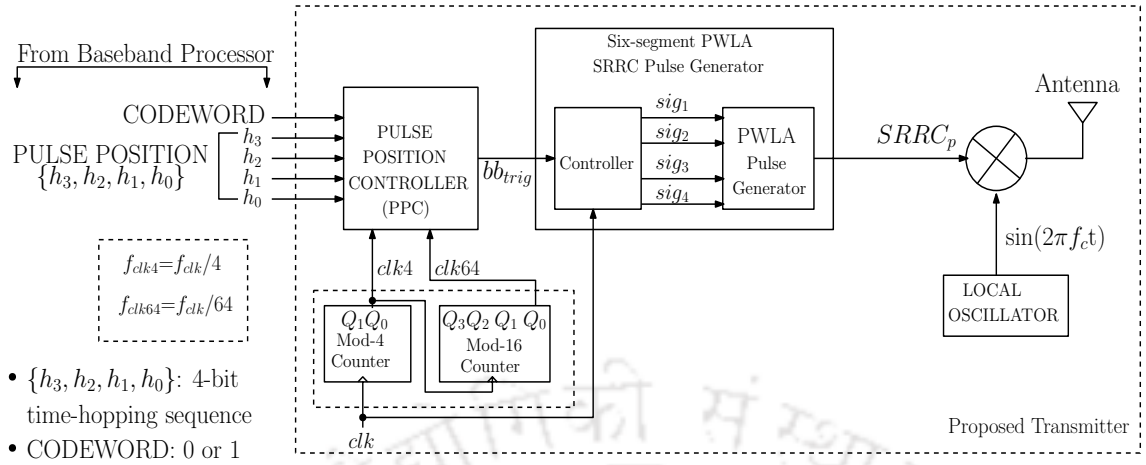


Figure 3.8: Block Diagram of the proposed IR-UWB TH-PPM transmitter

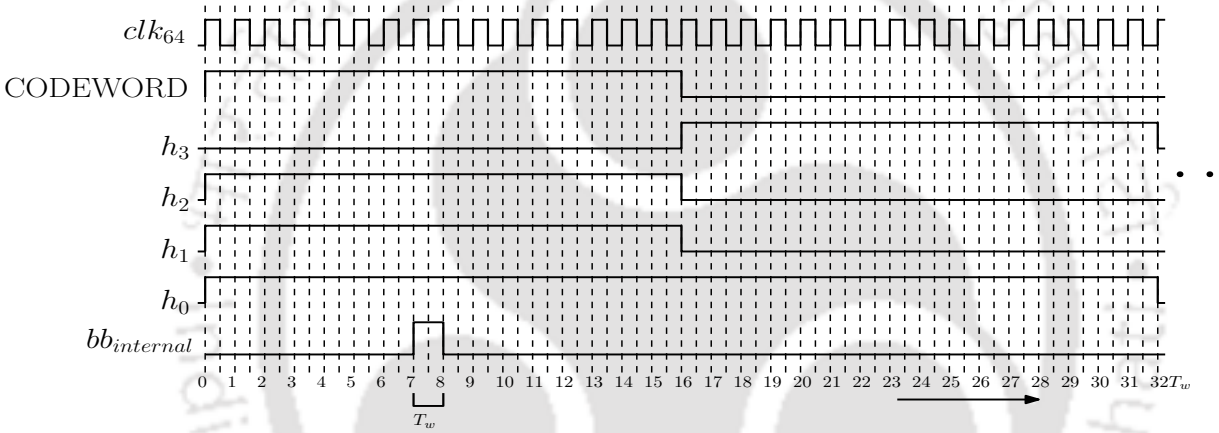


Figure 3.9: Timing Chart of the proposed PPC

3.5.1 PPC

The PPC generates the signal bb_{trig} to activate the pulse generator. The position of the pulse is at one of the sixteen positions defined by PULSE POSITION $\{h_3, h_2, h_1, h_0\}$ when CODEWORD is high (indicated by $bb_{internal}$ as shown in Fig. 3.9). For example, when CODEWORD is '1' and $\{h_3, h_2, h_1, h_0\}$ is '0111', the signal "$bb_{internal}$" is high at the eighth position for a duration of T_w (from $7T_w$ to $8T_w$ as shown in Fig. 3.9).

The advantage of the proposed PPC is that, the SRRC pulse generator is active only for a duration $T_w/8$ (bb_{trig}= 1) instead of the total allocated duration of T_w ($bb_{internal}$= 1). This procedure ensures that the peak of the SRRC pulse is placed exactly at the middle of the duration T_w (Fig. 3.10).

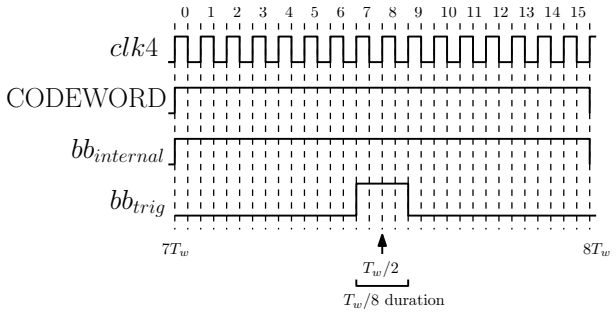


Figure 3.10: bb_{trigg} when CODEWORD is '1'

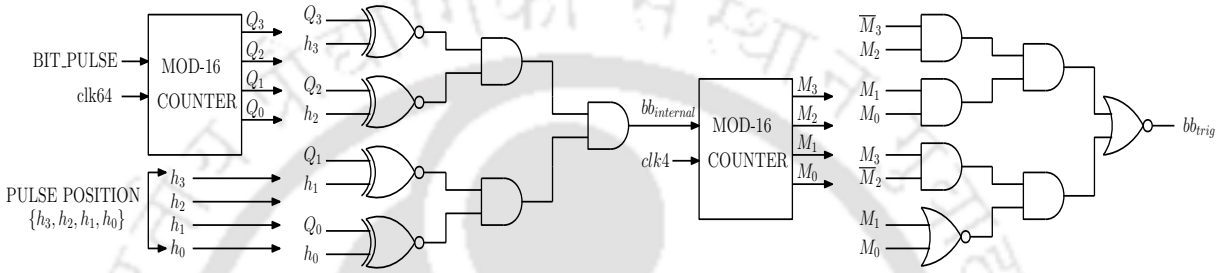


Figure 3.11: Circuit diagram of the proposed PPC

Fig. 3.11 shows the proposed PPC that implements the following logic:

$$bb_{internal} = (Q_3 \odot h_3)(Q_2 \odot h_2)(Q_1 \odot h_1)(Q_0 \odot h_0)$$

$$bb_{trig} = \overline{M}_3 M_2 M_1 M_0 + M_3 \overline{M}_2 (\overline{M_1 + M_0})$$

3.5.2 Six-segment PWLA SRRC pulse generator

The pulse generator produces the PWLA pulse only when bb_{trig} is high (Fig. 3.12). The different segments are generated by switching on/off the appropriate current sources through the signals sig_1, sig_2, sig_3 and sig_4 (Fig. 3.12). The controller and the PWLA pulse generator are explained below.

3.5.2.1 Controller

Fig. 3.13 shows the circuit diagram of the controller for generation of the pulse $SRRC_p$ of duration '8T' (as per Fig. 3.12). The outputs sig_1, sig_2, sig_3 and sig_4 are the inputs to the PWLA pulse generator.

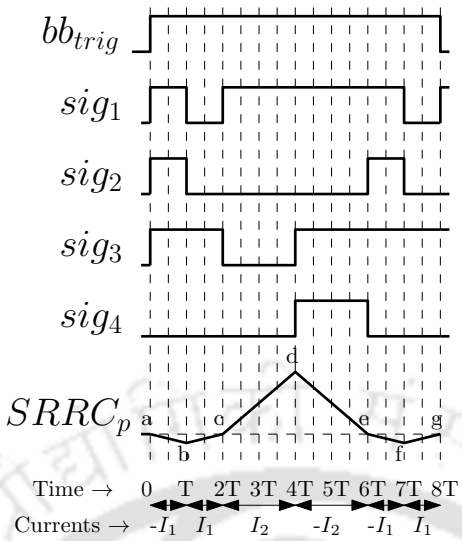


Figure 3.12: Timing diagram of six-segment PWLA SRRC pulse generator

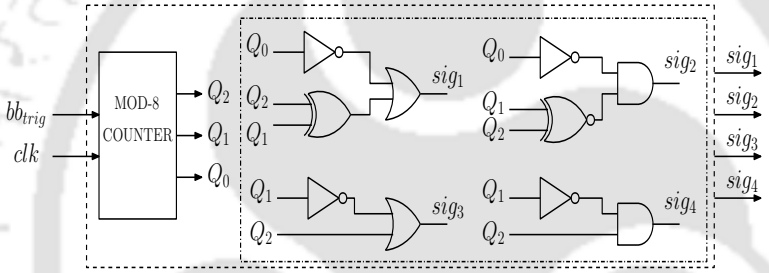


Figure 3.13: Circuit diagram of controller

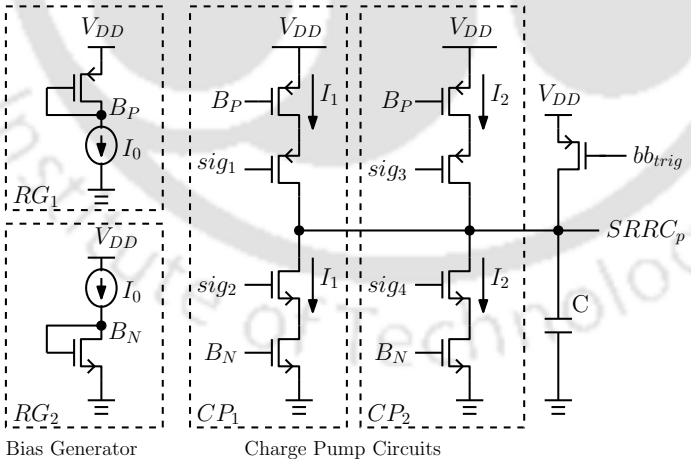


Figure 3.14: Circuit diagram of PWLA Pulse Generator

3.5.2.2 PWLA pulse generator

Fig. 3.14 shows the proposed PWLA pulse generator. The pulse generator consists of two charge pumps CP_1 and CP_2 for the current flows I_1 and I_2 to the capacitive load 'C'. The current source

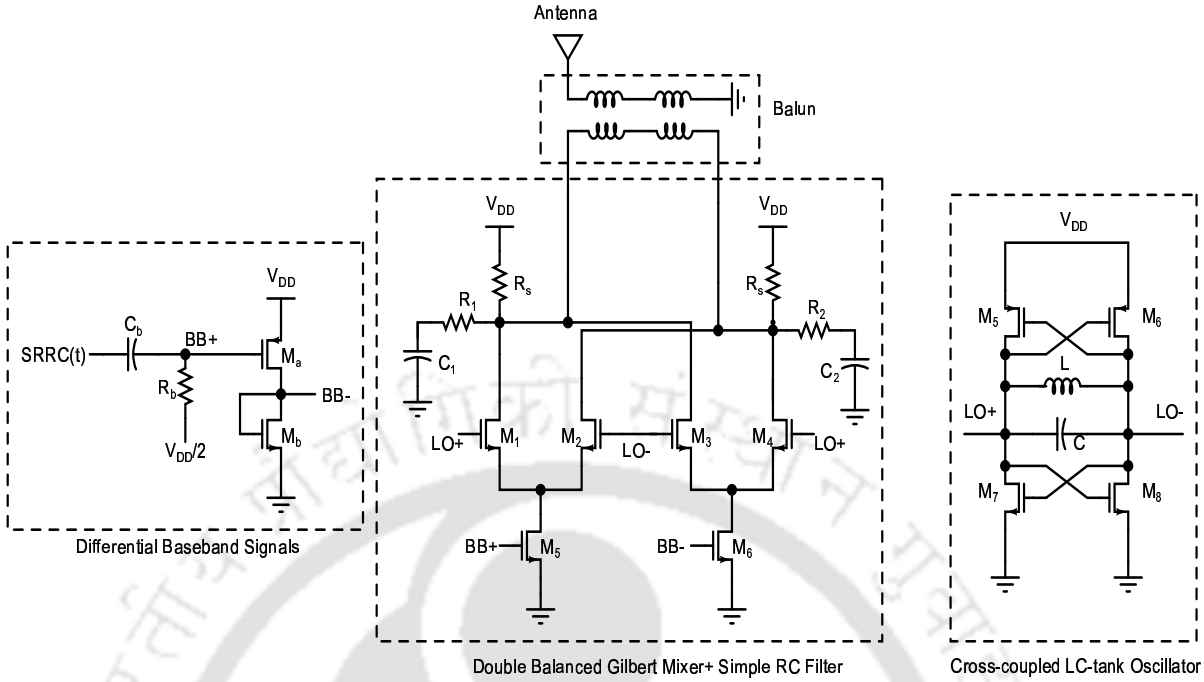
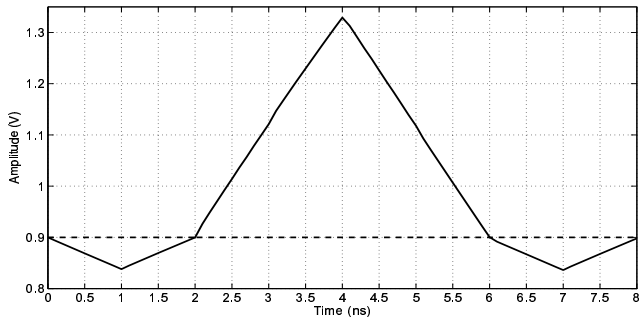


Figure 3.15: Up-conversion circuitry using double-balanced Gilbert Mixer

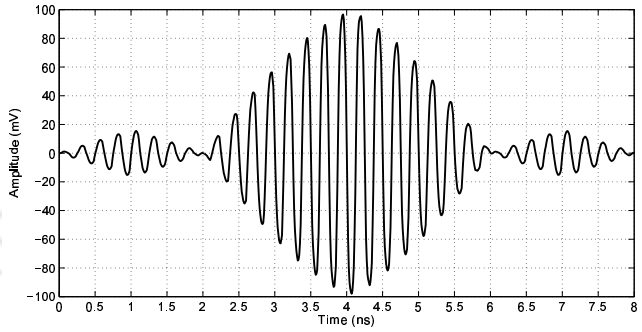
I_0 acts as the basic reference current source mirroring the currents I_1 and I_2. The current I_1 flows from the load to the first charge pump CP_1 when sig_2 is high (this generates the segments 'a-b' or 'e-f') as shown in Fig. 3.12. The same current I_1 flows from the charge pump to load when sig_1 is low (this generates the segments 'b-c' or 'f-g'). Similarly, the current I_2 flows through the second charge pump CP_2 to the load when sig_3 is low from 2T to 4T (this generates the segment 'c-d') and the same current I_2 flows from load to charge pump when sig_4 is high from 4T to 6T for the segment 'd-e'.

3.5.3 Up-conversion Circuitry

The single-ended baseband pulse SRRC(t) is next converted to differential baseband signals BB+ and BB- as shown in Fig. 3.15. The differential baseband signal (across BB+ and BB-) is up-converted by multiplying with a differential sinusoidal carrier at 4 GHz (across LO+ and LO-) that is generated by a cross-coupled LC-tank oscillator [337] shown in Fig. 3.15. The multiplier is designed with a double-balanced Gilbert Mixer [338]. The major advantage of double-balanced Gilbert mixer is that it provides good isolation between LO and RF ports and leads to reduced LO leakage to RF ports. The differential RF output of the Gilbert mixer is filtered by a simple RC filter with -3 dB cut-off frequency at 4.5 GHz and fed to a balun for differential to single-ended conversion. The up-converted SRRC waveform is finally fed to the antenna for transmission.



(a)



(b)

Figure 3.16: Simulated waveforms of (a) the six-segment baseband PWLA SRRC pulse "SRRC(t)" and (b) the corresponding up-converted RF pulse using double balanced Gilbert Mixer

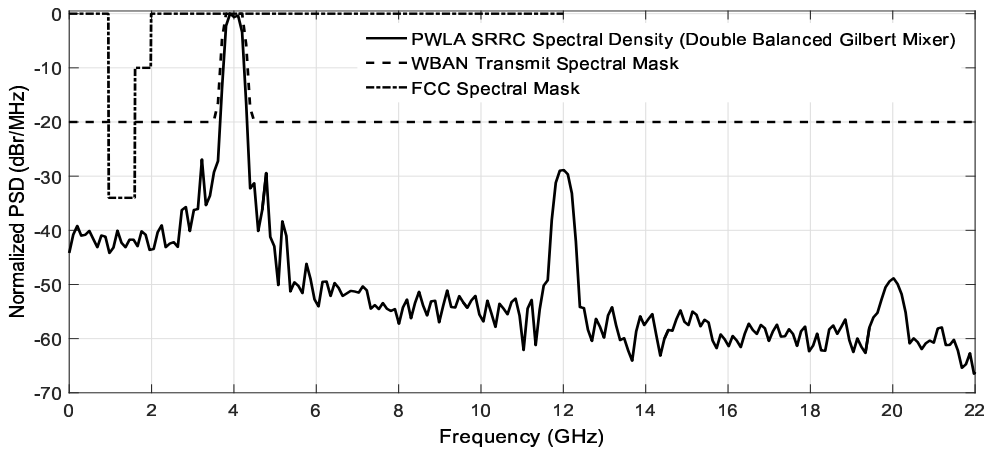


Figure 3.17: Normalized Spectral Density of the proposed six-segment PWLA SRRC pulse generator conforming to the FCC transmit spectral mask [3] and the 15.6 transmit spectral mask [2]

Fig. 3.16(a) shows the baseband PWLA SRRC pulse and Fig. 3.16(b) shows the corresponding up-converted RF pulse using double-balanced Gilbert Mixer. Fig. 3.17 shows the normalized power spectral density of the up-converted PWLA SRRC pulse satisfying both the FCC transmit spectral mask [3] and the 15.6 transmit spectral mask [2].

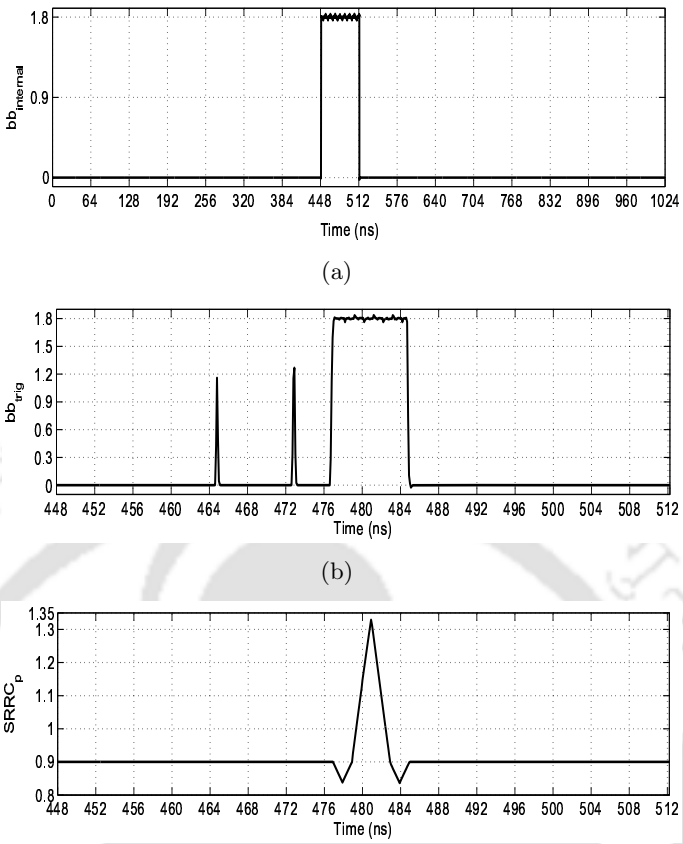


Figure 3.18: Simulated waveforms of (a) $bb_{internal}$ (b) bb_{trig} and (c) $SRRC_p$

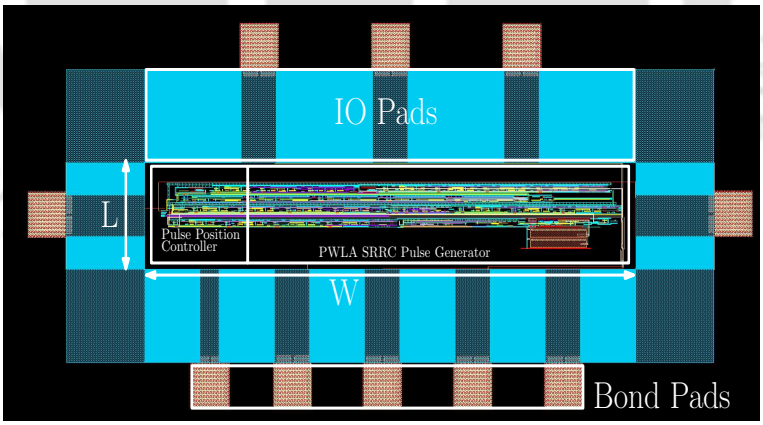


Figure 3.19: Layout of the proposed IR-UWB TH-PPM transmitter (excluding the up-conversion circuitry) having an active area of $W \times L$= 826 $\mu m \times 100\ \mu m$

3.6 Results and Discussions

In order to validate the proposed transmitter design for BANs, simulations are carried out using standard foundry MOSFET models in 180 nm CMOS technology. Fig. 3.18(a) and Fig. 3.18(b) show

Table 3.3: State-of-the-Art of carrier-modulated IR-UWB transmitter in 180-nm CMOS Technology

Parameters	Norimatsu *et al.* [335]	This Work
Pulse Type	RC	SRRC
Pulse Duration, T_p	1.75 ns	8 ns
Pulse Repetition Frequency, PRF	36 MHz	0.488 MHz
Power Consumption, PC	29.7 mW*	9.48 mW†
Supply Voltage	2.2 V	1.8 V
Pulse Bandwidth	1.4 GHz	500 MHz
Modulation	DBPSK	TH-PPM
Chip Area	0.4 mm^2	0.086 mm^2

∗: Power Consumption of power amplifier = 16 mW;
†: Power Consumption of Up-conversion circuitry using Double Balanced Gilbert Mixer= 8 mW.

the output of the PPC when CODEWORD is '1' and PULSE POSITION $\{h_3, h_2, h_1, h_0\}$= {0,1,1,1}. Fig. 3.18(c) shows the pulse generated by the six-segment PWLA SRRC pulse generator.

The layout of the proposed transmitter (excluding the up-conversion circuitry) is shown in Fig. 3.19 with an active chip area of 826 $\mu m \times 100\ \mu m$. It is very difficult to directly have a fair comparison of the proposed carrier-modulated transmitter with SRRC signaling pulse and the state-of-the-art RC signaling pulse based UWB transmitter in [335]. The UWB transmitter in [335] follows the DBPSK modulation and is intended for an 1.4 GHz bandwidth carrier-modulated IR-UWB applications at a carrier frequency of 4.1 GHz. Table 3.3 reports the results of the proposed SRRC TH-PPM transmitter and the RC DBPSK transmitter presented in [335] which is not intended for WBAN applications.

3.7 Conclusions

A novel IEEE 802.15.6 IR-UWB TH-PPM transmitter featuring a six-segment piece-wise linear approximation (PWLA) based SRRC pulse generator is designed and implemented in 180 nm CMOS technology. The transmitter operates at the mandatory data rate of 0.4875 Mbps and employs a pulse position controller (PPC) to place the Square Root Raised Cosine (SRRC) pulse in a time-hopping pulse position modulation (TH-PPM) scheme. It is found from simulation results that the generated PWLA SRRC pulse is fully compliant with the 15.6 transmit spectral mask. The proposed PWLA approach has the potential to approximate an arbitrary signaling waveform with a high degree of accuracy and hence should be useful in transceiver realizations.

4

IR-UWB Non-coherent Energy Detection based Receiver

Contents

4.1 Introduction

The conventional approach [339–341] for designing an IR-UWB energy-detection based receiver is to sample the RF signal employing a high-speed and high-power analog-to-digital converter (ADC) operating at clocks at several GHz followed by squaring and integrating the samples in the digital back-end for demodulation of the data bits. This approach is power-hungry and is not suitable in BAN scenario involving battery-operated nodes. A better option is to use the "integrate-and-digitize" approach [314, 342]. This approach integrates the square of the received signal for every integration window of duration T_{int} followed by digitization at the clock frequency of $f_{clk} = 1/T_{int}$. It reduces the power consumption due to the use of the ADC operating at a much lower frequency. A similar "integrate-and-digitize" approach has been followed in energy-detection based receiver [343, 344] to reduce the receiver complexity.

In this work, an energy-detector based UWB receiver using "integrate-and-digitize" approach for demodulation of M-ary PPM signal is presented. The proposed energy-detection based receiver passes the square of the received signal, the output of the RF front end, through a windowed integrator and successive approximation register analog-to-digital converter (SAR ADC) for generation of digitized samples. These digitized samples representing the received energy at every T_{int} duration are passed to the proposed digital back-end for demodulation of data bits. The proposed demodulator utilizes a mixed-signal technique for windowed integrator design and employs a new counter-based SAR controller for the single-ended SAR ADC.

This chapter presents the design, implementation and performance evaluation of a low-power UWB receiver operating in the mandatory low-band channel (Ch.#1) centered at 3.9936 GHz and employing the mandatory on-off signaling with a mandatory data rate of 0.4875 Mbps. The organization of the chapter is as follows. Section 4.2 discusses the link-budget for the default mode of operation. Section 4.3 presents the system-level architecture of the proposed energy-detection based receiver for BANs compliant to the 15.6 standard [2]. Section 4.4 and Section 4.5 present the design concepts and an implementation approach of the RF front-end and the mixed-signal demodulator respectively. This is followed by conclusions in Section 4.6.

4.2 Link Budget Analysis

The IEEE 802.15.6 [2] standard emphasizes that the transmission power of WBAN devices should be limited for reducing interference to other devices and for minimizing the specific absorption rate (SAR) into human bodies.

A top-level link budget analysis is the preliminary step for validation of feasibility of any wireless communication system. The received power (P_{RX}) is an important factor in a link budget analysis for determining the link margin of the system and can be expressed logarithmically as,

$$P_{RX} = \underbrace{P_{TX} + G_{TX}}_{\text{EIRP}} - PL + G_{RX} \quad (in\ dBm) \tag{4.1}$$

where P_{TX}: Transmitter output power, G_{TX}: Transmitter antenna gain, PL: Path loss in the radio channel and G_{RX}: Receiver antenna gain.

The maximum transmitted power (P_{TX}) is computed as per the FCC specifications [3] and it is given by

$$P_{TX} = -41.3 \text{ dBm/MHz} + 10log_{10}(BW) = -14.3\ dBm \tag{4.2}$$

for a bandwidth (BW) of 500 MHz.

Two wireless communications links are considered: (i) a body-to-body (BTB) link and (ii) a body-to-gateway (BTG) link as per the reported 15.6 channel model [4]. On-body UWB links need omni-directional antenna beam pattern [345], such as monopole antenna [346], ring-slot antenna [347] and micro-strip antenna [348]. Off-body links require unidirectional radiation patterns [345], for example, folded antenna [349] and dielectric resonator antenna [350]. For simplicity and for the purpose of demonstrating the impact of receiver performance, G_{TX} and G_{RX} are assumed to be 0 dBi.

The calculation of the expected path-loss (PL) for BTB and BTG wireless systems is considered next. We consider a BTB link for a maximum transmitter-receiver distance of 1.7 m (from forehead to toe) and a BTG link of 5 m. The channel models of the BTB and BTG links for WBAN communication are CM3 and CM4 respectively [4]. The path-loss (PL) is calculated as per the linear-fitting model [4] given by

$$PL(d) = alog_{10}(d) + b + N \tag{4.3}$$

where a and b are the coefficients of linear-fitting, d is the transmitter-receiver distance in mm and N is a normally distributed random variable with mean zero and standard deviation σ_N (Table 4.1).

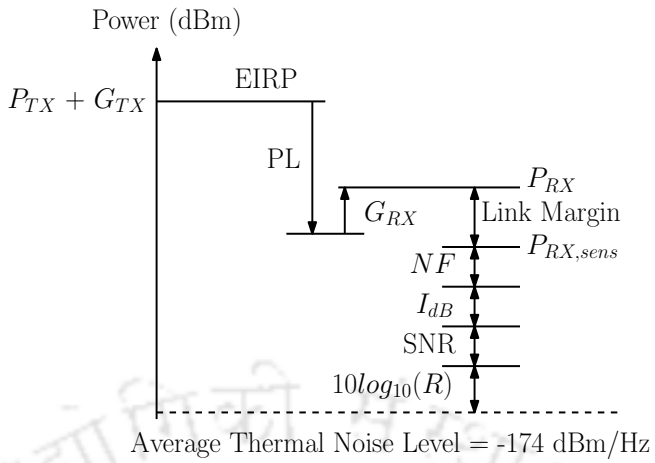


Figure 4.1: Analysis of Link Budget

Table 4.1: Coefficients of Linear-fitting Model for path loss [4]

a	19.2
b	3.38
σ_N	4.4

Table 4.2: Link Budget Analysis for 15.6-compliant receiver design in the default mode of operation

Application Scenario	BTB[1]	BTG[2]	
Parameter	Value		Unit
Modulation	M-ary PPM		-
R	0.4875		Mbps
BW	500		MHz
SNR_{min}	12		dB
NF	10		dB
I_{dB}	5		dB
PL	65.4[3]	74.4[4]	dB
P_{RX}[5]	-79.7	-88.7	dBm
$P_{RX,sens}$	-91		dBm
Link Margin[6]	11.3	2.3	dB

[1] BTB= Body-to-body communication link; [2] BTG= Body-to-gateway off-body communication link; Maximum Distance [3]d=1.7 m and [4]d= 5 m; [5]EIRP = -14.3 dBm, $G_{TX} = G_{RX} = 0$ dBi; [6]Link Margin = P_{RX} - $P_{RX,sens}$

The path losses for BTB and BTG communication are 65.4 dB and 74.4 dB respectively.

For successful demodulation, the received power (P_{RX}) must be greater than the receiver sensitivity $P_{RX,sens}$ given by

$$P_{RX,sens} = 10\ log_{10}(R) + SNR_{min} + NF + I_{dB} - 174\ dBm \tag{4.4}$$

where $P_{RX,sens}$ is the receiver sensitivity ($P_{RX,sens}$= -91 dBm for the data rate (R) of 0.4875 Mbps [2]), SNR_{min} is the minimum required signal-to-noise ratio (SNR) at demodulator input [2], NF is the noise

figure of the receiver [2] and I_{dB} is the implementation loss in the receiver [2]. The analysis of the link-budget is illustrated in Fig. 4.1.

The receiver sensitivity $P_{RX,sens}$ is the minimum power required at the input to the receiver antenna that yields a packet error rate (PER) less than 1% with a packet length of 24 octets. $P_{RX,sens}$ depends on the hardware implementation through NF, I_{dB} and PHY receiver design. The 15.6-compliant IR-UWB receiver design assumes a NF of 10 dB and an I_{dB} of 5 dB for fulfilling the receiver sensitivity requirements and successful data demodulation. The entire top-level link budget for IR-UWB transceivers operating at the default mode with data rate of 0.4875 Mbps for BTB and BTG communications is shown in Table 4.2. From Table 4.2 it is clear that the available link margins for BTB and BTG communications are positive and sufficient for reliable transmission and reception.

4.3 System-Level Architecture of Energy Detection based Receiver

Fig. 4.2 shows a simplified block diagram of the proposed energy detector based receiver. The various blocks in Fig. 4.2 can be broadly classified into two sections, namely, the RF front-end and the mixed-signal demodulator.

The RF front-end of the receiver consists of a low-noise amplifier (LNA), a multi-stage RF amplifier and a squarer. The main target of the RF front end is the amplification of the low level RF signal, attenuation of the out-of-band interference and conversion of the RF signal to the square of the baseband signal which is used for energy detection at a later stage. Since the commercially available UWB antennas are single-ended, the receiver input to the LNA is assumed to be single-ended [342]. The LNA performs single-ended to differential conversion followed by a cascade of multi-stage RF amplifiers. The input to the LNA is of the order of μVs[1] whereas the minimum input voltage requirement to the squarer is in mVs [342]. This demands the need of a high voltage gain intermediate stage [342]. The non-coherent receiver typically employs one of the following configuration [342]: super-regenerative amplifier [351] or multi-stage RF amplifier [352]. The multi-stage RF amplifier is normally preferred due to its low RF leakage current [342]. Further, it supports squaring and integrating functions [342]. Finally, the squarer shifts the frequency of RF signal to baseband frequency eliminating the need for a RF local oscillator [342, 343]. Unlike the local oscillator mixer configuration, the squarer generates square of the baseband signal and produces the best performance among the possible energy detector

[1]The minimum input to the LNA is $P_{RX,sens}$= -91 dBm. $\Rightarrow$ This corresponds to a voltage level of 6.3 μV for 50 Ohm system

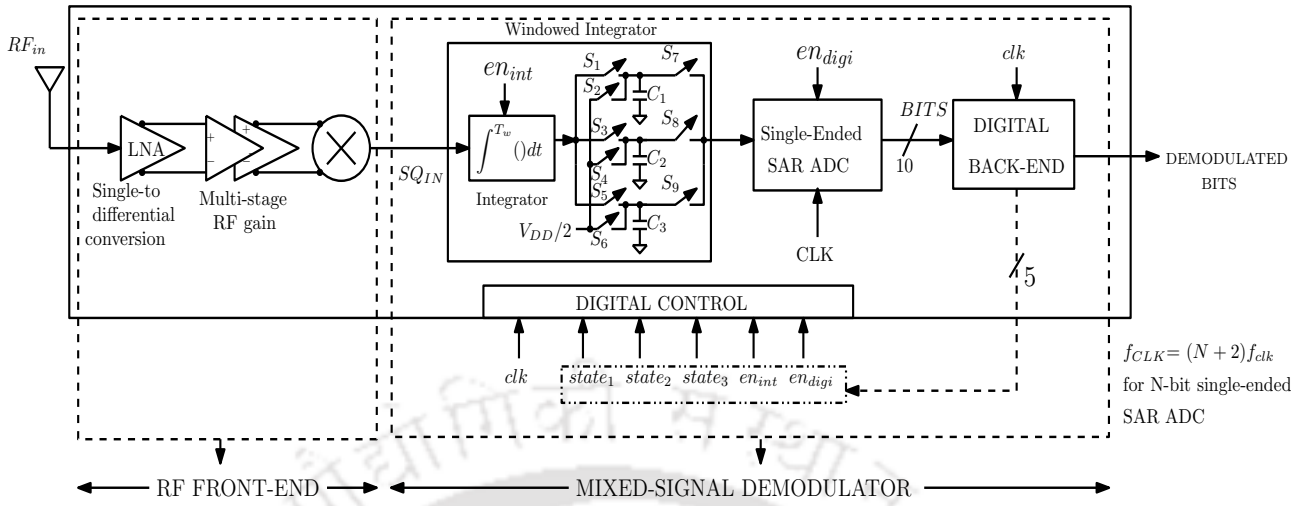


Figure 4.2: Block diagram of the proposed energy-detection based receiver

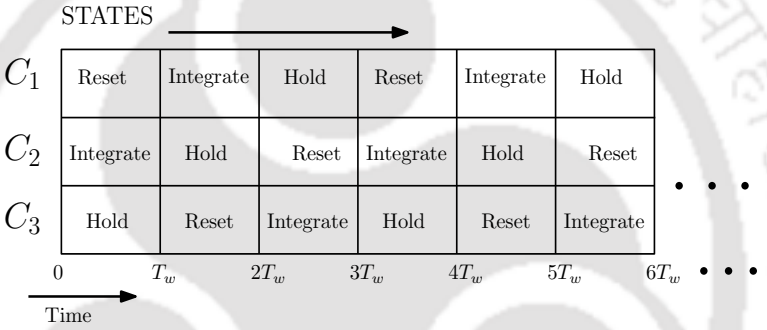


Figure 4.3: States of windowed integrator

receivers [353]. Next, the baseband signal is passed through the mixed-signal baseband demodulator described below.

The mixed-signal baseband demodulator is comprised of a windowed integrator, a single-ended SAR ADC and a digital back-end. The baseband integrator is designed for an integration window of T_w. The total number of integration windows is $2log_2(M)$ for demodulation of M-ary symbol (2 for binary symbol and 8 for 16-ary symbol). The windowed integrator shown in Fig. 4.2 is activated only when en_{int} signal is high. The three states of windowed integrator are 'reset', 'integrate' and 'hold'. The 'reset' state sets the voltage across the capacitor to $V_{DD}/2$ for a duration of T_w and the 'integrate' state stores the integrated values of energies for the next T_w duration. The 'hold' state stores the output of the integrator for the next T_w duration to perform digitization when en_{digi} is high. The enable signals (en_{int} and en_{digi}) are asserted by the digital back-end. Based on the switching positions of switches S_1 to S_9, the states of the capacitors are changed as shown in Fig. 4.3.

For example, during the duration 0 to T_w, C_1 goes to 'reset' state (i.e. C_1 is reset to $V_{DD}/2$), C_2 is in 'integrate' state while C_3 is in 'hold' state. Similarly, during T_w to $2T_w$, C_1 goes to 'integrate state, C_2 to 'hold' state and C_3 to 'reset' state and so on. Digitization of the analog samples is performed using a simplified 10-bit single-ended SAR ADC. The SAR ADC employs a counter-based SAR digital controller and a modified merged capacitor switching scheme. The digitized energy samples are passed to the digital back-end for demodulation of data bits. The demodulated bits are forwarded to the baseband processor which decodes the data bits conforming to the 15.6 specifications [2]. The design concepts and circuit implementation of the RF front-end and the mixed-signal demodulator are described in the following sections.

4.4 Implementation of the RF Front-end

The RF front-end of the receiver consists of a LNA, a multi-stage RF amplifier and a squarer. The main objective of the RF front end is the need for high voltage gain from the input to the LNA (of the order of μVs) to the input of the squarer (of the order of mVs) followed by conversion of the amplified RF signal to the square of the baseband signal (by the squarer) which is used for energy detection at a later stage.

The gain to be provided by the LNA and the multi-stage RF amplifier prior to the squarer (Fig. 4.2) is calculated by taking into account the following factors:

(i) Received power at the input of the antenna: P_{RX}

Let $P_{RX,max}$ be the maximum received power for a minimum transmitter-receiver distance of 2 cm in a BTB link and let $P_{RX,min}$ be the minimum received power for a maximum transmitter-receiver distance of 5 m in a BTG link. Under the assumption that G_{TX}= G_{RX}= 0 dBi, the values of $P_{RX,max}$ and $P_{RX,min}$ are computed as

$$P_{RX,max} = P_{TX} - PL(d = 2\ cm) = -14.3\ dBm - 28.36\ dB = -42.7\ dBm \tag{4.5}$$

$$P_{RX,min} = P_{TX} - PL(d = 5\ m) = -14.3\ dBm - 74.4\ dB = -88.7\ dBm \tag{4.6}$$

where,

P_{TX} is the maximum transmitted power equal to -14.3 dBm obtained using the relation

$$P_{TX} = -41.3\ \text{dBm/MHz} + 10\ log_{10}(BW) = -14.3\ dBm \tag{4.7}$$

for a bandwidth (BW) of 500 MHz.

In (4.5) and (4.6), PL (d= 2 cm) and PL (d= 5 m) are the path losses in the radio channel corresponding to the transmitter-receiver distance of 2 cm and 5 m respectively using the relation

$$PL(d) = alog_{10}(d) + b + N \tag{4.8}$$

Here, a= 19.2 and b= 3.38 are the co-efficients of linear-fitting, d is the transmitter-receiver distance in mm and N is a normally distributed random variable with mean zero and standard deviation σ_N= 4.4.

(ii) Required power at the input to the squarer: $P_{RX,squarer}$

As stated in [342], the input to the LNA is of the order of μVs while the input to the squarer is of the order of a few tens of mVs. Accordingly, it is assumed that the maximum amplitude of the squarer input is 20 mV. This roughly corresponds to $P_{RX,squarer} \approx$ -20 dBm.

The minimum and the maximum gain, $Gain_{min}$ and $Gain_{max}$ (from the LNA and the multi-stage RF amplifier) are equal to 23 dB and 71 dB respectively and are computed as

$$Gain_{min} = P_{RX,squarer} - P_{RX,max} = -20\ dBm - (-42.7\ dBm) \approx 23\ dB \tag{4.9}$$

$$Gain_{max} = max \begin{cases} P_{RX,squarer} - P_{RX,min} = -20\ dBm - (-88.7\ dBm) & \approx 69\ dB \\ P_{RX,squarer} - P_{RX,sens} = -20\ dBm - (-91\ dBm) & \approx 71\ dB \end{cases} \tag{4.10}$$

Therefore, the LNA and the multi-stage RF amplifier are to be designed in such a way that it provides a minimum gain of $Gain_{min}$= 23 dB and a maximum gain of $Gain_{max}$= 71 dB for amplification of received signal prior to the squarer.

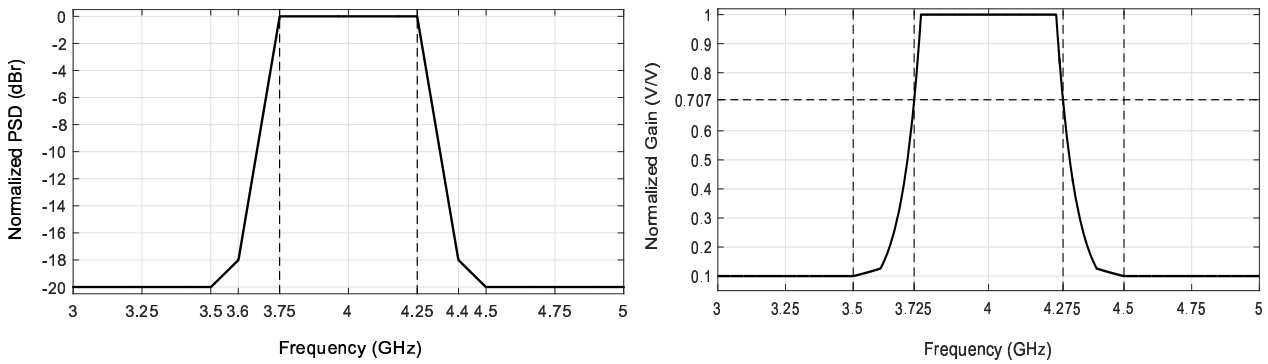
Let $BW_{-3dB,i}$ be the bandwidth of the i^{th} stage in a cascade of n tuned stages (i= 1, 2,..., n). Then the overall -3 dB bandwidth can be computed by the relation [354]:

$$BW_{-3dB,overall} = \left(\frac{1}{BW^2_{-3dB,1}} + \frac{1}{BW^2_{-3dB,2}} + \frac{1}{BW^2_{-3dB,3}} + \cdots + \frac{1}{BW^2_{-3dB,n}} \right)^{-\frac{1}{2}} \tag{4.11}$$

where,

$BW_{-3dB,overall}$= Overall -3 dB bandwidth of a cascade of n tuned stages (in Hz),

$BW_{-3dB,n}$= -3 dB bandwidth of the n^{th} tuned stage (in Hz),



(a) (b)

Figure 4.4: (a) Normalized WBAN Transmit Spectral Mask and (b) corresponding normalized Gain Spectrum

n= number of stages.

The cascading of the gain stages reduces the overall -3 dB bandwidth of the LNA and the multi-stage RF amplifier. Therefore, the -3 dB bandwidth of the LNA and the multi-stage RF amplifier is designed in such a way that it meets the WBAN transmit spectral mask (Fig. 4.4(a)). The corresponding gain spectrum of the WBAN spectral mask is shown in Fig. 4.4(b).

The circuit implementation of the RF front-end is described next.

4.4.1 LNA

The LNA is a single-to-differential conversion RF amplifier architecture employing the approaches presented in [355,356]. Fig. 4.5 presents the circuit schematic of the LNA. The LNA is a common-gate, common-source (CG-CS) amplifier. It uses the CG stage to provide a wideband impedance matching of 50 Ω to the output of the antenna at the receiver for the full frequency band of operation. The CG stage amplifies the input to the LNA in-phase; the parallel CS stage amplifies the same input with a phase difference of 180°. The input signal is amplified with the same gain in both the CG and CS stages. The LNA is designed by proper sizing of the CMOS transistors and by proper choice of the resistance 'R' of the resonant load (Fig. 4.5).

Fig. 4.6 shows the simulated single-ended gain of the single-to-differential LNA (Fig. 4.5). From Fig. 4.6 it is seen that a single-ended gain of 5.68 V/V (= 15.1 dB) is obtained for a -3 dB bandwidth ($BW_{-3dB,LNA}$) of 960 MHz:

$$Gain_{LNA} \sim 15\ dB \tag{4.12}$$

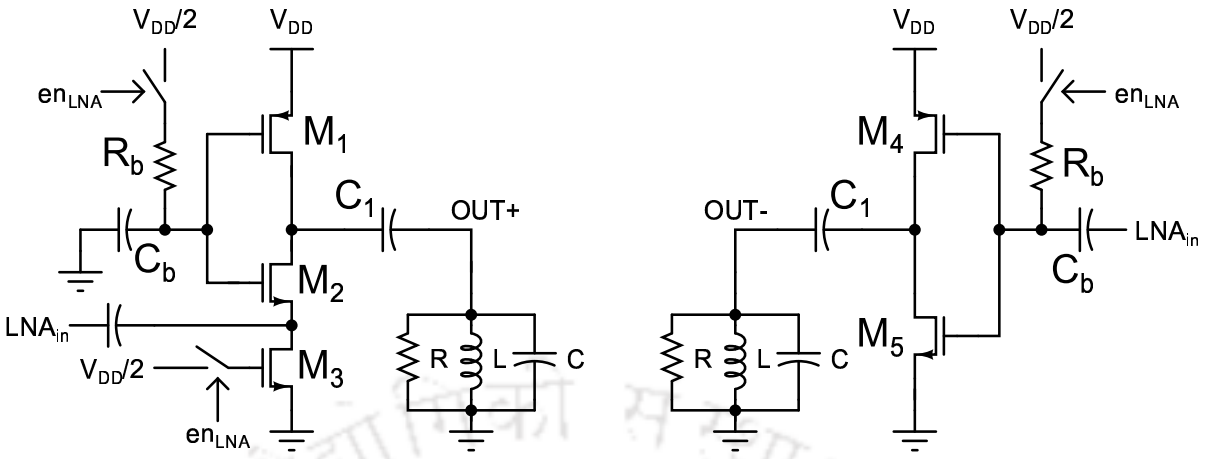
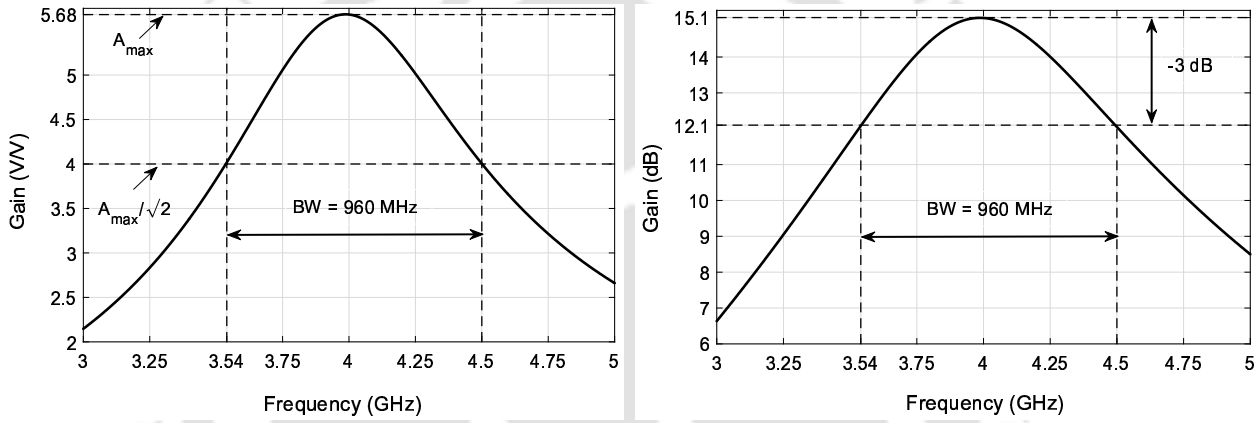
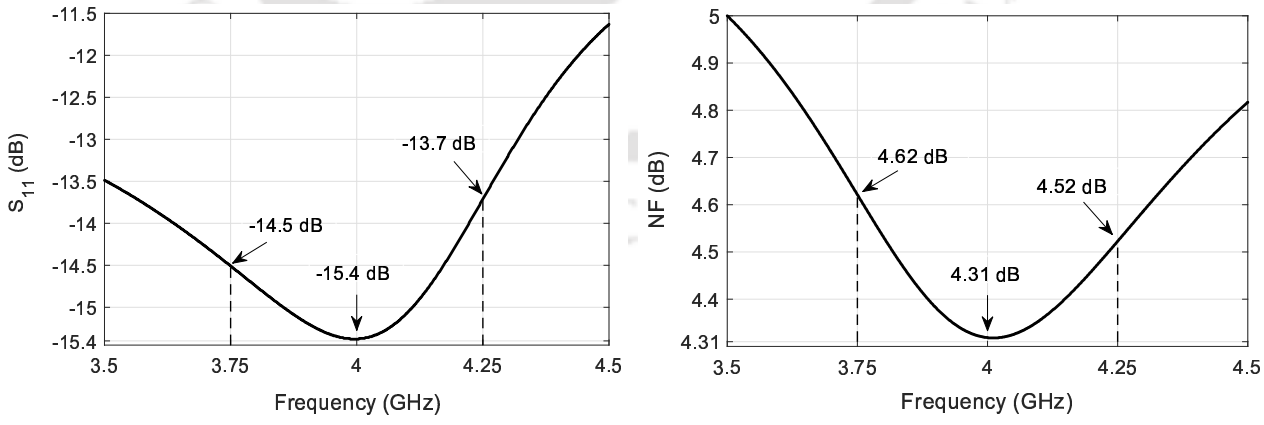


Figure 4.5: Circuit schematic of a single-to-differential LNA



(a) (b)

Figure 4.6: Simulated single-ended gain of the single-to-differential LNA (a) in V/V (b) in dB



(a) (b)

Figure 4.7: Simulated (a) S_{11} and (b) NF performance of the single-to-differential LNA

The S_{11} and the noise figure (NF) for frequency span from 3.5 GHz to 4.5 GHz are shown in Fig. 4.7(a) and Fig. 4.7(b) respectively. The obtained values of S_{11} is -15.4 dB and that of NF is 4.31 dB at the centre frequency.

4.4.2 Multi-stage RF Amplifier

The multi-stage RF amplifier follows the LNA (Fig. 4.2). The LNA provides a gain of 15 dB and the remaining gain is to be achieved by the multi-stage RF amplifier.

The employed multi-stage RF amplifier is a cascade of 'n' identical and equal gain stages[2]. Each gain stage is an inverter-based amplifier with a RLC resonant load. The inverter-based amplifier shown in Fig. 4.8 is the most suitable amplifier structure for gain stages of the multi-stage RF amplifier [342].

Each inverter-based amplifier stage (Fig. 4.8) provides a gain of 2.52 V/V (= 8 dB) as shown in Fig. 4.9:

$$Gain_{per\_stage} = 8\ dB \tag{4.13}$$

Hence using (4.9) and (4.10), the maximum and the minimum number of inverter-based amplifier can be found:

$$No\_of\_gain\_stages_{max} = \frac{Gain_{max} - Gain_{LNA}}{Gain_{per\_stage}} = \frac{71\ dB - 15\ dB}{8\ dB} = 7 \tag{4.14}$$

$$No\_of\_gain\_stages_{min} = \frac{Gain_{min} - Gain_{LNA}}{Gain_{per\_stage}} = \frac{23\ dB - 15\ dB}{8\ dB} = 1 \tag{4.15}$$

Fig. 4.10 shows the circuit schematic of the implemented multi-stage RF amplifier with a cascade of seven gain stages followed by a single squarer. Each gain stage for RF amplification is an inverter-based amplifier with a RLC resonant load (Fig. 4.8). $en_{RF,1}$, ..., $en_{RF,7}$ are the signals (Table 4.3) enabling or disabling the gain stages of the multi-stage RF amplifier. The amplified signals from the gain stages are output to a single squarer through switches controlled by digital signals $en_{sq,1}$, ..., $en_{sq,7}$ (Table 4.3).

At the lowest gain setting, the signal is amplified by the first gain stage providing a gain of

[2]The most energy-efficient way of designing the multi-stage RF amplifier is by cascading equal gain stages [357]. In case of equal gain stages, with the increase of the number of gain stages, the total gain increases exponentially but the power consumption increases linearly. However, in case of unequal gain stages, both the gain and power consumption increases exponentially [357].

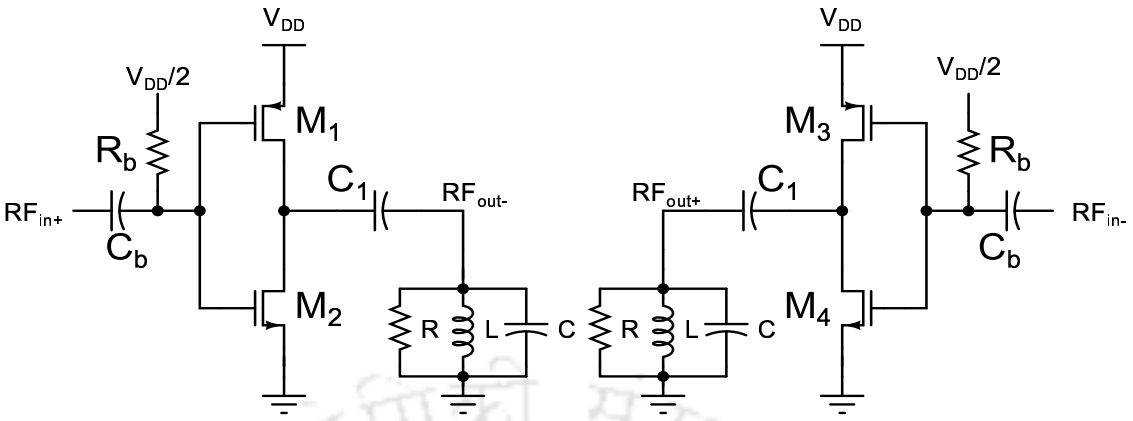
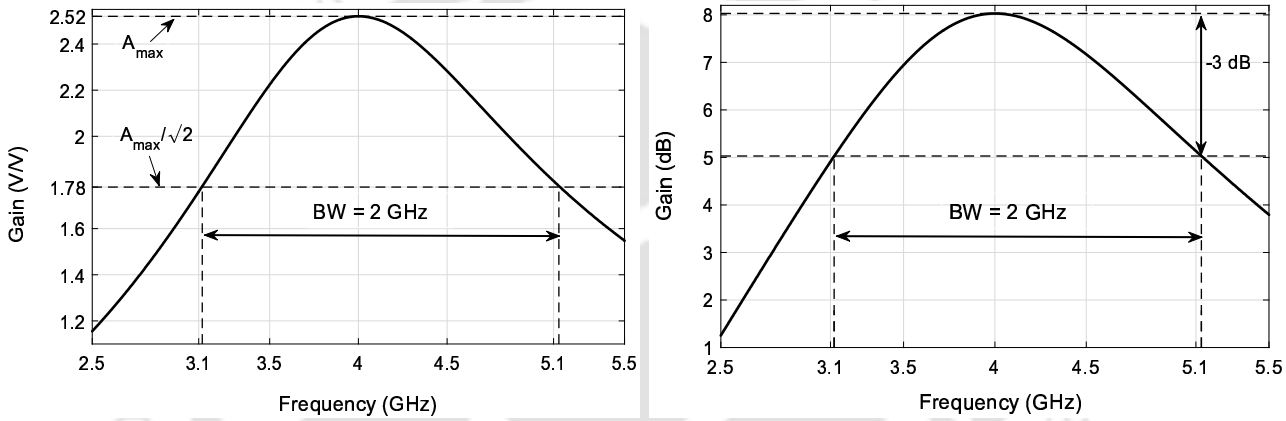


Figure 4.8: Schematic of the inverter-based amplifier with a RLC resonant load



(a) (b)

Figure 4.9: Simulated single-ended gain of the inverter-based amplifier (a) in V/V (b) in dB

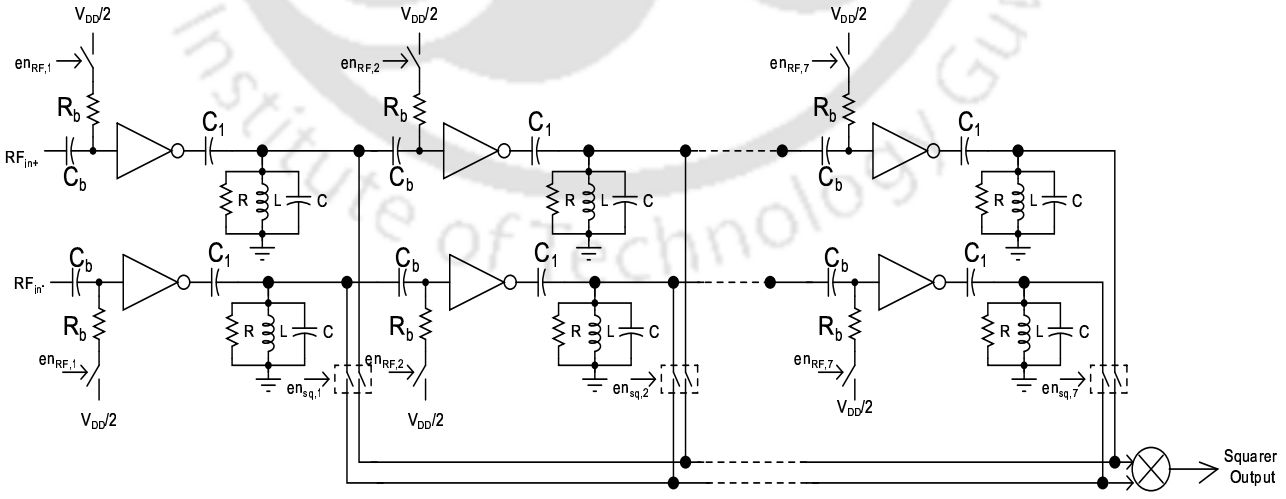


Figure 4.10: A complete schematic of the multi-stage RF amplifier with seven gain stages and followed by a single squarer

Table 4.3: Digital Settings of the Multi-stage RF Amplifier with seven equal gain stages: $Gain_{per\_stage}$= 8 dB

Gain Stages	Digital Signals	On/Off States						
		Required Gain from Multi-stage RF amplifier						
		8 dB	16 dB	24 dB	32 dB	40 dB	48 dB	56 dB
$Stage_1$	$en_{RF,1}$	✓	✗	✗	✗	✗	✗	✗
	$en_{sq,1}$	✓	✗	✗	✗	✗	✗	✗
$Stage_2$	$en_{RF,2}$	✓	✓	✗	✗	✗	✗	✗
	$en_{sq,2}$	✗	✓	✗	✗	✗	✗	✗
$Stage_3$	$en_{RF,3}$	✓	✓	✓	✗	✗	✗	✗
	$en_{sq,3}$	✗	✗	✓	✗	✗	✗	✗
$Stage_4$	$en_{RF,4}$	✓	✓	✓	✓	✗	✗	✗
	$en_{sq,4}$	✗	✗	✗	✓	✗	✗	✗
$Stage_5$	$en_{RF,5}$	✓	✓	✓	✓	✓	✗	✗
	$en_{sq,5}$	✗	✗	✗	✗	✓	✗	✗
$Stage_6$	$en_{RF,6}$	✓	✓	✓	✓	✓	✓	✗
	$en_{sq,6}$	✗	✗	✗	✗	✗	✓	✗
$Stage_7$	$en_{RF,7}$	✓	✓	✓	✓	✓	✓	✓
	$en_{sq,7}$	✗	✗	✗	✗	✗	✗	✓

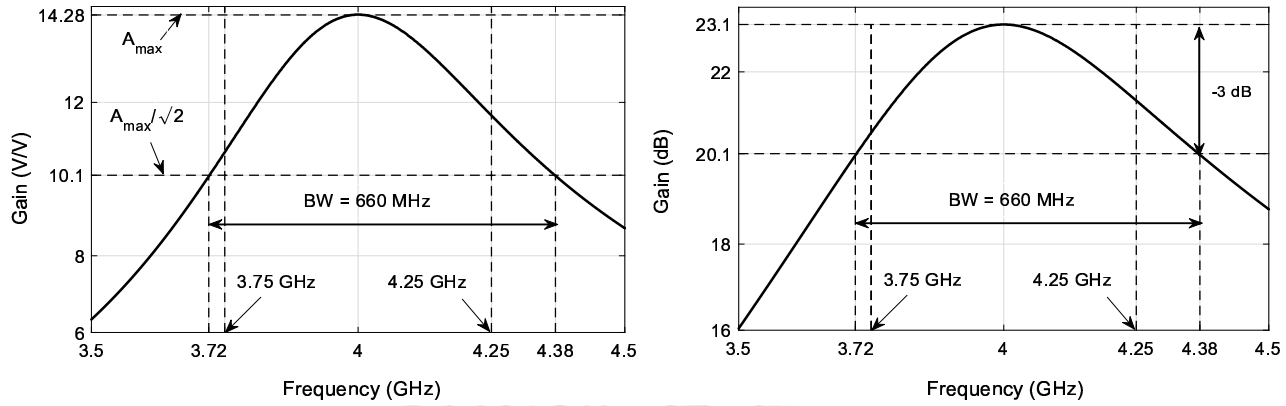
✓: Closes the switch; ✗: Opens the switch

$Gain_{min}$= 8 dB and output to the squarer. At the highest gain setting, the signal is amplified by all the seven stages providing maximum amplification of $Gain_{max}$= 56 dB and then fed to squarer. Hence the multi-stage RF amplifier supports gain scalability from $Gain_{min}$= 8 dB to $Gain_{max}$= 56 dB by a multiple of $Gain_{per\_stage}$= 8 dB.

The frequency response of a cascade of the LNA and the multi-stage RF amplifier ($No\_of\_gain\_stages$ = 1, 2, . . . , 6, 7) is shown in Fig. 4.11, Fig. 4.12, Fig. 4.13, Fig. 4.14, Fig. 4.15, Fig. 4.16 and Fig. 4.17. It can be observed from Fig. 4.17 that the maximum single-ended gain obtained is $Gain_{overall}$= 3306.7 V/V (= 70.4 dB) for a $BW_{-3dB,overall}$= 544 MHz. The overall bandwidth $BW_{-3dB,overall}$= 544 MHz is close to the normalized gain spectrum (Fig. 4.4(b)).

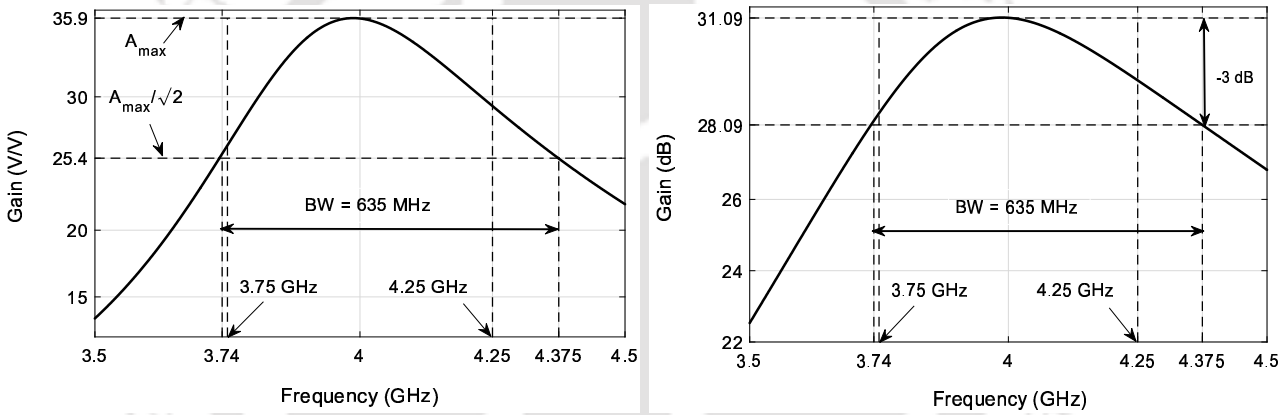
Discussions

It is observed that in 180 nm technology (technology employed in this work) the inverter-based amplifier exhibits a -3 dB cut-off frequency at around 1.5 ∼ 2 GHz (Appendix B.1). Thus it may be inferred that an inverter-based amplifier with a resonant load at f_c ∼ 4 GHz will display a skewed bandpass characteristic with a much reduced gain. Hence it was felt that an advanced technology should be explored. Appendix B.2 gives a design of the RF front-end (LNA and Multi-stage RF amplifier) in 65 nm technology. Though the basic amplifier in 65 nm technology has a wider frequency response, it is seen that there is no significant improvement in the overall response of the RF stage and requires around the same number of stages of RF amplification.



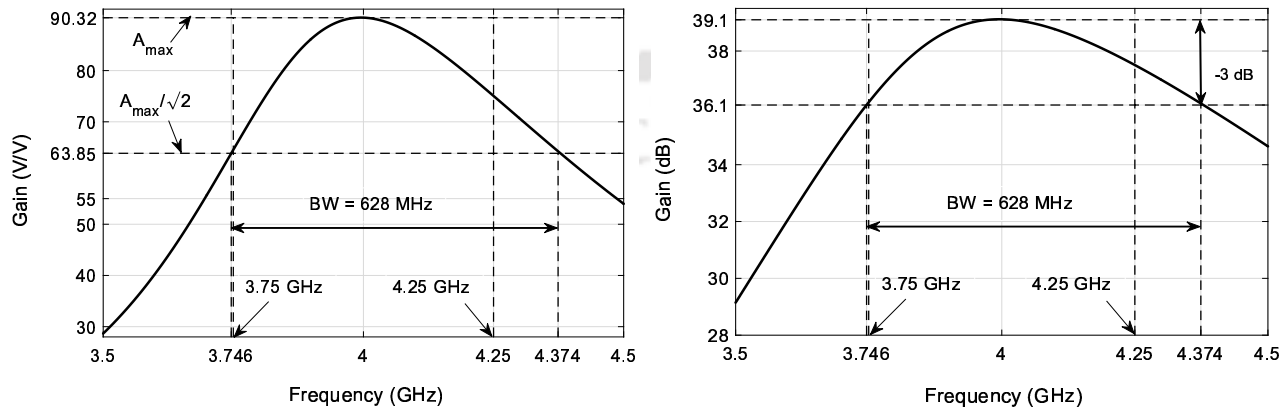
(a) (b)

Figure 4.11: Simulated single-ended gain of a cascade of the LNA and the multi-stage RF amplifier ($No\_of\_gain\_stages_{min}$= 1) (a) in V/V (b) in dB



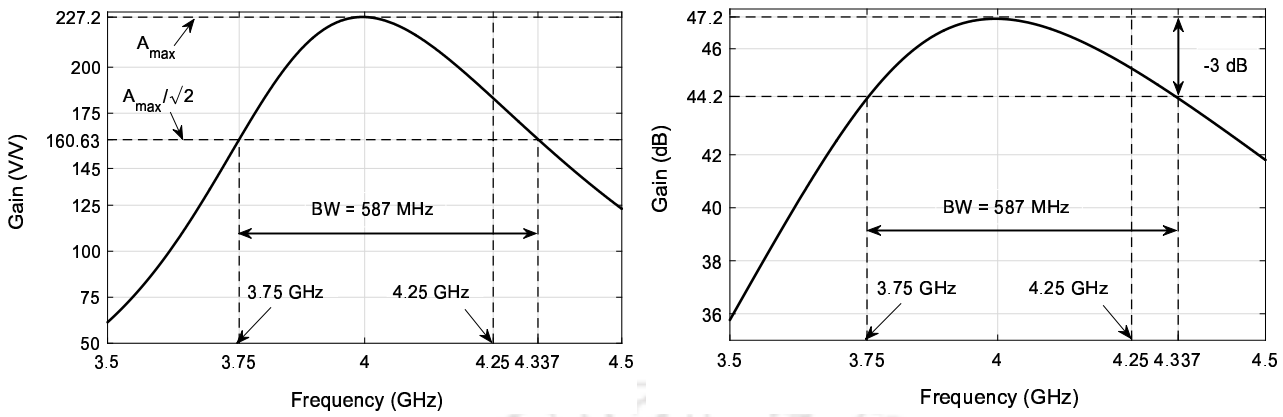
(a) (b)

Figure 4.12: Simulated single-ended gain of a cascade of the LNA and the multi-stage RF amplifier ($No\_of\_gain\_stages$= 2) (a) in V/V (b) in dB



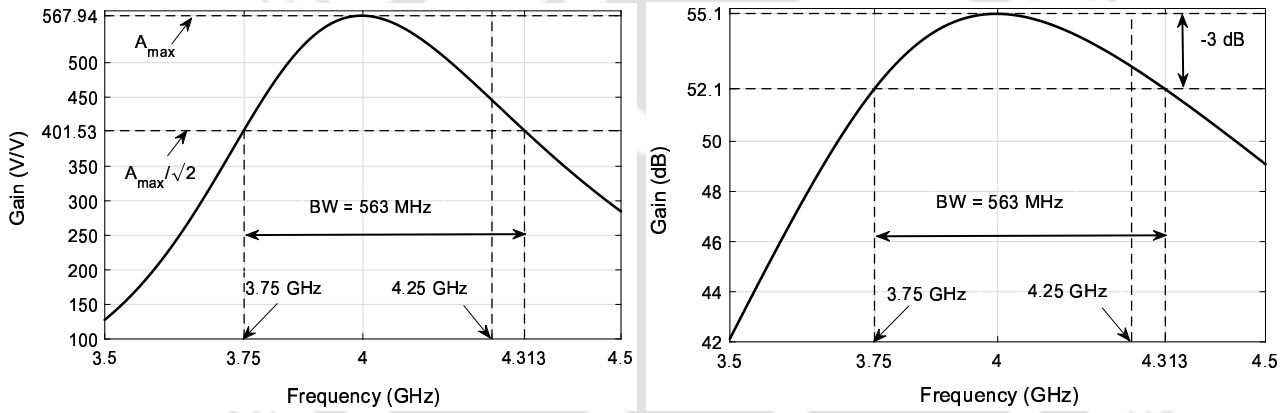
(a) (b)

Figure 4.13: Simulated single-ended gain of a cascade of the LNA and the multi-stage RF amplifier ($No\_of\_gain\_stages$= 3) (a) in V/V (b) in dB



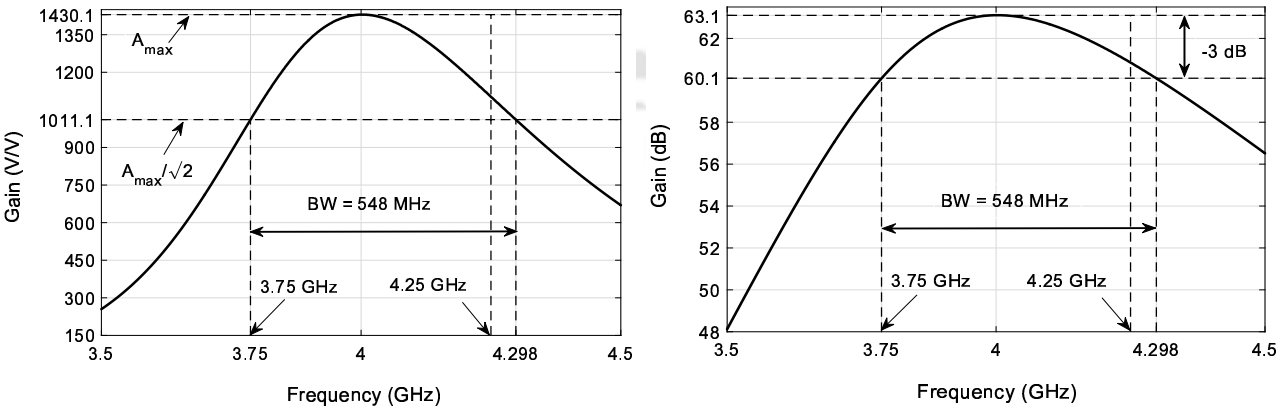
(a) (b)

Figure 4.14: Simulated single-ended gain of a cascade of the LNA and the multi-stage RF amplifier ($No\_of\_gain\_stages$= 4) (a) in V/V (b) in dB



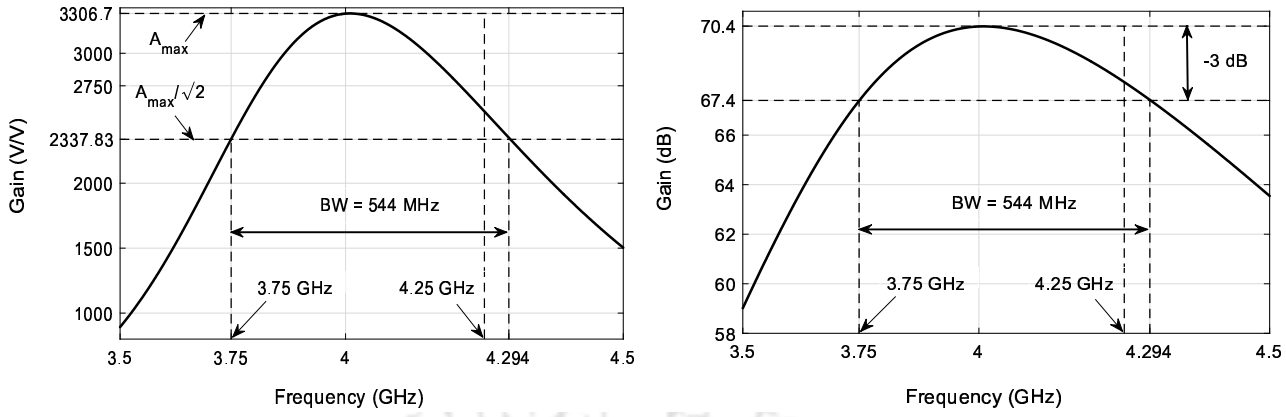
(a) (b)

Figure 4.15: Simulated single-ended gain of a cascade of the LNA and the multi-stage RF amplifier ($No\_of\_gain\_stages$= 5) (a) in V/V (b) in dB



(a) (b)

Figure 4.16: Simulated single-ended gain of a cascade of the LNA and the multi-stage RF amplifier ($No\_of\_gain\_stages$= 6) (a) in V/V (b) in dB



(a) (b)

Figure 4.17: Simulated single-ended gain of a cascade of the LNA and the multi-stage RF amplifier ($No\_of\_gain\_stages_{max}$= 7) (a) in V/V (b) in dB

4.4.3 Squarer

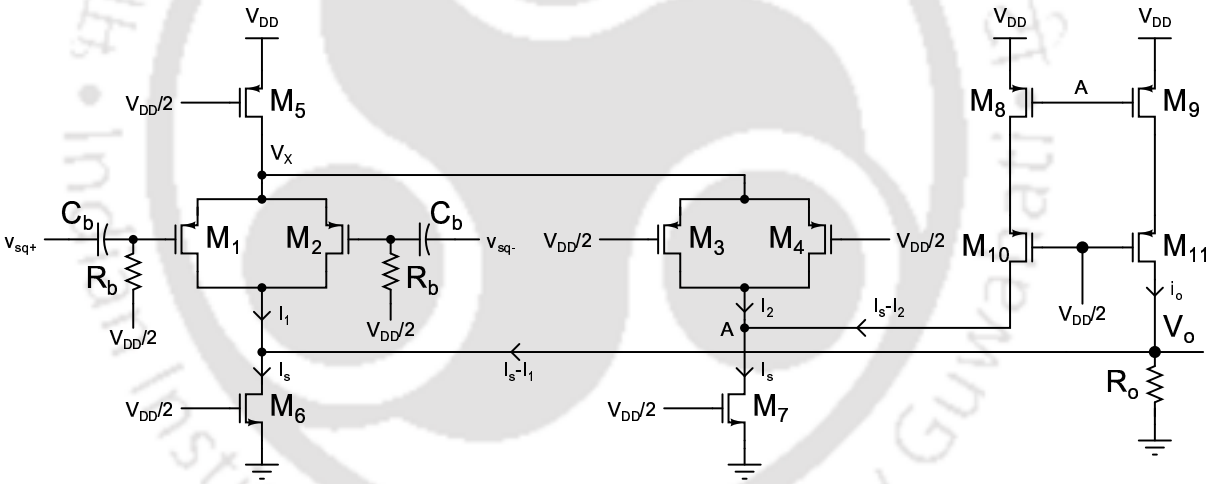


Figure 4.18: Circuit schematic of the squarer

The (voltage) squarer is a useful non-linear block gaining attention of circuit designers for realization of the RF front-ends. The purpose of the squarer used in Fig. 4.2 is to shift the information bearing RF spectrum to baseband thereby eliminating the need for a RF local oscillator.

Fig. 4.18 shows the circuit schematic of the squarer using the approach presented by Giustolisi *et al.* [358]. The squarer has a fully differential input (v_{sq+} and v_{sq-}) at a common-mode voltage level of $V_{DD}/2$. M_1- M_4 are the transistors that perform the basic squaring function (by keeping the transistors biased in the saturation region), M_5- M_7 provide the bias currents and M_8- M_{11} take care of the differential to single-ended conversion by forming a cascode current mirror. The details of the

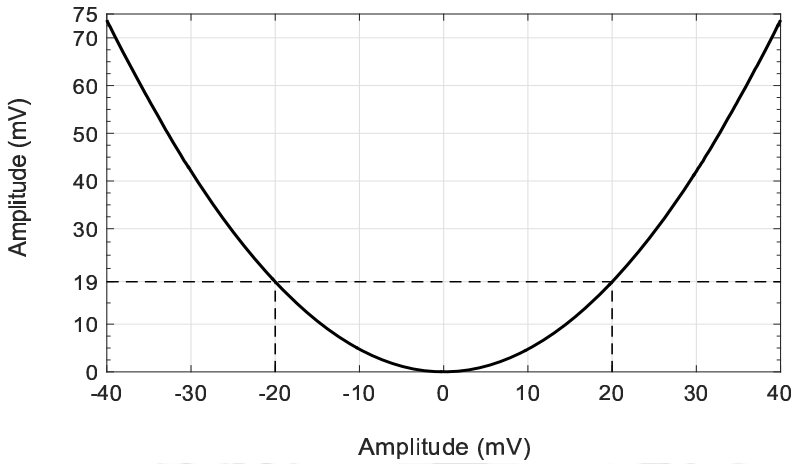


Figure 4.19: Output voltage against input voltage of the squarer

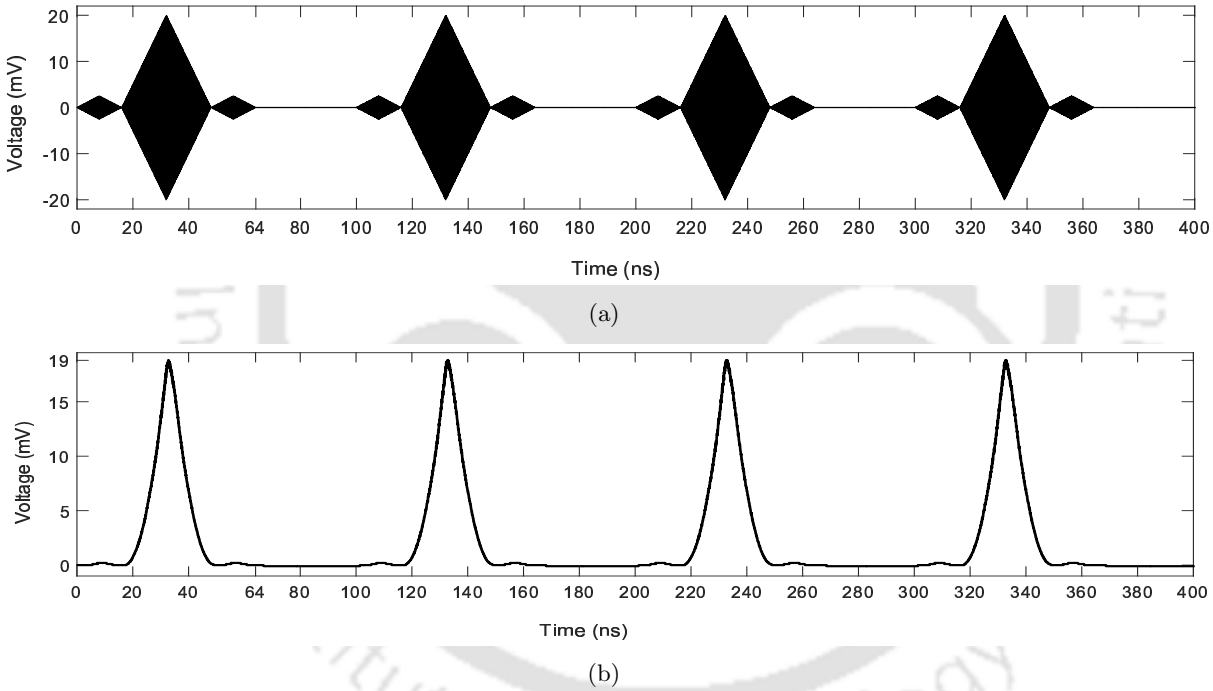


Figure 4.20: Simulation response of the squarer: (a) 40 mV V_{p-p} RF input and (b) Output of squarer having a peak amplitude of around 19 mV

squaring operation is given in Appendix A.1.

The voltage transfer characteristics of the squarer is shown in Fig. 4.19. It can be observed from Fig. 4.19 that the circuit performs squaring operation for input signals in the range of -40 mV to 40 mV.

A simulation of the squarer in response to a RF input signal of amplitude 40 mV V_{p-p} (Fig. 4.20(a)) is performed. Fig. 4.20(b) shows the transient response of the squarer in response to this

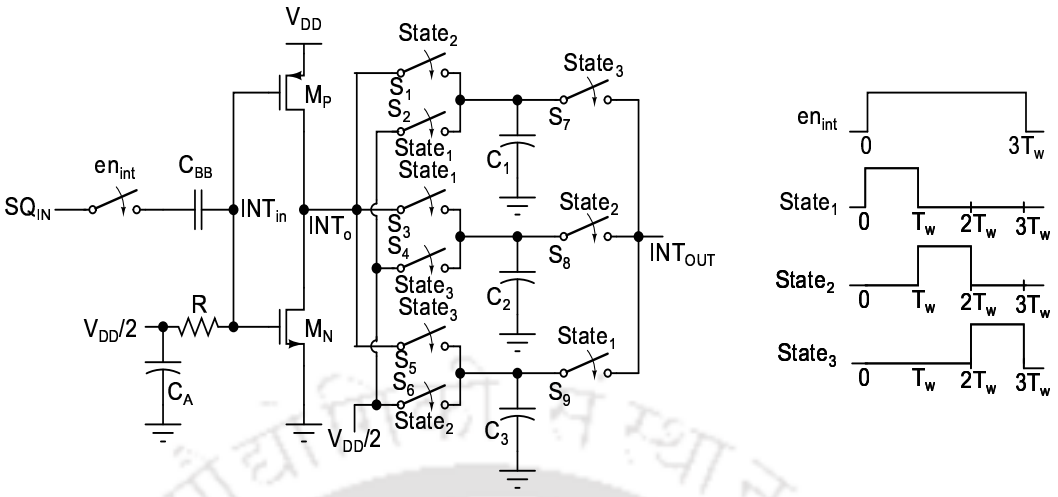


Figure 4.21: Windowed Integrator and its timing diagrams

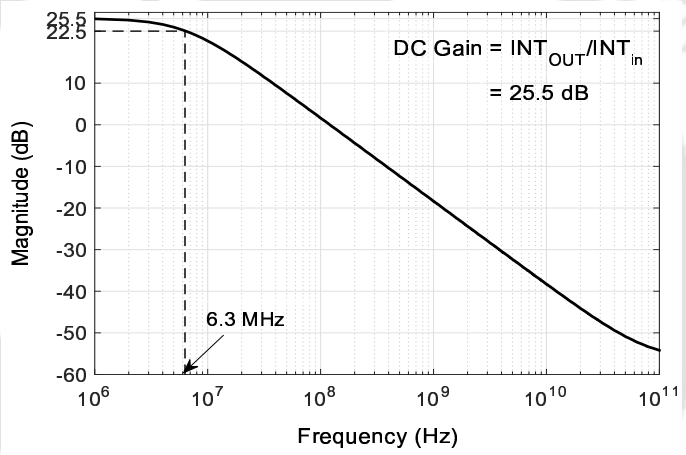


Figure 4.22: Simulated frequency response of windowed integrator

input (Fig. 4.20(a)).

The output of squarer (the squared baseband signal of the received RF signal) is next fed to the integrator of the mixed-signal demodulator (Fig. 4.2).

4.5 Implementation of the Mixed-Signal Demodulator

4.5.1 Windowed Integrator

The windowed integrator is designed using mixed-signal techniques employing the integrator design approach in [343]. However, unlike the switching mechanism in [343], we propose a new digital switching method for the windowed integrator (Fig. 4.2) in order that the method is applicable for both binary and 16-ary PPM signaling conforming to the 15.6 standard. Fig. 4.21 shows the proposed

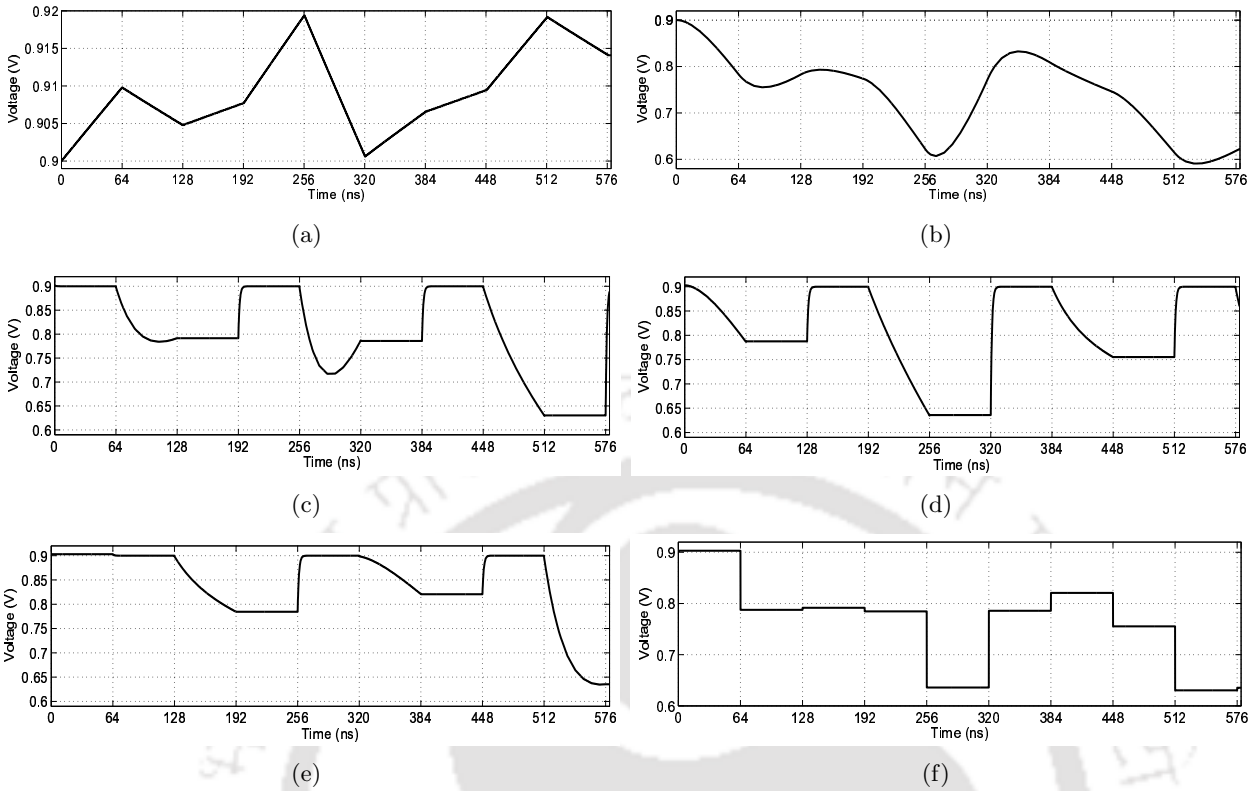


Figure 4.23: Simulated transient response of windowed integrator: (a) INT_{in} (b) INT_o (c) voltage across C_1 (d) voltage across C_2 (e) voltage across C_3 (f) INT_{OUT}

windowed integrator where SQ_{IN} is the squared baseband signal at the output of the RF front-end.

The input to the windowed integrator is biased at the switching threshold $V_{DD}/2$ through a high impedance isolation resistance (R). Use of a symmetric inverter ensures that the output INT_o also gets biased to $V_{DD}/2$. By properly sizing of the CMOS transistors M_P and M_N and by proper choice of external capacitors: C_1= C_2= C_3, an integrator is realized with a DC gain of 25.5 dB and a -3 dB frequency at around 6.3 MHz (Fig. 4.22).

The input and the output of the integrator are shown in Fig. 4.23(a) and Fig. 4.23(b) respectively. The integrated output is available on one of the three capacitors C_1, C_2 and C_3 for every T_w duration in accordance to the change of states of the capacitors as shown in Fig. 4.3. The waveforms across the capacitors C_1, C_2 and C_3 are shown in Fig. 4.23(c), Fig. 4.23(d) and Fig. 4.23(e) respectively and the final output is shown in Fig. 4.23(f). For example, the capacitor C_1 stays in 'Reset' state for the first T_w duration. This is followed by an increment of T_w duration as integration period at 'Integrate' state. Next, the capacitor C_1 holds the final integration value for an additional T_w duration in 'Hold'

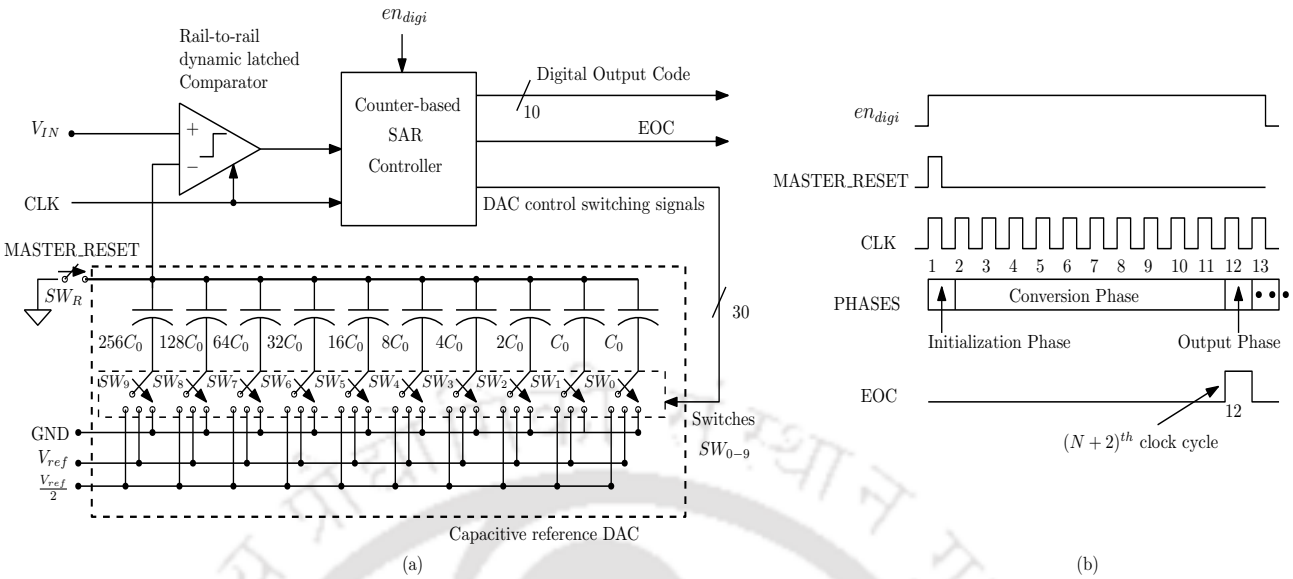


Figure 4.24: (a) Basic Block Diagram of the proposed single-ended SAR ADC and (b) Timing Diagram of the proposed counter-based SAR digital controller for single-ended SAR ADCs

state. The time taken during the 'Hold' state is the time during which the digitization of integrated value stored in the capacitor C_1 takes place for subsequent demodulation. The INT_{OUT} connects the final output of the windowed integrator to the 10-bit single-ended SAR ADC for digitization.

4.5.2 Single-ended SAR ADC

The block diagram of the proposed single-ended SAR ADC is shown in Fig. 4.24(a). The ADC core consists of a master reset, a capacitive reference digital-to-analog converter (DAC), a rail-to-rail dynamic latched comparator and a counter-based SAR controller. The master reset switch acts as the initialization switch for discharging the top plates of the capacitive DAC to ground at the start of ADC conversion. The DAC capacitors are implemented using binary weighted capacitors as $[2^{N-2}C_0,\ 2^{N-3}C_0,\ \ldots,\ 2C_0,\ C_0,\ C_0]$ for N-bit implementation with C_0 unit capacitor. When the MASTER_RESET switch is closed, the top plates of the DAC capacitors connected to the negative terminal of the comparator are discharged to ground through the switch SW_R. The EOC signal acts as the enable signal for outputting the "ten-bit" digitized version of an analog sample. The output "sample-and-hold" integrated value from the windowed integrator (Fig. 4.21) is connected to the positive terminal V_{IN} of the dynamic latched comparator. The output of the windowed integrator serves as the input to the single-ended SAR ADC. The timing diagram of the proposed SAR ADC is illustrated in Fig. 4.24(b). The circuit implementations of the various blocks of the single-ended SAR

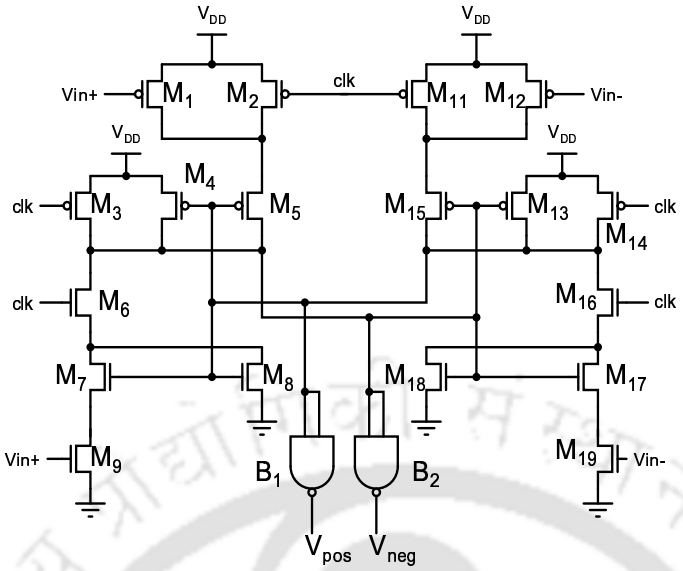


Figure 4.25: Rail-to-rail dynamic latched comparator

ADC are explained below:

4.5.2.1 Rail-to-rail dynamic latched comparator

It is desirable to have a comparator with a small offset and a fast decision time for SAR ADC design. In order to meet these requirements, the rail-to-rail dynamic latched comparator proposed in [359] is considered and shown in Fig. 4.25. The design exhibits good performance upto 500 MHz with zero static power dissipation. Moreover, the design eliminates the need for pre-amplifier.

4.5.2.2 Capacitive reference DAC

The capacitive reference DAC controls the switching of DAC capacitors using a particular switching scheme. Several single-ended switching schemes for SAR ADC are reported in literature [138, 360, 361]. The single-ended merged capacitor switching (MCS) scheme proposed in [361] uses a three-level capacitive switching scheme having 50% reduction in the total capacitance value compared to [139]. This is preferable over other DAC switching schemes in terms of implementation, however at the cost of three reference voltages [0, $\frac{V_{ref}}{2}$, V_{ref}]. For simplicity, this work assumes off-chip reference voltages $\frac{V_{ref}}{2}$ and V_{ref}. However, on-chip low-power reference voltage generation is possible as presented in [362]. Using the framework of [361], we employed a "modified merged capacitor switching (MMCS)" scheme to design a single-ended SAR ADC. The proposed MMCS scheme halves the total number of unit capacitors compared to the single-ended SAR ADC [138, 360] and the traditional SAR ADC [139].

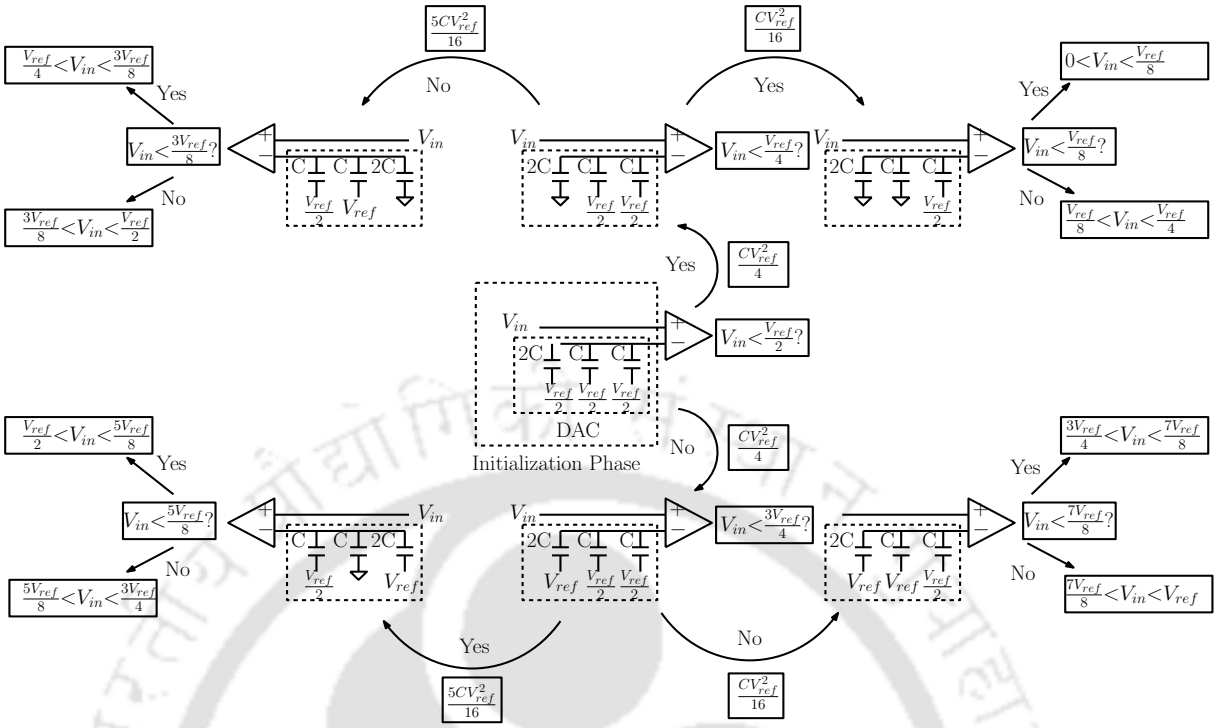


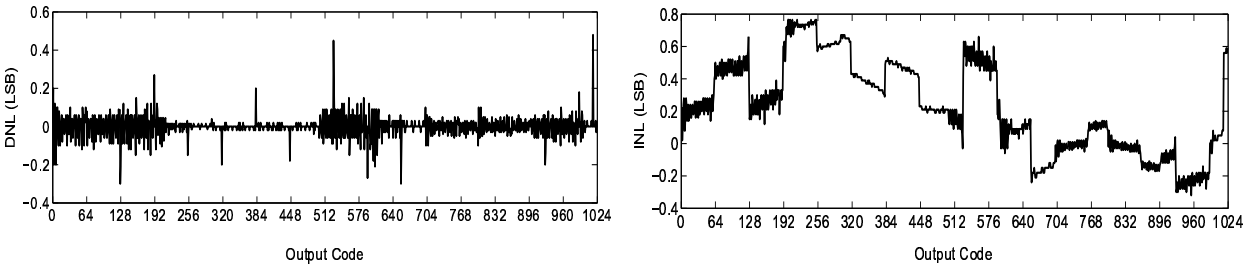
Figure 4.26: MMCS single-ended switching procedure for 3-bit SAR ADC; V_{ref}= V_{DD}= Reference Voltage

Table 4.4: Comparison of average switching energy for 10-bit single-ended SAR ADCs

Switching Method	Switching Energy ($C_0V_{ref}^2$)	Energy Savings (%)
Traditional [139]	681.65	0% (Reference)
Split Capacitor [360]	425.66	37.55%
Hu *et al.* [138]	84.7	87.57%
MCS [361]	84.7	87.57%
MMCS (This work)	84.7	87.57%

It uses the same number of unit capacitors employed in [361]. The proposed MMCS scheme results in two advantages: (a) it nullifies the requirement of sampling the input at the virtual node as the sampled output is directly available from the windowed integrator to ADC and further (b) there is no requirement of extra sampling switches thereby resulting in an overall reduction of DAC switches.

Fig. 4.26 illustrates the modifications in the proposed MMCS scheme, with an example of a 3-bit SAR ADC. The same procedure can be extended to the 10-bit capacitive reference DAC used in Fig. 4.24. Table 4.4 compares the average switching energy of different switching methods for 10-bit single-ended SAR ADCs. Although the MMCS single-ended switching scheme consumes the same switching energy as that in [138] and [361], nevertheless it simplifies the design of the controller using a counter-based SAR controller proposed here.



(a) (b)

Figure 4.27: DNL and INL of the proposed 10-bit single-ended SAR ADC

4.5.2.3 Counter-based SAR Controller

The controller in a SAR ADC consumes approximately upto 80% of the total power [363]. The asynchronous techniques presented in [364–371] reduce power consumption and improve speed at the cost of hardware complexity. The major drawback in an asynchronous ADC is that it requires an internal clock of $(N+2)f_s$, where f_s is the sampling frequency. This work presents a new counter-based synchronous controller that also works at $(N+2)f_s$ using a mod-12 counter, twelve 4-input NOR gates and a code-register with 10 S-R flip-flops– all at the same frequency of $12f_s$. The proposed controller does not require any startup circuitry to initialize the next digitizing cycle (a major advantage) unlike that in a N-bit shift-register based sequencer in traditional SAR ADC. In the proposed controller the EOC signal is generated by the mod-12 counter. The other advantage of the counter-based controller is that it uses only (N+2) NOR gates and $\lceil log_2 N \rceil$ flip-flops [vs.(N+2) FFs in a traditional SAR ADC [372, 373].

Fig. 4.27 shows the differential non-linearity (DNL) and the integral non-linearity (INL) of the proposed SAR ADC. The peak DNL and INL errors are within +0.48/-0.3 LSB and +0.76/-0.32 LSB repsectively. Table 4.5 summarizes the proposed SAR ADC with other state-of-the-art single-ended 10-bit SAR ADC designs in 180-nm CMOS technology. The proposed ADC attains better trade-off between power consumption, speed and operating supply voltage. This is the main challenge for WBAN transceiver design. The Walden figure-of-merit (FOM) [374] – a measure of energy efficiency – of the proposed single-ended SAR ADC is 134.3 fF/step. The FOM of the proposed technique and the FOMs of works reported by several researchers at 1.8 V supply voltage [369, 370, 375, 376] are listed in Table 4.5. It may be noted that the improvement in FOM can be achieved by lowering supply voltage which also results in drastic dynamic power reduction. However, in order to meet the requirements of

Table 4.5: Comparison Table with the state-of-the-art 10-bit single-ended SAR ADCs using 180-nm CMOS technology

References	Pipelined [369]	Pipelined [370]	SAR [375]	SAR [376]	This work
Comparator	-	Op-amp	Preamp-latch	Preamp-latch	Single-latch
ADC type	Differential	Differential	Single-ended	Single-ended	Single-ended
DAC type	BW—step[#]	BW—step[#]	CBW[*]	BW—step[#]	BW—step[#]
Technology	180-nm	180-nm	180-nm	180-nm	180-nm
Resolution	10-bit	10-bit	10-bit	10-bit	10-bit
Sampling Rate	50 MS/s	50 MS/s	0.46 MS/s	25 MS/s	15.625 MS/s
Supply Voltage	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V
Input Range	1	-	1.8	1.8	1.8
SNDR[§]	58.2 dB	56.04 dB	54.2 dB	54.01 dB[†]	56.6 dB
ENOB[‡]	9.4	9.02	8.7	8.68[†]	9.11
Power	9.9 mW	5 mW	0.021 mW	3.834 mW	1.16 mW
FOM= $\frac{P}{2^{ENOB} f_s}$ fF/step	300	192	110	374.4	134.3

[*]CBW: Cascaded Binary Weighted Capacitive DAC; [#]BW-step: Binary Weighted Step Capacitive DAC; [†]Calculated from reported results; [§]SNDR: Signal-to-noise + distortion ratio; [‡]ENOB: Effective number of bits

several other blocks discussed earlier that use a V_{DD}= 1.8 V, the proposed single-ended SAR ADC is also designed using V_{DD} or V_{ref} of 1.8 V.

4.5.3 Digital Back-end

The input to the digital back-end is the 10-bit digital representation of the samples of the received energy in the integration period of T_w (Fig. 4.2).

Demodulation of 2-ary symbol: We consider N_w= 32 energy samples in the symbol duration T_{sym}. The samples are partitioned into two subsets: E_1 and E_2 where E_1 contains the first sixteen samples and E_2 contains the last sixteen samples. For each 2-bit codeword (d_0, d_1) for the data symbol $b_0 \in \{0,1\}$ in Chapter 2: Table 2.2, the time-hopping sequence generator [2] generates two hopping positions H_0 and H_1 where H_i can take any one of the sixteen positions (from 0 to 15). H_0 indicates the hopping position in the first half of the symbol duration while H_1 indicates the hopping position in the second half of the symbol duration. Let E_{1,H_0} and E_{2,H_1} respectively represent the energy samples at H_0 and H_1 hopping position.

Define a decision metric:

$$M_{d_0 d_1} = (2d_0 - 1)E_{1,H_0} + (2d_1 - 1)E_{2,H_1} \tag{4.16}$$

If $M_{10} > M_{01}$, the 2-bit codeword is demodulated as '10' and hence the data symbol is '0'. Else, the 2-bit codeword is demodulated as '01' and the data symbol declared as '1'.

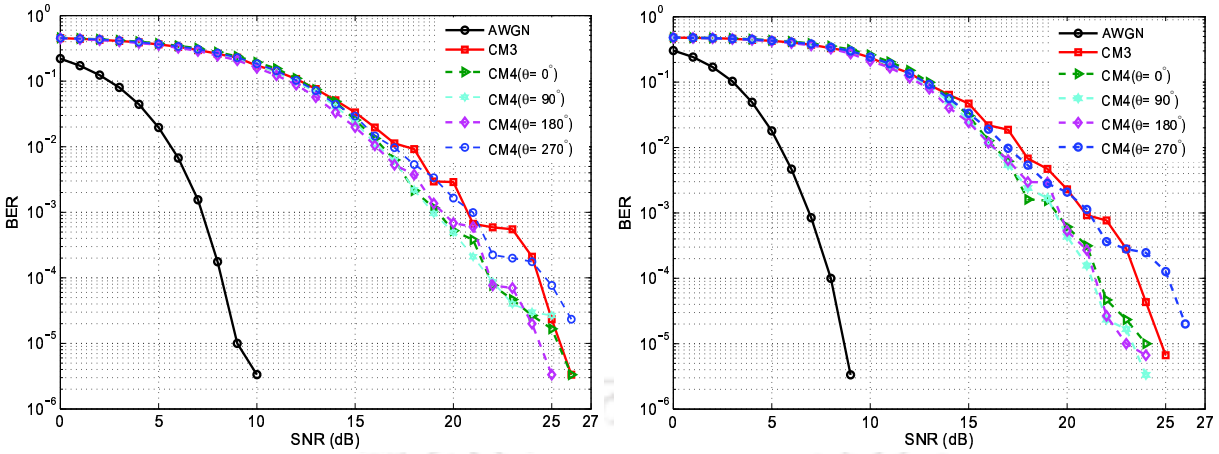


Figure 4.28: BER performance (post-layout simulations) of digital back-end under CM3 and CM4 channel models of digital back-end for (a) 2-ary PPM and (b) 16-ary PPM signaling

Demodulation of 16-ary symbol: We consider $4N_w$= 128 energy samples in the symbol duration $4T_{sym}$. The samples are partitioned into eight subsets: E_1, ..., E_8 where E_1 contains the first sixteen samples, E_2 contains the next sixteen samples and so on. For each 8-bit codeword for the data symbol $\{b_0, b_1, b_2, b_3\}$ in Chapter 2: Table 2.3, the time-hopping sequence generator [2] generates eight hopping positions H_0, ..., H_7 where H_i can take any one of the sixteen positions (from 0 to 15). Note that the symbol duration $4T_{sym}$ is divided into eight intervals each of duration $T_{sym}/2$ (Fig. 2.9(b)). Here H_i represent the hopping position in the $(i+1)^{th}$ interval where i $\in \{0, \ldots, 7\}$. Let E_{i+1,H_i} represent the energy sample at H_i in the $(i+1)^{th}$ interval.

Define a decision metric:

$$M_{d_0d_1d_2d_3d_4d_5d_6d_7} = \sum_{i=0}^{7}[(2d_i - 1)E_{i+1,H_i}] \tag{4.17}$$

The 4-bit data symbol corresponding to the maximum of the sixteen values of $M_{d_0d_1d_2d_3d_4d_5d_6d_7}$ is declared as the transmitted data symbol. For example, if $M_{10011001}$ is the maximum of the sixteen values, the 8-bit codeword is demodulated as '10011001' and the data symbol is declared as '1001' (Chapter 2: Table 2.3).

Fig. 4.28(a) shows the BER performance (post-layout simulations) of 2-ary PPM in CM3 and CM4 channel models (for four different body directions: θ=0°, 90°, 180°, 270°). Fig. 4.28(b) shows the BER performance (post-layout simulations) corresponding to 16-ary PPM in CM3 and CM4 channel models (for four different body directions: θ=0°, 90°, 180°, 270°). The power consumption in the 2-ary

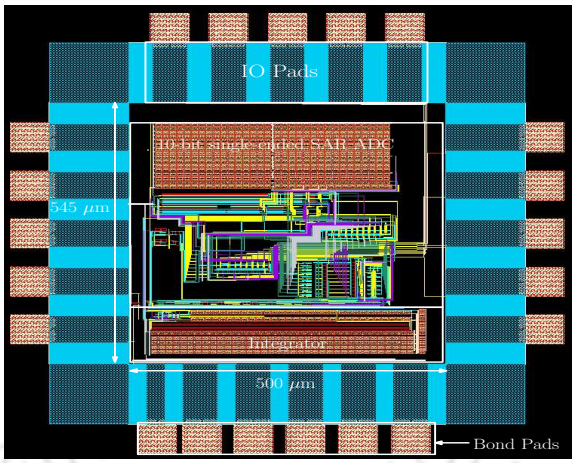


Figure 4.29: Layout of the mixed-signal demodulator (Integrator and SAR ADC)

Table 4.6: Summary of the proposed mixed-signal demodulator

Technology	180 nm
Supply	1.8 V
Active Die Size	500 μm $\times$ 545 μm
Modulation	PPM
Data Rate	0.487 Mbps
Pulse Bandwidth	500 MHz
Power Consumption†	1.25 mW

†Windowed Integrator and SAR ADC

and the 16-ary demodulators are found to be 85 μW and 215 μW respectively.

The proposed mixed-signal demodulator is implemented in 180 nm technology operating at 1.8 V supply. The layout of the proposed demodulator is shown in Fig. 4.29 and it occupies an active area of 500 μm $\times$ 545 μm. A summary of the proposed demodulator is given in Table 4.6.

4.6 Conclusions

An 802.15.6 compliant IR-UWB non-coherent energy-detection based receiver for BANs is designed. The "integrate-and-digitize" approach is adopted for the implementation of the receiver and this simplifies and reduces the implementation complexity. The RF front-end of the receiver is implemented using a single-to-differential LNA, a multi-stage RF amplifier (a cascade of multiple gain stages which are switchable to implement a step-wise variable gain stage) and followed by a single squarer. The output of the RF front-end (the square of the received signal) is passed through a windowed integrator that uses a new switching technique. The samples are digitized by a single-ended SAR ADC for generation of digitized samples. The proposed single-ended SAR ADC uses a modified

merged capacitor switching scheme for a capacitive reference DAC and works using a novel counter based SAR controller. Digital back-ends for demodulation of 2-ary and 16-ary PPM signaling are designed. The performance evaluation of the demodulators in different WBAN channels (CM3 and CM4 channels) has been carried out. The BER performance is found to be acceptable.

5

DAC Switching Technique for Single-Ended SAR ADCs

Contents

5.1 Introduction

The Non-coherent Energy Detection based Receiver described in Chapter 4 employs a single-ended SAR ADC (Section 4.5.2). SAR ADC is an attractive solution for signal acquisition in low-power portable and implantable devices [135–137] in BANs. This has rejuvenated research interests in designing low-power SAR ADCs having highly digital architecture and exploiting shrinking CMOS technologies. SAR ADCs have advanced towards achieving sampling rates from kS/s to hundreds of MS/s [136, 138, 360, 364, 375, 377]. Although differential input SAR ADC is a superior solution for low-level signal acquisition due to its ability to suppress common-mode noise, single-ended ADCs can nevertheless be a preferred solution especially when energy conservation is the over-riding concern and the SNR is at acceptable level. Further, common-mode output voltage variation in single-ended SAR ADCs can be mitigated by using a low-offset comparator [378] as shown in [138]. The capacitive reference DAC (Fig. 4.24(a) and Section 4.5.2.2) - employed in SAR ADC - contributes a significant portion to the total power consumption in SAR ADCs. The consumption of switching energy (during charging/discharging of the capacitive reference DAC) is the highest in the first few comparison cycles. Thus it is imperative to bring down the consumption of switching energy in the first few comparison cycles.

Several recent studies have been carried out for reduction of switching energy of single-ended SAR ADCs [138, 360, 361]. The split capacitor method [360] uses the method of recycling charge while the merged capacitor technique [361] employs merged capacitor switching resulting in switching energy reduction of 37.55% and 87.51% respectively as compared to conventional single-ended SAR ADC [139]. In [138], a pseudo-differential method is proposed. This method uses two DACs with a single reference voltage of $\frac{V_{ref}}{2}$ (rather than V_{ref}) to digitize an input voltage in the range of [0, V_{ref}] with the total capacitance value being the same as that in the traditional single-ended SAR ADC. One of the DACs (the top DAC) is essentially a "dummy" DAC–it merely mimics a differential operation. This technique results in zero switching energy consumption in the first comparison cycle, i.e., during the computation of the most-significant-bit (that incurs the maximum energy consumption in a traditional SAR ADC). In the proposed method, a similar technique is employed with two major differences: (a) top-plate sampling is used as opposed to bottom-plate sampling used in [138], (b) even in the second switching cycle, i.e., during the computation of (MSB-1), no switching energy is drawn from the supply voltage. The traditional technique [139] and the split capacitor technique [360] use

V_{ref} as the reference voltage for digitizing an input signal in the amplitude range of [0, V_{ref}]. The merged capacitor technique [361] uses two reference voltages V_{ref}, $\frac{V_{ref}}{2}$ while the technique in [138] uses only a single reference voltage $\frac{V_{ref}}{2}$ for digitizing an input signal within the amplitude range of [0, V_{ref}].

This work presents a new energy-efficient DAC switching technique which also uses a single reference voltage $\frac{V_{ref}}{2}$ similar to the method in [138] for digitizing an analog signal in the amplitude range of [0, V_{ref}]. This technique shows savings in switching energy of 92.21% over the traditional single-ended DAC switching technique.

The organization of the chapter is as follows. Section 5.2 discusses in details the proposed DAC switching technique. Section 5.3 gives a comparison with the existing state-of-the-art DAC switching techniques. The conclusions are drawn in Section 5.4.

5.2 Proposed DAC switching technique in N-bit Single-ended SAR ADCs

The differential SAR ADC uses a reference voltage of V_{ref} for digitizing an input analog signal within the range of [-V_{ref}, +V_{ref}]. In other words, in a differential SAR ADC, the absolute range of input signal voltage $2V_{ref}$ is twice the reference voltage V_{ref}. Analogously, the proposed single-ended SAR ADC uses a single reference voltage of $\frac{V_{ref}}{2}$ for digitizing an input signal of amplitude 2.$\frac{V_{ref}}{2}$, i.e., V_{ref}. The digitizing voltage $\frac{V_{ref}}{2}$ for generation of the MSB in a traditional single-ended SAR ADCs is based on binary-weighted capacitor array configuration using a single reference voltage V_{ref}. However, in the proposed SAR, the largest digitizing voltage $\frac{V_{ref}}{2}$ is the reference voltage itself. The remaining (N-1) digitizing voltages are also generated using $\frac{V_{ref}}{2}$ and appropriate DAC configurations.

Fig. 5.1 illustrates the proposed DAC switching technique for a 3-bit single ended SAR ADC. The reference voltage $\frac{V_{ref}}{2}$ and the input voltage V_{in} are sampled onto the top plates of the upper and the lower DACs, DAC1 and DAC2 respectively– each with 2^{N-1} unit capacitors resulting in a total of 2^N unit capacitors–the same as that in the traditional single-ended SAR ADCs. The bottom plates of the capacitors in both the DACs are connected to [0, $\frac{V_{ref}}{2}$, $\frac{V_{ref}}{2}$]. The top-plate sampling ensures zero-switching energy in the first switching cycle as shown in [361, 377, 379]. During the first comparison cycle, if $V_{in} < \frac{V_{ref}}{2}$, the bottom plates of DAC1 are switched to [0, 0, 0]. Otherwise, these are connected to $\frac{V_{ref}}{2}$. This, in turn, results in zero switching energy during the second switching cycle (i.e. after the first comparison) as shown in Fig. 5.1 and as explained below:

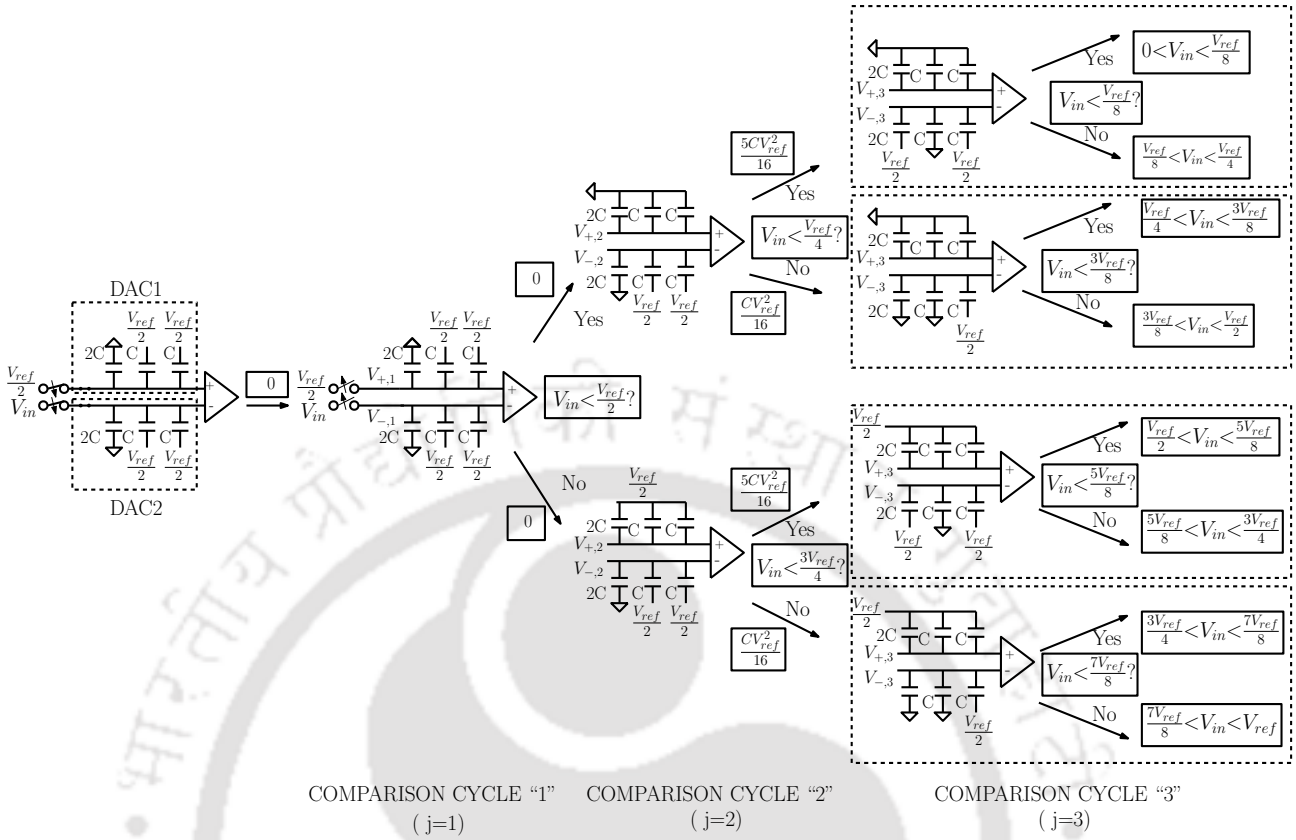


Figure 5.1: Proposed DAC Switching technique applied to a 3-bit single-ended SAR ADC

Using equation (21) of [375] and applying superposition theorem, the net switching energy incurred during j^{th} to $(j+1)^{th}$ comparison cycle may be computed as

$$E_{j\rightarrow j+1} = \sum_{i=1}^{N=3} \Big[C_i \Big\{ (V_{t,i} - V_{b,i}) - (V_{t,i+1} - V_{b,i+1}) \Big\} V_{b,i+1} \Big] \tag{5.1}$$

where $V_{t,i}$ and $V_{b,i}$ are the voltages at the top-plate and the bottom-plate of C_i with C_1= 2C, C_2= C_3= C, j$\in$ {1,2}.

Comparison Cycle "1" (j= 1):

(a) When $V_{in}<\frac{V_{ref}}{2}$, the switching energy may be computed as

$$\begin{aligned} E_{1\rightarrow 2} = \Big[2C. \Big\{ (V_{+,1} - 0) - (V_{+,2} - 0) \Big\}.0 \; + C. \Big\{ (V_{+,1} - \frac{V_{ref}}{2}) - (V_{+,2} - 0) \Big\}.0 \\ + C. \Big\{ (V_{+,1} - \frac{V_{ref}}{2}) - (V_{+,2} - 0) \Big\}.0 \Big] = 0 \end{aligned} \tag{5.2}$$

(b) When $V_{in}>\frac{V_{ref}}{2}$, the switching energy is

$$E_{1\to2} = \Big[2C.\Big\{(V_{+,1}-0)-(V_{+,2}-\frac{V_{ref}}{2})\Big\}.\frac{V_{ref}}{2} + C.\Big\{(V_{+,1}-\frac{V_{ref}}{2})-(V_{+,2}-\frac{V_{ref}}{2})\Big\}.\frac{V_{ref}}{2} + C.\Big\{(V_{+,1}-\frac{V_{ref}}{2})-(V_{+,2}-\frac{V_{ref}}{2})\Big\}.\frac{V_{ref}}{2}\Big] = 0 \tag{5.3}$$

Thus, the switching energy in the second switching cycle (i.e., after the first comparison) is zero. In contrast the method proposed in [138] exhibits a non-zero switching energy as verified below:

(a) For $V_{in}<\frac{V_{ref}}{2}$ using (5.1), the switching energy is

$$E_{1\to2} = 2C.(V_{-,1}-V_{-,2}).\frac{V_{ref}}{2} = \frac{CV_{ref}^2}{4} \neq 0 \tag{5.4}$$

(b) For $V_{in}>\frac{V_{ref}}{2}$, the switching energy is

$$E_{1\to2} = 4C.(V_{+,1}-\frac{V_{ref}}{2}-V_{+,2}).0 + 2C.(V_{-,1}-V_{-,2}).\frac{V_{ref}}{2} = \frac{CV_{ref}^2}{4} \neq 0 \tag{5.5}$$

Comparison Cycle "2" (j= 2):

(a) For $V_{in}<\frac{V_{ref}}{4}$, the switching energy is

$$E_{2\to3} = \{3C.(V_{-,2}-V_{-,3}) + 2C.\frac{V_{ref}}{2}\}.\frac{V_{ref}}{2} = \frac{5CV_{ref}^2}{16} \tag{5.6}$$

(b) For $V_{in}>\frac{V_{ref}}{4}$, the switching energy is

$$E_{2\to3} = C.(V_{-,2}-V_{-,3}).\frac{V_{ref}}{2} = \frac{CV_{ref}^2}{16} \tag{5.7}$$

(c) For $V_{in}<\frac{3V_{ref}}{4}$, the switching energy is

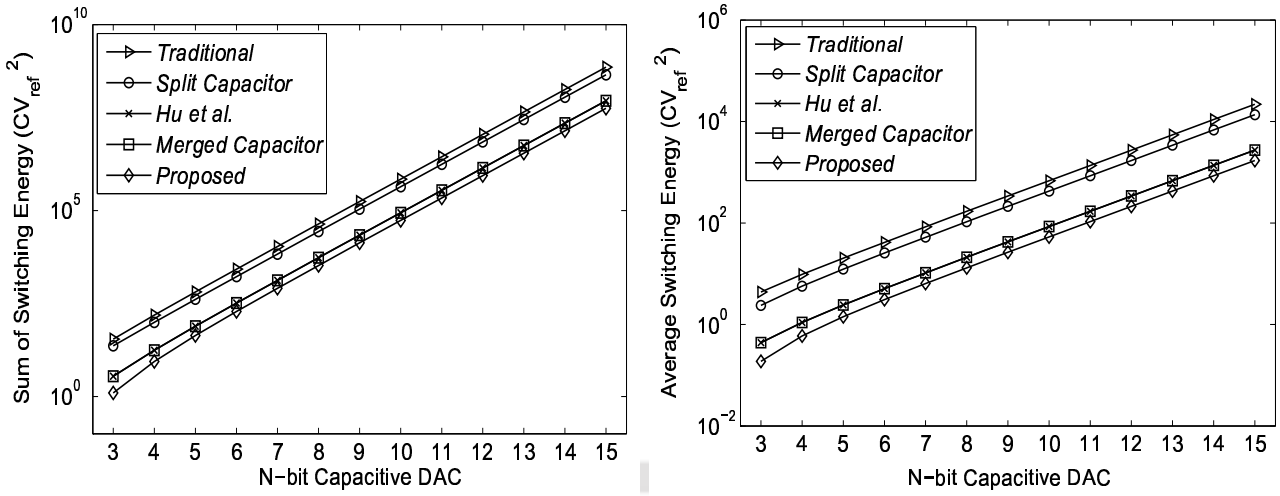
$$E_{2\to3} = \{3C.(V_{-,2}-V_{-,3}) + 2C.\frac{V_{ref}}{2}\}.\frac{V_{ref}}{2} = \frac{5CV_{ref}^2}{16} \tag{5.8}$$

(d) For $V_{in}>\frac{3V_{ref}}{4}$, the switching energy is

$$E_{2\to3} = C.(V_{-,2}-V_{-,3}).\frac{V_{ref}}{2} = \frac{CV_{ref}^2}{16} \tag{5.9}$$

5.3 Comparison with state-of-the-art DAC switching techniques

The behavioral simulation of different DAC switching techniques for an N-bit single-ended SAR ADC is performed in MATLAB and the switching energies are compared with that of the proposed



(a) (b)

Figure 5.2: (a) Sum of switching energy comparison and (b) average switching energy comparison over all output codes in an N-bit single-ended SAR ADC

Table 5.1: Comparison of sum of switching energy with reported 10-bit single-ended SAR ADCs

Switching Methods	Sum of switching energy (CV_{ref}^2)	Energy Savings (%)
Traditional differential [380]	1352873	-
Traditional single-ended [139]	698027	0% (Reference)
Split Capacitor [360]	436395	37.48%
Merged capacitor [361]	87126	87.51%
Hu *et al.* [138]	87126	87.51%
This work	54294	92.21%

technique.

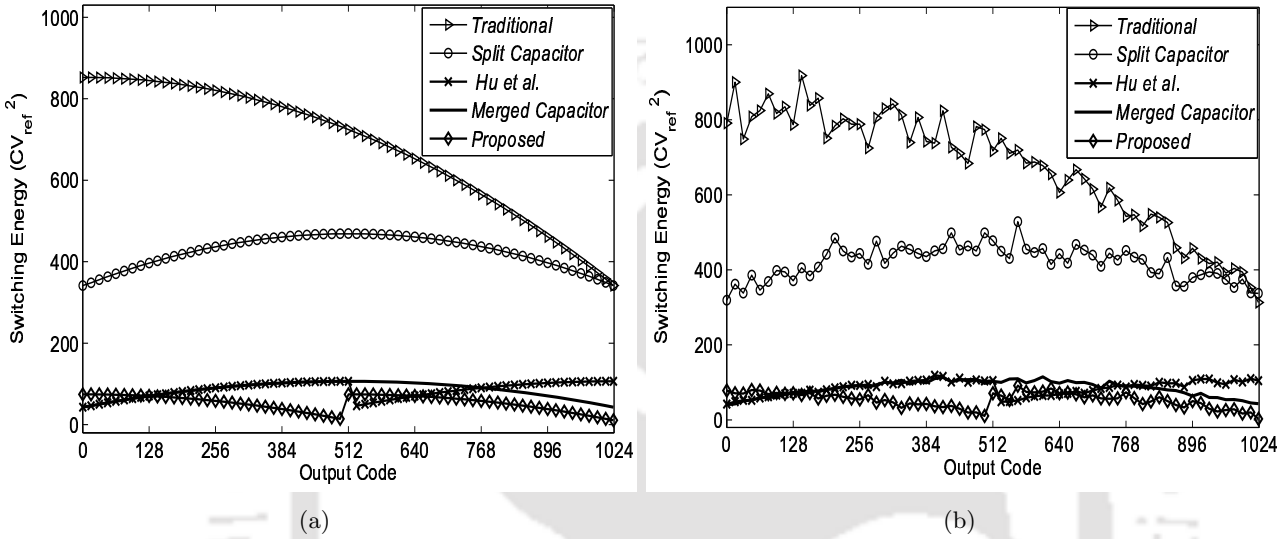
The sum of switching energies in the proposed DAC switching technique over all output codes for an N-bit single-ended SAR ADC is shown in Fig. 5.2(a) and compared with the reported techniques [138, 139, 360, 361]. Table 5.1 shows the sum of switching energy values of various DAC switching techniques [138, 139, 360, 361] for a 10-bit single ended SAR ADC. The average switching energy of the proposed switching technique for an N-bit capacitive DAC can be expressed as

$$E_{avg(proposed)} = \sum_{i=2}^{N-1} 2^{N-2i-3}(2^i - 1)CV_{ref}^2 \tag{5.10}$$

Fig. 5.2(b) shows the average switching energies over all output codes of the proposed technique in comparison to [138,139,360,361] for an N-bit single-ended SAR ADC. Table 5.2 shows the average switching energy values of various DAC switching techniques [138, 139, 360, 361] for a 10-bit single ended SAR ADC. Thus, there is 92.21% reduction in switching energy in the proposed switching

Table 5.2: Comparison of average switching energy with reported 10-bit single-ended SAR ADCs

Switching Methods	Switching Energy (CV_{ref}^2)	Energy Savings (%)
Traditional differential [380]	1363.3	-
Traditional single-ended [139]	681.65	0% (Reference)
Split Capacitor [360]	425.66	37.55%
Merged capacitor [361]	84.7	87.57%
Hu *et al.* [138]	84.7	87.57%
This work	53.08	92.21%



(a) (b)

Figure 5.3: Switching energy comparison for a 10-bit single ended SAR ADC with (a) Ideal capacitor (b) Non-ideal capacitor

technique in comparison to the traditional single-ended SAR ADC. Further, as compared to the result in [138], this corresponds to a reduction by an amount of $32CV_{ref}^2$, equivalent to a reduction by 37.6%.

The switching energy in the proposed DAC switching technique over all output codes for a 10-bit single-ended SAR ADC is shown in Fig. 5.3(a) and compared with the reported switching techniques [138,139,360,361]. Moreover, the non-idealities of the capacitors in DAC have an effect on the switching energy over all output codes; since the switching energy is directly proportional to the unit capacitor 'C'. Fig. 5.3(b) shows the switching energy over all output codes for a 10-bit single-ended SAR ADC taking these into account. Simulations are based on the assumption that the unit capacitor 'C' follows the Gaussian distribution having the standard deviation of 1%.

5.4 Conclusions

An energy-efficient capacitive reference DAC switching technique for a 10-bit single-ended SAR ADC is presented. The proposed DAC switching technique exhibits 92.21% savings in switching energy in comparison to the traditional DAC switching technique. Unlike the methods that use two reference voltages of V_{ref} and $\frac{V_{ref}}{2}$ or a single reference voltage V_{ref}, the proposed switching technique uses only a single reference voltage of $\frac{V_{ref}}{2}$ for digitizing an input signal within the amplitude range of [0, V_{ref}].

6

Design Methodology for Event-driven PWLA Waveform Generator

Contents

6.1 Introduction

The shape of a pulse is of utmost importance to an IR-UWB transceiver system as it dictates the frequency spectrum of the transmitted signal. In other words, the generation of such pulse shape is required to acquire the accurate frequency characteristics. It is necessary to design an IR-UWB pulse generator, a key component of the transmitter, that provides an accurate pulse shape and follows the mandatory FCC spectral mask [3].

IR-UWB pulse generation can be classified into two categories. The first category generates the IR-UWB pulse which directly falls in the 3.1-10.6 GHz frequency band without the need of frequency translation (up-conversion). In the second category, the pulse is generated at the baseband followed by an up-conversion (using a LC oscillator and a mixer). Most of the IR-UWB pulse generation topologies employ one of the following techniques: (i) LC oscillator-switching technique [273, 381–383] (ii) filter-excitation technique [384] (iii) digital pulse-shaping technique [385–389] (iv) edge-combination techniques [335,390–394] (v) on-chip/off-chip band-pass filtering technique [395,396]. The pulse generation technique presented in [397] employs an accurate approximation of a Gaussian pulse by exploiting the exponential behavior of a BJT. The pulse generator presented in [389] employed a triangular pulse generation technique to generate a Gaussian pulse and a first-derivative Gaussian pulse.

In Chapter 3, a method for generation of a SRRC signaling pulse by an N-segment piece-wise linear approximation (PWLA) approach was presented. The fundamental assumption in the PWLA approach is that the duration of each line segment is a multiple of some basic time period T that is related to the System Clock – thereby facilitating a simple clock-driven state-machine controller. However, in the most general case, duration of a line segment need not be related to the system clock in a simple manner (i.e. a multiple of some basic clock period T). While the zero-crossings of a SRRC pulse are indeed multiples of some T, the extrema (the maxima and the minima) are not.

The constraint on the time duration of a segment can be circumvented if the controller can be made “event-driven” with the “events” designed to occur at the “desired time instants”. Such an event-driven state machine will permit accurate approximation of a waveform (to any desired degree of accuracy subject to complexity and cost) as compared to that achievable by a simple clock-driven controller. This work presents an event-driven PWLA methodology for an accurate approximation of an arbitrary signaling waveform.

The organization of the chapter is as follows. Section 6.2 illustrates the event-driven PWLA

approach and describes the methodology for generation of an arbitrary signaling waveform. Section 6.3 describes six different approximations of the 15.6-compliant SRRC pulse. Their performance in terms of percentage relative error, cross-correlation, power-spectral density and implementation complexity are compared in Section 6.4. Section 6.5 presents a comparison of the "best-fit" clock-driven SRRC PWLA waveform approximation (in Chapter 3) and the "best-fit" event-driven SRRC PWLA waveform approximation. Section 6.6 presents the implementation methodology of a "best-fit" event-driven PWLA SRRC pulse generator. Using the event-driven PWLA approach, the generation of the "closest-fit" N-segment Gaussian pulse and its derivatives (first-, third- and fifth-derivatives of the Gaussian pulse) is also presented in Section 6.7. The conclusions are drawn in Section 6.8.

6.2 Event-Driven PWLA Approach for generation of Arbitrary Signaling Waveform

Consider an arbitrary waveform p(t) to be approximated. Let $\tilde{p}$(t) be the N-segment piecewise linear approximated waveform as shown in Fig. 6.1. The approximated waveform $\tilde{p}$(t) can be expressed as:

$$\tilde{p}(t) = \sum_{i=1}^{N} s_i(t) \tag{6.1}$$

where

$$s_i(t) = \begin{cases} v_{init} + \underbrace{\left(\dfrac{v_i - v_{init}}{t_i - t_{init}}\right)}_{slope_i}(t - t_{init}), & i = 1 \\ v_{i-1} + \underbrace{\left(\dfrac{v_i - v_{i-1}}{t_i - t_{i-1}}\right)}_{slope_i}(t - t_{i-1}), & i = 2, 3, \ldots, N \end{cases} \tag{6.2}$$

Here, v_{init}: initial voltage at time t_{init} and v_i: voltage breakpoint at time t_i.

The breakpoint of each line segment (Fig. 6.1) is realized by a comparator with appropriate reference voltage (known-a-priori) switched-in through a multiplexer controlled by select lines ($trig_1$, $trig_2$, ..., $trig_7$) generated by an event-driven controller. As time proceeds, a set of events {$sig_{1\to0}$ and $sig_{0\to1}$} are generated at the desired breakpoints by an event generation block, which in turn, drives the event-driven controller. This controller generates the control signals sig_1, sig_2, ..., sig_{m+n-1}, sig_{m+n} that drives the PWLA waveform generator (Chapter 3: Fig. 3.2) to realize the approximated waveform $\tilde{p}$(t).

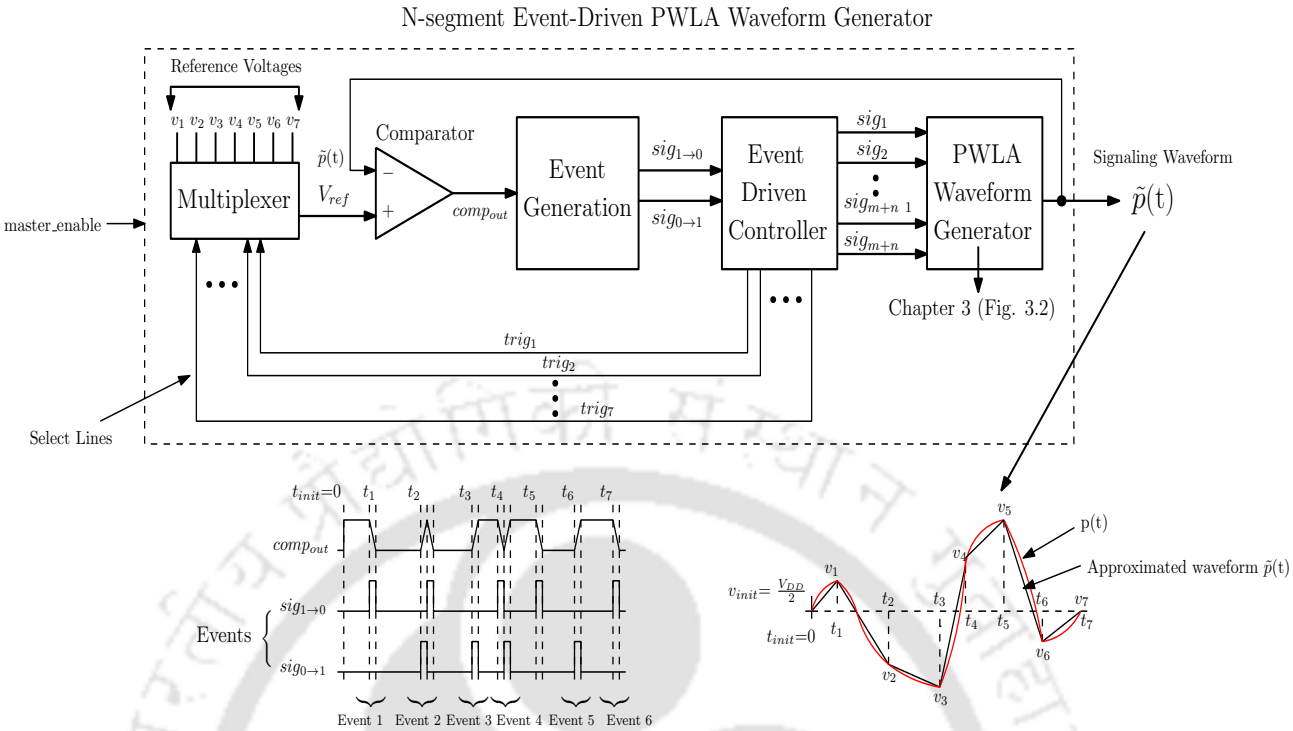


Figure 6.1: (N= m+n) – segment Event-Driven PWLA Waveform Generator

6.3 Event-Driven Approximations of N-segment PWLA SRRC Pulse Generation

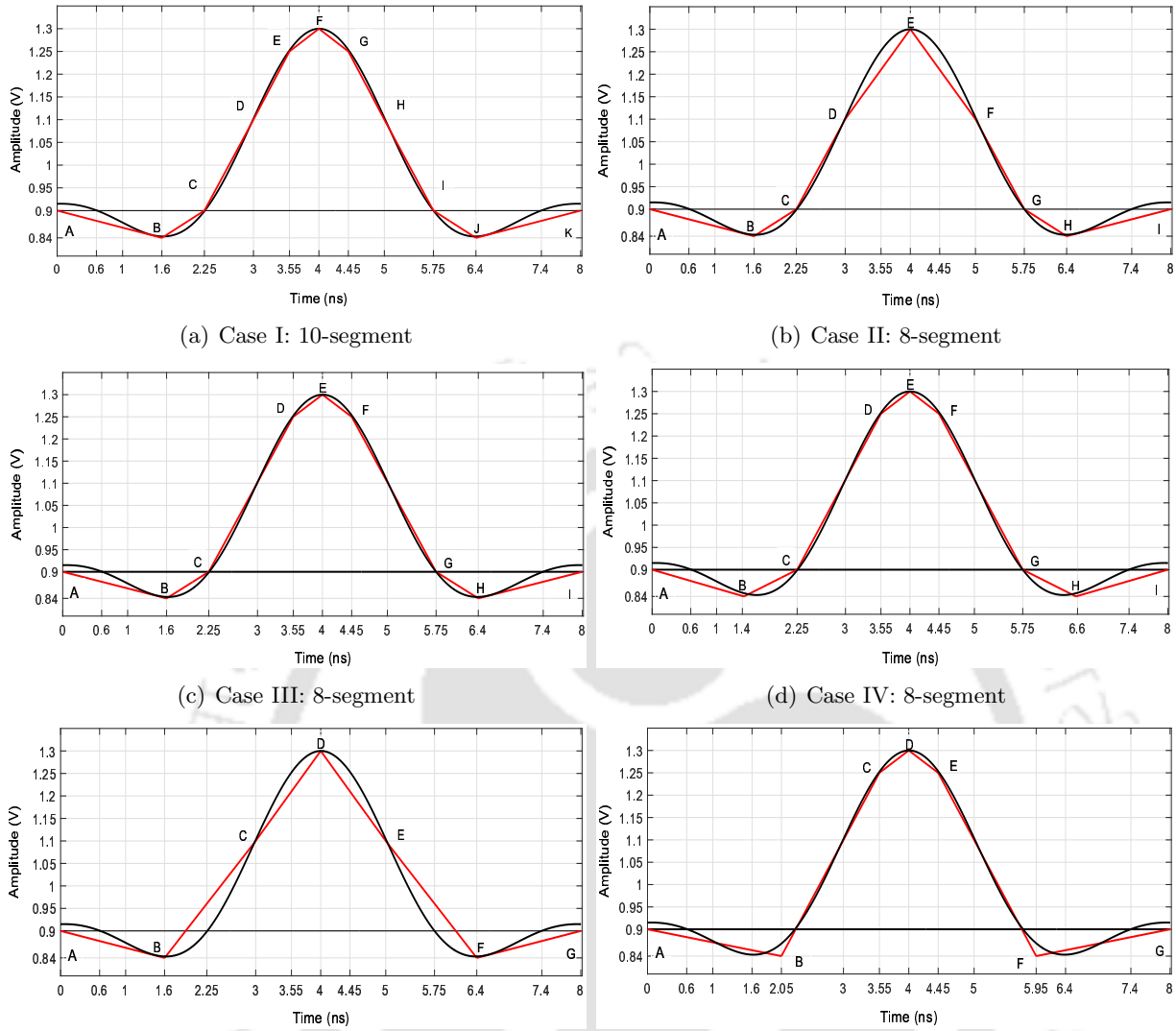
The event-driven PWLA approximations of the SRRC pulse given by (2.6) is considered for six cases. A detailed description is given in the following.

6.3.1 Case-I: 10-segment PWLA SRRC Pulse

The Case-I PWLA pulse approximating the actual SRRC pulse is shown in Fig. 6.2(a). The ten-segments are generated by switching five positive current sources I_1, I_2, I_3, I_4, I_5 and five negative current sources -I_1, -I_2, -I_3, -I_4, -I_5 (Appendix C: Table C.1) activated by the event-driven control signals sig_1, sig_2, sig_3, sig_4, sig_5, sig_6, sig_7, sig_8, sig_9 and sig_{10} as illustrated in Fig. 6.3.

6.3.2 Case-II: 8-segment PWLA SRRC Pulse

An eight-segment Case-II PWLA SRRC pulse (Fig. 6.2(b)) can be generated by switching four positive current sources I_1, I_2, I_3, I_4 and four negative current sources -I_1, -I_2, -I_3, -I_4 (Appendix C: Table C.2) that are switched into the charge/discharge of the capacitor 'C' by the event-driven control signals sig_1, sig_2, sig_3, sig_4, sig_5, sig_6, sig_7 and sig_8 at appropriate instants (Fig. 6.4).



(a) Case I: 10-segment

(b) Case II: 8-segment

(c) Case III: 8-segment

(d) Case IV: 8-segment

(e) Case V: 6-segment

(f) Case VI: 6-segment

Figure 6.2: (a) Case-I: 10-segment (b) Case-II: 8-segment (c) Case-III: 8-segment (d) Case-IV: 8-segment (e) Case-V: 6-segment and (f) Case-VI: 6-segment PWLA SRRC pulse approximating SRRC pulse (Equation (2.6))

6.3.3 Case-III: 8 segment PWLA SRRC Pulse

This eight-segment Case-III PWLA pulse (Fig. 6.2(c)) is generated by switching four positive current sources I_1, I_2, I_3, I_4 and four negative current sources -I_1, -I_2, -I_3, -I_4 (Appendix C: Table C.3) activated by the event-driven control signals sig_1, sig_2, sig_3, sig_4, sig_5, sig_6, sig_7 and sig_8 as illustrated in Fig. 6.5.

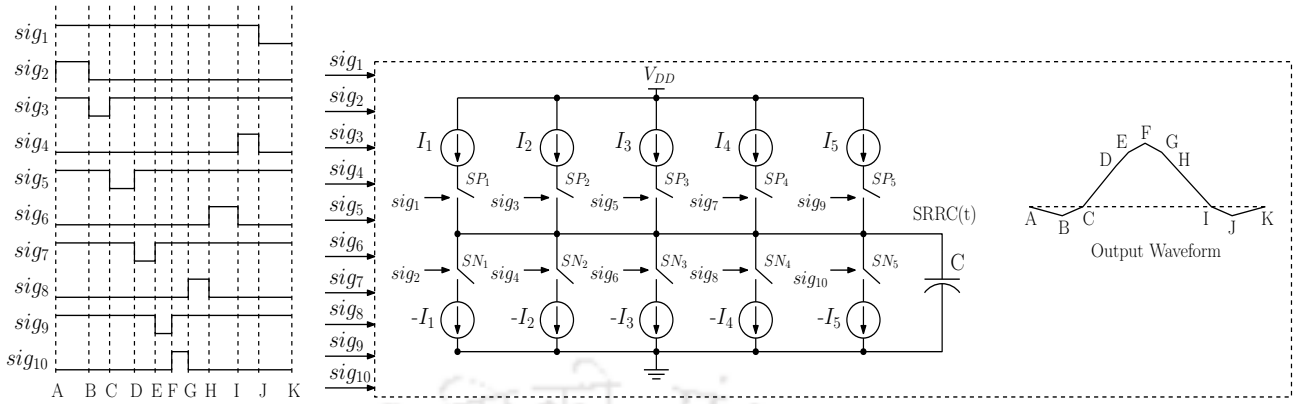


Figure 6.3: Case-I: 10-segment PWLA SRRC Pulse Generator

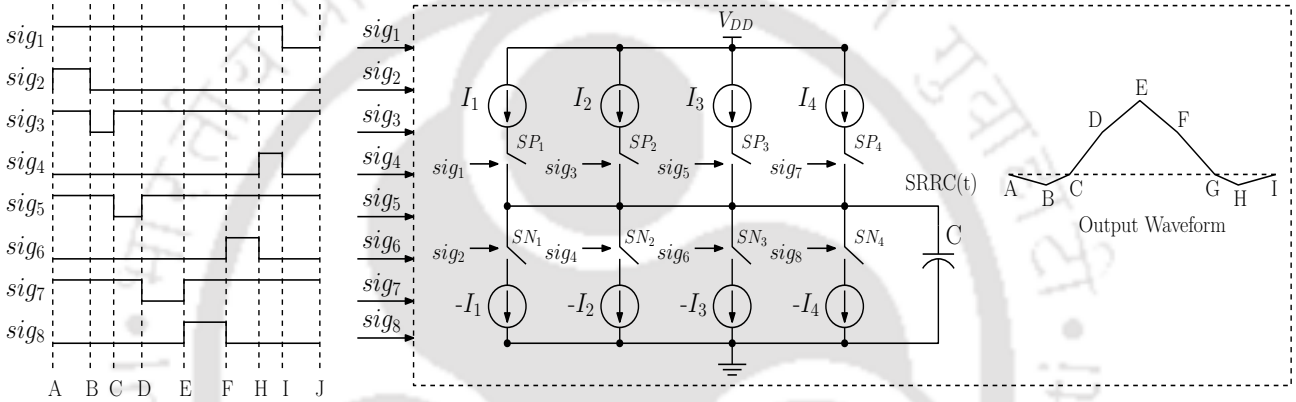


Figure 6.4: Case-II: 8-segment PWLA SRRC Pulse Generator

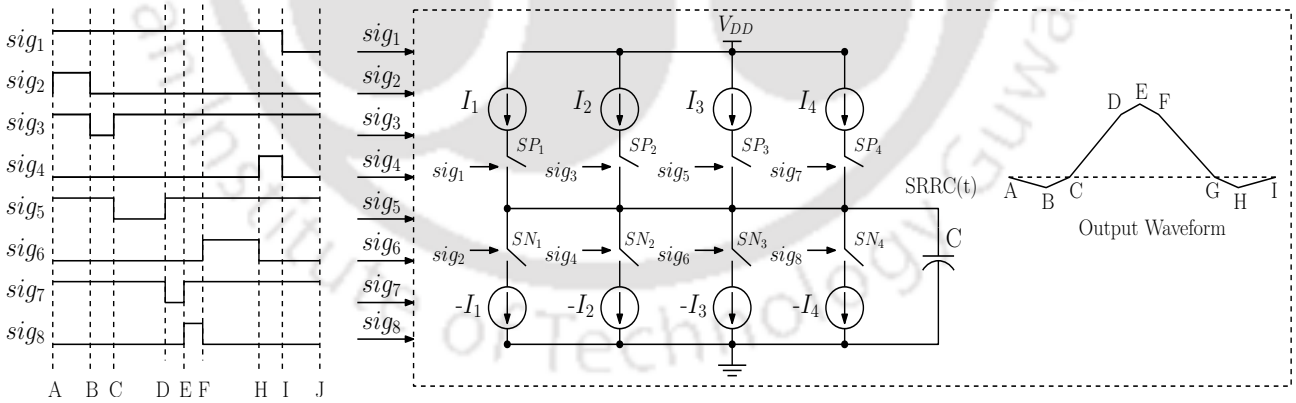


Figure 6.5: Case-III: 8-segment PWLA SRRC Pulse Generator

6.3.4 Case-IV: 8-segment PWLA SRRC Pulse

The Case-IV PWLA pulse (Fig. 6.2(d)) of eight-segments can be generated by using four positive current sources I_1, I_2, I_3, I_4 and four negative current sources -I_1, -I_2, -I_3, -I_4 (Appendix C: Table C.4) activated by the event-driven control signals sig_1, sig_2, sig_3, sig_4, sig_5, sig_6, sig_7 and sig_8 as

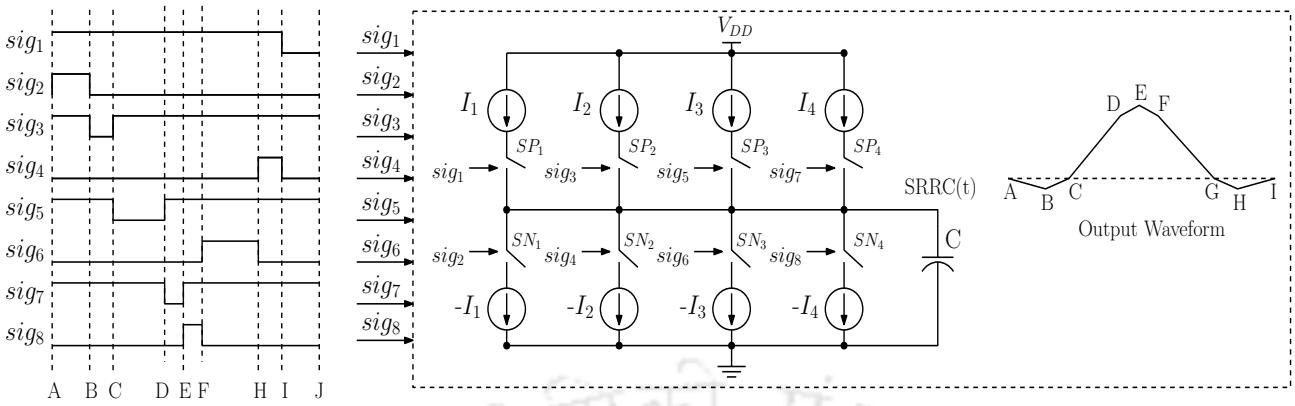


Figure 6.6: Case-IV: 8-segment PWLA SRRC Pulse Generator

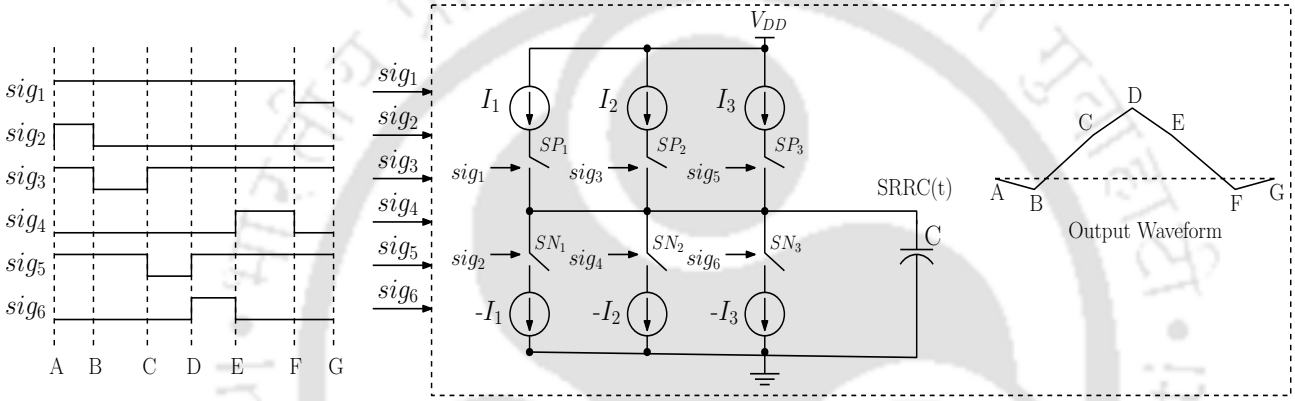


Figure 6.7: Case-V: 6-segment PWLA SRRC Pulse Generator

illustrated in Fig. 6.6.

6.3.5 Case-V: 6-segment PWLA SRRC Pulse

The Case-V PWLA SRRC pulse as shown in Fig. 6.2(e) can be generated by switching three positive current sources I_1, I_2, I_3 and three negative current sources -I_1, -I_2, -I_3 (Appendix C: Table C.5). The current sources are controlled by the switching signals sig_1, sig_2, sig_3, sig_4, sig_5 and sig_6 as illustrated in Fig. 6.7.

6.3.6 Case-VI: 6-segment PWLA SRRC Pulse

A six-segment Case-VI PWLA SRRC pulse as shown in Fig. 6.2(f) can be generated by three positive current sources I_1, I_2, I_3 and three negative current sources -I_1, -I_2, -I_3 (Appendix C: Table C.6) that are switched by the event-driven control signals sig_1, sig_2, sig_3, sig_4, sig_5 and sig_6 (Fig. 6.8).

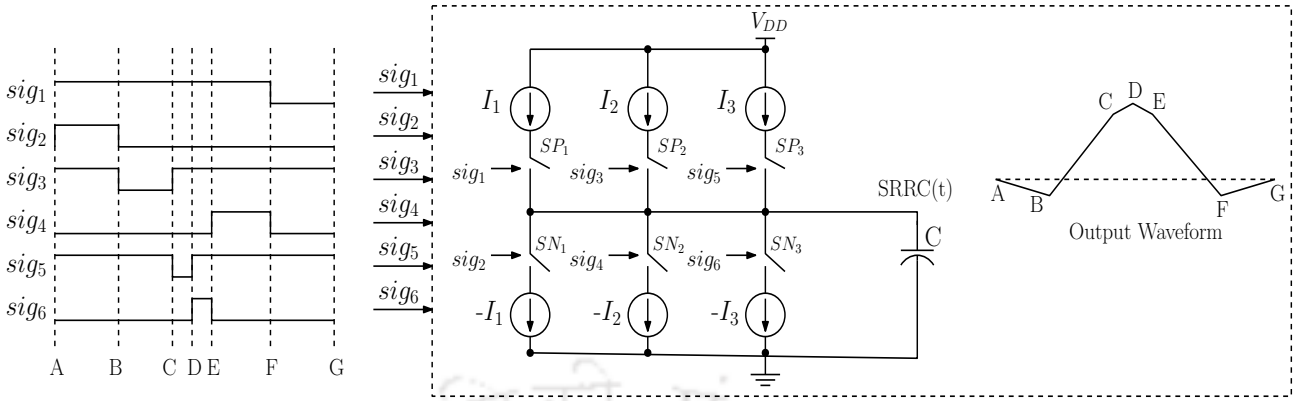
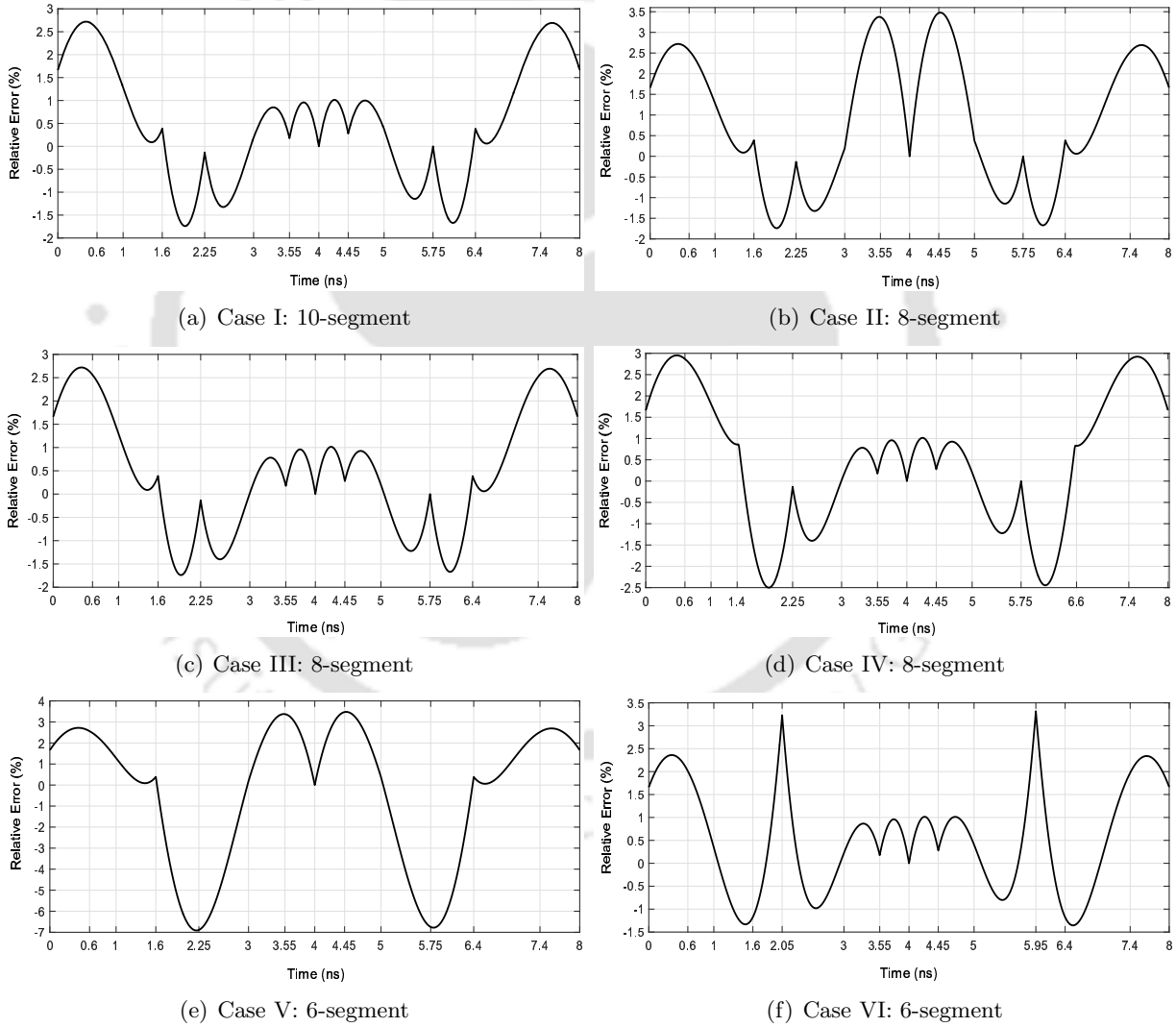


Figure 6.8: Case-VI: 6-segment PWLA SRRC Pulse Generator



(a) Case I: 10-segment

(b) Case II: 8-segment

(c) Case III: 8-segment

(d) Case IV: 8-segment

(e) Case V: 6-segment

(f) Case VI: 6-segment

Figure 6.9: The percentage relative error of (a) Case-I: 10-segment (b) Case-II: 8-segment (c) Case-III: 8-segment (d) Case-IV: 8-segment (e) Case-V: 6-segment and (f) Case-VI: 6-segment PWLA SRRC pulse

6.4 Evaluation of the "best-fit" event-driven PWLA SRRC pulse generation

Table 6.1: Percentage Relative Error of event-driven PWLA SRRC Pulse

Different PWLA Approximations	Percentage Relative Error
Case-I: 10-segment	+3% to -2%
Case-II: 8-segment	+3.5% to -2%
Case-III: 8-segment	+3% to -2%
Case-IV: 8-segment	+3% to -2.5%
Case-V: 6-segment	+4% to -7%
Case-VI: 6-segment	+3.5% to -1.5%

Table 6.2: Normalized Cross-correlation of event-driven PWLA SRRC Pulse

Different PWLA Approximations	Normalized Cross-correlation
Case-I: 10-segment	0.979
Case-II: 8-segment	0.924
Case-III: 8-segment	0.981
Case-IV: 8-segment	0.980
Case-V: 6-segment	0.931
Case-VI: 6-segment	0.978

Table 6.3: No. of current sources required for event-driven PWLA SRRC Pulse

Different PWLA Approximations	No. of Current Sources	
	Positive	Negative
Case-I: 10-segment	5	5
Case-II: 8-segment	4	4
Case-III: 8-segment	4	4
Case-IV: 8-segment	4	4
Case-V: 6-segment	3	3
Case-VI: 6-segment	3	3

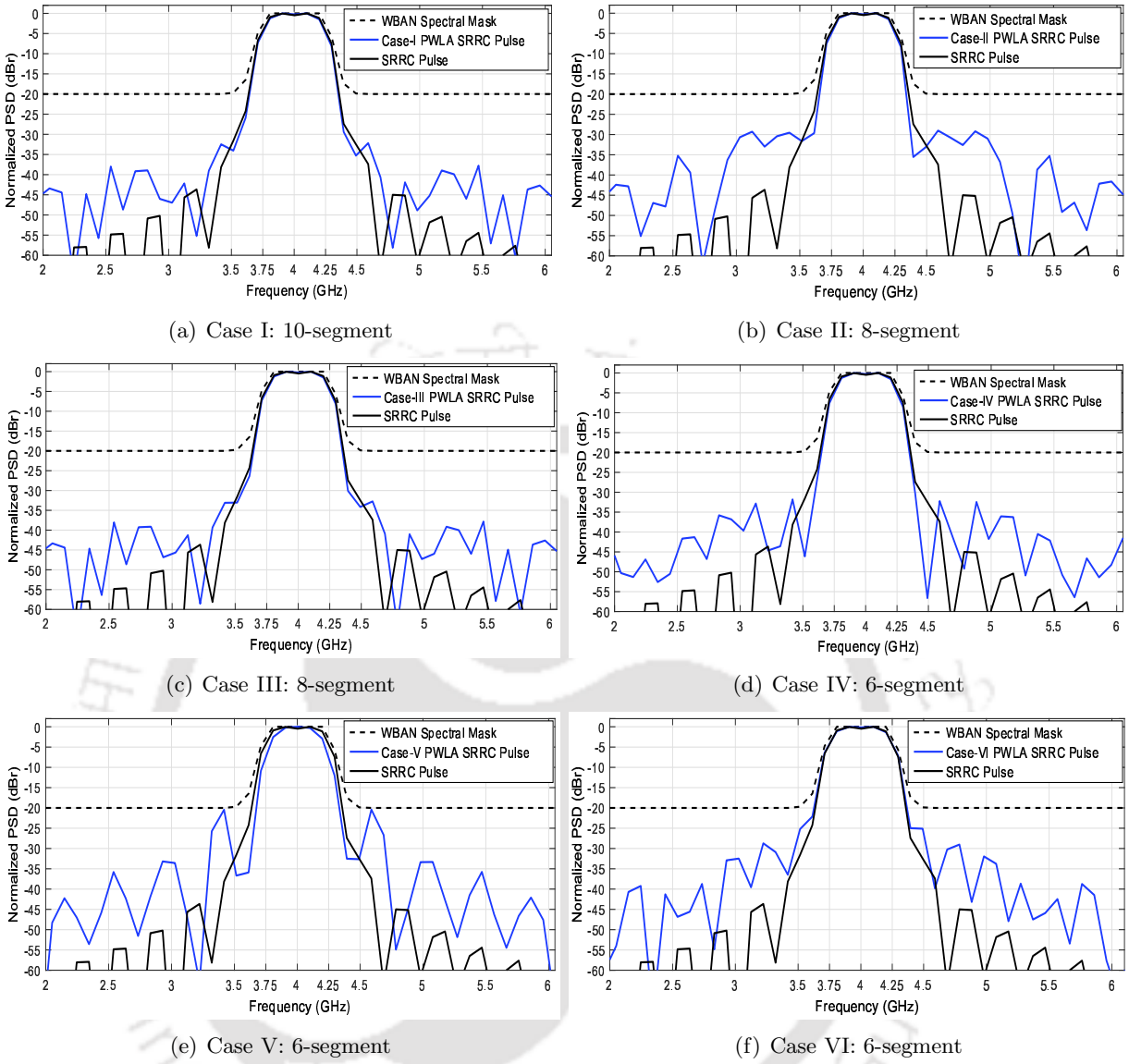
The "best-fit" among the six cases of event-driven PWLA SRRC pulse generation are evaluated in terms of percentage relative error, cross-correlation, the number of current sources and PSD:

6.4.1 Percentage Relative Error

The percentage relative error of different event-driven PWLA SRRC pulse approximations with respect to the SRRC pulse is shown in Fig. 6.9. Table 6.1 shows the percentage relative error in the six cases.

6.4.2 Cross-correlation

Table 6.2 shows the normalized cross-correlation of various event-driven PWLA approximations with the SRRC pulse.



(a) Case I: 10-segment (b) Case II: 8-segment

(c) Case III: 8-segment (d) Case IV: 6-segment

(e) Case V: 6-segment (f) Case VI: 6-segment

Figure 6.10: PSDs of (a) Case-I: 10-segment (b) Case-II: 8-segment (c) Case-III: 8-segment (d) Case-IV: 8-segment (e) Case-V: 6-segment and (f) Case-VI: 6-segment PWLA SRRC pulse

6.4.3 No. of Current Sources

Table 6.3 shows the number of current sources required for the generation of the PWLA SRRC approximations.

6.4.4 PSD

The normalized PSDs of the six different approximations with respect to the WBAN spectral mask are shown in Fig. 6.10. It is clear from Fig. 6.10(a) and Fig. 6.10(c) that the PSDs in the Case-I:

10-segment and the Case-III: 8-segment PWLA approximations closely fit the PSDs of the SRRC pulse and the WBAN spectral mask. Further, even by increasing the PWLA segments from eight (Case-III) to ten (Case-I), the PSDs are more or less invariant in the main lobe and are well within the WBAN spectral mask in the side lobes. The Case-V: 6-segment PWLA SRRC pulse shows the worst PSD among the six approximations (Fig. 6.10(e)). Further, the PSDs in Case-II, Case-IV and Case-VI approximations fit the WBAN spectral mask fairly well in the main lobe, however, the values are not low enough in the side lobes (Fig. 6.10(b), Fig. 6.10(d) and Fig. 6.10(f)).

Thus, it may be concluded that the Case-III: 8-segment approximation is the best choice in terms of performance and implementation complexity.

6.5 Comparison of the "best-fit" Clock-driven and the "best-fit" Event-Driven PWLA SRRC Pulse Approximations

The comparison of efficacy between the "best-fit" clock-driven and the "best-fit" event-driven PWLA SRRC pulse approximations are evaluated in terms of cross-correlation and PSDs.

Table 6.4 shows the normalized cross-correlation of the "best-fit" clock-driven (6- and 8-segment) and the "best-fit" event-driven (Case-VI: 6-segment and Case-III: 8-segment) PWLA SRRC pulse approximations.

It may be observed from Fig. 6.11 that the event-driven (Case VI: 6-segment) PWLA SRRC pulse approximation closely fits the PSDs of the SRRC pulse and the WBAN spectral mask as compared to the clock-driven (6-segment) PWLA SRRC pulse approximation. Further, by increasing the no. of segments from six to eight, the PSD of the event-driven (Case-III: 8-segment) fits the WBAN spectral mask very well in the main lobes as compared to the clock-driven (8-segment) PWLA SRRC pulse as shown in Fig. 6.12.

Thus, it can be concluded that the event-driven PWLA approximations has higher potential to approximate a desired pulse with a high degree of accuracy as compared to the clock-driven PWLA approximations.

6.6 Implementation Methodology for Case-III: 8-segment PWLA SRRC Pulse Generator

As a proof of concept, a design procedure for the generation of the control signals sig_1, sig_2, sig_3, sig_4, sig_5, sig_6, sig_7 and sig_8 for the Case-III: 8-segment PWLA SRRC pulse generator (Fig. 6.5) is

Table 6.4: Normalized Cross-correlation of the "best-fit" clock-driven and event-driven PWLA SRRC Pulse

Sl. No.	PWLA Approximations	Normalized Cross-correlation
1	Clock-Driven (6-segment)	0.927
	Event-Driven (Case-VI: 6-segment)	0.978
2	Clock-Driven (8-segment)	0.971
	Event-Driven (Case-III: 8-segment)	0.981

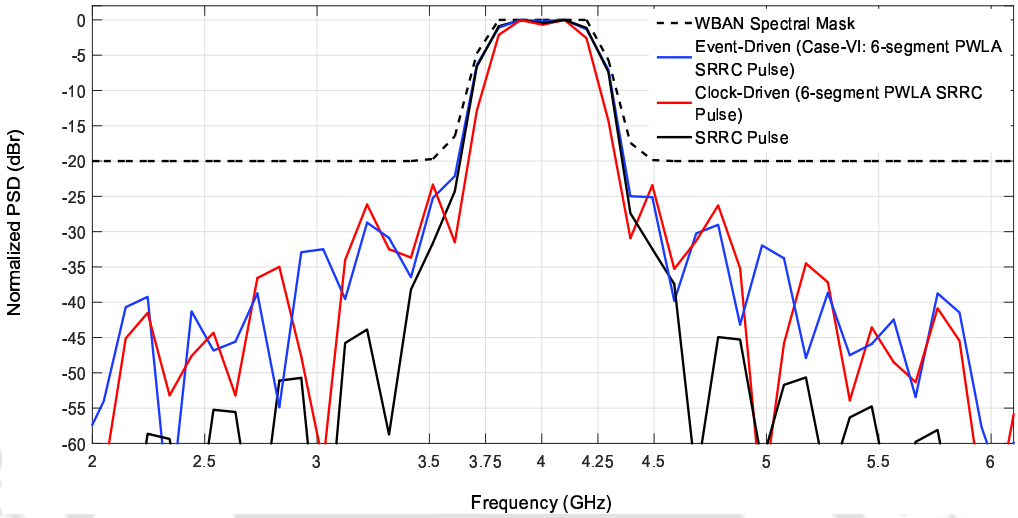


Figure 6.11: PSDs of the clock-driven (6-segment) and the event-driven (Case-VI: 6-segment) PWLA SRRC pulse

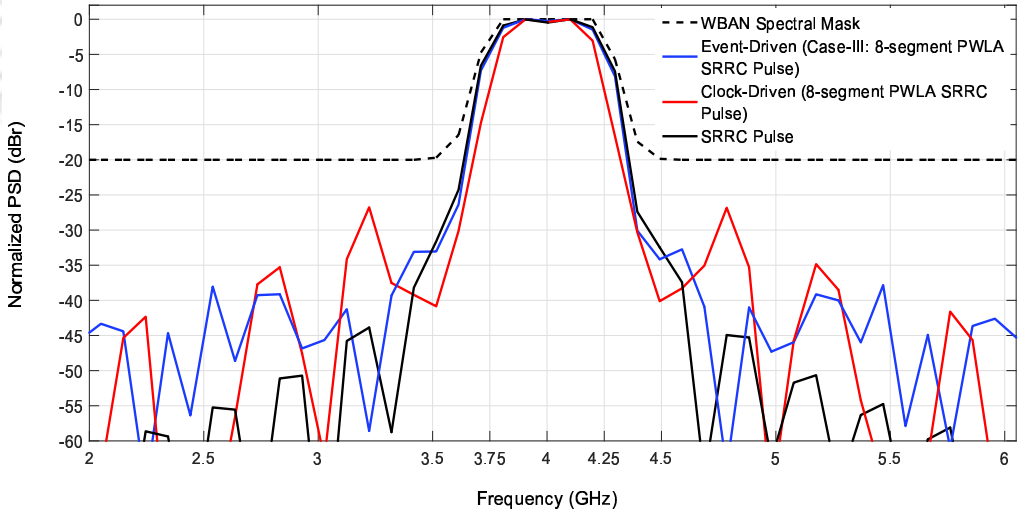


Figure 6.12: PSDs of the clock-driven (8-segment) and the event-driven (Case-III: 8-segment) PWLA SRRC pulse

next considered. The design methodology is explained in the following.

The event-driven approach proposed in Section 6.2 is employed to generate the segments 'AB', 'BC', 'CD', 'DE', 'EF', 'FG', 'GH' and 'HI' of the PWLA SRRC pulse (Fig. 6.2(c)). The output of

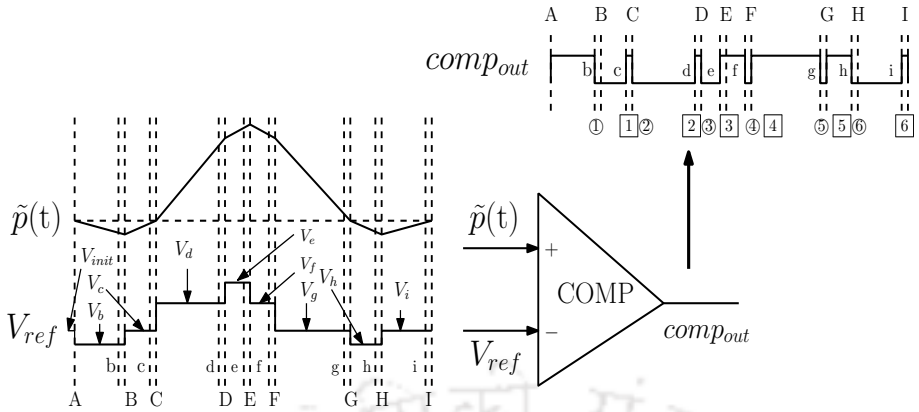


Figure 6.13: Realization of voltage breakpoints for Case-III: 8-segment PWLA SRRC pulse generator

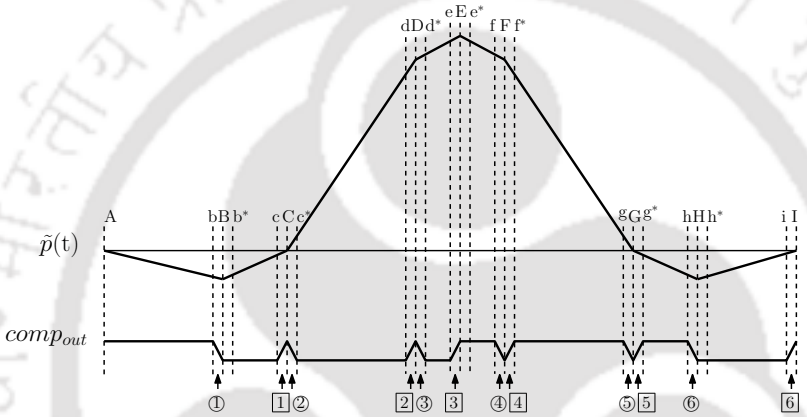


Figure 6.14: A detailed actual view of six 0→1 transitions and six 1→0 transitions

Table 6.5: Digital states of sig_1-sig_8 with respect to ①, ②,..., ⑥ and [1], [2], ..., [6] transitions

Serial No.	Change of Transition States		Digital States of sig_1-sig_8								PWLA Segment
			sig_1	sig_2	sig_3	sig_4	sig_5	sig_6	sig_7	sig_8	
1.	From A	Till ①	High	High	High	Low	High	Low	High	Low	AB
2.	After ①	Till [1]	High	Low	Low	Low	High	Low	High	Low	BC
3.	From ②	Till [2]	High	Low	High	Low	Low	Low	High	Low	CD
4.	From ③	Till [3]	High	Low	High	Low	High	Low	Low	Low	DE
5.	After [3]	Till ④	High	Low	High	Low	High	Low	High	High	EF
6.	From [4]	Till ⑤	High	Low	High	Low	High	High	High	Low	FG
7.	From [5]	Till ⑥	High	Low	High	High	High	Low	High	Low	GH
8.	After ⑥	Till [6]	Low	Low	High	Low	High	Low	High	Low	HI

the comparator '$comp_{out}$' is generated by comparing the voltage '$\tilde{p}(t)$' with an appropriate reference voltage 'V_{ref}' obtained through a multiplexer that selects one among the possible reference voltages : V_{init}, V_b, V_c, ..., V_i (Fig. 6.13). A close observation of '$comp_{out}$' shows that the signal has six 1→0

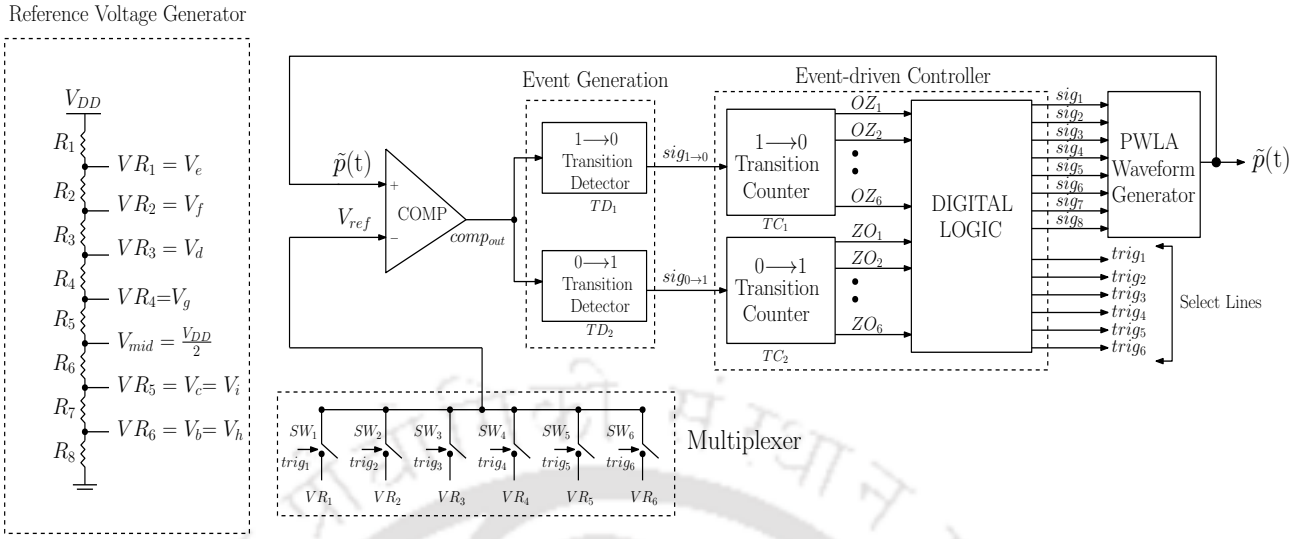


Figure 6.15: Block Diagram of the proposed event-driven PWLA SRRC pulse generator: Case-III

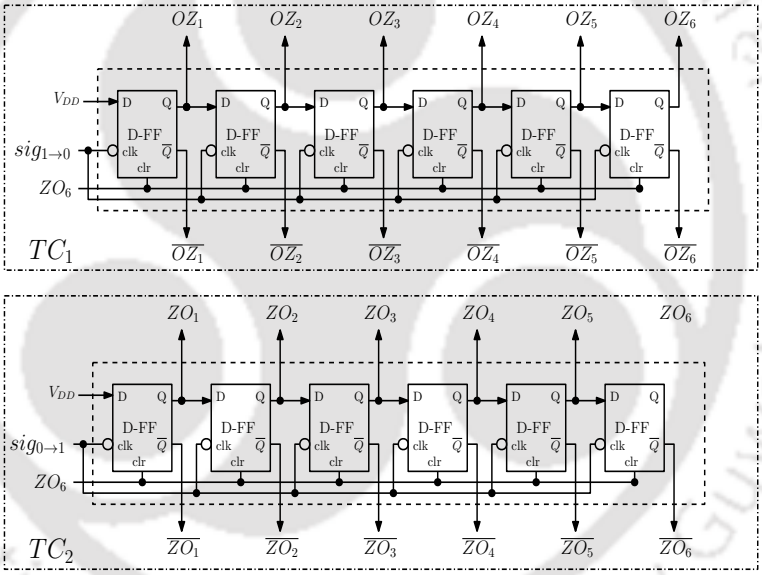


Figure 6.16: Circuit diagram of transition counters: TC_1 and TC_2

and six 0→1 transitions. The 1→0 transitions are marked as ①, ②, ③, ④, ⑤ and ⑥ while the 0→1 transitions are marked as 1, 2, 3, 4, 5 and 6. It may be noted that in a practical circuit the view of '$comp_{out}$' signal in reference to '$\tilde{p}(t)$' illustrating the twelve transitions is more like the one shown in Fig. 6.14. These transitions provide a practical solution to design an event-driven controller for the generation of control signals sig_1-sig_8 (Table 6.5).

The block diagram of the proposed event-driven PWLA SRRC pulse generator is shown in Fig. 6.15. The pulse generator consists of the following blocks: an analog comparator (COMP), an event

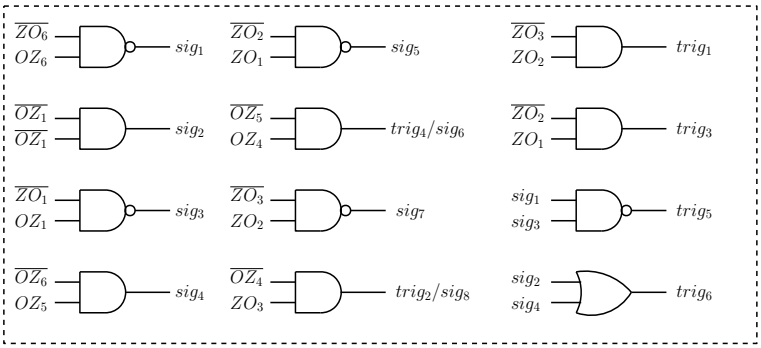


Figure 6.17: Circuit diagram of digital logic for generation of sig_1, sig_2, ..., sig_8 and $trig_1$, $trig_2$, ..., $trig_6$

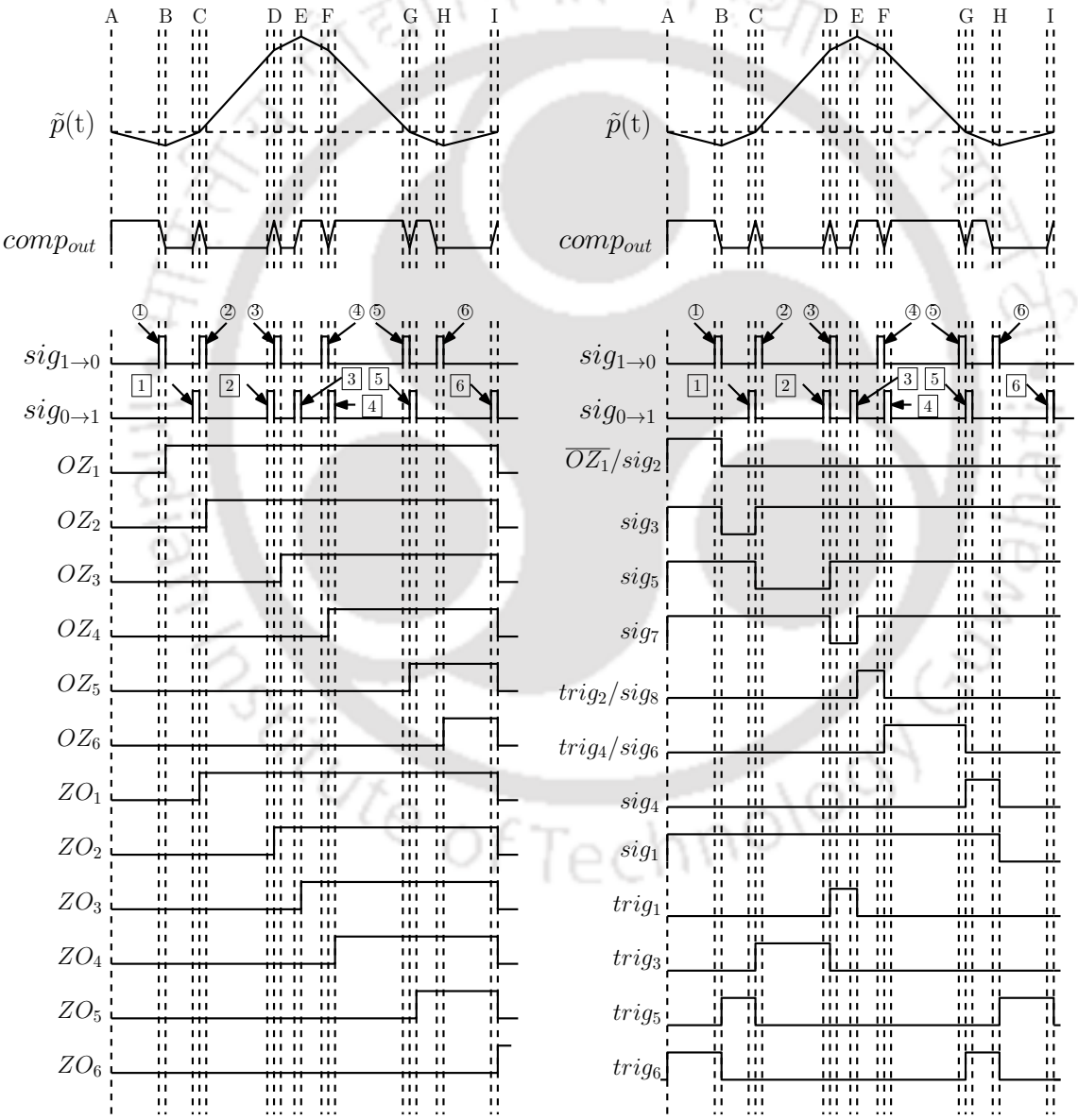


Figure 6.18: Timing Diagram of event-generation block and event-driven controller

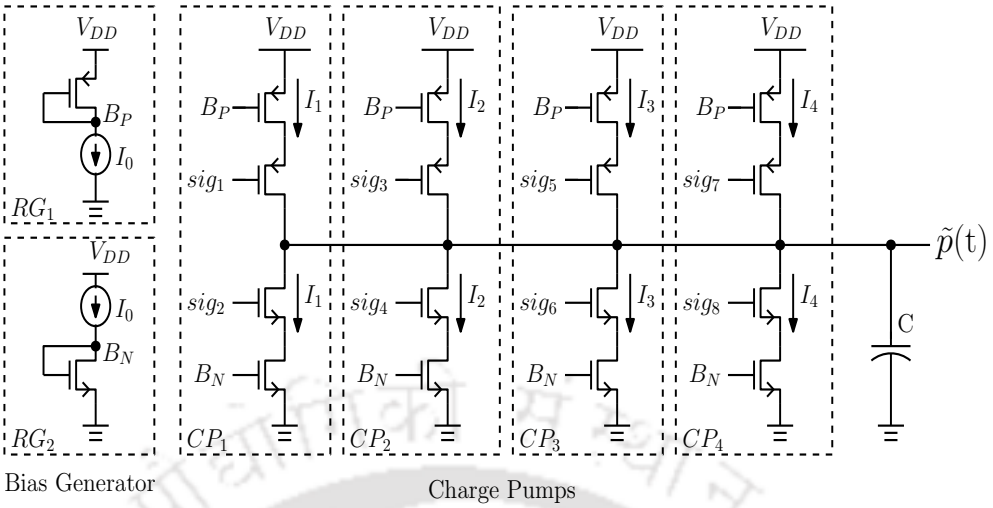


Figure 6.19: Circuit Diagram of 8-segment PWLA Waveform Generator

generation block and an event-driven controller. The event-generation block consists of a 1→0 transition detector (TD_1) and a 0→1 transition detector (TD_2). The event-driven controller core consists of a 1→0 transition counter (TC_1), a 0→1 transition counter (TC_2) and digital logic circuitry. The reference switches SW_1, SW_2, SW_3, SW_4, SW_5 and SW_6 act on a multiplexer for selecting the appropriate reference voltage V_{ref} triggered by the select lines $trig_1$, $trig_2$, $trig_3$, $trig_4$, $trig_5$ and $trig_6$. The TD_1 and TD_2 respectively detect an 1→0 transition and a 0→1 transition in the signal $comp_{out}$ by flagging the respective digital outputs $sig_{1\to0}$ and $sig_{0\to1}$. The transition detector circuit presented by Wang and Singh [398] is considered. The transition counters TC_1 and TC_2 count the number of occurrence of '1' state in $sig_{1\to0}$ and $sig_{0\to1}$ by outputting the digital signals $\{OZ_1, OZ_2, OZ_3, OZ_4, OZ_5, OZ_6\}$ and $\{ZO_1, ZO_2, ZO_3, ZO_4, ZO_5, ZO_6\}$ respectively. For example, the occurrence of transition ① or transition ② are indicated by TC_1 as '100000' or '110000' respectively. Similarly, as an example, the occurrence of transition $\boxed{5}$ is indicated by TC_2 as $\{ZO_1, ZO_2, ZO_3, ZO_4, ZO_5, ZO_6\}$= {1,1,1,1,1,0}. Fig. 6.16 shows the proposed transition counters TC_1 and TC_2. The outputs from the transition counters serve as the inputs to the digital logic circuitry (Fig. 6.17) for generation of sig_1, sig_2, ..., sig_8 and $trig_1$, $trig_2$, ..., $trig_6$. Fig. 6.18 shows the timing diagram of the event-generation block and the event-driven controller. The PWLA waveform generator block (in Fig. 6.15) for generation of Case-III: 8-segment SRRC pulse is detailed in Fig. 6.19. The waveform generator consists of four charge pump circuits CP_1, CP_2, CP_3 and CP_4 for the corresponding current flows I_1, I_2, I_3 and I_4 to the same capacitive load 'C'. The current source I_0 serves as the basic reference current source

mirroring the currents I_1, I_2, I_3 and I_4.

6.7 Event-driven Approximation of N-segment PWLA IR-UWB Pulse Generation

For additional illustration, the proposed event-driven approximation approach is applied to a few selected IR-UWB pulse shapes, such as a Gaussian pulse and its derivatives (first-, third- and fifth-derivatives of a Gaussian pulse). The details are as follows:

6.7.1 N-segment PWLA Gaussian Pulse

The Gaussian pulse given by (Appendix C: Equation (C.1)) can be approximated by an eight-segment PWLA Gaussian pulse shown in Fig. 6.20(a). This can be generated by switching four positive current sources I_1, I_2, I_3, I_4 and four negative current sources -I_1, -I_2, -I_3 and -I_4 (Appendix C: Table C.7). The normalized PSD of this approximation is shown in Fig. 6.20(b).

6.7.2 N-segment PWLA First-derivative Gaussian Pulse

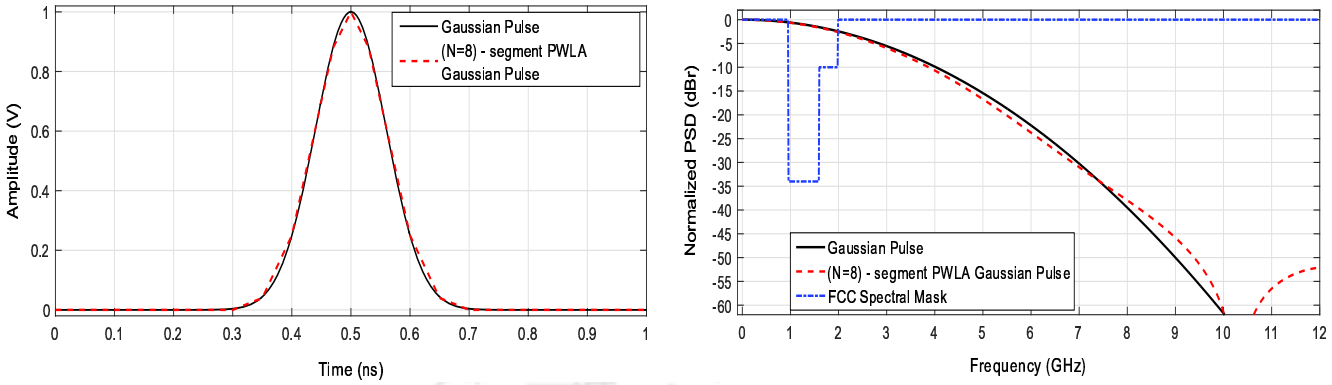
The (N=13)- segment PWLA first-derivative Gaussian pulse approximating the first-derivative Gaussian pulse $G_1(t)$ given by (Appendix C: Equation (C.2)) is shown in Fig. 6.21(a). This approximation can be generated using five positive current sources I_1, I_2, I_3, I_4, I_5 and two negative current sources -I_1 and -I_2 that are switched into the charge/discharge of the capacitor (Appendix C: Table C.8). Fig. 6.21(b) shows the normalized PSD of the thirteen-segment approximation with respect to the FCC spectral mask [3].

6.7.3 N-segment PWLA Third-derivative Gaussian Pulse

A seventeen-segment PWLA pulse for the third-derivative Gaussian pulse $G_3(t)$ (Appendix C: Equation (C.3)) is shown in Fig. 6.22(a). The seventeen-segments are generated by switching six positive current sources I_1, I_2, I_3, I_4, I_5, I_6 and seven negative current sources -I_1, -I_2, -I_3, -I_4, -I_5, -I_6 and -I_7 as illustrated in Appendix C: Table C.9. The normalized PSD of this approximation is shown in Fig. 6.22(b).

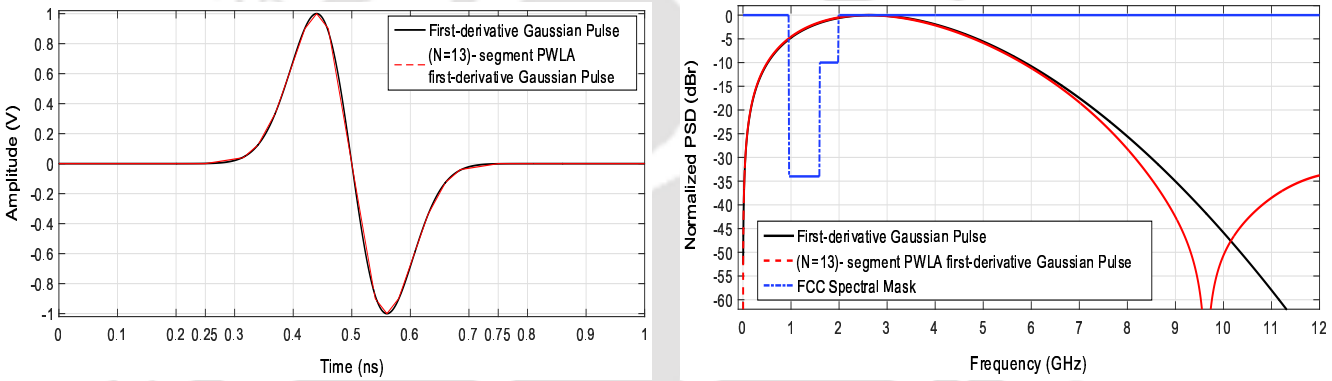
6.7.4 N-segment PWLA Fifth-derivative Gaussian Pulse

The "closest-fitting" 22-segment fifth-derivative Gaussian pulse approximating the fifth-derivative Gaussian pulse $G_5(t)$ given by (Appendix C: Equation (C.4)) is shown in Fig. 6.23(a). This can be



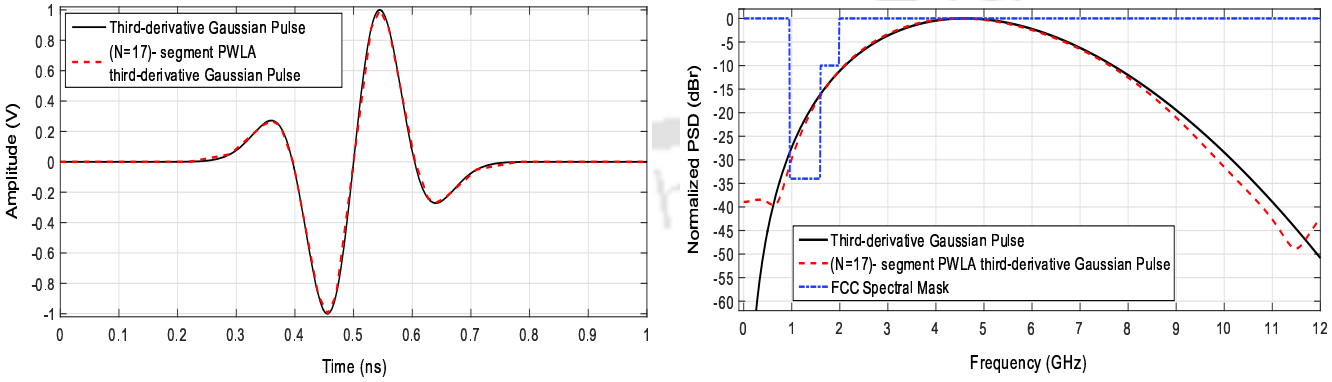
(a) (b)

Figure 6.20: (a) (N= 8) - segment PWLA Gaussian pulse approximating a Gaussian pulse and (b) the PSD of the "PWLA Gaussian pulse"



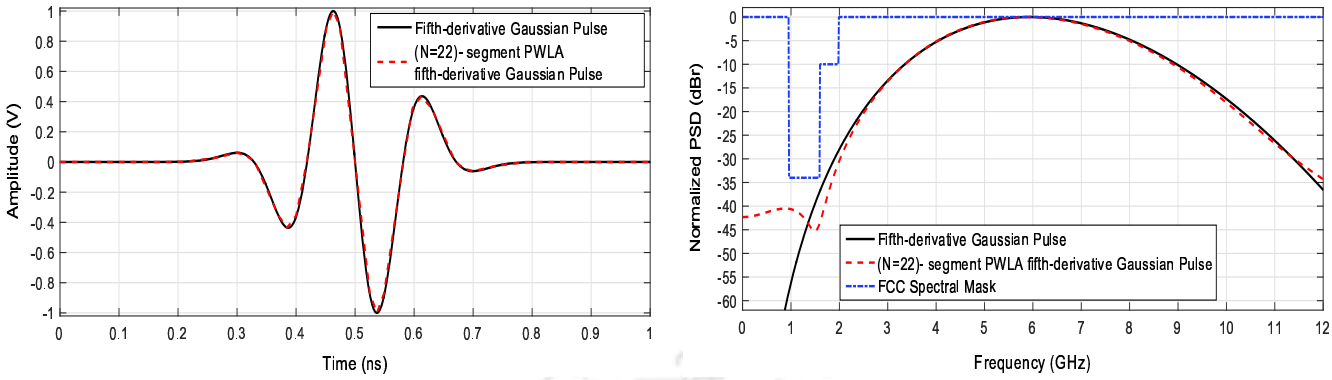
(a) (b)

Figure 6.21: (a) (N= 13) - segment PWLA first-derivative Gaussian pulse approximating the first-derivative Gaussian pulse and (b) the PSD



(a) (b)

Figure 6.22: (a) (N= 17) - segment PWLA third-derivative Gaussian pulse approximating a third-derivative Gaussian pulse and (b) the PSD



(a) (b)

Figure 6.23: (a) (N= 22) - segment PWLA fifth-derivative Gaussian pulse approximating a fifth-derivative Gaussian pulse and (b) the PSD

generated by using eight positive current sources I_1, I_2, I_3, I_4, I_5, I_6, I_7, I_8 and eight negative current sources -I_1, -I_2, -I_3, -I_4, -I_5, -I_6, -I_7, -I_8 and is illustrated in Appendix C: Table C.10. Fig. 6.23(b) shows the normalized PSD of this approximation.

6.8 Conclusions

An event-driven piece-wise linear approximation (PWLA) approach for generation of an arbitrary signaling waveform is presented. This design methodology yields an accurate approximation of the desired signaling pulse. This chapter describes six different types of event-driven approximations of the SRRC pulse and evaluation of the "best-fit' PWLA SRRC pulse vis-à-vis the theoretical SRRC pulse. The implementation details of the "best-fit" SRRC pulse generator is also discussed. Furthermore, approximations of the Gaussian pulse and its first-, third- and fifth-derivatives are also presented. The proposed event-driven approach has the potential to approximate a desired pulse with a high degree of accuracy in a simple architectural implementation.

7

Conclusions and Scope for Future Work

Contents

7.1 Conclusions

Keeping in view of some of the requirements of health-care systems in current technologies, this research has attempted to address certain issues in Transceiver design for 15.6 BANs – from methodology to architectural level – in order to take full advantage from system-level perspective.

The specific contributions made are as follows:

- *IR-UWB Transmitter:* Generation of an arbitrary signaling waveform is not always physically realizable; it can only be approximated to a certain degree of accuracy. The thesis presents a novel piece-wise linear approximation (PWLA) approach for generation of a desired signaling waveform and considers its practical implementation in simple mixed signal realization involving mostly digital circuits. The proposed PWLA approach has the potential to approximate a desired waveform with a high degree of accuracy. Various PWLA approximations of the SRRC pulse are evaluated in terms of goodness-of-fit (cross-correlation, percentage relative error, PSD and implementation complexity) along with its efficacies from the point of hardware implementation. The "best-fit" six-segment PWLA SRRC pulse generator is developed and using this PWLA SRRC baseband waveform a complete design of an IEEE 802.15.6 compliant IR-UWB transmitter operating in the mandatory low-band at 3.9936 GHz with a data rate of 0.4875 Mbps is presented. The simulation results demonstrated the applicability and the feasibility of the proposed PWLA pulse generator in IR-UWB transmitter design.

- *IR-UWB Receiver:* A non-coherent energy-detection based receiver is a practical approach in WBAN receiver design due to its energy efficiency and structural simplicity. The RF front-end is implemented using a single-to-differential LNA, energy-efficient inverter-based RF gain stages that can be selectively enabled/disabled followed by a squarer. Such an architecture is attractive in BAN scenario involving battery operated nodes. The implementation simplicity of the receiver is further enhanced by employing a windowed integrator and a single-ended SAR ADC for "integration" and "digitization" of the received signal. The single-ended SAR ADC utilizes a new digital switching technique for the capacitive reference DAC. The ADC works using a novel counter-based SAR controller. For demodulation of 2-ary and 16-ary PPM signals in 15.6 IR-UWB signaling format, a digital back-end has been presented.

Simulations studies and the performance evaluation are also carried out for validation of the

proposed energy detection based receiver.

- *Energy-efficient DAC Switching Scheme:* Suggestions are made in improving savings in switching energy in a capacitive reference DAC (employed in N-bit single-ended SAR ADCs) by introducing a new DAC switching technique. This technique brings down the switching energy in the first few comparison cycles where the switching energy consumption is the highest among the 'N' comparison cycles. Simulations are carried out to validate the proposed DAC switching technique and results are compared with the existing state-of-the-art DAC techniques.

- *Generalization of the PWLA Approach - Event-driven PWLA Waveform Generator:* One limitation of the PWLA generator (Chapter 3) is that the controller is a clock-driven state machine where the clock is constrained to be related to the system clock. For a more accurate piece-wise linear approximation, this constraint should be overcome. To this end, an event-driven approach for PWLA pulse generator is considered and its performance evaluated. A set of "events" are generated at the break-points of a suitably chosen piece-wise linear approximation and these events in turn drives the PWLA segment generator to realize an arbitrary signaling waveform with a high degree of accuracy. A detailed study of six possible cases of PWLA approximations of SRRC pulse is carried out and the performance evaluated (in terms of cross-correlation, percentage relative error, PSD and implementation complexity). Lastly, as a special case study, this approach is applied for approximation of a few selected IR-UWB pulses (Gaussian pulse and its first-, third- and fifth derivatives). This study of the event-driven PWLA approach shows promising potential for applicability of the proposed pulse generator methodology in transceiver design.

7.2 Scope for Future Work

The thesis explores simple yet effective methods for the design of IR-UWB transceivers for 15.6 BAN systems. This research can be further extended in the following directions:

- The work presented in this thesis can be extended along the following directions:
  - *Transmitter:* The data rates (R) can be readily enhanced from the current data rate of 0.4875 Mbps to higher rates (up to 15.6 Mbps) by changing the Clock as depicted in Table 7.1 and the control signals for the generation of the SRRC pulse (Figure 3.8).

Table 7.1: Enhancements in the Transmitter for Higher Data Rates

Data Rate (Mbps)	0.4875	0.975	1.95	3.9	7.8	15.6
Clock	clk†	clk†	clk†	clk†	clk‡	clk§
	clk4	clk4	clk4	–	–	–
	clk64	clk32	clk16	clk8	clk8	clk8
Slot Duration (T_w)	64 ns	32 ns	16 ns	8 ns	4 ns	2 ns
SRRC Pulse Duration	8 ns	8 ns	8 ns	8 ns	4 ns	2 ns

$^{\dagger}f_{clk}$= 1 GHz, $^{\ddagger}f_{clk}$= 2 GHz, $^{\S}f_{clk}$= 4 GHz
f_{clk64}= f_{clk}/64, f_{clk32}= f_{clk}/32, f_{clk16}= f_{clk}/16, f_{clk8}= f_{clk}/8, f_{clk4}= f_{clk}/4

Table 7.2: Enhancements in the Receiver for Higher Data Rates

Data Rate (Mbps)	0.4875	0.975	1.95	3.9	7.8	15.6
f_{clk}(MHz)	15.625	31.25	62.5	125	250	500
$f_{CLK}{}^{\ddagger}$(MHz)	187.5	375	750	1500	3000	6000

$^{\ddagger}f_{CLK}$= (N+2)f_{clk}= 12f_{clk} for 10-bit single-ended SAR ADC

  - *Receiver:* The corresponding modifications in the receiver (Fig. 4.2) will involve the changes in f_{clk} and f_{CLK} as depicted in Table 7.2. Further, the windowed integrator will need to be redesigned for full-scale at the integrator output as the available integration time is progressively decreasing.

- Circuit realization of the DAC switching scheme proposed in Chapter 5 and design of a SAR ADC using this capacitive reference DAC.

- *Generalized PWLA approach:* Complete circuit design, verification and performance evaluation of the Event-driven Waveform Generator vis-à-vis a variety of signaling waveforms.

- Exploration of the Event-driven Waveform Generator for possible high data rate applications requiring very short duration signaling waveforms. A few examples are [399]:

  - Carrier-less Waveforms: Gaussian Pulse and Inverse Fast Fourier Transform (IFFT) Pulse
  - Carrier-based Waveforms: Gaussian Raised-Cosine (RC) Pulse, Hann RC Pulse, Sinc RC Pulse, Rectangular RC Pulse

- Recent research has incorporated Internet of Things (IoT) technology in various healthcare solutions, specifically for m-health solutions. IoT technology is capable of providing excellent feedback on physical and mental health conditions using real-time monitoring systems [400]. Seamless Integration of WBAN technology in IoT systems is an exciting application area that opens up a plethora of new and interesting applications of WBAN systems. Recently, Wu *et*

al. [401] have introduced enhanced interactive telecare systems (ITCS) adopting IoT technology aiming for diabetic patients and their caregivers. The current usage of 4G or the upcoming 5G cellular communications is also to provide promising features in IoT healthcare system.

IR-UWB transceiver systems will emerge as a great option for future global market of IoT due to its advantages: low-complexity, low-power consumption, low transmission power and high resistance to eavesdropping. Moreover, health-care specific IoT applications would require IR-UWB for long battery life rather than high data rates. Thus, a solution for IR-UWB transceiver based IoTs is an exciting option that needs to be explored.

- Another area where the proposed transceiver system can be explored is its application as a compliant device for the proposed IEEE 802.15.4-2015 [134] WPANs. The proposed IR-UWB transceiver system for WBANs can be an effective dual-standard 15.6-2012 and 15.4-2015 compliant IR-UWB transceiver solutions that can be used for both WPANs and WBANs.

A

On Squarer

Contents

A.1 Operation of the Squarer

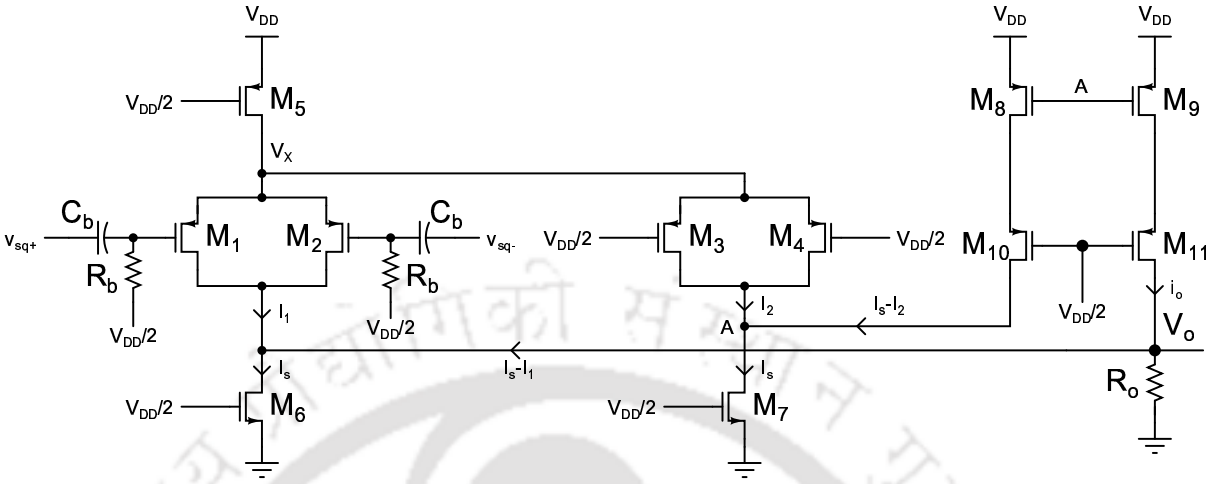


Figure A.1: Circuit schematic of the squarer

The mathematical expressions for the operation of the squarer (shown in Fig. A.1[1]) can be described as follows:

Considering the transistors M_1- M_4 to be in saturation region and neglecting the channel-length modulation, the mobility degradation and the body effect, the current flowing through the transistors M_1- M_4 may be expressed as

$$\begin{aligned} i_{M1} &= \mu_p C_{ox}\left(\frac{W}{L}\right)_1\left(V_x - \frac{V_{DD}}{2} - (v_{sq+}) + V_{tp}\right)^2 \\ &= \beta\left(V_{cons} - v_{sq+}\right)^2 \end{aligned} \tag{A.1}$$

$$\begin{aligned} i_{M2} &= \mu_p C_{ox}\left(\frac{W}{L}\right)_2\left(V_x - \frac{V_{DD}}{2} - (v_{sq-}) + V_{tp}\right)^2 \\ &= \beta\left(V_{cons} - v_{sq-}\right)^2 \end{aligned} \tag{A.2}$$

$$\begin{aligned} i_{M3,M4} &= \mu_p C_{ox}\left(\frac{W}{L}\right)_{3,4}\left(V_x - \frac{V_{DD}}{2} + V_{tp}\right)^2 \\ &= \beta V_{cons}^2 \end{aligned} \tag{A.3}$$

Here, $\beta = \mu_p C_{ox}\left(\frac{W}{L}\right)_{1,2,3,4}$ is the transconductance of the devices

and

$V_{cons} \triangleq V_x - \frac{V_{DD}}{2} + V_{tp}$

[1]Fig. 4.18 is reproduced as Fig. A.1 for ready reference

The current i_1 flowing through transistors M_1 and M_2 is given by

$$\begin{aligned} i_1 &= i_{M1} + i_{M2} \\ &= \beta\Big(V_{cons} - v_{sq+}\Big)^2 + \beta\Big(V_{cons} - v_{sq-}\Big)^2 \\ &= \beta\Big[\Big(V_{cons} - v_{sq+}\Big)^2 + \Big(V_{cons} - v_{sq-}\Big)^2\Big] \\ &= \beta\Big[2V_{cons}^2 + v_{sq+}^2 + v_{sq-}^2 - 2V_{cons}v_{sq+} - 2V_{cons}v_{sq-}\Big] \\ &= \beta\Big[2V_{cons}^2 + v_{sq+}^2 + v_{sq-}^2 - 2V_{cons}\Big(v_{sq+} + v_{sq-}\Big)\Big] \\ &= 2\beta\Big(V_{cons}^2 + v_{in}^2\Big) \end{aligned} \tag{A.4}$$

where $v_{in}^2 = v_{sq+}^2 = v_{sq-}^2$

The current i_2 flowing through transistors M_3 and M_4 is given by

$$i_2 = i_{M3} + i_{M4} = 2\beta V_{cons}^2 \tag{A.5}$$

Using (A.4) and (A.5) the current i_o can be computed as:

$$\begin{aligned} i_o &= i_1 - i_2 \\ &= 2\beta\Big(V_{cons}^2 + v_{in}^2\Big) - 2\beta V_{cons}^2 \\ &= 2\beta v_{in}^2 \end{aligned} \tag{A.6}$$

The current i_o is linearly related to the square of the input voltage. Therefore, the output of the squarer is given by

$$v_o = i_o R_o = 2\beta R_o v_{in}^2 \tag{A.7}$$

B

Implementation of RF Front-end in 65 nm Technology

Contents

B.1 Frequency Response of an Inverter-based Amplifier in 180 nm Technology

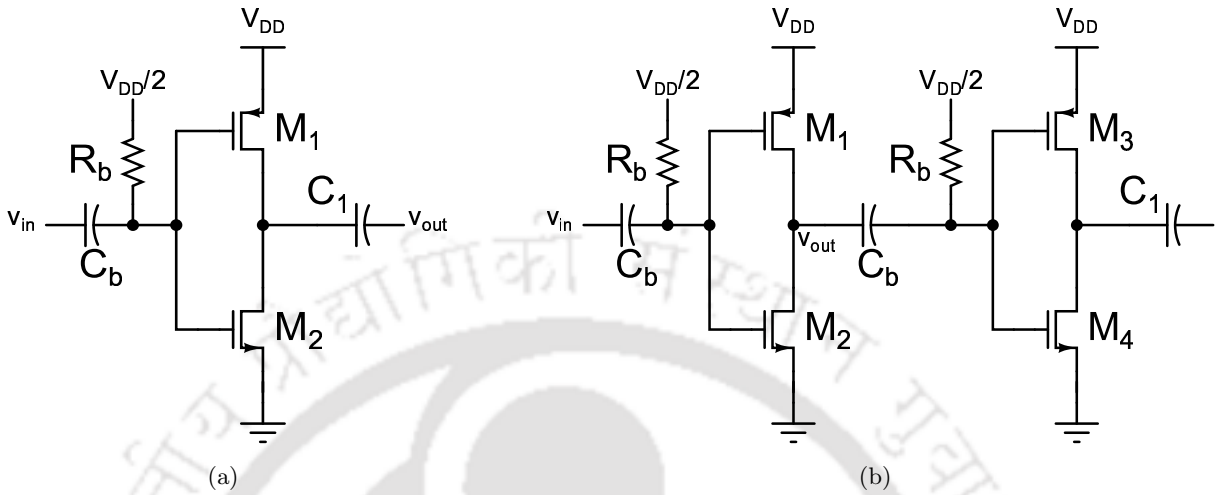


Figure B.1: Circuit schematic of an inverter-based amplifier: (a) Unloaded state (b) Loaded state (where Gain $\triangleq v_{out}/v_{in}$)

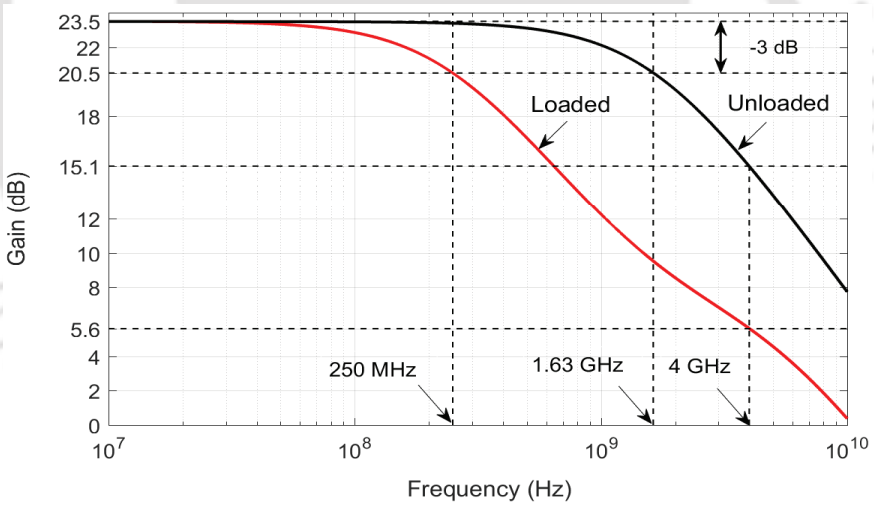


Figure B.2: Simulated frequency response of an inverter-based amplifier in loaded state and unloaded state using minimum-sized devices in 180 nm technology

It is observed that in 180 nm technology (technology employed in this work) the frequency response of an inverter-based amplifier (using minimum-sized devices) exhibits a -3 dB cut-off frequency of 1.63 GHz (Fig. B.2) in unloaded state depicted in Fig. B.1(a) whereas, in loaded state (Fig. B.1(b)), the cut-off frequency falls to 250 MHz (Fig. B.2). Further, it is seen that the inverter-based amplifier (with device sizes same as that for RF amplifier stages in Section 4.4.2) exhibits a - 3 dB cut-off

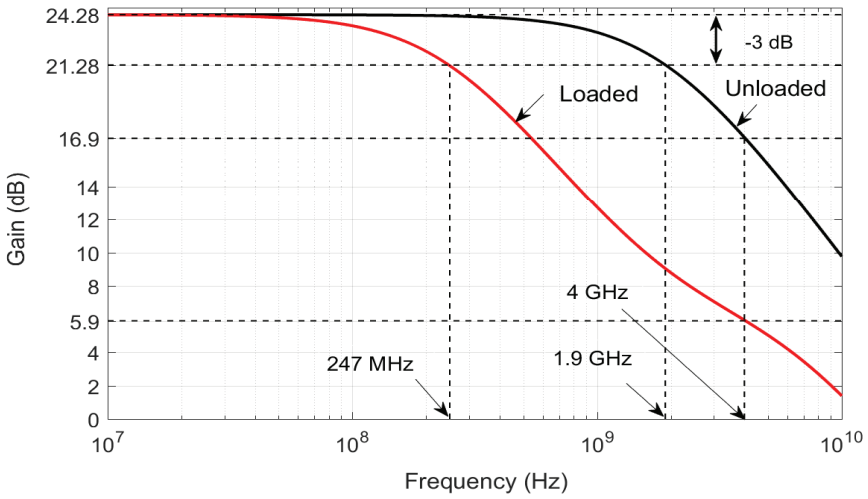


Figure B.3: Simulated frequency response of an inverter-based amplifier in loaded state and unloaded state (with device sizes same as that used for RF amplifier stages in Section 4.4.2) in 180 nm technology

frequency of 1.9 GHz (Fig. B.3) in unloaded state (Fig. B.1(a)) and a -3 dB cut-off frequency of 247 MHz (Fig. B.3) in loaded state (Fig. B.1(b)).

Thus it may be inferred that an inverter-based amplifier with a resonant load at $f_c \sim 4$ GHz will display a skewed bandpass characteristic with a much reduced gain. Hence it was felt that an advanced technology should be explored.

B.2 Design of RF Front-end in 65 nm Technology

B.2.1 LNA

Fig. B.5 shows the simulated single-ended gain of the single-to-differential LNA[1] (Fig. B.4). From Fig. B.5 it is shown that a single-ended gain of 5.55 V/V (= 14.9 dB) is obtained for a -3 dB bandwidth ($BW_{-3dB,LNA}$) of 1080 MHz:

$$Gain_{LNA} = 14.9\ dB \tag{B.1}$$

The S_{11} and the noise figure (NF) for the required frequency span from 3.5 GHz to 4.5 GHz are shown in Fig. B.6(a) and Fig. B.6(b) respectively. The obtained values of S_{11} is -16.3 dB and that of NF is 3.94 dB at the centre frequency.

[1]Fig. 4.5 is reproduced as Fig. B.4 for ready reference

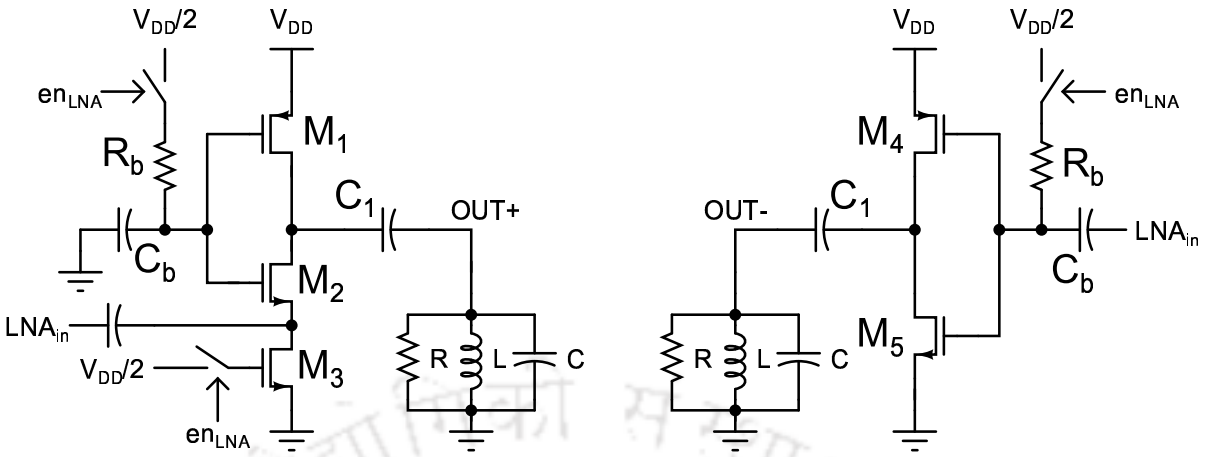


Figure B.4: Circuit schematic of the single-to-differential LNA

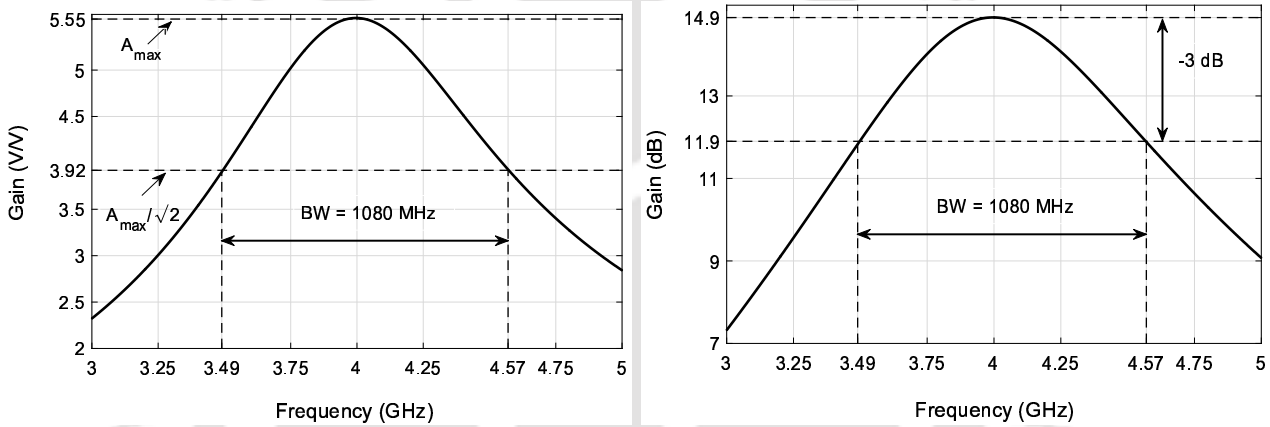
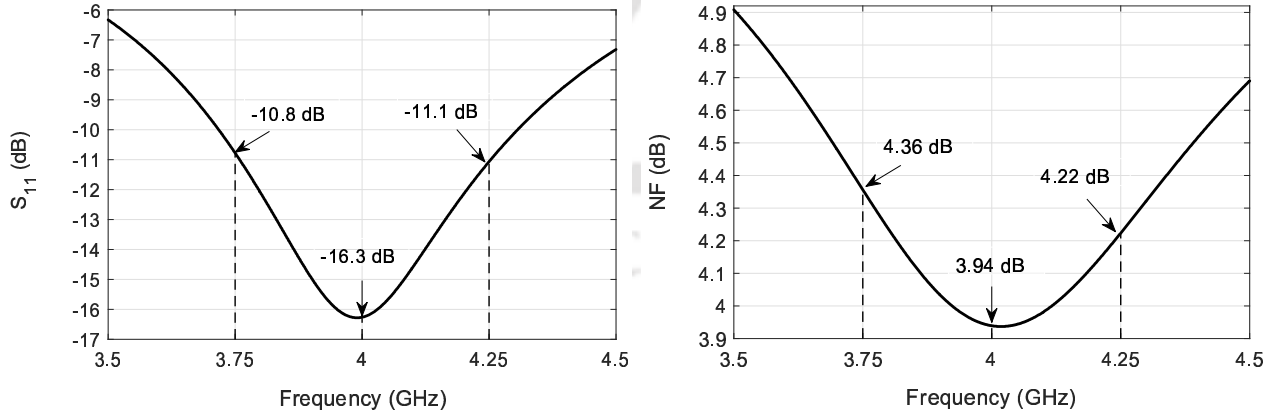


Figure B.5: Simulated single-ended gain of the single-to-differential LNA (a) in V/V (b) in dB



(a) (b)

Figure B.6: Simulated (a) S_{11} and (b) NF performance of the single-to-differential LNA

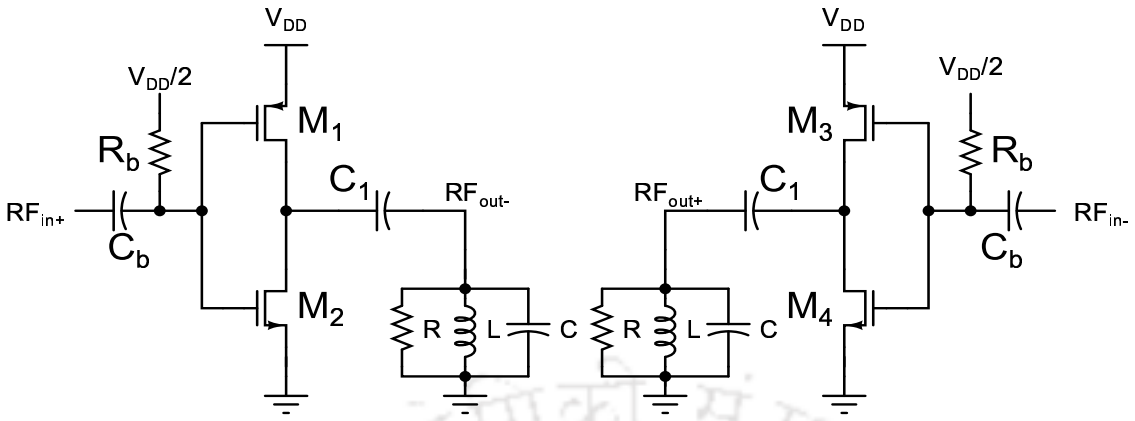


Figure B.7: Schematic of the inverter-based amplifier with a RLC resonant load

B.2.2 Multi-stage RF Amplifier

The multi-stage RF amplifier follows the LNA (Fig. 4.2). The LNA provides a gain of 14.9 dB and the remaining gain is to be achieved by the multi-stage RF amplifier.

The inverter-based amplifier topology[2] (Fig. B.7) is chosen as a suitable amplifier structure for gain stages of the multi-stage RF amplifier.

Each inverter-based amplifier stage (Fig. B.7) provides a gain of 2.57 V/V (= 8.2 dB) as shown in Fig. B.8:

$$Gain_{per\_stage} = 8.2\ dB \tag{B.2}$$

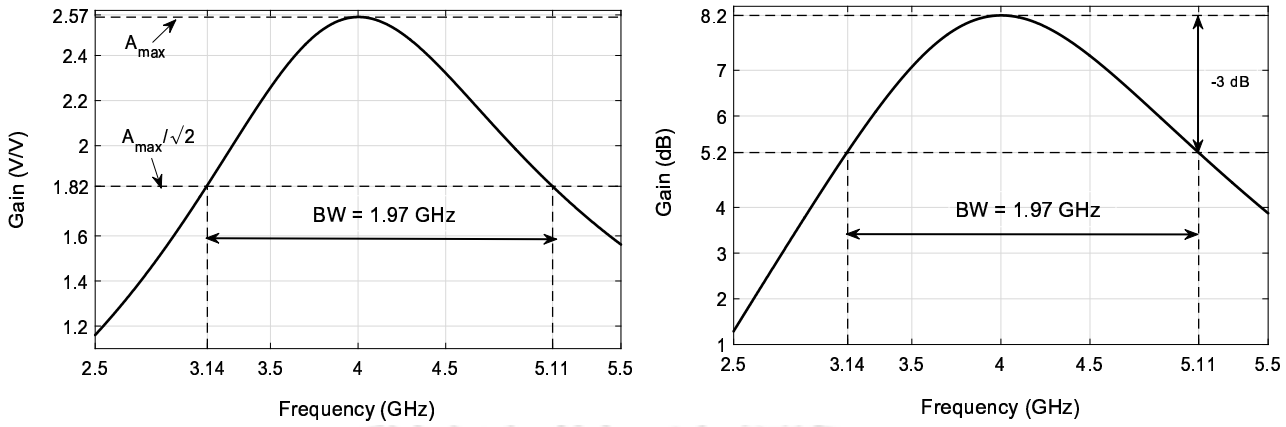
Hence using (4.9) and (4.10), the maximum and the minimum number of inverter-based amplifier can be found:

$$No\_of\_gain\_stages_{max} = \frac{Gain_{max} - Gain_{LNA}}{Gain_{per\_stage}} = \frac{71\ dB - 14.9\ dB}{8.2\ dB} = \lceil 6.84 \rceil \sim 7 \tag{B.3}$$

$$No\_of\_gain\_stages_{min} = \frac{Gain_{min} - Gain_{LNA}}{Gain_{per\_stage}} = \frac{23\ dB - 14.9\ dB}{8.2\ dB} = \lceil 0.987 \rceil \sim 1 \tag{B.4}$$

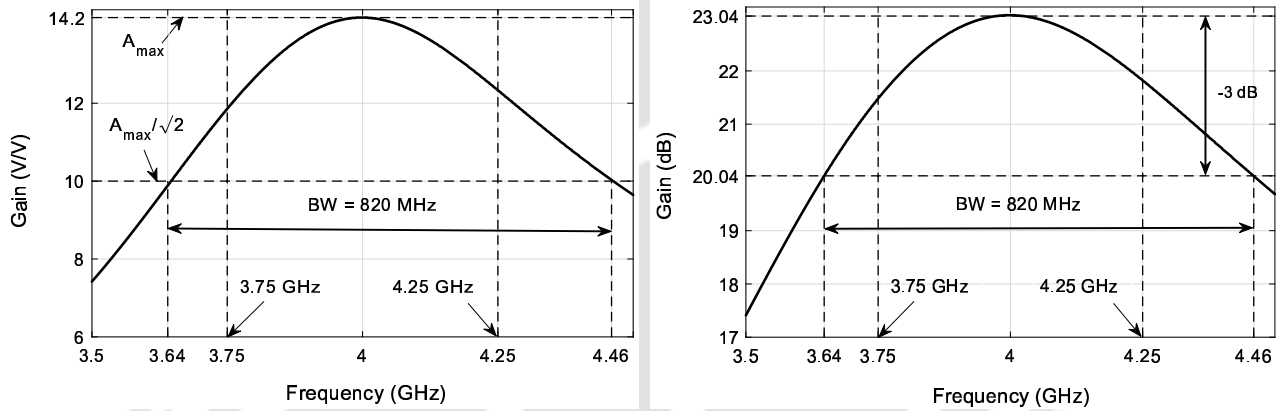
The frequency response of a cascade of the LNA and the multi-stage RF amplifier ($No\_of\_gain\_stages$ = 1, 2, ..., 6, 7) is shown in Fig. B.9, Fig. B.10, Fig. B.11, Fig. B.12, Fig. B.13, Fig. B.14 and Fig. B.15.

[2]Fig. 4.8 is reproduced as Fig. B.7 for ready reference



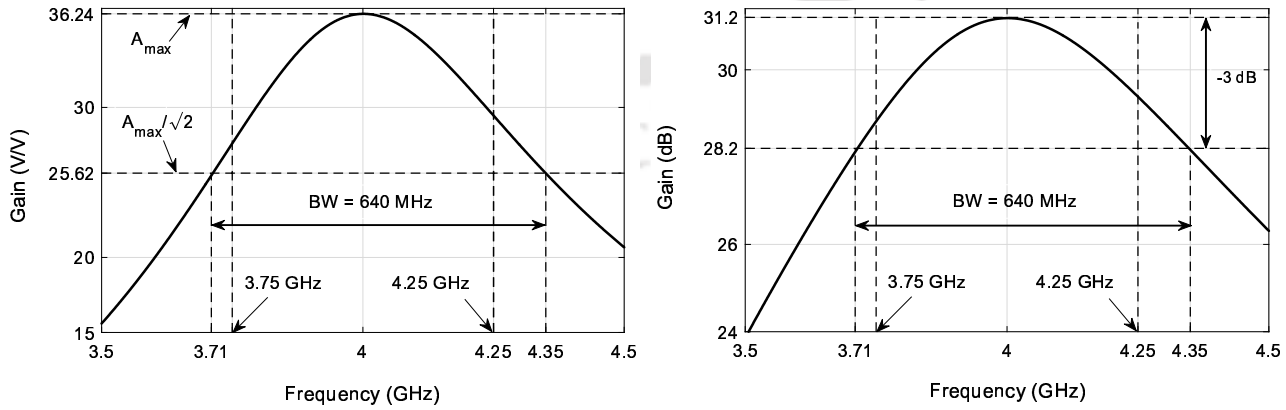
(a) (b)

Figure B.8: Simulated single-ended gain of the inverter-based amplifier (a) in V/V (b) in dB



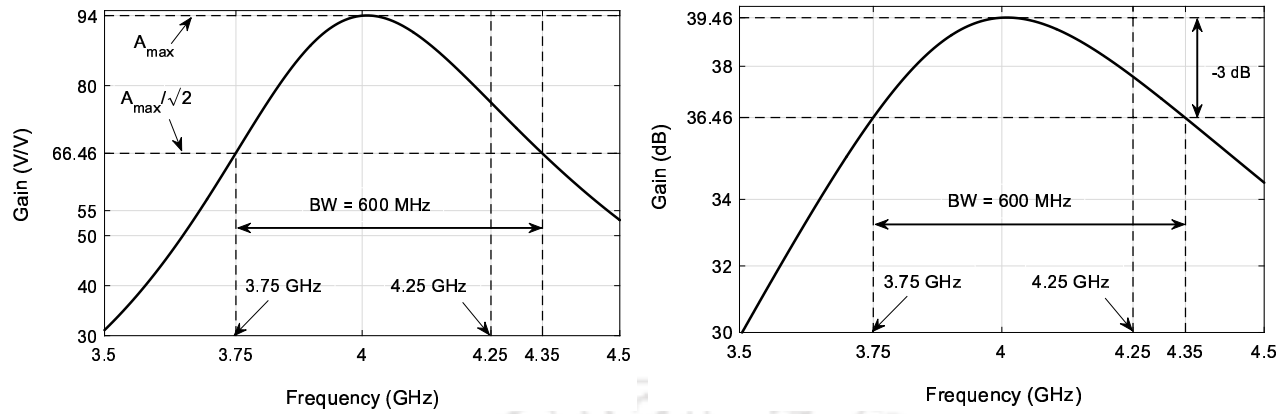
(a) (b)

Figure B.9: Simulated single-ended gain of a cascade of the LNA and the multi-stage RF amplifier ($No\_of\_gain\_stages_{min}$= 1) (a) in V/V (b) in dB



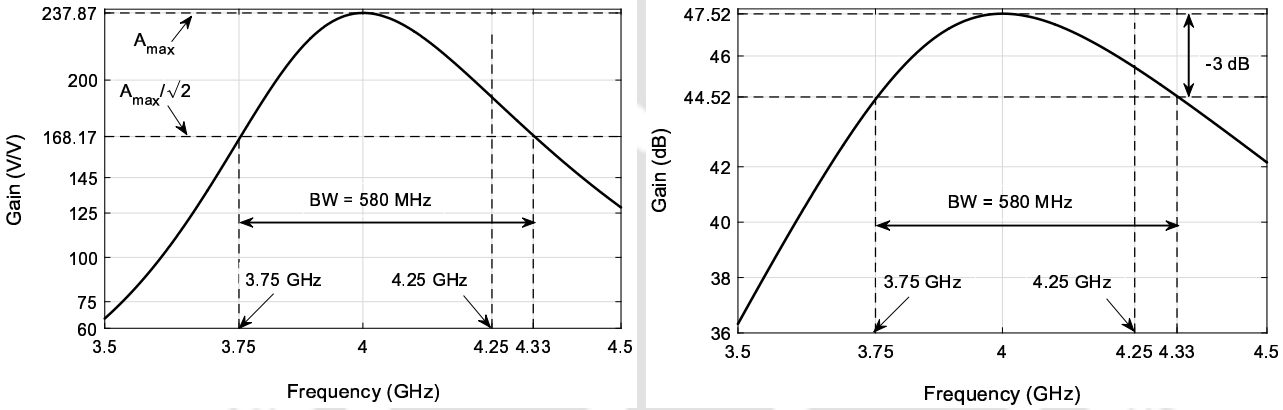
(a) (b)

Figure B.10: Simulated single-ended gain of a cascade of the LNA and the multi-stage RF amplifier ($No\_of\_gain\_stages$= 2) (a) in V/V (b) in dB



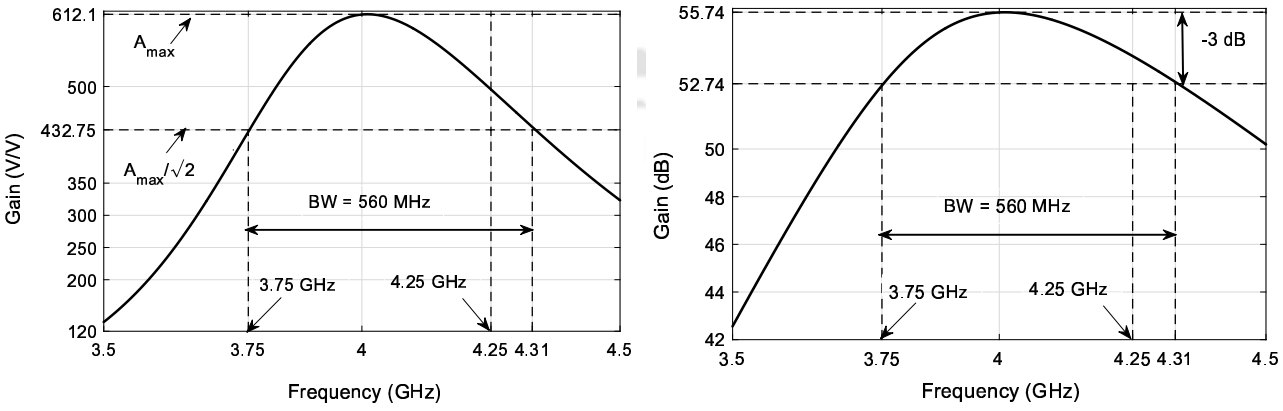
(a) (b)

Figure B.11: Simulated single-ended gain of a cascade of the LNA and the multi-stage RF amplifier ($No\_of\_gain\_stages$= 3) (a) in V/V (b) in dB



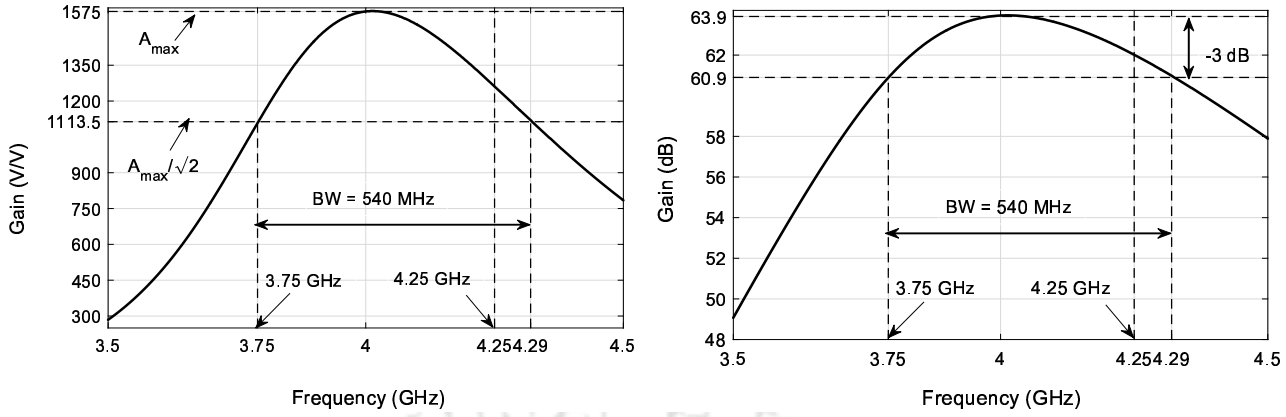
(a) (b)

Figure B.12: Simulated single-ended gain of a cascade of the LNA and the multi-stage RF amplifier ($No\_of\_gain\_stages$= 4) (a) in V/V (b) in dB



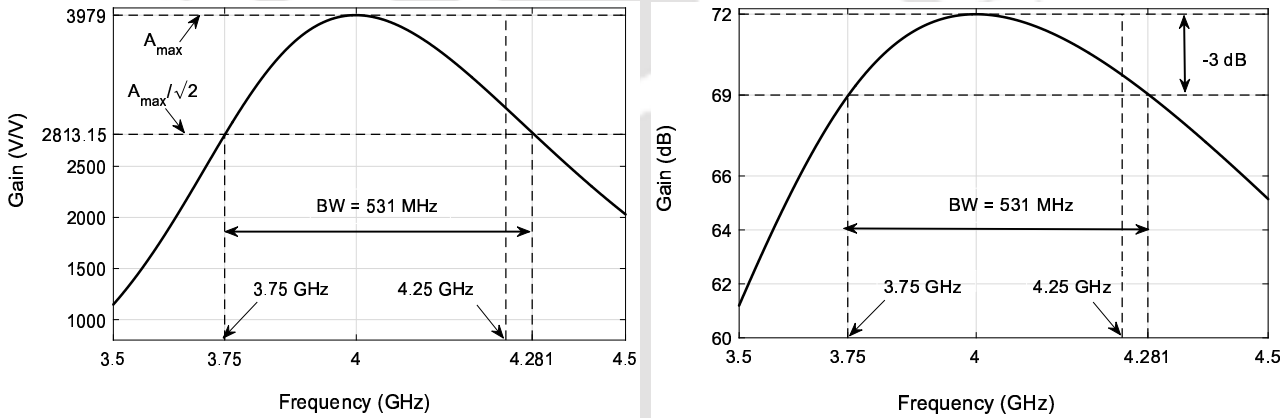
(a) (b)

Figure B.13: Simulated single-ended gain of a cascade of the LNA and the multi-stage RF amplifier ($No\_of\_gain\_stages$= 5) (a) in V/V (b) in dB



(a) (b)

Figure B.14: Simulated single-ended gain of a cascade of the LNA and the multi-stage RF amplifier ($No\_of\_gain\_stages$= 6) (a) in V/V (b) in dB



(a) (b)

Figure B.15: Simulated single-ended gain of a cascade of the LNA and the multi-stage RF amplifier ($No\_of\_gain\_stages_{max}$= 7) (a) in V/V (b) in dB

B.2.3 Discussions

It is observed in 65 nm technology that the frequency response of an inverter-based amplifier (using minimum-sized devices) exhibits a -3 dB cut-off frequency f_{-3dB}= 4.94 GHz in unloaded state and f_{-3dB}= 723 MHz in loaded state (Fig. B.16). Further, it is seen that the inverter-based amplifier (with device sizes same as that used for RF amplifier stages in Section B.2.2) exhibits a - 3 dB cut-off frequency f_{-3dB}= 5.94 GHz in unloaded state and f_{-3dB}= 891 MHz in loaded state (Fig. B.17).

Though the inverter-based amplifier in 65 nm technology has a wider frequency response, it is seen that there is no significant improvement in the overall response of the RF stage and requires around

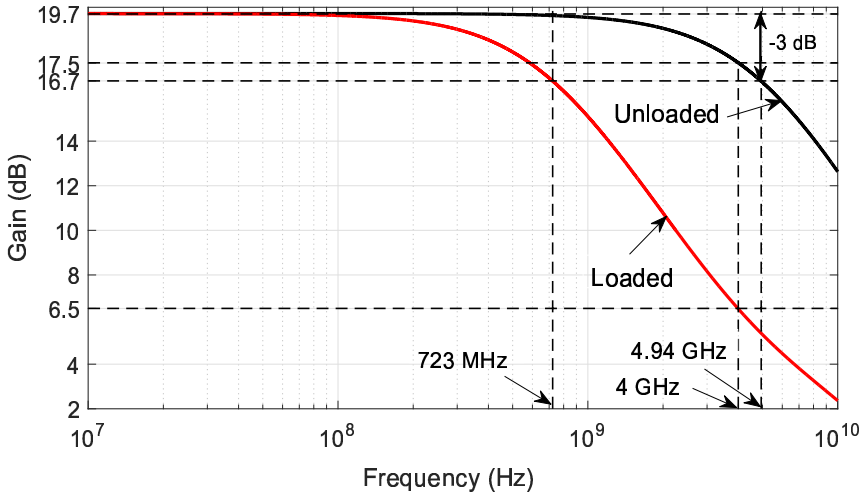


Figure B.16: Simulated frequency response of an inverter-based amplifier in loaded state and unloaded state using minimum-sized devices in 65 nm technology

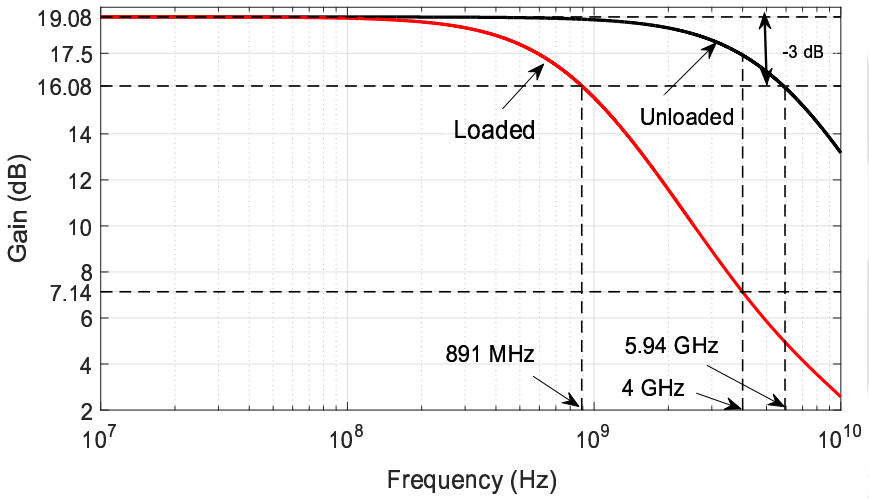


Figure B.17: Simulated frequency response of an inverter-based amplifier in loaded state and unloaded state (with device sizes same as that used for RF amplifier stages in Section B.2.2) in 65 nm technology

the same number of stages of RF amplification.

C

Event-driven PWLA Waveforms

Contents

C.1 Event-driven N-segment PWLA approach to Generation of SRRC Pulse

Table C.1: Case-I: 10-segment PWLA SRRC Pulse

PWLA Segments (i)	Voltage breakpoint (v) at time (t)				$slope_i$ (V/ns)	Charge/Discharge		Current Source	
	t_i (ns)	v_i (V)	t_{i-1} (ns)	v_{i-1} (V)		Charge	Discharge	Positive	Negative
1	1.6	0.84	t_{init}= 0	v_{init}= 0.9	-0.04		✓		$-I_1$
2	2.25	0.9	1.6	0.84	0.09	✓		I_2	
3	3	1.1	2.25	0.9	0.26	✓		I_3	
4	3.55	1.25	3	1.1	0.27	✓		I_4	
5	4	1.3	3.55	1.25	0.11	✓		I_5	
6	4.45	1.25	4	1.3	-0.11		✓		$-I_5$
7	5	1.1	4.45	1.25	-0.27		✓		$-I_4$
8	5.75	0.9	5	1.1	-0.26		✓		$-I_3$
9	6.4	0.84	5.75	0.9	-0.09		✓		$-I_2$
10	8	0.9	6.4	0.84	0.04	✓		I_1	

Table C.2: Case-II: 8-segment PWLA SRRC Pulse

PWLA Segments (i)	Voltage breakpoint (v) at time (t)				$slope_i$ (V/ns)	Charge/Discharge		Current Source	
	t_i (ns)	v_i (V)	t_{i-1} (ns)	v_{i-1} (V)		Charge	Discharge	Positive	Negative
1	1.6	0.84	t_{init}= 0	v_{init}= 0.9	-0.04		✓		$-I_1$
2	2.25	0.9	1.6	0.84	0.09	✓		I_2	
3	3	1.1	2.25	0.9	0.26	✓		I_3	
4	4	1.3	3	1.1	0.2	✓		I_4	
5	5	1.1	4	1.3	-0.2		✓		$-I_4$
6	5.75	0.9	5	1.1	-0.26		✓		$-I_3$
7	6.4	0.84	5.75	0.9	-0.09		✓		$-I_2$
8	8	0.9	6.4	0.84	0.04	✓		I_1	

Table C.3: Case-III: 8-segment PWLA SRRC Pulse

PWLA Segments (i)	Voltage breakpoint (v) at time (t)				$slope_i$ (V/ns)	Charge/Discharge		Current Source	
	t_i (ns)	v_i (V)	t_{i-1} (ns)	v_{i-1} (V)		Charge	Discharge	Positive	Negative
1	1.6	0.84	t_{init}= 0	v_{init}= 0.9	-0.04		✓		$-I_1$
2	2.25	0.9	1.6	0.84	0.09	✓		I_2	
3	3.55	1.25	2.25	0.9	0.27	✓		I_3	
4	4	1.3	3.55	1.25	0.11	✓		I_4	
5	4.55	1.25	4	1.3	-0.11		✓		$-I_4$
6	5.75	0.9	4.55	1.25	-0.27		✓		$-I_3$
7	6.4	0.84	5.75	0.9	-0.09		✓		$-I_2$
8	8	0.9	6.4	0.84	0.04	✓		I_1	

Table C.4: Case-IV: 8-segment PWLA SRRC Pulse

PWLA Segments (i)	Voltage breakpoint (v) at time (t)				$slope_i$ (V/ns)	Charge/Discharge		Current Source	
	t_i (ns)	v_i (V)	t_{i-1} (ns)	v_{i-1} (V)		Charge	Discharge	Positive	Negative
1	1.42	0.84	t_{init}= 0	v_{init}= 0.9	-0.04		✓		-I_1
2	2.25	0.9	1.42	0.84	0.07	✓		I_2	
3	3.55	1.25	2.25	0.9	0.27	✓		I_3	
4	4	1.3	3.55	1.25	0.11	✓		I_4	
5	4.55	1.25	4	1.3	-0.11		✓		-I_4
6	5.75	0.9	4.55	1.25	-0.27		✓		-I_3
7	6.6	0.84	5.75	0.9	-0.07		✓		-I_2
8	8	0.9	6.6	0.84	0.04	✓		I_1	

Table C.5: Case-V: 6-segment PWLA SRRC Pulse

PWLA Segments (i)	Voltage breakpoint (v) at time (t)				$slope_i$ (V/ns)	Charge/Discharge		Current Source	
	t_i (ns)	v_i (V)	t_{i-1} (ns)	v_{i-1} (V)		Charge	Discharge	Positive	Negative
1	1.6	0.84	t_{init}= 0	v_{init}= 0.9	-0.04		✓		-I_1
2	3	1.1	1.6	0.84	0.18	✓		I_2	
3	4	1.3	3	1.1	0.2	✓		I_3	
4	5	1.1	4	1.3	-0.2		✓		-I_3
5	6.4	0.84	5	1.1	-0.18		✓		-I_2
6	8	0.9	6.4	0.84	0.04	✓		I_1	

Table C.6: Case-VI: 6-segment PWLA SRRC Pulse

PWLA Segments (i)	Voltage breakpoint (v) at time (t)				$slope_i$ (V/ns)	Charge/Discharge		Current Source	
	t_i (ns)	v_i (V)	t_{i-1} (ns)	v_{i-1} (V)		Charge	Discharge	Positive	Negative
1	2.05	0.84	t_{init}= 0	v_{init}= 0.9	-0.03		✓		-I_1
2	3.55	1.25	2.05	0.84	0.27	✓		I_2	
3	4	1.3	3.55	1.25	0.11	✓		I_3	
4	4.55	1.25	4	1.3	-0.11		✓		-I_3
5	5.95	0.84	4.55	1.25	-0.27		✓		-I_2
6	8	0.9	5.95	0.84	0.03	✓		I_1	

C.2 Mathematical Expressions for Gaussian Pulse and its first-, third- and fifth- derivative

The mathematical expressions for the Gaussian pulse and its derivatives (first-, third- and fifth-derivatives of the Gaussian pulse) are given as follows [402, 403]:

Gaussian Pulse:

$$G(t) = \frac{A}{\sqrt{2\pi}\sigma}\ exp\left(\frac{-t^2}{2\sigma^2}\right) \tag{C.1}$$

First-derivative Gaussian Pulse:

$$G_1(t) = \frac{-At}{\sqrt{2\pi}\sigma^3}\ exp\left(\frac{-t^2}{2\sigma^2}\right) \tag{C.2}$$

Third-derivative Gaussian Pulse:

$$G_3(t) = A\left(\frac{3t}{\sqrt{2\pi}\sigma^5} - \frac{t^3}{\sqrt{2\pi}\sigma^7}\right)\ exp\left(\frac{-t^2}{2\sigma^2}\right) \tag{C.3}$$

Fifth-derivative Gaussian Pulse:

$$G_5(t) = A\left(\frac{10t^3}{\sqrt{2\pi}\sigma^9} - \frac{15t}{\sqrt{2\pi}\sigma^7} - \frac{t^5}{\sqrt{2\pi}\sigma^{11}}\right)\ exp\left(\frac{-t^2}{2\sigma^2}\right) \tag{C.4}$$

where A: amplitude of the pulse; σ: Spread of the pulse

C.3 PWLA approach to Generation of Gaussian Pulse and its first-, third- and fifth- derivative

Table C.7: Eight-segment PWLA Gaussian pulse $G(t)$

PWLA Segments (i)	Voltage breakpoint (v) at time (t)				$slope_i$ (V/ns)	Charge/Discharge		Current Source	
	t_i (ns)	v_i (V)	t_{i-1} (ns)	v_{i-1} (V)		Charge	Discharge	Positive	Negative
1	0.35	0.04	t_{init}= 0.3	v_{init}= 0	0.8	✓		I_1	
2	0.4	0.25	0.35	0.04	4.2	✓		I_2	
3	0.47	0.88	0.47	0.25	9	✓		I_3	
4	0.5	1	0.5	0.88	4	✓		I_4	
5	0.53	0.88	0.5	1	-4		✓		-I_4
6	0.6	0.25	0.53	0.88	-9		✓		-I_3
7	0.65	0.04	0.6	0.25	-4.2		✓		-I_2
8	0.7	0	0.65	0.04	-0.8		✓		-I_1

Table C.8: Thirteen-segment PWLA first-derivative Gaussian pulse $G_1(t)$

PWLA Segments (i)	Voltage breakpoint (v) at time (t)				$slope_i$ (V/ns)	Charge/Discharge		Current Source	
	t_i (ns)	v_i (V)	t_{i-1} (ns)	v_{i-1} (V)		Charge	Discharge	Positive	Negative
1	0.315	0.04	t_{init}= 0.25	v_{init}= 0	0.615	✓		I_1	
2	0.34	0.125	0.315	0.04	3.4	✓		I_2	
3	0.37	0.34	0.34	0.125	7.16	✓		I_3	
4	0.42	0.9	0.37	0.34	11.2	✓		I_4	
5	0.44	1	0.42	0.9	5	✓		I_5	
6	0.46	0.9	0.44	1	-5		✓		-I_1
7	0.54	-0.9	0.46	0.9	-22.5		✓		-I_2
8	0.56	-1	0.54	-0.9	-5		✓		-I_1
9	0.58	-0.9	0.56	-1	5	✓		I_5	
10	0.63	-0.34	0.58	-0.9	11.2	✓		I_4	
11	0.66	-0.125	0.63	-0.34	7.16	✓		I_3	
12	0.685	-0.04	0.66	-0.125	3.4	✓		I_2	
13	0.75	0	0.685	-0.04	0.615	✓		I_1	

Table C.9: Seventeen-segment PWLA third-derivative Gaussian pulse $G_3(t)$

PWLA Segments (i)	Voltage breakpoint (v) at time (t)				$slope_i$ (V/ns)	Charge/Discharge		Current Source	
	t_i (ns)	v_i (V)	t_{i-1} (ns)	v_{i-1} (V)		Charge	Discharge	Positive	Negative
1	0.29	0.05	t_{init}= 0.22	v_{init}= 0	0.714	✓		I_1	
2	0.345	0.24	0.29	0.05	3.45	✓		I_2	
3	0.36	0.27	0.345	0.24	2	✓		I_3	
4	0.375	0.24	0.36	0.27	-2		✓		-I_1
5	0.397	0	0.375	0.24	-10.9		✓		-I_2
6	0.44	-0.88	0.397	0	-2.04		✓		-I_3
7	0.456	-1	0.44	-0.88	-7.5		✓		-I_4
8	0.47	-0.88	0.456	-1	8.57	✓		I_4	
9	0.53	0.88	0.47	-0.88	29.3	✓		I_5	
10	0.545	1	0.53	0.88	8	✓		I_6	
11	0.56	0.88	0.545	1	-8		✓		-I_5
12	0.605	0	0.56	0.88	-19.5		✓		-I_6
13	0.627	-0.24	0.605	0	-10.9		✓		-I_2
14	0.64	-0.27	0.627	-0.24	-2.31		✓		-I_7
15	0.655	-0.24	0.64	-0.27	2	✓		I_3	
16	0.71	-0.05	0.655	-0.24	3.45	✓		I_2	
17	0.78	0	0.71	-0.05	0.714	✓		I_1	

Table C.10: Twenty-two segment PWLA fifth-derivative Gaussian pulse $G_5(t)$

PWLA Segments (i)	Voltage breakpoint (v) at time (t)				$slope_i$ (V/ns)	Charge/Discharge		Current Source	
	t_i (ns)	v_i (V)	t_{i-1} (ns)	v_{i-1} (V)		Charge	Discharge	Positive	Negative
1	0.26	0.025	t_{init}= 0.21	v_{init}= 0	0.5	✓		I_1	
2	0.3	0.061	0.26	0.025	0.9	✓		I_2	
3	0.315	0.045	0.3	0.061	-1.1		✓		-I_1
4	0.33	0	0.315	0.045	-3		✓		-I_2
5	0.37	-0.355	0.33	0	-8.87		✓		-I_4
6	0.385	-0.435	0.37	-0.355	-5.33		✓		-I_3
7	0.4	-0.355	0.385	-0.435	5.33	✓		I_3	
8	0.418	0	0.4	-0.355	19.7	✓		I_4	
9	0.452	0.9	0.418	0	26.5	✓		I_5	
10	0.463	1	0.452	0.9	9.1	✓		I_6	
11	0.474	0.9	0.463	1	-9.1		✓		-I_6
12	0.525	-0.87	0	0.9	-3.5		✓		-I_5
13	0.537	-1	0.525	-0.87	-1.1		✓		-I_1
14	0.549	-0.87	0.537	-1	1.1	✓		I_7	
15	0.582	0.355	0.582	-0.87	2.4	✓		I_8	
16	0.612	0.435	0.582	0.355	5.33	✓		I_3	
17	0.63	0.355	0.612	0.435	-4.44		✓		-I_7
18	0.67	0	0.63	-0.05	-8.87		✓		-I_4
19	0.685	-0.045	0.67	0	-0.045		✓		-I_8
20	0.7	-0.061	0.685	-0.045	-1.1		✓		-I_1
21	0.74	-0.025	0.7	-0.061	0.9	✓		I_2	
22	0.79	0	0.74	-0.025	0.5	✓		I_1	

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List of Publications

Journal Publications

1. B. Jajodia, A. Mahanta and R. A. Shaik, "Mixed-Signal Demodulator for IEEE 802.15.6 IR-UWB WBAN Energy Detection based Receiver", *in IET Circuits, Devices & Systems*, April, 2018. (DOI: 10.1049/iet-cds.2017.0350)

Conference Publications

1. B. Jajodia, A. Mahanta and R. A. Shaik, "A Six-Segment SRRC Pulse Generator for IEEE 802.15.6 WBAN Standard", *BODYNETS 2014 - 9th International Conference on Body Area Networks*, Senate House, London, Great Britain, pp. 46-49, Nov. 2014.

2. B. Jajodia, R. A. Shaik and A. Mahanta, "PPM Demodulation Schemes for IEEE 802.15.6 IR-UWB WBAN Receivers", *2015 IEEE International Conference on Signal Processing, Informatics, Communication and Energy Systems (SPICES)*, NIT Calicut, India, pp. 1-5, Feb. 2015.

3. B. Jajodia, R. A. Shaik and A. Mahanta, "Demodulation techniques for IEEE 802.15.6 IR-UWB DBPSK WBAN transceivers", *2015 IEEE 3rd International Conference on Smart Instrumentation, Measurement and Applications (ICSIMA)*, Putrajaya Marriott Hotel, Malaysia, 2015, India, pp. 1-5, Nov. 2015.