APPLICATION OF REDUCED SWITCH SINGLE DC SOURCE BASED CASCADED H-BRIDGE MULTILEVEL INVERTER FOR POWER QUALITY IMPROVEMENT

A THESIS

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To Maa

and your eternal presence

THESIS CERTIFICATE

This is to certify that the thesis entitled **"Application of reduced switch single DC source based cascaded H-bridge multilevel inverter for power quality improvement"** submitted by **Ramyani Chakrabarty** to the Indian Institute of Technology Guwahati, Guwahati, India for the award of the degree of Doctor of Philosophy is a bonafide record of the research work done by her under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

Increase in load complexity is increasing the deviation of voltage and current from the desired waveform. These undesired characteristics of voltage and current can be termed as power quality issues. Power quality issues not only impact the performance of equipment, but also cause increased losses due to presence of unwanted harmonics. Deterioration of machine health and downtime caused by poor power quality translates to financial losses for the consumer. These issues, along with stringent voltage and current characteristics demanded by various industries, are propelling research in maintaining power quality in distribution system. Distribution static compensator (DSTATCOM) is a shunt connected custom power device which is widely used for load compensation and improvement of power quality. In this thesis, literature review is presented on power electronic inverters and control techniques used for DSTATCOM implementation. For DSTATCOM implementation, multilevel inverters (MLIs) are being preferred over two-level inverters for various advantages like lower switch rating, reduction in $\frac{dv}{dt}$ stress and smaller harmonic distortion. Apart from their various advantages, the multilevel inverters used for realization of DSTATCOM, also exhibit certain drawbacks like large component count, multiple DC-link capacitors and capacitor voltage balancing issues which complicate the design and control of the inverter.

To overcome the drawbacks posed by conventional MLIs, a 7-level reduced switch single DC source based cascaded H-bridge multilevel inverter (RSDCHBMLI) topology is presented in this thesis. RSDCHBMLI utilizes lesser number of switches, operates with single DC source and has no requirement of additional diodes or capacitors. This topology utilizes transformers for generation of stepped waveform, and thus provide inherent isolation between the distribution system and the DSTATCOM. Also, the boosting ability of the inverter leads to proportional reduction in the desired DC-link voltage. As the number of switches in this topology is less than the conventional MLIs, existing multi-carrier pulse-width modulation (PWM)techniques , where the number of carriers is same as number of independent switches, cannot be applied here. To solve this issue, existing PWM technique is modified to work with the developed topology. Subsequently, a single-carrier level shifted pulse width modulation (SC-LS-PWM) strategy is developed in this

thesis which further allows for easier implementation in digital controllers.

The operation of the developed 7-level RSDCHBMLI is implemented in open loop for different values of modulation indices. The inverter operation if analyzed to compute the switching loss and conduction loss in the inverter and also, the calculate the power sharing between the two full-bridge cells that are used for generation of 7-level waveform. In closed loop, both in stand-alone mode and grid connected mode, state-feedback (SFB) control is implemented to attain the control objectives. It ensures stability of the closed loop system and permits simple realization of control objectives. SFB controller combined with SC-LS-PWM results in a constant switching frequency operation that simplifies filter design for RSDCHBMLI. The inverter operation is verified using PSCAD simulations and experiments on a laboratory prototype.

The 7-level RSDCHBMLI is implemented as a DSTATCOM connected to weak distribution system. For load compensation, the RSDCHBMLI is to be operated in current controlled mode. Both SFB current control and finite-control-set model predictive control (FCS-MPC) is implemented for the DSTATCOM control. The performance of RSDCHBMLI based DSTATCOM is compared for both these control techniques. It is seen that using FCS-MPC, the settling time for the source currents is 4 times smaller than that using SFB control. Also, the tracking error of source currents using FCS-MPC control exhibit smaller overshoot under load change. This indicates that FCS-MPC lead to a better dynamic response as compared to SFB control in case of load compensation using RSDCHBMLI based DSTATCOM. In this thesis, a current based DC-link voltage controller is also developed whose gains can be easily computed and also offers better performance than conventional controllers. The operation of the DSTATCOM is further extended for load compensation when the source voltage exhibits both magnitude and phase unbalance. This thesis also performs detailed case studies for DSTATCOM operation under various conditions of loads and source voltages. The operation of the DSTATCOM is verified using detailed simulation in PSCAD/EMTDC environment.

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CHAPTER 1

INTRODUCTION

With advancement in technology, the nature of load connected in the power system is also evolving, with the loads demanding reliable and stringent levels of incoming supply [1]. The increased proliferation of non-linear loads like domestic appliances, workstations, programmable speed drives, energy saving ballasts, computers, compact fluorescent lamps draw harmonic current from the grid [2] which cause distortion in the voltage due to presence of feeder impedance. The distortions in incoming voltage adversely affect sensitive loads that demand stringent regulation of supply, like computerized tomography scanners, various medical equipment, data-center loads, semiconductor processing industry etc [3], [4]. The large number of inductive loads present in the distribution system is responsible for degradation of power factor which leads to increase in the magnitude of current drawn from the supply that can cause voltage dips, along with increase in losses. These issues in the distribution network is drawing attention to improvement of power quality in distribution network. Also, with the appearance of multiple utilities in the deregulated power market, reliability and power quality is emerging as important factors in consumers' choice of utility. Another important domain of power quality improvement is in microgrids where the source impedance tends to be higher. The higher source impedance leads to higher voltage drop due to harmonic distortion and hence power quality improvement techniques become essential for protection of vital loads in microgrid operations [5].

This thesis focuses on power quality problems in the distribution grid and application of power electronic inverters to solve these. It describes usage of a shunt connected multilevel inverter that is operated in current controlled mode to compensate the distortion and unbalance caused by unbalanced and non-linear loads in the distribution network. In this chapter, various power quality issues and their impacts are discussed. Building upon the discussion of power quality, use of Distribution Static Compensator (DSTATCOM) for power quality improvement in the distribution network is presented. The DSTATCOM is a power-electronic converter that is operated in current controlled mode to achieve load compensation. This chapter presents a literature review on the

inverter topologies and control strategies that are used for DSTATCOM realization. Based on the literature review, the issues present in multilevel inverter topologies are highlighted and the objectives of the thesis are accordingly formulated. This chapter also presents the organisation of the thesis.

This chapter is organized into five sections. In Section 1.1, the relevance of power quality is discussed. The second section, Section 1.2 presents a literature review of the power electronic converters and controls with respect to power quality applications. In Section 1.3, the motivation is detailed, followed by the objectives of the thesis in Section 1.4. The final section of this chapter, Section 1.5, details the organization of the thesis.

1.1 Power Quality

In general terms, power quality can be expressed as the ability of supplying power to customers with minimum distortion and interruption. IEEE defined power quality as “The concept of powering and grounding electronic equipment in a manner that is suitable to the operation of that equipment and compatible with the premise wiring system and other connected equipment. Utilities may want to define power quality as reliability” [6]. The resemblance of a practical supply system with the ideal one can be expressed in terms of power quality [7]. Power quality issues can also be defined in general terms as "any occurrence manifested in voltage, current, or frequency deviations that results in damage, upset, failure, or mis-operation of end-use equipment" [4]. With increase in complexity and interconnection of various sensitive loads, regulations pertaining to power supplied to the customers are tightened which is drawing attention to the issue of power quality in the distribution network. Extensive use of equipments like programmable logic controllers, adjustable speed drives, energy efficient lighting, power electronic converters introduce distortion in voltage and current profile due to their non-linearity. Such distortions cause detrimental effects on digital controllers. These can also result in erroneous operation of protection systems leading to unwanted tripping of breakers. Presence of harmonic currents on the utility distribution system may lead to interference in communication circuits sharing the common path. Voltages induced due to common harmonic currents generally lie within the bandwidth of voice communications, causing interference. Current flowing due to inductive coupling in

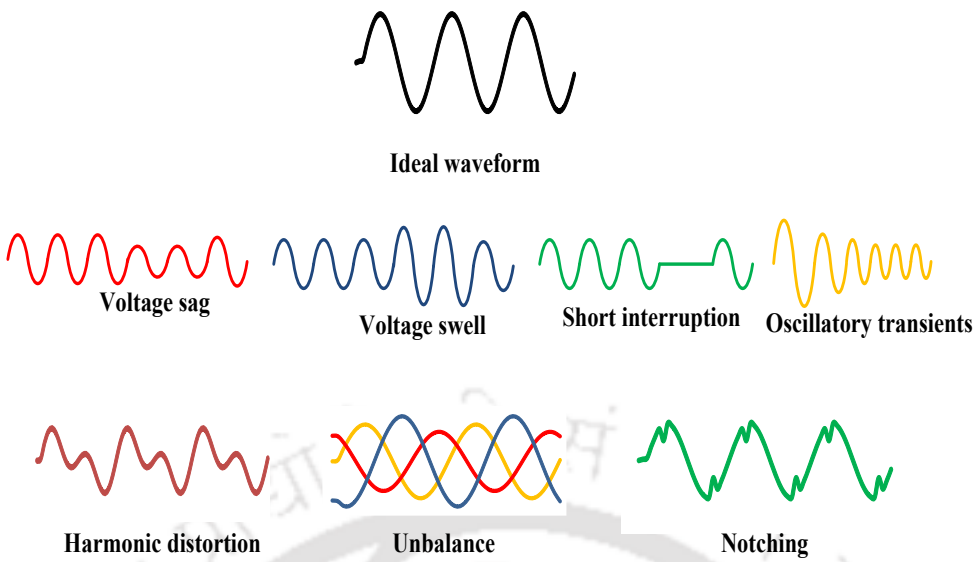


Fig. 1.1 Representation of some power quality problems

the shield of telephone communication cable cause potential differences in the ground references at the end of the cable [8]. Further, deregulation in distribution system is creating a competitive environment where quality of power delivered by the utilities is emerging as an important parameter of customer choice. The emergence of micro grids, with large amount of non-linear loads and comparatively higher source impedance, is also prone to large voltage drops due to harmonic distortions. This makes power quality an important issue in microgrid operations also [9].

1.1.1 Power Quality Issues

The sources of poor power quality can be broadly classified into two categories: usage of loads, components and equipments by the consumer that degrade power quality form the first category while the subsystems of transmission and distribution systems constitute the other [10]. While almost all power quality issues arise in the distribution network [11], some of the commonly found power quality issues [12] are shown in Fig 1.1. A brief description of these power quality issues are also given below:

- **Voltage Sag:** It refers to decrease in normal voltage level to $10-90\%$ of nominal voltage at power frequency, for duration greater than 10 ms but less than 1 s. Voltage sags can be caused by energization of large load, starting of large motors and single line to ground faults [10].

- **Voltage Swell:** It refers to increase in voltage level to 110% to 180% of its nominal value for duration greater than 10 ms but less than 1 s. Sudden removal of large load from the network, energization of capacitor banks are some common causes of voltage swell. It is also seen in the unfaulted phase during occurrence of single line to ground faults [10].

- **Interruption:** Interruptions can be short duration interruptions or sustained interruptions. During short interruptions, the voltage level falls below 10% in the bus for a time period ranging between 10 ms to 1 minute. For long interruptions, the bus voltage falls to zero for a time greater than 1 minute. Interruptions are generally caused by faults, breaker opening or equipment failure [8].

- **Oscillatory transients:** These are damped oscillation with frequency ranging between a few hundred Hertzs to Megahertzs. Oscillatory transients with frequency component less than 5 kHz with a typical duration between 0.3 to 50 ms is characterized as low frequency transient. When the frequency of transient ranges within 5 to 500 kHz and its duration is limited to 20 μs, it is medium frequency oscillatory transient. High frequency oscillatory transients are characterized with frequency ranging between 0.5 to 5 MHz, and duration of 5 μs. Oscillatory transients can be caused by back to back capacitor energizations, cable switching and also as a local system response to oscillatory transients [8].

- **Harmonic Distortion:**Voltage and current assume a non-sinusoidal shape due to presence of components having frequencies which are multiples of power frequency. Harmonics occur in steady state and are caused by non-linear loads. Harmonics are characterized using the complete harmonic spectrum with magnitude, angle and frequency of each component. Total harmonic distortion (THD) and total demand distortion (TDD) are used to express the effective value of harmonics distortion [1].

- **Unbalance:** A voltage or current variation in three-phase system where magnitude of the phases and/or angle between them are not equal is categorized as unbalance. Typically, unbalances are characterized using symmetrical components. The ratio of negative sequence component to positive sequence component is taken as a measure of unbalance. Unbalances, usually less than 2% can be caused by single-phase loading in three-phase systems, blown out fuse on one

phase of a capacitor bank. Single phasing conditions generate severe unbalance that is higher than 5% [8].

- **Notching:** It is a periodic voltage distortion seen during commutation of power-electronic converters. The frequency associated with notching is much higher than harmonics. The high rate of rise of voltage encountered during notching may cause damage to capacitive components [1].

Poor power factor of load also contributes to power quality issues as the power factor correction equipment in the form of capacitor banks act as causes of over-voltage conditions and also transients. Thus the solutions for power quality improvement also simultaneously focus on power factor correction of the current drawn from the source. Voltage fluctuations, spikes, and interruptions also cause power quality problems.

1.1.2 Financial Impact of Poor Power Quality

Poor power quality adversely impacts customers and network suppliers. Financial losses are the ultimate consequence of poor power quality. Industrial customers are more vulnerable to voltage magnitude variations and interruptions. Continuous manufacturing industries, semiconductor production industries, medical equipments have stringent power quality requirement for their operation. Voltage magnitude variations cause enormous financial losses in these industries [13]. Poor power quality leads to premature ageing of machines, increases losses and makes them more susceptible to faults. Induction motors, which account for 96% of the total electrical energy consumed by motors, are highly affected by poor voltage quality and harmonic distortion. Voltage sags cause higher copper losses in the machine, temperature rise and reduction of efficiency. It causes torque transients that may damage the shafts. Unbalance and harmonics in supply voltages increase thermal stresses in the machine. Condition monitoring of induction machine has to be done to predict probability of machine breakdown. If power quality of the supply is maintained then efficiency of the machine increases. Also the cost associated with machine maintenance, condition monitoring can be significantly reduced along with reduction of downtime in the industry.

Surveys have been performed to ascertain the cost of power quality problems in various countries. In the countries of European Union, €151.2 billion is annually lost

for poor power quality issue [14]. In USA, survey done in 2002-2003 pin this cost to $ 150 billion per year. In India, no comprehensive data regarding the financial loss is available. Asia Power Quality Initiative has estimated the direct cost of downtime in India to be Rs.20000 crore per annum, 57% of which occur due to voltage sags and interruptions. Thus, apart from technical benefits of harmonics reduction and distortion cleaning, maintaining good power quality results in financial gains in terms of reduction in monitoring costs, machine failures and total downtime [15].

1.1.3 Solution to Power Quality Issues

In this part, the solutions available for the various power quality problems discussed above are summarized. A popular approach towards solution of these issues is usage of custom power devices (CPDs). Custom power devices are applications of power electronic converters in the distribution system to enhance the quality and reliability of power delivered to the customers. CPDs can be of two types [16]:

- **Network re-configuring type:**

  Network reconfiguring type custom power devices are used mostly during occurrence of faults. Solid State Current limiter (SSCL), Solid State Circuit Breaker (SSCB) are used for fast limiting and breaking of the fault current. SSCB is also equipped with auto re-closing function. Solid State Transfer Switch (SSTS) is another type of network re-configuring device that protects load by transferring them to a healthy feeder in less than a cycle's time.

- **Compensating type:**

  Compensating type devices are mostly used for load compensation, active filtering and voltage regulation. These can also mitigate unbalance in the system, generating a balanced voltage/ current profile, along with compensating for poor power factor. The compensating type of devices include:

  - **Distribution static compensator (DSTATCOM):** The schematic of an ideal DSTATCOM for load compensation is shown in Fig 1.2. The DSTATCOM is a shunt connected compensating device which is usually realized using a voltage source inverter. As the inverter is operated in current controlled

mode to inject desired current for load compensation, the DSTATCOM here is represented using a current source. In the absence of load compensation, the current i_s is non-linear due to non-linear load present at bus 2. The DSTATCOM should inject current i_f into the system such that current i_s becomes sinusoidal so that the load behaviour connected at bus 2 doesn't distort the voltage available at bus 1. Also, load compensation can make i_s in phase with bus 2 voltage.

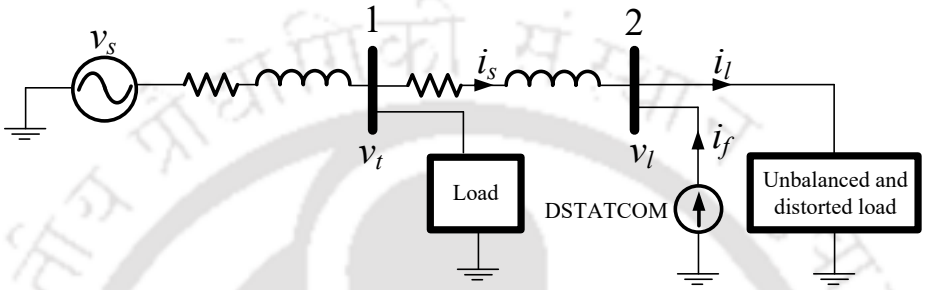


Fig. 1.2 Schematic of an ideal DSTATCOM for load compensation

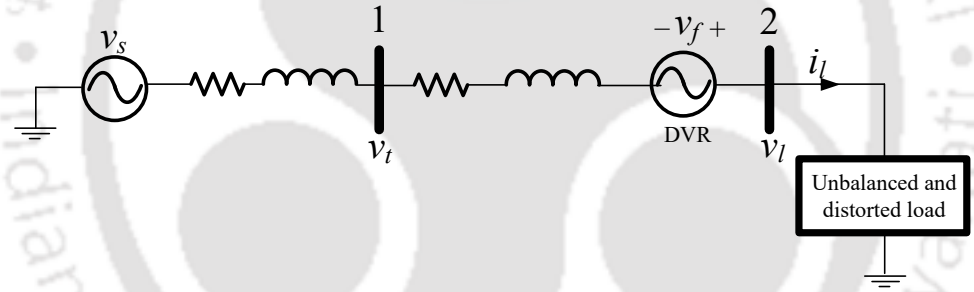


Fig. 1.3 Schematic of an ideal DVR for protection of sensitive loads

– **Dynamic voltage restorer (DVR):** The schematic of an ideal DVR is shown in Fig 1.3. DVR performs series compensation and is used to protect sensitive loads from variations and disturbances in supply voltage. The DVR is represented using a ideal voltage source which is capable of regulating the bus voltage v_t at a desired value by supplying v_f.

– **Unified power quality conditioner (UPQC):** UPQC provides the benefit of both series and shunt compensation. The schematic of an ideal UPQC compensated system is shown in Fig. 1.4. It can regulate the bus voltage v_l to be sinusoidal and also make the current i_s drawn from the source to be sinusoidal and in phase with the terminal voltage v_t. The inverter realizing both the shunt and series compensation devices are supplied from the same DC capacitor.

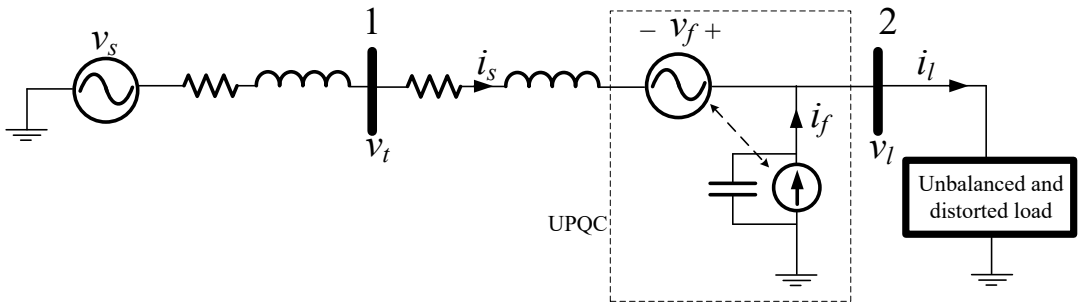


Fig. 1.4 Schematic of an ideal UPQC for compensation of voltage and current

1.2 Literature review

Among the compensating type of devices used for power quality improvement, DSTATCOM is most commonly implemented in the distribution system. It is a shunt connected device and is capable of performing load compensation. It is usually connected at the load terminals and can nullify the effect of unbalanced load, resulting in balanced and sinusoidal currents being drawn from the source. It can clean the distortions introduced in the source currents by non-linear and power electronic loads. DSTATCOM can also cause the source currents to have a desired power factor. Fig.1.5 shows the schematic of a DSTATCOM connected to the load bus. DSTATCOM is a power electronic inverter which can be operated in voltage controlled or current con-

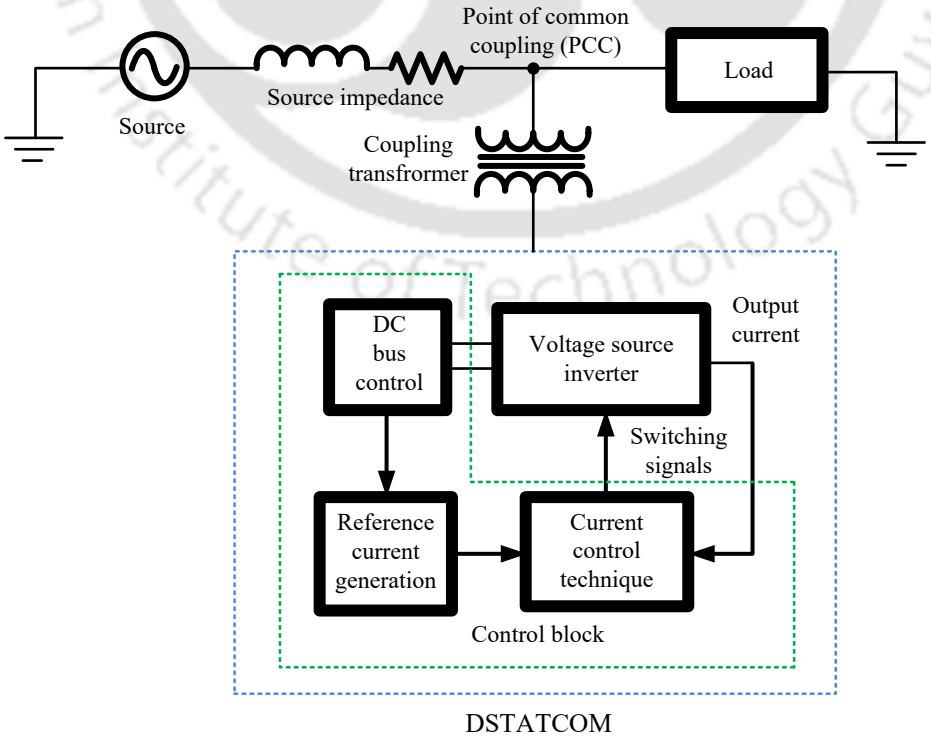


Fig. 1.5 Structure of DSTATCOM connected at the point of common coupling for load compensation

trolled mode to mitigate various power quality issues faced in the distribution network. The DSTATCOM operated in current controlled mode is implemented for performing load compensation in the distribution system. Thus the two broad parts of DSTATCOM implementation are

1. Power electronic inverter which is usually a voltage source inverter (VSI) operated in current controlled mode.
2. The control of DSTATCOM, which can be further sub-divided in to three parts:
   (a) DC bus voltage control
   (b) Inverter current control
   (c) Reference source current generation

The objective of the VSI is to generate a three-phase AC voltage from the DC source using a suitable current compensation technique such that the compensator current tracks the desired reference current. The desired reference compensator current is calculated using reference source current generation algorithm to achieve desired control objectives. For load compensation, DSTATCOM is usually operated in current controlled mode. In current controlled mode, the reference current to be supplied by the DSTATCOM has to be first calculated. The DSTATCOM should be able to supply the reactive and distorted part of the load current such that the current drawn from the source is sinusoidal and unity power factor. The desired source current is obtained from the basis that the source current shall be responsible only for supplying the real power to the load. The compensator current is obtained by subtracting the reference source current from the actual load current. After obtained the reference DSTATCOM current, switching signals for VSI the are generated such that the output current tracks the reference current. As the DSTATCOM is not required to supply any real power to the load, the DC voltage source for the VSI is realized using a capacitor and the DC bus voltage control is implemented to maintain the voltage across the DC-link capacitor at the required value.

1.2.1 Voltage Source Inverter

Voltage source inverters used to realize DSTATCOM can be of varied topologies. It can be either a two-level inverter or a multilevel inverter (MLI). A schematic representation of two-level inverter and an N-level MLI is shown in Fig. 1.6. In conventional two-level inverters, the output of one leg of the inverter varies between $+V_{dc}$ and 0, or $-V_{dc}$ and 0. For MLIs, the output for one leg of the inverter is a stepped waveform. The schematic representation of multilevel waveform for various cases is shown in Fig 1.7. The number of steps in the output voltage depend on the topology of the inverter and the modulation index at which the inverter is operated. V_{dc} is the input DC-voltage of the inverter and k is a fraction which depends on the inverter design. If $k = 1$, then the inverter exhibits boosting function, for $k < 1$, the inverter output never exceeds the input DC value. MLIs are now-a-days extensively used because of their numerous advantages. MLIs have a staircase output waveform and hence lower distortion. They have lower dv/dt stress. The switching frequency is lower as com-

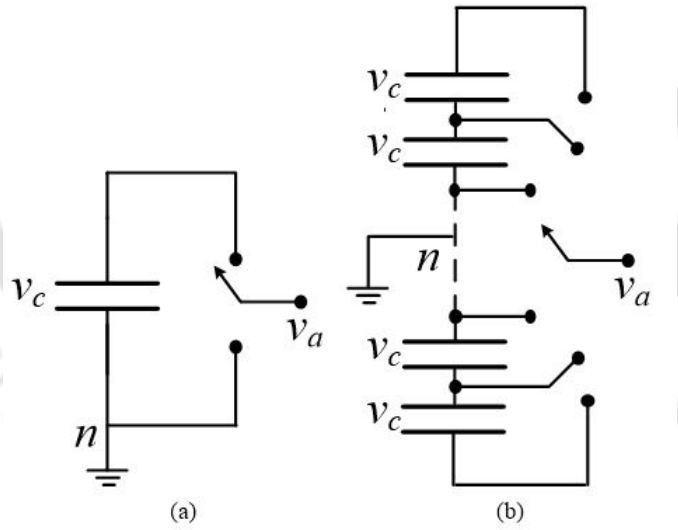


Fig. 1.6 Schematic representation of: (a) Two-level inverter (b) Multilevel inverter

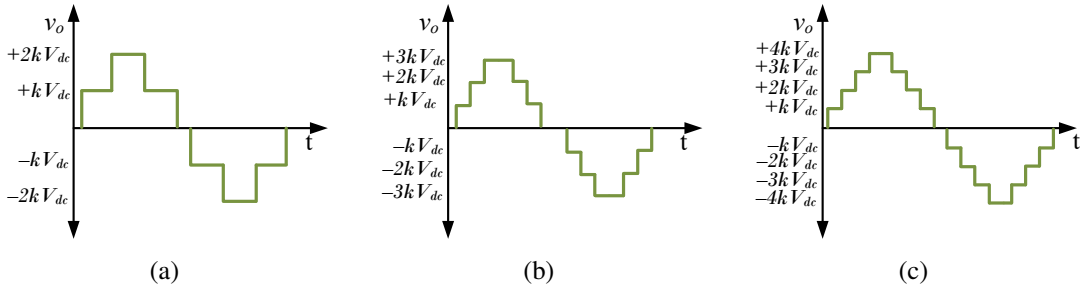


Fig. 1.7 Multilevel inverter output voltage: (a) 5-level output (b)7-level output (c) 9-level output

pared to their two-level counterparts, but increase in number of switches lead to higher cost and control complexity. These drawbacks are outweighed by their advantages and MLIs are increasingly dominating over two-level inverters in medium and high voltage application [17]. In the next part, some conventional and recent topologies of MLIs are described along with their advantages and disadvantages for application in load compensation.

A. Neutral Point Clamped Inverter

Neutral point clamped multilevel inverter (NPCMLI) is one of the earliest MLI proposed in 1981 [18]. Fig.1.8 shows one phase leg of a 5-level neutral point clamped inverter. The inverter legs consist of eight switches (S_{1p}, S_{1n}), (S_{2p}, S_{2n}), (S_{3p}, S_{3n}), (S_{4p}, S_{4n}) that form complimentary switching pairs. Since the diodes clamp voltages across the switches, this configuration of MLI is also termed as the diode clamped multilevel inverter (DCMLI). A description of NPCMLI and their application is available in [19]. For an N-level inverter, number of DC bus capacitors required is $(N-1)$. The voltage across each DC bus capacitor is then $\frac{V_{dc}}{(N-1)}$. The clamping diodes limit voltage stress across each switch to the voltage across one DC capacitor. NPCMLI is in use since 1980s for its various advantages like reduction of switching stress and availability of common DC bus configuration. Here five switching combinations generate five

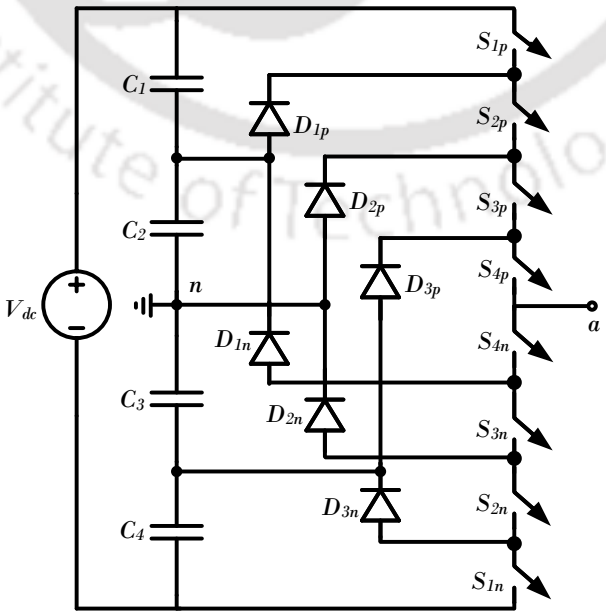


Fig. 1.8 One phase leg of 5-level neutral point clamped inverter

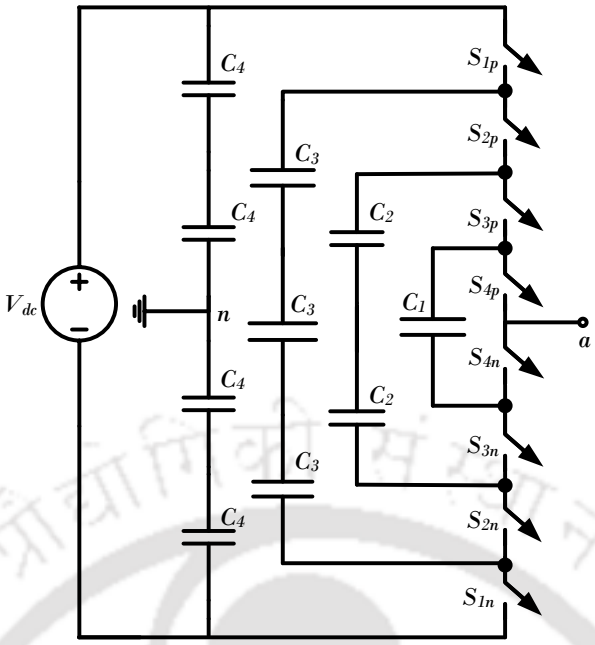


Fig. 1.9 One phase leg of 5-level flying capacitor multilevel inverter

voltage levels and no redundant switching states are available. Also, due to unsymmetrical semiconductor loss distribution, unbalance in capacitor voltages can occur which impacts its operation. NPCMLIs have also been applied for load compensation and active filtering [20], [21]. Though NPCMLI requires a very simple protection circuit, the requirement of diodes and its layout restrict the number of levels to five. Also, additional circuitry is required for capacitor voltage balancing [22], [23] which is vital for its operation as a DSTATCOM.

B. Flying Capacitor Multilevel Inverter

A flying capacitor multilevel inverter (FCMLI) was proposed in 1992 by Meynard and Foch [24]. The schematic representation of a single-phase FCMLI is shown in Fig 1.9. This topology differs from diode clamped structure in the fact that here clamping diodes are replaced with capacitors. Capacitors are used to limit voltage stress across the power electronic devices. The eight switches form four complimentary switching pairs. The complimentary pairs $(S_{1p}, S_{1n}), (S_{2p}, S_{2n}), (S_{3p}, S_{3n}), (S_{4p}, S_{4n})$ are arranged as shown in Fig 1.9. This arrangement is done to prevent short circuiting of the flying capacitors. One of the major advantages of this topology is the availability of multiple switching combinations for synthesis of a particular voltage level. This redun-

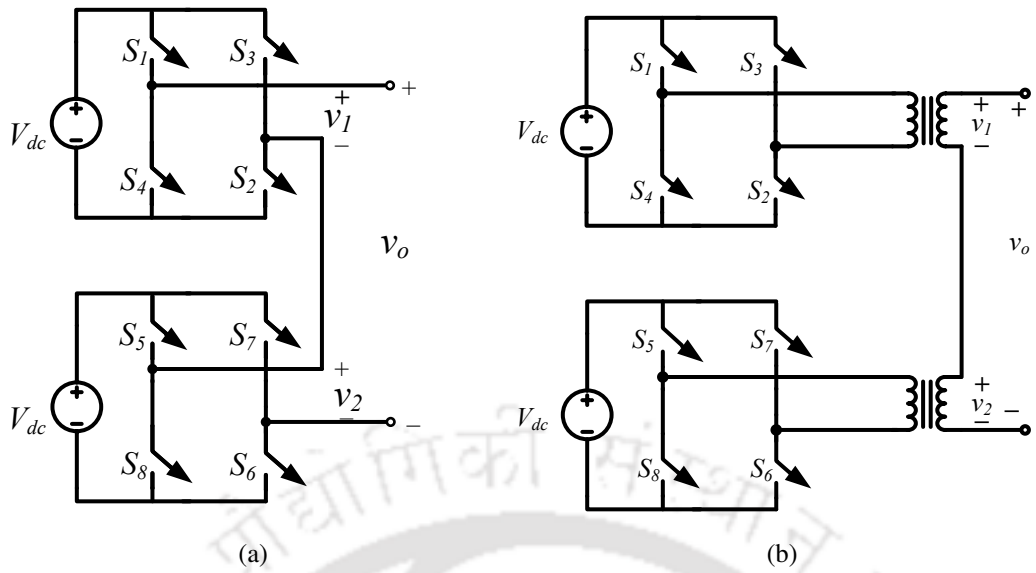


Fig. 1.10 One phase leg of a 5-level cascaded H-bridge multilevel inverter: (a) Conventional topology (b) Modified topology with transformers

dancy is exploited for capacitor voltage balancing when it is used as a DSTATCOM. While this eliminates the requirement for auxiliary voltage balancing circuitry, the requirement of large number of capacitors increases the cost and size of FCMLI [21], [25].

C. Cascaded H Bridge Multilevel Inverter

Cascaded H bridge multilevel inverter (CHBMLI) is formed by connecting multiple full-bridge inverters in series. If an N-level output is desired, $\frac{(N-1)}{2}$ full-bridge inverters are required. The output multilevel waveform is generated by a series combination of the voltage outputs of individual inverters. This topology has no requirement for clamping diodes or capacitors. It has a modular structure, is reported for levels greater than five [26], and can be scaled up for a transformer-less connection with the distribution grid. Each individual inverter here requires a separate DC source which can be either stand alone DC source or supplied from isolated windings of three-phase transformers. Such usage of isolated DC sources complicate the voltage regulation loop. In case of DSTATCOM implementation, where the DC sources are replaced with DC-link capacitors, voltage balancing among the capacitors pose difficulties in the inverter operation and control. This act as a deterrent for its application in load compensation [27], [28].

To overcome the problem of voltage balancing among the capacitors used in

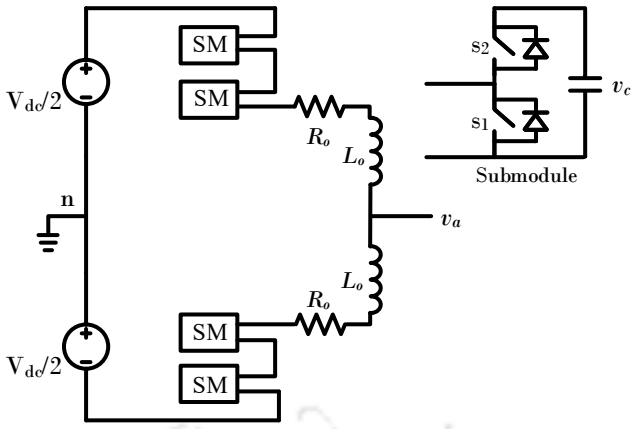


Fig. 1.11 One phase leg of 5-level modular multilevel inverter

different inverter modules, a modified topology of the CHBMLI was proposed in [29]. It made use of cascade connection of transformers to generate the multilevel wave form.

D. Modular Multilevel Inverters

Modular multilevel inverters are one of the newest addition to the family of MLIs. It was proposed by Glinka and Marquardt [30]. Fig. 1.11 shows one leg of a 5-level modular multilevel inverter. Each leg consists of two arms. Each arm has identical number of sub-modules. The sub-modules can be composed of different inverter topologies like full bridge, half bridge, clamp double circuit, three-level inverters, etc [31]. The sub-modules are connected in series with each other. An interfacing inductor is used which can suppress the high frequency components in the arm current. Modular MLIs have a high scalability and modularity. It has better harmonic performance than other inverters and a lower switching frequency. The voltage balancing problem among the capacitors of the different sub modules is one of the challenges of its applications. Application of modular multilevel inverters in reactive compensation have been reported in [32], [33]. Most of the modular multilevel inverters reported use half bridge inverters as the sub module because of reduction in number of components and hence reduced losses.

E. Recent modifications in MLI topology

To overcome the problems posed by the conventional MLIs, newer topologies of MLIs are being reported in the literature [34]–[40]. In [34], [36], the topology is

modified to reduce the number of semiconductor switches. To generate stepped multilevel waveform, [34] utilizes multiple DC-link capacitor, while the topology presented in [36] uses series capacitors. In these two topologies, the generation of the multilevel waveform is affected by capacitor voltage balancing. Thus auxiliary control strategy is required for these topologies. In [35], a self balancing MLI topology is presented, along with a reduction in the component count. It utilizes a voltage doubling network of half-bridge in augmentation with the main inverter structure to increase the number of steps in the output voltage. Here, the requirement of large sized capacitors for the DC bus, along with multiple DC sources make the inverter design and operation complicated. In [39], [40], flying capacitors are used to generate multilevel waveform. In [39], three floating capacitors per phase are used while [40] uses one flying capacitor per phase and two DC-link capacitors. In both inverters switching state redundancies are exploited for balancing and control of capacitor voltages. A CHBMLI based topology is reported in [38] where switched capacitors are used for voltage boosting. In this topology, the number of power electronics switches remain same as in conventional MLIs, and the voltage stress across the switches are higher than the input voltage. This topology also requires additional circuit for capacitor charging. Another single DC source based CHBMLI topology is described in [37]. Here, MLI waveform is generated by charged capacitors connected in series with the DC source. The total number of switches required for generating an N-level output is given as $\frac{(5N-7)}{2}$, which is higher than the number of switches required in conventional MLIs, and number of series capacitors are $\frac{(N-3)}{2}$. The voltage stress across each switch is limited to input DC voltage.

Thus, from the review of the state of art of MLI topologies, it can be seen that a number of newer MLIs are coming up that attempt to solve different issues present in conventional MLI topologies. The conventional MLIs require large number of diodes, capacitors and isolated DC-links to generate a multilevel waveform [21], [22], [26], [41]–[45]. The recently reported multilevel inverters, [34]–[36] explore different topologies where number of components are reduced as compared to that of the conventional ones. Another important factor is the usage of multiple DC-link capacitors or isolated DC sources for generation of stepped waveform. The usage of multiple isolated DC sources are seen in [41], [26], [45], [35]. The usage of multiple DC-link capacitors are seen in [21], [22], [36], [42]–[44], [46]. In all these topologies, the problem of capacitor voltage balancing poses challenge in the realization and operation of DSTAT-

COM. In many topologies, apart from the DC-link capacitors, multiple capacitors are used for generation of stepped waveform [21], [37], [38], [44], [46]. In [37], [38], pre-charging of capacitors are required. Though certain topologies like [35], [37], [38] are self-balancing, in other topologies like [36], [41], redundant switching combination is used for capacitor voltage balancing. The balancing of neutral point in [42] is done using zero-sequence combination while capacitor voltage balancing in DCMLI [43] is done with additional chopper circuit.

1.2.2 DC Bus Voltage Control

Voltage source inverters used for modelling of DSTATCOM require a DC source for DC to AC conversion. As the DSTATCOM supplies only the reactive and harmonic power demand of the load, the DC source for the inverter is realized using a capacitor. The voltages of DC bus capacitors have to be regulated at their reference values for proper operation of the DSTATCOM. DC bus voltage determines the amount of compensation possible at the point of common coupling (PCC). Since terms associated with DC bus voltage is utilized in deriving reference currents, improper DC bus voltage leads to errors in reference current generation. Also, transients that occur in the bus voltage during load change should die out fast to ensure stable operation. Usually PI controllers are used for DC bus voltage regulation. Classical PI controllers suffer from drawbacks like slow transient response and calculation of controller parameters by trial and errors. Various literature are available on different methods of improving the controller response, and a short survey on these methods are presented here.

A discrete derivative control is proposed in [47]. Here the error between the desired and actual DC bus voltage, V_{dc}^{*} and V_{dc} is sampled at discrete time intervals. The difference between the errors at consecutive sampling instants is also calculated.

$$e_1(k) = V_{dc}^{*}(k) - V_{dc}(k) \tag{1.1}$$

$$e_2(k) = e_1(k) - e_1(k-1) \tag{1.2}$$

e_1, e_2 are scaled by constants α_e and α_c respectively so that their magnitudes lie in the same numerical range. These values are used to obtain the weighing functions w_e and w_c. E_{max} and E_{cmax} denote the maximum allowable values of the scaled errors. ρ is a

small number that is used to maintain a finite value of the weighing functions in events of errors and their differences approaching 0.

$$E = \alpha_e * e_1, \ |E| \leq E_{max} \tag{1.3}$$

$$E_c = \alpha_c * e_2, \ |E_c| \leq E_{cmax} \tag{1.4}$$

$$w_e = \frac{|E|}{(|E| + |E_c| + \rho)} \tag{1.5}$$

$$w_c = \frac{|E_c|}{(|E| + |E_c| + \rho)}$$

The weighing functions in combination with E, and E_c generate the control law which is then fed to the PI controller. The output of the controller, p_{loss} indicates the amount of active power that should be drawn by the DC bus to maintain its desired voltage level.

$$w = w_e * E + w_c * E_c \tag{1.6}$$

$$p_{loss} = K_{pd}\Sigma w + K_{id}\Sigma w \tag{1.7}$$

This algorithm of DC bus voltage control suppresses the initial transients in the DC-link voltage. It leads to faster response, reduces steady state error and fluctuations of the DC bus voltage under dynamic load situation. Determining the scaling factors and maximum allowable error and error difference impacts it performance.

Another technique for improving the DC bus voltage control is provided in [48]. In this method, amount of energy required by the DC bus capacitor to attain the desired voltage level from its current state is utilized.

$$W_{dc} = \frac{1}{2} C_{dc} (V_{dc}^{*\,2} - v_{dc}{}^2) \tag{1.8}$$

$V_{dc}^{*\,2}$, $V_{dc}{}^2$ are provided as inputs to the PI controller. Considering T_c as the time period of DC capacitor voltage ripple, authors have also derived the controller parameters K_p, K_i as follows:

$$K_p = \frac{C_{dc}}{2T_c}; \quad K_i = 0.5K_p \tag{1.9}$$

p_{loss}, the amount of power to be drawn by the DC bus is given by the controller output.

$$p_{loss} = K_p(V_{dc}^{*\,2} - V_{dc}{}^2) + K_i \int (V_{dc}^{*\,2} - V_{dc}{}^2) \tag{1.10}$$

As the name suggests, this controller gives a faster response as compared to conventional controller. To get similar response using a conventional controller, the controller gains required are very high. Also, the ripples in v_{dc} should be negligible for comparable implementation in a conventional controller.

Other methods like adaptive droop control [49], fuzzy logic controllers [50] have also been utilized for DC bus voltage control.

1.2.3 Current Control Techniques

The voltage source inverter is to be operated in closed-loop current controlled mode to realize its functionality as a DSTATCOM. Different current control techniques for DSTATCOM control are available in the literature. The main concerns in choosing a current control technique are ease of application, stability of the system, robustness in face of parameter variations, dynamic response, and switching frequency. In the following sections, brief descriptions of some commonly used current control techniques are presented.

A. Hysteresis control

It is one of the most common current controlled techniques used in DSTATCOM control [25], [26]. Here the measured current, i and reference current, i^* , is compared to get the error. The error is then compared with hysteresis band, h, to generate the switching signals. While hysteresis control generates fast response with a continuously spread harmonic spectrum, it leads to variable switching frequency. One serious drawback of hysteresis control is that it cannot ensure stability in systems with feeder impedance.

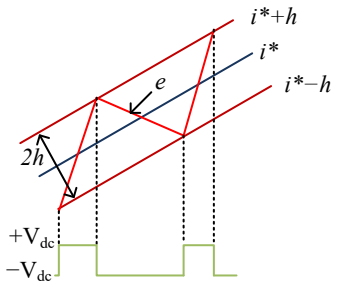


Fig. 1.12 Switching signal generation with hysteresis control

B. Deadbeat control

Deadbeat control [51], [52] is one of the earliest predictive controls used. Here, the discretized state space model is used in deriving the control law. The control law aims to nullify the error at the end of each sampling instant. Deadbeat control technique is highly sensitive to variations in the current loop parameters. It gives a fast convergence with variable switching frequency.

C. State feedback control

State feedback control for DSTATCOM operation is reported in [21], [53]. The state space model of the system is used to solve the algebraic Ricatti equation:

$$0 = \mathbf{A}^T\mathbf{P} + \mathbf{PA} - \frac{\mathbf{PBB}^T\mathbf{P}}{r} + \mathbf{Q} \tag{1.11}$$

A is the state vector, **Q** is a symmetric positive definite matrix and r is a positive scalar that penalizes the maximum control action. The equation is solved to obtain **P** which is then utilized to compute the gain matrix $mathbfK$. This gain matrix is multiplied with the errors of state variables to generate the control law u_c.

$$\mathbf{K} = \frac{\mathbf{B}^T\mathbf{P}}{r} \tag{1.12}$$

$$u_c = -\mathbf{K}(\mathbf{X} - \mathbf{X_{ref}}) \tag{1.13}$$

It is a robust control with large gain margin and phase margin. State feedback control ensures the stability of closed-loop systems. Another important feature is that it can handle input non-linearities.

D. Sliding mode control

Sliding mode control is an useful technique for higher order systems. Initially, a sliding surface,which is time varying, is defined. The aim of the control law is to converge the system states to the sliding surface. The sliding surface is generally defined as a line. The system states should continue to be in the sliding line for all ($t > 0$). Sliding mode control have been utilized for current control of VSI to achieve load compensa-

tion [54], [55]. This control technique is robust to parameter variation, but difficulty may arise in initial convergence of the system states to the sliding line.

E. Ramp comparison control

In this method, the current error is compared with a triangular carrier to generate switching signals for the inverter switches. Ramp comparison control technique makes the switching frequency same as that of the carrier. The amplitude of the carrier wave is determined by the maximum error that can be allowed in the actual current [56]. The choice of the carrier frequency should be done so as to prevent over crossing and under crossing effects. An improper carrier frequency will cause the switching frequency to deviate from the constant value.

F. Model predictive control

Model predictive control determines switching states depending on the prediction of error. Application of Finite Control Set Model Predictive Control (FCS-MPC) in power electronic converters is increasing with enhancement of computing capabilities of modern systems. In this technique, a cost function is defined. For a single objective MPC, the cost function can be defined as

$$g = |i^*(k+1) - i(k+1)| \tag{1.14}$$

where, $i^*(k+1)$ is the reference current and $i(k+1)$ is the current for a possible switching combination. FCS-MPC determines the cost function for every allowable switching combinations upto the prediction horizon. The switching corresponding to the minimum value of error is applied [57], [58]. The algorithm is simple and doesn't require a modulator. It particularly relevant in multi-variable systems and also allows easier inclusion of non-linearities. The cost function of FCS-MPC can include multiple objectives. Calculation of weighing factors in multi-objective FCS-MPC poses challenge. This technique is affected by change in plant parameters. Another drawback of the method is generation of signals with variable switching frequency.

1.3 Motivation

Based on the literature review of the multilevel inverters presented in Subsection 1.2.1, it can be seen that the major challenges in multilevel inverters are:

- Most of the MLI topologies require large number of diodes, capacitors and switches for their design. The component requirement increase with the increase in levels of the output voltage.
- In absence of boosting ability in most of the MLI topologies, connection to medium voltage distribution system demands switches with higher rating.
- Usage of multiple isolated sources or multiple DC capacitors that require additional controls or circuits for voltage balancing, which increases the complexity of design and control, particularly when these topologies are utilized for DSTATCOM realization.
- The conventional MLI topologies do not have inherent isolation in their design and hence, additional isolation transformers are required in their usage.

Among these issues, the main hindrance in DSTATCOM applications of MLIs, is the issue of capacitor voltage balancing. Though many self balancing topologies are present, the usage of multiple DC capacitors and DC sources in them also pose a problem as the charging currents for the multiple capacitors will be drawn from the distribution system itself. The size and cost issues also limit their applications for power quality improvement and small scale grid integration.

In this thesis, the motivation is to develop a simple and modular topology of the multilevel inverter which can overcome the issues of capacitor voltage balancing, multiple capacitor charging and also increase the number of levels without increasing the component count. For this, the transformer based CHBMLI topology presented in [29] is considered and modified to increase the number of levels in the output voltage. The developed topology is termed as reduced switch single DC source based CHBMLI (RSDCHBMLI) topology in this thesis.

The next step in the operation of the modified CHBMLI topology is the pulse-width modulation of multilevel inverter. Due to reduction in number of switches, the

conventional multi-carrier modulation techniques [59] cannot be directly applied to this topology. For this, a modified modulation technique is needed that generates a multi-level output voltage with constant switching frequency. Also, for ease of implementation of the controller in digital signal processing (DSP) platform, further simplification of the pulse-width modulation technique should be done.

As MLIs are also utilized for integration of distributed generation with the grid, and in stand-alone systems for voltage control, the performance of designed MLI should also be tested in stand-alone voltage controlled mode and grid connected mode. In grid connected mode, the MLI should be capable of injecting desired real and reactive power into the grid. Further, as the literature review discussed the application of MLIs for DSTATCOM operation, the designed topology is utilized to realize a DSTATCOM for load compensation in the medium voltage system.

The literature review also presents an overview of different control techniques that are utilized for control of inverters, particularly for load compensation. Though hysteresis is the most commonly applied technique, it is seen that it cannot ensure stability in the higher order systems, and also generates variable switching frequency operation. For choice of the control technique, the desired requirements are ease of application, stable operation and constant switching frequency that enables easy design of filter, and good tracking of the reference voltage or current quantities. To attain these objectives, the control law chosen in this thesis is the state-feedback (SFB) control law for both voltage and current control. In case of state-feedback control, though stability of the closed-loop system is ensured, the issue of variable switching frequency remains. The tracking performance of the SFB control is further improved by augmenting SFB controller with additional terms for reference tracking. The SFB control is further modified to work with a constant switching frequency.

The next section in DSTATCOM operation is the DC bus voltage controller. This is responsible for maintaining the required voltage across the DC-link capacitor for DSTATCOM operation. Generally PI controllers are utilized calculate the power required for maintaining the DC-link voltage and supply the losses in DSTATCOM. As the PI controller gains are generally tuned manually by observing the system response at different values, it becomes difficult and time-taking. To work around this problem, a current based DC-bus voltage controller is also explored in this thesis where the

controller gain parameters are calculated from the system parameters.

Thus, the motivation of this work is to investigate the operation of RSDCHBMLI topology, that uses a single DC-link capacitor along with reduction in the component count. This topology aims to overcome the problems posed by conventional MLIs. For inverter operation, multilevel SPWM technique is developed so that it can be applied to N-level inverters where the number of switches are less than $2(N-1)$. Also, to simplify the hardware implemetation of the modulation technique, a single carrier level shifted SPWM method is also developed in this thesis. For closed-loop operation, the SFB control is modified to work with constant switching frequency for tracking of reference quantities. Also, the DC bus voltage controller is simplified such that gains can be calculated using system parameters.

1.4 Objectives of the thesis

The literature survey is performed on three major building blocks of DSTATCOM- the voltage source inverter, current control technique and DC bus voltage control method. It is seen that the existing structures of multilevel inverters pose certain problems. Flying capacitor multilevel inverter and diode clamped multilevel inverters lack modularity as compared to cascaded H-bridge structure. FCMLI and DCMLI also require large number of clamping capacitors and diodes which pose problem in their design. These inverters have not been reported for levels greater than 5. Reverse recovery time for diodes used in DCMLI is an issue in their operation. Also DCMLI require auxiliary chopper circuits for voltage balancing. In FCMLI, though their are no diodes, requirement of large number of capacitors increase its cost and size. FCMLI is not suitable for compensation of a purely reactive or capacitive load. Modular multilevel converters are being explored for their highly modular structure that can be scaled to obtain outputs with level greater than 5. The circulating currents between adjacent phases of modular multilevel converters can be used for balancing the capacitor voltages of different modules in the inverter. The various modern topologies of MLI structures are also investigated. In many topologies, through there is a significant reduction in the component count as compared to the conventional topologies, these use multiple DC-link capacitors [21], [22], [36], [42]–[44], [46] or isolated DC sources [41], [26], [45], [35] for generation of stepped waveform. In all these topologies, the problem of capacitor volt-

age balancing persists. To solve this, redundant switching combinations or additional circuits are utilized. In many topologies, apart from the DC-link capacitors, multiple capacitors are used for generation of stepped waveform [37], [38] where pre-charging of capacitors are required. Thus, based on the literature review performed on DSTATCOM topology and control, presented in Section 1.2, the research gaps were identified. The literature review and research gaps guided the formulation of the objectives of the thesis, which are listed as follows:

1. To develop the topology of 7-level reduced switch single DC source based cascaded H-bridge multilevel inverter which overcomes the drawback of conventional MLIs and leads to simplification of DSTATCOM operation. This topology is named as RSDCHBMLI.

2. To develop a single carrier based multilevel modulation technique that can be implemented for topologies with reduced number of switches and should be realizable in DSP platform.

3. To design state-feedback control technique for constant switching frequency operation of RSDCHBMLI, and verify its operation in stand-alone mode with simulations and experiments.

4. To develop the grid connected operation of RSDCHBMLI for desired power injection into the grid, using SFB current control. The grid connected operation is verified using simulation and experiments.

5. To implement RSDCHBMLI based DSTATCOM connected to a weak distribution system and study its operation.

6. To implement the current control of DSTATCOM using FCS-MPC control and SFB control, and to compare their performance for load compensation.

7. To design a current based DC-bus voltage controller that permits simple calculation of controller gains and to compare the performance of the designed controller with existing DC bus voltage controllers.

8. To verify the DSTATCOM operation for different load conditions under unbalanced distribution system source voltage.

1.5 Organization of the thesis

This thesis is organized into five chapters. The first chapter, Chapter 1, provides an introduction to the thesis and is organized into five sections. It discusses the importance of power quality and application of multilevel inverters for load compensation. A review of various MLI topologies available in the literature, along with control techniques are presented. Depending on the literature review, the motivation for the thesis is discussed and objectives of the thesis are formulated. The first chapter also presents the structure and organization of the thesis.

In Chapter 2, the 7-level RSDCHBMLI topology is presented along with its open-loop operation. This chapter addresses the first and second objectives. It is divided into six sections. The topology of the RSDCHBMLI is compared with other existing MLI topologies in this chapter. The development of the single carrier level shifted PWM modulation strategy is presented in this chapter. The losses taking place in the RSDCHBMLI is also calculated. The findings are supported with PSCAD simulation and experimental results.

The third chapter, Chapter 3 describes the closed-loop operation of the RSDCHBMLI and is organized into two major sections; Section 3.1 details the voltage controlled operation of the inverter while Section 3.2 describes the grid connected current controlled operation of the inverter. In both the sections, the control law is described, along with simulation and experimental results. In this chapter, the third and fourth objectives are addressed.

In the fourth chapter, the RSDCHBMLI is used to design a DSTATCOM for weak distribution system. Two current control techniques are implemented for load compensation- state-feedback control and finite control set-model predictive control (FCS-MPC). The DSTATCOM operation is verified for both balanced ans unbalanced source voltages. A current based DC bus voltage controller is developed for easier calculation of controller gains and its performance is compared with conventional controllers. PSCAD simulation results are presented to support the operation of RSDCHBMLI based DSTATCOM. This chapter address the final four objectives of the thesis.

The conclusions obtained from the work presented in the previous chapters are

summarized in Chapter 5, Conclusion and Future work. This chapter also provides a brief description of possible research path for future extension of the work presented here.

CHAPTER 2

RSDCHBMLI: REDUCED SWITCH SINGLE DC SOURCE BASED CASCADED H-BRIDGE MULTILEVEL INVERTER

From the literature review presented in Chapter 1, it is observed that multilevel inverters demonstrate various advantages over their two-level counterparts. These advantages include reduction in $\frac{dv}{dt}$ stress, reduction in harmonic content of the output waveform, generation of smaller common mode voltage, etc. [17]. The widely used conventional topologies of multilevel inverters are flying capacitor multilevel inverter (FCMLI), diode clamped multilevel inverter (DCMLI) and cascaded H-bridge multilevel inverter (CHBMLI). The literature available on application of these inverters also highlight some major disadvantages of these topologies, *viz.*, high component requirement, usage of multiple DC-link capacitors and capacitor voltage balancing problems. To overcome these problems, various new topologies of MLIs are also presented in the literature which were discussed in the previous chapter. From the review of conventional and recent MLI topologies, the major issues in MLI design and implementation are listed as:

1. Large component count: DCMLI, FCMLI and CHBMLI require $2(N-1)$ switches to generate an N-level output. Additionally, in case of FCMLI and DCMLI, large number of capacitors and diodes are required to synthesize multilevel waveform [60], [61]. In most of the recent MLI topologies, attempt is made to reduce the component count [46], [36].

2. Multiple DC sources and capacitors: While CHBMLI requires identical, isolated DC sources for each full-bridge cell (FBC) [62], in FCMLI and DCMLI, the single DC source is split into multiple levels using multiple DC-link capacitors. In some of the newer topologies, switched capacitors [36] are used, while some use floating capacitors for generation of multilevel waveform. The usage of capacitors demand pre-charging and often requires additional charging mechanism [38].

3. Problem of Capacitor Voltage Balancing (CVB): The presence of unbalance among capacitor voltages leads to unequal stresses in switches and asymmetrical output voltage waveform. This problem is observed both in conventional and modified MLI topologies. CVB issues are solved either by exploiting the available redundancies in the switching combinations [60] or by incorporation of additional circuitry in the system [61].

In this chapter, with reference to the objectives of the thesis formulated in Chapter 1, a reduced switch topology of cascaded H-bridge multilevel inverter is developed that utilizes single DC source and attempts to solve the common issues plaguing MLI topologies. As the reduced switch single DC-source based cascaded H-bridge multilevel inverter (RSDCHBMLI) requires fewer switches compared to conventional MLI topologies, this chapter details a single carrier based level shifted PWM strategy that can be applied to such reduced switch topologies and is easily implementable in DSP platforms. The loss analysis of RSDCHBMLI is also presented in this chapter, along with power sharing among the cells. The operation of the RSDCHBMLI and the developed modulation technique is verified at different modulation indices using both simulation and experiments.

This chapter is organized into seven sections. The topology of RSDCHBMLI is presented and described in Section 2.1. In Section 2.2, the RSDCHBMLI is compared with existing state-of-the art MLI topologies. The multilevel modulation strategies for RSDCHBMLI are presented in Section 2.3, followed by loss analysis of the inverter in Section 2.4 and power sharing among the full-bridge cells in Section 2.5. The open-loop operation of the RSDCHBMLI is validated with simulation and experimental results which are described in Section 2.6. The conclusions obtained from the simulation and experiment are presented in Section 2.7.

2.1 Topology

The topology of single-phase 7-level RSDCHBMLI is shown in Fig. 2.1. It consists of two full-bridge cells (FBCs), Cell 1 and Cell 2. Each cell has four power electronic switches. These switches are realized using IGBT with an anti-parallel diode. The switches in Cell 1 are S_{11}, S_{12}, S_{13} and S_{14} which form complimentary switching

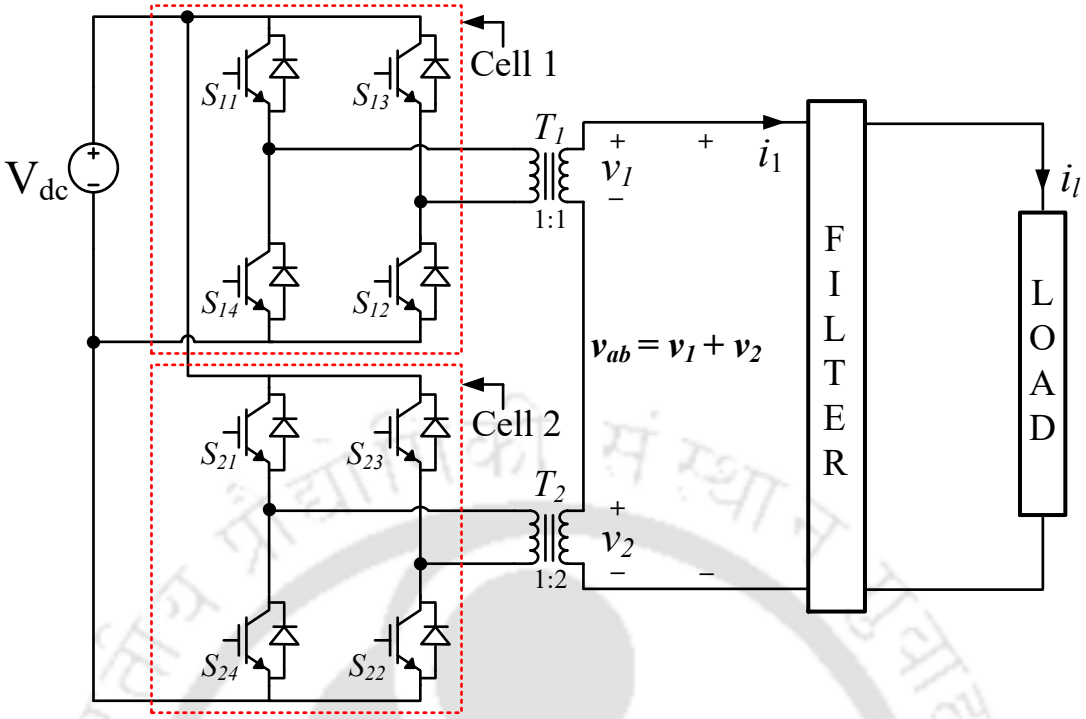


Fig. 2.1 Topology of single-phase 7-level RSDCHBMLI

pairs as (S_{11}, S_{14}), (S_{13}, S_{12}). The four switches used in Cell 2 also form similar complimentary pair as (S_{21}, S_{24}), (S_{23}, S_{22}). Both the cells are connected across a single

Table 2.1 SWITCHING STATES AND OUTPUT VOLTAGE OF 7-LEVEL RSDCHBMLI

S_{11}	S_{13}	S_{21}	S_{23}	v_1	v_2	$v_{ab}=v_1+v_2$
1	0	1	0	V_{dc}	$2V_{dc}$	$3V_{dc}$
0	1	0	0	0	$2V_{dc}$	$2V_{dc}$
1	1	1	0	0	$2V_{dc}$	$2V_{dc}$
1	0	0	0	V_{dc}	0	V_{dc}
1	0	1	1	V_{dc}	0	V_{dc}
0	1	1	0	$-V_{dc}$	$2V_{dc}$	V_{dc}
0	0	0	0	0	0	0
1	1	1	1	0	0	0
0	1	0	0	$-V_{dc}$	0	$-V_{dc}$
0	1	1	1	$-V_{dc}$	0	$-V_{dc}$
1	0	0	1	V_{dc}	$-2V_{dc}$	$-V_{dc}$
0	0	0	1	0	$-2V_{dc}$	$-2V_{dc}$
1	1	0	1	0	$-2V_{dc}$	$-2V_{dc}$
0	1	0	1	$-V_{dc}$	$-2V_{dc}$	$-3V_{dc}$

DC voltage source V_{dc}. Depending on the switching states, each FBC is capable of generating three output voltages, $+V_{dc}$, 0 and $-V_{dc}$. The outputs of Cell 1 and Cell 2 are connected to the primaries of transformers T_1 and T_2 respectively, as shown in Fig. 2.1. The multilevel output voltage v_{ab} is obtained by cascading the output voltages obtained

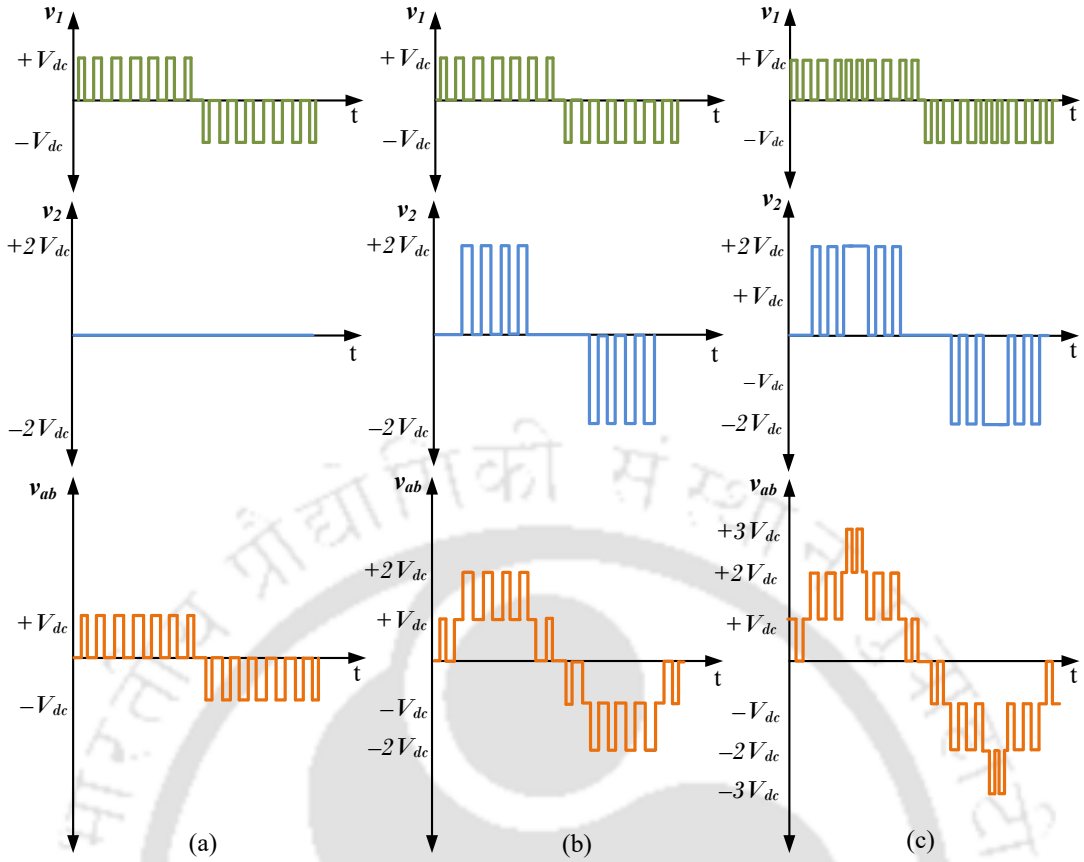


Fig. 2.2 RSDCHBMLI operation for: (a) 3-level output voltage (b) 5-level output voltage (c) 7-level output voltage

at transformer secondaries. The number of levels in the output voltage is dependent upon the turns-ratio of T_1 and T_2. For 7-level output, the turns-ratio for T_1 is chosen as 1 : 1 and that for T_2 is chosen as 1 : 2. Such a combination of turns-ratio leads to reduction in the number of components required to generate a 7-level waveform. The possible output voltages at the secondary of T_1 are $+V_{dc}$, 0 and $-V_{dc}$ while those at the secondary of T_2 are $+2V_{dc}$, 0 and $-2V_{dc}$. Various combinations of outputs of Cell 1 and Cell 2 enable the generation of 7-level output voltage waveform. The switching combinations and corresponding output voltages for the 7-level RSDCHBMLI are shown in Table 2.1. For example, if switches (S_{11}, S_{12}) are on for Cell 1, and (S_{21}, S_{22}) are on for Cell 2, then output at T_1 secondary is $+V_{dc}$ and that at T_2 secondary is $+2V_{dc}$. Thus the output voltage v_{ab} is obtained as $+3V_{dc}$. For $v_{ab} = 2V_{dc}$, (S_{21}, S_{22}) are turned on for Cell 2 such that $v_2 = 2V_{dc}$ while for Cell 1, either (S_{11}, S_{13}) are turned on or (S_{12}, S_{12}) are turned on so that v_1 is obtained as 0. The generation of 0-level output voltage for each FBC can be done by turning on either the upper pair of switches or the lower pair of switches. This adds flexibility and redundancy in the RSDCHBMLI. The table also indicates the availability of redundant switching combinations for output voltage levels

$\pm V_{dc}$, $\pm 2V_{dc}$ and 0. Utilizing the switching table, the theoretical output voltages obtained using PWM operation of RSDCHBMLI is shown in Fig. 2.2 for three different cases of output voltage,3-level, 5-level and 7-level. In RSDCHBMLI operation, Cell 1 continuously switches its output between $+V_{dc}$, 0 and $-V_{dc}$ for all levels of output voltage. Cell 2 modulates only when the output voltage switches between $+2V_{dc}$ to V_{dc} and $-2V_{dc}$ to $-V_{dc}$. For output voltage switching between $\pm V_{dc}$ and 0, Cell 2 output is 0 while for output voltage switching between $\pm 3_{dc}$ and $\pm 2V_{dc}$, Cell 2 output is $\pm 2V_{dc}$.

Considering pulse-width-modulated operation of the inverter, the output voltage of the inverter is dependent on the sinusoidal modulation signal $v_m = M \sin \omega t$, where $0 \leq M \leq 1$ is termed as the modulation index. The number of steps in output voltage is dependent on M. For the RSDCHBMLI topology that is described in this thesis, the maximum possible number of steps in the output voltage is 7. A typical 7-level output voltage is shown in Fig 2.2(c). The enhancement in number of levels also leads to reduction in harmonics content of the output voltage as compared to two-level and 5-level inverters. To obtain a sinusoidal output voltage from the RSDCHBMLI, a low pass filter must be connected to the inverter. Multilevel inverter topologies enable the usage of smaller filters for obtaining a sinusoidal output. The filter cut-off frequency can be further increased, thereby reducing the filter size, by choosing carrier frequency of the PWM operation in the range of kilohertz.

The RSDCHBMLI operation exhibits a maximum boosting ability of $3V_{dc}$. For all scenarios of inverter operation, the voltage stress across each switch is limited to V_{dc}, The current stress of the switches are dependent on the value of load current and inverter output current. For the switches of Cell 1, the current stress of the switches are limited to the peak value of inverter output current i_1. For Cell 2, the use of a transformer with turns ratio 1 : 2 increases the maximum value of current stress to twice the peak value of i_1.

The main advantages of this topology are:

1. **Usage of single DC source:** Unlike the conventional symmetrical and asymmetrical CHBMLI topology [17], here all the full-bridge cells are connected in parallel to the same DC source. This reduces the requirement of DC sources for the inverter design. Also, in case of applications where the DC-source is replaced with a DC-link capacitor, the usage of single capacitor eliminates the problem

of capacitor voltage balancing. As a result, the RSDCHBMLI topology doesn't require additional controls or circuits for CVB. This results in simplification of the inverter design and control.

2. **Reduction in component count:** In this RSDCHBMLI topology, the turns ratio of the full-bridge transformers are chosen such that the inverter is capable of generating a 7-level output voltage by utilizing two full-bridge cells. This results in reducing the component count of the inverter.

3. **Boosting ability and isolation:** The choice of transformer turns ratio as 1 : 1 and 1 : 2 not only reduces the component count, but also results in boosting of the inverter output voltage, without increasing voltage stress of the components. The presence of transformers also provides an inherent isolation the inverter topology along with eliminating the possibility of circulating currents.

The RSDCHBMLI also have some limitations which can be listed as:

1. **Doubling of current stress for switches in Cell 2:** Though these topology exhibit boosting ability which reduces the voltage stress of the switches in Cell 1 and Cell 2, the use of transformers lead to doubling of current stress of the switches in Cell 2. Thus the switches have unequal current stresses.

2. **Unequal switching loss:** From the typical voltage waveforms shown in Fig. 2.2, it is observed that Cell 1 and Cell 2 have unequal switchings in RSDCHBMLI operation. Switches (S_{11}, S_{13}) operate continuously for all levels of output voltage but S_{21} and S_{23} switch only during generation of $\pm 2V_{dc}$ output voltage. For the rest of the duration, the switches are held at either on or off position. This leads to unequal switching losses in among the switches.

2.2 Comparison with state-of-art MLI topologies

In this section, the 7-level RSDCHBMLI is compared with other state-of-the-art 7-level inverter topologies. The comparison is performed in terms of number of components (switches, diodes, capacitors, transformers), number of DC sources, maximum voltage stress, maximum current stress and total blocking voltage, and is presented in

Table 2.2 COMPARISON OF COMPONENT COUNT FOR A 7-LEVEL RSDCHBMLI WITH OTHER TOPOLOGIES IN TERMS OF COMPONENT COUNT, MAXIMUM VOLTAGE STRESS (MVS) (P.U), MAXIMUM CURRENT STRESS (MCS) (P.U) AND TOTAL BLOCKING VOLTAGE (TBV) (P.U)

	Diodes	**Capaci-tors**	**Switches**	**Transf -ormers**	**DC Source**	**MVS (p.u)**	**MCS (p.u)**	**TBV (p.u)**
DCMLI	30	6	12	–	1	0.5	$\sqrt{2}$	6.0
FCMLI	0	18	12	–	1	0.5	$\sqrt{2}$	6.0
CHBMLI	0	3	12	–	3	0.33	$\sqrt{2}$	4.0
[29]	–	–	12	3	1	0.33	$\sqrt{2}$	4.0
[36]	2	3	7	–	1	1.0	$\sqrt{2}$	5.0
[63]	2	–	8	–	2	2.0	$\sqrt{2}$	5.0
[37]	0	2	9	–	1	1.0	$\sqrt{2}$	4.67
[38]	4	3	13	–	1	1.0	$\sqrt{2}$	6.67
RSDCHBMLI	–	–	8	2	1	0.33	$2\sqrt{2}$	2.67

Table 2.2. It is observed from the table that RSDCHBMLI uses 8 switches for generation for 7-level waveform while DCMLI, FCMLI and CHBMLI topologies require 12 switches for the same. Also, DCMLI and FCMLI do not have any boosting function and the maximum of possible output obtained from these inverters is always less than input DC voltage. RSDCHBMLI also does not require any diodes or capacitors for synthesis of multilevel output voltage, which is an advantage over the requirement of large number of diodes or capacitors in cases of DCMLI and FCMLI topology. It can be seen that RSDCHBMLI utilizes the minimum number of components for generation of 7-level waveform. The maximum voltage stress (MVS), maximum current stress (MC) and total blocking voltage (TBV) of various MLI topologies, calculated in Table 2.2, are in per unit with base VA= $3V_{dc}I_L$ and base voltage= $3V_{dc}$, I_L being the load current. The boosting ability of the RSDCHBMLI leads to a reduction in MVS in the power electronic switches while the reduction in number of switches cause TBV in RSDCHBMLI to be lower than that for other topologies. One of the drawbacks of the RSDCHBMLI is the doubling of current stress for the switches of Cell 2, which is caused by the connection of the step-up transformer.

2.3 Multilevel modulation strategies

The 7-level RSDCHBMLI is to be modulated using sinusoidal pulse width modulation. For conventional multi-carrier sine PWM operation of an N-level inverter, $(N-1)$ number of triangular carriers are assigned to $(N-1)$ number of upper switches.

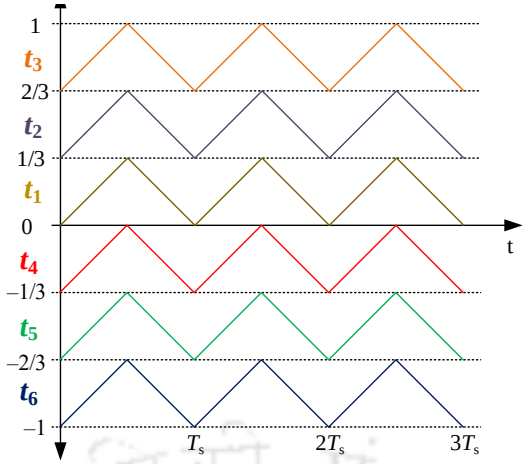


Fig. 2.3 6 Phase disposed level shifted carrier waves for $N = 7$

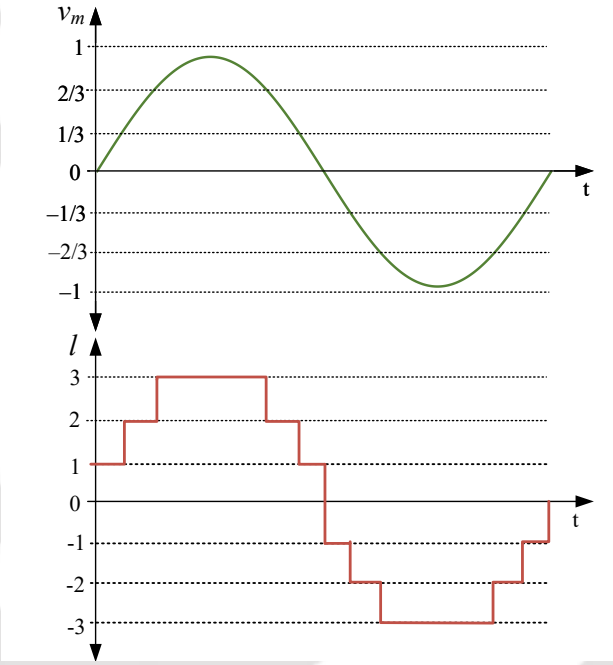


Fig. 2.4 Determination of level of operation l from v_m

For phase disposed PWM (PDPWM) technique, these triangular carriers are arranged to occupy contiguous bands between $+1$ and -1. The comparison between the carriers and the modulating signal generate the switching signals for the upper switches [59], and the lower switches operate with a complimentary switching function. In this topology, as the number of switches are reduced, PDPWM cannot be applied. Hence, a modified level shifted PDPWM (LS-PDPWM) technique is detailed in the next subsection.

2.3.1 Modified level shifted PD-PWM

In phase disposed PWM operation, the number of triangular carriers are chosen as $(N-1)$ for an N-level inverter. The peak to peak values of carrier waves are given by $\frac{2}{(N-1)}$, and these waves are stacked in a level shifted manner from -1 to $+1$. Thus, for a 7-level inverter, six carrier waves are required, which are shown in Fig. 2.3. The carriers t_1, t_2 and t_3 are arranged from 0 to $\frac{1}{3}$, $\frac{1}{3}$ to $\frac{2}{3}$ and from $\frac{2}{3}$ to 1 respectively. The carriers t_4, t_5 and t_6 are arranged from 0 to $-\frac{1}{3}$, $-\frac{1}{3}$ to $-\frac{2}{3}$ and from $-\frac{2}{3}$ to -1 respectively. In conventional PD-PWM operation, these six carrier waves are assigned to the six independent switches of conventional 7-level inverters. The comparison between the carriers and the sinusoidal modulation signal $v_m = M \sin \omega t$ yields switching signals for the conventional MLIs.

Table 2.3 CARRIER ASSIGNMENT TO SWITCHES FOR MODIFIED LEVEL SHIFTED PD-PWM OPERATION

	level *l*	S_{11}	S_{13}	S_{21}	S_{23}
$\frac{2}{3} \leq v_m \leq 1$	$l=3$	t_3	t_6	1	0
$\frac{1}{3} \leq v_m < \frac{2}{3}$	$l=2$	t_2	t_5	t_2	t_5
$0 \leq v_m < \frac{1}{3}$	$l=1$	t_1	t_4	1	1
$-\frac{1}{3} \leq v_m < 0$	$l=-1$	t_1	t_4	1	1
$-\frac{2}{3} \leq v_m < -\frac{1}{3}$	$l=-2$	t_2	t_5	t_2	t_5
$-1 \leq v_m \leq -\frac{2}{3}$	$l=-3$	t_3	t_6	0	1

In case of reduced switch MLIs, the number of independent switches are less than $(N-1)$, and so in such cases, it is not possible to directly assign the carriers to the switches. To overcome this problem, a modified level-shifted PD PWM strategy is utilized here. In this method, v_m is compared with k to determine the instantaneous level of operation l as shown in Fig 2.4. For an N-level inverter, k ranges from -1 to $+1$ in steps of $\frac{1}{N'}$ where $N' = \frac{(N-1)}{2}$. Thus for 7- level RSDCHBMLI, $k = -1, -\frac{2}{3}, -\frac{1}{3}, 0, \frac{1}{3}, \frac{2}{3}, +1$. Depending on l, the carriers shown in Fig. 2.3 are assigned to the four upper switches S_{11}, S_{13}, S_{21}, S_{23} as shown in Table 2.3. The carrier waves and the constants assigned to the switches are compared with v_m to obtain the switching signals for S_{11}, S_{13}, S_{21}, S_{23}. For $l > 0$, if v_m is greater than assigned carrier or constant, the switch is turned on, else the switch remains in the off state. For example, if $l = 1$, S_{11} is turned on when $v_m > t_1$ and S_{21} remains in the off state as v_m is always less than or equal to 1. For $l < 0$, if v_m is smaller than assigned carrier or constant, the switch is turned on, else the switch

remains in the off state. For $l = \pm 2$, the switches S_{11}, S_{21} and S_{13}, S_{23} are assigned the same carrier, but they are operated in complementary manner such that if $v_m > t_2$ turns on S_{11} then S_{21} is turned off and vice-versa.

2.3.2 Single carrier level shifted Sine PWM

In multi-carrier SPWM modulation, number of carriers increase with increase in output voltage levels. This makes the implementation of modulation technique difficult in DSP platforms. To overcome this problem, some modifications of the multi-carrier technique are proposed in the literature [64], [65]. In [64], the inverter modulation is achieved using a global decoding function. The reference signal here is modified such that it always lies between 0 and 1. The comparison of the modified reference with the carrier signal generates the switching signal which is used as a reference in the global decoding function to generate the switching signals for the switches of the full-bridge cells. In [65], two carrier signals are utilized to generate the switching signals for the switches. In the modulation technique described in this thesis, only one carrier signal is used for SPWM modulation of the inverter. In this method, only one triangular carrier signal is used while multiple reference signals are generated from the given modulation signal v_m depending on l. These new references, indicated as v_{ml} and v'_{ml}, are calculated as follows:

$$\begin{aligned} v'_{ml} &= |N'|(v_m + \frac{|l|}{3}), \text{ if } -N' \leq l < 0 \\ v_{ml} &= |N'|(v_m + \frac{l-1}{3}), \text{ if } 0 \leq l \leq N' \end{aligned} \tag{2.1}$$

The graphical representation is shown in Fig. 2.5 for a 7-level inverter. The references

Table 2.4 REFERENCE GENERATION FOR SC-LS-PWM IMPLEMENTATION

	level l	**modified reference**	S_{11}	S_{13}	S_{21}	S_{23}
$-1 \leq v_m \leq -\frac{2}{3}$	$l = -3$	$v'_{m3} = 3(v_m + 1)$	v'_{m3}	0	1	0
$-\frac{2}{3} \leq v_m < -\frac{1}{3}$	$l = -2$	$v'_{m2} = 3(v_m + \frac{2}{3})$	v'_{m2}	0	v'_{m2}	0
$-\frac{1}{3} \leq v_m < 0$	$l = -1$	$v'_{m1} = 3(v_m + \frac{1}{3})$	v'_{m1}	0	0	0
$0 \leq v_m < \frac{1}{3}$	$l = 1$	$v_{m1} = 3v_m$	0	v_{m1}	0	0
$\frac{1}{3} \leq v_m < \frac{2}{3}$	$l = 2$	$v_{m2} = 3(v_m - \frac{1}{3})$	0	v_{m2}	0	v_{m2}
$\frac{2}{3} \leq v_m \leq 1$	$l = 3$	$v_{m3} = 3(v_m - \frac{2}{3})$	0	v_{m3}	0	1

are calculated such that comparison of v_{ml} and v'_{ml} with v_{tri}, shown in Fig. 2.5, yields the same result as comparing v_m with the phase disposed carriers, shown in Fig. 2.3, in

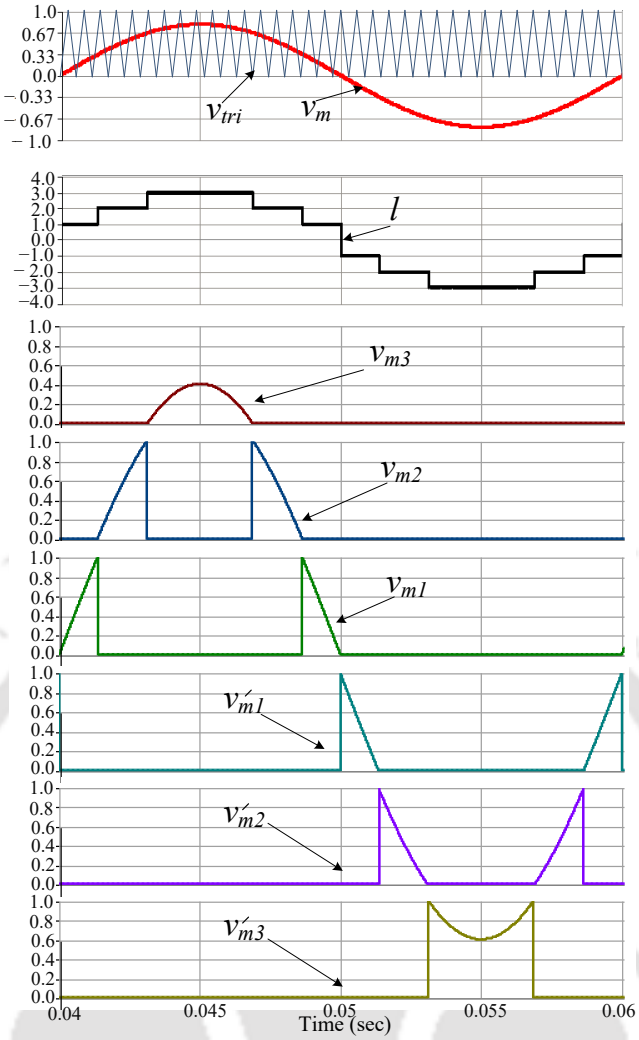


Fig. 2.5 Determination of l and generation of modified reference signals from v_m for 7-level inverter operation

modified LS-PDPWM technique. For a 7-level inverter, the modified references corresponding to different values of l is given in Table 2.4. These references are assigned to the upper switches as indicated in Table 2.4. Once the reference is assigned, comparison between the reference and v_{tri} give the switching signals for the upper switches, S_{11}, S_{13}, S_{21}, S_{23}. The switching signals for the lower switches are generated as $S_{14} = \overline{S_{11}}$, $S_{12} = \overline{S_{13}}$, $S_{24} = \overline{S_{21}}$, $S_{22} = \overline{S_{23}}$.

In this thesis, single-carrier level-shifted sinusoidal PWM technique is used for RSDCHBMLI operation due to it advantages over conventional multi-carrier modulation techniques.

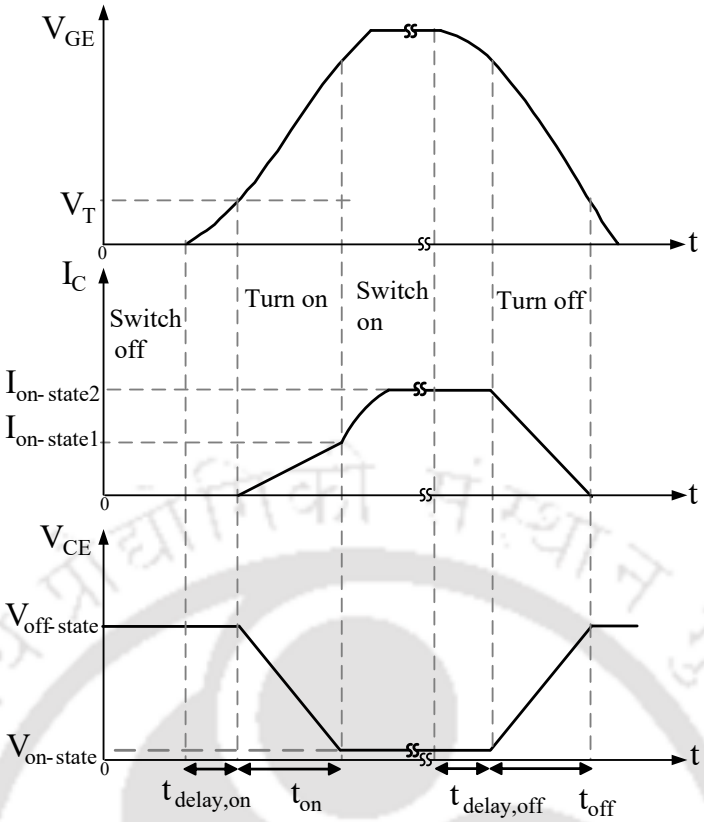


Fig. 2.6 Turning on and off a power electronic switch

2.4 Loss Analysis of RSDCHBMLI

Most of the power loss occurring in the RSDCHBMLI operation are of two types- switching loss and the conduction loss [37], [66]. Switching loss takes place due to non-idealities of power electronic switches where the switches take a finite time to shift from their 'ON' state to 'OFF' state and vice-versa. Switching loss takes place for the duration of turn on and turn off of the switches [37]. The conduction loss in a power electronic converter takes place due to non-ideal switch characteristics where the switch offers a small value of finite resistance in its on-state. In next parts, switching loss and conduction loss of the 7-level RSDCHBMLI is calculated in terms of the switching frequency, load current and DC voltage.

2.4.1 Switching loss of RSDCHBMLI

The transient process of turning on/off of power electronic switches is shown in Fig 2.6. After the switching signal for turning on of a switch is recieved, $t_{delay,on}$ time elapses during which the gate-emitter voltage (V_{GE}) rises to the threshold voltage (V_T). When V_{GE} reaches V_T, the collector current (I_C) starts increasing and collector emitter

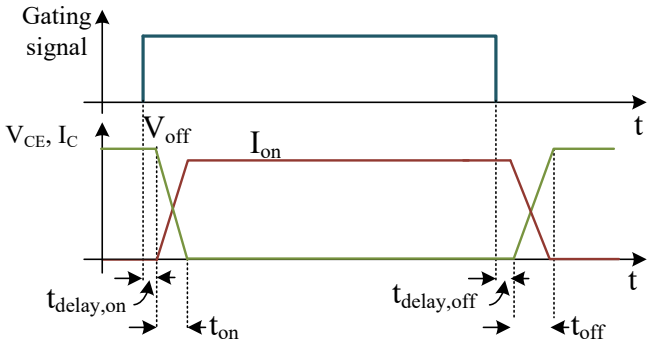


Fig. 2.7 Linearized switching characteristics of a power electronic switch

voltage (V_{CE}) starts decreasing. This duration indicates the turn-on process of the switch and it is can be noted from Fig 2.6 that during t_{on}, voltage and current simultaneously exhibit non-zero value which leads to switching loss in the switches. Similarly, during switching off process of the switch, I_C starts decreasing after elapsing of $t_{delay,off}$ and V_{CE} also starts increasing. The non-zero value of voltage and current is encountered during t_{off} time duration shown in Fig 2.6. Thus, t_{on} and t_{off} duration correspond to switching loss of the switches. For calculation of switching loss in this thesis, simplified linearized characteristics of the switches are considered as shown in Fig 2.7. During $t_{delay,on}$, V_{CE} is at the off-state voltage and and I_{CE} is zero as the turn-on process of the switch is not yet started. After $t_{delay,on}$, the turn-on process of the switch starts and V_{CE} starts decreasing from the off-state voltage while I_{CE} simulatenously starts increasing from zero. The turn-on switching loss takes place during the period t_{on} as shown in Fig. 2.7. From Fig 2.7, the turn-on power loss P_{ON}, for switching frequency f_{sw}, over one switching cycle can be calculated as

$$\begin{aligned} P_{ON} &= f_{sw}\int_0^{t_{on}} V_{off}(1-\frac{t}{t_{on}})\frac{I_{on}}{t_{on}}t\,dt \\ &= f_{sw}\frac{1}{6}V_{off}I_{on}t_{on} \end{aligned} \tag{2.2}$$

For each switching cycle, V_{off} is the collector-emitter voltage across the switch at the instant when the turn-on process starts and I_{on} is the current through the switch after it turns on completely. Thus the value of V_{off} and I_{on} needs to be measured at every switching instant. Similarly, power loss during turn-off is given as

$$P_{OFF} = f_{sw}\frac{1}{6}V_{off}I_{on}t_{off} \tag{2.3}$$

Thus, total power loss, P_{sw} due to turn-on and turn-off of the switches is given by equation (2.4) where N_{sw} is the total number of switches, N_{on} is the number of times k^{th} switch is turned on and N_{off} is the number of times k^{th} switch is turned off.

$$P_{sw} = \sum_{N_{sw}} (\sum_{N_{on}} (P_{ONk}) + \sum_{N_{off}} (P_{OFFk})) \tag{2.4}$$

2.4.2 Conduction loss of RSDCHBMLI

The conduction loss in RSDCHBMLI depends on the resistance of the current path at each instant of operation of the RSDCHBMLI. Thus, for different combinations of output voltage and current direction, the possible paths for inverter current is analyzed in this section. For this, depending on the polarity of the output voltage, v_{ab} and

Table 2.5 CONDUCTING PATH IN RSDCHBMLI FOR DIFFERENT POLARITIES OF OUTPUT VOLTAGE AND OUTPUT CURRENT

Mode	level l	Cell 1 output	path	Cell 2 output	path
I: $v_{ab} > 0, i_1 < 0$	1	V_{dc}	D_{11}, D_{12}	0	D_{21}, S_{23}
		0	D_{11},S_{13}	0	D_{21}, S_{23}
	2	0	D_{11}, S_{13}	$2V_{dc}$	D_{21}, D_{22}
		V_{dc}	D_{11},D_{12}	0	D_{21},S_{23}
	3	V_{dc}	D_{11},D_{12}	$2V_{dc}$	D_{21},D_{22}
		0	D_{11},S_{13}	$2V_{dc}$	D_{21},D_{22}
II:$v_{ab} > 0, i_1 > 0$	1	V_{dc}	S_{11},S_{12}	0	S_{21},D_{23}
		0	S_{11},D_{13}	0	S_{21},D_{23}
	2	0	S_{11},D_{23}	$2V_{dc}$	S_{21},S_{22}
		V_{dc}	S_{11},S_{12}	0	S_{21},D_{23}
	3	V_{dc}	S_{11},S_{12}	$2V_{dc}$	S_{21},S_{22}
		0	S_{11},D_{13}	$2V_{dc}$	S_{21},S_{22}
III:$v_{ab} < 0, i_1 > 0$	-1	$-V_{dc}$	D_{13},D_{14}	0	S_{21},D_{23}
		0	S_{11},D_{13}	0	S_{21},D_{23}
	-2	0	S_{11},D_{13}	$-2V_{dc}$	D_{23},D_{24}
		$-V_{dc}$	D_{13},D_{14}	0	S_{21},D_{23}
	-3	-1	D_{13},D_{14}	$-2V_{dc}$	D_{23},D_{24}
		0	S_{11},D_{13}	$-2V_{dc}$	D_{23},D_{24}
IV:$v_{ab} < 0, i_1 < 0$	-1	$-V_{dc}$	S_{13},S_{14}	0	D_{21},S_{23}
		0	S_{13},D_{11}	0	D_{21},S_{23}
	-2	0	S_{13},D_{11}	$-2V_{dc}$	S_{23},S_{24}
		$-V_{dc}$	S_{13},S_{14}	0	D_{21},S_{23}
	-3	$-V_{dc}$	S_{13},S_{14}	$-2V_{dc}$	S_{23},S_{24}
		0	S_{13},D_{11}	$-2V_{dc}$	S_{23},S_{24}

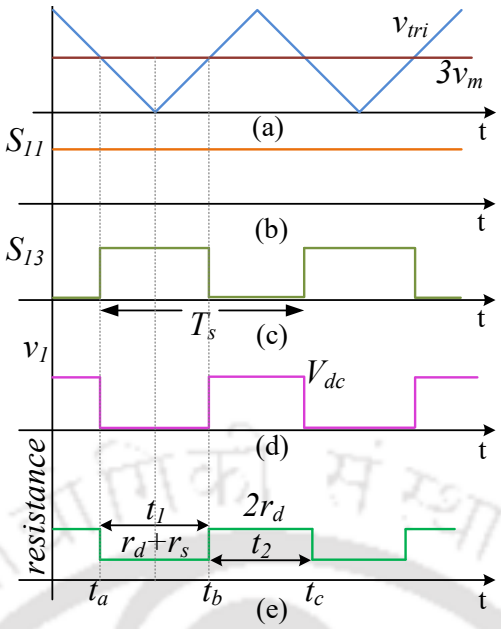


Fig. 2.8 Operation of Cell 1 of RSDCHBMLI for Mode I, $l = 1$: (a) triangular carrier v_{tri} and modulation signal v_m (b) Switching signal for S_{11} (c) Switching signal for S_{13} (d) Output voltage v_1 of Cell 1 (e) Resistance of the current path

direction of inverter output current i_1, the inverter operation is divided into four modes as shown in Table 2.5. Depending on these modes, the current paths for each possible output voltage for both Cell 1 and Cell 2 are obtained, which are listed in Table 2.5.

Now if the diode resistance is considered as r_d and power electronic swtich resistance as r_s, depending on the output of the cells, mode and level, the resistance of the current path can be computed. For Mode I, $l = 1$, the gating signals S_{11} and S_{13} for Cell 1 is shown in Fig. 2.8(b) and Fig. 2.8(c). The resistance of the current path is also shown in Fig. 2.8(e). From Fig. 2.8(e), it is seen that the resistance of the current path depends on the switching signal. Thus, for the switching interval shown in Fig. 2.8, conduction loss is computed as

$$\begin{aligned} P_{cond} &= \frac{1}{T_s}\int_{t_a}^{t_c} i^2 r(t)dt \\ &= \frac{1}{T_s}[\int_{t_a}^{t_b} i^2 r(t) + \int_{t_b}^{t_c} i^2 r(t)]dt \\ &= \frac{i^2}{T_s}[t_1(r_d+r_s)+t_2 2r_d]dt \end{aligned} \tag{2.5}$$

The time intervals t_1 and t_2 can be further calculated in terms of the carrier and the

modulation signal using Fig. 2.8 and Table. 2.4. The point t_a is calculated as

$$\begin{aligned} 3v_m &= v_{tri} \\ 3v_m &= \frac{1}{\frac{T_s}{2}} t_a \end{aligned} \tag{2.6}$$

$$t_a = \frac{3v_m T_s}{2} \tag{2.7}$$

Now from Fig. 2.8,

$$t_1 = 2t_a, \quad t_2 = T_s - t_1 \tag{2.8}$$

Thus, replacing (2.7) in (2.8), t_1 and t_2 is calculated to be

$$t_1 = 3v_m T_s, \quad t_2 = T_s(1 - 3v_m) \tag{2.9}$$

Replacing these values in (2.5), conduction loss for Cell 1 when the inverter is operating in Mode I, $l = 1$ is given by

$$P_{cond} = \frac{i^2}{T_s}[3v_m T_s(r_d + r_s) + T_s(1 - 3v_m)2r_d]dt \tag{2.10}$$

Similarly, the conduction loss can be found out for all the 12 cases shown in Table. 2.5, and the total conduction loss in one cycle of the modulation signal is calculated as

$$P_{cond_{total}} = f_{ref}[\sum_{j=Mode\ I}^{Mode\ II}\sum_{k=1}^{3} P_{cond_{ij}} + \sum_{j=Mode\ III}^{Mode\ IV}\sum_{k=-1}^{-3} P_{cond_{ij}}] \tag{2.11}$$

2.5 Power sharing among the full-bridge cells

The power sharing between the cascaded FBCs depends on output voltage of the individual FBC. As the power handled by each FBC impact the operating temperature of the semiconductor modules and thus affect the aging process, it is important to estimate the power sharing between Cell 1 and Cell 2 for different modulation indices [67], [65]. This can predict the life-cycle of the switches and also help in inclusion of redundant modules for applications demanding high reliability.

The fundamental component of the output voltages of the FBCs be given by

(2.12) where α and β indicate their phase differences with the capacitor voltage v_c

$$v_{1_f} = \sqrt{2}V_1 \sin(\omega t - \alpha);\ v_{2_f} = \sqrt{2}V_2 \sin(\omega t - \beta) \tag{2.12}$$

The fundamental component of the output current of the inverter can be written as

$$i_{1_f} = \sqrt{2}I_1 \sin(\omega t - \phi_1) \tag{2.13}$$

Considering no real power loss in the filters, ($R_f \approx 0.0$), the power balance equation becomes

$$V_1 I_1 \cos(\alpha - \phi_1) + V_2 I_1 \cos(\beta - \phi_1) = V_c I_L \cos(\phi_L) \tag{2.14}$$

where V_c, I_L and ϕ_L indicate the rms value of capacitor voltage, load current and the phase difference between V_c and I_L, respectively. Now as the modulation signal for both the FBCs are derived from the same v_m, $\alpha \approx \beta$. Thus, (4.10) can be written as

$$(V_1 + V_2) I_1 \cos(\alpha - \phi_1) = V_c I_L \cos\phi_L \tag{2.15}$$

Now, if P_L be the total load power, the real power sharing by the FBCs denoted P_1 and P_2 respectively, can be calculated as

$$P_1 = \frac{V_1 I_1 \cos(\alpha - \phi_1)}{V_c I_L \cos\phi_L} P_L \quad P_2 = \frac{V_2 I_1 \cos(\alpha - \phi_1)}{V_c I_L \cos\phi_L} P_L \tag{2.16}$$

Utilizing (2.15), (2.16) can be written as

$$P_1 = \frac{V_1}{V_1 + V_2} P_L \quad P_2 = \frac{V_2}{V_1 + V_2} P_L \tag{2.17}$$

If modulation indices for individual FBCs are defined as $M_1 = \frac{V_1}{V_{dc}}$ and $M_2 = \frac{V_2}{2V_{dc}}$, then (2.17) becomes

$$P_1 = \frac{M_1}{M_1 + 2M_2} P_L \quad P_2 = \frac{2M_2}{M_1 + 2M_2} P_L \tag{2.18}$$

Thus, for n cascaded FBCs, the real power shared by j-th FBC is given by

$$P_M = \frac{k_j M_j}{k_1 M_1 + k_2 M_2 + ... + k_n M_n} P_L \tag{2.19}$$

where $1 : k_j$ is the turns ratio of the transformer connected to the jth FBC and $M_j =$

$\frac{V_j}{k_j V_{dc}}$. The reactive power sharing among the FBCs can be calculated as

$$Q_1 = \frac{V_1}{V_{ab_f}} Q_L, \quad Q_2 = \frac{V_2}{V_{ab_f}} Q_L \tag{2.20}$$

where reactive power demand by the load is denoted as Q_L.

2.6 Results

The circuit diagram for simulation and experimental set-up is shown in Fig 2.9. The inductor and capacitor for output filter is chosen such that the cut-off frequency of the filter is 1 kHz.

2.6.1 Simulation results

The simulation of the RSDCHBMLI is performed with PSCAD/EMTDC software, with the parameters shown in Table 2.6 The on-state resistance of the IGBT, r_s, and the anti-parallel diode, r_d, is calculated from the datasheet of IRG7PH42UD-EP [68]. The values are obtained as $r_s = 0.057\ \Omega$ and $r_d = 0.073\ \Omega$. These values are also utilized to calculate the switching loss and conduction loss of RSDCHBMLI. The t_{on} and t_{off} value for the IGBT is also computed from the datasheet.

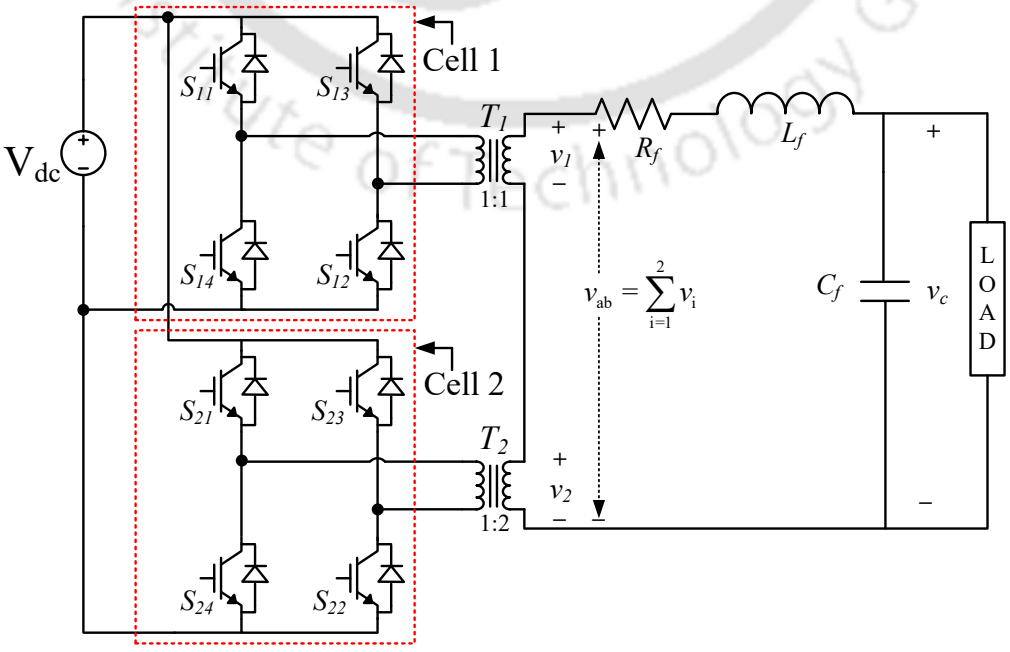


Fig. 2.9 Single-phase RSDCHBMLI circuit with LC filter supplying a standalone load

Table 2.6 PARAMETERS FOR SIMULATION OF OPEN-LOOP OPERATION OF 7-LEVEL RSDCHBMLI

Parameters	Values	Parameters	Values
V_{dc}	150 V	Resistance, R_f	0.02 Ω
Filter parameters, L_f, C_f	0.001 H, 22 μF	Switching frequency f_s	10 kHz

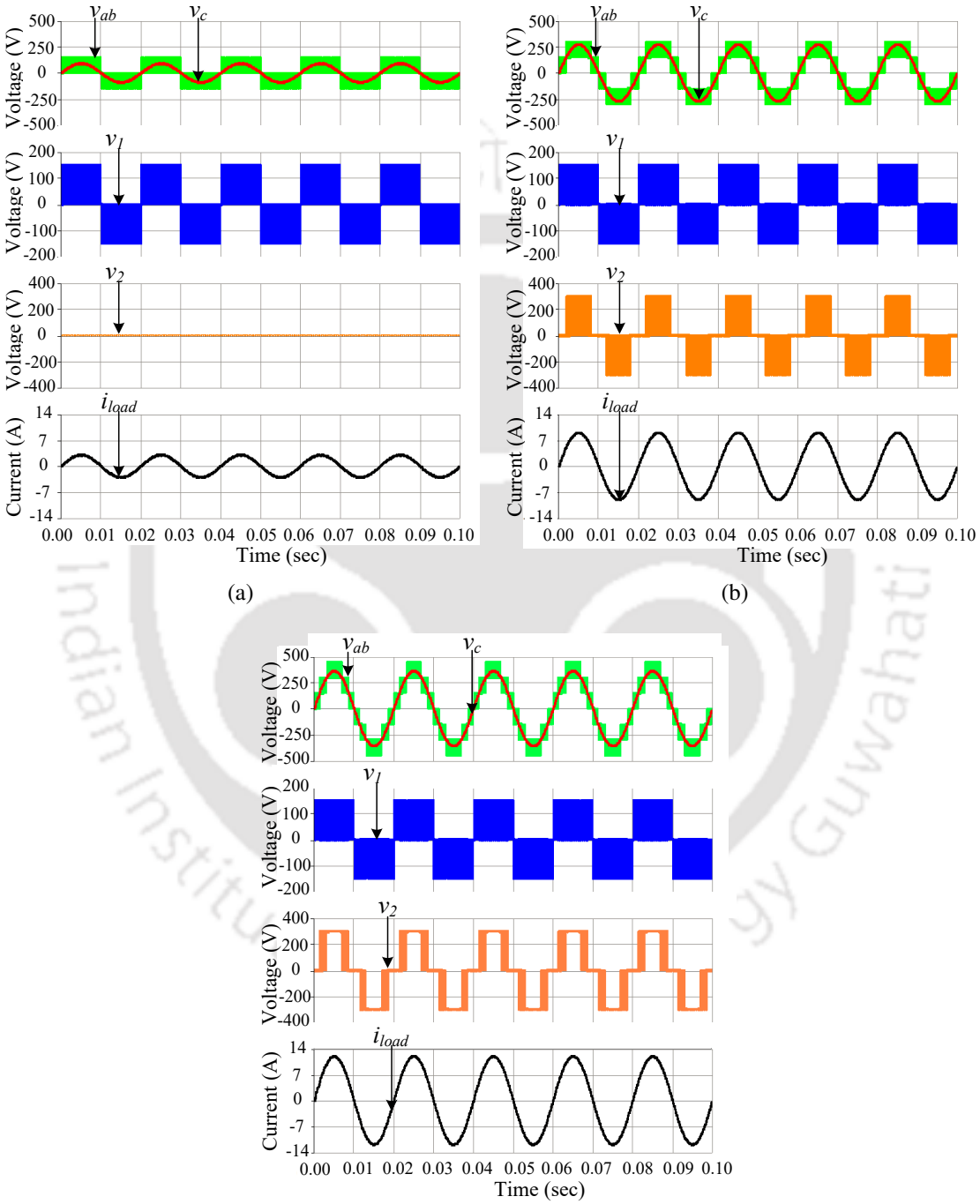


Fig. 2.10 Simulation results for open-loop operation of 7-level RSDCHBMLI at (a) $M = 0.3$ (b) $M = 0.6$ (c) $M = 0.8$

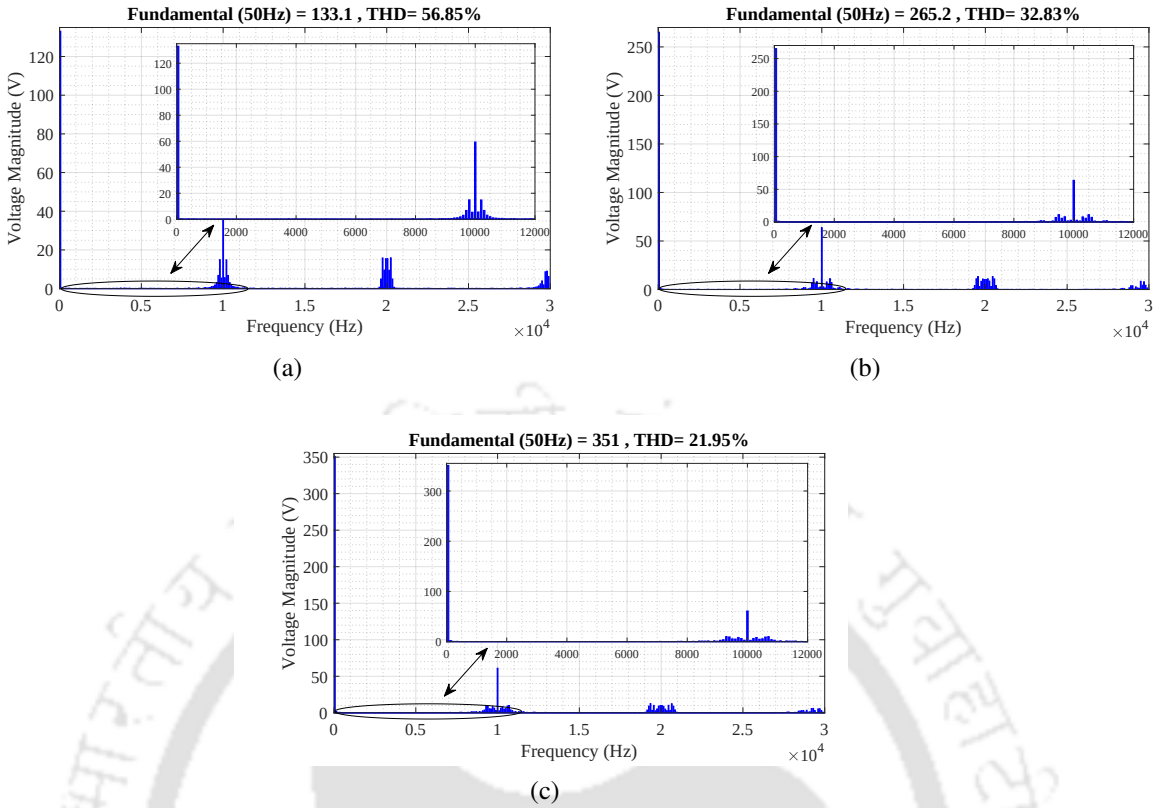


Fig. 2.11 Frequency spectrum of v_{ab}(simulation) for (a) M=0.3 (b) M=0.6 (c) $M = 0.8$

The output of the RSDCHBMLI is shown in Fig. 2.10 where the RSDCHBMLI is operated in open-loop and is supplying a resistive load. The output is obtained for three different cases of modulation index. In Fig 2.10(a), modulation index is 0.3, and thus the RSDCHBMLI generates a 3-level output voltage. This mode of operation corresponds to the scenario shown in Fig. 2.2(a). Here $l = +1$ and $l = -1$ conditions are satisfied and Cell 1 output switches between $+V_{dc}$, 0 and $-V_{dc}$, while Cell 2 output voltage is held at zero. The RSDCHBMLI operation for modulation index of 0.6 is shown in Fig 2.10(b). Here the output voltage is a 5-level waveform and l moves from $+2$ to -2. Here, both Cell 1 and Cell 2 undergo switching as per the pattern shown in Fig. 2.2(b). The RSDCHBMLI generates a 7-level output when the modulation index is increased to 0.8 and is shown in Fig. 2.10(c). Here, Cell 1 output switches between $\pm V_{dc}$ and 0 for all output levels. Cell 2 output switches during $l = \pm 2$, is held at 0 for $l = \pm 1$, and is kept at $\pm 2V_{dc}$ for $l = \pm 3$. Thus, it is seen from the v_{ab} waveforms in Fig 2.10 that number of levels in the output voltage depends on the modulation index and increases with increase in M. Also, v_{ab} is the linear combination of output of Cell 1, v_1 and output of cell 2 v_2. The voltage across the capacitor, v_c is also plotted and is a sinusoidal waveform. The harmonic spectrum of v_{ab} for the three different cases of

Table 2.7 RSDCHBMLI OPERATION FOR THREE DIFFERENT CASES OF MODULATION INDEX

M	V_{ab_f} (V)	V_{ab_f} from FFT (V)	THD (%)	load current (A)	V_{drop} (V)	P_{cond} (W)	P_{sw} (mW)
0.3	95.46	94.12	56.85%	3.14	1.34	6.85	1.75
0.6	190.92	187.52	32.83%	6.25	3.4	25.14	9.54
0.8	254.56	248.19	21.95%	8.27	6.37	44.69	8.17

modulation index is shown in Fig 2.11. The fundamental component of output voltage v_{ab_f} is obtained as

$$v_{ab_f} = 3V_{dc}M \tag{2.21}$$

As the number of levels in the output voltage increases, total harmonic distortion of v_{ab} decreases. The dominant harmonic in all the cases occur at 10 kHz which is the carrier frequency and hence the switching frequency chosen for SC-LS-PWM operation of the inverter. The harmonic spectrum resembles the harmonic spectrum of conventional PD-PWM technique of multi-carrier SPWM, and are clustered around the multiples of switching frequency.

The switching loss for the RSDCHBMLI is computed for the case when the inverter is supplying a purely resistive load. For calculation of conduction loss, Table 2.5 is utilized to obtain the resitance of the current path at every instant of inverter operation. The switching loss and conduction loss is computed at different values of M as shown in Table 2.7. The results obtained are summarized in Table 2.7.

2.6.2 Experimental Results

The results obtained in the simulation are experimentally verified using a laboratory prototype with parameters given in Table 2.8. The laboratory set up is shown in Fig. 2.12. The SC-LS-PWM technique is implemented using TMS320F28335. The

Table 2.8 PARAMETERS FOR EXPERIMENTAL VERIFICATION OF OPEN-LOOP OPERATION OF 7-LEVEL RSDCHBMLI

Parameters	Values
V_{dc}	30 V
Filter parameters, L_f, C_f	0.001 H, 22 μF
Switching frequency, f_s	10 kHz

open-loop results are shown in Fig. 2.13 for three different modulation indices. The

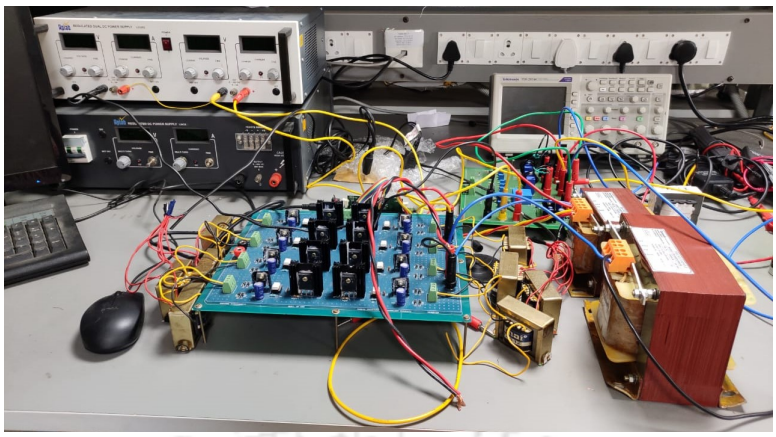


Fig. 2.12 Experimental setup of open-loop RSDCHBMLI

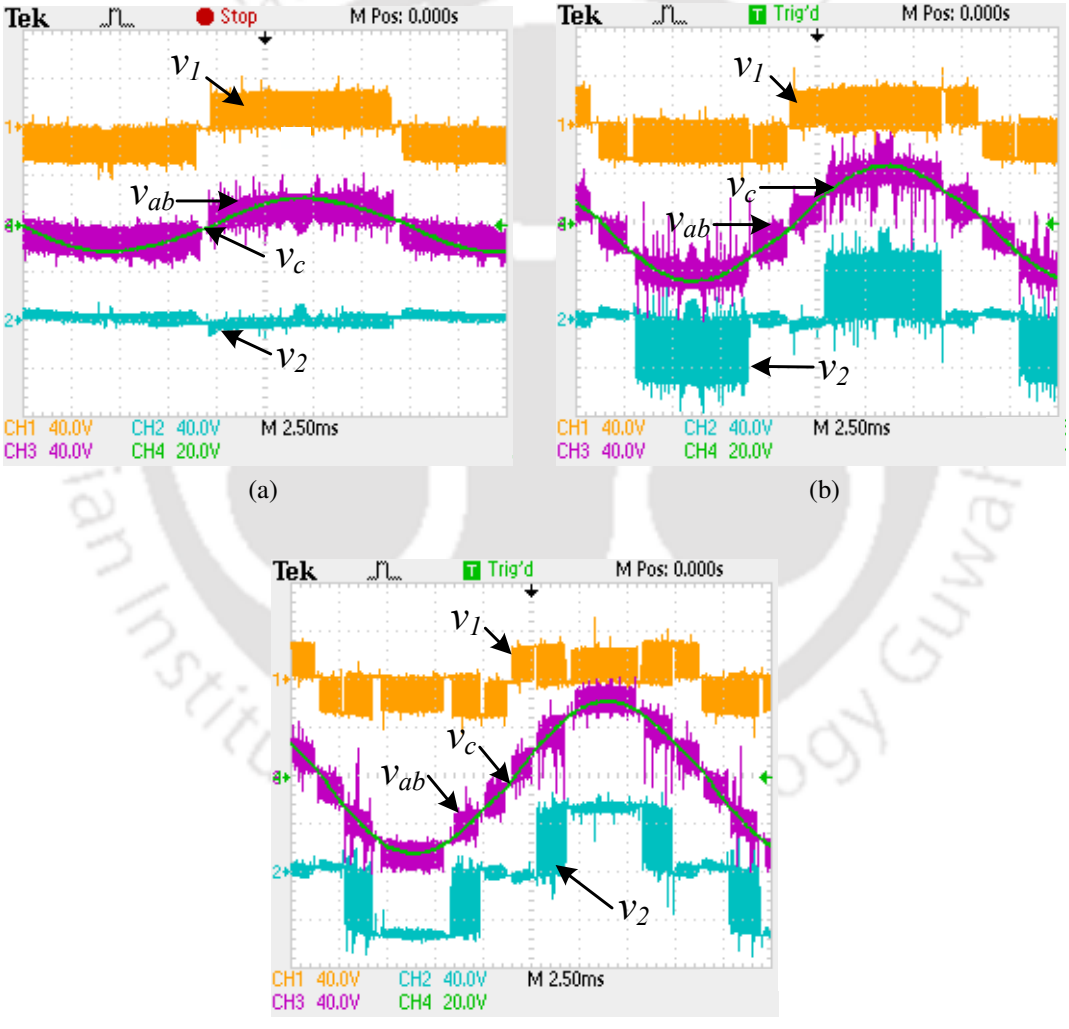


Fig. 2.13 Experimental results for open-loop operation of 7-level RSDCHBMLI at (a) $M = 0.3$ (b) $M = 0.6$ (c) $M = 0.8$

number of levels in the output voltage is affected by the value of M. The inverter generates a 5-level output when $M \geq 0.33$ and a 7-level output when $M \geq 0.66$. Thus Fig 2.13(a) has a 3-level output with negligible value of v_2. The 5-level output with

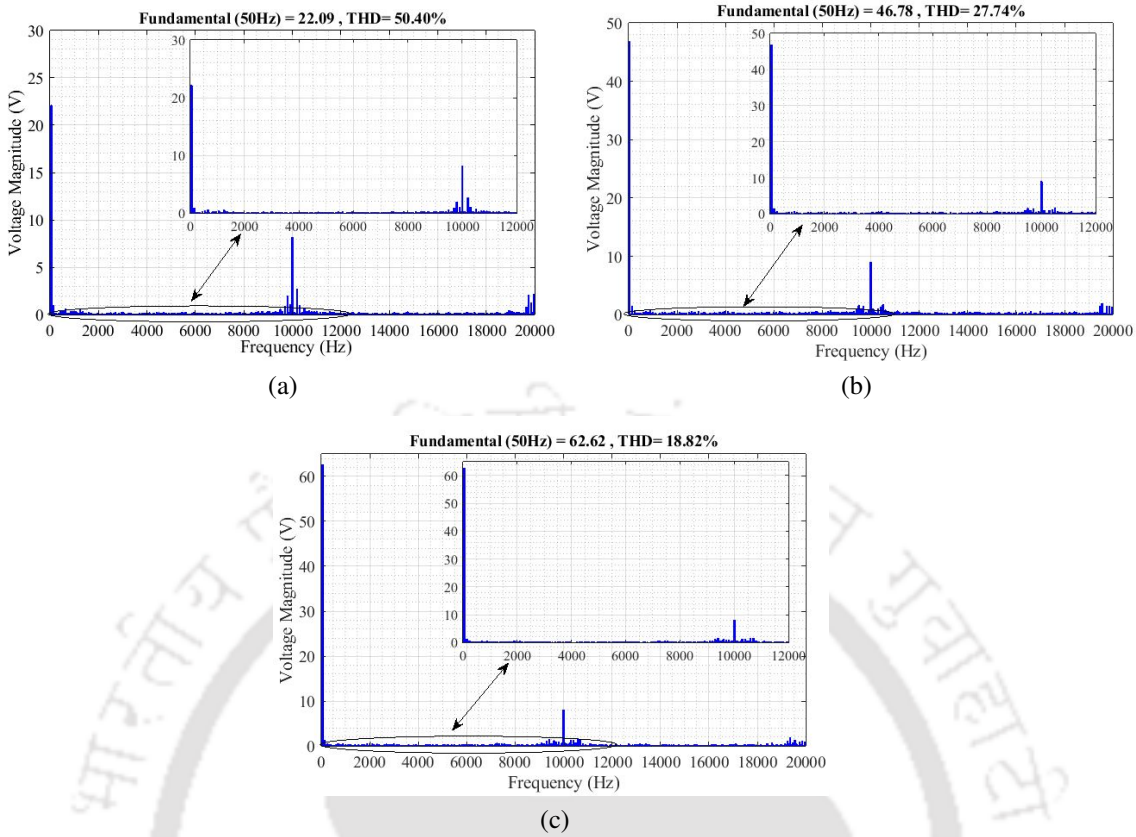


Fig. 2.14 Frequency spectrum of v_{ab}(experiment) for (a) M=0.3 (b) M=0.6 (c) $M = 0.8$

$M = 0.6$ is shown in Fig 2.13(b) and a 7-level output is obtained when $M = 0.8$ as shown in Fig 2.13(b). In each of the cases, the outputs of the individual FBCs are also plotted. The harmonic spectrum of the multilevel output voltage v_{ab} is shown in Fig 2.14, for three cases of M. The results obtained from the simulation are tabulated in Table 2.9. The voltage drop in the RSDCHBMLI inverter due non-idealities are shown in Table 2.9. The drop increases with increase in M. The increase in M also increases the output voltage levels and thus leads to a decrease in THD.

Table 2.9 EXPERIMENTAL RESULTS FOR RSDCHBMLI OPEN-LOOP OPERATION FOR THREE DIFFERENT CASES OF MODULATION INDEX

M	V_{ab_f} (V)	V_{ab_f} from FFT (V)	THD (%)	V_{drop} (V)
0.3	27.0	22.09	50.40%	4.91
0.6	54.0	46.78	27.74%	7.22
0.8	72.0	62.62	18.82%	9.38

2.6.3 Power sharing between FBCs

In this part, the power sharing among the two FBCs are verified for two modulation indices, $M = 0.6$ and $M = 0.8$. The fundamental values of the outputs of individual FBC V_1, V_2, fundamental peak value of the inverter current I_1, and the sinusoidal voltage across the capacitor is shown in Table 2.10. From V_1 and V_2, M_1 and M_2 is also

Table 2.10 MEASURED VALUES FROM EXPERIMENTAL SETUP

M	V_1 (V)	V_2 (V)	V_c (V)	i_1 (A)
0.8	10.7	52.58	63.85	0.91
0.6	15.74	30.52	46.77	0.66

calculated with $V_{dc} = 30$ V. The measured quantities from the experimental circuit are shown in listed in Table 2.10. Using the values in Table 2.10, calculation of M_1 and M_2 is done and values are shown in Table 2.11. The real power sharing among the FBCs are calculated using (2.16) and also (2.18). The values thus obtained are also listed in Table 2.11. It can be seen that values of P_1 and P_2 calculated in terms of M_1 and M_2 is in agreement with the values obtained from (2.16).

The variation of M_1 and M_2 with respect to M is shown in Fig 2.15. Using (2.16), the variation of real power sharing among the FBCs at different values of M is shown in Fig 2.16. It is seen that at lower values of modulation index, $M \leq 0.55$, FBC 1 delivers the higher amount real power while at higher values of modulation index, real power delivered by FBC 2 becomes higher. Utilizing Fig 2.15, the power sharing corresponding to the desired modulation index can be calculated.

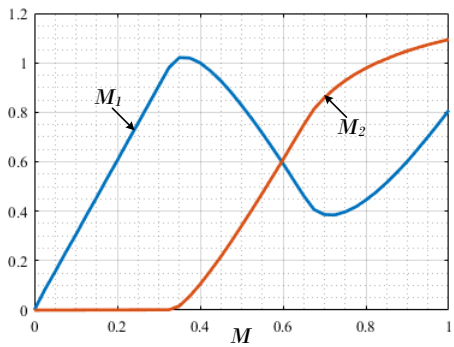


Fig. 2.15 M_1,M_2 vs M

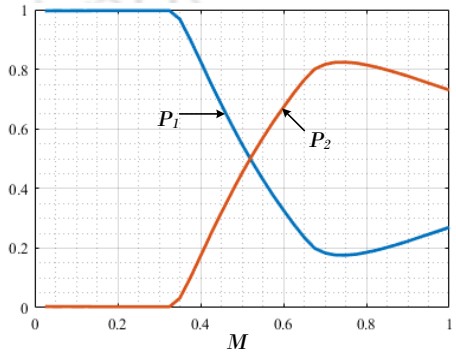


Fig. 2.16 P_1,P_2 vs M

Table 2.11 POWER SHARING

M	M_1	M_2	P_L (W)	P_1 (W) using (2.16)	P_2 (W) using (2.16)	P_1(W) using (2.18)	P_2 (W) using (2.18)
0.8	0.356	0.876	25.48	4.28	21.20	4.33	21.14
0.6	0.52	0.51	13.67	4.64	8.89	4.56	9.11

2.7 Conclusion

In this chapter, the topology and operation of the 7-level RSDCHBMLI is described in detail. The topology is also compared with other existing MLI topologies to demonstrate the benefits of RSDCHBMLI like usage of fewer components, reduction in voltage stress and total blocking voltage, and 3 times boosting ability. The increase in current stress for 4 switches in Cell 2 is a drawback of the inverter. The inverter is operated in open-loop using a single carrier level shifted PWM technique which enables easier practical implementation of the circuit. The switching loss and conduction loss of the inverter is computed at three different modulation indices, with three different values of load current. The conduction loss increase with the increase in load current, and is the major source of loss in the inverter while the switching loss in the inverter is negligible. The on-state resistance of the power electronic switches and diodes also cause voltage drop in the RSDCHBMLI and hence, the output voltage obtained in the simulation is slightly lower than the theoretical value. The presence of non-idealities in the circuits, wires and transformers in the practical circuit account for drop in the output voltage from the theoretical value.

CHAPTER 3

CLOSED-LOOP OPERATION OF RSDCHBMLI

In the previous chapter, the topology of RSDCHBMLI is analyzed. The comparison of RSDCHBMLI with other MLI topologies established the benefits of the developed topology. For inverter operation, single-carrier based level shifted modulation technique is presented and loss analysis is also performed. The RSDCHBMLI operation is verified using both simulation and experimental results, in open-loop.

As application of the inverter for power quality improvement demands the closed-loop operation of the inverter for attaining specific control objectives, in this chapter, the RSDCHBMLI operation is extended to investigate its closed-loop performance. This chapter details both voltage controlled and current controlled operation of RSDCHBMLI using state-feedback control (SFB). In the first section, the inverter is operated in standalone mode to maintain output voltage across the capacitor at desired value. Here the SFB control law is modified with an additional term for improved tracking of reference voltage. As the gains for SFB controller are obtained by solving the continuous time algebraic Ricatti equation, this chapter also investigates the effect of parameters of Ricatti equation on the closed-loop system poles. In the second section, the RSDCHBMLI is operated in the grid connected mode to inject desired power into the grid, which is attained through control of injected grid current. The current control is also attained using SFB control augmented with integral action. The closed-loop operation of RSDCHBMLI for both standalone and grid connected modes are substantiated with simulation and experimental results.

This chapter is organised into three sections. Section 3.1 describes the voltage control of the RSDCHBMLI and Section 3.2 describes the current controlled operation. The voltage control of RSDCHBMLI is further divided into two subsections where Subsection 3.1.1 describes the state-feedback control for reference tracking, followed the simulation and experimental results in Subsection 3.1.2. The current controlled operation of RSDCHBMLI is also divided into four subsections. The system description of the grid connected RSDCHBMLI is given in Subsection 3.2.1. The design of the *LCL*

filter is presented in Subsection 3.2.2. The control technique is detailed in Subsection 3.2.3 and the results are presented in Subsection 3.2.4. The last section of the chapter, Section 3.3 summarizes the findings of the closed-loop operation of RSDCHBMLI and concludes the chapter.

3.1 Voltage control of RSDCHBMLI in standalone mode

The schematic of the RSDCHBMLI in stand-alone mode is shown in Fig. 3.1. The RSDCHBMLI supplies a load through an inductive-capacitive filter denoted by L_f and C_f. The cut-off frequency of the filter is chosen such that sinusoidal voltage is available across the filter capacitor C_f. The aim is to control v_c at the desired value in presence of load changes. The RSDCHBMLI output should also be able to track the change in the reference voltage. To attain these objectives, state-feedback control technique is used, along with SC-LS-PWM method. This results in a constant switching frequency operation of RSDCHBMLI and thus choice of cut-off frequency for the filter is simplified.

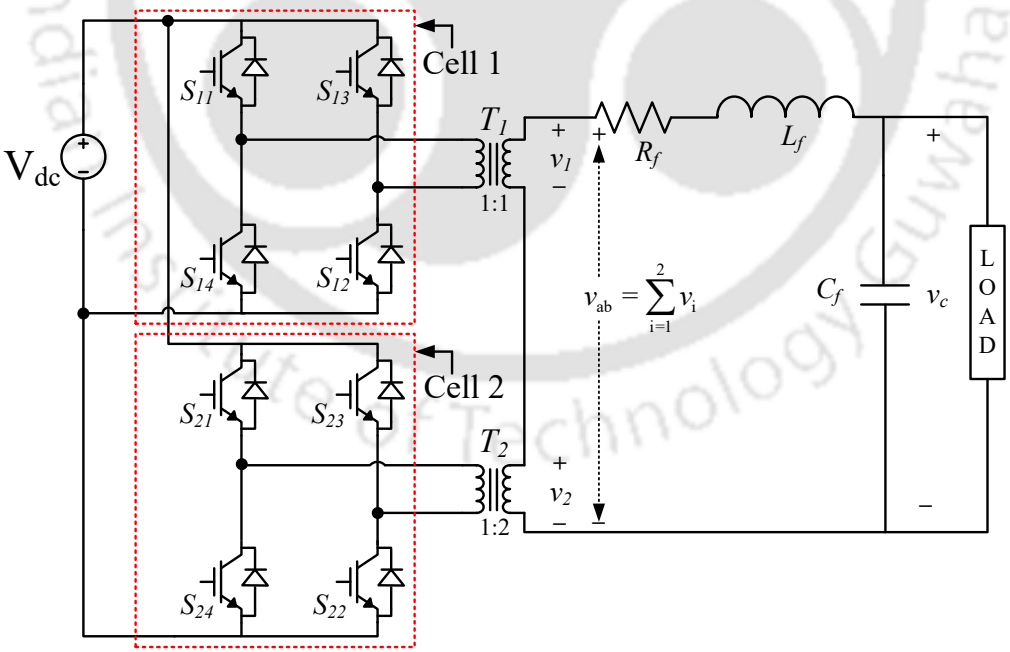


Fig. 3.1 Single-phase RSDCHBMLI circuit with LC filter supplying a standalone load

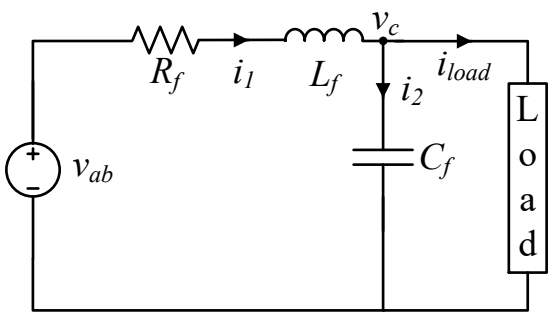


Fig. 3.2 Equivalent circuit of single-phase 7-level RSDCHBMLI supplying a load

3.1.1 Reference voltage tracking using State-feedback control

The 7-level RSDCHBMLI of Fig. 3.1 can be represented as an equivalent circuit as shown in Fig. 3.2. The inverter output is designated as a voltage source v_{ab} where $v_{ab} = uV_{dc}$, $u \in \{-3,-2,-1,0,+1,+2,+3\}$ depending on the output level of the inverter. Thus v_{ab} is a multilevel waveform. The inverter output is passed through a low-pass LC filter with cut-off frequency $f_c < f_{sw}$. In voltage controlled mode operation (VCM), v_c is to be maintained at the desired value v_{cref}, under conditions of load changes. The VCM operation of RSDCHBMLI is realized using SFB control with an additional term r for reference tracking. To differentiate this modified control law from the conventional SFB control where only errors of the state-variables are used to calculate the control law, the SFB control with additional term for reference tracking is denoted as (SFBR) control in this thesis. The control law obtained from SFBR control is used in SC-LS-PWM modulation of the inverter to obtain switching signals with constant frequency.

To obtain SFBR control law for voltage control of RSDCHBMLI, the state-space model of the equivalent circuit shown in Fig. 3.2 is required. The state variables are chosen as inverter output current i_1 and capacitor voltage v_c. The state-space model is obtained as follows:

$$\begin{aligned}
&\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B_1}v_{ab} + \mathbf{B_2}i_{load}; \quad y = \mathbf{C}\mathbf{x} \\
&\mathbf{x} = \begin{bmatrix} i_1 \\ v_c \end{bmatrix}; \quad \mathbf{A} = \begin{bmatrix} -\dfrac{R_f}{L_f} & -\dfrac{1}{L_f} \\ \dfrac{1}{C_f} & 0 \end{bmatrix}; \quad \mathbf{B_1} = \begin{bmatrix} \dfrac{1}{L_f} \\ 0 \end{bmatrix} \\
&\mathbf{B_2} = \begin{bmatrix} 0 \\ -\dfrac{1}{C_f} \end{bmatrix}; \quad \mathbf{C} = \begin{bmatrix} 0 & 1 \end{bmatrix}
\end{aligned} \tag{3.1}$$

To investigate the stability of the system, the characteristic equation for the open-loop system can be obtained from (3.1) as

$$|s\mathbf{I}-\mathbf{A}|=0 \tag{3.2}$$

$$s^2+\frac{R_f}{L_f}s+\frac{1}{C_fL_f}=0 \tag{3.3}$$

From (3.3), it is observed that all coefficients s are of the same sign, which indicates that that open-loop system is stable when R_f is non-zero. The natural frequency w_n and damping factor ζ of the open-loop system is given by

$$\omega_n=\frac{1}{\sqrt{L_fC_f}};\qquad \zeta=0.5R_f\frac{C_f}{L_f} \tag{3.4}$$

For attaining the control objective for tracking v_{cref}, the control law for the closed-loop operation of above state-space system is defined as

$$u_c=-\mathbf{K}(\mathbf{x}-\mathbf{x_{ref}}) \tag{3.5}$$

where $\mathbf{x_{ref}}$ indicates the desired references for the state variables and $\mathbf{K}$ is the gain for SFB control, which is given by

$$\mathbf{K}=r^{-1}\mathbf{B_1}^T\mathbf{P} \tag{3.6}$$

In (3.6) r is a measure of the control effort and $\mathbf{P}$ is a symmetric real matrix, obtained by solving the steady state algebraic Ricatti equation [69], given by

$$\mathbf{A}^T\mathbf{P}\mathbf{B_1}r^{-1}\mathbf{B_1}^T\mathbf{P}+\mathbf{P}\mathbf{A}+\mathbf{Q}=0 \tag{3.7}$$

$\mathbf{Q}$ is a positive semi-definite matrix that gives relative weights to each of the state variables. The value of $\mathbf{K}$ depends on the choice of $\mathbf{Q}$ and r. If $\mathbf{K}$ obtained in (3.6) is expressed as $\mathbf{K}=[K_1\ K_2]$, then the natural frequency and damping factor of the closed-loop system and the gains are related as

$$\omega_n=\sqrt{\frac{1+K_2}{C_fL_f}};\quad \zeta=\frac{0.5(R_f+K_1)}{\sqrt{1+K_2}}\sqrt{\frac{C_f}{L_f}} \tag{3.8}$$

Hence if the desired damping and natural frequency of the closed-loop system is specified, then instead of using (3.6) to compute the gains, the gain matrix can be calculated

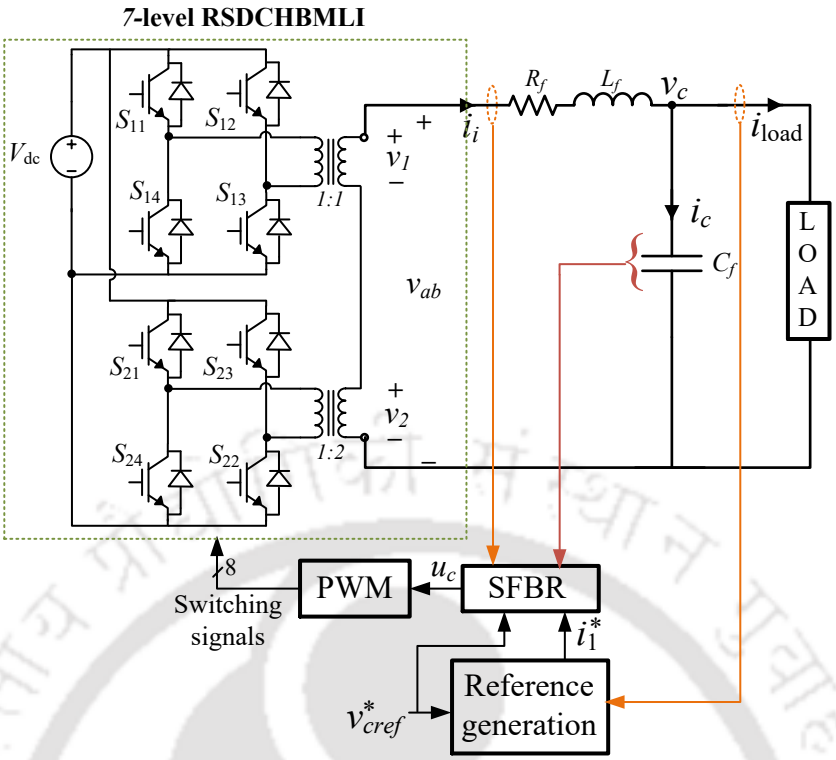


Fig. 3.3 Schematic diagram of output reference voltage tracking by RSDCHBMLI using SFBR control

using (3.8) and can be used in (3.5) to obtain the control law.

To ensure that v_c tracks the desired reference voltage, an additional term is added to (3.5) [69] such that the control law is now modified to

$$u_c = -\mathbf{K}(\mathbf{x} - \mathbf{x_{ref}}) + K_r v_{cref} \tag{3.9}$$

K_r is calculated from the assumption that, in absence of disturbances, the system should be stable and track the desired reference. The gain K_r is obtained as [69]

$$K_r = -[\mathbf{C}(\mathbf{A} - \mathbf{B_1}\mathbf{K})^{-1}\mathbf{B_1}]^{-1} \tag{3.10}$$

The control law, u_c, thus formulated using (3.20), (3.9) and (3.10) is used as the reference signal for SC-LS-PWM operation of the inverter as

$$v_m = \frac{u_c}{3V_{dc}} \tag{3.11}$$

The complete control block diagram of voltage controlled mode of RSDCHBMLI is shown in Fig 3.3.

Table 3.1 SIMULATION PARAMETERS FOR STANDALONE OPERATION OF RSDCHBMLI

Parameters	Values
DC voltage V_{dc}	150 V
Reference voltage v_{cref}	230 V
Fundamental frequency f_g	50 Hz
Filter parameters, L_f, C_f	0.001 H, 22 μF
Resistance, R_f	0.02 Ω
Switching frequency f_s	10 kHz

3.1.2 Results

The operation of RSDCHBMLI is simulated in PSCAD/EMTDC software, and verified using a low power laboratory prototype. The second order low pass LC filter is designed such that the cut-off frequency f_c lies between the fundamental frequency f_g which is 50 Hz, and the switching frequency f_s that is 10 kHz. The cut-off frequency here is chosen as 1 kHz. In case of inverter operation with variable switching frequency, filters with lower value of cut-off frequency and hence larger size, are used [70].

A. Simulation results

The simulation parameters for 7-level RSDCHBMLI are given in Table 3.1. For the closed-loop operation using SFB control, the gain matrix $\mathbf{K}$ and gain K_r are obtained as

$$\mathbf{K} = [1.2195 \quad 0.0165] \qquad K_r = 1.0165 \tag{3.12}$$

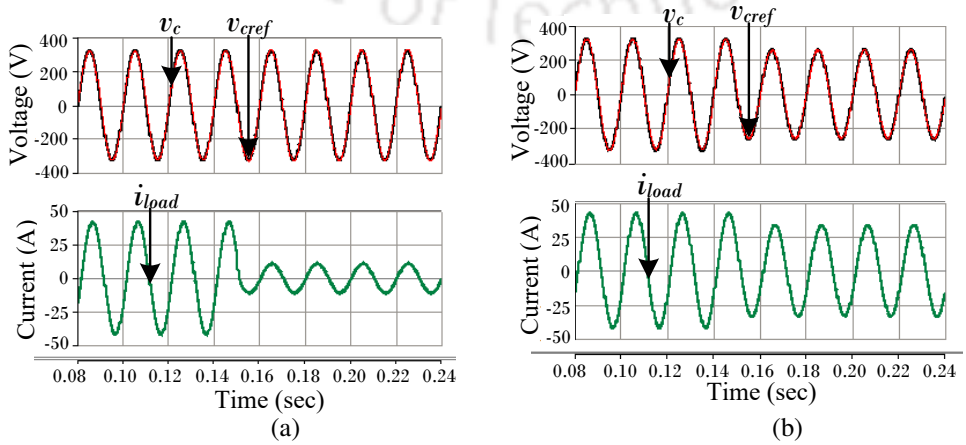


Fig. 3.4 Closed-loop operation of 7-level RSDCHBMLI (a) with step change in load (b) with step change in v_{cref}

The output of the RSDCHBMLI operating in voltage controlled mode is given in Fig. 3.4. The inverter is supplying a single-phase load with $z_{load} = (7 + j3.14)\ \Omega$. It is seen that capacitor voltage v_c is tracking the reference voltage v_{cref} in Fig 3.4(a). At 0.15 seconds, the resistive load changes from 7 Ω to 30 Ω as indicated by the change in peak value of i_{load} in Fig 3.4(a). The capacitor voltage v_c is maintained at the reference value despite step change in load. In Fig 3.4(b) the effect of step change in the reference quantity is examined. The reference voltage is changed to 80% of v_{cref} at 0.15 seconds. The plot of v_c and v_{cref} show that the SFB controller is able to track the changes in the reference quantity and the voltage is also maintained at the new reference.

B. Sensitivity of closed-loop poles to parameter variation in algebraic Ricatti equation

To compute the gains of SFBR controller, algebraic Ricatti equation (ARE) is used. The ARE given in (3.7) is solved to determine the value of **P** which is then used to compute **K**. From (3.7) and (3.6), it is clear that the value of **P** and hence, that of **K** is affected by the choice of **Q** and r. As establishment of analytical relationship between **Q**, r and **K** is not feasible, it is necessary to numerically investigate the effect of **Q** and r on the overshoot and damping of the system. The knowledge about the effect of **Q** and r on system damping and overshoot will facilitate easier choice of subsequent values of **Q** and r after the initial guess.

To observe the effect of various values of **Q** and r on the system poles, first the open-loop and closed-loop poles of the system are shown in in Fig. 3.5. It can be seen that the open-loop system has poles located close to the imaginary axis with overshoot as 99.5% and damping of 0.00148. To observe the effect of r on the system, **Q** is held

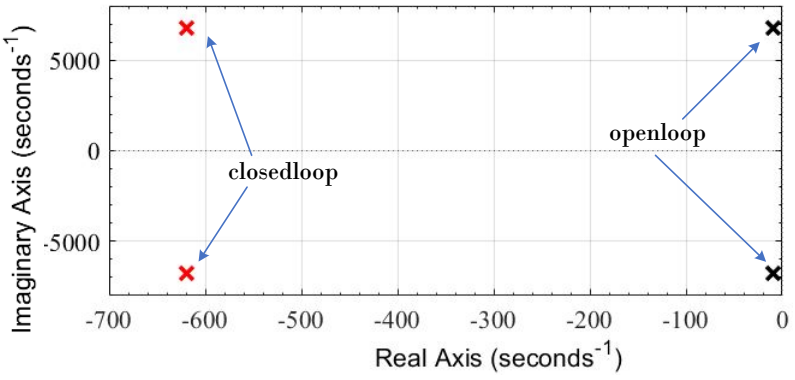
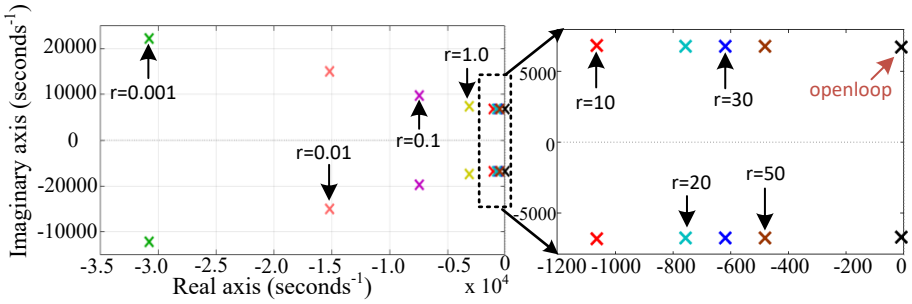
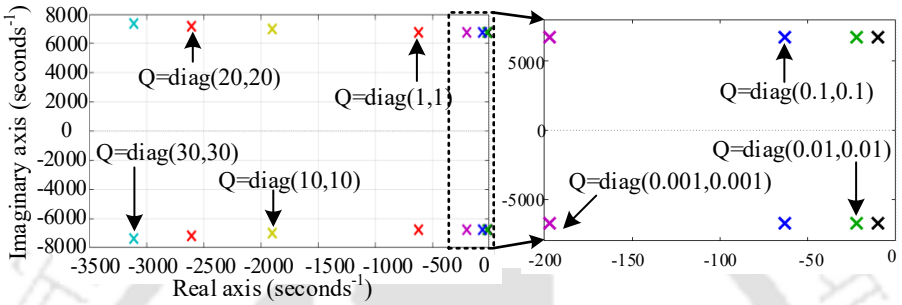


Fig. 3.5 The open-loop and closed loop poles of the RSDCHBMLI with output filter.



(a)



(b)

Fig. 3.6 Closed-loop poles: (a) Varying r with $\mathbf{Q} = diag(1,1)$ (b) Varying $\mathbf{Q}$ with $r = 30$

Table 3.2 EXPERIMENTAL PARAMETERS FOR STANDALONE OPERATION OF RSDCHBMLI

Parameters	**Values**	**Parameters**	**Values**
V_{dc}	30 V	Filter parameters, L_f, C_f	0.001 H, 22 μF
v_{cref}	60 V, peak	Switching frequency, f_s	10 kHz

constant and r is varied from $r = 0.001$ to $r = 50$ as shown in Fig 3.6(a). It is seen that increase in the value of r moves the system poles towards the imaginary axis and thus increases the overshoot with decrease in damping. Similarly, when r is held constant and $\mathbf{Q}$ is varied as shown in Fig 3.6(b), it is seen that an increase in Q shifts the pole pair away from the imaginary axis, increasing the damping in the closed-loop system, and hence decreasing the overshoot.

In this paper, the value of $r = 30$ and $\mathbf{Q} = diag(1,1)$ is chosen and the closed-loop system poles are also shown in Fig. 3.5. In the closed-loop system, the poles move away from the imaginary axis into the left half s-plane, improving the stability of the system and reducing the overshoot. The closed-loop system is under damped with damping of 0.0912 and an overshoot of 75%. This choice of $\mathbf{Q}$ and r ensure a good reference tracking of v_{cref} under dynamic conditions of changes in load parameters and reference values.

C. Experimental verification

The results obtained in the simulation are experimentally verified using a laboratory prototype with the paramaters given in Table 3.2. The single carrier SPWM technique is implemented using TMS320F28335. The closed-loop operation of the 7-level RSDCHBMLI is shown in Fig. 3.7. The inverter supplies a resistive load of 60 Ω. The multilevel waveform is shown in Fig. 3.7(a) and its frequency spectrum is shown in Fig. 3.7(b). The fundamental output voltage comes out to be 61.8 V, which has a 3% tracking error. Fig 3.7(c) shows the terminal voltage when the load is suddenly changed from 37 Ω to 60 Ω. The SFBR controller operation is verified by providing a step change in the reference from 45 V to 35 V, as shown in Fig. 3.7(d), where the capacitor voltage is seen to track the change in the reference.

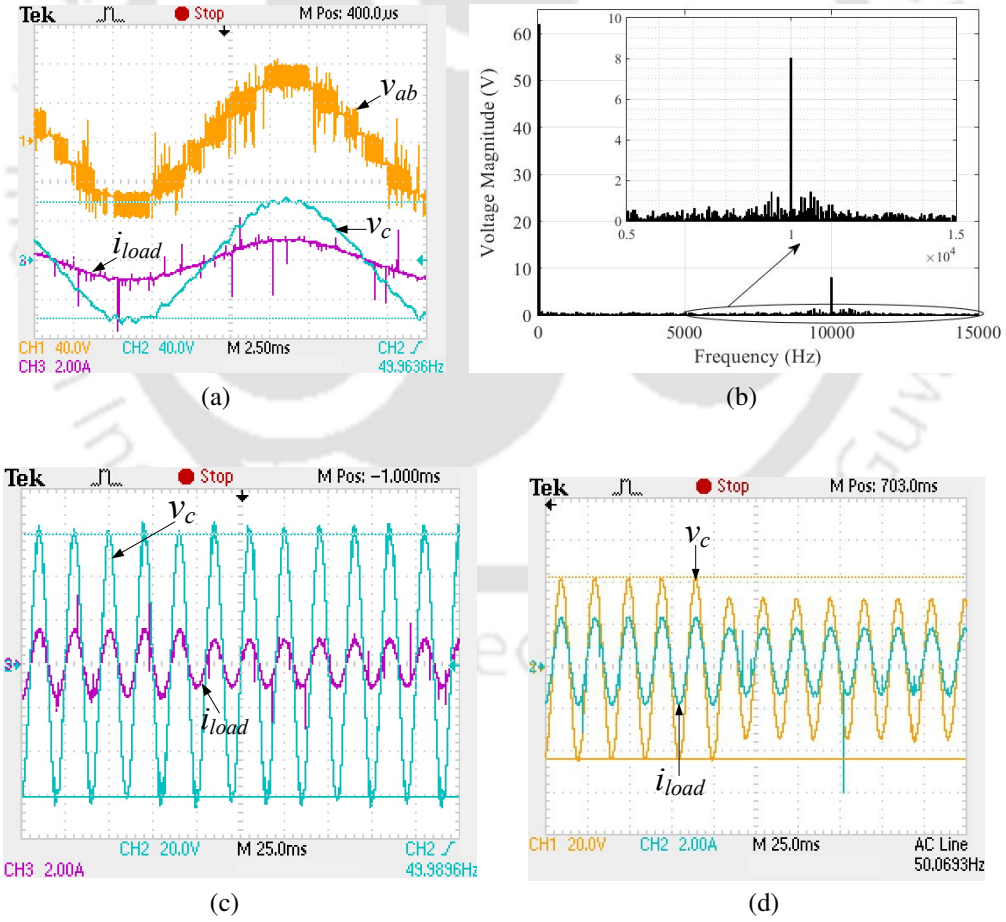


Fig. 3.7 Closed-loop operation: (a) steady state operation with $R = 60\ \Omega$ (b) FFT of v_{ab} (c) with 50% step change in load (d) with 22% step change in v_{cref}

3.2 Current control of RSDCHBMLI in grid connected mode

With increase in distributed generation and integration of renewable energy resources, the grid connected operation of inverters is gaining importance. Further, to operate RSDCHBMLI as DSTATCOM, the inverter must operate in grid connected mode with current control. Hence in this section, the grid connected operation of the RSDCHBMLI is explored. For operation of grid-connected inverters, various control techniques are available in the literature [71]–[75]. In [71], it is shown that proportional resonant controller gives poor performance when there is variation in the system parameters. Though the dynamic performance and current tracking is improved in synchronous reference frame-proportional integral controller (SRF-PI), usage of multiple PI controllers [72] poses the problem of tuning the parameter gains. The PI based vector control approach is extensively used in controlling three-phase grid connected inverters, but its implementation in a single-phase system requires generation of a delay [73] in the system with deteriorates the dynamic performance of the system. In the recent years, usage of model predictive control (MPC) in grid-connected inverter is gaining popularity [74], [75] because of its simplicity, flexibility in cost function and good transient response, but high computational burden and variable switching frequency are two main drawbacks of MPC.

In this section, the current control of grid connected RSDCHBMLI is implemented using state-feedback and integral control (SFBI) with SC-LS-PWM technique. As compared to the proportional-resonant controller [76], SFBI control results in better dynamic performance. In comparison to predictive control [75], the SFBI control requires less calculations, is robust to parameter variations and operates with a constant switching frequency.

3.2.1 Grid connected RSDCHBMLI system

The configuration of the grid connected RSDCHBMLI is shown in Fig. 3.8. The multilevel output v_{ab} is obtained by cascading the outputs of individual H-bridges with the help of transformers. The transformer turns ratios are chosen as $1:1$ and $1:2$ so that a 7-level waveform can be generated using minimum number of components as compared to conventional H-bridge inverters [77]. The RSDCHBMLI is connected to the

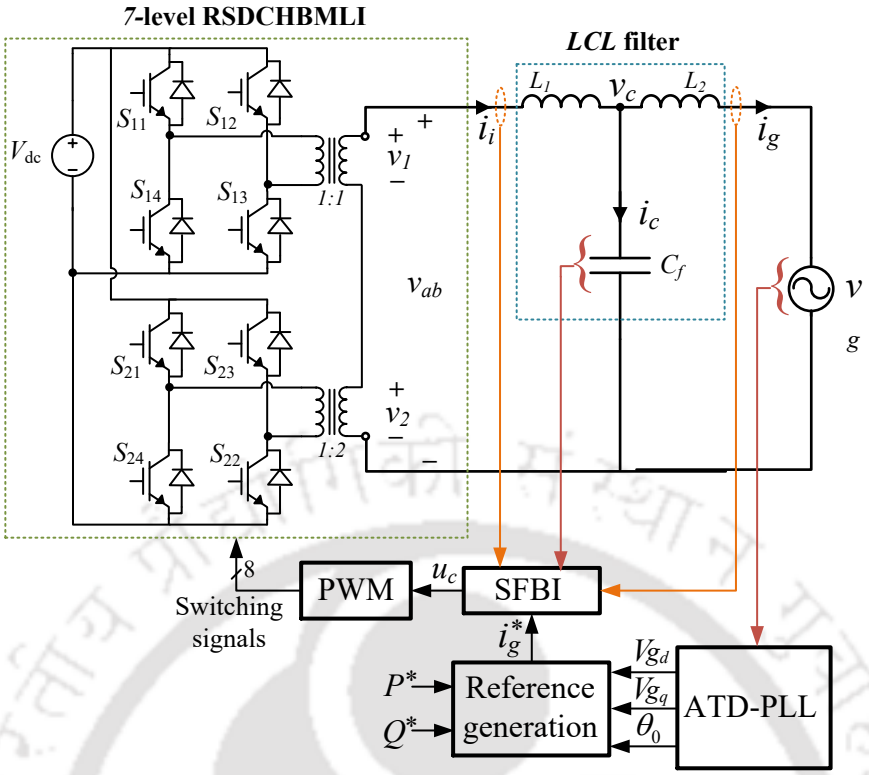


Fig. 3.8 7-level grid connected RSDCHBMLI with *LCL* filter

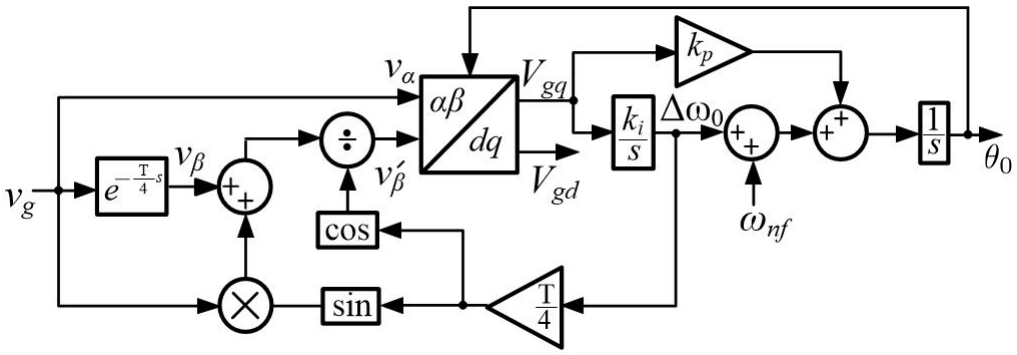


Fig. 3.9 Schematic of ATD-PLL

grid by the means of an *LCL* filter which offers better attenuation of switching harmonics with reduction in overall size and cost as compared to conventional *L* filters [78]. For synchronizing RSDCHBMLI with the grid, adaptive time delay-phase locked loop (ATD-PLL) is used [79]. ATD-PLL has fast dynamic response and a simple structure as shown in Fig. 3.9. The main advantage of ATD-PLL over other time-delay based PLLs is that it can work without phase-offset and double frequency error oscillations even when the grid frequency shifts from the nominal value. The gains k_p and k_i are selected based on damping factor and natural frequency of the ATD-PLL system which affect the settling time, overshoot and phase margin of the system. The input to the ATD-PLL is the grid voltage v_g and the output gives the phase θ_0 and frequency ω_g. The PLL

output θ_0 is used for $\alpha\beta$ to dq transformation as shown in Fig 3.9 and given by

$$\begin{bmatrix} V_{g_d} \\ V_{g_q} \end{bmatrix} = \begin{bmatrix} \sin\theta_0 & \cos\theta_0 \\ -\cos\theta_0 & \sin\theta_0 \end{bmatrix} \begin{bmatrix} v_\alpha \\ v'_\beta \end{bmatrix} \tag{3.13}$$

where v_α indicate the grid voltage and v'_β is a signal orthogonal to v_α with same frequency and amplitude. The d-axis component of the grid voltage computed from PLL, V_{g_d} gives the peak value of grid voltage, which is used to calculate the value of i_g required to inject desired power into the grid.

As the RSDCHBMLI should inject desired power into the grid and the grid voltage v_g is fixed, the control of power is done by controlling the injected grid current i_g. The current control is done using SFBI control which generates the control signal u_c. The control law generated from the SFBI block acts as the modulation signal for generation of PWM switching pulses as shown in Fig. 3.8.

3.2.2 Design of *LCL* filter parameters for grid connected operation

For connection of inverter output to the grid, the inverter output must be filtered so as to comply with the grid standards and maintain quality of injected power. Grid connected operation of inverters can be designed to operate with *L* filters or *LCL* filters. Though design of *L* filters are simpler, *L* filters result in poor harmonic attenuation, large voltage drop and large filter size [80]. To overcome the drawbacks of *L* filters, *LCL* filters are used in grid connected inverters. *LCL* filter design is contingent upon different factors like the desired control variable, damping scheme and reactive power produced by the inverter [80]. Here, for control of power injection into the grid, the control variable is the grid-injected current, i_g, as shown in Fig. 3.8. The stability of the grid connected operation depends on the resonant frequency of the *LCL* filter. To calculate the resonant frequency, the equivalent impedance of the *LCL* filter and RSDCHBMLI is calculated, as observed from the grid terminals. The equivalent impedance Z_{eq} in s-domain is calculated as

$$Z_{eq} = \frac{sL_1}{s^2 L_1 C_f + 1} + sL_2 \tag{3.14}$$

where L_1, L_2 are the filter inductors and C_f is the filter capacitor. Using $s = j\omega$, (3.14) is rewritten as

$$Z_{eq} = \frac{j\omega L_1 - j\omega^3 L_1 L_2 C_f + j\omega L_2}{1 - \omega^2 L_1 C_f} \tag{3.15}$$

At resonance frequency ω_r, the imaginary part of Z_{eq} should be zero. Thus,at ω_r,

$$j\omega_r L_1 - j{\omega_r}^3 L_1 L_2 C_f + j\omega_r L_2 = 0 \tag{3.16}$$

From (3.16), ω_r is calculated at

$$\omega_r = \sqrt{\frac{L_1 + L_2}{L_1 L_2 C_f}} \tag{3.17}$$

The *LCL* filter resonant frequency can be demarcated into two distinct regions- the low resonant frequency region where active damping is necessary for stability and the high frequency region where implementation of i_g feedback ensures stable operation of the system. The cross-over of these two regions occur at the critical resonant frequency ω_c where it is not possible to design a stable current control [78]. The critical resonant frequency of the *LCL* filter is obtained from the frequency response and root-loci of the transfer function $G_c(s) = \frac{i_g(s)}{v_{ab}(s)} = \frac{1}{s^3 L_1 L_2 C_f + s(L_1 + L_2)}$ is dependent on the sampling time period, T_{samp} of the system. It is given by [80], [78]

$$\omega_c = \frac{\pi}{3T_{samp}} \tag{3.18}$$

For stable operation of the system with a single current control loop, *LCL* filter parameters should be chosen such that ω_r is significantly greater than ω_c. This also nullifies the requirement of any additional resistor for passive damping [78]. For the resonant frequency to be visible to the digital controller, according to Shanon's sampling criteria, sampling frequency f_{samp} should be atleast equal to $2f_r$ [81]. Thus the critical resonant frequency f_c, resonant frequency f_r, and f_{samp} should satisfy the relation

$$\frac{f_s}{6} < f_r < \frac{f_{samp}}{2} \tag{3.19}$$

For PWM operation of the inverter, the relation between the sampling frequency and switching frequency is dependent on update method used in PWM implementation. If all the measurements are made at the beginning of PWM time period and registers

are updated at the end of the period, then it is single update mode. In this mode, the sampling frequency is same as the switching frequency f_{sw}. Defining $k = \frac{f_r}{f_{sw}}$, equation given in (3.19) becomes

$$2 < k < 6 \tag{3.20}$$

Considering total filter inductance $L_f = L_1 + L_2$, the product $L_f C_f$ is given by [80],

$$L_f C_f = \frac{k^2(1+\mu)^2}{4\pi^2 f_{sw}^2 \mu}, \quad \mu = \frac{L_2}{L_1} \tag{3.21}$$

For optimal size and efficiency of the *LCL* filter, $\mu = 1$ [82] and k is chosen to satisfy (3.20). The minimum filter inductance $L_{f_{min}}$ required to satisfy IEEE-519 standard is given by (3.22) [82],

$$L_{f_{min}} = \frac{1}{h_{sw}\left|\frac{i_{p.u}(h)}{v_{p.u}(h)}\right||1-k^2|} L_b \tag{3.22}$$

where L_b is the base inductance, $h_{sw} = \frac{f_{sw}}{f_g}$, $i_{p.u}(h) = \frac{i_g(h)}{i_g}$ and $v_{p.u}(h) = \frac{v_{ab}(h)}{v_g}$, h being the harmonic order. The nominal grid frequency is indicated by f_g. The filter capacitance C_f is calculated using the base capacitance C_b. From [83], it is seen that the value of the capacitance is affected by position of the sensor and it affects the power factor at PCC by absorbing reactive power. Considering α_{pf} as the maximum power factor variation seen by the grid [81], C_f is obtained as

$$C_f = \alpha_{pf} C_b \tag{3.23}$$

C_f thus calculated is used in (3.21) to obtain the value of L_f. This value should be greater than or equal to $L_{f_{min}}$. To elucidate the filter design procedure adopted in this work, a step by step procedure is given below.

LCL filter design example

1. As grid current i_g is considered as the control variable here, designing the *LCL* filter with resonant frequency much higher than the critical resonant frequency will lead to a stable operation without the requirement of any additional damping scheme.

2. The next step is to chose the value of k to satisfy (3.20). The choice of k deter-

mines the resonant frequency of the *LCL* filter and effects the filter design and performance. A higher value of k leads to better harmonic attenuation, but also increases the stored energy in the filter [80]. Thus, k can be chosen in mid-range of (3.20) to get an optimum filter design. In this case, k is chosen as 3.7.

3. Using this value of k in (3.21), the product of filter inductance and capacitance is calculated as

$$L_f C_f = 1.38 \times 10^{-8} \tag{3.24}$$

4. The next step is the calculate the minimum value of L_f that should satisfy the design requirements. It is done using (3.22). Considering $f_{sw} = 10$ kHz, $h_{sw} = 200$ is obtained. Calculation of $i_{p.u}(h)$ is done using IEEE-519 standards and it is taken as 0.3%. For calculation of $v_{p.u}(h)$, output voltage of RSDCHBMLI at h^{th} harmonic, i.e, at 10 kHz is obtained using the harmonic spectrum of v_{ab}. The base voltage for per unit calculation is taken as the grid voltage $v_g = 230$ V. Utilizing these values in (3.22),

$$l_{f_{min}}(p.u) = 0.021 \tag{3.25}$$

Considering base kVA of the system as 10 kVA, base impedance is calculated to be 5.29 Ω. Thus the minimum value of inductance is

$$L_{f_{min}}(p.u) = 0.35 \text{ mH} \tag{3.26}$$

5. For calculation of C_f, 1% variation of power factor at rated power is considered. So $\alpha_{pf} = 0.01$ is used in (3.23). Thus $C_f = 6\ \mu$F is obtained. The nearest standard value of capacitance, 6.6 μF is taken.

6. Using the value of C_f in (3.24),

$$L_f = 2 \text{ mH} \tag{3.27}$$

Thus $L_1 = L_2 = 1$ mH.

Thus the values of filter inductances and filter capacitance for *LCL* filter is obtained. A bode-plot of the LCL filter is now included as shown in Fig. 3.10. The filter gain magnitude falls to -3 dB at 113 Hz.

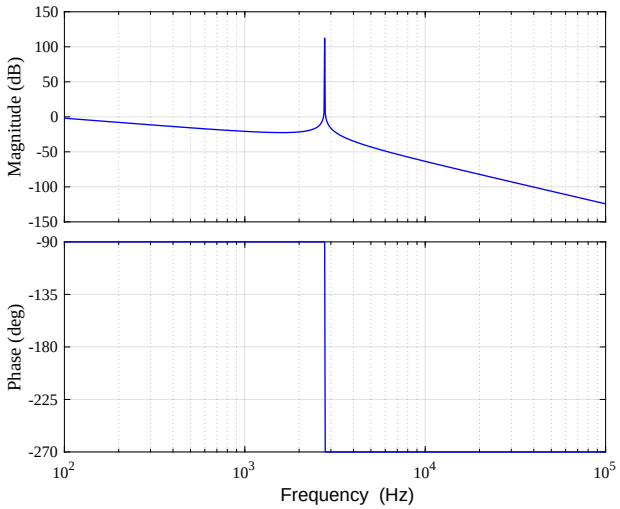


Fig. 3.10 Bode plot of the LCL filter

3.2.3 State-Feedback current control with integral action

In this section, a state-feedback control law is implemented to control the grid current. The use of k_r term for reference tracking is investigated in the previous section. In case of higher order systems, instead of k_r, usage of integral action to reduce the steady state-error is preferred as it can handle uncertainties in the system model. Thus, as in alternative to SFBR control presented in the previous section, SFB control with integral action (SFBI) is implemented for the current control of grid connected RSD-CHBMLI. The integral feedback action also ensures stability and reference tracking in presence of input disturbances [69]. The state-space model of the system shown in Fig. 3.8 is given by

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B_1} v_{ab} + \mathbf{B_2} v_g \;\; ; \;\; y = \mathbf{C}\mathbf{x} \tag{3.28}$$

where,

$$\mathbf{x} = \begin{bmatrix} i_g \\ i_i \\ v_c \end{bmatrix} ; \; \mathbf{A} = \begin{bmatrix} 0 & 0 & \frac{1}{L_2} \\ 0 & 0 & -\frac{1}{L_1} \\ -\frac{1}{C_f} & \frac{1}{C_f} & 0 \end{bmatrix} ; \; \mathbf{B_1} = \begin{bmatrix} 0 \\ \frac{1}{L_1} \\ 0 \end{bmatrix}$$
$$\mathbf{B_2} = \begin{bmatrix} -\frac{1}{L_2} \\ 0 \\ 0 \end{bmatrix} ; \; \mathbf{C} = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix} \tag{3.29}$$

As the control objective is to track the reference grid current i_g^*, error between the reference and the measured grid current is defined as $q(t)$ and this is incorporated in the state space model as the fourth state variable [69].

$$q(t) = \int_0^t (y(\tau) - r(\tau))d\tau \tag{3.30}$$

where $y(\tau)$ indicate the output of the system, i_g at time $t = \tau$, and $r(\tau)$ is the reference quantity i_g^* at $t = \tau$. Taking $q(t)$ as another state-variable, and using (3.30), the modified state-space system is given by

$$\begin{aligned} \begin{bmatrix} \dot{\mathbf{x}}(t) \\ \dot{q}(t) \end{bmatrix} &= \begin{bmatrix} \mathbf{A} & 0 \\ \mathbf{C} & 0 \end{bmatrix} \begin{bmatrix} \mathbf{x}(t) \\ q(t) \end{bmatrix} + \begin{bmatrix} \mathbf{B_1} \\ 0 \end{bmatrix} v_{ab} + \begin{bmatrix} \mathbf{B_2} \\ 0 \end{bmatrix} v_g - \begin{bmatrix} 0 \\ 1 \end{bmatrix} r(t) \\ y &= \begin{bmatrix} \mathbf{C} & 0 \end{bmatrix} \begin{bmatrix} \mathbf{x}(t) \\ q(t) \end{bmatrix} \end{aligned} \tag{3.31}$$

The SFBI control law for (3.31) is obtained

$$u_c = -\mathbf{K}(\mathbf{x} - \mathbf{x_{ref}}) + H \int_0^t (y(\tau) - r(\tau))d\tau \tag{3.32}$$

where $[\mathbf{K}, H]$ indicate the gains of the SFBI control law. $\mathbf{K}$ indicates gains corresponding to the errors between the measured state vector $\mathbf{x}$ and reference state vector $\mathbf{x_{ref}}$. The gain H corresponds to the integral of the error in reference tracking which is used as a feedback in the model for improvement of steady state performance. These gains are computed by solving the continuous time algebraic Ricatti equation. The reference state vector $\mathbf{x_{ref}}$ is obtained from the desired power to be injected into the grid. Let P^*, Q^* be the desired real power and reactive power to be injected into the grid. The reference current to be injected into the grid, in dq domain is given by (3.33) where V_{gd} and V_{gq} are obtained from the ATD-PLL as shown as Fig 3.9.

$$\begin{bmatrix} I_{gd}^* \\ I_{gq}^* \end{bmatrix} = 2 \begin{bmatrix} V_{gd} & V_{gq} \\ V_{gq} & -V_{gd} \end{bmatrix}^{-1} \begin{bmatrix} P^* \\ Q^* \end{bmatrix} \tag{3.33}$$

Using dq to $\alpha\beta$ transformation,

$$\begin{bmatrix} I^*_{g\alpha} \\ I^*_{g\beta} \end{bmatrix} = \begin{bmatrix} \cos\theta_0 & -\sin\theta_0 \\ \sin\theta_0 & \cos\theta_0 \end{bmatrix} \begin{bmatrix} I^*_{g_d} \\ I^*_{g_q} \end{bmatrix} \tag{3.34}$$

i^*_g is then obtained as,

$$i^*_g = I^*_{g\alpha} = I^*_{g_d}\cos\theta_0 - I^*_{g_q}\sin\theta_0 \tag{3.35}$$

After determination of i^*_g, v^*_c and i^*_i are obtained from (3.29) as,

$$\begin{aligned} v^*_c &= L_2\frac{di^*_g}{dt} + v_g \\ i^*_i &= i^*_g + C_f\frac{dv^*_c}{dt} \end{aligned} \tag{3.36}$$

The reference values of the state variables obtained from (3.35) and (3.36) are used in (4.34) to calculate u_c. The control law u_c is scaled by $3V_{dc}$ to generate modulation signal v_m that is used in SC-LS-PWM to obtain the switching signals.

$$v_m = \frac{u_c}{3V_{dc}} \tag{3.37}$$

3.2.4 Results

A. Simulation Results

The grid connected operation of RSDCHBMLI is simulated in PSCAD/EMTDC using the parameters given in Table 3.3. The filter parameters are chosen as per the design procedure given in subsection 3.2.2. The operation of 7-level RSDCHBMLI is investigated for different cases as tabulated in Table 3.4. For each of the cases, the

Table 3.3 SIMULATION PARAMETERS FOR GRID CONNECTED RSDCHBMLI

Parameters	Values
DC voltage V_{dc}	150 V
Grid voltage v_g	230 V
Grid frequency f_g	50 Hz
Filter capacitance C_f	6.6 μF
Filter inductances $L_1 = L_2$	1.0 mH
Switching frequency, f_{sw}	10 kHz

Table 3.4 POWER INJECTION SCENARIOS FOR SIMULATION

	P^* (kW)	Q^* (kVAr)	power factor
Case A	9	4.35	0.9, leading
Case B	9	0	unity
Case C	9	4.35	0.9, lagging
Case D	4.5	0	unity

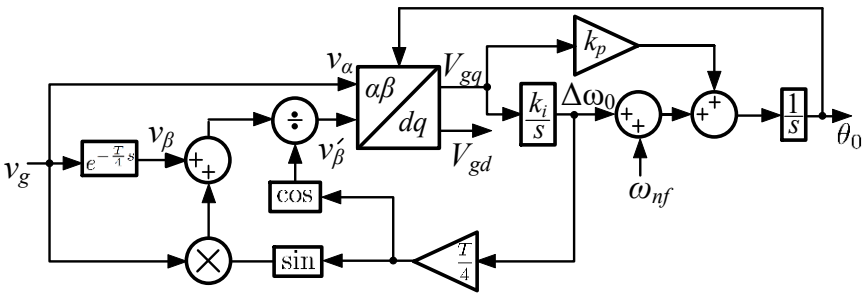


Fig. 3.11 Parameters obtained from ATD-PLL: (a) Frequency (b) Phase error

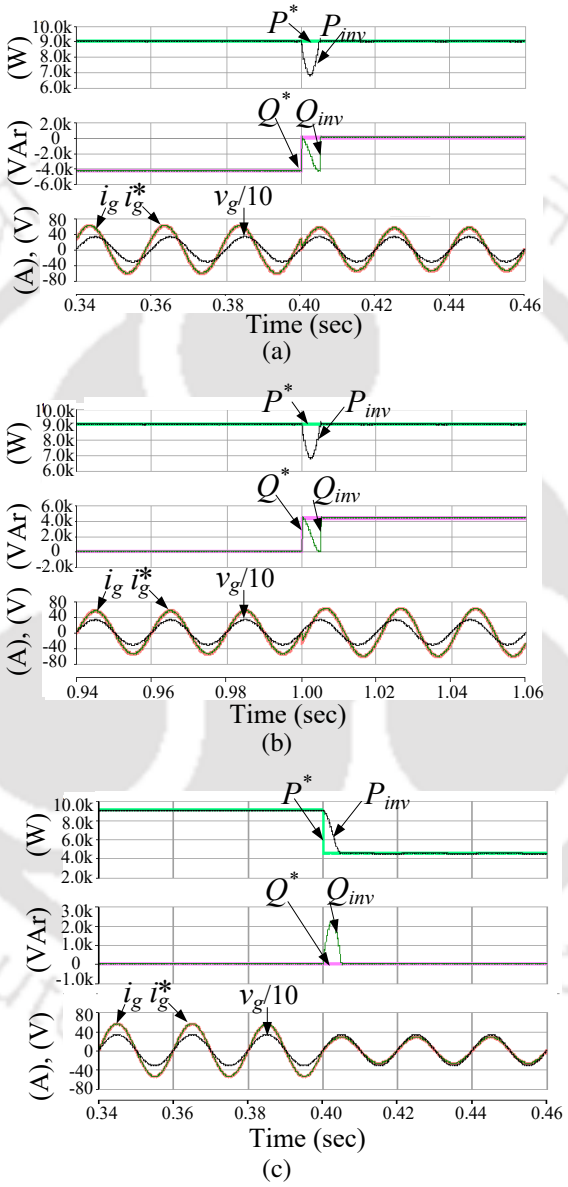


Fig. 3.12 RSDCHBMLI operation under different conditions: (a) Step change from Case A to Case B (b) Step change from Case B to Case C (c) Step change from Case B to Case D

reference value of the injected grid current, i_g^*, is calculated using (3.35). The reference values of other state variables are calculated using (3.36). The ATD-PLL operation is shown in Fig. 3.11. To verify the working of the ATD-PLL, a +5 Hz step change in frequency of the sensed signal is applied. It is seen that ATD-PLL is successful in

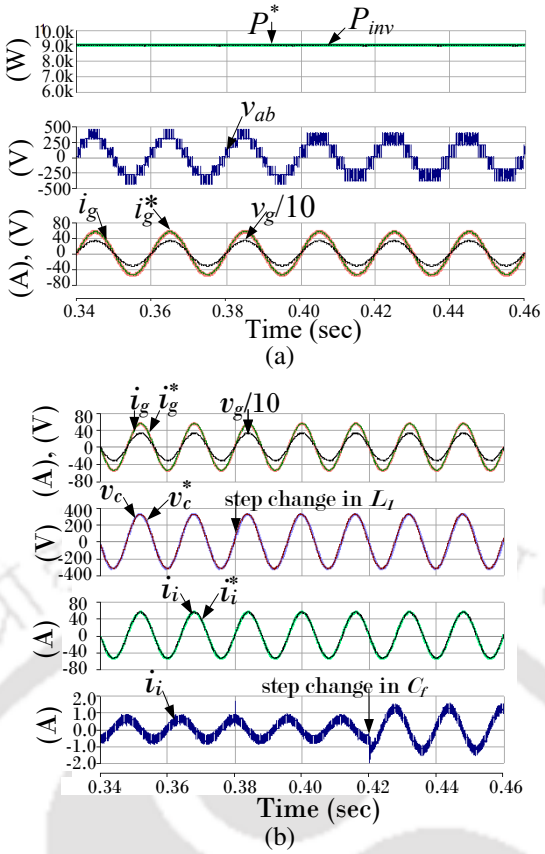
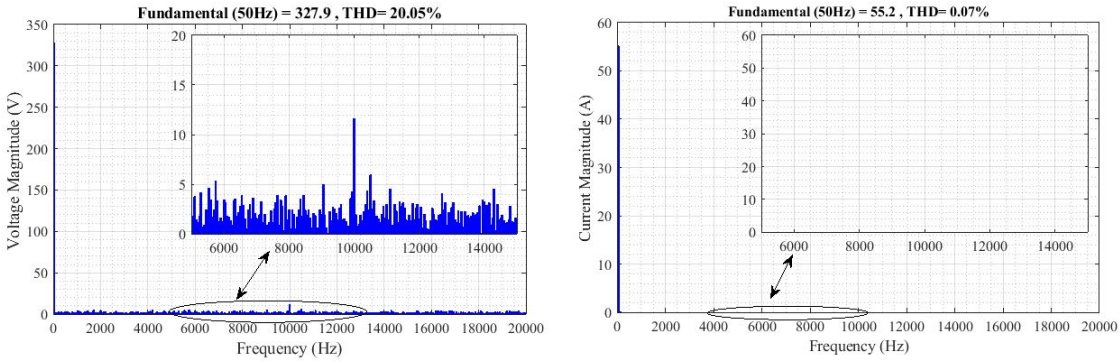


Fig. 3.13 RSDCHBMLI operation under parameter variation (a) Step change in V_{dc} (b) 100% step change in L_1 and C_f

tracking the change in frequency and the phase error is maintained at 0^{deg} both during the nominal and off-nominal grid frequency. Fig. 3.12(a) shows the operation of the grid connected RSDCHBMLI for Case A. It is seen that the real power and reactive power injected by the inverter tracks the desired value of P^* and Q^* as given in Table 3.4. At 0.4 seconds, there is a step change in Q^* from -4.35 kVAr (Case A) to 0 kVAr (Case B). It is seen that the Q_{inv} settles at the new reference in less than 1 cycle. The injected grid current i_g, which was leading grid voltage v_g in Case A, now becomes in phase with v_g. Fig. 3.12(b) indicates a step change from Case B to Case C where the power factor changes from unity to 0.9 lagging. Here also, P_{inv} is held at the desired value and Q_{inv} settles at the new reference of 4.35 kVAr. In the next case, the power factor of the system is held constant at unity and the reference real power is changed from 9 kW (Case B) to 4.5 kW (Case D) at 0.4 seconds. From Fig 3.12, it is verified that the grid connected RSDCHBMLI with *LCL* filter is successful in injecting the desired real and reactive powers into the grid. In all the cases, i_g tracks i_g^* with a maximum tracking error of 0.2%. The change in power factor in different cases is verified from i_g and v_g waveforms shown in Fig. 3.12.



(a) (b)

Fig. 3.14 Frequency spectrum of: (a) Multilevel output voltage v_{ab} (b) Injected grid current i_g

The system performance for 33.3% step change in V_{dc} is shown in Fig. 3.13(a). The change in V_{dc} is evident from the decrease in number of levels of the output voltage as the inverter now has to operate at lower modulation index to inject the same real power P as shown. To check the sensitivity of SFBI controller, a 100% change in L_1 and C_f is given at 0.4 seconds and 0.45 seconds respectively, as shown in Fig. 3.13(b). The current tracking indicates that SFBI control technique is robust in face of parameter variations. The frequency spectrum of the multilevel voltage, v_{ab}, and grid-injected current, i_g is shown in Fig. 3.14. The dominant harmonic in both cases occur at the switching frequency f_{sw}. The THD of i_g falls to 0.02% which is evident from scarce harmonics in Fig. 3.14(b).

B. Experimental Results

The grid connected operation of the RSDCHBMLI is verified using a low-power laboratory propotype. The set-up is shown in Fig. 3.15, and Fig 3.16 is the circuit diagram of the experimental setup. The parameters for experimental validation are shown in Table. 3.5 for the power injection scenarios listed in Table. 3.6. The experiment

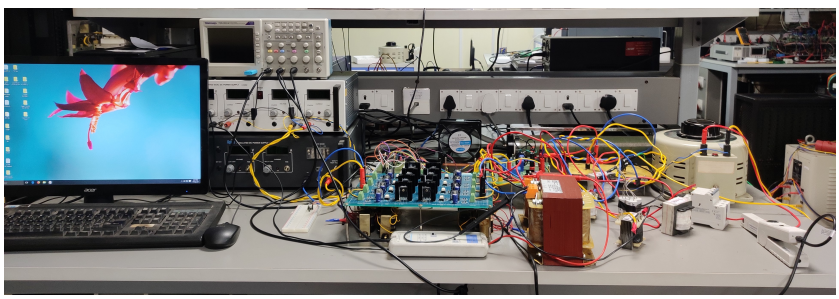


Fig. 3.15 Experimental set-up for grid connected RSDCHBMLI

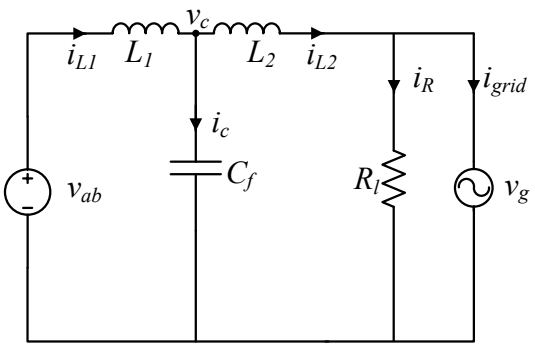


Fig. 3.16 Equivalent circuit for the experimental set-up

is performed with a resistive load R_l connected across the grid. The operation of

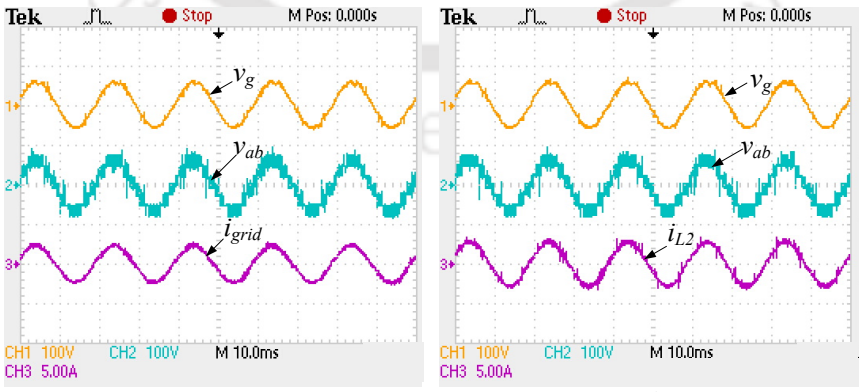
Table 3.5 PARAMETERS FOR EXPERIMENTAL VALIDATION OF GRID CONNECTED RSDCHBMLI

Parameters	Values
DC voltage V_{dc}	30 V
Grid voltage v_g	40 V rms, 50 Hz
Load resistance	110 Ω
Filter capacitance C_f	6.6 μF
Filter inductances $L_1 = L_2$	1.0 mH
Switching frequency, f_{sw}	10 kHz

Table 3.6 POWER INJECTION SCENARIOS FOR EXPERIMENTAL VALIDATION

	P^* (W)	Q^*(VAr)
Case A	80	0
Case B	80	−70
Case C	80	+70

RSDCHBMLI in the grid connected mode for Case A is shown in Fig 3.17(a). The waveform of the current injected by the RSDCHBMLI, i_{L2} is shown in Fig. 3.17(b). Here, as RSDCHBMLI injects power to the grid and load with unity power factor, i_{grid} is in phase with v_g. The power delivered by the RSDCHBMLI to the grid and the load is 79.5 watts. In the second case, the RSDCHBMLI should injects a leading current,

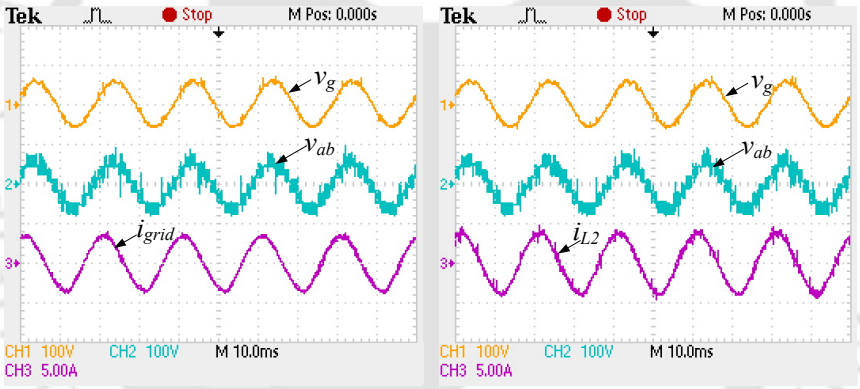


(a) (b)

Fig. 3.17 RSDCHBMLI operation in Case A: (a) Grid voltage, MLI waveform and injected grid current (b) Grid voltage and i_{L2}

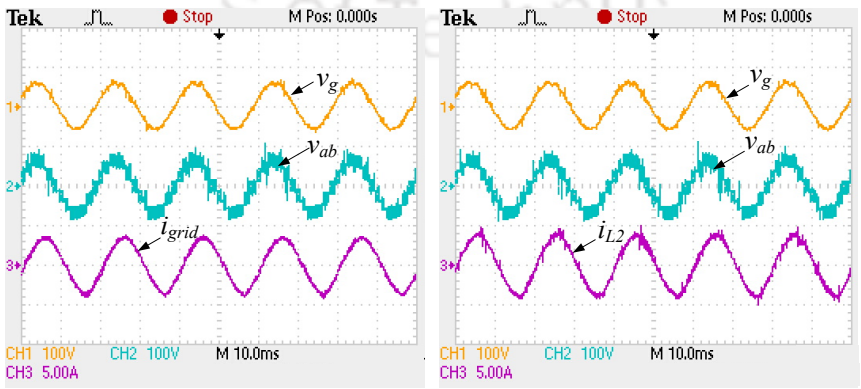
i_{L2} such that it delivers both real and reactive power into the grid and load combination. The experimental results for Case B is shown in Fig. 3.18. Along with grid voltage and

RSDCHBMLI output waveform, injected grid current i_{grid} and injected current into the grid-load combination, i_{L2} is shown in Fig. 3.18(a) and Fig. 3.18(b) respectively. The injected grid current leads the grid voltage in this case. The injected real power is computed as 74.7 Watts and the reactive power is 65 VAr. In Case C, shown in Fig. 3.19, the RSDCHBMLI delivers lagging reactive power to the grid-load combination. The currents i_{grid} and i_{L2} lags the grid voltage v_g as shown. The power injected here is 78 watts and 65.46 VAr. To verify the working of the controller, step changes are given to the system and the results are plotted in Fig. 3.20. In Fig. 3.20(a), a step change is given to the reference reactive power from 0 VAr to +70 VAr. It can be seen that i_{grid} which was initially in phase with v_g for the first two cycles, lags v_g after the step change. Also, the peak value of the injected grid current also increases. This verifies the working of the controller under step changes of reference reactive power. In Fig. 3.20(b), the reference reactive power is kept constant and the real power is given a step change from 50 Watts



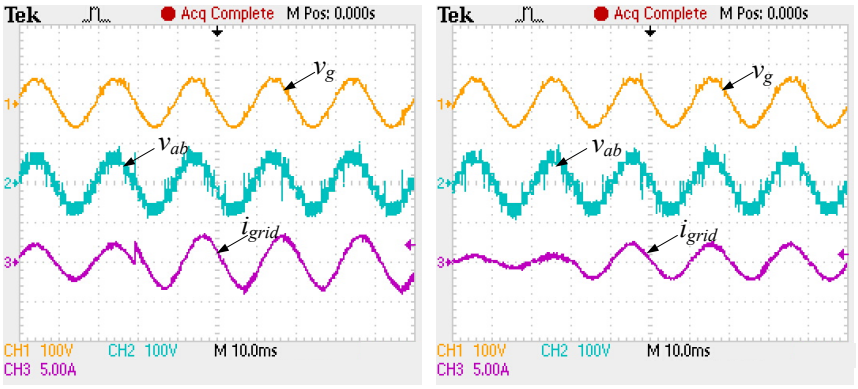
(a) (b)

Fig. 3.18 RSDCHBMLI operation in Case B: (a) Grid voltage, MLI waveform and injected grid current (b) Grid voltage and i_{L2}



(a) (b)

Fig. 3.19 RSDCHBMLI operation in Case C: (a) Grid voltage, MLI waveform and injected grid current (b) Grid voltage and i_{L2}



(a) (b)

Fig. 3.20 RSDCHBMLI operation in Case C: (a) with step change in real power (b) with step change in reactive power

to 80 watts. It is seen that the phase of i_{grid} remains constant and peak value of i_{grid} increases after the step increase P.

Thus from the experimental results, it is seen that the RSDCHBMLI in the grid connected mode can inject desired power into the grid under different power factors. The controller is also capable of tracking the step changes in the reference values.

3.3 Conclusion

In this chapter, the closed-loop operation of the 7-level RSDCHBMLI is presented. In the first section, the output voltage control of the RSDCHBMLI is done using state-feedback control with reference tracking. In the second section, state-feedback control is implemented for grid current when RSDCHBMLI operates in the grid connected mode. In both the cases, it is seen that the state-feedback control in conjunction with single carrier level shifted SPWM modulation is capable of controlling the desired voltage and current. The control technique used here resulted in a constant switching frequency operation of the inverter. The switching frequency here was chosen as 10 kHz, which resulted switching harmonics being obtained at higher frequency ranges. This lead to smaller filter size, along with simpler filter design. The simulation results are verified using a low-power laboratory prototype and results are presented to support the closed-loop operation of RSDCHBMLI.

CHAPTER 4

RSDCHBMLI OPERATION AS DSTATCOM FOR LOAD COMPENSATION

In the literature review presented in Chapter 1, the importance of maintaining good power quality in the distribution system is highlighted. It is discussed that distortion in voltage and current waveform, presence of unbalance and poor power factor lead to financial losses for the user in the form of increased power loss in the system, mal-operation of protective equipment, down-time of operation and degradation of machine health [84]. To alleviate the power quality issues in the distribution system, custom power devices are used [1]. Distribution static compensator (DSTATCOM) is a shunt connected custom power device which can maintain power quality in the distribution network by mitigating current based power quality problems like harmonic distortion, poor power factor and unbalance of source currents [1], [84]. The power electronic interface of the DSTATCOM is usually realized using a voltage source inverter (VSI) which is operated in current controlled mode. A literature survey performed on the power electronic inverters for DSTATCOM realization is also presented in Chapter 1. The survey highlights the popularity of MLIs [17], [21], [22], [26], [41]–[45] over conventional two-level VSIs in DSTATCOM implementation.

In this chapter, the operation of RSDCHBMLI as DSTATCOM is investigated for performing load compensation in a weak distribution system. Comparing RSDCHBMLI with conventional CHBMLI for DSTATCOM implementation, the following points can be observed as given in Table 4.1. It can be noted from the comparison that despite drawbacks of the RSDCHBMLI like unequal current stress and and high current through the DC-link capacitor, the RSDCHBMLI poses as a convenient choice for DSTATCOM implementation as it uses a single DC-link capacitor, eliminates the problem of capacitor voltage balancing, generates multilevel output voltage with boosting effect using smaller number of switches and has inherent isolation due to presence of transformers. The RSDCHBMLI is controlled using two current control techniques, *viz.*, SFBI control and finite control set-model predictive control (FCS-MPC). The RSDCHBMLI based DSTATCOM is successful in load compensation and power factor

Table 4.1 COMPARISON OF 7-LEVEL RSDCHBMLI AND CHBMLI FOR DSTATCOM OPERATION

	RSDCHBMLI	CHBMLI
DC-link capacitor	Single	Multiple
Capacitor voltage balancing issue	Eliminated	Present
Votlage stress	Equal in all switches	Equal in all switches
Current stress	Double in 4 switches	Equal in all switches
Transformers	Present in the inverter topolgy	Required for practical implementation
DC-link current	High current though single capacitor	Handled by submodule capacitors
Inveter failure	Fails with the failure of DC-link capacitor	Can operate with reduced voltage level in case of failure of single submodule capacitor
Switch count	8 switches	12 switches

improvement, along with maintaining a sinusoidal PCC voltage, using both the control techniques. In the next part of the chapter, a comparison between the two control techniques portray the superiority of FCS-MPC in terms of dynamic response and ease of application. The operation of the DSTATCOM is further extended to work with unbalance present in the distribution system voltages. A case study for DSTATCOM operation with different scenarios of load and source voltages is also presented. This chapter also develops a current based DC-bus voltage control technique which allows for easier calculation of controller gains. The current based controller is compared with conventional power based DC-bus voltage controller to establish its advantages over conventional controllers.

This chapter is organised into seven sections. The first section, Section 4.1, gives a detailed description of the DSTATCOM connected to the distribution system for load compensation. The reference current generation scheme is detailed in Section 4.2. In Section 4.3, both the current control techniques, SFBI and FCS-MPC are described while the DC bus voltage control is explained in Section 4.4. The complete control block diagram of the DSTATCOM operation, with both SFBI and FCS-MPC control, is presented in Section 4.5. The results of DSTATCOM operation under various loading conditions constitute Section 4.6, followed by the conclusion in Section 4.7.

4.1 System description

A three-phase distribution system supplying an unbalanced and distorted load, with the DSTATCOM connected at the point of common coupling (PCC) is shown in Fig 4.1. The circuit diagram of the three phase RSDCHBMLI used for realization of the DSTATCOM is shown in Fig. 4.2. The advantages of implementing RSDCHBMLI as DSTATCOM are:

- As the number of switches in MLIs increase with increase in the number of levels of output voltages, large number of switches with high rating are required for connection to medium voltage levels. In this topology, number of components required to generate 7-level waveform is reduced as compared to conventional MLIs.
- The usage of multiple DC-link capacitors are seen in [21], [22], [36], [42]–[44], [46]. In all these topologies, the problem of capacitor voltage balancing poses challenge in the realization and operation of DSTATCOM. It also imposes constraints on the inverter operation, and may require additional circuitry for capacitor voltage balancing. All these issues are eliminated in the RSDCHBMLI based

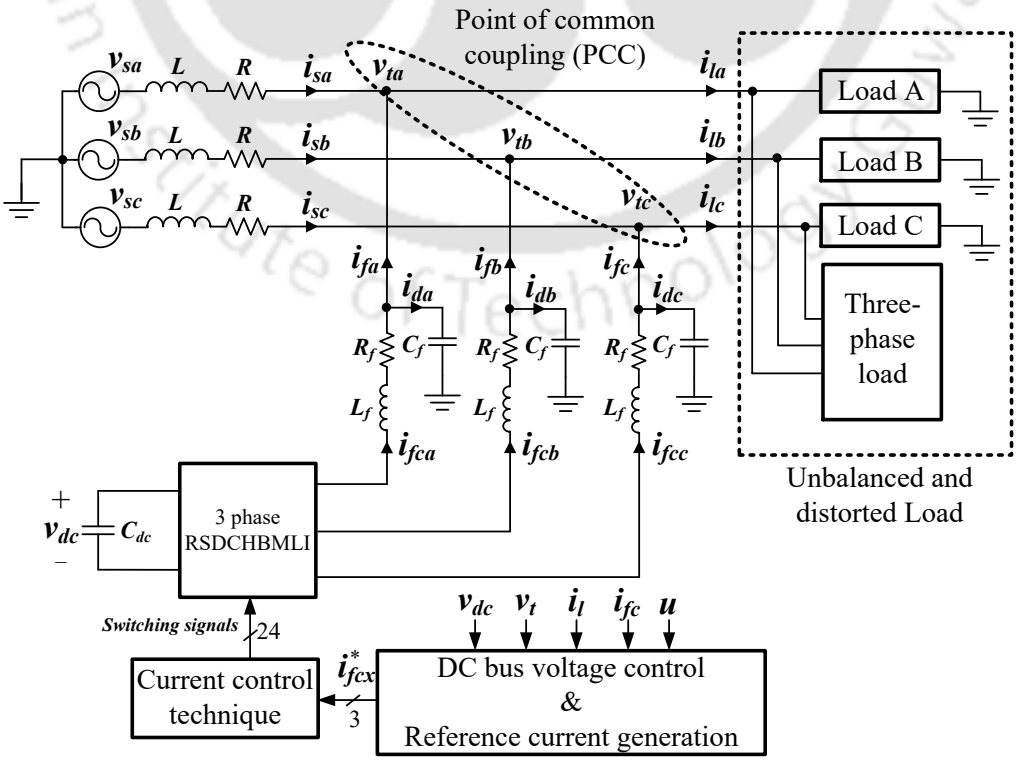


Fig. 4.1 Schematic diagram of RSDCHBMLI connected as DSTATCOM

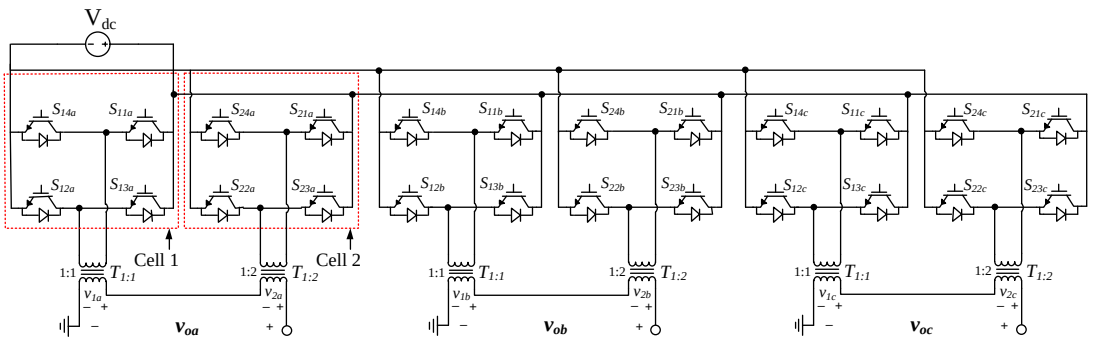


Fig. 4.2 Three phase RSDCHBMLI

DSTATCOM as it uses a single DC-link capacitor.

- The usage of transformers in the RSDCHBMLI ensure inherent isolation between the grid and the power converter, along with eliminating paths for circulating current. Also, the boosting ability of RSDCHBMLI permits usage of smaller DC-link voltage and components with smaller voltage rating.

In the distribution system shown in Fig. 4.1, the feeder impedance of the distribution network is also taken into consideration and is represented as R_f and L_f. In the situation where feeder impedance of the distribution system is negligible, then the voltages at PCC, v_{tx} become same as the distribution system voltages, v_{sx} where $x \in (a,b,c)$. In such situation, the distortion and unbalance in load currents do not affect the PCC voltages. The PCC voltages are also immune to distortion caused by injection of DSTATCOM currents. This configuration of distribution network can be termed as stiff distribution network. As v_{tx} remain sinusoidal and balanced, filter capacitances C_f are eliminated in the stiff network, thereby reducing the system order and complexity. Also, the calculation of reference source currents is simplified as the PCC voltages can be directly utilized for the same in case of stiff networks.

In the distribution system considered in this thesis, feeder impedance of the distribution network is taken into consideration. The PCC voltages are thus susceptible to variations due to voltage drops in the feeder impedances and the distribution network is termed as weak network. In case of weak AC grids, the voltages at PCC are affected by the dynamics of the power electronic converters connected to the PCC [85]. In case of DSTATCOM connected to a weak distribution system, the voltages at PCC are also affected by the injection of non-linear and unbalanced current [86]. The effect of weak grids in the design of control system is tabulated in Table 4.2.

Table 4.2 COMPARISON OF DSTATCOM FEATURES WITH RESPECT TO STRONG AND WEAK AC DISTRIBUTIONS SYSTEMS

	Strong grid (stiff grid)	Weak grid (non-stiff grid)
PCC voltages	Same as source voltage, not affected by injection of DSTATCOM currents.	Affected by injection of DSTATCOM currents, become distorted and unbalanced.
Filter Capacitance	The PCC voltages are sinusoidal and balanced, hence filter capacitors are not required.	Filter capacitors should be connected in each phase to provide a path for switching harmonic current to reduce the distortion in PCC voltages.
Reference current generation	Uses measured PCC voltages directly.	Fundamental positive sequence component of PCC voltages need to be extracted and used in reference current generation scheme.
Control technique	Proportional control techniques like hysteresis control can be used for control of DSTATCOM currents [21].	Hysteresis control cannot ensure the stable control of injected DSTATCOM currents [53]. Hence advanced control techniques are used for current control.

The DSTATCOM injects currents i_{fx} at PCC so that the source currents i_{sx} are regulated to their respective reference values, i^*_{sx}. To reduce the harmonic distortion in PCC voltages, filter capacitor C_f is added in each phase. For DSTATCOM operation, the DC-link of RSDCHBMLI can be realized using a capacitor C_{dc} as shown in Fig. 4.1. The DC-link capacitor C_{dc} and DC-link voltage v_{dc} impact the compensation ability of the DSTATCOM and are selected based upon the voltage level and the kVA rating of the system. The reference average value ,V^*_{dc}, of instantaneous DC-link voltage, v_{dc}, is usually selected to be greater than twice the L-G peak voltage [87]:

$$V^*_{dc} = \frac{2\sqrt{2}V_{LL}}{\sqrt{3}} \tag{4.1}$$

In case of RSDCHBMLI, as the final output voltage is an integral multiple of V_{dc}, for an N-level inverter, the reference voltage is calculated as

$$V^*_{dc} = \frac{2\sqrt{2}V_{LL}}{N'\sqrt{3}} \tag{4.2}$$

where $N' = \frac{N-1}{2}$. Thus, for the same system ratings, the reference DC-link voltage is reduced by N' times in case of RSDCHBMLI based DSTATCOM. The sizing of DC-link capacitor is dependent on the rated kVA of the system [88]. Let the rated kVA of the system be taken as X. If variation in X between twice and half of its rated value leads to a 20% change in average DC-link voltage V_{dc}, and C_{dc} takes n fundamental cycles to get stabilized, the value of C_{dc} is given by [88], where T is the fundamental

time period.

$$C_{dc} = \frac{2(2X - \frac{X}{2})nT}{(1.2V_{dc})^2 - (0.8V_{dc})^2} \tag{4.3}$$

4.2 Reference current generation

For current control of DSTATCOM, the switching signals for the RSDCHBMLI are generated such that the source currents track the reference currents. The reference current generation scheme with balanced and unbalanced source voltages are different and are described in the following subsections.

4.2.1 With balanced source voltages

The aim of load compensation using DSTATCOM is to ensure that even in presence of unbalanced and distorted load, the current drawn from the source should be balanced and sinusoidal, *i.e*, the reference source currents should satisfy

$$i_{sa}^* + i_{sb}^* + i_{sc}^* = 0 \tag{4.4}$$

Also, it is desired that the power factor of the source currents can be set to a desired value, preferably unity, so that the DSTATCOM also helps in power factor correction of source currents. To attain these objectives, use of instantaneous symmetrical components theory for generating reference currents is described in [1].

To obtain the reference current, first symmetrical transformation is applied to the instantaneous values of PCC voltages to resolve them into their symmetrical components.

$$\begin{bmatrix} v_t^0 \\ v_t^+ \\ v_t^- \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \end{bmatrix} \begin{bmatrix} v_{ta} \\ v_{tb} \\ v_{tc} \end{bmatrix} \tag{4.5}$$

Since feeder impedance is considered in this system, the PCC voltages may be distorted due to distortion in the load current and also due to injection of compensator current. So instead of using the directly using the sequence components, fundamental extraction is done from it to get v_{tx1}^+ and subsequent inverse transformation to get the requisite

terminal voltages for computing the reference current.

$$v_{t1}^{+} = \frac{\sqrt{2}}{T_o}\int_{T_o} v_t^{+} e^{-(\omega t - \frac{\pi}{2})} dt, \;\; T_o = \frac{2\pi}{\omega} \tag{4.6}$$

where $\alpha = e^{j\frac{2\pi}{3}}$ and ω is the fundamental frequency in rad/sec.

$$\begin{bmatrix} v_{ta1}^{+} \\ v_{tb1}^{+} \\ v_{tc1}^{+} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha^2 & \alpha \\ 1 & \alpha & \alpha^2 \end{bmatrix} \begin{bmatrix} v_{t1}^{0} \\ v_{t1}^{+} \\ v_{t1}^{-} \end{bmatrix} \tag{4.7}$$

If the reference source currents are desired to be in phase with the PCC voltages, then the phase of positive sequence component i_{sa1}^{*} of source currents and the phase of fundamental positive sequence component v_{ta1}^{+} of terminal voltages should be equal. Thus,

$$\angle v_{ta1}^{+} = \angle i_{sa1}^{*} \tag{4.8}$$

where

$$i_{sa1}^{*} = \frac{1}{\sqrt{3}}(i_{sa}^{*} + \alpha i_{sb}^{*} + \alpha^2 i_{sc}^{*}) \tag{4.9}$$

Also, if the reference source currents are balanced, sinusoidal and in phase with the terminal voltages,then only average value of the load power will be supplied from the source while the compensator will supply the rest of the power demand. Thus, the fundamental positive sequence components of the terminal voltages and the source currents should also satisfy

$$v_{ta1}^{+} i_{sa}^{*} + v_{tb1}^{+} i_{sb}^{*} + v_{tc1}^{+} i_{sc}^{*} = p_{lavg} \tag{4.10}$$

where p_{lavg} is the average power drawn by the load. The reference source currents are then calculated by solving (4.4), (4.8) and (4.10)

$$\begin{bmatrix} i_{sa}^{*} \\ i_{sb}^{*} \\ i_{sc}^{*} \end{bmatrix} = \frac{1}{\sum_{x=a}^{c} v_{tx_1}^{+2}} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_{ta_1}^{+} \\ v_{tb_1}^{+} \\ v_{tc_1}^{+} \end{bmatrix} (p_{lavg}) \tag{4.11}$$

Using (4.11), reference compensator currents i_{fx} is evaluated as:

$$i_{fx}^{*} = i_{lx} - i_{sx}^{*} \tag{4.12}$$

Thus, the reference output current for the RSDCHBMLI, i_{fcx}^{*}, is

$$i_{fcx}^{*} = i_{fx}^{*} + C_f \frac{dv_{tx}}{dt} \tag{4.13}$$

4.2.2 With unbalanced source voltages

For unbalanced voltages, the source currents can be derived to achieve any one of the following three cases [1]:

- Each phase draws equal current from the source

$$\begin{gathered} \text{RMS value of } i_{sa} = \text{RMS value of } i_{sb} = \text{RMS value of } i_{sc} \\ \angle i_{sc} = \angle i_{sb} - 120^{\circ} = \angle i_{sa} - 240^{\circ} \end{gathered} \tag{4.14}$$

- Each phase exhibits equal resistance

$$\frac{v_{sa}}{i_{sa}} = \frac{v_{sb}}{i_{sb}} = \frac{v_{sc}}{i_{sc}} \tag{4.15}$$

- Each phase draws equal average power

$$\frac{v_{sa}i_{sa}}{2} = \frac{v_{sb}i_{sb}}{2} = \frac{v_{sc}i_{sc}}{2} = \frac{p_{lavg}}{3} \tag{4.16}$$

In this thesis, the compensation technique is chosen such that source currents in each phase become equal and are balanced. For this, modified reference current generation algorithm detailed in [89] is utilized in this thesis. As detailed in the previous section, due to distortions that may creep in the PCC voltages, the fundamental components of the v_{tx}, v_{tx1} is used for calculating reference currents.

$$v_{tx1} = \frac{\sqrt{2}}{T_o} \int_{T_o} v_{tx} e^{-(\omega t - \frac{\pi}{2})} dt, \quad T_o = \frac{2\pi}{\omega} \tag{4.17}$$

Let the fundamental component of the unbalanced PCC voltages obtained from (4.17) be given by

$$\begin{aligned} v_{ta1} &= V_{ta1_m} \sin(\omega t) \\ v_{tb1} &= V_{tb1_m} \sin(\omega t + \phi_b) \\ v_{tc1} &= V_{tc1_m} \sin(\omega t + \phi_c) \end{aligned} \tag{4.18}$$

To generate the balanced reference source currents, (4.18) is utilized to generate a set of balanced fictitious PCC voltages given by

$$\begin{aligned} v'_{ta} &= V'_{tm} \sin(\omega t) \\ v'_{tb} &= V'_{tm} \sin\left(\omega t - \frac{2\pi}{3}\right) \\ v'_{tc} &= V'_{tm} \sin\left(\omega t - \frac{4\pi}{3}\right) \end{aligned} \tag{4.19}$$

where

$$V'_{tm} = \frac{V_{ta1_m} + \alpha_b V_{tb1_m} + \alpha_c V_{tc1_m}}{3} \tag{4.20}$$

For unity power factor operation in phase a,

$$\alpha_b = \cos\left(\phi_b + \frac{2\pi}{3}\right), \quad \alpha_c = \cos\left(\phi_c + \frac{2\pi}{3}\right) \tag{4.21}$$

If the source voltages do not have any magnitude unbalance, then the source currents in each of the three phases will be in phase with the terminal voltages. Utilizing (4.19)−(4.21) in the instantaneous symmetrical components theory [89], the reference source can be obtained as

$$\begin{bmatrix} i^*_{sa} \\ i^*_{sb} \\ i^*_{sc} \end{bmatrix} = \frac{1}{\sum_{x=a}^{c} {v'_{tx}}^2} \begin{bmatrix} v'_{ta} \\ v'_{tb} \\ v'_{tc} \end{bmatrix} (p_{lavg}) \tag{4.22}$$

where p_{lavg} is the average power absorbed by the load. From the reference source currents, the reference compensator currents i^*_{fx} are obtained by applying KVL at PCC in Fig. 4.1.

$$i^*_{fx} = i_{lx} - i^*_{sx} \tag{4.23}$$

The reference currents for RSDCHBMLI are given by

$$i^*_{fcx} = i^*_{fx} + C_f \frac{dv_{tx}}{dt} \tag{4.24}$$

4.3 Current control technique

For RSDCHBMLI to operate as DSTATCOM, the inverter is to be operated in current controlled mode (CCM) such that the compensator output currents i_{fa}, i_{fb} and i_{fc} track the desired reference currents i^*_{fa}, i^*_{fb} and i^*_{fc}, respectively. A number of current control strategies like hysteresis [22], [21], [88], deadbeat [90], sliding mode control [45], [91] are available in the literature. Deadbeat control is highly sensitive to parameter variations in the current control loop. Although sliding mode control is impervious to parameter variations and external perturbations, it results in high frequency chattering about the switching line [91]. Hysteresis controller is popular due to its ease of application and fast dynamic response. However, in this work the feeder impedance is taken into consideration and shunt filter capacitors are incorporated in each phase to reduce harmonic content in the voltages at PCC. In such a system, hysteresis current control cannot alone ensure stable current tracking, and can only be applied in conjunction with other control techniques [1], [21], [45]. To verify this, hysteresis current control is applied to a 2-level inverter based DSTATCOM for load compensation. For the simulation parameters given in Table 4.3, and the DC-link capacitor replaced with a DC-voltage source, the source currents are shown in Fig. 4.3. The source currents are distorted and do not track the reference source currents, which indicates that hysteresis control cannot be used for reference current tracking in a weak distribution system. This can also be mathematically verified by applying the Routh-Hurwitz's criterion to the system. For L_l being the load inductance, using parameters given in Table 4.3, the condition of stability as per Routh-Hurwitz's criterion is obtained as (4.25) where hysteresis controller is approximated as a proportional control K_{hys}. As this condition cannot be satisfied for any operating condition, hysteresis controller cannot be used for reference source current tracking in a weak distribution system.

$$L_l > [1 + 285.71 L_l (1 + K_{hys}) + K_{hys}] \tag{4.25}$$

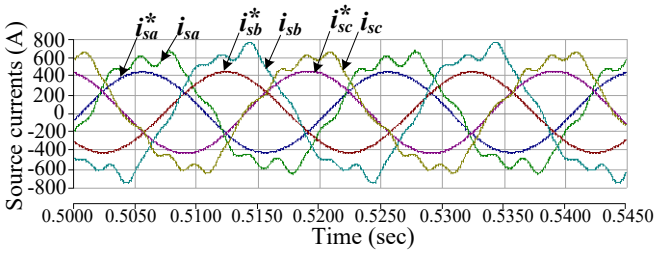


Fig. 4.3 Reference and actual source currents in presence of DSTATCOM operated with hysteresis control

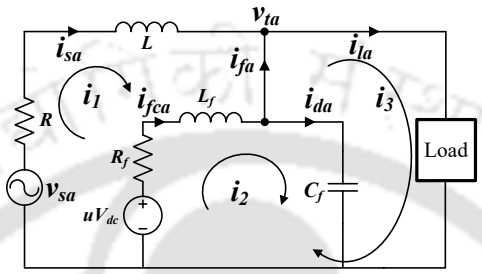


Fig. 4.4 Single-phase equivalent circuit

In this chapter, state-feedback control with integral action (SFBI) and finite control set- model predictive control (FCS-MPC) technique are implemented to generate the switching signals for RSDCHBMLI based DSTATCOM. The state-feedback controller is simple in implementation, and also ensures stability of the system. It is augmented with single-carrier level shifted SPWM (SC-LS-PWM) method that enables constant switching frequency operation of the RSDCHBMLI. One of the disadvantages of SFBI control is the requirement of the SC-LS-SPWM modulator to generate the switching signals. This drawback can be overcome by the usage of FCS-MPC technique. It doesn't require any modulator and has advantages like easier inclusion of non-linearities, fast dynamic response, simplicity and possibility of a multi-objective cost function [92], [93]. But FCS-MPC results in the variable switching frequency and requires higher computation. These two control techniques are compared with respect to their performance in load compensation.

This section is organized into two subsections. The SFBI control, using the state-space model of the system, is detailed in subsection 4.3.1. In Subsection 4.3.2, predictive model of the system is obtained for current control of RSDCHBMLI.

4.3.1 State-feedback control with integral (SFBI) action

For applying state-feedback control to the DSTATCOM, equivalent circuit for phase a is shown in Fig. 4.4. The RSDCHBMLI is represented as uV_{dc}. V_{dc} indicates the average voltage of the DC-link capacitor which should be maintained at V_{dc}^{*}, and $u \in (-3,-2,-1,0,+1,+2,+3)$ depending on the output voltage level of the RSDCHBMLI. For ease of obtaining the state-space model, the load is assumed to be linear and represented with R_l and L_l. As the load, as well as the feeder impedances in the three phases will be different, three different control laws can be obtained for three phases. But as the state-space model with integral action exhibit robustness in the face of parameter variations, the value of feeder impedance or load parameters can undergo changes without effecting the compensation ability of the DSTATCOM. Also, inclusion of non-linear loads in the system is also possible without changing the state-space model and the DSTATCOM is able to perform load compensation.

Considering i_1, i_2, i_3 as the loop currents, KVL can be applied to the loops with currents i_1, i_2 and i_3 to get the following equations

$$\begin{aligned} -v_{sa} + Ri_1 + L\frac{di_1}{dt} + v_{ta} &= 0 \\ -v_{ta} + R_f i_2 + L_f \frac{di_2}{dt} + uV_{dc} &= 0 \\ -v_{ta} + R_l i_3 + L_l \frac{di_3}{dt} &= 0 \end{aligned} \tag{4.26}$$

Utilizing (4.26) and taking i_1, i_2, i_3 and v_{ta} as the four state-variables, the state-space model of the circuit shown in Fig. 4.4 is obtained as

$$\begin{aligned} \dot{\mathbf{x}} &= \mathbf{A}\mathbf{x} + \mathbf{B_1} u V_{dc} + \mathbf{B_2} v_{sa} \\ y &= \mathbf{C}\mathbf{x} \end{aligned} \tag{4.27}$$

where,

$$\mathbf{x} = \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_{ta} \end{bmatrix}; \quad \mathbf{A} = \begin{bmatrix} -\frac{R}{L} & 0 & 0 & -\frac{1}{L} \\ 0 & -\frac{R_f}{L_f} & 0 & \frac{1}{L_f} \\ 0 & 0 & -\frac{R_l}{L_l} & \frac{1}{L_l} \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 & 0 \end{bmatrix}$$

$$\mathbf{B_1} = \begin{bmatrix} 0 \\ -\frac{1}{L_f} \\ 0 \\ 0 \end{bmatrix}; \quad \mathbf{B_2} = \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \end{bmatrix}; \quad \mathbf{C} = \begin{bmatrix} 1 & 0 & 0 & 0 \end{bmatrix} \tag{4.28}$$

Now, as the compensator current must track the reference current, i_{fa} should be considered as a state-variable in phase a. Also, v_{ta} should also be taken as a state-variable as it is desired to maintain v_{ta} at it fundamental value, free from distortion. Thus, the state-vector $\mathbf{x}$ is now modified to $\mathbf{z}$ as shown in (4.29).

$$\mathbf{z} = \begin{bmatrix} i_{fa} \\ i_{da} \\ v_{ta} \\ i_{la} \end{bmatrix} = \begin{bmatrix} -1 & 0 & 1 & 0 \\ 1 & -1 & -1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_{ta} \end{bmatrix} = \mathbf{Px} \tag{4.29}$$

Applying this transformation, (4.27) is modified as

$$\begin{aligned} \dot{z} &= \widetilde{\mathbf{A}} z + \widetilde{\mathbf{B_1}} u V_{dc} + \widetilde{\mathbf{B_2}} v_{sa}; \quad \widetilde{y} = \widetilde{\mathbf{C}} z \\ \widetilde{\mathbf{A}} &= \mathbf{PAP}^{-1}, \quad \widetilde{\mathbf{B_1}} = \mathbf{PB_1}, \quad \widetilde{\mathbf{B_2}} = \mathbf{PB_2}, \quad \widetilde{\mathbf{C}} = \mathbf{PC} \end{aligned} \tag{4.30}$$

To reduce the steady state error in the tracking of the compensator current i_{fa}, feedback of the integral of tracking error of compensator current i_{fa} in phase a is taken. This feedback term is denoted as $q(t)$ and is given by

$$q(t) = \int_0^t \tilde{\mathbf{y}}(\tau) - i_{fa}^*(\tau) d\tau \tag{4.31}$$

The term $q(t)$ given by (4.31) is added as the fifth state-variable in the the state-space model given in (4.30). The augmented system thus becomes

$$\begin{aligned} \begin{bmatrix} \dot{\mathbf{z}}(t) \\ \dot{q}(t) \end{bmatrix} &= \begin{bmatrix} \tilde{\mathbf{A}} & 0 \\ \tilde{\mathbf{C}} & 0 \end{bmatrix} \begin{bmatrix} \mathbf{z}(t) \\ q(t) \end{bmatrix} + \begin{bmatrix} \widetilde{\mathbf{B_1}} \\ 0 \end{bmatrix} u V_{dc} + \begin{bmatrix} \widetilde{\mathbf{B_2}} \\ 0 \end{bmatrix} v_{sa} - \begin{bmatrix} 0 \\ 1 \end{bmatrix} i_{fa}^*(t) \\ \tilde{y} &= \begin{bmatrix} \tilde{\mathbf{C}} & 0 \end{bmatrix} \begin{bmatrix} \mathbf{z}(t) \\ q(t) \end{bmatrix} \end{aligned} \tag{4.32}$$

The above equation is solved using algebraic Ricatti equation to generate the gains

$[\mathbf{K} \;\; H]$ and hence the control law u_c is obtained as

$$u_c(t) = \mathbf{K}(z - z_{ref}) + H \int_0^t (\tilde{y}(\tau) - i^*_{fa}(\tau))d\tau \tag{4.33}$$

As the load parameter is continuously varying, and is dependent on the customers, it is not possible to obtain a reference for load current i_{la}. Hence, the gain corresponding to error in i_{la} is set as zero and $u_c(t)$ is modified as

$$u_c(t) = K_1(i_{fa} - i^*_{fa}) + K_2(i_{da} - i^*_{da}) + K_3(v_{ta} - v^*_{ta}) + H \int_0^t (\tilde{y}(\tau) - i^*_{fa}(\tau))d\tau \tag{4.34}$$

Where K_1, K_2, K_3 are elements of $\mathbf{K}$ which is obtained from the solution of algebraic Ricatti equation. From the control law. the modulation signal is obtained as $\frac{u_c(t)}{3V_{dc}}$, which is then utilized in the single carrier level-shifted sine PWM operation to generate the switching signals.

4.3.2 Finite Control Set- Model Predictive Control (FCS-MPC)

In predictive control, mathematical model of the system is formulated to predict the future values of the quantities, which are used in the chosen cost function to generate the control signals. As MPC operates on minimization of a cost function [94], the computational requirement is high for its implementation. To circumvent this problem, finite control set-model predictive control (FCS-MPC) is used which exploits the finite possible switching combinations present in a power electronic converter to reduce the computation complexity [95].

The schematic representation of applying FCS-MPC to DSTATCOM is shown in Fig. 4.5. Here the measured quantities, x_m, are utilized in a predictive model to predict the future values of the parameters, x_p. The predicted values along with the reference values are utilized to minimize the requisite cost function and switching state, u_{opt_x}, corresponding to the minimum cost function is obtained for phase x. As shown in the Table 2.1 in Chapter 2, the switching combinations corresponding to the switching state u_{opt_x} is applied to the inverter. To obtain the switching signals for RSDCHBMLI based DSTATCOM shown in Fig. 4.1, i_{fca}, i_{fcb} and i_{fcc} need to be controlled to their reference values i^*_{fca}, i^*_{fcb} and i^*_{fcc}, respectively. For this, the equivalent circuit of phase a shown in Fig 4.4 is used. For other phases, the predictive model remains same considering the

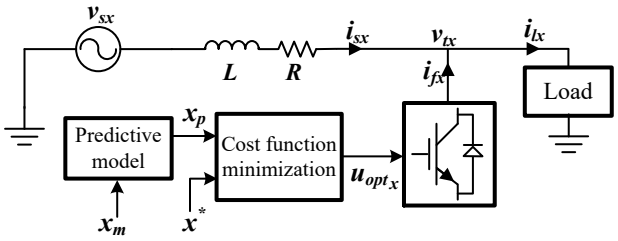


Fig. 4.5 Schematic representation of FCS-MPC control

same feeder impedance. Utilizing the equivalent circuit, voltage equation for the inner loop of Fig. 4.4 is obtained as:

$$-uV_{dc} + L_f \frac{di_{fca}}{dt} + R_f i_{fca} + v_{ta} = 0 \tag{4.35}$$

With the sampling time being T_s, (4.35) in discrete time domain is given by

$$-uV_{dc}(k) + L_f \frac{i_{fca}(k) - i_{fca}(k-1)}{T_s} + R_f i_{fca}(k) + v_{ta}(k) = 0 \tag{4.36}$$

with the approximation,

$$\frac{di_{fca}}{dt} \approx \frac{i_{fca}(k) - i_{fca}(k-1)}{T_s} \tag{4.37}$$

Thus, the value of i_{fca} at k^{th} time instant is

$$i_{fca}(k) = \frac{1}{1 + \frac{T_s R_f}{L_f}} i_{fca}(k-1) + \frac{1}{R_f + \frac{L_f}{T_s}} [uV_{dc}(k) - v_{ta}(k)] \tag{4.38}$$

To obtain the value of i_{fca} at $(k+1)^{th}$ instant, (4.38) is advanced by one sampling instant. Thus, the predicted value of i_{fca}, denoted by $\hat{i}_{fca}(k+1)$, is given by

$$\hat{i}_{fca}(k+1) = \frac{1}{1 + \frac{T_s R_f}{L_f}} i_{fca}(k) + \frac{1}{R_f + \frac{L_f}{T_s}} [uV_{dc}(k+1) - v_{ta}(k+1)] \tag{4.39}$$

Using (4.13) and (4.39), the cost function g_a for phase a is evaluated as

$$g_a = \mid i^*_{fca}(k+1) - \hat{i}_{fca}(k+1) \mid \tag{4.40}$$

The value of $i^*_{fca}(k+1)$ can be obtained using second order extrapolation given by

$$i^*_{fca}(k+1) = 3i^*_{fca}(k) - 3i^*_{fca}(k-1) + i^*_{fca}(k-2) \tag{4.41}$$

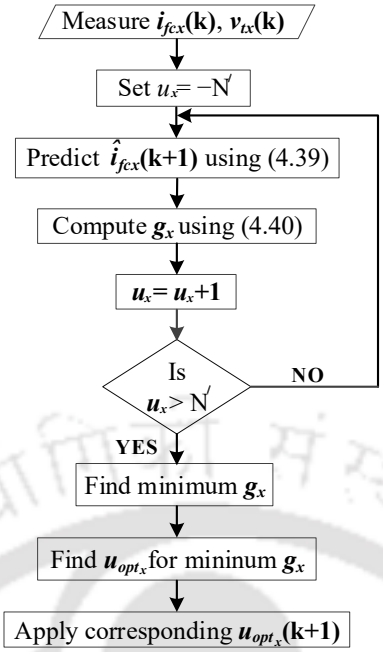


Fig. 4.6 Flowchart describing steps of FCS-MPC

If T_s is sufficiently small, then, $i^*_{fca}(k+1) \approx i^*_{fca}(k)$ [62]. The cost function g_x, $x \in (a,b,c)$ is calculated independently for three phases, for all feasible switching combinations , $-N' \leq u \leq N'$, where $N' = 3$ for a 7-level RSDCHBMLI. Then the switching state, u_{opt_x}, corresponding to the minimum g_x, is chosen and corresponding switching combinations from Table 2.1 are applied to the phase x of RSDDCHBMLI. The flowchart of FCS-MPC algorithm describing these steps is given in Fig. 4.6.

4.4 DC-bus voltage control

As DSTATCOM injects only reactive power into the system, the DC-link of the inverter is realized by a capacitor, C_{dc} as shown in Fig 4.1. The average value of voltage across the DC-link capacitor should be maintained at the desired value V^*_{dc}. The average voltage V_{dc} is regulated at V^*_{dc} by drawing real power from the distribution network, which is also responsible of supplying the losses. Thus the real power drawn for maintaining the DC-bus voltage should also be accounted for in the reference current generation scheme detailed in section 4.2.

Usually, a proportional-integral (PI) controller is used to maintain the voltage across C_{dc} at the value calculated by (4.2). In this section, two types of PI based DC-bus voltage controllers are described which can be used for maintaining voltage across

C_{dc} at V_{dc}^{*}. Conventionally, the DC-bus voltage controller calculates the power required to charge the capacitor to desired reference voltage. [43]- [21], [96]. The calculation of PI controller gains is not straightforward for such complex systems and have great impact on the compensation ability of DSTATCOM. To overcome this drawback, current based DC-bus voltage controller is described in this thesis where gains are related to system parameters and hence, easily computed. In the first subsection, the conventional power based controller is described, along with the challenges posed by it. In the next subsection, the current based controller and its advantages over the conventional controllers is detailed. A comparative study of conventional DC-bus voltage controllers and current based DC-bus controllers is presented in the later part of the chapter, in subsection 4.6.4.

4.4.1 Power based (p_{loss}) DC-bus voltage controller

The conventional power based controller is shown in Fig. 4.7. Here, the PI controller is used to compute the amount of real power, p_{loss}, that should be drawn from the distribution system to maintain the average DC-link voltage V_{dc} at desired reference value [26], [21]. The input to the PI controller is the deviation of V_{dc} from its reference value V_{dc}^{*}. Thus,

$$p_{loss} = K_{pc}(V_{dc}^{*} - V_{dc}) + K_{ic}\int (V_{dc}^{*} - V_{dc})dt \tag{4.42}$$

The reference source currents in (4.11) is modified as

$$\begin{bmatrix} i_{sa}^{*} \\ i_{sb}^{*} \\ i_{sc}^{*} \end{bmatrix} = \frac{1}{\sum_{x=a}^{c} v_{tx_1}^{+2}} \mathbf{I} \begin{bmatrix} v_{ta_1}^{+} \\ v_{tb_1}^{+} \\ v_{tc_1}^{+} \end{bmatrix} (p_{lavg} + p_{loss}) \tag{4.43}$$

As pointed out in [88], there is no systematic mathematical procedure to derive the gains of the PI controller, which complicates the choice of K_{pc} and K_{ic} for complex systems.

To overcome the problems posed in choosing the gain values for a conventional PI controllers, an energy based fast-acting PI controller (FAC) is described in [88]. In [88] p_{loss} is calculated based on the energy required by the capacitor to charge to V_{dc}^{*}.

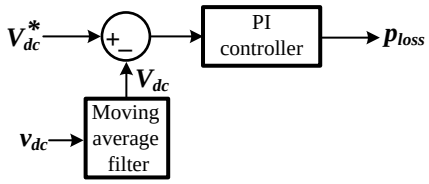


Fig. 4.7 Conventional power based DC-bus voltage controller

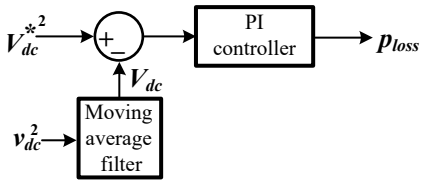


Fig. 4.8 Fast-acting DC-bus voltage controller

Considering T_c as the ripple period of the DC-link capacitor voltage, the power p_{loss} required by the capacitor to charge from its actual voltage V_{dc} to the reference voltage V_{dc}^* is given by

$$p_{loss} = \frac{1}{2T_c} C_{dc} (V_{dc}^{*\,2} - V_{dc}^{\,2}) \tag{4.44}$$

Also, considering p_{loss} as the output from the PI controller as shown in Fig. 4.8

$$p_{loss} = K_{pf} (V_{dc}^{*\,2} - V_{dc}^{\,2}) + K_{if} \int (V_{dc}^{*\,2} - V_{dc}^{\,2}) dt \tag{4.45}$$

From 4.44 and 4.45, proportional gain of the fast-acting controller given as:

$$K_{pf} = \frac{C_{dc}}{2T_c} \tag{4.46}$$

where T_c is the time period of ripple in capacitor voltage. The integral gain K_{if} is chosen to minimize the steady-state error with acceptable transient response and is given as , $K_{if} = 0.5 K_{pf}$ in [88]

4.4.2 Current based (i_{loss}) DC-bus voltage control

In this thesis, a current based DC bus voltage controller as shown in Fig. 4.9 is described. Here,relation between the current that is to be drawn by the DC-link capacitor to maintain V_{dc} at V_{dc}^*, and the deviation from the reference voltage is utilized to mathematically obtain the relationship between K_p, V_{dc}, V_{dc}^* and i_{loss}. The direct mathematical formula allows simple calculation of the value of K_p for any changes in the DC-link capacitance value. The value of the K_i is selected to minimize the steady state error along with obtaining an acceptable transient performance.

As shown in Fig. 4.9, the error between V_{dc}^* and V_{dc} is passed through a PI

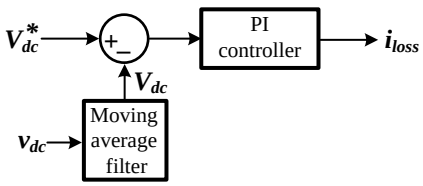


Fig. 4.9 Current based DC bus voltage controller

controller to generate the current i_{loss} which indicates the additional positive sequence current that should be drawn by the DSTATCOM from the grid to maintain the DC bus voltage. The current based PI controller is described by

$$i_{loss} = K_p(V_{dc}^{*} - V_{dc}) + K_i \int (V_{dc}^{*} - V_{dc})dt \tag{4.47}$$

Now the current drawn by the DSTATCOM, i_{loss} can be related to the voltage across as the DC link capacitor as

$$V_{dc}^{*} - V_{dc} = \frac{1}{C_{dc}} \int_{T_c} i_{loss} dt \tag{4.48}$$

From (4.47) and (4.48), K_p can be calculated as

$$K_p = \frac{C_{dc}}{T_c} \tag{4.49}$$

where T_c is the time period of the ripple in capacitor current, which is same as the time period of ripple in capacitor voltage used in (4.46). As the capacitor current and the capacitor voltage consists of a dominant double frequency harmonic, the value of T_c is related to the nominal grid frequency f_g as

$$T_c = \frac{1}{2f_g} \tag{4.50}$$

As the grid frequency in the system considered in this work, as per the values given in Table 4.3, is taken as 50 Hz, T_c is calculated to be 0.01 seconds. The ripple frequency remains unchanged as the capacitor is a linear element. Once K_p is calculated, $K_i = \frac{K_p}{2}$ is taken as the default value. Depending on the steady state error and transient response, fine tuning of K_i is done around the default value. Now, as i_{loss} is to be drawn equally from the three phases, for power invariant transformation, the additional amount of current that is to be drawn from the source for maintaining the DC-link voltage, i_{sx_d} is

given by

$$\begin{bmatrix} i_{sa_d} \\ i_{sb_d} \\ i_{sc_d} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha^2 & \alpha \\ 1 & \alpha & \alpha^2 \end{bmatrix} \begin{bmatrix} 0 \\ \frac{i_{loss}}{\sqrt{3}} \\ 0 \end{bmatrix} \tag{4.51}$$

The final reference source currents for each of the phases are calculated by adding (4.51) to the values calculated in (4.11).

4.5 Control block diagram

In this section, to summarize the DSTATCOM control structure, complete control block diagrams of DSTATCOM control using SFBI and FCS-MPC are presented in Fig. 4.10 and Fig. 4.11 respectively. It can be seen that, the control part of DSTATCOM operation is composed of three segments, *viz.*, the reference current generation, current control and DC-bus voltage control. The references for source currents, DSTATCOM currents and RSDCHBMLI output currents for each of the three phases are obtained using instantaneous symmetrical components theory, and the procedure is detailed in section 4.2. The reference source currents obtained utilizing the reference current generation technique is further augmented with the output obtained from the DC-bus voltage controller. The DC bus voltage controller determines the current that should be drawn by the DSTATCOM from the source to supply its losses and maintain the DC-link voltage at the desired value. In this thesis, a current based DC-bus controller is described in section 4.4 which is responsible of maintaining the average DC-link voltage at V_{dc}^*. The reference currents thus obtained are utilized in the current controller to generate the switching signals for the RSDCHBMLI switches. In this work, two current control techniques, *viz.,* SFBI and FCS-MPC are used for generating the switching signals, and are described in section 4.3. The complete control block diagram of DSTATCOM, indicating the reference current generation, predictive control and DC-bus control blocks is shown in Fig. 4.11. After obtaining u_{opt_x}, the corresponding switching combinations are selected using Table 2.1.

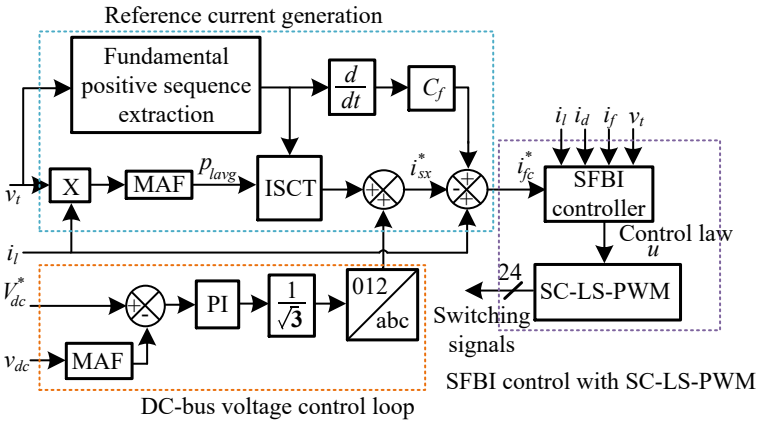


Fig. 4.10 Block diagram of DSTATCOM control with SFBI control

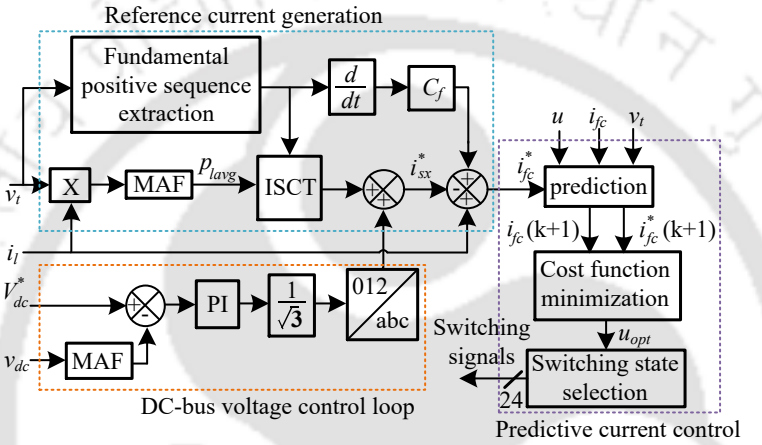


Fig. 4.11 Block diagram of DSTATCOM control with FCS-MPC

4.6 Results and discussion

To verify the DSTATCOM operation, detailed simulations are carried out in PSCAD.

4.6.1 DSTATCOM operation with balanced source

The simulation is carried out for a 11 kV distribution system with balanced sources. The simulation parameters are given in Table 4.3. The simulations are carried out for three cases: Case A, when the distribution system is supplying a linear and unbalanced load; Case B, where a balanced non-linear rectifier load is added with the unbalanced linear load and Case C where the load is purely non-linear.

Table 4.3 SIMULATION PARAMETERS FOR RSDCHBMLI BASED DSTATCOM

Parameters		Values
Source voltage		11 kV, line-to-line RMS 50 Hz
Short circuit capacity		36.76 MVA
Rated power		5 MVA
Feeder impedance		$(1 + j3.14)$ Ω
$\frac{X_{grid}}{R_{grid}}$		3.14
Transformer parameters		1 : 1, 3.25 MVA
		1 : 2, 6.5 MVA
DC-link voltage		6500 V
DC-link capacitance		4400 μF
Load scenario		
Case A	Linear	30 Ω, 0.1 H , 561.38 kW, 587.76 kVAr
		20 Ω, 0.05 H , 1013.26 kW, 795.21 kVAr
		20 Ω, 0.02 H , 1522.33 kW, 478.34 kVAr
	Non-linear	NIL
Case B	Linear	Same as in Case A
	Non-linear	3-phase rectifier with 50 μF, 500 Ω
Case C	Linear	NIL
	Non-Linear	3-phase rectifier with 20 μF, 100 Ω

A. DSTATCOM operation with SFBI control

For implementation of DSTATCOM with SFBI control, the filter parameters are taken as $C_f = 20$ μF and $L_f = 1$ mH. The switching frequency for single carrier multilevel sine PWM operation is 10 kHz. The DSTATCOM performance for different cases are given in the subsequent paragraphs.

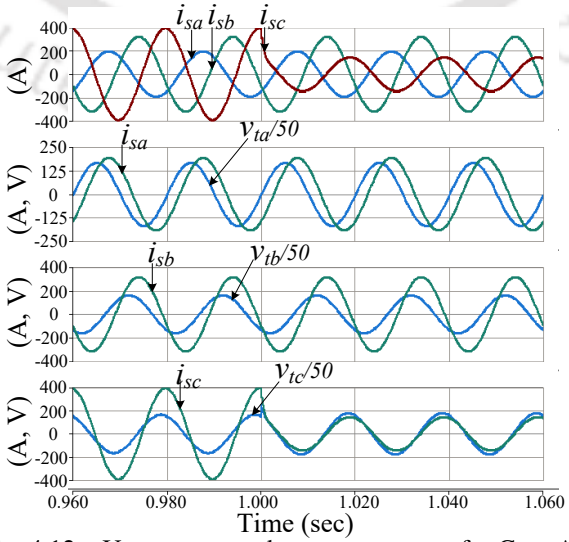


Fig. 4.12 Uncompensated system response for Case A

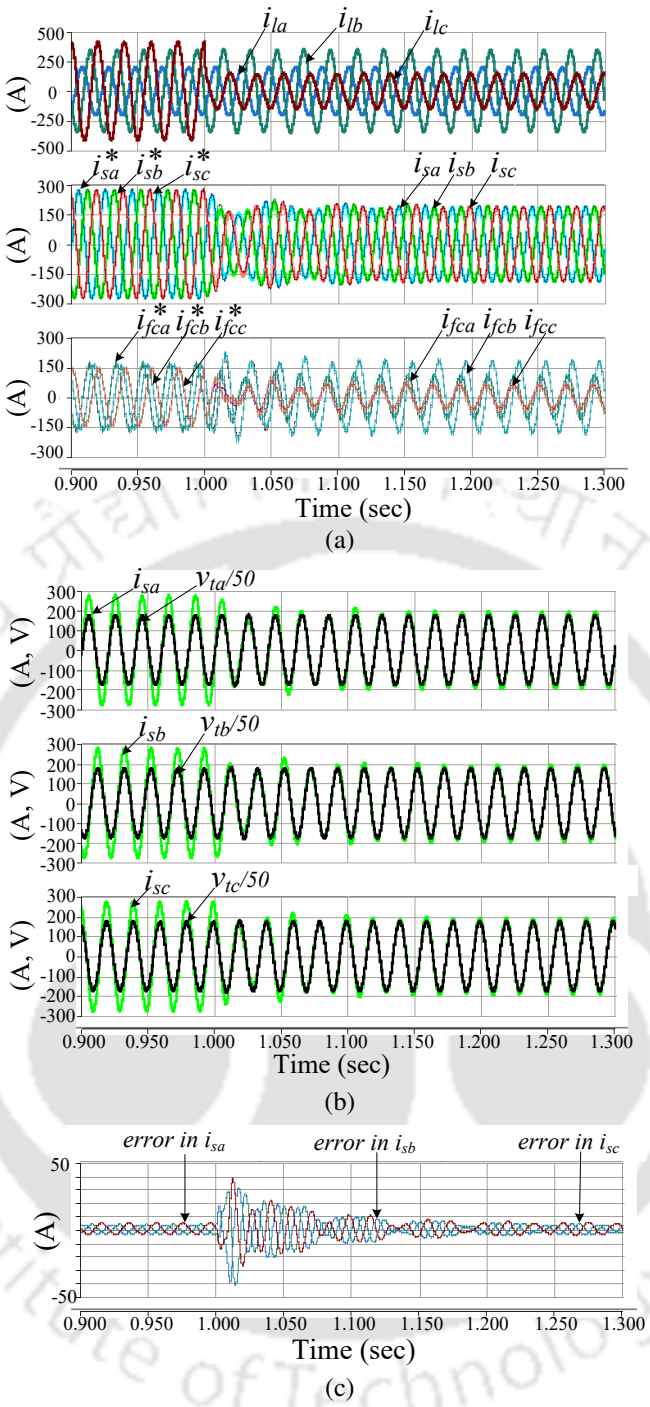


Fig. 4.13 Load compensation using RSDCHBMLI based DSTATCOM with SFBI for Case A: (b) source currents and terminal voltages for phases *a*(top), *b*(middle) and *c*(bottom) (c) Tracking error in source currents

Case A For unbalanced and linear load of Case A, listed in Table 4.3, the uncompensated system is shown in Fig. 4.12. The source currents are unbalanced and not in phase with the terminal voltages due to presence of inductive component in the load. The DSTATCOM should be able to compensate the unbalance in the source currents along with improving the power factor to unity in each phase. The compensated system response for Case A is shown in Fig. 4.13. The load in phase *c* is given a 3 times step in-

crease at 1 second. It is seen that the DSTATCOM is able to perform load compensation in presence of step change in load. The system takes around 9 cycles to settle after the step change in load. The maximum tracking error is 1.5% in steady state. To investigate

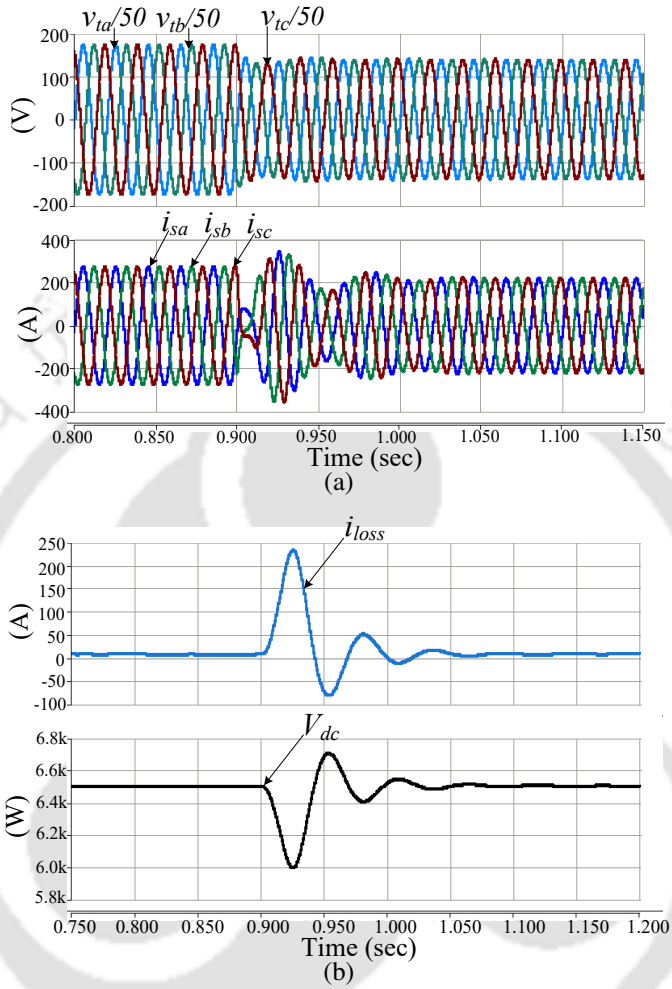


Fig. 4.14 System response for Case A under voltage sag:(a) terminal voltages (top), source currents(bottom) (b) i_{loss} (top), V_{dc} (bottom)

the performance of DC-bus voltage controller, a 20% voltage sag is introduced in the source voltages at 0.3 seconds. The terminal voltages and the source currents are shown in Fig 4.14(a). It is observed that the source currents are balanced both before and during the voltage sag. The DC-link parameters, i_{loss} and V_{dc} are shown in Fig 4.14(b). The DC-link controller is able to main the DC-link voltage at the desired reference even in presence of voltage sag.

Case B Here, a balanced non-linear load is added to the system and the uncompensated system response is shown in Fig 4.15. The FFT of source currents are shown in Fig 4.16. The source currents are unbalanced, and the effect of harmonic current drawn

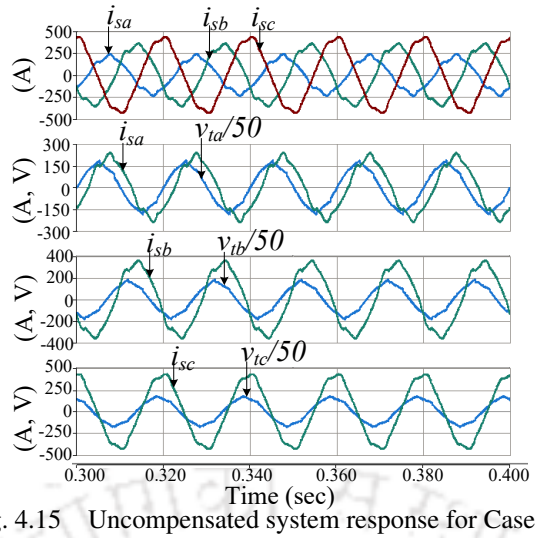


Fig. 4.15 Uncompensated system response for Case B

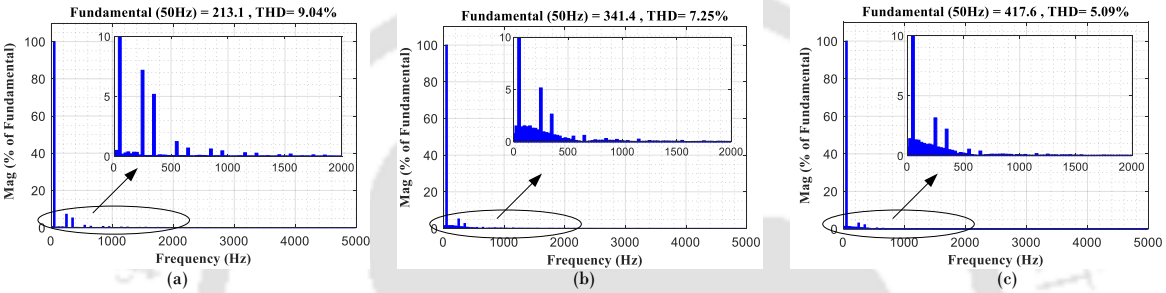


Fig. 4.16 Frequency spectrum of source currents without DSTATCOM for Case B: (a) i_{sa} (b) i_{sb} (c) i_{sc}

by the rectifier load is manifested as distortion in the source currents and the terminal voltages. The THD of the terminal voltages in phases a, b and c are 4.65%, 5.82% and 4.93% respectively. The plot of i_{sa} and v_{ta} show that the source current is lagging the terminal voltage. The power factor in phases a, b and c are 0.69, 0.78 and 0.95 respectively. The frequency spectrum of the source currents in the uncompensated system is shown in Fig 4.16. The fundamental component in each of the three phases are different and THD in phases a, b and c are 9.04%, 7.25% and 5.09%. The total current unbalance in presence of harmonic distortion (ITUD) is calculated using [97]

$$ITUD = \sqrt{\frac{I_1^{-2} + \sum_{h\neq 1}(I_h^{-2} + I_h^{0^2})}{I_1^{+2} + \sum_{h\neq 1}(I_h^{+})}} \tag{4.52}$$

where I_h^+, I_h^- and I_h^0 indicate the RMS value of positive, negative and zero sequence components of the h^{th} harmonic component of the source currents. The source currents in the unbalanced system exhibit an ITUD of 25.16%. The compensated system response is shown in Fig. 4.17. The source currents become balanced, and sinusoidal, as shown in Fig 4.17(a). The presence of C_f also results in maintaining sinusoidal terminal voltages. The THD of source currents and terminal voltages in each of the three phase

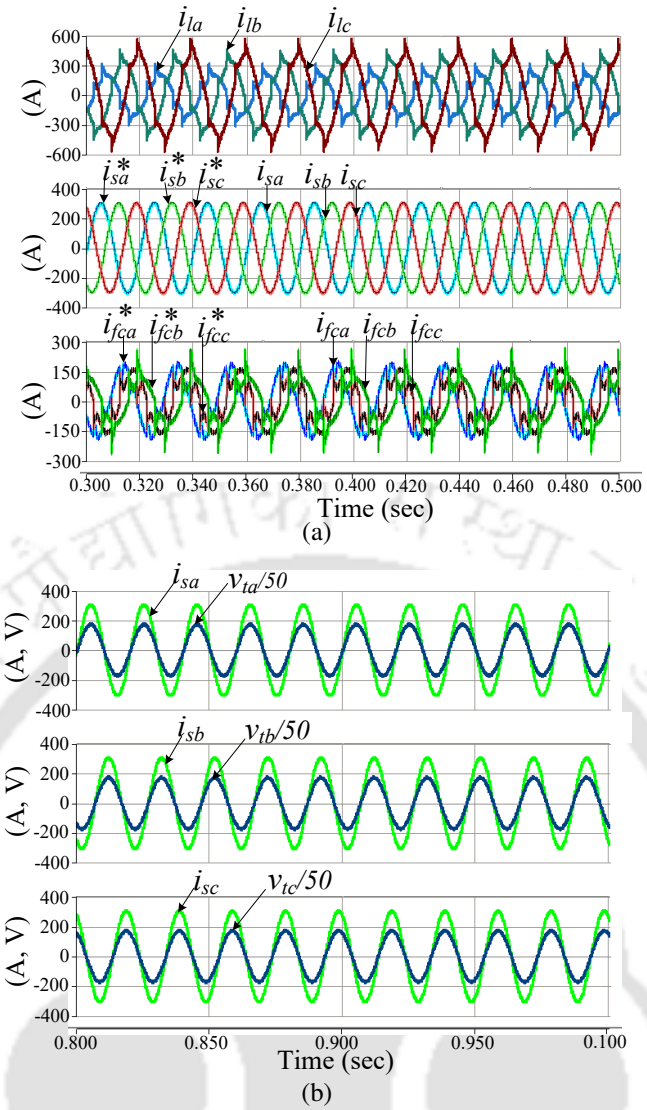


Fig. 4.17 Load compensation using RSDCHBMLI based DSTATCOM with SFBI for Case B (a) load currents (top), reference and measured source currents (middle), DSTATCOM currents (bottom) (b) source currents and terminal voltages for phases *a*(top), *b*(middle) and *c*(bottom)

falls below 0.1%. The power factor in each of the three phases become unity as seen from Fig 4.17(b).

Case C For the third case, the distribution system is supplying a purely non-linear load. The uncompensated source currents and terminal voltages are shown in Fig. 4.18. The THD of terminal voltages are 15.52% and that of source currents is 49.32%. The compensated system response is shown in Fig 4.19. In the compensated system, shown in Fig 4.19(a), the source currents are balanced, and the harmonic demand of the load is being supplied by the DSTATCOM. The THD of terminal voltages in the compensated system falls to 0.07% while the THD of the compensated source currents fall to 0.1%. The improvement in power factor is evident from Fig 4.19(b) where the source currents

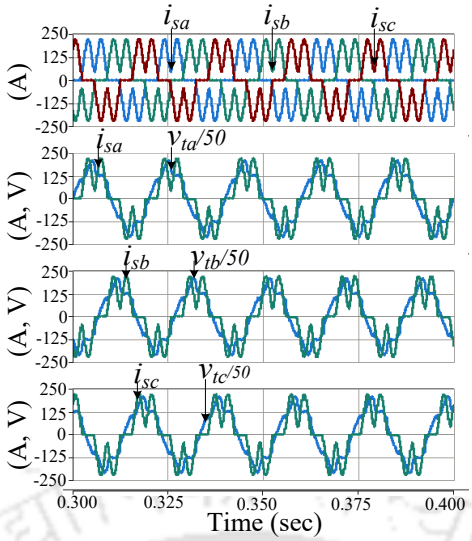
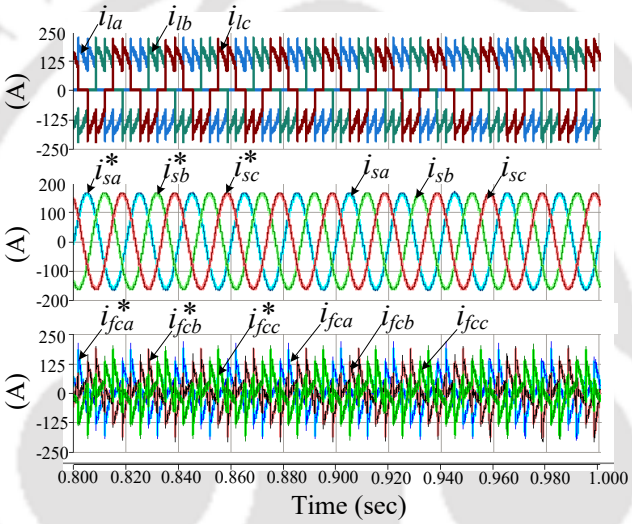
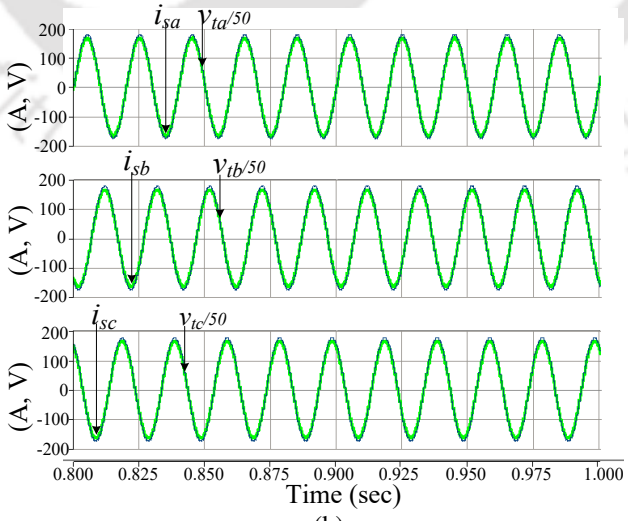


Fig. 4.18 Uncompensated system response for Case C



(a)



(b)

Fig. 4.19 Load compensation using RSDCHBMLI based DSTATCOM with SFBI for Case C (a) load currents (top), reference and measured source currents (middle), DSTATCOM currents (bottom) (b) source currents and terminal voltages for phases *a*(top), *b*(middle) and *c*(bottom)

and terminal voltages are in phase.

Thus from the results presented above, it is clear that the RSDCHBMLI based DSTATCOM is successful in performing load compensation in presence of both non-linear and linear load. It is capable of supplying the reactive and harmonic part of the load current and thus makes the current drawn from the source sinusoidal, and improves the source current power factor to unity. The DSTATCOM operation is verified in case of load changes and voltage sags. The results exhibit that the DC bus voltage controller is successful in maintain the DC-link voltage at the desired reference and the DSTATCOM is successful in load compensation and power factor improvement in presence of changes in source voltage magnitudes and loads.

B. DSTATCOM operation with FCS-MPC control

For implementation of FCS-MPC control, the sampling time is taken is 1 μS. The filter parameters are chosen as $L_f = 3.5$ mH, $C_f = 20$ μF. The other parameters are same as those mentioned in Table 4.3.

Case A For load scenario described in Case A, the response of the compensated system with RSDCHBMLI based DSTATCOM, controlled using FCS-MPC is given in Fig. 4.20. Comparing the response of the compensated system with that of the uncompensated system shown in Fig. 4.12, it is noted that using FCS-MPC control, the DSTATCOM is successful in compensating the unbalance of the source currents, and measured source currents track the reference source currents in Fig 4.20a. Also, the lagging power factor exhibited by the source currents in Fig. 4.12 due to presence of reactive loads, is improved to unity in the compensated system. Also, the load parameter in phase c is subjected a to step increase to check the DSTATCOM performance and current control under dynamic load conditions. This is manifested in the reduction of the magnitude of source currents after step change. The source currents continue to remain balanced and sinusoidal despite load changes.

Further, as in the previous case, to verify the operation of the DC-bus voltage controller when FCS-MPC is used for current control, a 20% voltage sag is introduced in the source voltages. It can be seen that the DC-bus voltage controller is able to bring back the DC-link voltage to the desired reference value in presence of voltage sag.

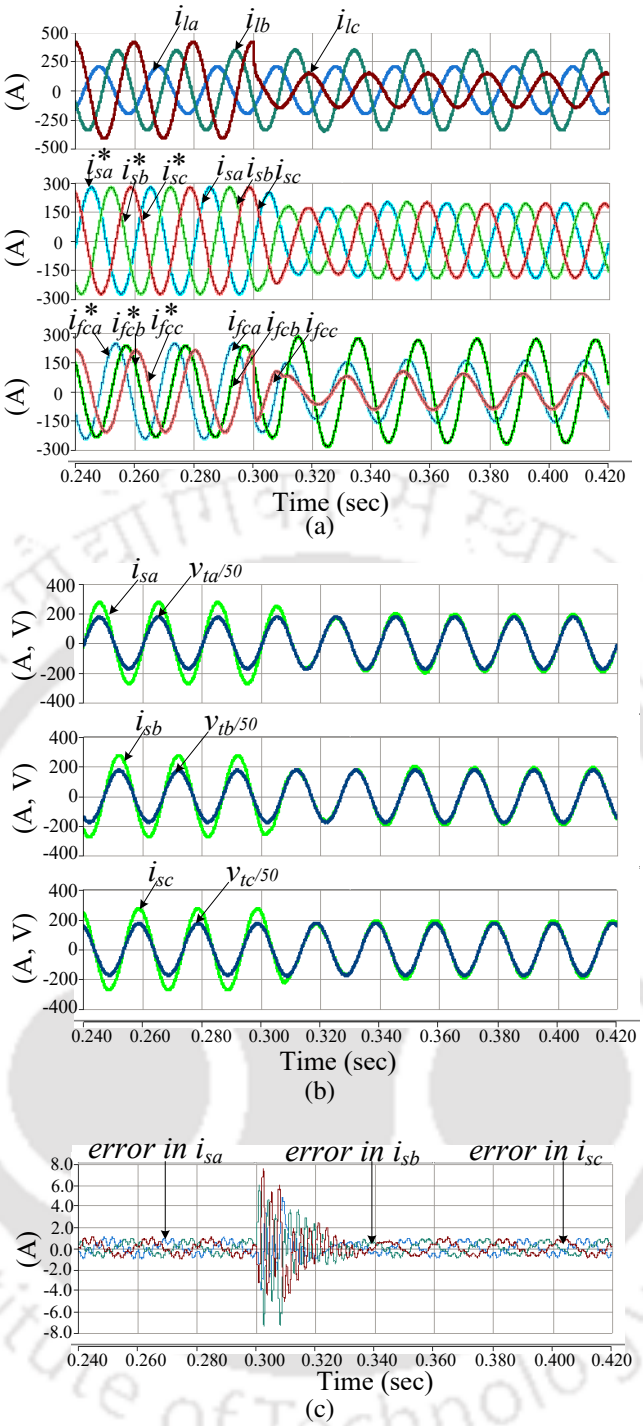


Fig. 4.20 Load compensation using RSDCHBMLI based DSTATCOM with FCS-MPC for Case A (a) load currents (top), reference and measured source currents (middle), DSTATCOM currents (bottom) (b) source currents and terminal voltages for phases *a*(top), *b*(middle) and *c*(bottom) (c) Tracking error in source currents

Case B In Fig. 4.21, the compensation by DSTATCOM in presence of non-linear loads, with FCS-MPC control is shown. The measured source currents and DSTATCOM currents, along with their reference quantities are shown in Fig. 4.21(a). The ITUD in the compensated system reduces to 0.04% and THD in each phase falls below 1%. The plot of three-phase terminal voltages and source currents in Fig 4.21(b) shows that unity power factor operation is achieved along with maintaining a sinusoidal PCC

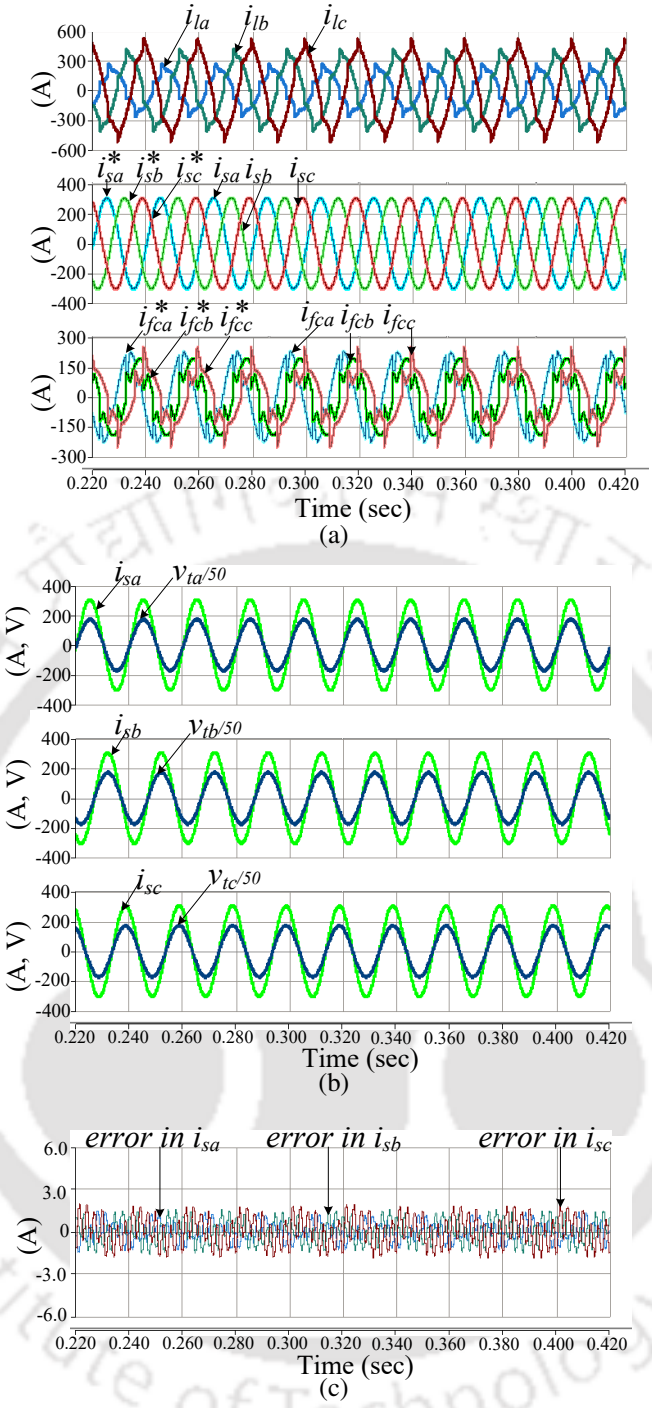


Fig. 4.21 Load compensation using RSDCHBMLI based DSTATCOM with FCS-MPC for Case B (a) load currents (top), reference and measured source currents (middle), DSTATCOM currents (bottom) (b) source currents and terminal voltages for phases *a*(top), *b*(middle) and *c*(bottom) (c) Tracking error in source currents

voltage. It can be seen from Fig 4.21(c) that with predictive current control, the maximum steady state tracking error in the source currents under the specified conditions is 2 A for peak value of 304.8 A, i.e, 0.66%.

Case C In Case C, when the distribution system supplies a balanced and non-linear load, the compensated system response, with FCS-MPC control is shown in Fig. 4.22.

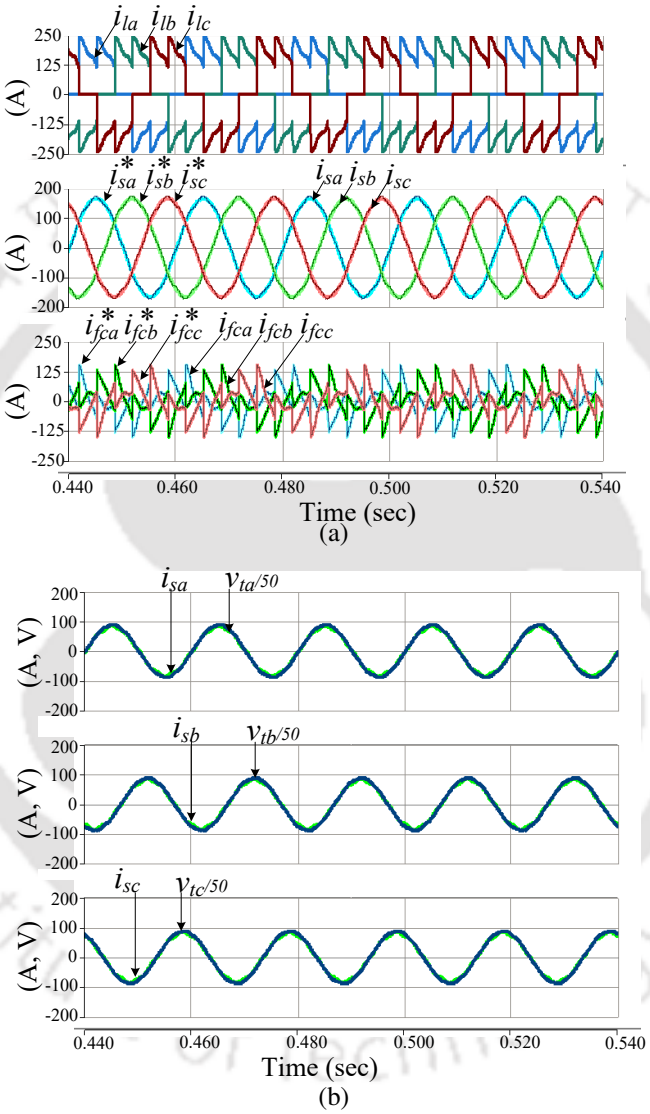


Fig. 4.22 Load compensation using RSDCHBMLI based DSTATCOM with FCS-MPC for Case C (a) load currents (top), reference and measured source currents (middle), DSTATCOM currents (bottom) (b) source currents and terminal voltages for phases *a*(top), *b*(middle) and *c*(bottom)

The THD in the compensated system falls The THD in source currents reduce to 2.7% from 49.32% in each phase. As the rectifier is supplying a resistive load, the power factor of the uncompensated source currents was 0.89 which is further improved to unity in the compensated system. Thus the load compensation performance of the RS-DCHBMLI based DSTATCOM for the three cases given in this section is summarized in Table 4.4. The load compensation performance for both the control techniques is given in Table 4.4.

Table 4.4 LOAD COMPENSATION PERFORMANCE OF RSDCHBMLI BASED DSTATCOM UNDER BALANCED SOURCE VOLTAGES

Load	**Current**	**Power factor**			**THD (%)**		
		without DSTAT-COM	DSTATCOM (SFBI)	DSTATCOM (FCS-MPC)	without DSTAT-COM	DSTATCOM (SFBI)	DSTATCOM (FCS-MPC)
Case A	i_{sa}	0.69	unity	unity	negligible	0.06	0.23
	i_{sb}	0.78				0.05	0.29
	i_{sc}	0.95				0.04	0.22
Case B	i_{sa}	0.68	unity	unity	9.04	0.08	0.22
	i_{sb}	0.77			7.25	0.07	0.32
	i_{sc}	0.84			5.09	0.05	0.37
Case C	i_{sa}	0.89	unity	unity	49.32	0.10	2.78
	i_{sb}					0.10	2.78
	i_{sc}					0.07	2.71

4.6.2 Comparison of DSTATCOM operation with SFBI and FCS-MPC control

In Subsection 4.6.1, using the same parameters, the RSDCHBMLI based DSTAT-COM is operated using two current control techniques- SFBI control and FCS-MPC. The performance of the two control techniques is compared in Table 4.5.

It is observed that the while MPC requires higher computation per phase as compared to the SFBI, it also provides a better dynamic response. The settling time of MPC controlled system under dynamic conditions of load change is 2 cycles, which is a 4 times improvement over the SFBI controlled system. But SFBI controlled system is successful is a better reduction of THD where the compensated current is almost a pure sine wave with a THD value as low as 0.1%. The steady state error is case of SFBI controlled system is limited to 1.6% while that in the MPC controlled system is 0.66%.

Table 4.5 COMPARISON OF PERFORMANCE OF RSDCHBMLI BASED DSTATCOM WITH SFBI AND FCS-MPC CURRENT CONTROL

	SFBI	**MPC**
Computation per phase	13	21
Modulator	Required	Not required
Offline calculation	Solution of LQR with choice of Q and r	Co-efficients of model prediction equation
Switching frequency	Constant	Variable
Filter Inductor	1mH	3mH
Settling time (Case A)	8.75 cycles	2 cycles
Steady state error (Case B)	1.60%	0.66%
Source current THD (Case C)	0.10%	2.70%

Also, as MPC results in a variable frequency operation, the line inductor values in case of MPC are required to be higher than that in case of SFBI. Thus, the choice of the control technique for RSDCHBMLI based system depends on the aim of compensation. If the goal is a faster compensation, without any constraint in the calculation capability and filter size, then MPC is a better option. In other cases, due to lower computational cost and filter size, SFBI poses as a better option, albeit compromising the dynamic response of the DSTATCOM.

4.6.3 DSTATCOM operation with unbalanced source

For verification of DSTATCOM operation in presence of unbalance in the source voltages, the control technique chosen is FCS-MPC as it eliminates the need of an additional modulator. Also, FCS-MPC results in a better dynamic response as compared to the SFBI control, which is shown in the previous section.

In this section, the different loading cases are shown in Table 4.6. In continuation to the previous subsection 4.6.1, the cases here are denoted as D, E, F and G

Table 4.6 DIFFERENT SOURCE VOLTAGE AND LOADING CONDITIONS FOR PERFORMANCE COMPARISON

Source voltages		**Cases**	**Load condition**
Magnitude	**Phase**		
Unbalanced	**Unbalanced**	**Case D**	Linear: Unbalanced Nonlinear: 3-ϕ rectifier
	Balanced	**Case E**	Linear: Unbalanced Nonlinear: 3-ϕ rectifier
		Case F	Linear: NIL Nonlinear: 3-ϕ rectifier
		Case G	Linear: Unbalanced Nonlinear: NIL

respectively.

Case D The source has got a -10% magnitude unbalance, and $+9\%$ phase unbalance in phase b and $+10\%$ magnitude unbalance, and -4% phase unbalance in c with respect to phase a. The linear load is given as $z_a = (25 + j31.4)\ \Omega$, $z_b = (20 + j15.71)\ \Omega$ and $z_c = (5 + j31.42)\ \Omega$. The non-linear load is a diode bridge rectifier supplying a parallel combination of 50 μF capacitor and 500 Ω resistor. The load in phase c experiences a step change at 0.25 seconds. For load compensation under unbalance in

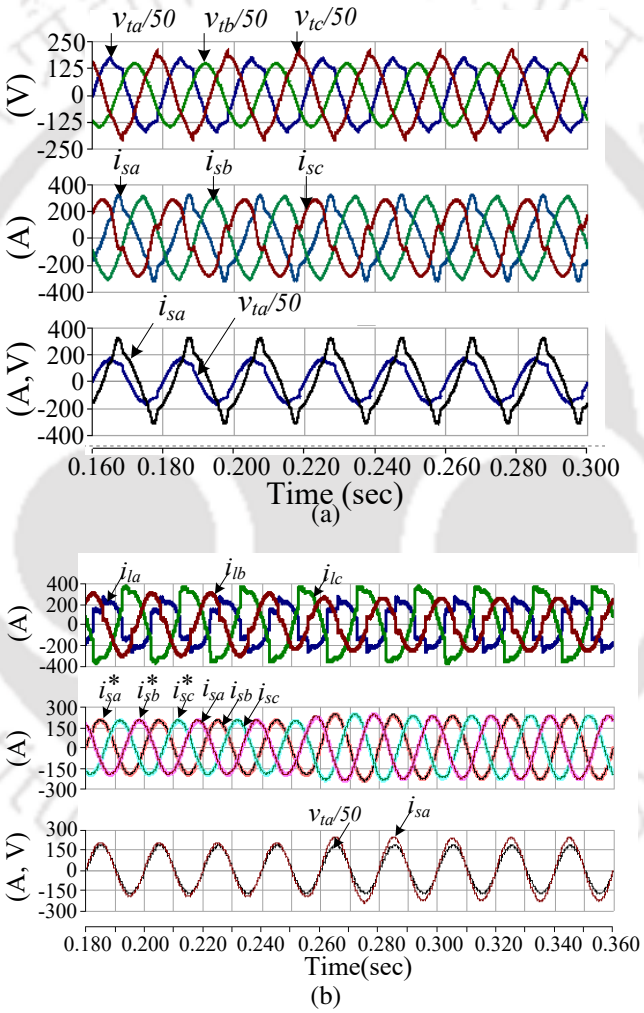


Fig. 4.23 System response for Case D: (a) Uncompensated source currents and voltages (b) Load currents and compensated source currents

source, the filter parameters are chosen as $R_f = 1.0\ \Omega$, $L_f = 3.5$ mH and $C_f = 44\ \mu$F. The performance of the uncompensated system is shown in Fig. 4.23(a). The source currents, along with the terminal voltages are unbalanced and distorted due to unbalance present in the source voltages as well as the load. The THD in phases a, b and c are 16%, 2.7% and 16% respectively. The compensated system response is shown in Fig. 4.23(b)

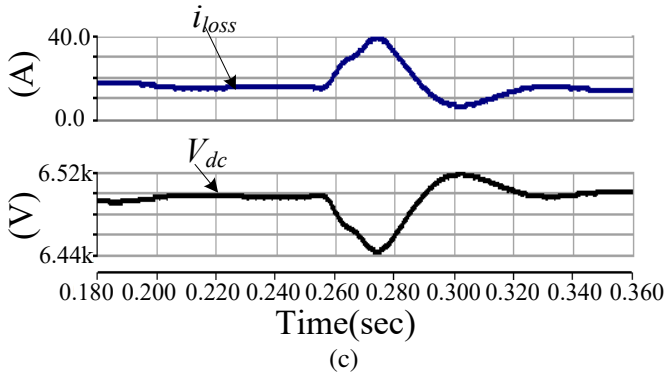


Fig. 4.23 System response for Case D:(c) Controller performance

where it is seen that the source currents are now balanced and sinusoidal, and tracks the reference values. At 0.25 seconds, the resistive load connected to phase *c* is changed from 5 Ω to 20 Ω. The source currents continue to be equal despite the load change. The THD in each of the phases fall to 2%. The source current in phase *a* is in phase with the terminal voltage as dictated by the reference current generation algorithm. The presence of phase unbalance in the source voltages hinder the unity power factor operation in the other phases. The controller performance is shown in Fig. 4.23(c). The DC-link voltage is maintained at 6514 V with a steady state error of 0.2%.

Case E Here the sources exhibit only magnitude unbalance as given in Case D. There is no phase unbalance and the system is supplying an unbalanced linear load with a three-phase non-linear load. The THD of the currents in the uncompensated system is 16%, 7% and 16% respectively. The compensated system response is shown in Fig. 4.24(a). The THD of phase *a* is 2.57%, *b* is 2.17% and *c* is 2.34%.

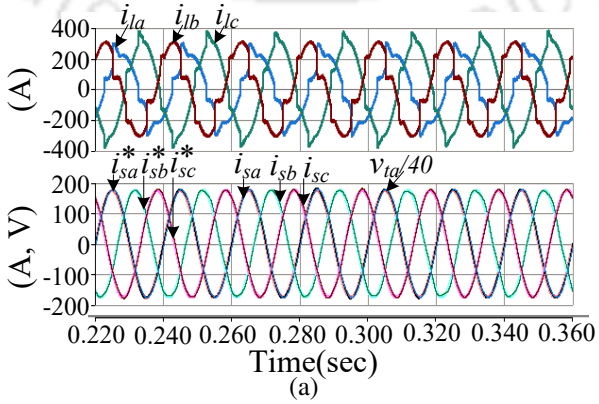
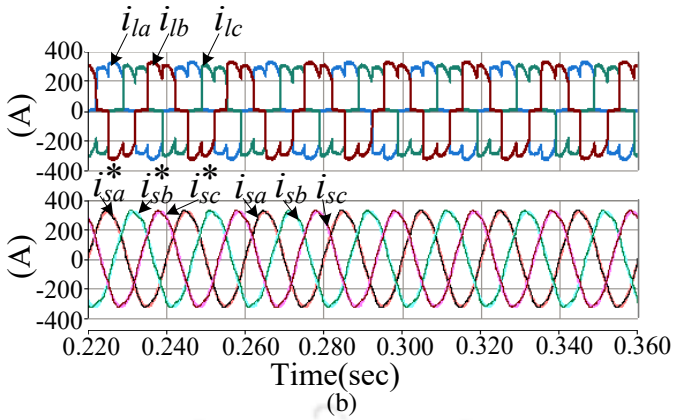
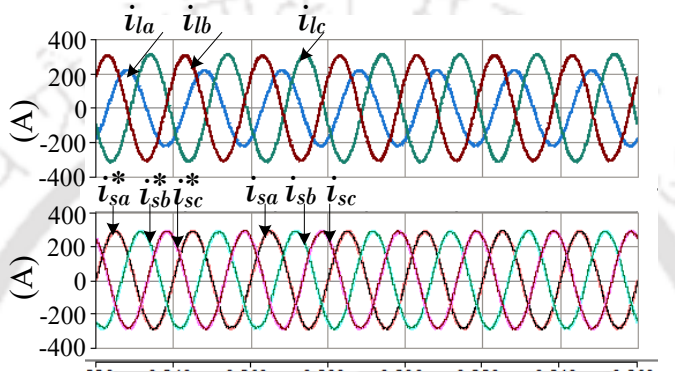


Fig. 4.24 Compensated system with unbalanced source: (a) Case E



(b)



(c)

Fig. 4.24 Compensated system with unbalanced source: (b) Case F (c) Case G

Case F The source with magnitude unbalance supplies an unbalanced purely non-linear rectifier load as given in Case B. The load currents and compensated source currents are shown in Fig. 4.24(b). The THD of uncompensated source currents are 27.31%, 33.03% and 29.06%, respectively. The THD of compensated source currents in each phase falls to 4.59%, 6% and 5.0%. The comparatively higher value of THD in phase *b* can be attributed to the higher magnitude of unbalance in the source voltage of phase *b*.

Case G Here the unbalanced source is supplying a purely linear, unbalanced load, as in Case C. The load currents and the balanced source currents of the compensated system are shown in Fig. 4.24(c). In all the above cases, except in cases B and F, the THD falls below 5%. In case of Case C, the THD of phase *b* is higher due to lower value of source voltage. This indicates that in cases with unbalanced load, the magnitude of unbalance in the source voltage impacts the compensation ability of the DSTATCOM, in equal current mode.

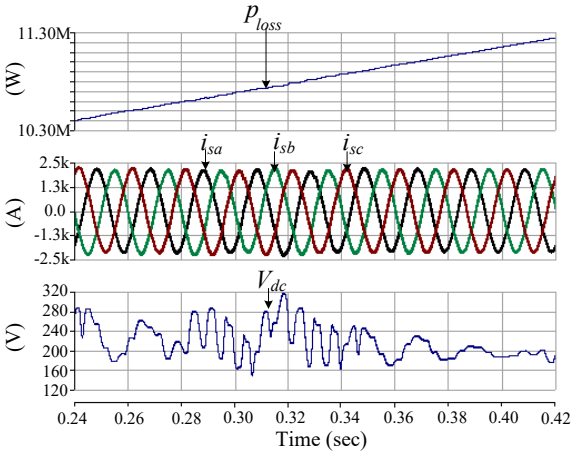


Fig. 4.25 Fast-acting PI controller with $K_p = 0.22$, $K_i = 0.11$

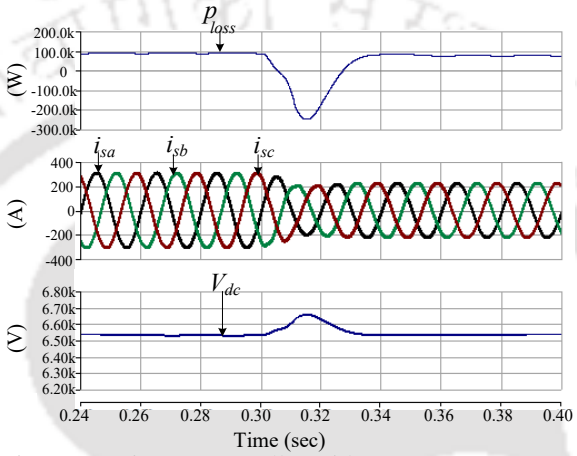


Fig. 4.26 Fast-acting PI controller with $K_p = 0.20$, $K_i = 0.10$

4.6.4 Comparison of DC bus controllers

In order to compare the performances of the different types of DC-bus voltage controllers, the compensated source currents and the DC-link voltage under transient conditions of load change is observed for different controllers- fast acting p_{loss} based controller proposed in [88], conventional p_{loss} based controller [21], and i_{loss} based controller described in Section 4.4.2. For this comparison, DSTATCOM controlled with FCS-MPC is taken into consideration. The gains for a fast acting controller come out to be $K_{pf} = 0.22$ F/s, $K_{if} = 0.11$ F/s^2. But it is found out that these gain values are not suitable for the MPC controlled system and causes instability in the DC-bus voltage control loop, as indicated in Fig. 4.25. Thus the gains are tuned to $K_{pf} = 0.20$ F/s, $K_{if} = 0.10$ F/s^2 . The controller response with the tuned gains are shown in Fig 4.26. For conventional p_{loss} based controller, the proportional and integral gains are chosen as $K_{pc} = 650$ A, $K_{ic} = 250$ A/s. The PI controller gain values for the i_{loss} based controller is calculated using (4.49) and K_i is tuned at 0.17 F/s^2. The performance of DC bus voltage controllers is tested with step change in load parameters as shown in Fig. 4.27. The

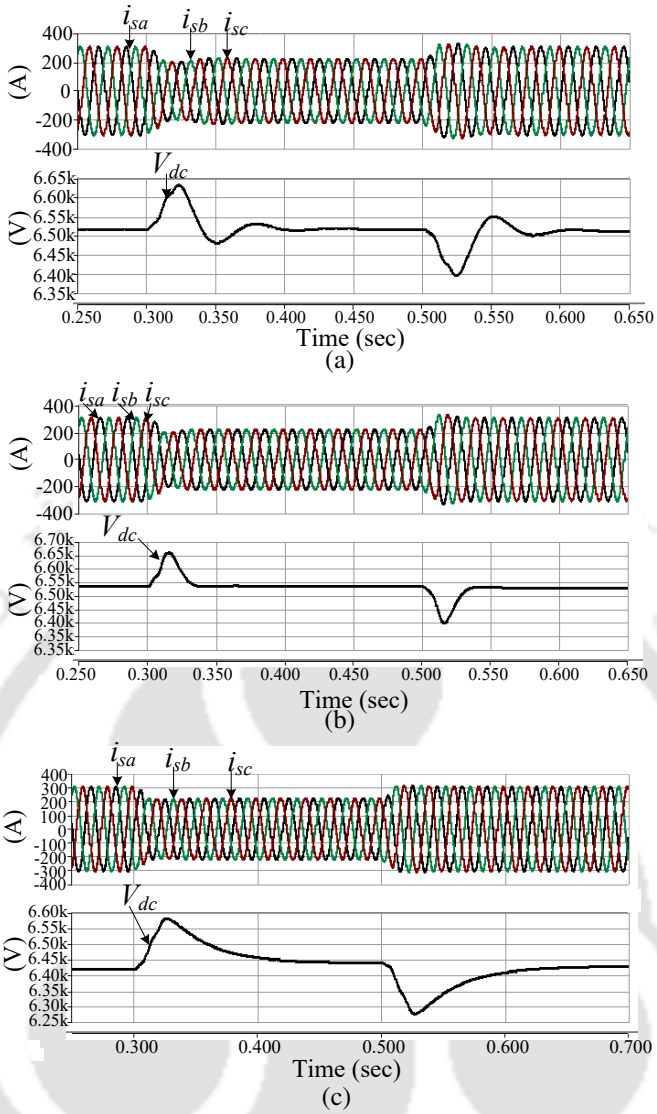


Fig. 4.27 Source currents (top) and V_{dc} for: (a) i_{loss} based controller (b) fast acting p_{loss} based controller (c) conventional p_{loss} based controller)

source currents and DC-link voltage for i_{loss} based controller is shown in Fig. 4.27(a). The DC-link voltage settles close to the desired value, after step change in load. The performance of p_{loss} based DC-bus voltage controllers is tested with step changes in load as shown in Fig 4.27(b) - Fig 4.27(c). The comparison of the DC-link controllers in terms of settling time t_{set}, steady state error, e_{ss}, overshoot and undershoot is presented in Table 4.7. It is seen that the t_{set} in case of i_{loss} based controller is higher than the fast acting controller. The steady state error in i_{loss} based controller comes out to be less than 5 V while the steady state error in the fast acting controller is about 65 V and that in the conventional controller is much higher. While the undershoot is below 1% in i_{loss} based controller and the fast-acting controller, the i_{loss} based controller also exhibits minimum overshoot under the test conditions.

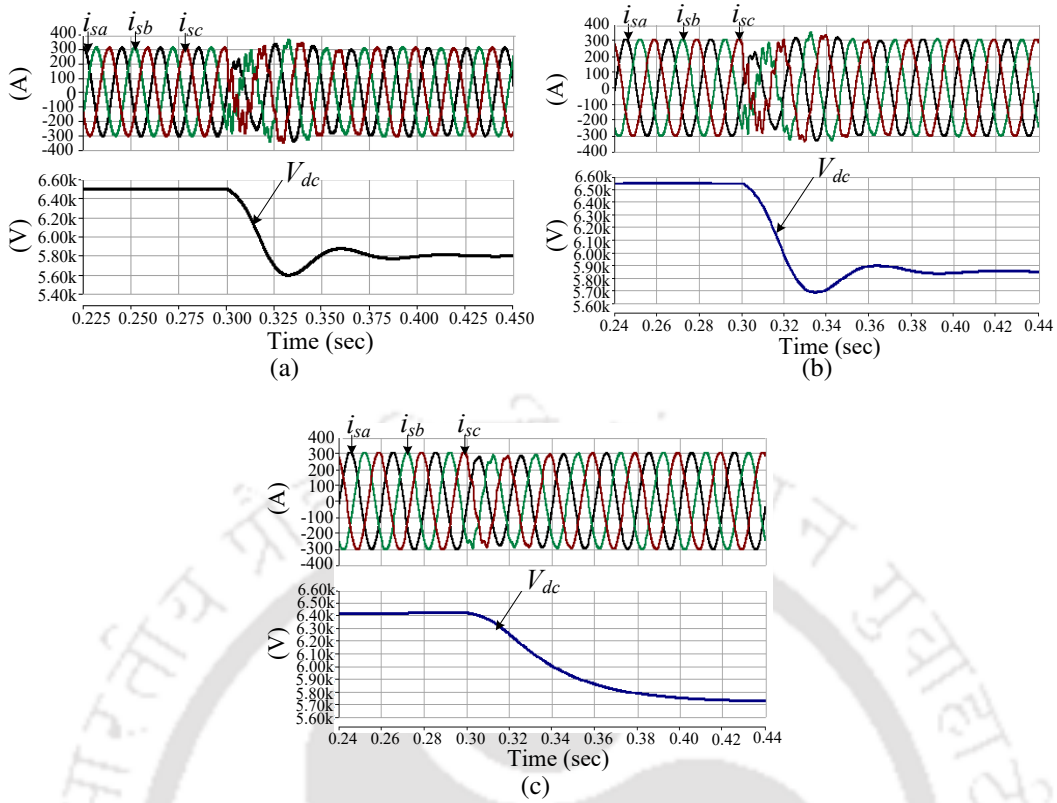


Fig. 4.28 Source currents (top) and V_{dc} for step change in V_{dc}^{*}: (a) i_{loss} based controller (b) fast acting p_{loss} based controller (c) conventional p_{loss} based controller

The performance of the DC-bus voltage controllers are further examined with step change in the reference value. At 3.0 seconds, the reference value of changed from 6.5 kV to 5.8 kV. The source currents and terminal voltages for different DC-bus controllers are shown in Fig 4.28. From Fig. 4.28(a), it can be seen that under such changes in the DC-link reference voltage, i_{loss} based controller can reach the new reference and maintains the value with a small steady state error of approximately 2 V. For p_{loss} based controllers, the steady state error exists as the DC-link tries to attain the reference value and the time taken to reach the new reference is higher in case of conventional controllers. The source currents in each of the three cases are balanced and sinusoidal which indicates successful load compensation by DSTATCOM. Among the controllers under consideration, the fast acting controller needs to handle large numerical values as it uses the square of the reference voltage which may create difficulty in the implementation of the controller for high values of reference voltage. The performance of the conventional controller shows that the steady state error and the settling time comes out to be higher than the other two controllers, along with the requirement of high gain values. From Table 4.7 and Fig 4.28, it can be seen that the overall performance of i_{loss}

based controller is better than that of p_{loss} based controller for the RSDCHBMLI based DSTATCOM controlled using FCS-MPC.

Table 4.7 COMPARISON OF DC BUS VOLTAGE CONTROLLERS

Parameters	i_{loss} **based controller**	p_{loss} **based controller**	
		Fast Acting controller (FAC)	**Conventional controller**
K_p	0.44 F/s	0.20 F/s	650 A
K_i	0.17 F/s^2	0.10 F/s^2	250 A/s
e_{ss}	< 4 V	≈ 36 V	≈ 80 V
t_{set}	0.12 sec	0.05 sec	0.16 sec
Overshoot	1.81%	1.99%	2.52%
Undershoot	0.5%	0.32%	none

4.7 Conclusion

For the results described in the previous subsections, it can be stated that the RSDCHBMLI based DSTATCOM is successful in performing load compensation under different load scenarios. The FCS-MPC and SFBI control described in this chapter is able to stabilize the DSTATCOM when it is connected to a weak distribution grid which is an advantage over hysteresis control of DSTATCOM. The inclusion of filter capacitors has improved the quality of PCC voltages as pointed out in Case B. The current control techniques are successful in reference tracking in presence of feeder impedances with low values of steady state error. The DSTATCOM is also successful in improving the power factor and THD of the source currents, along with mitigation of imbalance. This chapter also describes a current based DC bus voltage controller for maintaining the DC-link voltage. The current based controller is compared with conventional power based DC-bus voltage controllers and is shown to have a better response in terms of steady state error, settling time, and overshoot. The performance of the DC-bus controllers is also examined with step change in reference and the i_{loss} based controller is able to track the change in the reference value with minimum error.

The load compensation performance obtained in this chapter is also compared with the results given in [26] and [42]. In [26], the system is an 11 kV system with $\frac{X_{grid}}{R_{grid}} = 3.14$. The DSTATCOM is realized using a CHBMLI and uses proportional+resonant control along with hysteresis control for reference current tracking. There are no filter capacitance connected at PCC, and thus distortion is observed in the source voltages.

The topology uses multiple DC sources and PI controller is used to maintain the average of the DC-link voltages across all the capacitors at the desired value. As a result, unequal capacitor voltage convergence is seen at steady state operation. The THD in the source currents fall from 14.5% in uncompensated system to 3.5% in the compensated system, which is higher than that obtained using SFBI and FCS-MPC control. In [42], a 3-level NPC based topology is used for harmonic mitigation in a 220 kV system. The current control is done using PI controller, and capacitor voltage balancing is achieved by neutral current injection. The THD of the source currents in [42] falls from 28.45% in the uncompensated system to 3.42% in the compensated system, while supplying a purely non-linear load. In the present work, the RSDCHBMLI based DSTATCOM is implemented for load compensation in an 11 kV system with $\frac{X_{grid}}{R_{grid}} = 3.92$. For purely non-linear load, the THD in source currents improve from 49.32% to 0.1% using SFBI and 2.78% using FCS-MPC, which is better than that report in [42] and [26]. The inclusion of filter capacitance at PCC leads to a sinusoidal terminal voltages and thus PCC voltage quality is improved as compared to [26].

CHAPTER 5

CONCLUSION AND FUTURE WORK

This is the final chapter of the thesis and presents the concluding remarks of the thesis. It attempts to summarize the findings of the work with respect to the objectives of the thesis formulated in Chapter 1. In the later part of the chapter, some future possibilities of extension and improvement of the work presented in this thesis is discussed in brief.

5.1 Conclusion

This thesis focuses on load compensation in the distribution system for maintaining power quality and application of multi-level inverter based DSTATCOMS for attaining this objective. To understand the issues of multi-level inverter based DSTATCOM, the first objective of the thesis was to perform a literature review on the voltage source inverter and its control techniques for DSTATCOM design. This review is presented in the first chapter, *Introduction*. From the literature review, it was observed that while MLIs exhibit a number of advantages, their large component requirement and usage of multiple DC-sources/capacitors pose problems in their design and application as DSTATCOM. Balancing of the capacitor voltages demand usage of additional circuits or controls which increase the inverter complexity. Hence, the first objective of the thesis was to develop an 7-level MLI topology that provides a solution for common challenges in MLI implementation.

In Chapter 2, a 7-level RSDCHBMLI topology is developed. This topology has 3 times boosting ability and comparison with other MLI topologies show that maximum voltage stress is reduced to 0.33 times and total blocking voltage is reduced to 2.67 p.u as compared to other topologies. One of the drawbacks of RSDCHBMLI is the doubling of current stress in the four switches due to usage of 1 : 2 turns ratio transformer. The use of transformers provide inherent isolation between the AC side and DC side, along with eliminating any possible path of circulating currents. Hence, RSDCHBMLI

can pose as a suitable choice for implementation in stand-alone operation and also for power quality improvement. As this topology uses 8 switches instead of 12 switches used in conventional MLI topologies, multi-carrier modulation techniques present in the literature is not applicable to it. To overcome this problem, the second objective of the thesis is to develop a single carrier based level shifted pulse-width modulation strategy. This SC-LS-PWM strategy is described in Chapter 2 and its application is verified in both simulation and experiments. Here, multiple references are generated from the modulation signal and comparison between the references and carrier signal generate the switching signal. This technique is simpler, cost effective and doesn't require any look-up table. It can also be applied to conventional MLI strategies. This single carrier based strategy is successful in generating a constant switching frequency PWM operation of the inverter. The FFT of the multi-level waveform shows the presence of dominant harmonics in the switching frequency and the output voltage is proportional to the modulation index as in conventional multi-carrier modulation strategy. This chapter, thus, addresses the first and second objectives of the thesis.

The next stage in investigating RSDCHBMLI performance is to test its operation under voltage controlled mode and current controlled mode. For both the cases, SFB controller is used for attaining the control objectives. In case of voltage controlled mode, addition of K_r term in the control law limits tracking error to 3% in the measured capacitor voltage. For current controlled operation of RSDCHBMLI, the inverter is operated in grid connected mode for injection of desired power into the grid. The control of injected grid current is achieved using state-feedback control coupled with integral action. The filter design is considerably simplified due to use of SC-LS-PWM modulation as the switching frequency can be here determined by the user. From the simulation and experiments, the grid connected operation of the RSDCHBMLI is validated and the THD of the injected grid current is maintained below 5%. In this chapter, the third and fourth objectives of the thesis is attained.

After the operation of RSDCHBMLI in closed loop is verified, RSDCHBMLI is used to design a DSTATCOM for weak distribution system. For using RSDCHBMLI as DSTATCOM, the DC-source for the inverter is replaced using a single DC-link capacitor. This eliminates the need of circuitry or controls constraints for balancing and maintaining required voltage across multiple capacitors. But the RSDCHBMLI also exhibits drawbacks like doubling of current stress in four switches and high current

through the DC-link capacitor. The 3 times boosting ability leads to a 33% reduction in the desired DC-link voltage. The voltage across the DC-link capacitor is held at the desired value by implementing a current based DC-bus voltage controller which allows easier choice of the controller gains using the system parameters. For load compensation by the DSTATCOM, SFBI control, with constant switching frequency is chosen for current control. It is seen that RSDCHBMLI based DSTATCOM with SFBI control is successful in compensating harmonic distortions, unbalances and poor power factor of the load current, under conditions load changes and sag in source voltage. To compare the performance of SFBI control, DSTATCOM current control with FCS-MPC is also implemented and the load compensation performance is compared. It is observed that both control techniques are successful in compensating harmonic components of source currents and reduce source current THD below 5%. The compensation with SFBI is better than that by MPC, as SFBI control is capable of further reducing the THD to 0.1% for a purely non-linear load. While SFBI also requires 13 computations per phase against 21 demanded by MPC, MPC offers almost 4 times faster response as compared to SFBI under load change. Thus, from the results obtained in Chapter 4, it is observed that RSDCHBMLI is successful in operating as a DSTATCOM, in current controlled mode. The current based DC-bus voltage controller not only simplifies by the gain calculation, but also provides a better response as seen by comparing its performance with conventional power based DC-bus voltage controllers. Thus Chapter 4 achieves the objective of design and implementation of RSDCHBMLI based DSTATCOM and evaluates it performance with two current control techniques. It addresses the last four objectives of the thesis.

In conclusion, this thesis investigates the design and operation of a 7-level RSDCHBMLI. The advantages of RSDCHBMLI, like usage of single capacitor, reduction in component count, boosting ability, reduction in voltage stress and total blocking voltage, are highlighted through comparison with other MLI topologies. The disadvantages of the RSDCHBMLI like unequal current stress, unequal power distribution among the cells are also observed. For SPWM modulation of RSDCHBMLI, single carrier based level shifted modulation technique is developed which can be used for other MLIs with reduced number of switches and also permits a low cost implementation as seen from the experimental results. The inverter is also operated in the closed loop for both voltage and current control with SFB control. In both voltage and current controlled mode,

the SFB control law is augmented with additional terms for improved tracking of the reference quantities. The SFB control law is used in the single carrier level shifted PWM modulation to generate constant frequency switching signals that simplify the filter design and sizing. The SFB control law with integral action is also utilized in RSDCHBMLI operation as DSTATCOM. The control law is able to perform the objectives of load compensation in the weak distribution system, by mitigating imbalance and reducing THD of source currents to acceptable limits. The use of RSDCHBMLI as DSTATCOM also eliminated the capacitor voltage balancing issues of DSTATCOM along with reducing reference DC-link voltage due to its boosting capability. The DC-bus voltage control is further simplified using a current based controller where controller gains are related to the system parameters, and can be easily decided. Thus, this thesis attempts to address the challenges of MLI design, and their implementation in power quality improvement by presenting the design and operation of RSDCHMLI in stand-alone, grid connected and DSTATCOM mode. The problems in multi-carrier SPWM modulation for reduced switch topologies are also overcome by the single carrier based modulation technique presented here. The application of modified constant switching frequency SFB control and MPC control is also demonstrated in this thesis.

5.2 Future work

In this section, a few possibilities of extending the work presented in this thesis is discussed. The analysis of the RSDCHBMLI topology shows that the inverter has unequal current stress and power sharing among the two cells. The solution to these drawbacks will be investigated in future research. It was noted from the results presented in Chapter 4 that the dynamic response of the SFBI controller for load compensation was 4 times slower than that with finite control set model-predictive control (FCS-MPC). Thus, improving the dynamic performance of SFBI control is another aspect of expanding the work presented in the thesis. While the dynamic response of FCS-MPC control is an advantage over SFBI control, FCS-MPC results in a variable switching frequency operation. In future work, FCS-MPC control can be modified to limit the switching frequency for DSTATCOM operation. Also, as FCS-MPC permits multi-objective cost function, it can be attempted to include the DC-bus voltage control in the cost function to further simplify the cost function.

The design of RSDCHBMLI based other custom power devices like dynamic voltage restorer (DVR), design of DSTATCOM equipped with voltage control mechanism for maintaining PCC voltages at desired value in case of magnitude variations in source voltage along with performing load compensation, are some other applications where research can be carried out.

LIST OF PUBLICATIONS BASED ON THESIS

Journals

1. R. Chakrabarty and R. Adda, “DSTATCOM implementation using Reduced Switch Single DC Source Cascaded H-bridge Multilevel Inverter", *Elsevier Electric Power System Research*, vol. 199, pp-107373, 2021

Conferences

1. R. Chakrabarty and R. Adda, “State-feedback control of grid-connected RSD-CHBMLI with LCL filter", 9^{th} *Proc. IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES) 2020* , MNIT Jaipur, Dec. 2020.

2. R. Chakrabarty and R. Adda, “Case studies for load compensation using RSD-CHBMLI based DSTATCOM using predictive current control", *Proc.* 46^{th} *IEEE Annual Conference of Industrial Electronics Society (IECON) 2020*, pp. 2463-2468, Singapore, Oct. 2020.

3. R. Chakrabarty and R. Adda, “Output Voltage Control of Single Phase Reduced Switch Cascaded H-bridge Multilevel Inverter with Constant Switching Frequency Operation", 46^{th} *in Proc.* 46^{th} *IEEE Annual Conference of Industrial Electronics Society (IECON) 2020*, pp 4115-4120, Singapore, Oct. 2020.

4. R. Chakrabarty and R. Adda,“Reduced Switch Single DC Source Cascaded H-bridge Multilevel Inverter based DSTATCOM", *Proc.* 45^{th} *IEEE Annual Conference of Industrial Electronics Society (IECON) 2019*, pp. 7074-7079, Lisbon, Oct. 2019.

5. R. Chakrabarty and R. Adda, “Constant Switching Frequency State Feedback Control of Cascaded H bridge Multilevel Inverter with Reduced Switches", *Proc. 2018 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, pp. 1-6 , Dec. 2018.

6. R. Chakrabarty and R. Adda, “Model predictive control of DSTATCOM employ-

ing a single DC source cascaded H-bridge multilevel inverter in a weak distribution system", *Proc. 2018 20th National Power Systems Conference (NPSC)*, pp. 1-6, Tiruchirappalli, India, Dec. 2018.

Journal papers under review

1. R. Chakrabarty and R. Adda, “State-feedback control of grid connected RSD-CHBMLI with LCL filter"

Journal papers under preparation

1. R. Chakrabarty and R. Adda, “Constant Switching Voltage controlled operation of Cascaded H bridge Multilevel Inverter with Reduced Switches"
2. R. Chakrabarty and R. Adda, “State-feedback integral control of RSDCHBMLI based DSTATCOM for load compensation in weak distribution system"

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