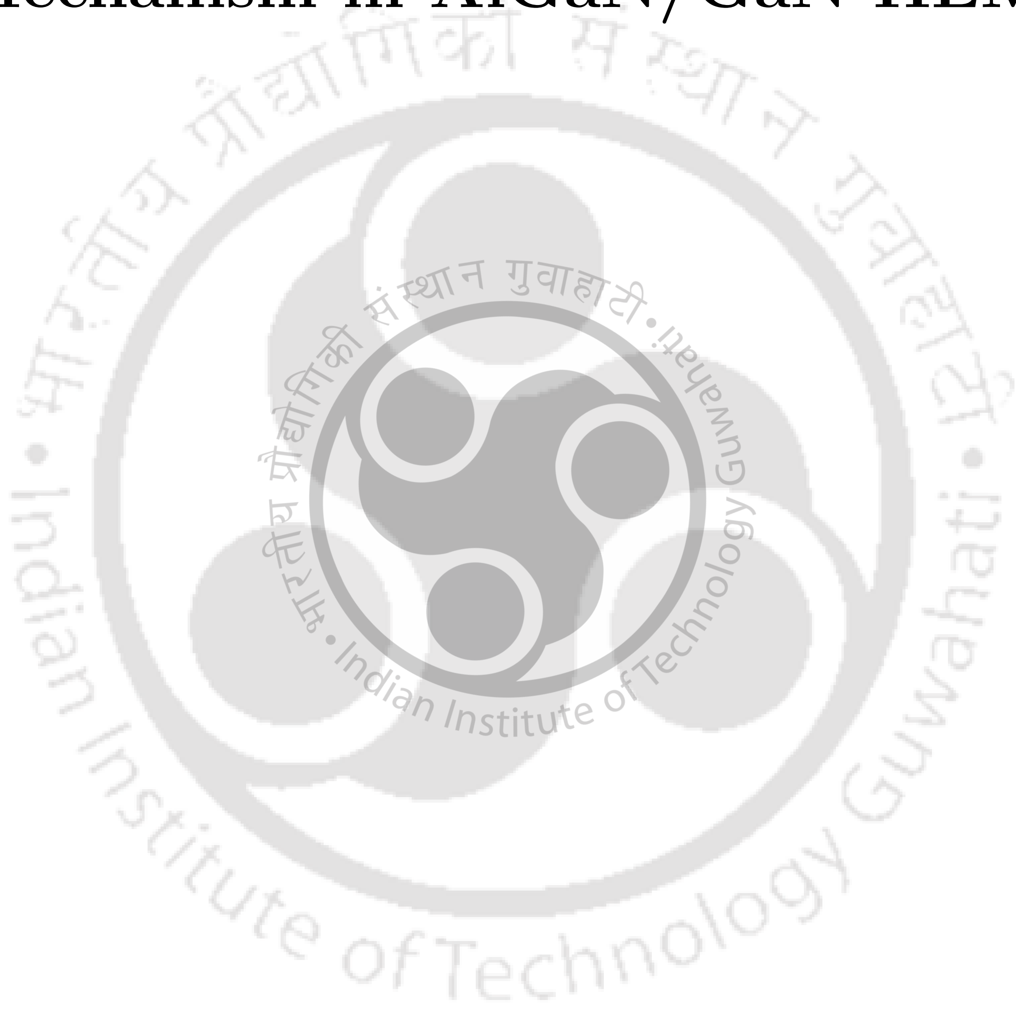
Investigation of Degradation Mechanism in AlGaN/GaN HEMTs



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Investigation of Degradation Mechanism in AlGaN/GaN HEMTs

A

Dissertation Submitted

for the award of the Degree of

Doctor of Philosophy

by

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Declaration

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Certificate

This is to certify that this thesis entitled **"Investigation of Degradation Mechanism in AlGaN/GaN HEMTs"** being submitted by Mr. Sushanta Bordoloi to the Department of Electronics and Electrical Engineering, Indian Institute of Technology Guwahati, is a record of bonafide research work under my supervision and is worthy of consideration for the award of the degree of Doctor of Philosophy of the Institute.

The results contained in this thesis have not been submitted in part or full to any other university or institute for the award of any degree or diploma.

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মা আৰু বাইদেউ,
তোমাৰলোকৰ আশীৰ্বাদ, স্নেহ আৰু অনুপেৰণাৰ বাবে
এই গবেষণামূলক প্ৰবন্ধ আগবঢ়ালো ।

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– **Sushanta Bordoloi**

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Abstract

With the advancement of technology and autonomous systems, such as electric vehicles, high electron mobility transistor (HEMT) have gained prominence in the present era. It is anticipated that in future, driver-less autonomous vehicles, high power smart electromechanical robots, deep space vehicles like giant engineering systems would replace conventional systems. The above mention requirement can be addressed by using an efficient HEMT, which can operate at high power and high temperature without any degradation in the reliability.

The reliability of a device depends on many factors, viz. electric field, electron temperature, self-heating and converse piezoelectric effect, leakage current. In this thesis, various techniques for the mitigation of electric field are proposed. Electric field is primarily responsible for the degradation of a device as it induces majority of the degradation mechanisms. In a conventional device, the gate edge is rectangular in shape and electric field crowding is observed at the gate edge toward the drain side. The concentration of electric field at the gate edge controls physical properties of a device, such as built-in strain, converse piezoelectric-electric strain, and critical voltage. It is well-established that the breakdown mechanisms originate from gate edge toward the drain side due to the presence of high electric field under normal operation of a device. This electric field may initiate avalanche breakdown, thermally-assisted tunnelling, or localized Schottky-barrier breakdown in the device. Therefore, it is imperative to engineer electric field in the vicinity of the gate edge in a device for performance enhancement.

Field plate technology is widely implemented to moderate high electric field at the drain edge of the gate of a device. The field plate topology assists in the uniform distribution of electric field in the gate–drain access region, and aids in the increase of breakdown voltage of a device. Several variations of field plate topology are reported in the literature, such as gate connected, source connected, and drain connected field plate etc. It is observed that in a gate connected field plate device, electric field peaks at the edge of field plate. Electric field is found to be quite high at the edge of field plate in the SEMI-ON state of a device. Experimental

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observations indicate the generation of hot carriers at the edge of field plate in the SEMI-ON state. This may act as a location for further degradation in a device. Therefore, it is essential to address the issue of electric field crowding at the drain side of gate edge as well as at field plate edge in a HEMT.

In this thesis, a method is proposed to mitigate electric field at the gate edge of a device by modifying shape of the gate edge. Although gate shape engineering is well-known for the enhancement of device performance with slant gate, a particular gate–shape (rounded gate edge) is depicted in this thesis. Additionally, the proposed device is integrated with field plate topology, namely, gate connected field plate to investigate behaviour of a device. The investigation is performed with the help of numerical analysis framework, which is calibrated with the parameters available in the literature and an experimental data. A comparison of the proposed device with a conventional device is carried out on various parameters, viz., electric field profile, electron temperature profile, DC characteristics, breakdown voltage and capacitance-voltage characteristics. It is found that the proposed device structure helps in improving all the above mentioned parameters increasing device reliability. Similarly, a comparison of the proposed gate structure with a staircase gate structure states reduction in the converse piezoelectric effect and vertical electric field. This makes the device structure presented in this thesis a suitable candidate to be utilized in the wide range of high power applications.

Additionally, as a consequence of shorter device gate length in the field plate structure, the gate to drain spacing shrinks, which results in an electric field peak at the field plate edge, when the device is biased in the SEMI-ON state. In this thesis, to mitigate this issue, the use of diamond layer is proposed on the top of a passivation layer with a SiO_2 pocket at the edge of a field plate. In order to validate it, a numerical analysis framework is calibrated with an experimental data. The outcome of numerical analysis indicates that employing diamond layer with a SiO_2 pocket at the edge of a field plate on the top of a passivation layer reduces electric field profile, carrier temperature, self heating and thermal resistance of the device. This helps in the reduction of device degradation, which is initiated at the edge of a field plate, and

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increases device reliability.

Keywords: AlGaN/GaN HEMT, Capacitance Voltage (CV), Diamond, Electric field, Electron temperature, Field Plate, Rounded gate devices, Leakage Current, Reliability, Self heating, Silicon dioxide, Thermal Resistance.

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List of Abbreviations

BJT Bipolar Junction Transistor

CMOSFET Complementary metal-oxide-semiconductor field effect transistor

CTE Coefficient of Thermal Expansion

EGS Electronic-Grade Silicon

EL Electroluminescence

FET Field Effect Transistor

FinFET Fin-shaped field effect transistor

FOMs Figures of Merits

GaAs Gallium Arsenide

GaN Gallium Nitride

GaP Gallium Phosphide

HCP Hexagonal Close Packed

HEMT High Electron Mobility Transistors

IC Integrated Circuit

IGBT Insulated Gate Bipolar Transistor

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InGaN Indium Gallium Nitride

InGaP Indium Gallium Phosphide

InP Indium Phosphide

IR Infrared Radiation

JFET Junction Field Effect Transistor

JFoM Johnson Figure of Merit

LEDs Light Emitting Diodes

MOSFET Metal Oxide Semiconductor Field Effect Transistor

MC Monte Carlo

NCD Nano Crystalline Diamond

NEA Negative Electron Affinity

NDC Negative Differential Conductance

NSD Noise-Spectra-Density

PAE Power Added Efficiency

PIN P-type I-intrinsic N-type

Si Silicon

SiC Silicon Carbide

TBR Thermal Boundary Resistance

TCAD Technology Computer Aided Design

TTF Time to Failure

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2DEG Two Dimensional Electron Gas

UV Ultraviolet

ZnS Zinc Blende Structure

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List of Symbols

$\boldsymbol{P_n}$	Absolute Thermoelectric Power of Electron
$\boldsymbol{P_p}$	Absolute Thermoelectric Power of Hole
$\boldsymbol{E_g}$	Bandgap
$\boldsymbol{\phi_b}$	Barrier Height
$\boldsymbol{\kappa_B}$	Boltzmann Constant
$\boldsymbol{\phi_b}$	Barrier Height
$\boldsymbol{c_n}$	Capture Probability of Electron
$\boldsymbol{c_p}$	Capture Probability of Hole
$\boldsymbol{q}$	Charge of Electron
$\boldsymbol{n}$	Concentration of Electron
$\boldsymbol{p}$	Concentration of Hole
$\boldsymbol{E_C}$	Conduction Band
$\boldsymbol{\Delta E_C}$	Conduction Band Offset
$\boldsymbol{E_{crit}}$	Critical Field
$\boldsymbol{\sigma_p}$	Cross section for Acceptor Traps
$\boldsymbol{\sigma_n}$	Cross section for Donor Traps
$\boldsymbol{f_T}$	Current Gain Cut-off Frequency
$\boldsymbol{\rho_m}$	Density of the Material
$\boldsymbol{N_c}$	Density of States in Conduction Band
$\boldsymbol{N_v}$	Density of States in Valence Band
$\boldsymbol{\hbar}$	Dirac Constant

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$\boldsymbol{I_D}$	Drain Current
$\boldsymbol{V_{DS}}$	Drain Voltage
$\boldsymbol{m_n}$	Electron Mass
$\boldsymbol{m^*}$	Effective Electron Mass
$\boldsymbol{E_{trap}}$	Energy of Trap
$\boldsymbol{S}$	Elastic Compliance
$\boldsymbol{C}$	Elastic Constant
$\boldsymbol{\chi}$	Electron Affinity
$\overrightarrow{J_n}$	Electron Current Density
$\boldsymbol{S_n}$	Electron Energy Flux Density
$\boldsymbol{\mu_n}$	Electron Mobility
$\boldsymbol{\phi_n}$	Electron quasi-Fermi Potential
$\boldsymbol{R_{net,n}}$	Electron Recombination Rate
$\boldsymbol{v_n}$	Electron Velocity
$\boldsymbol{e_n}$	Emission Probability of Electron
$\boldsymbol{G_n}$	Emission Generation Rate of Electron
$\boldsymbol{e_p}$	Emission Probability of Hole
$\boldsymbol{G_p}$	Emission Generation Rate of Hole
$\boldsymbol{E_{f,n}}$	Fermi Level of Electron
$\boldsymbol{E_{f,p}}$	Fermi Level of Hole
$\boldsymbol{F_{1/2}}$	Fermi integral of order $\frac{1}{2}$
$\boldsymbol{L_G}$	Gate Length
$\boldsymbol{C_g}$	Gate Capacitance
$\boldsymbol{L_{GD}}$	Gate to Drain Spacing
$\boldsymbol{C_{gd}}$	Gate to Drain Capacitance
$\boldsymbol{L_{GS}}$	Gate to Source Spacing
$\boldsymbol{C_{gs}}$	Gate to Source Capacitance

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V_{GS}	Gate Voltage
W_G	Gate Width
H	Heat Generation Rate
m_p	Hole Mass
$\vec{J_p}$	Hole Current Density
ϕ_p	Hole quasi-Fermi Potential
$R_{net,p}$	Hole Recombination Rate
a	Lattice Constant
c_L	Lattice Heat Capacity
f_{max}	Maximum Frequency of Oscillation
n_T	Number of Occupied Traps
f_t	Occupation Probability of Generation-Recombination Centres
G^{opt}	Optical Generation Rate due to Photons
R_{on}	On Resistance
e	Piezoelectric constant
P_{PZ}	Piezoelectric Polarization
P_{SP}	Spontaneous Polarization
ε	Strain
σ	Stress
T	Temperature
κ_L	Thermal Conductivity
$\upsilon_{th,\ n/p}$	Thermal Velocity of Electron and Hole
V_T	Threshold Voltage
N_T	Total number of traps
g_m	Transconductance
f_m	Unity Current Gain Limit
E_V	Valence Band

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ε_0	Vacuum's Dielectric Constant
v	Velocity of Carrier
ϕ	Work Function

1

Introduction

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1.1 Background

The advent of semiconductor device technology has changed the world significantly. This aided to the massive transformation of mechanical or electromechanical systems to electronic systems, which helped in making our lives comfortable and safer. When the first semiconductor amplifier was fabricated with germanium, it was assumed that germanium would be a promising candidate of the future semiconductor technology. However, in the short span of time other silicon technologies replaced germanium due to ease of manufacturing of the silicon devices. It was followed by various inventions, such as Texas Instrument of integrated circuits with resistors, capacitors and transistors; Intel 4004 chip with 2200 transistors in 1971 etc. Since then, the semiconductor industries progressed drastically and semiconductor technology is included in the list of top 10 future technologies recently. It is well established that without semiconductor device technology, advanced and sophisticated systems cannot be manufactured. Advancements in CMOS technology, FinFETs, sub-5nm semiconductor devices, high power devices based on compound semiconductors etc. enable us not only to integrate many diverse functionalities in a single die but also to design area and power efficient systems. It is expected semiconductor industries to grow to $ 522 Billion in 2021 worldwide despite COVID19 pandemic and shortage of supply [11].

The applications of semiconductor devices are classified into high power or high speed, which is represented as power frequency diagram of semiconductor materials in Fig. 1.1. The power axis is the combination of several factors, such current, voltage handling capability, selection of a particular technology for an application based on reliability (thermal considerations and ruggedness), performance (efficiency and linearity), cost, size, and legacy. The other axis denotes frequency of the device, which primarily depends on the device size (scaling) as well as device design. Semiconductor devices can also be classified on the basis of carriers as unipolar (majority carrier) or bipolar (minority carrier). Unipolar devices are generally faster, while bipolar devices has superior on-state performance. Unipolar devices include MOSFET, JFET, and Schottky diodes. Thyristor, BJT, IGBT, and variants of PIN diode constitute the bipolar

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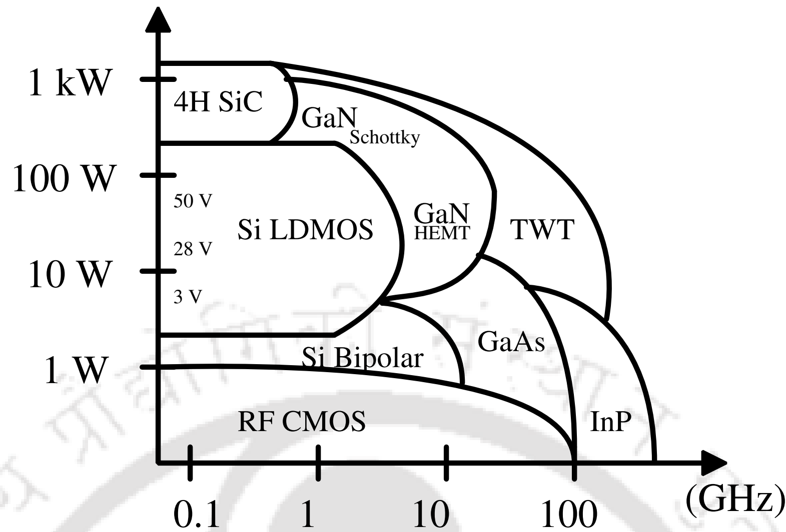

Figure 1.1: The power frequency diagram of application for the semiconductor materials [1]

devices. As we know, by employing voltage and electric field scaling high speed and low power devices can be designed according to the requirement.

Over the years, Moore's law dictated that number of transistors in an integrated circuit (IC) doubles approximately every two years. The impact of this law is the reduced cost per function, but due to aggressive technology scaling, this rule loses its significance. Further technology scaling puts several limits on the device design and it is anticipated that after a certain threshold, it would not be possible for us to realize an electronic circuit on silicon with high reliability. For smaller and faster reliable circuits, other alternatives are being researched, which includes spintronics, quantum computing, superconductivity etc. Theoretically, some indicators, viz. Shannon-von Neumann-Landauer minimum energy required to switch a bit from 1 to 0 in a device, $E_{s|min}$, [12]; the minimum size of a computational element, L_{min}, given by Heisenberg uncertainty principle; the minimum size corresponds to the maximum integration density of switches, n_{max}; the minimum time of gedanken least energy switch, τ_{min}, can be employed to estimate limits of a reliable device integration on the silicon. Theoretical estimates of $E_{s|min}$, L_{min}, n_{max} and τ_{min} are given below for the ready reference.

$$E_{s|min} = ln(2)\kappa_B T = 0.017 \text{ eV}$$

$$L_{min} = \frac{\hbar}{\sqrt{2m_e E_{s|min}}} = 1.5 \text{ nm}$$

$$n_{max} = \frac{1}{L_{min}^2} = 4.7 \times 10^{13} devices/cm^2$$

$$\tau_{min} = \frac{\hbar}{E_{s|min}} = 0.04 \text{ ps}$$

With the technology scaling down to 18 nm, several limits of the device design have already been reached, such as transistor integration density per □, i.e. 3.5×10^9 cm^{-2}, which impacts several vital operational parameters of a semiconductor device, viz. thermal stability, device reliability etc. Although, a large number of transistors on a silicon die aids in the realization of diverse functionalities, but it also increases non-linear effects, power consumption and area utilization of a device.This issue can be addressed by limiting the number of functional transistors at a moment, thus restricting the thermal load or operating the system at cryogenic temperature. Similarly, an increase in the number of longer interconnects becomes bottleneck in the signal propagation. As we know, the transistor density cannot be scaled beyond a particular point, and aggressive device scaling needs to be supplemented with novel devices and materials.

Among various semiconductor devices, compound semiconductors devices have a special place. In order to comprehend the role of compound semiconductors, it is essential to understand the dominant position of silicon. The primary advantage of silicon is the abundant source material silica, which is cheap and can be refined easily into electronic-grade silicon (EGS). Besides, wafers as large as 12 inch are possible to get manufactured. Silicon can be easily doped as n-type or p-type, and most importantly the high quality native oxide, SiO_2. As we know, the SiO_2 interfaces strongly with silicon, which facilitate less traps both at the interface as well

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Table 1.1: Commercial Device Market of Semiconductor Materials [7]

Items	Material	Applications	Revenue (in $ Billion)
Light Emitting Diodes (LEDs)	GaN, GaP	Indicators, Flat Panel display, Illumination	8.5
Solar Cell	GaAs, GaInP, CuGeSe	Satellite devices	0.5
Lasers	GaAs, GaN, InP	Data communications, switches, optical storage	2.5
Wireless	GaAs, GaN, InP	Mobile communications	8

as in the oxide.

The compound semiconductors can be considered as an alternative to silicon in terms of various technological parameters in order to compensate the advantage of cost effective device manufacturing using silicon. Information about compound semiconductor is enlisted in Table 1.1. Silicon being an indirect bandgap semiconductor cannot be used for light emitting diodes (LEDs), whereas GaN, GaP, and GaAs are used as materials for LEDs. Compound semiconductors, such as, GaN and SiC enable devices to perform at high operating voltages in power electronic circuits due to their wide bandgap. Therefore, commercial transistors operating above 100 GHz are realized with GaAs and InP.

Direct bandgap compound semiconductors produce an entire spectrum of light, i.e., near UV, blue and green light is generated by InGaN based LEDs, whereas, amber, red and IR light is produced by $GaAs$ or GaP based LEDs. There is a growing demand for high brightness LEDs for flash photography, back lighting, and general illumination in a bid to replace existing incandescent light bulb. In order to address this issue, InGaP based devices are utilized, in which lasers exploit the absorption minima of fiber optics. The integration of III-V laser with silicon based lasers in on-chip optical communication plays a crucial role in the advancement of telecommunication sector. Nakamura demonstrated blue light LED using $GaN/InGaN/GaN$ double heterostructure in 1993 [13], followed by laser diode in 1997 [14]. Since then, GaN is used for fabricating UV detectors [15].

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Table 1.2: Comparison of normalized Figures of Merit of Semiconductor Materials [8]

Semiconductor	Johson's FOM	Balinga's FOM
Si	1	1
Ge	0.03	0.3
GaAs	7.1	10.8
GaP	37	5
GaN	760	77.8
AlN	5,120	1,100
4H-SiC	180	22.9

The large bandgap and critical field of GaN and SiC enable operations at high temperature without complete carrier ionization as well as at high voltage. The large thermal conductivity of SiC eliminates the effects of self heating. It is to mention that the normalized thermal conductivity of GaN and $4H-SiC$ to Si are 0.87, and 3, respectively, which reduces self-heating effect with respect to silicon. Since on-resistance, R_{on}, is inversely proportional to mobility, $Al_xGa_{1-x}N$/GaN High Electron Mobility Transistors (HEMT) has lower R_{on} due to higher mobility.

Although there exist a number of predictions for the compound semiconductors, Figures of Merits (FOMs) is a quantitative way to evaluate the performance based on specific dependencies taken into consideration. Johnson's FOM [16] is described as power frequency product per unit width.

$$JFOM = \frac{\upsilon_{n,sat} \cdot E_{crit}^2}{2\pi} \tag{1.1}$$

where, E_{crit} is critical field for breakdown, and $\upsilon_{n,sat}$ is electron saturation velocity. Similarly, Baliga's FOM [17] is stated below.

$$BFOM = \mu_n \cdot E_{crit}^2 \tag{1.2}$$

It is an efficient measure of breakdown voltages in GaN HEMTs. It is to mention that efficient HEMTs have high-breakdown voltages and low-access resistances (high mobility). The Johnson and Baliga FOMs for common semiconductor material are listed in Table 1.2.

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GaN transistors possess electronic properties, which enable them as an ideal candidate for high power microwave devices [18]. These properties are the direct manifestation of wide bandgap (E_g = 3.4 eV) and high electric breakdown field ($\sim$ 3 MV/cm). The high electric field permits *GaN* devices to operate at high drain voltages with low noise (NF = 0.6 dB at 10 GHz), thereby increasing the range of operations [19]. On the other hand, *GaN* device operates at high temperature without any degradation due to its wide bandgap. Furthermore, the high saturation velocity ($\upsilon_{sat} = 2 \times 10^7$ cm/s) is accountable for high current density ($I_{max} \propto \upsilon_{sat}$) and operating frequency ($f_t \propto \upsilon_{sat}$) of the *GaN* devices.

GaN HEMTs find applications in high frequency and high power regime and it is found that their performance exceeds *SiC* or *GaAs* based devices. The emergence of RF and microwave application of *GaN* HEMTs is not only cost effective but also advantageous for numerous military and commercial systems, such as, X band radar systems, power amplifier for terrestrial and satellite communication [20] etc.

1.2 Motivation for the present work

GaN devices are known to have exceptional high power and high frequency performance, but the issues related with the stability and reliability of these devices [21] should be addressed efficiently for their extensive commercial use. The failure mechanisms include device degradation [22, 23], self heating [24, 25], and current collapse [26–29]. Device degradation is associated with trap-related phenomenon, where creation of new trap states takes place. Although there exist several causes of the device degradation, the two leading hypothesis are hot-electron induced effects [30] and converse piezoelectric effect assisted stress induced defects generation [31]. The latter hypothesis is corroborated by an experimental observation of the increased strain with the help of micro-Raman technique [32]. It is also observed that the device degrades when it is biased above a critical drain to gate voltage [33], even in the OFF state. Thus, the motivation of the proposed work is to study various degradation mechanisms, so that reliability and stability of *AlGaN*/*GaN* HEMTs can be improved.

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1.3 Objectives of the Thesis

In this thesis, we aim to study degradation mechanisms that arise due to high electric field at the gate edge. This task includes following objectives.

(i) Development of a numerical analysis framework to study degradation mechanisms in a device. The numerical analysis framework is proposed to be calibrated with parameters, models, and data available in the literature.

(ii) The high vertical electric field at the gate edge is the prime reason for several degradation mechanisms. It is proposed to study the impact of alteration of gate shape of a device (rounded gate device) as illustrated in Fig. 1.2(a) on the electrical field and other associated degradation mechanisms.

(iii) Field plate is a well established technology to address the issue of high electric field at the gate edge. In this work, we propose to examine the incorporation of field plate to rounded gate device as illustrated in Fig. 1.2(b) and to study electric field profile for understanding reduction in the degradation mechanisms.

(iv) Although electric field at the gate edge is managed by field plate technology, the crowding of electric field at the field plate edge can be a potential hot-spot of the electrical field in the SEMI-ON and OFF-states. A study of electric field profile in the SEMI-ON and OFF-states of a device is proposed to be conducted with Diamond/SiN_x passivation stack having a SiO_2 pocket around the field plate edge for suppressing electric field. Self-heating and thermal resistance of HEMTs are also aimed to be investigated for the proposed modifications to the device for improved reliability and stability.

1.4 Contribution of the Thesis

The contributions of the thesis are stated as follows.

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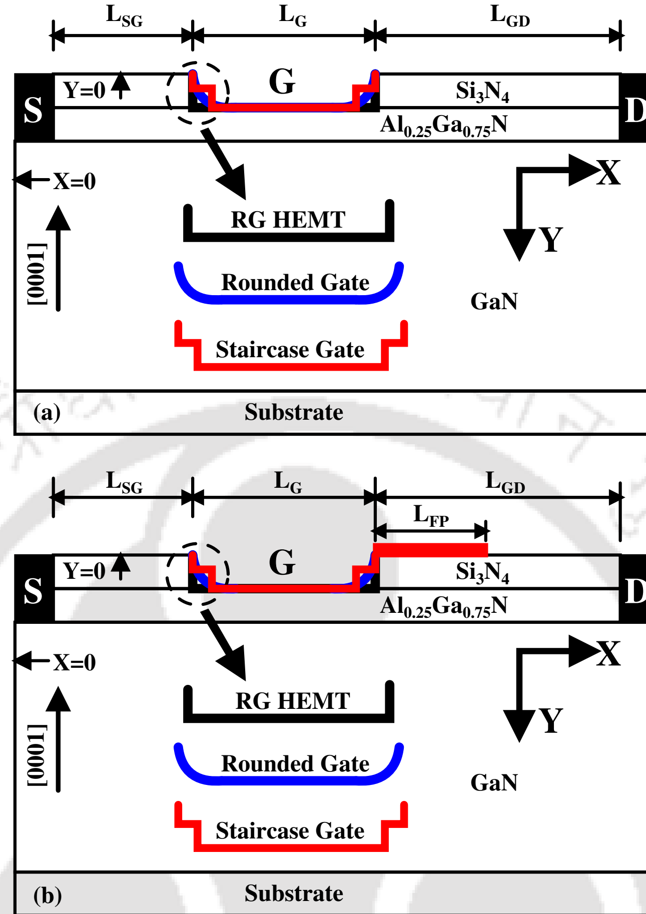

Figure 1.2: Schematic of proposed rounded gate along with rectangular and stair case device structure: (a) without and (b) with field plate.

(i) An increase in the electric field at the gate edge toward the drain terminal in a device is moderated by modifying gate structure of a device. The proposed rounded gate devices with and without field plate are observed to mitigate electric field at the gate edge, which is well corroborated with the findings of numerical analysis. The subdued electric field prohibits electric field induced degradation mechanisms in the proposed rounded gate device. Additionally, the proposed gate shape device is observed to have enhanced breakdown voltage.

(ii) The primary contributing factor in the converse piezoelectric strain is the vertical electric field. This electric field at the gate edge is moderated by changing gate geometry to either rounded gate or stair case as compared to conventional (rectangular) gate geometries. As

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a result, converse piezoelectric strain reduces in these devices and is found to vary linearly with the gate bias. Further, reduction in the gate bias decreases converse piezoelectric strain and vice-versa.

(iii) Similarly, electric field at the field plate edge of a device when biased in the SEMI-ON or OFF state is mitigated by employing a Diamond layer on the top of SiN passivation and a SiO_2 pocket around the edge of a field plate. It is found in the numerical analysis that electric field, electron temperature, self heating and thermal resistance get reduced in the proposed device. Moreover, carrier temperature, electric field, self heating and thermal resistance decrease consistently at the field plate edge in the proposed device, when the thickness of SiN and Diamond layers are varied.

1.5 Organization of the Thesis

The proposed research work is organized as mentioned below.

- **Chapter 2** introduces basics of a crystal structure, electrical properties of III-N materials and origin of two dimensional electron gas (2DEG) due to polarization effects. Properties of III-N based heterostructures, such as band discontinuity and polarization are discussed in this chapter along with the operation of AlGaN/GaN HEMT and key challenges. Finally, introduction to numerical analysis is also presented for the completeness.

- **Chapter 3** presents a brief of degradation mechanisms and the reliability aspects of AlGaN/GaN HEMTs.

- **Chapter 4** depicts the impact of rounded gate and field plate to the degradation mechanisms in a device. The electric field at the gate edge is examined for the proposed modifications and an associated degradation mechanism is explained in this chapter.

- **Chapter 5** states the mitigation of converse piezoelectric strain in a device as gate geometry is varied. Three type of gate geometries are considered for the investigation,

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namely, conventional gate geometry (RG), rounded gate ('dr5' as FG) and stair case geometry (SG). It is found that the moderation in converse piezoelectric strain is related to the reduction of electric field at the gate edge.

- **Chapter 6** investigates electric field at the edge of field plate of a device in SEMI-ON and OFF states. The high electric field at the field plate edge translates to hot-spots, which is addressed by introducing a SiO_2 pocket around the field plate edge along with Diamond/SiN_x stack. Self heating and thermal resistance is also examined for these proposed modification in this chapter.
- **Chapter 7** summarizes results stated in the previous chapters. Not only it draws corresponding conclusions but also outlines future directions.

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2

Basics of AlGaN/GaN HEMTs and Numerical Analysis

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This chapter depicts about GaN and its properties that enable it to be utilized in the design of high electron mobility transistor HEMT for high power and high frequency applications. Section 2.1 outlines crystal structure of GaN. Section 2.2 deals with the concept of hetero-structure in semiconductors. Section 2.3 introduces the polarization property that helps in the formation of two dimensional electron gas (2DEG) at the interface, which is discussed in Section 2.4. Section 2.5 states the principle of AlGaN/GaN HEMTs and its working, while Section 2.6 underlines the importance of substrate for these devices. Section 2.7 highlights the challenges in AlGaN/GaN HEMTs.

2.1 Crystal Structure

The group III nitride semiconductors, such as AlN, GaN, InN crystallize in both wurtzite hexagonal close packed (HCP) and cubic zinc-blende structures (ZnS). In comparison of the two crystal structures, wurtzite structure is more stable. This structure inherits the characteristics of spontaneous polarization, P_{SP}, which helps in the formation of (2DEG) at hetero-interfaces. The other semiconductors belonging to group III-V, viz. InP or GaAs, crystallize in the zinc-blende structure.

The wurtzite structure of GaN is a hexagonal bravais lattice with four atoms per unit cell [34]. Group III nitride compounds, such as, GaN are predominantly covalent, however the difference in electronegativity of Ga and N atoms leads to ionic contribution to the bond, which determines the stability of respective structural phase.

III-Nitrides crystallize in hexagonal wurtzite structure or zinc-blende structure. Since it lack the centre of symmetry, therefore it shows piezoelectricity. It is to mention that wurtzite exhibits poor symmetricity and polarizes spontaneously. The wurtzite structure is characterized by three lattice constants, namely a, c, and u as shown in Fig. 2.1. The side length of the hexagonal wurtzite structure is denoted as a, height of the cell as c, and the length of III-N bond as u. The parameter u is dimensionless and its value is defined in the ratio of c. For an ideal wurtzite structure, the ratio of these parameters are $u/c = 3/8 = 0.375$ and $c/a =$

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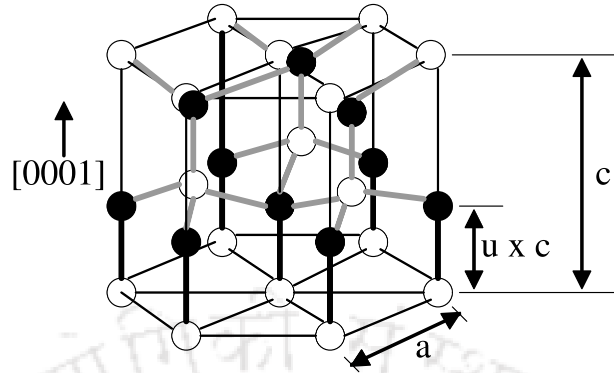

Figure 2.1: Hexagonal Wurtzite Structure

$\sqrt{8/3} \approx 1.633$. The structural parameters of common III-N wurtzite semiconductors is stated in Table 2.1.The arrows on hexagonal wurtzite structure denotes <111> directions [35].

Table 2.1: Structural parameters of common nitrides semiconductors [9]

Parameter	AlN	InN	GaN
a (A°)	3.108	3.580	3.197
c/a	1.6033	1.6180	1.6297
(u-u_{ideal}) $\times 10^{-3}$	6.4	3.7	1.9

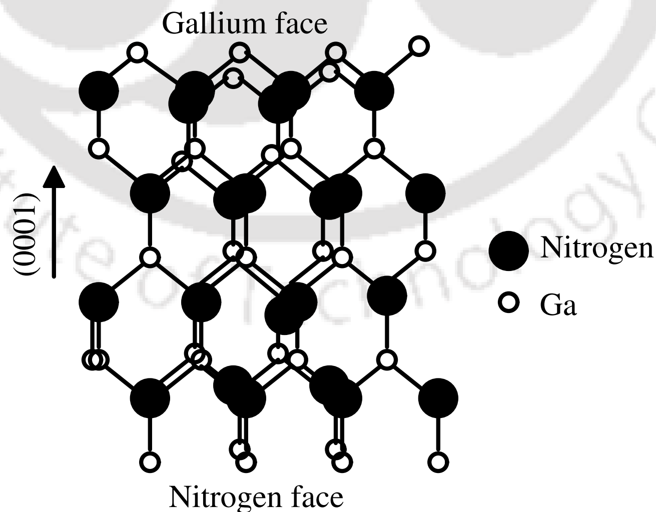

Figure 2.2: Crystal structure of Ga-face, GaN

As we know that wurtzite structure tends to have low symmetry. An ideal structure exhibits spontaneous polarization, P_{SP}, affecting 1/3 to 1/2 of the actual structure [36]. Due to the

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non-existence of inversion symmetry in wurtzite structure along the c-axis (also known as pyroelectric axis) [37], directions [0001] and [$000\bar{1}$] are not identical as shown in Fig. 2.2. The Ga and N atoms along this bond form the dipoles, which are the basis of macroscopic polarization. Also, wurtzite GaN crystal has two well-defined face corresponding to crystalline faces, known as Ga-face (0001) and N-face ($000\bar{1}$). In the GaN crystal, electric dipole is directed from the N to the Ga atom indicating negative magnitude of the polarization. Since polarization being a bulk property [38], the polarity of the crystal depends on direction of the crystal structure and has no dependency on the surface layer.

In the subsequent section, details about hetero-structure are presented, which is essential in the design of high electron mobility transistor (HEMT).

2.2 Hetero-structure

Hetero-structure is a structure that employ a hetero-junction, which consists of a junction with two different materials. The two materials differ in bandgap energies and different band structures. The resulting band structure of the hetero-junction determines behaviour of a device and is of great importance. Moreover, difference in the polarization of the materials and subsequent charges bounded at the interface play a pivotal role in the band diagrams of III-N semiconductors.

The contact to the device can be either non-rectifying metal semiconductor constant (also known as ohmic contact) or rectifying metal semiconductor contact (also known as Schottky contact). The non-rectifying contact has virtually no barrier height between metal and conduction band of the semiconductor, and facilitates supply of carriers to the device. Source and drain terminals of the device are non-rectifying or ohmic contact. In contrast to non-rectifying contact, gate terminal of the device is realized as rectifying contact because of barrier height present between metal and conduction band of the semiconductor. The barrier height is the difference of work function of the metal and electron affinity of the semiconductor.

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The semiconductors forming hetero-junction have different bandgaps and one of them should have wider bandgap. The bandgap of GaN is given as 3.42-3.50 eV [6], however, the bandgap of $Al_xGa_{1-x}N$ and other nitride ternary is given as [39, 40]

$$E_g(A_xB_{1-x}N) = xE_g(AN) + (1-x)E_g(BN) - b_{ABN}x(1-x) \tag{2.1}$$

where, x is the mole-fraction, b is the bowing parameter, and other letters have their usual meanings.

For $Al_xGa_{1-x}N$/GaN hetero-junction, $Al_xGa_{1-x}N$ has wide bandgap as compared to GaN. Due to the mismatch in the bandgap, there is a bandgap discontinuity, which is represented by $\triangle E_g$ (difference of the bandgap energies of two semiconductors). The bandgap discontinuity is represented as

$$\triangle E_g = \Delta E_C + \Delta E_V \tag{2.2}$$

where, $\triangle E_C$ and $\triangle E_V$ are conduction band and valence band offsets, respectively as shown in Fig. 2.3.

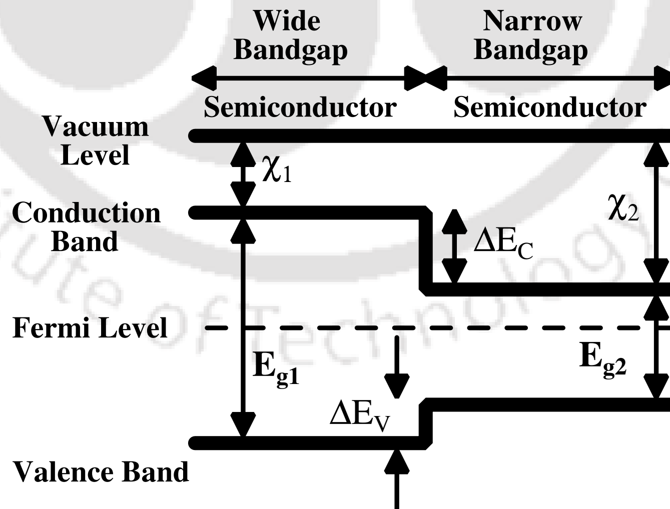

Figure 2.3: A hetero-structure with two semiconductors having different bandgap energies E_{g1} and E_{g2}, and affinities χ_1 and χ_2.

The conduction band discontinuity ΔE_C is due to difference of affinities, χ_1 and χ_2. The bandgap energy difference $(E_{g1} - E_{g2})$ determines valence band discontinuity ΔE_V. It is to

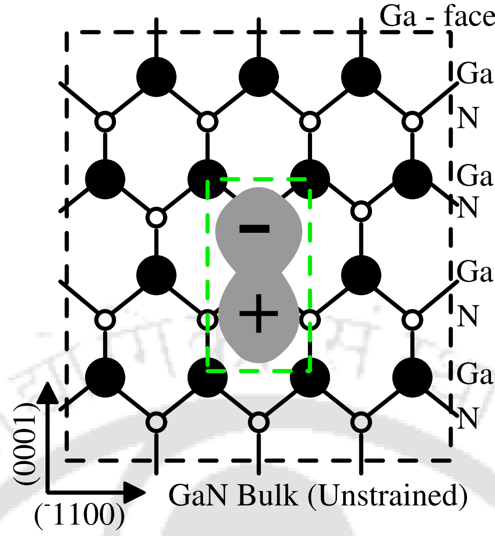

Figure 2.4: Spontaneous polarization charges due to crystal asymmetry in wurtzite crystal

mention that in III-N based devices, the channel electrons are provided by the polarization difference of two semiconductors. For $Al_xGa_{1-x}N$/GaN hetero-junction, the difference in bandgaps of the two semiconductors leads to band bending, which helps in the creation of a well with high electron density. This phenomenon is due to the polarization of III-Nitrides, which is discussed in Section 2.3. As a result, the requirement of doping for band bending in other semiconductors is eliminated.

2.3 Origin of Polarization

Polarization is a crucial material property in III-N semiconductor that determines the operation of nitride devices. This property arises due to the shift in centre of negative charges away from the centre of positive charges that exists between the bonding atoms [41]. It leads to polarize atoms, which form a dipole with the dipole moment, $\overrightarrow{p}$. The polarization of the material is described by an electric polarization vector, $\overrightarrow{P}$ as

$$\overrightarrow{P} = n\overrightarrow{p} = \overrightarrow{p}/\Omega_0 \tag{2.3}$$

where, n is the concentration of identical dipoles and Ω_0 is the volume of a dipole.

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Under the condition, when there is no electric field, materials either has no dipole or their orientation is random, such that the total polarization is zero. This is not true for the compound crystals, which has low symmetry, where dipoles are present even when there is no electric field. This condition gives rise to spontaneous polarization in the crystal as shown in Fig. 2.4. Piezoelectric polarization, P_{PZ}, exists in the structures having mechanical deformation and lacking centre of symmetry. Also, for a crystal which has no or a single rotation axis, the bonding in the crystal is asymmetric provided rotation axis is not an inversion axis. This type of materials are known as pyroelectric materials and they exhibit built-in spontaneous polarization, P_{SP}. Spontaneous polarization exists without any mechanical deformation or electric field. The low symmetry axis parallel to the built-in spontaneous polarization direction is known as pyroelectric axis. Similarly, ferroelectric materials exhibit polarization even when there is no electric field. It is to mention that the polarization in these materials can be inverted by applying an electric field to measure P_{SP}, whereas, this is not possible in pyroelectric materials.

Further, III-V semiconductors mostly crystallize either in cubic zinc-blende or hexagonal wurtzite structures. Since both the structures are non-centrosymmetric in nature, these are classified as piezoelectric materials. However, zinc-blende crystals do not possess spontaneous polarization unlike wurtzite crystals. This is due to the presence of rotational symmetry axis and an inversion axis in zinc blende crystals, while wurtzite crystals have rotational symmetry axis, but lack in inversion symmetry. Hence, zinc-blende crystals cannot be identified as pyroelectric material.

Under the condition of small/lower strains, polarization is linearly dependent. Therefore, if there exists any polarization, when strain is zero, it is referred as spontaneous polarization P_{SP}, which can be distinguished from piezoelectric polarization. In piezoelectric materials, the strain results in polarization field P_{PZ}. Thus, the overall polarization is the aggregate of both the polarizations, $P = P_{PZ} + P_{SP}$.

Let us consider AlGaN/GaN hetero-structure, wherein $Al_xGa_{1-x}N$ (a ternary alloy of ni-

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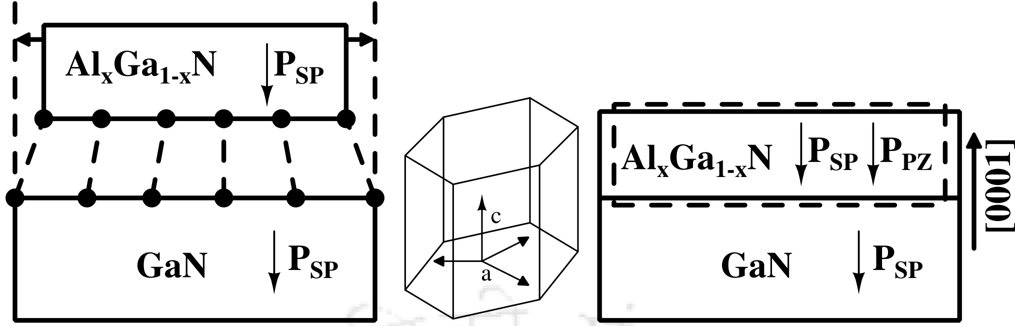

Figure 2.5: Strain effect in an $Al_xGa_{1-x}N$/GaN hetero-structure

tride) is grown on the top of GaN layer. As III-N semiconductor, such as AlN, GaN, and InN possess different lattice constants under unstrained conditions. The lattice constant of an unstrained $Al_xGa_{1-x}N$ layer is different than the unstrained GaN. Thus, when $Al_xGa_{1-x}N$ layer is grown on the top of GaN layer, $Al_xGa_{1-x}N$ layer is strained to match the lattice constant of an underlying GaN layer. The direction of growth in III-N is parallel to c-axis, which is normal to the basal plane {0001}. Also, c-axis and basal plane {0001} are represented by z-axis and xy-plane, respectively, as shown in Fig. 2.5. Since lattice constant of $Al_xGa_{1-x}N$ and GaN layers need to match, there exists strain in x and y directions, which is expressed as

$$\epsilon_1 = \frac{a - a_0}{a_0} \tag{2.4}$$

where, the lattice constants of an unstrained (relaxed) and a strained structure are represented by a_0 and a, respectively. Generally, GaN layer is thicker than $Al_xGa_{1-x}N$ layer and, it assumed that the former is relaxed, while the latter is strained. Therefore, the Eq. 2.4 is modified as

$$\epsilon_1 = \frac{a(0) - a(x)}{a(x)} \tag{2.5}$$

Here, $a(0)$ is the lattice constant of unstrained (relaxed) GaN layer and $a(x)$ is the lattice constant of $Al_xGa_{1-x}N$, which is the function of *Al* mole-fraction x in the layer.

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The piezoelectric polarization in wurtzite crystal is expressed as mentioned below [42].

$$P_{i,PZ} = \sum_{jk} d_{ijk}\sigma_{jk} = \sum_{jk} d_{ijk}\left(\sum_{lm} C_{jklm}\varepsilon_{lm}\right) = \sum_{lm} e_{ilm}\varepsilon_{lm} = \sum_{lm} e_{ilm}\left(\sum_{lm} S_{lmjk}\sigma_{jk}\right) \quad (2.6)$$

where, d, σ, C, ε, e and S are piezoelectric moduli, stress, elastic constant, strain, piezoelectric constant, and elastic compliance, respectively. The variables in the above equation are related with each other in the following manner.

$$e = d \cdot Cd = e \cdot SS = C^{-1} \quad (2.7)$$

Moreover, piezoelectric polarization does not depend on microscopic structure unlike spontaneous polarization [43], and piezoelectric polarization of any ternary alloy is evaluated using Vergard's law.

$$P_{PZ,A_xB_{1-x}N} = xP_{PZ,AN}(\varepsilon(x)) + (1-x)P_{PZ,BN}(\varepsilon(x)) \quad (2.8)$$

The polarization induced charge density, σ, which originates at hetero-interface of two dissimilar III-Ns, is associated with the gradient of polarization [44], i.e, $\sigma = \nabla P$. For $Al_xGa_{1-x}N$/GaN hetero-interface, the above equation can be rewritten as mentioned below.

$$\begin{aligned} \sigma &= P_{GaN} - P_{AlGaN} \\ &= P_{SP,GaN} + P_{PZ,GaN} - P_{SP,Al_xGa_{1-x}N} - P_{PZ,Al_xGa_{1-x}N} \\ &= P_{SP}(0) + P_{PZ}(0) - P_{SP}(x) - P_{PZ}(x) \end{aligned} \quad (2.9)$$

The argument x in the above mentioned equation is the mole fraction of Al in $Al_xGa_{1-x}N$. As GaN layer, in general, is thicker than $Al_xGa_{1-x}N$ layer, it is considered relaxed i.e., $P_{PZ}(0) = 0$. Since $Al_xGa_{1-x}N$ layer is grown on the top of GaN layer, it is assumed that it is strained due to their lattice mismatch. However, this is not true in all the scenarios. When the lattice constants of two layers exceed a threshold point, the top layer ($Al_xGa_{1-x}N$, here) grows partially in the relaxed state. It holds for $Al_xGa_{1-x}N$ layer having higher composition of Al [39]. Similarly,

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for lower mole fraction, x of Al in $\mathrm{Al_xGa_{1-x}N}$, $P_{SP,Al_xGa_{1-x}N} \approx P_{PZ,Al_xGa_{1-x}N}$. Further, it is to mention that for higher x, $P_{PZ,Al_xGa_{1-x}N}$ drops. If x attains a very high value, then $P_{SP,Al_xGa_{1-x}N}$ is the main contributing factor in the polarization process. Thus, for very high x, the polarization induced charge density at the hetero-interface is due to P_{SP} of the two layers. On the other hand, $\mid P_{SP,Al_xGa_{1-x}N} \mid$ is greater than $\mid P_{SP,GaN} \mid$, which results in a positive charge at the $\mathrm{Al_xGa_{1-x}N}$/GaN hetero-interface. This is exhibited in Fig. 2.6 for the ready reference.

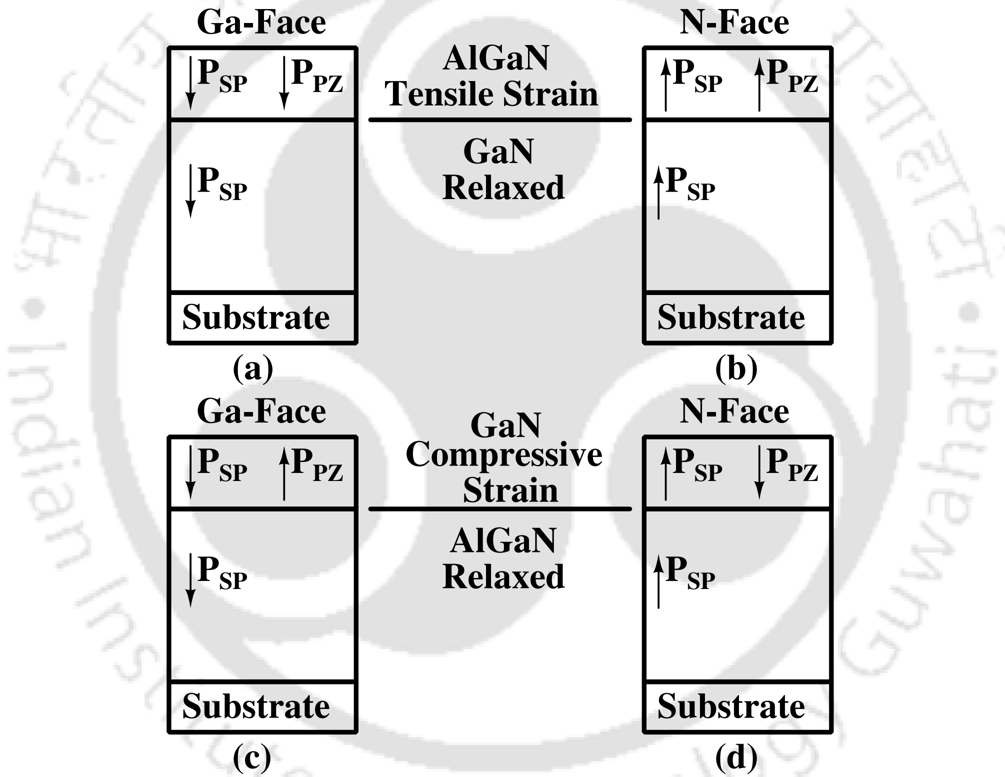

Figure 2.6: Polarization field condition for a thin AlGaN layer under tensile strain for (a) Ga-face, and (b) N-face, respectively. As the thickness of AlGaN layer is increased and GaN layer is reduced, the GaN layer experiences compressive strain for (c) Ga-face and (d) N-face.

2.4 Two Dimensional Electron Gas (2DEG)

In a hetero-junction, when two materials with different bandgaps are brought in the contact, band bending at hetero-interface takes place, which results in the formation of a narrow quantum well with high electron density known as two dimensional electron gas (2DEG). At

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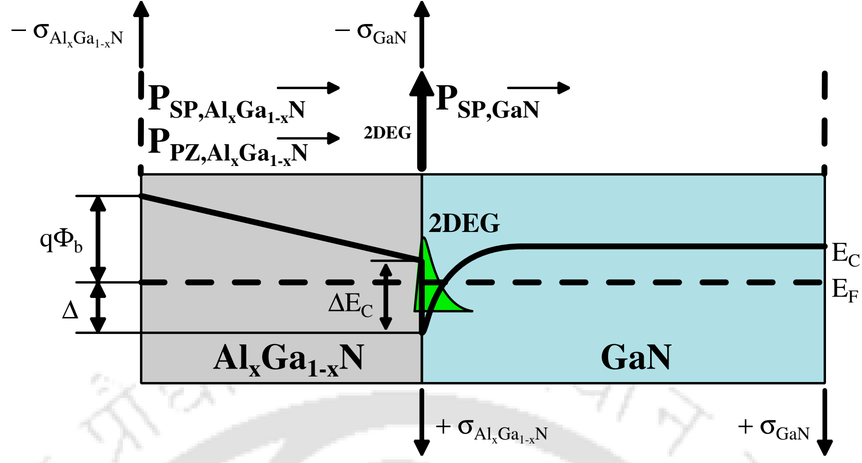

Figure 2.7: The vertical cross-section of the conduction band in AlGaN/GaN hetero-structure.

$Al_xGa_{1-x}N$/GaN hetero-interface, donor electrons from $Al_xGa_{1-x}N$ diffuse to GaN due to difference in the electron affinity (χ), bandgap (E_g) and work function (ϕ) of $Al_xGa_{1-x}N$ and GaN. This process of electron transfer halts, when an equilibrium condition is reached, i.e Fermi level becomes constant across the hetero-junction as shown in Fig. 2.7.

Owing to large difference in the polarization at hetero-structure interface, there exists bounded charges, σ_b, which results into high electron sheet density, n_{2D}. It is also referred as 2DEG. The dependency of n_{2D} on the barrier height ϕ_b is represented as [45, 46] and is stated below for completeness.

$$n_{2D}(x,d) = \frac{\sigma_b(x)}{e} - \frac{\varepsilon_0\varepsilon(x)}{e^2 d}\left(e\phi_b(x) + \Delta(x) - \Delta E_C(x)\right) \tag{2.10}$$

Here, ΔE_C, ε_0 and ε are the conduction band offset, vacuum's dielectric constant, relative dielectric constant of the barrier layer, respectively. Further, Δ is conduction band penetration below the Fermi level at the $A_xB_{1-x}N$/GaN interface (A and B can be either Al, Ga or In), which is dependent on the mole fraction, x and is expressed as mentioned below.

$$\Delta(x) = \left(\frac{9\pi\hbar e^2}{8\varepsilon_0\sqrt{8m_n^*}}\frac{n_{2D}(x,d)}{\varepsilon(x)}\right)^{2/3} + \frac{\pi\hbar^2}{m_n^*}n_s(x,d) \tag{2.11}$$

In the next section, details of AlGaN/GaN HEMT are provided briefly.

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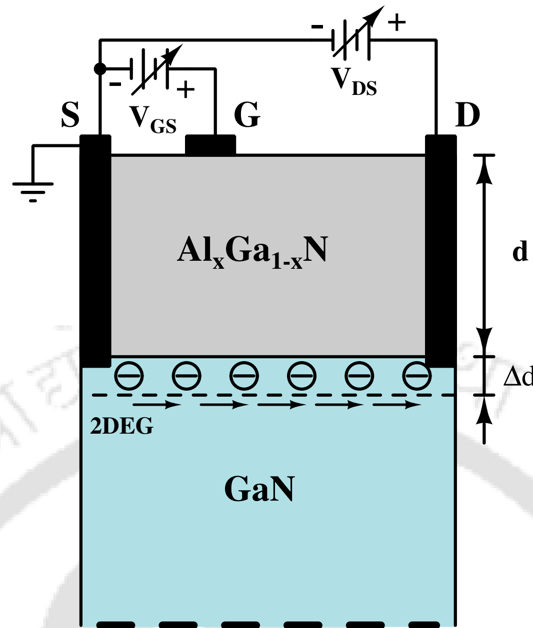

Figure 2.8: Schematic structure of a HEMT device (not to the scale). Here, $\triangle d$ represents the position of maximum 2DEG at the interface in a HEMT device

2.5 AlGaN/GaN HEMT

The High Electron Mobility Transistor (HEMT) works on the similar principle of a Field Effect Transistor (FET). The current flows between source and drain terminals through the channel, which is created because of potential well in the hetero-structure region. This potential well possesses high density of electrons, which form 2DEG. The movement of 2DEG is restricted to the direction parallel to the interface. The initial HEMTs were fabricated with GaAs, because arsenide based devices do not exhibit spontaneous and piezoelectric polarization as compared to the nitride based devices. The magnitude of 2DEG in the former device is lower than the latter one. The 2DEG density in GaAs based HEMTs can attain 2 $\times 10^{12}$ cm^{-2} with doping, while 2DEG density in GaN based HEMTs can achieve upto the order of $\times 10^{13}$ cm^{-2} without any doping. It is to mention that doping reduces electron mobility in GaAs based HEMTs due to scattering.

The schematic of GaN-based HEMT device is shown in Fig. 2.8, where gate is placed asymmetrically i.e., distance of source and drain contact is not equally spaced. The rationale

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behind this asymmetric placement of the gate is as follows. The electric field peaks at drain edge of the gate when drain voltage is high, thus gate must be placed at a larger distance from drain. This increase in distance between gate and drain contacts reduces cut-off frequency and high frequency performance of the device.

The current flow between the drain and source contacts, i.e., I_D is regulated by the voltage at gate contact. It can be expressed as a function of n_{2D} (2DEG carrier density), and the voltage along the lateral direction $V(x)$ as stated in [47].

$$I_D = W_G q n_{2D}(x)\mu_n \left(\frac{\partial V(x)}{\partial x}\right) \tag{2.12}$$

where, μ_n is electron mobility in the channel and W_G is width of the gate.

On integrating the above equation from $x = 0$ to $x = L_G$ (drain side of gate edge), drain current, I_D, can be expressed as

$$I_D = \frac{\varepsilon \mu_n W_G}{(d+\Delta d)L_G}\left\{(V_{GS} - V_T)\, V_{DS} - \frac{V_{DS}^2}{2}\right\} \tag{2.13}$$

For small drain to source voltage, V_{DS}, electron velocity is proportional to the electric field given by $\upsilon_n = \mu_n E$. When electric field increases beyond a threshold, electron velocity reaches to a saturation velocity ($\upsilon_{n,sat} = \mu_n E_S$), which further saturates I_D. Drain current, I_D is denoted by $I_{D,Sat}$ at after electron velocity attains the peak value, i.e. drain saturation current and equation 2.13 gets modified as stated below.

$$I_{D,Sat} = \frac{\varepsilon \mu_n W_G E_S}{d+\Delta d}\left\{\sqrt{(V_{GS} - V_T)^2 + E_S^2 L_G^2} - E_S L_G\right\} \tag{2.14}$$

Here, E_S is the electric field at which electron velocity attains peak value. The drain saturation current expression for shorter gate HEMTs, i.e., $L_G < (V_{GS} - V_T)/E_S$ is as follows.

$$I_{D,Sat} = \frac{\varepsilon W_G \upsilon_{n,sat}}{d+\Delta d}(V_{GS} - V_T) \tag{2.15}$$

From, the equation 2.15, it can be observed that $I_{D,Sat}$ varies linearly with V_{GS}. The

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constant term can be denoted as transconductance, g_m, which can be expressed by equation 2.16.

$$g_m = \frac{\varepsilon W_G v_{n,sat}}{d + \Delta d} \tag{2.16}$$

Hence, drain saturation current, $I_{D,Sat}$ can be expressed as

$$I_{D,Sat} = g_m (V_{GS} - V_T) \tag{2.17}$$

For a HEMT device, it is equally essential to explore substrate, which is outlined in the subsequent Section 2.6.

2.6 Choice of Substrate

The introduction of wide bandgap devices into systems depends generally on affordability, availability, large diameter and high quality. The following properties are taken into consideration while evaluating substrates for semiconductor devices [48].

- Lattice-mismatch relative to the materials of device layers
- Thermal conductivity κ_L and thermal expansion coefficient (CTE)
- Maximum electrical isolation at different temperatures
- Total price and price per unit area
- Availability with respect to the diameter (2-8 in.)
- Crystal quality and residual defect density
- Surface properties and residual defects density
- Wafer warp and wafer bowing
- Mechanical and chemical properties with respect to thinning and via hole etching

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The commonly used substrates for AlGaN/GaN HEMTs are Silicon, Sapphire, and Silicon Carbide. Diamond, and GaN are also used as substrates. The main advantage of the former is high thermal conductivity, which is helpful in heat dissipation that generates during device operation. On the other hand, the latter aids in reducing density of impurities. The heat flow in AlGaN/GaN HEMT is governed by the equation described below.

$$c_L \frac{\partial T}{\partial t} = \overrightarrow{\nabla} \cdot \left(\kappa_L \overrightarrow{\nabla} T \right) \tag{2.18}$$

where, c_L, κ_L, and H are lattice heat capacity, thermal conductivity and heat generation rate, respectively. The thermal conductivity, heat capacity for Si, GaN, and SiC are enlisted in Table 2.2. For Sapphire (Al_2O_3), the thermal conductivity, heat capacity are 0.35-0.42 ($Wcm^{-1}K^{-1}$) [25, 49], and 0.77 ($Jg^{-1}K^{-1}$), respectively, [25]. A brief about Silicon Carbide, Sapphire, and Silicon is stated below for completeness.

2.6.1 Silicon Carbide

The lattice mismatch between SiC and GaN is 4%, and due to its better thermal conductivity, it is the most attractive substrate. The density of dislocation is less than 3×10^8 cm^{-2} provided an AlN nucleation layer is placed between SiC and GaN, which ensures excellent crystallographic quality. Although SiC is expensive, devices made with this substrate exhibits higher frequency.

2.6.2 Sapphire

Sapphire (Al_2O_3) is the most commonly used substrate as it is easily available and cheap. However, the lattice match between GaN and Sapphire ranges between 14% - 23% depending on their relative orientation. One of the prominent issue with this material is the poor thermal conductivity, which hinders heat dissipation and may results in overheating the device.

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Table 2.2: Comparison of material parameters of semiconductors w.r.t Gallium Nitride [10]

Parameter	Symbol	Unit	Si	GaN	SiC	Diamond
Crystal structure	–	–	Diamond	Hexagonal, Cubic	Hexagonal, Cubic	Diamond
Lattice constant	–	A°	5.43	Hex 3.189/a, 5.185/c, cubic 4.52	(6H)3.086/a, 15.117/c, (4H) 3.073/a, 10.053/c, (3C) 4.3596/a, 3.073/c	3.567
Specific heat	–	$Jg^{-1}\ {}^{\circ}C^{-1}$	0.7	0.431	0.2	0.52
Thermal conductivity	–	$Wcm^{-1}\ {}^{\circ}C^{-1}$	1.5	2.1	2.3-4.9	6-20
Transition type	–	–	Indirect	Direct	Indirect	Indirect
Bandgap energy	E_g	eV	1.12	3.39(H)	3.02/6H, 3.26/4H, 2.403/3C	5.46-5.6
Dielectric constant	ϵ_r	–	11.7	12	10.0 (6H), 9.7 (4H)	5.7
Electron affinity	χ	eV	4.05	3.4	4	NEA
Electron mobility	μ_e	$cm^2V^{-1}s^{-1}$	1500	1000	460-980	2200
Hole mobility	μ_h	$cm^2V^{-1}s^{-1}$	450	~ 5	20	1800
Lattice matching	–	–	$\sim$ SiGe	$\sim$ SiC, Sapphire	$\sim$ GaN, 1N	–

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2.6.3 Silicon

Silicon has a reasonable thermal conductivity and is economically viable. The lattice constant of Si is larger than GaN with lattice mismatch at 17%. As a result, GaN layer grown over it has tensile stress, which creates crystal defects at the interface. With the employment of this substrate, we can harness the advantages of both the technologies, i.e., Si and GaN technology to build integrated circuits (ICs) comprising Si MOSFETs and GaN HEMT in the same chip [50].

Although HEMT devices depicts superior performance, these devices are too vulnerable to initiate degradation mechanisms. Some of the degradation mechanisms are stated in Section 2.7.

2.7 Challenges

In this section, device degradation, such as self heating, current collapse and thermal boundary resistance are stated.

2.7.1 Self heating

Owing to the high electron mobility, saturation currents in GaN HEMTs can reach as high as 2–3 A/mm [51]. At such high currents, there is a significant Joule heating effect in the transistor [52]. Although gallium nitride has higher thermal stability [53] as compared to silicon, the heating effect causes mobility of electrons in 2DEG to drop, which further reduces current [51] and hinders prolonged use of GaN HEMTs. The detailed analysis of heating effect reveals that the temperature rise is mainly concentrated at the drain side of the gate edge, where formation of thermal hotspots can be found [54]. As a result of the temperature rise, drop in electron mobility occurs at this point [55]. The temperature rise in the device can be seen as a linear function of Drain-Source voltage and decrease in the device current can be estimated using negative slope of I-V characteristics.

Self-heating results in the decrease of mobility and saturation velocity of electrons, causing

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significant performance degradation. Even the failure rate of GaN-HEMTs is linked with peak temperature in the device. The failure of GaN-HEMTs can be caused by temperature and field dependent phenomena. However, it is generally accepted that temperature dominates on almost all the phenomena responsible for performance degradation. Hence, for ensuring reliable operation and mitigating the chances of time-dependent or device failure, GaN-HEMTs are usually mandated to operate below "safe" levels of power, current and temperature. The maximum permissible channel temperature, T_{MAX}, not only determines the maximum power delivering capability and expected life of the device, but it also plays a crucial role in the design of heat sinks, device packaging, etc. [56]. Therefore, self-heating is extremely important for the prediction of device performance, assessment of lifetime and reliability, system design, etc. Two out of the above mentioned three parameters determining the device "safe" operation region, i.e. output power and current, can be easily measured, but the determination of temperature distribution across the device [57] and identification of hotspots are not easy.

In order to determine lattice temperature equation 2.25 can be utilized. A number of effective solutions to tackle self-heating problem have been proposed in the literature. Notable among these are: (a) altering the substrate material to improve heat dissipation [58]; (b) employing heat sink layers in the device made up of good thermal conductors, such as nanocrystalline diamond [59] etc.; (c) using an exterior heat sink over the entire chip [60] and (d) depositing a quilt-like structure over the entire transistor [61].

2.7.2 Current Collapse

Current collapse denotes the phenomenon where current degrades with an increase in the dynamic resistance and is depicted as a mismatch between output power measured at DC and RF conditions. It is also referred as current compression, current slump or DC/RF dispersion as shown in Fig. 2.9. This leads to the reduction of RF gain of the device, output RF power, dynamic transconductance [62, 63] and device efficiency in the high frequency regime. The existence of traps at the surface, in the buffer or in the barrier layer plays an important role in current collapse.

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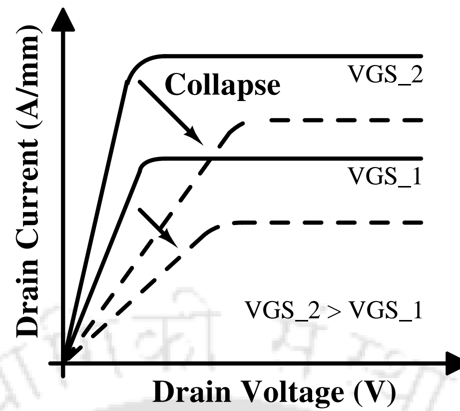

Figure 2.9: Pictorial representation of I_D vs V_D characteristics for AlGaN/GaN HEMT devices (*solid line* and *dotted line* represents before and after the current collapse, respectively)

To better understand the phenomenon of current collapse, the concept of virtual gate modeling can be employed [64]. The explanation of device behavior (trapping mechanism) under the influence of gate bias is shown in Fig. 2.10. For an applied negative bias gate voltage (Fig. 2.10(b)), which is below the pinch–off voltage (region A), the peak high electric field induced in the device occurs at the gate edge toward the drain. This leads to the leakage of electrons that fills ionized donor states (on the surface) close to gate electrode, as a result the surface potential becomes negative and channel underneath depletes. The negative surface potential extends the depletion region and behaves as a virtual gate.

In region B, as the gate bias starts becoming positive, the channel under gate electrode must appear (turn–on), but virtual gate effect hinders the quick response (Fig. 2.10(c)). The delay in response to the applied gate bias depends on the detrapping process of the surface traps. Even though gate bias is positive, the drain region is depleted and contains low carrier concentration.This makes drain region to behave as a highly resistive region and majority of the applied potential appear across here, which results in the low drain current.

However, eventually after some period of time (region C), the captured electrons are emitted from the trap and this helps drain current to reach steady state (Fig. 2.10(d)). Therefore, when electric field is sufficiently high, it fills surface traps, which makes the response of the device slow. Thus, a certain time is required for the device to obtain the maximum drain current, which

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determines feasibility of high frequency operation. When a device is operated in the pulsed bias condition, influence of trapping and detrapping is quite evident. The trapping phenomenon depends on the applied quiescent bias, while detrapping is observed during turn on pulse. The current collapse phenomenon affects the high power switching applications as well as degrades RF performance of the device. The gradual increase in the resistance of drain access region and knee voltage contributes to the power dissipation even in switched OFF conditions. There are various methods proposed in the literature to mitigate the issue of current collapse, such as surface passivation and the introduction of field plates [2, 65]. While surface passivation helps in the optimal dielectric semiconductor interfacing to prevent filling of surface traps, field plates distribute the electrical field over drain access region, thereby, shifting the peak electric field from the gate edge facing the drain side.

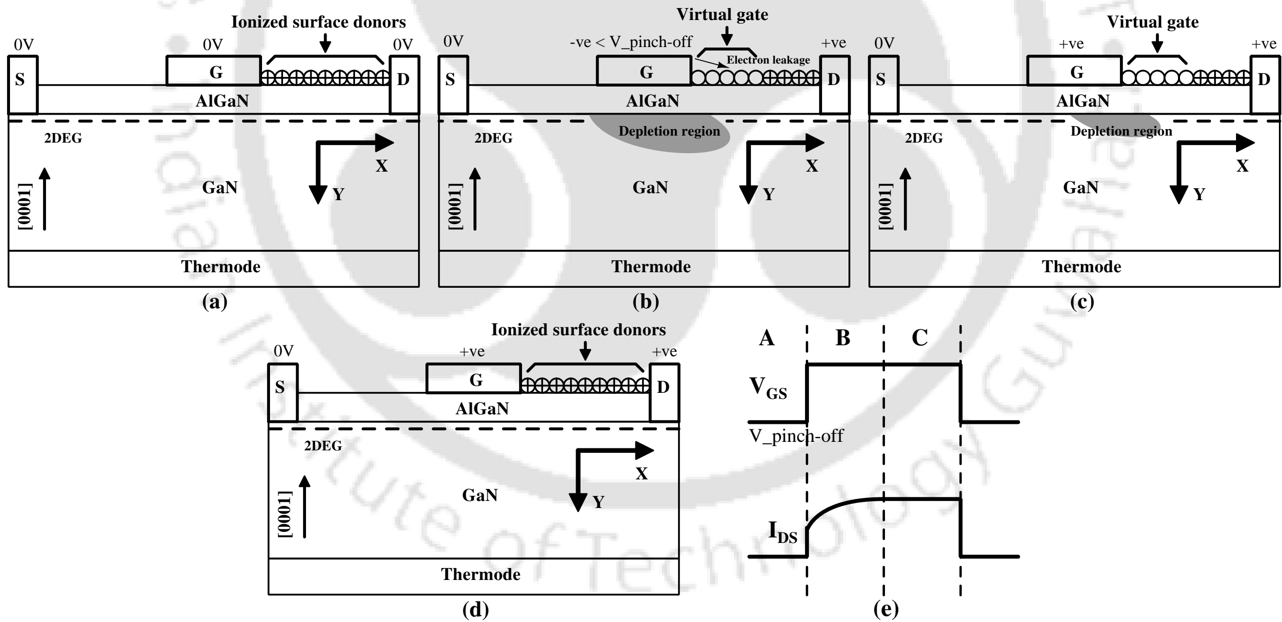

Figure 2.10: Current collapse phenomenon (with trap behavior) for the bias conditions: (a) Zero bias condition; (b) Negative bias condition (below pinch–off) (Region A); (c) Positive bias (Region B); (d) when the device is completed turned-on (Region C) and (e) Timing diagram for different regions (bias) of device operation

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2.7.3 Thermal Boundary Resistance

The heat flowing from one material to the another has to face thermal resistance at the interface. This resistance, which opposes heat flow, is referred as thermal boundary resistance (TBR). One of the approaches to model heat flow at the interface is through electrical equivalent circuit. In this electrical equivalent circuit, TBR can be treated as analogous to an electrical resistance. As resistance in an electrical circuit opposes current flow, similarly TBR resists heat flow from one material to the another. This resistance can lead to the accumulation of heat in the region, where it is generated. Raising the device temperature, which leads to the accelerated degradation of a HEMT, causes its failure. The thermal boundary resistance at the interface depends mainly on the growth conditions, hence, it can vary between samples from one manufacturer to another. Therefore, the proper TBR must be known apriori to design simulation framework to estimate device performance. If TBR is not known, then it can be evaluated numerically using Diffused mismatch model. This model takes into account the phonon behavior at the interface to evaluate TBR [66, 67]. From simulation perspective, TBR needs to be incorporated at all the interfaces as well as at the thermal contacts (points, which can be set to maintain a fixed temperature) of a HEMT, which enables thermal simulations to project a realistic device temperature and heat accumulation. A simulator generally ignores TBR, if it is not provided and in that case, the heat map turns out to be unrealistic leading to improper designs. Since the AlGaN layer is thin, hence, the thermal conductivity may change [68] and it becomes imperative to add TBR in the numerical analysis framework.

In the subsequent section, preliminary information on numerical analysis is depicted in short for completeness.

2.8 TCAD simulation

Technology computer-aided design (TCAD) refers to the use of computer simulations to develop and optimize semiconductor processing technologies. TCAD tools aids in minimizing time and funds invested in the early research and development phase of semiconductor device.

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Table 2.3: A complete list of tools available in Sentaurus TCAD (2016 Version)

Framework	Process Simulation	Device Creation	Device Simulation
Sentaurus Workbench	Sentaurus Process	Sentaurus Structure Editor	Sentaurus Device
Calibration Kit Inspect Optimizer Sentaurus Data Explorer Sentaurus Visual Tecplot SV Utilities	Advanced Calibration for Process Simulation Sentaurus Topography Sentaurus Topography 3D	Sentaurus Mesh	Advanced Calibration for Device Simulation Sentaurus Device Electromagnetic Wave Solvers Sentaurus Device Monte Carlo Solvers

It also assist in optimizing electrical, physical and processing technology of a semiconductor device. There are various software available in the research domain, which incorporate industry standard device processes and other associated tools. Synopsys Sentaurus TCAD is one of the popular TCAD platform. Its popularity is primarily due to the powerful graphic user interface, which helps in efficient coordination of simulation tasks and analyzing the results. Synopsys Sentaurus TCAD hosts a number of tools, such as process simulation, device simulation, interconnect simulation, workbench, structure editor and calibration etc. With these tools, a broad range of device analyses, such as complementary metal-oxide-semiconductor field effect transistor (CMOSFET), fin-shaped field effect transistor (FinFET), power devices, memory devices, image sensors, solar cells and analog/RF devices can be performed. The detailed list of all the available tool is stated below in Table 2.3. Also, the Sentaurus TCAD tool flow is depicted in Fig. 2.11 for the reference.

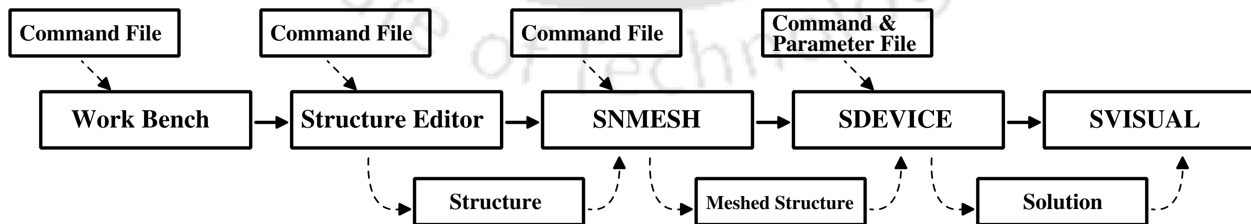

Figure 2.11: The typical flow among the tools/application in Sentaurus

This section explores the commonly used physical models in numerical analysis briefly.

2.8.1 Fermi Statistics

The Fermi statistics is represented as mentioned below.

$$n = N_c F_{1/2}\left(\frac{E_{f,n} - E_c}{k_B T}\right) \tag{2.19}$$

$$p = N_v F_{1/2}\left(\frac{E_v - E_{f,p}}{k_B T}\right) \tag{2.20}$$

where, n and p stand for concentration of electrons and holes, respectively. N_c and N_v represent density of states in conduction and valence band, respectively. $E_{f,n}$ and $E_{f,p}$ denote fermi levels of electrons and holes, whereas, $F_{1/2}$ is the fermi integral of order 1/2. The Fermi statistics cannot be activated in localized region of a device, thus if this model is activated, it applies to the entire device region.

2.8.2 Drift Diffusion Transport Model

The drift-diffusion model is used as carrier transport model. The current densities of electrons and holes are given by following mathematical expressions.

$$\overrightarrow{J_n} = \mu_n(n\nabla E_C - 1.5nk_B T\nabla \ln m_n) + D_n(\nabla n - n\nabla \ln \gamma_n) \tag{2.21}$$

$$\overrightarrow{J_p} = \mu_p(p\nabla E_V + 1.5pk_B T\nabla \ln m_p) - D_p(\nabla p - p\nabla \ln \gamma_p) \tag{2.22}$$

Here, the notations have usual meaning. The drift-diffusion model has a good convergence rate, but in certain situations other models are required to visualize situations like self-heating (thermodynamic). It is to mention that as a first hand approach, the drift-diffusion model provides a quick and a fairly accurate result with proper meshing.

2.8.3 Thermodynamics Model

In the thermodynamics model, temperature gradient as a driving term is included as mentioned below.

$$\overrightarrow{J_n} = -nq\mu_n(\nabla\Phi_n + P_n\nabla T) \tag{2.23}$$

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$$\overrightarrow{J_p} = -pq\mu_p(\nabla\Phi_p + P_p\nabla T) \tag{2.24}$$

Here, P_n and P_p are absolute thermoelectric powers for the carriers and T represents lattice temperature. The temperature is estimated by using equations for lattice temperature estimation as explained in Eq. (2.25).

$$\frac{\partial}{\partial t}(c_L T) - \nabla\cdot(k_L \nabla T) = -\nabla\cdot[(P_n T + \Phi_n)\overrightarrow{J_n} + (P_p T + \Phi_p)\overrightarrow{J_p}] - \frac{1}{q}\left(E_C + \frac{3}{2}k_L T\right)(\nabla\cdot\overrightarrow{J_n} - qR_{net,n}) - \frac{1}{q}\left(-E_V + \frac{3}{2}k_L T\right)(-\nabla\cdot\overrightarrow{J_p} - qR_{net,p}) + \hbar\omega G^{opt} \tag{2.25}$$

Here, k_L andc_L are thermal conductivity and lattice heat capacity, respectively. E_C and E_V are conduction and valence band energies, respectively. G^{opt} is optical generation rate due to photons. The RHS of the above mentioned equation is equal to the total heat, H. If the stationary case is considered, then the second and third terms can be ignored and Eq. (2.25) can be expressed as shown by Eq. (2.26).

$$H = -\nabla\cdot[(P_n T + \Phi_n)\overrightarrow{J_n} + (P_p T + \Phi_p)\overrightarrow{J_p}] + \hbar\omega G^{opt} \tag{2.26}$$

The solution to lattice temperature equation, when solved along with the current density equation, manifests a more realistic lattice temperature distribution and a carrier transport model that incorporates self-heating in the device. The thermodynamic physics requires a lots of computing power and convergence can also be an issue. Hence, proper selection of accompanying models are very important for accurate analysis of a device.

2.8.4 Shockley–Read–Hall Recombination Model

The recombination phenomenon can be represented as stated below.

$$R^{SRH} = \frac{np - n_{i,eff}^2}{\tau_p(n + n_1) + \tau_n(p + p_1)} \tag{2.27}$$

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where,

$$n_1 = n_{i,eff} exp\left(\frac{E_{trap}}{k_B T}\right) \tag{2.28}$$

$$p_1 = n_{i,eff} exp\left(\frac{-E_{trap}}{k_B T}\right) \tag{2.29}$$

where, E_{trap} is the difference between defect level and intrinsic level. The doping dependence on SRH lifetimes is modelled with Scharfetter relation described below.

$$\tau_{dop}(N_{A,0} + N_{D,0}) = \tau_{min} + \frac{\tau_{max} - \tau_{min}}{1 + \left(\frac{N_{A,0}+N_{D,0}}{N_{ref}}\right)^{\gamma}} \tag{2.30}$$

2.8.5 Thermionic Emission Current Model

The transport model for hetero-structure interface needs to be treated differently as conventional transport model ceases to be valid at hetero-junction interface. Currents and energy fluxes at this abrupt interface between two materials are better defined by an interface condition at the hetero-junction.

Let us consider that materials 1 and 2 form hetero-interface and the conduction edge jump is positive, that is $\Delta E_C > 0$, where $\Delta E_C = E_{C,2} - E_{C,1}$ (that is, $\chi_1 > \chi_2$). If $J_{n,1}$ and $S_{n,1}$ are electron current density and electron energy flux density leaving out of the material 1, respectively, and $J_{n,2}$ and $S_{n,2}$ are the electron current density and electron energy flux density entering into the material 2, respectively, then the interface condition can be represented as [69] mentioned below.

$$J_{n,2} = J_{n,1} \tag{2.31}$$

$$J_{n,2} = a_n q \left[v_{n,2} n_2 - \frac{m_{n,2}}{m_{n,1}} v_{n,1} n_1 \text{exp}\left(-\frac{\Delta E_C}{k_B T_{n,1}}\right)\right] \tag{2.32}$$

$$S_{n,2} = S_{n,1} + \frac{c_n}{q} J_{n,2} \Delta E_C \tag{2.33}$$

$$S_{n,2} = -b_n \left[v_{n,2} n_2 k_B T_{n,2} - \frac{m_{n,2}}{m_{n,1}} v_{n,1} n_1 k_B T_{n,1} \text{exp}\left(-\frac{\Delta E_C}{k_B T_{n,1}}\right)\right] \tag{2.34}$$

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where, $v_{n,i}$ stands for emission velocities, which is defined as

$$v_{n,i} = \sqrt{\frac{k_B T_{n,i}}{2\pi m_{n,i}}} \tag{2.35}$$

2.8.6 Mobility Model

Mobility of the carrier needs to be modelled appropriate for proper simulation of terminal current. In general, mobility is a function of lattice temperature. However, there are several other parameters that determines the mobility of the carriers. For the scenario, when more than one mobility model is considered for a carrier type, the overall mobility due to this models (μ_1, μ_2, ...) for bulk, surface mobility, and thin layers is given by Matthiessen's rule:

$$\frac{1}{\mu} = \frac{1}{\mu_1} + \frac{1}{\mu_2} + \cdots \tag{2.36}$$

For the proposed work, in this thesis, the mobility of the carriers is modelled as doping dependent, degradation at interfaces, and high-field saturation (velocity saturation) at high electric field. Arora model [70] is utilized to simulate doping-dependent mobility which is expressed as

$$\mu_{dop} = \mu_{min} + \frac{\mu_d}{1 + \left(\left(N_{A,0} + N_{D,0}\right)/N_0\right)^{A^*}} \tag{2.37}$$

where,

$$\mu_{min} = A_{min} \cdot \left(\frac{T}{300\ K}\right)^{\alpha_m}, \qquad \mu_d = A_d \cdot \left(\frac{T}{300\ K}\right)^{\alpha_d} \tag{2.38}$$

and

$$N_0 = A_N \cdot \left(\frac{T}{300\ K}\right)^{\alpha_N}, \qquad A^* = A_a \cdot \left(\frac{T}{300\ K}\right)^{\alpha_a} \tag{2.39}$$

Further details can be referred from [68, 70]. In the channel region, the high transverse electric field forces, carriers are subjected to scattering by acoustic surface phonons and surface roughness. To account into this effect, the Lombardi model [71] is included. The surface contribution due to acoustic phonon scattering is represented as

$$\mu_{ac} = \frac{B}{F_\perp} + \frac{C\left(\left(N_{A,0} + N_{D,0} + N_2\right)/N_0\right)^{\lambda}}{F_\perp^{1/3}\left(T/300\ K\right)^{k}} \tag{2.40}$$

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and the contribution due to surface roughness scattering is given by

$$\mu_{sr} = \left(\frac{(F_{\perp}/F_{ref})^{A^*}}{\delta} + \frac{F_{\perp}^3}{\eta} \right)^{-1} \tag{2.41}$$

Necessary details can be found in [68, 71]. In addition, the carrier drift velocity is observed to be longer proportional to the electric field, instead, the velocity saturates to a finite speed v_{sat} at high electric field. This phenomenon is modelled with Canali model [72] which is expressed as

$$\mu(F) = \frac{(\alpha + 1)\,\mu_{low}}{\alpha + \left[1 + \left(\frac{(\alpha+1)\mu_{low} F_{hfs}}{v_{sat}}\right)^{\beta}\right]^{1/\beta}} \tag{2.42}$$

Here, μ_{low} stands for the low-field mobility. The parameter β is temperature dependent defined as

$$\beta = \beta_0 \left(\frac{T}{300\ K} \right)^{\beta_{exp}} \tag{2.43}$$

Other details can be referred from [68, 72, 73].

2.8.7 Avalanche Generation

The generation of electron-hole pair due to avalanche generation (impact ionization) requires a threshold field strength and the possibility of acceleration, that is, wide space charge regions. When the width of the space charge region is greater than the mean free path between two ionizing impacts, charge multiplication can take place, which may results in electrical breakdown. The reciprocal of the mean free path is known as the ionization coefficient, α . van Overstraeten–de Man model is invoked to realise this physical phenomenon. This model is based on the Chynoweth law [74] and represented as

$$\alpha(F_{ava}) = \gamma a\ exp \left(-\frac{\gamma b}{F_{ava}} \right) \tag{2.44}$$

where,

$$\gamma = \frac{tanh\left(\frac{\hbar\omega_{op}}{2kT_0}\right)}{tanh\left(\frac{\hbar\omega_{op}}{2kT}\right)} \tag{2.45}$$

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The factor γ together with the optical phonon energy $\hbar\omega_{op}$ represents the temperature dependence of the phonon gas against which carriers are accelerated. The details on coefficients a, b, $\hbar\omega_{op}$, and others can be found in [68, 75].

2.8.8 Tunneling

In current semiconductor devices, tunneling has become a very important physical effect. In some cases, tunneling leads to undesired leakage currents. To model the tunneling effect at Schottky contacts, heterostructures, the nonlocal tunneling model is invoked. In general, 'electron tunneling' to the conduction band at the lower point on the line originates from the conduction band at the upper point, $j_C = j_{CC}$. Likewise, the tunneling to the valence band at the lower point originates from the valence band at the upper point, $j_V = j_{VV}$ (that is, 'hole tunneling'). The contribution to the electron tunneling current density by electrons that tunnel from the conduction band at points above l to the conduction band at point l is the integral over the recombination rate

$$\frac{dj_{CC}}{dl}(l) = -q\sum_{v}\int_{l}^{\infty}\int_{-\infty}^{\infty}\left[R_{CC,v}(u,l,\epsilon) - G_{CC,v}(u,l,\epsilon)\right] d\epsilon du \tag{2.46}$$

Additional details can be found in [68].

2.8.9 Traps

Traps originates due to various reasons, primarily due to dislocations, material defects formed during growth of the crystal, lattice mismatch between layers of two materials, variance in thermal expansion coefficients of substrate and epilayer(s), presence of dangling bonds on the surface and impurities within the crystal lattice [76–78]. Traps can be classified into two types, donor-like and acceptor-like traps. A trap, which is positive while unoccupied and neutral when filled with electron is a donor-like trap. Similarly, a trap, which behave as neutral while unoccupied and negative when occupied is an acceptor-like trap.

Nallatamby et al. [79] stated the relationship between cross section of trap σ_n/σ_p and capture probability of electron/hole, c_n/c_p as described below.

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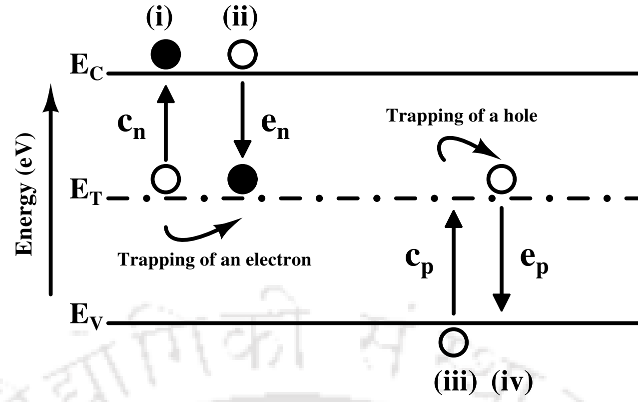

Figure 2.12: Trapping of electron and holes

$$c_n = \sigma_n \upsilon_{thn} \tag{2.47}$$

$$c_p = \sigma_p \upsilon_{thp} \tag{2.48}$$

Also, electron (hole) emission probability, e_n (e_p) is related to their corresponding capture probability as [79],

$$e_n = c_n N_C F_{1/2}\left(\frac{E_T - E_C}{k_B T}\right) \tag{2.49}$$

$$e_p = c_p N_V F_{1/2}\left(\frac{E_V - E_T}{k_B T}\right) \tag{2.50}$$

where, the effective densities of states of electron and holes are represented as N_C and N_V, respectively. Conduction and valence band energies are denoted as E_C and E_V, respectively, and the Fermi function of order 1/2 can be described as $F_{1/2}$.

$$\upsilon_{th} = \left(\frac{3k_B T}{m^*}\right)^{1/2} \tag{2.51}$$

In the Fig. 2.12, the four possible events of generation/recombination mechanism for a single level traps (at E_T) is shown [79, 80].

(i) When an electron is captured by an empty trap from the conduction band, which is stated

in terms of capture probability coefficient c_n and electron recombination rate R_n as,

$$R_n = c_n n N_T(1 - f_t) = c_n n p_t \tag{2.52}$$

(ii) Similarly, when the emission of an electron takes place from the trap energy level to the conduction band, it is stated in terms of emission probability e_n and emission generation rate G_n as,

$$G_n = e_n N_T f_t = e_n n_t \tag{2.53}$$

(iii) Further, when a hole is captured by an occupied trap from the valence band, which is related in terms of capture probability coefficient c_p and hole recombination rate R_p as,

$$R_p = c_p p N_T f_t = c_p p n_t \tag{2.54}$$

(iv) When a hole emits from the empty trap to the valence band with a hole emission probability coefficient e_p and hole generation rate G_p,

$$G_p = e_p N_T(1 - f_t) = e_p p_t \tag{2.55}$$

Here, N_T stands for the total number of traps and n_T represent the number of occupied traps. Moreover, the generation-recombination rate is stated below [79].

$$U = \frac{\partial n_t}{\partial t} = N_t \frac{\partial f_t}{\partial t} = (R_n - G_n) - (R_p - G_p) \tag{2.56}$$

$$\frac{\partial n_t}{\partial t} = N_t \left[c_n n(1 - f_t) + e_p(1 - f_t) - e_n f_t - c_p p f_t\right] \tag{2.57}$$

The occupation probability of generation-recombination centres (in steady state conditions) is given by following mathematical expression.

$$\frac{\partial n_t}{\partial t} = N_t \frac{\partial f_t}{\partial t} = 0; \tag{2.58}$$

$$f_{steady} = \frac{c_n n + e_p}{c_n n + e_n + c_p p + e_p} \tag{2.59}$$

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2.8.10 Basic Heat Equations

Understanding the heating effect in the semiconductor devices is quite essential, as it defines the overall performance of the device at high power device operation. With reference to the simulation, there are basically two major concerns. First, we need to figure out the overall temperature distribution profile using all the potential heat sources. In order to address this issue, we must take into account the heat flow through the substrate. Secondly, it is imperative to evaluate degradation of the performance of the device due to the distribution of heat. Our objective is to provide a thermal modeling environment, which considers all probable temperature dependencies.

It is to mention that for the simplification of device analysis, we first consider the heat flux followed by the heat source. The heat power flux J_h (in Watt/m^2) as a function of thermal conductivity can be defined as stated below.

$$\overrightarrow{J_h} = -\kappa_L \overrightarrow{\nabla} T \tag{2.60}$$

Energy conservation dictates that thermal distribution fulfils the basic thermal equation.

$$C_p \rho_m \frac{\partial T}{\partial t} = -\overrightarrow{\nabla} \cdot \overrightarrow{J_h} + H \tag{2.61}$$

or,

$$C_p \rho_m \frac{\partial T}{\partial t} = -\overrightarrow{\nabla} \cdot \kappa_L \overrightarrow{\nabla} T + H \tag{2.62}$$

where, C_p, ρ_m and H are specific heat, density of the material and the heat source, respectively.

2.9 Summary

In this chapter, basic properties of III-N semiconductor is discussed. The polarization in III-N is one of the main feature that has influence on the operation of these devices. The difference in polarization at the interface leads to formation of quantum well with high concentration

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of electron, commonly referred as 2DEG. Subsequently, the basic structure and working of AlGaN/GaN HEMT is elaborated. Further, the importance of selection of proper substrate is highlighted. In the second section of this chapter, an overview of TCAD numerical analysis and basic models employed thereof is described in brief. In the next chapter, we outline different milestones achieved by scientific community in the proposed area of research.

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3
Prior Art

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3.1 Introduction

In this chapter, we present key observations made by researchers in connection with the reliability and degradation mechanisms of HEMTs.

Mark J. Rosker stated that "While excellent performance is being shown routinely, the greatest challenge has been, and remains, achieving a high level of reliability and stability concurrently with high-performance operation [21]." Therefore, a better understanding of failure mechanisms of GaN HEMTs is required, which is a major challenge given the peculiarities of material imperfection, the stability of fabrication processes and the physics of GaN devices [81].

3.2 First Principles

Khan et al. [82] were the first to observe enhanced mobility in single and multiple GaN/Al_x $Ga_{1-x}N$ hetero-junction devices. The increased mobility is attributed to enhanced interfacial conduction due to the formation of two dimensional electron gas (2DEG) at the interface. The electron mobility of a single hetero-junction consisting of 500 A° of $Al_{0.09}Ga_{0.91}N$ on the top of 0.3 μm of GaN was around 620 cm^2/Vs at room temperature as compared to 56 cm^2/Vs for bulk GaN of the same thickness deposited under identical conditions. Electron mobilities as high as 1980 cm^2/Vs and charge densities of 1.5×10^{14} cm^{-3} at 77 K were reported for multichannel GaN/$Al_{0.15}Ga_{0.85}N$ structures. These structures were deposited on the basal plane sapphire using low-pressure metal organic chemical vapour deposition method. In continuation to their initial work, Khan et al. [83] demonstrated the first ever fabrication and DC characterization of n-GaN-$Al_{0.14}Ga_{0.86}N$ hetero-junction HEMT. The transconductance measured at the room temperature was 28 mS/mm for a device with 10 μm source to drain spacing, gate length of 4 μm and gate width of 50 μm at gate voltage of +0.5 V. Further, the transconductance increased to 46 mS/mm at 77 K. The complete pinch-off of the device was observed at gate bias = -6 V.

Karmalkar et al. [2] investigated the enhancement of breakdown voltage (V_{br}) with the implementation of field plate technique in AlGaN/GaN HEMTs as shown in Fig. 3.1 for detailed structure and electric field distribution. Parameters controlling the field distribution under field

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plate was presented in [2]. 2D simulation was performed to determine the maximum breakdown voltage with least on-resistance and frequency response degradation. It was observed that V_{br} increased significantly as dielectric constant of the insulator beneath the field plate surged. Additionally, field plate improved V_{br} by a factor of 2.8–5.1 based on the 2DEG concentration and dielectric constant of the insulator. For instance, V_{br} increased from 123 V to 630 V for HEMT with the following configuration; 2.2 μm field plate on 0.8 μm silicon nitride and gate to drain separation of 4.7 μm with 2DEG = 1×10^{13} cm^{-2}.

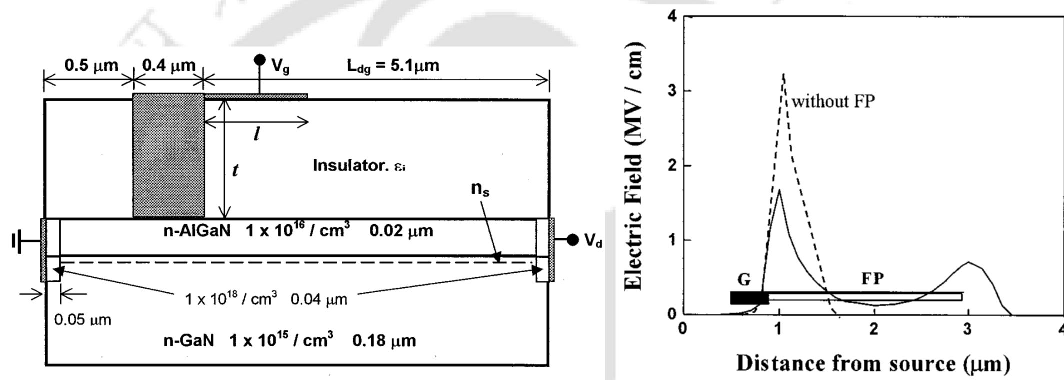

Figure 3.1: Field Plate HEMT structure, and Electric field distribution along the channel of HEMT with and without a field plate [2]

Sadi et al. [49] investigated thermal droop in the drain current characteristics and device temperature peak dependency on the bias condition and substrate material. Electrothermal Monte Carlo method was employed to investigate electron transport coupled with the heat diffusion equation. The investigation was carried out using devices grown on the substrate, such as Si, Sapphire, SiC, and GaN. The polarization effect was included in the numerical simulation to model its influence on the electron transport and creation of 2DEG. It was observed that a higher 2DEG density translated to better current handling capability in the device, which further increased thermal effect in a device. The electrothermal characteristics of the devices grown on the sapphire substrate demonstrated a significant reduction in the current with very high peak temperature, which concluded that sapphire was not an ideal candidate for high-power applications. Devices grown on SiC substrate was observed to have lowest peak temperature as compared to device grown on Si, sapphire and GaN substrates.

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The maximum reduction of drain current of the device using sapphire was 64% as compared to 12% reduction in the device using SiC. However, devices with GaN demonstrates a slight better thermal behaviour than Si, hence it exhibits second best device in the thermal performance among the substrates under consideration.

Vitanov et al. [84] proposed modification to the existing hydrodynamics mobility model, which aided in matching AC and DC characteristics of AlGaN/GaN HEMTs experimentally by employing Monte Carlo (MC) simulation. The proposed modified hydrodynamic model with $\beta = 1.2$ and $\alpha = -0.5$ is illustrated below. Additional details can be found in [84].

$$\mu^{LIT} = \frac{\mu^{LI}(T_n/T_L)^{\gamma}}{(1+\alpha^{1/\beta}(T_n - T_L)^{1/\beta})^{\beta}}, \text{ where } \alpha = \frac{3\kappa_B \mu^{LI}}{2q\tau_{\varepsilon}(\nu_{sat})^2}$$

Pei et al. [85] reported slant field plate AlGaN/GaN HEMTs with reduced DC-RF dispersion and parasitic capacitance. The proposed prototype exhibited excellent millimetre wave power density of 4.9 W/mm with a power-added efficiency of 45% at 30 GHz at $V_{ds} = 30V$.

Heller et al. [86] performed simulation incorporating hydrodynamics transport and thermal diffusivity equations. In this model, it was observed that heat was generated in the region, where electrical field is typically high, i.e. near the drain edge of the gate as electrons are thermalized at high electric field. A significant difference was observed during numerical analysis with deep traps. In the case of hydrodynamics simulations, hot electrons thermalized and diffused into deep traps in the GaN layer at a high drain voltage, whereas, for the drift diffusion model, it was in the entire layer between gate and drain.

Wang et al. [87] carried out 2-D numerical simulation to investigate DC characteristics of a double channel AlGaN/GaN HEMTs with the help of drift diffusion, thermodynamics, hydrodynamics and hot electron models. The experimental results were in the close agreement with the results obtained using numerical analysis incorporating hydrodynamics model. The hot electron model predicted a uniform reduction in drain saturation current, which indicated the onset of negative differential conductance (NDC) in the output characteristics of the device. However, self heating effect incorporated in the hydrodynamics model resulted in non-uniform

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reduction in the drain saturation current, which was an realistic approximation of NDC. Hence, it can be concluded that self heating is responsible for NDC.

3.3 Degradation Mechanism

Meneghesso et al. [30] investigated failure modes and mechanisms of AlGaN/GaN HEMTs. The hypotheses on the failure modes were validated by 2-D device simulations. The test results resembled close correlation between failure modes and bias condition. Measurement techniques, such as Electroluminescence (EL) and spectroscopy as a powerful failure analysis tool were employed to evaluate the effects of hot carrier in AlGaN/GaN HEMTs. Degradation was observed to be of maximum magnitude, when the device was in the SEMI-ON state, which was validated by electroluminescence (EL) measurements.

The device degradation is categorized into two regimes, i.e., at moderate drain bias ($V_{DS} <$ 30 V), device degradation is due to hot-electron effects, while at the high drain bias ($V_{DS} >$ 30–50 V), device degradation is triggered by gate leakage current. This is due to inverse piezoelectric effect, which leads to defect generation, and/or to localized permanent breakdown of AlGaN layer. The degradation mechanism can be categorized broadly into three groups [3]. Various degradation mechanisms are shown in Fig. 3.2 for completeness.

(i) Degradation mechanisms triggered due to hot electrons in SiN passivation layer or semiconductor material that generates lattice defects.

(ii) Degradation mechanisms at the gate edge due to reverse-bias and the generation of traps due to high stress conditions. This degradation mechanisms affect the properties of AlGaN/GaN hetero-structure.

(iii) Thermally-activated degradation mechanisms, which includes degradation of metal interconnections, ohmic contacts, gate metal and de-lamination of the passivation layer.

Alamo et al. [88] reviewed experimental evidences of failure mechanisms in GaN HEMTs due to electrical stress. They have listed some of the aspects of degradation mechanism below.

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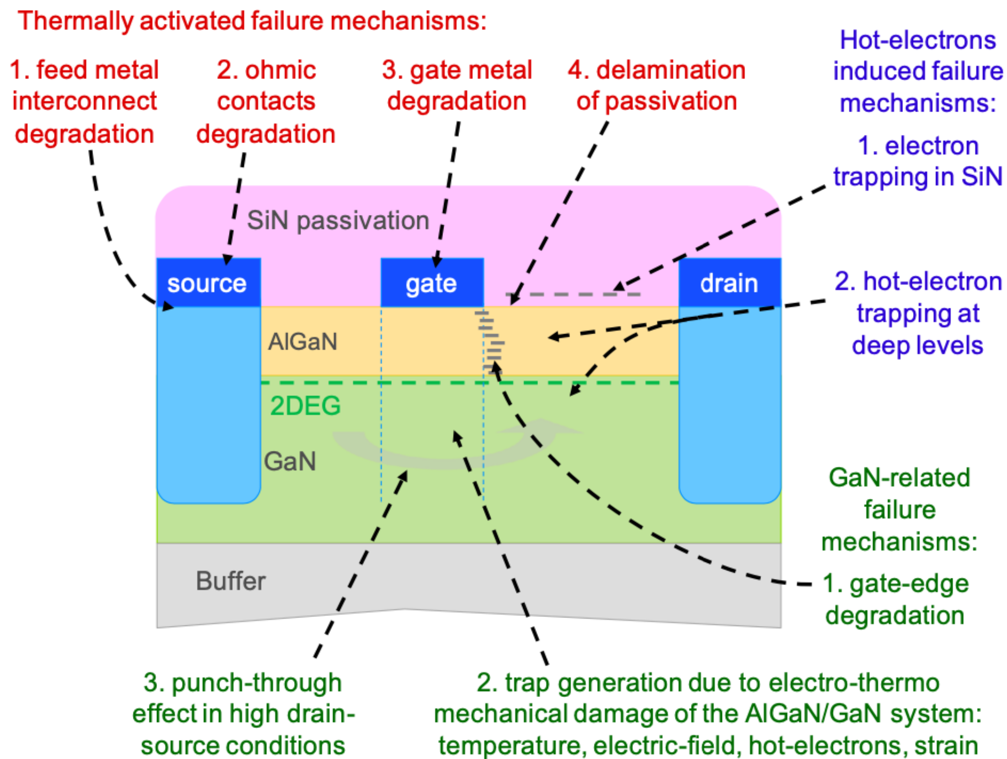

Figure 3.2: Critical areas where degradation may occur in a AlGaN/GaN HEMT [3]

- The degradation mechanism is an electric field driven mechanism, which produces mechanical stress through inverse piezoelectric effect. In particular, vertical electric field plays a key role, while horizontal electrical field does not contribute to the degradation mechanism. This is because of the horizontal electric field, which does not increase elastic energy significantly.

- The degradation happens only after a critical voltage. Degradation is unlikely to take place, unless elastic energy in AlGaN layer attains its critical value. For instance, elastic energy relaxes with the formation of crystalline defects, when AlGaN layer is grown beyond a certain thickness.

- Current in a device does not play a direct role, however, it is responsible for indirect heating of the lattice, which is likely to intensify the problem.

- In a normal operating condition, electrical defects are expected to be on the drain side as

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it is the high-field region of the device.

- Under normal operating condition, for a transistor with short gate length, gate-to-source voltage has an impact on the critical voltage. This is due to the influence of gate-to-source voltage on the electric field profile of a device on the drain side.
- If mechanical strain is applied, there is an enhancement of elastic energy in AlGaN layer. As a consequence, critical voltage either increases or decreases based on its sign.
- Any change in the initial elastic energy in AlGaN layer directly affects degradation, such as composition and thickness of AlGaN and material quality. In addition, strain and composition of the buffer layer and an AlN layer in the barrier too affects degradation.
- Device designs, such as field plates, slanted gates and gate corner rounding that address mitigation of electric field also improve reliability of the device.

The above hypothesis suggests several paths to enhance electrical reliability of GaN HEMTs, which are borne out of experimental observations.

Kuball et al. [4] proposed a methodology based on electroluminescence and UV assisted electrical trapping analysis to understand trap generation during off and on states induced stress in AlGaN/GaN HEMTs. The lateral and vertical electron trap locations in the device, and nature of degradation mechanism were identified in this analysis. The traps were generated with activation energy (0.45 - 0.65 eV) near the gate edge toward the drain side as a result of stress. The importance of diffusion process in the device degradation was studied by subjecting the device in different backplate temperature regimes. Diffusion constant indicated thermal activation energies of $\sim$ 0.26 eV for diffusion along dislocations, possibly due to additional contributions from bulk diffusion, which was accelerated by converse/inverse piezoelectric strain and leakage currents. The diffusion related degradation is shown in Fig. 3.3 [4]. The probability of dislocation near the gate edge and along its width is statistically high given the dislocation density in III-N grown on SiC substrates is $10^8 - 10^9$ cm^{-2}. The diffusion along dislocation

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forms the lowest energy pathway (Fig. 3.3(a)). This is the starting point of degradation, which is further accelerated by electric field, converse piezoelectric strain and the gate leakage current. As diffusion constants for impurities in bulk AlGaN or GaN is smaller than diffusion constant of diffusion of dislocations, the diffusion of impurities in the former is less likely than the latter. However, the large converse piezoelectric strain in the AlGaN layer near the gate edge toward the drain side assists in the diffusion of impurities (Fig. 3.3(b)). This opens up crystal planes for impurities to diffuse more easily. This creates a scenario, wherein AlGaN and GaN material modification and surface/interface degradation take place. Similarly, impurity transport leads to the generation of defect clusters during stress. The transport of material in a diffusion process assists the formation of pits (Fig. 3.3(c)), therefore such degradation are considered as severe device degradation.

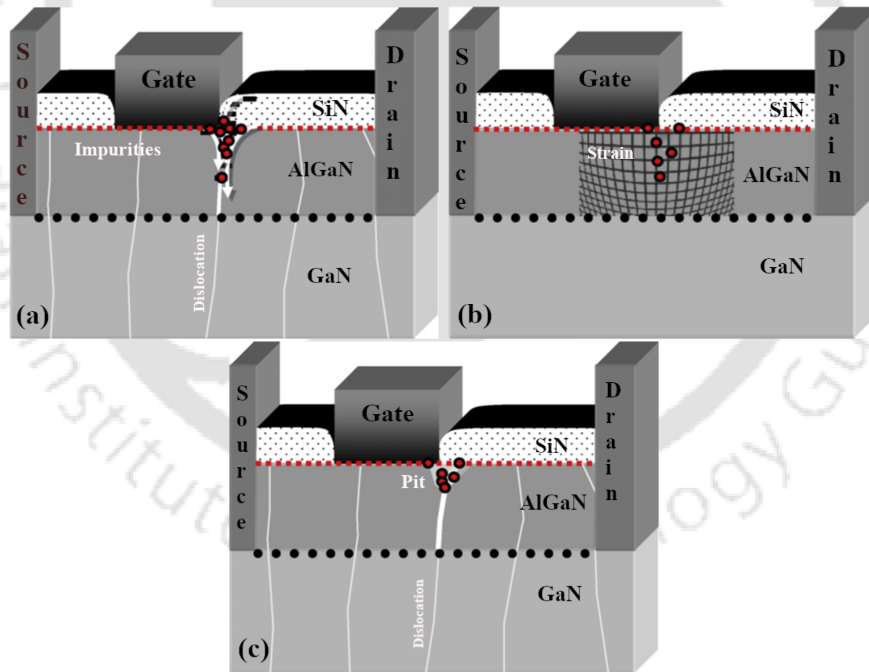

Figure 3.3: Schematic of possible diffusion related degradation mechanisms of AlGaN/ GaN HEMTs: (a) diffusion along dislocations, (b) diffusion enhanced by converse/ inverse piezo-electric strain (corresponding diffusion enhancement can also be achieved via gate leakage current and electric fields) and (c) pit or crack formation following a prior diffusion process. By diffusion we denote here processes which in the more advanced device degradation stage also include electro-chemical reactions [4]

Ancona et al. [89] presented a fully coupled multi-dimensional continuum model consisting

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of governing equations, such as linear thermoelectroelasticity, diffusion-drift transport theory, and heat conduction. The model includes "actual" device geometries and takes into consideration the field and stress concentration near the material discontinuities and at the corners. The electrical and mechanical degradation mechanisms in GaN HEMTs were discussed in [89] including inverse piezoelectric effect, thermal stress, SiN intrinsic stress, electron injection and device geometry. Additionally, the slant field gate structure and its property of mitigation of electric field at the gate corner was presented. It is observed that the slant gate design helps in spreading the electric field in the vicinity of gate edge, which reduces gate current and mitigates hot carrier damage, and increases breakdown voltage. The possibilities of crack propagation and fracture of the AlGaN were also analyzed in this work.

The primary advantage of InAlN/GaN HEMTs is higher electron concentration (three times) than AlGaN/GaN HEMTs. This is due to higher spontaneous polarization and absence of piezoelectric polarization in InAlN/GaN unlike piezoelectric polarization in AlGaN/GaN hetero-structure, which results into tensile strain in AlGaN barrier layer. Beside, InAlN and GaN is lattice matched, which enhances robustness against electromechanical related degradation. Tapajna et al. [90] investigated hot electron temperature in InAlN/GaN HEMTs using electroluminescence spectroscopy. The experimental hot electron temperature was found to be correlated with hot electron distribution obtained using hydrodynamics simulation. The peak localized temperature up to 30000 K at drain voltage of 30 V was observed, which had been found to be 2-3 times higher than that of AlGaN/GaN HEMTs. Channel degradation was observed when device was stressed in the SEMI-ON state. Moreover, the consequence of such high temperature is the increase in trap density in the channel region and surface/interface traps in gate-to-drain access region.

Zhu et al. [91] investigated $In_{15.7\%}Al_{84.3\%}N$/AlN/GaN hetero-junction field effect transistors under electrical stress for four different bias conditions, namely, on-state-low-field stress, reverse-gate-bias stress, off-state-high-field stress and on-state-high-field stress, to understand hot electron/phonon and thermal effects. The drain current and noise spectral density (NSD)

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of a device for the four different bias conditions were correlated with the location and nature of degradation. It can be corroborated that dominant degradation is caused by hot phonon and hot electron effects and is primarily located in the channel. Trap generation around the gate edge takes place, when the device is under reverse-gate-bias stress, which has an indirect influence on the channel. When the device is under off-state-high-field stress, the source to drain voltage is quite high, which results into hot electrons. These hot electrons start leaking along the channel and generating trap states in the channel, which causes reduction in channel conductivity (drain current) and increase in NSD.

Wang et al. [92] investigated the performance of AlGaN/GaN HEMT having diamond heat spreader layer. The thermal and electrical characteristics of the device was extracted using a finite element method. The observation indicates that the performance of device improves with an optimal heat spreading. Heat spreading depends on the lateral thermal conductivity of the diamond layer restricted to its initial few micrometers. The prominence of diamond layer in the device under pulse operation is observed, when the diamond layer is in close proximity to the heat source. Devices with diamond layer of thickness 5 μm exhibit 10.5% improvement in the drain current and self-heating effect can be neglected for 100 ns pulse width at 20 V drain voltage and 1 V gate voltage.

Faramehr et al. [93] investigated the trapping and de-trapping of the carriers in AlGaN/GaN HEMT with the help of 2-D TCAD transient simulation. To study the trapping and de-trapping processes in the device, gate and drain pulse techniques were implemented with hydrodynamics and diffusion transport models. Additionally, coupled electrical and thermal simulations were carried out to predict electron temperature in the channel, and model the exchange of energy between carriers and the lattice. The electrical stress due to traps (donor and acceptor) leads to the degradation of drain current. The degradation in the current level is observed as 5% and 75% for bulk and surface traps, respectively. The numerical simulation has a good agreement with the experimental results of the effects of bulk and surface traps on the current transient. Fig. 3.4 depicts the possible location of the traps in an AlGaN/GaN HEMT, namely, (1) at

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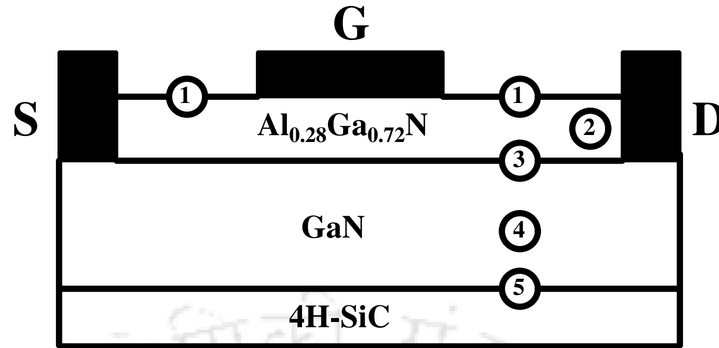

Figure 3.4: Possible trap locations in GaN HEMTs

Table 3.1: Trapping and de-trapping processes in a AlGaN/GaN HEMT

Type of Trap	Donor	Acceptor	Process
Empty Trap	Positively charged	Neutral	Trapping
Occupied Trap	Neutral	Negatively charged	De-trapping

the interface of semiconductor and dielectric, (2) in the barrier layer, (3) at the interface of barrier and channel, (4) in the buffer layer, and (5) at the interface of substrate and buffer. The process of trapping and de-trapping in an AlGaN/GaN HEMT is enlisted in Table 3.1.

Saito et al. [5] investigated breakdown mechanism of high-voltage GaN-HEMT and analysed it using experimental I–V characteristics and 2D simulation, which employed impact ionization and tunnelling model for realising avalanche breakdown, gate and substrate currents. The possible leakage path in the device is shown in Fig. 3.5. Although, the gate current dominated the drain current at low drain voltage below 600 V, rapid increase of gate current was not observed at the breakdown. It is verified that the gate current do not trigger device breakdown. On the other hand, at high drain voltage over 600 V, the substrate current increased rapidly and simultaneously with the source current. It is to mention that the breakdown basically occurs when source current increases after the increase of substrate current. The holes generated by impact ionization under high applied voltage accumulates beneath gate, which lowers gate potential barrier. As a result, source leakage current increases rapidly resulting into device breakdown. From this discussion, it is concluded that suppression of impact ionization is imperative for highly reliable device design as far as device breakdown is concerned.

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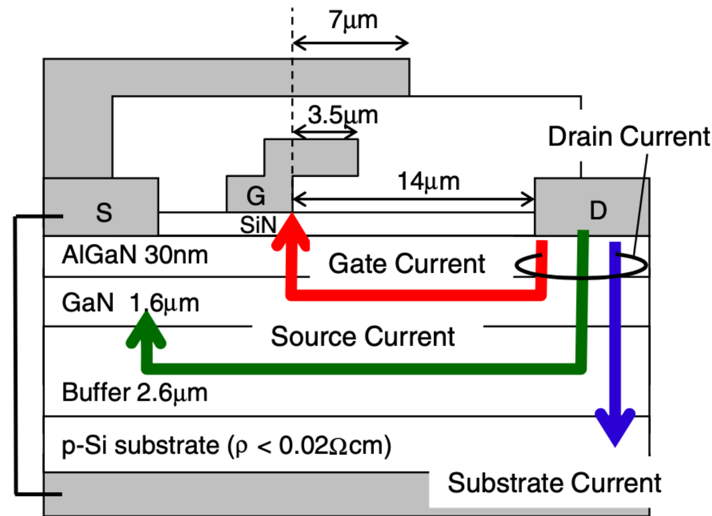

Figure 3.5: Cross-sectional structure of GaN-HEMT and current paths in the off-state depicting three types of leakage current path in the device [5]

Zhang et al. [94] investigated the use of p-diamond as back barrier (BB) and cap layer for the enhancement of performance in AlGaN/GaN HEMTs. It was observed that p-diamond back barrier and cap layer compensate 2DEG in the OFF-state. Complementary to GaN, diamond offers a heavily doped p-type layer. The p-diamond back barrier and cap layer enable uniform distribution of electric field with higher breakdown voltage of the device. Additionally, p-diamond cap layer is expected to reduce electron trapping in AlGaN and GaN layer, which is critical for high power devices. Besides, p-diamond cap layer is known to have a large modulation effect on the devices, such as breakdown voltage and on-resistance. It is found that the breakdown voltage increases by ~ 3.5 times, but the on-resistance also enhances by $\sim 12\%$, when p-diamond cap layer extends from gate towards drain. The investigation was performed with self-consistent electrothermal simulations. It was also found that the improvement of thermal performance in the device was due to the diamond surface heat spreaders.

Zhang et al. [95] proposed an innovative recessed float field plate (RFFP) structure for millimetre-wave AlGaN/GaN HEMTs. Field plates, such as source field plates (SFP) or gate field plates (GFP) are well-known for their ability to suppress electric field and improvement in breakdown voltage with changing electric field distribution near drain end of the gate. Although

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power density of 13.7 W/mm and power added efficiency (PAE) of 55% were obtained with T-gate field plate structure, introduction of field plate increased parasitic capacitances, which resulted into lower f_T, and f_{MAX} of the device. f_T, f_{MAX} and P_{RF} are expressed below for the reference. It can be said that mm-wave devices with shorter source-to-drain (L_{SD}) and gate length (L_G) are highly vulnerable to parasitic capacitances, C_{gs}, C_{gd}.

$$P_{RF} = \frac{I_{max}(V_{br} - V_{knee})}{8}$$

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

$$f_{max} \cong \frac{f_T}{2\sqrt{(R_i + R_S + R_g)g_0 + (2\pi f_T)R_g C_{gd}}}$$

The proposed RFFP enhances potential of modulating E-field without any increment in the parasitic capacitances. The reduced peak electric field aided in increasing breakdown voltage of RFFP GaN HEMTs with L_{GD} = 1.35 μm to 122–140 V, which was found to be higher than the breakdown voltage 84–101 V reported in the literature. The current collapse characteristic was also improved significantly. Additionally, no obvious increase in the parasites capacitance was observed after integrating novel RFFP, while maintaining high frequency performance of GaN HEMTs.

Murugapandiyan et al. [96] investigated breakdown characteristics of $Al_{0.295}Ga_{0.705}N/GaN$ HEMTs with $Al_{0.04}Ga_{0.96}N$ blocking layer and gate field plate technique. Devices with L_G = 0.4 μm and 0.8 μm SiN passivation exhibited $I_{DS,max}$=2.16 A/mm at V_{GS} = 2 V. The breakdown voltage of HEMT is investigated for various field plate lengths i.e. L_{FP} = 1, 1.25, 1.5, 1.75, and 2 μm during the numerical analysis. The maximum breakdown voltage, V_{br}=871 V, and JFoM=34.88 THz-V were estimated in a device with gate-field plate length (L_{FP}) = 1.75 μm. Device using high-k passivation HfO_2 layer with an identical structure was also studied. This device shows an enhanced V_{br}=912 V with JFoM=25.53 THz-V. These results indicate that the proposed $Al_{0.295}Ga_{0.705}N/GaN/Al_{0.04}Ga_{0.96}N$ double hetero-junction (DH) HEMTs are suitable

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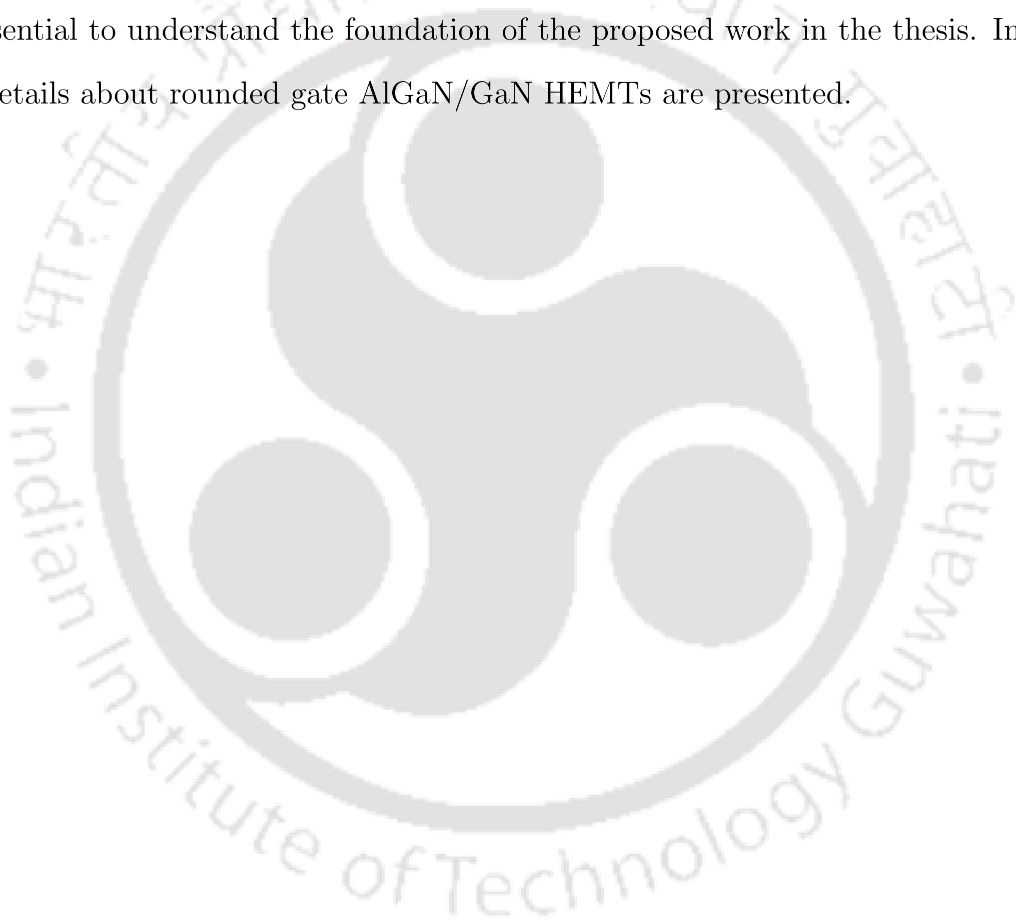
devices for the next-generation high-power microwave applications.

3.4 Summary

In this chapter, few of the pivotal observations in the scientific community that generated tremendous interest for AlGaN/GaN HEMT is stated. Further, the elemental information about degradation mechanism in AlGaN/GaN HEMT is presented along with some findings. This is essential to understand the foundation of the proposed work in the thesis. In the next chapter, details about rounded gate AlGaN/GaN HEMTs are presented.



4

Numerical Investigation of Rounded Gate Device

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4.1 Introduction

AlGaN/GaN High Electron Mobility Transistors (HEMT) are best known for their superiority in operating at elevated voltage and temperature along with outstanding integrity in handling high-frequency signals [34, 81, 97]. GaN being an important member of III–V semiconductor group finds its application in optoelectronic, high-power and high frequency device technologies [98–100]. This ability of AlGaN/GaN HEMT is primarily due to the large bandgap, high critical electric field and high carrier saturation velocity of the materials involved [101,102]. AlGaN/GaN HEMTs are normally-ON devices as 2DEG (2 Dimensional Electron Gas) naturally forms at the AlGaN/GaN interface due to polarization [39]. However, a normally-OFF operation is achieved by gate recess [103], fluorine implantation [104], and the inclusion of additional layer like InGaN, SiN_x [105, 106] etc. The performance of these devices are affected by the leakage current [107], which lowers the device breakdown voltage and can lead to its early breakdown [108]. This issue can be addressed by using a thicker buffer layer, which is doped with either Iron (Fe) or Carbon (C) [109–111].

The potential of AlGaN/GaN HEMT technology cannot be realized until reliability aspect is probed and enhanced. As the majority of degradation phenomenon originates in the gate edge of these devices, modifications in the rectangular gate geometry can be one of the alternatives to address this issue [112–115]. We postulate that mitigation of electric field at the gate edge can suppress degradation mechanisms. In this work, a detailed analysis for rounded gate AlGaN/GaN HEMT with and without field plate is presented. The reliability aspects are studied by evaluating the electric field profile, leakage current, electron temperature (eTemperature), and capacitance–voltage characteristics (CV). Pei et al. [85] emphasizes that reduction in peak electric field and parasitic capacitance leads to increase reliability of sub-μm AlGaN/GaN HEMTs. The proposed research work exhibits the impact of above mentioned factors on the device reliability by varying gate geometry along with simulatenous introduction of field–plates in the device structure. Field plate is usually implemented to scale down electric field in the drain access region. Several configuration are reported in the literature, such as

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gate field plate [2, 116–119], source-connected field plate [120–122], and drain-connected field plate [123–126]. Although field plate design exhibits high breakdown voltage due to electric field modulation at the gate, however a negative aspect of lateral/gate connected field plate design is that it increases Miller capacitance. Moreover, lateral scaling is limited in gate connected field configuration [2, 127, 128] as it hinders the ON–state performance of a device [119, 129]. It is worth mentioning that RF performance of the device degrades with scaling down as Miller capacitance dominates in the devices having field plate. Although CV characteristics of GaN-based Metal Oxide Semiconductor (MOS) HEMT (normally-OFF HEMTs) is presented in the literature [130–138], it is also imperative to understand CV characteristics of a normally-ON HEMT for reliability perspectives.

In this work, we primarily discuss key degradation mechanism in a device and introspect into the following approaches to increase the reliability of AlGaN/GaN HEMT devices.

- We propose alteration in gate geometry of HEMT (so called rounded gate device). To examine benefits of this approach in the performance of a device, device characteristics, namely, current-voltage (I–V) characteristics (transfer characteristics and output characteristics), leakage current, electric field profile along the channel, eTemperature profile, breakdown voltage, capacitance–voltage characteristics for rounded gate devices are observed.

- Field plate technology is widely implemented, and various configurations of field plates are reported in the literature. The proposed work focuses on examining the effect of field plates in rounded gate devices and its impact on the device reliability by studying their electrical characteristics.

Our major contribution in this work is the implementation of rounded gate device, and a well planned investigative study of the device structure to understand the reliability and performance aspect. Although, gate shape engineering (slant gate) is well known for enhancing of device performance, this work explores a particular rounded gate edge, which is unique. It is

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essential to investigate rounded gate edge for the device reliability on the context of gate–shape engineering, and an attempt is made in this work to carry out an investigative study. With this study, reliability and performance aspect of rounded gate shape geometry by analyzing electric field profile, eTemperature profile, current–voltage characteristics, breakdown voltage, and capacitance–voltage are presented.

It is to mention that the work presented in this chapter is an investigate study to gain new insights into the device behaviour as gate shape changes. There are numerous findings, in which device dimension, such as gate length and gate-to-drain spacing are based on the device application, viz. RF, HV or LV switching. However, it is necessary to note the fact that researchers carry out such investigative study without any conformity to any of device application as reported by Song et al. [139], wherein gate-length = 1.5 μm is considered and is an exploratory study. The aim of the proposed study is to enhance device reliability, therefore, all the application, where reliability is the main concern, the proposed device can be considered as a suitable candidate.

The rest of chapter is organized as follows. Section 4.2 describes physical model considered for the numerical analysis. Section 4.3 is dedicated to results and discussion consisting of six sub-sections namely, Current–Voltage Characteristics, Leakage Current, Electron Temperature Profile, Electric Field Profile, Breakdown Voltage and Capacitance–Voltage Characteristics. Finally, the summary is presented in section 4.4.

4.2 Numerical Analysis Framework / Physical Model

In the proposed work, device structures are examined with variations in the gate geometry (rounded–gate) for distinct value of 'dr', and field plate represented by 'L_{FP}'. An $Al_{0.25}GaN_{0.75}$/GaN HEMT is chosen for the proposed work, wherein the thickness of AlGaN and GaN layer is kept at 25 nm and 3 μm, respectively. For passivation, Si_3N_4 is employed in both the access regions. The schematic of device structures are shown in Fig. 4.1. It is stated in [140] that for a heterostructure containing AlGaN barrier, whose thickness is in the

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range of 20–40 nm, is expected to be fully strained for $0 \leq x \leq 0.38$, partially relaxed for $0.38 \leq x \leq 0.67$, and fully relaxed for $0.67 \leq x \leq 1$. Further it is reported in [46], AlGaN layer with mole-fraction, $x > 0.4$ and $x < 0.15$ are not applicable for high quality HFETs. It is described in [46], for $x > 0.4$, the high lattice and thermal mismatch between GaN buffer and AlGaN barrier layer causes high density of structural defects in AlGaN, while rough interfaces limits 2DEG mobility. Further, for $x < 0.15$, the conduction band offset becomes small ($\triangle E_C < 0.28$ eV), resulting in the poor confinement of the polarization induced sheet carrier concentration. However, with an increase in the mole-fraction, strain along $c - axis$ increases, which boosts in-plane stress significantly deteriorating device reliability [141]. Therefore, it is preferred to have mole-fraction, x in the range of 0.15–0.38.

The RG HEMT is numerically analyzed by varying x from 0.15 to 0.38. The extracted 2DEG and strain is shown in Fig. 4.2. It is evident that rise in x increases 2DEG and strain. For instance, strain changes by 9.26% and 16.36% as x is varied from 0.20 to 0.25 and, 0.25 to 0.30, respectively. It is to mention that 2DEG varies by 28.2% and 21.3% for above mentioned variations in x. As we know, the surge in strain affects reliability of the device. The rise in strain is quite significant when x changes from 0.25 to 0.30, which is not recommended considering device reliability. It is to be noted that at $x = 0.20$ and $x = 0.25$, strain values are very close, but 2DEG concentration at $x = 0.25$ is 28.2% more as compared to 2DEG concentration at $x = 0.20$. Therefore, it is preferred to have mole-fraction of Al as 0.25 or 25%, which not only helps in the formation of 2DEG but also keeps device reliability high. Study of various device structures having mole-fraction of Al as 0.25 can be found in [95, 139, 142] justifying the same.

The proposed device is designed and is numerical analyzed using Sentaurus TCAD [68]. In a hetero-structured device, the interface is of prime significance and energy exchange happens between the interface. In order to model such phenomenon hydrodynamic carrier transport model is implemented [68]. A 2DEG at AlGaN/GaN interface is formed by activating the polarization model. Shockley-Read-Hall (SRH) model is utilized to describe Generation–recombination in the device. Since, GaN and AlGaN are thermodynamically stable wurtzite hexagonal close-

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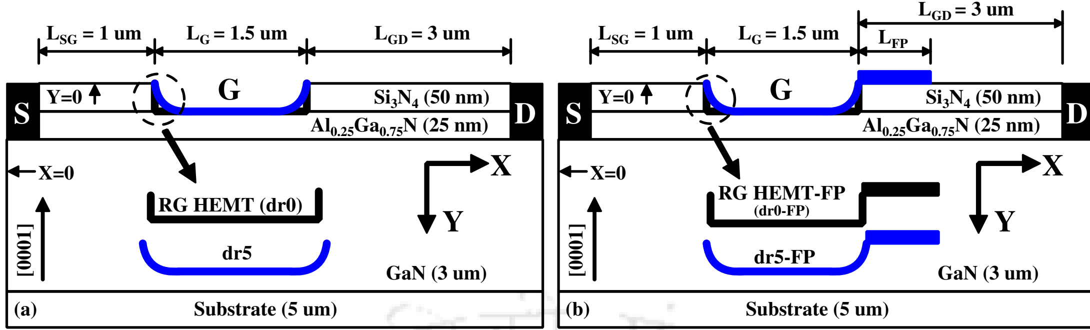

Figure 4.1: Schematics of the structure: (a) Rounded gate without Field plate, and (b) Rounded gate with Field plate considered for this work. Here, 'dr5' is gate shape parameter for rounded gate structure, and 'L_{FP}' is the length of field plate for Field-plated structures

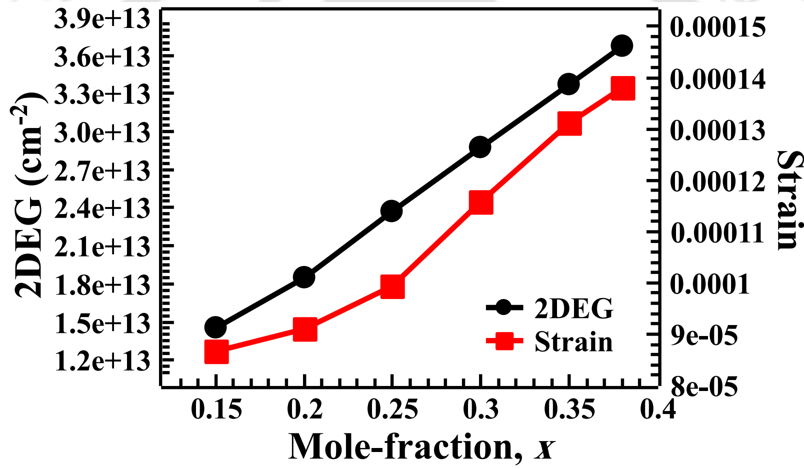

Figure 4.2: 2DEG and strain in the RG HEMT with respect to mole-fraction variation

packed crystal structure [87], AlGaN (having smaller lattice constant compared to GaN) layer is grown on top of GaN. Because of this, a tensile strain develops in the AlGaN layer, which gets uniformly distributed in the basal plane of the AlGaN/GaN to match the lattice constant of GaN [143]. At the AlGaN/GaN interface, polarization sheet charge density, σ is defined by

$$\begin{aligned} \sigma &= \sigma_{GaN} - \sigma_{AlGaN} \\ &= \{P^{sp}_{GaN} + P^{pz}_{GaN}\} - \{P^{sp}_{AlGaN} + P^{pz}_{AlGaN}\} \end{aligned} \tag{4.1}$$

where, P^{sp} and P^{pz} denotes the spontaneous and piezoelectric polarization, respectively.

The spontaneous polarization of $Al_xGa_{1-x}N$ in terms of mole fraction, x is expressed as

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[144, 145]

$$P^{sp}_{Al_xGa_{1-x}N} = -0.09x - 0.034(1-x) + 0.0191x(1-x) \tag{4.2}$$

The piezoelectric polarization arises due to lattice match between the layers that results into mechanical perturbation (strain), which is evaluated by Vegard's interpolation formula [144,145]

$$P^{pz}_{AlN} = -1.808\eta_1 + 5.624\eta_1^2 \text{ for } \eta_1 < 0$$

$$P^{pz}_{AlN} = -1.808\eta_1 - 7.888\eta_1^2 \text{ for } \eta_1 > 0$$

$$P^{pz}_{GaN} = -0.918\eta_1 - 9.541\eta_1^2 \tag{4.3}$$

where, η_1 represents the basal strain in AlN or GaN (binary compound). Similarly, the piezoelectric strain of $Al_xGa_{1-x}N$ using Vegard's interpolation formula can be expressed as [144, 145] as mentioned below. Further details can be referred from [144–146].

$$P^{pz}_{Al_xGa_{1-x}N} = xP^{pz}_{AlN}(\eta_1) + x(1-x)P^{pz}_{GaN}(\eta_1) \tag{4.4}$$

GaN crystal is anisotropic along c-axis ([0001]) and, for its modeling an Anisotropic model is activated. Bias dependent converse piezoelectric phenomena is modelled through gate-dependent polarization model. The model incorporated in the numerical analysis framework for the piezoelectric strain is as follow.

$$\begin{bmatrix} P_x \\ P_y \\ P_z \end{bmatrix} = \begin{bmatrix} P_x^{sp} \\ P_y^{sp} \\ P_z^{sp} + P_{strain} \end{bmatrix} \tag{4.5}$$

where, $P^{sp}_{x/y/z}$ stands for the spontaneous polarization vector (C/cm^2) in x, y, and z-axis respectively. P_{strain} stands for piezoelectric strain, which is expressed as

$$P_{strain} = 2d_{31} \cdot strain \cdot \left(c_{11} + c_{12} - \ 2c_{13}^2/c_{33}\right) \tag{4.6}$$

where, d_{31} stands for piezoelectric coefficient (cm/V), and c_{ij} are the stiffness constants

(Pa). The *strain* can be further simplified as

$$strain = (1 - r) \cdot (a_0 \; - \; a)/a \tag{4.7}$$

where, a_0, a stands for strained and unstrained lattice constant (A°), and r is a relaxation parameter. On inclusion of the above model, piezoelectric charge, q_{PE} is computed as

$$q_{PE} = - \; C_{act} \bigtriangledown P \tag{4.8}$$

where, C_{act} is a calibration parameter used to adjust the piezoelectric charge. The piezoelectric charge, q_{PE} adds up to the Poisson equation. The modified Poisson equation is

$$\bigtriangledown \epsilon \cdot \bigtriangledown \phi = -q\,(p - n + N_D - N_A + q_{PE}) \tag{4.9}$$

where, ϕ is the potential and q is the charge of an electron. p and n are the hole and electron densities, respectively. N_D, N_A, q_{PE} are the ionized donor concentration, ionized acceptor concentration, and piezoelectric charge, respectively.

From the above equation, we can infer that the potential at any point is evaluated by solving Poisson's partial differential equation considering the charges: p, n, N_D, N_A, and q_{PE}. Hence, the evaluated potential includes entire charge (mobile and immobile) in the device. The model parameters for polarization models are referred from [147], and are listed in Table 4.1.

Table 4.1: Parameters of Polarization Model used in TCAD simulation

Symbols	Units	GaN	AlN
P_z^{sp}	C/cm^2	-2.9 $\times 10^{-6}$	-8.1 $\times 10^{-6}$
e_{31}	C/cm^2	-3.5 $\times 10^{-5}$	-5.0 $\times 10^{-5}$
e_{33}	C/cm^2	1.27 $\times 10^{-4}$	1.79 $\times 10^{-4}$
c_{13}	GPa	106	108
c_{33}	GPa	398	373
a_0	A°	3.189	3.189
a	A°	3.189	3.112
relax	–	0.1	0.1

The Schottky gate contact, which corresponds to Nickel has a work-function, ϕ_m of 5.2 eV and, the work function for AlGaN (ϕ_s) is 4.3 eV. Hence, the work function difference is $\phi_\mathrm{ms} = \phi_\mathrm{m}$

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Table 4.2: Physical parameters used in TCAD simulation

S. No.	Parameter	Description	Dimension
1	L_G	Gate Length	1.5 μm
2	L_{SG}	Source to Gate Spacing	1 μm
3	L_{GD}	Gate to Drain Spacing	3.0 μm
4	L_{FP}	Field Plate Length	0.5 – 1.5 μm
5	dr	Gate shape parameter	0.0 – 0.07 μm
6	$t_{Si_3N_4}$	Thickness of Si_3N_4 layer	50 nm
7	t_{AlGaN}	Thickness of AlGaN layer	25 nm
8	t_{GaN}	Thickness of GaN layer	3.0 μm
9	t_{SUB}	Thickness of Substrate layer	5.0 μm

- $\phi_s = 0.9$ eV. Surface donor trap in AlGaN is set to 2×10^{13} cm^{-2} and the GaN bulk layer is C–doped having concentration 1×10^{16} cm^{-3}. The models employed for the numerical analysis are referenced from [148]. The physical parameters and dimensions are stated in Table 4.2 for the completeness. It may be noted that quantum confinement effects that causes the 2-DEG offset is not included in the numerical analysis.

For the numerical analysis, the gate–shape parameter 'dr' and field–plate length parameter 'L_{FP}' in the device structure are varied from 0 – 0.07 μm (0.0, 0.02 μm, 0.05 μm, 0.07 μm), and 0.5 – 1.5 μm (0.5 μm, 1.0 μm, 1.5 μm), respectively. The proposed gate–shape parameter 'dr' represents rounding radius of gate. The device structure with 'dr' = 0.0 is termed as RG HEMT, and remaining structures with 'dr' = 0.02, 0.05, 0.07 are nominated as dr2, dr5 and dr7, respectively. As there are a series of combinations for 'dr' and 'L_{FP}', results for dr7 is stated in this chapter for the sake of brevity. This is due to the fact that the trend of change in results for rounded gate devices tends to stabilize as 'dr' approaches 0.07 μm. Therefore, dr7 is considered for the comparison with field–plated devices. However, in some cases, results for dr2 and dr5 are stated to showcase the variations in the parameters of rounded gate devices without field plate as compared to the rounded gate devices with field plate.

In the numerical simulation, meshing plays a crucial role, especially around the corner at the interface, and it is essential to extract the results at a distance greater than 3 A° [89]. The results stated for Y-cut section (along the channel) is obtained at 20 A° below the SiN/AlGaN

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interface [at Y = 52 nm] and results for X-cut section is taken at the right edge of the gate contact (in the drain access region).

It is to mention that the entire numerical analysis in this work is performed in 2D (2-dimensional) TCAD framework, and the current values stated are expressed in terms of per unit width (/mm). Thus, if the effect of gate width needs to be evaluated on any electrical parameter, for example, leakage current, it can be done by multiplication with a factor, W_G (gate width).

In this work, we have proposed a new gate shape for which only numerical analysis is performed. This work aims at portraying the change in electrical and reliability behaviour of a device with respect to the variation in gate shape. However, with current advancements in fabrication technology, realization of un/non-rectangular gate shapes is possible [85, 149, 150]. For instance, Dannecker et al. [150] demonstrated 2 μm deep trenches in GaN with a width of 4 μm or less, etched with SF_6 based dry etching process. Followed by a wet etching post-treatment and employing tetramethylammonium hydroxide (TMAH) and potassium hydroxide (KOH), a smooth and vertical side-wall as well as rounded corners at the trench bottom was obtained. Chen [151] proposed the idea of modulating the light intensity on the photo-resist to create a gray scale mask with a sloped profile in it. The mask then transfer the slope profile to realize a sloped field plate structure. These processes can be tuned accordingly to realize the proposed device structure. It is expected that research community may explore this aspect given the benefit of the proposed device.

4.3 Results & Discussion

In this section results are presented in five sub–sections; Current–Voltage characteristics, Leakage current, eTemperature profile, Electric Field profile, and Capacitance–Voltage characteristics. In the subsequent sub–sections, four sets of result(s) for the devices are depicted. First set (SET 1) of the results corresponds to the change in gate–shape parameter of the device (without field plate), and the devices in this group are RG HEMT followed by dr2, dr5

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and dr7. The second set (SET 2) of results corresponds to device structure with field plate ('L_{FP}' = 0.5 μm) incorporated on the same sequence of devices as in SET 1. Third set (SET 3) highlights the results obtained for the change in 'L_{FP}' (= 0, 0.5 μm, 1.0 μm and 1.5 μm) in RG HEMT. For fourth set (SET 4), dr7 is chosen as the candidate and the field plate length is varied in the range 'L_{FP}' (= 0, 0.5 μm, 1.0 μm and 1.5 μm). The rationale behind the selection of aforementioned four sets is to exhibit the change in electrical property of the device whenever either the gate–shape parameter, 'dr' or field length plate parameter, 'L_{FP}' varies. In the subsequent section, it is found that the change in electrical property stabilizes for rounded gate devices as gate–shape parameter 'dr' approaches 0.07 μm, therefore, it is desirable to draw the comparison with rounded gate devices with the extreme design parameters i.e., RG HEMT, and dr7 with/without field plate. The requisite interpretation for the observations is stated in the subsequent subsections. For brevity, results for other possible combinations of gate–shape parameter, 'dr' and field length plate, 'L_{FP}' are not presented unless it is essential to corroborate the facts.

For preliminary investigation of the proposed rounded gate devices, we have extracted the conduction band profile and electron density profile of the devices at equilibrium condition (gate voltage = drain voltage = 0V) as shown in Fig. 4.3. It is evident that 2DEG is originates at the proposed rounded gate device. The sheet carrier concentration, n_{sheet} at the hetero-interface assuming no doping in the AlGaN layer is expressed below.

$$n_{\text{sheet}} = \frac{\sigma(x)}{e} - \left(\frac{\epsilon_0 \epsilon(x)}{d_{\text{AlGaN}}\ e^2}\right) [e\phi_B(x) + E_F(x) - \Delta E_C(x)] \tag{4.10}$$

where, $\sigma(x)$ is mole fraction dependent polarization sheet charge density, thickness of the $Al_xGa_{1-x}N$ barrier denoted by d_{AlGaN}, $e\phi_b$ is the Schottky barrier of the gate contact. E_F is the Fermi level with respect to the GaN conduction band edge energy, and ΔE_C is the conduction band offset at the AlGaN/GaN interface. Further, related information can be found in [45,46,152]. From Eq. 4.10, it is apparent that n_{sheet} depends on the polarization sheet charge density σ and conduction band offset ΔE_C. The electron density of the devices is found to be

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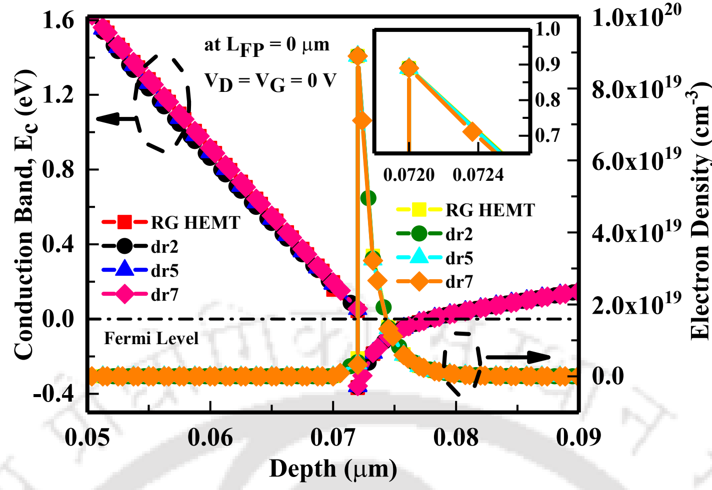

Figure 4.3: Conduction band and electron density profile at the AlGaN/GaN heterostructure of rounded gate devices (without field plate) at gate voltage = drain voltage = 0 V

8.90 $\times 10^{19}$ cm^{-3}($\approx$ 2.36 $\times 10^{13}$ cm^{-2}). The conduction band offset of the proposed devices is observed to be 0.37 eV. The polarization sheet charge density varies with mole fraction of the binary compound according to Eq. 4.1,4.2, & 4.4, therefore, for the proposed rounded gate devices, $\sigma(x)$ does not vary. Similarly, as the thickness of layers in the proposed rounded gate devices is same, ΔE_C remains constant. Hence, the observed electron density at the interface is same for all the devices, RG HEMT, dr2, dr5, and dr7, which means gate–shape does not modulate 2DEG in the proposed devices.

4.3.1 Current–Voltage Characteristics

In this subsection, two fundamental aspects of a device namely Transfer Characteristics (I_D vs V_{GS}) and Transconductance (g_m), and Output Characteristics (I_D vs V_{DS}) are discussed.

4.3.1.1 Transfer Characteristics & Transconductance

Transconductance, g_m is a key parameter from a circuit designer's perspective. As we know, the transconductance has its roots in the device's electrical characteristics, which ultimately depends on the quality of device design. Transconductance, g_m, can be expressed as [153]

$$g_m = \frac{\triangle I_D}{\triangle V_{GS}} = \left(\frac{\triangle n}{\triangle V_{GS}}\right) qv + \left(\frac{\triangle v}{\triangle V_{GS}}\right) nq \tag{4.11}$$

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where, $\triangle n$ represents change in carrier concentration. q is the charge of an electron and $\triangle v$ represents change in carrier velocity, while rest of the parameters have their usual meaning. The change in $\triangle n$ is notable in the gate region for the change in V_{GS}. The swift enhancement of carrier concentration as V_{GS} is changed from – 10 V to 2 V, and the rise in electron velocity ascertains the contribution of first term of equation (4.11) to g_m. This is because of the drop in $\triangle v$ due to rapid decrease in the electron velocity as V_{GS} moves toward the positive domain [153], and reduces the impact of second terms of equation (4.11) on g_m. Hence, g_m gradually increases and then decreases as gate voltage is varied from – 10 V to 2 V.

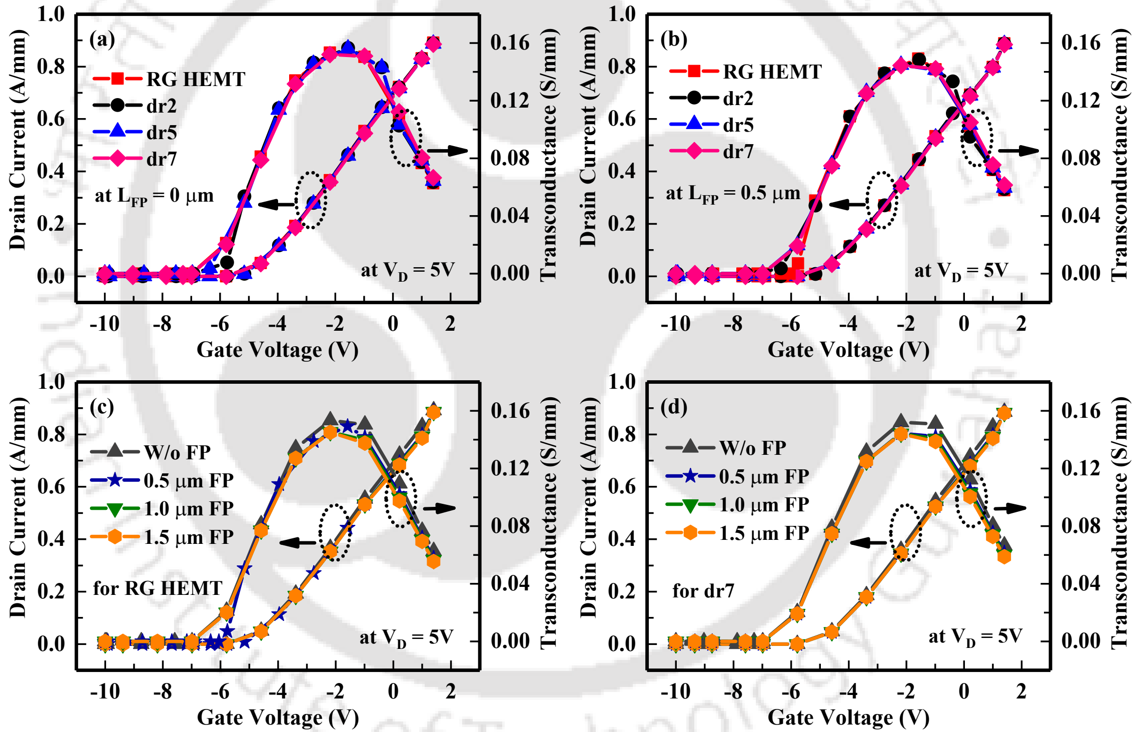

Figure 4.4: Comparison of Transfer characteristics (I_D vs V_{GS}) and Transconductance (g_m) for AlGaN/GaN HEMT devices with drain voltage = 5 V: (a) with variation in gate shape parameter 'dr', (b) with a constant field plate length 'L_{FP}'= 0.5 μm and variation in gate shape parameter 'dr', (c) Field plate length variation 'L_{FP}' for RG HEMT (dr=0), and (d) Field plate length variation 'L_{FP}' for dr7

The transconductance and transfer characteristics I_D vs V_{GS} for the devices under observation are shown in Fig. 4.4. As it can be seen from Fig. 4.4 (a,b,c,d), there is no variation in the transconductance, when 'dr' and 'L_{FP}' are varied. The peak transconductance observed for the devices without field plate and with field plate are ∼ 0.16 S/mm and ∼ 0.15 S/mm, respec-

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tively. The slight reduction in transfer characteristics (current level and transconductance) of the devices with field plate is attributed to decrease electron density with an introduction of the field plate [154].

The threshold voltages of the devices (with and without field plate) extracted from transfer characteristics (I_D vs V_{GS}) are found to be – 5.8 V. The numerical analysis is performed with gate voltage sweeping from – 10 V to 2 V. The threshold voltage for AlGaN/GaN HEMT (V_{T_HEMT}) can be expressed as [155]

$$V_{T_HEMT} = \phi_b + \frac{Q_{p1}}{C_{AlGaN}} \tag{4.12}$$

where, Q_{p1} stands for the polarization charge at AlGaN/GaN interface. ϕ_b is Gate-Metal/AlGaN interface barrier height, and C_{AlGaN} is the capacitance of AlGaN barrier layer. For the device structures considered in this chapter, as shape of the gate varies, the [Gate-Metal/AlGaN] contact interface remains consistent, i.e. the barrier height is constant for all the structures. Also, AlGaN/GaN interface does not shift in any of the structures, and it is observed that Q_{p1} is constant and C_{AlGaN} varies slightly. This indicates that the threshold voltages of the devices do not vary much and the marginal fluctuation in it is reported due to the incremental variations in the capacitance. In succession, we can surmise that the threshold voltages for the device structures with or without field plate barely varies and the peak transconductance observed is $\sim$ 0.16 S/mm and $\sim$ 0.15 S/mm for the devices without field plate and with field plate, respectively.

4.3.1.2 Output Characteristics

Output characteristics of the device is essential to understand the performance of a device, basically the current handling capacity. Heterostructure devices, especially III-N devices, are expected to have higher current due to the formation of 2DEG at AlGaN/GaN interface, which facilitates better electron confinement and lesser electron scattering. The $I_D - V_{DS}$ characteristics of the devices, RG HEMT, dr2, dr5, and dr7 are shown in Fig. 4.5 with the variation in field plate length 'L_{FP}'. It is observed that drain current, I_D, decreases as gate–shape parameter

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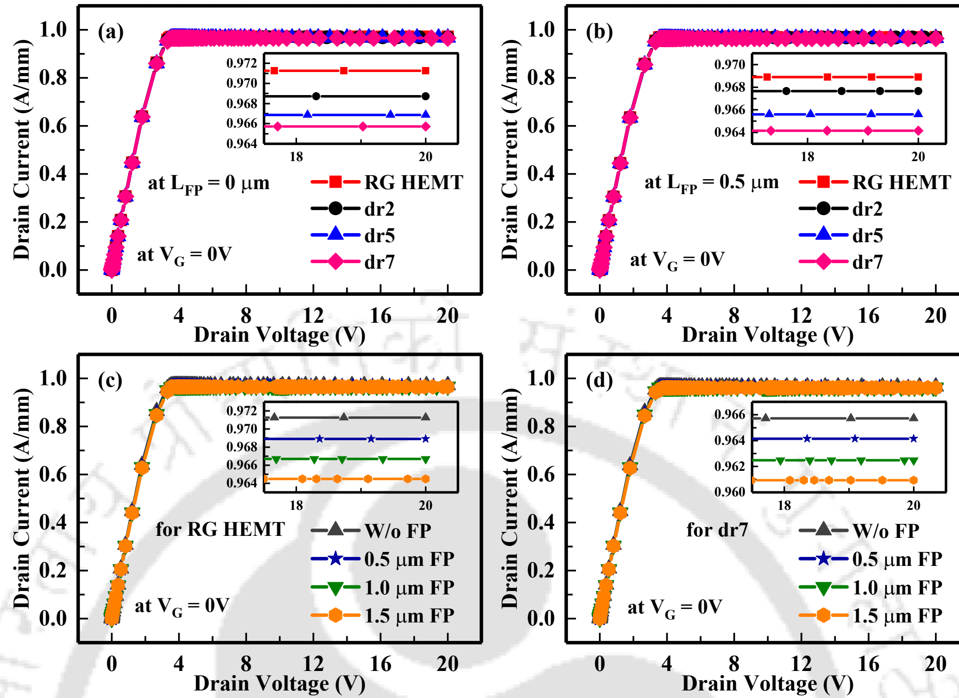

Figure 4.5: Output Characteristics for AlGaN/GaN HEMT with gate voltage = 0 V: (a) variation in drain current for change in gate shape parameter 'dr' (b) drain current for rounded gate device with a constant field plate length 'L_{FP}'= 0.5 μm (c) Field plate length variation 'L_{FP}' for RG HEMT (dr=0), and (d) Field plate length variation 'L_{FP}' for dr7

for the devices changes (RG HEMT, dr2, dr5 and dr7). This is to mention that drain current decreases by 6 mA as gate-shape parameter (SET 1) changes. With the introduction of field plate (SET 2), drain current decreases by 4 mA. Similarly, drain current of RG HEMT (SET 3) and dr7 (SET 4) devices with different field plate length decreases by 7 mA and 5 mA, respectively. This is attributed to the decrease in electron density in the channel region of the devices. The drain electric field interacts with 2DEG through the gate contact.

For rounded gate devices, as the magnitude of vertical electric field is reduced (refer Section 4.3.4 for detail), the total strain inclusive of the converse piezoelectric effect is low. As a consequence, the total piezoelectric polarization reduces for rounded gate devices. This leads to the reduced drain current for rounded gate devices as reported in [148]. Similar observations are noted in HEMTs with field plate, where electric field further reduces due to the introduction of field plate (refer Section 4.3.4 for detail). It can be deduced from Fig. 4.5 (a,b,c,d) that the

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drain current of field–plated device is less as compared to the drain current of the device without field plate. Therefore, drain current subsides marginally when gate geometry is modified or/and field plate is introduced.

4.3.2 Leakage Current

In this subsection, issues related with leakage current (I_G vs V_{DS}) of the rounded gate devices with/without field plate are discussed. Leakage current, I_G shows a diminishing trend as gate–shape parameter 'dr' varies. Two orders of magnitude reduction in I_G is observed when gate–shape parameter changes (SET 1), as shown in the Fig. 4.6 (a). With the introduction of field plate (SET 2), I_G decreases by a factor of 10^1 as depicted in Fig. 4.6 (b). Similar behaviour is observed for RG HEMT and dr7 devices with different field plate length, 'L_{FP}'and I_G scales down by a factor of 10^2 and 10^1 respectively, as shown in Fig. 4.6 (c) and (d).

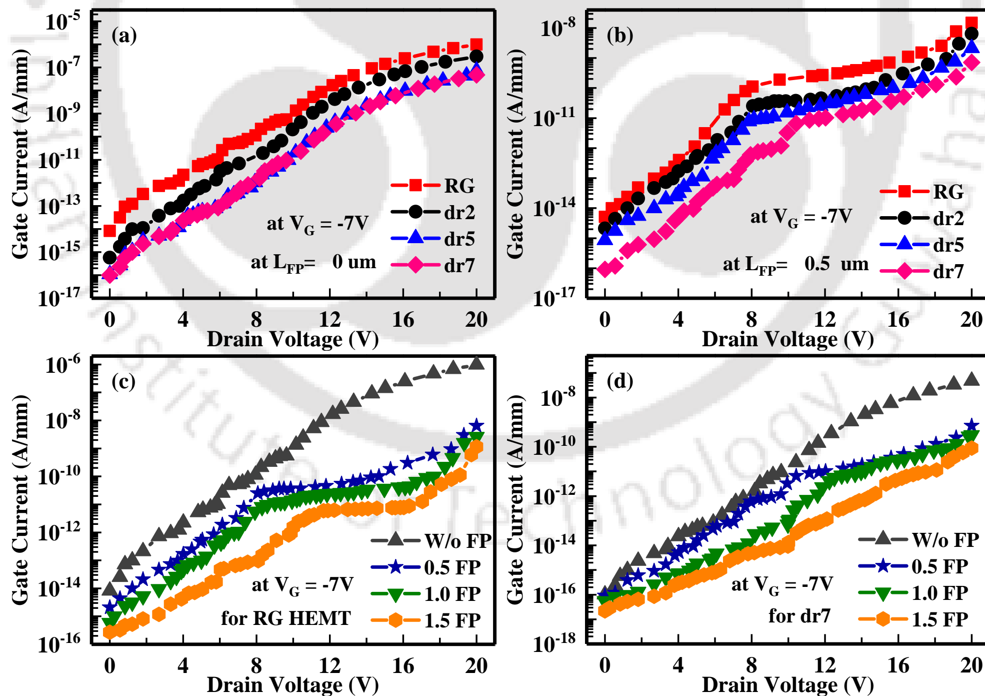

Figure 4.6: Leakage Current for AlGaN/GaN HEMT with gate voltage = -7 V: (a) with different gate shape parameter 'dr', (b) with fixed field plate length 'L_{FP}'= 0.5 μm and change in gate shape parameter 'dr', (c) for RG HEMT as 'L_{FP}' vary, and (d) for devices with same gate shape parameter of dr7 and variation in field plate length 'L_{FP}'

The reduction of leakage current is due to the decrease in space charge density in AlGaN

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layer (refer Table 4.3). With the introduction of field plate or/and change in gate–shape parameter of the device, the depletion width extends below the gate region i.e., into AlGaN layer. Since the mobile carriers (2DEG) are of the order of 10^{19} cm^{-3}, which is higher than immobile carriers having the order 10^{16} cm^{-3}, contribution of mobile carrier is significant to the overall space charge. It can also be inferred using Fig. 4.7 (a,b,c,d), which describes space charge profile of the devices with and without field plate with varying gate–shape parameter. The extension of depletion region into AlGaN layer leads to mobile carrier concentration reduction that results in scaling down of space charge and leakage current. The order of magnitude change in leakage current for device(s) with field plate is higher than the device(s) without field plate. Tunneling mechanism being electric field dependent can be a factor that may be responsible for decrease in gate current. The moderation in electric field at the edge of rounded gate further reduces the tunneling mechanism, as a result the gate current decreases. This is true as well when field plate is introduced to a device, as electric field at the gate edge gets moderated. A similar phenomenon is depicted in Saito et al. [156].

Table 4.3: Integrated Space Charge (SC) value in AlGaN layer value for different device structure (as gate shape parameter 'dr' and field plate length 'L_{FP}' vary)

SET	Device Geometry	SC (10^3 μm^{-1})
1	RG HEMT	-7.16
	dr2	-6.85
	dr5	-6.72
	dr7	-6.61
2	RG HEMT, $L_{FP} = 0.5\mu m$	-6.38
	dr2, $L_{FP} = 0.5\mu m$	-6.24
	dr5, $L_{FP} = 0.5\mu m$	-6.13
	dr7, $L_{FP} = 0.5\mu m$	-6.05
3	RG HEMT	-7.16
	RG HEMT, $L_{FP} = 0.5\mu m$	-6.38
	RG HEMT, $L_{FP} = 1.0\mu m$	-6.21
	RG HEMT, $L_{FP} = 1.5\mu m$	-6.04
4	dr7	-6.61
	dr7, $L_{FP} = 0.5\mu m$	-6.05
	dr7, $L_{FP} = 1.0\mu m$	-5.93
	dr7, $L_{FP} = 1.5\mu m$	-5.85

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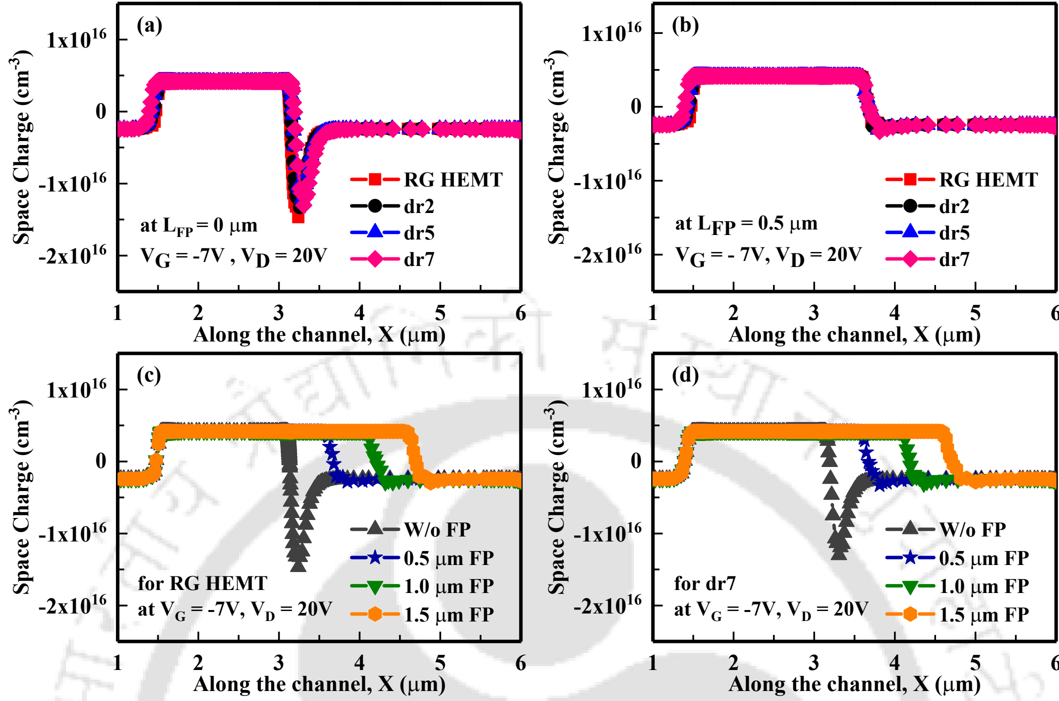

Figure 4.7: Space Charge profile for AlGaN/GaN HEMT (at gate voltage = -7 V and drain voltage = 20 V): (a) rounded gate devices, (b) with field plate length 'L_{FP}'= 0.5 μm and as gate shape parameter 'dr' vary, (c) for RG HEMT as 'L_{FP}' vary, and (d) change in field plate length 'L_{FP}' for device with gate shape parameter as dr7

The significant reduction in I_G translates to higher I_{ON}/I_{OFF} ratio. Gate leakage is one of the dominant phenomenon triggering the breakdown of devices, reduction in I_G increases breakdown voltage of the device [123, 157]. Therefore, considerable drop in leakage current of rounded gate devices with and without field plate restrains device degradation and increases its breakdown voltage.

4.3.3 eTemperature Profile

In general, drift-diffusion model fails to consider the velocity overshoot and usually overestimates the impact ionization rate. In order to model the aforementioned observation, hydrodynamic model is implemented, where driving force is the carrier energy. Since AlGaN/GaN HEMTs are uni-polar devices, the hole concentration is negligible as compared to the electron concentration. Therefore, holes have minimum influence on the device characteristics [158].

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Thus, the electron carrier temperature in hydrodynamic model needs to be analyzed. It is to mention that the electron temperature (e-Temp) profile is essential to study device degradation as it has been reported in [159] that the high energy electrons are responsible for electrochemical degradation of AlGaN layer. The e-Temp profile of the devices with the variations in gate–shape parameter, 'dr' and field plate length, 'L_{FP}' is depicted in Fig. 4.8.

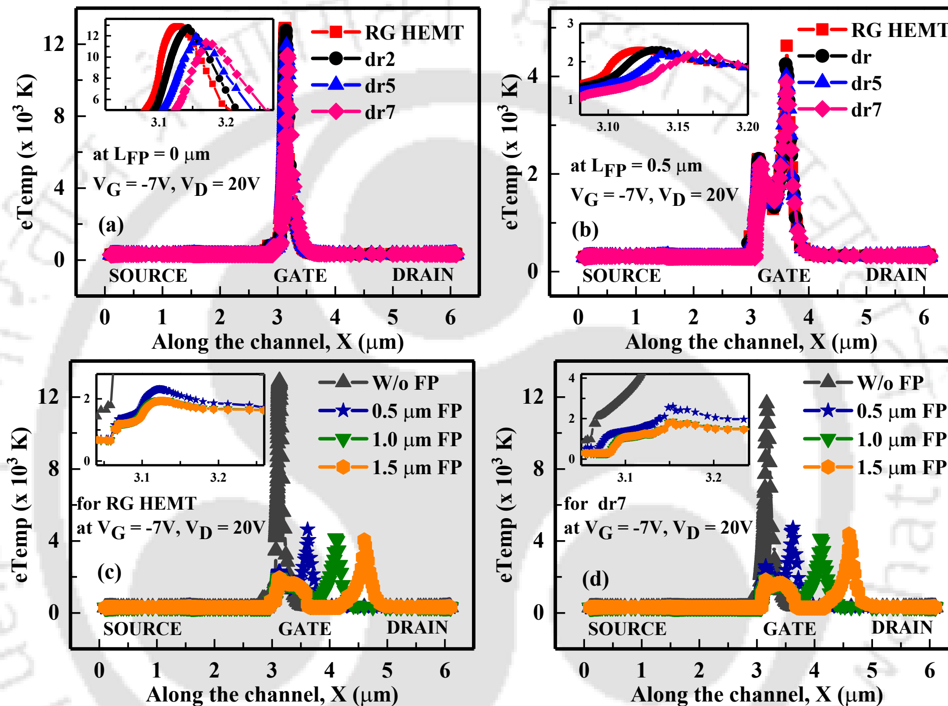

Figure 4.8: eTemperature profile along the channel (Y–Cut) for AlGaN/GaN HEMT (at gate voltage = -7 V and drain voltage = 20 V): (a) with different gate shape parameter 'dr', (b) with field plate length 'L_{FP}'= 0.5 μm as gate shape parameter 'dr' vary, (c) for RG HEMT as 'L_{FP}' vary, and (d) for device with gate shape parameter as dr7, and variation in 'L_{FP}'

It is observed that as gate–shape parameter 'dr' varies, the peak electron temperature at the gate edge decreases as shown in Fig. 4.8 (a)). This can be attributed to the diffused electric field due to 'dr' variations. Similarly, for the device structure with field plate, the electron temperature decreases at the gate edge and a second peak appears at the end of field plate extension. Although the second peak appears for the field plate devices, the magnitude of the peak electron temperature at the gate edge is significantly less as exhibited in Fig. 4.8 (b,c,d). The change in peak e-Temp at the gate edge toward drain side of the rounded gate device

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is ∼ 12% and is ∼ 85% for the field–plated device in both the cases of RG HEMT and dr7, respectively, as depicted in Table 4.4.

Table 4.4: Observed peak electron temperature (e-Temp) value for different device structure at gate edge toward drain side (as gate shape parameter 'dr' and field plate length 'L_{FP}' vary), and change (in %) from the maximum e-Temp value

Device Geometry	Peak e-Temp (10^3 K)	% Change
RG HEMT	12.89	–
dr2	12.75	↓ 1.09
dr5	11.92	↓ 7.53
dr7	11.37	↓ 11.79
RG HEMT	12.89	–
RG HEMT, $L_{FP} = 0.5\mu$m	2.34	↓ 81.85
RG HEMT, $L_{FP} = 1.0\mu$m	2.01	↓ 84.41
RG HEMT, $L_{FP} = 1.5\mu$m	1.91	↓ 85.18
dr7	11.37	↓ 11.79
dr7, $L_{FP} = 0.5\mu$m	2.32	↓ 82.00
dr7, $L_{FP} = 1.0\mu$m	1.87	↓ 85.49
dr7, $L_{FP} = 1.5\mu$m	1.82	↓ 85.88

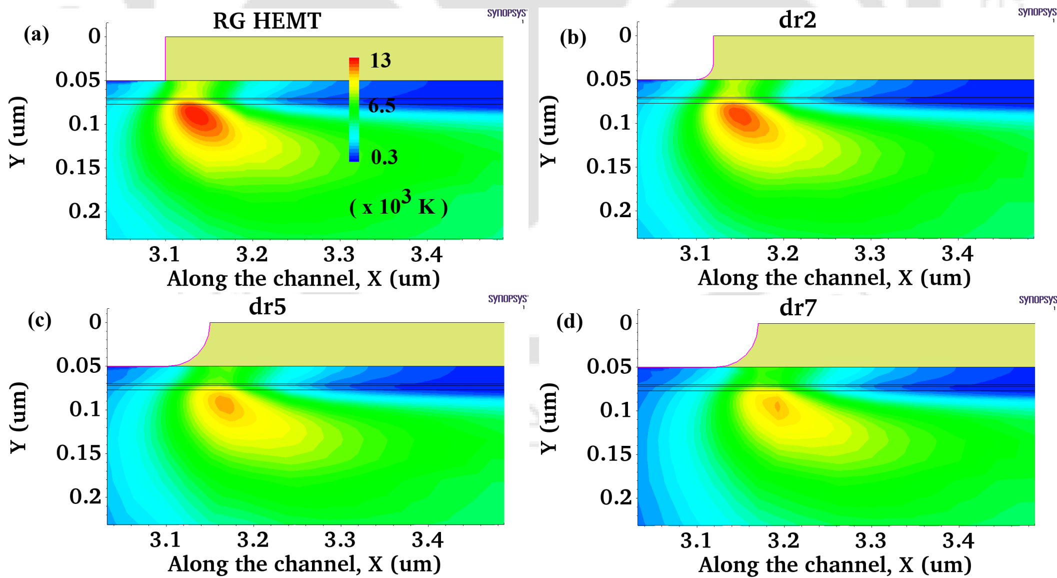

Figure 4.9: Illustration of eTemperature profile for rounded gate devices (without field plate, at gate voltage = -7 V and drain voltage = 20 V) extracted from the numerical analysis for: (a) RG HEMT, (b) dr2, (c) dr5, and (d) dr7

The affect of rounded gate devices on eTemp profile can be observed in Fig. 4.9. There is a substantial decrease in cross-section area of the region with higher electron temperature.

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The decrease in quantity of electron with higher electron temperature may contribute for the observed reduction in gate leakage current. Similarly, the decrease in cross-sectional area of higher electron temperature can be correlated with the reduce electric field at the gate edge of rounded gate devices.

For a device operating in the ON state, an additional rise in temperature leads to hot electron induced device degradation, which plays a pivotal role in determining device reliability [160,161]. A significant change in hot electron temperature in the vicinity of gate edge, which migrates towards the drain access region, triggers generation of traps [4] and defects by piezoelectric stress [162] or dislocations [163]. This can affect device stability and may initiate device breakdown [164]. Also, due to high electric field at the gate edge (refer Section 4.3.4), a hotspot is formed and the peak temperature of around 6000K [153] to 7000K [165] is reported in the literature. Hence, decrease in the hot electron temperature at the gate edge of the rounded gate devices with/without field plate helps in the reduction of device degradation.

4.3.4 Electric Field Profile

Vertical electric field along the channel is a crucial internal parameter influencing the device reliability. This field controls physical properties of the device, such as built-in strain, converse piezoelectric-electric strain, and critical voltage [32]. It is well established that one of the breakdown mechanisms originates from gate edge toward drain-side due to the presence of high electric field under normal operation [166]. This electric field initiates avalanche breakdown and thermally-assisted tunnelling in the device [167]. For an AlGaN/GaN HEMT, it is a well-known fact that the electric field is higher in magnitude at the gate edge in the drain access region. The peak vertical electric field reported in literature is around -7 MV/cm [165]. This high electrical field, which can lead to localized Schottky-barrier breakdown at a small drain voltage [116]. Therefore, it becomes imperative to engineer electric field in the vicinity of the gate for the improvement in device performance.

From Fig. 4.10 (a), it can be observed that the peak electric field at the gate edge toward the drain side for RG HEMT is approximately -3.61 MV/cm. The magnitude of peak electric

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field gradually decreases as gate–shape parameter 'dr' varies, which is -2.45 MV/cm for dr2, -2.18 MV/cm for dr5, and -1.99 MV/cm for dr7. This is due to the reduced electric field at the corner of gate edge, which subsides electric field crowding at the gate edge. The proposed gate structure helps not only in reducing electric field significantly but also enhancing device reliability as stated in [148].

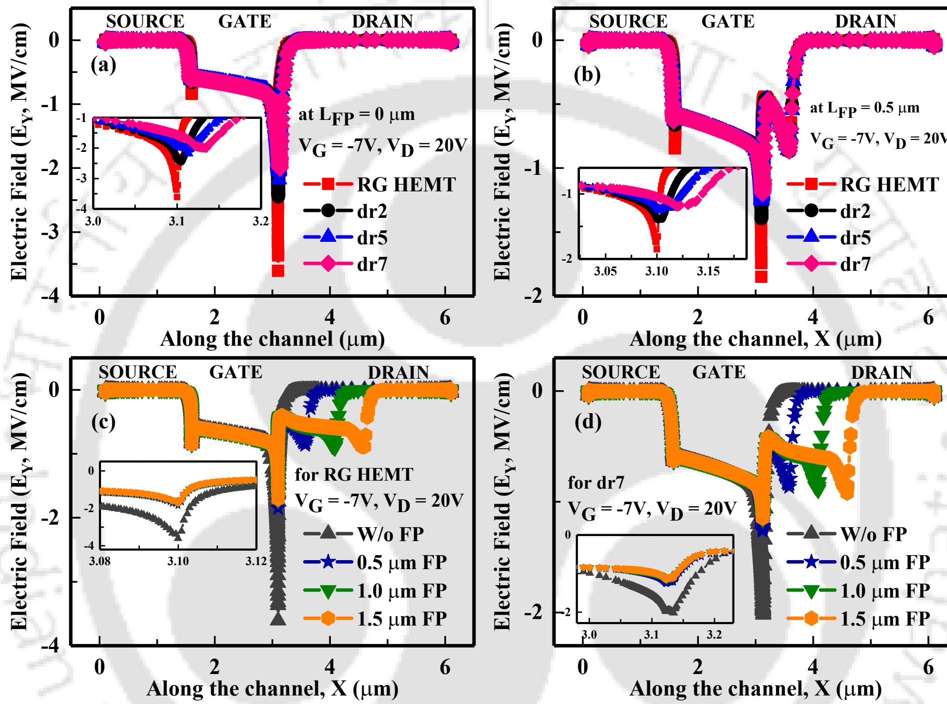

Figure 4.10: Electric Field profile along the channel (Y–Cut) for AlGaN/GaN HEMT at gate voltage = -7 V and drain voltage = 20 V: (a) with different gate shape parameter 'dr', (b) with field plate length 'L_{FP}'= 0.5 μm as gate shape parameter 'dr' vary, (c) for RG HEMT as 'L_{FP}' vary, and (d) for rounded gate device dr7 with variation in 'L_{FP}'

Similar behaviour is observed for the field plate structure(s). Its detailed information is enlisted in Table 4.5 and is shown in Fig. 4.10 (b,c,d). Introduction of the field plate brings up electric field with n+1 peaks, where n is the number of field plate [168]. In the proposed research work, we have taken n = 1. As shown in Fig. 4.10 (b,c,d), the second peak helps in reducing maximum electric field at the gate edge as the field is spread out over a region. By spreading the electric field between the large gate-drain spacing, the breakdown voltage is enhanced up to the limit of channel-substrate junction breakdown, which is quite high due to shallow doping of the substrate [168]. However, for longer field plate, 'L_{FP}' breakdown voltage of the device

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becomes less. As it is evident from Fig. 4.10 (b,c,d) that with an increase in 'L_{FP}', the second electric field peak moves closer to the drain terminal and its interaction with drain terminal results in isolation breakdown [120]. Thus, minimized electric field for the rounded gate devices with/without field plate further restrict effects of built-in strain, converse piezoelectric-electric strain, and critical voltage etc. It is also expected that reliability of these devices is enhanced. A detailed comparison of electric field reduction at gate edge of the proposed gate structure with existing literature is enlisted in Table 4.6. One of the possible analytical model for electric field of the rounded gate device is illustrated in Appendix A.

Table 4.5: Extracted peak vertical component of electric field, E_Y [at the right gate edge] for the devices with different gate shape parameter 'dr' (RG HEMT, dr2, dr5, and dr7) and field plate length 'L_{FP}', and change (in %) from the maximum E_Y value

Field Plate	Device Geometry	Peak E_Y (MV/cm)	% Change
L_{FP} = 0	RG HEMT	-3.61	–
	dr2	-2.45	↓ 32.13
	dr5	-2.18	↓ 39.61
	dr7	-1.99	↓ 44.88
L_{FP} = 0.5 μm	RG HEMT	-1.85	↓ 48.75
	dr2	-1.39	↓ 58.72
	dr5	-1.25	↓ 65.37
	dr7	-1.19	↓ 67.03
L_{FP} = 1.0 μm	RG HEMT	-1.72	↓ 52.35
	dr2	-1.26	↓ 65.09
	dr5	-1.18	↓ 67.31
	dr7	-1.15	↓ 68.14
L_{FP} = 1.5 μm	RG HEMT	-1.70	↓ 52.90
	dr2	-1.20	↓ 66.75
	dr5	-1.16	↓ 67.86
	dr7	-1.14	↓ 68.42

4.3.5 Breakdown Voltage

The breakdown voltage of a device limits its high voltage operation. Leakage current is one of the key factors, which affects device reliability [171]. In the previous section (refer 4.3.2), we have discussed reduction in the leakage current of the proposed devices. So, suppressing leakage current with suitable technological approach, such as the proposed devices presented

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Table 4.6: Comparison of techniques employed for reduction in peak E-Field at the gate edge of the device

S. No.	Reduction in peak E-Field (in %)	Technique employed
1	15%	Si_3N_4 region in the barrier [169]
2	29%	Slant Gate geometry [89]
3	42%	High-k passivation and gate-connected field plate [170]
4	48%	Incorporation of p-diamond back barriers and cap layers [94]
5	51%	Field plate [2]
6	45%	Proposed rounded gate device without field plate
	68%	Proposed rounded gate device with field plate

in this work increases breakdown voltage for a given gate-to-drain spacing. Furthermore, in certain cases, the drain current divides into source current and gate current. The gate current is basically due to the flow of electrons from gate to the drain terminal as a result of the injection of electrons across the Schottky gate barrier when drain voltage is positive. Since these effects are initiated by a high electric field at the gate edge of the device, the field plate helps in suppressing these effects and results in higher breakdown voltage [118, 172, 173].

The breakdown voltage for devices extracted from $I_D - V_D$ characteristics at gate voltage = -7 V (OFF–State) is shown in Fig. 4.11. As discussed in the preceding section, due to gate-shape parameter variations from RG HEMT to dr7, electric field at gate edge decreases and device breakdown voltage increases. Similarly, an introduction of field plate in the device structure increases breakdown voltage. The combined effect of rounded gate and field plate translates to breakdown voltage of 198 V for dr7 with $L_{FP} = 1.5\mu$m as compared to the breakdown voltage of 120 V for RG HEMT without field plate. Table 4.7 may be referred for details.

4.3.6 Capacitance–Voltage Characteristics

The dependency between gate capacitance C_g and gate voltage is studied by performing AC analysis with frequency of operation fixed at 1 MHz [174], source and drain terminals being grounded ($V_S = V_D = 0$ V), and gate voltage (V_G) being swept from -10 V to 0 V. From

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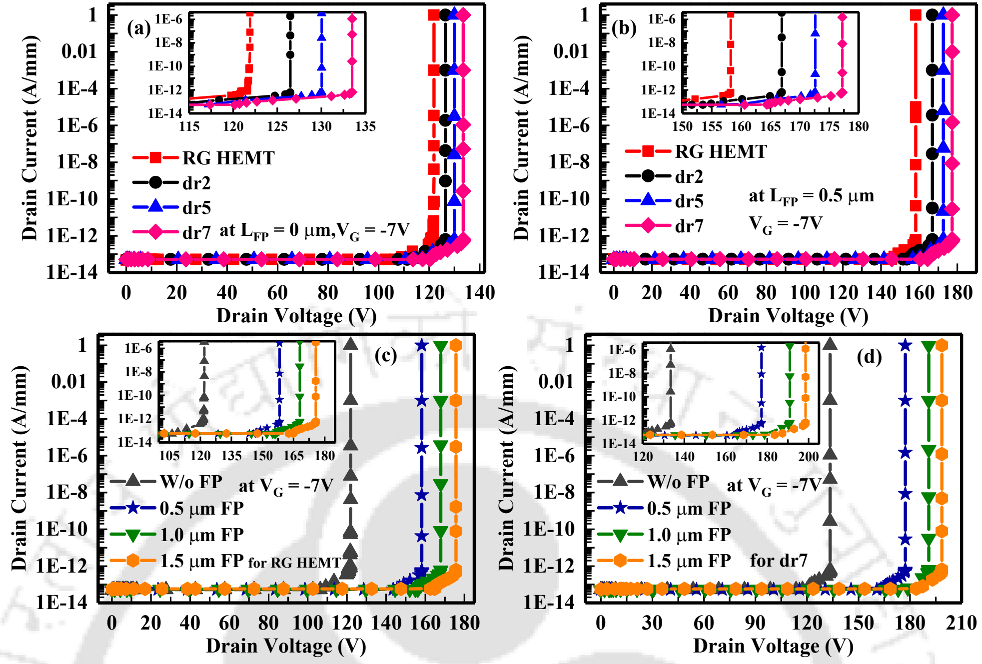

Figure 4.11: $I_D - V_D$ characteristics for Breakdown Voltage: (a) with different gate shape parameter 'dr', (b) with field plate length 'L_{FP}'= 0.5 μm and as gate shape parameter 'dr' vary, (c) for RG HEMT as 'L_{FP}' vary, and (d) Field plate length variation 'L_{FP}' for dr7

Table 4.7: Breakdown voltage, BV for the devices with different gate shape parameter 'dr' (RG HEMT, dr2, dr5, and dr7) for the scenario of without field plate and field plate length 'L_{FP}'=1.5 μm

Field Plate	Device Geometry	BV
L_{FP} = 0	RG HEMT	120 V
	dr2	126 V
	dr5	129 V
	dr7	133 V
L_{FP} = 1.5 μm	RG HEMT	175 V
	dr2	185 V
	dr5	190 V
	dr7	198 V

Fig. 4.12, it is indicative that the CV characteristics changes around the same gate voltage, which reaffirm the feature that threshold voltage of the devices (combination of rounded gate and field plate) is uniform. The magnitude of capacitance C_g dropping almost to 0 fF below V_G = -7 V suggests that the channel is depleted with electron or typically 2DEG [175]. Since threshold voltage of the devices is -5.8 V, it can also be inferred that below V_G = -7 V, devices are turned OFF. Similarly, when V_G surges toward 0 V, electron starts filling up the channel

and due to this C_g increases. It can be observed that depletion of channel (below V_G = -7 V), and accumulation of channel (as V_G > -7 V and moves toward 0 V) are clearly exhibited by the proposed device. The slight shift in the CV characteristics of rounded gate structure (Fig. 4.12 (a)) is a consequence of slanted nature of the gate as 'dr' increases, which effectively boosts the area under the gate electrode. The distinct vertical shift i.e., increase in the capacitance C_g as field plate is incorporated (Fig. 4.12 (b,c,d)) to the device structure is a consequence of increment of the area of gate electrode. The inflation in capacitance of field plate structure is in agreement with [156]. Thus, gate capacitance increases slightly in the rounded gate devices with and without field plate.

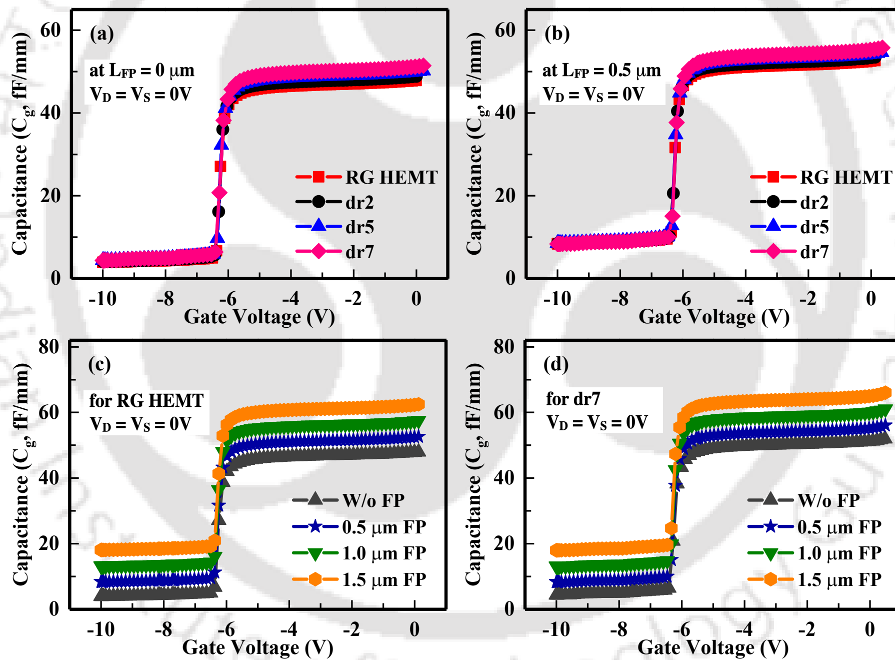

Figure 4.12: C_g vs V_G profile for AlGaN/GaN HEMT (at source voltage = drain voltage = 0V, and frequency = 1 MHz): (a) with different gate shape parameter 'dr', (b) with field plate length 'L_{FP}'= 0.5 μm and as gate shape parameter 'dr' vary, (c) for RG HEMT as 'L_{FP}' vary, and (d) Field plate length variation 'L_{FP}' for dr7

Similarly, as the gate voltage progresses towards 0 V from the negative value, C_{GD} suddenly jumps at a particular gate voltage as the depleted channel quickly replenishes. The peak in the jump is attributed to the device being in accumulation mode, where depletion region, which exists due to polarization charges, is non-existent at this point. As the gate voltage

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approaches 0 V, the depletion region due to polarization kicks in, and 2DEG depletes, which causes a reduction in C_{GD} (refer Figure 4.13 (a)). However, with the inclusion of field plate, the channel recovery occurs at a voltage lower than that of the voltage when no field plate is used. Consequently, it is observed that C_{GD} is higher as well as shoots up earlier for the devices with field plate (refer Figure 4.13 (b) & (c) & (d)).

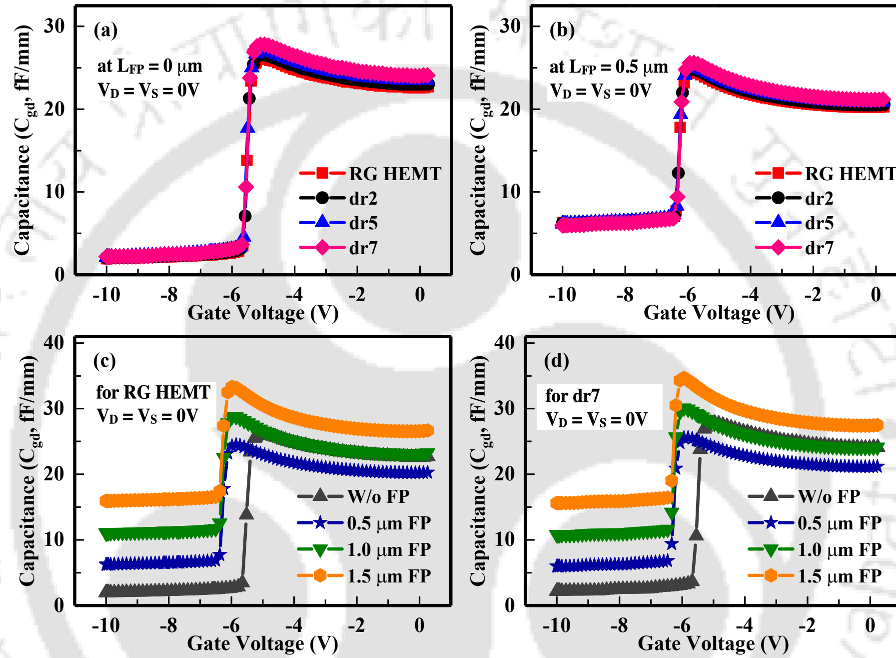

Figure 4.13: C_{gd} vs V_G profile for AlGaN/GaN HEMT (at source voltage = drain voltage = 0V, and frequency = 1 MHz): (a) with different gate shape parameter 'dr', (b) with field plate length 'L_{FP}'= 0.5 μm and as gate shape parameter 'dr' vary, (c) for RG HEMT as 'L_{FP}' vary, and (d) Field plate length variation 'L_{FP}' for dr7

Since AlGaN/GaN HEMT devices has wide applications in high frequency domain, it is essential to assess the effect of field plate on its frequency response. A comprehensive way to evaluate the frequency response is to estimate the change in unity current gain limit (f_m), when field plate is introduced in the device structure. This can be represented for the device structure under consideration as follows [2].

$$\frac{f_{m\mathrm{FP}}}{f_m} = \frac{1}{[1 + C_{\mathrm{FP}}/C_{\mathrm{g}}]^2} = \left[1 + \frac{L_{\mathrm{FP}}}{L}\right]^{-2} \tag{4.13}$$

where, f_m (f_{mFP}) is unity current gain limit (unity current gain limit due to field plate).

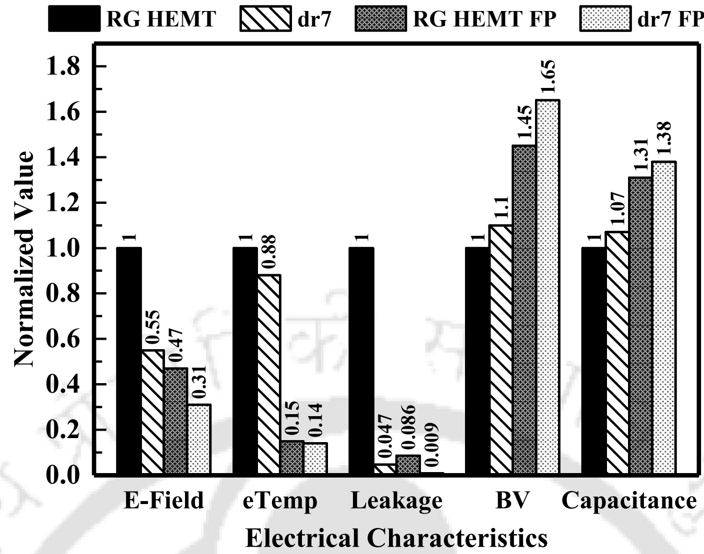

Figure 4.14: Representation of electrical characteristics (electric Field, electron temperature, leakage current, breakdown voltage, and capacitance C_g) of the rounded gate devices with/without Field plate. A comparison is drawn between RG HEMT (the benchmark), dr7, RG HEMT with field plate (RG HEMT FP), and dr7 with field plate (dr7 FP). The devices considered here have a field plate length, $L_{FP} = 1.5\ \mu$m

C_g is the gate capacitance and C_{FP} is the capacitance due to field plate. Since field plate is an extension of the gate, the capacitance due to the field plate just adds up to the gate capacitance [176]. Here, L is the length of channel. Thus, the field plate structure has a reduced unity current gain factor as compared to the structure without field plate and it further diminishes as 'L_{FP}' increases.

In this section, electrical characteristics of rectangular gate structure and rounded gate with/without field plate devices are presented. A concise representation of electrical characteristics of the devices is shown in Fig. 4.14. A comparison is drawn between the rectangular gate structure i.e., RG HEMT and rounded gate device structure dr7 with/without field plate. The electrical characteristics chosen for the comparison are electric field (at gate edge toward drain side), eTemperature (at gate edge toward drain side), leakage current, and capacitance (C_g). From Fig. 4.14, it is inferred that electric field, eTemperature (at gate edge toward drain side), and leakage current decrease in the rounded gate devices as compared to RG HEMT. A similar behaviour is exhibited when field plate is incorporated in these device structures.

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However, capacitance increases for the rounded gate devices as compared to RG HEMT. An additional increment with the introduction of field plate to the rounded gate devices is reported in the literature [156]. Also, on close inspection, it is quite evident that the rounded gate device without a field plate showcases a better electrical characteristics as compared to RG HEMT barring capacitance. Although the capacitance of the rounded gate devices increases, the magnitude/order of decrease in the electric field, eTemperature, and leakage current supersede the [nominal] increment in the capacitance. Therefore, rounded gate device is expected to have enhanced reliability as compared to RG HEMT. It may be highlighted that the rounded gate devices have almost the same threshold voltage and transconductance as RG HEMT, which further emphasizes the fact that the proposed device barely changes operating point regardless of subdued degradation phenomena.

4.4 Summary

In this work, rounded gate AlGaN/GaN HEMTs with and without field plate configuration are analyzed in detail to probe into their reliability aspect. In particular, it is observed that threshold voltage and transconductance have almost remained constant for the devices as gate shape is varied as well as when field plate is introduced to the device geometry. Leakage current reduces by an order of two, when device structure experiences change in the gate shape. It is to mention that incorporation of field plate in the devices leads to the reduction by an order of three in the leakage current. It can be attributed to the drop in trapping phenomenon near the gate edge. The moderation of electric field at the gate edge toward the drain side of rounded gate devices by $\sim$ 45% is due to diffusing effect that helps in easing electric field related degradation mechanism. Consequently, electron temperature is reduced at the gate edge by $\sim$ 12%. It is found that devices with field plate facilitate the spread of electric field toward the drain side in the gate-drain access region minimizing electric field at the gate edge by $\sim$ 68%.

For field plate structure, capacitance increases slightly as it adds up to the existing capacitance. However, the increment in capacitance for field plate structure as compared to the

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structure without field plate is nominal. The decrease of device degradation assisting mechanisms, such as, peak electric field and electron temperature at the gate edge as well as leakage current overpower the marginal increment in the capacitance(s) of rounded gate devices with or without field plate. This helps in enhancing reliability of the proposed device structure. The breakdown voltage of rounded gate device (dr7) is found to be 133 V, which is more than 10% as compared to the breakdown voltage of rectangular HEMT (RG HEMT). Further, with an incorporation of field plates to the devices, the breakdown voltage increases by 64% for dr7 with field plate. The increase in breakdown voltage for the rounded gate device thereby broaden its range of operations in power electronics applications. Among the candidates for rounded gate devices, dr7 is found to be reliable and it is inferred from the fact that degradation triggering factors, such as, electric field and electron temperature at the gate contact is suppressed comparatively in larger magnitude as compared to RG HEMT and other rounded gate devices, which in turn assist to improve reliability aspect of the device. This makes the rounded gate AlGaN/GaN HEMT with or without field plate as a suitable candidate for any high power application necessitating high reliability of the devices.

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5

Converse Piezoelectric Strain Moderation with variation in gate geometry

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5.1 Introduction

The rapid development of AlGaN/GaN high electron mobility transistors (HEMTs) has accelerated its deployment in high-speed and commercial high power applications [177]. However, the full capability of AlGaN/GaN HEMTs is limited by several reliability issues arising due to the material properties of constituent semiconductors [178]. Initiation of converse piezoelectric (CPE) strain inside AlGaN barrier layer of AlGaN/GaN HEMT is one of the critical reliability concerns. This effect amplifies when an AlGaN/GaN HEMTs is operated in the OFF-state. In particular, the rectangular gate HEMTs suffer from high electric field near the gate edge towards the drain. This triggers CPE-strain in the AlGaN barrier layer under the gate [88, 143]. At the instant, when the accumulated elastic energy due to CPE-strain becomes high and well above a threshold value, defects are created in the AlGaN layer as CPE-strain relaxes. Such defects under the influence of high electric field can act as charge trap locations inside AlGaN barrier layer [33, 88]. This lowers concentration of electrons in 2-dimensional electron gas (2DEG) and degrades ON-state drain current of a HEMT [179]. The defects initiated by CPE-strain can generate a leakage route in between gate and channel, and contributes to the gate leakage current [143]. In certain scenarios, CPE-strain induced defects can actually trigger complete failure of a device [88, 179]. The electrons after picking up energy from an elevated electric field, which exists at the gate edge, become hot. These energetic electrons are instrumental in influencing several degradation parameters like creation of traps and increasing leakage current [87, 180]. Thus, it is imperative to frame guidelines to reduce electric field for further lowering CPE-strain and eTemp in high power AlGaN/GaN HEMTs.

In continuation to our preceding work, in this chapter, we investigate the behaviour of CPE-strain and eTemp in AlGaN/GaN HEMTs as gate geometry is modified from a rectangular gate structure to staircase gate geometry and rounded gate geometry. Numerical analysis is performed using a 2-dimensional device structure to observe the profile of electric field and CPE-strain along the channel and gate edge. It is found that the proposed rounded gate (FG) HEMT exhibits better performance in comparison with the other gate designs to lower CPE-

Table 5.1: Material parameters used in TCAD numerical analysis [6]

S. No.	Material property	Unit	GaN	AlGaN
1	Electron Mobility	cm^2/Vs	1200	300
2	Bandgap	eV	3.50	4.39
3	Electron Affinity	eV	4.0	3.41
4	Relative Permittivity	-	8.9	8.8
5	Electron Saturation Velocity	cm/s	2.5×10^7	1.1×10^7
6	Electron Conduction Band Density of States (DOS)	cm^{-3}	2.23×10^{18}	2.71×10^{18}
7	Electron Valence Band Density of States (DOS)	cm^{-3}	2.51×10^{19}	2.06×10^{19}

strain. The analysis reported in this chapter depicts the significance of altering gate shape to suppress eTemp and CPE-strain induced damages in AlGaN/GaN HEMTs.

5.2 Numerical Analysis Framework / Physical Model

Alamo et al. observe that with gate geometry modification, electric field at the gate edge reduces [88]. Endoh et al. report that in a staircase (SG) HEMT, electric field at the gate edge reduces as it moves toward substrate because of modified gate geometry [181]. In this work, we propose a rounded gate (FG) HEMT geometry that further reduces the peak electric field at the gate edge. Three $Al_{0.25}Ga_{0.75}N$/GaN HEMTs namely, (a) rectangular gate (RG), (b) staircase gate (SG) and (c) rounded gate (FG) are considered as shown in Fig. 5.1. The numerical analysis is performed using Sentaurus-TCAD [68]. All the above mentioned devices have a gate length, gate-to-source, and gate-to-drain spacing of 1.5 μm, 1.5 μm, and 3.0 μm, respectively. The gate shape parameter (dr) is considered as 0.05 μm for FG HEMT. It is to mention that this is an optimum value and gate does not look like as a slanted gate. In the SG HEMT, dimensions are 0.02 μm for horizontal stairs and 0.025 μm for vertical stairs.

The numerical analysis was carried out with drift-diffusion (DD) and hydrodynamic (HD) transport model to study CPE-strain and eTemp, respectively. The other models included in the numerical analysis framework are Shockley-Read-Hall (SRH) generation-recombination and carrier mobility model. The contacts are considered as ohmic for source and drain, and

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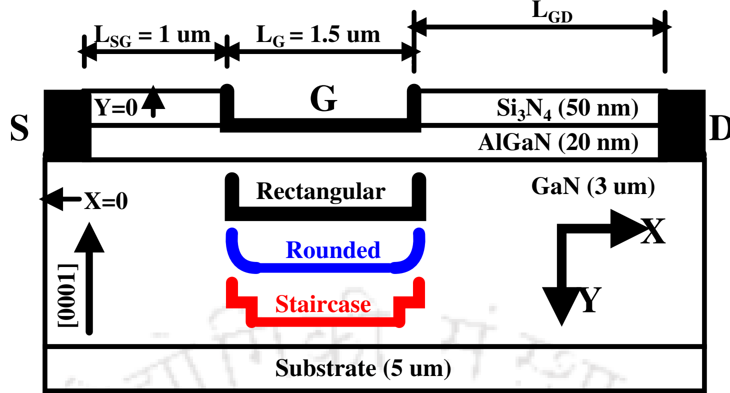

Figure 5.1: Schematic of the devices namely, rectangular (RG), staircase (SG), and rounded gate (FG) HEMT considered in this work. Gate terminal is not shown as solid to showcase the gate geometry of the devices under consideration. The X-axis lies in the basal plane, and Y-axis runs along the (negative) $c - axis$

Schottky for the gate terminal. The metal-semiconductor work function (ϕ_{ms}) is considered as 0.9 eV for the Schottky contact. The anisotropic model is also incorporated in the numerical analysis framework to account asymmetry of GaN crystal structure along the $c - axis$. The material parameters used in the numerical analysis framework are listed in Table 5.1. The charge generation at AlGaN/GaN interface is taken into consideration with the polarization model in the numerical analysis framework. For evaluating CPE-strain, the following model is considered.

$$[\varepsilon_i]_{6\times1} = [d_{ij}]_{6\times3} [E_j]_{3\times1} \quad (i = 1, 2, ..., 6; \; j = 1, 2, 3) \tag{5.1}$$

where, ε, d, and E represent a strain matrix (dimension-less), converse piezoelectric effect coefficient (m/V), and electric field (V/m), respectively [68].

GaN and AlGaN are thermodynamically stable wurtzite hexagonal close-packed crystal structure [87]. As AlGaN (having smaller lattice constant as compared to GaN) layer is grown on the top of GaN, a tensile strain develops in the AlGaN layer, which gets uniformly distributed in the basal plane of AlGaN/GaN to match lattice constant of GaN [143]. Additional details regarding the numerical analysis framework can be found in [33,68,148]. The numerical analysis is performed under the bias conditions, in which V_{DS} is fixed at 20 V and V_{GS} is –6 or 0 V according to device's OFF/ON state, respectively.

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The following model is incorporated in the numerical analysis framework for the converse piezoelectric strain.

$$\begin{bmatrix} P_x \\ P_y \\ P_z \end{bmatrix} = \begin{bmatrix} P_x^{sp} \\ P_y^{sp} \\ P_z^{sp} + P_{strain} \end{bmatrix} \tag{5.2}$$

where, $P_{x/y/z}^{sp}$ denotes spontaneous polarization vector (C/cm^2) in x, y, and z-axes, respectively. P_{strain} is piezoelectric strain, which is expressed below.

$$P_{strain} = 2d_{31} \cdot strain \cdot \left(c_{11} + c_{12} - 2c_{13}^2/c_{33}\right) \tag{5.3}$$

where, d_{31} is piezoelectric coefficient (cm/V), and c_{ij} are the stiffness constant (Pa). The *strain* can be further simplified as mentioned below.

$$strain = (1 - r) \cdot (a_0 \; - \; a)/a \tag{5.4}$$

where, a_0, a are strained and unstrained lattice constant (A°), respectively, and r is a relaxation parameter.

After inclusion of above mentioned model in the numerical analysis framework, piezoelectric charge, q_{PE}, is computed as mentioned below.

$$q_{PE} = - \; P_{activation} \bigtriangledown P \tag{5.5}$$

where, $P_{activation}$ is parameter that helps in the calibration of piezoelectric charge. Its default value is 1. The piezoelectric charge, q_{PE} adds up to Poisson equation. The modified Poisson equation is stated below.

$$\bigtriangledown \epsilon \cdot \bigtriangledown \phi = -q \left(p - n + N_D - N_A + q_{PE}\right) \tag{5.6}$$

Here, all the letters have their usual meaning. High electron temperature is considered as a factor that assists in the leakage current and other defects of a HEMT. To model this effect,

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we include the following terms in the numerical analysis framework for analysis.

$$\overrightarrow{J_n} = \mu_n \left(n\nabla E_C + kT_n \nabla n - nkT_n \nabla \ln \gamma_n + \lambda_n f_n^{td} kn \nabla T_n - 1.5nkT_n \nabla \ln m_n \right) \tag{5.7}$$

$$\overrightarrow{J_p} = \mu_p \left(p\nabla E_V - kT_p \nabla p + pkT_p \nabla \ln \gamma_p - \lambda_p f_p^{td} kp \nabla T_p + 1.5pkT_p \nabla \ln m_p \right) \tag{5.8}$$

In the above mentioned equations (Eq. 5.7 and 5.8), the first term ($n\nabla E_C$ and $p\nabla E_V$) estimates spatial variation of the band gap, electron affinity and electrostatic potential, respectively. The second term ($kT_n\nabla n$ and $kT_p\nabla p$) captures concentration gradient and the third term ($nkT_n\nabla\ln\gamma_n$ and $pkT_p\nabla\ln\gamma_p$) is related to Fermi statistics, where $\gamma_n = (n/N_C)\ exp\ ((E_C - E_{F,n})\ /kT)$ and $\gamma_p = (p/N_V)\ exp\ ((E_{F,p} - E_V)/kT)$. The fourth term ($\lambda_n f_n^{td} kn\nabla T_n$ and $\lambda_p f_p^{td} kp\nabla T_p$) is imperative for the hydrodynamics model, which captures temperature gradient of the carriers. It is to mention that constants f_n^{td} and f_p^{td} are thermal diffusion parameters. Spatial variation in the effective masses is taken into consideration by the last term ($1.5nkT_n\nabla\ln\ m_n$ and $1.5pkT_p\nabla\ln\ m_p$). In the next section, detailed discussion on the outcome of numerical analysis is presented.

5.3 Results and Discussion

In this section, details of current–voltage characteristics, electric field profile, converse piezoelectric strain, electron temperature profile and breakdown voltage are depicted for various device structures.

5.3.1 Current–Voltage Characteristics

The current-voltage characteristics of the devices are shown in Fig. 5.2. It is observed that drain current varies slightly and threshold voltage for the devices are found to be same, i.e., -5.8 V. The slight variation in the drain current is due to the reduced strain at the gate edge of the devices, which can be related to subdued electric field at the gate edge. The details about electric field and strain are stated in the succeeding sections.

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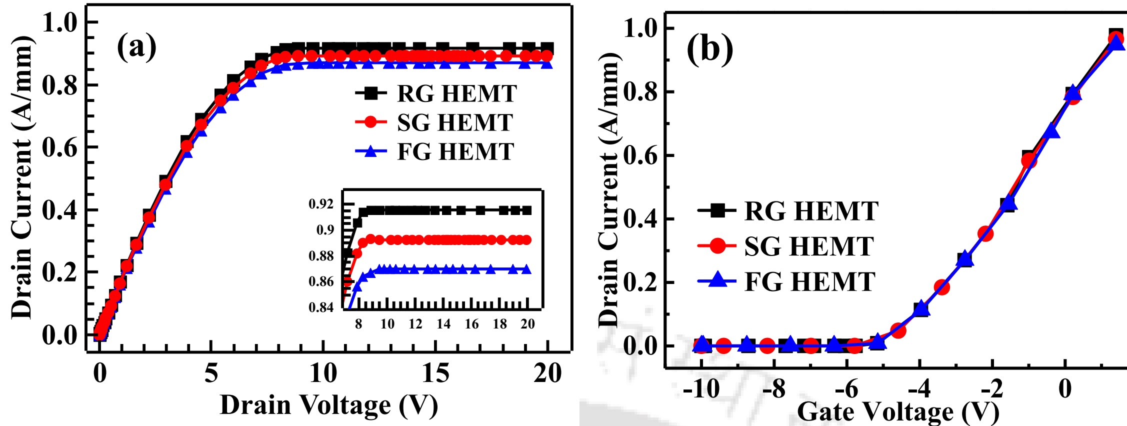

Figure 5.2: (a) I_D v/s V_{DS} characteristics at V_G = 0V, and (b) I_D v/s V_{GS} characteristics at V_D = 5V of the devices

5.3.2 Electric Field Profile

In the RG HEMTs, electric field crowding is observed at the gate edge, which is attributed either to the sharp gate edge or corners. The electric field along the channel of devices in the OFF-state is shown in Fig. 5.3. Fig. 5.3(a) and Fig. 5.3(b) depict the vertical electric field ($E_{Vertical}$) and absolute electric field profiles ($E_{Absolute}$) of the devices, respectively. Although an electric field peak at the gate edge is observed in all the devices (RG/SG/FG HEMT), the magnitude of peak electric field decreases in SG and FG HEMTs as compared to RG HEMT.

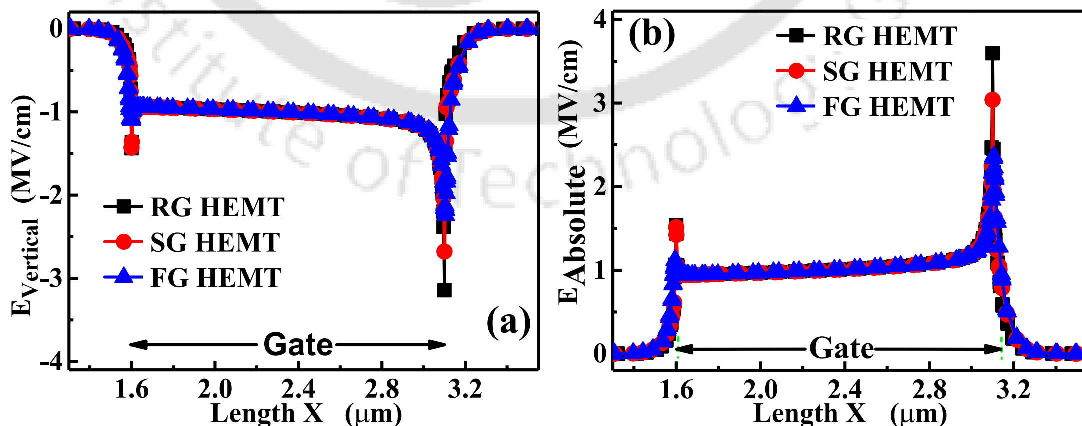

Figure 5.3: Distribution of (a) vertical and (b) absolute electric field under the gate of simulated HEMT structures in the OFF-state

This is due to enhanced dispersion of electric field at the gate edge of SG and FG HEMT.

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In SG HEMT, two edges of a staircase helps in diffusing electric field away from the gate edge and due to this electric field crowding is minimized. Similarly, diffusion of electric field in FG HEMT is observed to be further enhanced. $E_{Vertical}$ of the devices when operated in the OFF-state is found to be reduced by 14.65% and 24.84% in SG and FG HEMT, respectively, as compared to RG HEMT. Similarly, $E_{Absolute}$ at the gate edge are 15.59%, and 34.26% lower in SG and FG HEMT, respectively, than RG HEMT in the OFF-state.

5.3.3 Converse Piezoelectric Strain

AlGaN and GaN exhibit piezoelectric and converse piezoelectric effects as they belong to wurtzite crystal family. Piezoelectric effect is due to residual or inbuilt strain, while converse piezoelectric effect originates when electric field is developed due to biasing [88]. Both piezo-electric and converse piezoelectric effects result in the generation of strain in a device. It has been reported that a slight increase, such as 0.076%, in uni-axial strain decreases critical voltage from 25V to 20V [171]. Additionally, converse piezoelectric strain adds to existing piezoelectric strain and triggers device degradation and failures [33, 88, 143, 171, 182].

The primary contributing factor for CPE-strain is vertical electric field [88,143]. The density of stored elastic energy depends on the vertical electric field and varies linearly at the gate edge of a device [143]. Besides, high electric field and high strain field near the gate edge along with gate leakage current promote diffusion in the device. Here, diffusion is denoted as an advanced stage of device degradation, which includes electro-chemical reactions as well. The onset of diffusion generally happens at a dislocation, which gets accelerated by gate leakage currents, CPE-strain and electric field on the drain side of gate edge [4]. Hence, the reduction of peak vertical electric field in a FG HEMT lowers CPE-strain of a device and enhances its reliability. Fig. 5.4 illustrates profile of CPE-strain of the devices. The CPE-strain is categorised as planar and vertical [143]. CPE_{XX} and CPE_{YY} fall under the category of planar CPE-strain, while CPE_{ZZ} is the vertical CPE-strain. It is to mention that FG HEMT exhibits reduced CPE_{XX}, CPE_{YY} and CPE_{ZZ}. This behaviour of FG HEMT can be related to an electric field profile of a device. Further, it is found that the peak CPE_{ZZ} strain in FG HEMT is 25% less

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as compared to RG HEMT.

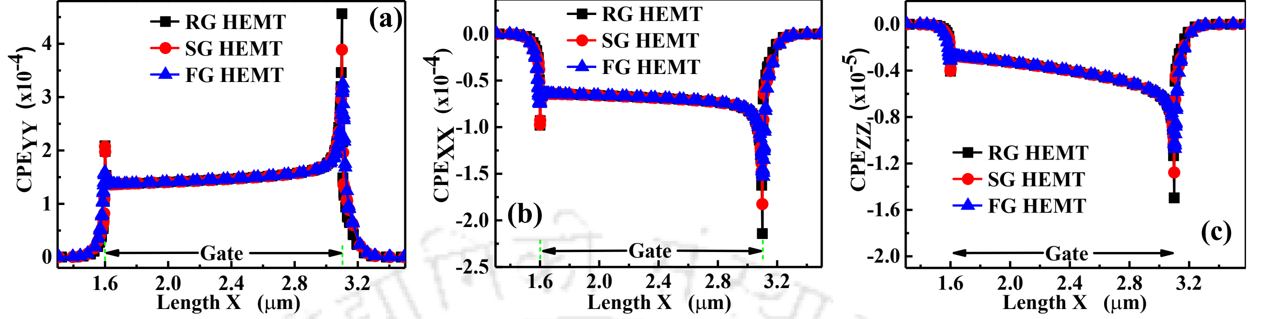

Figure 5.4: (a) and (b) Planar, and (c) vertical CPE-strain observed in the OFF-state of the devices

Since CPE-strain is a strong function of the gate bias [143], it is essential to examine variation of CPE-strain with respect to gate bias of the devices as shown in Fig. 5.5. The general trend remains same for the devices, i.e. CPE-strain decreases as gate bias decreases. At a given gate bias, FG HEMT has lower CPE-strain as compared to RG HEMT and SG HEMT. For a device, the accumulated elastic energy depends on the electric field at the gate edge [143]. Therefore, FG HEMT is expected to have the least accumulated elastic energy.

5.3.3.1 Analytical Analysis of Converse Piezoelectric Strain

In the device structure shown in Fig. 5.1, AlGaN layer is grown on the top of GaN layer, which means that the lattice constant of both the layers must match at the interface. However, lattice constant of AlGaN is smaller than GaN, and as a result AlGaN layer experiences strain in the basal plane (xy-plane) as lattice constant tries to match with an underlying GaN layer. This basal plane strain is denoted as mention below.

$$\epsilon_1 = \frac{a(0) - a(x)}{a(x)} \tag{5.9}$$

Here, $a(0)$ is lattice constant of unstrained (relaxed) GaN layer and $a(x)$ is lattice constant of $Al_xGa_{1-x}N$ as a function of Al mole-fraction, x in the layer. The symmetry of crystals in the basal plane results in redistribution of strain uniformly in x and y directions, i.e., $\epsilon_1 = \epsilon_2$ [183], where ϵ_1 and ϵ_2 represent strain in x and y directions, respectively. In a wurtzite crystal, strain

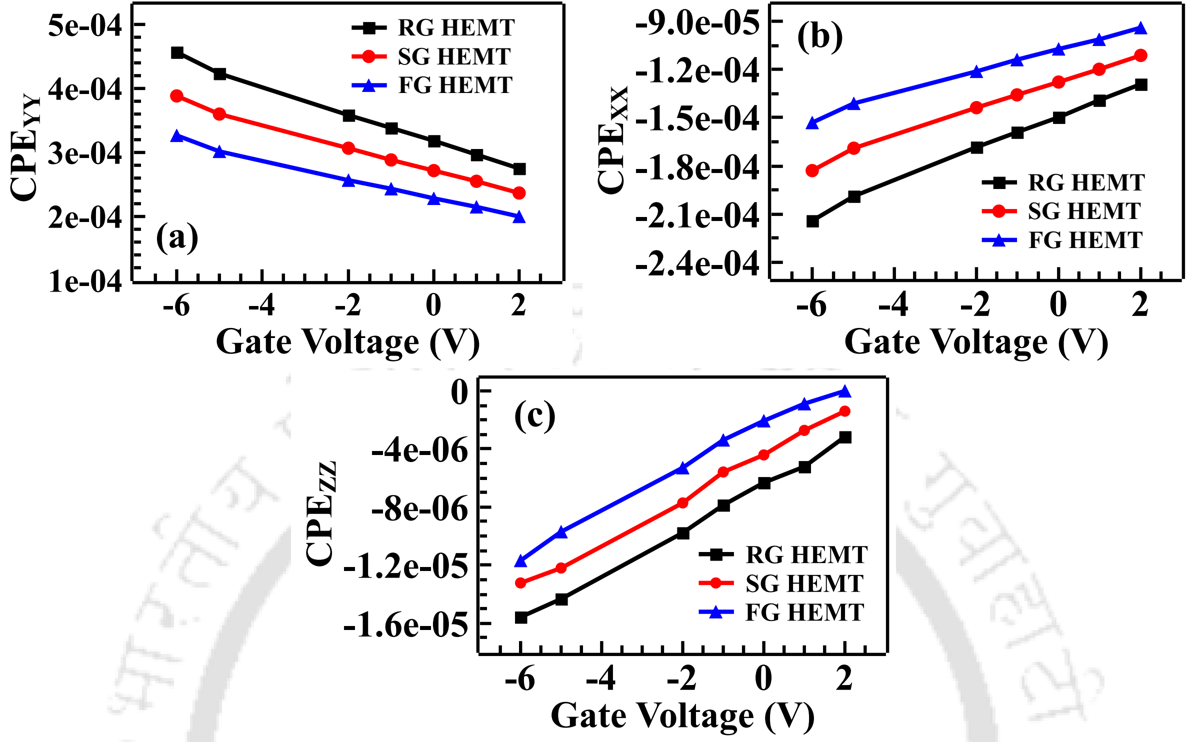

Figure 5.5: (a) and (b) Planar, and (c) vertical CPE-strain variation with gate bias of the devices

is responsible for the piezoelectric effect, which can be denoted in matrix form below.

$$e = \begin{pmatrix} 0 & 0 & 0 & 0 & e_{15} & 0 \\ 0 & 0 & 0 & e_{24} & 0 & 0 \\ e_{31} & e_{32} & e_{33} & 0 & 0 & 0 \end{pmatrix} \tag{5.10}$$

Additionally, in wurtzite crystal only five piezoelectric constants are non-zero due to crystal symmetry, $e_{24} = e_{15}$ and $e_{32} = e_{31}$. Hence, the above matrix can be simplified as

$$e = \begin{pmatrix} 0 & 0 & 0 & 0 & e_{15} & 0 \\ 0 & 0 & 0 & e_{15} & 0 & 0 \\ e_{31} & e_{31} & e_{33} & 0 & 0 & 0 \end{pmatrix} \tag{5.11}$$

On the other hand, piezoelectric constant e_{15} is related to shear strain, which does not contribute to the polarization and can be assumed as $e_{15} = 0$ [183]. Thus, the piezoelectric matrix is

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$$e = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ e_{31} & e_{31} & e_{33} & 0 & 0 & 0 \end{pmatrix} \tag{5.12}$$

From the above matrix, it can be inferred that three non-zero elements, i.e. e_{31}, e_{31} and e_{33}, estimate piezoelectric polarization [42]. The piezoelectric polarization vector (along the c-axis) can be represented as mentioned below with assumption that $\epsilon_1 = \epsilon_2$ as stated earlier.

$$P_{3,pz} = e_{31}(\epsilon_1 + \epsilon_2) + e_{33}\epsilon_3 = 2e_{31}\epsilon_1 + e_{33}\epsilon_3 \tag{5.13}$$

Similarly, strain in Eq. 5.13 can be related as

$$\epsilon_3 = -2\frac{C_{13}}{C_{33}}\epsilon_1 \tag{5.14}$$

where, C_{13} and C_{33} are crystal's stiffness constants. Substituting Eq. 5.14 in Eq. 5.13, following mathematical expression can be obtained.

$$P_{3,pz} = 2\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right)\epsilon_1 \tag{5.15}$$

This piezoelectric polarization vector adds to the spontaneous polarization and is responsible for the charge at AlGaN/GaN interface. The aforementioned expression (Eq. 5.15) is derived without considering converse piezoelectric strain that arises due to vertical electric field. To include converse piezoelectric strain, corresponding stress should be considered. As we know, the vertical electric field gives rise to the stress, which is responsible for converse piezoelectric strain. Moreover, the stress and strain are related, which can be expressed in Vigot's notation as [141] stated below.

$$\sigma_i = C_{ij}\epsilon_j - e_{ki}E_k \qquad (i, j = 1, 2, ..., 6;\ k = 1, 2, 3) \tag{5.16}$$

where, σ, ϵ, e and E represent stress, strain, piezoelectric constant and electric field, respec-

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tively. Using clamped model [141] in Eq. 5.16, planar stress can be denoted as

$$\sigma_2 = \sigma_1 = (C_{11} + C_{12})\epsilon_1 + C_{13}\epsilon_3 - e_{31}E_3 \tag{5.17}$$

Similarly, ϵ_3 in Eq. 5.17 can be substituted with ϵ_1. Using Eq. 5.16, stress along c-axis, σ_3, is denoted as

$$\sigma_3 = 2C_{13}\epsilon_1 + C_{33}\epsilon_3 - e_{33}E_3 \tag{5.18}$$

Also, the stress along c-axis is assumed to be zero, i.e., $\sigma_3 = 0$. Therefore, Eq. 5.18 is re-arranged as

$$\epsilon_3 = -2\frac{C_{13}}{C_{33}}\epsilon_1 + \frac{e_{33}}{C_{33}}E_3 \tag{5.19}$$

Eq. 5.19 reduces to Eq. 5.14 when vertical electric field is absent, i.e., $E_3 = 0$. Under this condition, a negative stress signifies that the interface experiences compressive strain along z-axis. Substituting ϵ_3 from Eq. 5.19 in Eq. 5.17, the following expression can be formulated.

$$\sigma_2 = \sigma_1 = \left(C_{11} + C_{12} - 2\frac{C_{13}^2}{C_{33}}\right)\epsilon_1 + \left(\frac{C_{13}}{C_{33}}e_{33} - e_{31}\right)E_3 \tag{5.20}$$

The above equation denotes the influence of vertical electric field, E_3, on the planar stress. Thus, as electric field moderates in SG and FG HEMTs, stress too follow the similar trend. While comparing three device structures, FG HEMT possess the least vertical electric field at the gate edge, which leads to the minimum stress in the device. Additionally, SG HEMT exhibits reduced vertical electric field than RG HEMT at the gate edge, therefore, stress is observed to be lower as well. It is evident that the trend of decrease in CPE-strain at the gate edge of devices closely follow vertical electric field peak, as listed in Table 5.2.

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Table 5.2: Vertical Electric Field and CPE-Strain of RG, SG, and FG HEMT in OFF-state

Device	$E_{Vertical}$ (MV/cm)	CPE_{ZZ} (10^{-4})
RG HEMT	-3.14	-1.56
SG HEMT	-2.68 ($\downarrow$ 14.65%)	-1.32 ($\downarrow$ 15.38%)
FG HEMT	-2.36 ($\downarrow$ 24.84%)	-1.17 ($\downarrow$ 25.00%)

5.3.4 Electron Temperature Profile

AlGaN/GaN HEMTs are known to experience a range of degradation mechanisms. Hot electrons or electron with higher temperature increases trap density under gate and gate-drain access region [90]. Besides, electron energy is reported to be a contributing factor for the negative differential output conductance (NDC) in a device, regardless operational power. Moreover, NDC is due to hot electron being captured in bulk traps [90, 184]. This indicates that electron temperature plays far more crucial role in device degradation than lattice temperature. These hot electrons are also responsible to shift breakdown voltage of a device [184]. Moreover, it is assumed that degradation/failure in AlGaN barrier layer is primarily due to electron injection. The localized strain and/or electron temperature further accelerate the damage due to electron injection. Hence, it is expected that the combined effect of damages due to elevated temperatures and/or electron injection weaken the barrier layer. The electric field at/under gate creates a thin Fowler Nordheim injection barrier of $\sim$ 3 nm. Further, long term device degradation occurs, when the device is subjected to slow electron injection at elevated temperature and stress [89]. The high stress may activate chemical processes like impurity diffusion, which can further degrade device [185]. Although, it is widely anticipated that stress at the drain side of the gate edge is responsible for structural failure, and it is observed that piezoelectric stress accounts for about half in it, while the other half is contributed by thermal stress. However, this stress is not sufficient to trigger any direct structural failures, such as, formation of pit or crack unless device is under strong electron injection and/or high operating temperature, which may lower the threshold of material failure. It is experimentally observed, when a device

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is stressed in high power bias condition results in the formation of pits and/or cracks in AlGaN barrier layer [186, 187].

In Fig. 5.6, electron temperature profile of the devices is shown. The electron temperature decreases as the gate geometry changes from RG HEMT to FG HEMT. The electron temperature peak at gate edge of RG HEMT, SG HEMT, and FG HEMT are found to be 523.4 $\times$ 10^4 K, 488.33 $\times$ 10^4 K, and 423.18 $\times$ 10^4 K, respectively. Hence, the reduction in peak electron temperature at the gate edge toward the drain side are 6.7% and 19.14% for SG HEMT and FG HEMT, respectively as compared to RG HEMT.

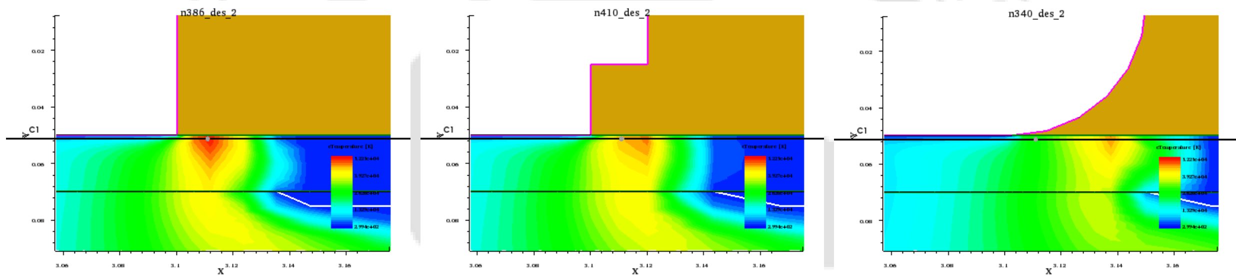

Figure 5.6: Electron Temperature profile of the devices at V_G= -6 V and V_D = 20 V

5.3.5 Breakdown Voltage

Breakdown is the manifestation of thermal runaway in a device, when power dissipation exceeds a particular threshold [188]. Generally, this occurs when a device is subjected to high drain voltage in the OFF-state, which results in the exposure of gate-drain junction to a high reverse bias. Moreover, it is reported that an AlGaN/GaN HEMT experiences time dependent failure i.e., an AlGaN/GaN HEMT, which has breakdown voltage higher than 1000 V exhibits time dependent failure, when gets exposed to the OFF-state stress at drain voltage of 600–700 V. Additionally, time to failure (TTF) is exponentially dependent on the strength of stress voltage and follows Weibull distribution [189]. Similarly, this time dependent breakdown of the device is due to the failure of SiN passivation/dielectric layer because electric field exceeds dielectric strength of SiN. Reduction of electric field strength in SiN by process improvements increases TTF by three orders of the magnitude [190].

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As stated in the earlier section that hot electrons are responsible for the shift in breakdown voltage, it is essential to understand its role on the breakdown voltage of RG/SG/FG HEMTs. The breakdown voltage of the devices are extracted and are tabulated in Table 5.3. The breakdown voltage is extracted, when a device is biased at V_{GS} = -6 V and V_{DS} = 20 V. It is evident that as electron temperature of the devices decreases in SG HEMT and FG HEMT as compared to RG HEMT, the breakdown voltage increases accordingly. Hence, decrease in electron temperature translates as an increase in breakdown voltage of the devices.

Table 5.3: Breakdown Voltage of RG, SG, FG HEMT

Device	Breakdown Voltage (V)	(% Change)
RG HEMT	120	–
SG HEMT	124	↑ 3.33%
FG HEMT	129	↑ 7.50%

Ancona et al. [89] stated that degradation centres initiate the process of defect creation at localized sites, where electric field, converse piezoelectric strain and electron temperature are maximum. In the proposed FG HEMT, since electric field, converse piezoelectric strain and electron temperature are reduced at the gate edge as compared to RG HEMT and SG HEMT, it is anticipated that localized defect creation is minimum,which reduces degradation phenomena. Detailed peak vertical/absolute electric field and CPE-strain of the devices in both the bias conditions (OFF and ON states) are tabulated in Table 5.4.

5.4 Summary

A comparative study of converse piezoelectric strain, electric field distribution and electron temperature for three different gate geometries are depicted in this chapter. The vertical converse piezoelectric strain, peak vertical electric field, electron temperature of FG HEMT geometry is observed to be lowered by 25%, 24.84%, and 19.34%, respectively as compared to RG HEMT. While comparing with RG HEMT, the reduction in vertical converse piezoelectric strain, peak vertical electric field, electron temperature of SG HEMT are 15.38%, 14.65%, and

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Table 5.4: Electric field, and CPE-strain of RG HEMT, SG HEMT, and FG HEMT at gate edge in both the bias condition

State	Parameter	RG	SG	FG
OFF	$E_{Vertical}$ (MV/cm)	–3.14	–2.68	–2.36
	$E_{Absolute}$ (MV/cm)	3.59	3.03	2.36
	CPE_{XX} (10^{-4})	-2.14	-1.83	-1.53
	CPE_{YY} (10^{-4})	4.56	3.89	3.26
	CPE_{ZZ} (10^{-5})	-1.56	-1.32	-1.17
ON	$E_{Vertical}$ (MV/cm)	-2.19	-1.87	-1.51
	$E_{Absolute}$ (MV/cm)	2.51	2.13	1.66
	CPE_{XX} (10^{-4})	-1.37	-1.21	-1.04
	CPE_{YY} (10^{-4})	2.93	2.58	2.22
	CPE_{ZZ} (10^{-5})	-1.37	-1.21	-1.04

6.7%, respectively. Although SG HEMT is observed to be better than RG HEMT in terms of the aforementioned parameters, FG HEMT outperforms both SG HEMT and RG HEMT. The comparative study presented here outlines the fact that the degradation promoting parameters are significantly reduced by changing gate structure, whereby performance of the devices gets enhanced. The proposed rounded gate, FG HEMT may find applications typically in the areas, that requires to be operated at high voltages, thus dissipating a significantly higher power, a condition generally observed in the power device applications.

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6

Access Region Stack Engineering for Mitigation of Degradation in AlGaN/GaN HEMTs with Field Plate

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6.1 Introduction

The material properties of AlGaN/GaN, such as wide bandgap, high electron mobility and high critical voltage are very attractive as compared to popular Silicon based technology [191, 192]. The distinct feature of GaN epi-structure is the emergence of two dimensional electron gas (2DEG) at an interface of AlGaN/GaN on the account of spontaneous and piezoelectric polarization. This confinement of electrons results into a channel having higher carrier density even without any doping or gate bias. A significant technological advantage of this heterostructure is the ability to maintain these properties even when it is grown on non-native substrates, such as Silicon, Sapphire or Silicon Carbide (SiC) etc., which contributes further to crystallographic defects in it. The exceptional attribute of thermal conductivity and semi-insulating nature of SiC as a substrate enables application of AlGaN/GaN HEMTs in RF power domain.

The wide bandgap property of AlGaN/GaN HEMT allows its operation at a high voltage, which generates tremendous electric field at the drain side of gate edge. This electric field crowding triggers degradation phenomenon, such as avalanche breakdown and thermally-assisted tunnelling in AlGaN/GaN HEMT [167]. When a device operates at high electric field, tensile stress enhances in AlGaN barrier layer, which further increases its elastic energy. After a critical value, this elastic energy gradually relaxes with the development of crystallographic defects, which acts as conduction paths, and reduces the drain current [88]. This phenomenon is known as inverse piezoelectric effect (IPE) and is described in [33, 193]. The effect of strong electric field can be observed in the vicinity of gate edge. Transmission Electron Microscopy (TEM) studies have revealed cracks and pits in the AlGaN surface near gate edge [186]. Additionally, the order of drain current degradation is correlated to the depth of damage (pits and cracks) [194–198]. Although IPE has been observed experimentally, Joh et al. [143] proposed a numerical analysis for modelling this effect based on an electromechanical model (2-D electrostatic simulation) with reasonable agreement to the experimental observations.

Electrical damages, such as drain current and transconductance reduction, slight shift in

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threshold voltage, and an increase in trapping activity without any trace of structural damages are observed when a devices is biased in the ON-state [30, 199]. This phenomenon is attributed to hot electron effect induced degradation [30] and is significant even at an average channel current. It is well corroborated through the observation of electroluminescene investigations [30]. The degradation due to hot electrons may be accelerated by pre-existing defects, which absorb energy and become electrically mobile. As we know that the electric field concentrated at a particular point influences device reliability, it is well-known that electric field affects physical properties of a device, such as, built-in strain, converse piezoelectric-electric strain, and critical voltage [32]. Additionally, electric field initiates avalanche breakdown and thermally-assisted tunnelling in the device [167]. Moreover, the rise in carrier temperature leads to hot electron induced device degradation, which plays a pivotal role in determining device reliability [160,161].

Any significant rise in the carrier temperature at the edge of field plate results in the migration of carriers, which creates traps, defects due to piezoelectric stress or dislocations in the vicinity of field plate edge towards the drain access region. This affect device stability and may initiate device breakdown [164]. Similarly, as heat diffuses from the hot spot region to other areas, thermal stress arises in AlGaN and GaN layer [179]. This assists degradation mechanisms in AlGaN/GaN HEMTs, which are initiated and accelerated thermally [143]. So, it is essential to mitigate the hot electron degradation with efficient electric field engineering that can be achieved with device designs, such as gate edge modification, field plates, and slanted gates etc. [2, 89, 148, 200]. Field plate technology is widely used for the moderation of electric field at the drain edge of a gate, which results in a uniform distribution of electric field in the gate-drain access region. Several variations of field plate technology are reported in literature, such as gate connected [2, 116, 118, 119, 201], source connected [121, 122, 202, 203], and drain connected [123–126, 204] field plates. The field plate topology is known to shape electric field profile at the drain edge of gate, which improves breakdown voltage of the devices as well [2, 205]. When a device is operated in the OFF state, electric field peaks at the drain edge of the gate and with an introduction of the field plate(s), electric field peaks appear at

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their edges.

Subramani et al. [6] observed that the electric field peaks at an edge of the field plate in the OFF state. Liao et al. [206] had similar observation in their work. Prior work and their observations are enlisted in Table 6.1, which corroborate the fact that no study/analysis on the heat profile at the field edge is performed earlier. It is well-known that the localized electric field in the OFF state facilitates localized electron temperature hotspots. Although literature is well versed with the heat profile study on the semiconductor devices at the gate edge, it is equally essential to investigate heat profile at the field plate edge and put forward solution to mitigate the same. With known prominence of hot electron degradation and its correlation with electric field peak, it can be inferred that slight reduction in the peak electric field strength can decrease peak temperature at localized spot improving device reliability and lifetime [160, 161, 200].

Table 6.1: Prior Works and their observation

S. No.	Author	Observation
1	Meneghesso et al. [30]	Reported the electroluminescene in the SEMI-ON state signifying peak electron temperature in that state.
2	Subramani et al. [6]	Observed electric field peak at the edge of field plate in the OFF state.
3	Liao et al. [206]	Observed electric field at the edge of field plate in the OFF state.
4	Subhash et al. [207]	Reported increase in breakdown of a device using passivation technique.
5	Nirmal et al. [208]	Reported new drain current model along with introduction of a cap layer beneath the gate and passivation.

In the proposed work, we present an investigation of the heat profile at the edge of field plate and propose an approach to mitigate peak electric field, which is primarily responsible for the heat at the field plate edge. Thus, the primary objective of the proposed work is to reduce peak electric field at the field plate edge. This is addressed by modifying access region stack, wherein a silicon dioxide pocket is created in a diamond layer below the field plate and on the top of the passivation layer. A detailed analysis of heat profile while varying thickness of silicon dioxide pocket with diamond layer and passivation layer is presented in this chapter.

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The chapter is organized as follows. Section 6.2 states the model employed for numerical analysis and calibration of numerical analysis framework. Section 6.3 discusses the result of the proposed device, and finally, summary of the work proposed in this chapter is presented in section 6.4.

6.2 Numerical Analysis Framework / Physical Model

The device structure used to investigate the proposed concept is shown in Fig. 6.1. The gate length (L_G), gate-to-drain spacing (L_{GD}), source-to-gate spacing (L_{SG}) are 0.25 μm, 2.7 μm, and 0.8 μm, respectively. The device structure from top to bottom of the composite layer comprises of a diamond layer (t_{Dia}), Si_3N_4 passivation layer (t_{SiN}), GaN cap layer (2 nm), $Al_{0.25}Ga_{0.75}N$ barrier layer (18 nm), GaN channel (30 nm), GaN buffer (1.7 μm) and Silicon Carbide (SiC) substrate (5 μm). A SiO_2 pocket around the field plate edge is introduced in the above mentioned device structure. The proposed idea of SiO_2 as a pocket at the field plate edge is to mitigate the peak electric field observed there. Subsequently, the peak electric field at the field plate edge may facilitate hot carriers that further generates heat. It is essential that the heat generated at the field plate edge is extracted efficiently with use of material having better thermal conductivity. As, the thermal conductivity of SiO_2 is not comparable to that of the diamond. Hence, a SiO_2 pocket is employed instead of a layer.

The width and the length of SiO_2 are 10 nm and 60 nm, and it is placed at 970 nm from the gate edge towards the drain terminal. When the length of SiO_2 pocket (L_{SiO_2}) varies from 60 nm to 80 nm, the variations observed in thermal resistance, peak electric field and eTemp are 0.91%, 1.9% and 2.79%, respectively, as compared to 16.20%, 10.20% and 5.75% change in these parameters, respectively, when L_{SiO_2} varies from 40 nm to 60 nm (refer Table 6.2, 6.3, and 6.4). It is observed that after $L_{SiO_2} > 60$ nm, all these aforementioned parameters do not vary significantly. Choosing L_{SiO_2} as 60 nm also provides large overlap margin of SiO_2 pocket with the field plate and aids in better fabrication yield as well. Therefore, a length of 60 nm for SiO_2 pocket is preferred in the numerical analysis of the proposed device.

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Table 6.2: Thermal Resistance, R_{TH} of the devices with variation in length of SiO_2 pocket (L_{SiO_2}) with t_{SiN} = 30 nm at V_{GS} = 0V, and V_{DS} = 20V

Device Structure	t_{Dia} (nm)	L_{SiO_2} (nm)	R_{TH} (K/W)
R1	–	–	6.26
Without SiO_2 Pocket	30	–	5.38
With SiO_2 Pocket	30	20	4.78
"	"	40	3.95
"	"	60	3.31
"	"	80	3.28
"	"	100	3.28

Table 6.3: Peak Electric Field of the devices at the edge of field plate with variation in length of SiO_2 pocket (L_{SiO_2}) with t_{SiN} = 30 nm at V_{GS} = −2V, and V_{DS} = 20V

Device Structure	t_{Dia} (nm)	L_{SiO_2} (nm)	E – Field (MV/cm)
R1	–	–	1.87
Without SiO_2 Pocket	30	–	1.43
With SiO_2 Pocket	30	20	1.27
"	"	40	1.18
"	"	60	1.06
"	"	80	1.04
"	"	100	1.03

Table 6.4: Peak eTemp of the devices at the edge of field plate with variation in length of SiO_2 pocket (L_{SiO_2}) with t_{SiN} = 30 nm at V_{GS} = −2V, and V_{DS} = 20V

Device Structure	t_{Dia} (nm)	L_{SiO_2} (nm)	eTemp ($\times 10^4$ K)
R1	–	–	3.312
Without SiO_2 Pocket	30	–	3.087
With SiO_2 Pocket	30	20	2.924
"	"	40	2.819
"	"	60	2.657
"	"	80	2.583
"	"	100	2.522

Silicon Carbide is a good substrate as it has better lattice match with GaN as compared to Silicon and Sapphire. It also has a higher thermal conductivity in comparison with the above mentioned substrates [48]. A field plate of length (L_{FP}) 1 μm is included in the device structure, which is pictorially depicted in the figures (refer Fig. 6.1) as a black rectangular box

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to highlight its extent for better clarity, whereas, the actual field plate is in contact with the passivation layer.

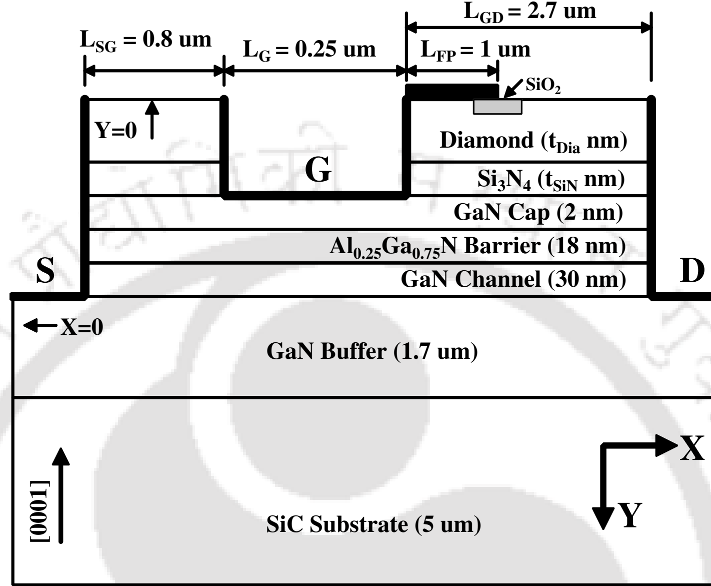

Figure 6.1: Schematics of the proposed device structure in this work (Not to scale). The diamond layer is introduced below field plate and on the top of passivation layer with SiO_2 pocket around field plate edge

The schematic of device structure is shown in Fig. 6.1. The device is numerically analyzed using Sentaurus TCAD [68]. Drift-diffusion (DD) transport model is solved self-consistently with Poisson's equation and continuity equations. Constant and field dependent mobility models for carriers (electrons and holes) are included in the analysis. Shockley-Read-Hall (SRH) recombination model is incorporated to capture generation and recombination of the carriers.

The polarization charge of equal magnitude and opposite polarity developed at the interfaces maintains an overall charge neutrality even in the absence of electric field [209]. This charge distribution has also been considered in the present work as illustrated in Fig. 6.2. The charges at the interface are σ_1 = $\pm$ 1.23 $\times$ 10^{13} cm^{-2} (AlGaN/GaN), and σ_2 = -2.0 $\times$ 10^{12} cm^{-2} (SiN/GaN). Similarly, the charges at diamond/SiN and SiO_2/diamond interfaces are 1.15 $\times$ 10^{12} cm^{-2} and -1.15 $\times$ 10^{12} cm^{-2}, respectively. Besides these, donor traps (σ_D^+) having a density of 1.0 $\times$ 10^{13} cm^{-2} at 0.2 eV below the conduction band have also been considered at Si_3N_4/GaN interface. The GaN buffer is doped with Carbon having concentration of 3 $\times$

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10^{16} cm^{-3} with activation energy, E_{AC} = 0.9 eV above GaN valence band. In addition to this, acceptor traps with a concentration of 5 × 10^{16} cm^{-3} at 0.4 eV below the conduction band is considered. The gate contact is considered as Schottky by employing a metal having work-function of 5.2 eV. The material parameters employed in the numerical analysis are enlisted in Table 6.5 [6]. Similarly, thermal conductivity of the materials is stated in Table 6.6. A thermal contact also known as thermode, defined at the bottom of the substrate is set at room temperature i.e., 300 K (27 °C).

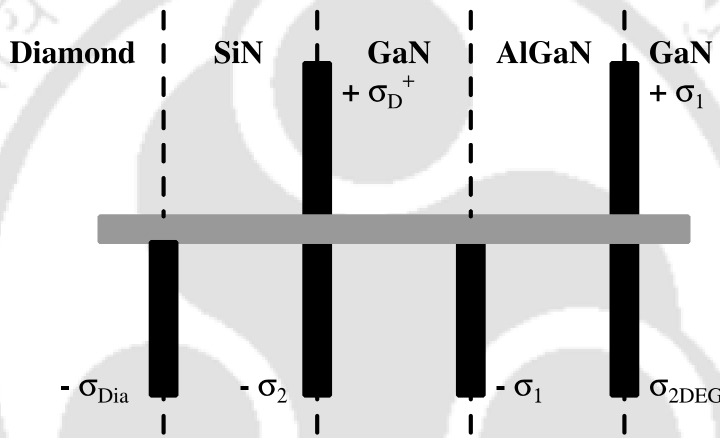

Figure 6.2: Polarization charges description at material interface of the device

Table 6.5: Material parameters used in TCAD simulation [6]

S. No.	Material property	Unit	GaN	AlGaN
1	Electron Mobility	cm^2/Vs	1200	300
2	Bandgap	eV	3.50	4.39
3	Electron Affinity	eV	4.0	3.41
4	Relative Permittivity	-	8.9	8.8
5	Electron Saturation Velocity	cm/s	2.5 × 10^7	1.1 × 10^7
6	Electron Conduction Band Density of States (DOS)	cm^{-3}	2.23 × 10^{18}	2.71 × 10^{18}
7	Electron Valence Band Density of States (DOS)	cm^{-3}	2.51 × 10^{19}	2.06 × 10^{19}

The numerical analysis framework considering a device without diamond layer, and silicon dioxide pocket, i.e., t_{Dia} = 0 nm, and SiN layer thickness, t_{SiN} = 30 nm, is referred as R1 subsequently as shown in Fig. 6.3 and is calibrated with an experimental data presented in [6]. The device characteristics, i.e., output (I_D versus V_{GS}), and transfer (I_D versus V_{DS})

Table 6.6: Thermal Conductivity for the materials

S. No.	Material	Thermal Conductivity ($Wm^{-1}K^{-1}$)
1	GaN	170 [210]
2	SiC	390 [210]
3	Diamond	2000 [210]
4	SiO_2	1.4 [211]

obtained using numerical analysis and experimental results are exhibited in Fig. 6.4. The close agreement of the analytical transfer and output characteristics with the experimental data resembles proper tuning of the parameters and model to mimic behaviour of an actual device.

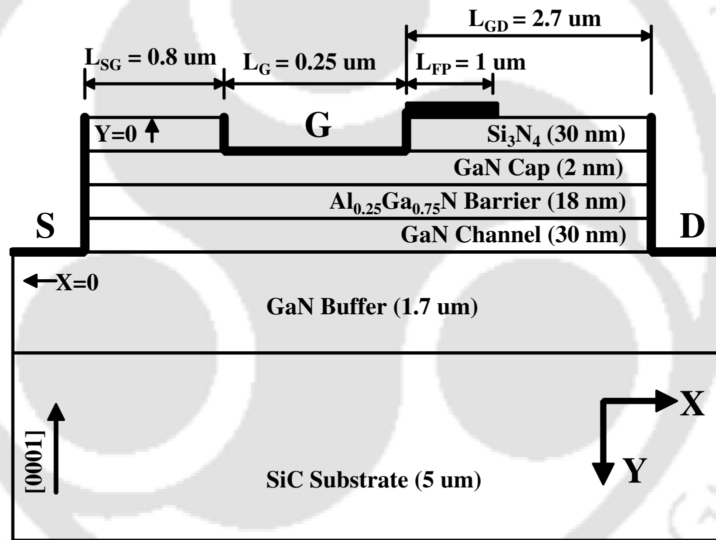

Figure 6.3: Schematic of R1 device calibrated with experimental data of [6]

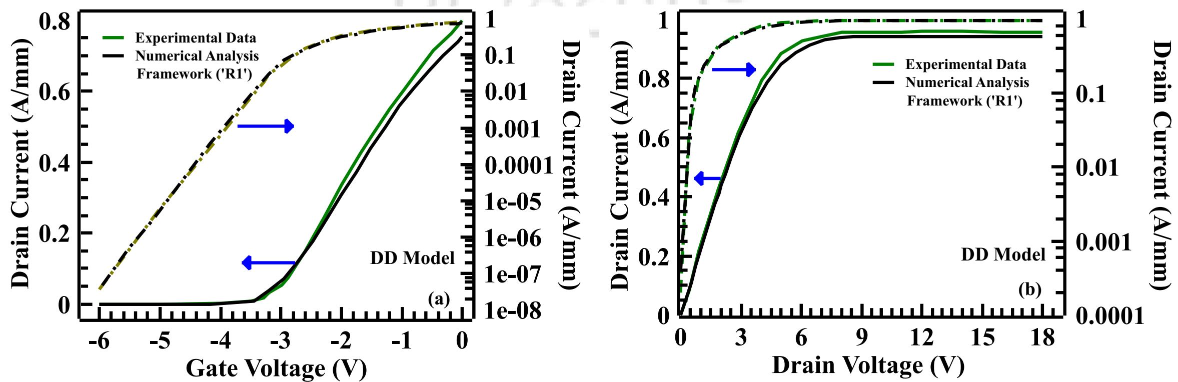

Figure 6.4: Comparison of DC characteristics from the numerical analysis framework with experimental data of [6]: (a) I_D versus V_{GS} (at V_{DS} = 5V); (b) I_D versus V_{DS} (at V_{GS} = 0V)

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Given the limitation of drift diffusion model to realize the velocity overshoot, and its overestimation, hydrodynamics model (HD) model is utilized while performing numerical analysis. The hydrodynamics model assists in the evaluation of carrier temperatures (T_n, T_p), described by Eq. 6.1, and 6.2.

$$\overrightarrow{J_n} = \mu_n \left(n\nabla E_C + kT_n \nabla n - nkT_n \nabla \ln \gamma_n + \lambda_n f_n^{td} kn \nabla T_n - 1.5nkT_n \nabla \ln m_n \right) \tag{6.1}$$

$$\overrightarrow{J_p} = \mu_p \left(p\nabla E_V - kT_p \nabla p + pkT_p \nabla \ln \gamma_p - \lambda_p f_p^{td} kp \nabla T_p + 1.5pkT_p \nabla \ln m_p \right) \tag{6.2}$$

In the above equations, the first term ($n\nabla E_C$ and $p\nabla E_V$) estimates spatial variation of bandgap, electron affinity and electrostatic potential of the proposed device. The second term ($kT_n\nabla n$ and $kT_p\nabla p$) captures concentration gradient. The third term ($nkT_n\nabla \ln\gamma_n$ and $pkT_p\nabla \ln\gamma_p$) is related to Fermi statistics, where $\gamma_n = (n/N_C)\ exp\ ((E_C - E_{F,n})/kT)$ and $\gamma_p = (p/N_V)\ exp\ ((E_{F,p} - E_V)/kT)$. The fourth term ($\lambda_n f_n^{td} kn\nabla T_n$ and $\lambda_p f_p^{td} kp\nabla T_p$) results due to hydrodynamics model, which captures temperature gradient of the carriers. Here, constants f_n^{td} and f_p^{td} are thermal diffusion parameters. The spatial variations in effective masses are taken into consideration by the last term ($1.5nkT_n\nabla \ln\ m_n$ and $1.5pkT_p\nabla \ln\ m_p$). Similarly, an energy balance equation in hydrodynamics model is described by Eqs. 6.3, 6.4, and 6.5.

$$\frac{\partial W_n}{\partial t} + \nabla \cdot \overrightarrow{S_n} = \overrightarrow{J_n} \cdot \nabla E_C / q + \frac{dW_n}{dt}\ |_{\text{coll}} \tag{6.3}$$

$$\frac{\partial W_p}{\partial t} + \nabla \cdot \overrightarrow{S_p} = \overrightarrow{J_p} \cdot \nabla E_V / q + \frac{dW_p}{dt}\ |_{\text{coll}} \tag{6.4}$$

$$\frac{\partial W_L}{\partial t} + \nabla \cdot \overrightarrow{S_L} = \frac{dW_L}{dt}\ |_{\text{coll}} \tag{6.5}$$

where, S_n, S_p, and S_L represent electron, hole and lattice energy flux, respectively. The energy densities of electron, proton, and lattice are denoted as W_n, W_p, and W_L, respectively. The *coll* indicates collision in the semiconductor.

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In the thermodynamics (TD) model of carrier transport, current density equations are analyzed employing temperature gradient given by Eq. 6.6 and Eq. 6.7.

$$\overrightarrow{J_n} = -nq\mu_n(\nabla\Phi_n + P_n\nabla T) \tag{6.6}$$

$$\overrightarrow{J_p} = -pq\mu_p(\nabla\Phi_p + P_p\nabla T) \tag{6.7}$$

Here, Φ_n and Φ_p stand for electron and hole quasi-Fermi potentials. P_n and P_p denote absolute thermoelectric powers for the carriers and T represents lattice temperature, which is computed using Eq. 6.8.

$$\frac{\partial}{\partial t}(c_L T) - \nabla \cdot (\kappa \nabla T) = A + B + C + D \tag{6.8}$$

where,

$$A = -\nabla \cdot \left[(P_n T + \Phi_n)\overrightarrow{J_n} + (P_p T + \Phi_p)\overrightarrow{J_p} \right]$$

$$B = -\frac{1}{q}\left(E_C + \frac{3}{2}kT\right)\left(\nabla \cdot \overrightarrow{J_n} - qR_{net,n}\right)$$

$$C = -\frac{1}{q}\left(E_V + \frac{3}{2}kT\right)\left(-\nabla \cdot \overrightarrow{J_p} - qR_{net,p}\right)$$

$$D = \hbar\omega G^{opt}$$

Here, κ and c_L stand for thermal conductivity and lattice heat capacity, respectively. The band energies in conduction and valence bands are given by E_C and E_V, respectively. G^{opt} denotes optical generation rate with frequency ω. The current densities and net recombination rate for the carriers are denoted as $\overrightarrow{J_n}$, $\overrightarrow{J_p}$, $R_{net,n}$, and $R_{net,p}$, respectively. The total heat H (for the stationary case) is given as

$$H = -\nabla \cdot \left[(P_n T + \Phi_n)\overrightarrow{J_n} + (P_p T + \Phi_p)\overrightarrow{J_p} \right] + \hbar\omega G^{opt} \tag{6.9}$$

In this section, we have discussed three transport models, namely, drift-diffusion (DD), hydrodynamics (HD), and thermodynamics (TD). The numerical analysis includes one of these transport models based on the necessity of the investigation to be performed. For instance, to

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study carrier temperature, hydrodynamics model is employed, whereas, for self heating study, thermodynamics model is included, and for the rest, drift-diffusion model is considered.

In this work, a numerical analysis is performed to investigate the proposed device. It is to mention that in the past, nano crystalline diamond (NCD) have been deposited over SiN layer of a fully fabricated HEMT to evaluate the performance of diamond in extracting the heat. This led to utilize diamond in HEMTs due to its high thermal conductivity. The deposition of diamond in HEMTs is quite challenging as it requires a hostile environment. It is carried out using chemical vapour deposition (CVD) [212, 213] in the presence of methane. A protective layer of SiN is employed during deposition process to protect underlying sensitive device from etching by hydrogen because methane, which is used in CVD, releases hydrogen during this process. Additionally, it is observed that NCD can be deposited on HEMTs using a SiN protective layer in microwave assisted plasma CVD process [214]. The NCD can be patterned using a plasma CVD SiN hard mask as stated in [214] to open windows on the diamond layer. These windows facilitate etching of diamond layer with high powered inductively coupled O_2/Ar plasma. After NCD removal, SiO_2 can be deposited in the pockets using plasma enhanced CVD (PECVD) [215]. The aforementioned process of diamond deposition on SiN along with etching and patterning of NCD can be utilized to implement the proposed device structure.

6.3 Results & Discussion

The primary focus of our study is to investigate electric field profile, carrier temperature behaviour, and self heating effect of a HEMT. The DC characteristics of the calibrated device R1 and a device with SiO_2 pocket is exhibited in Fig. 6.5. It is observed that output drain current barely changes for these devices and the threshold voltage for both the devices is found to be almost same as well, i.e., -3.4 V. Moreover, it is observed that $I_D - V_{GS}$ and $I_D - V_{DS}$ characteristics remain almost same with the variation in SiN and diamond layer thickness as shown in Fig. 6.6.

In the proposed study, the selection of V_{GS} = -2 V as SEMI-ON state is determined after

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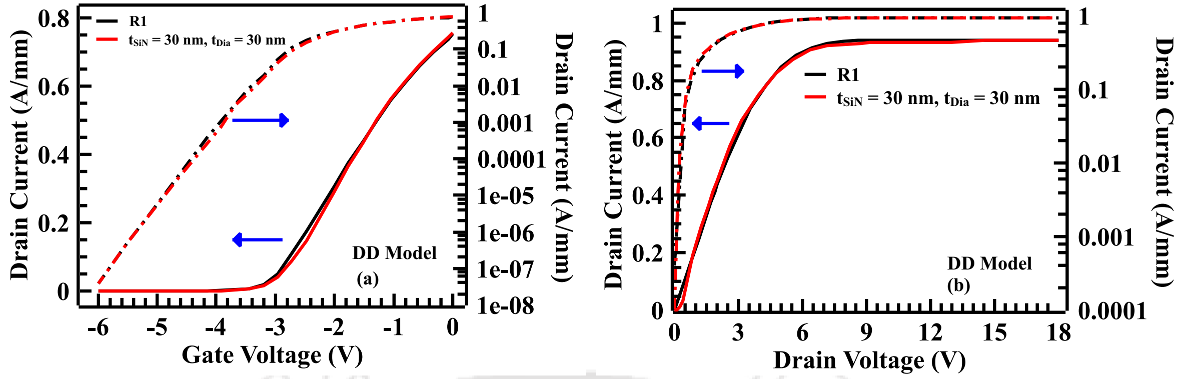

Figure 6.5: $I_D - V_{GS}$ (at V_{DS} = 5V) and $I_D - V_{DS}$ Characteristics (at V_{GS} = 0V); (a) R1 device, and (b) device with SiO_2 pocket

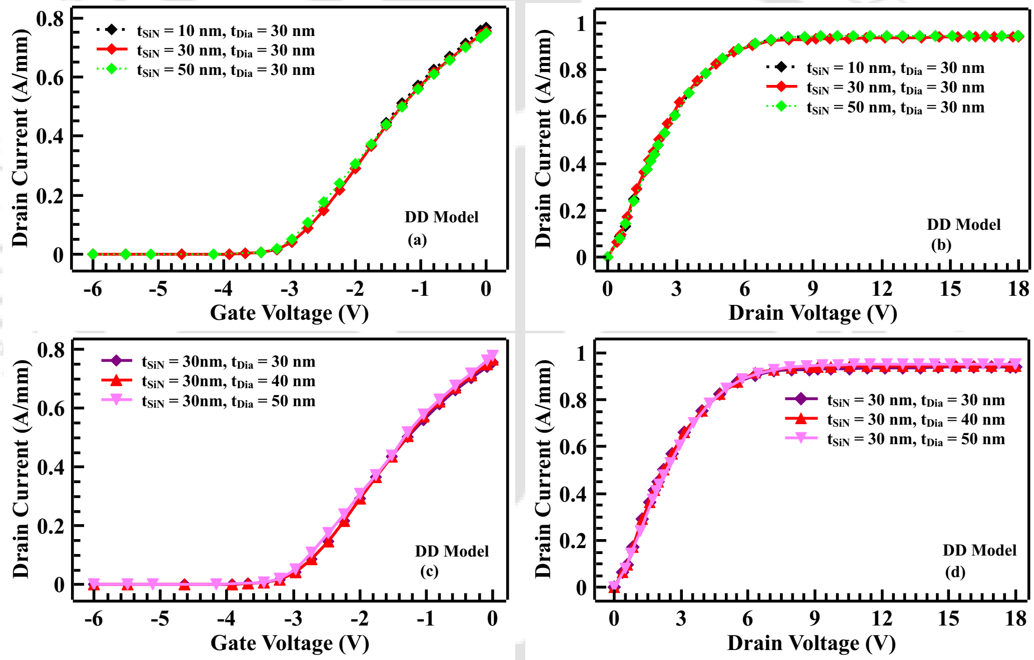

Figure 6.6: (a) $I_D - V_{GS}$ (at V_{DS} = 5V), (b) $I_D - V_{DS}$ characteristics (at V_{GS} = 0V) of the device with SiO_2 pocket for variation in t_{SiN} = 10/30/50 nm at t_{Dia} = 30 nm, (c) $I_D - V_{GS}$ (at V_{DS} = 5V), and (d) $I_D - V_{DS}$ characteristics (at V_{GS} = 0V) of the device with SiO_2 pocket for variation in t_{Dia} = 30/40/50 nm at t_{SiN} = 30 nm

examining electron-temperature (eTemp) profile of the device for V_{GS}= -6 V to 0 V at V_{DS}=20 V as shown in Fig. 6.7. It has been reported by Meneghesso et al. [30] that the SEMI-ON state is detrimental to the device, because of a very high electron-temperature in this state. Hence, V_{GS} = -2 V as SEMI-ON state in our case has been selected by studying eTemp profile. When V_{GS} is sufficiently low than the threshold voltage of the device, 2DEG channel beneath the gate

is completely removed, and device migrates in the OFF state [103]. At V_{GS} = -6 V, channel beneath the gate vanishes completely, which is evident from the electron density profile of the device illustrated in Fig. 6.8. Thus, gate bias of -6 V is denoted as OFF state of the device. Initially, the calibrated R1 device is compared to a device having SiO_2 pocket (t_{SiN} = 30 nm and t_{Dia} = 30 nm). Later, the same device is analyzed thoroughly by varying t_{SiN} and t_{Dia}. The thickness of SiN passivation layer is varied from 10 nm to 50 nm with a step size of 10 nm, whereas, diamond layer thickness is varied from 30 nm to 50 nm using the same step size.

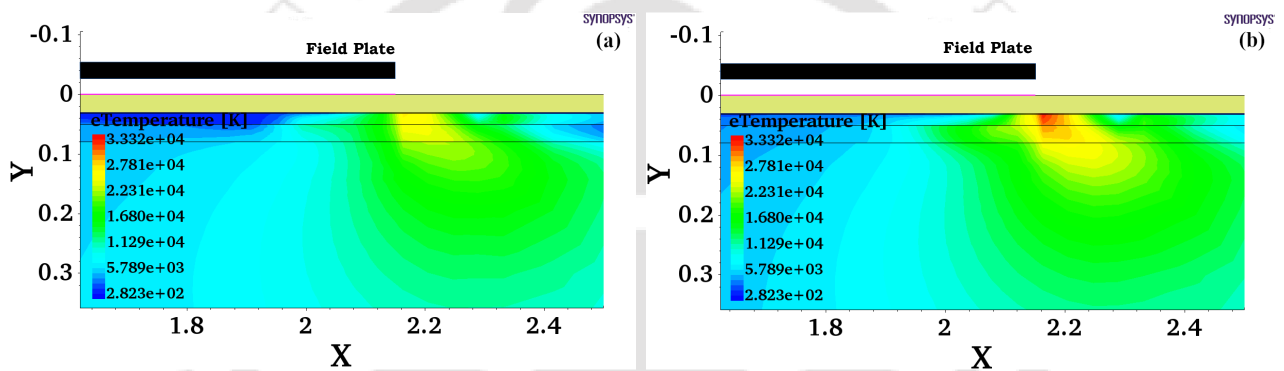

Figure 6.7: eTemp profile of R1 device; (a) at V_{GS} = -6 V (OFF), and (b) at V_{GS} = -2 V (SEMI-ON) for V_{DS} = 20 V

The subsequent section of the chapter details carrier temperature profile, electric field profile and self heating effect of the proposed device.

6.3.1 Carrier Temperature Profile

The electron-temperature (eTemp) profile is essential to study device degradation as high energy electrons are responsible for electrochemical degradation of AlGaN layer [159]. The electron-temperature (eTemp) profile of the proposed device is shown in Fig. 6.7. The device is analyzed for SEMI-ON and OFF states. It is evident that the device under SEMI-ON state has higher electron-temperature (eTemp) at the edge of field plate as compared to device under OFF state. Similarly, the electric field of the device in the SEMI-ON state is more as compared to the OFF state. This phenomenon is also observed by Meneghesso et al. [30] using Electroluminescence measurements (EL).

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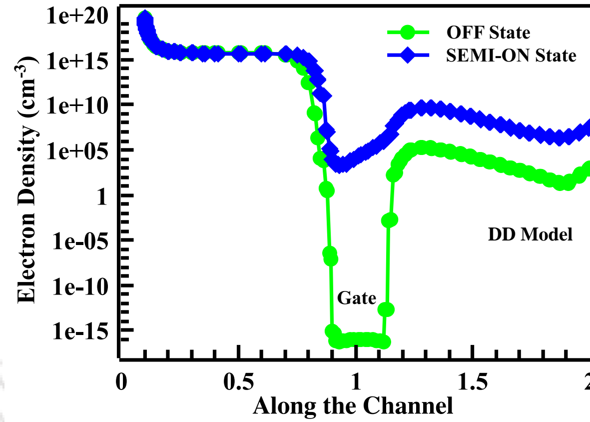

Figure 6.8: Electron Density profile of the R1 device under two bias condition; V_{GS} = -6 V, and V_{GS} = -2 V at V_{DS} = 20 V

Meneghesso et al. [30] perform "hot-electron-stress" on devices to observe intensity of electric field in the channel with respect to the variations of device bias. When V_{GS} is kept lower than the threshold voltage, a higher electric field is observed due to the influence of gate-drain voltage V_{GD}. Under this circumstance, electroluminescence is not realized in the channel due to the absence of electrons. As V_{GS} increases to the threshold voltage, electrons in the channel start accumulating, and they get "heated" due to the existence of high electric field in the device. Further, increase in the carrier concentration of primary electrons increases intensity of electroluminescene till a particular value of V_{GS}, beyond which it reduces with further increase in V_{GS} (refer Fig. 6 in [30]). Corresponding to a fixed V_{DS}, electroluminescene emission first increases and then reduces signifying electron energy lowering at both the extremes of V_{GS}. The V_{GS}, at which peak of electroluminescene is observed, is denoted as SEMI-ON state of the device. It is to mention that with the differences in the structures and technology of the devices along with testing conditions and failure criteria, a comparison of experimental results reported in the literature is extremely difficult. However, it is observed in AlGaN/GaN HEMTs that a gradual deterioration in drain current and transconductance is associated with the hot electron phenomenon [216–220].

The electric field profile of the device under OFF and SEMI-ON states is shown in Fig. 6.9(a). It is observed that the electron velocity is higher in SEMI-ON state as compared to

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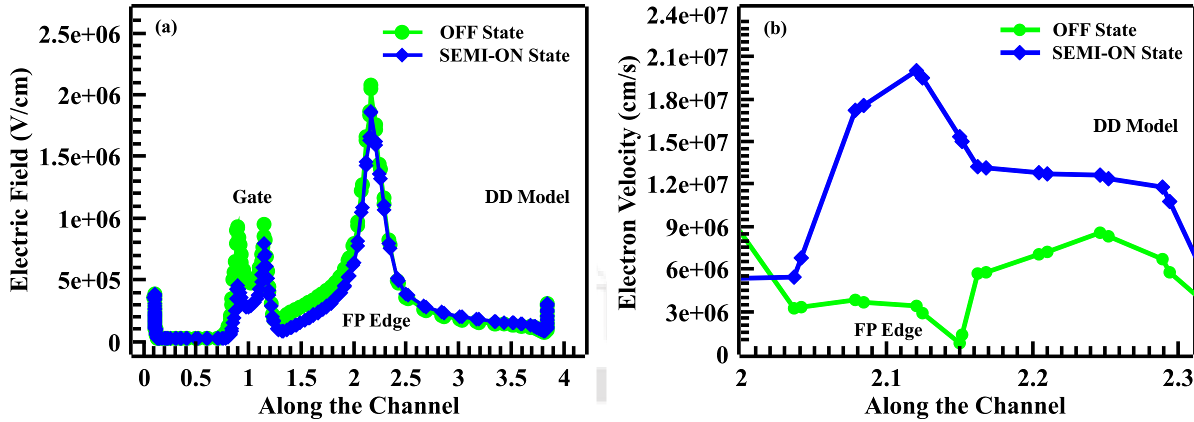

Figure 6.9: (a) Electric Field, and (b) Electron Velocity profile of the R1 device under two bias condition; V_{GS} = -6 V and V_{GS} = -2 V at V_{DS} = 20 V

OFF state, as depicted in Fig. 6.9(b). In the SEMI-ON state, device has a considerable number of carriers, while there are no carriers in the OFF state. Although, the number of carriers in the SEMI-ON state is less than the ON state, it is evident that the carriers undergo less collision resulting into an increase in the average mean free time of carriers. As we know that velocity of carriers is linearly dependent on the average mean free time, which aids carriers to possess higher velocity in the SEMI-ON state. The extracted carrier (electron) velocity of R1 device at field plate edge in the SEMI-ON and OFF states are 2.1×10^7 cm/s, and 3×10^6 cm/s, respectively. The higher carrier velocity and electric field in the SEMI-ON state leads to hot carriers, which makes SEMI-ON state to be of major concern in AlGaN/GaN HEMTs. However at $x = 2$ μm, electric field in the OFF state of the proposed device is observed to be higher than the SEMI-ON state. This leads to high gradient of electric field in the OFF state, which may be responsible for higher electron velocity than its velocity in the SEMI-ON state at $x = 2$ μm.

In order to address the issue of eTemp at the field plate edge, we propose a diamond layer on the top of the SiN passivation layer, and SiO_2 layer around the field plate edge in the diamond layer, which is preferred due to its high thermal conductivity. With the SiO_2 around the field plate edge, it is observed that eTemp of the device decreases in the SEMI-ON state, which is illustrated in Fig. 6.10. The eTemp of R1 device and the device with SiO_2 pocket ($t_{SiN} = t_{Dia} = 30$ nm) are 3.312×10^4 K and 2.657×10^4 K, respectively. This is basically

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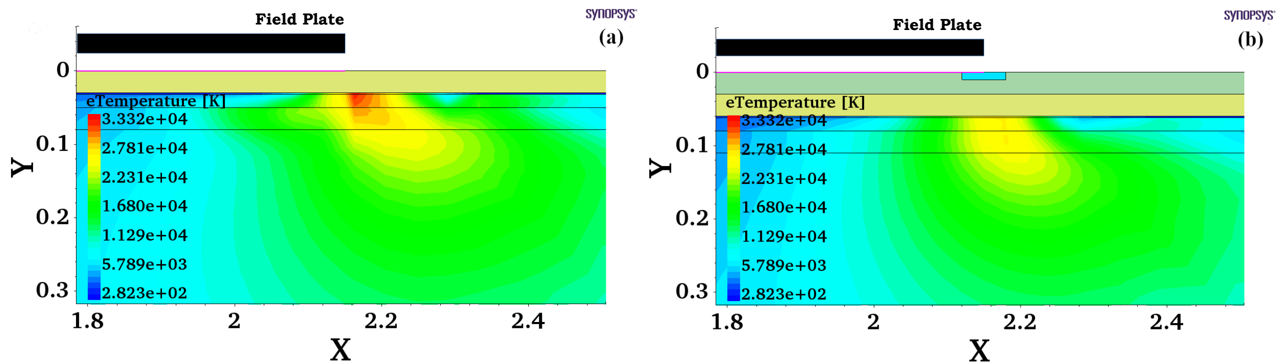

Figure 6.10: eTemp profile of: (a) R1 device, and (b) with SiO_2 pocket (t_{SiN} = t_{Dia} = 30 nm), at V_{GS} = -2 V (SEMI-ON) and V_{DS} = 20 V

due to reduction of peak electric field at the field plate edge because of employing SiO_2 pocket (refer Section 6.3.2 for details).

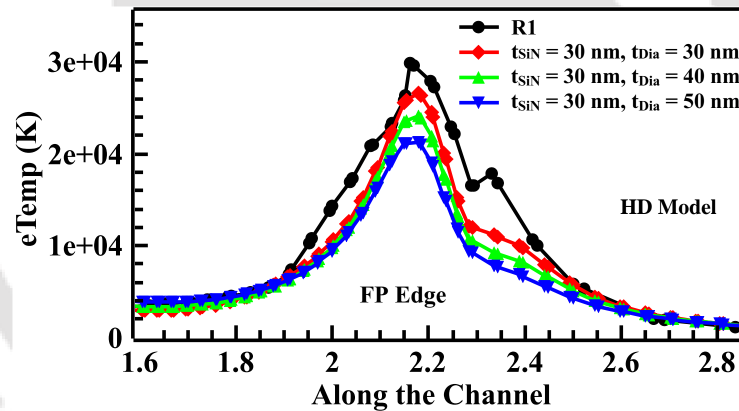

Figure 6.11: eTemp profile of R1 device, and with SiO_2 pocket for the device with t_{SiN} = 30 nm and varying t_{Dia}, at V_{GS} = -2 V (SEMI-ON) and V_{DS} = 20 V

The eTemp comparison of R1 device and the device with SiO_2 pocket having diamond layer is shown in Fig. 6.11. It can be seen that increasing thickness of diamond layer decreases eTemp near field plate edge in the proposed device. The reduction in hot carriers further lowers device degradation and improves device reliability [148,161,200]. Details of eTemp of the devices with the variation in thickness of SiN passivation layer and diamond layer is presented in Table 6.7.

Although eTemp estimated around 3E4 K may seems to be high, but a wide range of localized eTemp are reported in the literature. For instance, Kuzmik et al. [221] predicted eTemp as high as 20000 K, while Tapajna et al. [90] reported localized eTemp at 30000 K.

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Similarly, Shigekawa et al. [222] found eTemp in the range of 2000-2400 K, while in [223–230], eTemp at 1700 K was reported. A substantially higher eTemp at 5000 K was determined in [231]. Similarly, eTemp of around 6000 K [153] to 7000 K [165], and ∼ 13000 K [200] was also reported. It may be noted that localized hot electron temperature (eTemp) depends on the bias condition and device structure, therefore, a fair comparison of eTemp cannot be provided.

Table 6.7: Peak e-Temp at Field Plate edge of the devices in SEMI-ON state. The column (% Change) indicate the change in e-Temp of the devices w.r.t R1 device

t_{SiN}	t_{Dia}	e-Temp ($\times 10^4$ K)	% Change
R1 [6]	–	3.312	–
10 nm	30 nm	2.931	↓ 12.05%
	40 nm	2.814	↓ 15.04%
	50 nm	2.593	↓ 21.71%
20 nm	30 nm	2.823	↓ 14.76%
	40 nm	2.627	↓ 20.68%
	50 nm	2.365	↓ 28.59%
30 nm	30 nm	2.657	↓ 19.78%
	40 nm	2.411	↓ 27.20%
	50 nm	2.128	↓ 35.75%
40 nm	30 nm	2.455	↓ 25.88%
	40 nm	2.180	↓ 34.18%
	50 nm	1.915	↓ 42.18%
50 nm	30 nm	2.231	↓ 32.64%
	40 nm	1.958	↓ 40.88%
	50 nm	1.745	↓ 47.31%

6.3.2 Electric Field Profile

Field plate technology is widely implemented to address electric field crowding at the gate edge of a device. Since field plate is incorporated in a device, additional electric field peak appears at the edge of the field plate. Due to proximity of field plate edge to the drain terminal of a device, significant electric field of comparable order is observed in the OFF state and SEMI-ON state of the device as depicted in Fig. 6.9(a)). The electric field is observed to be comparable under OFF and SEMI-ON states. This high electrical field can lead to localized Schottky-barrier breakdown at a small drain voltage [116] along with avalanche breakdown and

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thermally-assisted tunnelling in the device [167]. The electric field peak at the field plate edge interacts with drain terminal, which results in an isolation breakdown of the device [120].

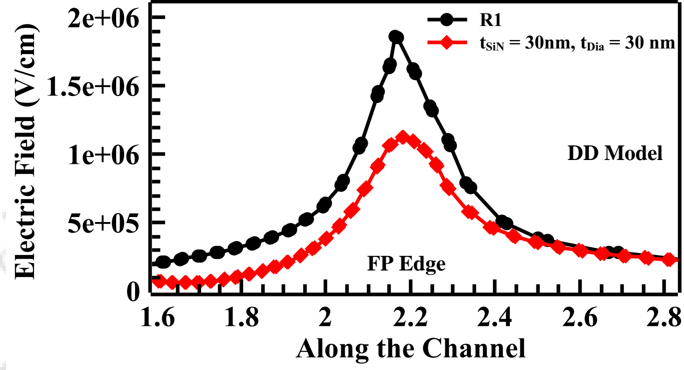

Figure 6.12: Electric field profile of the device; R1, and device with SiO_2 pocket ($t_{SiN} = t_{Dia} = 30$ nm), at V_{GS} = -2 V (SEMI-ON) and V_{DS} = 20 V

As electric field is one of the contributing factors of eTemp in the device, it is essential to reduce electric field at the field plate edge. For this purpose, SiO_2 pocket around the field plate edge is employed, which helps in reducing electric field as shown in Fig. 6.12). The electric field at field plate edge in SEMI-ON state for the R1 device, and the device with SiO_2 pocket ($t_{SiN} = t_{Dia} = 30$ nm) are 1.87 MV/cm and 1.06 MV/cm, respectively. This can be correlated with the boundary conditions of dielectrics. Further, the regions SiO_2 pocket and the diamond layer are characterized by ϵ_{SiO_2} and $\epsilon_{Diamond}$, where ϵ is the dielectric constant of a particular material. The electric flux densities of SiO_2 pocket and the diamond layer, D_{SiO_2} and $D_{Diamond}$, respectively, can be represented by following mathematical expression under the assumption that no charge exists at the SiO_2 and diamond interface.

$$D_{SiO_2} = D_{Diamond} \tag{6.10}$$

Since, electric flux density, $D = \epsilon E$, Eq. 6.10 can be written as

$$\epsilon_{SiO_2} E_{SiO_2} = \epsilon_{Diamond} E_{Diamond} \tag{6.11}$$

The Eq. 6.11 can be rearranged further as

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$$E_{Diamond} = \frac{\epsilon_{SiO_2}}{\epsilon_{Diamond}} E_{SiO_2} \tag{6.12}$$

Since dielectric constant of diamond is higher than the dielectric constant of SiO_2, ($\epsilon_{Diamond} > \epsilon_{SiO_2}$), which implies $E_{Diamond} < E_{SiO_2}$. This validates our observation of subdued electric field in diamond layer and in the device below the field plate. As a consequence, eTemp at the field plate edge is reduced significantly for the device with SiO_2 pocket around the field plate edge as illustrated in Fig. 6.10. The electric field profile at the field plate edge of the devices with respect to the thickness of SiN layer and diamond layer is depicted in Fig. 6.13 validating our claim.

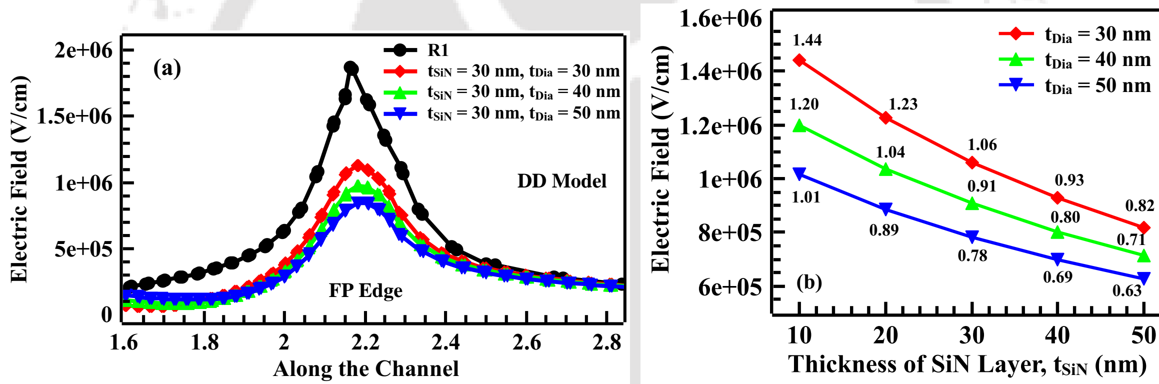

Figure 6.13: Electric Field profile of (a) R1 device, and with SiO_2 pocket for the device with t_{SiN} = 30 nm and (b) for combination of t_{SiN} and t_{Dia}, at V_{GS} = -2 V (SEMI-ON) and V_{DS} = 20 V

6.3.3 Self Heating

As it is extensively discussed in the preceding section about the behaviour of devices under "SEMI-ON" state, it is equally essential to explore self heating behaviour of the devices as well. Although GaN has higher thermal stability as compared to Si [232], heating effect reduces mobility of electrons in the channel, which subsequently lowers drain current [48, 233]. This hinders prolonged use of GaN-HEMTs under such condition. As we know, degradation mechanisms in AlGaN/GaN HEMTs are thermally initiated and are accelerated [30]. At a higher drain bias, due to high temperature and accumulation of heat, wavefunction of electron penetrates AlGaN barrier and triggers scattering [33]. Also, conduction to other areas in the

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HEMT from the hotspot region increases thermal stress in AlGaN and GaN layers [179]. It is to mention that the degradation mechanism is of diffusive nature because its generation and evolution are directly proportional to the square of time [30]. It has been reported that devices, which are subjected to high temperature for a prolonged duration, exhibit degradation initiated by converse piezoelectric effect and are further accelerated by the high temperature [90].

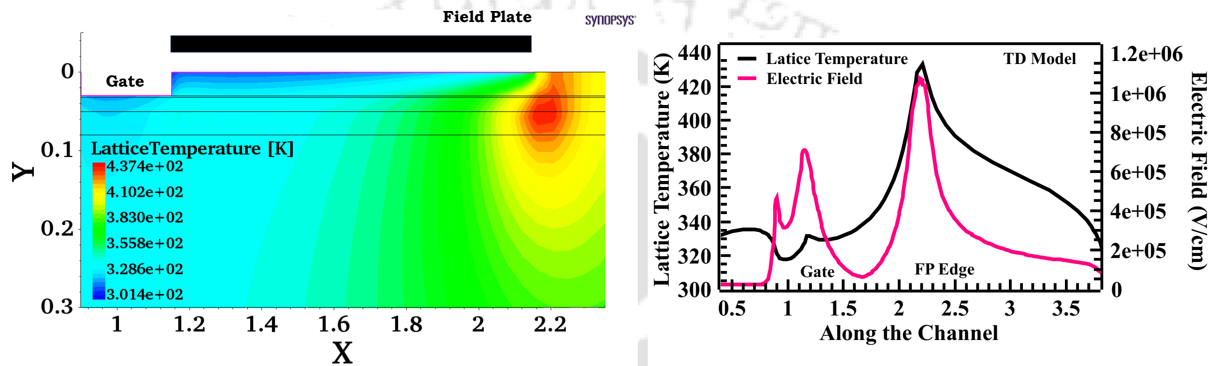

Figure 6.14: Self heating phenomena in R1 device and lattice temperature along with electric field profile of the device at V_{GS} = 0V and V_{DS} = 20V

Self heating behaviour is observed in a device, when it is operated in the ON state. As we know, AlGaN/GaN HEMT is ON at V_{GS} = 0V, the self heating is observed under bias conditions, V_{GS} = 0V and V_{DS} = 20V as shown in Fig. 6.14. The mathematical models, which need to be plugged into the numerical analysis framework to observe self heating is described in Section 6.2.

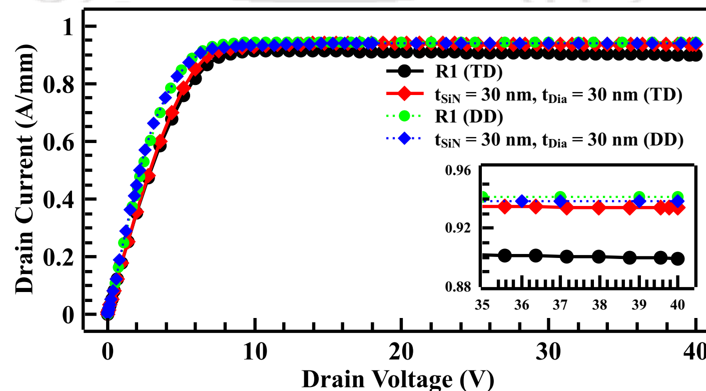

Figure 6.15: Output characteristics of the devices without (R1) and with SiO_2 pocket (t_{SiN} = t_{Dia} = 30 nm) depicting the self heating effect, at V_{GS} = 0 V and V_{DS} = 20 V

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The simultaneous solution of lattice temperature with current density equations exhibits a practical lattice temperature distribution. This carrier transport model incorporates device self-heating phenomenon. The $I_D - V_{DS}$ characteristics of the devices with the incorporation of thermodynamics model is shown in Fig. 6.15. It is evident that the impact of self heating in the output characteristics is less in the device with SiO_2 pocket as compared to R1 device. This is mainly due to subdued degradation of mobility of the carriers in the former device. As a result, drain current increases while channel temperature deceases in the devices having SiO_2 pocket. Hence, this device is expected to have better performance at higher temperature.

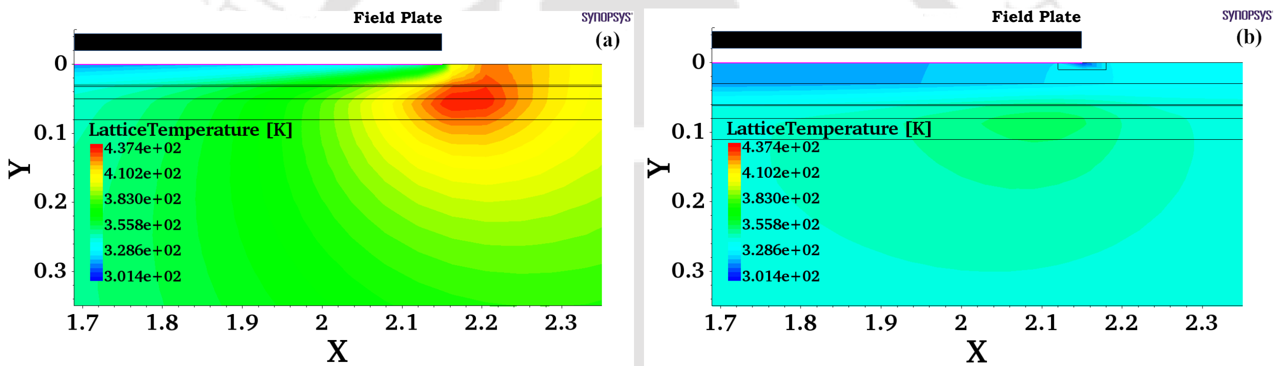

Figure 6.16: Self heating phenomena; (a) R1 device, and (b) device with SiO_2 pocket (t_{SiN} = t_{Dia} = 30 nm) at V_{GS} = 0 V and V_{DS} = 20 V

Moreover, to illustrate the effect of self-heating phenomenon using $I_D - V_{DS}$ characteristics, Fig. 6.15 showcases $I_D - V_{DS}$ characteristics with and without thermodynamics model. The absence of thermodynamics model in the equations exhibiting device characteristics transforms them to drift-diffusion model. As we know that this model does not account thermal effects, the evaluation of current densities by thermodynamics and drift-diffusion models are different. Hence, $I_D - V_{DS}$ characteristics of both the above mentioned models differ. Similarly, lattice temperature profiles of R1 device and the device having SiO_2 pocket are shown in Fig. 6.16. It is observed that SiO_2 pocket in AlGaN/GaN HEMTs aids in reducing hotspots and improves device performance as well as longevity. It is to mention that the lattice temperatures at the field plate edge of R1 device and device with SiO_2 pocket (t_{SiN} = t_{Dia} = 30 nm) are 437 K and 382 K, respectively.

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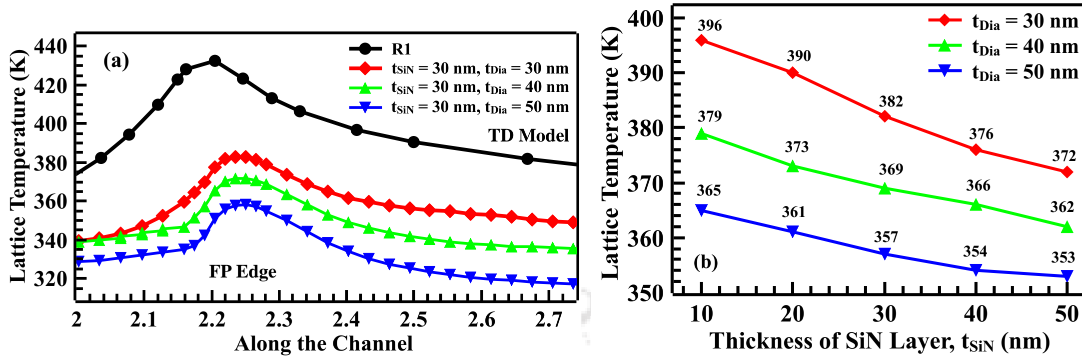

Figure 6.17: Lattice Temperature comparison of (a) R1 device, and device with SiO_2 pocket for t_{SiN} = 30 nm, (b) combination of t_{SiN} and t_{Dia}

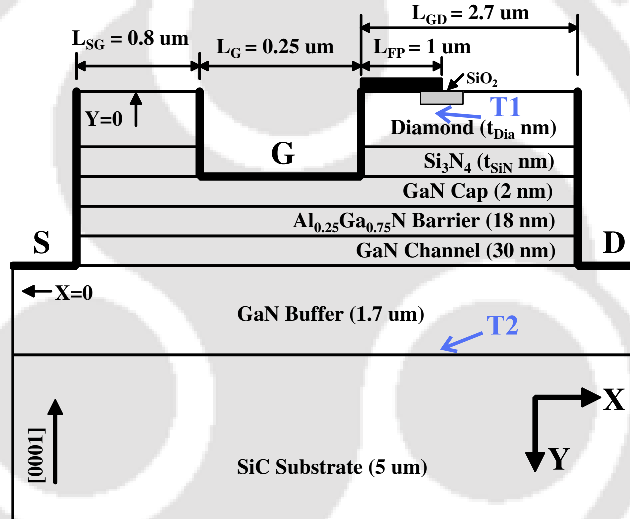

Figure 6.18: Depiction of T_1 and T_2 for estimation of R_{TH}

It is necessary to extract thermal resistance (R_{TH}) in order to understand the behaviour of heat conduction in a device. The thermal resistance is calculated by considering temperatures at two different points. First point, T_1, is the location of a hotspot and the second point, T_2 is the region having uniform temperature distribution, refer Fig. ??. Here, we have considered bottom of GaN Buffer or top of the SiC substrate as T_2. The temperature drop ($\Delta T = T_1 - T_2$) is related to thermal resistance given by Eq. 6.13.

$$\Delta T = R_{TH} \times P_{Dissipation}, \text{ or } R_{TH} = \frac{T_1 - T_2}{P_{Dissipation}} \tag{6.13}$$

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where, $P_{Dissipation}$ is the power dissipation in the device. The bias condition for the evaluation of thermal resistance, R_{TH}, are $V_{GS} = 0$V and $V_{DS} = 20$V. Employing the self heating profiles of the devices shown in Fig. 6.16, R_{TH} is estimated and is shown in Table 6.8. The lattice temperature profiles of the devices with respect to the thickness of SiN and diamond layers are shown in Fig. 6.17. Moreover, Fourier's law of heat conduction states that the rate of heat flow is inversely proportional to the thermal resistance [234], which indicates that the heat flow improvises with lower thermal resistance. Further, lower R_{TH} also implies that the proposed device can operate at higher ambient temperature with reduced mechanical deformation due to low lattice vibrations [210]. Thermal resistance of the devices with respect to the thickness of SiN and diamond layer is shown in Fig. 6.19. This indicates that a device with SiO_2 pocket offers less thermal resistance and improves its reliability. This can be corroborated with the findings of [210, 235].

Table 6.8: Estimation of Thermal Resistance, R_{TH} for R1 device, and device with SiO_2 pocket

Device Structure	T_1(K)	T_2(K)	I_{DS}(A)	V_{DS}(V)	$P_{Dissipation}$(W)	$R_{TH} = \frac{T_1 - T_2}{P_{Dissipation}}$ (K/W)
R1 [6]	437	318	0.95	20	19	6.26
With SiO_2 Pocket, $t_{SiN} = t_{Dia} = 30$ nm	382	317	0.98	20	19.6	3.31

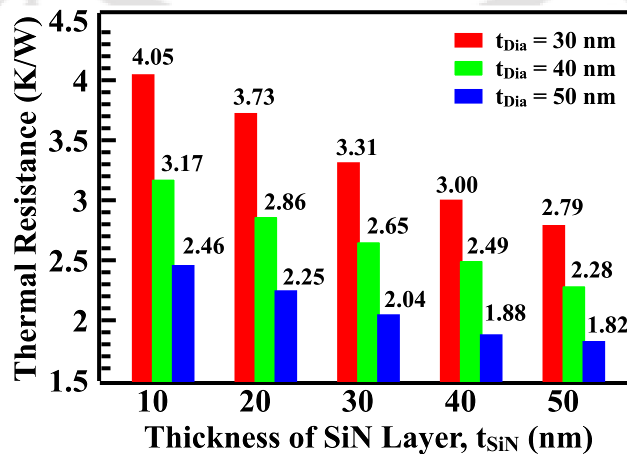

Figure 6.19: Thermal Resistance, R_{TH} for the device with SiO_2 pocket with varying t_{SiN} and t_{Dia}

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6.4 Summary

In this work, we have primarily focused on the degradation issue of AlGaN/GaN HEMTs in the SEMI-ON state. The electric field and velocity profiles of the device in the SEMI-ON state clearly indicate that the degradation mechanism is of greater significance in this state as compared to the OFF state. The average velocity of energized carriers in the SEMI-ON state is one order higher than the velocity of carriers in the OFF state. These energized carriers tend to accumulate at the edge of field plate due to the presence of high electric field. To mitigate this issue, a diamond layer is employed on the top of SiN passivation and a SiO_2 pocket is incorporated around the edge of field plate. Consequently, for a device having SiO_2 pocket along with SiN and diamond layers of 30 nm thickness, it is observed that the electric field and eTemp at the edge of field plate reduce by 43%, and 20%, respectively, than the device without SiO_2 pocket around the edge of field plate. Further, it is found that the self heating effect in the proposed device is lowered by 13% than the device without SiO_2 pocket. Also, the thermal resistance of the proposed device is reduced by 47% due to the incorporation of diamond layer and SiO_2 pocket in it. The eTemp, electric field, self heating and thermal resistance of our proposed device at the field plate edge varies consistently with the thickness of SiN and diamond layers. The proposed device exhibits superior performance and better reliability as compared to the existing HEMTs, and can be utilized in high power device applications.

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7

Summary and Conclusions

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7.1 Summary of the Observations

In this chapter, we present a brief summary of the proposed research work and its future directions. As AlGaN/GaN HEMTs can be devices for next generation technology, such as 5G, space exploration and high power, the present work tries to focus on the reliability and efficient high power devices.

- Reliability enhancement of AlGaN/GaN HEMT is a significant thrust area due to rapidly improving material and processing technology. A detailed analysis of rounded gate AlGaN/GaN HEMT with field plate is presented in this thesis. Although AlGaN/GaN HEMT with field–plate is well-known, its blending with gate–shaping leading to more robust and reliable behaviour is presented in this thesis. It is observed that the threshold voltage and transconductance invariably remain constant for various combinations of rounded gate and field plate length. The threshold voltage for all the devices are found to be –5.8 V. The peak transconductance of the devices without field plate and with field plate is $\sim$ 0.16 S/mm and $\sim$ 0.15 S/mm, respectively. Apart from leakage current, the electric field also gets mitigated for both rounded gate and field–plated devices by $\sim$ 45% and $\sim$ 68%, respectively. The moderation in electric field further assists in the reduction of electron temperature for rounded gate and field–plated structures by $\sim$ 12% and $\sim$ 85%, respectively. Additionally, breakdown voltage increases for the rounded gate devices to 133 V as compared to 120 V obtained using rectangular gate devices without field plate. Significant reduction in leakage current, electric field and electron temperature is accompanied by a minor increment in the capacitance of field–plated structure, hence the proposed structure is expected to enhance reliability of the device. Thus, it is anticipated that the proposed devices with enhanced reliability may be a step ahead of rectangular gate devices and would find major applications in the high power domain.

- As it is evident that converse piezoelectric strain leads to degradation, such as structural deformation, creation of traps, etc. in AlGaN/GaN high electron mobility transistors

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(HEMTs). We have presented a comparison of peak vertical electric field and vertical converse piezoelectric strain for these devices with rectangular gate structure, staircase gate structure and rounded gate devices. It is found that in rounded gate devices, the peak vertical electric field and vertical converse piezoelectric strain reduces by almost 25%, while electron temperature reduces by 20% as compared to rectangular gate HEMTs. It is also observed that the reduction in peak vertical electric field and peak vertical converse piezoelectric strain is more than staircase gate structure device. Thus, the proposed rounded gate device is expected to be a potential candidate, which can tackle converse piezoelectric strain induced damages in AlGaN/GaN HEMT devices.

- Although field plate technology assists in the mitigation of electric field at the gate edge in a device, however electric field peaks at field plate edge in the SEMI-ON state. Electric field in a device varies as it switches between ON and OFF states. These states have different intensities of electric field and carrier density. The regions having high electric field are not only the point of contention but also affects reliability of a GaN HEMT. In an AlGaN/GaN HEMT, degradation primarily initiates as a result of electric field crowding near its gate/field plate edges. The proposed work aims at suppressing high electric field in the SEMI-ON state at the field plate edge by incorporating a SiO_2 pocket at its edge. Numerical analysis is performed using a calibrated setup to investigate viability and performance of the proposed device. It is found that the electric field and electron temperature in the SEMI-ON state reduce significantly by incorporating a SiO_2 pocket around the field plate edge in the drain access region. For the device having SiO_2 pocket, in which Diamond and passivation layer thickness kept at 30 nm each, the electric field, carrier temperature and self heating reduces by 43%, 20%, and 13%, respectively at the field plate edge along with 47% reduction in the thermal resistance.

Therefore, it may be concluded that a rounded gate field plate AlGaN/GaN HEMT and Diamond/SiN stack with SiO_2 pocket can be a suitable device structure for high power applications with an enhanced reliability. It is predicted that the continued research in this direction

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would help scientific community to improve existing efficiency of AlGaN/GaN devices.

7.2 Proposed Future Work

Since we have explored the rounded gate with field plate and Diamond/SiN passivation stack with SiO_2 pocket for the mitigation of high electric field at the field plate edge, it is anticipated that investigation of drain connected field plate or multiple field plate configuration with SiO_2 pocket can be among the possible direction in the development of high power device technology. Further, various approaches to understand the minimization of parasitic capacitances in the field plate devices can also be pursued. Although GaN based devices exhibit superior performance as compared to Silicon based devices, there are certain issues that needs to be addressed to realize full potential of HEMTs.

- As GaN devices operates with very high switching speed, the high frequency content of the resultant voltage signals translates small inductances into high impedances, whereas low capacitances results into low impedances. Thus, not only the passive components but the layout and the interconnection of the individual components also need to be carefully designed. Reduction of inductances by shortening the connection length may be limited by the requirements on insulation distances and/or loss density.
- The high current density, higher operating temperature and higher switching frequency requires better handling. This includes new packaging solutions, improved passive components, such as capacitors and inductors, improved dielectric materials as well as new materials solutions with low-CTE (coefficient of thermal expansion) to increase yield and reliability during thermal stress. Furthermore, completely new topologies might be explored to make better use of GaN devices and modules.

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A

Analytical Model Development for Rounded Gate Devices

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In chapter 4, we have proposed rounded gate devices for the mitigation of electric field in the vicinity of gate edge of the device. It is known that gate shape modification leads to change in electric field profile in the vicinity of gate edge in the rounded gate devices. Hence, it is essential that an analytical formulation for the electric field and charge density at the gate edge of the device is developed. For the development of analytical model of charge density and electric field of the proposed rounded gate devices, several assumption are taken into account, which are elaborated below.

- The proposed rounded gate device structure with field plate is represented in Fig. A.1, in which regions between gate contact and drain contact are categorized as Region 1 and Region 2.
- Here, Region 1 corresponds to a fully depleted semiconductor, while Region 2 corresponds to the extension of depletion region beyond the metal boundary at the surface. Details regarding conformal mapping of Region 2 can be found in [166, 236].
- The channel under gate and field plate is considered as depleted, which results in a positive charge sheet (σ_z) in the channel. The dielectric constant (ϵ_u) of the material between channel and gate/field-plate metal is assumed to be constant.
- The distance from field plate to the channel is denoted as a_i and gate-to-channel is denoted as a_0. The charge is assumed to be either on metal or in the channel. It is presumed that boundary of Region 1 extends from -∞ to +∞ and left boundary of Region 2 extends to -∞, which is equivalent to a long gate and field plate approximation.

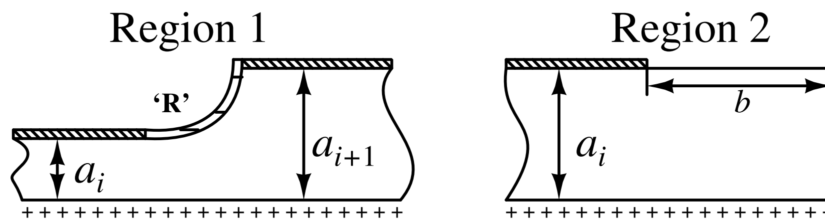
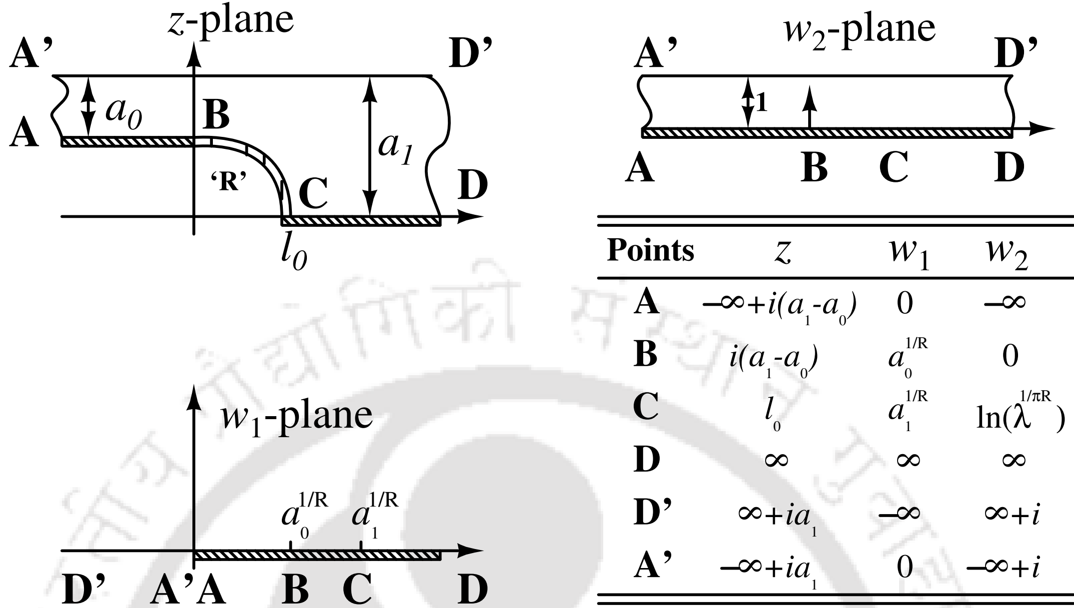


Figure A.1: Representation of Region 1 and Region 2 to be used for conformal transformation



Points	z	w_1	w_2
A	$-\infty+i(a_1-a_0)$	0	$-\infty$
B	$i(a_1-a_0)$	$a_0^{1/R}$	0
C	l_0	$a_1^{1/R}$	$\ln(\lambda^{1/\pi R})$
D	∞	∞	∞
D'	$\infty+ia_1$	$-\infty$	$\infty+i$
A'	$-\infty+ia_1$	0	$-\infty+i$

Figure A.2: Representation of Region 1 in different (z, w_1, w_2) planes after each conformal transformation. The key locations in each plane is stated in the table

Considering 2D nature of the device structure and charge appearing only at the boundaries, conformal mapping can be utilized for analyzing complex charge density function. For the application of conformal mapping as shown in Fig. A.2, Region 1 needs to be rotated so that metal contact is at the bottom, while drain contact is at the right side and is labelled as z-plane. Using Schwarz–Christoffel transformation [237, 238], the region between metal and positive charge sheet is transformed into upper half of w_1 plane. The relation between z and w_1 as stated in [239] is given below for completeness.

$$\frac{\pi z}{a_0} = \lambda \cosh^{-1}\left[\frac{(2w_1 a_0^{-2} - (\lambda^2+1))}{(\lambda^2-1)}\right] - \cosh^{-1}\left[\frac{((\lambda^2+1)w_1 a_0^{-2} - 2\lambda^2)}{((\lambda^2-1)w_1 a_0^{-2})}\right] \tag{A.1}$$

where, $\lambda = a_1/a_0$. Eq. A.1 is normalized with respect to gate-to-channel spacing, which allows solution to change proportionately with the change in parameters. The transformation from w_1-plane into the w_2-plane is performed using relation $w_1 = a_0^2 e^{\pi w_2}$. Also, z and w_2 are given by following mathematical expression.

$$\frac{\pi z}{a_0} = \lambda \cosh^{-1}\left[\frac{(2e^{\pi w_2} - (\lambda^2+1))}{(\lambda^2-1)}\right] - \cosh^{-1}\left[\frac{(\lambda^2+1)e^{\pi w_2} - 2\lambda^2}{(\lambda^2-1)e^{\pi w_2}}\right] \tag{A.2}$$

Let gate–shape parameter, 'dr' be represented by polar equation, $s = s(\theta)$, then the curvature R can be defined as

$$R = \frac{|s^2 + 2(s')^2 - ss''|}{[s^2 + (s')^2]^{\frac{3}{2}}} \tag{A.3}$$

Considering metal region and charge being extended from -∞ to +∞, the complex potential due to unit charge located at $w_0 = u_0 + i$ [237] can be depicted as

$$\Psi[w_2, u_0] = (2\pi\epsilon_u)^{-1} \ln\left[(w_2 - w_0^*)/(w_2 - w_0)\right] \tag{A.4}$$

From the conformal mapping theory, the proposed modified charge density in w_2 plane is defined as [237, 238]

$$\sigma[u_0] = \sigma_z \left(\frac{\partial z}{\partial w_1}\frac{\partial w_1}{\partial w_2}\right)^* |_{w_2 = u_0 + i} = \sigma_z \sigma_1 \left(\frac{e^{\pi u_0} + 1}{e^{\pi u_0} + \lambda^R}\right)^{1/R} \tag{A.5}$$

where, R is the parameter that takes into account the effect of proposed gate modification. Subsequently, the complex potential, Φ in w_2 plane is defined as

$$\Phi[w_2] = \int_{-\infty}^{\infty} \sigma[u_0]\ \Psi[w_2, u_0]\ \partial u_0 \tag{A.6}$$

Hence, the electric field, E can be evaluated from complex potential [237, 238] as mentioned below.

$$E[\omega_2[z]] = -\left(\frac{\partial \Phi}{\partial z}\right)^* = \int_{-\infty}^{\infty} \sigma[u_0]\left(-\frac{\partial \Psi[w_2, u_0]}{\partial z}\right)^* \partial u_0 \tag{A.7}$$

The parameter, R in Eq. A.5 accounts for the charge density of the proposed rounded gate device. As the reduction in charge density is predicted by Eq. A.5, this confirms a decrease in electric field of the proposed rounded gate device and is stated in Eq. A.7.

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Bibliography

[1] T. Li, M. Mastro, and A. Dadgar, *III–V compound semiconductors: integration with silicon-based microelectronics.* CRC press, 2010.

[2] S. Karmalkar and U. K. Mishra, "Enhancement of breakdown voltage in algan/gan high electron mobility transistors using a field plate," *IEEE transactions on electron devices*, vol. 48, no. 8, pp. 1515–1521, 2001.

[3] G. Meneghesso, M. Meneghini, A. Stocco, D. Bisi, C. De Santi, I. Rossetto, A. Zanandrea, F. Rampazzo, and E. Zanoni, "Degradation of algan/gan hemt devices: Role of reverse-bias and hot electron stress," *Microelectronic engineering*, vol. 109, pp. 257–261, 2013.

[4] M. Kuball, M. Tapajna, R. J. T. Simms, M. Faqir, and U. K. Mishra, "Algan/gan hemt device reliability and degradation evolution: Importance of diffusion processes," *Microelectronics Reliability*, vol. 51, no. 2, pp. 195–200, 2011.

[5] W. Saito, T. Suwa, T. Uchihara, T. Naka, and T. Kobayashi, "Breakdown behaviour of high-voltage gan-hemts," *Microelectronics Reliability*, vol. 55, no. 9-10, pp. 1682–1686, 2015.

[6] N. K. Subramani, J. Couvidat, A. Al Hajjar, J.-C. Nallatamby, R. Sommet, and R. Quéré, "Identification of gan buffer traps in microwave power algan/gan hemts through low frequency s-parameters measurements and tcad-based physical device simulations," *IEEE Journal of the Electron Devices Society*, vol. 5, no. 3, pp. 175–181, 2017.

[7] A. Zhalko-Tytarenko, "Compound semiconductor materials: Technology, developments and markets," *BCC Research*, 2008.

[8] A.-P. Zhang, F. Ren, J. Han, S. J. Pearton, S. S. Park, Y. J. Park, and J.-I. Chyi, "Gan and algan high voltage power rectifiers," in *Wide Energy Bandgap Electronic Devices.* World Scientific, 2003, pp. 125–171.

[9] F. Bernardini, V. Fiorentini, and D. Vanderbilt, "Accurate calculation of polarization-related quantities in semiconductors," *Physical Review B*, vol. 63, no. 19, p. 193201, 2001.

[10] D. Ueda, *Properties and Advantages of Gallium Nitride.* Cham: Springer International Publishing, 2017, pp. 1–26.

[11] "Despite shortage, global semiconductor market to hit $522b in 2021," https://www.business-standard.com/article/technology/despite-shortage-global-semiconductor-market-to-hit-522b-in-2021-121050800510_1.html, Accessed: 03-09-2021.

[12] V. V. Zhirnov, R. K. Cavin, J. A. Hutchby, and G. I. Bourianoff, "Limits to binary logic switch scaling-a gedanken model," *Proceedings of the IEEE*, vol. 91, no. 11, pp. 1934–1939, 2003.

TH-2691_166102020

[13] S. Nakamura, M. Senoh, and T. Mukai, "P-gan/n-ingan/n-gan double-heterostructure blue-light-emitting diodes," *Japanese Journal of Applied Physics*, vol. 32, no. 1A, p. L8, 1993.

[14] S. Nakamura, "Iii–v nitride based light-emitting devices," *Solid State Communications*, vol. 102, no. 2-3, pp. 237–248, 1997.

[15] P. Sandvik, K. Mi, F. Shahedipour, R. McClintock, A. Yasan, P. Kung, and M. Razeghi, "$Al_xGa_{1-x}N$ for solar-blind uv detectors," *Journal of crystal growth*, vol. 231, no. 3, pp. 366–370, 2001.

[16] E. Johnson, "Physical limitations on frequency and power parameters of transistors," *RCA Review*, vol. 26, pp. 163–177, 1965.

[17] B. J. Baliga, "Power semiconductor device figure of merit for high-frequency applications," *IEEE Electron Device Letters*, vol. 10, no. 10, pp. 455–457, 1989.

[18] J. W. Johnson, J. LaRoch, F. Ren, B. Gila, M. Overberg, C. Abernathy, J. Chyi, C. Chuo, T. Nee, C. Lee *et al.*, "Schottky rectifiers fabricated on free-standing gan substrates," *Solid-State Electronics*, vol. 45, no. 3, pp. 405–410, 2001.

[19] C. Oxley, "Calculation of minimum noise figure using the simple fukui equation for gallium nitride (gan) hemts," *Solid-State Electronics*, vol. 45, no. 5, pp. 677–682, 2001.

[20] M. Mastro, D. Tsvetkov, V. Soukhoveev, A. Usikov, V. Dmitriev, B. Luo, F. Ren, K. Baik, and S. Pearton, "Hydride vapor phase epitaxy-grown algan/gan high electron mobility transistors," *Solid-State Electronics*, vol. 47, no. 6, pp. 1075–1079, 2003.

[21] M. J. Rosker, "The present state of the art of wide-bandgap semiconductors and their future," in *2007 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium.* IEEE, 2007, pp. 159–162.

[22] M. Faqir, G. Verzellesi, G. Meneghesso, E. Zanoni, and F. Fantini, "Investigation of high-electric-field degradation effects in algan/gan hemts," *IEEE Transactions on Electron Devices*, vol. 55, no. 7, pp. 1592–1602, 2008.

[23] A. Chini, M. Esposto, G. Meneghesso, and E. Zanoni, "Evaluation of gan hemt degradation by means of pulsed i–v, leakage and dlts measurements," *Electronics letters*, vol. 45, no. 8, pp. 426–427, 2009.

[24] A. Sarua, H. Ji, M. Kuball, M. J. Uren, T. Martin, K. P. Hilton, and R. S. Balmer, "Integrated micro-raman/infrared thermography probe for monitoring of self-heating in algan/gan transistor structures," *IEEE Transactions on Electron Devices*, vol. 53, no. 10, pp. 2438–2447, 2006.

[25] M. Kuball, G. Riedel, J. Pomeroy, A. Sarua, M. Uren, T. Martin, K. Hilton, J. Maclean, and D. Wallis, "Time-resolved temperature measurement of algan/gan electronic devices using micro-raman spectroscopy," *IEEE electron device letters*, vol. 28, no. 2, pp. 86–89, 2007.

[26] M. Faqir, G. Verzellesi, A. Chini, F. Fantini, F. Danesin, G. Meneghesso, E. Zanoni, and C. Dua, "Mechanisms of rf current collapse in algan–gan high electron mobility transistors," *IEEE Transactions on Device and Materials Reliability*, vol. 8, no. 2, pp. 240–247, 2008.

[27] G. Meneghesso, F. Rampazzo, P. Kordos, G. Verzellesi, and E. Zanoni, "Current collapse and high-electric-field reliability of unpassivated gan/algan/gan hemts," *IEEE Transactions on Electron Devices*, vol. 53, no. 12, pp. 2932–2941, 2006.

TH-2691_166102020

[28] G. Verzellesi, R. Pierobon, F. Rampazzo, G. Meneghesso, A. Chini, U. Mishra, C. Canali, and E. Zanoni, "Experimental/numerical investigation on current collapse in algan/gan hemt's," in *Digest. International Electron Devices Meeting,*. IEEE, 2002, pp. 689–692.

[29] G. Bilbro and R. Trew, "Rf knee walkout and source access region of unpassivated hfets," *Electronics Letters*, vol. 42, no. 24, pp. 1425–1426, 2006.

[30] G. Meneghesso, G. Verzellesi, F. Danesin, F. Rampazzo, F. Zanon, A. Tazzoli, M. Meneghini, and E. Zanoni, "Reliability of gan high-electron-mobility transistors: State of the art and perspectives," *IEEE Transactions on Device and Materials Reliability*, vol. 8, no. 2, pp. 332–343, 2008.

[31] J. Joh and J. A. del Alamo, "Mechanisms for electrical degradation of gan high-electron mobility transistors," in *2006 International Electron Devices Meeting*. IEEE, 2006, pp. 1–4.

[32] A. Sarua, H. Ji, M. Kuball, M. J. Uren, T. Martin, K. J. Nash, K. P. Hilton, and R. S. Balmer, "Piezoelectric strain in algan/gan heterostructure field-effect transistors under bias," *Applied physics letters*, vol. 88, no. 10, p. 103502, 2006.

[33] J. Joh and J. A. Del Alamo, "Critical voltage for electrical degradation of gan high-electron mobility transistors," *IEEE Electron Device Letters*, vol. 29, no. 4, pp. 287–289, 2008.

[34] O. Ambacher, "Growth and applications of group iii-nitrides," *Journal of physics D: Applied physics*, vol. 31, no. 20, p. 2653, 1998.

[35] D. Balaz, "Current collapse and device degradation in algan/gan heterostructure field effect transistors," Ph.D. dissertation, University of Glasgow, 2011.

[36] A. Zoroddu, F. Bernardini, P. Ruggerone, and V. Fiorentini, "First-principles prediction of structure, energetics, formation enthalpy, elastic constants, polarization, and piezoelectric constants of aln, gan, and inn: Comparison of local and gradient-corrected density-functional theory," *Physical Review B*, vol. 64, no. 4, p. 045208, 2001.

[37] E. Hellman, "The polarity of gan: a critical review," *Materials Research Society Internet Journal of Nitride Semiconductor Research*, vol. 3, 1998.

[38] R. M. Martin, "Piezoelectricity," *Physical Review B*, vol. 5, no. 4, p. 1607, 1972.

[39] O. Ambacher, B. Foutz, J. Smart, J. Shealy, N. Weimann, K. Chu, M. Murphy, A. Sierakowski, W. Schaff, L. Eastman *et al.*, "Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped algan/gan heterostructures," *Journal of applied physics*, vol. 87, no. 1, pp. 334–344, 2000.

[40] D. Brunner, H. Angerer, E. Bustarret, F. Freudenberg, R. Höpler, R. Dimitrov, O. Ambacher, and M. Stutzmann, "Optical constants of epitaxial algan films and their temperature dependence," *Journal of applied physics*, vol. 82, no. 10, pp. 5090–5096, 1997.

[41] F. Bernardini, "Spontaneous and piezoelectric polarization: Basic theory vs. practical recipes," pp. 49–68, 2007.

[42] J. F. Nye *et al.*, *Physical properties of crystals: their representation by tensors and matrices.* Oxford university press, 1985.

TH-2691_166102020

[43] F. Bernardini and V. Fiorentini, "Nonlinear macroscopic polarization in iii-v nitride alloys," *Physical Review B*, vol. 64, no. 8, p. 085207, 2001.

[44] A. Brannick, N. A. Zakhleniuk, B. K. Ridley, J. R. Shealy, W. J. Schaff, and L. F. Eastman, "Influence of field plate on the transient operation of the algan/gan hemt," *IEEE electron device letters*, vol. 30, no. 5, pp. 436–438, 2009.

[45] E. Yu, G. Sullivan, P. Asbeck, C. Wang, D. Qiao, and S. Lau, "Measurement of piezoelectrically induced charge in gan/algan heterostructure field-effect transistors," *Applied Physics Letters*, vol. 71, no. 19, pp. 2794–2796, 1997.

[46] O. Ambacher, J. Smart, J. Shealy, N. Weimann, K. Chu, M. Murphy, W. Schaff, L. Eastman, R. Dimitrov, L. Wittmer *et al.*, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in n-and ga-face algan/gan heterostructures," *Journal of applied physics*, vol. 85, no. 6, pp. 3222–3233, 1999.

[47] M. T. Hasan, "Mechanism and suppression of current collapse in algan/gan high electron mobility transistors," *Dissertation, University of Fukui*, 2013.

[48] R. Quay, *Gallium nitride electronics.* Springer Science & Business Media, 2008, vol. 96.

[49] T. Sadi, R. W. Kelsall, and N. J. Pilgrim, "Investigation of self-heating effects in submicrometer gan/algan hemts using an electrothermal monte carlo method," *IEEE Transactions on Electron Devices*, vol. 53, no. 12, pp. 2892–2900, 2006.

[50] J. W. Chung, J.-k. Lee, E. L. Piner, and T. Palacios, "Seamless on-wafer integration of si (100) mosfets and gan hemts," *IEEE Electron Device Letters*, vol. 30, no. 10, pp. 1015–1017, 2009.

[51] T. Zimmermann, D. Deen, Y. Cao, J. Simon, P. Fay, D. Jena, and H. G. Xing, "AlN/GaN Insulated–Gate HEMTs With 2.3 A/mm Output Current and 480 mS/mm Transconductance," *IEEE Electron Device Letters*, vol. 29, no. 7, pp. 661–664, July 2008.

[52] R. Gaska, A. Osinsky, J. W. Yang, and M. S. Shur, "Self–heating in high-power AlGaN–GaN HFETs," *IEEE Electron Device Letters*, vol. 19, no. 3, pp. 89–91, March 1998.

[53] A. Aouf, F. Djeffal, and F. Douak, "Thermal stability investigation of power GaN HEMT including self–heating effects," in *Proceedings of IEEE, 6th International Conference on Systems and Control (ICSC)*, May 2017, pp. 451–454.

[54] V. O. Turin and A. A. Balandin, "Electrothermal simulation of the self-heating effects in GaN–based field–effect transistors," *Journal of Applied Physics*, vol. 100, no. 5, p. 054501, 2006.

[55] J. D. Albrecht, R. P. Wang, P. P. Ruden, M. Farahmand, and K. F. Brennan, "Electron transport characteristics of GaN for high temperature device modeling," *Journal of Applied Physics*, vol. 83, no. 9, pp. 4777–4781, 1998.

[56] A. M. Darwish, A. J. Bayba, and H. A. Hung, "Thermal resistance calculation of AlGaN-GaN devices," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, no. 11, pp. 2611–2620, Nov 2004.

[57] J. Pomeroy, M. Uren, B. Lambert, and M. Kuball, "Operating channel temperature in GaN HEMTs: DC versus RF accelerated life testing," *Microelectronics Reliability*, vol. 55, no. 12, pp. 2505 – 2510, 2015.

TH-2691_166102020

[58] X. Chen, F. N. Donmezer, S. Kumar, and S. Graham, “A Numerical Study on Comparing the Active and Passive Cooling of AlGaN/GaN HEMTs,” *IEEE Transactions on Electron Devices*, vol. 61, no. 12, pp. 4056–4061, Dec 2014.

[59] M. Dipalo, M. Alomari, J. F. Carlin, N. Grandjean, M. A. Diforte-Poisson, S. L. Delage, and E. Kohn, “Thick nano–crystalline diamond overgrowth on InAlN/GaN devices for thermal management,” in *Proceedings of IEEE, Device Research Conference*, June 2009, pp. 103–104.

[60] Y. Han, B. L. Lau, X. Zhang, Y. C. Leong, and K. F. Choo, “Enhancement of Hotspot Cooling With Diamond Heat Spreader on Cu Microchannel Heat Sink for GaN–on–Si Device,” *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 4, no. 6, pp. 983–990, June 2014.

[61] Z. Yan, G. Liu, J. M. Khan, and A. A. Balandin, “Graphene quilts for thermal management of high-power GaN transistors,” *Nature Communications*, vol. 3, pp. 827–834, May 2012.

[62] M. A. Khan, M. S. Shur, Q. C. Chen, and J. N. Kuznia, “Current/voltage characteristic collapse in algan/gan heterostructure insulated gate field effect transistors at high drain bias,” *Electronics Letters*, vol. 30, no. 25, pp. 2175–2176, Dec 1994.

[63] C. Roff, P. McGovern, J. Benedikt, P. J. Tasker, R. S. Balmer, D. J. Wallis, K. P. Hilton, J. O. Maclean, D. G. Hayes, M. J. Uren, and T. Martin, “Detailed analysis of dc-rf dispersion in algan/gan hfets using waveform measurements,” in *Proceedings of IEEE, European Microwave Integrated Circuits Conference*, Sept 2006, pp. 43–45.

[64] V. Ramakrishna, “Polarization Induced 2DEG in AlGaN/GaN HEMTs: On the origin, DC and transient characterization,” *University of California Santa Barbara, Santa Barbara*, 2000.

[65] B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy, and L. F. Eastman, “The effect of surface passivation on the microwave characteristics of undoped algan/gan hemts,” *IEEE Electron Device Letters*, vol. 21, no. 6, pp. 268–270, June 2000.

[66] P. Reddy, K. Castelino, and A. Majumdar, “Diffuse mismatch model of thermal boundary conductance using exact phonon dispersion,” *Applied Physics Letters*, vol. 87, no. 21, p. 211908, 2005.

[67] K. Filippov and A. Balandin, “The effect of the thermal boundary resistance on self-heating of algan/gan hfets,” *MRS Internet Journal of Nitride Semiconductor Research*, vol. 8, p. e4, 2003.

[68] Synopsys, *Sentaurus Device User Guide*, 03rd ed., 2016.

[69] K. Horio and H. Yanai, “Numerical modeling of heterojunctions including the thermionic emission mechanism at the heterojunction interface,” *IEEE Transactions on Electron Devices*, vol. 37, no. 4, pp. 1093–1098, April 1990.

[70] N. D. Arora, J. R. Hauser, and D. J. Roulston, “Electron and hole mobilities in silicon as a function of concentration and temperature,” *IEEE Transactions on electron devices*, vol. 29, no. 2, pp. 292–295, 1982.

[71] C. Lombardi, S. Manzini, A. Saporito, and M. Vanzi, “A physically based mobility model for numerical simulation of nonplanar devices,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 7, no. 11, pp. 1164–1171, 1988.

TH-2691_166102020

[72] C. Canali, G. Majni, R. Minder, and G. Ottaviani, "Electron and hole drift velocity measurements in silicon and their empirical relation to electric field and temperature," *IEEE Transactions on electron devices*, vol. 22, no. 11, pp. 1045–1047, 1975.

[73] D. M. Caughey and R. Thomas, "Carrier mobilities in silicon empirically related to doping and field," *Proceedings of the IEEE*, vol. 55, no. 12, pp. 2192–2193, 1967.

[74] A. G. Chynoweth, "Ionization rates for electrons and holes in silicon," *Physical Review*, vol. 109, no. 5, p. 1537–1540, 1958.

[75] R. Van Overstraeten and H. De Man, "Measurement of the ionization rates in diffused silicon pn junctions," *Solid-State Electronics*, vol. 13, no. 5, pp. 583–608, 1970.

[76] B. S. Eller, J. Yang, and R. J. Nemanich, "Electronic surface and dielectric interface states on gan and algan," *Journal of Vacuum Science & Technology A*, vol. 31, no. 5, p. 050807, 2013.

[77] A. Chini, F. Soci, M. Meneghini, G. Meneghesso, and E. Zanoni, "Deep levels characterization in gan hemts; part ii: Experimental and numerical evaluation of self-heating effects on the extraction of traps activation energy," *IEEE Transactions on Electron Devices*, vol. 60, no. 10, pp. 3176–3182, Oct 2013.

[78] O. Mitrofanov and M. Manfra, "Mechanisms of gate lag in gan/algan/gan high electron mobility transistors," *Superlattices and Microstructures*, vol. 34, no. 1, pp. 33 – 53, 2003.

[79] J.-C. Nallatamby, S. Laurent, M. Prigent, J.-C. Jacquet, D. Floriot, and S. Delage, "Comprehensive analysis of gr noise in ingap–gaas hbt by physics-based simulation and low frequency characterization," *Journal of Computational Electronics*, vol. 14, no. 1, pp. 4–14, Mar 2015.

[80] W. Shockley and W. T. Read, "Statistics of the recombinations of holes and electrons," *Phys. Rev.*, vol. 87, pp. 835–842, Sep 1952.

[81] U. K. Mishra, L. Shen, T. E. Kazior, and Y.-F. Wu, "Gan-based rf power devices and amplifiers," *Proceedings of the IEEE*, vol. 96, no. 2, pp. 287–305, 2008.

[82] M. A. Khan, J. Van Hove, J. Kuznia, and D. Olson, "High electron mobility gan/al$_x$ga$_{1-x}$n heterostructures grown by low-pressure metalorganic chemical vapor deposition," *Applied physics letters*, vol. 58, no. 21, pp. 2408–2410, 1991.

[83] M. A. Khan, A. Bhattarai, J. Kuznia, and D. Olson, "High electron mobility transistor based on a gan-al$_x$ga$_{1-x}$n heterojunction," *Applied Physics Letters*, vol. 63, no. 9, pp. 1214–1215, 1993.

[84] S. Vitanov, V. Palankovski, S. Murad, T. Rodle, R. Quay, and S. Selberherr, "Hydrodynamic modeling of algan/gan hemts," in *Simulation of Semiconductor Processes and Devices 2007*. Springer, 2007, pp. 273–276.

[85] Y. Pei, Z. Chen, D. Brown, S. Keller, S. Denbaars, and U. Mishra, "Deep-submicrometer algan/gan hemts with slant field plates," *IEEE electron device letters*, vol. 30, no. 4, pp. 328–330, 2009.

[86] E. R. Heller, R. Vetury, and D. S. Green, "Development of a versatile physics-based finite-element model of an algan/gan hemt capable of accommodating process and epitaxy variations and calibrated using multiple dc parameters," *IEEE Transactions on Electron Devices*, vol. 58, no. 4, pp. 1091–1095, 2011.

TH-2691_166102020

[87] X.-D. Wang, W.-D. Hu, X.-S. Chen, and W. Lu, "The study of self-heating and hot-electron effects for algan/gan double-channel hemts," *IEEE Transactions on Electron Devices*, vol. 59, no. 5, pp. 1393–1401, 2012.

[88] J. A. del Alamo and J. Joh, "Gan hemt reliability," *Microelectronics reliability*, vol. 49, no. 9-11, pp. 1200–1206, 2009.

[89] M. G. Ancona, S. C. Binari, and D. J. Meyer, "Fully coupled thermoelectromechanical analysis of gan high electron mobility transistor degradation," *Journal of Applied Physics*, vol. 111, no. 7, p. 074504, 2012.

[90] M. Tapajna, N. Killat, V. Palankovski, D. Gregusova, K. Cico, J.-F. Carlin, N. Grandjean, M. Kuball, and J. Kuzmik, "Hot-electron-related degradation in inaln/gan high-electron-mobility transistors," *IEEE Transactions on Electron Devices*, vol. 61, no. 8, pp. 2793–2801, 2014.

[91] C. Zhu, M. Wu, C. Kayis, F. Zhang, X. Li, R. Ferreyra, A. Matulionis, V. Avrutin, Ü. Özgür, and H. Morkoc, "Degradation and phase noise of inaln/aln/gan heterojunction field effect transistors: Implications for hot electron/phonon effects," *Applied Physics Letters*, vol. 101, no. 10, p. 103502, 2012.

[92] A. Wang, M. Tadjer, and F. Calle, "Simulation of thermal management in algan/gan hemts with integrated diamond heat spreaders," *Semiconductor science and technology*, vol. 28, no. 5, p. 055010, 2013.

[93] S. Faramehr, K. Kalna, and P. Igić, "Drift-diffusion and hydrodynamic modeling of current collapse in gan hemts for rf power application," *Semiconductor Science and Technology*, vol. 29, no. 2, p. 025007, 2014.

[94] Y. Zhang, K. H. Teo, and T. Palacios, "Beyond thermal management: incorporating p-diamond back-barriers and cap layers into algan/gan hemts," *IEEE Transactions on Electron Devices*, vol. 63, no. 6, pp. 2340–2345, 2016.

[95] S. Zhang, K. Wei, X. Ma, Y. C. Zhang, and T. Lei, "Millimeter-wave algan/gan hemt breakdown voltage enhancement by a recessed float field plate," *Applied Physics Express*, vol. 12, no. 5, p. 054007, 2019.

[96] P. Murugapandiyan, M. T. Hasan, V. Rajya Lakshmi, M. Wasim, J. Ajayan, N. Ramkumar, and D. Nirmal, "Breakdown voltage enhancement of gate field plate $al_{0.295}ga_{0.705}n$/gan hemts," *International Journal of Electronics*, pp. 1–15, 2020.

[97] S. Huang, S. Yang, J. Roberts, and K. J. Chen, "Threshold voltage instability in $al_{2}o_{3}$/gan/algan/gan metal–insulator–semiconductor high-electron mobility transistors," *Japanese journal of applied physics*, vol. 50, no. 11R, p. 110202, 2011.

[98] R. F. Davis, "Iii-v nitrides for electronic and optoelectronic applications," *Proceedings of the IEEE*, vol. 79, no. 5, pp. 702–712, 1991.

[99] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE transactions on Power Electronics*, vol. 29, no. 5, pp. 2155–2163, 2013.

TH-2691_166102020

[100] A. Lidow, M. De Rooij, J. Strydom, D. Reusch, and J. Glaser, *GaN transistors for efficient power conversion.* John Wiley & Sons, 2019.

[101] T. P. Chow and R. Tyagi, "Wide bandgap compound semiconductors for superior high-voltage power devices," in *[1993] Proceedings of the 5th International Symposium on Power Semiconductor Devices and ICs.* IEEE, 1993, pp. 84–88.

[102] J.-G. Lee, B.-R. Park, H.-J. Lee, M. Lee, K.-S. Seo, and H.-Y. Cha, "State-of-the-art algan/gan-on-si heterojunction field effect transistors with dual field plates," *Applied Physics Express*, vol. 5, no. 6, p. 066502, 2012.

[103] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, and I. Omura, "Recessed-gate structure approach toward normally off high-voltage algan/gan hemt for power electronics applications," *IEEE Transactions on electron devices*, vol. 53, no. 2, pp. 356–362, 2006.

[104] K. J. Chen, L. Yuan, M. Wang, H. Chen, S. Huang, Q. Zhou, C. Zhou, B. Li, and J. Wang, "Physics of fluorine plasma ion implantation for gan normally-off hemt technology," in *2011 International Electron Devices Meeting.* IEEE, 2011, pp. 19–4.

[105] T. Mizutani, M. Ito, S. Kishimoto, and F. Nakamura, "Algan/gan hemts with thin ingan cap layer for normally off operation," *IEEE Electron Device Letters*, vol. 28, no. 7, pp. 549–551, 2007.

[106] Z. Tang, Q. Jiang, Y. Lu, S. Huang, S. Yang, X. Tang, and K. J. Chen, "600-v normally off $\sin_x$ / algan / gan mis-hemt with large gate swing and low current collapse," *IEEE Electron Device Letters*, vol. 34, no. 11, pp. 1373–1375, 2013.

[107] G. Dutta, N. DasGupta, and A. DasGupta, "Low-temperature icp-cvd $\sin_x$ as gate dielectric for gan-based mis-hemts," *IEEE Transactions on Electron Devices*, vol. 63, no. 12, pp. 4693–4701, 2016.

[108] Z. Tang, S. Huang, Q. Jiang, S. Liu, C. Liu, and K. J. Chen, "600v 1.3 m$\mu\cdot$ cm^2 low-leakage low-current-collapse algan/gan hemts with aln/sinx passivation," in *2013 25th International Symposium on Power Semiconductor Devices & IC's (ISPSD).* IEEE, 2013, pp. 191–194.

[109] S. L. Selvaraj, T. Suzue, and T. Egawa, "Breakdown enhancement of algan/gan hemts on 4-in silicon by improving the gan quality on thick buffer layers," *IEEE electron device letters*, vol. 30, no. 6, pp. 587–589, 2009.

[110] I. B. Rowena, S. L. Selvaraj, and T. Egawa, "Buffer thickness contribution to suppress vertical leakage current with high breakdown field (2.3 mv/cm) for gan on si," *IEEE Electron Device Letters*, vol. 32, no. 11, pp. 1534–1536, 2011.

[111] S. Iwakami, O. Machida, M. Yanagihara, T. Ehara, N. Kaneko, H. Goto, and A. Iwabuchi, "20 mω, 750 v high-power algan/gan heterostructure field-effect transistors on si substrate," *Japanese journal of applied physics*, vol. 46, no. 6L, p. L587, 2007.

[112] S. Singhal, J. Roberts, P. Rajagopal, T. Li, A. Hanson, R. Therrien, J. Johnson, I. Kizilyalli, and K. Linthicum, "Gan-on-si failure mechanisms and reliability improvements," in *2006 IEEE International Reliability Physics Symposium Proceedings.* IEEE, 2006, pp. 95–98.

TH-2691_166102020

[113] H. Jung, R. Behtash, J. R. Thorpe, K. Riepe, F. Bourgeois, H. Blanck, A. Chuvilin, and U. Kaiser, "Reliability behavior of gan hemts related to au diffusion at the schottky interface," *physica status solidi c*, vol. 6, no. S2 2, pp. S976–S979, 2009.

[114] M. Zhao, X. Wang, X. Liu, J. Huang, Y. Zheng, and K. Wei, "Thermal storage of algan/gan high-electron-mobility transistors," *IEEE transactions on device and materials reliability*, vol. 10, no. 3, pp. 360–365, 2010.

[115] F. Vitobello and A. Barnes, "Long duration high temperature storage test on gan hemts," in *2012 IEEE International Reliability Physics Symposium (IRPS)*. IEEE, 2012, pp. 2C–4.

[116] H. Xing, Y. Dora, A. Chini, S. Heikman, S. Keller, and U. Mishra, "High breakdown voltage algan-gan hemts achieved by multiple field plates," *IEEE Electron Device Letters*, vol. 25, no. 4, pp. 161–163, 2004.

[117] Y.-F. Wu, A. Saxler, M. Moore, R. Smith, S. Sheppard, P. Chavarkar, T. Wisleder, U. Mishra, and P. Parikh, "30-w/mm gan hemts by field plate optimization," *IEEE Electron Device Letters*, vol. 25, no. 3, pp. 117–119, 2004.

[118] Y. Dora, A. Chakraborty, L. Mccarthy, S. Keller, S. DenBaars, and U. Mishra, "High breakdown voltage achieved on algan/gan hemts with integrated slant field plates," *IEEE Electron Device Letters*, vol. 27, no. 9, pp. 713–715, 2006.

[119] J. Wong, K. Shinohara, A. L. Corrion, D. F. Brown, Z. Carlos, A. Williams, Y. Tang, J. F. Robinson, I. Khalaf, H. Fung *et al.*, "Novel asymmetric slant field plate technology for high-speed low-dynamic ron e/d-mode gan hemts," *IEEE Electron Device Letters*, vol. 38, no. 1, pp. 95–98, 2016.

[120] W. Saito, Y. Kakiuchi, T. Nitta, Y. Saito, T. Noda, H. Fujimoto, A. Yoshioka, T. Ohno, and M. Yamaguchi, "Field-plate structure dependence of current collapse phenomena in high-voltage gan-hemts," *IEEE Electron Device Letters*, vol. 31, no. 7, pp. 659–661, 2010.

[121] G. Xie, E. Xu, J. Lee, N. Hashemi, B. Zhang, F. Y. Fu, and W. T. Ng, "Breakdown-voltage-enhancement technique for rf-based algan/gan hemts with a source-connected air-bridge field plate," *IEEE electron device letters*, vol. 33, no. 5, pp. 670–672, 2012.

[122] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, I. Omura, and T. Ogura, "Design and demonstration of high breakdown voltage gan high electron mobility transistor (hemt) using field plate structure for power electronics applications," *Japanese journal of applied physics*, vol. 43, no. 4S, p. 2239, 2004.

[123] Y.-W. Lian, Y.-S. Lin, H.-C. Lu, Y.-C. Huang, and S. S. Hsu, "Drain e-field manipulation in algan/gan hemts by schottky extension technology," *IEEE Transactions on Electron Devices*, vol. 62, no. 2, pp. 519–524, 2015.

[124] W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, I. Omura, and T. Ogura, "Design optimization of high breakdown voltage algan-gan power hemt on an insulating substrate for r_{ON} av_b tradeoff characteristics," *IEEE transactions on electron devices*, vol. 52, no. 1, pp. 106–111, 2004.

[125] B. Liao, Q. Zhou, J. Qin, and H. Wang, "Simulation of algan/gan hemts breakdown voltage enhancement using gate field-plate, source field-plate and drain field plate," *Electronics*, vol. 8, no. 4, p. 406, 2019.

TH-2691_166102020

[126] Y.-W. Lian, Y.-S. Lin, H.-C. Lu, Y.-C. Huang, and S. S. Hsu, "Algan/gan hemts on silicon with hybrid schottky–ohmic drain for high breakdown voltage and low leakage current," *IEEE electron device letters*, vol. 33, no. 7, pp. 973–975, 2012.

[127] S. Karmalkar, J. Deng, and M. S. Shur, "Resurf algan/gan hemt for high voltage power switching," *IEEE Electron Device Letters*, vol. 22, no. 8, pp. 373–375, 2001.

[128] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, I. Omura, T. Ogura, and H. Ohashi, "High breakdown voltage algan-gan power-hemt design and high current density switching behavior," *IEEE Transactions on electron devices*, vol. 50, no. 12, pp. 2528–2531, 2003.

[129] V. Kumar, G. Chen, S. Guo, B. Peres, I. Eliasevich, and I. Adesida, "Field-plated 0.25 μm gate-length algan/gan hemts on 6h-sic with power density of 9.1 w/mm at 18 ghz," *Electronics Letters*, vol. 41, no. 19, pp. 1080–1081, 2005.

[130] M. Tapajna and J. Kuzmik, "A comprehensive analytical model for threshold voltage calculation in gan based metal-oxide-semiconductor high-electron-mobility transistors," *Applied Physics Letters*, vol. 100, no. 11, p. 113509, 2012.

[131] M. Tapajna, M. Jurkovic, L. Valik, S. Hascik, D. Gregusova, F. Brunner, E.-M. Cho, and J. Kuzmik, "Bulk and interface trapping in the gate dielectric of gan based metal-oxide-semiconductor high-electron-mobility transistors," *Applied Physics Letters*, vol. 102, no. 24, p. 243509, 2013.

[132] B. Lu, M. Sun, and T. Palacios, "An etch-stop barrier structure for gan high-electron-mobility transistors," *IEEE electron device letters*, vol. 34, no. 3, pp. 369–371, 2013.

[133] C. Mizue, Y. Hori, M. Miczek, and T. Hashizume, "Capacitance–voltage characteristics of al_2o_3/algan/gan structures and state density distribution at al_2o_3/algan interface," *Japanese Journal of Applied Physics*, vol. 50, no. 2R, p. 021001, 2011.

[134] M. Tapajna and J. Kuzmik, "Control of threshold voltage in gan based metal–oxide–semiconductor high-electron mobility transistors towards the normally-off operation," *Japanese Journal of Applied Physics*, vol. 52, no. 8S, p. 08JN08, 2013.

[135] P. Kordos, R. Stoklas, D. Gregusova, K. Husekova, J. F. Carlin, and N. Grandjean, "Defect states characterization of non-annealed and annealed zro_2/inaln/gan structures by capacitance measurements," *Applied Physics Letters*, vol. 102, no. 6, p. 063502, 2013.

[136] K. Tang, W. Huang, and T. P. Chow, "Gan mos capacitors and fets on plasma-etched gan surfaces," *Journal of electronic materials*, vol. 38, no. 4, pp. 523–528, 2009.

[137] B. Lee, C. Kirkpatrick, X. Yang, S. Jayanti, R. Suri, J. Roberts, and V. Misra, "Normally-off algan/gan-on-si moshfets with tan floating gates and ald sio_2 tunnel dielectrics," in *2010 International Electron Devices Meeting*. IEEE, 2010, pp. 20–6.

[138] K. Civco, D. Greguvsova, J. Kuzmik, M. Jurkovivc, A. Alexewicz, M. A. di Forte Poisson, D. Pogany, G. Strasser, S. Delage, and K. Frohlich, "Influence of processing and annealing steps on electrical properties of inaln/gan high electron mobility transistor with al_2o_3 gate insulation and passivation," *Solid-state electronics*, vol. 67, no. 1, pp. 74–78, 2012.

TH-2691_166102020

[139] S. Yang, Z. Tang, M. Hua, Z. Zhang, J. Wei, Y. Lu, and K. J. Chen, "Investigation of sinx and aln passivation for algan/gan high-electron-mobility transistors: Role of interface traps and polarization charges," *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 358–364, 2020.

[140] A. Bellakhdar, A. Telia, L. Semra, and A. Soltani, "Effect of strain relaxation on the drain conductance in algan/gan hemts," in *2012 International Conference on Engineering and Technology (ICET)*. IEEE, 2012, pp. 1–5.

[141] A. Anwar, R. T. Webster, and K. V. Smith, "Bias induced strain in algan/gan heterojunction field effect transistors and its implications," *Applied physics letters*, vol. 88, no. 20, p. 203510, 2006.

[142] W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura, and M. Yamaguchi, "On-resistance modulation of high voltage gan hemt on sapphire substrate under high applied voltage," *IEEE Electron Device Letters*, vol. 28, no. 8, pp. 676–678, 2007.

[143] J. Joh, F. Gao, T. Palacios, and J. A. Del Alamo, "A model for the critical voltage for electrical degradation of gan high electron mobility transistors," *Microelectronics reliability*, vol. 50, no. 6, pp. 767–773, 2010.

[144] H. Morkoc, *Handbook of nitride semiconductors and devices, Materials Properties, Physics and Growth*. John Wiley & Sons, 2009, vol. 1.

[145] A. Mohanbabu, N. Anbuselvan, N. Mohankumar, D. Godwinraj, and C. Sarkar, "Modeling of sheet carrier density and microwave frequency characteristics in spacer based algan/aln/gan hemt devices," *Solid-state electronics*, vol. 91, pp. 44–52, 2014.

[146] A. Mohanbabu, N. Mohankumar, D. G. Raj, P. Sarkar, and S. K. Saha, "Efficient iii-nitride mis-hemt devices with high-κ gate dielectric for high-power switching boost converter circuits," *Superlattices and Microstructures*, vol. 103, pp. 270–284, 2017.

[147] I. Vurgaftman, J. R. Meyer, and L. R. Ram-Mohan, "Band parameters for iii–v compound semiconductors and their alloys," *Journal of applied physics*, vol. 89, no. 11, pp. 5815–5875, 2001.

[148] A. Ray, S. Bordoloi, B. Sarkar, P. Agarwal, and G. Trivedi, "Numerical simulation of enhanced-reliability filleted-gate algan/gan hemt," *Journal of Electronic Materials*, vol. 49, no. 3, pp. 2018–2031, 2020.

[149] J. Moreke, M. Tapajna, M. J. Uren, Y. Pei, U. K. Mishra, and M. Kuball, "Effects of gate shaping and consequent process changes on algan/gan hemt reliability," *physica status solidi (a)*, vol. 209, no. 12, pp. 2646–2652, 2012.

[150] K. Dannecker and J. Baringhaus, "Fabrication of crystal plane oriented trenches in gallium nitride using sf_6^+ ar dry etching and wet etching post-treatment," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, vol. 38, no. 4, p. 043204, 2020.

[151] X. Chen, "High voltage gan-on-si field-effect transistors for switch- ing applications," Ph.D. dissertation, Department of Electrical Engineering, University of California Los Angeles, 2015.

[152] P. Asbeck, E. Yu, S. Lau, G. Sullivan, J. Van Hove, and J. Redwing, "Piezoelectric charge densities in algan/gan hfets," *Electronics letters*, vol. 33, no. 14, pp. 1230–1231, 1997.

TH-2691_166102020

[153] S. Vitanov, V. Palankovski, S. Maroldt, R. Quay, S. Murad, T. Rodle, and S. Selberherr, "Physics-based modeling of gan hemts," *IEEE transactions on electron devices*, vol. 59, no. 3, pp. 685–693, 2012.

[154] H. Huang, Y. C. Liang, G. S. Samudra, T.-F. Chang, and C.-F. Huang, "Effects of gate field plates on the surface state related current collapse in algan/gan hemts," *IEEE transactions on power electronics*, vol. 29, no. 5, pp. 2164–2173, 2013.

[155] G. Dutta, N. DasGupta, and A. DasGupta, "Effect of sputtered-al_2o_3 layer thickness on the threshold voltage of iii-nitride mis-hemts," *IEEE Transactions on Electron Devices*, vol. 63, no. 4, pp. 1450–1458, 2016.

[156] W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, I. Omura, and T. Ogura, "Influence of surface defect charge at algan-gan-hemt upon schottky gate leakage current and breakdown voltage," *IEEE Transactions on Electron Devices*, vol. 52, no. 2, pp. 159–164, 2005.

[157] N. Zagni, F. Puglisi, P. Pavan, A. Chini, and G. Verzellesi, "Insights into the off-state breakdown mechanisms in power gan hemts," *Microelectronics Reliability*, vol. 100, p. 113374, 2019.

[158] T. Simlinger, H. Brech, T. Grave, and S. Selberherr, "Simulation of submicron double-heterojunction high electron mobility transistors with minimos-nt," *IEEE Transactions on Electron Devices*, vol. 44, no. 5, pp. 700–707, 1997.

[159] G. J. Syaranamual, W. A. Sasangka, R. I. Made, S. Arulkumaran, G. Ng, S. C. Foo, C. L. Gan, and C. V. Thompson, "Role of two-dimensional electron gas (2deg) in algan/gan high electron mobility transistor (hemt) on-state degradation," *Microelectronics Reliability*, vol. 64, pp. 589–593, 2016.

[160] G. Meneghesso, R. Pierobon, F. Rampazzo, G. Tamiazzo, E. Zanoni, J. Bernat, P. Kordos, A. F. Basile, A. Chini, and G. Verzellesi, "Hot-electron-stress degradation in unpassivated gan/algan/gan hemts on sic," in *2005 IEEE International Reliability Physics Symposium, 2005. Proceedings. 43rd Annual.* IEEE, 2005, pp. 415–422.

[161] Y. S. Puzyrev, B. R. Tuttle, R. D. Schrimpf, D. M. Fleetwood, and S. T. Pantelides, "Theory of hot-carrier-induced phenomena in gan high-electron-mobility transistors," *Applied Physics Letters*, vol. 96, no. 5, p. 053505, 2010.

[162] J. Joh and J. A. Del Alamo, "A current-transient methodology for trap analysis for gan high electron mobility transistors," *IEEE Transactions on Electron Devices*, vol. 58, no. 1, pp. 132–140, 2010.

[163] M. Tapajna, S. W. Kaun, M. H. Wong, F. Gao, T. Palacios, U. K. Mishra, J. S. Speck, and M. Kuball, "Influence of threading dislocation density on early degradation in algan/gan high electron mobility transistors," *Applied Physics Letters*, vol. 99, no. 22, p. 223501, 2011.

[164] M. Montes Bajo, C. Hodges, M. J. Uren, and M. Kuball, "On the link between electroluminescence, gate current leakage, and surface defects in algan/gan high electron mobility transistors upon off-state stress," *Applied Physics Letters*, vol. 101, no. 3, p. 033508, 2012.

[165] A. Brannick, N. A. Zakhleniuk, B. K. Ridley, L. F. Eastman, J. R. Shealy, and W. J. Schaff, "Hydrodynamic simulation of surface traps in the algan/gan hemt," *Microelectronics Journal*, vol. 40, no. 3, pp. 410–412, 2009.

TH-2691_166102020

[166] W. Frensley, "Power-limiting breakdown effects in gaas mesfets," *IEEE Transactions on Electron Devices*, vol. 28, no. 8, pp. 962–970, 1981.

[167] R. J. Trew and U. K. Mishra, "Gate breakdown in mesfets and hemts," *IEEE Electron Device Letters*, vol. 12, no. 10, pp. 524–526, 1991.

[168] S. Karmalkar and U. K. Mishra, "Very high voltage algan/gan high electron mobility transistors using a field plate deposited on a stepped insulator," *Solid-State Electronics*, vol. 45, no. 9, pp. 1645–1652, 2001.

[169] S. Razavi, S. T. Pour, and P. Najari, "New gan based hemt with si_3n_4 or un-doped region in the barrier for high power applications," *Superlattices and Microstructures*, vol. 118, pp. 221–229, 2018.

[170] B. Prasannanjaneyulu and S. Karmalkar, "Relative effectiveness of high-k passivation and gate-connected field plate techniques in enhancing gan hemt breakdown," *Microelectronics Reliability*, vol. 110, p. 113698, 2020.

[171] E. Zanoni, M. Meneghini, A. Chini, D. Marcon, and G. Meneghesso, "Algan/gan-based hemts failure physics and reliability: Mechanisms affecting gate edge and schottky junction," *IEEE Transactions on Electron Devices*, vol. 60, no. 10, pp. 3119–3131, 2013.

[172] E. Bahat-Treidel, O. Hilt, F. Brunner, V. Sidorov, J. Wurfl, and G. Trankle, "Algan/gan/algan dh-hemts breakdown voltage enhancement using multiple grating field plates (mgfps)," *IEEE Transactions on Electron Devices*, vol. 57, no. 6, pp. 1208–1216, 2010.

[173] Z. Li, R. Chu, D. Zehnder, S. Khalil, M. Chen, X. Chen, and K. Boutros, "Improvement of the dynamic on-resistance characteristics of gan-on-si power transistors with a sloped field-plate," in *72nd Device Research Conference*, 2014, pp. 257–258.

[174] S. Latrach, E. Frayssinet, N. Defrance, S. Chenot, Y. Cordier, C. Gaquiere, and H. Maaref, "Trap states analysis in algan/aln/gan and inaln/aln/gan high electron mobility transistors," *Current Applied Physics*, vol. 17, no. 12, pp. 1601–1608, 2017.

[175] M. Tapajna, M. Jurkovic, L. Valik, S. Hascik, D. Gregusova, F. Brunner, E. M. Cho, T. Hashizume, and J. Kuzmik, "Impact of gan cap on charges in al_2o_3/(gan/) algan/gan metal-oxide-semiconductor heterostructures analyzed by means of capacitance measurements and simulations," *Journal of Applied Physics*, vol. 116, no. 10, p. 104501, 2014.

[176] Y. Hori, M. Kuzuhara, Y. Ando, and M. Mizuta, "Analysis of electric field distribution in gaas metal-semiconductor field effect transistor with a field-modulating plate," *Journal of Applied Physics*, vol. 87, no. 7, pp. 3483–3487, 2000.

[177] E. A. Jones, F. F. Wang, and D. Costinett, "Review of commercial gan power devices and gan-based converter design challenges," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 707–719, 2016.

[178] G. Meneghesso, M. Meneghini, I. Rossetto, D. Bisi, S. Stoffels, M. Van Hove, S. Decoutere, and E. Zanoni, "Reliability and parasitic issues in gan-based power hemts: A review," *Semiconductor Science and Technology*, vol. 31, no. 9, p. 093004, 2016.

TH-2691_166102020

[179] V. Moroz, H. Y. Wong, M. Choi, N. Braga, R. Mickevicius, Y. Zhang, and T. Palacios, "The impact of defects on gan device behavior: Modeling dislocations, traps, and pits," *ECS Journal of Solid State Science and Technology*, vol. 5, no. 4, pp. 3142–3148, 2016.

[180] S. Vitusevich, S. Danylyuk, N. Klein, M. Petrychuk, A. Y. Avksentyev, V. Sokolov, V. Kochelap, A. Belyaev, V. Tilak, J. Smart *et al.*, "Separation of hot-electron and self-heating effects in two-dimensional algan/gan-based conducting channels," *Applied physics letters*, vol. 82, no. 5, pp. 748–750, 2003.

[181] A. Endoh, I. Watanabe, A. Kasamatsu, and T. Mimura, "Monte carlo simulation of inalas/ingaas hemts with various shape of buried gate," in *2014 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*. IEEE, 2014, pp. 261–264.

[182] M. Meneghini, M. Bertin, G. Dal Santo, A. Stocco, A. Chini, D. Marcon, P. Malinowski, G. Mura, E. Musu, M. Vanzi *et al.*, "A novel degradation mechanism of algan/gan/silicon heterostructures related to the generation of interface traps," in *2012 International Electron Devices Meeting*. IEEE, 2012, pp. 13–3.

[183] F. Bernardini, V. Fiorentini, and D. Vanderbilt, "Spontaneous polarization and piezoelectric constants of iii-v nitrides," *Physical Review B*, vol. 56, no. 16, p. R10024, 1997.

[184] N. Braga, R. Mickevicius, R. Gaska, X. Hu, M. Shur, M. A. Khan, G. Simin, and J. Yang, "Simulation of hot electron and quantum effects in algan/gan heterostructure field effect transistors," *Journal of applied physics*, vol. 95, no. 11, pp. 6409–6413, 2004.

[185] M. Tapajna, U. Mishra, and M. Kuball, "Importance of impurity diffusion for early stage degradation in algan/gan high electron mobility transistors upon electrical stress," *Applied Physics Letters*, vol. 97, no. 2, p. 023503, 2010.

[186] U. Chowdhury, J. L. Jimenez, C. Lee, E. Beam, P. Saunier, T. Balistreri, S.-Y. Park, T. Lee, J. Wang, M. J. Kim *et al.*, "Tem observation of crack-and pit-shaped defects in electrically degraded gan hemts," *IEEE Electron Device Letters*, vol. 29, no. 10, pp. 1098–1100, 2008.

[187] P. Makaram, J. Joh, J. A. del Alamo, T. Palacios, and C. V. Thompson, "Evolution of structural defects associated with electrical degradation in algan/gan high electron mobility transistors," *Applied Physics Letters*, vol. 96, no. 23, p. 233509, 2010.

[188] W. Tan, P. Houston, P. Parbrook, D. Wood, G. Hill, and C. Whitehouse, "Gate leakage effects and breakdown voltage in metalorganic vapor phase epitaxy algan/gan heterostructure field-effect transistors," *Applied physics letters*, vol. 80, no. 17, pp. 3207–3209, 2002.

[189] D. Marcon, T. Kauerauf, F. Medjdoub, J. Das, M. Van Hove, P. Srivastava, K. Cheng, M. Leys, R. Mertens, S. Decoutere, G. Meneghesso, E. Zanoni, and G. Borghs, "A comprehensive reliability investigation of the voltage, temperature and device geometry-dependence of the gate degradation on state-of-the-art gan-on-si hemts," in *2010 International Electron Devices Meeting*, 2010, pp. 20.3.1–20.3.4.

[190] M. Meneghini, I. Rossetto, F. Hurkx, J. Sonsky, J. A. Croon, G. Meneghesso, and E. Zanoni, "Extensive investigation of time-dependent breakdown of gan-hemts submitted to off-state stress," *IEEE Transactions on Electron Devices*, vol. 62, no. 8, pp. 2549–2554, 2015.

TH-2691_166102020

[191] S. Lee, R. Vetury, J. D. Brown, S. R. Gibb, W. Z. Cai, J. Sun, D. S. Green, and J. Shealy, "Reliability assessment of algan/gan hemt technology on sic for 48v applications," in *2008 IEEE International Reliability Physics Symposium.* IEEE, 2008, pp. 446–449.

[192] M. Hikita, M. Yanagihara, K. Nakazawa, H. Ueno, Y. Hirose, T. Ueda, Y. Uemoto, T. Tanaka, D. Ueda, and T. Egawa, "Algan/gan power hfet on silicon substrate with source-via grounding (svg) structure," *IEEE Transactions on Electron Devices*, vol. 52, no. 9, pp. 1963–1968, 2005.

[193] J. Joh, L. Xia, and J. A. del Alamo, "Gate current degradation mechanisms of gan high electron mobility transistors," in *2007 IEEE International Electron Devices Meeting.* IEEE, 2007, pp. 385–388.

[194] J. Joh, J. A. Del Alamo, K. Langworthy, S. Xie, and T. Zheleva, "Role of stress voltage on structural degradation of gan high-electron-mobility transistors," *Microelectronics Reliability*, vol. 51, no. 2, pp. 201–206, 2011.

[195] A. Barnes and F. Vitobello, "Preliminary reliability data from accelerated rf life tests on european gan hemts," in *Proc. CS-MANTECH*, 2012, pp. 87–90.

[196] M. Dammann, M. Baeumler, F. Gutle, M. Casar, H. Walcher, P. Waltereit, W. Bronner, S. Muller, R. Kiefer, R. Quay *et al.*, "Reliability and degradation mechanism of 0.25 μm algan/gan hemts under rf stress conditions," in *2011 IEEE International Integrated Reliability Workshop Final Report.* IEEE, 2011, pp. 42–46.

[197] D. A. Cullen, D. J. Smith, A. Passaseo, V. Tasco, A. Stocco, M. Meneghini, G. Meneghesso, and E. Zanoni, "Electroluminescence and transmission electron microscopy characterization of reverse-biased algan/gan devices," *IEEE Transactions on Device and Materials Reliability*, vol. 13, no. 1, pp. 126–135, 2012.

[198] C.-Y. Chang, E. Douglas, J. Kim, L. Lu, C.-F. Lo, B.-H. Chu, D. Cheney, B. P. Gila, F. Ren, G. Via *et al.*, "Electric-field-driven degradation in off-state step-stressed algan/gan high-electron mobility transistors," *IEEE Transactions on Device and Materials reliability*, vol. 11, no. 1, pp. 187–193, 2011.

[199] S. Mukherjee, Y. Puzyrev, J. Chen, D. M. Fleetwood, R. D. Schrimpf, and S. T. Pantelides, "Hot-carrier degradation in gan hemts due to substitutional iron and its complexes," *IEEE Transactions on Electron Devices*, vol. 63, no. 4, pp. 1486–1494, 2016.

[200] S. Bordoloi, A. Ray, and G. Trivedi, "Introspection into reliability aspects in algan/gan hemts with gate geometry modification," *IEEE Access*, vol. 9, pp. 99 828–99 841, 2021.

[201] M. T. Hasan, T. Asano, H. Tokuda, and M. Kuzuhara, "Current collapse suppression by gate field-plate in algan/gan hemts," *IEEE electron device letters*, vol. 34, no. 11, pp. 1379–1381, 2013.

[202] W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura, and M. Yamaguchi, "Suppression of dynamic on-resistance increase and gate charge measurements in high-voltage gan-hemts with optimized field-plate structure," *IEEE transactions on electron devices*, vol. 54, no. 8, pp. 1825–1830, 2007.

[203] H.-C. Chiu, C.-W. Yang, H.-C. Wang, F.-H. Huang, H.-L. Kao, and F.-T. Chien, "Characteristics of algan/gan hemts with various field-plate and gate-to-drain extensions," *IEEE transactions on electron devices*, vol. 60, no. 11, pp. 3877–3882, 2013.

TH-2691_166102020

[204] Z. Sheng-Lei, W. Yuan, Y. Xiao-Lei, L. Zhi-Yu, W. Chong, Z. Jin-Cheng, M. Xiao-Hua, and H. Yue, "Reverse blocking enhancement of drain field plate in schottky-drain algan/gan high-electron mobility transistors," *Chinese Physics B*, vol. 23, no. 9, p. 097305, 2014.

[205] S. L. Zhao, B. Hou, W. W. Chen, M. H. Mi, J. X. Zheng, J. C. Zhang, X. H. Ma, and Y. Hao, "Analysis of the breakdown characterization method in gan-based hemts," *IEEE Transactions on power electronics*, vol. 31, no. 2, pp. 1517–1527, 2015.

[206] W.-C. Liao, J.-I. Chyi, and Y.-M. Hsin, "Trap-profile extraction using high-voltage capacitance–voltage measurement in algan/gan heterostructure field-effect transistors with field plates," *IEEE Transactions on Electron Devices*, vol. 62, no. 3, pp. 835–839, 2015.

[207] S. Chander, S. Gupta, M. Gupta *et al.*, "Enhancement of breakdown voltage in algan/gan hemt using passivation technique for microwave application," *Superlattices and Microstructures*, vol. 120, pp. 217–222, 2018.

[208] D. Nirmal, L. Arivazhagan, A. A. Fletcher, J. Ajayan, and P. Prajoon, "Current collapse modeling in algan/gan hemt using small signal equivalent circuit for high power application," *Superlattices and Microstructures*, vol. 113, pp. 810–820, 2018.

[209] W. Hu, X. Chen, Z. Quan, C. Xia, W. Lu, and P. Ye, "Self-heating simulation of gan-based metal-oxide-semiconductor high-electron-mobility transistors including hot electron and quantum effects," *Journal of applied physics*, vol. 100, no. 7, p. 074501, 2006.

[210] L. Arivazhagan, D. Nirmal, P. P. K. Reddy, J. Ajayan, D. Godfrey, P. Prajoon, and A. Ray, "A numerical investigation of heat suppression in hemt for power electronics application," *Silicon*, pp. 1–8, 2020.

[211] S. Sze, *Physics of semiconductor devices.* John wiley & sons, 1981.

[212] M. Seelmann-Eggebert, P. Meisen, F. Schaudel, P. Koidl, A. Vescan, and H. Leier, "Heat-spreading diamond films for gan-based high-power transistor devices," *Diamond and Related Materials*, vol. 10, no. 3-7, pp. 744–749, 2001.

[213] J. E. Butler and A. V. Sumant, "The cvd of nanodiamond materials," *Chemical Vapor Deposition*, vol. 14, no. 7-8, pp. 145–160, 2008.

[214] D. J. Meyer, T. I. Feygelson, T. J. Anderson, J. A. Roussos, M. J. Tadjer, B. P. Downey, D. S. Katzer, B. B. Pate, M. G. Ancona, A. D. Koehler *et al.*, "Large-signal rf performance of nanocrystalline diamond coated algan/gan high electron mobility transistors," *IEEE Electron Device Letters*, vol. 35, no. 10, pp. 1013–1015, 2014.

[215] J. Batey and E. Tierney, "Low-temperature deposition of high-quality silicon dioxide by plasma-enhanced chemical vapor deposition," *Journal of Applied Physics*, vol. 60, no. 9, pp. 3136–3145, 1986.

[216] G. Koley, V. Tilak, L. F. Eastman, and M. G. Spencer, "Slow transients observed in algan/gan hfets: effects of sin$_x$ passivation and uv illumination," *IEEE Transactions on Electron Devices*, vol. 50, no. 4, pp. 886–893, 2003.

[217] J. Mittereder, S. Binari, P. Klein, J. Roussos, D. Katzer, D. Storm, D. Koleske, A. Wickenden, and R. Henry, "Current collapse induced in algan/gan high-electron-mobility transistors by bias stress," *Applied Physics Letters*, vol. 83, no. 8, pp. 1650–1652, 2003.

TH-2691_166102020

[218] A. P. Edwards, J. A. Mittereder, S. C. Binari, D. S. Katzer, D. F. Storm, and J. A. Roussos, "Improved reliability of algan-gan hemts using an nh_3 plasma treatment prior to sin passivation," *IEEE electron device letters*, vol. 26, no. 4, pp. 225–227, 2005.

[219] P. Valizadeh and D. Pavlidis, "Effects of rf and dc stress on algan/gan modfets: A low-frequency noise-based investigation," *IEEE Transactions on Device and Materials Reliability*, vol. 5, no. 3, pp. 555–563, 2005.

[220] R. Coffie, Y. Chen, I. Smorchkova, B. Heying, V. Gambin, W. Sutton, Y.-C. Chou, W.-B. Luo, M. Wojtowicz, and A. Oki, "Temperature and voltage dependent rf degradation study in algan/gan hemts," in *2007 IEEE International Reliability Physics Symposium Proceedings. 45th Annual*. IEEE, 2007, pp. 568–569.

[221] J. Kuzmik, S. Vitanov, C. Dua, J.-F. Carlin, C. Ostermaier, A. Alexewicz, G. Strasser, D. Pogany, E. Gornik, N. Grandjean *et al.*, "Buffer-related degradation aspects of single and double-heterostructure quantum well inaln/gan high-electron-mobility transistors," *Japanese Journal of Applied Physics*, vol. 51, no. 5R, p. 054102, 2012.

[222] N. Shigekawa, K. Shiojima, and T. Suemitsu, "Optical study of high-biased algan/gan high-electron-mobility transistors," *Journal of applied physics*, vol. 92, no. 1, pp. 531–535, 2002.

[223] N. Killat, M. Uren, D. Wallis, T. Martin, and M. Kuball, "Origin of kink effect in algan/gan high electron mobility transistors: Yellow luminescence and fe doping," *Applied Physics Letters*, vol. 101, no. 15, p. 153505, 2012.

[224] S. Vitanov, V. Palankovski, S. Maroldt, and R. Quay, "High-temperature modeling of algan/gan hemts," *Solid-State Electronics*, vol. 54, no. 10, pp. 1105–1112, 2010.

[225] T. Grasser, T.-W. Tang, H. Kosina, and S. Selberherr, "A review of hydrodynamic and energy-transport models for semiconductor device simulation," *Proceedings of the IEEE*, vol. 91, no. 2, pp. 251–274, 2003.

[226] M. Tapajna, K. Cico, J. Kuzmik, D. Pogany, G. Pozzovivo, G. Strasser, J. Carlin, N. Grandjean, and K. Frohlich, "Thermally induced voltage shift in capacitance–voltage characteristics and its relation to oxide/semiconductor interface states in ni/al2o3/inaln/gan heterostructures," *Semiconductor science and technology*, vol. 24, no. 3, p. 035008, 2009.

[227] F. Gutle, V. Polyakov, M. Baeumler, F. Benkhelifa, S. Muller, M. Dammann, M. Casar, R. Quay, M. Mikulla, J. Wagner *et al.*, "Radiative inter-valley transitions as a dominant emission mechanism in algan/gan high electron mobility transistors," *Semiconductor Science and Technology*, vol. 27, no. 12, p. 125003, 2012.

[228] S. Mukherjee, Y. Puzyrev, J. Hinckley, R. D. Schrimpf, D. M. Fleetwood, J. Singh, and S. T. Pantelides, "Role of bias conditions in the hot carrier degradation of algan/gan high electron mobility transistors," *physica status solidi c*, vol. 10, no. 5, pp. 794–798, 2013.

[229] E. Zanoni, G. Meneghesso, G. Verzellesi, F. Danesin, M. Meneghini, F. Rampazzo, A. Tazzoli, and F. Zanon, "A review of failure modes and mechanisms of gan-based hemts," in *2007 IEEE International Electron Devices Meeting*. IEEE, 2007, pp. 381–384.

[230] M. Meneghini, A. Stocco, N. Ronchi, F. Rossi, G. Salviati, G. Meneghesso, and E. Zanoni, "Extensive analysis of the luminescence properties of algan/gan high electron mobility transistors," *Applied Physics Letters*, vol. 97, no. 6, p. 063508, 2010.

TH-2691_166102020

[231] M. Tapajna, R. J. Simms, Y. Pei, U. K. Mishra, and M. Kuball, "Integrated optical and electrical analysis: Identifying location and properties of traps in algan/gan hemts during electrical stress," *IEEE Electron Device Letters*, vol. 31, no. 7, pp. 662–664, 2010.

[232] P. Klein, S. Binari, K. Ikossi, A. Wickenden, D. Koleske, and R. Henry, "Effect of deep traps on sheet charge in algan/gan high electron mobility transistors," *Electronics Letters*, vol. 37, no. 25, pp. 1550–1551, 2001.

[233] M. J. Uren, S. Karboyan, I. Chatterjee, A. Pooth, P. Moens, A. Banerjee, and M. Kuball, ""leaky dielectric" model for the suppression of dynamic ron in carbon-doped algan/gan hemts," *IEEE Transactions on Electron Devices*, vol. 64, no. 7, pp. 2826–2834, 2017.

[234] J. Holman, "Heat transfer tenth edition," 2010.

[235] J. Due and A. J. Robinson, "Reliability of thermal interface materials: A review," *Applied Thermal Engineering*, vol. 50, no. 1, pp. 455–463, 2013.

[236] R. Coffie, "Analytical field plate model for field effect transistors," *IEEE Transactions on Electron Devices*, vol. 61, no. 3, pp. 878–883, 2014.

[237] W. Smythe, "chap. iv," *Static and dynamic electricity*, 1968.

[238] E. Weber, *Electromagnetic Field Theory and Applications.* Wiley, USA, 1950.

[239] H. Kober, *Dictionary of conformal representations.* Dover New York, 1957, vol. 2.

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List of Publications

Journal Publications

1. **S. Bordoloi**, A. Ray and G. Trivedi, *"Introspection into Reliability Aspects in AlGaN/GaN HEMTs with Gate Geometry Modification"*, **IEEE Access**, 2021,Vol. 9, pp. 99828-99841, doi: 10.1109/ACCESS.2021.3096988.

2. **S. Bordoloi**, A. Ray and G. Trivedi, *"Access Region Stack Engineering for Mitigation of Degradation in AlGaN/GaN HEMTs with Field Plate"*, **IEEE Transactions on Device and Materials Reliability**, Vol. 22, no. 1, pp. 73-84, March 2022, doi: 10.1109/TDMR.2022.3150714.

Book Chapter

1. **S. Bordoloi**, A. Ray, and G. Trivedi, *"Simulation Framework for GaN Devices with Special Mention to Reliability Concern"*, **VLSI and Post-CMOS Electronics. Volume 2: Devices, circuits and interconnects**, 2019, Chap. 4, pp. 63–83, Institution of Engineering and Technology, doi: 10.1049/PBCS073G_ch4.

Conference

1. **S. Bordoloi**, A. Ray and G. Trivedi, *"Numerical analysis of the Impact of Gate Geometry variations on the Reliability of AlGaN/GaN HEMT"*, **IEEE Industry Application Society sponsored 4th International Conference on Computing, Power and Communication Technologies (GUCON), 24 - 26 Sep, 2021, Kuala Lumpur, Malaysia**, pp. 1-5, doi: 10.1109/GUCON50781.2021.9573607.

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Other Publications

1. A. Ray, **S. Bordoloi**, B. Sarkar, P. Agarwal and G. Trivedi, *"Numerical Simulation of Enhanced-Reliability Filleted-Gate AlGaN/GaN HEMT"*, **Journal of Electronics Material**, 2020, 49, (3), pp. 2018-2031.

2. A. Ray, **S. Bordoloi**, P. Agarwal and G.Trivedi, *"Investigation of electrical aspect in lateral and vertical SiC Diodes"*, **XXth International Workshop on the Physics of Semiconductor Devices (IWPSD 2019)**, 17-20 December 2019, Kolkata.

3. K. Bharadwaj, A. Ray, **S. Bordoloi** and Gaurav Trivedi, *"Current Collapse reduction technique using N-doped buffer layer into the bulk region of a Gate Injection Transistor"*, **32nd International Conference on VLSI Design (VLSID)**, 5-9 January 2019, New Delhi, pp. 494-495, IEEE.

4. A. Ray, G. Kumar, **S. Bordoloi**, D. K. Sinha, P. Agarwal, and G. Trivedi, *"FEM based Device Simulator for High Voltage Devices"*, **21st International Symposium on VLSI Design and Test (VDAT 2017)**, IIT Roorkee, pp. 127-135.

5. M. Singh, G. Kumar, **S. Bordoloi** and G. Trivedi, *"A study on modeling and simulation of Multiple-Gate MOSFETs"*, **Journal of Physics: Conference Series**, 2016, 759, pp. 012093.

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